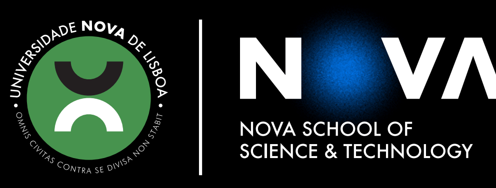

DEPARTAMENT OF
MATERIALS SCIENCE

OPTOELECTRONIC MEMRISTIVE DEVICES BASED ON OXIDE SEMICONDUCTORS FOR THE NEXT GENERATION OF INFORMATION TECHNOLOGY

MARIA ELIAS PEREIRA

Master in Micro and Nanotechnology Engineering

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MARIA ELIAS PEREIRA

Master in Micro and Nanotechnology Engineering

Adviser: Asal Kiazadeh
Principal Researcher, NOVA School of Science and Technology, NOVA University Lisbon

Co-advisers: Pedro Miguel Cândido Barquinha
Associate Professor, NOVA School of Science and Technology, NOVA University Lisbon

Pydi Ganga Mamba Bahubalindruni
Associate Professor, Indian Institute of Science Education and Research Bhopal

Examination Committee:

Chair: José Paulo Moreira dos Santos,
Full Professor, NOVA School of Science and Technology, NOVA University Lisbon

Rapporteurs: Carlo Ricciardi,
Full Professor, University of Politecnico di Torino

Valeria Bragaglia,
Researcer, IBM Research, Switzerland

Adviser: Asal Kiazadeh
Principal Researcher, NOVA School of Science and Technology, NOVA University Lisbon

Members: Konstantinos Rogdakis,
Assistant Professor, Hellenic Mediterranean University

Sérgio de Almeida Matos,
Associate Professor with Habilitation, ISCTE- University Institute of Lisbon

Elvira Maria Correia Fortunato,
Full Professor, NOVA School of Science and Technology, NOVA University Lisbon

DOCTORATE IN IN NANOTECHNOLOGIES AND NANOSCIENCES

NOVA University Lisbon
July, 2024

Optoelectronic memristive devices based on oxide semiconductors for the next generation of information technology

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Step by step, task by task, sacrifice by sacrifice, to turn a wish into a goal and that goal into reality: This is how dreams come true.

- Vasco Pontes -

The only person you are destined to become, is the person you decide to be.

Miss or Mrs.?

Dr. please.

- Ralph Waldo Emerson / Unknown -

ACKNOWLEDGMENTS

First things first, I would like to thank my advisers: Dr. Asal Kiazadeh, Professor Pedro Barquinha and Professor Ganga Bahubalindruni.

To Dr. Asal Kiazadeh, my main adviser, thank you for ALL your support throughout these years. Thank you for allowing me to grow both professionally and personally under your guidance. Thank you for the thousand meetings we had, for the thousand advice, and for being more than just an adviser, but also a career manager and a Friend. I believe this has made all the difference in the success of this work. I could not have hoped for more as you gave me everything. Thank you.

To Professor Pedro Barquinha, with whom I started my research journey six years ago in my master's thesis, I thank you for taking a chance on me then, and for continuing to take a chance on me now. With no doubt, your mentorship has shaped my research skills and academic path. I deeply appreciate your unwavering support, feedback, and the opportunities you have provided that have significantly contributed to the success of this PhD thesis and to my development as a researcher and as a person. I am profoundly grateful.

I have to thank also my non-official advisers. Firstly, to Dr. Jonas Deuermeier for teaching me all I know of the XPS technique, for promptly performing it on my thousand samples, and for all your input in this work throughout the years. To Professor Joana Vaz Pinto, for giving me the opportunity to assist her in Microelectronics I practical classes, which has not only been fun, it has enhanced my CV and has allowed me to meet so many wonderful students that call me Professora… (what? Me?). And finally, to my coco-adviser- Dr. Emanuel Carlos. Yes, coco is a fruit and this is an inside joke. Thank you for being my mentor and my role model in this journey. It has made it easier to be, not only always understood, but also advised and guided by someone who has been through the same not so long ago and with such an excellent performance.

I would like to express my gratitude to Professor Rodrigo Martins and Professor Elvira Fortunato for creating our outstanding center, Cenimat/Cemop, and for putting Portugal not only on the map but at the forefront of research in semiconductor technology.

I would also like to thank Professor Regina Dittmann and her amazing team for the warm welcome during my stay at Forschungszentrum Jülich. It was a truly great experience that advanced my

research and paved the way for a deeper understanding on the physics of my devices. I am very thankful for the opportunity, as well as for the time Professor Regina has dedicated to my work in the many meetings that followed my stay.

I gratefully acknowledge Fundação para a Ciência e Tecnologia (FCT) for funding my research over the past four years, under the grand DFA/BD/8335/2020. I am proud to say I was a recipient of the FCT PhD scholarship, supported by Portuguese national funds. I am also thankful for all the projects that have financed my work from FEDER funds through the COMPETE 2020 program and National Funds through the FCT with references UIDB/50025/2020-2023, LA/P/0037/2020, UIDP/50025/2020 and the projects OPERA, reference 2022.08132.PTDC and NeurOxide, reference PTDC/NAN-MAT/30812/2017, of the Associate Laboratory Institute of Nanostructures, Nanomodelling and Nanofabrication—i3N. This work also received funding from the European Community's H2020 program under Grant Agreements 716510 (ERC-2016-StG TREND), 787410 (ERC-2019-AdG DIGISMART), 952169 (SYNERGY, H2020-WIDESPREAD-2020-5, CSA) and 101008701 (EMERGE, H2020-INFRAIA-2020-1). Under the HORIZON-EIC-2023-PATHFINDERCHALLENGES-01 program, this work was also financed from ELEGANCE project reference 101161114. Additionally, TERRAMETA project has also funded this work, receiving support from the Smart Networks and Services Joint Undertaking (SNS JU) under the European Union's Horizon Europe research and innovation program under Grant Agreement No 101097101.

I extend my heartfelt appreciation to all the individuals at Cenimat and Cemop who have contributed to making it a place of excellence. Each and every one of you has had a significant impact on my journey, whether directly or indirectly. Therefore, my appreciation extends to ALL of you. In particular, I would like to express my sincere appreciation to Ana Santa. Firstly, for teaching me the basis about Clean-room techniques all those years ago, which has been invaluable to this work. Secondly, for your assistance over the past months in covering my responsibilities in the Clean-room, allowing me to focus on completing my PhD thesis. Another special thanks to Cátia Figueiredo, my dearest friend, and once Clean-room colleague. You have made everything lighter to me. Thank you for making me laugh so hard and for reminding me I used to be fun. And finally, another special acknowledge to the ones accompanying me in this crazy journey we all chose - Sara Silvestre and Tomás Pinheiro. We have been together from the start, and I believe we have made each other stronger and better by supporting and applauding each other. I thank you for all the genuine conversations full of outbursts, never having to think twice if we could trust or rely on each other. We were always on each other's corners and I believe that is the best example we can leave to younger students just starting their PhDs. Plus, our office was the best office.

On a more personal note, I thank my father, Víctor, who, not being a scientist, has never left a word I have written unread. Thank you for being my biggest supporter, critic and adviser in this journey. Thank you for trying so hard to learn incredibly complex concepts just to discuss the topic with

me so I would never feel alone. Mainly, thank you for being the best father any woman could ever hope to have. I share with you this accomplishment and would like to make it as much yours as mine.

I thank my mother, Fátima, who has never read a word I wrote, and yet has supported me through it all as well. Thank you for worrying if I have slept or eaten. Thank you for providing the equilibrium often necessary so I would not obsess and get lost in it. Thanks for calling just to ask if I am ok. Thanks also to my brother, Miguel, my Christmas gift from 21 years ago, for the support, for believing in me, and for being this unbelievably happy kid that can make my day when it has not been that great. Queria agradecer também aos meus avós, Avó Mila e Avô Joaquim. Um dos meus sonhos era tornar-me "*Senhora Doutora*" convosco a ver. Espero que se consigam orgulhar do meu percurso e da minha pessoa. Ambos tornaram tudo isto possível e estar-vos-ei eternamente grata por isso. I would also like to thank my best friend Cláudia. Thank you for always agreeing with me, even when I am wrong. You are going through the same which makes it easier for us to understand each other. However, I'm thankful for that understanding anyway, because it was so important… not to feel crazy or overwhelmed. It would have been 1000 times harder without you. Who knew, 11 years ago, this would be us?

Finally, I have to thank my core family now. To my "*pequeno*" Pedro, who is now a GIANT. Thank you for all the patience and support in these hard years. Thank you for being my personal team, for all the dinners and lunches, for all the laughs, for all the care. And thank you for all the scientific discussions as well, for allowing me to incessantly talk about memristors and transistors and for your own contributions to my work. Most of all, thank you for waiting.

And, of course, thanks to my "lila baby" Mel. She has made me company through all the sleepless nights and the long days at the computer. Never complained about the many absences either and always threw a huge party when I arrived home. And, in fact, knowing this PhD might allow me to buy her more toys was a big motivation to finish it.

ABSTRACT

Neuromorphic computing is based on the development of device concepts which arise from biological neural systems. Memristors can behave as artificial synapses and are, therefore, promising candidates towards power-efficient systems for neuromorphic computing with high-density information, in-memory computation and parallel data processing. However, the requirements for a linear and symmetric synaptic weight update and low cycle-to-cycle (C2C) and device-to-device (D2D) variabilities as well as the sneak-path current issue have been delaying its further development. Once these challenges are overcome, artificial neural networks (ANNs) could be built in hardware using crossbars for pattern recognition applications. Moreover, in ANNs, optoelectronic memristors (OEMs) can act as an artificial retina and combine optical sensing and high-level image processing. In OEMs, resistive switching (RS) can be controlled by both optical and electronic signals. Light can, therefore, be used as image input or as synaptic weigh modulator which provides a high-speed non-destructive method.

In this dissertation, the development of an optoelectronic memristive system based on oxide-semiconductors for image sensing, as well as the supporting read-out electronics for pattern recognition is presented. Firstly, an Indium-Gallium-Zinc Oxide (IGZO)-based memristor is developed, compatible with the IGZO-based thin-film transistor (TFT), providing the means for cost-efficient and fast chip fabrication. The crosstalk challenge is solved by using TFTs as access devices to memristors and a 4 x 4 IGZO 1-transistor-1-memristor (1T1M) crossbar is successfully reported on a flexible polyimide substrate. Other state-of-art challenges are also tackled such as D2D and C2C variability and linear and symmetric plasticity characteristics is achieved, resulting in 93.2 % of pattern recognition accuracy in simulations. Moreover, the physical mechanism of interface-RS behavior is extensively studied and data retention is optimized by introducing a thin layer of Al_2O_3. Finally, the optoelectronic features of IGZO memristors are explored for visible light detection envisioning an upcoming integration in a photoperceptron hardware composed of OEMs and 1T1M crossbars in a prototype for neuromorphic vision sensors.

Keywords: Memristors, IGZO, Artificial neural network, Crosstalk, 1T1M, Interface resistive switching, Area-dependent resistive switching, Optoelectronic memristor.

RESUMO

A computação neuromórfica baseia-se no desenvolvimento de dispositivos cujo conceito advém de sistemas neuronais biológicos. Os memristors podem comportar-se como sinapses artificiais e são, portanto, excelentes candidatos para a conceção de sistemas energeticamente eficientes para computação neuromórfica com elevada densidade de informação, computação *in-memory* e processamento de informação paralelo. Contudo, problemáticas como a atualização linear e simétrica de peso sináptico, variabilidade tanto entre ciclos (C2C) como entre dispositivos (D2D), e o problema de *sneak-path* têm-se apresentado como barreiras ao desenvolvimento deste tipo de dispositivos. A resolução destas problemáticas torna possível a construção de redes neuronais artificiais em *hardware*, utilizando *crossbars* para aplicações de reconhecimento de padrões. Além disto, em redes neuronais artificiais, memristors optoeletrónicos poderão atuar como uma retina artificial e combinar deteção ótica e processamento de imagem de alto nível. O *switching* resistivo (RS) de memristors optoeletrónicos pode ser controlado tanto por sinais óticos como por sinais eletrónicos. Assim, a luz pode ser usada como imagem de *input* ou como modulador de peso sináptico, o que confere um método de alta velocidade não destrutivo.

Nesta dissertação, é apresentado o desenvolvimento de um sistema memristivo optoeletrónico com base em óxidos semicondutores para deteção de imagem e o respetivo sistema eletrónico de leitura para reconhecimento de padrões. Primeiro, é desenvolvido um memristor de óxido de Índio-Gálio-Zinco (IGZO) compatível com o transístor de filme fino (TFT) de IGZO, potenciando a fabricação de chips rápida e económica. O *crosstalk* é resolvido com a utilização de TFTs como dispositivos de acesso aos memristors e é reportada com sucesso uma *crossbar* 1T1M de 4 x 4 células num substrato flexível de poli-imida. É atingida uma característica de plasticidade linear e simétrica, resultando numa precisão de reconhecimento de padrão de 93.2% em simulação. Para além disto, o mecanismo físico do comportamento de RS interfacial é estudado extensivamente e a retenção de informação é otimizada pela introdução de uma camada extremamente fina de Al_2O_3. Por último, as propriedades optoeletrónicas de memristors de IGZO são exploradas para deteção de luz visível, com vista na integração de um *photoperceptron hardware* composto por memristors optoeletrónicos e *crossbars* 1T1M num protótipo de um sensor visual neuromórfico.

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ABBREVIATIONS

1D1M	1-Diode-1-Memristor.
1M	1-Memristor.
1T1M	1-Transistor-1-Memristor.
AI	Artificial Intelligence.
ALD	Atomic Layer Deposition.
AlO	Aluminum Oxide.
ANNs	Artificial Neural Networks.
AOS	Amorphous Oxide Semiconductors.
APS	Active Pixel Sensor.
AZO	Aluminum-doped Zinc Oxide.
AZTO	Aluminum-doped Zinc-Tin Oxide.
BP	Black Phosphorous.
BL	Bit Line.
C2C	Cycle-to-Cycle.
CC	Current Compliance.
CCD	Charged-Coupled Device.
CFs	Conductive Filaments.
CMOS	Complementary Metal–Oxide–Semiconductor.
CTA	Conventional Thermal Annealing.
CVD	Chemical Vapor Deposition.

D2D	Device-to-Device.
DNNs	Deep Neural Networks.
DAC	Digital-to-Analog Converter.
DRAM	Dynamic Random Access Memory.
eCDF	experimental Cumulative Distribution Function.
ECM	Electrochemical Mechanism.
EDS	Energy Dispersive Spectroscopy.
EFA	Electric-field Assisted.
FTO	Fluorine-doped Tin Oxide.
GaO	Gallium Oxide.
GTO	Gallium-Tin Oxide.
GZO	Gallium-Zinc Oxide.
HAADF	High Angle Annular Dark Field.
H-doped	Hydrogen doped.
HfO	Hafnium Oxide.
HRS	High Resistance State.
HO	High Oxygen.
ICP-MS	Inductively Coupled Plasma Mass Spectrometry.
IGZO	Indium-Gallium-Zinc Oxide.
IoT	Internet-of-Things.
IPA	Isopropanol.
IR	Infrared.
ITO	Indium-Tin Oxide.
IZO	Indium-Zinc-Oxide.
LEDs	Light Emitting Diodes.
LEMs	Light Emitting Memristors.
LO	Low Oxygen.

LRS	Low Resistance State.
LSPR	Localized Surface Plasmon Resonance.
LTM	Long-Term Memory.
LTP	Long-Term Plasticity.
MLC	Multi-Level Cell.
MnO	Manganese Oxide.
MoO	Molybdenum Oxide.
MoW	Molybdenum Tungsten.
VLC	Visible Light Communication.
VMMs	Vector-Matrix Multiplications.
MRS	Medium Resistance State.
MoO_x	Molybdenum Oxide.
MWI	Microwave Irradiation.
NIR	Near-Infrared.
NPs	NanoParticles.
NRi	NanoRibbon.
NRs	NanoRods.
NW	NanoWire.
OEMs	Optoelectronic Memristors.
OPS	One Operation (multiply or add) per Second.
PbS	Lead Sulfide.
PEN	Polyethylene naphthalate (poly(Ethylene 2,6-Naphthalate).
PET	PolyEthylene Terephthalate.
PLD	Pulsed Laser Deposition.
PMMA	PolyMethyl MethAcrylate.
PPC	Persistent Photoconductivity.
PPD	Paired-Pulse Depression.

PPF	Paired-Pulse Facilitation.
PSC	Post-synaptic Current.
PVA	PolyVinyl Alcohol.
QDs	Quantum Dots.
RF	Radio-Frequency.
RGB	Red-Green-Blue.
RS	Resistive Switching.
SEF	Stretched-Exponential Function.
SL	Source Line.
SN	Shared Node.
SNNs	Spiking Neural Networks.
SnO	Tin Oxide.
SoP	System-on-Panel.
SRAM	Static Random Access Memory.
STEM	Scanning Transmission Electron Microscopy.
STDP	Spike-Time Dependent Plasticity.
STM	Short-Term Memory.
STP	Short-Term Plasticity.
TaO	Tantalum Oxide.
TCO	Transparent Conductive Oxide.
TFT	Thin-Film Transistor.
TiN	Titanium Nitride.
TiO	Titanium Oxide.
TiON	Titanium Oxynitride.
TiW	Titanium Tungsten.
TMO	Transition Metal Oxide.
UV	Ultraviolet.

VBM	Valence Band Maxima.
VBS	Voltage Bias Scheme.
VCM	Valence Change Memory.
VMMs	Vector-Matrix Multiplications.
VO	Oxygen Vacancy.
VLSI	Very-Large-Scale Integration.
WIZO	Tungsten-doped Indium-Zinc Oxide.
WL	Word Line.
XPS	X-ray Photoelectron Spectroscopy.
ZnO	Zinc Oxide.
ZP	Phosphorene.
ZrO	Zirconium Oxide.
ZTO	Zinc-Tin Oxide.

SYMBOLS

$\mathbf{I_{LRS}}$	Measured current at the low-resistance state for a fixed applied voltage.
$\mathbf{I_{HRS}}$	Measured current at the high-resistance state for a fixed applied voltage.
I_0	Initial current state.
I-V	Current-voltage characteristic.
$\mathbf{V_{Set}}$	Required voltage for full Set.
$\mathbf{V_{Reset}}$	Required voltage for full Reset.
ΔW	Synaptic weight change.
Δt	Time interval between two spikes.
$\mathbf{I_{gate}}$	Leakage current at the gate electrode of the TFT.
$\mathbf{V_{ON}}$	Turn-on voltage of the TFT.
$\mathbf{V_{drain}}$	Voltage applied to the drain electrode of the TFT.
ΔG	Conductance change.
Δt	Time intervale.
G	Conductance.
$\mathbf{G_{LRS}}$	Conductance in low-resistance state.
$\mathbf{G_{HRS}}$	Conductance in high-resistance state.
W	Internal variable of synaptic weight which varies from 0 to 1.
α_p	Non-linearity parameter in potentiation.
α_d	Non-linearity parameter in depression.

$\mathbf{V_{WL}}$	Voltage applied to the word line.
$\mathbf{W_{SL}}$	Voltage applied to the source line.
$\mathbf{V_{BL}}$	Voltage applied to the bit line.
$\mathbf{E_c}$	Energy consumption.
W	Synaptic weigh.
$\varphi(t)$	Relaxation function.
τ	Characteristic relaxation time.
β	Stretch index.
η	Ideality factor.
T	Absolute temperature.
K_B	Boltzmann constant,
A*	Effective Richardson constant.
Φ_{SBH}	Schottky barrier height.
A	Area of the device.
R_p	Parallel resistance.
R_s	Series resistance.
I_c	Parallel capacitance current.
σ_{RN}	Normalized low-frequency Read Noise.
j	Current density.
E_f	Fermi level.
E_c	Conduction band minimum.
E_g	Band gap energy.
E_k	Kinetic energy.
E_v	Valence band maximum.

CHAPTER 1

INTRODUCTION

This chapter presents an introduction to this dissertation. Firstly, the motivation behind the work is revised and the primary goals are explained in detail in regard to their scientific relevance to the research community. Afterwards, the structure of the document is discussed in terms of chapter content. Finally, the research impact that the work has had is reviewed in terms of published material in international journals, oral and poster presentations in international and national conferences and meetings and granted awards.

1.1 Motivation

The urgency to replace the traditional Von Neumann architecture is growing due to the persistent bottleneck in data transfer between the processor and memory unit, impeding the realization of complex computational tasks with high speed and accuracy. Particularly in data-centric applications like artificial intelligence (AI), innovative computational paradigms are crucial to reduce power consumption. Neuromorphic computing based on memristors is a brain-inspired technology that offers a promising ultra-low power consumption alternative. By performing the processing of the data directly at the memory element, it eliminates data shuffling, enabling cost and power-efficient real-time in-memory computation.

Memristors, also known as resistive switching (RS) devices, which are nonlinear resistors typically composed of metal-oxide-metal structures, exhibit tunable resistance into multiple states by application of an external electric field. The transition from the highest-resistance state (HRS) to the lowest-resistance state (LRS) is known as Set operation, and from LRS to HRS, as Reset operation. The retention of these programmed states is influenced by both the material structure of the device and the type of switching observed. RS mechanisms can involve either the creation/dissolution of one or more conductive filaments (CFs), called filamentary-type switching, or the contributions of oxygen ions or cations at one of the device interfaces or at the oxide bulk, called area-dependent switching. Filamentary-type switching typically ensures long retention of states, whereas area-dependent switching tends to suffer from a relaxation decay of the programmed states in time. Both characteristics can be leveraged for different applications. Moreover, multi-level cell (MLC) operations, which are possible when the memristor presents more than two trainable states and is achievable through filamentary and area-dependent switching, are required for in-memory computation tasks in artificial neural networks (ANNs). In ANNs composed by memristors organized in crossbars, synaptic behavior is mimicked through gradual resistance state adjustments with electric pulses. In fact, several synaptic characteristics have already been emulated by RS devices,[1,2] showcasing significant potential to revolutionize the AI field.

The employment of ANNs in hardware involves two key stages: training and inference. During training, the resistance state of the memristors in the crossbar is independently and continuously adapted via a predefined pulsing scheme, in a process known as learning. This process enables the memristor-based neural network to learn from labeled or unlabeled input data, applied as voltage/current vector at the rows connected to the electrodes of the memristors. After learning, the output can be read at the columns, as the result of Ohm's and Kirchhoff 's summation laws, as the neural network performs vector-matrix multiplications (VMMs). This process is called inference in which the ANN solely executes its designated task.

Moreover, the training process in an ANN hardware can be performed online or offline. Typically, in offline learning, training occurs only one time, following a once-training-multiple-inference

strategy. In such case, the memristor devices in the crossbar are required to have full retention of the programmed states to ensure proper function of the neural network in time. On the contrary, online learning involves an iterative update on model parameters as new data becomes available, allowing for continuous adaptation to changing environments or data distributions with massive potential for real-time adaptation. Consequently, in scenarios where online learning is employed, the distinction between training and inference becomes less pronounced. In such cases, the memristor devices are not required to present a long retention of states. In turn, the programmed weights should persist at least until the next update cycle, which can vary from milliseconds to seconds depending on the envisioned application. The continuous learning process ensures that the memristors are constantly being updated and adapted to the changing data stream, mitigating the effects of any retention loss between cycles. However, considering that the training stage is the more energy-intensive phase in a neural network, online training inherently results in higher energy consumption.

Different computing paradigms can also be employed during the training process, such as deep neural networks (DNNs) or spiking neural networks (SNNs). In DNNs training, the memristors should present symmetry and linearity in potentiation (gradual increase of conductance state) and depression (gradual decrease of conductance state), as a function of repetitive applied pulses, to allow the highest number of available states and for the fastest and most efficient algorithm to be employed. In its turn, SNNs operate using discrete pulses or spikes in asynchronous events that should result in a change in resistance state on the memristor only when a certain current threshold is reached, enabling the integration of spatiotemporal information. This spike-based communication allows for more efficient computation and better mimics the asynchronous and event-driven nature of biological neural systems.

Regardless of the targeted computing paradigm, the development of a memristor-based ANN entails on the fulfillment of a specific set of requirements to attain optimal accuracies in any given task.[3] These include securing high LRS/HRS ratios to minimize measurement noise interference and enable MLC functionality, as well as ensuring low switching energy by minimizing the energy barrier for RS. However, reducing the energy barrier may decrease retention properties of the memristors. Additionally, achieving 10 nm scalability is crucial for very-large-scale integration (VLSI), which often hinders device-to-device (D2D) and cycle-to-cycle (C2C) reproducibility.

Consequently, the development of a memristor device that follows all the above requirements has been extremely challenging. A device that presents area-dependent switching would be preferred since it shows inherent analog behavior with multiple possible resistance states, differing from the MLC presented by filamentary-type of switching where a finite number of states are available, that usually present high random telegraph noise (RTN). The switching energy in area-dependent switching is also, typically, lower and no electroforming step is required. Another advantage of area-dependent switching is low D2D and C2C variabilities whereas filamentary-type of switching usually suffers from high variability due to the randomness of CFs formation. However, area-dependent switching usually presents poor retention of programmed states which is unsuited for DNNs applications in which a

strategy of once-training-multiple-inference is applied for offline learning. Symmetry and linearity in potentiation and depression is also challenging to be accomplished without resorting to complex programming schemes, which in turn complicate the peripheral circuits necessary for training inputs for on-chip learning. Moreover, one of the most challenging aspects of circuit implementation with memristors is crosstalk. Crosstalk is related to the sneak-path current interference during training between different memristor cells in crossbars and often leads to misinterpretation of the output results.[4]

Furthermore, for applications in artificial visual systems, these neural networks, serving as processing units, would need to be integrated with different sensing units for light information collection. These photodetectors can, in fact, be optoelectronic memristors (OEMs) that use both light and electronic signals as inputs and can themselves behave as sensory artificial synapses with high energy-efficiency and low crosstalk. OEMs are, thus, suitable to link artificial visual systems with image processing on hardware.[5] This novel application concept, known as neuromorphic vision sensors, possesses the ability to directly detect instant changes, similarly to the human eye. In such, the OEM crossbar captures movement as a continuous flow of data and adapts and retains its resistance state until further motion is detected following the rules of SNNs. When this sensing crossbar perceives movement, an image pre-processing task can also be realized before that information is sent to the post-processing stages such as image stylization, edge enhancement, contrast correction and/or noise reduction.[6] This novel approach not only produces far less data than the conventional one, resulting in increased energy efficiency, it significantly decreases the response time of the system, and it also results in higher accuracies in image recognition tasks due to the pre-processing added stage. However, this being a novel field, only a few reports exist in the literature on non-patterned optoelectronic memristors with low light/dark ratios of less than 10. Moreover, sensitivity to visible (red/green/blue) light is of extreme importance to the development of trustworthy and cutting-edge image recognition technologies.[7]

It is important to note that light can also be used as synaptic weigh modulator during training in ANNs composed of OEMs. However, in such cases, light is usually not applied as input during inference for image sensing and, thus, a different sensing unit must be employed, to avoid disrupting the trained weights. Alternatively, complex architectures are required where more than one device is used per pixel to allow light to be both the training and the sensing source.[8]

1.2 Objectives

This PhD project aimed to significantly contribute to the neural network hardware field by proposing an entire multifunctional-optoelectronic system composed of memristors and the supporting

electronics for applications in artificial visual memory systems and image processing, addressing the state-of-the-art challenges. Targeting extensive research on this topic, the most important goals were:

(1) To develop an amorphous oxide semiconductor (AOS)-based memristor with area-dependent switching:

AOS materials are mostly based on ternary or quaternary oxides of post-transition metals, such as indium-gallium-zin oxide (IGZO), zinc-tin oxide (ZTO) and gallium-tin oxide (GTO) and have long been explored for thin-film transistors (TFTs) technology, one that has grown fast to its application on flat-panel displays, since the first IGZO-based TFT report in 2004.[9,10] Due to their superior performance, excellent stability and easy, low-cost and compatible fabrication with complementary metal–oxide–semiconductor (CMOS), this class of materials show tremendous potential as active layer in RS devices. In fact, their most attractive characteristic, is the high level of control on the conductivity of the pristine AOS film by adapting its oxygen[11] or cation composition.[12] This condition allows for both filamentary and area-dependent switching depending on the electrodes chosen which expands the range of possible applications. In this project, area-dependent switching was pursued due to its overall superior performance in meeting application requirements, such as low D2D and C2C variability, analog behavior with MLC properties and retention decay suited for SNNs. Additionally, the optimization of its drawbacks was also aimed as a specific goal for DNNs (longer retention periods).

AOS materials are also known to be transparent and can act both as active layer and electrodes enabling the realization of all-transparent memristors[13,14] and optoelectronic features. Moreover, AOS materials have high flexibility and allow for conventional patterning strategies and low-processing temperature. This facilitates the use of low-cost flexible substrates (paper, polyimide, polyethylene naphthalate (poly(ethylene 2,6-naphthalate) (PEN) / polyethylene terephthalate (PET)),[15,16] which is fundamental for embedded flexible technologies for wearables and internet-of-Things (IoT) applications.

Therefore, in this project, IGZO was chosen as active layer material since it shows potential for area-dependent switching and for the development of OEMs. The scalability requirement is also fulfilled due to the characteristic lack of grain boundaries of AOS materials that allows for a device miniaturization to the nanometer scale and therefore enables high-density circuit integration.

(2) To solve crosstalk in crossbars by adding a TFT in each cell as selector device:

This project aimed to solve crosstalk by using the 1-transistor-1-memristor (1T1M) configuration. In such, a transistor is added in each cell of the crossbar as a selector device. The transistor behaves like a switch that when turned on, acts like a high conducting wire and, when turned off, no current reaches the not selected memristor. It allows for improved control on the plasticity characteristic through current input, while providing an on-chip current compliance (CC), at the expense of cell area in crossbars. In this strategy, the IGZO-TFT can, therefore, be used, allowing for both elements

(transistor and memristor) to be fabricated at the same level. However, to employ the same IGZO layer for both devices, a deposition condition should be found compatible with the TFT's high-stability and low-leakage current and the memristor's defect-enabled switching with decent LRS/HRS ratio. Since an extreme power-efficient system is envisioned, the developed memristor should present high resistance values for both LRS and HRS. In this way, the IGZO-TFT is the best choice as selector device since it is the transistor with the lowest ever reported off-current, in the range of femtoamperes (fA) to hundreds of picoamperes (pA).[17] Moreover, it was proposed to use the IGZO TFT output as synaptic weigh modulator to achieve linearity and symmetry in potentiation and depression by current pulsing.

(3) To optimize the memristor performance for long periods of retention:

Profound research should be undertaken to understand the physical mechanism behind the RS of the IGZO-memristor in order to optimize the necessary figures of merit for application in DNNs and SNNs. In this regard, a collaboration with Professor Regina Dittmann, one of the leading scientists in the memristor field, and a research stay in Forschungszentrum Jülich was planned as part of this project, to tackle the optimization of retention properties in IGZO-based memristors with area-dependent switching.

(4) To develop an IGZO-based optoelectronic memristor:

The development of patterned IGZO-based OEMs was an important goal of this dissertation. Strategies for visible light (red/green/blue) detection were to be explored and the physical mechanism of photonic switching and how to manipulate it studied. The synaptic behavior of the OEMs should present transition from short to long-term memory and follow the rules of SNNs by making use of the PPC decay inherent to AOS materials.

(5) To propose a prototype for a multifunctional optoelectronic system:

As a final task, this project intended to propose a proof-of-concept prototype for artificial visual systems applications using an OEM crossbar, composed of the devices developed in goal (4), as sensing and pre-processing units and an active crossbar, composed of 1T1M cells developed and optimized in goals (1), (2) and (3), for information processing. Such a system can be called a photoperceptron hardware.[18] In this way, high accuracy image recognition tasks could be performed and the overall performance of artificial visual systems hardware would be greatly enhanced.[6,19] Moreover, using PPC decay on the OEM crossbar can be an efficient way to, on one hand, store the input image for some time (sufficient for inference), and, on the other hand, achieve low power operation, due to auto-resetting of the system following relaxation time.

1.3 Structure of dissertation

This dissertation is divided into ten chapters, in which the aforementioned goals are tackled in detail.

- **Chapter 1** presents the motivation and objectives of this work, the structure of this dissertation and a summary of the research impact this thesis has had in the scientific community.
- **Chapter 2** provides the state-of-the-art on AOS-based memristors. This chapter is divided in two sections: the first section describes available device level studies on AOS-based memristors fabricated by either sputtering deposition tools or solution processing methods; in the second section the suitability of these devices for specific neuromorphic applications such as in-memory computation and ANNs are analyzed. The main challenges for chip integration are reviewed.
- **Chapter 3** presents the results on the interface switching-based IGZO memristor developed in this work. The memristor structure and its synapse behavior are investigated for neuromorphic applications.
- **Chapter 4** describes the optimization on the IGZO layer of the memristor for TFT compatibility which allows for a joint fabrication of both devices on the same level. In this chapter, the synaptic properties of the memristor are also tailored for linear and symmetric synaptic weight update for applications in DNNs hardware.
- **Chapter 5** focuses on the 1T1M cell and 1T1M active crossbar fabricated on a flexible polyimide substrate. In this chapter, the crosstalk problem is discussed and successfully solved by the memristor's integration with the TFT.
- **Chapter 6** is devoted to the thorough study of the physical mechanism of RS and data retention optimization of the IGZO memristor. This chapter marks the conclusion of the first part of this dissertation, entirely dedicated to the development and optimization of an IGZO-based memristor for neuromorphic applications.
- **Chapter 7** presents an introduction to the second part of this dissertation with the state-of-the-art on optoelectronic memristors. Firstly, proposed memristor structures with different materials such as metal oxides, oxide semiconductors and 2D and 1D structures are described. Secondly, the memristor's potential for applications in arithmetic units and Boolean logic, in-memory and neuromorphic computation and artificial visual systems is assessed.
- **Chapter 8** describes the IGZO-based optoelectronic memristor developed in this work. This chapter provides details on the selection of a transparent top contact, the optimization for visible light detection and the emulation of synaptic properties suitable for applications in neuromorphic vision.

- **Chapter 9** focuses on the final goal of this dissertation: the prototype proposal as future work of a photoperceptron hardware composed of a 1T1M crossbar and an optoelectronic memristor crossbar for applications in artificial visual systems.
- **Chapter 10** provides the main conclusions of this work.

1.4 Research impact

1.4.1 List of publications

The output of this PhD project has been published, is under review or is to be submitted soon, as referenced below, in 6 original papers, 1 topical review article and one book chapter.

(1) **M. Pereira,** J. Deuermeier, R. Nogueira, P.A. Carvalho, R. Martins, E. Fortunato and A. Kiazadeh, "Noble-Metal-Free Memristive Devices Based on IGZO for Neuromorphic Applications", in Advanced Electronic Materials, vol 6, 10, 2000242, 2020. DOI: 10.1002/aelm.202000242

(2) **M.E. Pereira,** J. Deuermeier, P. Freitas, P. Barquinha, W. Zhang, R. Martins, E. Fortunato and A. Kiazadeh, "Tailoring the synaptic properties of a-IGZO memristors for artificial deep neural networks", in APL materials, vol 10, 1, 011113, 2022. DOI: 10.1063/5.0073056

(3) **M.E. Pereira,** J. Deuermeier, C. Figueiredo, Â. Santos, R. Martins, E. Fortunato, P. Barquinha and A. Kiazadeh, "Flexible active crossbar arrays using amorphous oxide semiconductor technology towards artificial neural networks hardware", in Advanced Electronic Materials, vol 8, 11, 2200642, 2022**.** DOI: 10.1002/aelm.202200642

(4) **M.E. Pereira,** R. Martins, E. Fortunato, P. Barquinha and A. Kiazadeh, "Recent progress in optoelectronic memristors for neuromorphic and in-memory computation", in Neuromorphic Computing and Engineering, vol 3, 2, 022002, 2023. DOI: 10.1088/2634-4386/acd4e2

(5) **M.E. Pereira**, E. Carlos, E. Fortunato, R. Martins, P. Barquinha and A. Kiazadeh, "Amorphous oxide semiconductor memristors: brain-inspired computation", Chapter 16 in Advanced Memory Technology: Functional Materials and Devices. Royal Society of Chemistry, 2023. DOI: 10.1039/BK9781839169946-00431

(6) **M.E. Pereira,** J. Deuermeier, R. Martins, P. Barquinha and A. Kiazadeh, **"**Unlocking Neuromorphic Vision: Advancements in IGZO-based Optoelectronic Memristors with Visible Range Sensitivity", in ACS applied electronic materials, 2024. DOI: 10.1021/acsaelm.4c00752.

(7) **M.E. Pereira,** J. Deuermeier, T. Mingates, P. Carvalho, T. Calmeiro, M. Cortinhal, E. Fortunato, R. Martins, P. Barquinha and A. Kiazadeh, "Comprehensive analysis on the eightwise resistive switching mechanism of a-IGZO based memristors", in preparation, 2024.

(8) **M.E. Pereira**, E. Fortunato, R. Martins, P. Barquinha and A. Kiazadeh, "Photoperceptron hardware based on IGZO for artificial visual systems", in preparation, 2024.

Moreover, since the beginning of this PhD project, the student has contributed to the 6 subsequent referenced articles, in which the PhD student is co-author:

(9) C. Silva, J. Martins, J. Deuermeier, **M.E. Pereira**, A. Rovisco, P. Barquinha, J. Goes, R. Martins, E. Fortunato and A. Kiazadeh, "Towards Sustainable Crossbar Artificial Synapses with Zinc-Tin Oxide", in Electronic Materials, vol 2, 2, 105–15, 2021. DOI: 10.3390/electronicmat2020009

(10) G. Carvalho, **M. Pereira**, A. Kiazadeh and V. G. Tavares, "A neural network approach towards generalized resistive switching modelling", in Micromachines, vol. 12, 9, 1132, 2021. DOI: 10.3390/mi12091132

(11) G. Carvalho, **M.E. Pereira**, C. Silva, J. Deuermeier, A. Kiazadeh and V. Tavares, "Characterization and modeling of resistive switching phenomena in IGZO devices", in AIP Advances, vol. 12, 8, 085017, 2022. DOI: 10.1063/5.0098145

(12) R.A. Martins, E. Carlos, J. Deuermeier, **M.E. Pereira**, R. Martins, E. Fortunato and A. Kiazadeh, "Emergent solution based IGZO memristor towards neuromorphic applications", in Journal of Materials Chemistry, vol. 10, 1991–8,2022. DOI: 10.1039/D1TC05465A

(13) G. Carvalho, **M. Pereira**, A. Kiazadeh and V. G. Tavares, "Depletion Based Digital and Analogue Circuits with n-Channel IGZO Thin Film Transistors", in 2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 1-5, 2023. DOI: 10.1109/ISCAS46773.2023.10181633

(14) C. Bordoni, A. Ciavatti, M. Cortinhal, **M. Pereira**, T. Cramer, P. Barquinha and B. Fraboni, "Dielectric multilayers impact on radiation-induced charge accumulation in highly sensitive oxide field effect transistors", in APL materials, vol. 12, 3, 031106, 2024. DOI: 10.1063/5.0189167

1.4.2 List of presentations in conferences

The work developed in the course of this thesis has been presented in 10 conferences or seminars with 5 oral and 5 poster presentations and distinguished by 5 international and national awards.

(1) Poster “AOS-based memristive devices towards TFT integration: Materials and challenges” at Materials Challenges for Memory, APL Materials, April 2021

(2) Poster “Memristive devices for neuromorphic applications based on amorphous oxide semiconductor nanoscale films” at DOCEIS, 12th Advanced Doctoral Conference on Computing, Electrical and Industrial Systems, July 2021.

(3) Oral presentation “Synaptic characteristics of IGZO-based memristors networks for pattern recognition applications” at 10th International PhD Meeting, Fraunhofer, Dresden Germany, September 2021.

(4) Poster "Tailoring resistive switching characteristics of IGZO-based memristive devices for artificial deep learning neural networks" at the 4th International Conference on Memristive Materials, Devices & Systems (MEMRISYS, 2021), Japan, November 2021 - Won **Excellent Poster Presentation Award**

(5) Poster "Tailoring the synaptic characteristics of a-IGZO memristors for pattern recognition applications" at Ciência 2022- Encontro com a ciência e tecnologia em Portugal, Lisbon, May 2022

(6) Oral presentation "Active crossbar using amorphous oxide semiconductor technology towards artificial neural networks hardware" at the 2022 European Materials Research Society (E-MRS) Conference - Symposium E: Adaptive materials and devices for brain-inspired electronics, May-June, 2022 - Won **Young Researcher Award**

(7) Oral presentation "In-memory vector-matrix multiplication using flexible thin-film 1-transistor-1-memristor crossbar" at the 17th International Thin-Film Transistor Conference (ITC 2022), Surrey UK, September 2022 - Won **Best Contributed Presentation Award**

(8) Oral presentation "Flexible 1-transistor-1-memristor crossbar for Artificial Neural Network hardware" at the 11th European School for Young Materials Scientists, Lisbon, September 2022 - Won **Best Oral Presentation Award**

(9) Poster " Sustainability in memristor technology using non-critical elements and additive manufacturing" at Ciência 2023- Encontro com a ciência e tecnologia em Portugal, Aveiro, July 2023

(10) Oral presentation "Optoelectronic memristor devices based on oxide semiconductors for neuromorphic vision sensors" at the IX Annual Meeting i3N, Praia da Vieira, May 2024 - Won **Best PhD Oral Presentation Award**

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Chapter 2

Amorphous oxide semiconductor-based Memristors

Memristors in crossbar arrays can accomplish computing operations while storing data at the same physical location, enabling a cost-efficient latency-free solution to the Von Neuman's bottleneck. Amorphous oxide semiconductor (AOS)-based memristors can be engineered to perform filamentary and/or interface-type resistive switching. Their superior characteristics such as high flexibility compatible with low-temperature and easy manufacturing evidence the potential for embedded flexible neuromorphic technologies. In this chapter, the state-of-the-art on AOS-based resistive switching devices is analyzed, along with their suitability for specific neuromorphic applications such as in-memory computation and deep and spiking neural networks. Currently, crosstalk is the main obstacle to large-scale crossbar integration and, therefore, the proposed main approaches to overcome it are discussed. Here, given the high level of behavior control offered by AOS-based memristors, self-rectifying characteristics or optoelectronic features can be established. Moreover, the compatibility of AOS films with both memristors and thin-film transistors, provides the necessary means for active crossbars to be developed in a cost-efficient, simple and with higher-interconnectivity manner.

The literature review presented in this chapter is published in:

M.E. Pereira, E. Carlos, E. Fortunato, R. Martins, P. Barquinha and A. Kiazadeh, Chapter 16 "**Amorphous oxide semiconductor memristors: brain-inspired computation**", in Advanced Memory Technology: Functional Materials and Devices. Royal Society of Chemistry, 2023.

2.1 Introduction

New computing paradigms are urgently required to replace the outworn von-Neumann's architecture that, currently, carries numerous constraints such as latency, high-power consumption and scaling limitations to the highly demanded technologies of Artificial Intelligence (AI). Neuromorphic systems based on resistive switching (RS) devices are a promising solution, due to their ability to perform in-memory computation with adaptive learning algorithms on hardware in a low-power and cost-efficient manner, realizing tasks like real-time unstructured data arrangement, parallel data processing or pattern recognition.

The idea of an artificial neural network (ANN) hardware by using interconnected and adaptive electronic elements goes back to 1962.[1] The RS device, or memristor, concept was then introduced by Leon Chua in 1971[2] and later achieved by HP labs[3] in 2008. The memristor is a non-linear two-terminal device, usually composed of a three-layer metal-oxide-metal sandwich structure. The device's resistance level can be modified with the application of an electric field. The transition between high-resistance state (HRS) to low-resistance state (LRS) is called Set while the reverse transition, from LRS to HRS, is referred to as Reset. The fastest switching speed ever reported, up to now, is of 50 ps for both Set[4] and Reset[5] operations. Additionally, RS devices have an outstanding potential for very-large-scale integration (VLSI) systems as demonstrated by the smallest 4 nm^2 memristor reported up to date.[6]

When it comes to AI applications using RS devices, there are several approaches that can be followed, as memristors can perform computing in distinct manners. A complete review on the potential of the memristor for implementation of in-memory computing, deep neural networks (DNNs), and spiking neural networks (SNNs) is provided elsewhere.[7] Naturally, a specific set of requirements related to the memristor performance are in place, depending on the application envisioned. As an example, for in-memory computation a long retention of data is crucial while for SNNs is not the most critical feature.

The RS behavior of a memristor can be tuned by the choice of materials to be assembled. Several dielectric materials have been studied as active layer including titanium oxide (TiO_x), tantalum oxide (TaO_x) or hafnium oxide (HfO_x).[8–10] Typically, the physical mechanism attributed to RS is related to the formation of one or more conductive filaments (CFs) during the electroforming step which entails on a soft breakdown of the insulating material by application of an electric bias, usually of higher voltage than the operating one. The CFs are then dissolved/recreated in the oxide film, by a local redox process, leading to the change in resistance state,[11–13] as shown in **Figure 2.1(a)**. Filamentary-type of switching usually results in an abrupt transition between HRS to LRS and *vice-versa* as can be observed in the example of **Figure 2.1(c)**.

Another, less common, type of RS is interface-switching. Here, the switching occurs at the interface between a metal electrode and the oxide and is, typically, attributed to an exchange or trapping of ions, at the interface between the oxide and a metal electrode,[14] as in the illustration of **Figure 2.1(b)**. There is a homogeneous contribution of oxygen vacancies (VOs) and ions throughout the entire interface, which results in an area-dependent behavior with lower device-to-device (D2D) and cycle-to-cycle (C2C) variability, when compared with filamentary-type of switching. Interface-type of RS mainly results in analog behavior, as presented in **Figure 2.1(d)**, with multiple resistance states, which is very appealing for neuromorphic applications. However, retention data is often a challenge since these devices are more sensitive to slight variations in number of VOs generated.[15]

Amorphous oxide semiconductors (AOS) are mostly based on ternary or quaternary oxides of post-transition metals, such as indium-gallium-zinc oxide (IGZO), zinc-tin oxide (ZTO) and gallium-tin oxide (GTO). AOS materials have long been explored for thin-film transistors (TFTs) technology, one that has grown fast to its application on flat-panel displays, since the first IGZO-based TFT report in 2004.[16,17] Due to their superior performance, excellent stability and easy, low-cost and CMOS compatible fabrication, this class of materials show tremendous potential as active layer in RS devices. In fact, their most attractive characteristic, is that it can be controlled whether the pristine AOS film is insulating or conducting by adapting the oxygen[18] or cation composition.[19] This condition allows for both filamentary and interface-type of switching which expands the range of possible applications.

Moreover, AOS materials are known to be transparent and can act both as active layer and electrodes enabling the realization of all-transparent memristors[20,21] and optoelectronic features. On the other hand, AOS materials have high flexibility, due to the lack of grain boundaries, and allow for conventional patterning strategies and low-processing temperature. This facilitates the use of low-cost flexible substrates (paper, Polyethylene naphthalate (poly(Ethylene 2,6-Naphthalate) (PEN), and Polyethylene Terephthalate (PET)),[22,23] which is fundamental for embedded flexible technologies for wearables and Internet-of-Things (IoT) applications. For this reason, the research interest on AOS materials as active layer and electrodes for memristors have been rapidly growing as evidenced by **Figure 2.1(e)**.

In this chapter, the state of the art on RS devices based on AOS materials will be discussed. Moreover, the potential of AOS-based memristors for circuit implementation, in-memory computation, deep learning accelerators and SNNs applications will be examined, along with the current challenges and future perspectives.

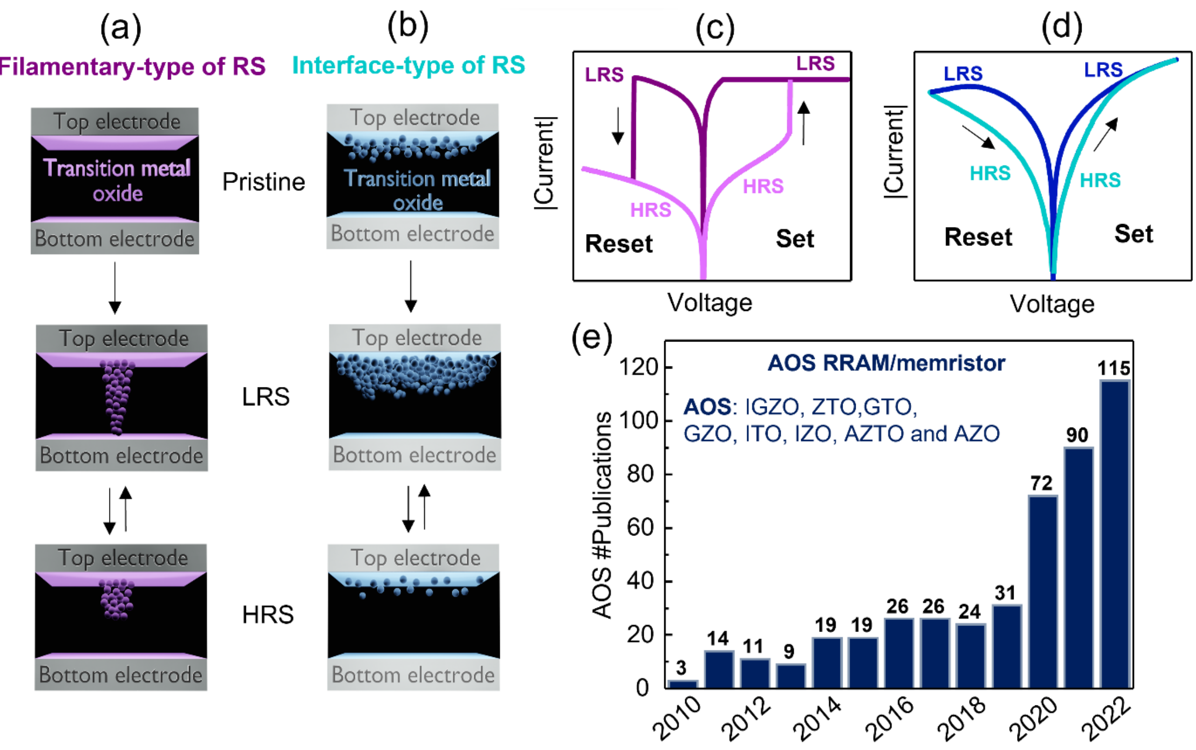

Figure 2. 1 Most common types of RS. Illustrations of (a) filamentary-type RS, comprising the filament formation/rupture during LRS/HRS and (b) Illustration of interface-type RS, including the oxygen vacancies movement and density during LRS/HRS. Typical IV curve of a (c) filamentary-type memristor displaying digital Set/Reset transitions and (d) interface-type memristor showing analog Set/ Reset transitions. (e) Publications on AOS materials for memristors from 2010 to 2022 (search engine: Google Scholar, accessed on July 2023; keywords: IGZO;ZTO;ITO;IZO;AZO;AZTO;GZO;GTO RRAM;memristor).

2.2 Device level studies

Several fabrication techniques have been reported for the realization of AOS-based RS devices such as radio frequency (RF) sputtering, chemical vapor deposition (CVD), atomic layer deposition (ALD) and solution processing. Sputtering deposition is the most common since it provides highly uniform films in large areas and an accurate control of oxygen content during deposition. Solution processing methods have been promptly improving and are now a promising technology that offers low-cost and simple fabrication of memristive devices.[24] Therefore, in this chapter, the focus will be on AOS-based memristors fabricated by these two techniques.

2.2.1 AOS-based Memristors by Sputtering Deposition

2.2.1.1 One-layer AOS-based Memristors

The first AOS-based memristor, reported in 2010, envisioned the integration with IGZO-TFTs for advanced system-on-panel display applications. Therefore, IGZO was used as active layer and indium-tin oxide (ITO), as bottom and top electrodes, accomplishing the first transparent AOS-based

memristor. An abrupt filamentary-type of switching was demonstrated with retention data up to 10^3 s at 90 °C. The formation of VOs filaments explained LRS, whereas HRS was attributed to the rupture of filaments by recombination of VOs and moveable oxygen ions, causing a bipolar behavior. The I_{LRS}/I_{HRS} ratio was 10 and C2C variability was slightly high in the 100 DC-sweep cycles performed.[20]

Since then, several strategies have been reported to improve I_{LRS}/I_{HRS} ratio. Hwang *et al.* reported that conventional thermal annealing (CTA) or microwave irradiation (MWI) treatments on the IGZO layer results in a smoother surface and reduces the current in HRS.[25] Ma *et al.* showed that an oxygen plasma treatment to the bottom Al contact improves I_{LRS}/I_{HRS} ratio to 10^5. This is related to a smoother bottom electrode interface due to the induced Al_2O_3 layer by oxygen plasma in the Al electrode. Moreover, in their study, an enhanced I_{LRS}/I_{HRS} ratio was achieved when Al was replaced by Ag as top electrode. In this case, an Ag^+ filament is created between the electrodes and a Schottky barrier at Ag/IGZO interface leads to lower current in HRS.[26]

IGZO doping can also lead to the improvement of memristor performance. Li *et al.* showed Ru doping weakens the bond between the metal and oxygen atoms enabling the creation of strong CFs and stable 10^5 I_{LRS}/I_{HRS} ratio.[27] Zhang *et al.* reported on the memristor structure illustrated in **Figure 2.2(a)**, in which a 4 nm partial layer of the IGZO was doped with N close to the TiN electrode.[28] The typical bipolar filamentary-type RS presented improved C2C variability and retention data of up to 10^4 s at 125 °C, as can be seen in **Figure 2.2(b)** and **2.2(c)**. The authors explained the IGZO:N can act as an oxygen reservoir layer, facilitating the recovery and rupture of CFs in fixed paths.

Moreover, the oxygen content during IGZO deposition is a crucial parameter to tune RS behavior. Higher oxygen content enables a forming-free RS attributed to a higher quantity of oxygen-related defects.[29] Fan and co-workers showed that increasing the oxygen content leads to a decrease of current in HRS, resulting in higher I_{LRS}/I_{HRS} ratios, at the expense of higher C2C variability. In their work, the insertion of a Ti interlayer, between IGZO and titanium nitride (TiN) top electrode, showed lower initial resistance since Ti creates VOs in the switching oxide, due to its high oxygen affinity. This resulted in more stable devices with lower electroforming voltage and higher yield.[30] Hsu *et al.* reported multi-level cell (MLC) operation, where 4 different resistance states by changing current compliance (CC) during Set were obtained.[31] Higher CC increases the diameter of CFs which decreases its resistance and thus multiple LRS levels for different CC values can be achieved.[32]

Besides the common bipolar behavior, unipolar RS in IGZO-based memristors has been demonstrated using different electrodes.[33–36] In these devices, the randomly rupture of filaments takes place due to Joule heating oxidation and is unrelated to voltage polarity, leading to low C2C reproducibility and endurance. However, a filamentary type-unipolar RS can shift to bipolar interface-type switching when an extra oxygen-deficient layer is created by application of opposite bias at a high CC.[37]

As mentioned previously, the interface-type RS is homogeneously distributed over the electrode area and, therefore, it can be controlled by the selection of a Schottky and an ohmic electrode[38] or by

the modulation of asymmetric barrier heights induced by changing the active layer oxygen content or cation composition through its thickness.[39,40]

Jang *et al.* revealed analog interface-type RS using Pd/IGZO/Mo structure and compared it with filamentary RS of Pd/IGZO/Pd structure. The authors explained that the analog RS behavior was not related to the Ohmic junction at Mo/IGZO interface, but to the Schottky junction at IGZO/Pd interface. When under positive bias, VOs easily migrate from Mo to Pd, reducing the Schottky barrier height of IGZO/Pd junction and performing Set. Under negative bias, the opposite occurs, and VOs migrate from Pd to Mo, increasing the Schottky barrier height of IGZO/Pd junction and achieving Reset.[41]

In **Figure 2.2(d)**, the memristor structure reported by Pereira *et al.* is illustrated. The molybdenum oxide (MoO_x) thin layer is induced by an oxygen plasma treatment to the Mo bottom contact prior to IGZO deposition, establishing the necessary Schottky contact. In **Figure 2.2(e)**, the I-V characteristics are presented, where the analog behavior of multiple resistive states is clear. Here, retention loss is usually dependent on the voltage or duration/number of pulses applied, as can be seen in **Figure 2.2(f)**.[42] This type of behavior is common in interface-type of switching and is well-suited for SNN applications. A similar strategy was also reported using p^+Si substrate, which presents a native SiO_2, that serves as Schottky contact at the IGZO interface.[43]

Qin *et al.* concluded that changing the oxygen content during IGZO deposition could dictate if the RS behavior was filamentary or interface-type.[44] Bang *et al.* produced an IGZO double-layer, one oxygen rich close to the Cu top electrode and another oxygen deficient at the bottom electrode. The IGZO/Cu junction resulted in a Schottky barrier diode, leading to analog performance of RS.[45] Katagiri and team showed a similar IGZO double-layer but with a symmetric structure using Au as electrodes for filamentary-type of switching with 7.2×10^2 of I_{LRS}/I_{HRS} ratio at 1 V.[46]

Besides IGZO, ZTO is another promising AOS material studied for RS devices. Even if less common, its applications to electronics are wide and have the advantage of being critical raw materials free, without indium and gallium used in IGZO.[47] The filamentary-type RS of ZTO memristors have been demonstrated using several electrodes.[48,49] MLC with 6 levels of RS was demonstrated by Ismail *et al.* using Ta and TiN as top and bottom electrodes, respectively.[50]

Kiazadeh *et al.* developed a ZTO memristor with asymmetric structure, as illustrated in **Figure 2.2 g)**. The electroforming process in the reverse polarity led to typical abrupt RS, as depicted in **Figure 2.2(h)**, with retention data up to 10^5 s, I_{LRS}/I_{HRS} ratio of 10^3 and low C2C variability. In this study, interface-type of switching was accomplished, with the same structure, by initiating the device in the forward direction showing area-dependent switching over 10^2 ratio at the expense of retention data.[51] Kim *et al.* also observed both types of RS where the Reset and Set stop voltage controlled the analog RS behaviour.[52]

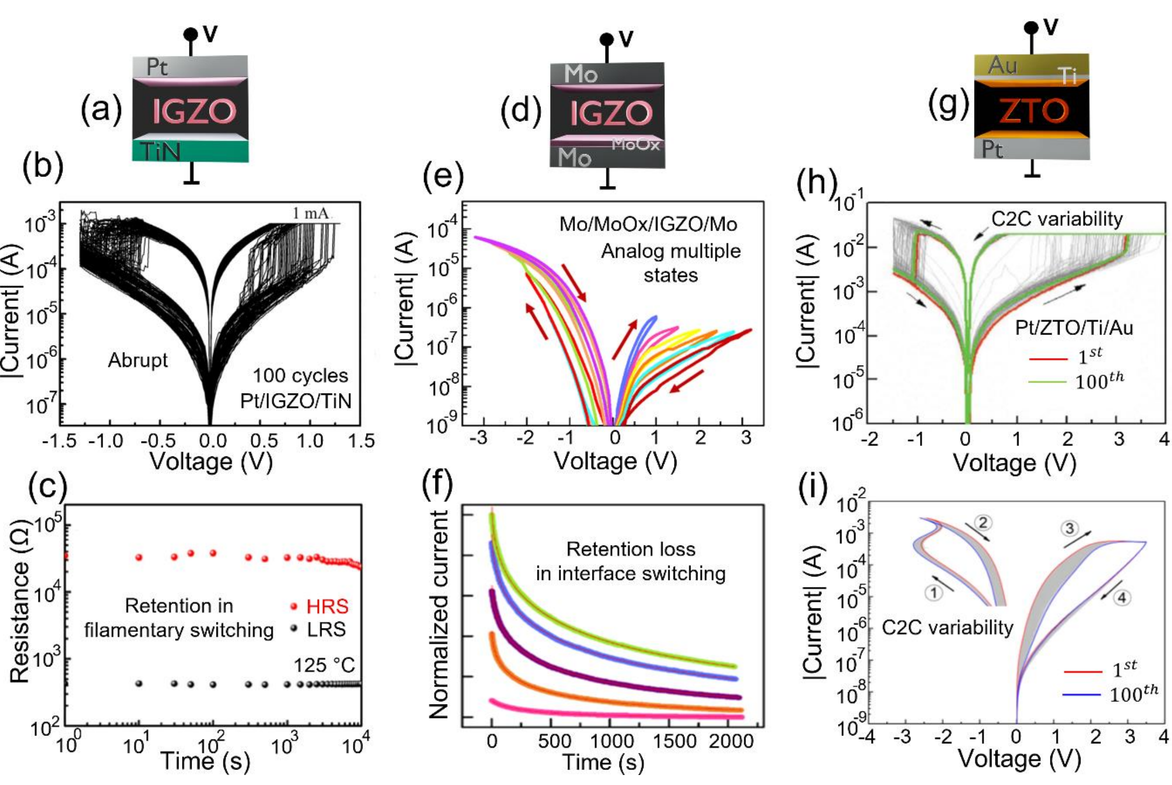

Figure 2. 2 Typical RS behavior in one-layer AOS-based memristors. TiN/IGZO/Pt memristor: (a) structure illustration; (b) correspondent abrupt behavior in I-V sweep and (c) retention data of HRS and LRS states. Adapted from Ref. 28 with permission from Elsevier, Copyright © 2020. Mo/MoO_x/IGZO/Mo memristor: (d) structure illustration; (e) correspondent analog switching in I-V sweep and (f) retention loss of multiple states. Adapted from Ref. 42 with permission from John Wiley & Sons, Copyright © 2020 Wiley-VCH GmbH. Pt/ZTO/Ti/Au memristor: (g) structure illustration; (h) correspondent abrupt switching in IV sweep. Adapted from Ref. 51 with permission from John Wiley & Sons, Copyright © 2019 Wiley-VCH Verlag GmbH & Co KGaA, Weinheim. (i) correspondent analog interface-type of switching in I-V current and voltages sweeps for Set and Reset operations, respectively. Adapted from Ref. 54, https://doi.org/10.3390/electronicmat2020009, under the terms of the CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

Additionally, fully analog performance was reported for a n^+Si/ZTO/Ni[53] structure and for patterned Pt/ZTO/Ti/Au where a controllable RS was obtained with low C2C variability as shown in **Figure 2.2(i)**, by combining current and voltages sweeps for Set and Reset operations, respectively.[54]

Other AOS materials have been used as active layer in RS devices, such as tungsten-doped indium-zinc oxide (WIZO),[55] aluminium-doped ZnO (AZO),[56] aluminium-doped ZTO (AZTO)[57] and ITO.[58] ITO is most commonly used as transparent electrode and, therefore, when used as active layer, memristors composed solely of one material can be accomplished.[59–61] Analog switching was, as well, demonstrated for oxygen rich-deficient double-layer GTO memristors.[62–67]

Hence, AOS-based memristors composed of one-layer as active material can perform filamentary or interface-type RS depending on the symmetric/asymmetric choice for electrodes, the AOS deposition parameters controlling VOs gradient and even on how one electrically operates the device. Filamentary RS can be tuned for MLC with up to 6 levels reported so far with long retention data.

However, for AI applications a fully analog behavior with more resistive states would be preferred, which is difficult to achieve without retention data loss.

2.2.1.2 Double-layer AOS-based Memristors

The insertion of a layer between the oxide and one of the electrodes can further improve RS device performance. In regards to the IGZO memristor, Pei *et al.* revealed that inserting an SiO_2 buffer layer can improve I_{LRS}/I_{HRS} ratios in filamentary-type RS.[68] Later, Choi *et al.* used the SiO_2 layer for analog RS and showed an improvement of retention time,[69] promising for in-memory computation and DNNs applications.

The I_{LRS}/I_{HRS} ratio can be increased by inserting a thin gallium oxide (GaO) layer close to one of the electrodes.[70] Here, the filament is not entirely ruptured during Reset and is, instead, confined to the small GaO_x area, due to its higher thermal conductivity than IGZO. Moreover, the thickness of filament rupture of the bi-layer device is longer when compared to the single-layer device, which explains a higher resistance in HRS. After Reset, the remaining part of the filament attached to the bottom electrode can be generated at that exact location, resulting in improved C2C stability and MLC operation up to 3 levels, obtained by changing CC.[70] GaO has also been implemented coupled with ITO as a single-layer, deposited by co-sputtering of ITO and GaO targets. Both interface and filamentary-type RS could be observed depending on the electroforming CC.[71] Moreover, reversible transition between volatile and non-volatile MLC RS was observed in IGZO/manganese oxide (MnO) memristors by regulating CC during Set. For low CC, unstable CFs were created leading to an immediate rupture showing a typical volatile RS, whereas for higher CC, the CFs grew stronger and showed a non-volatile RS.[72]

Adding an aluminum oxide (Al_2O_3) layer further improves I_{LRS}/I_{HRS} ratio by several orders of magnitude in filamentary RS, as reported by Gan *et al.* on a Pt/ Al_2O_3/IGZO/titanium tungsten(TiW)/Cu structure,[73,74] see **Figure 2.3(a)**. These devices present a stable and high I_{LRS}/I_{HRS} ratio up to 10^8, and 10^4 s of retention data, displayed in **Figure 2.3(b)** and **2.3(c)**, related to the formation/rupture of Cu filaments in the Al_2O_3 layer at the IGZO/Al_2O_3/Pt interface. The use of Al_2O_3 was also employed in a multilayer stack of IZO/ Al_2O_3, illustrated in **Figure 2.3(d)**, by Park *et al.*.[22] A lower electroforming voltage was achieved with increased number of IZO layers, due to an easier formation of VOs filaments. Additionally, a high C2C stability was reached, as depicted in **Figure 2.3(e)** and **2.3(f)**.

MLC operation can be achieved in double layer AOS-based memristors by inserting a TaO layer next to IGZO[75] or ZTO. Kumar *et al.* compared ZTO single-layer and ZTO/TaO bi-layer memristors using ITO for both electrodes,[76] **Figure 2.3(g)**. A higher switching ratio was achieved with the bi-layer, along with a much more stable C2C operation. Furthermore, an analog behavior with multiple resistive states by changing Reset stop voltage was demonstrated, as can be seen in **Figure 2.3(h)**. Interestingly, the analog behavior is not assigned to interface-type RS, further confirmed by long 10^3 s retention data on multiple states, shown in **Figure 2.3(i)**. Instead, the RS behavior is attributed to a much lower quantity of VOs at the TaO/ZTO interface compared to TaO and ZTO layers. As a result, the growth and rupture

of CFs takes place at the TaO/ZTO junction. A similar behavior can be observed in n-type Si/TiO_x/IGZO/molybdenum tungsten (MoW) memristor, in which the filament is created at the IGZO and continues to the bottom electrode in the LRS, being then ruptured at the IGZO/TiO_x interface during HRS.[77]

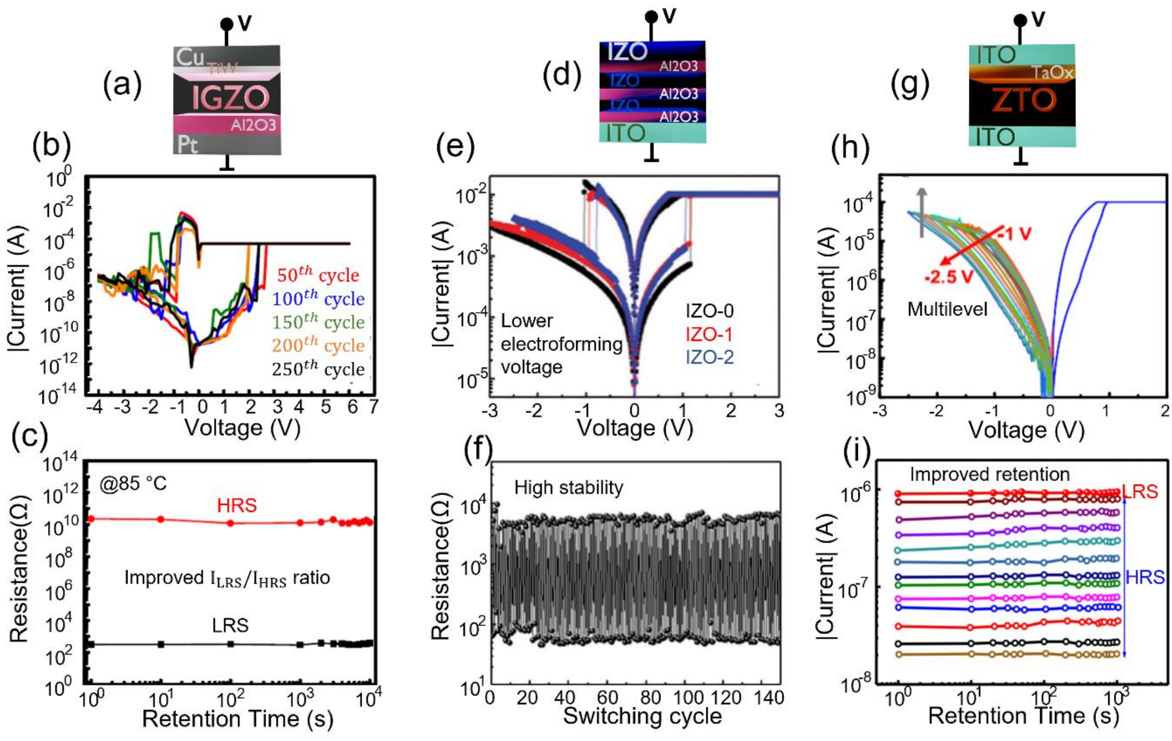

Figure 2. 3 Typical RS behavior in double-layer AOS-based memristors. Pt/Al_2O_3/IGZO/TiW/Cu memristor: (a) structure illustration; (b) correspondent abrupt switching in IV sweep and (c) improved I_{LRS}/I_{HRS} ratio in retention data. Adapted from Ref. 74 with permission from Elsevier, Copyright © 2020. ITO/Al_2O_3/IZO/Al_2O_3/IZO/Al_2O_3/IZO memristor: (d) structure illustration; (e) correspondent abrupt RS in I-V sweep showing decrease in electroforming voltage with increased number of IZO layers and (f) C2C improved stability. Adapted from Ref. 22, https://doi.org/10.1002/gch2.202100118, under the terms of the CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/. ITO/ZTO/TaO_x/ITO memristor: (g) structure illustration; (h) correspondent analog switching in I-V sweep, displaying multiple resistance states by changing Reset stop voltage and (i) improved retention data of MLC. Adapted from Ref. 76 with permission from American Chemical Society (ACS), Copyright © 2022.

Additionally, the ZnO/IGZO double-layer has resulted in improved C2C stability and lower Set/Reset voltages, allowing for low-operating voltage, a parameter demanded for neuromorphic applications.[78] This was explained by a higher number of VOs in the ZnO layer, which meant filaments could be easily ruptured there. A similar decrease in operating voltage had been, previously, observed when a ZnO buffer layer was implemented in gallium-zinc oxide (GZO)-RS devices with Ag electrode. This indium-free structure showed 2×10^3 of I_{LRS}/I_{HRS} ratio with retention data up to 10^4 s.[79]

HfO_x is another dielectric paired with AOS materials, to form bi-layers in RS devices with improved capabilities.[80] In the AZTO/HfO_x double-layer, the creation and rupture of localized filaments

takes place in the HfO_2 layer, provoking the formation of a small amount of localized filaments in the AZTO layer.[81] This particular bi-layer has the advantage of the mature compatibility of HfO_2 to semiconductor industry processes, in which Hf element is utilized for its high affinity to oxygen.

Furthermore, ZTO has been added to zirconium dioxide (ZrO_2)-based memristors with MLC characteristics. The RS was described to take place in ZrO_2 layer which acted as a high series resistance layer or VOs reservoir, while, ZTO/bottom contact interface provided the low series resistance or oxygen reservoir during Set and Reset operations, respectively. With the ZTO added layer, Reset completely shifted from abrupt to analog.[82,83] Rahmani *et al.* reported a thin layer of ZTO coupled with tin oxide (SnO)-based memristors with larger I_{LRS}/I_{HRS} ratio and improved C2C stability, explained by the creation of an interfacial titanium oxynitride (TiON) layer at the bottom ZTO/TiN interface, acting as oxygen reservoir.[84] ITO has also been used as oxygen reservoir, in the case of cerium oxide (CeO_2)-based memristor, improving analog behavior, C2C stability and retention data.[85]

Thus, several materials, usually high-K dielectrics, have been combined with AOS materials to form double-layer memristors. For filamentary-type RS, this buffer layer strategy usually improves C2C variability and I_{LRS}/I_{HRS} ratio, while for interface-type RS, the addition of an interlayer has improved retention time, this being the most critical parameter currently blocking its implementation for in-memory computation and DNN applications.

2.2.2 AOS-based Memristors by Solution Processing Methods

Encouraged by to the fast performance improvement on solution-based TFTs,[86] significant efforts have been made towards fabrication of RS devices by low-cost solution processing methods. An excellent review paper from Carlos *et al.* can be consulted on the matter, where the state-of-the-art, on all-types of materials, and current challenges for memristors fabricated by these emerging techniques is analysed.[24] Here, the focus will be solely on AOS-based memristors fabricated by solution processing methods.

The first AOS-based RS device fabricated by solution processing was reported in 2011, with a structure of ITO/GZO/ITO. All layers were deposited by solution processing techniques, spin-coating and inkjet printing. Analog RS behavior was observed with stable I_{LRS}/I_{HRS} ratio of 1.5×10^1. The switching was attributed to different crystallinity levels of the bottom and top electrodes caused by different surface treatments, which lead to different work functions and conductivities.[87] A higher RS ratio of 10^2 was later demonstrated in a solution-based GZO memristor that underwent H_2O_2 treatment in different stages of the GZO layer.[88]

In 2012, Kim *et al.* developed the first IGZO solution-based memristor with a low 2.7 RS ratio.[89] Later, the effect on RS characteristics of different surface IGZO treatments was demonstrated on a Pt/IGZO/Pt memristor, where bipolar and unipolar RS was accomplished with improved switching ratio.[90] Unipolar RS was also achieved by tunning Ga composition and introducing a Ni thin layer at the

IGZO interface, acting as oxygen reservoir.[91] Moreover, Hwang and team showed that, by increasing Ga composition in the IGZO film, a transition from analog to abrupt RS occurs.[92] In this work, increasing zinc composition led to a change of RS ratio for analog behavior. The results suggest that RS characteristics of IGZO-based memristors could be controlled by adjusting the films composition ratio, indicating a crucial parameter to consider in AOS memristors.

Rosa *et al.* proposed a memristor based on solution processed IGZO-nanoparticles, produced at low temperature (200 ℃). Bipolar RS was demonstrated with low programming voltages, a good retention time of 10^4 s and high endurance cycle.[93] Later, Li *et al.* reported a higher 10^5 I_{LRS}/I_{HRS} ratio and improved stability in C2C by applying IGZO surface treatments of ultraviolet (UV) and deep UV irradiation.[94] Furthermore, MLC operation was achieved in microwave-assisted nitridation of solution-processed IGZO RS devices.[95]

Martins and co-workers proposed the memristor structure illustrated in **Figure 2.4(a)**. MLC operation with 8 distinct states by varying Reset stop voltage, as presented in **Figure 2.4(b)**, was achieved. Different annealing temperatures, applied after IGZO deposition, and active layer thicknesses, accomplished by repeating the IGZO spin-coating process, were performed. **Figure 2.4(c)** shows the I-V characteristics and C2C variability of the various conditions. Using a higher annealing temperature and thickness produced a more stable RS behaviour.[96]

Moreover, solution-based AZTO memristors can be accomplished. Filamentary-type RS was observed for the first time in 2017[97] and later it was found that decreasing Al content of the film leads to analog RS with lower ratio.[98] In **Figure 2.4(d)**, the structure suggested by Kim *et al.* is shown. Devices without any AZTO surface treatment, with MWI at low temperature and CTA processes were compared. The I-V characteristics are displayed in **Figure 2.4(e)**. The devices that underwent MWI show higher RS ratio and lower C2C variability. This is because the MWI treatment reduces the overall number of defects more efficiently, which decreases the randomness of filament formation. In addition, the study demonstrated MLC operation with 8 separate resistive states with retention data up to 10^4 s.[99]

In regards to ZTO memristors, both abrupt-type RS, with I_{LRS}/I_{HRS} ratio of 10^4 and 10^3 s of retention data[100] and analog-type RS can be accomplished.[101] A ZTO film based on nano-cubes was employed by Siddiqui *et al.*, in a 3 × 3 crossbar structure, and the devices exhibited analog behavior with low C2C variability.[102] Additionally, a PET substrate has been utilized for the fabrication of ZTO, deposited by electrohydrodynamic inkjet technique, flexible memristors.[103] However, D2D variability was high, probably due to a common bottom electrode strategy.

Lastly, solution-based IZO is, as well, employed as switching matrix in RS devices. Hsu *et al.* presented an analog behavior by increasing the IZO thickness which resulted in 10^2 RS ratio.[104] Then, a 4 × 4 crossbar was built with a multi-layer IZO stack with uniform and reproducible RS and 10^3 s retention time.

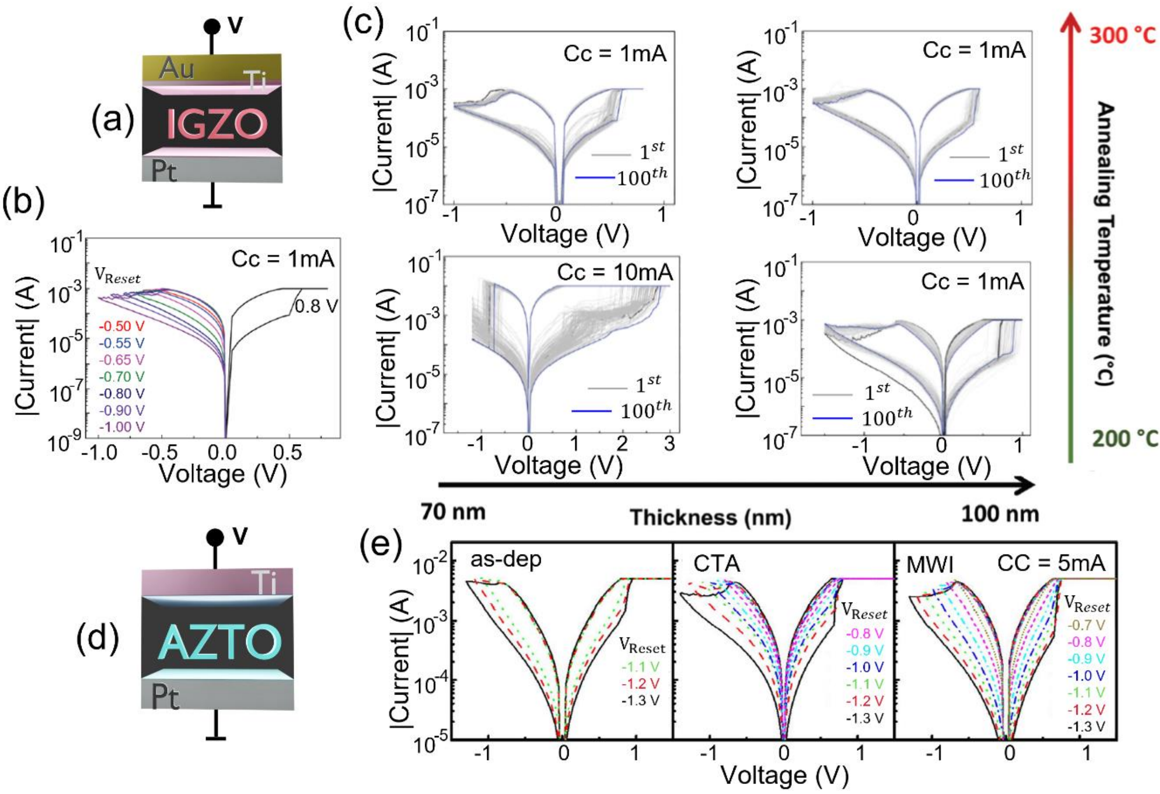

Figure 2. 4 Typical RS behavior in solution-based AOS memristors. Pt/IGZO/Ti/Au memristor (a) structure illustration; (b) correspondent I-V characteristic displaying RS with MLC on Reset operation by changing stop voltage and c) RS characteristic and C2C variability of the various conditions. Pt/AZTO/Ti memristor. Adapted from Ref. 96 with permission from The Royal Society of Chemistry, Copyright © 2022. d) Structure illustration and e) correspondent I-V characteristic displaying RS with different treatments. Namely, without any surface treatment (as-dep), with CTA and with MWI processes on AZTO layer. Adapted from Ref. 99 with permission from Elsevier, Copyright © 2017.

These results show the tremendous potential of solution-based AOS memristors with easy and low-cost manufacturing for VLSI. However, it is not yet a matured technology and needs further improvement specially on D2D variability and scalability.

2.3 Neuromorphic Applications

AOS-based memristors can be specifically designed for a certain AI application. A data-driven ANN model has been developed for AOS interface-type RS and is capable of simulating dynamic systems quickly and with few measurements.[105] In addition, an empirical model based on thermionic emission is drafted for interface-type RS behavior of IGZO memristors.[106]

In-memory computing is an alternative to the Von Neuman's approach in which computational tasks are performed at the memory itself. Not only it eliminates time, energy and cost associated with moving data, but it can improve computational time of certain complex tasks due to the massive parallelism provided by large-scale integration of loads of nanoscale RS devices. Filamentary-type RS with

abrupt behavior can be exploited for in-memory memristive logic. HRS can serve as logic “0” while LRS can be logic “1”, enabling logic operations, along with processing and storage at the same location, with input voltage and resistance state as variables.

MLC operation or full analog behavior are also much desired features for in-memory computation, allowing for more than 2 states to be processed and stored. Vector-matrix multiplication (VMM) operations can be employed to exploit the full potential of multiple states. For such, memristors in crossbar arrays are used to perform Ohm’s and Kirchhoff ’s current summation laws. However, retention data is crucial for long storage and endurance of the circuit blocks, which makes the employment of interface-type memristors a challenge, given their typical immediate retention loss more suited to SNNs. Moreover, crosstalk issues related to the current interference between cells is an enormous challenge to be overcome. Strategies will be discussed later in this chapter.

2.3.1 Deep neural networks (DNNs)

Memristive devices in crossbar configurations can be used as in-memory computing units, with their resistance levels as synaptic weights, realizing training on hardware. The input data is applied as a voltage/current vector at the rows connected to the electrodes of the memristors and the output is at the columns, as the result of Ohm’s and Kirchhoff ’s summation laws, performing VMMs.[7]

For DNNs on-chip training, the memristor needs to follow a specific set of requirements for the highest accuracies to be achieved. A 10^2 I_{LRS}/I_{HRS} ratio must be secured, for no measurement noise interference, with MLC (5-bit, 32 levels at least). Switching energy must be lower than 10 fJ, which requires a small energy barrier for RS. However, the decrease in energy barrier might cost the required retention of more than 10 years. 10 nm scalability is necessary for VLSI, which typically harms D2D and C2C reproducibility.[107] Moreover, the most important requirement to be fulfilled for an accurate DNN is symmetry and linearity of conductance state increase, called potentiation, and decrease, referred to as depression, as a function of repetitive applied pulses. Linearity enables the highest number of states and symmetry allows for the fastest and most efficient algorithm to be employed. On AOS-based memristors, several strategies have been emerging to improve linearity as most RS devices exhibit a natural non-linear response to consecutive identical spiking, visible in the purple curve of graph in **Figure 2.5(a)**.

Pereira *et al.* showed the dependence of the plasticity characteristic of IGZO-based memristors on the pulse scheme applied, **see Figure 2.5(a)**. A linear and symmetric potentiation and depression was achieved with incremental pulse amplitude and width. Extremely low C2C variability was obtained, as depicted in **Figure 2.5(b)**.[108] Similar strategies have been successfully shown for ZTO memristors by increasing pulse width[53] and IGZO memristors by increasing pulse amplitude.[41] However, a complex spiking scheme increases the complexity of peripheral circuit for on-chip training. Some studies

reported an improved plasticity characteristic by simply using a low voltage and reduced width identical pulse train.[52,54] However, this usually implies a drastic decrease in I_{LRS}/I_{HRS} ratios.

Shrivastava *et al.* compared a ZTO RS device with and without N_2 annealing treatment performed at the upper interface of ZTO,[109] see **Figure 2.5(c)**. Both linearity and symmetry were effectively improved by the treatment with low C2C variability, as can be seen in **Figure 2.5(d)**, **2.5(e)** and **2.5(f)**. The authors explained that the grain size on the ZTO interface increases with the treatment, resulting in a reduced grain boundary scattering and higher mobility.

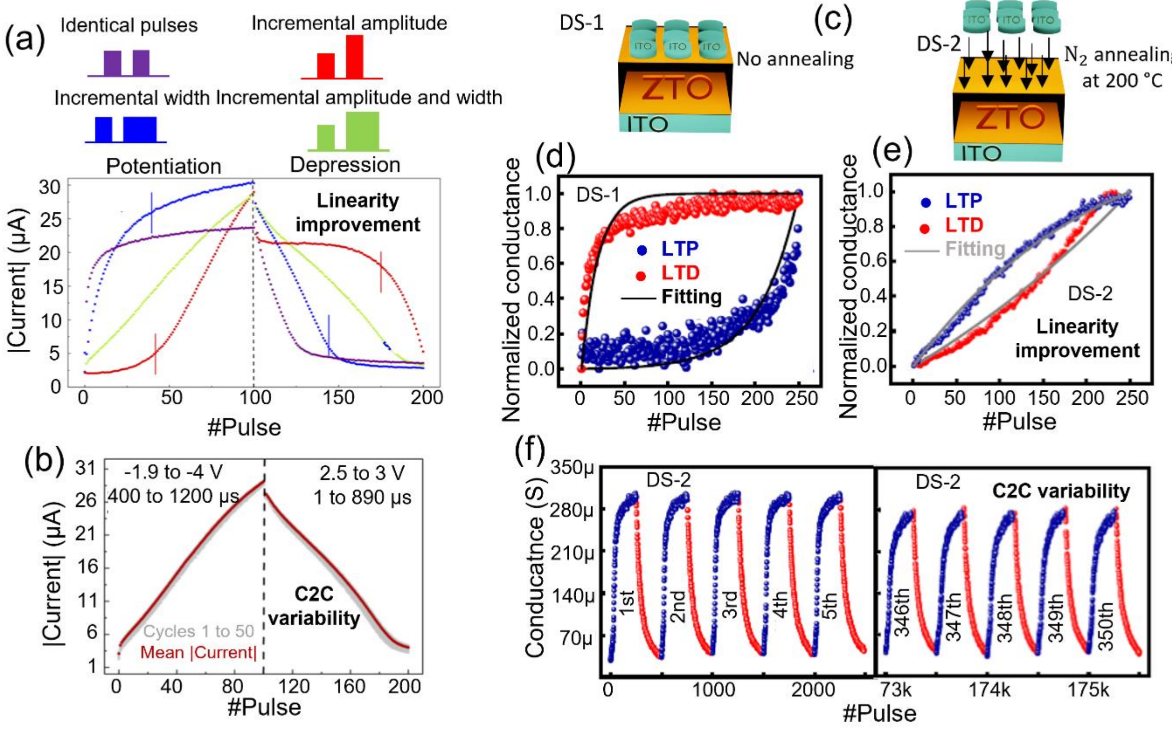

Figure 2. 5 Strategies for linearity/symmetry improvement of plasticity characteristic in AOS-based memristors. (a) Potentiation and depression results for different pulse schemes illustrated in different colors and (b) 50 cycles of potentiation and depression using incremental pulse amplitude and width. Adapted from ref. 108, https://doi.org/10.1063/5.0073056, under the terms of the CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/. (c) schematic illustration ITO/ZTO/ITO structure without (DS-1) and with N2 annealing treatment (DS-2). (d) and (e) correspondent plasticity characteristic showing improved linearity and symmetry for DS-2 and (f) Cycles of potentiation and depression for DS-2. Adapted from ref. 109 with permission from American Chemical Society, copyright © 2022.

Moreover, higher oxygen content during deposition leads to higher resistance across AOS thickness, which is related to higher linearity in potentiation and depression.[40] The synaptic behavior can also be improved by the bi-layer structure, as the added layer usually provides a more stable device with improved C2C variability and MLC operations. As an example, Choi *et al.* showed that the ZnO highly conductive layer, coupled with IGZO, makes it easier for charge carriers to be injected under small voltages, therefore, improving plasticity.[78]

Despite the vast efforts in achieving a memristor suitable for DNNs hardware, it has yet to appear the ideal synaptic element that meets all the requirements. AOS-based memristors can present the necessary analog behavior and several strategies have proven obtainable excellent linearity and symmetry on the plasticity characteristic. This is very promising for a cost-effective manufacturing where the peripheral circuit can be composed of the same AOS materials for TFTs. Retention loss in interface-type RS is the main challenge to overcome and needs to be exploited in the future.

2.3.2 Spiking neural networks (SNNs)

With SNNs the notion of time is incorporated in the algorithms. The input data is translated into the relative timing of pre and post-spikes, and is not related to the specific shape of pulses. When compared with DNNs, input signals in SNNs are more easily implemented as binary spiking and, therefore, the forward propagation operation is in place that requires only adding operations. The scaling potential of memristive devices, together with low operating voltages/currents, indicate that RS device crossbar implementation can supply a significant efficiency improvement over silicon-based technologies.[110]

The investigation on memristor based hardware for SNNs is still on an early stage and most efforts with AOS-based RS devices have been focused on developing the single synaptic element that can behave with the specific characteristics. Here, retention data should be dependent on a number of factors, such as number of pulses applied. A transition from short-term memory (STM) to long-term memory (LTM) can then be emulated. Retention loss, associated with the forgetting function of human brain, is usually fitted with a stretched-exponential function (SEF) with characteristic relaxation time that increases with number of pulses. Wang *et al.* showed such feature with IGZO memristors with the ratio of memory retention after 70 s increasing from 37% for 10 pulses to 52% for 150 pulses.[39] A similar behavior was observed by Ryu *et al.* in a ZTO memristor in which 50 pulses were enough for full retention data during 1000 s while 10 pulses resulted in relaxation of the state.[52] More interestingly, a re-learning experience can be observed. Pereira *et al.* showed learning and forgetting ability in IGZO memristors, shown in **Figure 2.6(a)**, where faster re-learning and harder forgetting with repetition, just like in the human brain, was observed.[42]

Paired-pulse facilitation and depression (PPF/PPD) are other common tests to elaborate on short term synaptic plasticity. The PPF/PPD index is calculated as the relative current difference between single and double spikes ($(I_2 - I_1)/I_1$), with different pulse intervals in double spikes. Ismail *et al.* demonstrated, in a double layer ZTO/ZrO_2 memristor, that the shortest interval presented a PPF of 183% while the longest interval induced 18% PPF,[83] which is in agreement with the phenomenon of biological synapses. Later, the authors also demonstrated PPF and PPD on a single-layer ZTO device, illustrated in **Figure 2.6(b)**. Once again, the PPF/PPD index decreased/increased exponentially with the

maximum pulse interval. The behavior was explained by fewer VOs drifting back with smaller pulse intervals.[50]

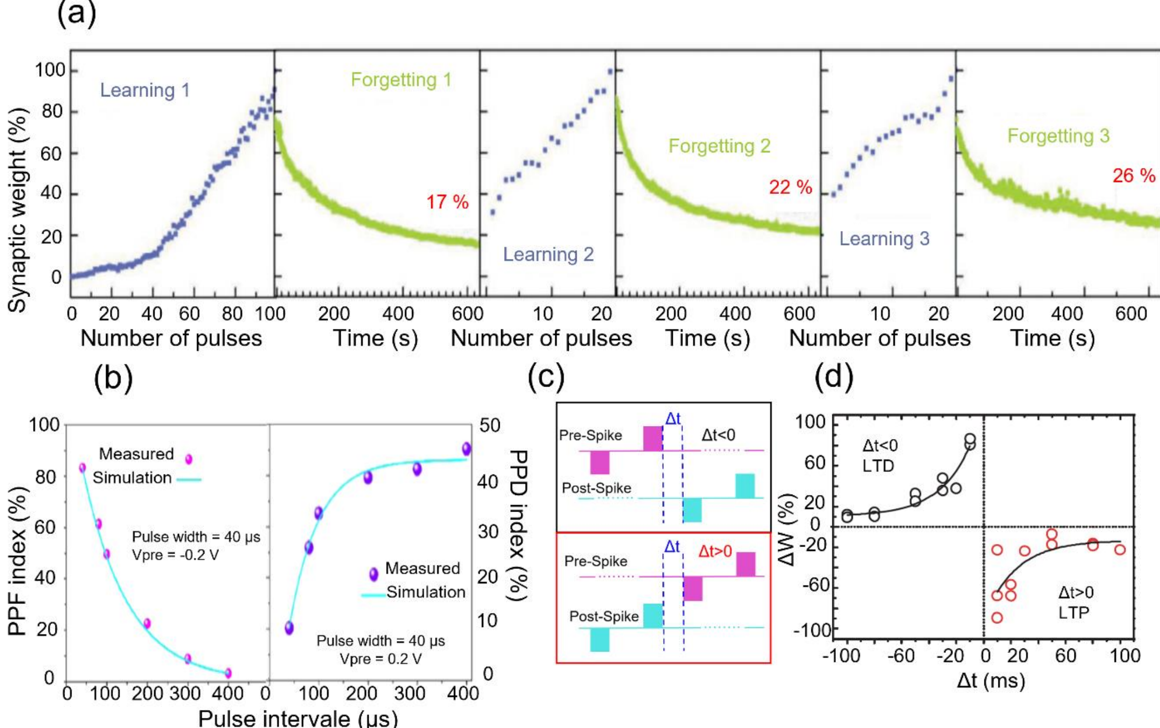

Figure 2. 6 Typical characteristics in AOS-based memristors for SNNs. (a) Learning and forgetting experience emulated in an IGZO memristor. Adapted from ref. 42 with permission from John Wiley & Sons, Copyright © 2020 Wiley-VCH GmbH. (b) PPF and PPD index with different pulse intervals for a ZTO memristor. Adapted from Ref. 50 with permission from Elsevier, Copyright © 2020. (c) and (d) Designed pulse scheme and correspondent STDP characteristic in an IGZO memristor. Adapted from ref. 39 with permission from John Wiley & Sons, Copyright © 2012 Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim.

Perhaps the most important synaptic feature for SNNs is spike-time dependent plasticity (STDP), already accomplished in AOS-based memristors.[53,66,75] Here, the synaptic weight change is modulated by the time difference between pre-synaptic spike, applied to one of the electrodes, and post-synaptic spike, applied to the other electrode. As an example, in **Figure 2.6(c)** is illustrated a simple pulse scheme designed for STDP by Wang *et al.* for the IGZO memristor. The device showed the STDP characteristics presented in **Figure 2.6(d)**, in which a dependence of synaptic weight change (ΔW) and the synaptic time interval (Δt) is clear. ΔW was calculated by the difference between initial and final (after spike-pair application) current states of the device (I_2-I_1), divided by the initial current state (I_1). The smaller Δt, the larger ΔW and the results are well fitted with an exponential function. These are typical STDP characteristics of biological synapses.[39]

The fact that this SNNs advantageous features have been already implemented in AOS-based memristors shows their potential for implementations in SNNs hardware, both with off-chip and on-chip training. However, the field has only witnessed small proof-of-concept demonstrations. New

specifically designed algorithms for SNNs and further studies on devices non-idealities and D2D and C2C variabilities are necessary.

2.3.3 The Crosstalk Challenge and Outlook

One of the most challenging aspects of circuit implementation with memristors is crosstalk. It is related to the sneak-path current interference between different memristor cells in crossbars and often leads to misinterpretation of the output results.[111]

The most practical solution to suppress the sneak-path current is applying a voltage bias scheme (VBS) in which each line and column of the crossbar is given a specific input. In other words, the unselected devices are biased, at top and bottom electrodes, with a fraction of the selected memristor input voltage. The output current of the unselected cells is successfully decreased in small crossbars, implying, however, a significant increase in energy consumption. Devices with extremely high resistance on the HRS and large I_{LRS}/I_{HRS} ratio are also, usually, required.[112] This strategy has been demonstrated with VMM operations in a 10×10 crossbar composed of Al_2O_3/IGZO double-layer memristors, with extremely high efficiency. However, retention data was shown only up 25 s.[113]

Another straightforward method to tackle crosstalk is the realization of self-rectifying memristors, maintaining down-scaling potential at lower cost. The self-rectifying behavior is usually associated with an asymmetry established by a Schottky and an ohmic contact or asymmetric switching oxide and has been demonstrated in IGZO-memristors.[114,115] However, self-rectifying memristors typically show poor endurance due to higher voltage operation, which also diminishes the much-needed energy-efficiency. Moreover, these single-device strategies usually come with worst linearity and symmetry on the plasticity characteristic.

Adding a selector device in each cell of the crossbars allowing individual cell activation is the immediate solution for energy-efficient high performance ANNs hardware. In this regard, a diode can be connected in series with a memristor, in 1-diode-1-memristor configuration (1D1M), resulting in rectifying behavior as described above. However, a high rectification ratio is crucial for sneak-path current elimination in large crossbars. Wu *et al.* reported on an IGZO-based diode, with rectifying ratio of 10^8 at ±1 V, that had been utilized in a 1D1M structure using HfO_2 memristors.[116] A promising upcoming approach would be to pair this IGZO-diode with an IGZO-memristor by changing the IGZO deposition parameters for the memory unit. Towards high density circuitry, pure vertical structure will be beneficial, where a field effect electronic device (transistor as selector) is avoided. AOS composition can be tuned for both diode and memristor.

The transistor, in a so-called 1-transistor-1-memristor (1T1M) configuration, behaves like a switch that when turned on, acts like a high conductance wire and, when turned off, no current reaches the not selected memristor. It allows for improved control on the plasticity characteristic through current input, while providing an on-chip CC, at the expense of cell area in crossbars.

As already explained, AOS materials are also widely used in TFTs. Therefore, 1T1M crossbars can be built where both device elements are fabricated at the same level, providing the necessary conditions for flexible and cost-effective ANN hardware with improved interconnectivity. As such, significant efforts have been made towards the optimization of an AOS layer and electrodes compatible for both devices, which would further reduce the manufacturing cost. However, to use the same AOS layer a trade-off must be ensured in performance, since TFTs should present high-stability and low-leakage current and memristors a defect-enabled switching with high I_{LRS}/I_{HRS} ratio.

Pereira *et al.* showed an optimized IGZO layer compatible with TFTs, by decreasing the oxygen content during deposition, lowering the RS ratio. The authors show a working TFT fabricated using the same IGZO and electrode layers as the memristor, but did not show 1T1M cell functionality at that point.[108] Later, in a more recent paper, the group presented the first flexible 4×4 1T1M crossbar using the same layers for the fabrication of both devices. Moreover, this IGZO crossbar did not suffer from the crosstalk problem.[117] The IGZO 1T1M has been demonstrated by other works, where one of the TFT electrodes was utilized for the bottom contact of the RS device, and the switching oxide is suited for both elements.[118,119] Although this shows tremendous potential, the RS devices proposed showed abrupt behavior with binary states, which significantly limits their range of applications in neuromorphic computing. Similarly, Fan *et al.* showed an AZTO-based 1T1M cell with binary states, in which the AZTO layer was different for each device element.[120] In a later study, a thin layer of HfO_2 was added to the RS device which allowed for 1T1M cell with MLC characteristics displaying 4 distinct states.[121] On solution-based technology, AZTO films were also optimized for memristor and TFT compatibility, but a 1T1M cell was not yet shown.[98]

Finally, optoelectronic memristors can be implemented as a more drastic path to solve sneak-path current issue. In these devices, light serves as an extra degree of control on crossbars and can be used to select the desired cells, through light potentiation, or to force a Reset in unselected cells, see **Figure 2.7(a)**.

Due to their inherent transparency, several AOS materials are used as electrodes in their most conductive forms for optoelectronic RS devices.[122–125] As active layers, Hu *et al.* could control both Set and Reset operations thought blue and near-infrared (NIR) light pulses, respectively, as illustrated in **Figure 2.7(b)**. The memristor structure consisted in a transparent 30 nm ITO layer and 10 nm Au for top electrode which provided a transmittance of >55% for 400 to 1000 nm light wavelengths,[126] and a double-layer IGZO. The plasticity characteristic and STDP test is demonstrated in **Figure 2.7(c)** and **2.7(d)** and shows the device capability to emulate synaptic functions by only light control. However, switching ratio appears to be small and should be improved for high accuracy in neuromorphic activities.

A 3×3 optoelectronic crossbar was developed by Song *et al.* using IGZO/Al_2O_3 as active layer and ITO as top electrode. Here, potentiation and depression in STDP were achieved by UV light and

electrical pulses, respectively. The work reported that the synaptic weight of each memristor on the crossbar could be tuned separately and summed, obtaining a crosstalk-free crossbar.[127]

Moreover, ZTO memristors have also proven its capabilities as an optoelectronic device. Blue light has been shown as the precursor for photonic potentiation coupled with electrical depression.[109] The reverse, electrical potentiation and photonic depression, was demonstrated with blue, green and red light pulses.[76,128] A photonic Reset was carried out with blue light pulses with very little C2C variation, **Figure 2.7(e)**. Moreover, different wavelengths can provide different current states, as demonstrated in **Figure 2.7(f)**. As all these studies are very recent, further work is required on large crossbars implementation to determine the feasibility of optoelectronic memristors in eliminating crosstalk.

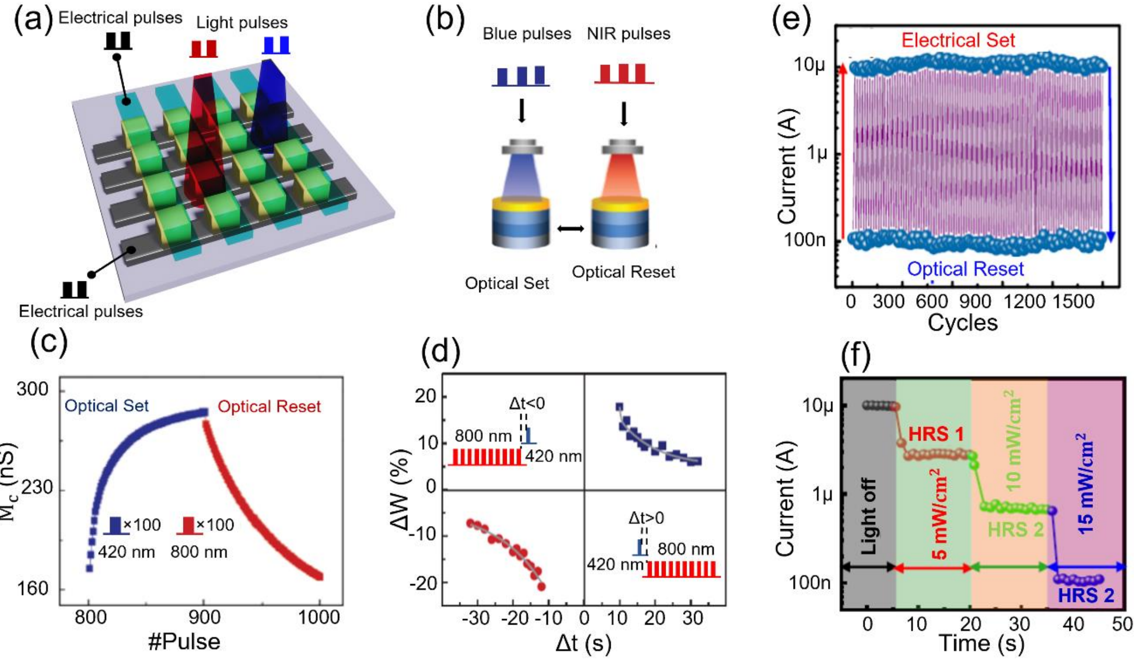

Figure 2. 7 Optoelectronic memristor as a strategy to eliminate crosstalk on crossbars. (a) Illustration of optoelectronic crossbar. (b) Illustration of combined blue and NIR pulses for Set and Reset, respectively, correspondent to (c) potentiation and depression results and (d) STDP demonstration in a double-layer IGZO memristor. Adapted from Ref. 126 https://doi.org/10.1002/adfm.202005582, under the terms of the CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/. (e) cycles of electrical Set and optical Reset and (f) variation of current state with red, green and blue light pulses. Adapted from Ref. 76 with permission from American Chemical Society (ACS), Copyright ©2022.

2.4 Conclusions and Remarks

The conductivity of AOS-materials can be precisely tuned by deposition parameters, both with sputtering and solution-based tools, and thus they can act as active layer and electrodes in RS devices with controlled switching behavior. This class of materials also present high flexibility with

conventional patterning strategies and low-processing temperature, which allows the use of low-cost flexible substrates for flexible neuromorphic technologies with the potential to replace the Von Neuman's architecture.

Evidently, developing an appropriate device should consider the envisioned neuromorphic application. In AOS-based memristors, filamentary-type RS is usually coupled with long retention times suited for in-memory computation and DNNs, while interface-type RS shows lower switching ratios and relaxation of states behavior appropriate for SNNs. MLC operation is possible in filamentary RS, by applying different CCs during Set and different stop voltages during Reset, combining multiple resistive states with retention data, which shows tremendous potential for neuromorphic applications. However, D2D and C2C variabilities are higher when compared to fully analog interface-type RS devices.

Double-layer AOS memristors provide additional improvement regarding I_{LRS}/I_{HRS} ratio, D2D and C2C reproducibility and retention properties for both types of RS. A systematic study on the effect of AOS composition ratio and oxide thickness in RS behavior is lacking in the literature and could further enhance RS behavior.

Several strategies have emerged to adjust the memristor performance to specific applications. For DNNs, the most challenging aspect of employing AOS-based RS devices is the required linearity and symmetry on the plasticity characteristic with simple pulse scheme, coupled with long retention data for each state. The double-layer approach is the most promising one to achieve such performance in a filamentary-type RS device with MLC operation. On the other hand, SNNs applications require relaxation of states dependent on input repetition and timing. For this, fully analog memristors can be employed. Several learning rules such as re-learning, transition from STM to LTM, PPF, PPD and STDP have been shown in AOS-memristors. For both computing paradigms, very little circuit implementation has been demonstrated and only small crossbars were accomplished suggesting that D2D and C2C variabilities and endurance need special attention. New algorithms should also be developed that consider devices non-idealities and noise introduced by down-scaling.

Moreover, the fundamental challenge blocking large-scale implementation of ANNs hardware is sneak-path current in crossbars. The most promising approaches to eliminate it are i) the 1T1M configuration, providing individual cell activation through a transistor at the expense of cell area, and ii) the development of optoelectronic memristors, in which light is used for individual control of the cells. AOS materials are the ideal candidate for such proposals since: i) in the 1T1M configuration they can be used for both TFT and memristor manufacturing, offering a cost-effective and simple solution and ii) AOS materials are transparent and very responsive to different wavelengths of light. The field is still at its infancy, but some small proof-of-concepts were already realized with AOS-based memristors for both strategies showing no interference between cells. Further work is required in developing memristor features towards circuit implementation that meets all the requirements for specific neuromorphic applications.

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CHAPTER 3

IGZO-BASED MEMRISTORS FOR NEUROMORPHIC APPLICATIONS

Amorphous indium-gallium-zinc-oxide (a-IGZO) based memristive devices with molybdenum contacts as both top and bottom electrodes are presented aiming to be used in neuromorphic applications. Devices down to 4 μm^2 are fabricated using conventional photolithography processes, with an extraordinary yield of 100%. X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) performed on the developed structures confirm the presence of a thin intermixed oxide layer (4–5 nm) containing Mo^{6+} oxidation state at the interface with the bottom contact. This results in Schottky diode like characteristics at the pristine state with a rectification ratio of 3 orders of magnitude. The devices have electroforming-free and area-dependent analog resistive switching properties. Temperature analysis of resistive switching I–V data reveals barrier height variations of the junction. Several synaptic functions, such as synaptic potentiation and depression as response to programmed pulses, short- to long-term plasticity transition (STP to LTP) and "learning experience" properties are presented. The Mo/IGZO/Mo memristive device shows potential application of an electronic synapse for brain inspired computing application. Integration in System-on-Panel (SoP) architectures is possible at negligible cost, because all materials are used in commercial IGZO thin-film transistor (TFT) fabrication.

The results presented in this chapter are published in:

M.E. Pereira, J. Deuermeier, R. Nogueira, P.A. Carvalho, R. Martins, E. Fortunato and A. Kiazadeh, "**Noble-Metal-Free Memristive Devices Based on IGZO for Neuromorphic Applications**", in Advanced Electronic Materials, vol 6, 10, 2000242, 2020

3.1 Introduction

Memory technologies have been intensively studied in the past years and are of great interest to the nowadays world where technology is everywhere. Currently, it is the Von Neumann's architecture that is applied to the electronic computing systems in which the different elements (memory, processor, and controller) are separated.[1] Nearly all the circuits within the memory and the processor are composed of complementary metal–oxide– semiconductor (CMOS) devices, which can be a problem once this technology cannot be further miniaturized without compromising its performance.[2] A practical example could be that in order to increase the operating frequency and the device density, which is necessary when downscaling, the power supply and the operation temperature would also increase, which would obviously degrade the system performance. Moreover, the Von Neumann system is not suited to solve real world problems where inputs and outputs are sometimes not specified[3] or to execute adaptive learning algorithms as it would be necessary in tasks, such as classification of unstructured data or pattern recognition.[4]

To overcome the Von Neumann's bottleneck, the development of artificial intelligence (AI) technologies and new computer architecture designs are necessary. One of such novel approaches is neuromorphic computation, which operates with extremely low power consumption. It also maintains the massive parallelism found in the human brain[5] where neurons communicate information by electrical or chemical input signals passing through synapses. Synapses present a very important behavior called plasticity which consists in changing their strength (synaptic weight), either facilitating or inhibiting the connection between two neurons, through potentiation and depression, respectively.[6] One of the solutions to emulate biological synapses is the resistive switching (RS) device, or memristor.

A memristor is basically a nonlinear two-terminal device whose conductance can be altered by external inputs and depends on the history of current that has flowed through the device. Application of both weight programming and weight processing signals are through its input terminals thus mimicking a synapse. In fact, the memristor can simulate the synapses' plasticity by continuously adapting its resistance into excitatory and inhibitory weights upon application of electrical pulses. Furthermore, the analog controlling of the resistance states lead to extraordinary high-density processing and storage for brain-inspired neuromorphic computing.[7]

Amorphous oxide semiconductors (AOS) are promising as RS materials due to the great advantages they offer in terms of their high performance,[8] excellent stability,[9] easy and low cost manufacturability, and compatibility with CMOS processes. The lack of grain boundaries allows for a device miniaturization to the nanometer scale and therefore enables high-density circuit integration.[10] Furthermore, the electrical conductivity of an AOS film can be controlled over 8 orders of magnitude by regulating the oxygen/cation composition,[11,12] making it suitable for a dynamic response to input signals, just like in the biological synapse. Nevertheless, AOS are less studied than the conventionally used

materials, such as Al_2O_3,[13] HfO_2,[6,14,15] or TaO_x[16,17] due to the fact that for a filamentary type of switching, there is no significant advantage in using another type of material.

However, for the construction of a reliable neuromorphic system, the area-dependent analog switching has certain advantages over the filamentary type. When the RS occurs due to a local and random effect where only a few oxygen vacancies (VOs) and ions contribute to the switching event in establishing and rupturing localized conductive filaments (CF), the device reliability is dependent on the reproducibility of the filament formation.[18] The randomness of the filament formation increases device-to-device (D2D) variability,[19] which significantly limits the number of physical circuit implementations of memristors.[20] Furthermore, pattern recognition accuracy of area-dependent systems is higher due to a lower random telegraphic noise than in filamentary systems.[21] We note that this issue is not presented for devices where the electrode area is confined to the conductive filaments area.[22] In the area-dependent type, the RS could either involve the homogeneous migration of defects or ions through the thickness of the switching matrix,[23] or comprise an exchange of ions (or charge trapping) at the interface between the switching matrix and the electrode[24] and thus there is a homogeneous contribution of VOs and ions throughout the entire area which results in better D2D reproducibility and cycle-to-cycle (C2C) uniformity.[25]

In fact, the area-dependent RS have been already demonstrated on devices using AOS films as active layer namely zinc oxide materials for instance ZnO[26,27] and ZTO.[28] IGZO-based devices with abrupt/gradual switching characteristics using metal electrodes, such as Pt, Al, and Cu, have previously been studied by few different research groups.[16,29–35] In most of the studies emerged on IGZO-based memristors for neuromorphic applications[36,37] so far it is understood that the oxygen concentration plays an important role when it comes to achieving a tunable device.[38]

Two different approaches can be followed to control the asymmetry in the memristor structure: the oxygen gradient can be built into the structure by changing the stoichiometry of the oxide during deposition[15] or a reactive electrode can be used that will be oxidized at the interface and in turn will reduce the switching oxide in the region close to the oxide/electrode interface.[39–41]

Here, we report for the first time IGZO-based memristive devices that use molybdenum both as top and bottom electrodes, in which the current is controlled by a potential barrier and the switching involves changes to the barrier characteristics. A device with such a behavior has been termed a memdiode and a corresponding model was presented.[42,43] We show that the diode-type characteristics is a result of oxidized molybdenum at the interface with the bottom electrode. Molybdenum was chosen for the electrodes to facilitate integration with high performance IGZO-based thin-film transistor (TFT), which use molybdenum as source and drain electrodes.[44] The device reveals retention loss mimicking the memory loss in biological system,[45] similar to synapses with various time-scale dynamics. The concept of “fast weight” was proposed in 2016[46,47] meaning that the synaptic weight does not require “erasing weight” into forget processing. This property is beneficial for artificial neural networks (ANNs) in sequence-to-sequence models. We demonstrate the synaptic behavior of the devices

through potentiation and depression, short-term to long-term memory transition (STM-LTM) and by simulating the learning process. The presented results demonstrate that the Mo/IGZO/Mo memristive device can be integrated on crossbar structures as previously achieved with other materials[48,49] and/or joined with IGZO-based TFTs for neuromorphic hardware systems. The area dependency and forming free performance allow to employ low-cost fabrication methods and conventional patterning strategies. Together with the low processing temperature, this facilitates the use of unconventional substrates (like plastic and paper), which is fundamental for Internet-of-Things (IoT) applications.

3.2 Experimental

The memristive devices were fabricated on glass substrates that were previously cleaned in subsequent ultrasonic baths of acetone and isopropanol, methanol, followed by rinsing with deionized water and dry nitrogen. In **Figure 3.1(a)**, a schematic of the memristive device structure is presented.

For the bottom and top electrodes, a 70 nm thick molybdenum layer was deposited by radio-frequency (RF) magnetron sputtering in an AJA ATC-1800 system with a flow rate of 50 sccm of Argon, a sputtering power of 175 W, and a deposition pressure of 1.7 mTorr. The sputter deposition method was selected because it guaranties a good uniformity on large areas and a precise control of the oxygen amount which allows to regulate the oxygen content of the material.[50]

As the active layer, a 30 nm thick IGZO thin film was deposited also by RF magnetron sputtering, in the same system, using a flow rate of 20 sccm of Argon and 20 of Oxygen with an RF power of 160 W and a deposition pressure of 2.3 mTorr. An oxygen plasma treatment was carried out to the bottom electrode immediately before the IGZO deposition. The parameters used during this plasma treatment were a flow rate of 20 sccm of oxygen gas with 10 W of substrate bias and an RF power to the IGZO target of 40 W for 10 min. All the depositions were done without intentional substrate heating.

As a part of the optimization of the memristor performance, co-sputtering from three binary ceramic oxide targets was also performed. The sputtering powers used on each target were In_2O_3: 121 W, Ga_2O_3: 100 W, and ZnO: 50 W, aiming for the same composition as in case of the single target deposition (IGZO 211). All other deposition conditions were kept the same as for the single-target IGZO deposition.

The patterning of the electrodes was achieved by reactive ion etching in a Trion Phantom 3 system, using SF_6, whereas the semiconductor etching was done by wet etching using a 1:20 solution of $HCl:H_2O$.

The I–V characteristics of the devices were extracted using a Keithley 4200 SCS semiconductor analyzer connected to a Janis ST-500 probe station. The voltage was applied to the top electrode maintaining the bottom electrode connected to ground. The speed of the measurements was at normal mode and the integration time was in autosetting, which allows the system to optimize its value based on the range and other conditions. Both hold and delay time were zero and the step was 0.1 V.

The XPS measurements were done with a Kratos Axis Supra spectrometer. A monochromated Al Kα source was run at 300 W. An aperture of 110 µm was used, and the analyzer was set to a pass energy of 40 eV. Argon clusters of 500 atoms with a kinetic energy of 10 keV, scanned over 1.5 × 1.5 m^2, were used for depth profiling. The data were analyzed with CasaXPS.

STEM of the device cross-sections was carried out at 300 kV with an FEI Titan G260-300 instrument equipped with a DCOR probe Cs-aberration corrector and a Super-X Bruker energy dispersive spectrometer with 4 silicon drift detectors. Imaging was performed with a probe current of ≈100 pA and nominal spatial resolution of 0.08 nm. The samples were prepared by focused ion beam (Ga^+) with an FEI Helios G4 dual-beam instrument.

3.3 Results and Discussion

3.3.1 As-fabricated devices

The device structure is represented in **Figure 3.1(a)**. This includes a scanning tunneling microscopy (STEM) image of the device cross-section, using the high angle annular dark field (HAADF) detector. The first I–V curve in the range of −1 to +1 V is called the pristine state. The rectifying I–V characteristics of pristine devices with different areas are shown in **Figure 3.1(b)**. On the left, devices are shown where the IGZO layer was deposited from a single target, whereas for the devices on the right, the IGZO layer was deposited by co-sputtering of three binary ceramic oxide targets. Both types of IGZO depositions lead to rectifying I–V characteristics, but the co-sputtered devices are more resistive than the single-target ones. The current density versus voltage plots are presented in **Figure A.1 - Appendix A**. Further electrical results presented throughout this paper are in regard of devices with an area of 4 μm^2 if not pointed out otherwise.

It is important to note that even if the device has a symmetric structure (two Mo contacts and an IGZO middle layer), the I–V curves are rectifying, related to a limited electron injection at the bottom interface. To understand the origin of the rectification, STEM and X-ray photoelectron spectroscopy (XPS) results of the interface between single-target IGZO and the bottom contact are presented in **Figure 3.1(c)–(f)**. The HAADF images with the energy dispersive spectroscopy (EDS) signals from the constituent elements are shown in **Figure 3.1(c)**. The dark region at the interface is related to a lower density of the interfacial layer compared to the IGZO layer (this will be commented further below). The thickness of the interfacial layer was determined to be 4–5 nm. The EDS maps show that the interfacial layer contains small amounts of indium, gallium, and zinc, a high amount of oxygen and also molybdenum. This information is summarized in a line profile shown in **Figure 3.1(d)**. In **Figure 3.1(f)**, XPS together with argon cluster depth profiling was employed to determine the oxidation state of molybdenum at the bottom interface of IGZO. This measurement was performed on a Mo/IGZO structure, without the molybdenum top contact. When the first molybdenum signal is encountered at the

interface between IGZO and molybdenum (after 150 and 180 s), the main oxidation state corresponds to Mo^{6+} (Mo $3d_{5/2}$ at 232.3–232.7 eV).[51] Besides the absolute binding energy, the characteristic energy separation of the Mo 3d doublets (3.13 eV) allows to conclude, that the main contribution to this emission is Mo^{6+}. With additional etching, the oxidation state is gradually reduced, which is both related to the tendency of MoO_3 to be reduced under X-ray exposure[52] and the reducing effect of the argon beam. Hence, the interface layer contains more Mo^{6+} than our measurements can detect. Considering that the interfacial layer has a high content of MoO_3, the mass densities can be compared to explain the contrast in the HAADF image of **Figure 3.1(c)**: The density of MoO_3 is significantly lower (4.7 g cm–3)[53] than of IGZO (6 g cm^{-3}).[54]

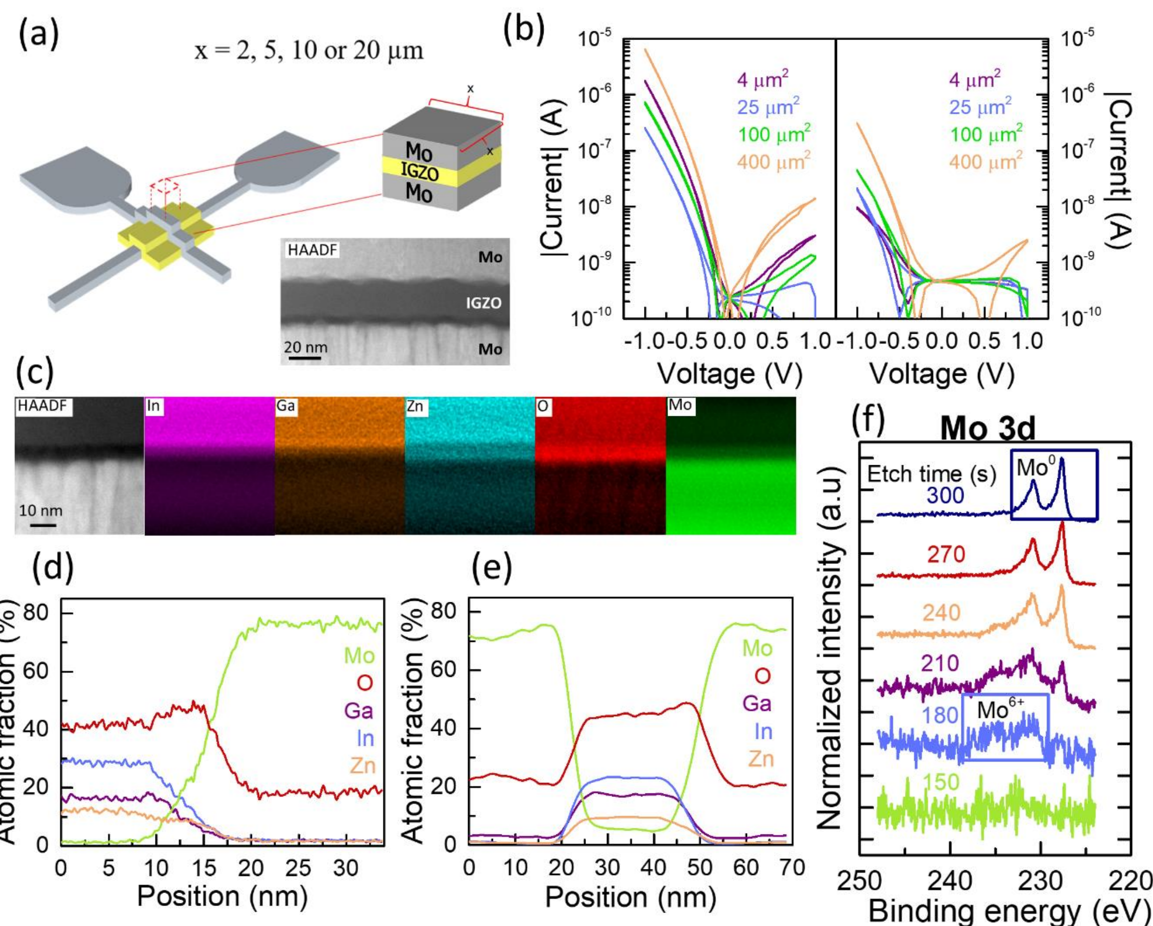

Figure 3. 1 As fabricated Mo/IGZO/Mo structures I-V characteristic and material characterization for single-target and co-sputtering IGZO. (a) Schematic illustration of the Mo/IGZO/Mo structure with a STEM cross-section. (b) I–V characteristic between −1 and 1 V of the diodes with different areas, left: single-target IGZO, right: co-sputtered IGZO. (c) STEM bright field image and EDS maps of the IGZO bottom interface. (d) Atomic fraction with respect to position (from IGZO to Mo bottom electrode), obtained from the EDS data cubes. (e) Atomic fraction from EDS throughout the whole device stack. (f) XPS argon cluster depth profiling through a Mo/IGZO structure.

Besides the interface region at the bottom contact, the composition of the IGZO layer in the Mo/IGZO/Mo device was analyzed by additional STEM measurements: **Figure 3.1(e)** shows the elemental composition profile throughout the device thickness obtained by STEM. A uniform cation distribution is observed as well as an increased oxygen content towards the bottom interface. The latter corroborates with the lower conductivity of the IGZO at the electron barrier present at the bottom interface.

In conclusion, the XPS and STEM results provide the explanation for the rectification observed in **Figure 3.1(b)**: When the Mo bottom contact is subjected to the oxygen plasma treatment and during the subsequent IGZO deposition in the oxygen containing reactive process gas, an interfacial layer of 4–5 nm is formed, which contains highly oxidized molybdenum. Due to the high work function of MoO_3, a depletion region is formed in the IGZO close to the bottom contact, which creates an electron barrier at this contact. In addition, the inhomogeneous oxygen distribution causes the IGZO to be more conductive at the top contact than at the bottom contact. This influences the electron injection into the IGZO, being facilitated by the high doping at the top, and hindered by the low doping in the bottom.

3.3.2 Analog switching characteristics

The typical analog behavior of the Mo/IGZO/Mo devices is shown in **Figures 3.2(a)** and **3.2(b)**. The memristive devices can be programmed to higher conductance states by application of negative voltages up to −3 V in the forward direction of the pristine diode. By application of successive DC sweeps on negative and positive polarities, the device conductance is gradually increased and decreased, respectively.

Figure 3.2(a) is in regard of samples in which IGZO was deposited from a single target, while **Figure 3.2(b)** presents the analog behavior of devices with a co-sputtered IGZO layer. The results regarding the relation between the resistance states and the device area is shown in **Figure 3.2(c)** for co-sputtered IGZO devices. It can be concluded that there is a clear linear relationship where the resistance decreases with the increase of the area, confirming our assertion that the present switching is area-dependent. The area-dependency of the single-target IGZO is also shown in **Figure A.2- Appendix A**. The current at 0.1 V after application of different pulse schemes (−1.5 V/100 ms, −2V/50 ms, −2V/100 ms) can be found in **Figure 3.2(d)**. Longer pulse widths and higher pulse durations increase the conductance change. For this reason, the combination of −2 V with 100 ms pulse width was chosen for the synaptic tests.

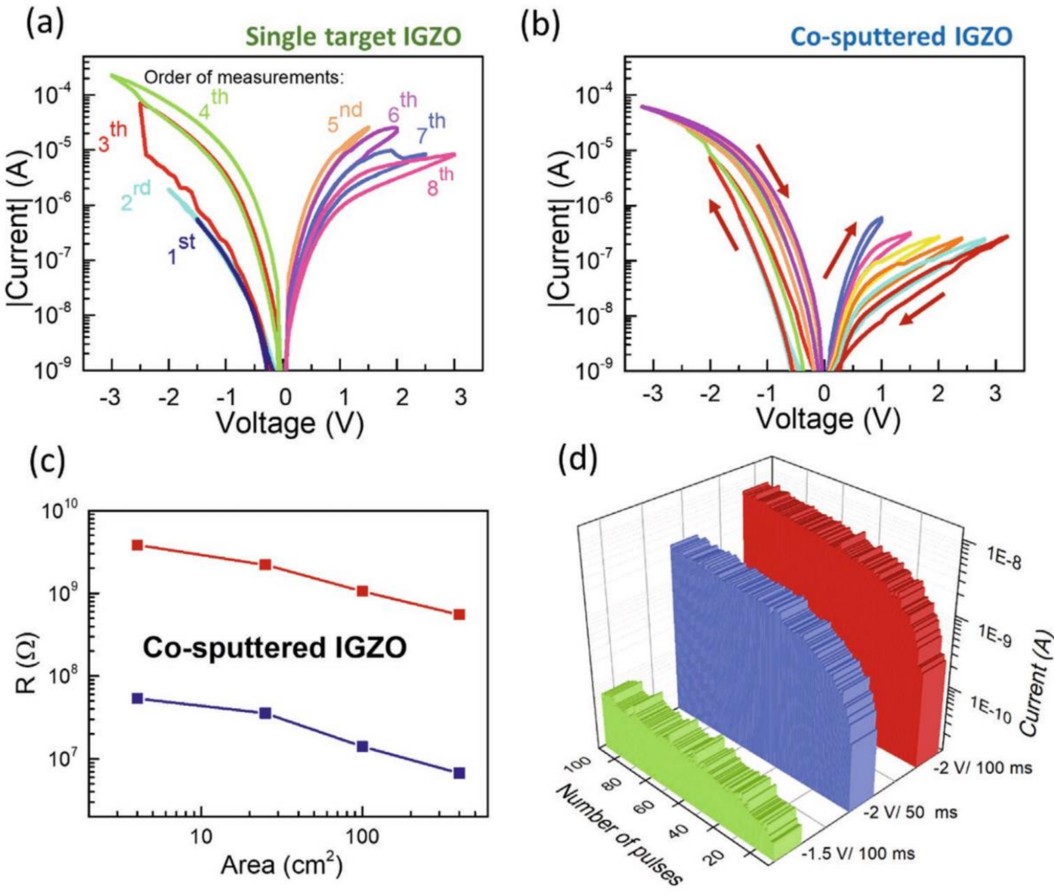

Figure 3. 2 I–V characteristics showing analog behavior by gradually changing voltage sweep span of (a) IGZO memristor deposited with a single target approach and (b) IGZO memristor deposited by co-sputtered approach. (c) Maximum and minimum resistance change versus device area of co-sputtered IGZO. (d) Current read showing the change of conductance states at 0.1 V after application of different pulse schemes (−1.5 V/100, −2 V/50, and −2 V/100 ms). Longer pulse widths/higher pulse duration increase the conductance levels.

3.3.3 Synapse behavior

In **Figure 3.3(a)**, a schematic of the artificial synapse alongside the biological one is shown. The synaptic weight is related to the conductance state of the memristive device. Synaptic plasticity implies facilitating or inhibiting the connection between two neurons, through potentiation and depression steps. To create both situations, negative/positive pulses are used to excite/inhibit the synapse. The programmed pulse amplitudes and width is ± 2 V pulse and 100 ms, respectively, as can be seen in **Figure 3.3(b)**. **Figure 3.3(c)** shows the conductance response to a series of negative pulses (potentiation) immediately followed by positive pulses (depression), under a 0.1 V voltage read, for the co-sputtered IGZO device with an area of 4 μm^2. The potentiation and depression results of single-target IGZO are shown in **Figure A.3 - Appendix A**. An ideal artificial synapse should present a linear and

symmetric change in conductance under constant applied pulses for maximum accuracy, due to the nature of the algorithms used in neural networks (backpropagation algorithm) in pattern recognition.[55] However, the nonlinear response is not a serious issue thanks to learning algorithms which are dynamic and self-adjusting to errors in synapse programming.[56]

The learning process in biological systems is established by the modification of synaptic weight or the plasticity mechanism, categorized as short-term and long-term memory. What researchers call a short-term memory is a small amount of information which the brain holds for a short period of time (not more than 30 s).[57] On the other hand, long-term memory does not mean an everlasting retention time in the brain, hence anything longer than 30 s would qualify.

Quantitatively, it is appropriate to fit the memory retention loss of the device with a stretched-exponential function (SEF) which has been already described as suited for this type of application.[58] SEF, also known as the Kohlrausch law, is written as followed in **Equation (3.1):**

$$\varphi(\mathrm{t}) = I_0 exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] \quad (\mathbf{3.1})$$

where φ (t) is the relaxation function, τ is the characteristic relaxation time, I_0 is initial current state, and β is the stretch index ($0 < \beta < 1$). Analyzing **Equation (3.1)**, it can be concluded that while $t < \tau$ an abrupt drop will be in place, followed by a much slower decay when $t > \tau$, which resembles the human memory behavior.[59] In order to demonstrate the resemblance between the dynamic memory retention of the resistance states of the memristive device and that of the human memory, we performed a test in which a 30 min retention at 0.1 V read would be realized after different numbers of pulse stimulations (100, 80, 50, 30, and 10). The pulses are of −2 V with 100 ms duration. The results can be found in **Figure 3.3(d)** where a perfect fitting with **Equation (3.1)** is also presented. The fitting parameters are plotted in **Figure 3.3(e)**. Both the relaxation time constant and the initial normalized current is increasing with the number of pulses meaning that the dynamic retention can be increased by repeating stimulations, corresponding to the transition from STM to LTM. Moreover, the stretch index remains fairly the same at 0.4 meaning the trap distribution is not altered upon increasing number of pulses.

Interestingly, the STP upon repeated rehearsals can transition to LTP, a process known as "learning." Learning is the fundamental process for adaptation on living beings and is also a core characteristic for neural networks. To demonstrate that the IGZO-based artificial synapse can perform learning processes, the following test was implemented, and the results are presented in **Figure 3.3(f)**.

First, 100 pulses of −2 V (100 ms width, 10 ms interval) are applied to simulate the first learning process. After this, a memory retention of 640 s is performed, the read voltage is 0.1 V. By the end of this time, the device seems to "remember" 17% of the signal. Immediately after this process, another set of pulse stimulations are carried out as the second learning. Each learning is followed with another

memory retention record of 640 s. During the second learning, only 20 pulses are required to reach the same current state as after the first learning and after the second forgetting process the device remembers 22%. The same experiment of third learning was carried out and after 20 pulse stimulations the synaptic weight is 100% and again on the third retention the device remembers more than before (26%). As a result, fewer pulse stimulations are required for memory recovery indicating an "easier relearning" and "harder forgetting" similar to the human brain. **Figure A.4 - Appendix A** shows the "learning" test of single target IGZO devices.

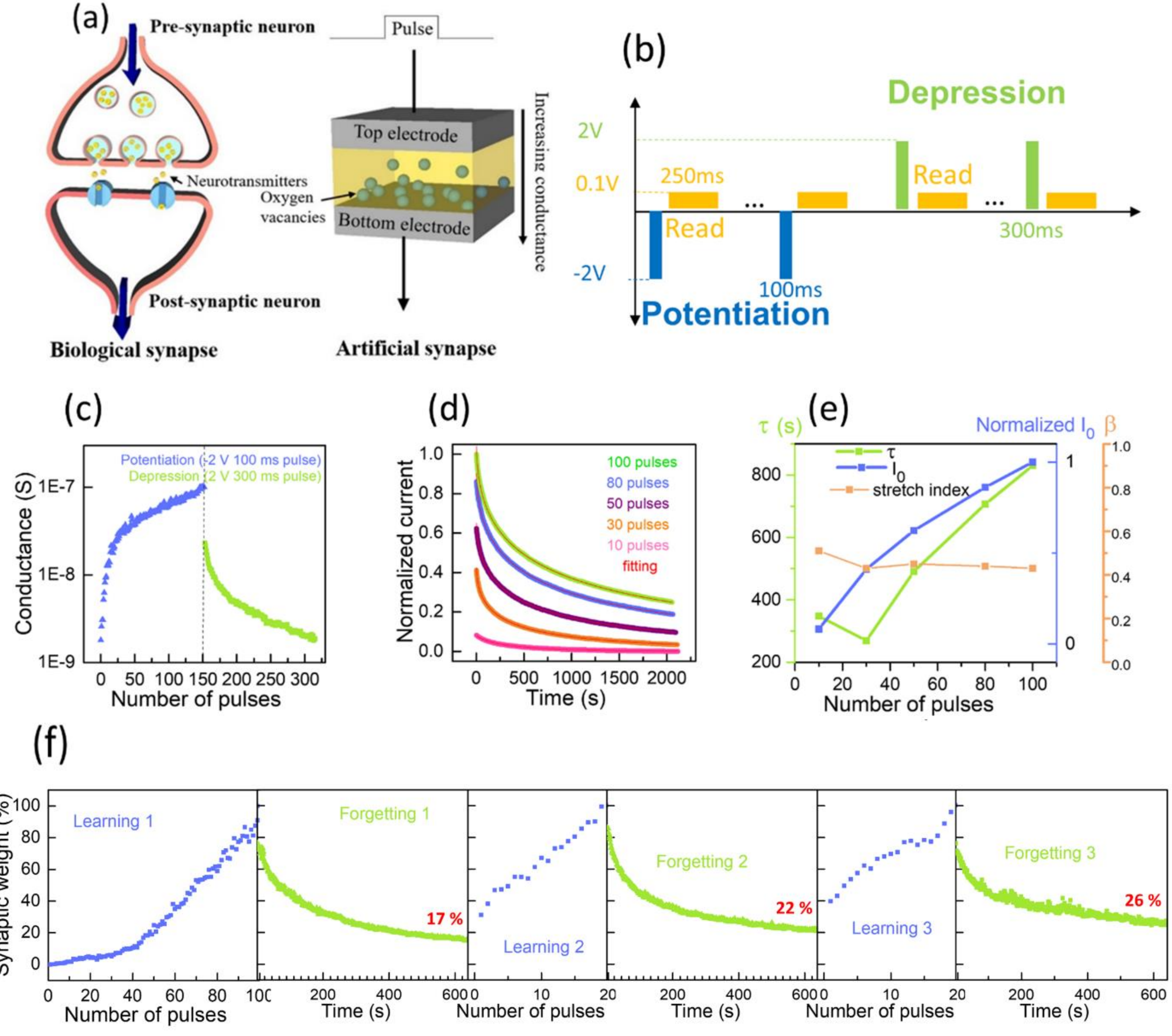

Figure 3. 3 Synaptic behavior of the memristors. (a) Schematic illustration of the implementation of the synapse devices in bioinspired neuromorphic systems. (b) Pulse scheme with the positive (green) and negative (blue) bias responding to depression and potentiation respectively. (c) Conductance change with negative (potentiation)/ positive (depression) pulses of co-sputtered IGZO device. (d) Typical retention for 30 min after different number of pulses applied. e) Fitting results showing relaxation time and initial current state change with number of applied pulses and f) synaptic weight change in percentage with number of pulses for learning 1, learning 2, and learning 3 with their retention after each potentiation.

3.3.4 Fitting According to Thermionic Emission Model

The diode characteristics (forward direction, i.e., only the negative voltage regime) of the devices from the single-target IGZO deposition are fitted based on the thermionic model[60] presented in **Equation (3.2)**:

$$J = A^* \times T^2 exp\left(\frac{-\Phi_B}{k_B T}\right) \times \left[\exp\left(e\frac{V - R_S I}{\eta k_B T}\right) - 1\right] + \frac{V - R_S I}{AR_p} + \frac{I_C}{A} \qquad (\mathbf{3.2})$$

where η is the ideality factor, k_B is the Boltzmann constant, T is the absolute temperature, A* is the effective Richardson constant, A is the device's area, Φ_B is the effective barrier height, V is voltage, R_S is the series resistance, R_p is the parallel (shunt) resistance, and I_C is the parallel capacitance current due to charging and discharging of trap states. The fittings had root mean-square-errors of 1×10^{-6} A or lower and R^2-values above 0.99 996. For the I–V curve of pristine state, a barrier height of 0.57 eV and an ideality factor of 6.17 were obtained. Several possible reasons may result in nonideal diode properties (η > 1), such as barrier inhomogeneity due to defects distribution, presence of an insulating layer at the interface which causes voltage-dependence of the barrier height and tunneling effects.[61] The transition between different states is not entirely clear. However, in order to shed light on different conductance states, DC current sweeps in the range of resistive switching at different temperatures were performed. The maximum temperature tested was 440 K to ensure no atomic rearrangement of the device as it has been proved by previous studies that no significant change on electrical properties of IGZO films occurs until 473 K annealing.[62] The maximum conductance change corresponding to the voltage ramp-up between 0 and −3 V and the voltage ramp-down between −3 and 0 V on the forward direction was selected for temperature analysis. Accordingly, the two branches of the I–V curve are referred to as forward ramp up (F-up) and forward ramp down (F-down). The data are shown in **Figure 3.4(a)**. The temperature dependence of the effective barrier height and the ideality factor is shown in **Figure 3.4(b)**. The F-up shows higher ideality factors and effective barrier heights compared with the F-down. Based on the model of Werner[63] $\Phi_B^{eff} = \Phi_B^m - \sigma_B^2/2k_B T$, the mean barrier value (Φ_B^m) is calculated, and its Gaussian distribution is obtained by the standard deviation (σ_B). Note, that the effective barrier height is lower than the mean barrier potential since the charge carriers only pass through the local minima of the barrier height. The temperature dependence of the ideality factor was calculated using **equation (3.3)**:

$$\eta = \frac{1}{1 - \rho_2 + \rho_3/2k_B T} \qquad (\mathbf{3.3})$$

where ρ_2 and ρ_3 express the voltage dependence of the mean barrier and the square of the standard deviation for Schottky contacts. For most of the Schottky contacts ρ_3 is negative and ρ_2 is positive as

reported for IGZO diodes.[64] The mean barrier height and standard deviation are higher for the F-up than for the F-down. The results are summarized in **Table 3.1**. Considering the ratios between standard deviation and mean barrier height, almost no variation can be observed (18% for F-up and 20% for F-down). In Pt/ZTO diodes, the mean barrier height and standard deviation increase in a similar fashion, when an additional semi-insulating layer at the Schottky contact is inserted.[60]

Table 3. 1 Voltage dependence of the mean barrier (ρ_2), square of the standard deviation for the Schottky contacts (ρ_3), mean barrier potential (Φ_B^m) and standard deviation of the mean barrier potential for F-up and F-down.

	ρ_2 [a.u]	ρ_3 [meV]	Φ_B^m [eV]	σ_B [eV]
F-up	0.45	-23	1.1	*0.20*
F-down	**0.60**	**-16**	**0.8**	***0.16***

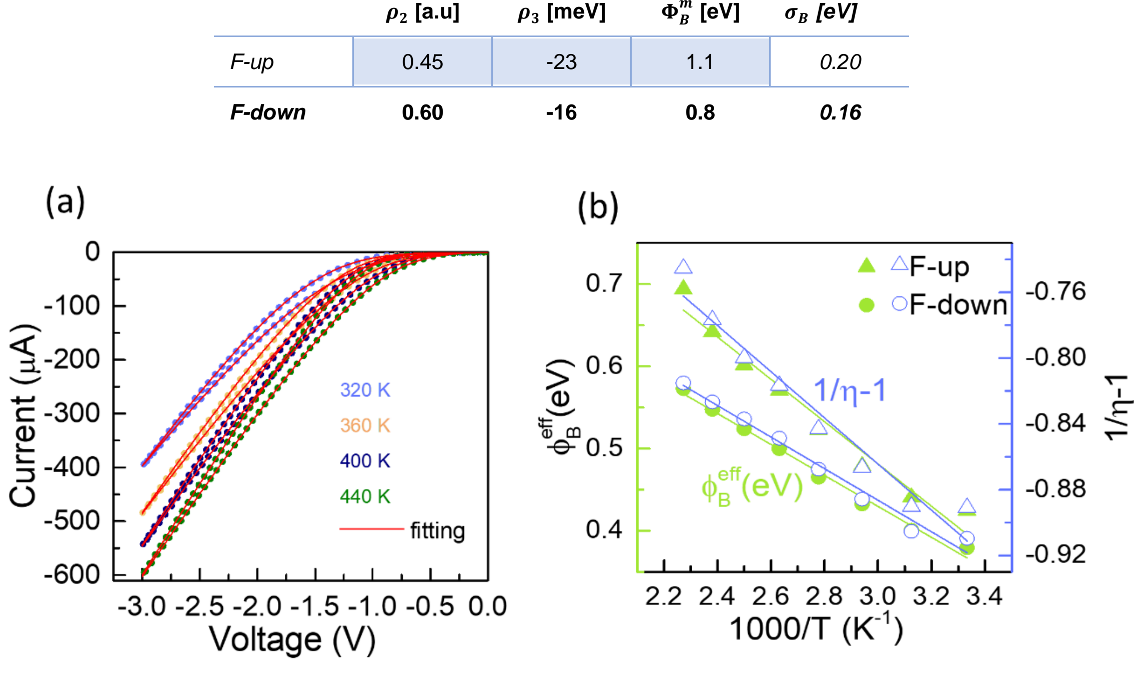

Figure 3. 4 Fitting according to the Thermionic Emission model on the Forward direction. (a) Typical DC current sweeps at different temperatures. (b) Temperature dependency of the effective barrier height and the ideality factor.

In conclusion, both the effective barrier and the mean barrier profile are altered depending on the resistance states. Thus, field-assisted redistribution of defects/dopants in the semiconductor close to the bottom contact interface and consequently the reversible change of current density at the Schottky contact is likely responsible for the RS characteristic of the device. Moreover, for both F-up and F-down the ideality factor variation is decreased by elevating the temperature suggesting a charge/discharge process of defects (such as oxygen vacancies) at the interface.[60] Further studies are necessary to elucidate whether interface reactions are involved in the resistive switching.

3.4 Conclusions

Amorphous IGZO-based memristive devices with Mo as both top and bottom electrodes were fabricated and optimized by using sputter deposition from a single ceramic target as well as co-sputtering from three binary ceramic targets. The as-fabricated devices showed a pristine state with the current rectification of a Schottky diode. This rectification is due to the presence of a thin intermixed oxide layer (4–5 nm), containing Mo^{6+} oxidation state, at the bottom electrode interface. Devices represent analog resistive switching properties. The resistance change is area dependent. Finally, we successfully demonstrated the synaptic behavior of the memristive devices through potentiation and depression, STM to LTM transition and by simulating the learning process. Temperature analysis of DC sweeps of the forward current confirms that the resistive switching occurs due to a uniform Schottky barrier characteristic change. The results presented here show that the Mo/IGZO/Mo structure with analog resistive switching properties can be integrated on crossbar structures and/or joint with IGZO-based TFTs for neuromorphic hardware systems.

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CHAPTER 4

TAILORING THE SYNAPTIC PROPERTIES OF IGZO-BASED MEMRISTORS

Neuromorphic computation based on resistive switching (RS) devices represents a relevant hardware alternative for artificial deep neural networks (DNNs). For the highest accuracies on pattern recognition tasks, an analog, linear and symmetric synaptic weight is essential. Moreover, the RS devices should be integrated with the supporting electronics, as thin film transistors (TFTs) to solve crosstalk issues on the crossbar arrays. Here, an a-IGZO memristor is proposed, with Mo and Ti/Mo as bottom and top contacts, with forming-free analog switching ability for an upcoming integration on crossbar arrays with a-IGZO TFTs for neuromorphic hardware systems.

The development of a TFT compatible fabrication process is accomplished, which results in an a-IGZO memristor with a high stability and low cycle-to-cycle (C2C) variability. The synaptic behavior through potentiation and depression tests using an identical spiking scheme is presented and the modulation of the plasticity characteristics by applying non-identical spiking schemes is also demonstrated. The pattern recognition accuracy, using MNIST handwritten digits dataset, reveals a maximum of 91.82% accuracy, which is a promising result for crossbar implementation. The results displayed here reveal the potential of Mo/a-IGZO/Ti/Mo memristors for neuromorphic hardware.

The results presented in this chapter are published in:

M.E. Pereira, J. Deuermeier, P. Freitas, P. Barquinha, W. Zhang, R. Martins, E. Fortunato and A. Kiazadeh, "**Tailoring the synaptic properties of a-IGZO memristors for artificial deep neural networks**", in APL materials, vol 10, 1, 011113, 2022.

4.1 Introduction

Artificial intelligence (AI) is currently the key feature on innovative technologies for smart systems, pushing for breakthroughs in numerous fields ranging from healthcare to security solutions. However, the AI requirements of fast processing and low energy consumption are slowing its further development since the currently applied Von Neumann's architecture cannot fulfill both demands. Therefore, a new type of compatible hardware is demanded and neuromorphic computation is an exciting alternative.

Neuromorphic computation allows power-efficient systems with high density information, in-memory computation and parallel data processing by preserving the massive parallelism observed in the human brain.[1] Endowed with intelligent functions, neuromorphic systems can execute adaptive learning algorithms and perform tasks ranging from real-time big data analysis to pattern recognition. A great potential candidate for this technology is the resistive switching (RS) device or memristor.[2]

The memristor is a non-linear two-terminal device with the capability of being reduced to the nanoscale, whose conductance level depends on present and past external inputs. Inputs are through its two terminals, resembling a biological synapse where neurons convey data through electrical or chemical pulses. In fact, the memristor can simulate a variety of synaptic functions, the most important being plasticity.

In the biological synapse, plasticity implies the reinforcement or impairment of the connection between two neurons by potentiation or depression steps, respectively, in which the update of their synaptic weight takes place. This behavior can be simulated by the memristor in which the synaptic weight is related to its conductance state. When the memristor adapts its resistance level from low resistance state (LRS) to high resistance state (HRS), in the Reset process, it is simulating the synaptic weight decrease through depression. Similarly, when the memristor is in the Set event, adapting its resistance from HRS to LRS, it is mimicking potentiation and increasing the synaptic weight.

RS devices in crossbar arrays have been proposed for deep neural networks (DNNs) hardware, a high-performance algorithm for classification and recognition applications.[3,4] Common DNNs require iterative multiply-accumulate operations of high-precision weights (> 6 bits)[5] and, therefore, a linear current change in respect to the repeated training pulses and a symmetric rate at potentiation and depression translates into the most accurate learning. However, most RS devices exhibit a natural non-linear response to consecutive identical spiking. Hence, several approaches have been reported on the pulse scheme modulation which resulted in an improved linearity and symmetry,[6] for instance applying incremental pulse voltage or width[7] or current pulses[8] or a heating spike before Set/Reset pulses.[9]

Moreover, to develop an integrated, analog controlled weight storage on-chip technology, for a large-scale energy-efficient DNN, the RS devices should be integrated with supporting electronics. An active element such as the transistor solves crosstalk issues on the crossbar arrays[10] which occur due

to the interference of neighboring cells.[11] They can also act as an on-chip current compliance (CC) to the memristor input and/or compose the additional signal conditioning circuit or support electronics.

The development of a RS device that is eligible for circuit integration and meets all the requirements for DNNs depends on the selection of the RS material and the engineering of top and bottom electrodes, since the modulation of the plasticity characteristics can be controlled by the oxygen concentration in oxides and reactivity of the electrodes.[6]

Several materials have been proposed for the RS layer such as titanium oxide,[8] hafnium dioxide,[12] tantalum oxide,[13] aluminum oxide,[14] and others.[15,16] However, most of the devices are conductive filaments (CF)-based memristors. For neuromorphic computing, CF-type memristors imply some disadvantages related to their natural abrupt switching behavior,[17] which typically translates into a digitalized plasticity characteristic, displaying either full potentiation or full depression.[18] The most common solutions involve multiple devices and complex added circuits to represent one synapse or multilevel cell (MLC) devices capable of some discrete conductance levels.[19,20] Nevertheless, these solutions add complexity to the neuromorphic system and the filament formation and destruction within each device often leads to poor reproducibility.[17]

Therefore, a RS device with analog type of switching, where a gradual conductance change occurs on both Set and Reset side, is preferable for the implementation of an integrated system coupled with synaptic functions.[17] It is due to interfacial RS properties which results in a high reproducibility and low cycle-to-cycle (C2C) variation.[21] Amorphous oxide semiconductors (AOS) have been suggested as active layer for analog memristors[22,23] since the films electrical conductivity can be meticulously controlled by the oxygen/cation composition,[24] enabling a dynamic response to input signals.

Indium-gallium-zinc-oxide (IGZO) is a transparent AOS, employed on thin-film transistors (TFTs) in display technology,[25,26] that greatly favors a cost-efficiency and high integration density on a single IC without the need of interfacing with diverse technologies (i.e. CMOS devices). The a-IGZO-based RS device is the ideal candidate for the memristor integration with TFT and, in fact, it has been previously reported in a single memristor,[27–31] including by our group,[32] and also integrated with TFT.[33–35] However, a fully integrated circuit has not been demonstrated where both transistors semiconductor and memristors RS layer share the one and same processing step as well as the electrodes materials, which would imply a significant decrease in total lithography mask count, improved interconnectivity, and drastic cost reduction. The reason behind this gap is the fact that TFT should be optimized for a high stability and low leakage and the RS device should be optimized for a defect-enabled switch ability with high on/off ratio, which results in a contradictory film optimization where compromises must be made. In fact, most of the studies on IGZO memristors that focus on artificial neural networks (ANNs) applications and show a simulation of pattern recognition accuracies either do not report on crosstalk effect[30,36] or use different IGZO layers and/or electrodes for the TFT.[34]

On our previous work, we reported on the a-IGZO-based memristor with Mo as both top and bottom electrodes. In these devices, the conductivity state is controlled by a potential barrier and the

switching entails adjustments on the barrier height. The a-IGZO memristor has a forming-free and area-dependent performance and enables analog control of resistance states.[32]

Here, we demonstrate the modulation of the a-IGZO-based plasticity characteristics by applying non-identical spiking schemes. The pattern recognition accuracy, using MNIST handwritten digits dataset, was tested and revealed a maximum of 91.8% accuracy using consecutive pulses with a linear increase on voltage amplitude and width which presents itself as very promising. Moreover, we optimize the memristors a-IGZO composition for a lower oxygen content for compatibility with TFTs semiconductor aiming for a forthcoming integration with the a-IGZO based-TFT with Mo as gate and source and drain electrodes.[37] The results displayed here reveal the potential of Mo/a-IGZO/Ti/Mo RS device for crossbar and/or TFT integration for neuromorphic hardware systems.

4.2 Experimental

The RS devices were fabricated on glass substrates, formerly cleaned in repeated ultrasonic baths of acetone and isopropanol and rinsed with deionized water and dry nitrogen. In **Figure 4.1(a)** and **4.1(b)**, a schematic of one RS device in a cross-point structure and a micro-graph of a 4 μm^2 device are presented, respectively.

In **Figure 4.1(c)**, the materials structure is displayed- Mo/a-IGZO/Ti/Mo. For the bottom and top electrodes, radio-frequency (RF) magnetron sputtering was used to deposit a 70 nm thick Mo layer in an AJA ATC-1800 system with a flow rate of 50 sccm of Ar, a sputtering power of 175 W and a deposition pressure of 1.7 mTorr. For the active layer, IGZO thin films were deposited by RF magnetron co-sputtering from three binary ceramic oxide targets. The sputtering powers used on each target were In_2O_3: 121 W, Ga_2O_3: 100 W, and ZnO: 50 W.

Since this study has envisioned an upcoming memristors integration with TFTs, two different conditions were performed regarding the oxygen content during the IGZO film deposition. One which we will refer to $20Ar/5O_2$, that used a flow rate of 20 sccm of Ar and 5 of O_2 being the most similar with the IGZO deposition for TFTs.[38] And another for comparison, $20Ar/20O_2$, that used a flow rate of 20 sccm of Ar and 20 of O_2 previously reported.[32] In **Figure B.1 - Appendix B**, the transfer curves of TFTs fabricated using both IGZO films are presented. The IGZO deposition pressure was kept constant at 2.3 mTorr. The thicknesses were 40 nm in the case of $20Ar/20O_2$ and 65 nm for $20Ar/5O_2$, confirmed by profilometer. E-beam evaporation in a homemade apparatus was used to deposit a thin 6 nm layer of Ti between the IGZO and Mo top layers.

The patterning of the bottom Mo electrode was achieved by reactive ion etching in a Trion Phantom 3 system, using SF_6, whereas the IGZO active layer and Ti/Mo top electrode patterning was done via lift-off. An annealing step of 150°C was performed on a hot plate for 60 minutes after the IGZO patterning and again after the top electrodes patterning, to better simulate the co-fabrication of TFTs which require annealing for improved stability and performance.[39]

All the electrical characterization of the devices was done using a Keithley 4200 SCS semiconductor analyzer connected to a Janis ST-500 probe station. The DC sweeps and the pulses were applied to the top electrode while maintaining the bottom electrode connected to ground.

The XPS argon cluster depth profiles were performed with a Kratos Axis Supra, using a monochromatic Al Ka source running at 300 W. The analysis area was limited to 110 µm in diameter by an aperture and the analyzer was set to a pass energy of 80 eV. Argon clusters of approximately 500 atoms with a kinetic energy of 10 keV were employed for etching with a step duration of 100 s. CasaXPS Version 2.3.19PR1.0 was used for data analysis. Further EDS analysis was undertaken, using a Carl Zeiss AURIGA CrossBeam FIB-SEM workstation, to confirm the XPS results.

4.3 Results and discussion

4.3.1 Memristor cell

In **Figure 4.1(d)** and **4.1(e)**, the results from the XPS argon cluster depth profile are shown. In order to maximize the signal from the a-IGZO and to obtain a clear analysis of the bottom contact interface, the IGZO films have been measured without the Mo/Ti top contact.

The bottom interface is critical for the conduction since it represents the barrier for electron injection due to an oxidation of the Mo at the interface.[32] The modulation of the Schottky barrier controls the RS.[22,40] Concerning the top electrode, a thin Ti layer was added due to its well-known oxygen getter effect.[41] Ti reacts with the switching oxide by extracting oxygen ions which increases the donor concentration and, therefore, boosts the conductance of the Ohmic contact and creates a highly conductive interface region in a-IGZO memristors.[42] Contrasting with the Schottky barrier at the Mo bottom electrode, an asymmetry is built in the oxide which results in a more pronounced non-linear profile and memristors with higher I_{LRS}/I_{HRS} ratio.[43]

The difference in IGZO thickness due to the different oxygen amounts in the process gas affects the etch times until the Mo bottom contact is reached, being higher for the 20Ar/20O_2 sample. Moreover, the 20Ar/5O_2 is likely more resistive to the etching, due to a higher film density caused by the increased kinetic energy of ions in the process gas, compared to 20Ar/20O_2.[44,45] An important observation is that the oxygen amount is identical in the two samples, around 44 at%, despite the different levels of oxygen flow. However, the cation ratio of IGZO is strongly altered. The sample 20Ar/20O_2 has an average bulk In:Ga:Zn atomic composition of 2.1:1.0:1.9 whereas 20Ar/5O_2 has a composition of 2.5:1.0:1.5. The ratio was normalized to the Ga concentration, since both samples have an identical Ga concentration of 11 at%. It can be excluded that this difference is caused by damage induced by the argon cluster beam, because the trend is the same for the films prior to the etching. In a previous study, the In/Ga ratio had been found to be critical for the a-IGZO resistivity. More In content leads to a more conductive material.[24]

To confirm these results, EDS was performed on the films deposited on silicon. The results are shown in **Figure 4.1(f)** where the comparison of the atomic composition obtained by XPS and EDS techniques is shown. EDS shows the same trend in the cation ratios as it was revealed by XPS cluster depth profiling. The 20Ar/20O_2 film presents less In and more Zn which is in accordance with previous reports.[46] This can be explained by an increased bombardment of O_2 on the film itself while growing. During the deposition, O_2 gas is inserted in the sputtering system near the substrate while Ar gas is inserted near the target. The additional oxygen bombardment can lead to the removal of material from the film, which has resulted in a lower density in previous studies.[47] The elements with the weaker bonds in the film will be removed preferentially, such as In compared to Ga.

The oxygen content obtained with both techniques is given in **Figure 4.1(f).** The absolute amounts differ between techniques, but the identical oxygen content in the two samples is confirmed. The fact that the oxygen amount in the films remains unaltered can infer that with the smallest oxygen flow (5 sccms), there is already a saturation of this element in the film since oxide targets are being used. In addition, it needs to be mentioned, that the oxygen amount at the surface, determined from XPS prior to argon cluster etching, is indeed higher in the 20Ar/20O_2 sample, about 46 % compared to 44%. However, this does not represent the bulk oxygen content, which is confirmed by the EDS results. Since the devices are controlled by the barrier properties at the bottom contact, the surface of the IGZO is of minor relevance for the RS.

In **Figure 4.1(g),** the comparison between the Set and Reset of 20Ar/5O_2 and 20Ar/20O_2 is shown and in the inset, the read current after each measurement at -0.1 V is provided. The 4 μm^2 devices work in bipolar switching mode, Set occurs in negative polarity while Reset happens under positive polarity. 20Ar/20O_2 device has a higher I_{LRS}/I_{HRS} ratio compared to 20Ar/5O_2 device due to lower conductivity of the semiconductor in pristine state and the increased Schottky barrier height. The impact of the In/Ga ratio on conductivity in IGZO is well known.[24] In IGZO Schottky diodes, the barrier height has been found to be sensitive to the In/Ga ratio[48]: lower In/Ga ratios lead to higher barriers. This is explained by the strong Ga-O bond (compared to In-O and Zn-O), which suppresses oxygen vacancies (VOs).[49] Note that the depletion width is also affected by the In/Ga ratio, being smaller for higher values of In/Ga.[48] The principle behind the RS is a change of Schottky barrier profile[32] which is in agreement with other reports with rectifying and analog RS properties.[40]

The typical analog behavior of a 20Ar/20O_2 device is shown in **Figure 4.1(h)**, where successive voltage DC sweeps on negative and positive polarities were applied to the top contact which resulted in the device conductance being gradually increased and decreased, respectively. To demonstrate a gradual Set process, four voltage sweeps were carried out starting from 0 to -1.5 V during the first measurement until 0 to -3 V for the last measurement. The results are displayed in red in **Figure 4.1(h)** where it is clear the gradual increase of the device conductance state. For the Reset process, the same methodology was used for positive polarities with the first voltage sweep being from 0 to 1.5 V and the last sweep from 0 to 2.4 V, displayed in dark blue in **Figure 4.1(h).** In this case, there is a gradual

decrease of the conductance state. All measurements were performed with a voltage step of 0.1 V, the speed was at normal mode and the integration time was in auto setting. Both hold and delay time were zero.

Several devices with different areas were fabricated and a micrograph of a representative part of a sample can be consulted on **Figure B.2 - Appendix B**. Generally, in AOS materials, the switching mechanism is area-dependent. All the results presented throughout this paper are in respect to 4 µm^2 devices.

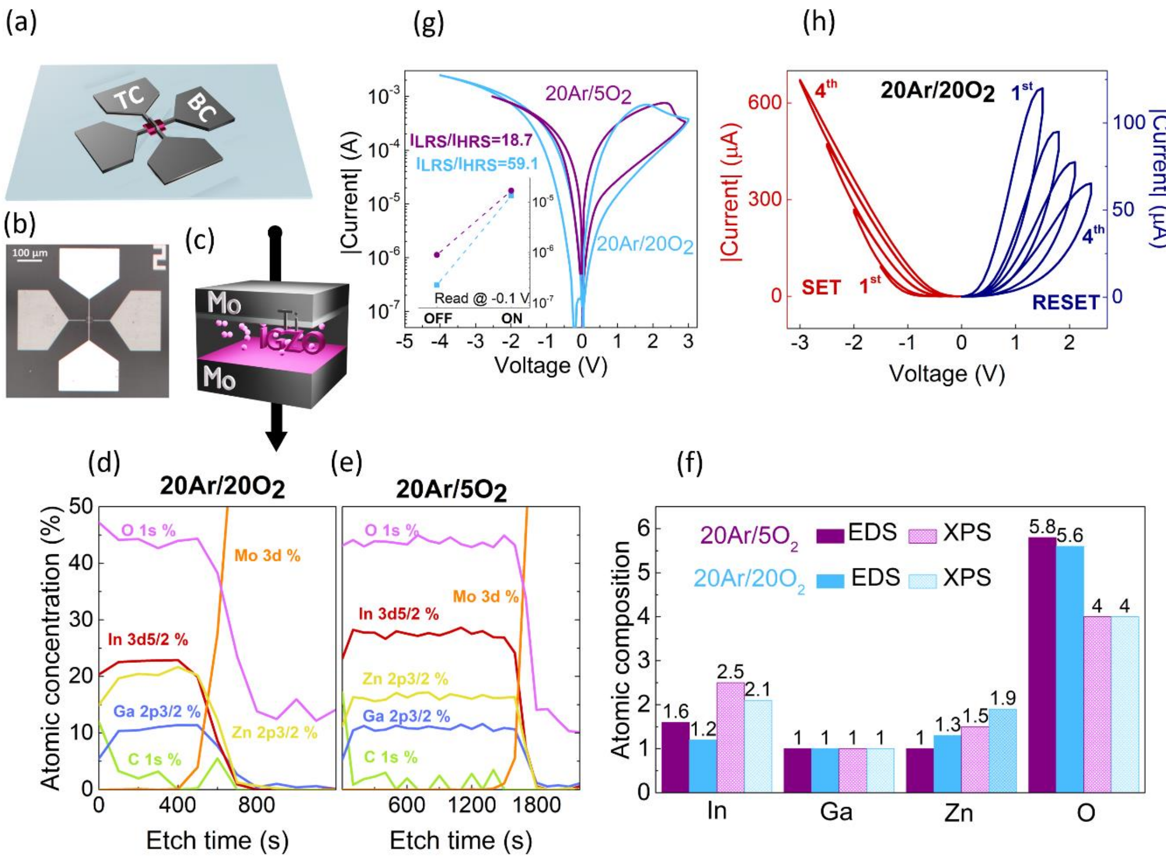

Figure 4. 1 Mo/IGZO/Ti/Mo I-V characteristic for Set and Reset and material characterization for co-sputtered IGZO in different Ar/O$_2$ atmosphere. (a) Schematic illustration of the cross-point structure of the memristors with bottom contact (BC) and top contact (TC) hinted; (b) Micrograph of one 4 µm^2 device; (c) Schematic illustration of the Mo/a-IGZO/Ti/Mo materials structure; XPS argon cluster depth profiles of (d) 20Ar/20O$_2$ and (e) 20Ar/5O$_2$ films without the top contact. The relative atomic concentrations are displayed with respect to etch time; (f) Atomic composition of In, Ga, Zn and O of both IGZO films analyzed by EDS and XPS for comparison; (g) I–V characteristic of one Set and one Reset for comparison of both devices- 20Ar/5O$_2$ and 20Ar/20O$_2$- with inset of read current at -0.1 V after each Set and Reset displaying on/off ratios of 59.1 and 18.7, respectively; (h) I–V characteristic displaying analog behavior by gradual increase of voltage sweep span for Set and Reset. The order of the measurements is displayed highlighting the first (1st) sweep and the last (4th) for both Set and Reset.

4.3.2 Exponential synaptic response

To simulate the synaptic plasticity, through potentiation and depression tests, the device characteristics were studied using an identical pulse train. Here, potentiation implies facilitating the connection between two neurons and it is simulated by applying negative pulses to the top contact and increasing the current state of the device. Depression, which is constraining the neuron's connection, is replicated by applying positive pulses to the top contact and, therefore, decreasing the devices current state.

An optimal condition of pulse amplitude and width should be chosen for a gradual current state increase/decrease. In **Figure 4.2(a)** and **4.2(b)**, the 100 pulses potentiation tests for the 20Ar/5O_2 memristor with different pulse amplitudes for the same width, and the different pulse widths for the same amplitude are presented, respectively. The read step is always performed immediately after each pulse and at -0.1 V. All the conditions result in a non-linear curve and the difference lies on the current state achieved, which should be the maximum possible for a high I_{LRS}/I_{HRS} ratio. Evidently, the higher the pulse amplitude and width, the higher the current reached, but also the faster the current state gets saturated. For a gradual increase, a pulse scheme in which current state does not reach a saturated value is preferable as it is for lower pulse amplitudes/widths. One can also conclude that pulse amplitude is the principal parameter that controls the LRS state reached while the pulse width controls the gradualness of the increase.

The same tests for depression can be found in **Figure 4.2(c)** and **4.2(d)** for the 20Ar/5O_2 memristor, where 100 positive pulses with different pulse amplitudes for the same width and different pulse widths for the same amplitude are shown, respectively. Here, the gradual decrease of the current is desirable as it is for example on 3.1 V at 300 µs pulses. Therefore, one can conclude that by controlling the pulse width small adjustments to the current state are accomplished while for larger adjustments, the pulse amplitude should be tuned. The identical pulse training study for 20Ar/20O_2 devices can be found in **Figure B.3 - Appendix B**.

To evaluate C2C variability, 50 cycles of potentiation/depression tests were carried out using 5000 pulses. Considering the previous conclusions and the high number of pulses for this test, the programmed pulse amplitudes and widths chosen for 20Ar/5O_2 device were -2.5 V at 200 µs for potentiation and 2.3 V at 300 µs for depression, as can be seen in **Figure 4.2(e)**. For 20Ar/20O_2 devices, consecutive pulses of -3 V at 150 µs for potentiation and of 2.3 V at 150 µs for depression were applied as shown in **Figure 4.2(f).** In **Figure 4.2(g)** and **4.2(h)**, the experimental Cumulative Distribution Function (eCDF) lookup tables of the conductance change (ΔG) within the 50 cycles of potentiation/depression as a function of conductance (G) for the Set and Reset processes are presented for the 20Ar/5O_2 and 20Ar/20O_2 devices, respectively. Here, the color map of CDF indicates the probability that ΔG is less than or equal to the value on the y-axis for a given conductance on the x-axis. For the lowest C2C variability, a straight line with ΔG = 0 should be presented with red below zero and blue

above zero with this case colormap. C2C variation is more pronounced during Set operation of the 20Ar/5O_2 device, since the current state is not yet saturated. When comparing both devices, one can see that the LRS state of 20Ar/5O_2 is higher than the 20Ar/20O_2 devices. On the other hand, HRS state of 20Ar/20O_2 device is lower than the 20Ar/5O_2 providing a higher I_{LRS}/I_{HRS} ratio.

However, an ideal artificial synapse should present a linear and symmetric current increase/decrease under consecutive applied pulses for a maximum accuracy in pattern recognition.[6] The linearity condition comes from the fact that the device should be able to achieve as many distinct conductance states as possible according to the high weight precision requirement and the symmetry between Set and Reset enables the implementation of the fastest and most efficient programming method of the memristor arrays. In the 20Ar/5O_2 device, the current state does not saturate so prominently as in the 20Ar/20O_2 memristor. That has to do with the pulse scheme parameters that were chosen for the highest I_{LRS}/I_{HRS} ratio possible.

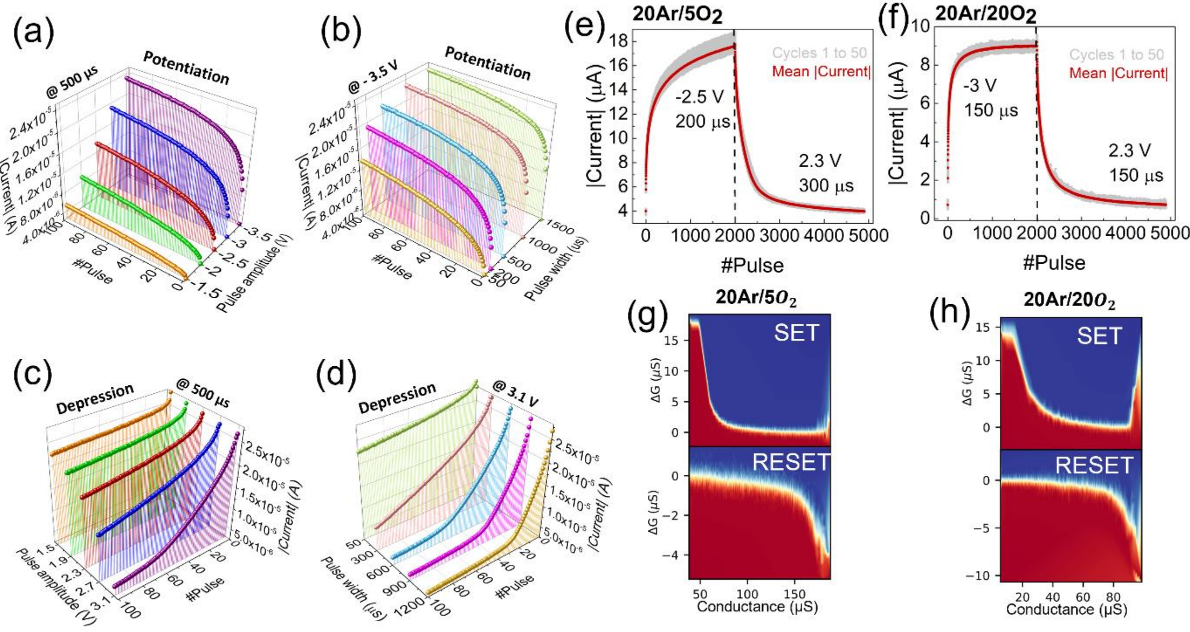

Figure 4. 2 Exponential synaptic response and C2C variability. 100 identical pulses potentiation tests, for the memristor with low oxygen (20Ar/5O_2), with (a) different amplitude, same width; (b) different width, same amplitude; and depression tests with identical pulses of (c) different amplitude, same width; (d) different width, same amplitude. Read current at -0.1 V; 50 cycles of 5000 pulses of potentiation and depression with the mean current in red for (e) memristor with low oxygen (20Ar/5O_2) and (f) memristor with high oxygen (20Ar/20O_2); experimental Cumulative Distribution Function (eCDF) Lookup tables of the conductance change (Δ G) within the 50 cycles of potentiation/depression as a function of conductance (G) for the Set and Reset processes for the (g) 20Ar/5O_2 and (h) 20Ar/20O_2 devices.

4.3.3 Linear and symmetric synaptic response

Different pulse schemes were tried to modulate the potentiation/depression characteristics, to improve linearity and symmetry and can be consulted on **Figure 4.3(a).** Scheme A consists of identical pulses. Pulse schemes B and C are non-identical spikes with either increasing pulse amplitude or width, respectively. In pulse scheme D a consistent increase in pulse amplitude and width in each pulse is applied. For all conditions, the read process is a pulse of 20 µs at -0.1 V.

In **Figure 4.3(b)**, potentiation and depression results for the 20Ar/5O_2 memristor are presented for each pulse scheme. Scheme A, the purple curve, shows an exponential response where a rapid current increase/decrease takes place within a few pulses and then reaches a saturated current regime, as previously discussed. Scheme B, the red curve, provides a slower current increase/decrease during the first few pulses and it becomes a linear change after -1.9 V for potentiation and 2.5 V for depression. On the other hand, scheme C, the blue curve, shows a current saturation after 800 µs pulse for potentiation and 890 µs pulse for depression.

For scheme D, a combination of both B and C schemes was tested. The pulse amplitude was linearly increased from -1.9 V to -4 V for potentiation and 2.5 V to 3 V for depression as scheme B suggested. On depression, the pulse width was also linearly increased according to the results of scheme C, from 1 to 890 µs. For potentiation, since -1.9 V was the starting pulse amplitude, a 1 µs pulse would not be sufficient for a linear current increase at the first few pulses and, therefore, a shift on the width interval was implemented. Instead of using a pulse width interval from 1 to 800 µs as pulse scheme C suggested, an interval of 400 to 1200 was used maintaining the difference between first and final pulses width applied. The results correspond to the green curve where a linear and symmetrical response to the input pulses from beginning to end is presented. It is noted that the proposed pulse scheme D is rather complex, involving an increase in pulse amplitude and width in each pulse. Nevertheless, in order to deal with non-linearity issues in an efficient pulse scheme, design of 1T1M is proposed[50] which is effectively implantable with IGZO condition as mentioned in the current report for both transistor and memristor devices.

To compare the linearity and symmetry on the synaptic plasticity tests that resulted from each pulse scheme, a non-linearity parameter α was extracted,[51] using the following **equation (4.1)**:

$$G = \begin{cases} \left((G_{LRS}^{\alpha} - G_{HRS}^{\alpha}) \times W + G_{HRS}^{\alpha} \right)^{1/\alpha} & if\ \alpha \neq 0, \\ G_{HRS} \times \left(\frac{G_{LRS}}{G_{HRS}} \right)^{W} & if\ \alpha = 0, \end{cases} \qquad \mathbf{(4.1)}$$

where G is the conductance change, G_{LRS} and G_{HRS} are LRS and HRS conductance respectively and w is an internal variable of the synaptic weight which varies from 0 to 1, w increases or decreases as potentiation or depression pulses are applied. α is the non-linearity parameter that controls potentiation

(α_p) or depression (α_d) characteristics. The closer α is to 1, the more linear is potentiation/depression. Furthermore, the smaller the difference between the values of α for potentiation and depression, the more improved symmetric response is obtained.

Figure 4.3(c) shows the values of α_p and α_d for all schemes. As can be seen, scheme D has α_p = 1.23 and α_d = 0.83, numerically revealing close to optimal linear and symmetric synaptic characteristics. The identical study for the 20Ar/20O$_2$ memristor is presented in **Figure B.4 - Appendix B**.

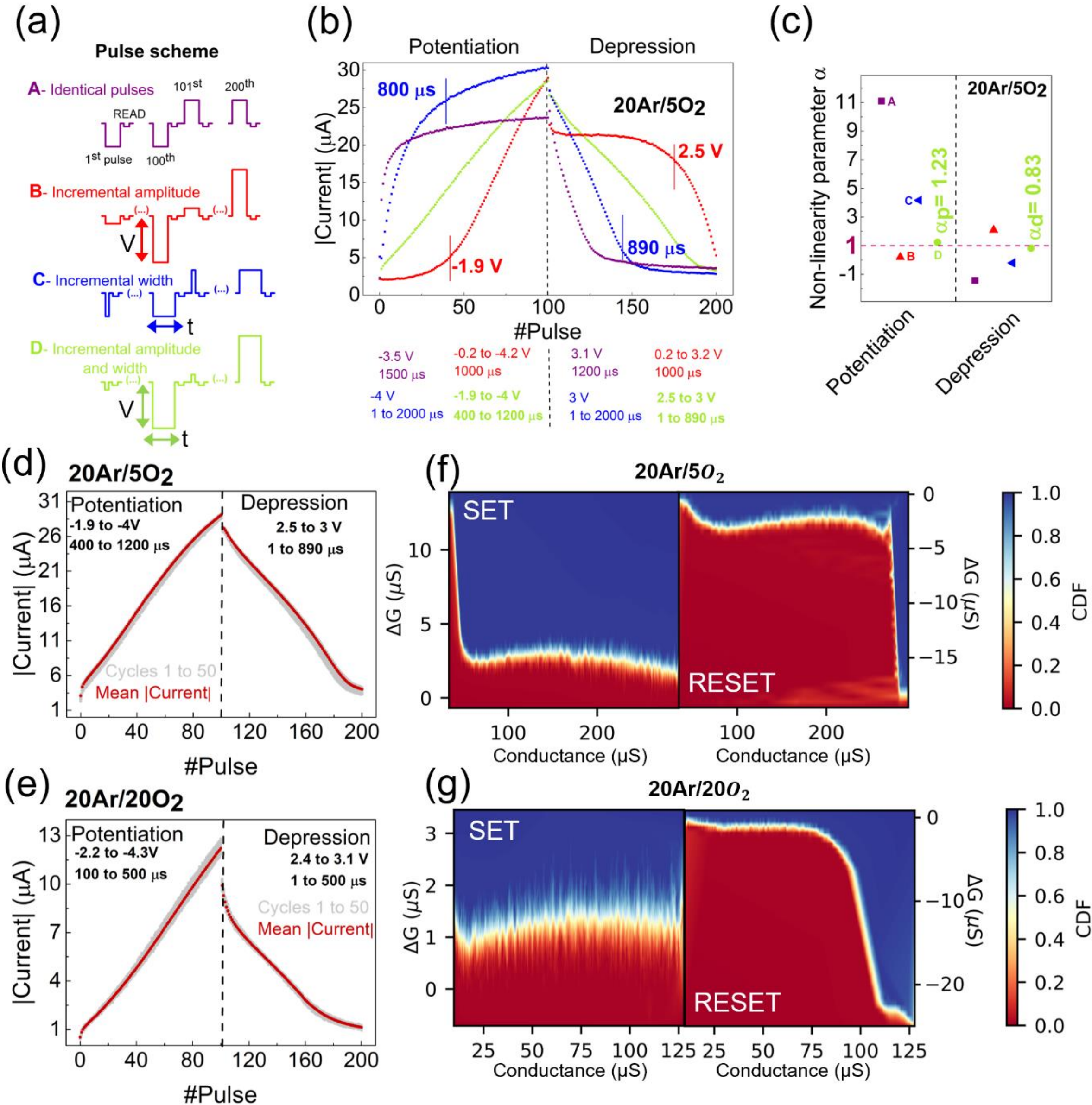

Figure 4. 3 Linear and symmetric synaptic response and C2C variability. (a) Schematic illustration of pulse schemes A identical pulses, B incremental amplitude pulse, C incremental width pulses and D incremental amplitude and width pulse. (b) Potentiation and depression results for 20Ar/5O$_2$ of the different pulses schemes with the numerical description of each scheme on the bottom of the graph. The conditions that limit linearity are within the graph. (c) Non-linearity parameter for potentiation and depression for each pulse scheme displayed on (b), with α_p =1.23 and α_d =0.83 of pulse scheme D

highlighted. 50 cycles of potentiation and depression for the linear pulse scheme D of 20Ar/5O_2 memristor and (e) optimized pulse scheme for 20Ar/20O_2 memristor. Experimental Cumulative Distribution Function (eCDF) Lookup tables of the conductance change (Δ G) within the 50 cycles of potentiation/depression as a function of G for the Set and Reset processes for the (f) 20Ar/5O_2 and (g) 20Ar/20O_2 devices. Read current is -0.1 V for all the tests.

Using pulse scheme D, 50 cycles of potentiation and depression were carried out on both 20Ar/5O_2 device, and the 20Ar/20O_2 memristor, shown in **Figure 4.3(d)** and **4.3(e)** respectively, to evaluate the linearity stability under incremental amplitude/with pulses. It is important to note that several devices were tested for the modulation of the pulse scheme and behave identical within their category, 20Ar/5O_2 20Ar/20O_2, as can be evaluated in **Figure B.5 - Appendix B**, where potentiation and depression tests under the same non-identical pulse schemes for 5 different devices is presented, proving the reproducibility of the fabrication process and the reliability of the proposed scheme for a linear and symmetric synaptic characteristic of the Mo/a-IGZO/Ti/Mo structure.

In **Figure 4.3(f)** and **4.3(g)**, where the eCDF lookup tables of Δ G within the 50 cycles as a function of G for Set and Reset of both types of devices are presented, one can confer that the higher variability during cycles is presented for the 20Ar/20O_2 devices. Nevertheless, it can be stated that both memristors have low variability between C2C, which proves the potential of the analog a-IGZO-based RS device. I_{LRS}/I_{HRS} ratio is higher for 20Ar/20O_2 devices, nonetheless an I_{LRS}/I_{HRS} ratio of more than 10 might be enough for a highly accurate pattern recognition[52] in a 1T1M active crossbar considering that crosstalk would be minimized.

4.3.4 1M Crossbar simulation

To assess the effect of the synaptic characteristics on pattern recognition accuracy, a simulation of a three-layer (input, hidden, and output layers) perceptron neural network was performed by CrossSim[53] using a hand-written digit dataset (MNIST). The number of neurons on the input, hidden and output layers is 784, 30 and 10, respectively, as shown in **Figure 4.4(a).** Each neuron on the input layer is connected to all neurons in the hidden layer through synapses and each neuron on the hidden layer is connected to all output neurons and they communicate by conveying the conductance states. **Figure 4.4(b)** presents the pattern recognition accuracies obtained with the linear response shown on **Figure 4.43d)** and **4.3(e)** and the exponential response displayed on **Figure 4.2(e)** and **4.2(f)** for the 20Ar/5O_2 and the 20Ar/20O_2 memristors, respectively.

The exponential response reaches higher accuracies than expected given the non-linearity presented (79.72% and 80.05%), due to the high number of pulses applied (5000 pulses) and low C2C variability. However, the linear response is the one with the excellent performance disclosing accuracies of 91.82% and 90.93% for the 20Ar/5O_2 and 20Ar/20O_2 memristors. For the 20Ar/5O_2 device, the default test provided by CrossSim that uses the 25% to 75% range of the on/off window was

performed. For the $20Ar/20O_2$ device, since the depression test was not as linear at the end of the test, an adjustment was made for 10% - 60% range instead (**Figure B.6 - Appendix B**).

These results reveal that with at least 6 bit precision (default for CrossSim) and disregarding any read noise induced errors, an on/off ratio of 1 order of magnitude does not pose as a drawback in achieving high accuracies, and instead C2C variability and linearity play a much more important role.

The impact of nonlinearity, asymmetry, cycle-to-cycle variability and noise can be accurately considered in the CrossSim.[53] Since the dynamic range of devices are different and for $20Ar/5O_2$ device is smaller (i.e. on/off ratio>10), additionally, the normalized low-frequency Read Noise (σ_{RN}) was measured for 1 s, using a sampling rate of 0.1 ms/sample (**Figure 4.4(c)**), where σ_{RN} is the standard deviation of the $\Delta G/G_0$.

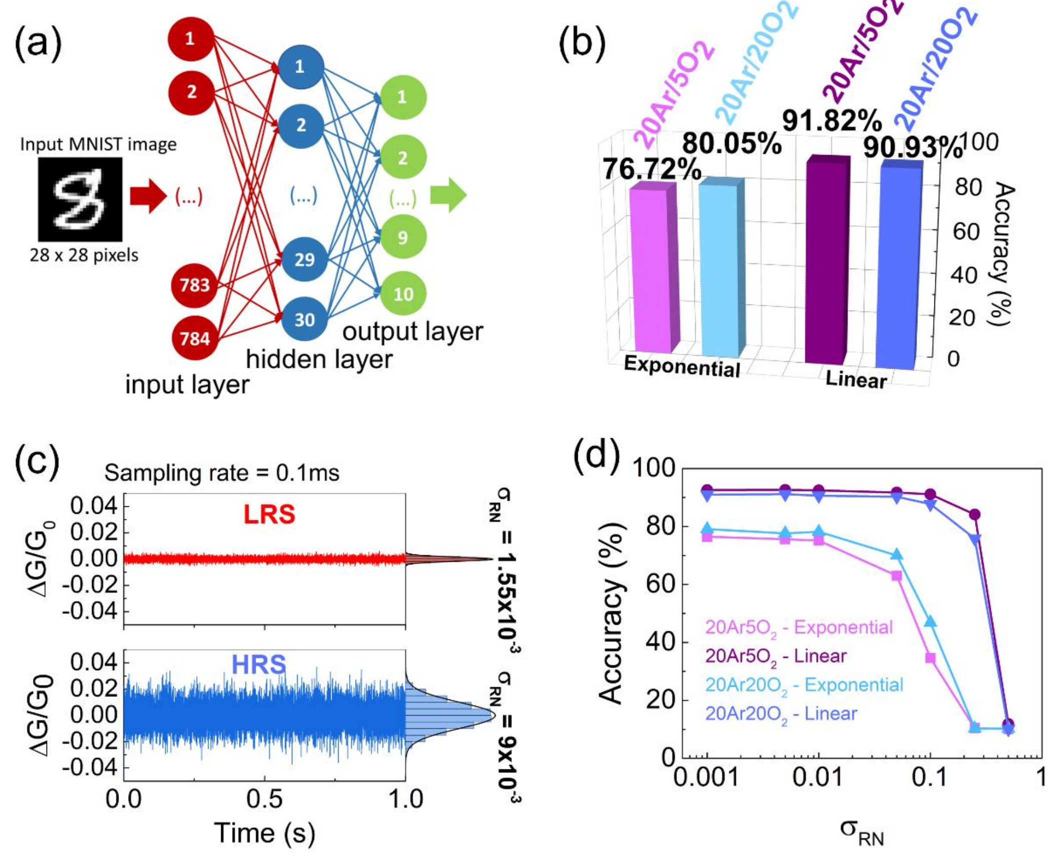

Figure 4. 4 1M CrossSim simulation results for pattern recognition applications. (a) Schematic illustration of a three-layer perceptron neural network, the number of neurons used on the input, hidden and output layers is 784, 30 and 10, respectively. (b) Accuracies for pattern recognition achieved for the exponential natural response on potentiation and depression using identical spiking (**Figure 4.2(e)** and **4.2(f)**) for both memristors: $20Ar/5O_2$ (76.72%) and $20Ar/20O_2$ (80.05%) and for the linear response achieved by pulse scheme D with incremental pulse amplitude and width (**Figure 4.3(d)** and **4.3(e)**), also for both memristors: $20Ar/5O_2$ (91.82%) and $20Ar/20O_2$ (90.93%); (c) Normalized low-frequency Read Noise (σ_{RN}) measured for 1 s, using a sampling rate of 0.1 ms/sample for HRS and LRS and (d) Impact of σ_{RN} on the training accuracy of both devices ($20Ar/5O_2$ and $20Ar/20O_2$).

The impact of σ_{RN} on the training accuracy was then evaluated by injecting noise into each weight's simulated conductance state, each time a read operation occurs, using the following **Equation (4.1)**:

$$G = G_0 + N(\sigma), \quad \sigma = \sigma_{RN} \times G_{Range} \qquad \mathbf{(4.1)}$$

Figure 4.4(d) shows the impact of σ_{RN} on the training accuracy of both devices (20Ar/5O_2 and 20Ar/20O_2) following both of their programming methods (exponential and linear responses). A noise threshold of σ_{RN} = 0.01 and σ_{RN} = 0.1 exists for the exponential and linear responses respectively, where the training accuracy starts to degrade. However, the highest measured σ_{RN} for these devices falls below the lowest threshold, indicating that the impact of read noise on training of both devices can be considered negligible.

4.4 Conclusions

In conclusion, amorphous IGZO-based memristors with Mo as bottom contact and Ti/Mo as top contact were fabricated. The IGZO film was optimized for a lower oxygen content, and annealing steps were integrated on the fabrication processes for compatibility with the TFTs semiconductor aiming for a forthcoming integration with the IGZO based-TFT with Mo as gate and source and drain electrodes.

Our proposed methodology is proven to be reproducible and reliable and uses conventional patterning strategies and no noble-metals, being a cost-effective approach, compatible with room temperature-based processes allowing for the implementation of transparent and flexible substrates, such as polymer and paper, which is a core feature for IoT applications.

The devices have electroforming-free and an area-dependent analog resistive switching which are very appealing properties for neuromorphic hardware applications. The modulation of the a-IGZO memristors plasticity characteristics was achieved by applying non-identical spiking schemes and a linear and symmetrical potentiation and depression was obtained proven by the calculated non-linearity parameter. The pattern recognition accuracy, using MNIST handwritten digits dataset, was tested and revealed a maximum of 91.82% accuracy using consecutive pulses with incremental voltage amplitude and width which presents itself as a very promising result for neuromorphic systems.

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CHAPTER 5

SOLVING CROSSTALK IN IGZO-BASED ACTIVE CROSSBAR ARRAYS

Memristor crossbar arrays can compose the efficient hardware for artificial intelligent applications. However, the requirements for a linear and symmetric synaptic weight update and low cycle-to-cycle and device-to-device variability as well as the sneak-path current issue have been delaying its further development. Here, we report on a thin-film amorphous oxide-based 4×4 1T1M crossbar. The a-IGZO crossbar is built on a flexible polyimide substrate, enabling IoT and wearable applications. In the novel framework, the TFT and memristor are fabricated at the same level, with the same processing steps and sharing the same materials for all layers. The 1T1M cells show linear and symmetrical plasticity characteristic with low cycle-to-cycle variability. The memristor performs like an analog dot product engine and we experimentally demonstrate vector-matrix multiplications in the 4×4 crossbars, in which the sneak-path current issue is successfully suppressed, resulting in a proof-of-concept for a cost-effective, flexible ANNs hardware.

The results presented in this chapter are published in:

M.E. Pereira, J. Deuermeier, C. Figueiredo, Â. Santos, R. Martins, E. Fortunato, P. Barquinha and A. Kiazadeh, "**Flexible active crossbar arrays using amorphous oxide semiconductor technology towards artificial neural networks hardware**", in Advanced Electronic Materials, vol 8, 11, 2200642, 2022.

5.1 Introduction

Neuromorphic computation based on resistive switching (RS) devices is a promising technology in solving the modern age artificial intelligence (AI) drawbacks such as latency and privacy issues related to the cloud usage, the high-power consumption required to support data centers and the scaling limitations of Von Neumann's architecture.

The RS device or memristor is a non-linear two terminal device, scalable to the nanoscale, and eligible as the synaptic element on neuromorphic chips. Neurons transmit important data by electrical or chemical pulses, which is modulated at the biological synapse. Plasticity characteristic relates to the strength of the connection between two neurons called synaptic weight. The RS device can simulate this behavior by continuously adapting its resistance state upon application of electrical stimuli. When the device transfers from high resistance state (HRS) to low resistance state (LRS), it is mimicking the synaptic weight reinforcement in a process called potentiation. Correspondingly, when the memristor shifts from LRS to HRS, it is emulating the synaptic weight being weakened in the depression process.

Neuromorphic systems perform in-memory computation with adaptive learning algorithms on hardware and can, therefore, execute intelligent functions on tasks ranging from the arrangement and real-time analysis of unstructured data to pattern recognition with power-efficient and parallel data processing. The algorithms consist in several multiply-accumulate operations (dot products). RS devices in crossbar arrays can compose the artificial neural networks (ANN) hardware.[1] In this respect, the input weight can be stored in each RS device with analog control of resistance modulation. Furthermore, the dot product can be well-executed in RS crossbars.

In fact, with a single step, vector-matrix multiplications (VMM) are computed inherently via Ohm's law for multiplication and Kirchhoff 's law for summation.[2–4] In such architecture, the data is stored at the hardware where the operations take place preventing communication issues. Naturally, a linear and symmetric synaptic weight update in potentiation and depression with respect to the continuous training pulses translates into a more effective learning. However, most RS devices present a natural exponential behavior to identical spiking. Several solutions have been proposed for the improvement of linearity and symmetry by using different training pulse schemes,[5–7] including our previous work.[8]

Another requirement for high performance in memristor crossbars is low cycle-to-cycle (C2C) and device-to-device (D2D) variability, difficult to achieve in filament-based RS devices.[9] Some strategies have been emerging to allow the restriction of the filament formation in certain locations and thus limit considerable variations from C2C.[10] However, an area-dependent switching that enables the analog control of conductance states is the most reliable solution for low C2C and D2D variabilities.

Furthermore, memristor crossbars usually suffer from sneak-path current issues related to the interference of neighboring devices, leading to the decrease of the read window, limiting the size of

the arrays and reducing the overall accuracy of any given task. To mitigate this problem, different bias schemes have been proposed[11,12] in which the unselected devices are biased with a fraction of the selected memristor voltage. However, they imply a significant increase on the energy consumption and require devices with extremely low conductance on the HRS and large I_{LRS}/I_{HRS} ratio to be successful.[13]

These challenges can be overcome by adding a selector device in each cell of the crossbars allowing individual cell activation. An active element such as the transistor, in series with memristors, acts like a switch- when in the on state, behaves as a high conductance wire and, when in the off state, no current flows and, therefore, the memristor is not selected. Moreover, the transistor can provide an on-chip current compliance (CC) and, therefore, allow a controlled current input to the memristor, which will assist in achieving the linear and symmetrical plasticity characteristic with low C2C variability.[14,15]

Hence, the integration of the memristor with the transistor in the 1-transistor 1-memristor (1T1M) configuration has been widely exploited in the past years. Several studies on HfO_x based memristors in a 1T1M configuration have been reported.[16–18] Yao *et al.* presented a 128 × 8 1T1M array implementation, using an interfacial switching HfO_2/Al_2O_3 multilayer based-memristor, where the sneak-path issue was solved and the application of CC was successfully controlled by the transistor.[19] In the latter, TaO_x was used as a capping layer that acts as CC and oxygen reservoir but it has been reported also as RS layer in 1T1M crossbars.[20] Later, various reports on HfO_x based memristors on large 1T1M crossbars appeared that further prove its potential for large-scale ANN hardware.[4,21–23] However, like most research on the 1T1M structure, the memristors are hybridly integrated with CMOS transistors thus limiting downsizing and large-scale implementations.

Actually, very few studies have emerged showing TFT and memristor monolithic integration, with both devices sharing some of the processing steps. Ghenzi *el al.* reports on a ZnO-based thin-film transistor (TFT) connected to a TiO_2 memristor on a single 1T1M cell in which the TFT is fabricated prior to the memristor.[24] Wang *et al.* reported on a 2 x 2 1T1M crossbar array using MoS_2 transistors and hBN RRAMs.[25] Sivan *et al.* presents a 1T1M structure in which the TFT and memristor are both composed of WSe_2, however, they are deposited in different fabrication steps due to the different morphology required for each device and, thus, the memristor is produced after the TFT.[26] More recently, Kim *et al.* reported on a fluoropolymer-based organic memristor in a 1T1M configuration built onto a flexible PEN substrate.[27] The TFTs source and drain material and deposition layer is also the memristors bottom contact and fluoropolymer memristor active layer is applied for passivation of the TFT.

The amorphous oxide semiconductor (AOS), indium gallium zinc oxide (IGZO) has also been demonstrated as active layer for memristors due to its great potential for 1T1M integration.[28–36] IGZO is often employed on TFTs in the display technology[37,38] as the semiconductor layer due to its excellent stability, cost-efficient manufacturing, and the additional control on its electrical conductivity provided by the oxygen and cation composition.[39] In fact, the development of neuromorphic displays is the

unavoidable new trend for system-on-panel applications. One in which the mature AOS technology is used both for the display and, naturally combined, with the ANN hardware.[40]

In regard to the memristor integration with TFT, some efforts on the optimization of the IGZO layer for memristor compatibility have been made,[41,42] including by our group.[8] Chang *et al.* successfully reported on a 1T1M structure using the same IGZO layer for both TFT and memristor, however the RS device had an abrupt type of switching which is not ideal for ANNs and, in fact, no plasticity characteristic was shown.[43] Later, Jang *et al.* demonstrated linear characteristics of IGZO-based 1T2M crossbar simulation. The memristor and TFTs have different deposition conditions with memristor owing an abrupt Set and gradual Reset like most filamentary devices.[44]

Therefore, a fully integrated monolithic 1T1M structure has not been demonstrated yet, in which both the TFTs semiconductor and RS layers share the same processing steps as well as the same materials (see **Table C.1 - Appendix C**). The reason why this has been a challenge is the fact that the TFT device should be optimized for a high long-term stability and low leakage and the memristor for a defect-enabled switching ability. In the past, this was only researched with different optimized films for active layer in memristors and channel in TFTs and without integration on the same substrate.[44] To our knowledge, no analog arithmetic crossbar fully based on AOS technology was ever presented.

Here, we report on a thin-film a-IGZO based 1T1M 4 × 4 crossbar array built on a flexible polyimide substrate, as a core feature for IoT applications and wearables. We propose a novel framework in which both TFT and memristor are fabricated at the same level, using the same processing steps and therefore, sharing the same material for all layers. We show the plasticity characteristic for ANNs with potentiation and depression tests on the 1T1M cells with a linear and symmetrical response. The endurance of our devices is also proved on bending tests, and we experimentally perform VMM operations in the 4×4 active crossbars with a relative error, from analytical to measured, of less than 10%, exposing the massive potential for an efficient, flexible and large-scale ANN hardware. Furthermore, for 1T1M crossbar-based online training, the pattern recognition accuracy of MNIST handwritten digits dataset is simulated and results in an accuracy of 93.28%.

5.2 Experimental

A step-by-step diagram is provided in **Figure C.1- Appendix C** with all the fabrication steps. The devices were fabricated on polyimide substrates deposited on Corning Eagle glass, previously cleaned in repeated ultrasonic baths of acetone and isopropanol and rinsed with deionized water and dry nitrogen.

The polyimide was deposited by spin-coating for the targeted 6 µm thickness on top of the sacrificial layer of Polyvinyl alcohol (PVA) soluble in water, previously spin-coated on the glass carrier.

For the bottom electrodes of the memristor and the TFTs gate, radio-frequency (RF) magnetron sputtering was used to deposit a 70 nm thick Mo layer in an AJA ATC-1800 system with a flow rate of 50 sccm of Ar, a sputtering power of 175 W (3” target) and a deposition pressure of 1.7 mTorr.

A parylene-C layer was deposited through a chemical vapor deposition tool (CVD-PDS-2010) to protect the memristors bottom contact from the etching of the TFT dielectric. The patterning of this Mo-parylene-C bi-layer was achieved by photolithographic steps. Two masks were required, the first for the bottom contact of the memristors, where the parylene should remain, and then a second one, used after the etching of the parylene layer, for the TFTs gates. Reactive ion etching in a Trion Phantom 3 system was used with O_2 gas for the parylene layer and SF_6 for Mo.

The dielectric layer was a 175 nm thick multilayer based on SiO_2/TaSiO[46] deposited in RF magnetron sputtering in an AJA ATC-1800 system with a flow rate of 14 sccm of Ar and 1 sccm of O_2, a sputtering power of 200 W for SiO_2 and 100 W for Ta_2O_5 (2” targets), a deposition pressure of 2.3 mTorr, a substrate bias of 15 W and at 180 °C. The patterning of this layer was accomplished by reactive ion etching in the same Trion Phantom 3 system using SF_6 gas. The remaining parylene was then etched using O_2.

A lift-off procedure was then employed to pattern the IGZO, used as active layer for memristor and TFTs semiconductor. The IGZO thin film was deposited by RF magnetron co-sputtering from three ceramic oxide targets. The sputtering powers used on each target (all 2” diameter) were In_2O_3: 121 W, Ga_2O_3: 100 W, and ZnO: 50 W using a flow rate of 20 sccm of Ar and 5 of O_2. The deposition pressure was kept constant at 2.3 mTorr. The thickness was 80 nm confirmed by profilometer and the average In:Ga:Zn atomic composition of the deposited film was 2.5:1.0:1.5, for a normalized Ga concentration analysis by XPS argon cluster depth profiling. Detailed information on the materials characterization can be found in our previous work.[8]

The top Ti/Mo electrode of the memristors and source and drain of the TFTs was also patterned via lift-off. A thin 6 nm layer of Ti was deposited by e-beam evaporation in a homemade apparatus and a 70 nm thick Mo layer in an AJA ATC-1800 system with a flow rate of 50 sccm of Ar, a sputtering power of 175 W and a deposition pressure of 1.7 mTorr.

Annealing steps at 150°C were performed on a hot plate for 60 minutes after the IGZO patterning and again after the top electrodes patterning for TFTs, which require annealing for improved stability and performance.[46]

The peel-off was performed in deionized water. PVA becomes soluble and the polyimide detaches itself from the glass. The samples rested after the peel-off for 24 hours in ambient air before any electrical characterization.

The electrical characterization of the 1T1M cells, TFTs, and memristors was done using a Keithley 4200 SCS semiconductor analyzer connected to a Janis ST-500 probe station. For the memristors, the DC sweeps and the pulses were applied to the top electrode while maintaining the bottom electrode connected to ground. Pulse tests on the structures were conducted using the ARB module which allows

for a manual entry of the pulse schemes as well as synchronized pulse schemes with different amplitude, in this case used for word and source lines. For the VMM operations test, a Keysight B1500A semiconductor parameter analyzer connected to a Cascade Microtech EPS 150 manual probe station was used.

5.3 Results and discussion

5.3.1 1T1M cell

A material schematic of the fabricated 1T1M cell is presented in **Figure 5.1(a)**, highlighting the structures of both the TFT and the memristor. The devices were fabricated on a polyimide substrate. The first Mo layer serves as the bottom contact/Schottky barrier of the memristor and the gate for the TFT. A multilayer stack of SiO_2/TaSiO composes the dielectric for the TFT as shown elsewhere.[45,47] The multilayer stack as TFT dielectric is reported to result in both reliable and high performance IGZO TFTs with low-temperature processing that can successfully be implemented into flexible electronic applications. An a-IGZO layer is employed as the TFT semiconductor and the active layer for memristor. The optimization of this layer was performed by changing the oxygen flux in IGZO depositions until both TFTs and memristors could be fabricated with the same film without significant performance degradation. The TFTs transfer characteristics under different conditions can be consulted in **Figure C.2 -Appendix C.** Regarding the memristor, it was previously found that a decrease in oxygen flux during IGZO deposition results only in a small degradation of the I_{LRS}/I_{HRS} switching ratio, since the electrical properties are mainly influenced by the contacting materials.[8] A bi-layer of Ti/Mo is used for the source and drain of the TFT and the top/ohmic contact of the memristor. In **Figure 5.1(b)**, a micrograph of a fabricated 1T1M cell is shown.

An electrical schematic of the 1T1M configuration is presented in **Figure 5.1(c)**. The gate of the TFT is called word line (WL) and it acts as a switch, thus controlling if the TFT is on or off, and therefore if the memristor is selected or not. The drain terminal of the TFT is called source line (SL) and it can control the current flow to the memristor. The TFT source is connected to the memristor top contact and the memristor bottom contact is called the bit line (BL).

Figure 5.1(d) presents the memristor Set and Reset operations. Firstly, a voltage sweep from 0 V to -2 V, with a step size of 0.1 V, was applied to the shared node of the 1T1M cell (top contact of the memristor), while grounding the BL, making the device switch from a HRS to a LRS, therefore performing a Set. Afterwards, the sweep was performed from 0 to 2 V, making the memristor evolve from the LRS to HRS, this being the Reset operation.

In our previous studies, it was reported that the resistive state of the a-IGZO memristor is controlled by a potential barrier on the bottom interface, created due to Mo oxidation,[8,34] and that the switching is related to variations on the Schottky barrier profile.[48] At the Ohmic contact, the oxygen

getter Ti reacts with the switching oxide by extracting oxygen ions, creating a highly conductive interface region in the a-IGZO layer,[49] thus building an asymmetry in the oxide, resulting in the required memristive hysteresis loop.[50] For the TFT, the same IGZO layer can be used for the channel without degrading its performance due to the planar configuration. In addition, the peripheral circuit of the neuromorphic chip could be composed of the same IGZO-TFTs which would decrease the complexity of manufacturing at separate stages.

The memristor analog control of resistance states is forming-free and area-dependent, as can be confirmed in **Figure C.3 - Appendix C**, in which the Set and Reset processes are presented for different memristor areas along their I_{LRS}/I_{HRS} ratio. The current states clearly decrease in smaller memristors while the I_{LRS}/I_{HRS} ratio increases with downsizing. The memristor integrated in the 1T1M structure has an area of 4 µm^2.

The TFT transfer curves can be found in **Figure 5.1(e)**. The word line voltage (V_{WL}) was swept from -15 to 15 V, in a step size of 0.25 V, and the TFT linear regime is shown in the brown curve with a source line voltage (V_{SL}) of - 0.1 V. The light blue curve represents a V_{SL} of 8 V and the dark blue a V_{SL} of -8 V. All these measurements were performed while grounding the shared node of the 1T1M cell. A negative voltage applied to the TFT drain is not usual, but is, in this case, necessary since the a-IGZO memristor has a bipolar characteristic in which the Set happens for negative polarities and Reset for positive polarities when inputting at the top contact. In **Figure C.4(a) - Appendix C**, the output curve of the TFT used for integration in 1T1M cells is presented. The TFT is quite large with a W/L of 240/20 µm, which will increase the unit cell area in the active crossbar when compared with the passive crossbar composed solely of memristors. Nevertheless, as explained before, if the memristor can be fabricated in smaller areas, increasing I_{LRS}/I_{HRS} ratio and decreasing the current state, a smaller TFT can also be employed. As an example, **Figure C.4(b) - Appendix C** shows the transfer curves in the linear and saturation regimes of a TFT fabricated with the exact same process as the ones integrated, but with W/L of 4/2 µm. Moreover, the structure presented here is a bottom gate one as a proof-of-concept. Different designs can result in higher density.

For ANNs applications, plasticity is the key characteristic and the synaptic element, in this case the memristor, should present a linear and symmetric potentiation and depression for the highest accuracies in any task. Potentiation consists in enabling the connection between two neurons and therefore increasing its synaptic weight, while depression is the restriction of the neuron's connection and decrease of the synaptic weight. Both processes are simulated by applying negative or positive pulses to one of the memristor terminals and thus increasing/decreasing the device's current state. In a previous study, we have reported a complex spiking scheme in which the amplitude and width of pulse was increased in a linear fashion to gain a linear and symmetrical potentiation and depression of a single RS device.[8] However, it is notable that if an actual crossbar was to be built, it would most likely suffer from sneak-path current issues and the selection of a single cell could not be possible. Strategies have been proposed to mitigate this problem such as the 1/2 and 1/3 voltage bias schemes

(VBS).[11,12] In **Figure C.5 - Appendix C**, an experimental study can be consulted in which these approaches were employed on the a-IGZO memristor. It was found that, even if reducing the sneak-path current, these approaches would not be sufficient to completely suppress it in large crossbars. Moreover, a complex spiking scheme involving increasing both amplitude and width in each pulse will complicate the required peripheral circuit for the modulation of states.

The 1T1M integration in active crossbars is crucial for the development of an efficient hardware technology for ANNs applications since it effectively solves the sneak-path current issue. In **Figure 5.1(f)**, the pulse scheme for potentiation and depression on a 1T1M configuration is presented for 200 pulses. For potentiation, 1.2 ms Set pulses were employed. To ensure the required linear response, the amplitude of the Set pulse was linearly increased by applying an incremental amplitude spiking scheme at the word line that started at -1 V (1st pulse) and increased to 15 V (100th pulse), as suggested elsewhere.[16] Simultaneously, on the source line an identical spiking scheme was used consisting of - 8 V pulses. The bit line was grounded during the tests. A read pulse was carried out at - 0.1 V at the source line and 15 V at the word line followed each Set pulse. For depression, a combination of 2 pulses in each step comprising a full Reset and a Set were applied as shown previously.[22] For the 16 ms full Reset pulse, the word line was at 15 V while the source line was pulsed with 8 V and the bit line was grounded. This full Reset was applied to decrease the memristor current state to the HRS. The current state of the memristor was then modulated by the set pulse, applied on the contrary order of potentiation. Therefore, at the word line depression starts with a 15 V pulse (101st pulse) and ends with a -1 V pulse (200th pulse), while at the source line the pulse amplitude remains the same. This strategy ensures the necessary symmetry between potentiation and depression. The TFT current output during potentiation and depression can be found in **Figure C.6 - Appendix C**.

In **Figure 5.1(g)**, the potentiation and depression results, using the previously explained synaptic weight update scheme, are presented. Each point in this graph represents the read step performed after each Set pulse. The memristor current state was read at 0.1 V before the application of the pulse scheme on the 1T1M structure, after potentiation and after depression to validate its successful modulation. In **Figure C.6 - Appendix C**, the results can be accessed. The 1T1M cell under much simpler pulse scheme provides a linear and symmetrical response, as targeted, extremely low C2C variability, in addition to solving the sneak-path issue. However, the 1T1M cell has an energy consumption of more than one order of magnitude compared to the only-memristor (1M) cell, mostly due to a slower operation and the need of larger pulses. **Figure C.7 - Appendix C** provides the comparison of energy consumption analysis for synaptic and read pulses for the 1T1M cell and the correspondent 1M cell. This increase in energy consumption is directly related to the W/L of the TFT as reported previously.[52] A smaller L would enable faster pulses for the modulation of the memristor's current state and the read process. Lower conductance at memristor level is, therefore, desired, enabling scaling to larger crossbar arrays, power efficiency and lower voltage drops at interconnections.[53]

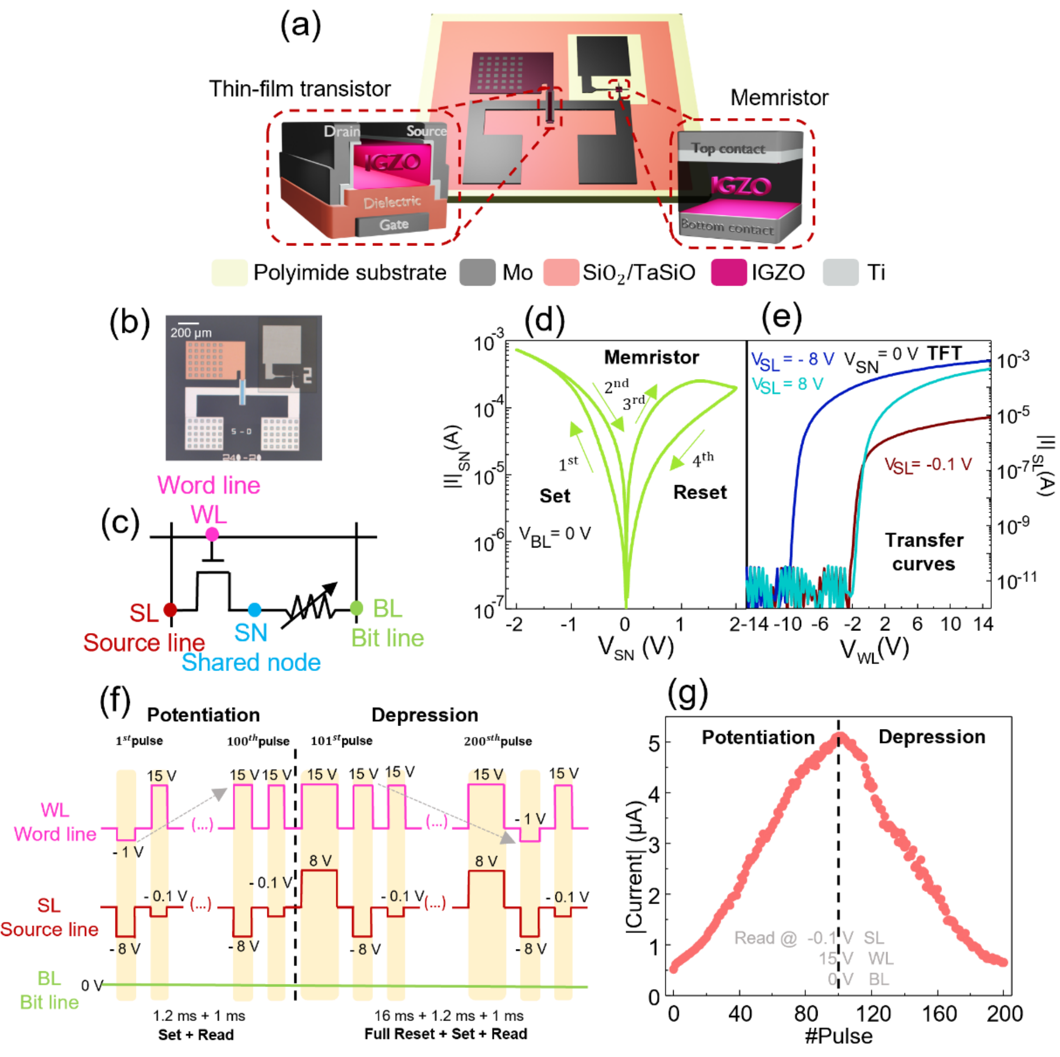

Figure 5. 1 1T1M cell structure and synaptic performance. (a) Schematic illustration of the 1T1M cell showing the TFT and the memristor material structures and shared layers. The memristor is in a cross-point configuration and has an area of 4 µm^2 while the TFT is in a bottom-gate configuration and has a W/L of 240/20 µm. (b) Optical microscope image of one fabricated 1T1M cell (scale bar, 200 µm). (c) Schematic diagram of the 1T1M equivalent circuit with the TFT gate as the word line (WL), the TFT drain as the source line (SL), the TFT source connected to the top contact of the memristor in a shared node (SN) and the bottom contact of the memristor as the bit line (BL). (d) I–V characteristic of the memristor in the 1T1M cell Set and Reset for negative and positive voltages applied to the SN, respectively with BL grounded. (e) Transfer curves of the TFT with V_{SL} of - 0.1 V (applied for the read step in synaptic tests), V_{SL} of 8 V (applied for the full reset step) and V_{SL} of - 8 V (applied for the set pulses), with V_{SN} grounded. (f) Schematic illustration of the pulse scheme applied to WL, SL and BL for potentiation and depression tests. (g) Potentiation and depression results. Each point represents the current measured immediately after the set pulse, read with 15 V at the WL, -0.1 V at the SL and 0 V at the BL.

5.3.2 1T1M Crossbar simulation

In addition to a linear and symmetric plasticity characteristic, low C2C variability is crucial for a high performance in crossbars. Therefore, 50 cycles of the previously explained pulse scheme for

potentiation and depression were performed on the 1T1M cell. The results can be found in **Figure 5.2(a)** with the mean current in orange. The experimental Cumulative Distribution Function (eCDF) lookup tables of the conductance change (ΔG) within the 50 cycles of potentiation/depression as a function of conductance for the Set and Reset processes are displayed is **Figure 5.2(b)**. For a certain conductance on the x axis, the CDF colormap shows the probability for ΔG to be less than or equal to the value on the y axis. The lowest C2C variability would be represented with a straight line at ΔG = 0 separated with red below zero and blue above zero. C2C variability is, therefore, extremely low.

To further confirm the effect on a crossbar performance of the linearity, symmetry and low C2C variability of the plasticity characteristic accomplished here, CrossSim was used.[54] A simulation of a three-layer (input, hidden, and output) perceptron neural network using a handwritten digit dataset (MNIST) was performed for pattern recognition applications. The number of neurons on the input, hidden, and output layers used 784, 30, and 10, respectively, as shown in **Figure 5.2(c)**. Each neuron in the input layer is connected to all neurons in the hidden layer through synapses with a given synaptic weight value (W) and each neuron in the hidden layer is connected to all 10 output neurons. The corresponding crossbar schematic can be found in **Figure 5.2(d)**, in which the inputs are through the source lines corresponding to the neurons on the input layer and the word lines act as a selector. The conductance of each 1T1M cell is corresponding to the synaptic weight and the bit lines correspond to the outputs.

The default test provided by CrossSim uses a 25%–75% range of the I_{LRS}/I_{HRS} window within the 50 cycles of potentiation and depression and the training epochs can be chosen. In **Figure 5.2(e)** and **5.2(f)**, the pattern recognition accuracies achieved for different training epochs for our device and the software benchmark can be consulted. An extremely high 93.28 % accuracy was obtained for 10 training epochs. It is important to note that this simulation was performed to assess the impact of linearity, symmetry and C2C variability of the synaptic characteristic of the 1T1M cell on the pattern recognition accuracy. It assumes no crosstalk effect, no line resistance and full retention of states. **Figure C.8 - Appendix C**, retention data of 7 states can be observed for 10^3 s. The states remain distinct despite some retention loss, expected from the interface-type of resistive switching.[55,56] The retention time is, therefore, the remaining challenge especially for these types of resistive switching. A strong non-linearity is required to tackle the issue of voltage-time dilemma.[57] In this respect the key answer relies on engineering of the electrode interface. Similar studies are still required for IGZO memristors before implementation of full system. Therefore, the resulted 93.28 % from the simulation is not to be regarded as the final accuracy of a manufactured three-layer neural network composed of IGZO 1T1M cells, but rather an indicative and comparable value to evaluate the synaptic plasticity. In a previous study, the CrossSim simulation was also carried out with the experimental 50 cycles of potentiation and depression using only memristor of the exact same structure as here and resulted in a 91.82% of pattern recognition accuracy. Here, the 1T1M integration improves linearity, symmetry and C2C variability due to a current pulse input on the memristor controlled by gate of the transistor.[7,8]

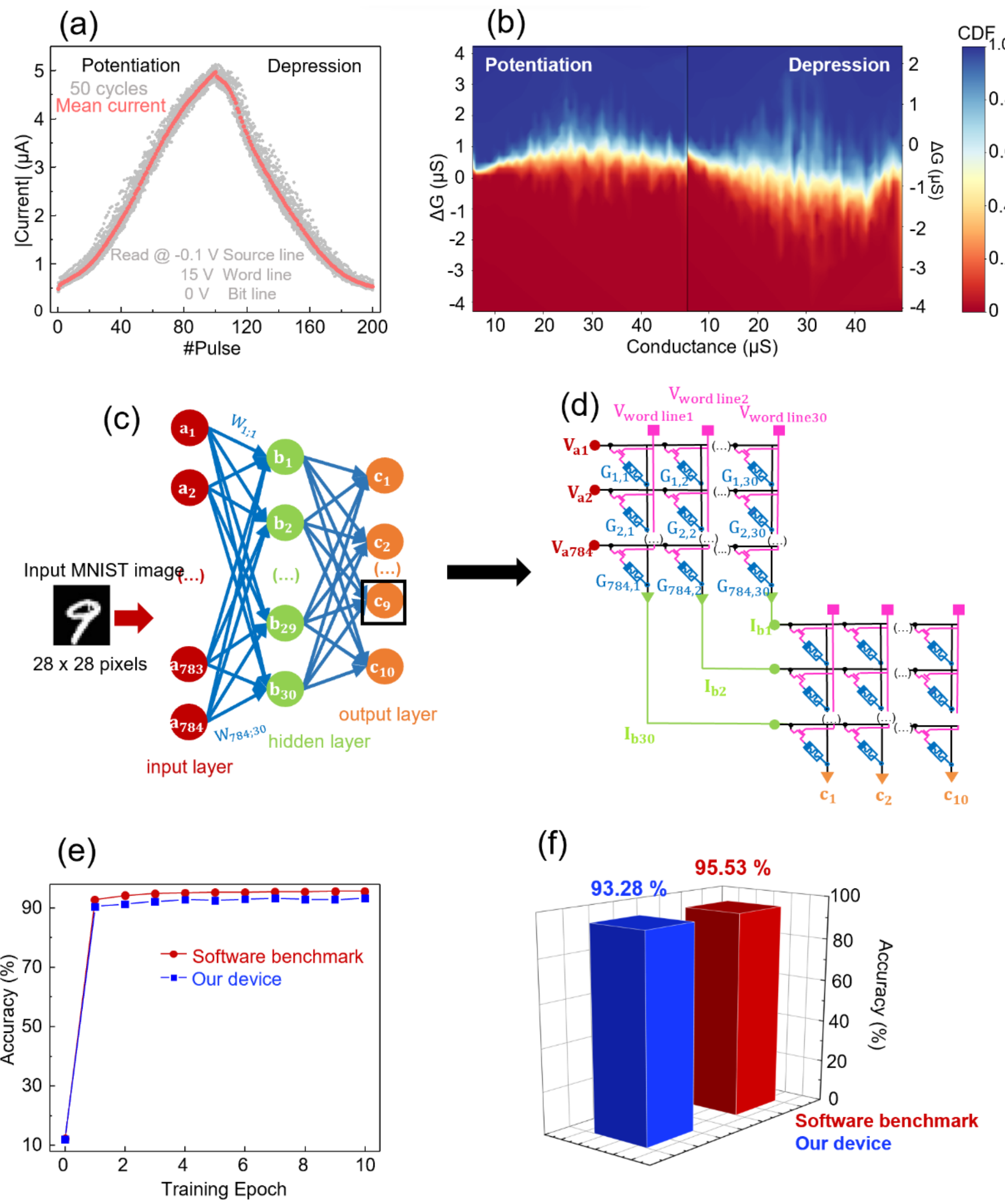

Figure 5. 2 1T1M CrossSim simulation results for pattern recognition applications. (a) 50 cycles of 200 pulses of potentiation and depression in grey and the mean current in orange. Each point represents the current immediately after the partial set pulse, read with 15 V at the word line and -0.1 V at the source line. (b) Experimental Cumulative Distribution Function (eCDF) lookup tables of the conductance change (Δ G) within the 50 cycles of potentiation/depression as a function of G for potentiation and depression. (c) Schematic illustration of a three-layer perceptron neural network (the number of neurons used in the input, hidden, and output layers is 784, 30, and 10, respectively. (d) Schematic illustration of the equivalent active crossbar. (e) Pattern recognition accuracies achieved for different training epochs for our device and the software benchmark. (f) Accuracy for pattern recognition achieved with the 50 cycles of potentiation and depression presented in c of 93.28 %, compared with the 95.53 % of the software benchmark.

5.3.3 1T1M Crossbar VMM operations

As mentioned, an important aspect, not considered in crossbar simulations, is the sneak-path current issue which causes crosstalk interference between nearby cells. As a proof-of-concept, a 4 × 4 1T1M crossbar was fabricated to evaluate this matter. The transfer curves in the linear regime of the individual TFTs as well as the pristine state of the memristors integrated on the crossbars can be consulted in **Figure C.9 - Appendix C**. In fact, low D2D variability is crucial for a high operation accuracy. D2D variability is characteristically low in area-dependent switching memristors since it is not dependent on filament reproducibility.[55] Moreover, the IGZO-TFT technology is advanced, providing low D2D variability on the TFT element as well.

In **Figure 5.3(a)**, a schematic of the active crossbar matrix is presented, the word and bit lines are parallel to each other, and the source lines are perpendicular to these. Microscope pictures of the fabricated crossbars are presented emphasizing a 1T1M cell in **Figure 5.3(b)**. Its corresponding ANN scheme is shown in **Figure 5.3(c)**. The input neurons, here displayed as a_1, a_2, a_3 and a_4, translate into numbers, which in the crossbars is embodied by a voltage vector V = [V_{S1}, V_{S2}, V_{S3}, V_{S4}] applied at the source lines. Each synaptic weight, represented as W in **Figure 5.3(b)**, is the conductance state of each cell on the crossbar (G). Finally, the output neurons, b_1, b_2, b_3 and b_4, are the collected output current (I) in each bit line. To accurately execute the ANN tasks, the crossbars should, therefore, perform the VMM operations as a result of Ohm's law: I = G x V, leading to a matrix to vector multiplication as formally presented in **Figure 5.3(d)**.

The experimental conductance values, mapping the cells of the crossbar, are presented in the colormap of **Figure 5.3(d)** and range from 9 to 54 µS. These measurements were performed in each cell independently, prior to the VMM tests, and consisted of a -0.1 V reading pulse set at the source line and 10 V at the word line. To perform VMM, a voltage vector [V_{S1}, V_{S2}, V_{S3}, V_{S4}] with V_{S1} = 0.30 V, V_{S2} = 0.15 V, V_{S3} = 0.15 V and V_{S4} =0.30 V was applied to the source lines. V_{S1} and V_{S4} were the same value as well as V_{S2} and V_{S3} to facilitate the measurements (more details can be found in **Figure C.10 - Appendix C**. A constant 10 V bias was applied to the word lines and the output current was then collected at each column bit line. A relative low error of less than 4 % was obtained for all 4 bit lines when confronting the measured output currents and the expected analytical values.

The precision of the VMM operations was further validated by changing the input voltage vector, multiplying it with an α parameter that was swept uniformly from -1 to 1, following a previously reported approach.[2] The results are reported in **Figure 5.3(e)**, in which the measured output current is compared with the analytical one. The relative error remains below 10%, as can be confirmed by **Figure 5.3(f)**, and its increase is mostly on the lowest measured currents, which can be related to the sensitivity of the equipment. The a-IGZO thin-film active crossbars can, therefore, accurately perform VMM operations required for ANN applications hardware, successfully suppressing the sneak-path current issue.

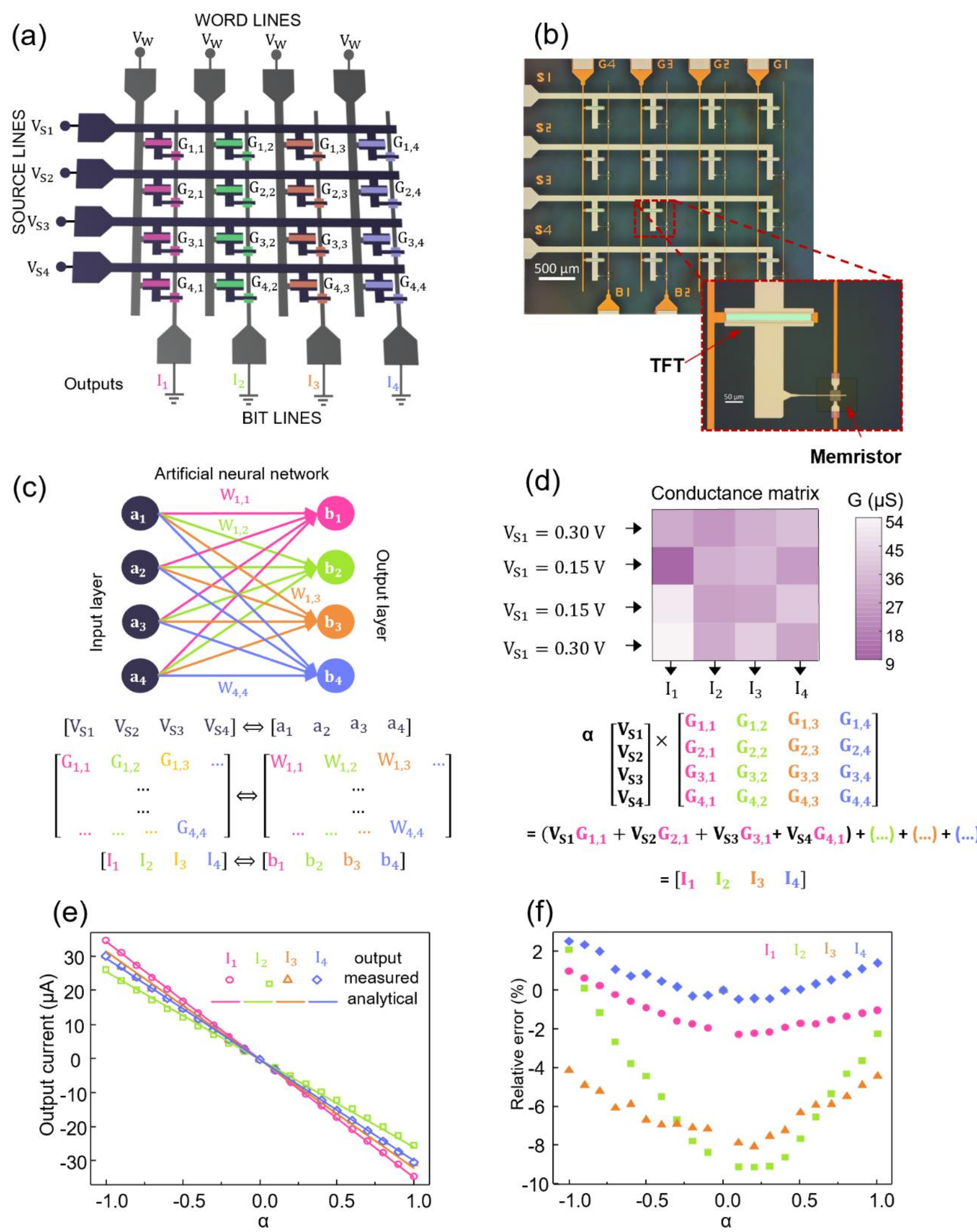

Figure 5. 3 VMM operations with 1T1M crossbar. (a) Schematic illustration of the 4×4 active crossbars with input vectors, word lines and output vectors specified. (b) Microscope images of 1T1M crossbars (scale bar, 500 µm) and a single 1T1M cell integrated in the crossbars (scale bar, 50 µm). (c) Schematic illustration of the equivalent artificial neural network and its execution. (d) Experimental conductance values colormap for all cells of the crossbar and Ohm's and Kirchhoff's laws applied analytically to the 4×4 crossbars. (e) Experimental results of the VMM operations, consisting in the measured current at each bit line as a function of α parameter, adjusting the amplitude of the input vector (V = α x [0.30, 0.15, 0.15, 0.30] V. α was

swept uniformly from -1 to 1. The measured values are compared with the analytical results disclosing a good accuracy. (f) Relative errors of the VMM operations related to the α[0.30, 0.15, 0.15, 0.30,] input vector.

This 4 x 4 1T1M crossbar can physically perform 32 operations by one single read process, therefore the efficiency of the circuit is determined by the speed of the current read step. One OPS is defined as one operation (multiply or add) per second and is used to estimate power efficiency.[21] If the previously described pulse scheme is applied, then the read process will be 1 ms and the 4 x 4 1T1M crossbar has 32 000 OPS. The scaling down of cell unit in larger crossbars would greatly increase this value.

5.3.4 Flexible 1T1M endurance

The endurance of the cells is also critical to ensure a stable performance over time. Bending tests were performed on the flexible crossbars to assess its impact on the behavior of the cells. In **Figure 5.4(a)**, a picture taken through a magnifying glass is shown where the flexibility of the substrate is demonstrated. In fact, the 6 µm polyimide substrate ensures a complete suppleness to any surface. In **Figure 5.4(b)**, the potentiation test response, in one cell, using the described pulse scheme, is presented before peel-off of the polyimide from the glass, after the peel-off, and after being subjected to a 30 minutes static bending with a curvature radius of 15 mm. After bending, the conductance state slightly increases. This can be explained by a shift in the TFT turn-on gate voltage to more negative values or an increase in the memristors current states.

Afterwards, a potentiation test was performed immediately after 1, 2, 5, 10, 20, 50 and 100 bending cycles with the same 15 mm radius curvature. **Figure 5.4(c)** displays the HRS and LRS achieved in each case. Before each test, a Reset was performed through DC sweep on the memristor. After the second bending, the conductance state increases once more. However, after 10 bending cycles the HRS and LRS stabilize and even at 100 bending cycles, the cell performance shows no further degradation.

Following the bending cycles, the bending curvature radius was gradually reduced from 15 mm to 1.25 mm and another potentiation test was performed after each trial. The results are displayed in **Figure 5.4(d)** and show no relevant variation on the HRS and LRS for different bending radii. The final potentiation characteristic, retrieved after all bending tests, is displayed in orange in **Figure C.5(b) - Appendix C** and shows a complete recovery to the before peel-off characteristic.

On the individual devices, the memristor presented no relevant variability after all the bending tests. The TFT performance shows a variation in the turn-on voltage towards more positive gate voltages immediately after the peel-off, which explains the decrease on the conductance of the cell after peel-off. However, the turn-on voltage after all the bending tests decreases closer to its initial, before-peel-off value, indicating a recovery and explaining the stability presented in the following cell bending

cycles. The TFTs transfer curve in the linear regime and the I-V sweeps for Set and Reset of the memristor, before and after peel-off and after all the bending cycles, can be found in **Figure C.11 - Appendix C**. Increased trapping sites at the interface of IGZO and dielectric is assumed as the cause of the positive threshold voltage shift from before and after peel-off, most likely trapped moisture at nanocracks,[58] caused by the peel-off process itself performed with deionized water. The shift to more negative turn-on voltages after bending indicates a recovery of the device to its natural before-peel-off state, in agreement with the final potentiation characteristic showing unsignificant variability when compared to the before and after peel-off process. The encapsulation of devices or an annealing step performed after peel-off would result in improved TFT characteristics.

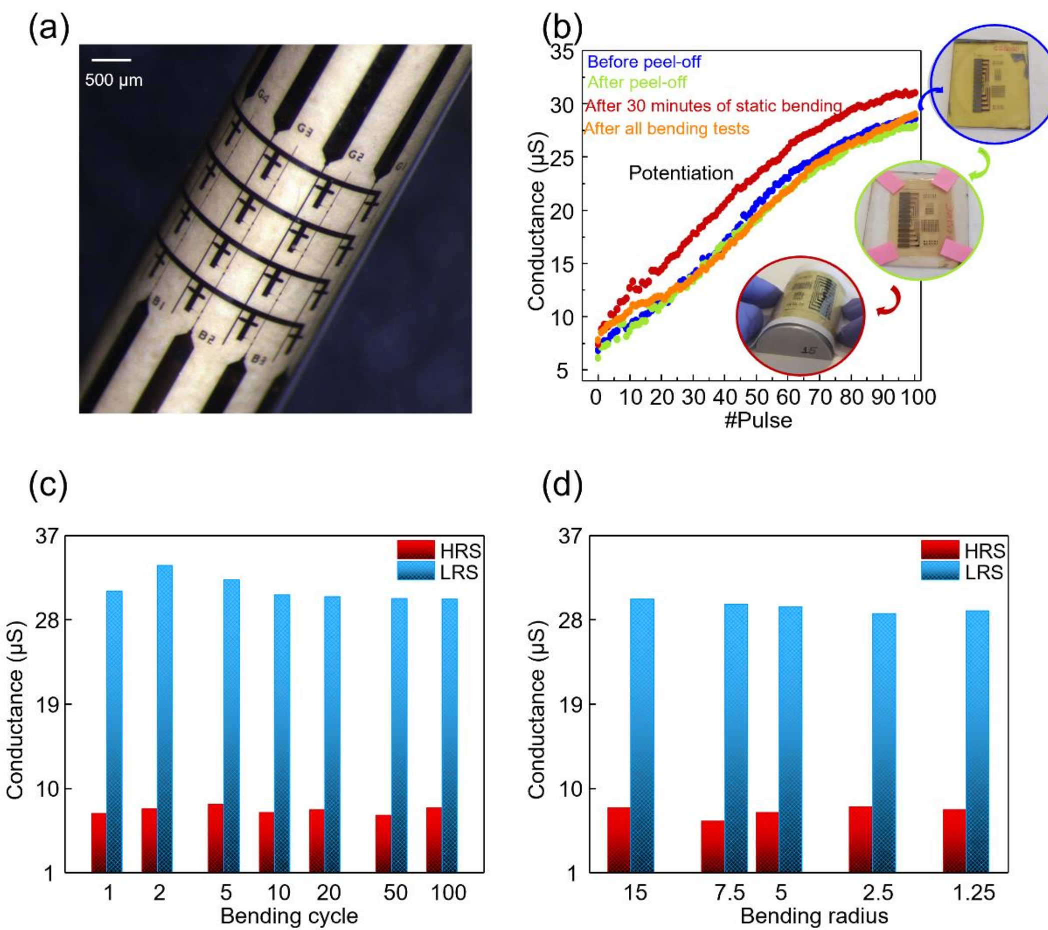

Figure 5. 4 Flexible 1T1M endurance through bending tests. (a) Flexible crossbar picture through magnifying glass. (b) Potentiation performance results of one cell before and after peel-off, after 30 minutes of static bending with a 15 mm curvature radius and after all bending tests, both cycles and radius, tests. (c) HRS and LRS of the potentiation characteristic of one cell after 1, 2, 5, 10, 20, 50 and 100 bending cycles with a 15 mm radius. (d) HRS and LRS of the potentiation characteristic of one cell after bending with a 15, 7.5, 5, 2.5 and 1.25 mm curvature radii.

5.4 Conclusions

In conclusion, a thin-film a-IGZO 1T1M 4×4 crossbar was successfully developed on a flexible polyimide substrate allowing for IoT applications and well suited for wearable applications. The TFT and memristor were fabricated at the same level, using the same processing steps and sharing the same material for all layers, which implies an improved interconnectivity between cells and a cost-effective approach.

The 1T1M plasticity characteristic for ANNs shows a linear and symmetrical weight update in potentiation and depression tests using a simple identical spiking scheme, as required for high accuracies in any given task. Accordingly, the pattern recognition accuracy of the MNIST handwritten digits dataset, for crossbar-based online training using CrossSim simulation, reveals an accuracy of 93.28%.

The crossbars were found to be resistant to the bending tests and vector-matrix multiplication operations were experimentally performed in the 4×4 active crossbars with a relative error, from analytical to measured, of less than 10%, effectively suppressing the sneak-path current issue and revealing the immense potential for a cost-effective, efficient, flexible and large-scale ANNs hardware, provided that the crucial figures of merit of a neuromorphic system such as scalability, speed and power efficiency are optimized.

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CHAPTER 6

RESISTIVE SWITCHING MECHANISM OF IGZO MEMRISTORS WITH EIGHTWISE POLARITY

The systematic study of resistive switching (RS) mechanisms of memristive devices is crucial for the development of reliable physical models, required for circuit integration and neural networks hardware applications. This work investigates the RS behavior in MoO_x/IGZO junctions, demonstrating the formation of a Schottky barrier that enables area-dependent switching with eightwise polarity. We explore the impact of fabrication processes, including annealing and plasma treatment on the bottom Mo electrode, showing that these adjustments can produce devices with the pristine state in the low-resistance state (LRS) or high-resistance state (HRS). Additionally, it is demonstrated that while changing the top contact primarily influences the I_{LRS}/I_{HRS} ratio, modifying the bottom contact can shift the switching mechanism to filamentary type. The typical relaxation decay is found to be caused by reoxidation of a previously oxygen-deficient region in IGZO, close to the interface. Accordingly, incorporating an Al_2O_3 layer between IGZO and MoO_x significantly improves retention properties. Our results suggest that the RS is driven by Schottky barrier modulation at the interface, induced by the exchange of oxygen ions between IGZO and MoO_x, which alters the depletion width and barrier height, in complete agreement to other eightwise switching devices.

The results presented in this chapter are being prepared to be submitted as:

M.E. Pereira, J. Deuermeier, T. Mingates, P. Carvalho, T. Calmeiro, M. Cortinhal, E. Fortunato, R. Martins, P. Barquinha and A. Kiazadeh, "**Comprehensive analysis on the eightwise resistive switching mechanism of a-IGZO based memristors**", in preparation, 2024.

6.1 Introduction

Resistive switching (RS) devices, also known as memristors, have attracted significant attention in recent years due to their immense potential to revolutionize artificial intelligence (AI) hardware, which, to this day, is still based on the outworn CMOS technology and still suffering from the limitations of the Von Neumann's architecture. Memristors can alter their resistance state in response to the applied electric field, exhibiting either volatile or non-volatile behavior. This capability makes them ideal to be employed as artificial synapses in brain-inspired technologies, where learning and forgetting processes are incorporated, in endeavors to mimic the human brain's energy-efficiency and fast operations.

Allowing miniaturization to the nanometer scale,[1] RS devices are built in vertical structures usually composed of an oxide layer sandwiched between two metal electrodes. Typically, one or more conductive filaments (CFs), usually composed of oxygen vacancies (VOs), located inside the oxide and connecting the top to the bottom electrode are appointed as the cause for RS. These CFs are generated in an electroforming process in which a high electric field is applied to the device, causing a soft breakdown of the insulating material and changing the resistance state of the device to its first low-resistance state (LRS). The CFs can then be partially dissolved, and then restored, by application of reversed/non-reversed bias, changing the resistance state from LRS to high-resistance state (HRS), in a process called Reset, and from HRS to LRS, in a process named Set, by local redox processes.[2–4] Due to the randomness of filament formation, these devices often suffer from poor reproducibility and high cycle-to-cycle (C2C) variability,[5,6] which can be improved by confining the CF to the entire electrode area.[7] Moreover, several works have shown that multi-level cell (MLC) operations can be achieved in filamentary-type of switching by the manipulation of filament width.[8,9] However, the transition between discrete number of states is usually abrupt which hinder their possible applications as true analog devices.

Unlike filamentary RS, area-dependent switching presents a gradual conductance change in the device. Either interface or bulk-related, this type of switching is characterized by a uniform distribution of mobile defects within the oxide, which results in inherent high reproducibility and low C2C variability.[10] In interface-RS a reaction takes place at the electrode/oxide interface(s), while bulk switching pertains to changes in the dopant distribution within the oxide bulk.[11,12] Additionally, the learning and forgetting processes of the human brain are better reproduced by devices with area-dependent switching, wherein the retention of programmed states follows a relaxation process that closely mirrors the forgetting process of the human brain.

Several materials have been proposed as RS layer for such devices such as STO,[13] ZTO,[14,15] PCMO,[16] CoO_x,[17] IGZO,[18] etc. Since IGZO is also successfully employed in thin-film transistors (TFTs) in panel display applications,[19,20] it is the ideal choice for 1-transistor-1-memristor (1T1M) strategies to

solve crosstalk in memristive crossbars.[21–24] IGZO is an amorphous oxide semiconductor (AOS), a class of materials that offer several advantages related to their excellent stability, easy and low cost manufacturability and possible miniaturization to the nanometer scale due to the lack of grain boundaries.[25,26] Moreover, AOS materials are transparent and allow for room temperature processing, which means flexible devices can be designed for IoT and wearable applications with optoelectronic properties.[27]

Regarding IGZO-based memristors, both filamentary and area-dependent switching can be exhibited depending on the choice of materials for electrodes and the oxide cation/oxygen composition.[18,28–30] In fact, the movement of charge carriers in IGZO is primarily due to VOs which means the conductivity of the film can be controlled over 8 orders of magnitude by regulating the oxygen/cation composition.[31,32] As such, the physical mechanism responsible for area-dependent RS has to be analyzed for each particular device, taking into account its specific electrical behavior and material structure. Nonetheless, it is highly necessary to make sense of the literature results which seems to report on contradictory conclusions, as can be inferred from **Table 6.1**.

Bulk switching has been proposed for memristors using an oxygen-rich and an oxygen-poor IGZO layers. The movement of oxygen ions induced by electric field would change the relative thicknesses of these layers, thus modulating the device conductance.[33,34] In some devices, a forming process before Set and Reset operations is required, which is ascribed to a filament formation composed of positively charged VOs (VOs^{2+}). It is then assumed that this CF is not destroyed between the gradual change of RS, still attributed to bulk switching caused by oxygen ion movement.[35] In other studies, however, the addition of a SiO_2 layer would shift the device's RS mechanism from bulk to interface-type of switching, ascribed to barrier modulation by electron trapping and detrapping.[36,37]

Interface-type of switching is mostly, attributed to a Schottky/tunnel barrier modulation at the interface(s) of the device. The confusion seems to arise regarding the cause of the barrier modulation. In the previously mentioned study, the barrier was identified at the SiO_2/IGZO interface. It is then proposed that the cause for RS is the ionization and neutralization of VOs. When positive voltage is applied to the top contact, VOs near the barrier have a higher energy state than the Fermi level, and become ionized to VO^{2+}, detrapping electrons and lowering the barrier's height. In contrast, electrons can easily reach the top interface with negative bias, neutralizing VOs and increasing the barrier height.[36,37] When the top Pd contact was replaced by Ti/Au, Set and Reset operations remained at the same voltage polarity and no forming was necessary, which corroborates the authors assertion that the SiO_2/IGZO interface is the active one. However, the I-V characteristic seems to have significantly changed.[38] In another structure, Pd/IGZO/Mo, a Schottky barrier was identified at the Pd/IGZO interface. The migration of VOs to the active interface would decrease the Schottky barrier height, inducing an increase in conductance state. Here, negative voltage applied to the active Schottky-type electrode would perform Set and positive voltage would perform Reset, known as "counter-eightwise" switching (to note it is mentioned reversely on the original paper since voltage was applied to the top electrode and the

Schottky interface is at the bottom).[39] Later, the physical mechanism for RS in this same structure was further elucidated as a combination of electronic and ionic processes. During Set, the migration of VOs would take place towards the Pd/IGZO interface and VOs would become VO^{2+}, decreasing the Schottky barrier and detrapping electrons that can participate in the conduction. In contrast, VOs would be neutralized with reversed bias, due to the drift of O^{2-}, while the Schottky barrier height would be increased.[36] However, in another work on the same stack, the ionic process is disregarded and electron trapping and detrapping due to ionization of VOs is once again pointed as the cause for barrier modulation. In the latter work, it is also mentioned that retention properties are improved by the addition of an Al_2O_3 layer at the top ohmic junction, which is explained by the authors with its suppressing effect in oxygen diffusion.[40]

More recently, an Al/Al_2O_3/IGZO/Al structure was presented in which RS mechanism was attributed to barrier modulation at the Al_2O_3/IGZO interface, due to ionization and neutralization of VOs.[41] A different explanation was provided for RS at ITO/IGZO interface, in which the movement of VO^{2+} towards the ITO/IGZO interface would form a depletion region and the increase and decrease of its width, due to ionization and neutralization of VOs, would cause Set and Reset operations.[42]

Table 6. 1 Literature on area-dependent switching shown by IGZO memristors. Only the works which provided an explanation for the RS phenomenon were considered. The active interface mentioned is the one appointed by the original authors as the relevant interface for RS. NA- not applicable.

Type of switching	Memristor structure	Forming	Active interface	8W or C8W	Explanation for RS	Ref.
Bulk	Pt/$IGZO_x$/$IGZO_y$/Pt	No	NA	NA	Migration and diffusion of oxygen ions in the IGZO double layer	33
Bulk	p^+Si/$IGZO_x$/$IGZO_y$ /Cu	No	NA	NA	Migration and diffusion of oxygen ions in the IGZO double layer	34
Bulk	p^+Si/IGZO/Pd	Yes	NA	NA	Migration and diffusion of oxygen ions in the IGZO layer	35
Interface	p^+Si /SiO_2/IGZO/Pd	Yes	SiO_2/IGZO	C8W	Barrier modulation by electron trapping and detrapping	36, 37
Interface	p^+Si/SiO_2/IGZO/Ti/Au	No	SiO_2/IGZO	C8W	Barrier modulation by electron trapping and detrapping	38
Interface	Pd/IGZO/Mo	No	Pd/IGZO	C8W	Schottky barrier modulation by migration of oxygen ions inside the IGZO	39
Interface	Pd/IGZO/Mo	No	Pd/IGZO	C8W	Schottky barrier modulation by migration of oxygen ions inside the IGZO + electron trapping and detrapping	36
Interface	Pd/IGZO/Mo	No	Pd/IGZO	C8W	Schottky barrier modulation by electron trapping and detrapping	40

Interface	Pd/IGZO/Al_2O_3/Mo	No	Pd/IGZO	C8W	Schottky barrier modulation by electron trapping and detrapping	40
Interface	Al/Al_2O_3/IGZO/Al	No	Al_2O_3/IGZO	C8W	Barrier modulation by electron trapping/detrapping	41
Interface	ITO/IGZO/Ag	No	ITO/IGZO	C8W	Depletion region width modulation by electron trapping/detrapping	42
Our work	Mo/MoO_x/IGZO/Ti/Mo Mo/MoO_x/IGZO/Mo Mo/MoO_x/IGZO/Ti/Au	No Yes No	MoO_x/IGZO	8W	Schottky barrier modulation by exchange of oxygen ions between MoO_x and IGZO	43, 44, 45

In our previous studies, we proposed an IGZO-based memristor compatible with IGZO TFTs. To fully showcase the tremendous potential of our device for IoT and wearable applications, a flexible crosstalk-free 1T1M crossbar was presented. The memristor presented rectifying behavior in the pristine state, which was attributed to a Schottky barrier formed between the IGZO and highly oxidized MoO_x at the bottom interface.[43,45] Therefore, it was concluded that the principle behind the RS is a change of Schottky barrier profile.[44] Assuming that the Schottky-type electrode has been identified correctly in all of the mentioned studies for interface-type of switching in IGZO memristors, "eightwise switching" has only been demonstrated by our works. This type of switching cannot be explained by electron trapping/detrapping or the model of purely internal redistribution of VOs due to the Set and Reset polarities. It has been shown, for other active layer materials, such as TiO_x,[46] TaO_x[47] and STO,[48] that the barrier modulation is, in such cases, due to an interface exchange reaction of oxygen and VOs in combination with ion movement in the oxide bulk.[49–51]

In this study, a comprehensive analysis on memristors with MoO_x/IGZO as the Schottky-type electrode and 8w switching is further conducted. Specifically, here, we evaluate the effects of low-temperature post-fabrication annealing and the plasma treatment on the bottom contact. We also examine the impact of the top and bottom contacts on RS properties to prove which active interface is responsible for RS. It is found that the top contact does not alter the RS behavior, impacting only the I_{LRS}/I_{HRS} ratio. On the contrary, changing the bottom contact from Mo to Al completely alters RS from analog to abrupt, indicating a shift to filamentary-RS. Additionally, introducing a thin layer of Al_2O_3 at the Schottky barrier interface is shown to improve retention of programmed states. Based on the experimental results, we confirm that the modulation of the Schottky barrier at the bottom interface of the device is the cause for RS and we propose that the exchange of O^{2-} ions at this interface modulates the depletion width and Schottky barrier height, as previously proposed for other 8w switching devices.

6.2 Experimental

Corning Eagle glass was used as substrate for the fabrication of the memristors in crosspoint structures, which had been pre-cleaned through multiple ultrasonic baths in acetone and isopropanol, followed by rinsing with deionized water and drying with nitrogen gas. For the devices with Mo as bottom electrode, radio-frequency (RF) magnetron sputtering was used to deposit a 70 nm thick layer in an AJA ATC-1800 system using a flow rate of 50 sccm of Ar, a sputtering power of 175 W (3" target) and a deposition pressure of 1.7 mTorr. For patterning, SF_6 gas was used for reactive ion etching in a Trion Phantom 3 system. For the devices with Al as bottom electrode, patterning was achieved via a lift-off procedure and a 70 nm thick layer was deposited by e-beam evaporation in a homemade apparatus. The oxygen plasma treatment carried out in some of the samples on the bottom electrodes was performed inside the sputtering chamber prior to IGZO deposition. The parameters used for the treatment were a flow rate of 20 sccm of O_2 gas with 10 W of substrate bias and an RF power to the Ga2O3 target of 40 W to create the plasma for 10 min in a 20 mTorr pressure (shutter closed). ALD was used to deposit 1, 2, 3 or 5 nm of Al_2O_3 on some of the samples at 200ºC in a BENEQ TFS-200, using alternative pulses of trimethylaluminium (TMA) and DI water, with pulse/purge step durations of 150 ms/650 ms (TMA) and 150 ms/1000 ms (DI water). This layer was then patterned by dry etching in the same system as Mo by a combination of CF_4 and O_2 gases. Three ceramic oxide targets (all 2" diameter) were then used in RF magnetron co-sputtering to deposit 50 nm of IGZO using powers of In_2O_3:121 W, Ga2O3:100 W, and ZnO:50 W in a flow rate of 20 sccm of Ar and 5 of O_2, at 2.3 mTorr. The In:Ga:Zn atomic composition is 2.2:1.0:1.1, for a normalized Ga, calculated by XPS results through area report on the Ga 3s, Zn 3s and In 4s spectra. Once again, patterning was carried out by lift-off for both the IGZO and the top electrodes. For the devices with Mo as top electrode, the same procedure as the bottom electrode was employed. For the devices with Ti at the interface, 6 nm of Ti were deposited by e-beam evaporation in a homemade apparatus. 60 nm of Au were then deposited without breaking vacuum at the same system for the devices with Ti/Au as top electrode. All depositions, except the ALD one, were carried out with no intentional heating. An annealing step was performed at the end of fabrication in all samples, unless mentioned otherwise, at 150℃ for 1 hour. The aged devices procedure has been previously reported in ref. 43. The parylene-C deposition for passivation was carried out through a chemical vapor deposition tool, CVD-PDS-2010. Patterning was achieved by reactive ion etching using O_2 gas.

The electrical characterization of the memristors was conducted at a Keithley 4200 SCS semiconductor analyzer connected to a Janis ST-500 probe station. The DC sweeps were acquired by applying a voltage to the top electrode while maintaining the bottom electrode connected to ground.

X-ray photoelectron spectroscopy (XPS) measurements were performed with a Kratos Axis Supra, using a monochromatic Al Kα source at 120 W (spectroscopy) and 150 W (imaging). Resolution was 80 eV for survey and 20 eV for detail scans, as well as 160 eV for imaging. Charge neutralization

with low energy electrons was used and all spectra were shifted to C 1s at 284.8 eV a posteriori. CasaXPS Version 2.3.25PR1.0 was used for data analysis. Sputter depth profiles were prepared with a monoatomic argon beam of 15 keV scanned over an area of 1.5 x 1.5 mm^2. The incident angle with respect to the surface was 60°. XPS was acquired after etching steps of 500 s with an X-ray power of 225 W, a pass energy of 80 eV and a 110 micrometer aperture.

Atomic force microscope (AFM) topographs were acquired with an Asylum Research MFP-3D Standalone system (Oxford Instruments, UK) operated in tapping mode at ambient room conditions. Commercially available silicon probes were used (Olympus AC160TS, Olympus Corporation, Japan; f_0 = 300 kHz, k = 29 N/m) and the resulting topographs were exported using Asylum Research's software packages after low-level flattening.

6.3 Results and discussion

6.3.1 Annealing effect and plasma treatment

The standard device structure, which will be referred from now on as Plasma/Not Annealed device, is illustrated in **Figure 6.1(a)**. Mo is used as bottom and top electrodes and a thin layer of MoO_x is created by an in-situ O_2 plasma treatment, between the IGZO layer and the bottom electrode. At the top interface, a thin Ti layer is also added. VOs are assumed to be the main sources of shallow donor levels in IGZO, localized close to the conduction band, that grant the characteristic n-type conduction to this semiconductor.[52,53] These VOs are formed when oxygen atoms are missing from the lattice and are readily ionized at room temperature with each doubly charged VO leaving 2 free electrons contributing to the conduction.[54–57] Due to its high oxygen affinity, Ti reacts with IGZO by extracting oxygen atoms, creating VOs in the oxide.[58] This creates a highly conductive region in the IGZO at the Ti/IGZO interface, therefore establishing an Ohmic junction. On the contrary, at the bottom interface there is a highly oxidized region, due to the presence of MoO_x, which creates a barrier for electron injection. This Schottky barrier modulation is believed to be the cause of RS in the device.[58–60]

To further ascertain our conclusions, XPS measurements with monoatomic argon cluster depth profiling were performed from the Ti to the bottom Mo electrode and the results can be consulted in **Figure 6.1(b)**. By analyzing the In 3d spectra more closely, it was found that metallic In^0 is present at the top interface (until etching time = 7000 s), while at the bulk and at the bottom interface mainly oxidized In^{3+} can be detected. The full analysis is presented in **Figures D.1(a), D.1(b) and D.1(c) - Appendix D**, where the In 3d spectra is presented for the Ti/IGZO interface and for the bulk IGZO and the relative percentages of In^0 and In^{3+} are estimated. In is the main element contributing to the conduction in IGZO as it connects weakly to oxygen due to its larger ionic radius, compared to Ga and Zn. This means that differences in VOs concentration are more noticeable in In, as demonstrated. Analyzing

the individual elements roles, In is polycrystalline even when deposited at low temperatures. With the addition of Zn, IZO films are created and are amorphous until 600 °C. However, the free carrier concentration cannot be easily decreased to be used as a semiconductor, which is solved by adding Ga. Ga^{3+} has a high ionic potential (3+ valence and smaller ionic radius that In^{3+}). Therefore, Ga can establish stronger bonds to oxygen preventing excessive free carrier generation due to VOs.[52,53,61] At the bottom interface of our proposed device, In concentration decreases faster than Ga or Zn, which means In/Ga ratio is lower at the interface than at the bulk. In/Ga ratios can affect both the IGZO conductivity and the barrier height: lower In/Ga ratio leads to lower conductivity and higher barrier height.[61–63]

In **Figure 6.1(c)**, the same XPS depth profile is presented for a sample with the exact same structure but in which a low-temperature annealing of 150 ℃ was performed post-fabrication in air conditions (Plasma/Annealed device). The I-V characteristic of the pristine state, between -1 V and 1 V applied to top contact, of the memristors can be consulted in **Figure 6.1(d)**. In this paper, all results are in regard to 4 μm^2 memristors, unless stated otherwise. It is clear that the Plasma/Not Annealed device has a rectification ratio of 2 orders of magnitude that confirms the Schottky barrier at the bottom interface. Moreover, in a previously reported device without Ti at the top interface, and therefore with a symmetric structure (Mo at both electrodes), this rectification was also notable, further confirming the influence of MoO_x at the bottom interface.[43] However, the Plasma/Annealed memristor has lost the rectification, maintaining the conductance level for negative polarities. By evaluating the XPS depth profiles (**Figures 6.1(b) and 6.1(c)**), the immediate conclusion is that with annealing there is a redistribution of In, Ga and Zn cations at the bulk IGZO, with tendency to higher In content at the bottom interface. This could indicate that a redistribution of VOs would take place, decreasing the Schottky barrier. In fact, the most dominant process occurring at low-temperature annealing of IGZO is the structural relaxation within the film to accommodate defects created during fabrication.[64]

The Mo 3d emissions were also evaluated in detail at the interface. Fittings were done according to Baltrusaitis et al.,[65] as exemplified in **Figures D.1(d) and D.1(e) - Appendix D**, and the summary of the relative percentage of the deconvoluted contributions for increasing etching time can be found in **Figures 6.1(e) and 6.1(f)**. Both samples contained Mo^{6+}, Mo^{5+}, Mo^{4+} and metallic Mo^0. In the Plasma/Annealed structure, a reduction of Mo^{6+} to Mo^{5+} and Mo^{4+} to Mo^0 took place. Mo^0 is the metallic component of the Mo 3d spectra and Mo^{4+} can also present a metallic behavior.[66] It is not clear if oxygen is released to the atmosphere or captured by IGZO. It is known that the O-H bonds in IGZO can generate and release H_2O molecules when annealing is performed under air conditions. This increases the VOs concentration at the IGZO which can be balancing the oxygen insertion from the reduced Mo. On the other hand, the process of oxygen absorption in IGZO has been proven to be thermally activated, becoming significant at temperatures above 200 °C.[64] While this process cannot be completely ruled out, since the annealing performed here was accomplished at 150 °C, it can be concluded that oxygen absorption is too low to be relevant.

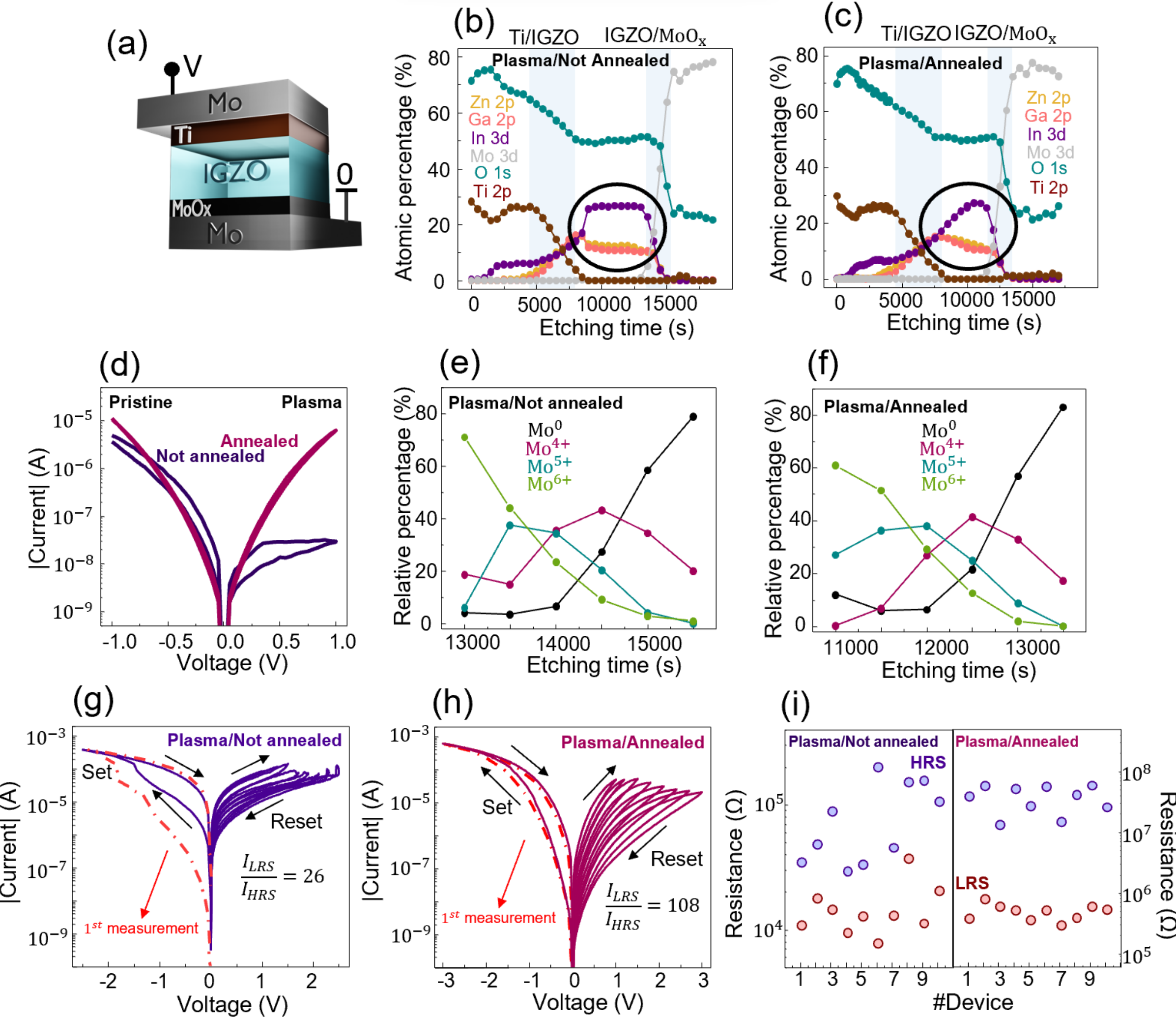

Figure 6. 1 Annealing effect on the Mo/MoO$_x$/IGZO/Ti/Mo memristor. (a) Schematic illustration of the device. (b) and (c) XPS argon cluster depth profiling through Ti/IGZO/MoO$_x$/Mo structure, fabricated using plasma to create the MoO$_x$ and Not Annealed and Annealed, respectively. (d) I-V characteristic of the pristine state, between -1 V and 1 V applied to the top electrode, of the Plasma/Not Annealed and Plasma/Annealed memristors. (e) and (f) Relative percentage of the deconvoluted Mo 3d spectra contributions at the bottom interface of the Plasma/Not Annealed and Plasma/Annealed structures, respectively. (g) and (h) I–V characteristic of full Set and gradual Resets of the Plasma/Not Annealed and Plasma/Annealed structures. (i) D2D variability presented for 10 devices of each evaluated memristor structure.

Set and Reset of the memristors are presented in the I-V characteristics of **Figures 6.1(g) and 6.1(h)**. In both devices, for negative polarities applied to the top electrode Set occurs, and the conductance increases from HRS to LRS, and for positive polarities the conductance decreases from LRS to HRS, realizing Reset. As explained before, since the active Schottky-type electrode is at the bottom interface, the switching on these devices can be classified as 8w. Both devices show analog behavior

with multiple conductance states. However, the Plasma/Not Annealed device must undertake a forming process before being able to perform Set and Reset, as shown in the red curve of **Figure 6.1(g)**, after which it never returns to the pristine state. On the contrary, the Plasma/Annealed device can function with no forming, immediately performing Set and Reset, and remaining at the pristine state when in the HRS. This is most likely due to the MoO_x layer in the Plasma/Not Annealed device having more Mo^{6+}. The work function of Mo^{6+} is higher than that of Mo^{5+} and Mo^{4+} and can go up to 6.6 eV.[67] At the same time, IGZO has a work function of around 4.5 eV.[68] This creates a high barrier for electron injection at this interface, which means that with the first application of negative voltage a soft breakdown is imposed to the MoO_x layer, which can lead to decreased control over the RS behavior. However, in the annealed memristor, no forming is necessary due to the lower barrier induced by the reduction of Mo^{6+}. Here, RS phenomenon takes place at the whole Schottky-like interface by modulation of the barrier height. This conclusion is further verified by the enormous decrease in device-to-device (D2D) variability found from the not annealed devices to the annealed devices (**Figure 6.1(i)**).

Given that the MoO_x/IGZO interface was identified as the Schottky barrier where RS takes place, further investigation on this interface was carried out. For such, memristors in which no plasma treatment was performed on the bottom Mo electrode were fabricated, from now on referred to as No Plasma/Not Annealed and No Plasma/Annealed. In **Figure 6.2(a)**, the I-V characteristic of the pristine state of annealed memristors with plasma and without plasma can be compared. It is noticeable, that the No Plasma/Annealed device also does not present rectification, which is once again a consequence of the annealing. In **Figure D.2 -Appendix D**, the entire analysis on the annealing effect of the devices fabricated without plasma can be consulted. Here, Mo^{6+} reduction cannot be noted which further elucidates on the loss of rectification being a process taking place in the IGZO. The No Plasma/Not Annealed devices also need forming before Set and Reset operations and D2D variability is drastically improved by the annealing step as well. It is important to note that the pristine of the No Plasma/Not Annealed and Plasma/Not Annealed devices show very identical pristine states. The major difference lies in the pristine of the annealed devices, with the No Plasma/Annealed memristor having a much more conductive pristine. Not many differences can be found by comparing the XPS depth profiling, presented in **Figure 6.2(b)**. Hence, the plasma treatment is found to not be the cause for the oxidized Mo at the interface, since the Mo 3d spectra for the memristors without the plasma treatment also present Mo^{6+}, Mo^{5+}, $Mo^{4+}$and Mo^{0}, as shown in **Figure 6.2(c)**. It is entirely possible that the Mo electrode can be oxidized by air contact before IGZO deposition, or even that the IGZO deposition induces oxidation to the Mo, since it is done in an Ar/O_2 gas atmosphere. The major distinction between the sample with Plasma/Annealed and No Plasma/Not Annealed is in the Mo^{6+} percentage, which is lower in the No Plasma device, and, most probably, in the density/thickness of the created oxide.

In terms of interface properties, the plasma treatment on Mo seems to slightly reduce the surface roughness, as evidenced by the AFM images, shown in **Figures 6.2(d) and 6.2(e)**. However, in both presented images the root mean square (RMS) roughness is very low (< 1 nm), which means it is not

expected to be affecting the pristine or the RS. In **Figure D.3 -Appendix D**, the AFM image of the IGZO surface is also presented with a low RMS roughness value of 0.461 nm. The Set and Reset operations by I-V sweep during 100 repeated cycles are presented in **Figure 6.2(f)** for the already discussed Plasma/Annealed device, displaying very low variability. The retention properties measured for 1 hour at 0.1 V for 8 programmed states (by I-V sweep) are depicted in **Figure 6.2(g)**. The relaxation decay is typical of area-dependent switching and the equilibrium state (here also the pristine state), is closer to the HRS than to the LRS. The area-dependent switching of both Plasma/Annealed and No Plasma/Annealed memristors is further confirmed by the linear relationship of resistance states (in LRS and HRS) with device area, shown in **Figure D.4 -Appendix D**, typical of interface-type switching.[13]

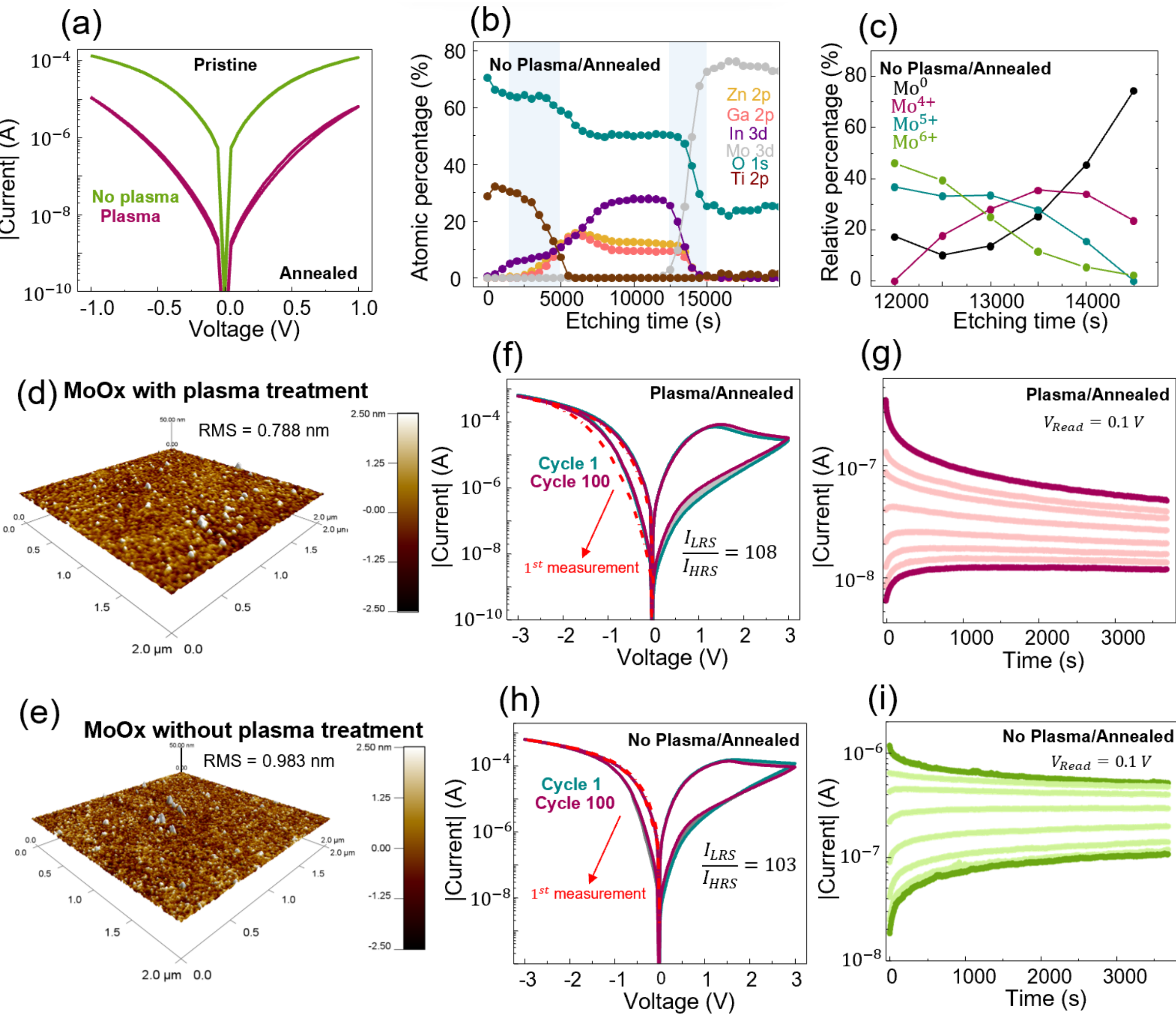

Figure 6. 2 O_2 Plasma treatment effect on the Mo/MoO_x/IGZO/Ti/Mo memristor. (a) I-V characteristic of the pristine state, between -1 V and 1 V applied to the top electrode, of the Plasma/Annealed and No Plasma/Annealed memristors. (b) XPS argon cluster depth profiling through Ti/IGZO/MoO_x/Mo structure on the No Plasma/Annealed structure. (c) Relative percentage of the deconvoluted Mo 3d spectra contributions at the bottom interface for the No Plasma/Annealed structure. (d) and (e) AFM 3D images of the Mo surface after the plasma and without any plasma treatment, respectively. (f) I–V

characteristic of 100 cycles of full Set and full Reset for the Plasma/Annealed structure memristor. (g) Retention properties of the Plasma/Annealed device recorded for 1 hour at 0.1 V after 8 programmed states via I-V sweep at different Reset stop voltages. (h) I–V characteristic of 100 cycles of full Set and full Reset for the No Plasma/Annealed memristor. (i) Retention properties of the No Plasma/Annealed device recorded for 1 hour at 0.1 V after 8 programmed states via I-V sweep at different Reset stop voltages.

C2C variability is also extremely low for the No Plasma/Annealed memristors as evidenced by the Set and Reset cycles, displayed in **Figure 6.2(h)**. However, retention properties, demonstrated in **Figure 6.2(i)**, show that the relaxation decay of the programmed states tend towards a much higher equilibrium state than the Plasma/Annealed device. This explains the higher pristine state of the No Plasma/Annealed memristor: after annealing, the device is already very close to the LRS. This is why the first measurement, displayed in **Figure 6.2(h)**, which as to our protocol is always the sweep on the negative polarity to induce Set, did not show any RS. This suggests that whatever physical/chemical reactions that happen during Set, took place during the annealing step for the No Plasma/Annealed structure. It is not clear why the reaction does not take place at the Plasma/Annealed device during annealing. It can be related to different MoO_x thickness or density or/and it could have to do with the increased Mo^{6+} concentration in the Plasma/Not Annealed memristor. Further research is necessary to understand the differences between RS mechanism in devices with and without plasma. For instance, transmission electron microscopy (TEM) measurements could provide more information on the MoO_x thicknesses or even film densities.

6.3.2 Different electrodes and aging

The impact on RS properties by the top electrode choice was also investigated. In **Figure 6.3(a)**, a schematic illustration is presented with the device structure and the chosen top electrodes- Ti/Mo, Ti/Au and Mo. The Plasma/Annealed procedure was chosen for the comparison. In **Figure 6.3(b) and 6.3(c)**, the I-V characteristic of the pristine and Set and Reset processes are displayed. Comparing the devices with Ti/Au and with Ti/Mo as top electrode, no significant differences are identified, other than a higher overall conductivity on the memristor with Ti/Au, which is easily explained by the lower resistance of Au. On the other hand, the device without Ti as interlayer, only with Mo as top electrode, shows significantly lower I_{LRS}/I_{HRS} ratio. To confirm this conclusion, D2D variability was assessed and is summarized in **Figure D.5 -Appendix D**. All the memristors with only Mo as top electrode showed lower I_{LRS}/I_{HRS} ratios (below 40). Without Ti as interlayer at the top contact there is less VOs in IGZO to be distributed in the annealing step and that will participate in RS, which explains the lower I_{LRS}/I_{HRS} ratios. However, this would also imply that IGZO is less conductive in this stack, which would decrease the overall conductance of the device, a fact not observed in the I-V of the pristine or in Set and Reset. In fact, LRS is the same in memristors with Ti/Mo and Mo as top electrode. This is because the lower

IGZO conductivity in the memristor without Ti is compensated by the increased resistance of oxidized Ti in the stack with Ti/Mo as top electrode.

Curiously, when this research started, the I_{LRS}/I_{HRS} ratio improvement caused by Ti and the annealing effect was not yet discovered and, therefore, the proposed stack by Pereira *et al.*[43] in 2020 was Plasma/Not annealed using Mo as top and bottom electrodes. These memristors were fabricated in 2019 and some were passivated with a parylene-C layer to evaluate the aging effect. The importance of passivation in microelectronics cannot be overstated. Microelectronics devices are increasingly being subjected to harsh operating environments, ranging from automotive and aerospace to medical and consumer electronics applications. Effective passivation shields devices from corrosive agents and electrical interference, preserving performance and extending lifespans. Various materials, including AlO_x,[69] SiO_x,[70] SiN_x,[70] polyimide,[71] SU-8,[72] and parylene,[73] have been used as passivation layers. Parylene stands out due to its exceptional protective properties, flexibility, chemical inertness, and ability to form conformal, pinhole-free layers at room temperature, making it ideal for flexible microelectronics.

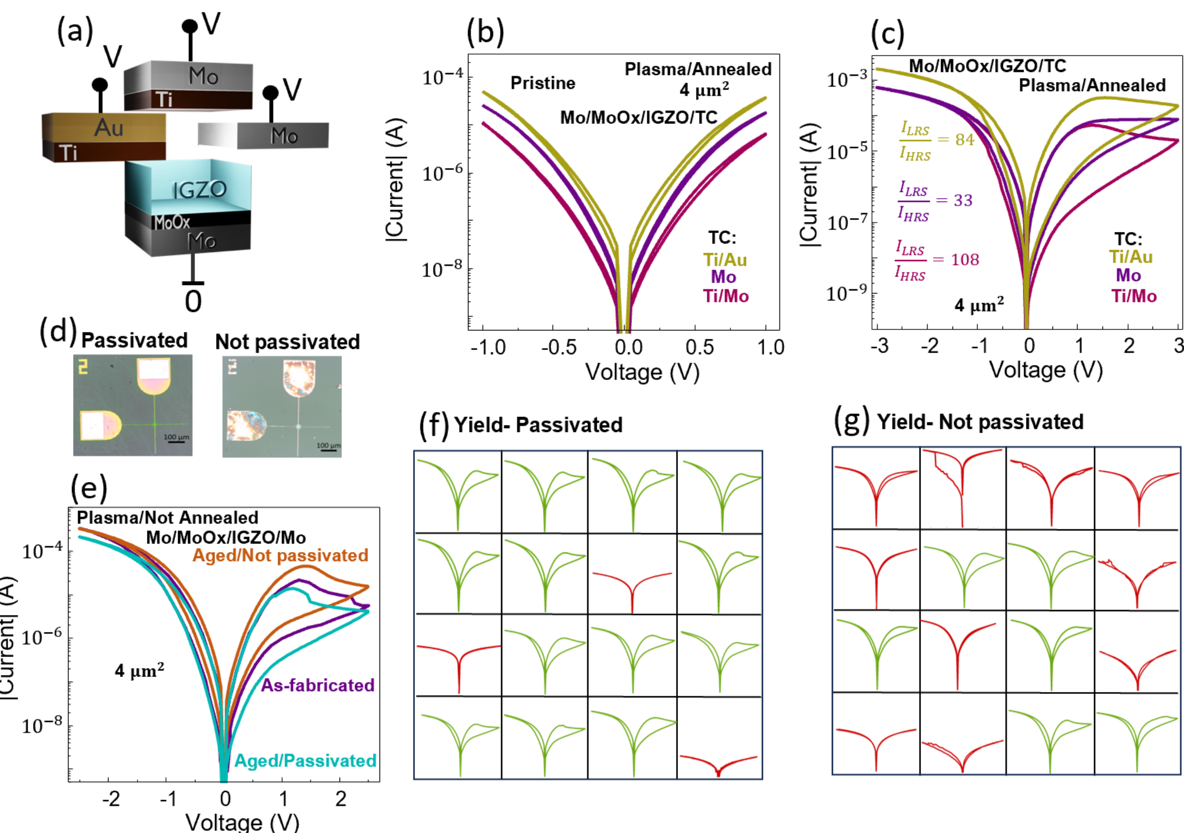

Figure 6. 3. Top contact (TC) effect and aging on the Mo/MoO$_x$/IGZO/TC memristor. (a) Schematic illustration of the device with the different chosen top electrodes. (b) I-V characteristic of the pristine state, between -1 V and 1 V applied to the top electrode, of the memristors with different top contact using the Plasma/Annealed method and correspondent (c) I–V characteristic of full Set and full Reset. (d) Micrograph of 5 years aged memristors with Mo/MoO$_x$/IGZO/Mo structure and the Plasma/Not annealed procedure Passivated and Not Passivated with parylene-C and correspondent (d) I–V characteristic of

full Set and full Reset. (e) and (f) D2D variability and yield represented through I-V Set and Reset of 16 aged devices Passivated and Not Passivated.

Figure 6.3(d) shows the micrograph of devices with and without Parylene-C passivation. As can be seen on passivated devices, in the area where the parylene layer was etched out, exposing the Mo bottom electrode, there are no visible signs of degradation, unlike the devices without passivation. This suggests that the passivation step somehow changed the oxidizing properties of the exposed Mo layer. XPS was performed on the exposed Mo in both passivated and non-passivated devices and the results are shown in **Figure D.6 -Appendix D**. Accordingly, it was found that only passivated devices displayed metallic Mo^0 in the exposed part of the electrode, which will surely improve electrical connection. Moreover, a comparison between the I-V characteristics of the as-fabricated and the aged devices, both passivated and non-passivated, depicted in **Figure 6.3(e)**, shows that the characteristics remained similar through time. In fact, the passivated device seems to have a higher I_{LRS}/I_{HRS} ratio. The most notable difference between passivated and not passivated aged devices occurs in the yield, with the passivated devices displaying a yield of 81 %, significantly higher than that verified for the non-passivated aged counterpart, which displayed a yield of just 38 % with increased D2D variability, visible in **Figures 6.3(f) and 6.3(g)**. Hence, parylene seems to successfully prevent reactions with air that hinder the memristor performance in time.

Additionally, the Mo bottom contact was replaced by Al, to verify its effect on RS behavior of the stack (**Figure 6.4(a)**). In **Figure 6.4(b)**, the 3D AFM image on the Al surface can be consulted, displaying an extremely high RMS roughness of over 9 nm. This explains the typical abrupt behavior then observed in the Set and Reset operations performed by I-V sweep and the correspondent retention, shown in **Figure 6.4(c)**. As previously explained, in abrupt RS, VOs form vertical CFs that connect the top to the bottom electrodes, creating a conductive path. In this case, the roughness on the bottom Al electrode creates needle-like structures that are closer to the top electrode, facilitating the formation of a localized CF. In fact, abrupt switching characteristics has, in some memristor stacks, already been attributed to the roughness of the bottom contact. For instance, the electroforming voltage has been reported to be reduced with increased bottom electrode roughness for both Pt and TiN electrodes.[74,75] In IGZO-based memristors with Al as bottom electrode, abrupt RS was identified when Al was deposited by a higher deposition rate, which resulted in higher surface roughness, while a lower Al deposition rate would result in memristors with area-dependent switching.[41]

Another interesting feature is that the presented stack displays MLC properties by varying the Reset stop voltage. This phenomenon can be extremely advantageous for deep neural networks (DNNs) applications in which more than 2 conductance states with full retention are preferred. MLC has been identified before for IGZO-based abrupt memristors by controlling the compliance current (CC) or the Reset stop voltage and can be attributed to the control of CFs width.[76,77] However, as

presented in Figure 6.4(d), retention failure happens at some of the programmed states which means the created CFs are unstable.

The plasma treatment was also attempted on the Al bottom electrode as it has previously been reported as an effective method to improve surface smothness.[41] Set and Reset and correspondent retention properties are displayed in Figures 6.4(e) and 6.4(f). Abrupt RS is still observed and, in fact, no MLC can now be detected. Full retention of LRS and HRS suggests the formation of one or more robust CFs. This is, most likely, due to the increased oxidation state, density and/or thickness of the oxidized Al layer formed between the Al bottom electrode and the IGZO. It is expected that the optimization of the plasma treatment on the Al bottom electrode, to reduce the surface roughness without increasing the oxide thickness, and a slower Al deposition rate could lead to area-dependent switching properties.[41]

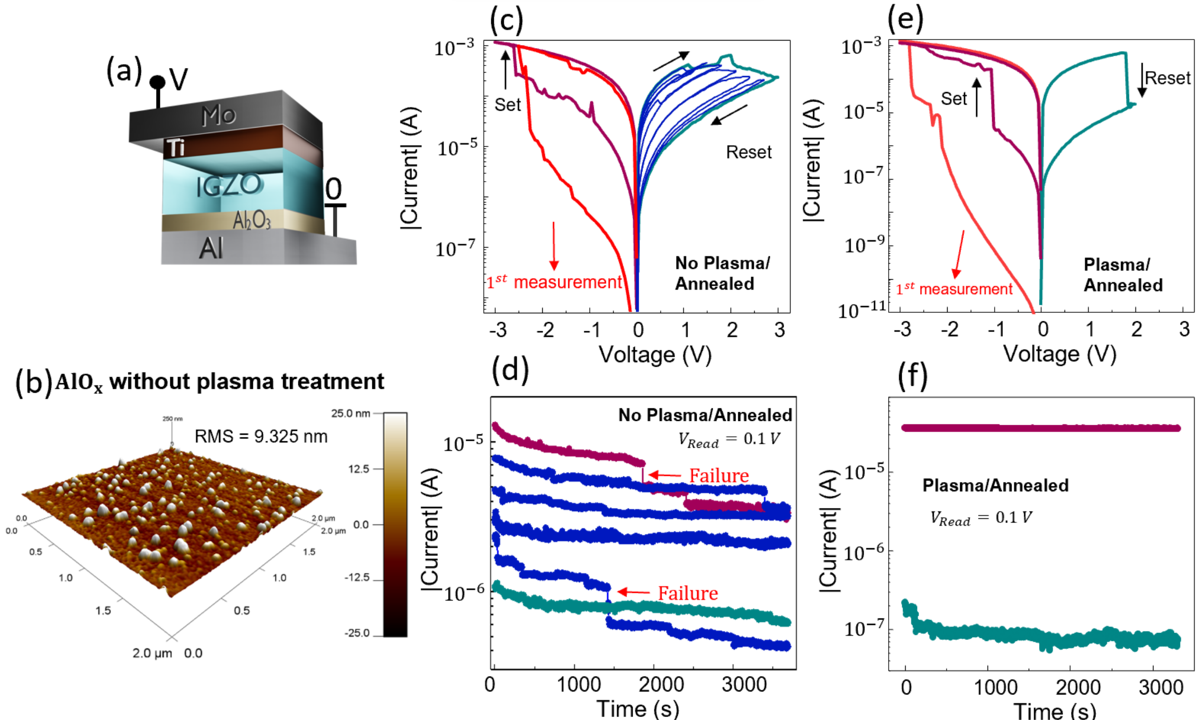

Figure 6. 4 Bottom contact (BC) effect on the BC/IGZO/Ti/Mo memristor. (a) Schematic illustration of the device with the Al/AlO_x/IGZO/Ti/Mo. (b) AFM 3D images of the Al surface without plasma treatment. (c) I–V characteristic of full Set, full Reset and gradual Reset for the No Plasma/Annealed structure memristor with Al as bottom contact and correspondent (d) retention properties recorded for 1 hour at 0.1 V after 6 programmed states via I-V sweep with different Reset stop voltages. (e) I–V characteristic of full Set and full Reset for the Plasma/Annealed structure memristor with Al as bottom contact and correspondent (d) retention properties recorded for 1 hour at 0.1 V after programmed LRS and HRS via I-V sweep.

6.3.3 Resistive switching mechanism

Having now explicitly proven that RS takes place at the bottom interface, we investigate the retention behavior of the LRS and HRS on the standard Mo/MoO_x/IGZO/Ti/Mo memristor, and its dependence on the surrounding atmosphere to determine if environmental conditions significantly impact the decay. The results can be found in **Figure D.7 -Appendix D**. It was found that in the Plasma/Annealed device there was an improved stability on the LRS in vacuum suggesting that the device interacts with the environment. On the other hand, the No Plasma/Annealed memristor did not show any relevant variation in retention properties in vacuum. The Plasma/Annealed memristor has the equilibrium state closer to the HRS than to the LRS, and since retention is improved in vacuum, it can be concluded that oxygen from atmosphere play a role in the (re)oxidation of IGZO during state relaxation. On the contrary, the No Plasma/Annealed device is in equilibrium closer to the LRS, which means the rate of the (re)oxidation of the IGZO is already much slower in air and cannot be improved in vacuum.

It is, therefore, assumed that retention failure (relaxation of programmed state) happens through oxygen incorporation and diffusion to/from the IGZO and that the oxygen supply is the MoO_x and/or the surrounding atmosphere. We validate this hypothesis through the insertion of a thin layer of Al_2O_3 between the MoO_x and the IGZO, as schematically illustrated in **Figure 6.5(a)**. Al_2O_3 has a diffusion coefficient of $D_0^{Al_2O_3}(\mathbf{500\ K}) \approx 10^{-65}$ $cm^2.s^{-1}$, which means it presents extremely slow oxygen migration.[78] Given that the Al_2O_3 layer was deposited through ALD, no plasma treatment was performed on these devices on the bottom contact, since the in-situ method was no longer an option. The I-V displaying full Set and gradual Reset of the memristors with 1 nm of Al_2O_3 and corresponding retention properties are displayed in **Figures 6.5(b) and 6.5(c)**. Not many differences can be identified in the I-V if compared with the No Plasma/Annealed memristors without Al_2O_3. The analog behavior is still observed and LRS and HRS are practically at the same state. However, retention properties seem to have improved with the addition of the oxygen diffusion suppressing layer, which is further evidenced by the device with 2 nm of Al_2O_3 - **Figures 6.5(d) and 6.5(e)**. In **Figure 6.5(f)**, the extrapolation of the fitting on the experimental data of LRS and HRS is presented. The stretched exponential equation[43,79] was used with one characteristic relaxation parameter (τ) for HRS and two (τ_1 and τ_2) for LRS, as explained in the **Figure D.8 -Appendix D**, to achieve the best possible fitting. It is clear that the devices with 2 nm of Al_2O_3 have better retention properties since it requires more time for the LRS and HRS to meet at the equilibrium state, at 109 853 s. This is even more clear if the comparison is made with the devices with no Al_2O_3 layer, in which the equilibrium state is reached at 35 247 s (**Figure D.7(c) -Appendix D**). Devices with 3 and 5 nm of Al_2O_3 were also tested and the results are depicted in **Figure D.8 -Appendix D**. It was found that 3 nm of Al_2O_3 already shift the RS behavior to filamentary, proven by the typical random telegraphic noise (RTN) apparent in the retention measurements, and 5 nm of Al_2O_3 completely inhibit any RS behavior.

The improved retention properties of the Plasma/Annealed memristor in vacuum, which has the equilibrium state at the HRS, along with the further retention enhancement observed when an oxygen diffusion suppressing layer is added at the active interface, confirm that the retention failure is due to the reoxidation/oxidation of a previously oxygen-deficient/rich IGZO surface. These results therefore indicate that oxygen-ion migration rather than electron trapping and detrapping is responsible for the RS in our proposed memristor.

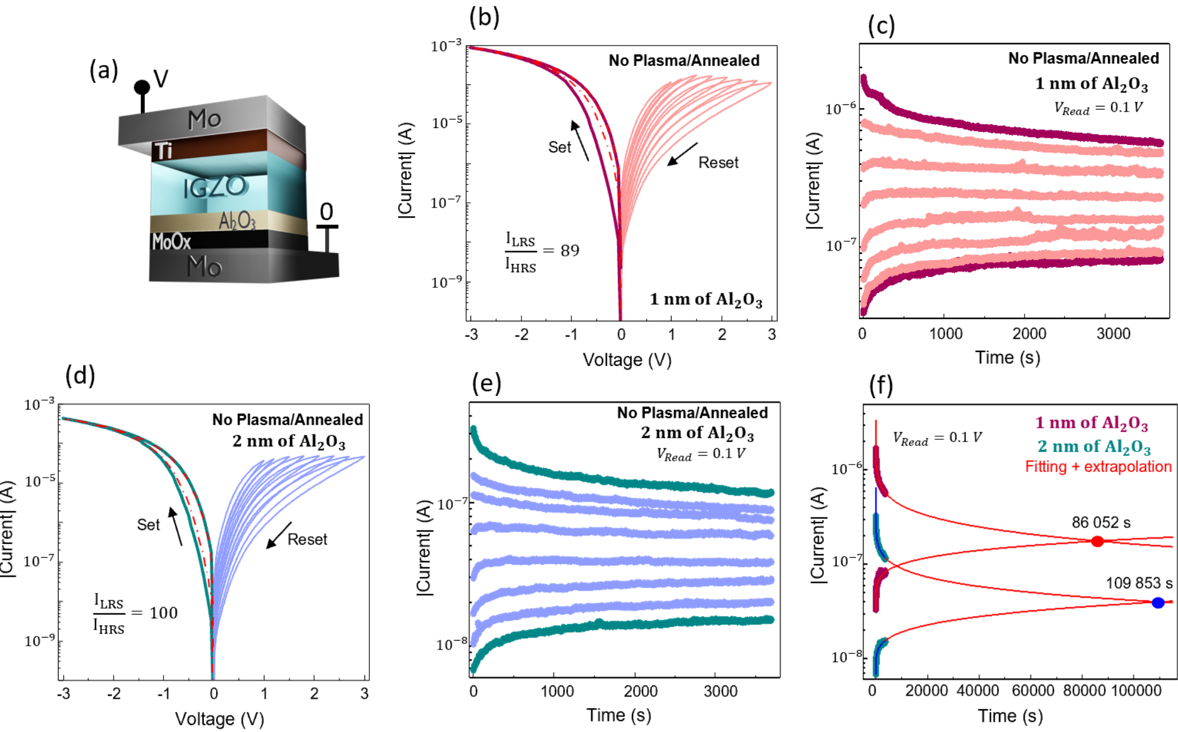

Figure 6. 5 Retention improvement on the IGZO memristor by Al_2O_3 insertion at the Schottky-like interface. (a) Schematic illustration of the device with the Mo/MoO_x/Al_2O_3/IGZO/Ti/Mo. No plasma was performed on these stacks. I–V characteristic of full Set and gradual Reset and correspondent retention properties recorded for 1 hour at 0.1 V after 8 programmed states via I-V sweep with different Reset stop voltages for the No Plasma/Annealed memristors with (b) and (c) 1 nm of Al_2O_3 and (d) and (e) 2 nm of Al_2O_3. (f) Extrapolation of the fitting on the experimental data on retention of LRS and HRS to discover the equilibrium state of the memristors and the time at which LRS meets HRS for the No Plasma/Annealed devices with 1 nm of Al_2O_3 and 2 nm of Al_2O_3.

In a previous work, we have already studied the Plasma/Annealed device regarding its conduction mechanism during Set and Reset. From the analysis, it could be concluded that RS is directly related to the modulation of the Schottky barrier. At low reverse bias, the electron transmission probability was found to be temperature dependent. At higher fields, field emission becomes the dominant carrier flow mechanism and under forward bias, thermionic field emission occurs.[44] Here, the same procedure is applied for the device with No Plasma/Annealed with 2 nm Al_2O_3 as interlayer, to confirm the previous conclusions. Hence, quasi-static I–V sweeps for Set and Reset are applied to the device at

a temperature range of 130–300 K, starting with the Set. The results are displayed in **Figure 6.6(a)**. The first considered conduction mechanism is described by the thermionic emission (TE, or Schottky emission) **Equation (6.1)**:

$$\ln\left(\frac{j}{A^{*}T^{2}}\right) = -\frac{\left(e\Phi_{\mathrm{SBH}} - \beta\sqrt{V}\right)}{k_B}\frac{1}{T} = m\frac{1}{T} \qquad \mathbf{(6.1)}$$

with the $e\Phi_{SBH}$ being the Schottky barrier height, β the factor for barrier lowering and A^* the effective Richardson constant. **Figure 6.6(b)** displays the experimental I-V characteristics for four selected temperatures (T = 130, 210, 270, and 290 K), fitted by **Equation (6.1)**. The focus is on the LRS in the positive voltage branch, corresponding to the reverse direction at the Schottky-like IGZO/MoO_x interface. The red lines fitting **Equation (6.1)** align well with the observed experimental currents. The different I–V curves intersect at a certain voltage, which has been observed in our IGZO-studies as well as for eightwise switching $SrTiO_3$ memristors.[44,80] According to **Equation (6.1)**, the logarithmic current's slope m is inversely proportional to temperature, which is shown in **Figure 6.6(c)**. Two distinct temperature regimes emerge: at high temperatures, there is a strong voltage dependence, whereas at low temperatures, the slope m remains relatively constant. **Figure 6.6(d)** clarifies this difference by plotting the slope against the applied voltage. This finding is in agreement with the previous IGZO study on devices without Al_2O_3 (Plasma/Annealed).[44] Another interesting observation is that the slope m is positive for the low temperature regime which is nonconformant with the Schottky emission theory, hinting that electron tunneling through the barrier as well as thermionic-based electron emission can be considered as the main present conduction mechanisms.

Considering all the conclusions drawn in this work, the RS mechanism in our eightwise switching memristor is based on the Schottky barrier modulation mainly by oxygen-ion exchange between the IGZO and the MoO_x. In **Figure 6.6(e)**, a schematic illustration is presented. During Set, when negative voltages are applied to the top electrode, negatively charged oxygen ions are forced to the MoO_x, increasing the VO concentration at the IGZO interface. With increasing VOs, the depletion zone decreases as expected from the classical Schottky theory - more doping leads to a narrower depletion zone. Moreover, the Schottky barrier height decreases, and, therefore, the tunnel current through the Al_2O_3 increases. Conversely, when positive voltage is applied to the top electrode, negatively charged oxygen ions in the MoO_x are attracted to the IGZO and partially fill the VOs. This decreases the doping at the interface, which results in a wider depletion zone and in the increase of the Schottky barrier height, which decreases the tunnel current through the Al_2O_3. These mechanisms can explain the observed eightwise switching polarity, which other theories struggle to justify. Although direct evidence for these processes is hard to obtain, numerous studies on similar structures suggest this theory as the most probable explanation for the observed RS.[46–48] Nonetheless, more studies are required for ultimate prove and so far cation contributions from In^{3+}, Ga^{3+} or Zn^{+} cannot be excluded from the RS mechanism.

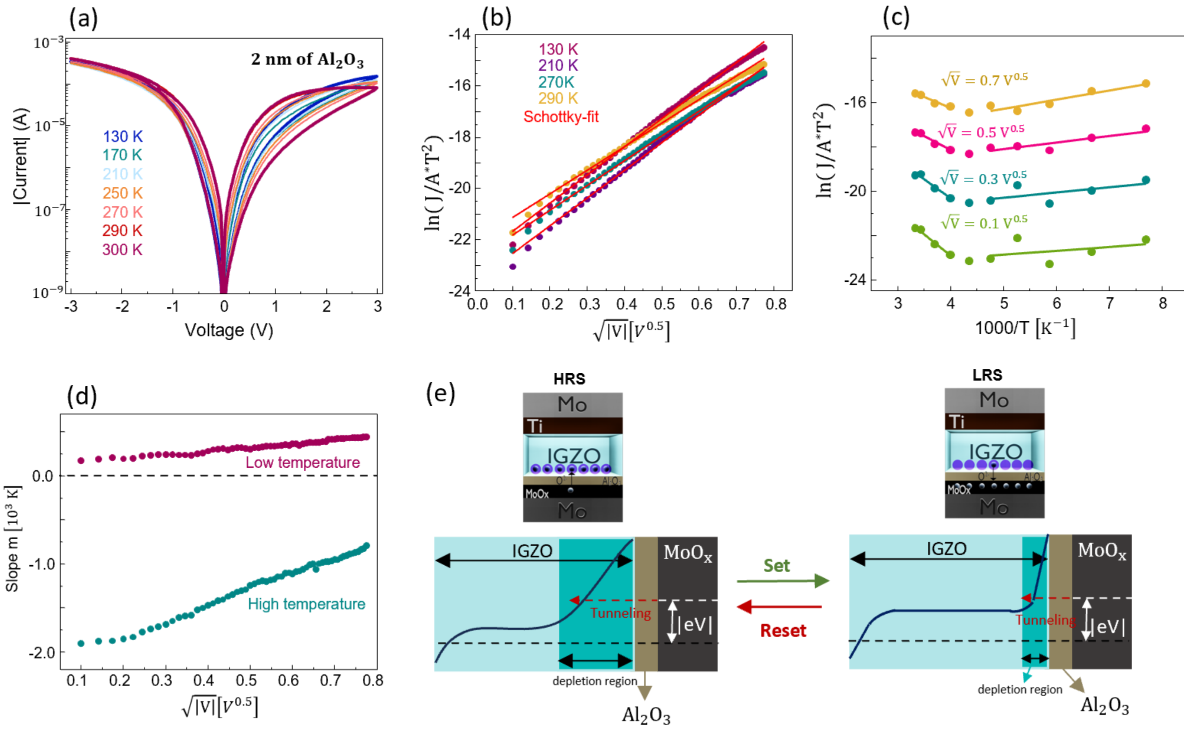

Figure 6. 6 Temperature measurements and RS mechanism on the Mo/MoO_x/Al_2O_3/IGZO/Ti/Mo memristor (2 nm of Al_2O_3). (a) I-V characteristic of full Set and full Reset at different temperatures. (b) I-V dependence of the LRS measured at difference temperatures. (c) Logarithmic current dependence on the inverse temperature, according to Equation 6.1. (d) Extracted slope (m) dependence on input voltage. (e) Schematic illustration of the effect on the band diagram during Set and Reset and of the LRS and HRS.

6.4 Conclusions

In summary, in this work we give evidence that, in the MoO_x/IGZO junction, a Schottky barrier is formed in which area-dependent RS can take place in eightwise polarity. By changing the fabrication procedure, namely annealing steps and the plasma treatment on the bottom Mo electrode, devices with the pristine at the LRS can be achieved. Changing the top contact can only affect the I_{LRS}/I_{HRS} ratio, while altering the bottom electrode can completely shift the RS to filamentary. Additionally, we have proven that the insertion of an oxygen diffusion suppressing layer (Al_2O_3) between the IGZO and the MoO_x, dramatically improves retention properties. Based on these experimental findings, we suggest that the modulation of the Schottky barrier at the device's bottom interface is responsible for the RS and that this is induced by the exchange of oxygen ions between the IGZO and MoO_x, which adjusts the depletion width and Schottky barrier height, similar to what has been proposed for other eightwise switching devices.

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CHAPTER 7

RECENT PROGRESS IN OPTOELECTRONIC MEMRISTORS

Neuromorphic computing has been gaining momentum for the past decades and has been appointed as the replacer of the outworn technology in conventional computing systems. Artificial neural networks (ANNs) can be composed by memristor crossbars in hardware and perform in-memory computing and storage, in a power, cost and area efficient way. In optoelectronic memristors (OEMs), resistive switching (RS) can be controlled by both optical and electronic signals. Using light as synaptic weigh modulator provides a high-speed non-destructive method, not dependent on electrical wires, that solves crosstalk issues. In particular, in artificial visual systems, OEMs can act as the artificial retina and combine optical sensing and high-level image processing. Therefore, several efforts have been made by the scientific community into developing OEMs that can meet the demands of each specific application.

In this Review, the recent advances in inorganic OEMs are summarized and discussed. The engineering of the device structure provides the means to manipulate RS performance and, thus, a comprehensive analysis is performed regarding the already proposed memristor materials structure and their specific characteristics. Moreover, their potential applications in logic gates, ANNs and, in more detail, on artificial visual systems are also assessed, taking into account the figures of merit described so far.

The literature review presented in this chapter is published in:

M.E. Pereira, R. Martins, E. Fortunato, P. Barquinha and A. Kiazadeh, "**Recent progress in optoelectronic memristors for neuromorphic and in-memory computation**", in Neuromorphic Computing and Engineering, vol 3, 2, 022002, 2023.

7.1 Introduction

It is becoming increasingly urgent to find an alternative to the long-time used Von Neuman architecture, in which the bottleneck of transferring data between the processor and the memory unit remains a severe issue and blocks the realization of complex problems with high speed and accuracy. Moreover, in extensively data-centric applications like artificial intelligence (AI), novel computational paradigms are vital to bring down power consumption. Neuromorphic computing based on resistive switching (RS) devices, or memristors, is a brain-inspired technology that has emerged as a viable ultra-low power consumption alternative. In this technology, information processing is performed directly at the memory element, preventing data shuffling and, therefore, enabling cost and power-efficient, real-time in-memory computation.

The memristor, discovered by Leon Chua,[1] is a non-linear resistor, usually composed of a metal-oxide-metal structure in which the metal layers compose the electrodes and an oxide film is referred to as active layer. Typically, these devices are fabricated in a vertical stack which allows for further miniaturization when compared with technologies such as SRAM, DRAM or flash, as evidenced by the smallest 4 nm^2 device reported up to now.[2] The most interesting feature of the memristor is the fact that its resistance state can be tuned by an external electric field into two or more distinct states. The switching process occurs at the active layer and the transition from the highest-resistance state (HRS) to the lowest-resistance state (LRS) is known as Set operation and from LRS to HRS, as Reset operation. An exceedingly fast 50 ps switching speed has been obtained which is, naturally, of extreme importance to ensure power efficiency.[3,4] The retention of the programmed states is related to the material structure of the device and can be translated into short- or long-term memory behavior, suited for different neuromorphic applications.

The first fabricated memristor was reported in 2008 with TiO_2 as active layer and Pt as electrodes.[5] To date, the most popular materials for oxide-based memristive devices are still the transition metal oxides (TMOs), for which the switching occurs, most commonly, in a filamentary form, such as tantalum oxide (Ta_2O_5), hafnium oxide (HfO_2) or aluminum oxide (Al_2O_3).[6-8] Typically, the transition between different resistance states is an abrupt one, as exemplified in **Figure 7.1(a)**. An initial step, called electroforming, is required to create conductive filaments (CFs), usually composed of oxygen vacancies (VOs), within the insulating layer. This is, usually, accomplished with a once electric bias application of higher voltage than the operating one. Once these filaments are created, current can pass through which decreases the resistance of the device, now at the LRS. Then an operating voltage will cause the dissolution and consequent restoration of CFs resulting in Set and Reset operations. The CFs are typically robust and can only be dissolved by the operating voltage which results in long retention of programmed states. In the case of valence change memories (VCM), the dominant mechanism

is determined by the balance between thermochemical and electrochemical redox reactions, which is mostly defined by the combination of the materials used in the device stack.[9-11]

As opposed to abrupt-RS, analog switching behavior, displayed in **Figure 7.1(b)**, can be achieved using, for example, oxide semiconductors such as zinc oxide (ZnO), indium-gallium-zinc oxide (IGZO) or zinc-tin oxide (ZTO) as active layers.[12-16] Typically, this type of switching occurs at the interface and is attributed to an interchange or trapping of ions between a metal electrode and the oxide.[17] It, usually, results in a lower device-to-device (D2D) and cycle-to-cycle (C2C) variability, since an area-dependent behavior with a uniform contribution of defects is in place. Additionally, the programmed resistance state is, usually, not retained for a long period of time and is, instead, gradually replaced by the equilibrium state of the oxide. This retention time can be manipulated with the amplitude or number of programming electric pulses.[18] This behavior is unsuited for inference-only applications in which a stable retention of at least two well-separated states is required. However, it can be advantageous in the realization of synaptic functions.

Moreover, the manipulation of several distinct resistance states can be accomplished by both the abrupt and the analog RS and is preferred for in-memory computation tasks in stateful logic and/or artificial neural networks (ANN) loosely inspired by the human brain. An ANN hardware composed by interconnected and adaptive electronic elements was first envisioned in 1962[19] and can be accomplished with RS devices organized in crossbars to perform parallel data processing. The human brain has 10^{11} neurons that communicate between each other through more than 10^{14} synapses, in which their connection strength varies.[20] In Deep neural networks (DNNs) composed by memristor crossbars, synaptic behavior is mimicked when electric short pulses are continuously applied to the device to gradually decrease or increase its resistance state, in processes called potentiation and depression, respectively. In fact, several synaptic characteristics have already been emulated by RS devices[13,21,22] proving its overwhelming potential to substitute the classical computing system.

Nonetheless, memristor crossbars that operate under only electric stimuli often suffer from heat generation and crosstalk issues, related to the interference of neighboring devices, which is blocking high-scale implementation.[23] Crosstalk can be eliminated with the addition of a selector transistor in each crossbar cell. However, this approach undoubtedly increases cell area and energy consumption.[24] In fact, the biological system cannot be matched with purely voltage-assisted neuromorphic platforms. The human brain itself is stimulated by a number of sensing inputs such as light, sound, smells or touch, with about 80 % of this information being acquired through visual perception.[20] Hence, an ideal AI system should merge the capabilities offered by electrical and optical domains.[25]

Optoelectronic memristors (OEMs) use both light and electronic signals as inputs and can behave as sensory artificial synapses with high energy-efficiency, low crosstalk and fast data processing and are, thus, suitable to link artificial visual systems with its processing on hardware.[26] In detail, OEM technology offers the possibility of a non-electric programming method, and can, thus, be an enhanced solution to challenges such as excessive Joule heating and crosstalk that occur in high-density passive

crossbar architectures. Beyond that, learning functions and signal transmissions cannot be simultaneously performed on devices operated solely with electric field. Adding light as a third terminal facilitates parallel data transmission and processing. Hence, the applications of such a system can be extended to all mobile computing applications where the near/in sensor computation concept is developed such as wearables, visual information processing, invisible touch screens, electronic eyes, and smart processors.

To build an OEM, firstly one must consider the targeted application, since a particular set of requirements related to its performance will be in place. **Figure 7.1(c)** illustrates the most relevant applications of reported OEMs in literature. As a photodetector, the optical induced change in resistance should only be detected during light input since the purpose is to reveal when there is, in fact, light irradiation. Contrary, in DNNs a quasi-full state retention after light pulse is mandatory for the highest accuracies in any task. In its turn, spiking neural networks (SNNs) is the paradigm closer to accurately simulating brain functionality and demands a dependent state retention on several factors such as number or frequency of applied input light pulses to mimic learning and forgetting capabilities of the human brain.

The retention of the light provoked resistance state is, usually, ascribed to a persistent photoconductivity (PPC) effect that is, often, inherent to the active layer material.[27-30] The PPC effect is, typically, attributed to i) macroscopic physical barriers at the interfaces or doping defects that decrease the rate of recombination of photogenerated electron/hole pairs[31] or ii) atomic scale barriers located at the large lattice relaxation sites in which the energy level of the empty defects is above the conduction band minimum and the occupied energy level is located in the band gap, preventing recombination.[29,32]

Consequently, the choice of memristor material structure is of the most importance. There should be at least one transparent electrode, such as indium-tin oxide (ITO) or aluminum-doped ZnO (AZO),[33-36] or a nm thick semi-transparent electrode, such Au, to allow light to reach the active layer. Moreover, the bandgap of the active layer material should be considered for proper light wavelength irradiation, as depicted in **Figure 7.1(d)**. Naturally, a lower bandgap material is desired for wide sensitivity to multiple wavelengths. However, these materials often suffer from inferior retention stability.

As evidenced in the graph of **Figure 7.1(e)**, where the number of publications in optoelectronic and photonic RS devices is presented pear year, there is an obvious growing interest in researching OEMs, as their potential becomes more and more clear. However, as it is still a novel topic, only few review articles can be efficiently consulted for a comprehensive analysis on the recent advances.

This review paper aims to fill in this gap, providing a summary on the developments on inorganic-based OEMs fabricated in a vertical stack, with focus on metal and semiconducting-oxides, 2D-based materials and 1D structures as active layer. The planar structure has also been widely explored,[37-42] however for high-scale integration and power-efficiency, the vertical stack is the favored one. Organic materials have also been widely investigated for optoelectronic features[43–46] due to their advantages

in low temperature and simple solution processing techniques. In addition, organic molecular tuning is possible and desirable which leads to certain optical and electrical properties.[47] Nevertheless, organic materials are not, usually, as stable as inorganic ones mainly due to oxidation issues. In optoelectronic applications, metal oxide semiconductors are the ones which show high mobility and sufficient mechanical and electrical stability, besides transparency in some cases.[48] Furthermore, recent works of inorganic materials show immense progress in low-cost fabrication techniques using solution and printing methods.[49] Other classes of materials explored as active layer for optoelectronic features are ferroelectric or magnetic[50–53] and organic/inorganic perovskites materials.[54–64] However, most of the available studies are at the device level and, therefore, only a small sum have demonstrated synaptic functions[40,65–67] or logic gates implementation.[35,68–71]

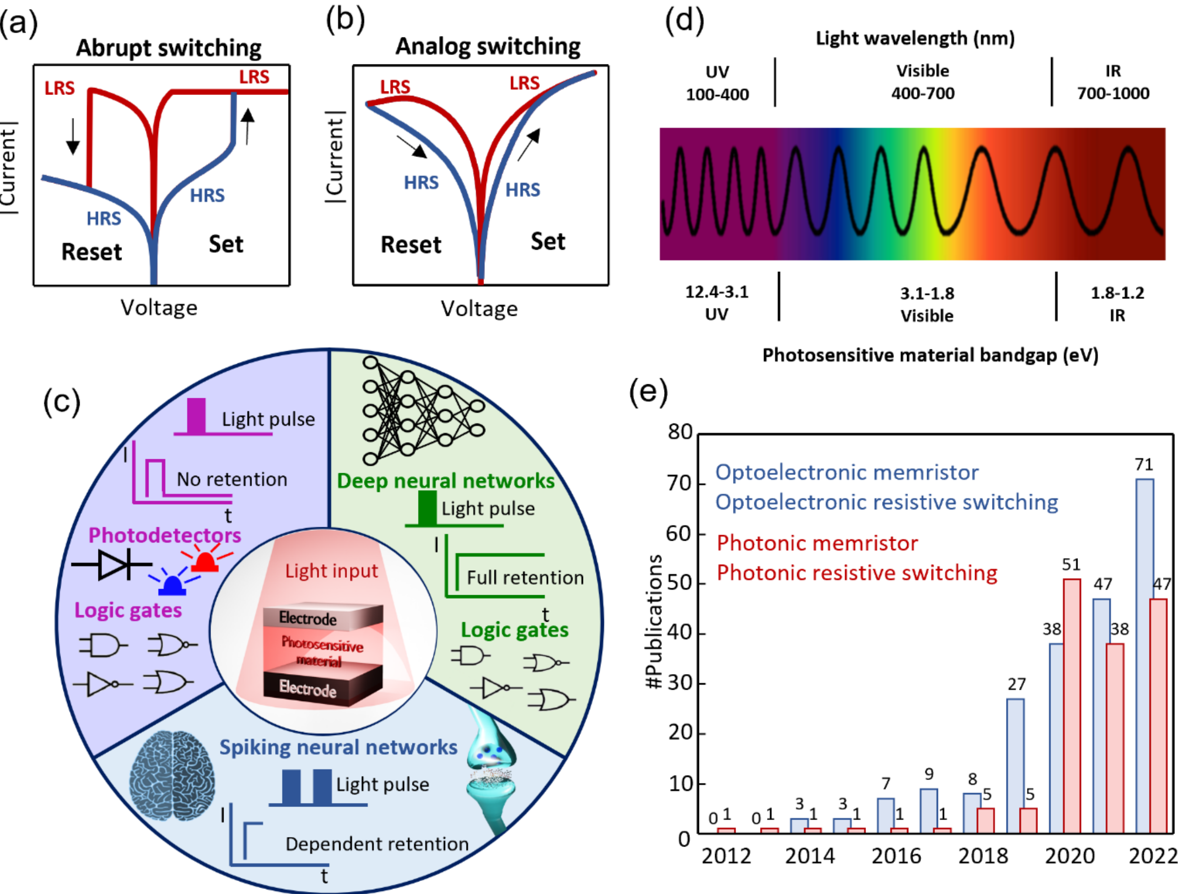

Figure 7. 1 Optoelectronic memristor applications. Typical memristor DC sweep showing (a) abrupt and (b) analog type of switching displaying Set and Reset for positive and negative polarities, respectively. (c) Illustration of potential OEMs applications and their state retention upon light pulse requirements. (d) UV-IR electromagnetic spectrum with light wavelength and bandgap material relation described. (e) Publications on optoelectronic and photonic memristors from 2012 to 2022 (search engine: Google Scholar, accessed on January 2023; keywords: Optoelectronic memristor; optoelectronic RRAM; Photonic memristor; Photonic RRAM.)

The potential applications of OEMs based on the targeted materials in logic gates, ANNs and, in more detail, on artificial visual systems are also evaluated here, with the assist of the reported individual features. Additionally, the current challenges and future perspectives in this field are also discussed.

7.2 Optoelectronic memristors: materials and devices

7.2.1 Metal oxide OEMs

The first report on controlling the resistance state in a memristor using light in combination with voltage signals was in 2012 by Ungureanu *et al.*.[72] An active layer of Al_2O_3 on a Si/SiO_2 substrate was used with patterned Pd as top electrode. Under dark, there was barely any RS and the device could be considered a resistor, but combining -10/10 V electric pulses and a 6 V read pulse with ultraviolet (UV) or infrared (IR) light pulses, multiple resistance states could be achieved. As soon as light was switched off, the dark current value immediately returned, showing no PPC effect. However, for data storage and short/long-term memory applications, PPC effect is required. This long-lived effect after light exposure is beneficial to modulate a non-volatile multi-resistance state.

Later, HfO_x was proposed using Si substrates as bottom contact and Au[73] or Pt[74] as top electrodes. In these preliminary studies, PPC effect was not shown or discussed. In fact, the authors show RS behavior only under light irradiation. The former showed RS behavior under a broadband halogen–tungsten light source with multiple resistance states dependent on light intensity. The latter showed visible light sensitivity, with blue irradiation enabling RS characteristics. In this case, the optically boosted carriers transfer from Si together with electrically redistributed oxygen vacancies within the oxide, result in the switching behavior under light. Since these devices show memristive switching characteristics only under light, logic gates could be targeted as application, in which light is irradiated constantly from surroundings.

Light can be used as a third input to control Set or Reset operations in OEMs for a more power-efficient and fast approach. For instance, light irradiation was found to perform Reset in a HfO_x-based memristor.[75] The proposed structure, illustrated in **Figure 7.2(a)**, presented a typical bipolar and abrupt switching behavior in dark, as shown in **Figure 7.2(b)**, with a high I_{LRS}/I_{HRS} ratio of more than 10^3. When the device was Set in the LRS, visible light irradiation forced a transition to a higher resistance state and depending on its intensity, could perform a full Reset. **Figure 7.2(c)** presents a graph where multiple resistance states can be distinguished that correspond to different light intensities for multi-level cell (MLC) operation. The different resistance states were proven to be non-volatile, which is related to the light-sensing mechanism. As explained before, this abrupt-type of switching is, usually, associated with the formation and rupture of CFs with different dimensions located within the oxide layer bandgap. A small CF is composed of a low amount of oxygen vacancies and, therefore, requires

low light intensity for recombination with the surrounding oxygen interstitials, which causes filament rupture. A large CF is formed by a higher amount of oxygen vacancies and, thus, requires light of higher intensity to be annihilated. Additionally, it was observed that blue light triggers the same Reset effect as white light while the longer, less energetic, wavelength of red light did not incite any reaction. The dependency on light wavelength was suggested to be associated with the position of oxygen vacancies inside the HfO_x bandgap after set. In fact, a wide-bandgap oxide such as HfO_x (E_g=5.7 eV) is by nature not photo-responsive. However, photoexcitation of defects located at a level of ≈2−3 eV below the conduction band minimum is possible and would bring the device back to its initial HRS.[75]

Similarly, More *et al.* proposed a titanium oxide (TiO_x)-based memristor in which illumination with a tungsten lamp could decrease V_{Reset} from 3.5 V to 0.8 V, reducing energy consumption.[76] More recently, a Pt/TiO_x/Ti memristor was reported to respond to multiple irradiation wavelengths, ranging from UV to red light, in a completely different manner.[77] In this work, an analog-type of switching was observed for Pt/TiO_x/Ti devices. The current state increased as the irradiated wavelength shortened, particularly for blue and UV illumination, which is in agreement with TiO_x bandgap of ≈3.2 eV. Photons with shorter wavelengths provide enough energy to excite more electron-hole pairs within the TiO_x layer.

A different mechanism for photoexcitation was proposed by Zhou *et al.*, related to a Pd/molybdenum oxide (MoO_x)/ITO memristor structure.[78] In this study, a light induced manipulation of Mo valence states in the MoO_x thin film explained the photonic Set. UV light irradiation caused the generation of electrons and holes in the MoO_x layer. As photogenerated electrons transferred to the MoO_x conduction band, a reaction would take place between photogenerated holes and absorbed water molecules that produced protons (H^+). Under surface science studies, authors revealed that the photogenerated electrons together with the protons would trigger the creation of H_yMoO_x and incite a shift from Mo^{6+} to Mo^{5+}, which ultimately resulted in the increase of current to LRS. When light was switched off, the current state did not return to HRS and, instead, suffered a slow decay (PPC effect). During electronic Reset, an electric field forced the protons away from the MoO_x layer towards the Pd electrode and Mo^{5+} changed back to Mo^{6+}, causing a decrease in current state to HRS.

A bi-layer structure of Ta_2O_{5-x}/Ta_2O_5, sandwiched between an Si substrate and an Ag top electrode, demonstrated significant potential as an OEM.[79] This device showed a dependent current increase on UV and visible light irradiation with full retention of the photo-produced states, proving light information can be stored in situ. The bandgap of Ta_2O_5 is ≈4.0 eV, and therefore, it responds mostly to UV light. However, due to VOs in the Ta_2O_{5-x} film, the electrons at the defect energy level can still be forced to the conduction band by lower energy wavelengths.

Therefore, a bi-layer switching medium can be used to enhance the performance of optoelectronic features, similar to electric field-induced counterpart. The AlO_y/Cerium oxide (CeO_x) memristor with Al as bottom and ITO as top contacts- **Figure 7.2(d)**- was reported by Tan *et al.*.[80–82] A native AlO_y layer was created upon deposition of Al to form the Schottky junction with the CeO_x, that resulted in

analog switching behavior, shown in **Figure 7.2(e)**. The photo-sensitive mechanism was explained by electrons trapped in the VOs at the AlO_y/CeO_x interface. These electrons could be excited by photons and leave positively charged VO^{2+}s. This would lower the effective Schottky barrier by reducing its width, which would cause a decrease in the resistance of the junction. This memristor structure presented photocurrents dependent both on light intensity and wavelength, as shown in **Figure 7.2(f)**. Naturally, shorter wavelengths and higher light intensity triggered the highest current change. Moreover, PPC effect could be noticed as, even after light pulse, the current state remained unaltered. A voltage Reset was then required to fully erase the resistance state.

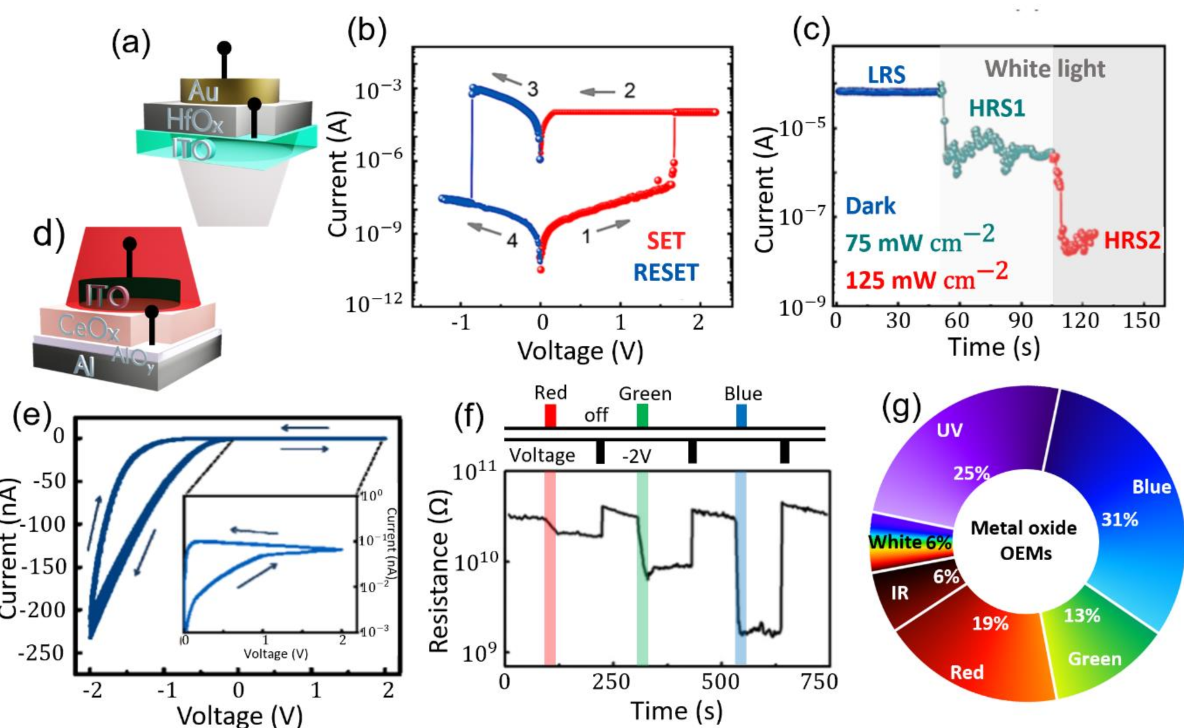

Figure 7. 2 Metal oxide OEM characteristics. (a) $ITO/HfO_x/Au$ OEM illustrative structure; (b) correspondent abrupt behavior in I-V sweep displaying Set/Reset for positive/negative polarities, respectively and (c) correspondent LRS read at 0.1 V in the dark, during 75 mW cm^{-2} and 125 mW cm^{-2} of white light irradiation. Reprinted (adapted) with permission from ref. 75. Copyright (2019) American Chemical Society. (d) $Al/Al_2O_3/CeO_x/ITO$ illustrative structure; (e) correspondent analog behavior in I-V sweep displaying Set/Reset for positive/negative polarities, respectively and (f) resistance state measured in time with alternative dark and light irradiation (red/green/blue cycles) with Reset electrical pulse of −2 V before each cycle. Reprinted (adapted) for ref. 80, John Wiley & Sons. [© 2015 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim]. (g) Statistical percentage on the light wavelength inducing RS reported by the works on metal oxide-based vertical OEMs.

Additionally, metal-oxide materials have been used in double-layer strategies in combination with semiconducting-oxides for switching medium in OEMs and will be discussed in the following section. In **Table 7.1**, the comparison of the most important characteristics in metal-oxide OEMs can be consulted and it is noticeable some devices show optical Set/Reset coupled with electric Reset/Set,

respectively. Naturally, photo-induced switching can be abrupt or analog depending on material stacks. The working principal of analog optical memristors is mainly related to the change of barrier profile at the interface of the electrode and the switching layer, which resembles to analog electric field-induced RS devices. Abrupt optical RS shows higher retention stability, however, inferior C2C and D2D reproducibility is expected due to the switching dependent on CFs. When reset is induced by light, the resistance state obtained is always maintained after light pulse. However, this is not considered PPC since, in this case, light is used to partially/fully break CFs and not to increase the conductance state.

No fully photonic switching behavior has been demonstrated within the same device, which hinders their possible application in wire-free crossbars. Moreover, as demonstrated in **Figure 7.2(g)**, most studies report on UV or blue irradiation which makes the discrimination between signals of different wavelengths challenging. Future technology will rely on visible light communication (VLC), where the application of abundant light sourcing devices (lamps, mobile displays, TV, etc) will be very important in the concept of ambient intelligence.

Table 7. 1 Characteristics of vertical OEMs with metal oxides as active layer.

N.S.: not specified at the original paper; N.A.: not applicable; BB: broadband. Endurance is related to optical induced RS properties.

Active layer	Electrodes	Size (μm^2)	RS Behavior	λ_{light} (nm)	Light effect	DC Sweep Set/Reset (V)	I_{LRS}/I_{HRS} ratio	Endurance (cycles)	Electric retention	PPC
Al_2O_3[72]	Si/Pd	1.00×10^8	Abrupt	390 950	Enables switching behavior	-10/10	$>1.00\times10^3$	N.S.	1 year	No
HfO_x[73]	Si/Au	4.00×10^4	Abrupt	BB	Enables switching behavior	4.0/-4.0	$>1.00\times10^3$	N.S.	N.S.	N.S.
HfO_x[74]	p-Si/Pt	1.26×10^3	Abrupt	450	Enables switching behavior	6.0/-4.0	$\approx1.00\times10^4$	N.S.	1.00×10^4	N.S.
HfO_x[75]	ITO/Au	N.S.	Abrupt	400 400-700	Performs Reset	2.6/-1.2	$>1.00\times10^3$	25	1.00×10^3	N.A.
TiO_2[76]	Al/Pt	5.00×10^1	Abrupt	320-1100	Decreases V_{Reset}	5.0/5.0	$>1.00\times10^1$	300	6.00×10^5	N.A.
TiO_2[77]	Pt/Ti	4.91×10^2	Analog	365 465 532 650	Increases current	3.0/-3.0	N.S.	N.S.	No	Yes
MoO_x[78]	ITO/Pd	4.91×10^4	Abrupt	365	Performs Set	N.S./-2.5	$\approx4.00\times10^1$	N.S.	1.44×10^3	Yes
Ta_2O_{5-x}/Ta_2O_5[79]	n-Si/Ag	1.26×10^3	Abrupt	460 620	Performs Set	4.0/-4.0	$\approx3.00\times10^3$	10	2.00×10^4	Yes
AlO_y/CeO_{2-x}[80,81]	Al/ITO	7.85×10^3	Analog	254 499 560 638	Performs Set	2.0/-2.0	$\approx1.00\times10^3$	30	1.00×10^4	Yes

7.2.2 Oxide semiconductors OEMs

Oxide semiconductors can provide additional advantages as active layer on memristors. In particular, amorphous oxide semiconductors (AOS), such as IGZO or ZTO, have high flexibility, due to a lack of grain boundaries, which enables low-processing temperatures. This facilitates the use of flexible substrates (paper, polyimide, PEN/PET),[24,83,84] providing the means for embedded flexible technologies in wearables and Internet-of-Things (IoT) applications. Furthermore, AOS are used in flat-panel display technology for active-matrix driver circuits, making them ideal candidates for future integrated memristor-based hardware for artificial intelligence.

ZnO has been the most popular material as switching medium for OE devices. Using Pt and ITO as bottom and top contacts, Xie *et al.* showed a decrease in V_{Set} and V_{Reset} upon UV light for more efficient power consumption.[85] Contrary, Shih *et al.* showed an increase in V_{Set} and V_{Reset} which is not very appealing.[86] However, PPC effect was present in these devices, as a change in RS behavior was observed even after UV light was turned off, which means ANNs could be targeted as applications. Moreover, the memristor showed improved I_{LRS}/I_{HRS} ratio after UV illumination. The authors explained that the conduction mechanism changed from Schottky emission to Poole-Frenkel after UV illumination, which induced the creation of extra oxygen ions and radicals due to an accelerated breaking of Zn-O bonds.

The analog behavior of the ZnO memristor was also studied using different electrodes for OE applications.[87,88] UV light was proven to increase the current state with a PPC effect. Interestedly, one of the reported OE structures for analog-type of switching, ITO/ZnO/Ag,[88] was also described by another group yet with an abrupt-type of RS.[89] On both reports, the sputtering technique is employed to deposit ZnO and similar thicknesses for all composing memristor layers are used. However, ZnO deposition conditions are different which can explain the observed differences. Generally, electrochemical mechanism (ECM) is responsible for devices with active electrodes such as Ag and Cu. In this respect, depending on the electric field, switching can be tuned to be abrupt for higher field or analog, depending on the size of metallic filament. The analog RS behavior could be also related to interface properties of ZnO with the contacts which is directly related to deposition conditions. In fact, in the original works, the reported analog switching for this memristor structure is associated with VOs filaments whereas the abrupt switching is related to ECM with Ag filaments.[88,89]

A semi-transparent ZnO OEM, with Pt and Au as electrodes, that could perform both Set and Reset with optical inputs has been developed, with the structure illustrated in **Figure 7.3(a)**.[90] In detail, Yang and co-workers showed Set could be induced by UV, blue or green irradiation with PPC characteristics, showing MLC operation. UV illumination resulted in the highest current increase with an I_{LRS}/I_{HRS} ratio of ≈10^4. Nonetheless, less energetic wavelengths such as green light could also induce a sufficiently high I_{LRS}/I_{HRS} ratio of ≈10^2, as can be seen in **Figure 7.3(b)**. ZnO has a wide bandgap of 3.2

eV. However, deposition in pure Ar atmosphere can result in a larger amount of VOs along with material heterogeneity with different energy levels.[91] Visible light irradiation can, thus, induce an ionization of VOs, converting them into positively charged VO^{2+}s and free electrons which leads to an increase of the current state, as commonly accepted for AOS materials.[92] Interestingly, the retention time (or PPC effect) was also impacted by light exposure. The retention decay was fastened by irradiation with longer wavelengths such as red and near-IR (NIR) illumination, leading to an optical Reset, in the scale of seconds (see **Figure 7.3(b)**). This photonic Reset was explained with an injection of electrons from the metal to the ZnO layer, by internal photoemission or photo-assisted tunnelling. Part of these electrons neutralized ionized oxygen vacancies, decreasing its density, and fastening the PPC decay.

Similarly, the same research group showed photonic Set and Reset in a double layer IGZO memristor, illustrated in **Figure 7.3(c)**.[26] The analog RS behavior was attributed to the formation of a potential barrier and well at the interface of a layer with low oxygen (LO) content ($IGZO_{(LO)}$) and a layer with high oxygen (HO) content ($IGZO_{(HO)}$). The width of this interfacial barrier would be dependent on the ionized oxygen vacancies density. The lower this density, the smaller the barrier, which facilitates electron tunnelling and increases the current state of the device. On the other hand, during Reset, the neutralization of ionized oxygen vacancies would increase the barrier width and result in a decrease of current state. Set could be induced by light in wavelengths from 420 to 1000 nm. Naturally, the longer the wavelength used for irradiation, the less change the current state would suffer. It was found that the PPC decay time could be decreased (Reset) by red or NIR (800/900 nm) light, only if the previous Set process was performed by short wavelengths illumination (350/420 nm), as can be seen in **Figure 7.3(d)**. To explain this phenomenon, the authors proposed that during illumination, the photocurrent would depend on a dynamic equilibrium between ionization and neutralization of VOs (**Figure 7.3(e)**). When the memristor was exposed to visible light of higher energy to perform Set, a small amount of VOs was left that could be further ionized by subsequent irradiation with light of lower energy. In this case, a neutralization of VOs would, therefore, be dominant and enable a decrease in the current state-Reset.

Later, a double-layer ZTO OEM was described, following the above explained strategy of oxygen rich and deficient layers.[93] Set was performed electrically with a ≈10^2 I_{LRS}/I_{HRS} ratio. Reset could be performed with MLC properties via blue, green and red light irradiation and the I_{HRS} was not only dependent on wavelength, but also on light power. It was clarified that light would provide the necessary energy for interstitial ions to recombine with electrically produced oxygen vacancies within the ZTO layer, causing CFs to disrupt. Interestedly, analyzing the DC sweep displaying RS behavior, Set and Reset transitions do not seem abrupt. However, the CF formation/annihilation explanation for the RS behavior is aligned with the full 10^5 s retention of states obtained for this memristor structure. The same behavior was observed in a bilayer memristor with ZTO/TaO_x (structure illustrated in **Figure 7.3(f)**), in which MLC could be achieved by different power of blue light irradiation, as can be seen in **Figure 7.3(g)**.

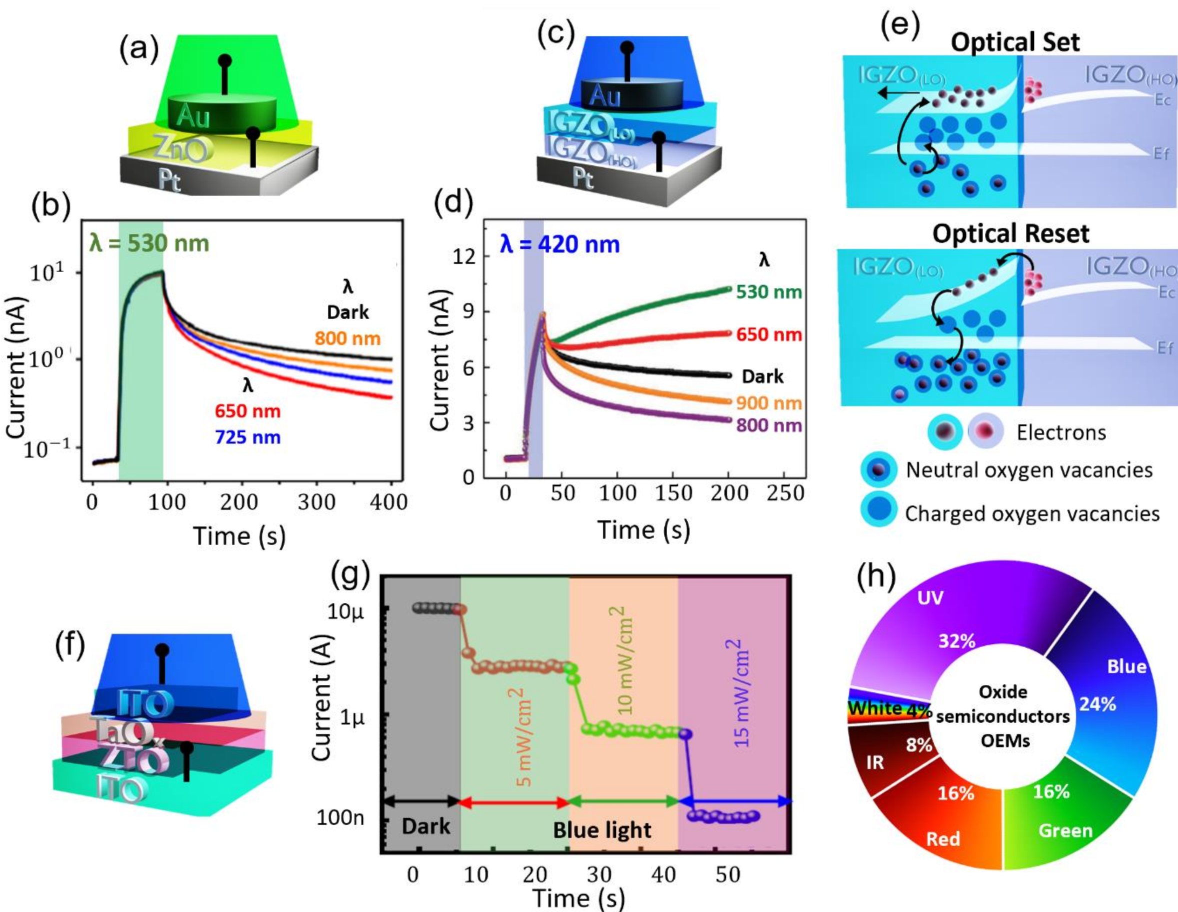

Figure 7. 3 Oxide semiconductors OEMs characteristic behaviors. (a) Pt/ZnO/Au OEM illustrative structure and (b) correspondent current increase under green light irradiation and PPC decay fastened by 650, 725 and 800 nm wavelength of light. Reproduced from ref. 90 CC BY 4.0. (c) Pt/$IGZO_{(HO)}$/$IGZO_{(LO)}$/Au OEM illustrative structure and (d) correspondent current increase under blue light irradiation and PPC decay fastened by 800 and 900 nm wavelength of light. (e) Schematic illustrations of oxygen vacancies ionization and neutralization during light irradiation on optical Set and Reset operations. The reaction marked by arrows plays a dominating role in the OE response. Reproduced from ref. 26 CC BY 4.0. (f) ITO/ZTO/TaO_x/ITO OEM illustrative structure and (g) correspondent multilevel states achieved by different blue light intensities. Reprinted (adapted) with permission from ref. 97 Copyright (2022) American Chemical Society. (h) Statistical percentage on the light wavelength inducing RS reported by the works on oxide semiconductors OEMs.

In **Table 7.2**, a list is provided with the most relevant features on the, so far reported, OEMs based on oxide semiconductor materials and bi-layers. To our knowledge, this class of materials was the only one so far not relying on nanostructured materials to demonstrate full photonic RS behavior with Set and Reset being performed by light with different wavelengths. However, as evidenced by the statistical percentages on different light-induced RS presented in **Figure 7.1(h)**, the research is, still, mostly on UV and blue light irradiation. Since IR light is the transmission method for data in wireless systems, it is highly desirable that further research on longer wavelengths is realized to allow conversion and storage of IR data.[94] High-speed process is one of the main challenges for further development of OEMs, relying on the working principal as mentioned in most of the reports. In this respect, there

are several solutions such as increase the built-in potential by engineering the memristive device layer stack, either via defect engineering of the RS layers or via modification of the effective work function at the contacts. The second main challenge is the bandgap tunability of oxide thin films for a broader spectrum. Here, the same approaches reported for visible light AOS-based photodetectors can be adopted. For instance, an absorption layer composed of hydrogen-doped IGZO revealed visible light detection.[95] RGB-color detection is also possible with strategies such as using a system combining an AOS film with colloidal quantum dots (QDs),[96] as will be later discussed.

Table 7. 2 Characteristics of vertical OEMs based on semiconductor oxides and bilayer structures composed of metal/semiconducting oxides as active layer.

N.S.: not specified at the original paper; N.A.: not applicable. Endurance is related to optical induced RS properties.

Active layer	Electrodes	Size (μm^2)	RS Behavior	λ_{light} (nm)	Light effect	DC Sweep Set/Reset (V)	I_{LRS}/I_{HRS} ratio	Endurance (cycles)	Electric retention	PPC
ZnO[98]	Pt/Pt	3.14×10^4	Abrupt	365	Adds intermediate state	2.2/1.1	$\approx1.00\times10^2$	100	N.S.	No
ZnO[85]	Pt/ITO	1.96×10^5	Abrupt	365	Decreases V_{Set}/V_{Reset} Adds intermediate state	2.0/-2.0	$\approx4.00\times10^1$	N.S.	1.00×10^4	N.S.
ZnO[86]	TiN/ITO	4.00×10^0	Abrupt	>380	Increases V_{Set}/V_{Reset} Decreases I_{HRS}	-0.1/0.3	$\approx1.00\times10^1$	N.S.	N.S.	N.A.
ZnO[87]	FTO/In2O3	N.S.	Analog	365	Increases current	2.0/-2.0	N.S.	N.S.	N.S.	Yes
ZnO[88]	ITO/Ag	7.85×10^3	Analog	366	Increases current	1.5/-1.5	N.S.	100	No	Yes
ZnO[90]	Pt/Au	7.85×10^3	Analog	350 420 530 650 725 800	UV/Blue/Green performs Set Red/IR performs Reset	Nonpolar (-2.0/2.0)	$<1.00\times10^1$	20	N.S.	Yes
ZnO[89]	ITO/Ag	4.00×10^4	Abrupt	White	Performs Set	3.0/-3.0	$\approx1.00\times10^1$	N.S.	1.00×10^4	Yes
$IGZO_{(HO)}/IGZO_{(LO)}$[26]	Pt/Au	7.85×10^3	Analog	420 530 650 800 900	VIS performs Set IR performs Reset	2.0/-2.0	$>1.00\times10^1$	10	1.00×10^4	Yes

ZTO_y/ZTO_x[93]	ITO/ITO	1.00×10^{4}	Abrupt	450-495 495-570 620-760	Performs Reset	1.0/-1.0	$\approx1.00\times10^{2}$	2200 1800 1800	1.00×10^{5}	N.A.
ZTO/TaO_x[97]	ITO/ITO	1.00×10^{4}	Analog	405	Performs Reset	2.0/-2.5	$<1.00\times10^{2}$	1500	1.00×10^{4}	N.A.
ZTO[99]	ITO/ITO	1.77×10^{4}	Analog	405	Increases current	2.0/-2.0	1.80×10^{1}	N.S.	1.00×10^{4}	Yes
SiO_x[100]	p-Si/ITO	2.50×10^{5}	Abrupt	410 532 632 650	Increases I_{LRS} Decreases V_{Set}	6.0/-5.0	$\approx1.00\times10^{3}$	N.S.	N.S.	Yes
AlO_y/ZnO_{1-x}[101]	Al/ITO	7.85×10^{3}	Analog	310	Performs Set Increases I_{LRS}	3.5/-6.5	$>1.00\times10^{1}$	N.S.	1.00×10^{3} LRS	Yes
ZnO/CeO_x[102]	ITO/TiN	3.14×10^{4}	Analog	405	Performs Set	8.0/-8.0	$\approx1.00\times10^{1}$	N.S.	N.S.	Yes
$Al_2O_3/IGZO$[103]	Al/ITO	2.25×10^{4}	Analog	400	Enables switch-ing behavior	3.0/-3.0	8.00×10^{0}	N.S.	No	Yes

7.2.3 2D-materials OEMs

2D-materials such as graphene (G), transition metal dichalcogenides (MoS_2, WS_2, WSe_2, $MoSe_2$, $MoTe_2$, etc.) or black phosphorus (BP), have also been widely explored for OEMs due their excellent photoresponsivity,[104] related to a large surface-to-volume ratio, and RS switching performance.[105,106] A review paper from 2019 can be consulted, where mainly planar 2D-based structures for OEMs are described in detail, to that date.[94] Here, as previously explained, the focus is on vertically stacked devices, which were mostly reported more recently.

In this regard, a monolayer of MoS_2 was used as switching medium in Si substrates and W top electrodes.[30] UV illumination was used to perform Set with one order of magnitude of I_{LRS}/I_{HRS} ratio and PPC effect was observed related to a spontaneous trapping/detrapping of electrons. However, the necessary voltage to perform Reset on these devices was high (-8 V). Since this monolayer has a bandgap of 1.8 eV, it would be interesting to test these devices under IR illumination. WO_3 OEMs showed enhanced performance under light input.[107] A combination of a 600°C annealing and 45 min. of white light irradiation resulted in an improved I_{LRS}/I_{HRS} ratio that went from 1.7 (as-prepared device) to 25.

Later, Jaafar *et al.* demonstrated a current increase induced by UV light in a GO based-memristor.[108] A planar structure was compared to a vertical one. The latter showed superior features with an abrupt RS of ≈10^4 ratio. Moreover, during UV irradiation, both V_{Set} and V_{Reset} were reduced. This behavior was attributed to photogenerated electron-hole pairs which increased the current state in both LRS and HRS. A PPC decay was also shown, that can be useful for ANNs applications.

Reset induced by light was also reported on 2D OEMs. For instance, an heterostructure of $MoSe_2/Bi_2Se_3$ nanosheets was embedded in a polymethyl methacrylate (PMMA) film to form the active layer on a device that showed Reset under NIR light.[109] PMMA was included in the active layer to passivate the trap states on $MoSe_2/Bi_2Se_3$. The full device structure is illustrated in **Figure 7.4(a)**. The memristor showed abrupt RS behavior assigned to Joule-heating provoked formation/disruption of metallic CFs. The authors explained NIR light would facilitate the rupture and prevent the creation of CFs since the Ag clusters would react with photogenerated holes and oxidize back to Ag^+. In the graph of **Figure 7.4(b)**, the current state of the device with multiple stimulus can be evaluated in time. It can be seen that the current decreases to the full-HRS only under both NIR illumination and electric Reset.

A different mechanism for Reset by light was proposed by Zhou *et al.* regarding a memristor based on BP nanosheets coated with polystyrene (PS) (BP@PS),[110] with the structure illustrated in **Figure 7.4(c)**. The DC sweep displaying Set and Reset under different light wavelengths can be consulted in **Figure 7.4(d)**. It is clear that a higher energy illumination, further decreased V_{Reset} from 2 V (dark) to 1.17 V (UV), as summarily presented in **Figure 7.4(e)**, and achieved a lower current state in the HRS, enabling higher I_{LRS}/I_{HRS} ratio. The authors explained that during electric Reset, the external electric

field would change the direction of the internal electrical field (induced by a transfer of electrons from the BP@PS to the ITO layer, due to the different material work functions), forming a Schottky barrier. When the memristor was exposed to light, the trapping sites would capture the photogenerated electrons and the surface potential would increase, further increasing the Schottky barrier, and, therefore, increasing I_{LRS}/I_{HRS} ratio. Additionally, as the scattering centers were negatively charged by the captured photogenerated electrons, the internal electric field would increase and a lower V_{Reset} would be necessary to switch off the device.

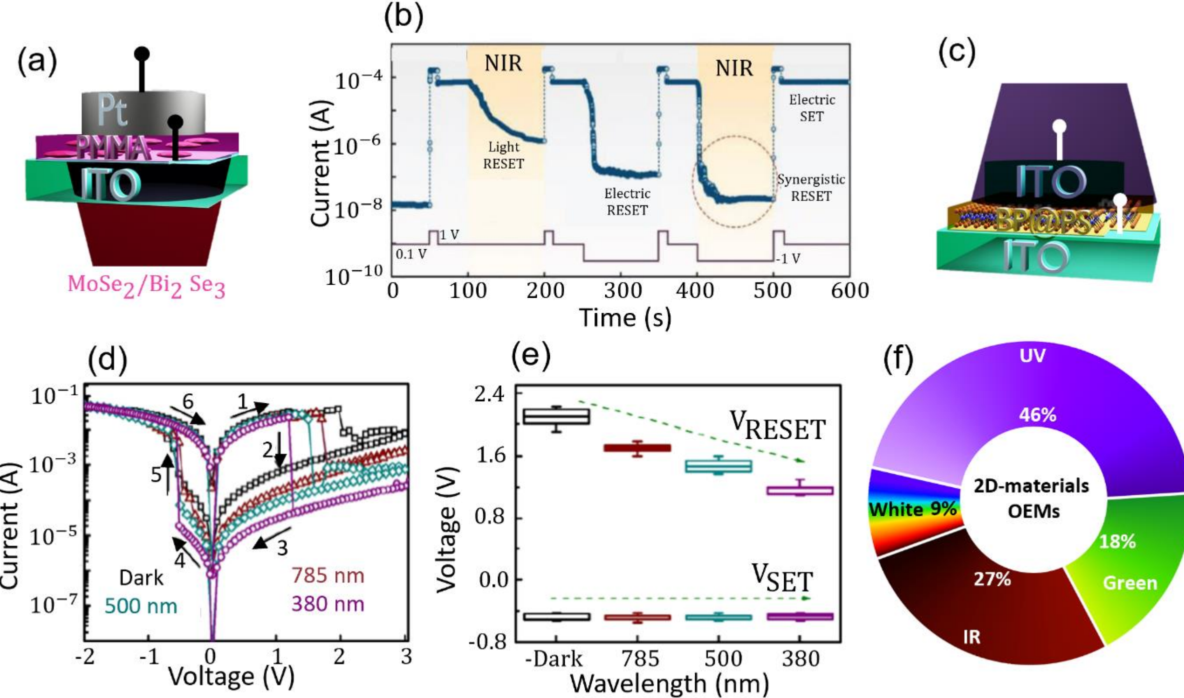

Figure 7. 4 2D-materials based OEMs characteristic behaviors. (a) ITO/$MoSe_2$/Bi_2Se_3@PMMA/Pt OEM illustrative structure and correspondent (b) current increase due to Set electric pulse and induced current decrease due to IR light irradiation (1.65 mW cm^{-2}). A synergistic Reset strategy, in which both electric and optical pulses are applied, could realize full Reset. ref. 109 John Wiley & Sons. [© 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim]. (c) ITO/BP@PS/ITO OEM illustrative structure and correspondent (d) I – V sweeps modulated by different wavelengths, displaying Set/Reset for negative/positive polarities, respectively and (e) V_{Set} and V_{Reset} obtained under different light illuminations. UV irradiation enables a smaller V_{Reset}. Reprinted (adapted) with permission from ref 110. Copyright (2020) American Chemical Society. (f) Statistical percentage on the light wavelength inducing RS reported by the works on 2D-materials OEMs.

The research on 2D-materials for vertically stacked OEMs is still at its infancy and requires further investigation. A complete review on 2D-based memristors and its challenges and future perspectives can be consulted in reference [111] in which the need for the development of proper 2D material films, that can be employed in high performance devices in a large-scale, is emphasized. Once this is accomplished, it is expected that this type of OEMs will offer a faster and more energy efficient switching, due to the atomically thin characteristics of 2D materials.[112] In fact, the switching speed is not yet

widely investigated in the small amount of available literature on vertically stacked OEMs based on 2D materials. As can be seen in **Table 7.3**, so far, mostly abrupt RS related to trapping and detrapping of electrons was described, which is more advantageous for in-memory computation and DNNs applications. NIR light irradiation has been explored in a higher percentage when compared with other classes of materials, as evidenced by **Figure 7.4(f)**, mostly for Reset operation. In fact, it has been previously observed that 2D-based photodetectors can be built for Terahertz detection[113,114] which can be very promising for memristors. To our knowledge, no fully-photonic 2D-based memristor has been proposed.

Table 7. 3 Characteristics of vertical OEMs based on 2D-materials.

N.S.: not specified at the original paper; N.A.: not applicable. Endurance is related to optical induced RS properties.

Active layer	Electrodes	Size (μm^2)	RS Behavior	λ_{light} (nm)	Light effect	DC Sweep Set/Reset (V)	I_{LRS}/I_{HRS} ratio	Endurance (cycles)	Electric retention	PPC
MoS_2[30]	p-Si/W	1.96×10^3	Analog	310	Performs Set	7/-6	$>1.00\times10^1$	N.S.	No	Yes
WO_3[107]	AZO/ITO	2.50×10^5	Abrupt	400-760	Enables switch-ing behavior	6/-6	$\approx2.00\times10^1$	200	1.00×10^3	Yes
GO[108]	ITO/Ag	1.26×10^5	Abrupt	380	Increases cur-rent	1/-1	$\approx1.00\times10^4$	5	N.S.	Yes
TiS_3[115]	ITO/Al	3.14×10^4	Abrupt	400 430 808	Increases cur-rent	-1/2	$\approx4.00\times10^2$	N.S.	1.00×10^4	N.S.
TiN_xO_{2-x}/MoS_2[116]	ITO/Al	7.85×10^3	Analog	365	Increases cur-rent	3/-3	$\approx1.00\times10^1$	N.S.	No	Yes
$MoSe_2/Bi_2Se_3$/PMMA[109]	ITO/Ag	N.S.	Abrupt	790	Performs Reset	2/-2	2.83×10^3	N.S.	1.00×10^6	N.A.
BP@PS[110]	ITO/ITO	3.14×10^4	Abrupt	380 500 785	Performs Reset	3/-1	1.52×10^3	N.S.	1.00×10^4	N.A.

7.2.4 1D-structured OEMs

Another strategy to build an OEM is to take advantage of 1D structured materials, such as nanorods (NRs) or nanoparticles (NPs) (**Figure 7.5(a)**), in order to achieve enhanced performance. Compared with thin-films, nanostructures provide higher surface-to-volume ratio and larger photon harvesting, that ultimately results in improved photoconductivity, with highly localized RS.[117] Another major advantage is the potential for miniaturization, as these nanostructures can usually be produced by bottom-up approaches allowing for a rigorous control of structures dimensions.[118,119]

The first report on a 1D-structured OEM dates back to 2012. Park *et al.* reported on a ZnO NR-based device with fluorine-doped tin oxide (FTO) and Au as electrodes.[120] Showing an abrupt-behavior, RS was only observed when the device was illuminated by a xenon light source and was ascribed to VOs filament formation/rupture. In the dark, oxygen molecules would be chemisorbed onto the surface of ZnO NRs acting as an oxygen source and preventing the VOs filament formation. Upon light irradiation, electron-hole pairs would be created, and the holes would combine with oxygen ions adsorbed at the ZnO, allowing for CFs creation. Moreover, the modulation of light incident angle was shown to regulate RS in ZnO NRs.[121] In this work, a surface treatment was carried out to induce hydrophobic properties on ZnO NRs, inducing the formation of an air bubble protecting the memristor when emerged into water. The device behaved as a resistor with no RS properties when the light beam incidence surpassed a critical angle at the water/air interface, because total internal reflection would occur and light would not reach the ZnO NRs. When the light beam incidence was below the critical angle, RS was observed. In another study, the photoconductivity of a ZnO NRs-based device was calculated to be about 10^4 and compared to the much lower 70 achieved in a ZTO thin-film based memristor.[122]

Furthermore, an heterojunction composed of ZnO and phosphorene (ZP) NPs showed a decreased V_{Set} under irradiation of UV, green, red and IR light, with the possibility of MLC.[123] In another work, ZP NPs were sandwiched between two PMMA layers and an analog RS was observed,[124] in which the current state could be increased by UV, green and red light. However, no PPC effect could be noticed.

Li *et al.* proposed an heterostructure composed of lead sulfide (PbS) QDs crammed between ZnO thin-films.[20] The authors were able to design a photonic memristor making use on the bandgap of the ZnO film (3.37 eV) and of the PbS QDs (1.15 eV). An optical induced Set was demonstrated by UV light, whereas photonic Reset was performed by IR light. Upon UV light exposure the same explanation in the concept of ionized oxygen vacancies was given by authors. However, for lower light energies such as IR light irradiation, electrons from QDs are excited, neutralizing ionized oxygen vacancies, resulting in the decrease of the current state of the device.

In another work, red light was used to achieve multiple states for MLC characteristics in a memristor composed of Sb_2Se_3/CdS NRs, with PPC effect.[125] The RS behavior was attributed to the

formation/rupture of CFs. It was clarified that under exposure, part of the irradiated light would be directly absorbed by NRs and other part would be reflected towards adjacent NRs, enhancing energy harvesting. NRs would act as trapping sites for photogenerated holes on the Se_2Sb_3 surface, which would increase the current state and the lifetime of photogenerated electrons, resulting in PPC effect.

Another interesting approach for MLC operation was proposed by Guo *et al.*. The memristor structure, had an active layer composed of Ag NPs embedded in Mxene-TiO_2 nanosheets. In this study, both Set and Reset were accomplished by electrical means and an additional state, medium resistance state (MRS) was realized by exposure to UV light, as exemplified in **Figure 7.5(b)**. MRS could be 2 orders of magnitude higher than HRS with fair retention of states (**Figure 7.5(c)** and **7.5(d)**).[126] The physical mechanism of switching was explained by VOs CFs facilitated by Ag NPs. A missing peak of atom signals around Ag NPs was found on the TEM analysis, which the authors related to an VO where the conductive path on LRS would originate. UV light could create electron-hole pairs in the TiO_2, increasing the content of Ti^{3+} and, thus, facilitating the creation of oxygen vacancies. Therefore, Ag NPs do not take part of the optical induced reaction in this case. This strategy can be used to decrease D2D and C2C variabilities by controlling the CFs position and minimizing randomness.

On the contrary, UV light was used to perform reset on an Ag NPs@TiO_2-based OEMs device[127] and, in this work, Ag NPs provided the means for an optical Set and Reset. An additional absorption peak in the visible region, not observed in the TiO_2 film, was found with the introduction of Ag NPs. Both visible light and UV irradiation caused an immediate current increase when the device was on the HRS. As can be seen in **Figure 7.5(e)**, when visible light was turned off, the device gradually decreased its current and stabilized in a state higher than the initial state (HRS) -indication of PPC effect. During UV irradiation, the current would also increase similarly to the previous described study. However, after UV was turned off, the current decreased to a lower conductance state than the HRS (**Figure 7.5(f)**). This light induced Set and Reset was related to an oxidation and reduction of Ag NPs, respectively. As schematically illustrated in **Figure 7.5(g)**, under visible illumination, hot electrons would be excited within the Ag NPs through the localized surface plasmon resonance (LSPR) effect and would hop to the conduction band of TiO_2, leaving positively charged Ag^+. This charge separation would induce an oxidation of Ag NPs and decrease the Schottky barrier at the Ag/TiO_2 interface, increasing the current state. On the other hand, UV light irradiation would promote the creation of electron-holes pairs in TiO_2. The resulting free electrons would then react with Ag, reducing the Ag^+ to Ag^0, increasing the Schottky barrier and decreasing the current state.

1D structures were also coupled with perovskites materials[128–131] for enhanced OE features. In most cases, an abrupt behavior on RS was reported and UV light was used to decrease V_{Set} and V_{Reset}.

Undoubtedly, meaningful attempts have been made in understanding how one can use 1D-structures coupled with other materials to manipulate light-induced RS and achieve photonic Set and Reset operations. A summary of the most relevant works, and its figures of merit, on this topic is

provided in **Table 7.5**. Once again, IR light provoked RS has the smallest percentage on the works reported, as can be seen in **Figure 7.5(h)**.

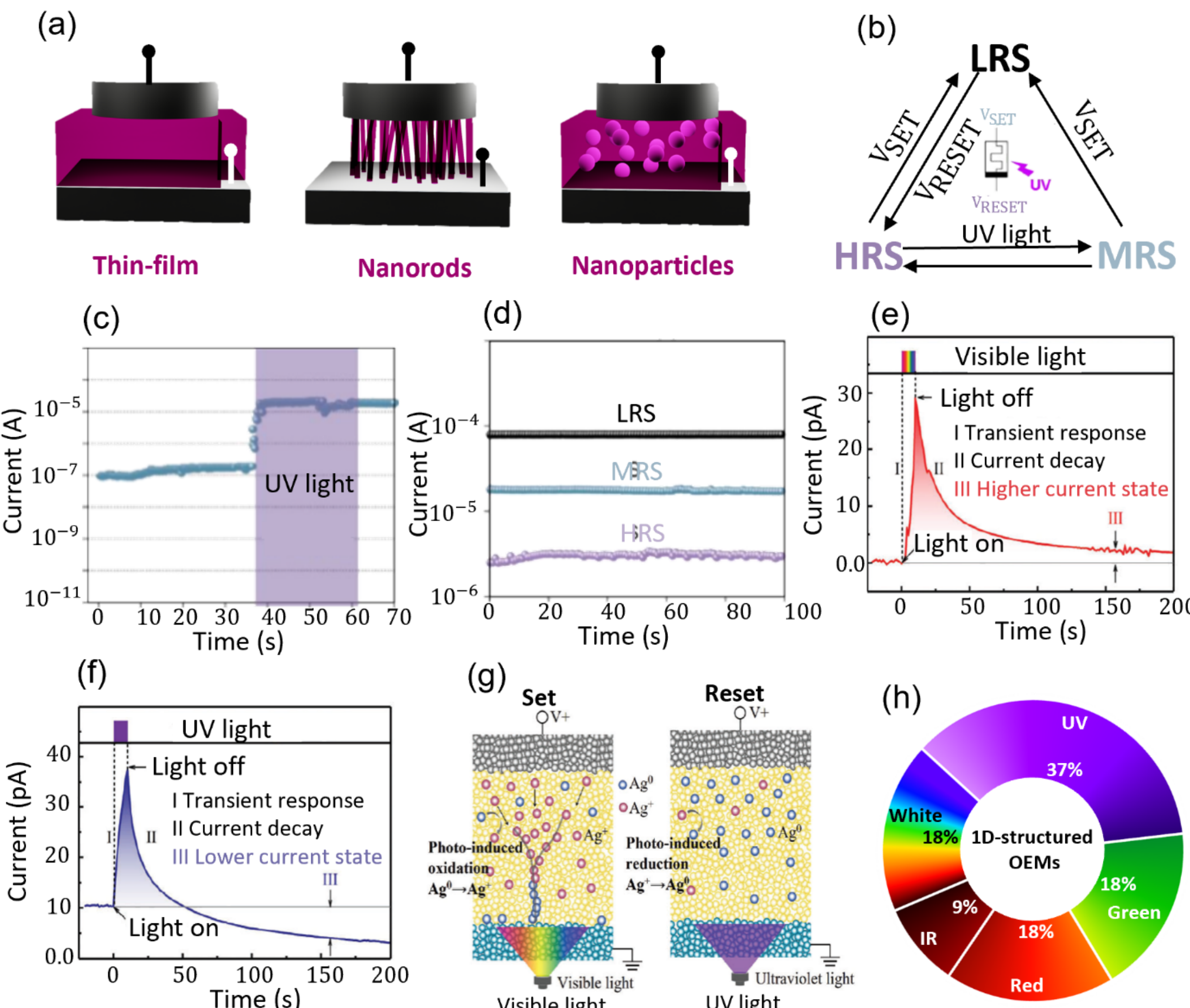

Figure 7. 5 One-dimensional-structured OEMs characteristic behaviors. (a) Schematic illustration of memristors based on thin-films, NRs and NPs; (b) Proposed operating procedure using light as input to add a medium resistance state (MRS), on a memristor composed of Ag NPs embedded in Mxene-TiO_2 nanosheets and correspondent (c) current response under UV irradiation and (d) retention of the 3 resistance states achieved with this memristor structure. Reprinted (adapted) with permission from ref. 126. Copyright (2021) American Chemical Society. (e) Current increase under visible light irradiation (21.8 mW cm^{-2}) on a memristor based on Ag NPs embedded on a TiO_2 thin film. Once the light was turned off, the current decreased and stabilized in a state higher than the initial one (Set) and (f) current response, correspondent to the same memristor structure, under UV illumination (3.7 mW cm^{-2}). When the light was turned off, the current decreased and stabilized in a state lower than the initial one (Reset) and (g) correspondent proposed physical mechanism of light induced Set and Reset operations schematic illustrated. Reproduced from ref. 127 CC BY 4.0. (h) Statistical percentage on the light wavelength inducing RS reported by the works on 1D-structured based OEMs.

It is noticeable, however, that the physical mechanism of RS behavior under light on nanostructured materials still requires clarification for further progress. One NR/nanowire (NW)/nanoribbon

(NRi) can be considered as a single device as a means to fully understand the light interaction with the material in these nanostructures. However, manipulating the RS behavior still poses as a challenge since this type of memristors usually suffer from poor retention and endurance related to Joule heating, high C2C variability and high operating voltages.[118,132] As an alternative, a network of the nanostructures can be considered as a single device or as an array of devices. The second approach could offer incredible high-density integration since the nanostructured network could be organized in a crossbar configuration. As a prospective example, core-shell NRs could be employed as both bottom and top contacts and single memristor cells would be represented in each crosspoint. The main challenge here is the ordered positioning of the nanostructures.[132] Additionally, the access to single cells would be hard to accomplish due to such small features.[118] Moreover, high D2D variability has been reported for memristors with the smallest areas[2] which can be an indication of how challenging decreasing variability is in single nanostructures. At this point of the research and while effective solutions do not arise to all the above challenges, NPs embedded in thin-films as active layer appears to be a more straight-forward approach to take advantage of nanostructured materials to enhance photo-harvesting in OEMs.

Table 7. 4 Comparison of OEMs characteristics based on 1D structures.

NRs (nanorods); NPs (nanoparticles); NWs (nanowires); NS (nanostructure); QDs (quantum dots); NRis (nanoribbons).

N.S.: not specified at the original paper; N.A.: not applicable. Endurance is related to optical induced RS properties.

Active layer	1D Structure	Electrodes	RS Behavior	λ_{light} (nm)	Light effect	DC Sweep Set/Reset (V)	I_{LRS}/I_{HRS} ratio	Endurance (cycles)	Electric retention	PPC
ZnO[120]	ZnO NRs	FTO/Au	Abrupt	200-2500	Enables switching behavior	4.5/-3	≈1.00×10^{1}	N.S.	No	Yes
ZnO[133]	ZnO NRs	FTO/Ag	Analog	365	Increases I_{LRS}/I_{HRS} ratio Improves endurance	4/-4	N.S.	40	N.S.	Yes
ZnO[122]	ZnO NRs	FTO/Pt	Analog	310	Increases current	2.5/-2.5	>1.00×10^{2}	N.S.	No	Yes
ZP[123]	ZP NPs	ITO/Al	Abrupt	380 532 633 785	Decreases V_{Set}	5/-5	3.63×10^{8}	N.S.	N.S.	N.S.
PMMA/ZP/PMMA[124]	ZP NPs	ITO/Al	Analog	380 532 633	Increases current	6/-6	<1.00×10^{2}	N.S.	No	No
ZnO/PbS/ZnO[20]	PbS QDs	ITO/Al	Analog	356 780	UV performs Set IR performs Reset	1/-1	>1.00×10^{1}	N.S.	N.S.	Yes
ZWO_4[134]	ZWO_4 NWs	Ti/Ag	Abrupt	400-760	Increases I_{LRS}/I_{HRS} ratio	6/-6	≈3.00×10^{1}	N.S.	N.S.	N.S.
$SnWO_4$[135]	$SnWO_4$ NPs	FTO/Ag	Abrupt	400-760	Adds intermediate state	1/-2	≈1.00×10^{2}	100	>5.00×10^{2}	N.S.
$Ce_2W_3O_{12}$[136]	$Ce_2W_3O_{12}$ NS	FTO/Ag	Abrupt	400-760	Adds intermediate state	3/-3	≈1.00×10^{1}	50	N.S.	N.S.

$CuCr_2O_4$[137]	$CuCr_2O_4$ NPs	FTO/Ag	Abrupt	400-760	Adds intermediate state	1/-1	≈1.00×10^3	100	N.S.	N.S.
Cu_3P[138]	Cu_3P NRis	ITO/Ag	Abrupt	660	Increases current	-1.5/3	>1.00×10^3	N.S.	1.00×10^4	Yes
Sb_2Se_3/CdS[125]	Sb_2Se_3/CdS NRs	$MoSe_2$/ITO	Abrupt	650	Increases current	1/-0.5	5.00×10^1	3000	2.00×10^4	Yes
AMT (Ag @Mxene-TiO_2)[126]	Ag NPs	ITO/Au	Abrupt	375	Adds intermediate state	5/-5	<1.00×10^2	3000	5.00×10^3	Yes
Ag-TiO_2[127]	Ag NPs	FTO/Au	Abrupt	350 532	Green performs Set UV performs Reset	2/-2	N.S.	N.S.	>1.00×10^3	Yes

7.2.5 Remarks

All the works analyzed have provided significant developments in the realization of OEMs using light as an additional input to modulate RS behavior. Both analog and abrupt-RS can be obtained by engineering all sort of material structures. Therefore, it is important to keep in mind what is the application envisioned for the development of an OEM with the required features, as will be discussed in the next section.

Metal oxide-based OEMs, in their majority, show abrupt RS with sufficient retention time well-suited for digital processing in-memory architecture. For such application, the PPC decay should be suppressed for large enough time, hence, any charge/ion drift destructing the stored state can arise an issue. As shown in the tables above, especially for 2D-materials based OE RS devices, IR light has been demonstrated to induce Reset in some cases. IR induced RS is very appealing for wireless systems to enable conversion and storage of IR data. However, for the realization of completely wire-free systems, both Set and Reset operations need to be performed by light.

Semiconductor oxides and 1D-structured materials as switching medium in OEMs have already shown desirable photonic behavior. Here, strategies such as double-layered thin films with different oxygen contents to arrange a dynamic equilibrium between ionization and neutralization of defects can be applied. In this case, a high energy wavelength can be used to set the device into a saturated photocurrent and then a low energy wavelength can promote the neutralization of defects performing reset. Moreover, the combination of thin films with nanostructured materials such as QDs or NPs can also be employed for a photonic approach. 2D-materials such as graphene can also be coupled with nanostructures such Au NPs for an enhancement of the photocurrent as already shown for a 3-terminal device.[139]

The switching speed was expected to be enhanced in optical induced transitions, especially for 2D-based or nanostructured OEMs. However, from the available literature this is not yet noticeable. One of the reasons is the immaturity of the technological concept, which leads to most of the reported devices having common bottom contact and not ready for further investigations. However, the switching speed improvement should be a top priority in future developments.

To tackle high performance, OE devices based on metals of nanometer dimension should be also investigated, which has not been explored yet. As can be seen in reference [140] the performance in terms of switching speed and retention is superior than bulky systems where slow-driving physical mechanisms are dominant. However, one restriction of the pure metallic device concept relies on miniaturization, where maintaining compositional integrity is difficult at reduced dimensions.

If the PPC effect is suppressed in favor of sufficient retention time, DNN applications can be targeted. On the other hand, PPC decay can be further investigated in the scope of SNNs systems. In this regard, short term and long-term memory and time notion should be realized. Time encoding

based on optical stimulus turns the system into an event-driven network which favors power efficiency and allows the computational machine to become a truly scalable hardware SNN with yet unexplored computational capabilities.[140]

7.3 OEMs beyond the device level

OEMs have tremendous potential for the development of AI hardware. Since these devices can realize computing in different forms depending on their single-cell characteristics, new possible applications are constantly being trialed.

To be integrated in circuits, novel architecture models should be envisioned as a matrix of OEMs, forming as many synapses as possible, processing element inputs, with built-in auxiliary electronics inspired by pixel circuit, forming an artificial optical neuron.

The advantage of dense circuits and high-speed optics can be realized if program/write always happens in optical domain following electrical read-out signal. However, for different applications such as DNN or SNN, various electrical components are required to be considered such as photovoltaic devices and photodetectors to convert/revert electrical/optical signals.

For instance, plasmonic OEMs with the possibility of optical read-out have been proposed. For this purpose, conductive-bridge memristors were developed in which metallic CFs are responsible for RS behavior. In such, when the device is at LRS, metallic CFs block the passage of light whereas at the HRS, light can easily reach a detector.[141,142] Other studies show an optical read using photovoltaic effect.[143,144]

Light emitting memristors (LEMs) have been developed that can be used for an optical read and write-strategy.[145] Moreover, these light emitting devices can be used as optical communication between layers in ANNs without the need of external light sources. Zhu *et al.* proposed an OE artificial nerve composed of LEM layers in which the optical output of one layer was transmitted to the next layer, while simultaneously realizing dynamic adjustable transmissions.[146]

Therefore, light stimulus can be used in different strategies to propel the development of an efficient ANNs hardware. On the neural network itself, light input can modulate the synaptic weight update, which corresponds to the conductance state of the memristor. In this case, OEMs can accomplish a variety of synaptic functions bringing us closer to a brain-inspired AI technology. In the next sections of this paper, a review on the already demonstrated capabilities of inorganic OEMs regarding logic gates, neuromorphic functions and, in more detail, artificial visual systems is presented.

7.3.1 Arithmetic units and Boolean logic

Boolean logic is a form of algebra based on the truth possibilities of true or false that correspond to logic 1 or 0. OEMs can exhibit different non-volatile resistance states at different light wavelengths irradiation, which allows for logic gates and arithmetic functions to be employed. This approach

enables in-memory computation which is a significant enhancement from the conventional logic gates based on volatile switches such as transistors, where extra power consumption and time are required due to the physical separation of storage and processing units.

AlO_y/CeO_2 OEM in which 4 different resistance states could be realized using blue and green irradiation with different intensities (4 and 6 pW/µm^2), enabling information storage of 8-bit codes, was reported by Tan *et al.*.[80] Broadband light irradiation also showed an increase of current state dependent on light intensity with a retention of state demonstrated for 10^4 s. Moreover, a linear relation between resistance state and number of light pulses was used to employ counter and adder arithmetic functions.

Moreover, an OR gate can be accomplished by OEMs,[61,70,71] in which a light pulse is used as input A, with 0 corresponding to no light and 1 to irradiation, and an electric pulse as input B, with 0 corresponding to 0 V (or to the read voltage) and 1 corresponding to an input voltage value of X V, in which X > 0 V (or the read voltage) and depends on the device's material structure and its Set voltage, as schematically illustrated in **Figure 7.6(a)**. The output should be 1 when A or/and B is at 1 state. In **Figure 7.6(b)** and **7.6(c)**, an experimentally demonstration of an OR gate is presented, relating to an OEM of structure $FTO/BiVO_4/TiN$.[147] The authors defined the optical input as 1 when the device was irradiated with laser of 405 nm and 11 pW/µm^2 and the electric input 1 was not described in the original work. A threshold value of current (10^{-6} A) was decided and, therefore, a current output below 10^{-6} A is logic 0 and above 10^{-6} A is logic 1. PPC effect was not shown, which significantly hinders applications where light-induced state storage is necessary. Therefore, OEMs that can respond to multiple light wavelengths with some degree of retention are preferred.

In this regard, an AND and OR logic gate has been employed in a single cell by OEMs.[79,89] Light and electric pulses are inputs A and B with 0 and 1 possibilities. Contrary to the OR gate, in the AND gate the output should be 1 only when both inputs A and B are 1. Wang *et al.* demonstrated an AND logic gate in which red light was used as input A with a low energy consumption of 4.503 nJ.[79] Red light irradiation by itself could not increase the current state to the defined output logic 1 (I_{output} > 400 nA). Therefore, the output logic value was 1 only when the electric input was 1 (4 V with current compliance (CC) set to 1 µA) and the optical input was 1 (red light irradiation). Additionally, using the same device, blue light irradiation could be used for an OR gate with an energy consumption of 4.526 nJ. Blue light illumination supplied enough energy to increase the current state to above the threshold value defined to the output 1 (I_{output} > 400 nA). Moreover, the electric input (input B) for the OR gate was defined as 1 for a 4 V input with higher CC than the AND gate (1 mA) to ensure that only the combination of both logic inputs 0 would result in the logic 0 output.

In a different approach, a 5×5 array was constructed to perform logic optoelectronic AND and OR gates. In this experiment, schematically illustrated in **Figure 7.6(d)**, two images were introduced by visible light (λ = 600 nm for 4 s) in the form of letter Y and X for both AND and OR gates. In this case, both logic inputs are optical (letter Y and X). The AND gate could be realized when all OEMs in the

crossbar were in HRS before light irradiation, since only the cells irradiated twice would show an increase of current state to above the threshold value, as can be seen in Figure 7.6(e). The OR gate was in place when all devices in the crossbar were in LRS before irradiation, since the output current of all cells irradiated at least once would increase to above the threshold defined to output logic 1. The results showed an accurate output, proving these crossbar logic OE operations could be applied in larger scales for image processing and storage.[81]

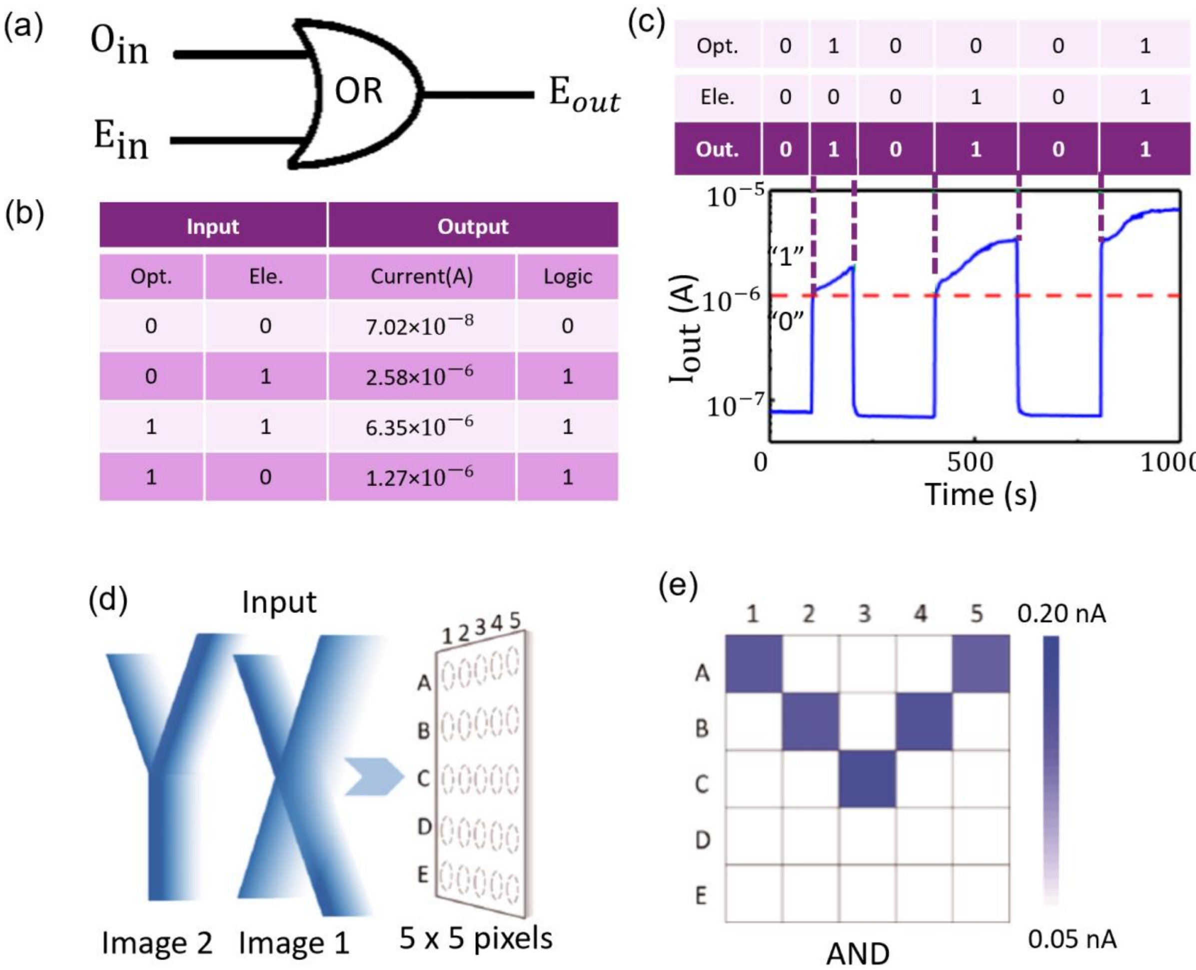

Figure 7. 6 Typical OR and AND logic gates. (a) Schematic illustration of OR gate with two inputs, one optical (O_{in}) and one electric (E_{in}), and one electric output (E_{out}). Reprinted from ref. 147, with the permission of AIP Publishing. (b) OR truth table displaying experimental E_{out} values of an OEM and (c) respective E_{out} measured in time for different OR gate combinations. Reprinted [adapted] from ref. 147 with the permission of AIP Publishing. (d) Two images were inputted through visible light in the form of letters Y and X when the devices in a 5 × 5 matrix were in (e) the HRS for an AND gate. Reprinted with permission from ref. 81. Copyright (2017) American Chemical Society.

NOT operation is also indispensable to the spanning set of a complete logic vector space. Tan *et al.* showed NOT operation with an electric pulse that performed reset.[81] In this work, a complex logic

design was proposed that comprised an AND gate when input A (light) and input B (electric Set) were applied. This AND gate could be reconfigured to an OR gate by applying an additional light pulse before inputs A and B. To perform NOT, an additional electric pulse for Reset was applied after inputs A and B, deleting the information encoded, as illustrated in **Figure 7.7(a)**. The experimental results can be consulted in **Figure 7.7(b)** and show that this strategy can accurately perform these operations. Additionally, optical adder and digital-to-analog converter (DAC) functions were realized by employing two light pulses as inputs. These light inputs can be combined into binary digital inputs in 00, 01, 10, 11 forms, in which 0 corresponds to dark and 1 corresponds to light irradiation. The current output will be the analog addition of the equivalent of the inputs.

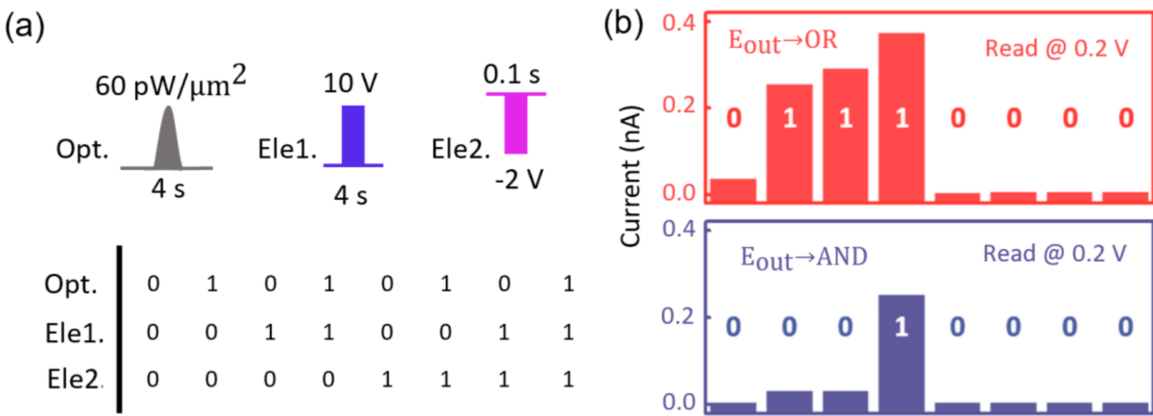

Figure 7. 7 Example of NOT operation in OEMs. (a) Schematic illustration of three possible inputs comprising one optical (O_{in}) and 2 electric (E_{in1} and E_{in2}) and one electric output (E_{out}). E_{in2} was used to reset the device and perform NOT. Truth table of logic operations (AND, OR, AND with NOT and OR with NOT. (b) Experimental results of AND and AND reformatted with NOT operation (in blue) and OR and OR reformatted with NOT operation (in red). Reprinted (adapted) with permission from ref. 81. Copyright (2017) American Chemical Society.

More complex logic gates were also demonstrated such as IMP using two OEMs in series with a conventional resistor in a more complex strategy. NAND could also be observed using blue light.[74] In a recent work, all possible 16 logic functions were realized in a single cell ZnO OEM.[90] However, except for the OR and NIMP functions, a control light had to employed to experimentally demonstrate the other 14 logic functions which ultimately means two light inputs in different sequences for each specific function.

Although these works provide efficient methods for complicated operations using OEMs, the proposed system strategies are somewhat complex utilizing several inputs as part of the operations procedure. In **Table 7.5**, a summary of the demonstrated logic gates and arithmetic functions by OEMs can be consulted. It is important to note that Boolean logic is not the only approach to construct integrated circuits that perform mathematical operations. A programmable fuzzy-logic gate approach was

proposed as a simpler alternative, in which negative pulses would not be necessary for NOT operation,[148] using an OEM that performed material nonimplication and logical true operations using light and electric stimulus.

Table 7. 5 Description of logic gates realized with OEMs and its characteristics.

N.S.: not specified at the original paper; N.A.: not applicable; BB: Broadband. ILRS/IHRS ratio is related to the maximum ratio accomplished by light irradiation.

Structure	Size (μm^2)	λ_{light} (nm)	$P_{light\ pulse}$ (mW/cm^2)	$W_{light\ pulse}$ (s)	I_{LRS}/I_{HRS} ratio	Logic gate / Arithmetic function	PPC
$Al/AlO_y/CeO_{2-x}/ITO$[80]	7.85×10^3	400-800 499 560	VIS 0.40, 0.60, 6.00 BB 0.08, 2.10, 6.00	3.00	VIS≈3.00×10^2 BB≈1.00×10^3	Counter Adder	Yes
FTO/PVA/SPTP/Ag[71]	N.S.	365	1.00	N.S.	>1.00×10^1	Adder OR	No
$FTO/BiVO_4/TiN$[147]	7.85×10^3	405	1.10	N.S.	>1.00×10^1	OR	No
ITO/ZnO/Ag[89]	4.00×10^4	400-700	N.S.	1.00	>1.00×10^1	AND OR	Yes
$n-Si/Ta_2O_5/Ta_2O_{5-x}/Ag$[79]	5.03×10^3	460 620	7.00	0.40	>1.00×10^3	AND OR	Yes
$Al/AlO_y/CeO_{2-x}/ITO$[81]	7.85×10^3	600	6.00	4.00	>1.00×10^1	Adder AND OR NOT	Yes
$p-Si/HfO_2/Pt$[74]	1.26×10^3	450	7.96×10^{-4}	N.A.	>1.00×10^4	IMP NAND OR	No
Pt/ZnO/Au[90]	7.85×10^3	530 650	3.60×10^{-2}	N.S.	>1.00×10^2	ALL	Yes

7.3.2 In-memory and neuromorphic computation

A range of synaptic functions can be emulated by memristors using their resistance levels as synaptic weights. A non-volatile gradual increase in the memristor conductance state is usually called potentiation, which translates into a higher synaptic weight and simulates the connection between two neurons becoming stronger. On the contrary, depression is when the conductance states decrease related to a lower synaptic weight, which happens as the connection of two neurons become weaker. Therefore, memristive crossbars have been proposed as an alternative to realize ANNs, on hardware in a highly energy, cost and fast efficient manner. OEMs, with their additional light stimulus, can further enhance the advantages reported for neuromorphic computing. Since it is physical separated from the memristor's electrodes, light can act as non-invasive write input to train synaptic weights in cross-bars.[149,150]

DNNs are used in several tasks such as pattern recognition, speech recognition or machine translation.[151] In memristor-based DNNs, crossbars perform vector-matrix-multiplication operations (VMMs) as the result of Ohm's and Kirchhoff's summation laws,[152] as schematically illustrated in **Figure 7.8(a)**. The input data is applied as a voltage/current vector at the rows and the output can be read at the columns.[153] These crossbars usually suffer from sneak-path current issues, which are related to electric interference between cells, since all the memristors are connected to each other through conducting wires.[154] A transistor in each cell can be added as a selector element,[24,155,156] however, it increases energy consumption and cell area. In photonic crossbars, light as an alternative strategy could solve this problem in an energy efficient manner.

DNNs composed of ZnO-based OEMs to perform pattern recognition[89] was proposed by Wang *et al.*. A simulation was carried out using potentiation and depression experimental results using input, hidden and output layers composed by 1024, 256 and 15 neurons, respectively. The potentiation and depression were demonstrated using visible light pulses and electric pulses, correspondingly, with a ratio of 25. Based on the back-propagation algorithm simulation, 15 input images were trained in the DNN and after 1000 epochs, the recognition rate was of 86.7 %, demonstrating excellent potential. To our knowledge, this work reports on the highest POT/DEP ratio achieved by an OEM so far. However, it still does not quite reach the requirement of 10^2 ratio to ensure less impact of noise in the measurement.[157] Another ZnO-based OEM suited for DNNs was proposed and simulated for pattern recognition as depicted in **Figure 7.8(b)**. All-photonic potentiation and depression was demonstrated using visible light inputs and a pattern recognition accuracy of more than 90 % was achieved (**Figure 7.8(c)**) and 8d)).[90] However, potentiation/depression ratio was only 3.2 which is very low for real implementation.

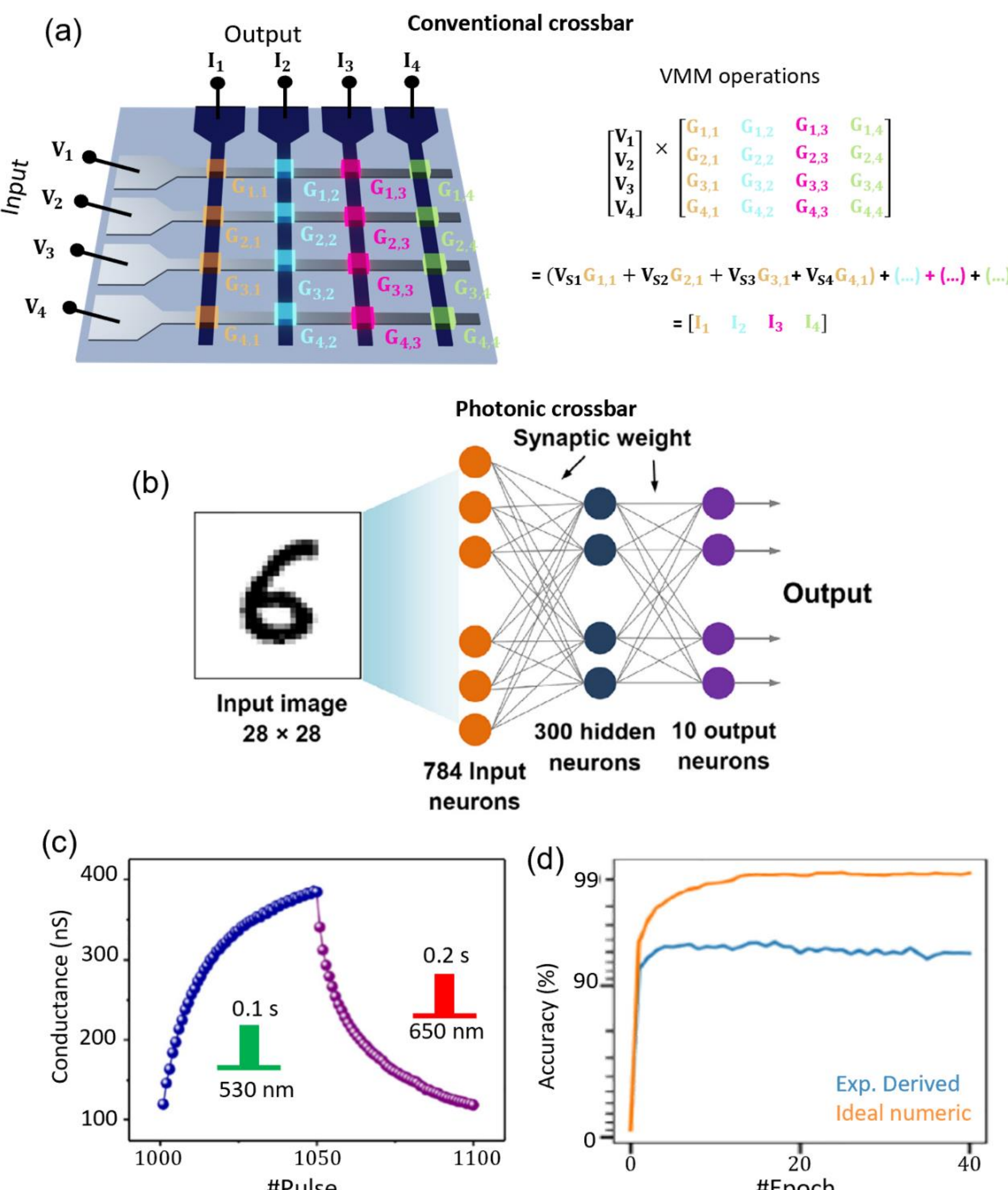

Figure 7. 8 Example of DNNs features using OEMs. (a) Schematic illustration of a 4 × 4 conventional memristive crossbar and corresponding VMM operations. (b) Illustration of a pattern recognition simulation based on a photonic memristive crossbar. DNN composed of 784 input neurons, 300 hidden neurons and 10 output neurons, connected by OE synapses. (c) Experimental optical potentiation and electric depression test realized by green and red light pulses displaying possible synaptic weights to be implemented in the DNN. (d) Recognition rate of simulated DNN for pattern recognition. Reproduced from ref. 90 CC BY 4.0.

In fact, very few works related to OEMs report on DNNs applications. Not only because of the high ratio requirement but also due to the unwavering criterion of long retention data.[157] As evidenced by the previous sections of this review, this long light-induced current retention is possible with

suppression of PPC decay. However, a controlled PPC decay effect by temporal light stimulus is much more useful for SNNs.

The exploration of the PPC effect to emulate SNN related synaptic functions was first proposed by Lee *et al.* using planar AOS-based memristors.[158] Since then, several works have followed the trend using vertical OEMs. For instance, using different long enough irradiation time (not light pulses < 1 s), Wang *et al.* showed the transition from short-term plasticity (STP) to long-term plasticity (LTP) as can be seen in **Figure 7.9(a)**.[125] The irradiation time affected the PPC dynamic. In the biological system, STP usually last from seconds to dozens of minutes whereas LTP can be determined by hours-weeks or even a life-time of no memory loss.[159] Another way to realize the transition from STP to LTP is by increasing light power, as can be seen in **Figure 7.9(b)**.[160] A schematic illustration of the multistore memory model is presented in **Figure 7.9(c)**.[161] As can be perceived, the transition from STP to LTP should be performed by repetition (rehearsal) which can be accomplished by increasing the frequency of light pulses. An example is presented in **Figure 7.9(d)**.[30]

In fact, by continuously irradiating an OEM, the device will suffer a learning process.[116,138] In **Figure 7.9(e)**, a learning and forgetting test is presented from a double layer ZnO/HfO_x based memristor.[160] During the first learning/forgetting stage, the synaptic weight increases during a 7 s long UV illumination and then, when the light is turned off, gradually decreases (PPC effect) to an intermediate state. Once the light is turned on again, only 4 s are required for the device to return to the synaptic weigh achieved with the first leaning, which shows faster re-learning. Moreover, the retention ratio also increases from 52 % to 74% in the second process, showing harder forgetting. The learning and forgetting synaptic function can also be demonstrated under light pulses which is more realistic for future energy-efficient applications, instead of a constant illumination method.[99]

Another common synaptic function is paired-pulse facilitation/depression (PPF/PPD). The PPF/PPD index is calculated as the relative current state difference between single and double spikes ($(I_2 - I_1)/I_1$) with the same power and width, yet different intervals between double pulses.[77,87,101] An experimental demonstration of PPF can be consulted in **Figure 7.9(f)**, related to a Mo/Sb_2Se_3/CdS/ITO OEM and 650 nm light pulses.[125] PPD was also reported regarding an OEM in which potentiation was performed electrically and depression in a combination of electric pulses and constant optical input.[109]

A more complex synaptic function is spike-time dependent plasticity (STDP), key performance applied in SNN models. Here, the synaptic weight change (ΔW) is modulated by the time difference between pre and post-synaptic spikes. As an example, Song *et al.* designed a pulse scheme strategy for STDP using two OEMs.[103] The pre-synaptic light spike was applied to one of the devices and the post-synaptic light spike was applied to the other one. In another work, the pre-synaptic pulse was applied with light and post-synaptic pulse was electrical.[125] The time interval between the two spikes was defined as $\Delta t = t_{pre} - t_{post}$ and the $\Delta W = (\Delta W_2 - \Delta W_1)/\Delta W_1$. In **Figure 7.9(g)**, the experimental results can be seen. ΔW decreases with longer Δt, as expected, which is typical STDP characteristics of biological synapses.[21]

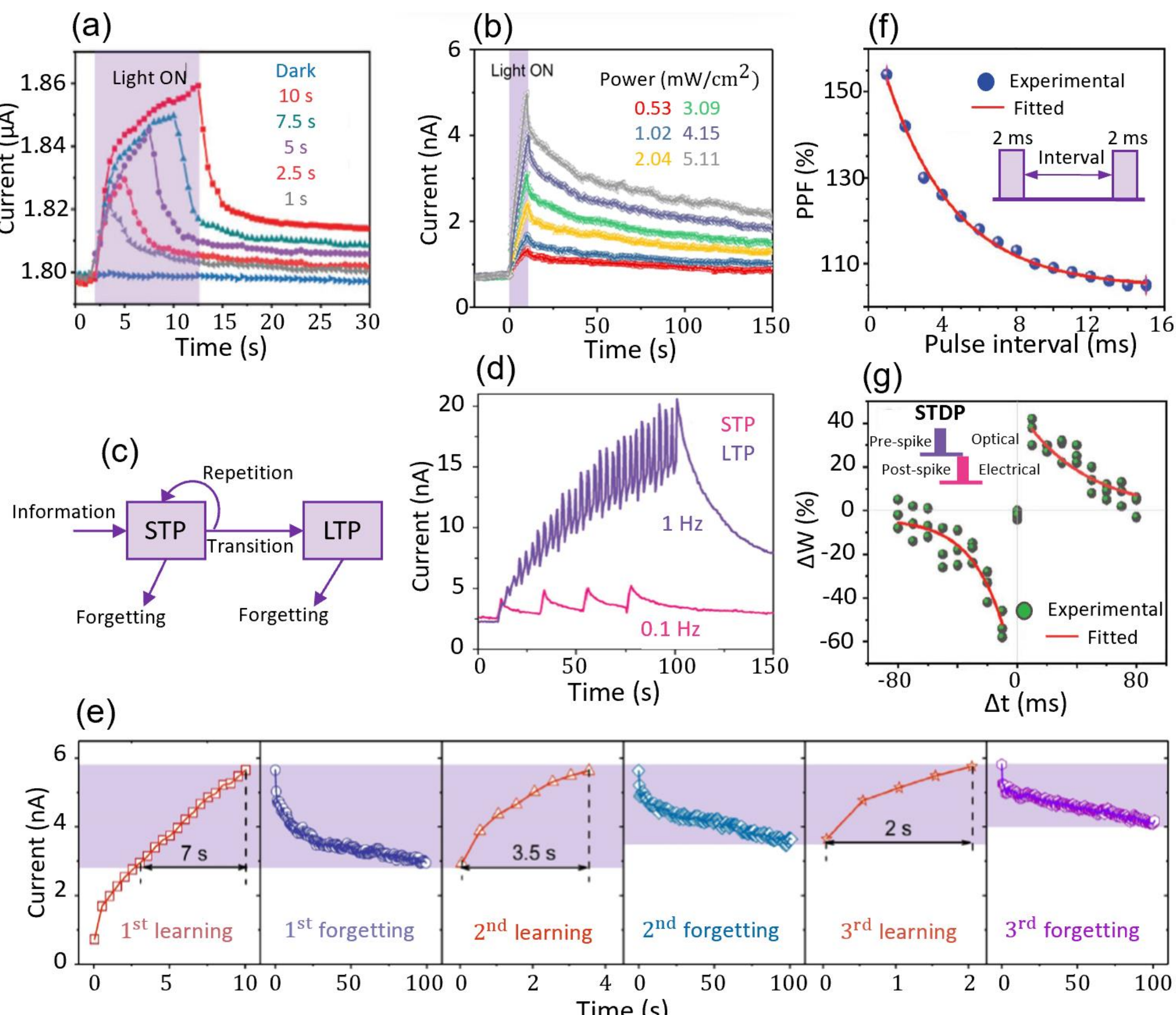

Figure 7. 9 SNNs synaptic functions performed by OEMs. (a) Synaptic weight increase under 3.58 mW cm^{-2} of UV light with different irradiation time, followed by the PPC decay, displaying the transition between STP to LTP.[116] John Wiley & Sons. [© 2021 Wiley-VCH GmbH]. (b) Synaptic weight increase under different power of UV light, followed by PPC decay, displaying transition between STP to LTP. Reprinted [adapted] from ref. 160, with the permission of AIP Publishing. (c) Schematic illustration of the multistore memory model, showing transition from STP to LTP trough repetition (rehearsal). (d) Experimental transition from STP to LTP trough different frequencies of optical UV pulses.[30] John Wiley & Sons. [© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim]. (e) Photo-induced learning and forgetting experience, displaying an easier re-learning and harder forgetting by sequenced processes. Reprinted [adapted] from ref. 160, with the permission of AIP Publishing. (f) PPF variation with respect to a double light spike with different intervals. (g) STDP- Variation of connection strength (ΔW) between optical pre and electrical post synaptic spikes applied in a vertical OEM as a function of Δt.[125] John Wiley & Sons. [© 2022 Wiley-VCH GmbH].

Furthermore, brain-inspired synaptic functions were realized in all-photonic memristors.[26,20] STDP was emulated in an IGZO device using blue light for potentiation and IR light for depression.[26] The transition from STP to LTP and PPF/PPD functions were demonstrated using UV and IR light on a ITO/ZnO/PbS(QDs)/ZnO/Al photonic memristor.[20]

The few studies reporting on all-photonic realized synaptic functions uncover the infinite potential of OEM for brain-inspired neuromorphic computation. In **Table 7.6**, a summary on the synaptic

functions of inorganic OEMs is presented. The scaling possibilities of RS devices, together with an all optical controlled strategy for the implementation of different weights in ANNs, suggest that OEMs crossbar implementation could offer an abysmal efficiency improvement over silicon-based technologies.[162]

Table 7. 6 Characteristics of vertical OEMs with metal oxides as active layer.

N.S.: not specified at the original paper; N.A.: not applicable; BB: broadband. Endurance is related to optical induced RS properties.

Structure	Size (μm^2)	λ_{light} (nm)	$P_{light\ pulse}$ (mW/cm^2)	$W_{light\ pulse}$ (s)	$V_{electric\ pulse}$ (V)	$W_{electric\ pulse}$ (ms)	POT	DEP	POT/DEP ratio	Synaptic functions	PPC
ITO/ZnO/Ag[91]	4.00×10^4	400-700	N.S.	1.00	-2.00	10	Optical	Electrical	25.0	DNNs	Yes
Pt/ZnO/Au[92]	7.85×10^3	530 650	0.03	POT 0.10 DEP 0.20	N.A.	N.A.	Optical	Optical	3.20	DNNs	Yes
Mo/Sb_2Se_3/CdS/ITO[127]	N.S.	650	200	0.02	N.S.	N.S.	Optical	Electrical	50.0	STP/LTP PPF STDP Learning/Forgetting	Yes
ITO/MoS_2/Bi_2Se_3@PMMA/Ag[111]	N.S.	790	1.65	Const.	0.50	1	Electrical	Optical/Electrical	≈2.00	PPD	N.A.
ITO/Cu_3P/Ag[140]	5.03×10^3	660	200 140 80.0	Const.	0.54 0.42 0.39	10	Optical	Electrical	>10.0 >10.0 >10.0	Learning/Forgetting	Yes
ITO/TiS/Al[117]	3.14×10^4	400 530 808	10.0	Const.	0.42 0.39 0.35	10	Optical	Electrical	>2.00	Pavlov's dog	Yes
ITO/TiN_xO_{2-x}/MoS_2/Al[118]	7.85×10^3	365	3.15	10.0	N.S.	N.S.	Optical	N.S.	N.S.	STP/LTP PPF Learning/Forgetting	Yes
Pt/TiO_x/Ti[79]	1.96×10^3	465	12.0	0.05 to 2.00	N.S.	N.S.	Optical	N.S.	N.S.	PPF	Yes
ITO/ZnO/Ag[90]	7.85×10^3	366	4.60	0.10	N.S.	N.S.	Optical	N.S.	N.S.	STP/LTP PPF	Yes

$Al/AlO_y/Zn_{O1-x}/ITO$[103]	7.85×10^3	310	N.S.	1.00	-4.00	10	Optical	Electrical	≈10.00	STP/LTP PPF	Yes
$FTO/ZnO/In_2O_3$[89]	N.S.	365	0.40	1.00	-1.00	20	Optical	Electrical	≈2.00	STP/LTP PPF	Yes
Al/IGZO/ITO[105]	2.50×10^3	400	0.15	0.25	2.50	10	Optical	Electrical	≈8.00	STP/LTP STDP	Yes
ITO/ZTO/ITO[101]	1.77×10^4	405	50.0	N.S.	-1.80	0.07	Optical	Electrical	<2.00	PPF Learning/Forget-ting	Yes
$ITO/ZnO/HfO_x/Au$[162]	3.14×10^4	365	5.11	2.00	-2.00	50	Optical	Electrical	≈10.00	STP/LTP PPF Learning/Forget-ting	Yes
$p\text{-}Si/MoS_2/W$[31]	1.96×10^3	310	0.11	1.00	-800	5	Optical	Electrical	≈10.00	STP/LTP PPF	Yes
$Pt/IGZO_{(HO)}/IGZO_{(LO)}/Au$[27]	7.85×10^3	420 800	POT 0.020 DEP 0.024	POT 1.00 DEP 1.00	N.A.	N.A.	Optical	Optical	≈2.00	STDP	Yes
ITO/ZnO/PbS QDs/ZnO/Al[20]	N.S.	356 980	0.70 800	0.20 0.20	N.A.	N.A.	Optical	Optical	>10.00	STP/LTP PPF/PPD	Yes

7.3.3 Artificial visual systems

In the human visual system, eyes collect information through light signals and convert it to electrical pulses, which are then detected by visual neurons and analyzed and memorized by the visual cortex in the brain. Several kinds of artificial visual systems have been proposed that try to emulate this behavior.[163,164] Usually, in the conventional image processing based on deep learning -based computer visions, an array of photodetectors and image sensors are employed, to act as the retina, that gathers light information and converts it to electric signals, transferred to software-based ANN for further processing and storage.[165–168] To improve computer visions, novel algorithms are required to be investigated, especially in the context of human vision-inspired models and SNN approach to synthesize the most realistic image. Furthermore, better sensor performance for long distance and low-light resolution is another research priority in this regard.

OEMs can directly respond to light stimulus and perform light induced synaptic functions, which can simplify the peripheral circuit while offering a more energy and area efficient alternative.[169,170] Two layers ANNs can easily be realized using crossbars of OEMs, composed of input and output layers, and has already been simulated several times with high pattern recognition accuracies,[102,116,160,171] proving the outstanding potential of this approach. However, using photocurrent and light intensity as synaptic weigh modulator in a more complex ANN, with several hidden layers, is a hard to surpass challenge.[66] The light irradiation that inputs on the first layer of the neural network cannot be cascaded into the following layers, unless the already reported strategy on LEM is in place. In such, the first layer OEMs emit light to the second layer, as illustrated in **Figure 7.10(a)**.[146] Even then, VMM operations would be extremely hard to be accomplished with high accuracy, since photonic I_{LRS}/I_{HRS} ratio is usually low (<10). More studies are demanded to increase the memory window.

A combination of OEMs with ANNs electric-field assisted memristors crossbar looks closer to the reality of today’s technology development and can be considered as an effective way to construct an artificial visual system, as illustrated in **Figure 7.10(b)**. An OE memristive crossbar can be used for a primary in-situ processing and image sensing, acting as a neuron that then transfers this information to an electronic-based memristive crossbar, where the processing and storage of this data would take place. In this way, high accuracy recognition tasks can be performed, and the overall performance of artificial visual systems would be greatly enhanced.[66,78] Moreover, using PPC decay on the photonic crossbar can be an efficient way to, on one hand, store the input image for some time (sufficient for inference), and, on the other hand, low power due to auto-resetting of the system following relaxation time. Synaptic functions could also be applied and the whole system could undergo learning processes, in which the more times an image is inputted, the harder it gets for the photonic crossbar to “forget it”.

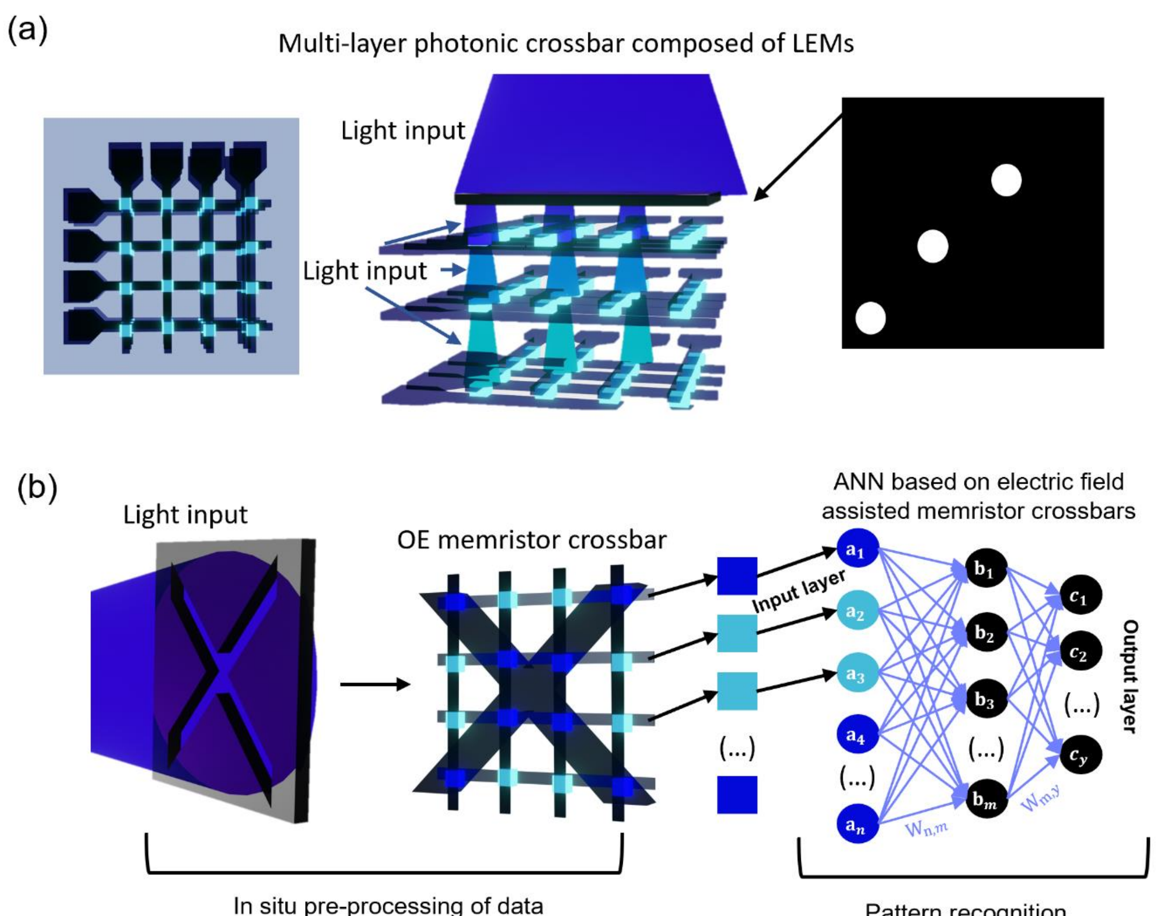

Figure 7. 10 Proposed strategies for the realization of energy efficient artificial visual systems. (a) Illustration of multi-layer photonic crossbar composed of LEMs. (b) Illustration of a photonic crossbar for in-situ pre-processing and an ANNs that can be composed of memristors for image recognition.

7.4 Conclusions

In this Review, the state of the art in inorganic OEMs is described and analyzed. Since the development of these devices should be carried out with a specific application in mind, due to different performance requirements, both memristor materials and structures with its figures of merit and different applications are covered.

On the materials point of view, metal oxides and 2D-materials based OEMs mostly show abrupt RS, suitable for in-memory computation in logic gates or DNNs. IR irradiation has been used to induce Reset, which is very appealing for wireless systems, to enable conversion and storage of IR data. Semiconducting-oxides and 1D-structured materials employed as active layer enabled the realization of fully-photonic devices, in which both Set and Reset were induced by different light wavelengths.

However, in the future, it would be important that further studies on the physical mechanism of light-induced RS, and how to control it, be developed.

In regard to possible applications, the PPC effect induced by light can be used to realize all sort of neuromorphic computing requirements. The logic gates already accomplished using inorganic OEMs are discussed in detail. Moreover, in some cases, the PPC decay was shown to be dependent on irradiation time, intensity, frequency and wavelength which was explored to emulate several synaptic functions, also described in this review. In particular, these synaptic functions can be applied for the construction of a more energy, cost and area efficient artificial visual system. Several approaches have been proposed and are analyzed here. Since the photonic ratio has demonstrated to be low (<10) and due to a lack of an efficient way to optical transfer photo-inputs from one to another layer in an ANN, a combination of photonic and electric crossbars is suggested to efficiently solve these issues.

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CHAPTER 8

OPTOELECTRONIC IGZO-BASED MEMRISTOR

Optoelectronic memristors (OEMs) based on amorphous oxide semiconductors (AOS) are promising devices for the development of spiking neural networks (SNNs) hardware in neuromorphic vision sensors. In such devices, the conductance state can be controlled by both optical and electrical stimuli while the typical persistent photoconductivity (PPC) of AOS materials can be used to emulate synaptic functions. However, due to the large bandgap of these materials, sensitivity to visible light (red/green/blue) is hard to accomplish which hinders applications in which color discrimination is required. In this work, we report on a 4 μm^2 hydrogen doped (H-doped) IGZO optoelectronic memristor that emulates all the important rules of SNNs such as short to long-term memory transition (STM-LTM), paired-pulse facilitation (PPF), spike-time-dependent plasticity (STDP) and learning and forgetting capabilities. By incorporating hydrogen gas in the sputtering deposition of IGZO, visible sensitivity was achieved for green and blue wavelengths. Additionally, extremely high light/dark ratios of 179, 93 and 12 are demonstrated for wavelengths of 365, 405 and 505 nm, respectively, due to hydrogen induced sub-gap states and device miniaturization. Therefore, the proposed device shows remarkable potential for integration with the pixel circuits of IGZO-based displays with extreme resolution, for a true intelligent self-processing display.

The results presented in this chapter are published in:

M.E. Pereira, J. Deuermeier, R. Martins, P. Barquinha and A. Kiazadeh, "**Unlocking Neuromorphic Vision: Advancements in IGZO-based Optoelectronic Memristors with Visible Range Sensitivity**", in ACS applied electronic materials, 2024.

8.1 Introduction

In common image processing systems based on deep-learning, two-dimensional arrays of photodetectors and image sensors that use semiconductor technology are employed to collect light information as digital inputs. This information is then converted into electric data and saved in a separated memory unit. A processing computing unit with software-based artificial neural networks (ANNs) is required to execute computer vision algorithms, such as object classification.[1,2] Apart from the obvious delay in response time, due to the necessary data shuffle between the sensors and the processing unit, as well as the high-power consumption required to run these complex neural networks, conventional image processing systems face a significant limitation that further aggravates the previously mentioned challenges. The light sensors capture visual information based on a fixed frame rate, with each recorded frame retaining data from all pixels within the array. On the one hand, low frame rate may lead to the loss of crucial information, on the other hand, a high frame rate results in the generation of excessive and unnecessary data. In either case, redundant data is shuffled, stored, and processed, coming from the recorded pixels in which no new information was created.[3,4]

An ideal artificial visual system should be able to read, recognize and perform parallel processing of electrical and optical signals, just as the human brain does. In fact, about 80 % of the data collected from the human brain is acquired through light signals by visual perception.[5] In more detail, our eyes can sense light information and convert it to electrical data, which is subsequently processed and saved in the visual cortex of the brain. Here, the connection between two neurons is referred to as synapse, involving the transmission of chemical or electrical spikes. The connection between two neurons can become stronger or weaker, which is known as synaptic plasticity and is closely tied to the memory capacity of the human brain. Naturally, short-term memory (STM) denotes a temporary change in synaptic connection that rapidly decays to its original state once the spike has ended. On the contrary, long-term memory (LTM) is the long lasting, and sometimes permanent, transformation of the synaptic weight.[6,7]

Neuromorphic vision sensors possess the ability to directly detect rapid changes, similarly to the human eye. In such, the sensor captures movement as a continuous flow of data rather than a frame-by-frame approach. By allowing each pixel to independently record when triggered, only relevant information is sent to the post-processing stages.[8–11] This novel approach not only produces far less data than the conventional one, resulting in increased energy efficiency, but also significantly decreases the response time of the system. Emerging optoelectronic memories, using both light and electrical signals as inputs, can behave as sensory artificial synapses with high energy-efficiency, low crosstalk and fast data processing and are, thus, suitable for spiking neural networks (SNNs) hardware applications in neuromorphic vision sensors.[12,13]

Amorphous oxide semiconductors (AOS) are a specially interesting class of materials to be employed as photosensitive layer in such devices.[14] Firstly, AOS have high flexibility and low-processing temperatures, allowing the use of flexible substrates, which is crucial for Internet-of-things (IoT) applications.[15,16] Additionally, using AOS in optoelectronic memories allows to benefit from the mature AOS pixel-driver circuit technology employed in commercial flat panel displays. This holds great promise for a straight-forward integration of AOS optoelectronic memories into neuromorphic system on panel (SoP) technology.

As such, the research community has dwelled into understanding how to develop an AOS-based synaptic device for neuromorphic vision. The persistent photoconductivity (PPC) and associated relaxation process in oxide semiconductors can be used as a basis to emulate synaptic functions.[17–19] The precise mechanism for the photogeneration and recombination of charges in oxide semiconductors has not yet been conclusively proven. However, the prevailing theory states that, under light stimulation, neutral oxygen vacancies (VOs) are ionized and become positively charged (VO^{+} or VO^{2+}). Following light interruption, a slow deionization process takes place in which electrons slowly move back to VOs.[9,18,20,21] The activation energy for neutralization of the ionized VOs strongly influences the decay of photocurrent, following light irradiation. Notably, this activation energy has been observed to be particularly elevated in Indium-Gallium-Zinc oxide (IGZO), in the range of 0.7 eV.[22] Moreover, IGZO-based memristors can be seamlessly integrated with the pixel circuits of IGZO-based displays for ultra-high-resolution SoPs, for a new era of neuromorphic displays systems. These displays would not only emit light to create images but would also possess the ability to sense and process visual information in real-time. By detecting the intensity of incident light, and discriminate between different colors, dynamically adjusting its resistance, the IGZO optoelectronic memristor emulates synaptic plasticity, enabling the pixel to adapt its response to different lighting conditions and visual stimuli.

Nevertheless, IGZO has a bandgap of 3.05 eV, which means it is mostly sensitive to UV light.[23–25] The effective tunability of its sensitivity to the visible range is of the most importance for applications in which color discrimination is necessary. Therefore, strategies such as adding an absorbing layer composed of organic materials,[26] 2D materials,[27] quantum dots[28] or the engineering of a defective IGZO absorbing layer[29] have been successful in 3-terminal phototransistors used as synaptic devices. However, this heterostructure approach has its own drawbacks such as high device to device (D2D) variability due to increased process complexity, high off-currents (dark current) which then decrease the total photocurrent and worse overall transistor performance. Hydrogen-doping (H-doping) has also been suggested for visible range detection either in a double-layer structure30 or by spontaneous doping within one of the device`s interfaces.[31] The hydrogen atoms incorporated in the IGZO serve as electron donors, that increase the concentration of free electrons,[32–34] and create subgap states in the IGZO layer with different energy levels that can be stimulated by visible light.[30,31]

Although 3-terminal optoelectronic synaptic devices can effectively sense and process optical image information in nearly real-time, demonstrating considerable potential for ultrafast machine

vision applications, they also show large-scale integration restrictions due to increased pixel area. Such neuromorphic visual devices with a planar structure are unsuited for applications such as self-driving cars and robots where the capture of stereo dynamic images with a wide-field of view with high resolution is imperative.[3] In such, optoelectronic memristors (OEMs), with a two-terminal configuration, can meet the criterion due to their smaller cell size, simpler device structure and fabrication process and lower energy requirements.

While several studies on electrically controlled IGZO memristors have been reported showcasing its great potential for both analog and digital resistive switching (RS) behaviors,[35–38] the advantages of the optoelectronic memristor have not yet been fully investigated. A complete review on the available literature demonstrates that low photocurrent is one of the biggest limitations currently hampering further development of optoelectronic memristors in general.[13] On IGZO-based optoelectronic memristors, only few articles have been published to date. An UV-sensitive device was reported, using solution-processed IGZO, in which some of the synaptic functions could be realized, such as spike-time-dependent-plasticity (STDP) and STM-LTM transition.[39] Hu *et al.* proposed an interesting device based on an IGZO double layer in which a resistance decrease (Set) could be induced by blue light irradiation (420 nm) and a resistance increase (Reset) by red light (800 nm).[40] More recently, in 2024, an heterostructure based on IGZO/tungsten oxide (WO_{3-x}) was demonstrated with sensitivity up to the 420 nm wavelength for image segmentation and object tracking.[41] Although these studies demonstrate tremendous potential of IGZO optoelectronic memristors, they all report low I_{light}/I_{dark} ratios (below 10) for all demonstrated wavelengths even after a few seconds of light irradiation, and none have explored the patterning of miniaturized devices, which should be critically considered. According to the review manuscript on the recommended methodology of RRAM studies published in 2019,[42] it is evident that with a large device area, distinct RS properties and related physical mechanisms can emerge, potentially differing from those observed in miniaturized, patterned devices. Patterning is also fundamental for large-scale implementation of optoelectronic memristors, which to our knowledge has not been reported.

Here, we report a 4 μm^2 optoelectronic memristor based on a H-doped IGZO layer, with visible range sensitivity with wavelength of up to 505 nm. Extremely high I_{light}/I_{dark} ratios of 179, 93 and 12 are achieved for wavelengths of 365, 405 and 505 nm, respectively. This is explained by both the H-doping and by the use of a thin Ti/Au layer as top electrode which, despite its lower than 65% transmittance, increases the VOs concentration in the IGZO layer, increasing photosensitivity. We also provide a comparative study on devices with different patterned areas, demonstrating the impact of device area on the I_{light}/I_{dark} ratio and on the sensitivity to less energetic wavelengths, proving miniaturization is a priority in this field. All significant synaptic functions are demonstrated such as STM to LTM transition, paired-pulse facilitation (PPF), STDP, and learning and forgetting capabilities, unravelling the device's potential for integration with the IGZO-based display mature technology for neuromorphic vision sensors. The combination of light sensing and synaptic functionality at the pixel level opens up a myriad

of possibilities for applications such as adaptive brightness control, dynamic scene enhancement, and even image processing tasks. Moreover, by reducing system complexity and energy consumption, these neuromorphic display systems pave the way for immersive and adaptive display technologies that enhance user experience across various domains, including augmented reality, smart signage, and human-machine interfaces.

8.2 Experimental

The devices were fabricated on Corning Eagle glass, previously cleaned in repeated ultrasonic baths of acetone and isopropanol and rinsed with deionized water and dry nitrogen.

For the bottom electrode of the OEMs, radio-frequency (RF) magnetron sputtering was used to deposit a 70 nm thick Mo layer in an AJA ATC-1800 system with a flow rate of 50 sccm of Ar, a sputtering power of 175 W (3" target) and a deposition pressure of 1.7 mTorr. Then reactive ion etching in a Trion Phantom 3 system was used with SF_6 to pattern this layer.

Then, an oxygen plasma treatment was carried out on the bottom electrodes inside the sputtering chamber prior to IGZO deposition. The parameters used were a flow rate of 20 sccm of oxygen gas with 10 W of substrate bias and an RF power to the Ga_2O_3 target of 40 W to create the plasma for 10 min in a 20 mTorr pressure. 110 nm of IGZO were deposited by RF magnetron co-sputtering from three ceramic oxide targets. The sputtering powers used on each target (all 2" diameter) were In_2O_3: 121 W, Ga_2O_3: 100 W, and ZnO: 50 W using a flow rate of 20 sccm of Ar and 5 of O_2 for the standard IGZO film and 14 sccms of Ar, 3 sccms of O_2 and 0.3 sccms of H_2 for the hydrogen-doped IGZO film. The deposition pressure was kept constant at 2.3 mTorr. The In:Ga:Zn atomic composition of the deposited films was 2.2:1.0:1.1, for a normalized Ga concentration. The IGZO compositions were estimated by X-Ray Photoelectron Spectroscopy (XPS) results through the area report on the Ga 3s, Zn 3s and In 4s spectra.

A lift-off procedure was employed to pattern the IGZO and the top electrodes. A thin 1 nm layer of Ti was deposited immediately followed by the evaporation of 6 nm of Au by e-beam evaporation in a homemade apparatus, without breaking vacuum. For the devices with ITO as top electrode, a 65 nm thick ITO layer was deposited in an AJA ATC-1800 system using a single target (2" diameter, 90:10 wt%) with a flow rate of 20 sccm of Ar and 0.25 sccm of O_2, a sputtering power of 95 W and a deposition pressure of 1.2 mTorr. All the depositions were carried out with no intentional heating and no annealing steps were performed.

A UV–VIS-NIR spectrophotometer, Perkin Elmer Lambda 950, was used to acquire the transmittance of the various transparent films, between 1000 and 299.5 nm with 1.5 nm steps. The sheet resistances of the films were measured by the four-point probe method.

The electrical characterization of the optoelectronic memristors was conducted at a Keithley 4200 SCS semiconductor analyzer connected to a Janis ST-500 probe station. The DC sweeps and

transient responses were acquired by applying a read voltage (V_{Read}) to the bottom electrode while maintaining the top electrode connected to ground. Fiber-coupled light-emitting diodes (LEDs) of 660, 505, 405 and 365 nm wavelengths from Thorlabs were then placed on top of each measuring device by an optical arm, part of the Janis probe station. These LEDs were connected to a LED driver from Thorlabs that allows the accurate application of pulses from 1 Hz on.

The XPS measurements were performed with a Kratos Axis Supra, using a monochromatic Al Kα source running at 150 W. The analyzer was set to a pass energy of 10 eV for detail scans and 80 eV for surveys. CasaXPS Version 2.3.25PR1.0 was used for data analysis. The Fermi level was calibrated using a sputter-cleaned gold sample. AFM topographs were acquired with an Asylum Research MFP-3D Standalone system (Oxford Instruments, UK) operated in tapping mode at ambient room conditions. Commercially available silicon probes were used (Olympus AC160TS, Olympus Corporation, Japan; f_0 = 300 kHz, k = 29 N/m) and the resulting topographs were exported using Asylum Research's software packages after low-level flattening.

8.3 Results and discussion

8.3.1 Influence of top contact on optoelectronic properties

The undoped OEM structure can be found in **Figure 8.1(a)**. Mo was used as bottom contact, as it is often employed in TFTs and would facilitate the targeted pixel integration.[16,43] An oxygen plasma treatment was carried out on the Mo bottom contact, to create a thin MoO_x layer, following our previous work.[35] This oxide layer creates a barrier for electron injection and is usually the reason for the rectification found in the pristine devices. The photosensitive IGZO layer was then used as active material, deposited by sputtering in an Ar/O_2 atmosphere.[44] Two different transparent top electrodes were investigated with the intent of comparing electrical and optical device performance: indium-tin oxide (ITO) and thin titanium/gold (Ti/Au). ITO was deposited by sputtering with a 65 nm thickness and presented a sheet resistance of 124 Ω/sq. Ti/Au was deposited by e-beam with 1 nm of Ti and 6 nm of Au. The atomic force microscope (AFM) image of the Ti/Au film is shown in **Figure E.1 - Appendix E** with a very low root mean square (RMS) roughness of 402.2 pm. The absence of island formation confirms the morphological integrity of the top electrode. The devices were patterned via conventional photolithography into 4 μm^2 devices. More details on the fabrication procedure can be found in the Experimental section. In **Figure 8.1(b)**, the current-voltage (I-V) characteristics, between -0.5 V and 0.5 V, of the pristine of both devices is presented. Voltage is applied to the bottom Mo contact while keeping the top electrode (ITO or Ti/Au) grounded. A rectification ratio of more than 2 orders of magnitude is presented for the ITO configuration, with higher conductivity for positive polarities while the

Ti/Au device presents a slight rectification in the opposite direction (higher conductivity for negative polarities).

In order to investigate the reason for the different rectifications, XPS measurements were conducted on the bulk IGZO film and the IGZO/ITO and Ti/Au interfaces. To ensure XPS detection of the IGZO cations at the interfaces, thin 1/3 nm Ti/Au and 4 nm of ITO were deposited on top of thick IGZO films on Si substrates. In **Figures 8.1(c)** and **8.1(d)**, the O 1s spectra is shown for the bulk IGZO film and the IGZO/Ti/Au interface. The peaks were fitted with a Gaussian-Lorentzian (G-L) function and a Shirley background subtraction. The O 1s spectra is deconvoluted into two peaks with binding energies of 530.1 eV and 531.8 eV, which are assigned to metal-oxygen bonds (M-O) and to oxygen from oxygen-poor regions, respectively. The oxygen deficiency increases drastically at the interface of IGZO/Ti/Au. In fact, the Ti oxygen getter effect has been reported several times.[52,53] In this case, Ti reacts with the IGZO layer by removing oxygen ions increasing VOs concentration at the interface. The titanium oxidation is confirmed by the Ti $2p_{3/2}$ binding energy at 458.8 eV (**Figure E.2 - Appendix E**). Note that the change to the O 1s emission cannot be related with the TiO_x formation, because its lattice oxygen peak is at the same binding energy as of IGZO.[47] Unfortunately, the same analysis cannot be conducted at the IGZO/ITO interface because ITO itself contains a large fraction of oxygen. The Zn LMM Auger emission further reveals that the zinc in IGZO is reduced to a metallic state. The modified Auger parameter can be employed to determine the chemical state.[48] The parameter was calculated by adding the binding energy of the Zn $2p_{3/2}$ peak and the kinetic energy (E_k) of Zn L3M45M45 Auger peak (**Table 8.1**). There is a clear reduction of Zn at the interface with Ti/Au, due to the oxygen deficiency on IGZO found at the interface and the well-known Ti oxygen getter effect. For the IGZO/ITO interface, the Zn LMM Auger peak cannot be measured due to overlap with the Sn 3d emission.

Table 8. 1 Modified Auger parameter of the bulk IGZO and the IGZO/Ti/Au interface.

	E_b Zn 2p 3/2 (eV)	E_k Zn LMM (eV)	M-Auger parameter	Dominant species
IGZO	1021.85	988.2	2010.05	Zn (II) oxide
IGZO/Ti/Au	1021.55	991.2	2012.75	Zn (0)

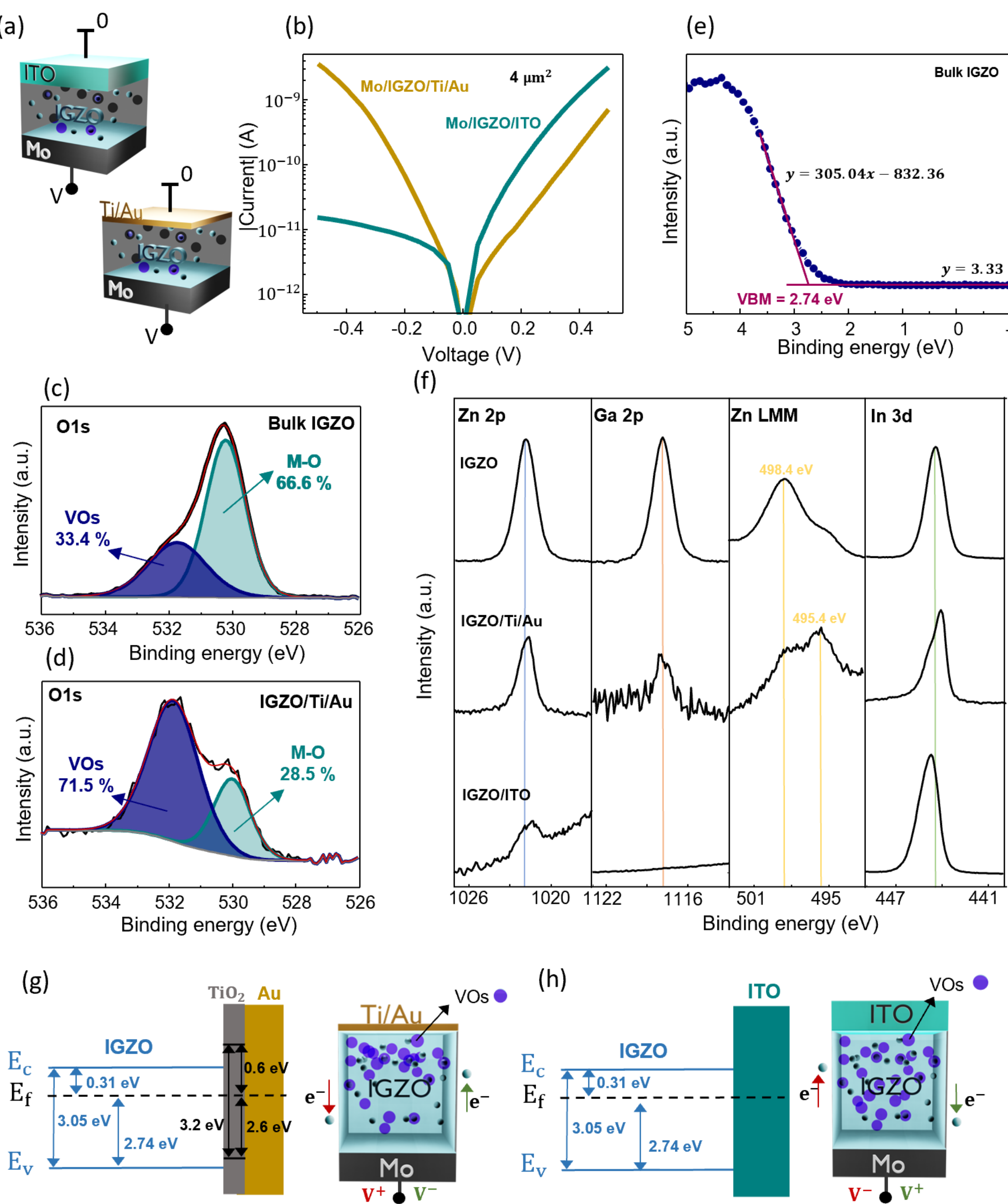

Figure 8. 1 Analysis of I-V characteristic in the dark. (a) Schematic illustration of the proposed IGZO devices, with Mo as bottom contact and Ti/Au or ITO as top contact. (b) I-V characteristic of the pristine of both devices from -0.5 V to 0.5 V with voltage sweep applied to bottom contact and ground at top contact, displaying different rectification for different top contacts. (c) and (d) Fitting of O 1s XPS spectra displaying the oxygen vacancies (VOs) percentage compared to the metal-oxygen (M-O) bonds for the IGZO bulk film and the IGZO/Ti/Au interface, respectively. (e) Valence band spectra of the bulk IGZO film, used to calculate the valence band maxima (VBM). (f) Core levels spectra of Zn 2p, Ga 2p, Zn LMM and In 3d of the IGZO

and the Ti/Au and ITO interfaces displaying the offsets. (g) and (h) Schematic illustrations of the energy band diagram for the IGZO/Ti/Au and the IGZO/ITO interfaces, respectively.

The energy band alignment of the interfaces was also investigated by XPS. **Figure 8.1(e)** shows the valence band spectrum of the bulk IGZO film, used to calculate the valence band maxima (VBM) of 2.74 eV determined by linear extrapolation of the leading edge of the spectrum. Since IGZO presents an optical bandgap of 3.05 eV,[49] the difference between the E_f and conduction band minimum (E_c) can be calculated to 0.31 eV. The energy band alignment at the interfaces is then derived from the offsets of the core levels spectra.[50,51] The Zn 2p, Ga 2p, Zn LMM and In 3d spectra of the IGZO bulk film and both studied interfaces (IGZO/Ti/Au and IGZO/ITO) are presented in **Figure 8.1(f)**. The core level Ga 2p emission at the interface has too low intensity to be analyzed with confidence. The core level In 3d has to be discarded for the IGZO/ITO interface because it is present in ITO. In the IGZO/Ti/Au interface, the In 3d spectra shows a 0.3 eV shift to lower binding energies and it has become asymmetric which shows high conductivity. By considering the core level Zn 2p at both interfaces, 0.3 eV shifts to lower binding energies were identified. For such low shifts, it is concluded that potentially a slight differential charging was present at the plain IGZO surface. This means that the band alignment of both interfaces shows flat bands in the IGZO.

Based on these results, the schematic illustration of the energy band diagrams of the IGZO/Ti/Au and IGZO/ITO interface are presented in **Figures 8.1(g)** and **8.1(h)**. For the TiO_2, optical band gap and VBM values were extracted from elsewhere.[52] In the current work, the reference electrode functions as the bottom contact for voltage application. Previously, we reported the presence of a rectifying barrier at the bottom interface of MoO_x/IGZO.[35] In the ITO device, an ohmic junction is also present at the top interface IGZO/ITO, and therefore the rectification comes from the bottom interface, demonstrating consistent properties with our prior findings. However, in devices with a thin Ti/Au top electrode, the 1 nm of Ti, which absorbs oxygen from the IGZO, becomes fully oxidized. This creates a TiO_2/Au junction, which can therefore present a barrier to electron injection from Au.[53] In this case, the slight rectification observed in this device can be explained by the second barrier arising from the Au/TiO_2 interface.

In **Figure 8.2(a)**, a photograph is provided in which the transparency of the IGZO, Ti/Au and ITO can be separately evaluated. In **Figure 8.2(b)**, optical measurements reveal that IGZO and ITO have similar transmittance values, while Ti/Au transmittance does not surpass 65 % for wavelengths ranging from 300 and 1000 nm. For the evaluation of the device response to light, LEDs with wavelengths of 660, 505 nm, 405 and 365 nm were chosen for irradiation and placed on top of the devices, as presented in photographs of **Figure 8.2(c)**. In **Figure 8.2(d)** is depicted a micrograph of a 4 μm^2 device with ITO as top contact. The optical response of the memristor can be evaluated in **Figure 8.2(e)**, where the I-V characteristic is presented in the dark and under irradiation. Before any optical measurement, the devices underwent electrical Resets, which are clarified in section 8.2.3 of this chapter, to eliminate

any photoexcitation from ambient or microscope light. As explained before, under light stimulation, it is expected that neutral VOs on the IGZO are ionized and become positively charged (VO^+ or VO^{2+}). With a bandgap of 3.05 eV, IGZO is expected to respond to UV light (3.1 eV) mostly,[49] and even if the focus of this work is on visible light sensitivity, the UV performance is always shown throughout the paper for proper comparison with the state of the art. Accordingly, there seems to be no response to 660 nm red light as the I-V characteristic falls precisely on top of the measurement performed in the dark. The highest ratio between measured current in the dark (I_{dark}) and in light irradiation (I_{light}) can be distinguished at -0.5 V for all other wavelengths and this is, therefore, the read voltage (V_{Read}) applied for the transient test presented in **Figure 8.2(f)**. Here, the current state is recorded for 10 s of constant light irradiation, followed by 30 s in the dark. The lack of response to red light is confirmed and for the other wavelengths, I_{light}/I_{dark} ratios of 15, 10 and 2.3 are achieved for 365, 405 and 505 nm irradiation, respectively. Photocurrent saturation is reached for all three wavelengths within 1 s of illumination which means the device is extremely fast. The PPC effect seems to have a fast decay, which is due to the high negative voltage applied. This voltage provides enough energy to accelerate the movement of electrons into the VOs, increasing the rate of neutralization of photoexcited defects. It can be inferred then that, even if -0.5 V as V_{Read} provides higher I_{light}/I_{dark} ratio, it also hinders the PPC effect and slowly decreases the photocurrent with increasing illumination time. **Figure E.3 - Appendix E** displays the same test with a V_{Read} of 0.1 V that shows the current state slightly increasing during irradiation. PPC decay is still quite fast, but this could be related to the low I_{light}/I_{dark} ratio.

Similarly, the analysis for the device with Ti/Au as top contact is presented in **Figure 8.2(g)**, **8.2(h)** and **8.2(i)**. The green response is very faint since the Ti/Au has a transmittance of 61.5% at 505 nm. However, despite the even lower Ti/Au transmittance of 40.5% (at 365 nm-UV) and 42.9 % (at 405 nm – blue), the I_{light}/I_{dark} ratios achieved with this device are 46 and 14, respectively. This indicates that the benefits from using Ti/Au as top electrode outweigh the losses derived from its lower transparency. A positive 0.1 V is applied as V_{Read} and after 10 s of illumination the photocurrent is still increasing, which means that it has not reached saturation. Comparing with the results of the device with ITO as top contact, it can be concluded that the Ti/Au device has lower switching speed. This is easily explained by the lower transmittance of Ti/Au which in turn results in a lower energy reaching the photosensitive layer IGZO. However, PPC effect can be seen clearly with two different current levels retained after blue or UV irradiation.

It is important to note that the polarity of the V_{Read} should be chosen for the lowest I_{dark} to provide the highest I_{light}/I_{dark} ratios. For the ITO device, this means a negative V_{Read} and for the Ti/Au this means a positive V_{Read}. The I_{dark} of the Ti/Au device is lower than the I_{dark} of the ITO device. However, the I_{light} is comparable in both devices, despite the lower Ti/Au transmittance, because of the higher VOs content at its top interface, which explains the superior performance of the Ti/Au devices.

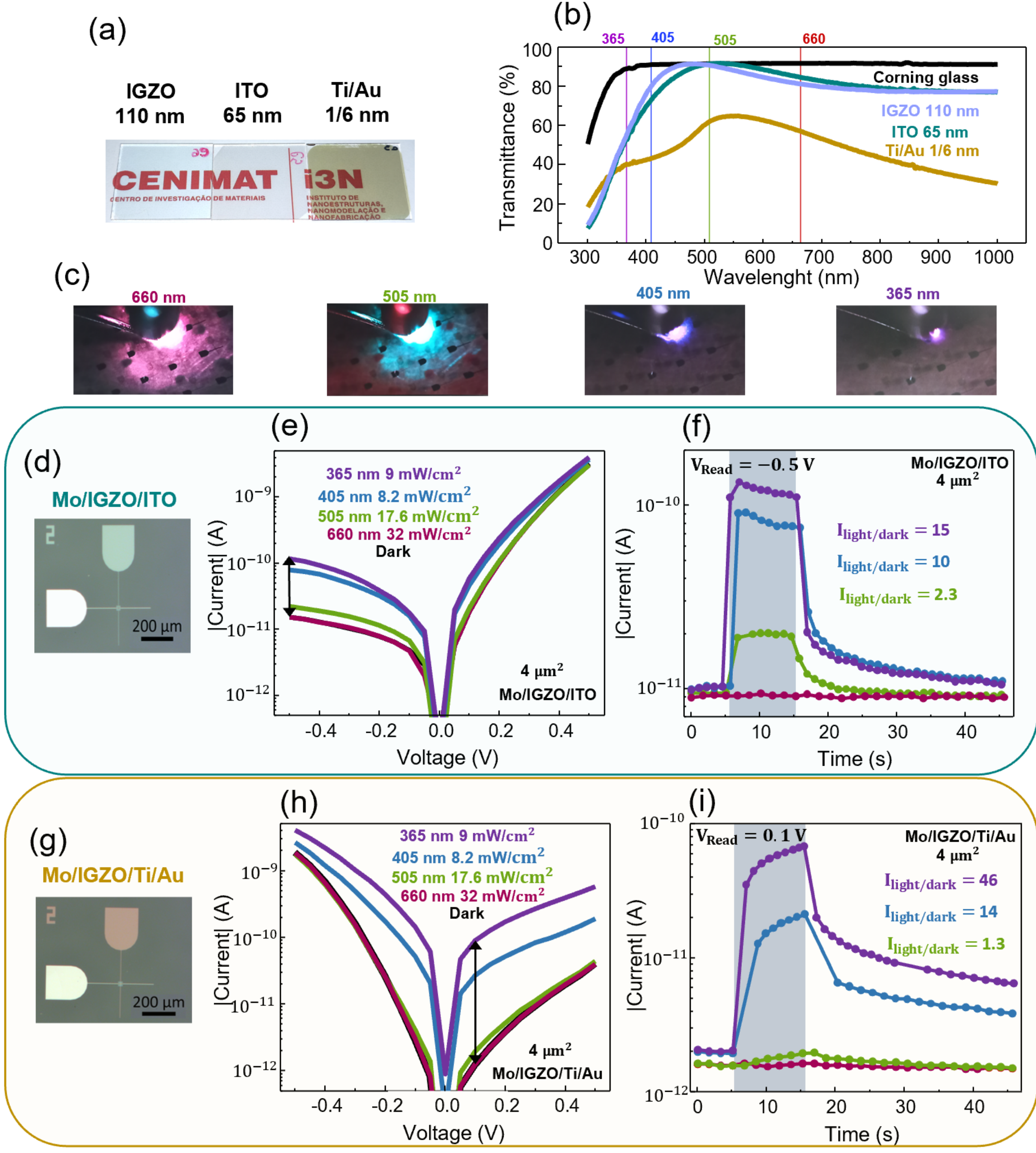

Figure 8. 2 Optoelectronic properties of the IGZO-based memristor. (a) and (b) Photograph and transmittance results on IGZO, Ti/Au and ITO films deposited on glass. (c) Photographs of a device being irradiated by the chosen light wavelengths. (d) Micrographs of the 4 µm² ITO device with no intentional light input. (e) I-V characteristic and (f) transient response with V_{Read} of -0.5 V of 10 s of irradiation followed by 30 s in the dark of the ITO device with wavelengths of 660, 505, 405 and 365 nm. (g) Micrograph of the 4 µm² Ti/Au device. (h) I-V characteristic and (i) transient response with V_{Read} of 0.1 V of 10 s of irradiation followed by 30 s in the dark of the Ti/Au device with wavelengths of 660, 505, 405 and 365 nm.

8.3.2 Optimization for visible light detection by hydrogen-doping

To improve visible range sensitivity, H-doping was performed on the IGZO film with both ITO and Ti/Au as top contacts, as schematically illustrated in **Figure 8.3(a)**. In more detail, IGZO deposition was carried out in an $Ar/O_2/H_2$ atmosphere with 2 % of hydrogen gas. As can be seen in **Figure 8.3(b)**, the transmittance of the doped-IGZO film is decreased in the green wavelength, indicating that the film absorbs more of the incident radiation than the undoped-IGZO. In fact, even macroscopically, the doped film presents a greenish tone while the undoped-IGZO shows more of a blueish tonality. The atomic composition of the IGZO was calculated to be 2.2:1:1.1, through XPS measurements of the cations s orbitals (Ga 3s, Zn 3s and In 4s), for both the doped and undoped film. The VOs percentage was also not modified, as can be seen in **Figure E.4(a) - Appendix E**. However, the VBM was found to be 0.08 eV closer to the Fermi level in the IGZO:H films, compared to undoped samples as can be seen in **Figure E.5 - Appendix E**. With a constant band gap, this means that the doped films have 22 times lower carrier concentration than the undoped films (Boltzmann approximation). In **Figure 8.3(c)**, the I-V characteristic of the pristine for the doped and undoped-IGZO devices, with Ti/Au as top contact, is compared. It is clear that by H-doping, the device has become less conductive overall. This can be explained by the lower carrier concentration in the doped film which increased the series resistance of the IGZO:H layer.[54]

Similarly to the undoped IGZO device, the VOs percentage increases at the interface with Ti/Au, as can be confirmed in **Figure E.4(b) - Appendix E**. It is known that H atoms can passivate VOs and create stable states in which H atoms become trapped at VOs (VO/2H). The resulting VO/2H is referred to as shallow-level donor.[55] Moreover, in AOS, H atoms can also bond with oxygen, forming O-H bonds and creating free electrons. Both these processes increase sub-gap states, leading to improved optical absorption.[30,31] By passivating the defect states, hydrogen doping can also improve the mobility of the charge carriers. This allows for faster and more efficient transport of photogenerated carriers, leading to a higher photocurrent and quicker response times.[56,57] This is confirmed by the significantly increased photocurrents of the doped-memristor, presented in **Figures 8.3(d)**, **8.3(e)** and **8.3(f)**. In fact, for 10 s illumination, the I_{light}/I_{dark} ratio increases from 1.3 to 12, from 14 to 93 and from 46 to 179 for wavelengths of 505, 405 and 365 nm, respectively. The photoresponsivity speed is also improved by H doping as saturation of the photocurrent is achieved much faster. Moreover, doping does not seem to fasten the PPC decay, which means the device presents outstanding performance for SNNs applications, namely neuromorphic vision sensors.

For the H-doped device with ITO as top contact, the same results could not be replicated, as shown in **Figure E.6 - Appendix E**. In the doped device, the rectification ratio is significantly decreased and the conductance increases, with I_{dark} now more than one order of magnitude higher. I_{light} is also higher for all tested wavelengths, nonetheless, due to the I_{dark} increase, the I_{light}/I_{dark} ratio is not improved with H-doping. One possible explanation is the fact that ITO is also strongly affected by H-

doping. In fact, H-doping of ITO has been reported to enhance its conductivity.[58] It is possible that there is an exchange of H-atoms at the ITO/IGZO interface, increasing I_{dark}. Another possible explanation is that the H-doping of the IGZO film is decreasing the barrier at the bottom interface MoO_x/IGZO and, therefore, decreasing the rectification ratio. This explanation is in line with previously reported findings of decreased contact resistance between Mo and IGZO by hydrogen plasma treatments.[59]

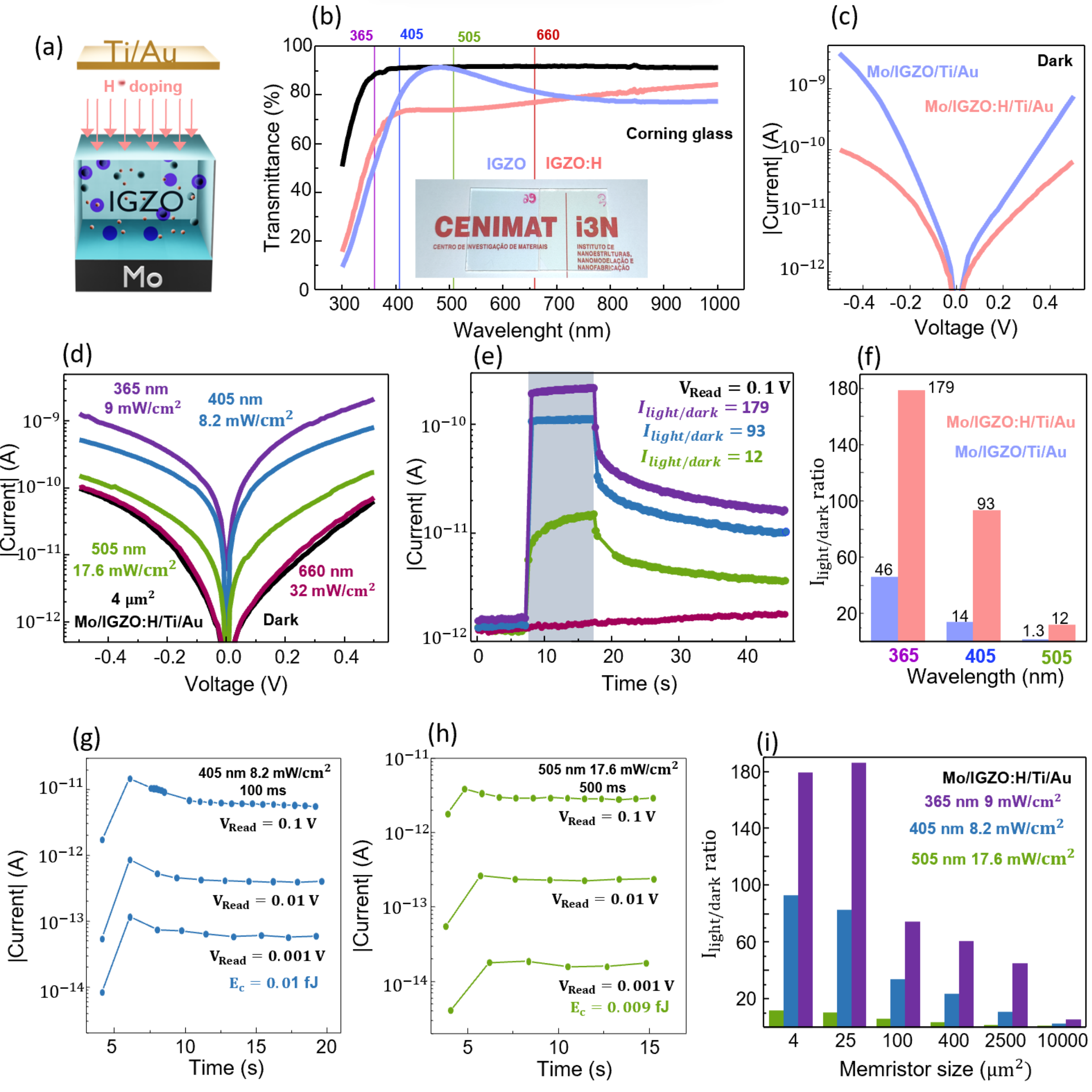

Figure 8. 3 Optoelectronic properties of the hydrogen-doped (H-doped) IGZO memristor. (a) Schematic illustration of a H-doped IGZO memristor device. (b) Photograph and transmittance results on IGZO and H-doped IGZO films deposited on glass. (c) Comparison of the I-V characteristic in the dark of the IGZO and the H-doped IGZO devices. (d) I-V characteristic and (e) transient response with V_{Read} of 0.1 V and 10 s of irradiation followed by 30 s in the dark of the H-doped device for 660, 505, 405 and 365 nm illumination. (f) I_{light}/I_{dark} ratio comparison of both mentioned devices. (g) Photocurrent response to 100 ms

pulse of blue light with V_{Read} of 0.1, 0.01 and 0.001 V. (h) Photocurrent response to 500 ms pulse of green light with V_{Read} of 0.1, 0.01 and 0.001 V and (i) I_{light}/I_{dark} ratio comparison of devices with different sizes.

The switching speed of the optimized device was analyzed and can be found in **Figures 8.3(g)** and **8.3(h)** for different V_{Read} for 100 ms of blue light irradiation and for 500 ms of green light illumination, respectively. Following a previously reported strategy,[60] the energy consumption (E_c) per single pulse was calculated through **Equation 8.1**:

$$E_c = V_{Read} \times I_{Photo} \times t \qquad \mathbf{(8.1)}$$

Therefore, for V_{Read} of 0.001 V, E_c can be decreased to 0.01 fJ for blue and 0.009 fJ for green light, which is much lower compared to both biological synapses and to the state-of-the-art artificial photonic synapses for visible light detection, as summarized in **Table E.1 - Appendix E**. This shows the proposed doped device is extremely power efficient which is due to both the doping effect on the switching speed and the decreased patterned memristor area.

The I-V characteristic comparison in the dark can be consulted in **Figure E.7 - Appendix E**, together with the full analysis of miniaturization. In summary, by decreasing the memristor area, the I_{dark} and I_{light} are decreased and the I_{light}/I_{dark} ratio is greatly enhanced, as showcased in **Figure 8.3(i)**. As an example, by increasing the area of the device 100 times (400 μm^2), the I_{light}/I_{dark} ratio decreased from 179, 93 and 12 to 61, 24 and 3 for 10 s illumination with wavelengths of 505, 405 and 365 nm, respectively. This can be explained by the current density increase with downsizing, also observed for IGZO-based diodes,[61] indicating that the current flow is not uniform across the entire device area, and in fact it flows through local current conduction paths.[6]

8.3.3 Emulation of synaptic properties

Having developed a device (Mo/IGZO:H/Ti/Au) with such potential for neuromorphic vision sensors, other figures of merit were investigated in that regard. Firstly, the device should be fully controllable concerning Set - the increase of conductance by light - and Reset - the decrease of conductance by electrical pulse. In **Figure 8.4(a)**, different current states can be distinguished from irradiation with light of different wavelengths. The higher the current state reached by light, the higher the voltage (or the longer the electrical pulse duration) required to perform a Reset and bring the current back to the value in dark. The same test can be found in **Figure E.8 - Appendix E**, for the H-doped IGZO memristor with ITO as top contact. Apart from the decreased I_{light}/I_{dark} ratio, a similar behavior is observed. Low cycle-to-cycle (C2C) and device-to-device (D2D) variabilities are also a crucial requirement for any envisioned application. In **Figure E.9 - Appendix E**, 10 cycles of UV illumination, followed by 10 s in the

dark and a Reset pulse, are depicted with no considerable change in device performance. Moreover, 10 devices with an area of 4 μm^2 were measured in terms of their optical performance and I_{dark}. The results are displayed in **Figure E.10 - Appendix E** and show low variability. Moreover, this minimum variability can be ascribed to expected fabrication variability and the unavoidable randomness of the measurement in terms of LED positioning on top of the device. Since physical vapor deposition tools that ensure good uniformity on large areas are used for all layers on the proposed structure, batch to batch variability is also not expected to be significant.[63]

As formerly discussed, the PPC decay on AOS can be used to emulate synaptic functions of the human brain. As such, this decay should be accurately controlled to simulate the transition between STM and LTM, schematically illustrated in **Figure 8.4(b).** According to the memory model suggested by Atkinson and Shiffrin, most of the information we receive is saved by the brain only temporarily, which is called STM. Subsequently, if the input is repeated several times, STM can transition to LTM. This behavior can be simulated by the H-doped IGZO OEM by increasing power, illumination time or frequency of the light input. **Figures 8.4(c)**, **8.4(d)** and **8.4(e)** show the impact of these three parameters using blue radiation (405 nm). In **Figure 8.4(c)**, 6 different current states can be distinguished following 30 s of illumination and powers ranging from 0.1 to 8.2 mW/cm^2, **Figure 8.4(d)** shows the effects of illumination time on the photocurrent and **Figure 8.4(e)** presents the PPC with varying frequency, from 0.1 to 1 Hz. The same measurements were performed for UV (365 nm) and green (505 nm) radiation, as presented in **Figure E.11 - Appendix E**. In all trials, different conductance states can be achieved by the varying conditions.

It is believed that the ionization of VOs ($VO \rightarrow VO^{+} + 1e^{-}$ or $VO \rightarrow VO^{2+} + 2e^{-}$) is responsible for the photocurrent observed in AOS. Following light irradiation, a recombination reaction takes place in which free electrons neutralize VOs ($VO^{+} + 1e^{-} \rightarrow VO$ or $VO^{2+} + 2e^{-} \rightarrow VO$).[64] Therefore, the manipulation of the PPC decay in AOS requires control of this reaction rate, which is directly related to the energy barrier necessary for neutralization of ionized VOs. Therefore, while the ionization is a rapid process occurring due to the optical energy provided to the system, neutralization is a thermally activated process with activation energy, that will take place gradually.[65] IGZO is one of the AOS materials with higher activation energy, which explains the prolonged PPC characteristic observed here. Additionally, it has been reported that higher activation energies can be achieved with lower wavelengths. This is related to a shift in the Fermi level to values closer to the conduction band minimum as a result of increased free electron concentration.[22] A higher activation energy can, therefore, be achieved with not only lower wavelengths, but also with prolonged irradiation time or a more frequent input.

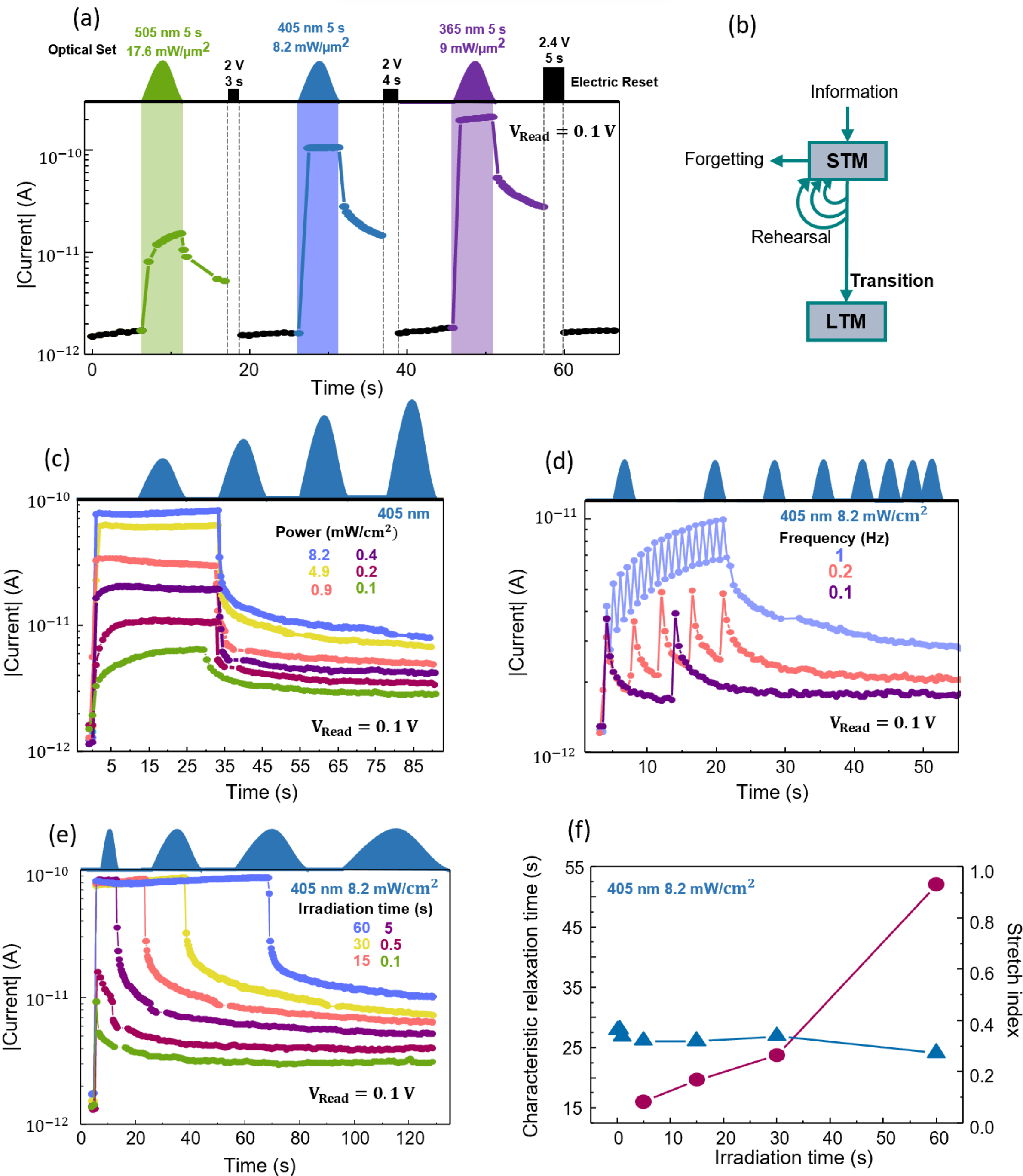

Figure 8. 4 Reset by electrical pulse and PPC dependence on power, time and frequency of optical input. (a) Increased conductance states achieved by decreased wavelengths illumination and respective electrical Reset pulse. (b) Schematic illustration on the transition from short-term memory (STM) to long-term memory (LTM). Different conductance states reached by (c) increased power, (d) increased frequency and (e) increased time of illumination with a 405 nm wavelength LED. (f) Characteristic relaxation time and stretch index for different irradiation times.

In this work, the PPC decay was fitted following the Kohlrausch stretched exponential function, as it has been previously shown to well describe the transition from STM to LTM,

$$\varphi(t) = I_0\, exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] \quad \mathbf{(8.2)}$$

in which, $\varphi(t)$ is the relaxation function, τ is the characteristic relaxation time, I_0 is the current state immediately after light illumination, and β is the stretch index ($0 < \beta < 1$). The increase in the characteristic relaxation time implies a lower forgetting rate, demonstrating the transition from STM to LTM.[66] It is important to note that the decay profile and characteristic relaxation time τ will be influenced by the initial carrier density, making it challenging to isolate the effects of recombination dynamics from the effects of initial carrier density. Therefore, here, the fittings were performed on the decay of different irradiation time, that had reached the same or very similar photocurrent (60 s, 30 s, 15 s and 5 s), to ensure the same initial photogenerated carrier density which enables the accurate comparison of the recombination rate. The fittings can be found in **Figure E.12 - Appendix E** for all tested wavelengths. In all cases, the relaxation time constant τ is increasing for longer irradiation time as can be inferred from **Figure 8.4(f)** for blue light irradiation and **Figure E.12 - Appendix E**, corresponding to a clear transition from STM to LTM, meaning we can effectively control the PPC behavior of the proposed device.

As illustrated in **Figure 8.5(a)**, eyes collect information through light. This information is then processed in the visual cortex of the human brain by neurons and their synapses, involving the transmission of chemical or electrical spikes. Synapses are connected by a pre-synaptic neuron and a post-synaptic neuron. The connection between the two can be enhanced or weakened, which is known as synaptic weight change, and is responsible for mechanisms such as learning and memorizing. An artificial synapse should follow the learning rules of the human brain to accurately simulate it.

In a biological synapse, PPF relates to the synaptic weight becoming stronger after the application of two spikes in the pre-synaptic neuron. In other words, the post-synaptic current (PSC) triggered by the second pulse will increase the PSC caused by the first pulse due to memory effect. The time interval between the two pulses (Δt) dictates the increase of PPF index. The higher the Δt, the lower the PPF index should be. In **Figure 8.5(b)**, the PSC evolution in the H-doped IGZO optoelectronic memristor, for V_{Read} of 0.1 V, can be seen during a PPF test for two optical pulses with 500 ms each and a Δt of 10 s. It is confirmed that the PSC is enhanced by the second spike. The PPF in the memristor is calculated by the following **Equation 8.3**:

$$PPF\ index = \frac{A_2 - A_1}{A_1} \quad \mathbf{(8.3)}$$

in which A_2 is the PSC after the second pulse and A_1 is the PSC of the first pulse. The PPF index for increasing Δt can be consulted in **Figure 8.5(c)**. The experimental data was then fitted with **Equation 8.4**:

$$PPF\ index = c_1 e^{-\Delta t/\tau_1} + c_2 e^{-\Delta t/\tau_2} \quad \mathbf{(8.4)}$$

where c_1 and c_2 are the initial facilitation magnitudes of different phases, and τ_1 and τ_2 are the characteristic relaxation times of the respective stages. In biological synapses, the decrease of the PPF decay with pulse interval can be ascribed to a transition between a fast memory stage of tens of milliseconds and a slower phase lasting hundreds of milliseconds.[7] The memristor also presents this behavior, as can be seen by the fitting with equation 2 returning τ_1 of 1.82 s and τ_2 of 32.55 s.

Another important synaptic rule is STDP. According to STDP, the synaptic weight change (ΔW) is positive (connection becomes stronger) if a pulse applied to the pre-synaptic neuron arrives before a pulse is applied to the post-synaptic neuron. Contrarily, if the post-synaptic pulse arrives before the pre-synaptic pulse, ΔW is negative (connection becomes weaker). Moreover, ΔW should be weakened by non-coincidental neuronal firing.[67] Here, Δt represents the time interval between the pre- and post-synaptic pulses. ΔW represents the difference between the PSC after both spikes have been applied and the PSC before any pulse arrives. Therefore, the higher the Δt, the lower the ΔW should be. To simulate this behavior with the H-doped IGZO OEM, the pre-synaptic and post-synaptic pulses were first decided as an optical pulse of 1 s (blue light) and an electrical pulse of 2.5 V for 1 s applied to the bottom contact, respectively. The results are displayed in **Figure 8.5(d)** in which the ΔW is positive for $\Delta t>0$ and negative for $\Delta t<0$. Moreover, a decrease in $|\Delta W|$ is also observed for $\Delta t>>0$ and $\Delta t<<0$. The STDP learning rule was, therefore, successfully replicated in our optoelectronic synapse. The STDP time window was fitted by **Equation 8.5**:

$$\Delta w = \begin{cases} A^{+}e^{-|\Delta t|\tau^{+}}, & if\ \Delta t > 0, \\ A^{-}e^{-|\Delta t|\tau^{-}}, & if\ \Delta t < 0 \end{cases} \quad \mathbf{(8.5)}$$

where A^+, A^-, τ^+ and τ^- are free parameters representing the scaling factor and time constant of the exponential function, respectively, that can be discovered by fitting the experimental data with no restriction.[67] The STDP data is well described using this equation returning τ^+ of 32 ms and τ^- of 54 ms. It is important to note that the STDP characteristic presents the typical asymmetric Hebbian learning rule form, similar to a hippocampal neurons culture,[68] as often shown in previous works reporting on synaptic devices.[69] Here, since the effect caused by the pre-synaptic pulse (optical) does not correspond to the one caused by the post-synaptic pulse (electrical), the synaptic weight changes are not symmetric in Δt>0 and in Δt<0. The higher current change achieved in positive time interval can come from more significant Joule heating, which can enhance mobility and accelerate the switching process. This can be adjusted with calibration of different pulse schemes (duration, amplitude), waveform shape (rise and fall time) or even application of current limiting technique. As other studies report, the STDP characteristic can be tuned by the development of appropriate spiking inputs and order that depend on the envisioned application.[70]

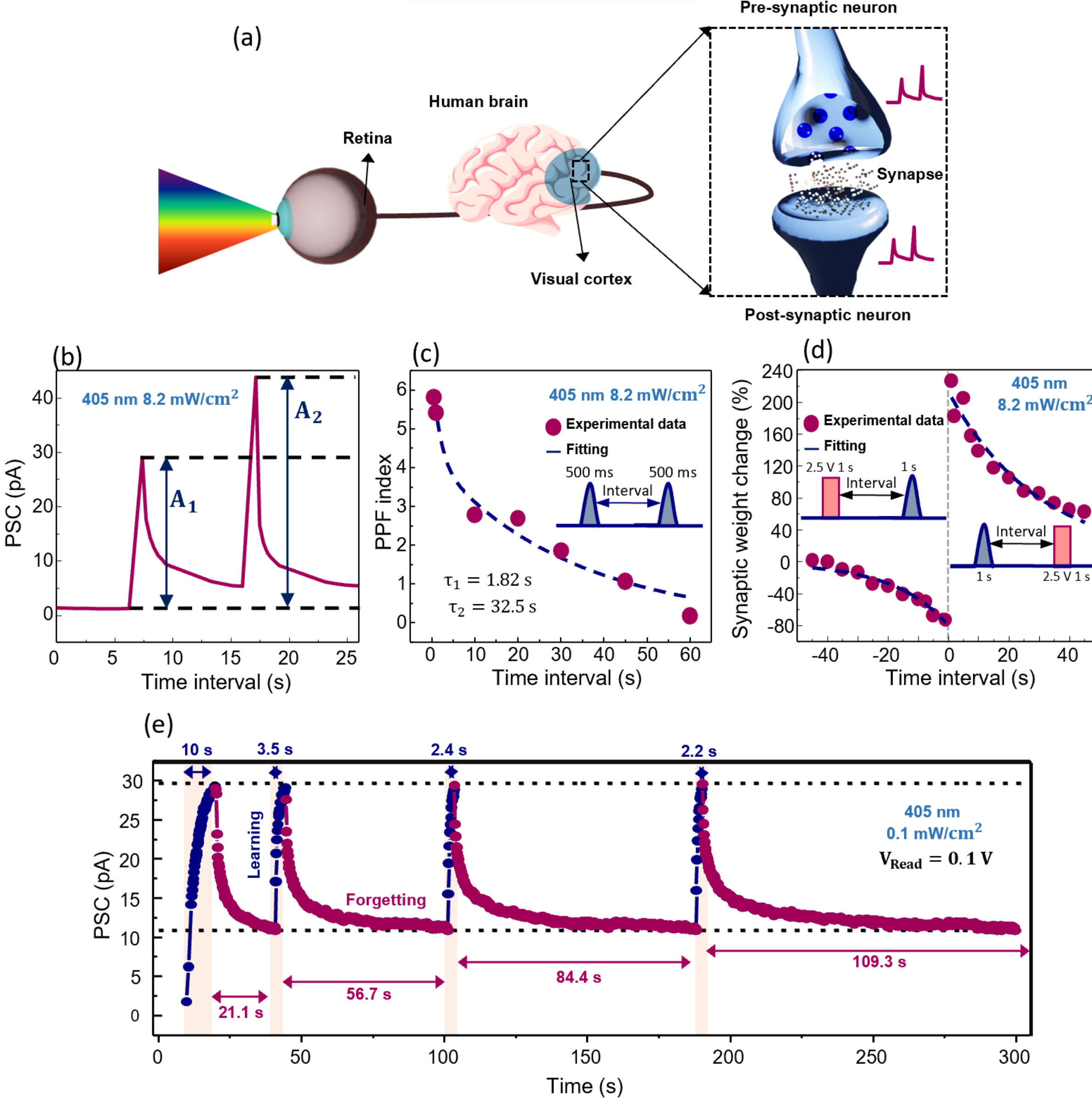

Figure 8. 5 Synaptic functions emulated by the H-doped IGZO optoelectronic memristor. (a) Schematic illustration of the human visual system. (b) Post-synaptic current (PSC) evolution during a pair of optical pulses of 500 ms each with time interval 10 s. (c) Paired-pulse facilitation (PPF) index for different time intervals. (d) STDP learning rule. An optical pulse of blue light for 1 s serves as the pre-synaptic pulse and an electrical pulse of -2.5 V for 1 s is implemented as the post-synaptic pulse. (e) Learning and Forgetting demonstration. Learning is performed by illumination with 405 nm wavelength and 0.1 mW/cm^2. Forgetting is performed in the dark by applying the V_{Read} of 0.1 V.

Finally, learning and forgetting behaviors were also reproduced by our memristor. In Figure 8.5(e), 4 cycles of learning and forgetting processes are shown. Learning is simulated by applying constant blue light with 0.1 mW/cm^2 intensity. Each learning cycle is stopped as soon as the maximum current achieved in the first learning is reaches. Forgetting is performed in the dark by applying solely the V_{Read} of 0.1 V. Each forgetting cycle is stopped as soon as the current state from the first forgetting

process is reached. The time it takes the device to learn decreases with each cycle, starting with 10 s in the first cycle and finishing with 2.2 s at the fourth cycle, indicating faster relearning with task repetition. On the contrary, the forgetting time increases with each cycle, starting with 21.1 s in the first cycle and finishing with 109.3 s in the fourth cycle, indicating harder forgetting, once again successfully mimicking the human brain. In **Figure E.13 - Appendix E**, the learning and forgetting behavior is shown in a different form and by pulsed light.

8.4 Conclusions

In summary, a 4 μm^2 optoelectronic memristor based on IGZO is presented in this work with enhanced characteristics. Thin Ti/Au is employed as transparent top electrode since it increases VOs concentration at the IGZO interface due to the oxygen affinity of Ti, improving optical performance. H-doping is performed by introducing H_2 in the IGZO sputtering deposition to induce the creation of sub-gap states for visible range photodetection. Extremely high light/dark ratios of 179, 93 and 12 are observed for UV, blue and green illumination, respectively. Moreover, all relevant synaptic functions for SNNs are demonstrated such as STM to LTM transition, PPF, STDP and learning and forgetting capabilities by manipulating the PPC decay. Therefore, the proposed optoelectronic memristor can be considered for applications in flexible neuromorphic vision sensors, representing an enormous enhancement on conventional artificial visual systems, and in more detail to the IGZO-based display AOS pixel-driver circuit technology employed in commercial IGZO flat panel displays.

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CHAPTER 9

PHOTOPERCEPTRON HARDWARE FOR ARTIFICIAL VISUAL SYSTEMS

Traditional image sensor technologies are limited in efficiently capturing dynamic visual information. Neuromorphic vision sensors, inspired by biological vision systems, offer continuous motion detection and selective data processing, minimizing redundancy and enhancing energy efficiency. Leveraging optoelectronic synaptic devices, near-sensor and in-sensor computing paradigms enable real-time image processing within hardware. In fact, implementations of neuromorphic vision sensors using optoelectronic devices, in crossbar and pixel arrays, with trainable photoresponsivities illustrate their potential in pattern recognition and object tracking applications. Here, we propose an IGZO-based photoperceptron hardware designed for neuromorphic vision sensors and evaluate its potential across various tasks including contrast enhancement, color detection, pattern recognition, and motion tracking. The prototype development of this hardware stands as a natural future perspective of this Ph.D. work, and is already in progress. The IGZO-based photoperceptron hardware for neuromorphic vision sensors promises efficient manufacturing and integration, potentially revolutionizing high-resolution display systems with real-time sensing and processing capabilities.

The results presented in this chapter are being prepared for submission in:

M.E. Pereira, R. Martins, E. Fortunato, P. Barquinha and A. Kiazadeh, "**All-in-one photoperceptron hardware based on IGZO for neuromorphic vision sensors**", under preparation, 2024.

9.1 Introduction

Modern image sensors predominantly rely on photodetectors, such as charge-coupled devices (CCD)[1] and CMOS active pixel sensors (APS),[2] organized in 2D arrays to capture digital images of the environment. These systems typically include a memory unit for storing images and a processing unit for executing algorithms for tasks such as pattern recognition and motion detection. Operated by artificial timing and digital signals, the sensors capture a series of static images called frames, recording data from all pixels regardless of changes since the previous frame. This frame-based method can miss critical information at low frame rates or generate excessive redundant data at high frame rates, especially problematic in applications requiring real-time data and high-speed processing, such as autonomous navigation and motor control. The transfer of large volumes of visual data to processing units results in delays, increased bandwidth demands, and high-power consumption.[3–9]

In contrast, neuromorphic vision sensors emulate the human eye by detecting rapid changes directly and continuously recording motion data. Each pixel operates independently, activating only when a change occurs, ensuring only relevant data is processed.[10–13] This approach significantly reduces data volume, enhances energy efficiency and accelerates system responses. The most suitable neural network architecture for processing this type of data is Spiking Neural Network (SNN), which mirrors biological neural networks. Unlike conventional artificial neural networks (ANNs), SNN neurons fire only when their membrane potential exceeds a threshold, sending spike signals that adjust the synaptic weights of connected neurons and potentially triggering them to fire as well. However, the vision algorithms such as motion detection are still in the early stages of development. Therefore, it is important to highlight that just as event cameras are designed based on biological sensing principles, the algorithms for processing event-driven data should also be bio-inspired, obtaining relevant data in a similar approach to biological vision.[13]

Optoelectronic synaptic devices are emerging as promising components for the future of artificial vision due to their ability to directly respond to optical signals, present temporary or permanent optical memory, and process visual data in real time.[14] Unlike typical image sensors that measure light intensity linearly at each pixel, these novel devices can sense visual information with light wavelength/intensity and time-dependent memory. Having initially being conceived for in-memory computing using optical signals to modulate conduction states without crosstalk,[15–17] these devices have recently gained attention as neuromorphic vision sensors capable of both optical sensing and in-memory computing. Consequently, neuromorphic vision sensors can be categorized into near-sensor and in-sensor computing, reflecting the optoelectronic synaptic devices' dual functionality in sensing and processing visual data.[12]

Neuromorphic vision sensors for in-sensor computing perform optical sensing and post-processing within a single device, enabling self-processing of image recognition tasks. This integration can minimize data transmission and significantly enhance the efficiency of the image recognition process.

In-sensor computing is therefore ideal for future artificial visual systems and mobile electronic devices, paving the way for more efficient and compact AI technologies.[9] In this regard, Jang *et al.* developed a 32x32 crossbar array based on MoS_2 FET transistors for pattern recognition, employing the array first as an optical image sensor and then reconfiguring it for analog vector-matrix multiplications (VMMs) for image recognition. The FETs' persistent photoconductivity (PPC) allowed the crossbar to store optical images as electrical data, which were then used as input to the software-based convolutional neural network (CNN) for pattern recognition. The crossbar array was then optically reprogrammed based on the training weights returned by the software-based CNN, to recognize images, achieving 94% accuracy on 1000 MNIST digits. Thus, the proposed crossbar could perform sensing and processing to pattern recognition but could not perform both tasks simultaneously.[18] In another work, Mennel and his team designed a 9x9 pixel array with trainable responsivities using lateral p-n junction photodiodes, enabling real-time multiplication of projected images with a photoresponsivity matrix. Each pixel employed three photodiodes coupled with two controlling gates.[19] In a similar strategy, another study demonstrated that image sensors based on vertical heterostructures could emulate biological photoreceptors and bipolar cells, enabling simultaneous image sensing and processing for tasks like pattern recognition.[20] Although these works show outstanding potential for future applications, using light as synaptic weight modulator and as sensing unit, impedes the implementation of advanced multi-layer neural networks. The optical inputs cannot be cascaded into subsequent hidden layers, limiting processing performance and accuracy. Additionally, the proposed complex architectures require multiple devices per pixel to allow light to be both the training and sensing source, further complicating the system.[21]

In contrast, near-sensor computing can perform a pre-processing of an input image, enhancing electrical signals, to be sent to a post-processing unit for image recognition. Visual information arrives to the synaptic device array and changes the conductance state in each pixel in a non-volatile manner, by making use of PPC. The conductance states can be additionally updated via subsequent image exposures, owing to the existence of analog conductance states. Consequently, by mapping the updated conductance values of the synaptic array, an incident image can be captured and converted into a more refined image. This pre-processing step greatly reduces the computational load and processing time in the post-processing unit compared to working with raw image data. Accordingly, in near-sensor computing, the image sensor and the processing unit are separated.[22] For instance, Zhou *et al.* introduced an optoelectronic memristor (OEM) composed of Pd/MoO_x/ITO, capable of sensing ultraviolet (UV) light and displaying light-tunable synaptic behaviors. The memristor array enabled image sensing, memorization, and pre-processing. Due to the light-dosage tunable plasticity of the memristor, it effectively highlighted key features of the input images while reducing background noise, which was shown to enhance the efficiency and accuracy of the image recognition task. It was then proposed by the authors that after pre-processing, the enhanced electric signals would be transferred to a software-based ANN for final image recognition.[23]

Even more advanced, an all-in-one neuromorphic vision sensor can be designed to be able to simultaneously perform image sensing and neuromorphic in-memory computing during and after the input of visual data. In such a system, image sensing and primary in-situ processing is achieved by the optoelectronic synaptic device array and the enhanced data is then processed in hardware as well, allowing for truly real-time tasks in a power-efficient manner. In this regard, Seo *et al.* proposed an optic-neural network by implementing a synaptic device (memristor) and an optical-sensing device on h-BN/WSe_2 heterostructure. The authors simulated a 28x28 crossbar using the extracted device parameters of the heterostructure. This system would perform color and color-mixed identification between red, green and blue while distinguishing between the algorithms 1 and 4 (e.g. red algorithm 1, green algorithm 2, etc). However, from what can be understood, since the input voltage is also dependent on the color being applied to each pixel, the proposed system is not in fact realizing color discrimination by itself. For that, the only changing parameter would have to be the photocurrent produced by each pixel. Nonetheless, the accuracy of the task was greatly enhanced by this color filtering function. Moreover, this work has shown the potential of this kind of systems for color discrimination applications and suggested the integration of sensing ability in the first layer of a neural network composed of memristors.[24] In another work, a coordinated perceptive computing scheme was proposed using vertically integrated dual-mode organic memristors in sequential integration of a single-layer perceptron (SLP) neural network and a CNN. Light would pass through lenses and filters, reaching the optoelectronic perceptive layer where it would be converted into a photocurrent signal. In the upper layer, device photoresponsivity's could act as synaptic weights for VMM operations in a SLP neural network, enabling preliminary image processing and classification based on contours. In the lower layer, further VMM operations were carried out, enhancing recognition accuracy with the CNN algorithm.[21] Finally, a more recent, and very exciting study, introduced a flexible artificial visual system that combines optical perception, in-memory computation, and on-chip learning. Using SnO-based optoelectronic synaptic transistors as event-driven sensors, the system enabled dynamic image perception, noise reduction, detection, and recognition. The transistors could produce a gate-tunable bidirectional optical response, mimicking the biological functions of bipolar cells. Each pixel would independently trigger an ON or OFF action according to changes in light intensity, by the increase and decrease of the transistors' conductance states. Pre-processed images were then inputted as voltage signals into a multilayer neural network for on-chip learning, achieving up to 95.2% accuracy in pattern recognition tasks.[25] This latter work has shown the immense possibilities for neuromorphic vision sensors all built in hardware. However, using transistors as synaptic element for sensing unavoidably increases cell area when compared with vertical memristors.[3]

In our previous work, we developed an OEM based in IGZO that could successfully emulate all relevant synaptic functions of SNNs, such as learning and forgetting behavior, spike-time dependent plasticity (STDP) and paired-pulse facilitation (PPF). This hydrogen-doped device presented extremely high I_{light}/I_{dark} ratio and was photosensitive to green, blue and UV light in different conductance ranges.

In another study, we have also proposed a 1T1M crossbar for in-memory computation in which cross-talk was solved by the IGZO-thin film transistor (TFT) added to each memristor cell.[26] The memristor itself was also based in IGZO and presented analog conductance states.[27,28] Here, we discuss the potential applications of our developed IGZO-based OEM as a sensor unit and our 1T1M crossbar as a processing unit for a all-in-one neuromorphic vision sensor using near-sensor computing, aiming for an upcoming prototype development.

Neuromorphic vision sensors are generally designed for computing tasks such as denoising (contrast enhancement), spectral filtering, pattern recognition of visual information, and/or object tracking, which are therefore the main tasks discussed here. The proposed hardware for neuromorphic vision sensors, all based in IGZO, could be termed a "photoperceptron", and could be manufactured very efficiently. This is due to the shared material layers among all devices and the utilization of the same deposition and patterning techniques, allowing for a straightforward, cost-effective, and rapid fabrication process that can accommodate flexible substrates due to low processing temperatures. IGZO TFTs could also compose the peripheral circuits for on-chip learning. The integration of IGZO-based devices with pixel-driver circuit technology utilized in commercial flat panel displays could pave the way for ultra-high-resolution System on Panel (SoP) applications, ushering in a new era of neuromorphic display systems. These displays would not only emit light to generate images but also have the capability to sense and process visual information in real-time. Collectively, these factors could culminate in the development of an exceptional and highly advanced prototype for neuromorphic vision sensors.

9.2 Neuromorphic vision sensor tasks

9.2.1 Pre-processing by contrast enhancement

The task of contrast enhancement can be performed by employing an OEM crossbar as the sensing unit in neuromorphic vision hardware, utilizing the analog conductance states. **Figure 9.1(a)** presents a schematic illustration of an experiment design for proof-of-concept, involving the developed IGZO-OEM. In this design, a shadow mask allows green light from a LED common source to pass through in the shape of the letter X to a 3x3 crossbar, composed of nine 4 μm² OEMs. The considered experimental device parameters are shown in **Figure 9.1(b)**, demonstrating the photoresponse increasing during 30 seconds of exposure time and the PPC in the dark after exposure. **Figure 9.1(c)** depicts theoretical color maps of the crossbar, illustrating conductance state changes after 1, 5, and 30 seconds of exposure. The contrast enhancement is evident at each step.

For pattern recognition of the input letter X, this pre-processing layer would then be connected to either a software or hardware neural network. The accuracy of the task would be significantly

enhanced if performed after 30 seconds of exposure due to the contrast enhancement. The same experiment could be performed using light pulses instead of constant exposure. Device-to-device variability is not considered here, though it will be in practical experiments, as it has been shown to be extremely small (Chapter 8). As described previously, a study by Zhou *et al.* demonstrated through simulation that recognition accuracy reached 98% after 1000 training epochs with pre-processing through an OEM crossbar, whereas double (2000) training epochs were required to achieve the same accuracy without OEMs. Consequently, the image-recognition efficiency, including processing speed and energy consumption, was also significantly improved by 41.5% to reach a pattern recognition accuracy of 99%.[23] This work showcased the potential of the optoelectronic device, which in the case was sensitive only to UV light. Our IGZO memristor would be able to perform not only the same tasks while using visible light as input, launching unlimited possibilities in a range of applications such as in displays and cameras, where visible light LEDs are used as light sources.

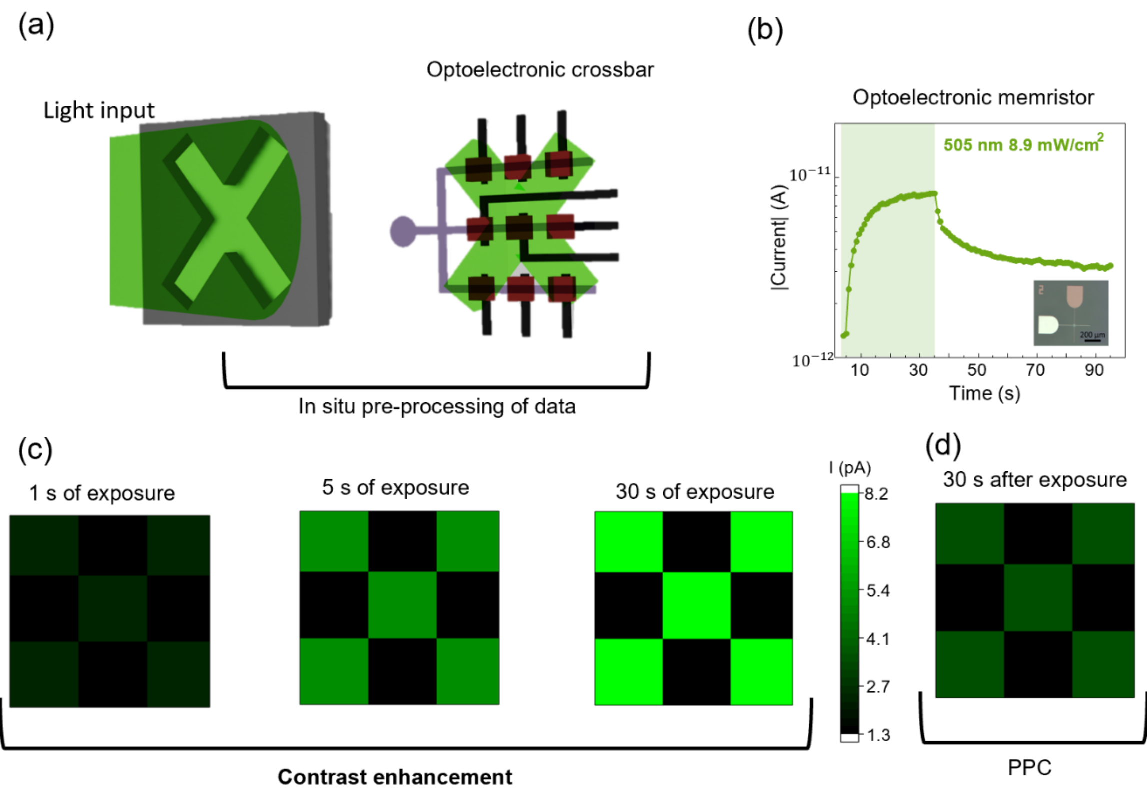

Figure 9. 1 Experiment design for in-situ preprocessing of data through the IGZO optoelectronic memristor crossbar. (a) Schematic Illustration showing a shadow mask for the letter X allowing green light to pass to a 3x3 optoelectronic memristor crossbar. (b) Experimental transient response of the 4 μm^2 IGZO-based optoelectronic memristor during 30 s of exposure to green light and 1 min. of PPC effect. (c) Theoretical color maps of the conductance in each cell of the IGZO crossbar during exposure for 1, 5 and 30 s of exposure, showcasing contrast enhancement features. (d) Theoretical color map of the conductance in each cell of the IGZO crossbar after 30 s in the dark following 30 s of exposure.

Another advantage of using OEMs instead of standard photodetectors is that the PPC effect can be used to store the input image after stimuli. As an example, **Figure 9.1(d)** presents the theoretical color map of the IGZO optoelectronic memristor crossbar 30 seconds after stimuli to the letter X. Here, the contrast enhancement feature can also be employed by changing exposure time; more exposure time results in less pronounced state decay and, therefore, an image with enhanced features.

9.2.2 Motion detection by SNNs rules

As explained, neuromorphic vision sensors have as a primary goal to mimic the human eye by detecting changes and recording motion data continuously. Each pixel should activate independently when changes occur, processing only relevant information, reducing data volume. SNNs are ideal for processing this data, as their neurons fire only when a certain threshold is met. However, developing vision algorithms like motion detection is challenging, and there have been limited efforts to address the application challenges posed by 3D signals, such as videos. This limits memristor-based neural networks to simpler tasks and prevents them from achieving complex biomimetic functions.

In a recent work by Wu *et al.,* object tracking was simulated using experimental data from OEMs by marking the object to be tracked in the first frame of a video.[29] Thus, here a similar experiment is designed for future practical demonstration. A shadow mask is once again employed to allow blue light in the form of the letter T to pass through to a 3x3 optoelectronic memristor crossbar. The light is inputted through a 500 ms pulse. After 1 second, the shadow mask moves to the right, and another 500 ms pulse is applied. Relevant SNN rules demonstrated by the IGZO- OEM are shown in Chapter 8. For this experiment, PPF is used to exemplify the motion tracking task. **Figures 9.2(a)**, **9.2(b)**, and **9.2(c)** display the experimental device parameters (G_{dark}, G_1, G_2, and $G_{after\ 1s}$). **Figure 9.2(d)** depicts theoretical color maps of the crossbar, showing conductance state changes before and after the shadow mask movement. If the threshold is set slightly higher than the first pulse, only neurons a_2 and a_3, subjected to two consecutive pulses, will fire, signaling the system that there was movement, as illustrated in **Figure 9.2(e)**. With the information from the two consecutive pulses on specific pixels, the system can determine the direction of the letter T's movement and follow it. Naturally, the timing between consecutive pulses should be studied and optimized to determine the speed at which the hardware system can operate. A command can also be implemented to record changes, similar to event-driven cameras.

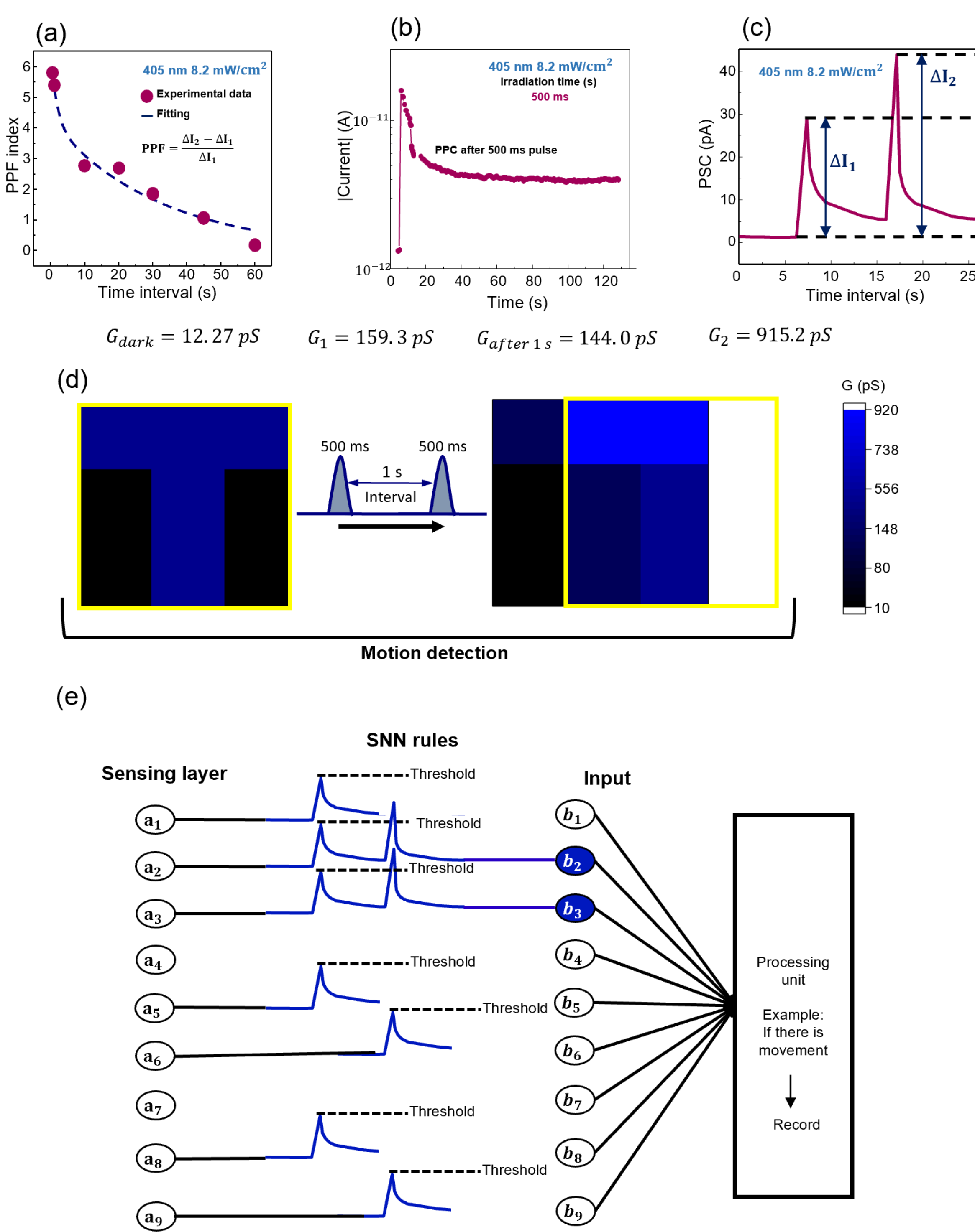

Figure 9. 2 Experiment design for motion tracking through the IGZO optoelectronic memristor crossbar. (a) Experimental paired pulse facilitation test by applying two 500 ms blue light pulses with different intervals. (b) Experimental PPC decay after one pulse of 500 ms. (c) Post-synaptic current (PSC) evolution during a pair of optical pulses of 500 ms. (d) Theoretical color maps of the conductance in each cell of the IGZO crossbar during the first pulse and during the second pulse, after letter T movement, for time interval of 1 s. (d) Schematic of the conductance evolution in each pixel showing only a_2 e a_3 firing.

9.2.3 Color discrimination neural network

As the IGZO OEM exhibits different photoconductivity depending on the wavelength of the visible light input, it can be used to develop an optic-neural network for color discrimination and pattern recognition, similar to the proposal by Seo *et al.*.[24] **Figure 9.3(a)** schematically illustrates an experiment with four possible inputs: a blue X, a blue T, a green X, and a green T. These inputs can be applied through a shadow mask to a 3x3 crossbar, as described in the above experiment designs. The input voltage would remain constant for all the pixels, while the conductance of each device would depend on whether their particular pixel was exposed to blue light, green light or no light at all. The experimental conductance for the color maps were extracted from the graph presented in **Figure 9.3(b)**. Preprocessing could be performed in-situ through contrast enhancement as previously explained, after which this unit would be connected to the input layer of a software or hardware neural network for data processing. This neural network would have nine input neurons, one for each pixel, and four output neurons, one for each possible solution.

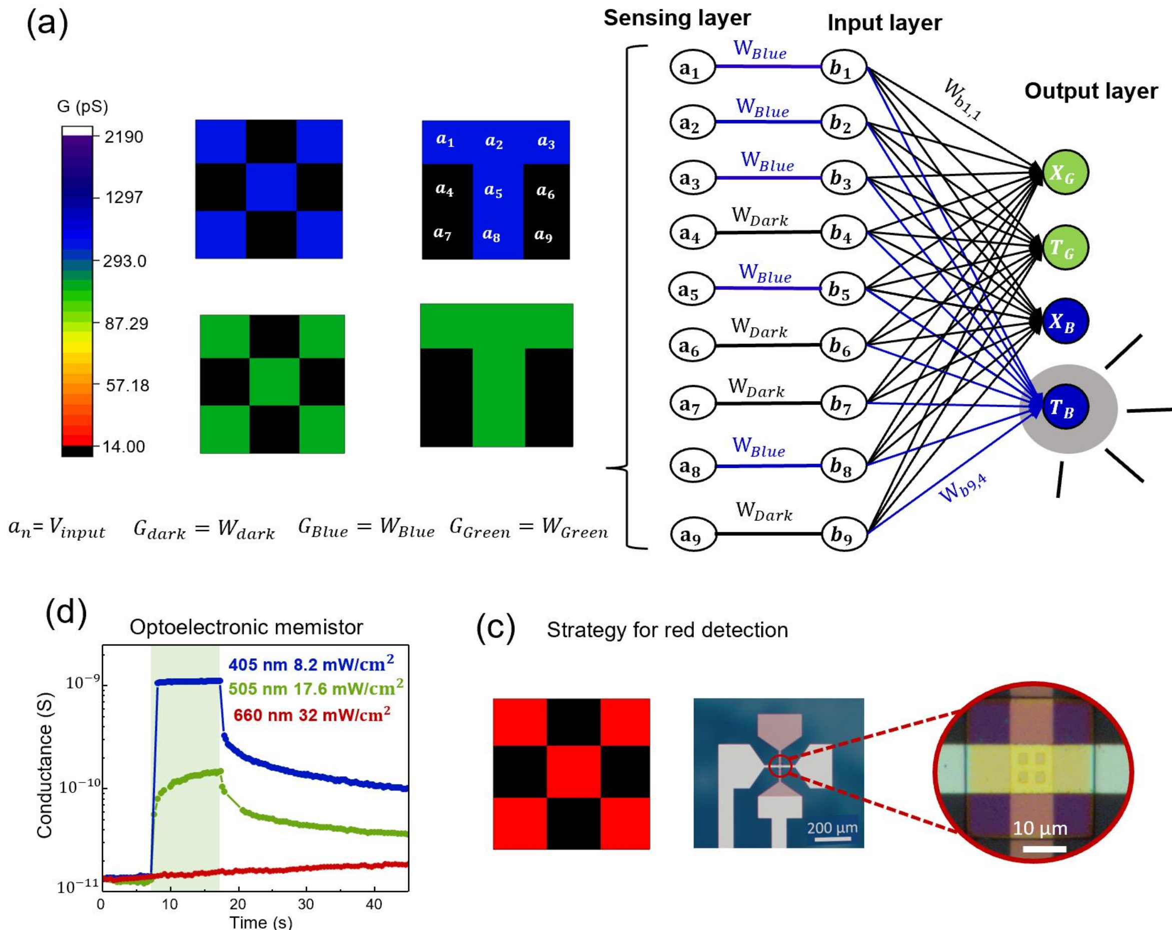

Figure 9. 3 Experiment design for color discrimination and pattern recognition through the IGZO optoelectronic memristor crossbar. (a) Schematic illustration of the envision neural network displaying the theoretical color maps of the conductance in each cell of the IGZO crossbar for each possible input. (b) Experimental transient response of the 4 µm² IGZO-based

optoelectronic memristor during 10 s of exposure to red, green and blue light and PPC effect. (c) Strategy for red detection showing micrographs of fabricated optoelectronic memristors with an implemented mesh as the top contact (Ti/Au) to improve transmittance.

Only green and blue light were considered since the IGZO memristor cannot detect red light, as shown in **Figure 9.3(b)**. Future strategies to improve detection include replacing the Ti/Au layer with a Ti/ITO layer as the top contact. As shown in Chapter 8, the Ti/Au top contact provided higher photoresponse than the ITO layer, despite having less than 60% light transmission, due to the Ti effect of oxygen gettering, which leaves more oxygen vacancies (VOs) in the IGZO to be photoexcited. However, using Ti/ITO is expected to maintain the Ti effect while allowing higher transmittance. Another strategy is to apply a photonic structure for light trapping[30] or a simple mesh,[31,32] as shown in the micrograph of **Figure 9.3(c)**, as the top contact. This approach would allow light to directly reach the IGZO layer using Ti/Au, potentially increasing the I_{light}/I_{dark} ratio for all wavelengths, improving photoresponsivity speed, and enabling red light detection.

9.2.4 All-in-one IGZO photoperceptron hardware

For the all-in-one neuromorphic hardware, a simpler neural network has been envisioned to copulate both a sensing unit composed of an OEM crossbar and a processing unit composed of 1T1M cells, all built in hardware. Such a system can be named a photoperceptron hardware. The concept dates back to 1957[33] when the term photoperceptron was first introduced as a system designed to accept optical or visual patterns as inputs. Here, we develop a single-layer photoperceptron network as schematically illustrated in **Figure 9.4(a)**. It consists of nine binary inputs (a_i) corresponding to a 3 x 3 pixel array and one binary output Y. The inputs have the values 1 or 2 and the outputs have logical values +1 or -1. The task of the photoperceptron is to organize the input patterns, displayed in **Figure 9.4(b)**, into two groups by following **Equation 9.1**:

$$Y = sgn\left(\sum_{i=1}^{9} a_i W_i\right) \qquad (\mathbf{9.1})$$

where W_i is the analogue weight representing the synaptic strength between i-input and output. The considered sets of patterns (**Figure 9.4(b)**) represent the letters “X” and “T” and their noisy versions and are adopted from previously reported strategies.[34,35] Such weights cannot be calculated analytically for the considered patterns but are found via an optimization procedure, such as the training process in the context of ANNs. During one training epoch, randomly ordered patterns from the training set are individually fed to the perceptron, and the weights are updated according to the following training rule (**Equation 9.2**) every time a new pattern is processed:

$$\Delta W_i = \alpha \times a_i^{X_1} \times (L^{X_1} - Y^{X_1}) \quad \mathbf{(9.2)}$$

where α is the learning rate, $a_i^{X_1}$ is the input from neuron i in pattern X_1 and L^{X_1} and Y^{X_1} are the labeled outputs and the actual output for the particular pattern X_1. It is important to note that the proposed perceptron is a feed-forward neural network and, therefore, does not use the back propagation algorithm for weight update, as commonly reported.

Figure 9.4(c) shows the schematic of the photoperceptron hardware implementation. The physical variables corresponding to a_i and W_i are the voltage drops in V_{a_i} nodes and the equivalent memristor conductance (G_i) of the parallel memristors G_i^+ and G_i^-. This means each synaptic weight of the neural network is represented by a pair of memristors to allow the implementation of negative values of weight. By grounding the outputs (BLs), the crossbar circuit will efficiently implement VMM operations by multiplying V_{a_i} by the correspondent G_i and the summation of the resulting currents in each 1T1M cell on each BL.

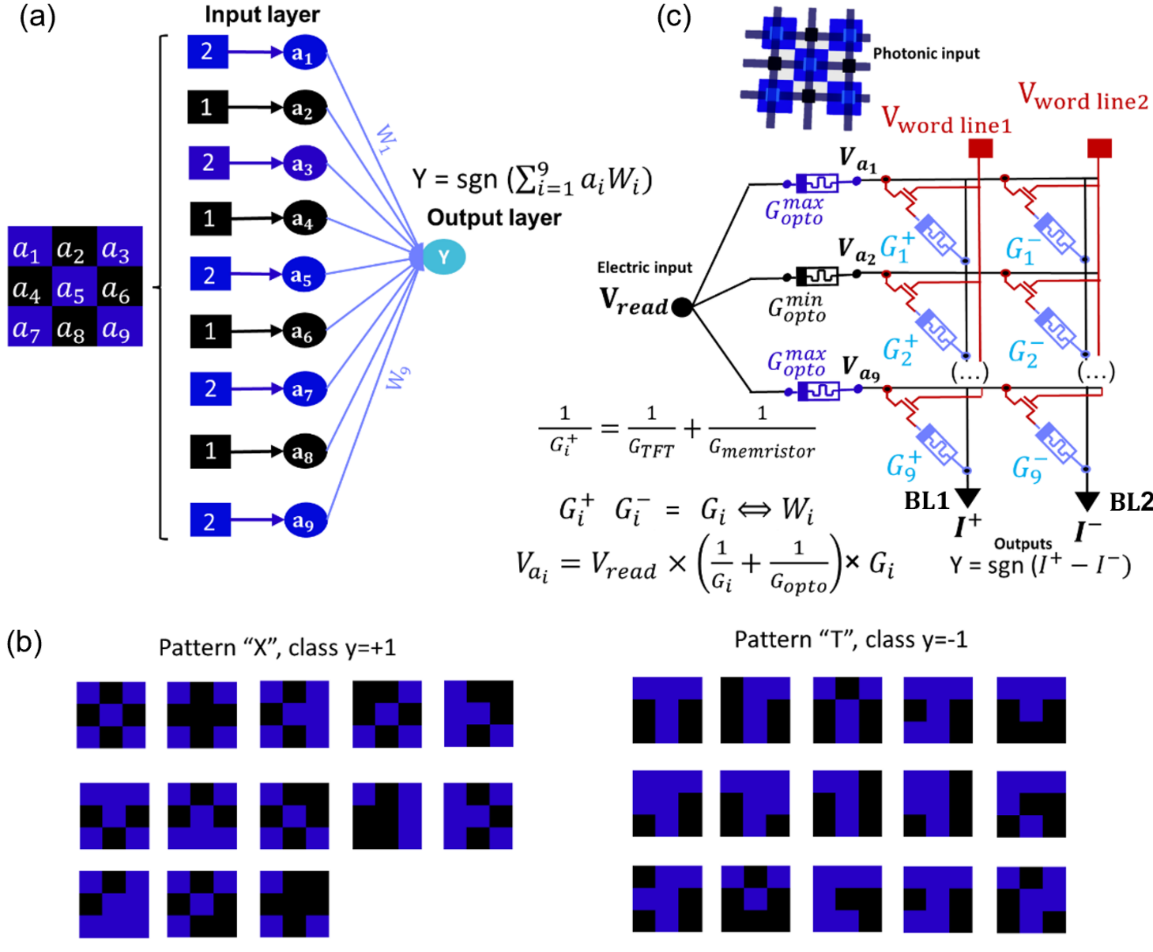

Figure 9. 4 Pattern classification setup for the all-in-one IGZO photoperceptron. (a) Schematic illustration of a single layer perceptron neural network with 9 input neurons and 1 output neuron. (b) The 28 considered patterns in the classification

experiment divided into their correspondent categories “X” (class Y=+1) and “T” (class T=-1). (c) Schematic illustration of the proposed photoperceptron hardware implementation.

As in the above experiments, the input patterns to the photoperceptron can be carried out by photonic inputs to an OEM crossbar through shadow masks. When light reaches the memristor cell, the OEM will be in the LRS and therefore present the value of maximum conductance (G_{opto}^{max}). Contrary, when the light is blocked by the shadow mask, the OEM will be in the HRS and present the value of minimum conductance (G_{opto}^{min}). These operations will then dictate the inputs V_{a_i} on the neural network.

For simplicity, ex-situ training can be performed via a software-implemented precursor network and, then, the final set of weights can be imported to the hardware. The code, written in python, can be consulted in **Figure F.1 - Appendix F**.

For the purpose of showcasing the feasibility of the proposed photoperceptron, the experimental values in **Table 9.1** were used for the calculations of the theorical outputs of the circuit, according to the developed devices during this PhD work.

Table 9. 1 Experimental values for maximum and minimum conductance used in the IGZO photoperceptron simulation.

G (S)	OEM (25 μm²)	TFT in sat. (W/L=20/5)	Memristor (25 μm²)	1T1M cell
G_{max}	3.1 x 10^{-9}	1 x 10^{-4}	3.3 x 10^{-6}	3.2 x 10^{-6}
G_{min}	4.1 x 10^{-11}		6.8 x 10^{-8}	6.8 x 10^{-8}

The final G_i^++and $G_i^-$and the theoretical output currents in each BL and the correspondent Y, for all 28 patterns representing “X” or “T”, were calculated according to the ex-situ trained W_i. The results were estimated according to the conditions in **Equation 9.3** and the results can be consulted in **Table 9.2** and **Table 9.3**. As can be seen, all 28 theoretical experiments were successfully conducted.

$$\begin{cases} G_i = W_i \times (G_{max} - G_{min}) + G_{min} \\ G_i^+ = G_i - G_{min}\,,\ G_i^- = G_{min} \quad if\ W_i > 0 \\ G_i^+ = G_{min}\,,\ G_i^- = G_i - G_{min} \quad if\ W_i < 0 \end{cases} \quad (9.3)$$

Table 9. 2 1T1M cells conductance values to be programmed in the photoperceptron hardware resulting from ex-situ training.

i	Trained weights (W_i)	G_i (μS)	G_i^+(μS)	G_i^- (μS)
[1]	-0.54	1.7	G_{min} = 0.068	1.670
[2]	-1.00	3.2	G_{min} = 0.068	3.093
[3]	0.60	1.9	1.856	G_{min} = 0.068

[4]	0.18	62	0.556	G_{min} = 0.068
[5]	-0.12	44	G_{min} = 0.068	0.371
[6]	-0.03	16	G_{min} = 0.068	0.928
[7]	0.80	2.5	2.474	G_{min} = 0.068
[8]	-1.00	3.2	G_{min} = 0.068	3.093
[9]	0.80	2.5	2.474	G_{min} = 0.068

Table 9. 3 Calculated photoperceptron output for all 28 photonic patterns representing the letters 'X' and 'T' and their noisy versions. V_{Read} =0.5 V and assuming blue light as input.

Pattern		I^+(nA)	I^- (nA)	Y
X		4.856	2.999	+1.00
		4.629	1.706	+1.00
		5.502	3.872	+1.00
		4.805	1.521	+1.00
		4.747	3.111	+1.00
		4.898	4.505	+1.00
		4.898	4.505	+1.00
		3.381	2.945	+1.00
		3.769	2.538	+1.00
		6.231	3.165	+1.00
		5.535	5.377	+1.00
		3.368	2.958	+1.00
		3.145	1.652	+1.00
T		1.936	5.928	-1.00
		1.876	4.451	-1.00
		1.903	4.423	-1.00
		3.434	5.969	-1.00
		1.903	4.423	-1.00
		3.302	6.095	-1.00
		2.574	6.801	-1.00
		0.453	5.874	-1.00
		1.819	6.040	-1.00
		3.066	4.802	-1.00
		3.242	4.617	-1.00
		1.870	2.917	-1.00
		4.563	4.843	-1.00
		3.434	5.969	-1.00
		2.541	5.295	-1.00

The fabrication of this photoperceptron hardware involves the integration of several devices and therefore, it requires an optimization procedure to make sure D2D variability is low enough for the proof-of-concept. In **Figure 9.5**, a picture of one fabrication batch taken through a magnifying glass is presented. Adapting the concepts from the work first describing perceptrons,[33] the sensory system (S-system) consists in the photonic inputs through the shadow masks. During inference, these masks would be placed on top of the OEM crossbar in a 3 x 3 configuration for image sensing, which is the association system (A-system) with in-situ pre-processing capabilities. Each pixel is then connected to one input of the 1T1M crossbar which is the processing unit, also called response system (R-system), comprising a 9 x 2 1T1M crossbar in which the memristors conductance has been previously programmed following the calculated G_i from the in-situ training explained above.

In summary, by applying an input voltage at V_{Read} and using a shadow mask to control the exposure of each pixel to blue light at the sensing unit, this proof-of-concept can distinguish between a letter X and a letter T, as well as their noisy versions. If the output current at the BLs of the 1T1M crossbar is higher at BL_1, then the input is an X. If the output current at BL_2 is higher, then the input is a T. Additionally, PPC can be used to determine the input after it has been turned off.

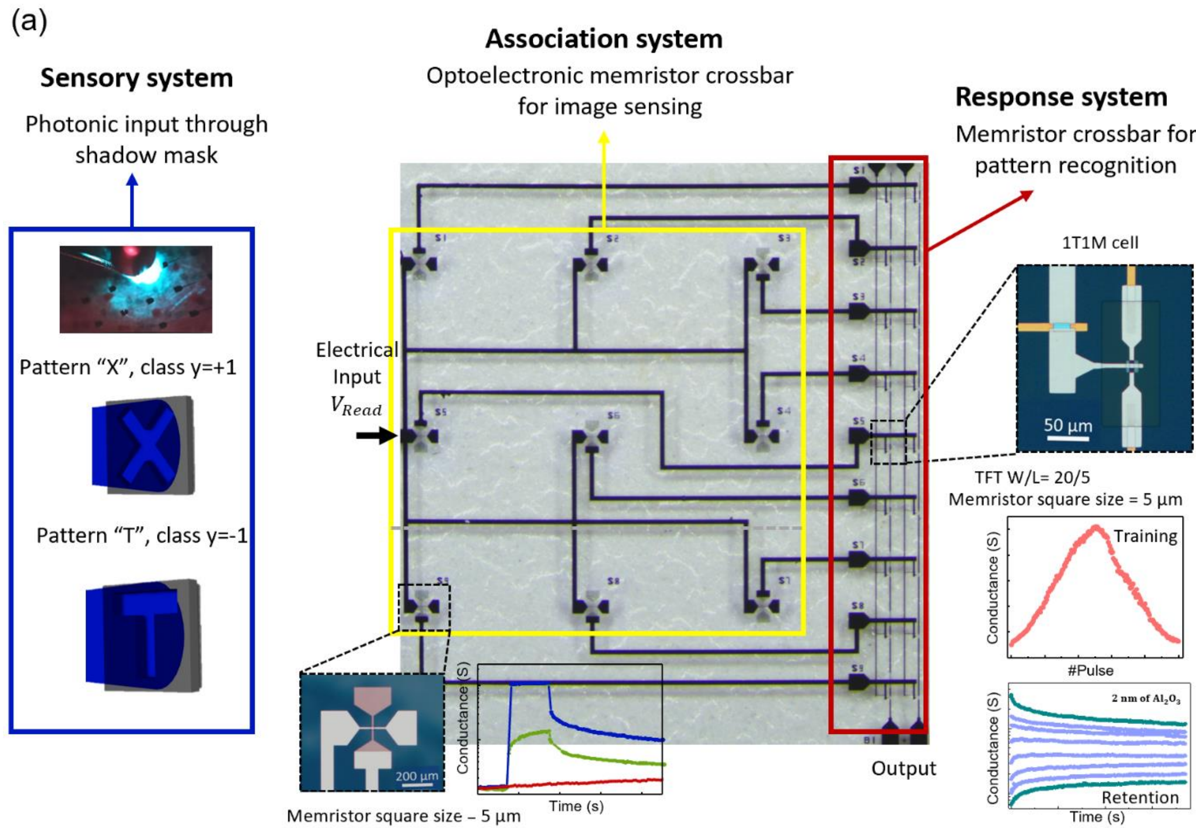

Figure 9. 5 Photograph of fabricated IGZO photoperceptron for neuromorphic vision sensor hardware. (a) Schematic illustration of two possible inputs pattern "X" and "T". Light should pass through the blue squares and perform Set on the OEMs

exposed. The final circuit will be composed of an OEMs crossbar for image sensing and SNNs and a 1T1M crossbar for image recognition through DNNs.

9.3 Conclusions

In this chapter, an IGZO-based photoperceptron hardware designed for neuromorphic vision sensors is proposed and its potential is evaluated across various tasks including contrast enhancement, color detection, pattern recognition, and motion tracking. The prototype development, optimization and fabrication of this hardware is a logical future perspective of this Ph.D. work and is already in progress. The IGZO-based photoperceptron hardware for neuromorphic vision sensors promises efficient manufacturing and integration, potentially revolutionizing high-resolution display systems with real-time sensing and processing capabilities. This work therefore builds upon the development of the devices presented in previous chapters, highlighting their potential for real-life applications such as advanced surveillance systems, autonomous vehicles, and interactive display technologies.

9.4 References

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CHAPTER 10

FINAL CONCLUSIONS AND REMARKS

The research presented in this PhD thesis has significantly contributed to the field of neuromorphic computing through the development and optimization of amorphous indium-gallium-zinc-oxide (a-IGZO) based memristive devices. The project aimed to develop AOS-based memristors with area-dependent switching, leveraging their superior performance for applications in neuromorphic computing such as spiking and deep neural networks (SNNs and DNNs), with special focus on artificial visual systems. Crosstalk in crossbars was to be solved by the integration with thin-film transistors, to act as selector devices. Moreover, the development of an IGZO-based optoelectronic memristor with visible light sensitivity was targeted for applications in neuromorphic vision sensors and a multifunctional optoelectronic system was to be proposed. Every single goal was successfully achieved as follows.

An a-IGZO memristor device was proposed using Mo as bottom and top electrodes, releasing the fabrication procedure of the common noble-metals. Endowed with area-dependent switching, excellent reliability and stability with no need for electroforming was achieved, which is crucial for large-scale manufacturing and integration into commercial systems.

The reported devices effectively emulated several synaptic functions, including synaptic potentiation and depression, short- to long-term plasticity transition (STP to LTP), and learning experience properties, making them ideal candidates for brain-inspired computing applications such as spiking neural networks (SNNs). Pushing the boundaries further, a thorough investigation into their potential for deep neural networks (DNNs) was conducted. Through meticulous optimization on the pulse scheme to achieve linear and symmetric plasticity characteristics, a remarkable pattern recognition accuracy of up to 91.82% using the MNIST dataset in simulations was attained, showcasing the potential for integration into neuromorphic hardware for in-memory computation. Since DNNs usually require a long period of retention of the programmed state, this figure of merit was meticulously optimized by the addition of an Al_2O_3 layer at the active interface, aiming nonetheless for online learning applications that do not require a full retention, usually only observed in filamentary resistive

switching. Detailed studies on the eightwise resistive switching mechanism revealed the critical role of Schottky barrier modulation and oxygen ion exchange at the bottom interface of the memristor device.

The crosstalk problem was addressed by integrating the developed IGZO-memristor with the already commercialized IGZO TFT. As a proof-of-concept, a 4×4 1T1M crossbar array was fabricated on a flexible polyimide substrate, illustrating the potential for wearable and IoT applications, with the devices demonstrating low cycle-to-cycle and device-to-device variability and with the effective suppression of sneak-path currents. Scaling up manufacturing for very-large-scale integration should not pose a significant challenge in the future, and 1T1M IGZO crossbars can effectively serve as neuromorphic processors.

Additionally, for artificial visual systems a hydrogen-doped IGZO optoelectronic memristor was developed with sensitivity to visible light in green and blue wavelengths with the highest light/dark ratios reported so far in optoelectronic memristors. Moreover, all relevant synaptic functions for SNNs were demonstrated by manipulation of persistent photoconductivity. A crossbar composed of the reported devices can easily be manufactured as a sensing unit in neuromorphic vision sensors.

Finally, an IGZO-based photoperceptron hardware design is proposed as proof-of-concept, tailored for neuromorphic vision sensors, using the developed IGZO optoelectronic memristor as sensing and pre-processing unit and a 1T1M crossbar as processor, showcasing its potential for tasks such as contrast enhancement, color detection, pattern recognition, and motion tracking. The ongoing optimization and fabrication of this hardware represents a natural progression of this Ph.D. research and is already in progress. With the potential to enhance high-resolution display systems with real-time sensing and processing abilities on flexible platforms, this IGZO-based photoperceptron hardware holds promise for diverse applications, including advanced surveillance systems, autonomous vehicles, and interactive display technologies, thus amplifying the impact of the devices developed in this work. Moreover, the use of materials and processes compatible with existing IGZO TFT fabrication techniques suggests that these advancements can be integrated into current manufacturing lines at negligible additional costs, enhancing their commercial viability. Future work should focus on further optimizing device performance and refining integration processes to fully realize the potential of these technologies in commercial and industrial applications.

A

APPENDIX

Appendix A contains additional results to the Chapter 3 of this dissertation. In summary, current density plots are presented for different memristor areas that further confirm the area-dependent switching of both the single-target and the co-sputtering devices. Resistance variation of the LRS and HRS with device size is also demonstrated for the single-target memristor. To complete the main analysis presented in Chapter 3 on the potential of the co-sputtered device as synaptic element, the same procedure is applied here on the single-target memristor, showing potentiation and depression tests and the learning behavior.

Figure A.1 shows the pristine I-V characteristics of devices with different areas fabricated with single target and co-sputtered IGZO and corresponding current density plots. All I-V curves are rectifying, related to a limited electron injection at the bottom interface.

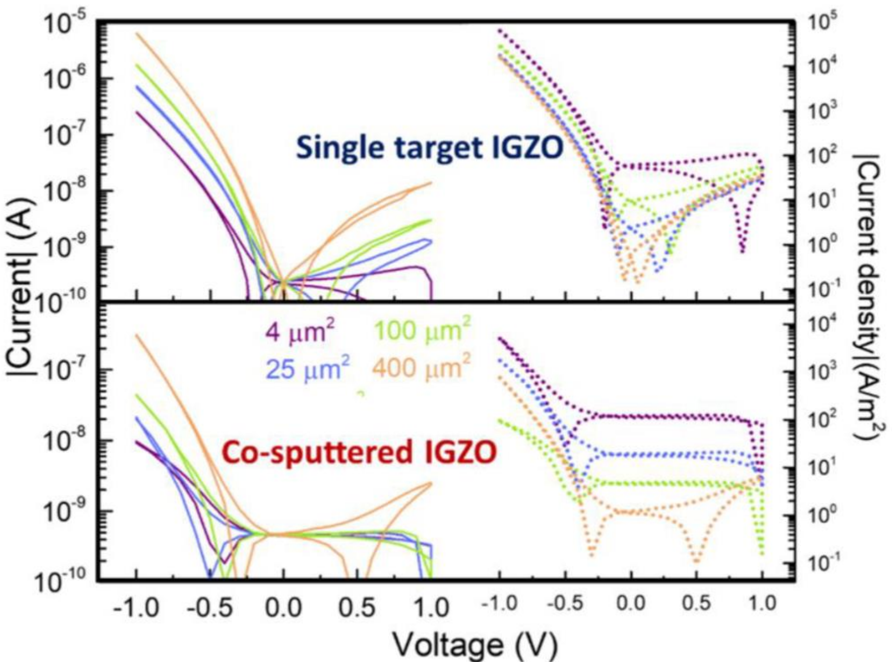

Figure A. 1 I-V characteristic between -1V and 1V, for both conditions of IGZO, with different areas and corresponding current density plots.

Figure A.2 presents the area dependence study for the devices fabricated with single target IGZO. DC sweeps were performed on devices with different areas. The lowest current at -1 V and the highest at 1 V was extracted and the resistance was then calculated according to Ohm's law.

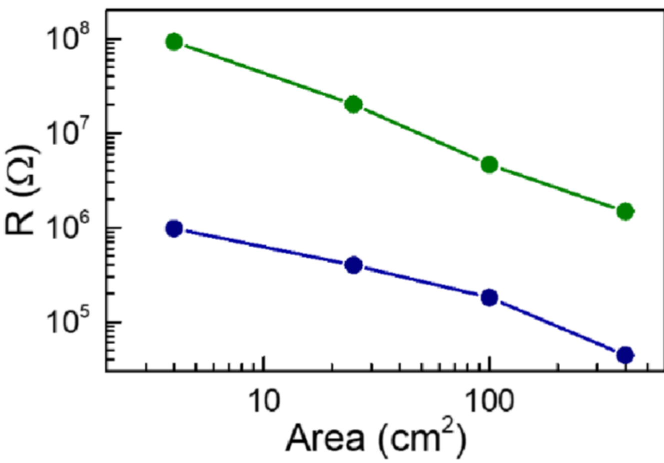

Figure A. 2 Resistance change for devices fabricated with single-target IGZO.

Figure A.3 shows the synaptic tests on the device fabricated with single target IGZO. The programming pulse amplitude and width is ± 1.5 V pulse and 100 ms, respectively, as can be seen in **Figure A.3(a)**. **Figure A.3(b)** shows the conductance response to a series of negative pulses (potentiation) immediately followed by positive pulses (depression). Reading is done between each pulse at 0.1 V, the device area is 100 µm^2. In **Figure A.3(c)**, the learning scheme is demonstrated. First, 100 pulses of -1.5 V (100 ms width) are applied to simulate the first learning process. After this, a memory retention of 700 s is performed, the read voltage is 0.1 V. By the end of this time, the device "remembers" 32 % of the signal. Immediately after this process, another set of pulse stimulation is carried out as the second learning. Each learning is followed with another memory retention record of 700 s. During the second learning, only 20 pulses are required to reach the same current state as first learning. The same experiment of third learning was carried out and after only 14 pulse stimulations the synaptic weight is again 100 %.

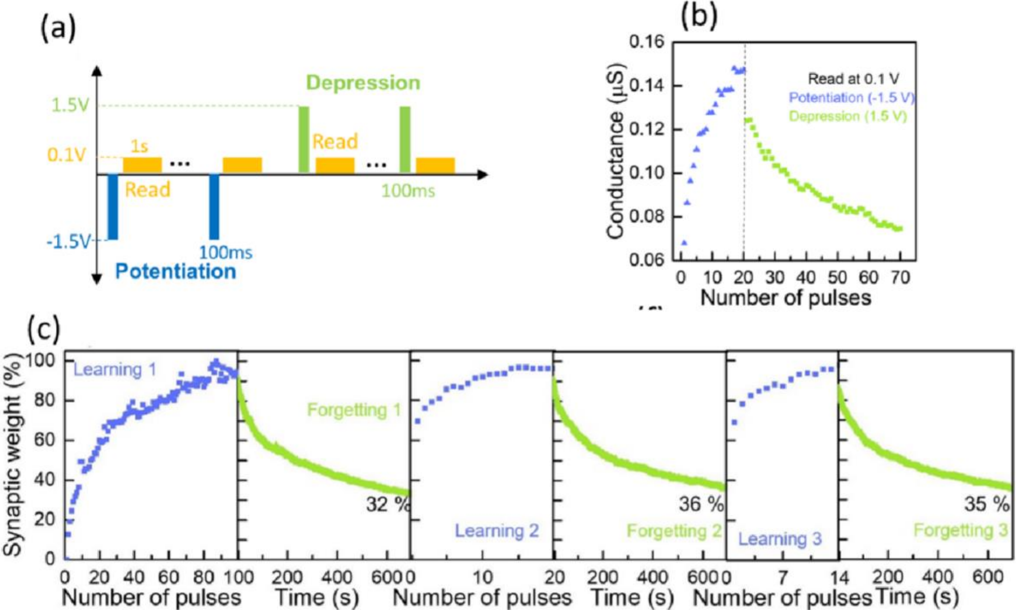

Figure A. 3 (a) pulse scheme with the positive (green) and negative (blue) bias responding to depression and potentiation respectively (b) conductance change with negative (potentiation) /positive (depression) pulses (c) synaptic weight change in percentage with number of pulses for learning 1, learning 2 and learning 3 with their retention after each potentiation.

B

APPENDIX

Appendix B contains additional results to the Chapter 4 of this dissertation. In summary, the TFT transfer curves are presented for transistors fabricated using both discussed IGZO compositions; the I-V sweeps for Set and Reset for various memristor areas are also shown; the experimental data on 20Ar/20O_2 devices, namely on the pulse scheme modulation for both exponential and linear responses, and details on the CrossSim simulation can be consulted and D2D variability for 5 different devices is discussed for both IGZO conditions.

Figure B.1 shows the transfer curve of TFTs fabricated with the same two IGZO conditions displayed for memristors. One can see that 20Ar/20O_2 TFT does not turn on for the voltages applied while the 20Ar/5O_2 TFT reveals sufficient output current proving the 1T1M integration possible using the same IGZO layer for TFT and memristor.

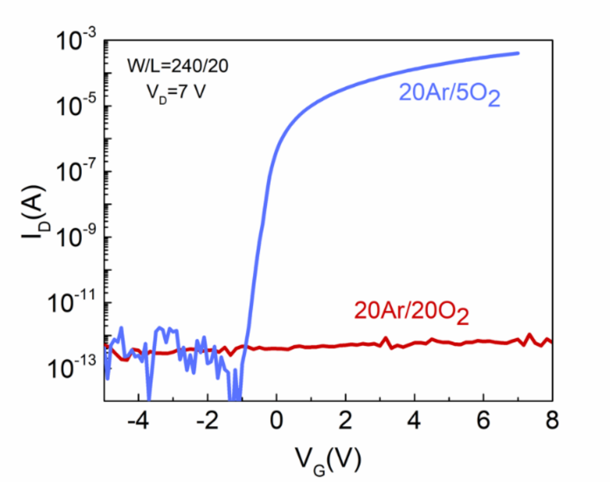

Figure B. 1 TFTs transfer curves for both IGZO conditions tried, in blue 20Ar/5O_2 and in red 20Ar/20O_2.

Figure B.2(a) shows a micrograph of a representative part of the samples displaying devices with 4, 25, 100, 400 and 900 µm^2. **Figure B.2(b)**and **B.2(c)** show the IV sweeps of one Set through current sweep and one Reset through voltage sweep for various device areas for high (20Ar/20O_2) and low oxygen (20Ar/5O_2) memristors, respectively. Current sweep was used to reduce the overshoot current and for a precise control of the current state (Doi: 10.1186/s11671-014-0721-2). The switching mechanism is area-dependent on both types of memristors since the current state increases with the devices area increase.

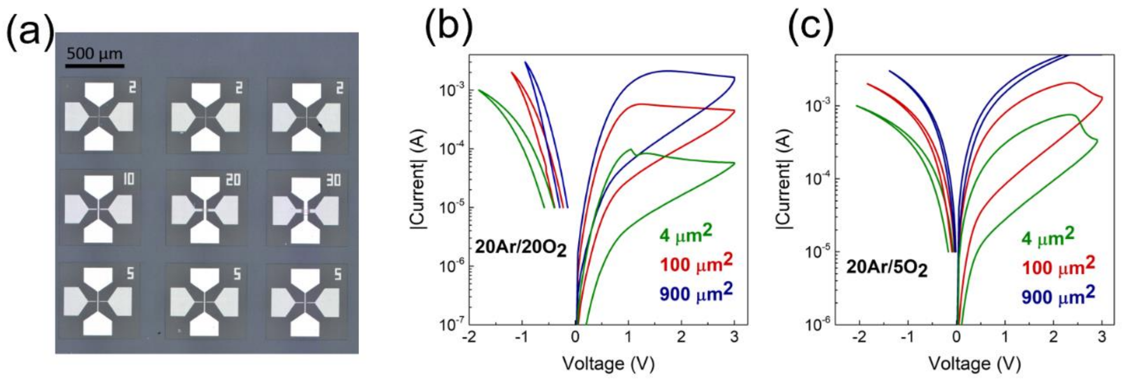

Figure B. 2 (a) micrograph of a representative part of the samples displaying devices with 4, 25, 100, 400 and 900 µm^2; IV sweeps of one Set through current sweep and one Reset through voltage sweep for various device areas for (b) high oxygen memristor 20Ar/20O_2 and (c) low oxygen memristor 20Ar/5O_2.

Figure B.3shows the study of the device characteristics under identical pulse train. Potentiation is simulated by applying negative pulses to the top contact and increasing the current state. Depression is simulated by applying positive pulses to the top contact and, therefore, decreasing the devices current state.

In **Figure B.3(a)**and **B.3(c)**, the 100 pulses potentiation for the 20Ar/20O_2 memristor with different voltage amplitudes for the same width, and the different pulse widths for the same amplitude is presented, respectively. The read step is always performed immediately after each pulse and at -0.1 V. The higher the pulse amplitude and width, the higher the current reached, but also the faster the current state gets saturated. A gradual increase seems harder to achieve than the 20Ar/5O_2 devices presented throughout the manuscript. The pulse amplitude is the parameter that controls the current state reached while the pulse width controls the gradualness of the increase.

The same tests for depression can be found in **Figure B.3(c)** and **B.3(d)**, where 100 positive pulses with different pulse amplitudes for the same width and different pulse widths for the same amplitude are shown, respectively. Using a higher pulse width means achieving the HRS state too quickly and the pulse amplitude, controls how low the HRS state can be.

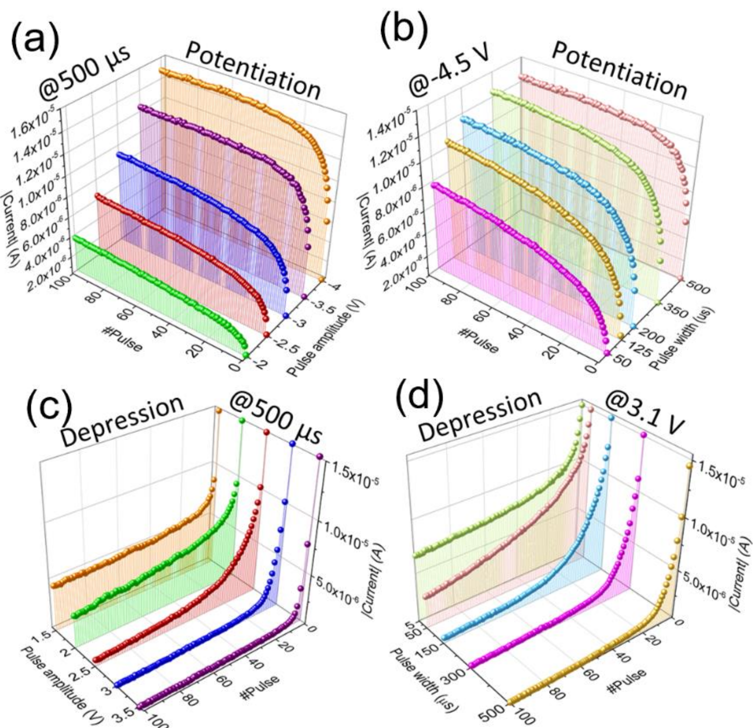

Figure B. 3 Read current at -0.1 V during application of 100 identical pulses for 20Ar/20O_2 memristors potentiation of (a) different amplitude, same width; (b) different width, same amplitude; and for depression of (c) different amplitude, same width; (d) different width, same amplitude.

Figure B.4 shows the potentiation and depression tests for the different pulse schemes tried to modulate its characteristics, to improve linearity and symmetry. In purple is the result for identical pulses and it shows an exponential response where a rapid current increase/decrease takes place within a few pulses and then reaches a saturated current regime. In red and blue are the results for non-identical schemes with either increasing pulse amplitude or width, respectively. The red curve shows a slower current increase/decrease during the first few pulses and it becomes a linear change after that and the blue curve starts in a linear fashion but it shows a current saturation after some pulses.

In green a pulse scheme of a consistent increase in pulse amplitude and width in each pulse were applied. The pulse amplitudes and widths were linearly increased from -2.2 V at 100 µs to -4.5 V at 500 µs for potentiation and 2.3 at 100 µs V to 3 V at 600 µs for depression. A linear and symmetrical response to the input pulses from beginning to end is accomplished. For all conditions, the read process is a pulse of 20 µs at -0.1 V.

To compare the linearity and symmetry on the synaptic plasticity tests that resulted from each pulse scheme, a non-linearity parameter α was extracted. The closer α is to 1, the more linear potentiation/depression is and the smaller the difference between the values of α for potentiation and depression, the more symmetric they are. In **Figure B.4(b)** the values of α_p and α_d for the different schemes are presented. For the scheme of the green curve, the most linear one, α_p = 0.97 and α_d = -0.26, these values are close to 1 and to each other, numerically revealing linear and symmetric synaptic characteristics.

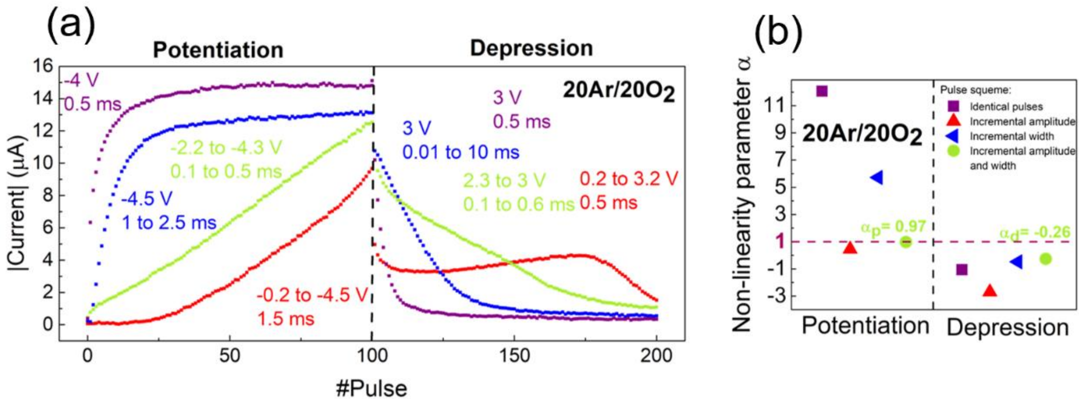

Figure B. 4 Device with high oxygen 20Ar/20O$_2$ (a) potentiation and depression results for the different pulses schemes in purple identical pulses, in blue incremental pulse width, in red incremental pulse amplitude and in green the optimized pulse scheme with incremental pulse amplitude and width; (b) non-linearity parameter for potentiation and depression for each pulse scheme, with α_p = 0.97 and α_d = -0.26 of pulse scheme D highlighted.

Figure B.5 shows the potentiation and depression tests carried out with the same optimized conditions for a linear and symmetric response for 5 different devices with the same area, for the low oxygen memristor 20Ar/5O_2 in (a) and for the high oxygen memristor 20Ar/20O_2 in (b).

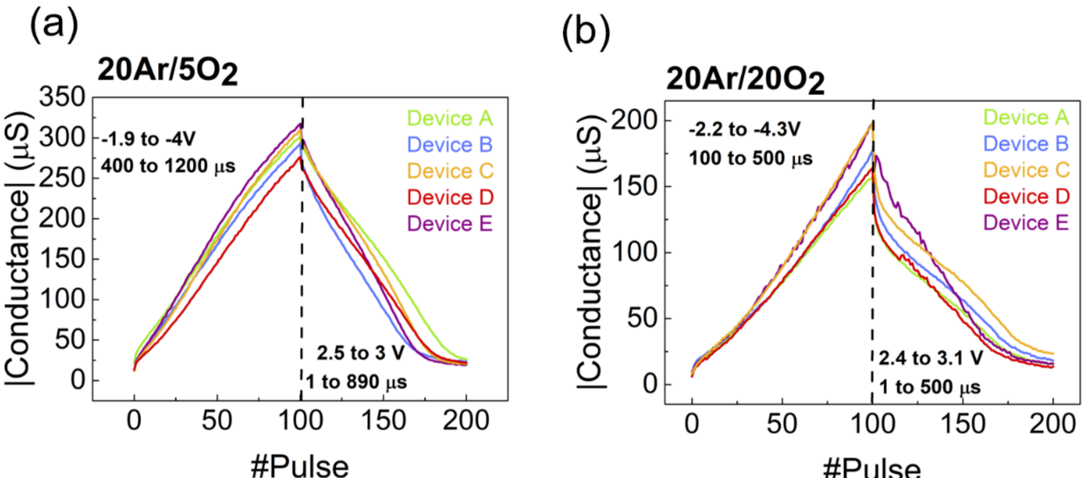

Figure B. 5 Potentiation and depression tests using the optimized scheme D for 5 different devices of (a) 20Ar/5O_2 and (b) 20Ar/20O_2 types.

Figure B.6 shows the experimental Cumulative Distribution Function (eCDF) lookup tables of the conductance change (Δ G) within the 50 cycles of potentiation/depression for the linear pulse scheme as a function of conductance (G) for the Set and Reset processes for the 20Ar/20O_2 devices. Here, the color map of CDF indicates the probability that Δ G is less than or equal to the value on the y-axis for a given conductance on the x-axis. For the lowest C2C variability, Δ G range should be small and the graph would be mostly blue with this case colormap. When the default test provided by CrossSim that uses the 25% to 75% range of the on/off window was performed a low 64.49% accuracy was obtained due to a high variability at the first cycles of depression. An adjustment was made for 10% - 60% range instead, and a high 90.93 % accuracy was achieved instead.

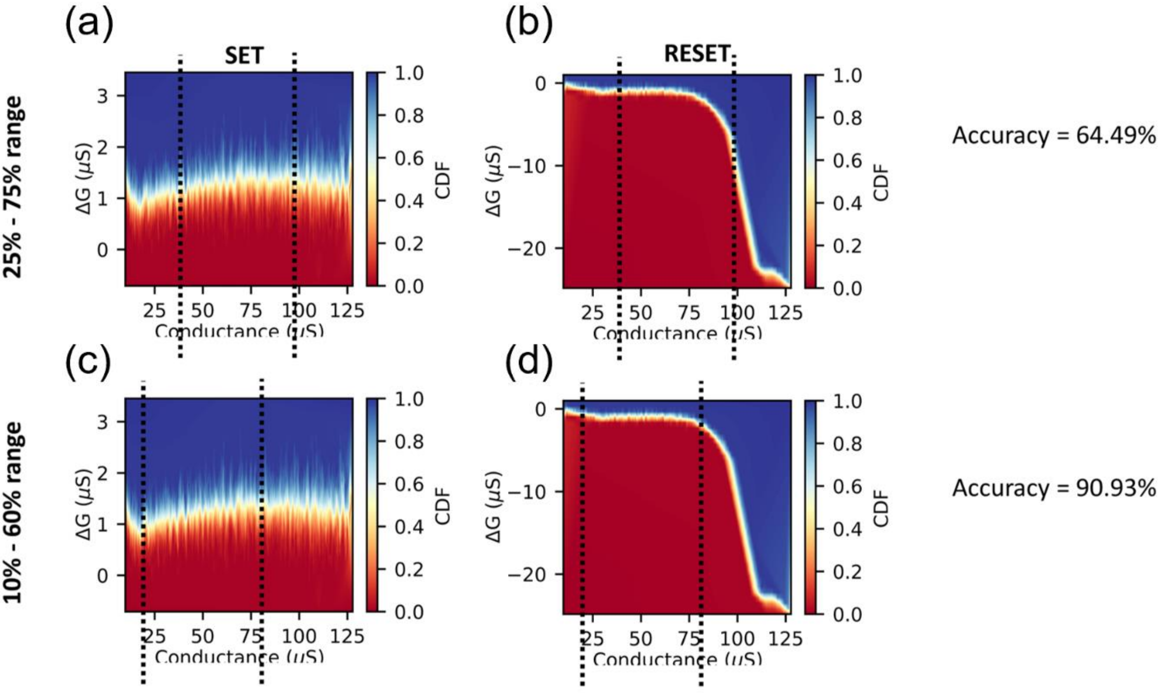

Figure B. 6 eCDF) lookup tables of the conductance change (Δ G) within the 50 cycles of potentiation/depression for the linear pulse scheme as a function of conductance for 20Ar/20O_2 with the (a) and (b) default test provided by CrossSim that uses the 25% to 75% range of the on/off window which revealed a 64.49% accuracy and (c) and (d) adjustment made for 10% - 60% range which resulted on an improved accuracy of 90.93%.

C
APPENDIX

Appendix C contains additional results to the Chapter 5 of this dissertation. In summary, a table is provided summarizing the state of the art on the 1T1M Integration and details on the proposed fabrication procedure, for IGZO 1T1M integration, using the same processing steps and materials are further elucidated. The area-dependent switching of the memristors is confirmed by performing Set and Reset on different device areas and the TFT scaling potential is briefly discussed to clarify on the potential for future miniaturization of cell size. Other known strategies for crosstalk elimination, such as voltage bias schemes, are examined in detail in terms of their results when applied to our IGZO-memristor, for comparison with the proposed 1T1M method. Moreover, the energy consumption of the 1T1M cell during training and inference is compared to the analogous 1M cell. The retention properties of the 1T1M cell are also presented and both memristor and TFT variability is discussed. Finally, the memristor and TFT characteristics before and after peel-off from the polyimide are directly compared.

Table C.1 presents a summary of the literature in 1T1M cells.

Table C.1 Comparison of this work with the state of the art on 1T1M integration.

Year/Ref.	Transistor technology	Memristor structure	Memristor size (μm^2)	Same materials for both devices?	Array size
2014[1]	CMOS	$Cu/HfO_x/Pt$	1.20 x 10^{-1}	N.A.	N.A.
2016[2]	CMOS	$Ta/TaO_x/Pt$	3.14	N.A.	4 x 4
2017[3]	CMOS	$TiN/HfO_2/Al_2O_3/TaOx/TiN/Al$	N.A.	N.A.	128 X 8
2017[4]	CMOS	$TiN/ HfO_2/Ti$	8.00 x 10^{-3}	N.A.	N.A.
2017[5]	CMOS	$Ta/HfO_2/Pd$	1.60 x 10^{1}	N.A.	128 x 64
2018[6]	**Thin-film**	$Pt/Al_2O_3/IGZO/ITO$	3.14 x 10^{5}	**Not all**	**N.A.**
2018[7]	CMOS	$Pt/HfO_2/Ta$	N.A.	N.A.	128 x 64
2018[8]	CMOS	$Ta/HfO_2/Pt$	N.A.	N.A.	128 x 64
2018[9]	**Thin-film**	$Ti/TiO_2/Pd$	2.50 x 10^{1}	**No**	**N.A.**
2019[10]	CMOS	$Pd/HfO_2/Ta$	1.60 x 10^{1}	N.A.	128 x 64
2019[11]	**Thin-film**	$Ag/WSe_2/Ag$	5.00 x 10^{3}	**No**	**N.A.**
2020[12]	CMOS	$TiN/TaO_x/HfO_x/TiN$	0.25	N.A.	128 x 16
2020[13]	**Thin-film**	$TiN/Ti/HfO_2/TiN$	9.00	**No**	**N.A.**
2021[14]	**Thin-film**	Au/Fluoropolymer/Ag	2.50 x 10^{5}	**No**	**N.A.**
This work	**Thin-film**	**Mo/IGZO/Ti/Mo**	**4.00**	**YES**	**4 x 4**

Figure C.1 provides a schematic illustration displaying all the fabrication steps of the amorphous oxide-based 1T1M crossbar divided in layers of deposition.

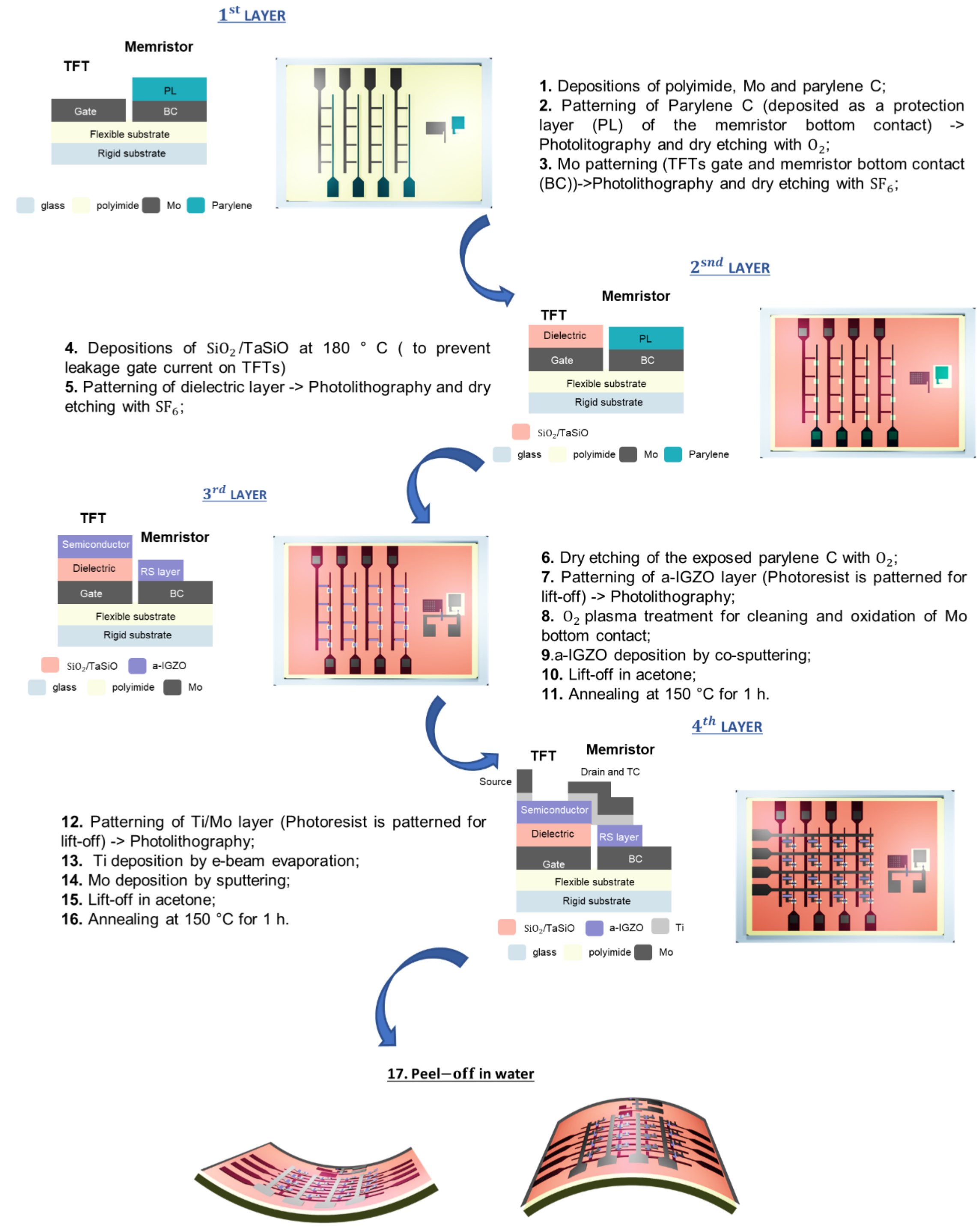

Figure C. 1 Schematic illustration of the fabrication steps of the flexible IGZO-based 1T1M crossbar.

Figure C.2 shows the transfer characteristic in the saturation regime for TFTs with different Ar/O_2 ratio during IGZO deposition. The 20Ar/5O_2 is the only condition with sufficient output current to turn on the memristor. Further details on memristor characteristics with different Ar/O_2 ratio during IGZO deposition can be consulted in our previous work.[15]

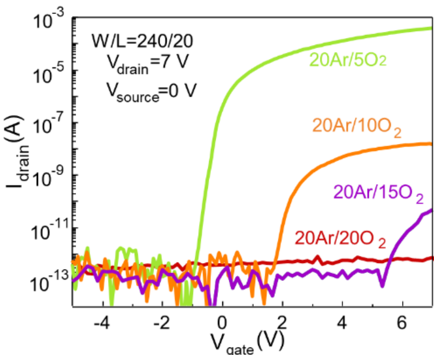

Figure C. 2 IGZO layer optimization for compatibility with both TFT and memristor. Transfer characteristic in saturation regime for TFTs with different Ar/O_2 ratio during IGZO deposition.

Figure C.3(a) shows the I-V characteristics of the a-IGZO memristors with different areas (4, 25, 100 and 900 µm^2), with Set for negative polarities and Reset for positive polarities applied to the top contact. It is clear the smaller the memristor area, the lower the current state and the higher the I_{LRS}/I_{HRS} ratio, presented in **Figure C.3(b)**. I_{LRS}/I_{HRS} ratio was calculated by dividing the LRS-state current by the HRS-state current, extracted from a read process at -0.1 V, applied to the top contact, immediately after the Set/Reset DC sweep.

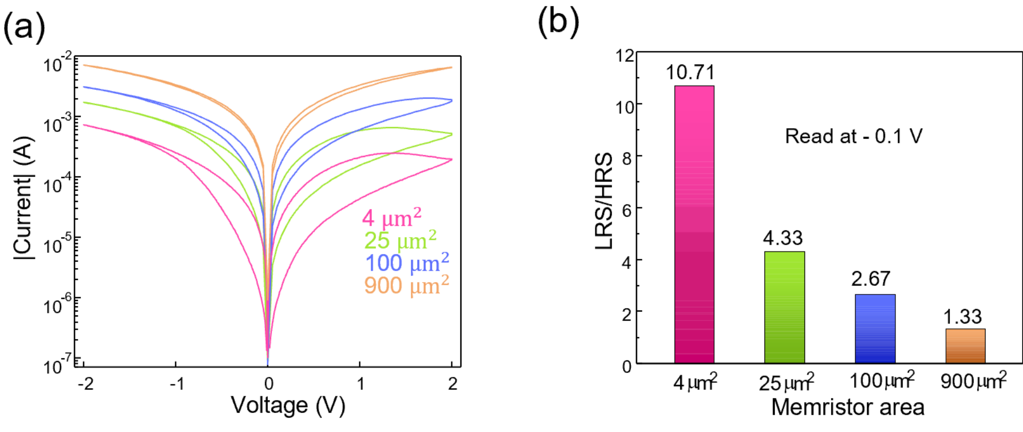

Figure C. 3 Different area memristors and their I_{LRS}/I_{HRS} ratios. (a) I-V characteristics for different area memristors, 4, 25, 100 and 900 µm^2, showing Set and Reset operations for negative and positive DC sweeps, respectively. (b) Respective I_{LRS}/I_{HRS} ratios calculated with current states read at -0.1 V at the top contact after the Set and Reset sweeps.

Figure C4(a) shows the output curves of the integrated TFTs with W/L of 240/20 µm. **Figure C4(b)** presents the transfer curves in the linear and saturation regime for a smaller TFT with W/L of 4/2 µm. The on current with a drain voltage of 5 V reaches 10 µA. If the a-IGZO memristor can be tunned to lower current states by downsizing, then smaller TFTs can also be employed like the 4/2 or smaller, increasing the overall circuit density.

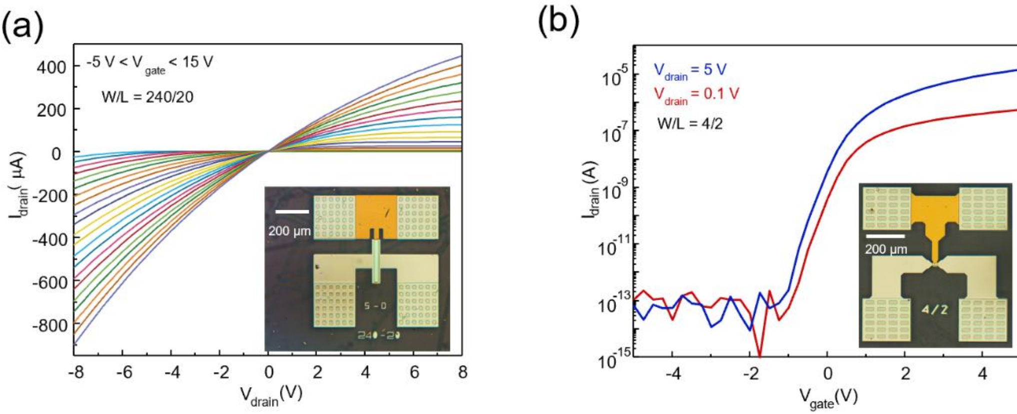

Figure C. 4 TFTs characterization and downsizing. (a) Output characteristic of the integrated TFT with W/L of 240/20 µm with gate voltage from -5 V to 15 V. (b) Transfer curves in the linear (drain voltage of 0.1 V) and the saturation regime (drain voltage of 5 V) of a smaller TFT with W/L of 4/2 µm. Insets are micrographs of the TFTs characterized (scale bar, 200 µm).

Figure C.5 shows our previous proposed pulse scheme for the a-IGZO memristor.[15] It consists of an incremental pulse amplitude and width in each pulse. For the memristors presented in this paper, the potentiation operation starts with a -0.8 V pulse for 1 µs and it linearly increases to the 100th pulse of -2.7 V for 70 µs, and depression starts at the 101st pulse of 1.5 V for 10 µs and ends at the 200th pulse with 2.6 V/ 100 µs, as can be seen in the schematic of **Figure C.5(a)**.

In a passive crossbar composed solely of memristors, a selected cell would behave in a very linear fashion, which is required for ANNs applications. However, the sneak-path current issue would be a major limitation to a physical implementation. To mitigate this problem, the 1/2 and 1/3 voltage bias schemes (VBS) have been proposed.[16,17] **Figure C.5(b)** shows a schematic for implementing these methods and **Figure C.5(c)** presents the experimental results of a single memristor.

Using the 1/2 VBS, the selected cell is biased fully with V Volts at the word line and grounded at the bit line. The remaining word and bit lines are biased with half voltage (V/2). This means that the selected cell is under V bias, the unselected cells are under no bias (V/2-V/2) and some cells are half-selected cells, that either share the word or the bit lines with the selected one, under V/2 bias. For the 1/3 VBS, the selected word line is fully biased, and the bit line is grounded at 0 V. The unselected word lines are biased with a third of the voltage (V/3) and the unselected bit lines are biased at 2/3 V. Therefore, the selected cell is, once again, fully biased, the half-selected cells are under 1/3 V bias, and the unselected cells are under 2/3 V bias.

In **Figure C.5(c)**, the potentiation and depression tests as synaptic weight in percentage are presented. The synaptic weight is the conductance change with each pulse and should be zero for cells not selected for the minimum sneak-path current. Using the 1/2 VBS, the half-selected cells show an increase of the synaptic weight to about half of the selected cell, which means the sneak-path current would still be significantly high and block large scale implementation. While the 1/3 VBS results on the half-selected cells show an increase of 16 % on the synaptic weight which is, in fact, lower. However, the non-selected cells using the 1/3 VBS would not reach the HRS with the depression scheme, which would affect the performance of the entire crossbar.

Therefore, these VBS methodologies are effective in reducing the leakage current on passive crossbars, but they are not sufficient for real-world ANNs applications in which large crossbars are required.

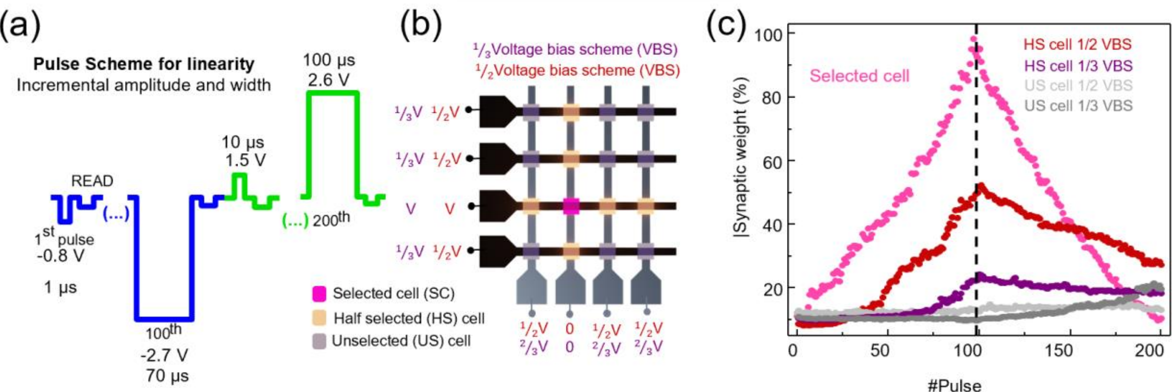

Figure C. 5 Passive crossbar employing the 1/2 and 1/3 Voltage bias schemes. (a) pulse scheme for a linear potentiation (in blue) and depression (in green) of increasing pulse amplitude and width. (b) Schematic of the implementation of 1/2 (in red) and 1/3 (in purple) Voltage bias schemes on passive crossbars highlighting one selected cell in pink, the half selected cells in yellow and the unselected cells in grey. (c) Synaptic weight change in percentage for potentiation and depression tests using the 1/2 and 1/3 voltage bias schemes.

Figure C.6(a) and C.6(b) shows the output of a TFT during the potentiation and depression tests using the described pulse scheme. Since the current output of the TFT is the input current of the memristor, the application of this pulse scheme to a TFT with no memristor connected should result in a stable output during the read pulse. The current should remain unaltered during this phase, enabling a successful control of the memristor input. As can be seen in **Figure C.6(a) and C.6(b)**, the current state during each read step remains unaffected by the previous pulses as required. The memristor current state was read at 0.1 V before the application of the pulse scheme on the 1T1M structure, after potentiation and after depression to validate its successful modulation. In **Figure C.6(c)**, the results can be assessed. The memristor current state starts at 369 nA, it increases to 13.7 µA after potentiation and decreases once more to 355 nA after depression, achieving a 38.59 I_{LRS}/I_{HRS} ratio.

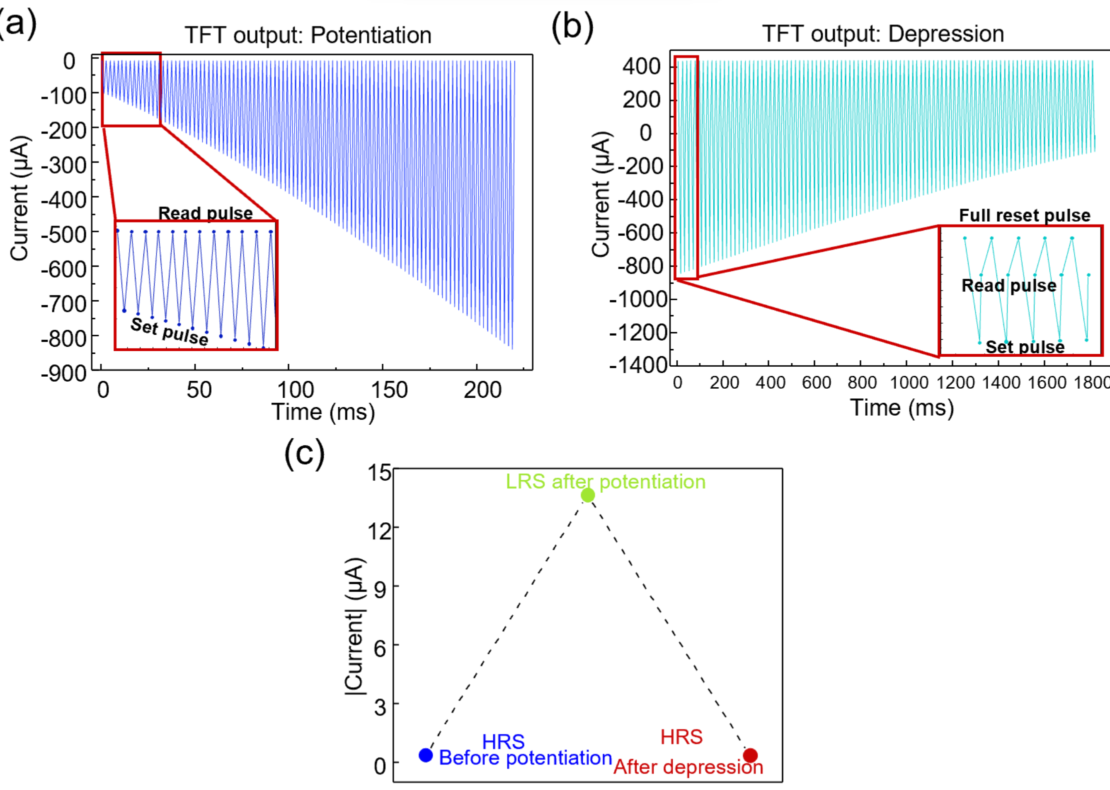

Figure C. 6 Pulse scheme effect on TFT and memristor. Output current of the TFT during the pulse scheme application which corresponds to the input current on the memristor during (a) potentiation and (b) depression. (c) Memristor current state read at 0.1 V before the 1T1M pulse scheme application, after potentiation and after depression displaying a 38.59 I_{LRS}/I_{HRS} ratio.

Figure C.7(a) and C.7(b) presents the energy consumption (E_c) of the 1T1M cell for synaptic pulses and read pulses using the pulse scheme introduced in Figure 5.1 of Chapter 5, respectively. **Figure C.6(c) and C.6(d)** shows the E_c of the correspondent memristor cell without the TFT for synaptic pulses and read pulses using the pulse scheme described in **Figure C.5(a) - Appendix C**. For the calculation, E**quation C.1** was used, according to reference:[18]

$$E_c = V \times I \times t \quad (\mathbf{C.1})$$

V is the voltage applied to the source line for the 1T1M cell and the voltage applied to the memristors top contact for the memristor, I is the current during pulse and t is the synaptic/read pulse width. To program the 1T1M cell to LRS, an energy consumption of 4 µJ is necessary while for the 1M cell only 0.05 µJ would be required. For the reading process at LRS, the 1T1M cell requires 500 pJ and the 1M cell 20 pJ. The 1T1M cell shows an energy consumption of more than one order of magnitude compared to the memristor, due to a slower operation and the need of larger pulses both for synaptic and read pulses.

In **Figures C.7(e) and C.7(f)**, the effect of the TFT W/L on its output current during synaptic and read pulses is presented. A gate voltage of 10 V was used for these tests for a precise comparison with a TFT of smaller W/L which might not stand the 15 V used in the proposed pulse scheme for the read process. The TFT with W/L of 240/20 takes 733 µs and 659 µs to stabilize during a synaptic and read pulse, respectively. As an example, switch-on response of TFTs with W/L of 4/2 is much faster.

Downscaling the memristor would result in lower required current input for its conductance modulation, which in turn would allow for a TFT with smaller W/L to be employed, greatly decreasing the 1T1M cell energy consumption both during training and inference.

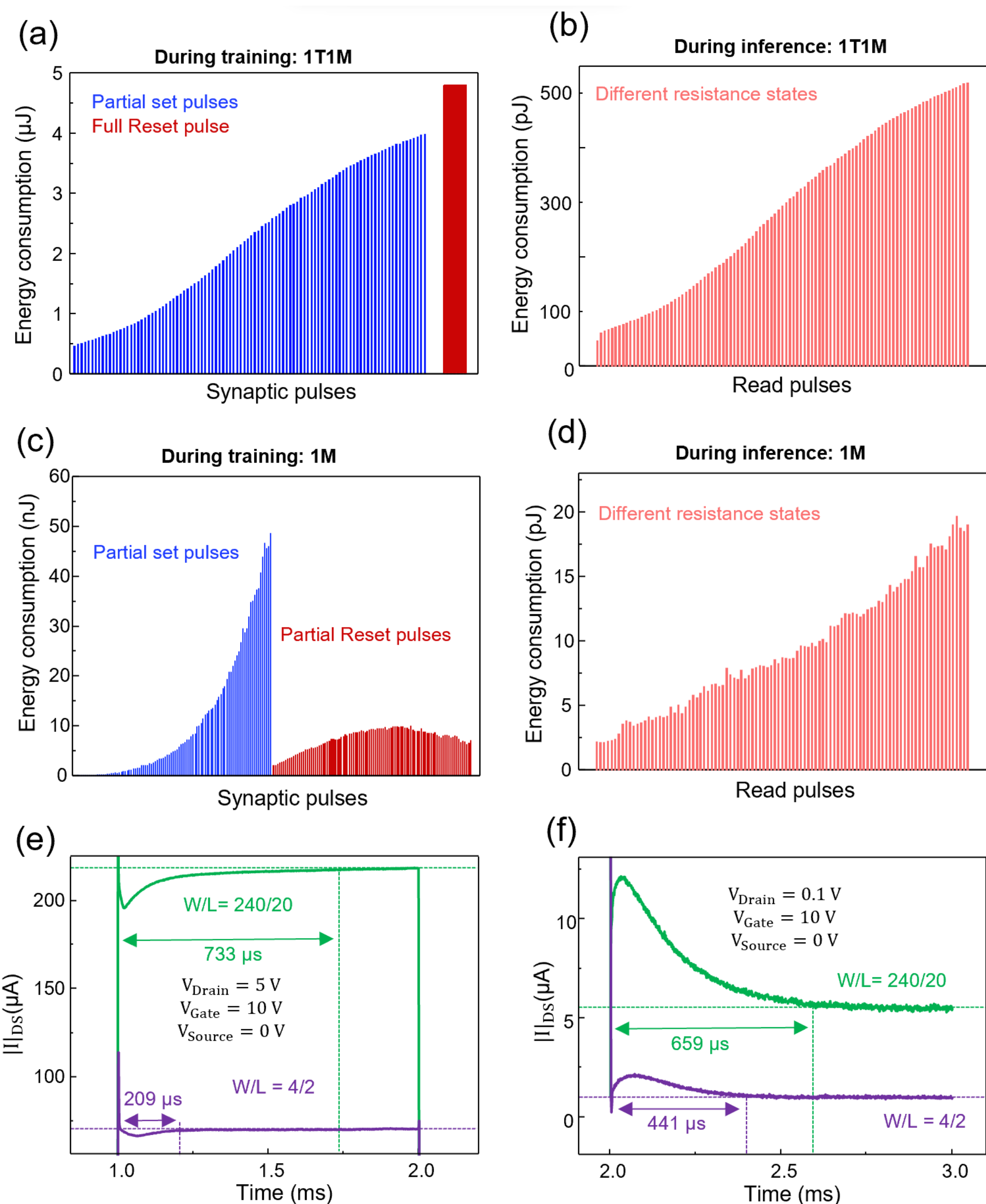

Figure C. 7 Energy consumption analysis. Energy consumption of 1T1M cell during (a) training and (b) inference. Energy consumption of one memristor (1M) cell during (c) training and (d) inference. Effect of TFT W/L on stability of TFT output in time for (e) a synaptic pulse of 10 V at the gate and 5 V at the drain and (f) a read pulse of 10 V at the gate and 0.1 V at the drain.

The retention data for different states of the 1T1M cell is shown in **Figure C.8**. Before each potentiation, a Reset was performed through DC sweep on the memristor of the correspondent cell.

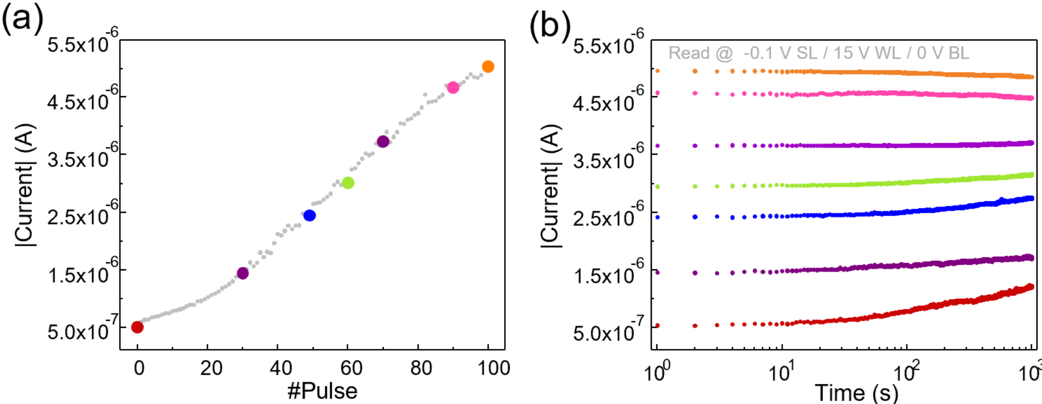

Figure C. 8 Retention characteristics of 1T1M cell. (a) Selected points/number of applied pulses during potentiation for retention test. (b) Retention data for 103 s at each selected point. Read at -0.1 V at the Source Line (SL), 15 V at the Word Line (WL) and 0 V at the Bit Line (BL).

Figure C.9 presents the transfer curves in the linear regime of the individual TFTs as well as the pristine state of the memristors integrated on the crossbars for evaluation of the device-to-device variability.

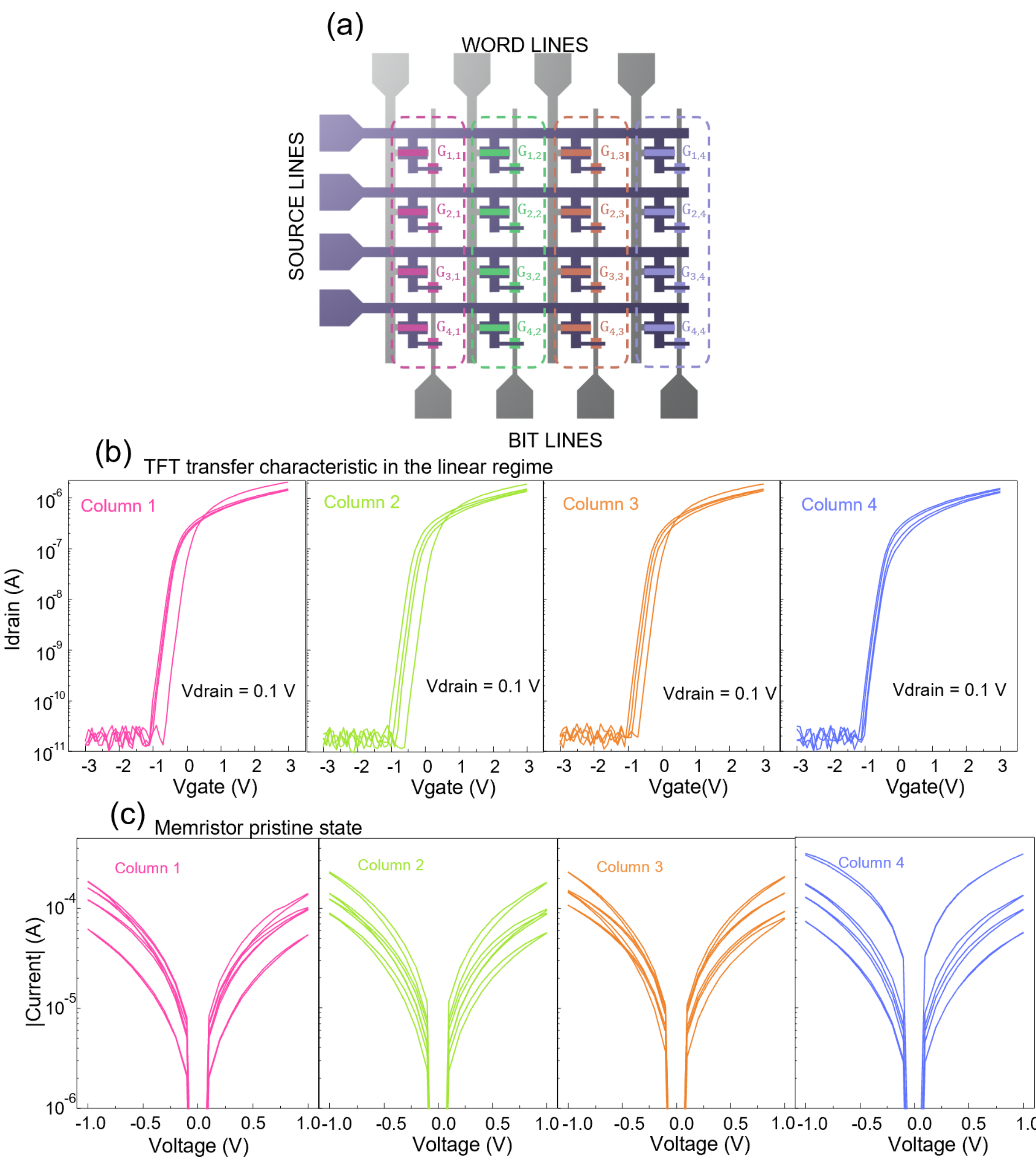

Figure C. 9 Crossbar D2D variability. (a) Schematic illustration of the 4×4 1T1M crossbar exposing word, source and bit lines connections. (b) TFT transfer curves in the linear regime of the individual TFTs present on the crossbar arranged through bit lines. (c) Pristine state of each memristor on the crossbar arranged through bit lines.

Figure C.10 presents the schematic of the vector-matrix multiplications (VMM) test set-up. A Keysight B1500A semiconductor parameter analyzer connected to a Cascade Microtech EPS 150 manual probe station was used. 6 probes were necessary for each test, one on the word line, one on the bit line (output) and 1 for each of the 4 source lines. During measurements, SMU 1 was connected to probe 1 connected to the word line at 10 V. The output on the bit line was biased at 0 V at the probe 6 connected to SMU 4. The input vector [V_{S1}, V_{S2}, V_{S3}, V_{S4}] with V_{S1} = 0.30 V, V_{S2} = 0.15 V, V_{S3} = 0.15 V and V_{S4} =0.30 V was applied to the source lines and changed by multiplying it with an α parameter that was swept uniformly from -1 to 1. Source line 1 was connected to probe 2 and source line 4 to probe 3 and both probes were connected to SMU 2, therefore in short-circuit. SMU 3 was connected to both probe 4 and 5.

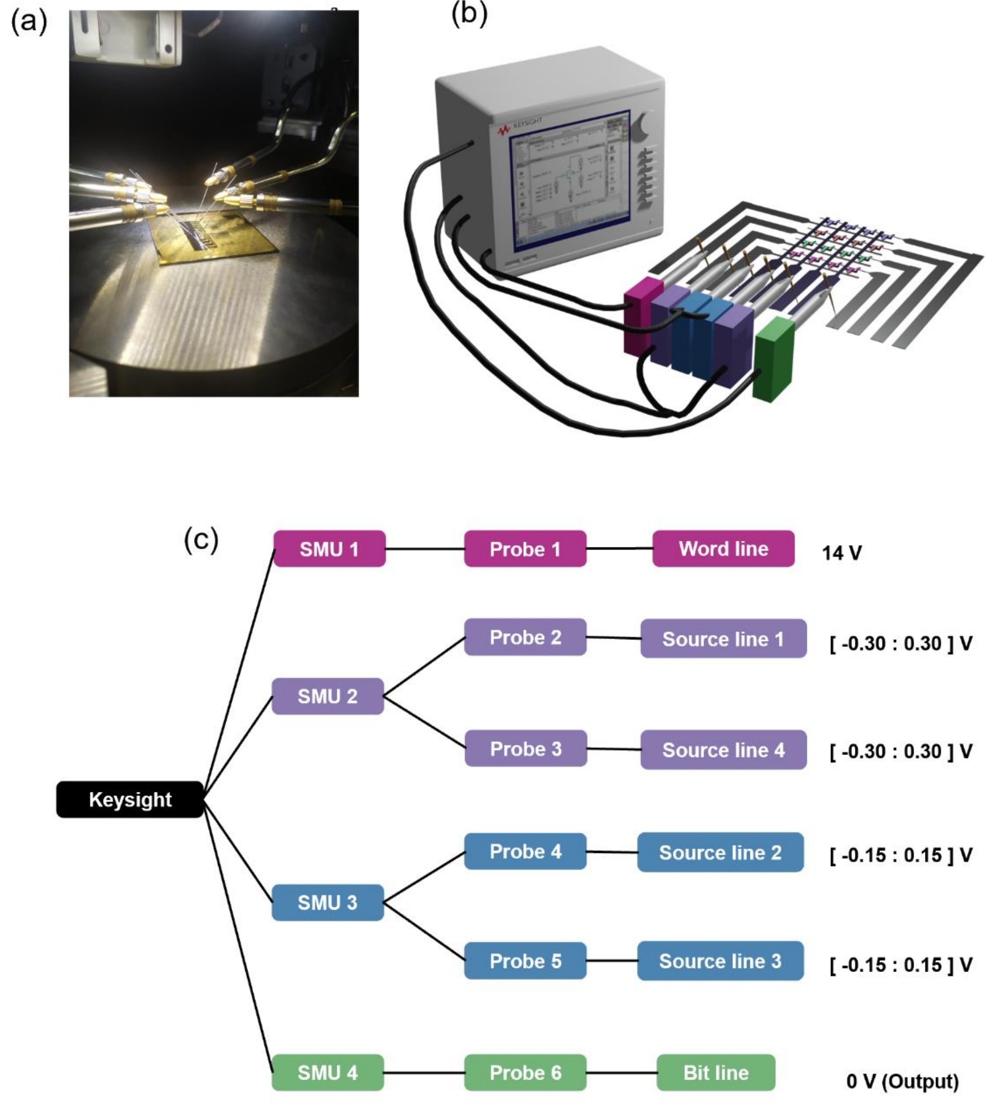

Figure C. 10 Set up for VMM tests. (a) Photograph of the crossbar being measured in the manual probe station. (b) Schematic illustration of the VMM set-up test using the Keysight B1500A semiconductor parameter analyzer connected to the manual probe station connected to the different terminals of the crossbar. (c) Schematic of the connections between the SMUs, probes and crossbar terminals.

Figure C.11 shows the results before and after peel-off and after all bending tests on the individual memristor and TFT. **Figure C.11(a)**, the IV sweeps for set and reset of the memristor presented no performance degradation after all the bending tests. In **Figure C.11(b)**, the TFT transfer curve in the linear regime (V_{drain} = 0.1 V) shows a variation on the turn-on voltage for more positive gate voltages immediately after the peel-off. After all the bending tests, the turn-on voltage decreases again closer to its initial value.

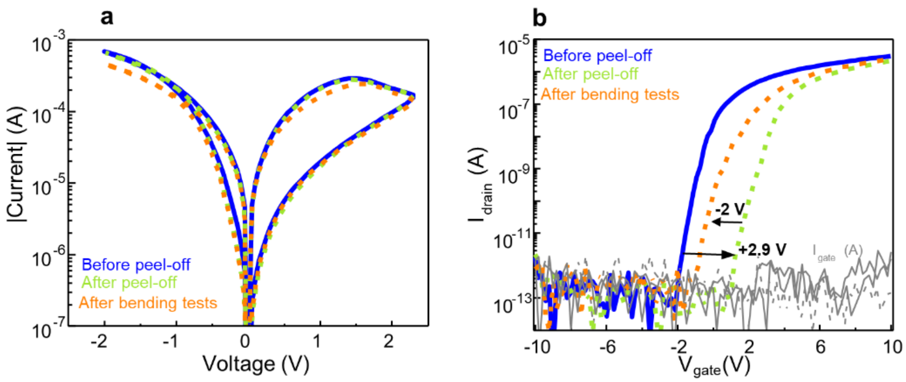

Figure C. 11 Flexible individual memristor and TFT bending. (a) I-V characteristics for the memristor set and reset before and after peel-off and after all bending tests. (b) TFT transfer curve in the linear regime (V_{drain} = 0.1 V) before and after peel-off and after all bending tests.

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D

APPENDIX

Appendix D contains additional results to the Chapter 6 of this dissertation. In summary, In 3d spectrum are analyzed at the top interface with Ti and at the bulk of IGZO to prove the oxygen getter effect of the Ti. The annealing study on the devices fabricated without plasma is presented as well as supporting AFM images. Area-dependency analysis is provided for the Plasma and No Plasma/Annealed devices. Device-to-device variability is presented for memristor with different top contacts in regards to their LRS and HRS and I_{LRS}/I_{HRS} ratio. On the aged devices, the Mo 3D spectrum on exposed Mo in passivated and not passivated aged samples is provided. Further prove on the resistive switching mechanism is provided in the results of retention properties measured in vacuum. Finally, the results on the structures in which thin layers of 3 nm and 5 nm of Al_2O_3 were added at the bottom interface are displayed.

In **Figure D.1(a) and D.1(b)**, the deconvolution of the XPS In 3D spectra can be found, for the Plasma/Annealed sample at etching time of 4500 s, which is related to the Ti/IGZO top interface and at etching time of 8000 s, which corresponds to the bulk IGZO film. Two contributions can be identified: metallic In^0 and oxidized In^{3+}. It is clear that in the interface there is more metallic In^0 due to the "oxygen getter" effect of Ti. This is further evidenced by the graph presented in **Figure D.1(c)**, where this information is summarized for various etching times. From 7500 s onwards the contribution of oxidized In^{3+} increases to almost 100 %, indicating a movement away from the interface region.

Regarding the bottom interface (IGZO/MoO_x), an example of the fittings performed on the Mo 3D spectrum is depicted in **Figures D.1(d) and D.1(e)**, for the Plasma/Not Annealed and the Plasma/Annealed samples, respectively. In order to allow for a direct comparison of the spectrum, and disregard any contribution of the monoatomic Ar, the first etching time in which the Mo 3D detected any signal was chosen from the data of the depth profile. The fittings were done according to Baltrusaitis *et al.* (DOI: 10.1016/j.apsusc.2014.11.077). There are contributions of Mo^0, Mo^{4+}, Mo^{5+} and Mo^{6+} in both structures. However, it is noticeable that the annealed sample has more metallic Mo^0 and less Mo^{6+}.

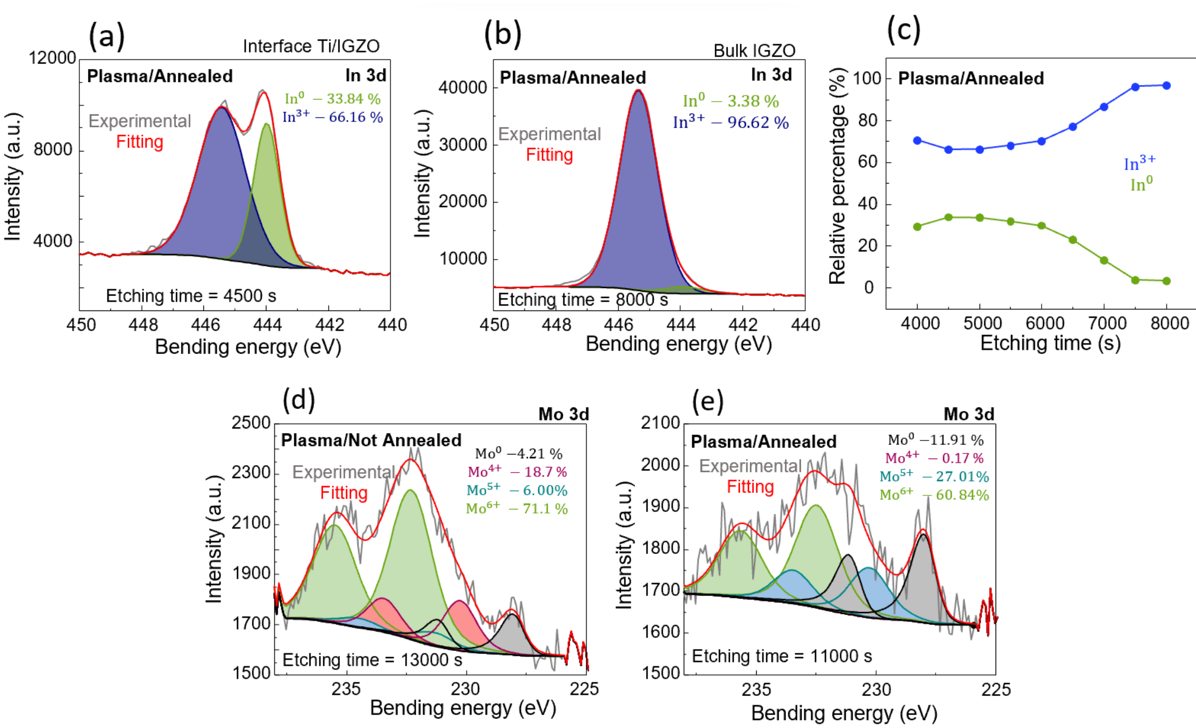

Figure D. 1 (a) and (b) Deconvolution of XPS spectrum through depth profiling with monoatomic Ar of In 3d at the Ti/IGZO interface and at the bulk IGZO, respectively, in the structure with plasma and annealed. (c) Relative percentages of metallic In and oxidized In at the top interface and in the bulk. (d) and (e) Deconvolution of XPS spectrum through depth profiling with monoatomic Ar of Mo 3d at the bottom interface for the structures not annealed and annealed, respectively.

In **Figure D.2**, the analysis of the annealing effect on the No Plasma sample is displayed. The pristine state (**Figure D.2(a)**), of the memristor with no annealing is very similar to the pristine of the sample with plasma also without annealing. However, with the annealing step, the No Plasma device not only lose the rectification but also become more conductive in both the forward and the reverse polarity direction. The loss of rectification is well explained by the expected structure relaxation of the IGZO film to accommodate different concentrations of defects, which reduces the Schottky barrier height/width. No relevant differences are found in the XPS depth profile of the No Plasma/Not annealed sample (**Figure D.2(b)**) compared with the No Plasma/Annealed or even with the Plasma samples. However, Mo^{6+} is drastically decreased in the No Plasma devices (**Figure D.2(c)**).

As in the Plasma devices, the No Plasma memristors without annealing suffer a forming step, shown in **Figure D.2(d)**. This forming process can be eliminated by the annealing step. In **Figure D.2(e)**, the full Set and gradual Reset is presented for the device with No Plasma/Annealed, with the red curve being the first measurement corresponding to the pristine. It can be concluded that the No Plasma/Annealed device is the low-resistance state (LRS) when in equilibrium (also the pristine). If all of the so far described devices are compared, the I_{LRS}/I_{HRS} ratio is higher for the No Plasma/Annealed procedure. Variability on the I_{LRS}/I_{HRS} ratio does not seem to be impacted by the plasma treatment. Once again, due to the filament creation in the Not Annealed sample, recognizable from the required electroforming step, device-to-device variavility is very much higher in the No Plasma/Not Annealed samples, which can be reduced by the annealing step.

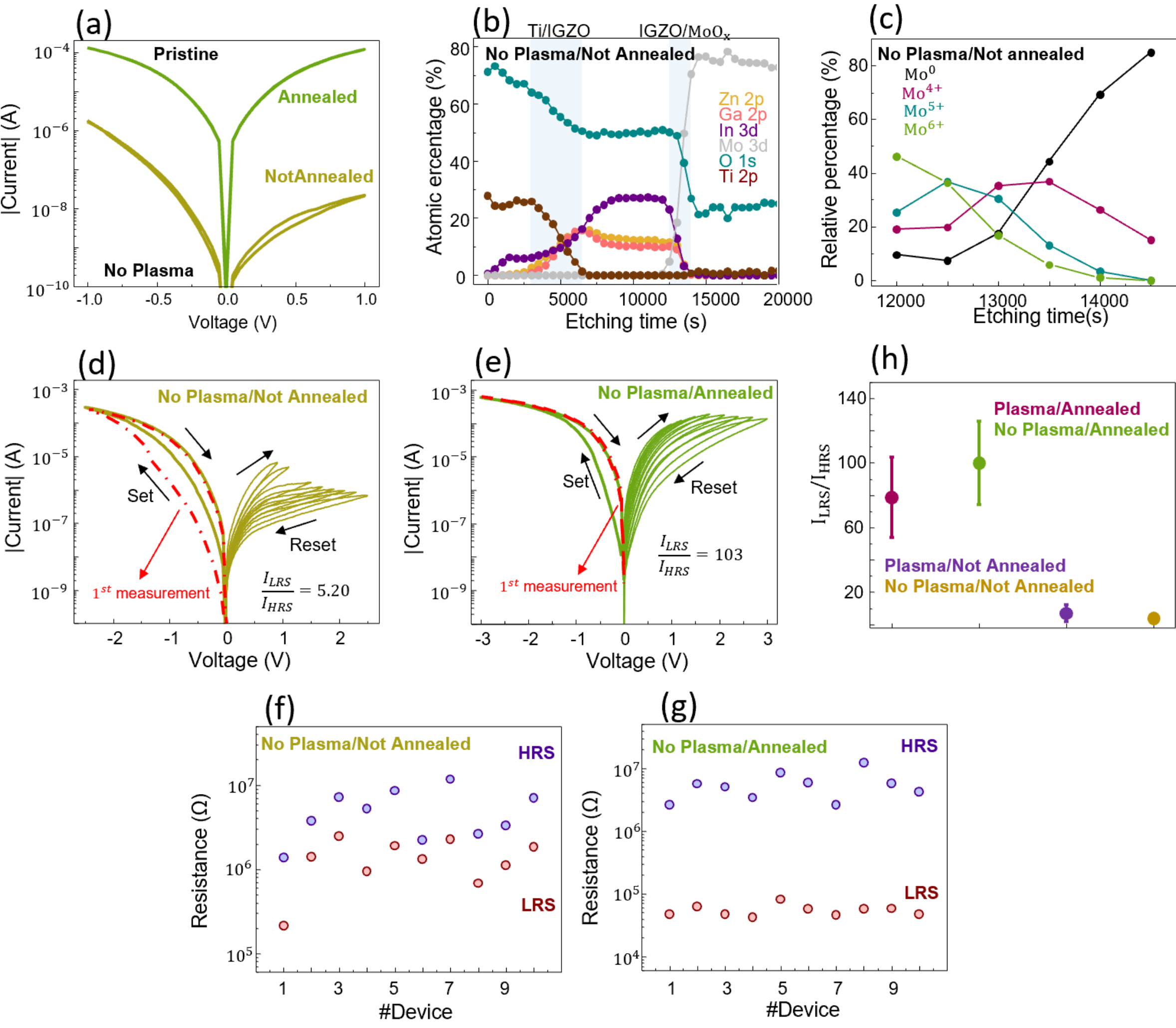

Figure D. 2. (a) I-V characteristic of the pristine state, between -1 V and 1 V applied to the top electrode, of the No Plasma/Not Annealed and No Plasma/Annealed memristors. (b) XPS argon cluster depth profiling through Ti/IGZO/MoO_x/Mo structure on the No Plasma/Not Annealed structure. (c) Relative percentage of the deconvoluted Mo 3d spectra contributions at the bottom interface for the No Plasma/Not Annealed structure. I–V characteristic of full Set and gradual Reset for the (d) No Plasma/Not Annealed and (e) No Plasma/Annealed memristors. D2D variability presented for 10 devices of (f) No Plasma/Not Annealed and (g) No Plasma/Annealed memristors. (h) Mean On/Off ratio and variability of all studied 4 memristor structures.

In **Figure D.3**, the AFM 3D image of the IGZO surface is presented displaying very low RMS roughness of 0.461 nm, which indicates a smooth interface with the Ti/Mo top electrode.

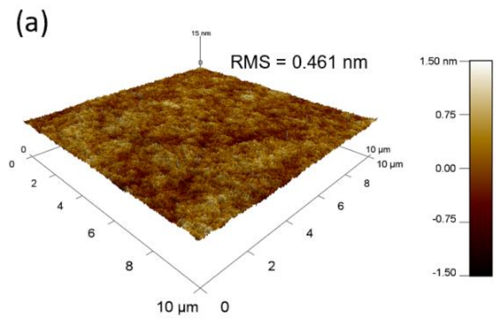

Figure D. 3 AFM 3D image of the IGZO surface.

The area-dependent switching can be further confirmed in **Figure D.4**. Three device areas are shown for the I-V Set and Reset of the Plasma/Annealed device structure (**Figure D.4(a)**) and it can be seen the LRS and HRS increasing. The I_{LRS}/I_{HRS} ratio also seems to decrease with area-scaling. This is because, due to the MoO_x layer, voltage above 3 V cannot be applied because it causes oxide soft breakdown- exemplified in **Figure D.4(b)**. Therefore, V_{Set} and V_{Reset} cannot accompany the area-scaling, gradually reducing the I_{LRS}/I_{HRS} ratio. On the contrary, the No Plasma/Annealed device allows for V_{Reset} to be progressively higher with increasing device area. In fact, if V_{Reset} is maintained at 3 V for all device areas, Reset failure starts to be noticeable, as in **Figure D.4(d)** for a 10000 μm^2 device, since the voltage is not enough to perform Reset. It is not clear why the MoO_x is different for the Plasma and the No Plasma devices and why it results differently in the Set and Reset characteristics. It can be related to the Mo^{6+} quantity and/or due to different densities/thicknesses. Both types of devices show a linear fit on the resistance dependency to the device size on both LRS and HRS, as displayed in **Figures D.4(e) and D.4(f)**.

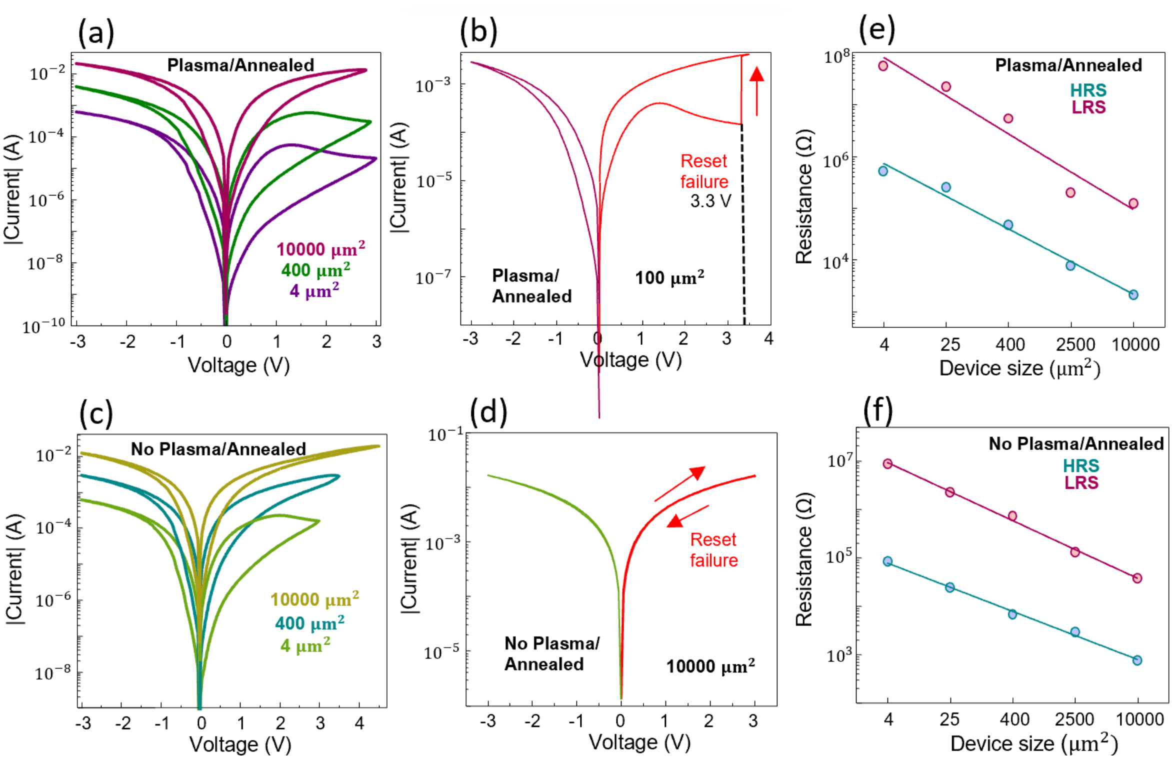

Figure D. 4 I–V characteristic of full Set and full Reset for different device areas for the (a) Plasma/Annealed and the (c) No Plasma/Annealed memristor structure. (b) Reset failure for a 100 μm^2 device with Plasma/Annealed procedure, due to V>3 V. (d) Reset failure for a 1000 μm^2 device with No Plasma/Annealed procedure, due to V=3 V. Linear fitting of the LRS and HRS dependence of device size of the (e) Plasma/Annealed and the (f) No Plasma/Annealed memristor structure.

In **Figure D.5(a)**, device to device variability on the LRS and HRS for memristors with different top contacts can be consulted. 10 devices of each structure were characterized, and the Plasma/Annealed procedure was chosen for this study. The mean I_{LRS}/I_{HRS} ratio and deviation is displayed in **Figure D.5(b)**. The devices without Ti as interlayer show lower I_{LRS}/I_{HRS} ratio of less than 40 due to a lower quantity of VOs in the IGZO, that can then take part in the resistive switching process.

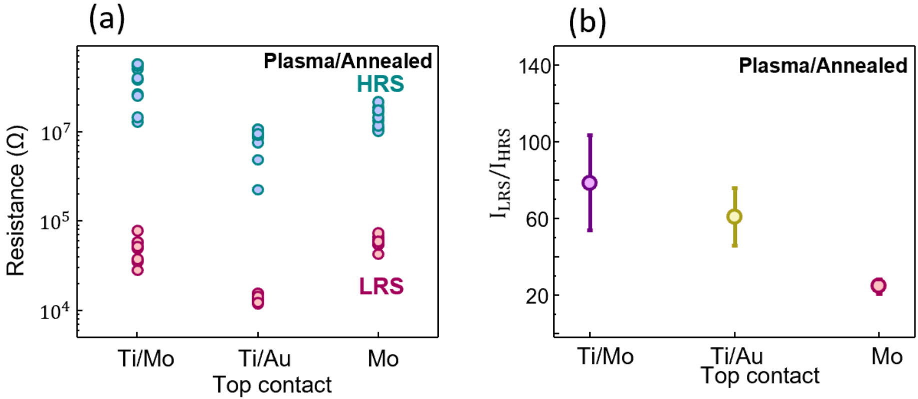

Figure D. 5 (a) D2D variability presented for 10 devices of each memristor structure with different top electrodes (Ti/Au Ti/Mo and Mo) and (b) correspondent mean On/Off ratio.

The Mo 3d emission was recorded for both non-passivated and passivated samples (**Figure D.6(a) and D.6(b)**, respectively). Once again, fittings were done according to Baltrusaitis *et al.* [Doi: 10.1016/j.apsusc.2014.11.077]. Both samples contained mainly Mo^{6+} and some Mo^{5+} and M^{4+}. The major difference is that only the passivated samples showed metallic Mo^{0}. This is likely related to a reduced thickness of the oxidized molybdenum surface layer. Using the Hill equation [DOI: 10.1016/0009-2614(76)80496-4] and inelastic mean free paths from TPP-2M, a Mo oxide thickness of 4 nm was calculated for the passivated sample, whereas this value was 7.5 nm or higher for the non-passivated sample. Using an aperture, the analysis area was reduced to a diameter of about 100 µm (**Figure D.6(c)**) and the elemental composition of the exposed Mo contact pads of the passivated samples was calculated, together. These values are shown in **Table D.1**, together with the elemental quantification of the parylene surface.

Table D. 1 Elemental composition of the exposed Mo contact pads and the parylene of the passivated samples.

%At. Conc.	Mo 3d	C 1s	F 1s	O 1s	Si 2p	Cl 2p
on Mo contact pad	8.89	48.98	1.44	38.30	2.39	-
on Parylene	-	73.88	1.21	19.41	2.06	3.43

The elemental surface quantification shows that no chlorine was detected on the Mo surface. However, both on the Mo and the Parylene surface, fluorine was found, as can be seen in **Figure D.6(d) and D.6(e)**. Although the reactive ion etching was done with oxygen plasma, fluorine is a known contaminant in chambers that are used also with fluorine-containing etchants [Doi: 10.1002/admi.202000264]. It is suspected that the presence of fluorine at the molybdenum surface hinders the surface oxidation of Mo during storage in ambient conditions.

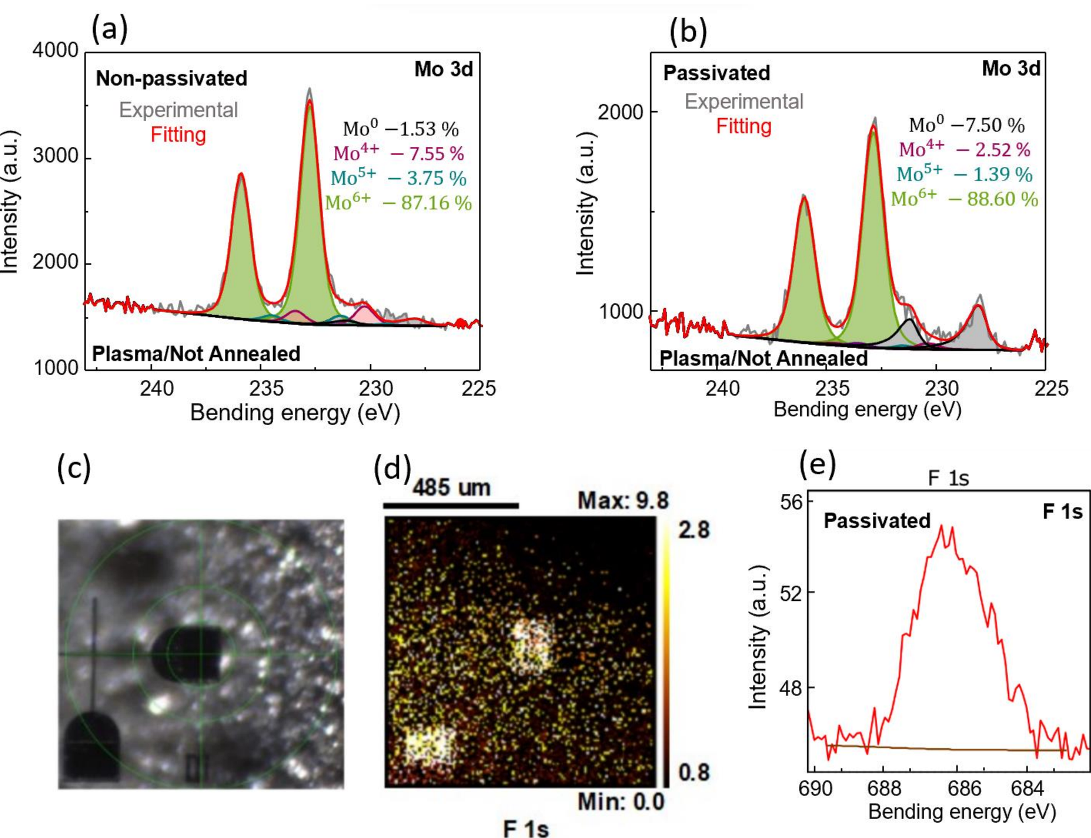

Figure D. 6 Deconvolution of XPS spectrum acquired from the surface of exposed Mo in (a) non-passivated and (b) passivated with parylene-C aged devices. (c) Photography of the aperture to ensure the analysis area was reduced to a diameter of about 100 µm (d) Photoelectron imaging of the F 1s emission in the region of a passivated cross-point device. (e) XPS spectra acquired from the surface of exposed Mo in the passivated sample for binding energies correspondent to F 1s.

In **Figure D.7(a) and D.7(b)**, the retention properties for LRS and HRS in air and in vacuum can be compared for the Plasma/Annealed and the No Plasma/Annealed devices. It can be seen that the relaxation decay is lower in vacuum for the Plasma device since its equilibrium state is the HRS. Contrary, given that the equilibrium state of the No Plasma device is the LRS, vacuum does not seem to affect the retention properties.

The extrapolation of the fitting on the experimental data of LRS and HRS is presented in **Figure D.7(c)** for the devices without Al_2O_3 as oxygen diffusion suppressing layer. The stretched exponential equation was used with one characteristic relaxation parameter (τ) for HRS, as in:

$$\varphi(\mathrm{t}) = I_0 \exp\left[\left(\frac{t}{\tau}\right)^{\beta}\right] \qquad (\mathrm{D.1})$$

where φ(t) is the relaxation function, τ is the characteristic relaxation time, I_0 is initial current state, and β is the stretch index ($0 < \beta < 1$). For the LRS, two characteristic relaxation time parameters were used (τ_1 and τ_2), to achieve the best possible fitting, as in:

$$\varphi(\mathrm{t}) = I_0 \exp\left[-\left(\frac{t}{\tau_1}\right)^{\beta}\right] + I_0 \exp\left[-\left(\frac{t}{\tau_2}\right)^{\beta}\right] \qquad (\mathrm{D.2})$$

By the extrapolation of the fittings, it is found that the equilibrium state (when LRS meets HRS) is encountered earlier in these devices (Plasma and No Plasma/Annealed without Al_2O_3). This suggests that Al_2O_3 is delaying the relaxation of the programmed states which is another evidence of the resistive switching being related to ionic movement.

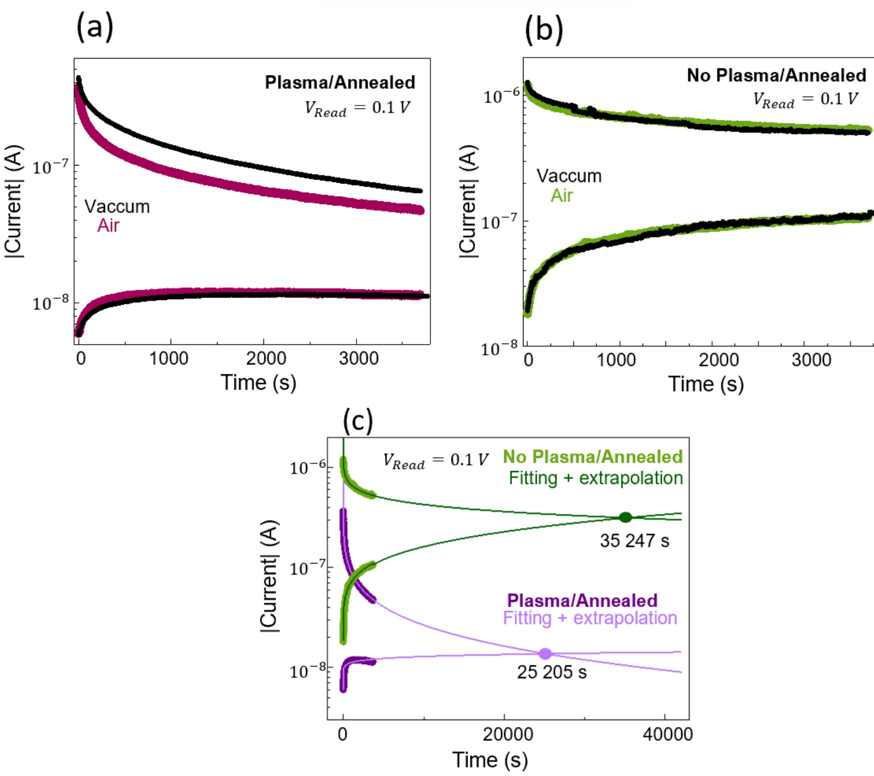

Figure D. 7 Comparison of retention properties of LRS and HRS in air and in vacuum for (a) Plasma/Annealed and for the (b) No Plasma/Annealed devices. (c) Extrapolation of the fitting on the experimental data on retention of LRS and HRS to discover the equilibrium state of the memristors and the time at which LRS meets HRS for the Plasma/Annealed and No Plasma/Annealed devices.

Devices with 3 and 5 nm of Al_2O_3 were also fabricated to confirm the optimized thickness for retention. The results are depicted in **Figure D.8**. 3 nm of Al_2O_3 is already too thick of a layer since it shifts the resistive switching behaviour to filamentary, proven by the typical random telegraphic noise (RTN) apparent in the retention measurements. RTN decreases the operational I_{LRS}/I_{HRS} ratio because of the extensive fluctuations in the read current, which is not ideal and should be avoided. [Doi: 10.1186/s11671-020-03299-9]. Accordingly, with 5 nm of Al_2O_3 it is completely impossible to see any resistive switching behaviour.

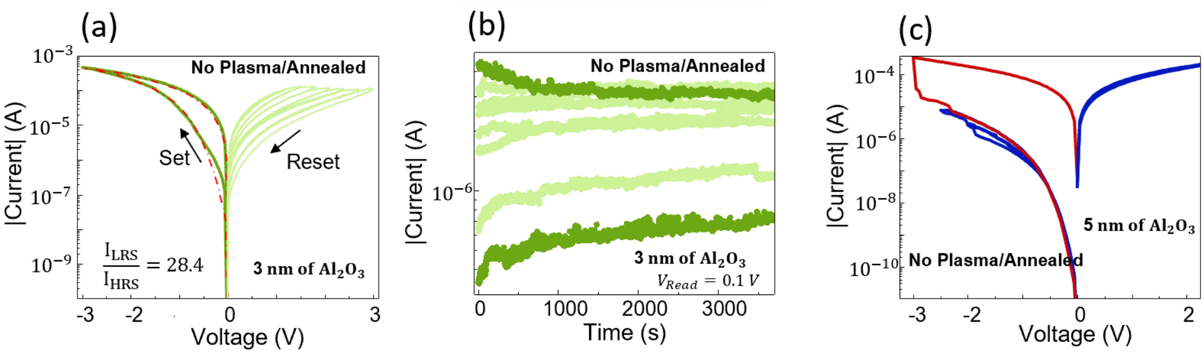

Figure D. 8 (a) I–V characteristic of full Set and gradual Reset and (b) correspondent retention properties recorded for 1 hour at 0.1 V after 8 programmed states via I-V sweep with different Reset stop voltages for the No Plasma/Annealed memristors with 3 nm of Al_2O_3. (a) I–V characteristic of the No Plasma/Annealed structure with 5 nm of Al_2O_3 displaying leakage current.

E

APPENDIX

Appendix E contains additional results to the Chapter 8 of this dissertation. In summary, the Ti 2p XPS spectra from the IGZO/Ti/Au interface is presented to prove oxidation of the Ti by extracting O ions from the IGZO. The O 1s spectra is also shown for direct comparison of VOs quantity in the bulk doped IGZO film and the doped IGZO/Ti/Au interface. On the ITO top electrode, additional results are presented namely, the transient response showing photocurrent under V_{Read} of 0.1 V, I-t showing the photoresponse of the device with doped and not doped IGZO and the electrical Reset operation. On the optimized device with IGZO:H and Ti/Au as top electrode, the studies on device size, C2C and D2D variability are provided. Finally, different current states are shown to be achieved by increasing light power, irradiation time and pulse frequency for green and UV lights. Transitions from STM to LTM are shown by increasing irradiation time by fittings with the Kohlrausch stretched exponential function. A table is also provided for comparison of device size and energy consumption of the proposed optimized device with the state-of-the-art synaptic optoelectronic devices for visible light detection.

In **Figure E.1**, the atomic force microscope (AFM) image of the Ti/Au film with 7 nm is presented showing low root mean square (RMS) roughness of 402.2 pm.

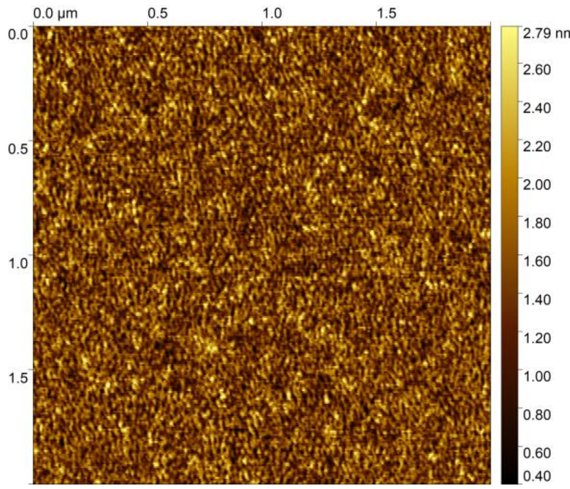

Figure E. 1 AFM image of Ti/Au surface.

In **Figure E.2**, the Ti $2p_{3/2}$ XPS spectra is shown. The titanium oxidation is confirmed by the Ti $2p_{3/2}$ binding energy at 458.8 eV. Ti reacts with the IGZO layer by removing oxygen ions increasing VOs concentration at the interface.

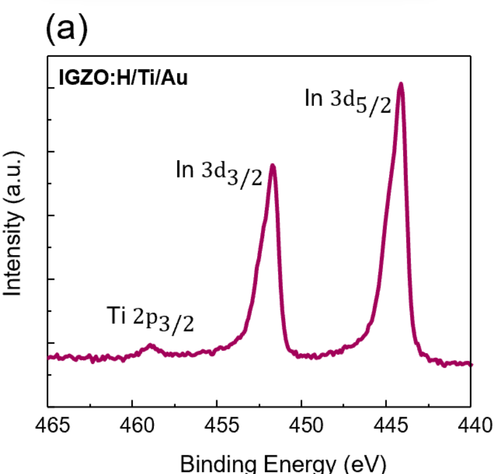

Figure E. 2 Ti 2p XPS spectra

In **Figure E.3**, the transient response for 10 s of illumination, followed by 30 s in the dark, of the Mo/IGZO/ITO device with a V_{Read} of 0.1 V is presented. There is no response to red light. For the other wavelengths, I_{light}/I_{dark} ratios of 2.8, 2.3 and 1.2 are achieved for 365, 405 and 505 nm irradiation, respectively. Higher I_{light}/I_{dark} ratios are accomplished for a V_{Read} of -0.5 V, as discussed in Chapter 8 of this dissertation. However, the higher voltage applied forces electrons into VOs decreasing the photocurrent during illumination and fastening the PPC decay. For a V_{Read} of 0.1 V this is solved, and the photocurrent continues to slightly increase during illumination. The reason why the photocurrent does not increase during irradiation as much as in the Ti/Au devices lies in the transmittance of the top electrodes. Since ITO is more transparent than the Ti/Au, the light intensity reaching the IGZO layer is higher and therefore the photoresponse is faster. The PPC decay is still fast, but this could be due to the very low I_{light}/I_{dark} ratios. Moreover, the I_{dark} is more than 1 order of magnitude higher for the ITO device than for the Ti/Au device for the same V_{Read}.

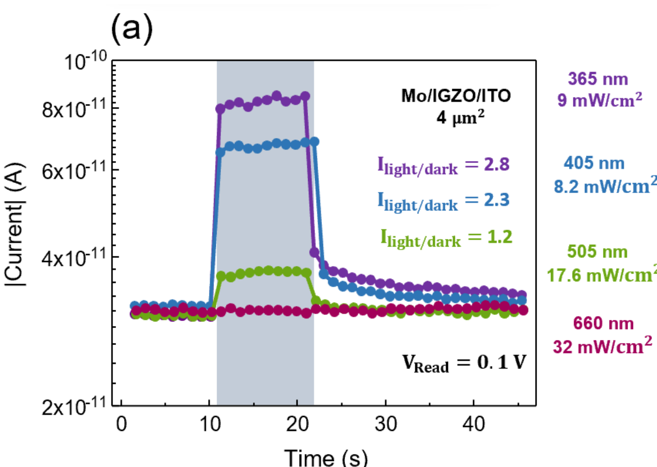

Figure E. 3 Transient response of the Mo/IGZO/ITO device for 10 s of illumination followed by 30 s in the dark with V_{Read} of 0.1 V for different wavelengths.

In **Figure E.4**, the O1s spectra is shown for the bulk hydrogen-doped (H-doped) IGZO film and the H-doped IGZO/Ti/Au interface. The peaks were fitted with a Gaussian-Lorentzian (G-L) function and a Shirley background subtraction. Similarly to the undoped IGZO results presented in **Figure 8.1** of Chapter 8, the VOs percentage increases drastically from 34.6% to 67.7% at the interface with Ti/Au. This result confirms the Ti oxygen getter effect.

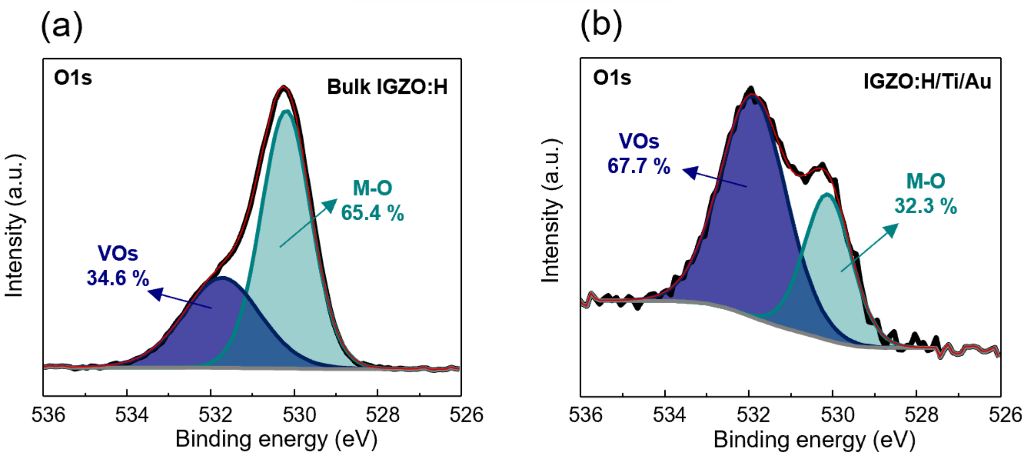

Figure E. 4 (a) and (b) Fitting of O 1s XPS spectra displaying the oxygen vacancies (VOs) percentage compared to the metal-oxygen (M-O) bonds percentage for the doped-IGZO bulk film and the doped-IGZO/Ti/Au interface, respectively.

In **Figure E.5**, the valence band spectrum of the H-doped IGZO film is presented, used to calculate the valence band maxima (VBM) of 2.66 eV determined by linear extrapolation of the leading edge of the spectrum. This presents a decrease of 0.08 eV compared to the undoped IGZO film, which means the carrier concentration has decreased 22 times with the doping (Boltzmann approximation).

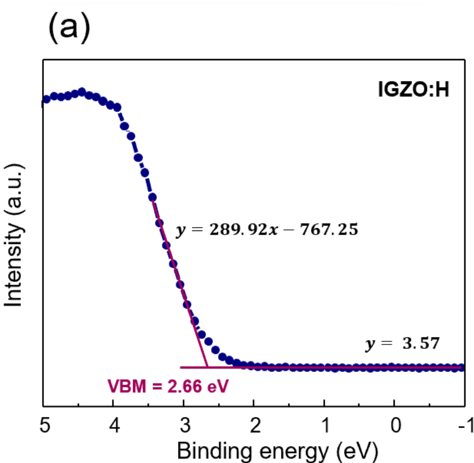

Figure E. 5 Valence band spectra of the bulk IGZO:H film, used to calculate the valence band maxima (VBM).

In **Figure E.6**, the H-doped IGZO device with ITO as top contact is analyzed. **Figure E.6(a)** shows the I-V characteristic in the dark, between -0.5 and 0.5 V, of the undoped device and the doped device. The conductance state is substantially increased, especially for negative polarities which means the I_{dark} is increased with doping. This can be related to H diffusion to the ITO which would increase the conductance of the top contact. In **Figure E.6(b)**, the transient response of the optoelectronic memristor can be found for 365, 405 and 505 nm wavelength irradiation. I_{light}/I_{dark} ratios of 11.6, 6.5 and 2.2 can be distinguished, respectively, which is not an improvement in relation to the undoped-device.

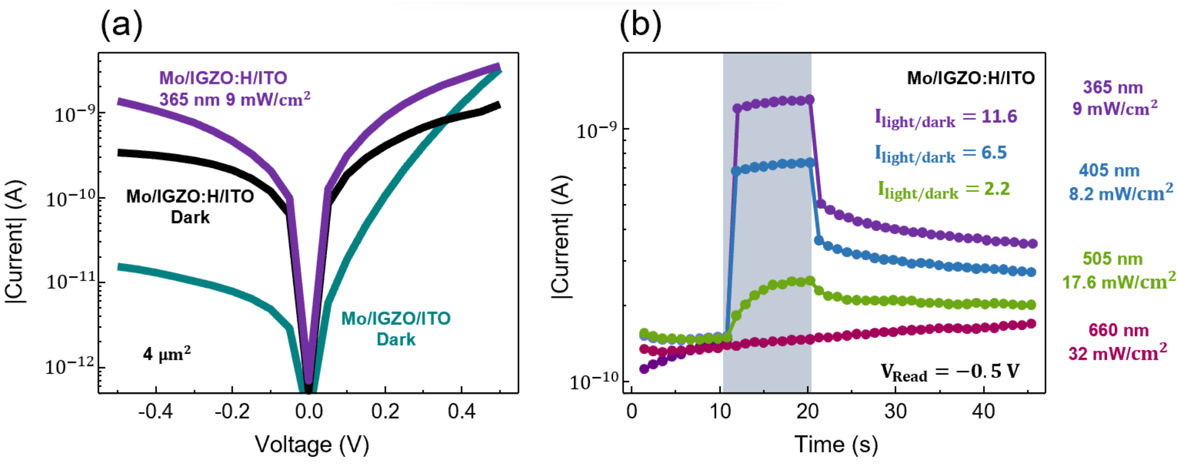

Figure E. 6 (a) Comparison of the I-V characteristic in the dark of the IGZO and the H-doped IGZO devices, with ITO as top contact. (b) Transient response with V_{Read} of -0.5 V and 10 s of irradiation followed by 30 s in the dark of the H-doped device with ITO as top contact for 660, 505, 405 and 365 nm illumination.

In **Figure E.7**, H-doped with Ti/Au as top contact devices with different areas are analyzed. The I-V characteristic comparison in the dark can be consulted in **Figure E.7(a)** for devices with 4, 25, 100, 400, 2500 and 10000 μm². In **Figure E.7(b)**, the summary of the I_{dark} and I_{light} for 505, 405 and 365 nm wavelength illumination is presented in regard to the transient results shown in **Figure E.7(c)**. A steady increase of all mentioned currents is noted with increasing memristor size. However, the I_{light}/I_{dark} ratio is greatly reduced. Green sensitivity is also gradually lost as the memristor size increases. In fact, the 10000 μm² device shows no green detection and reduced ratios of 5 and 3 for UV and blue illumination, respectively.

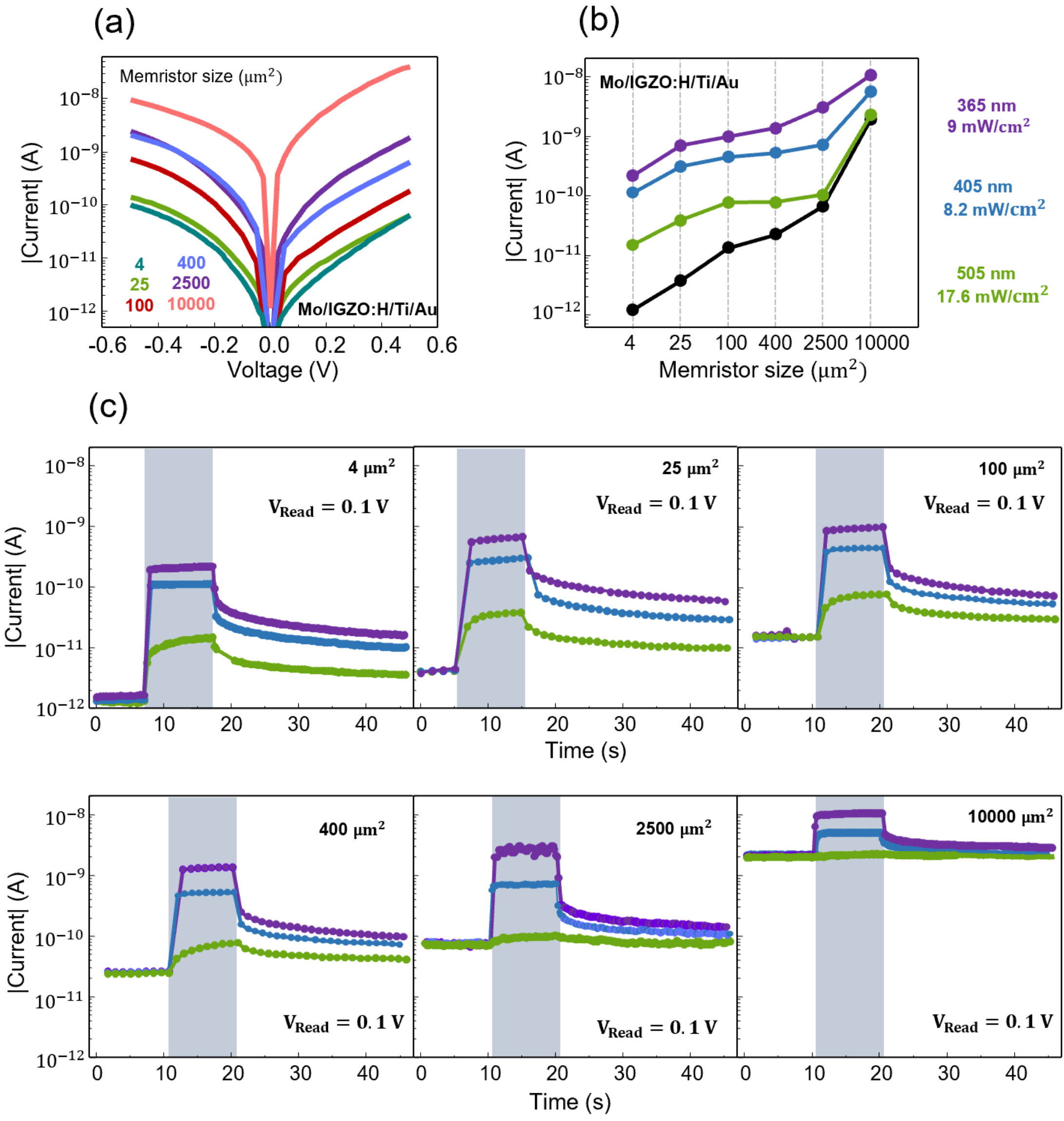

Figure E. 7 (a) I-V characteristic in the dark from -0.5 to 0.5 V for Mo/IGZO:H/Ti/Au devices with different sizes. (b) I_{dark} and photocurrents after 10 s of illumination with 365, 405 and 505 nm wavelength for devices with different sizes and (c) Transient response of devices with different sizes for 10 s of illumination followed by 30 s in the dark with V_{Read} of 0.1 V for different wavelengths.

In **Figure E.8**, the transient response to optical and electrical inputs on the doped memristor with ITO as top contact can be evaluated. Increasing current states are achieved with more energetic wavelengths. The Reset electrical pulses are also discriminated. The higher the current state, the higher the voltage or the longer the pulse required to perform a full Reset.

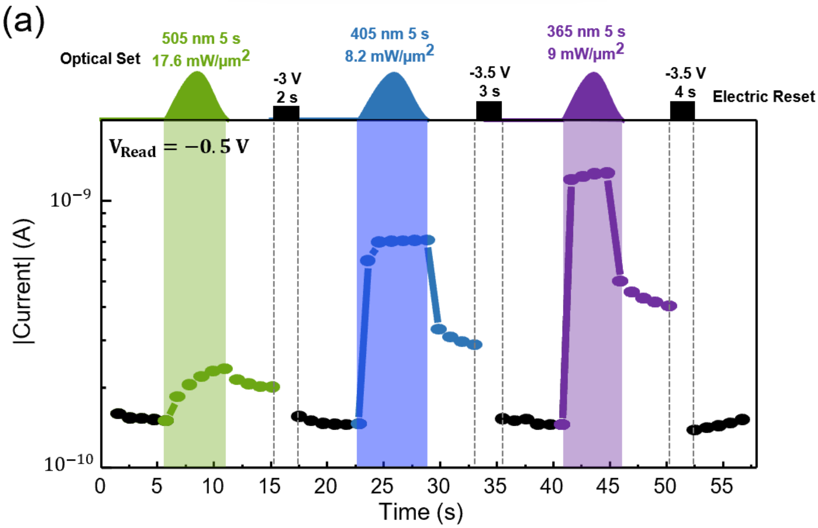

Figure E. 8 (a) Increased conductance states achieved by decreased wavelengths illumination and respective electrical Reset pulse for the Mo/IGZO:H/ITO device.

Cycle-to-cycle (C2C) variability evaluation was performed on the optimized devices with H-doping and Ti/Au as top contact. The results can be found in **Figure E.9**, where the transient response to 10 cycles of UV, blue and green illumination, followed by few seconds in the dark and a Reset pulse, is presented with no considerable change in device performance.

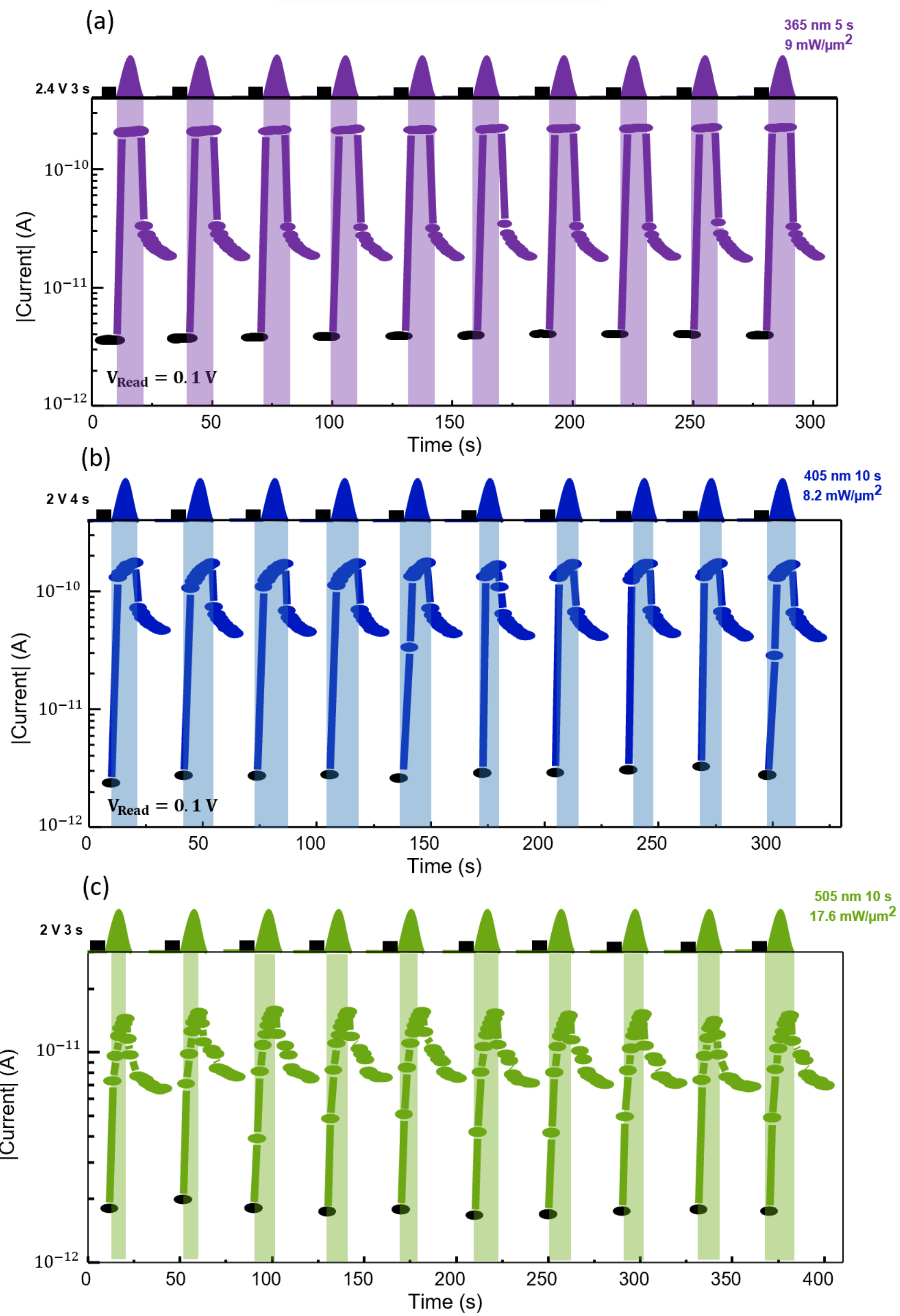

Figure E. 9 10 cycles of (a) UV, (b) blue and (c) green illumination, followed by a few seconds in the dark and a Reset pulse for the Mo/IGZO:H/Ti/Au device.

Device to device variability (D2D) was evaluated by the measurement of 10 devices with area of 4 µm^2 of their optical performance and I_{dark}. The results are displayed in **Figure E.10** and show minimal variability. Moreover, the variability that is presented is due to the unavoidable randomness introduced in the measurement by human LED positioning, on top of the device.

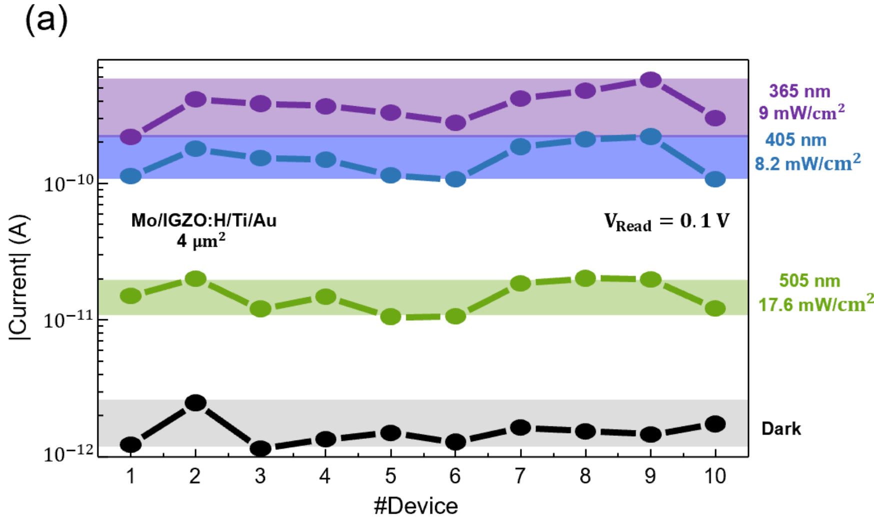

Figure E. 10 (a) I_{dark} and photocurrents after 10 s of illumination with 365, 405 and 505 nm wavelengths for 10 randomly chosen 4 µm^2 devices.

In **Figure E.11**, the transition from short-term memory (STM) to long-term memory (LTM) is shown by increasing power, illumination time or frequency of the light input. **E.11(a)**, **E.11(b)** and **E11(c)** presents the results for optical green inputs (505 nm wavelength) and **E.11(d)**, **E.11(e)** and **E.11(f)** are in regard to optical UV inputs (365 nm wavelength). The PPC decay is effectively manipulated by increased exposure simulating task repetition.

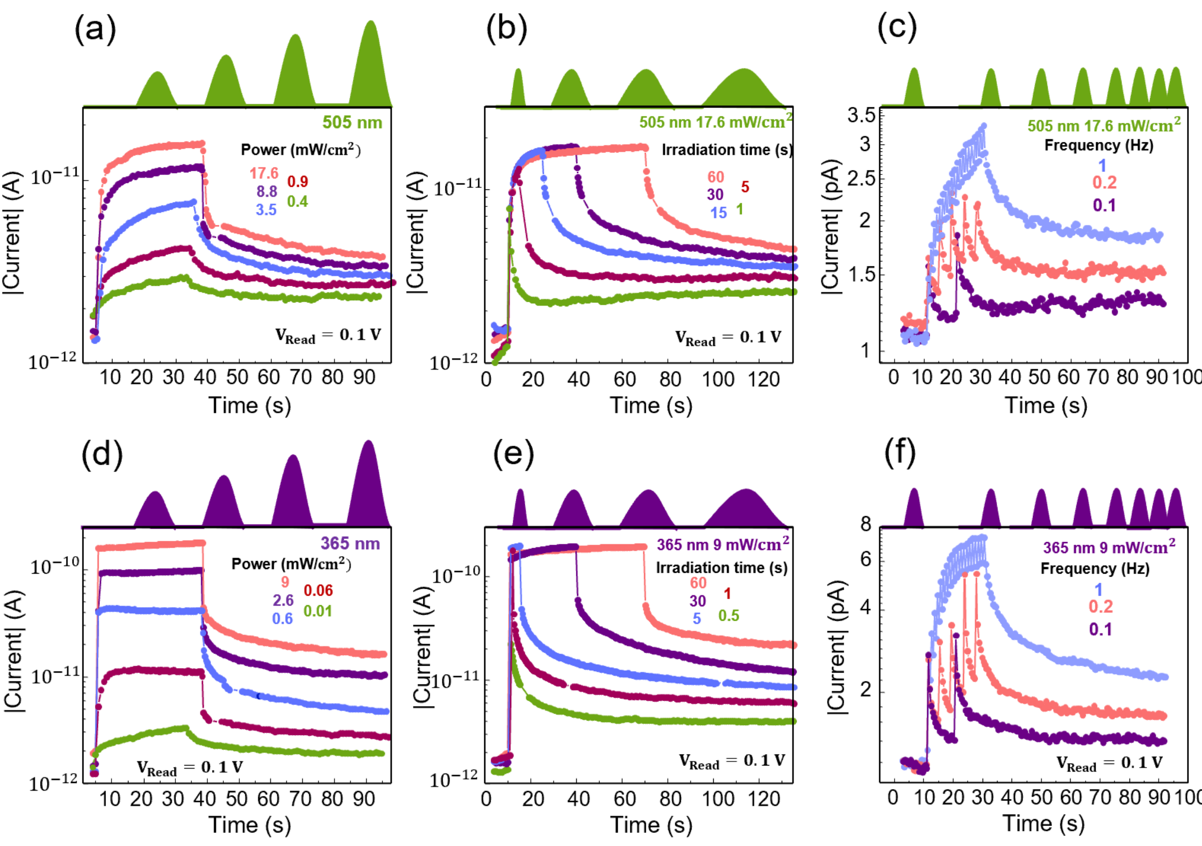

Figure E. 11 Transition from short-term memory (STM) to long term memory (LTM) by (a) increased power, (b) increased time and (c) increased frequency of illumination with a 505 nm wavelength LED. Transition from short-term memory (STM) to long term memory (LTM) by (d) increased power, (e) increased time and (f) increased frequency of illumination with a 365 nm wavelength LED.

In **Figure E.12**, the Kohlrausch stretched exponential fitting (equation 8.2 of Chapter 8) on the PPC that follows different irradiation times is shown for the tested wavelengths- **Figure E.12(a)** - 405 nm, **Figure E.12(b)** - 505 nm and **Figure E.12(c)** - 365 nm. The same photocurrent is reached in each of the different irradiation times assuring an accurate comparison of the recombination reaction. It can be seen that the PPC decay is effectively manipulated by increased exposure simulating task repetition. In **Figure E.12(d)** and **E.12(e)**, the characteristic relaxation time and stretch index are presented for different **E.12(d)** 505 nm and **E.12(e)** 365 nm illumination times that further confirm that the PPC decay is slower for longer irradiation times.

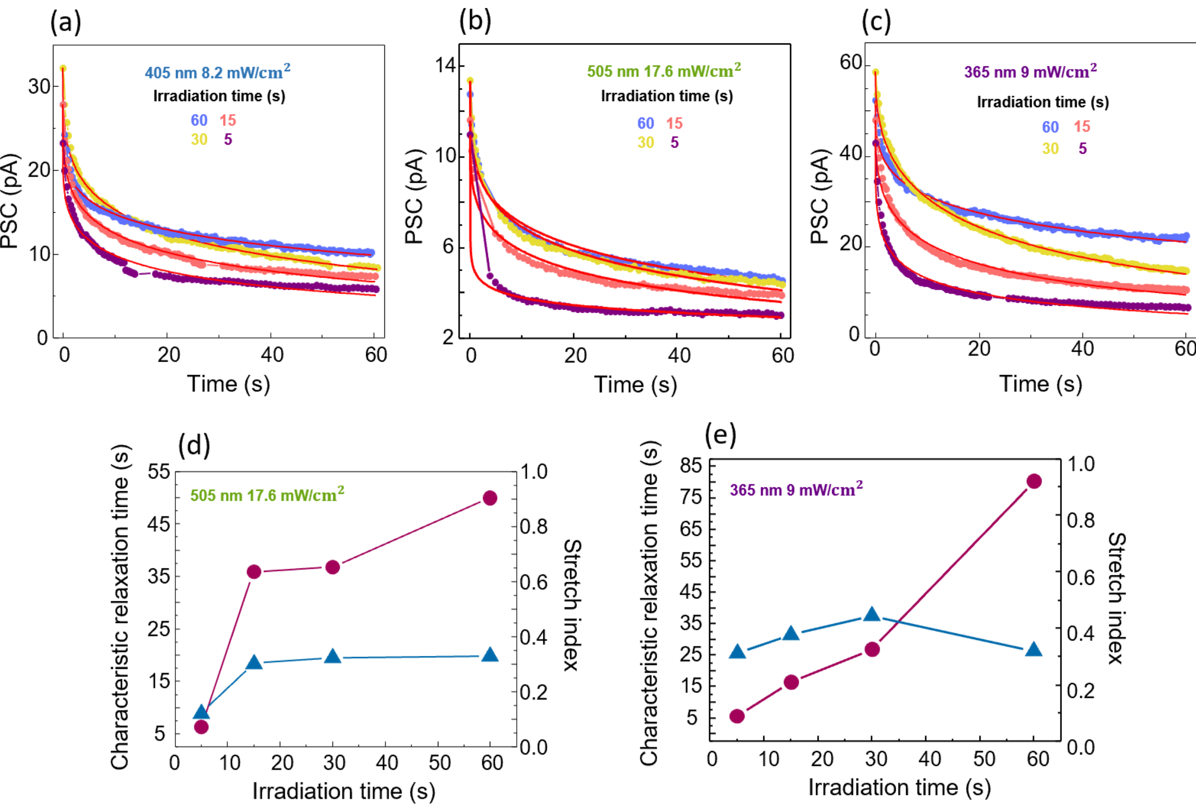

Figure E. 12 Kohlrausch stretched exponential PPC fitting on different irradiation times for (a) blue, (b) green and (c) UV light irradiation. Characteristic relaxation time and stretch index for different irradiation times for (d) green light irradiation and (e) UV light irradiation.

In **Figure E.13**, learning and forgetting behavior by pulsing light is shown with 3 cycles. Learning is simulated by applying 30 optical pulses of 150 ms in at 1 Hz, and forgetting is performed in the dark by applying solely the V_{Read} of 0.1 V for 20 s. After the first forgetting process the device has retained 48 % of the learned state. During the second cycle, the memristor needed 4 s to reach the previously learned state and during forgetting it retained 69 % of the state. In cycle 3, only 1 s was required to reach maximum current and the device remembered 78 % of the state by the end of the forgetting process. This indicates harder forgetting and easier relearning by task repetition, once again successfully mimicking the human brain.

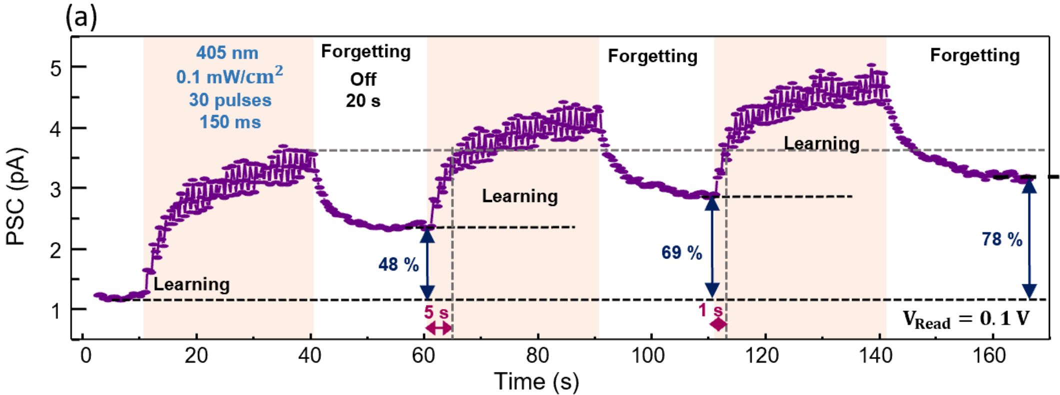

Figure E. 13 Learning and Forgetting demonstration by pulsing. Learning is performed by 30 optical pulses of 150 ms, 405 nm wavelength, 0.1 mW/cm² of power and 1 Hz of frequency. Forgetting is performed in the dark by applying the V_{Read} of 0.1 V for 20 s.

Photosensitive layer	Configuration	Size (μm^2)	Light wavelength (nm)	Energy consumption	Ref.
IGZO/SnO_x/PP	Planar	400000	400-650	40 pj – 450 nm	1
Si-NM/$MAPbI_3$	Planar	12500	532	1 pJ	2
MoS_2/BTO	Planar	60	450-650	1.8 pJ – 450 nm	3
IGZO/$CsPbBr_3$ QDs	Planar	820 000	350-600	1.35 pJ – 520 nm	4
$CsPbBr_3$/TIPS	Planar	16 000	365-500	0.076 pJ -450 nm	5
DPPDTT/SEBS	Vertical	N.M.	430	0.12 fJ	6
Si NM/P_3HT/PbS QDs	Planar	1000	365-1342	15.8 pJ – 532 nm	7
PbS QDs+ PMMA/pentacene	Planar	500 000	365-850	0.55 fJ	8
ZnAlSnO/SnO	Planar	200 000	635	0.75 fJ	9
IGZO:H	Planar	N.M.	400-1000	2.3 pJ – 500 nm	10
IGZO:H	Vertical	4	365-505	0.01 fJ - 405 nm 0.009 fJ - 505 nm	This work

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F

APPENDIX

Appendix F contains additional results to the Chapter 9 of this dissertation. In summary, the code written in python for the neural network ex-situ training is provided. The code trains the neural network using the training data defined for 28 patterns that represent the letters 'X' and 'T' and their noisy versions.

In **Figure F.1**, the code written in python for the neural network ex-situ training is provided. This code generates nine W_i from which the conductance for the 1T1M cells of the photoperceptron can be calculated.

(a)

```
import numpy as np

class Perceptron:
   def __init__(self, input_size, learning_rate):
      self.weights = np.random.uniform(-1, 1, size=input_size).round(2) # Defining Wi between -1 and 1 with two decimal points
      self.learning_rate = learning_rate

   def predict(self, inputs): # Activation function sgn
      summation = np.dot(inputs, self.weights)
      if summation >= 0:
         return 1
      else:
         return -1

   def train(self, training_inputs, labels):
      for _ in range(100): # epochs
         for inputs, label in zip(training_inputs, labels):
            prediction = self.predict(inputs)
            self.weights += self.learning_rate * (label - prediction) * inputs # Weight adjustment rule
            self.weights = np.clip(self.weights, -1, 1).round(2)

   def get_weights(self):
      return self.weights

# Defining the training data
training_inputs = np.array([
   [2, 1, 2, 1, 2, 1, 2, 1, 2],   [2, 1, 2, 1, 1, 1, 2, 1, 2],   [2, 1, 2, 1, 2, 2, 2, 1, 2],   [1, 1, 2, 1, 2, 1, 2, 1, 2],   [2, 1, 1, 2, 2, 1, 2, 1, 2],   [2, 2, 2, 1, 2, 1, 2, 1, 2],   [2, 1, 2, 1,
2, 1, 2, 2, 2],   [2, 1, 1, 1, 2, 1, 2, 1, 2],   [2, 1, 2, 1, 1, 2, 1, 1, 2],   [2, 1, 2, 2, 2, 1, 2, 1, 2],   [2, 1, 2, 1, 2, 2, 2, 2, 2],   [2, 1, 2, 1, 2, 1, 2, 1, 1],   [2, 1, 1, 1, 1, 1, 2, 1, 2],
[2, 2, 2, 1, 2, 1, 1, 2, 1],   [1, 2, 2, 1, 2, 1, 1, 2, 1],   [2, 1, 2, 1, 2, 1, 1, 2, 1],   [2, 2, 2, 1, 2, 1, 2, 2, 1],   [2, 2, 2, 1, 2, 1, 1, 1, 1],   [2, 2, 2, 2, 2, 1, 1, 2, 1],   [2, 2, 2, 1, 2,
2, 1, 2, 1],   [2, 2, 1, 1, 2, 1, 1, 2, 1],   [2, 2, 1, 2, 2, 1, 1, 2, 1],   [2, 2, 2, 2, 1, 1, 1, 2, 1],   [1, 2, 2, 2, 2, 1, 1, 2, 1],   [2, 1, 2, 1, 2, 1, 1, 1, 1],   [2, 2, 2, 2, 1, 1, 2, 2, 1],
[2, 2, 2, 1, 2, 1, 2, 2, 1],   [2, 1, 2, 1, 2, 2, 1, 2, 1]
   ])

# Defining the labels
labels = np.array([1] * 13 + [-1] * 15)

# Creating a Perceptron instance and training it
perceptron = Perceptron(input_size=9, learning_rate=0.1)
perceptron.train(training_inputs, labels)

# Get the trained weights
weights = perceptron.get_weights()

# Display the trained weights
print("Trained Weights:")
print(weights)
```

Figure F. 1 Code written in python for the proposed feed-forward neural network. The code trains the neural network using the training data defined for 28 patterns that represent the letters ‘X’ and ‘T’ and their noisy versions.

2024

MARIA ELIAS PEREIRA

OPTOELECTRONIC MEMRISTIVE DEVICES BASED ON SEMICONDUCTORS FOR THE NEXT GENERATION OF INFORMATION TECHNOLOGY