NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTAMENT OF
Electrical and Computer Engineering

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BSc in Electrical and Computer Engineering

Design of a very high frequency 4-bit current steering DAC for a high speed SerDes transmitter driver

MSc Thesis

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ABSTRACT

Nowadays, communication between chips is becoming more complex, however the output number of chips has kept mostly unchanged, turning parallel communication harder to implement. To make the jump from parallel to serial communications, a new system is needed to be implemented: Serializer/De-serializer. Along with the increased complexity of the data, also there is a necessity for higher speeds for the data to be transferred. Therefore, we propose to develop a high frequency Digital to Analog Converter which is to be implemented in a transmitter circuit for a high speed Serializer/De-serializer system.

The proposed project is implemented in 16nm FinFet technology and with the objective to be able to reach 10GHz frequency, 50Ω output impedance and 0.8V output swing. In order to accomplish this objective, the architecture implemented will be a segmented current-steering DAC with 2LSBs and 2MSBs composed of Current Source Array, Biasing Circuit, CML Driver with an output impedance calibrator, Decoder, Retiming and Drivers Circuit and a Current Reference Generator.

This implementation does not only have the objective of reaching high frequencies, but also maintain good non-linearity and minimize sensibility to the process and temperature. Due to the calibrator of the CML Driver having a bigger area, this implementation is expected to have higher power consumption then other implementations. These consequences of the design will try to be overcome.

Resumo

Hoje em dia, a comunicação entre chips tem-se tornado mais complexa, no entanto, o número de saídas dos chips tem-se mantido maioritariamente inalterado, tornando comunicação paralela obsoleta. De forma a dar o salto de comunicação paralela para comunicação série, um novo sistema tem que ser implementado: Serializer/De-serializer. Conjuntamente com o aumento da complexidade dos dados, também há uma necessidade para maiores velocidades para os dados serem transferidos. Assim, propomos desenvolver um Conversor Digital-Analógico de alta frequência a ser implementado num circuito transmissor para um sistema Serializer/De-serializer de alta velocidade.

O projeto a ser executado neste documento é implementado em tecnologia FinFet de 16nm e com o objetivo de ser capaz de alcançar 10GHz de frequência e 0.8V de output swing, mantendo 50Ω de impedância de saída. De forma a atingir os objetivos, a arquitetura implementada será um DAC de corrente segmentado com 2LSBs e 2MSBs composto por Fontes de Corrente, Circuito de Polarização, Driver CML com respetivo calibrador de impedância, Descodificador, Sincronizador e Drivers e Fonte de Corrente de Referência.

Esta implementação não só tem como objetivo atingir altas frequências, mas também manter uma boa não linearidade e minimizar a sensibilidade ao processo e temperatura. É expectável nesta implementação ter um maior consumo energético comparativamente com outras implementações e, devido ao calibrador da Driver CML, ter uma maior área. Estas consequências do design tentaremos superar.

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ACRONYMS

DAC- Digital to Analog Converter

SerDes- Serializer/De-serializer

CMOS- Complementary Metal Oxide Semiconductor

MOSFET- Metal Oxide Semiconductor

FinFet- Fin Field-Effect

SoCs- System on Chip

HPC- High Performance Computing

AI- Artificial Intelligence

IoT- Internet of Things

PLL- Phase-Locked Loop

CDR- Clock and Data Recovery

FSM- Finite State Machine

FFE- Feed Forward Equalizer

INL- Integral Non-Linearity

DNL- Differential Non-Linearity

LSB- Least Significant Bit

MSB- Most Significant Bit

FFT- Fast Fourier Transform

SNR- Signal to Noise Ratio

SNDR- Signal to Noise-plus-Distortion Ratio

SFDR- Spurious Free Dynamic Range

OPAMP- Operational Amplifier

OTA Operational Transconductance Amplifier

LVT- Low v_t

HV- High Voltage

1

INTRODUCTION

The project is to be executed in cooperation with Synopsys and consists in the development of a high frequency 4 bits current-steering Digital to Analog Converter (DAC) with a frequency of 10GHz to be used in a high speed SerDes (Serializer/De-serializer) transmitter drive. The DAC will be implemented in 16 nm CMOS technology matched with characteristic an impedance of 50Ω.

In this chapter we will present our initial objective along with the motivation for the need of the development of this project and then have a quick analysis of the problems and challenges to be overcome.

1.1 Motivation

As the demand of high-speed communication between chips grows and, as explained in [2], the number of chip's outputs staying mostly unchanged, despite the increased complexity and silicon density of those chips, along with the synchronism problems associated with parallel communication, high speed SerDes devices have become a standard in most chips. As described in [3], although SerDes systems add latency, they can reduce the chips complexity by reducing its number of pins and resulting in a more power efficient option.

In order to respond to the latency problem, faster SerDes must be developed, and along with them, the requirement for high-speed low-power DACs have increased since they are a fundamental block of the transmitter unit.

1.2 Problem Description

The main objective of the thesis project is to design a high frequency 4 bits DAC to be integrated in a high speed SerDes driver and implemented with 16 nm CMOS technology. For this objective to be accomplished, several steps have to be taken and some issues to be considered. Firstly, the technology to be used (16 nm), as described in [4] and further explored in Section 2.3 brings many advantages, but some challenges along to. Secondly, there are three main DAC architectures described in Section 2.2.3, which had to be studied in order to proceed with Current Steering DAC Architecture. Within Current Steering DAC, different architectures and Calibration Techniques can be applied as referenced in [5]. As a next step, there must be designed the output resistance so to have a characteristic impedance of 50Ω. The final step of the project is to design the layout of the circuit and analyze the post-layout results. An additional challenge is to maximize the output swing of the converter and minimize power consumption.

1.3 Document Organization

In the second chapter we will go through a background study where there will be present a simplified explanation of what a SerDes is, the benefits and drawbacks of its implementation, how it generally works and study in specific how a SerDes transmitter utilizing a DAC is composed and its functioning. Then we will study the basic definitions of digital to analog conversion including how it proceeds, how it can be evaluated and interpreted, and the errors associated with the conversion. After understanding digital to analog conversion, we will analyze the different implementations of the three main architectures for converters: resistive, capacitive and current- steering. Since the DAC designed in this project will be a current-steering DAC, we will analyze all the main modules that composes it in a traditional architecture along

with some compensation and calibration techniques. To finalize the second chapter, we will study the functioning of FinFet technology, along with its benefits and design challenges.

In the third chapter we will present the proposed architecture, along with its design and results. This chapter will be divided by the modules developed and its results, being those modules the Current Source Array, CML Driver and its calibrator, Retiming and Drivers, Reference Current Generator and Decoder. At every module will be presented the isolated results of the respective module and at the end we will present the final results for all modules working together.

At the fourth chapter we will present the layout implementation of the Current Source Array module along with the biasing system and of the CML Driver along with its calibrator. With these layouts we will extract the complete capacitance and resistance of the circuit, therefor altering our results which will be presented at the end of this chapter.

Finally, we will analyze the results obtained and the proposed objective in order to define future work and optimizations for this project.

2

BACKGROUND

2.1 SerDes System

A SerDes (Serializer/De-serializer) is a system meant to serialize and deserialize digital data for high-speed communications from one chip to another. This block, as referenced in [3], has become predominant in systems such as SoCs (System on Chip) especially dedicated to HPC (high-performance computing), AI (artificial intelligence), automotive systems, mobile systems and IoT (Internet of Things).

Most systems used to operate with parallel communications can be exemplified as in Figure 1.

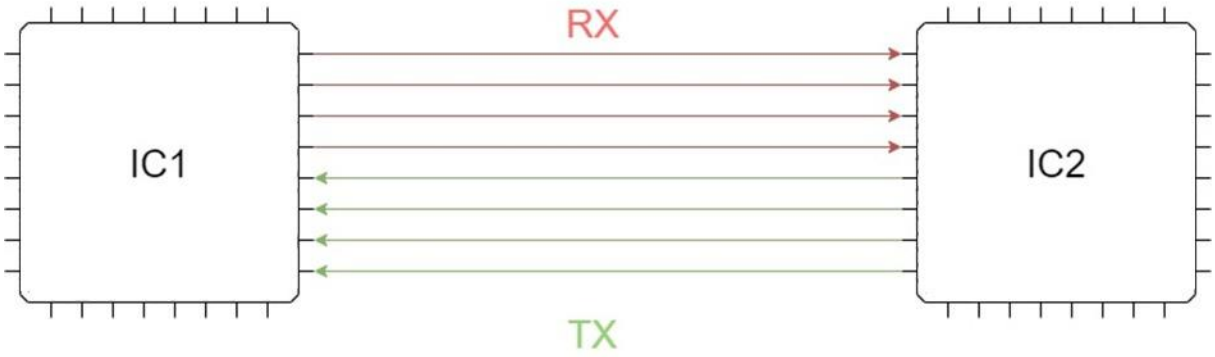

Figure 1: Simplified representation of parallel communication.

Parallel communication may have some advantages like almost no latency, however, as previously said at Section 1.2, the number of chip inputs and outputs has mainly stayed the same and not keeping up with the increased complexity of the chips and information being

transfer within them. Alongside that, as referenced in [3], parallel communication systems require more power.

As an alternative, serial communication systems have become a main form of communication between chips. The systems not only need less input/output connections as demonstrated in Figure 2, but also require less power and, as referred in [3], the clocks can be recovered from the data transferred, this way helping resolve synchronism problems.

Figure 2: Simplified representation of serial communication.

Although serial communication may seem to resolve most of the issues, it comes at a cost: higher latency. Therefor the necessity to reduce the latency and develop components able to reach higher frequencies.

2.1.1 Blocks

A SerDes system can be generally described by two main blocks represented in Figure 3: transmitter and receiver. These blocks communicate with another chip through a channel.

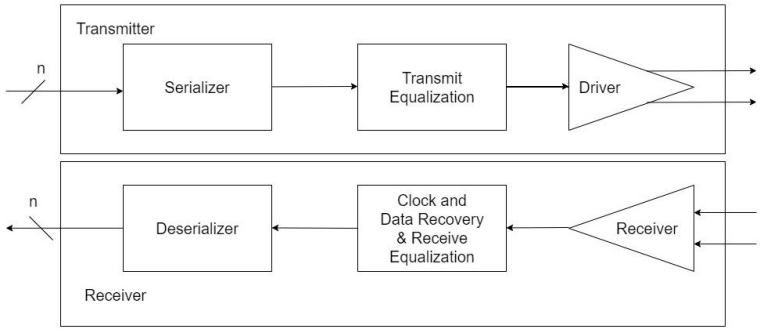

Figure 3: Simplified block diagram of a typical high-speed SerDes (adapted from [2]).

According to [6], the transmitter block receives n bits of information from within the chip at a frequency of $baud\ rate/_n$ and divides down the speed clock in the SerDes. After the n bits are serialized, they are sent to an output stage.

Still according to [6], the de-serializer follows the invert path, receiving the serialized information and clock value, deserializes to n bits and multiplies the clock for the original baud rate before sending the information to the rest of the chip.

A broader diagram of a SerDes system can be observed in Figure 4.

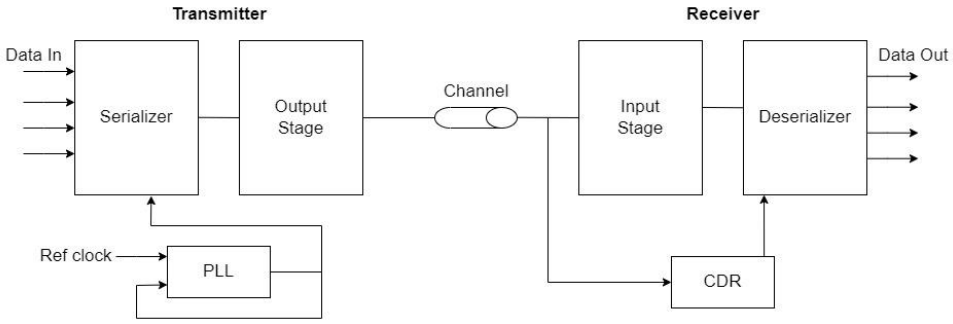

Figure 4: Block diagram of conventional SerDes (adapted from [7]).

As presented in Figure 4, the clock in which the system operates is controlled by the PLL (phase-locked loop) circuit on the transmitter and the CDR (clock and data recovery) circuit on the receiver.

2.1.2 Transmitter

As the objective of the project is to develop a DAC for a SerDes transmitter driver, then becomes relevant to analyse more specifically this block of the system. The block can be represented as shown in Figure 5, where is shown a block diagram of a 7-bit DAC based PAM-4 Transmitter. In this example from [8], we can observe as input the source clock from the PLL block, which was observed in Section 2.1.1. In this specific case, there are two paths for the clock: high frequency clock (HF CK Path) and low frequency clock (LF CK Path) to accommodate a broader range of data rates. The TXDIG block contains the CK Cal FSM (Finite State Machine) sub-block, which is responsible for the clock calibration, a Phase Rotator Controller, Pattern Generator and an FFE (Feed Forward Equalizer).

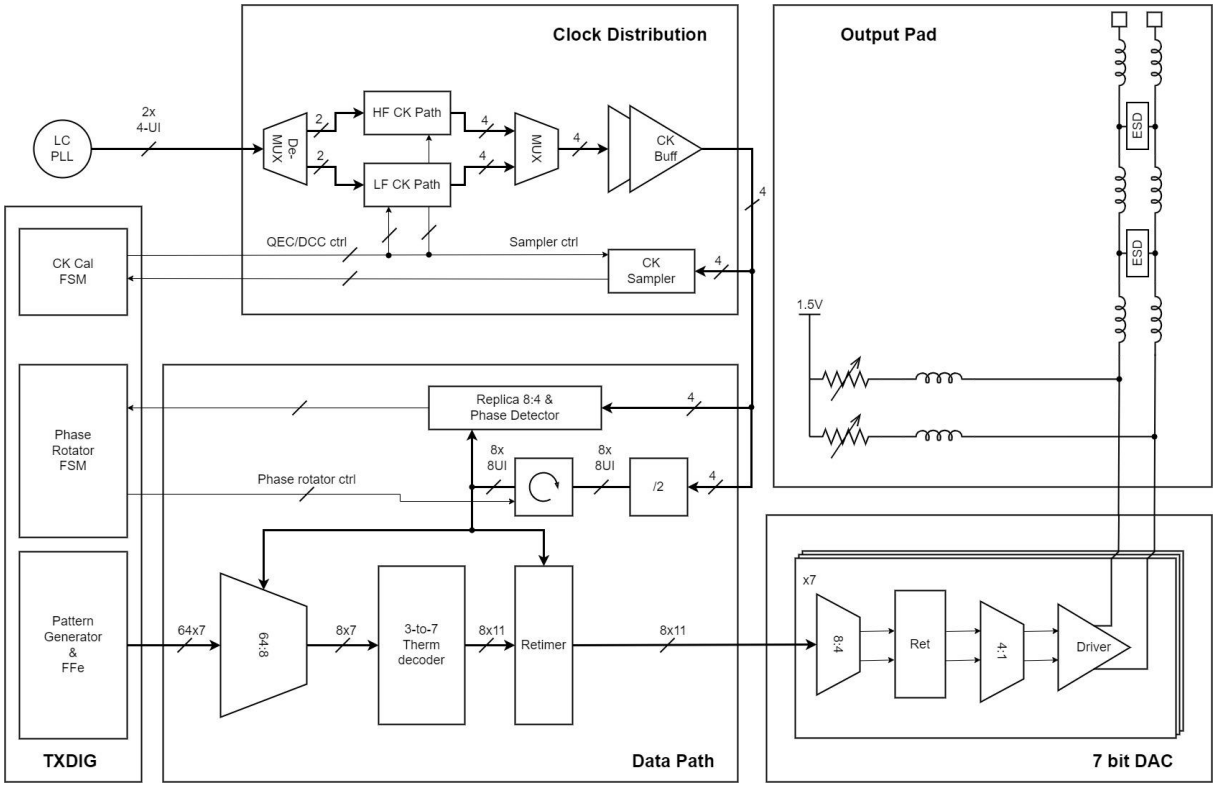

Figure 5: High-level block diagram of a SerDes Transmitter (adapted from [8])

As explained in [9], an equalizer cancels the distortion introduced by the channel re-sorting in a specific transfer function. In a transmitter this equalization is done in the FFE sub-block. The consequences of this equalization can be observed in Figure 6.

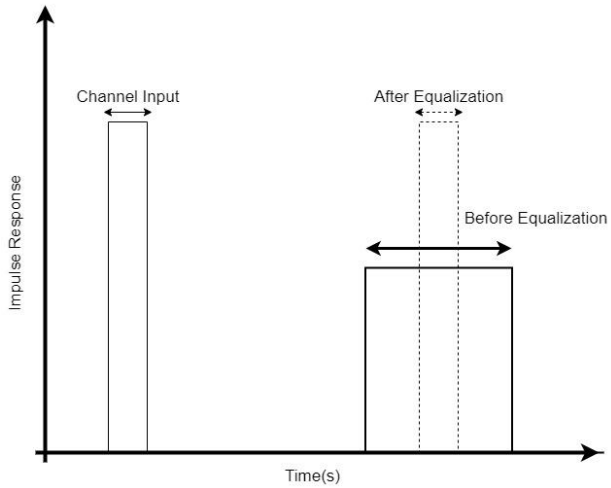

Figure 6: Pulse broadening due to ISI (Inter Symbol Interference) and effect of equalization.

At the data path we can observe a 3 to 7 Thermometer Decoder, which as explained in [10], is used to convert digital data into thermometer data.

The final blocks of a 7-bit DAC, CML Driver and an RL-filter-based matching network to match the impedance of the Output Pad to the Channel. The DAC and CML Driver blocks will be further explored in this report.

2.2 Digital to Analog Converter

A DAC is a device intended to convert digital data into an analog signal at a given sampling frequency as can be shown on Figure 7.

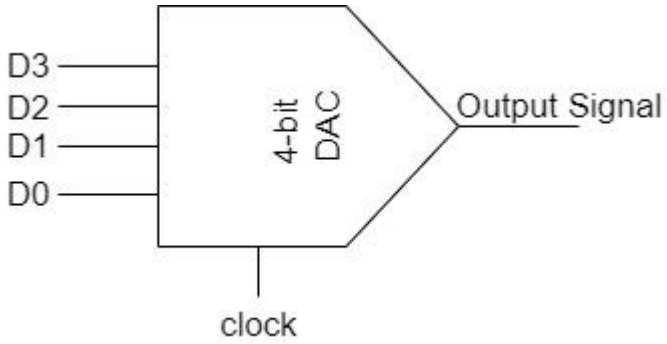

Figure 7: Simplified block of a 4-bit DAC.

In the conversion, the DAC receives a digital code and translates to voltage. In Figure 8, we can observe the output of a 6-bit DAC from a digital code formed by a sine wave.

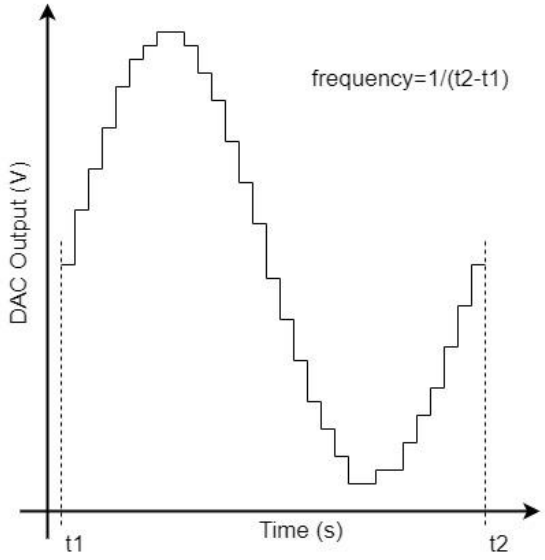

Figure 8: 6-bit DAC Output.

Each code is converted into a determinate voltage. The graphic incorporating all voltages to each code is called transfer function.

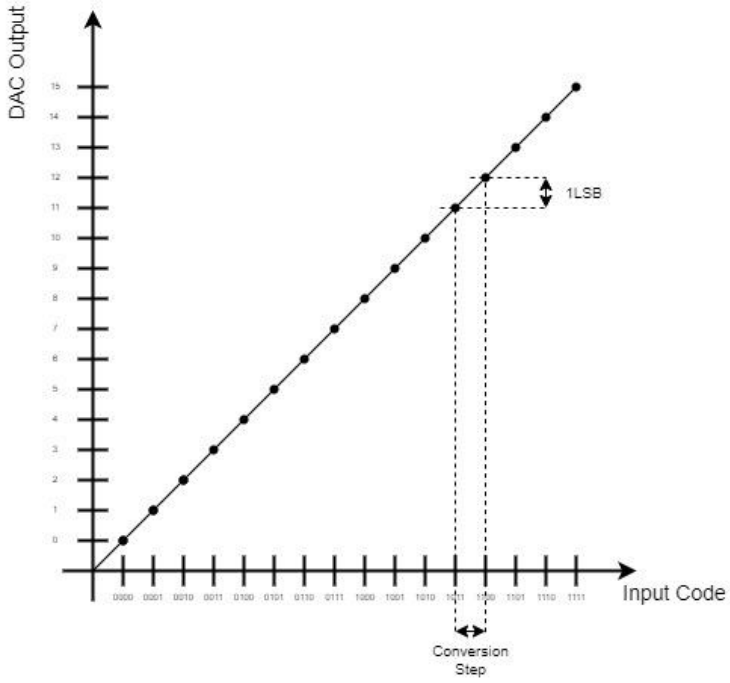

Figure 9: Ideal Transfer Function of a DAC.

In the time domain, there are certain evaluations that must be taken into consideration, mostly considering static errors.

2.2.1 Static errors

When inputting a DC signal into a converter, the errors affecting the accuracy of that converter are call static errors. According to [11], there are four main static errors: offset error, gain error, integral nonlinearity (INL) and differential nonlinearity (DNL).

2.2.1.1 Offset Error

As described in [11], offset error is defined by the difference between the ideal offset and the real offset of the transfer function, being characterized by the output value when the input code is 0. Such can be represented as shown in Figure 10.

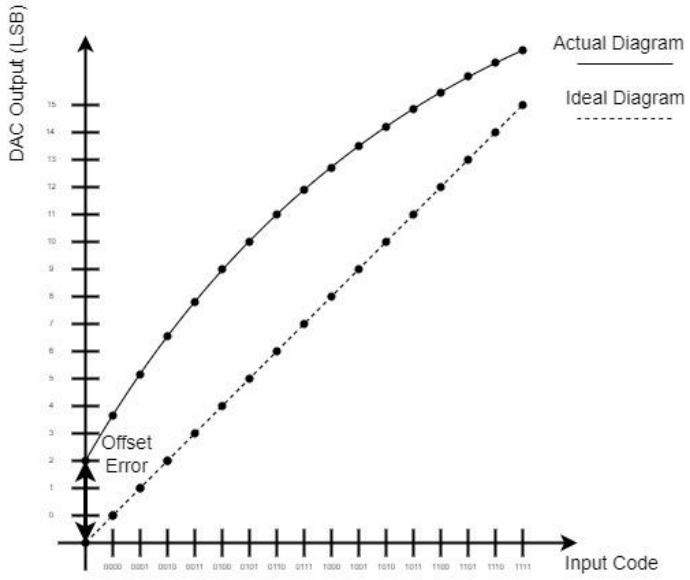

Figure 10: Offset Error of a 3-bit DAC.

2.2.1.2 Gain Error

The gain error, as referred in [11], is the difference between the ideal gain of the different points of the transfer function and the real gain of those points. The gain error can only be evaluated after the offset error is corrected to zero. The gain error can be represented as in Figure 11.

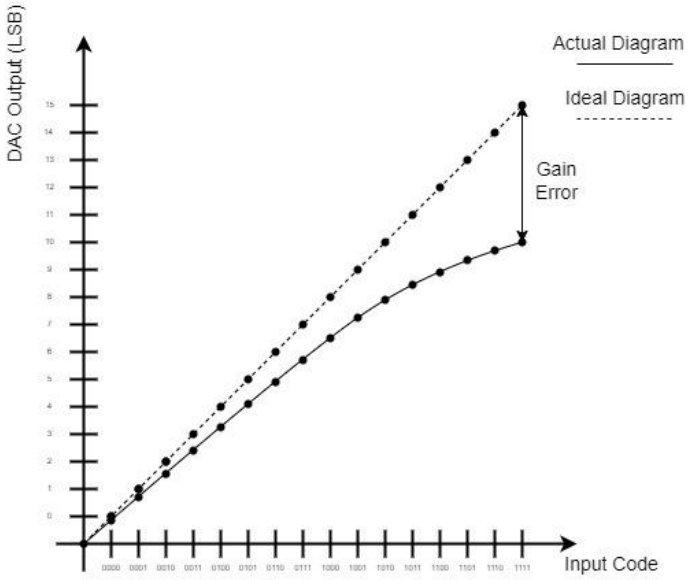

Figure 11: Gain error of a 3-bit DAC.

2.2.1.3 DNL

The DNL is calculated as the difference between the real height of a step and one LSB (Least Significant Bit). The LSB value is defined by the reference voltage of the DAC divided by the number of digital codes ($2^{n\ bits}$). DNL analysis must be done to every step as it can happen differently in each or not happen at all. This kind of behaviour can be observed in Figure 12 and the representation of a DNL analysis is shown by the example in Figure 13.

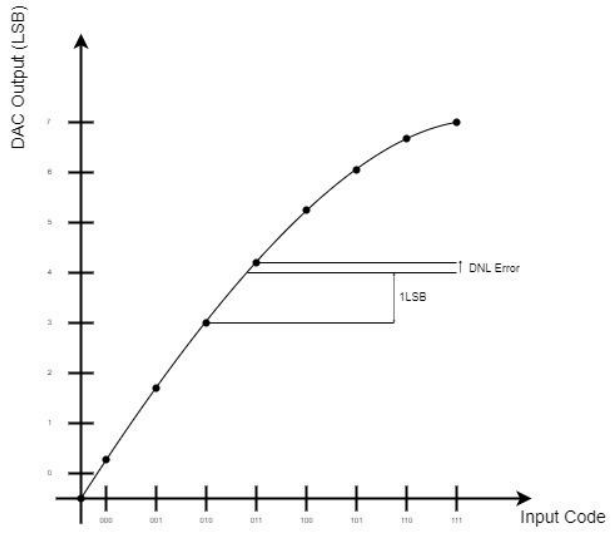

Figure 12: DNL of a 3-bit DAC.

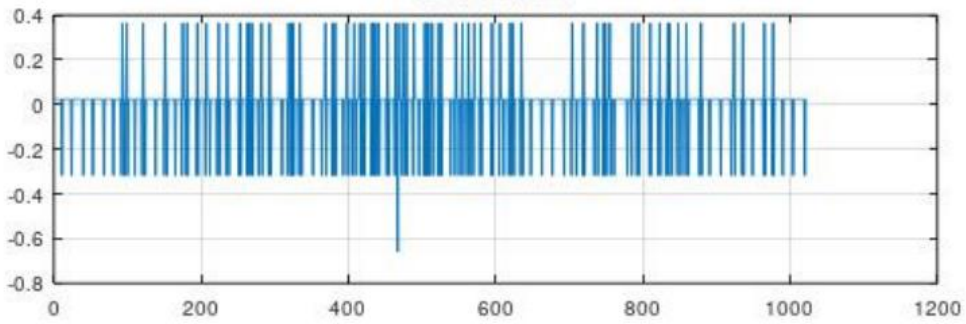

Figure 13: DNL Analysis of a DAC.

2.2.1.4 INL

The INL is, as explained in [11], the deviation of the values of the real transfer function from the straight line that characterises the ideal transfer function of the converter. Resembling DNL, INL is also represented in LSB as can be shown in Figure 14 and must be calculated at every step of the transfer function as represented in the example of Figure 15.

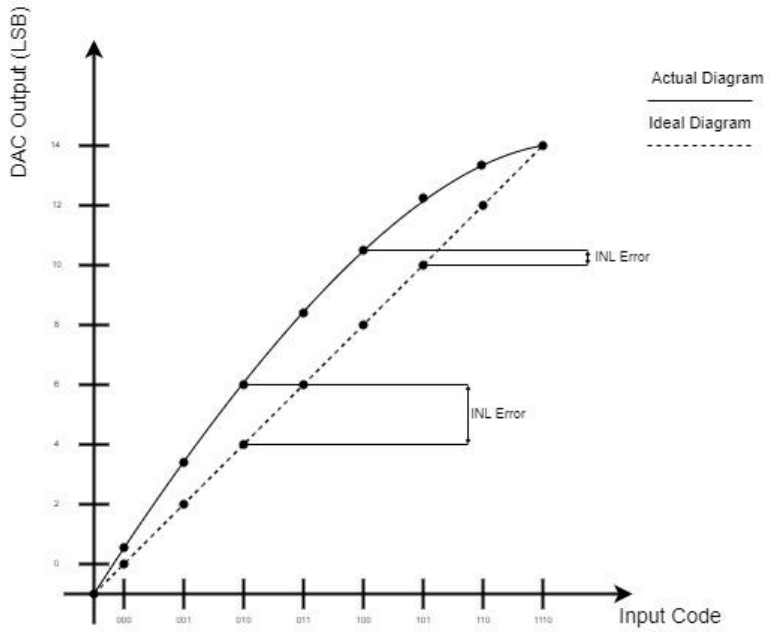

Figure 14: INL of a 3-bit DAC.

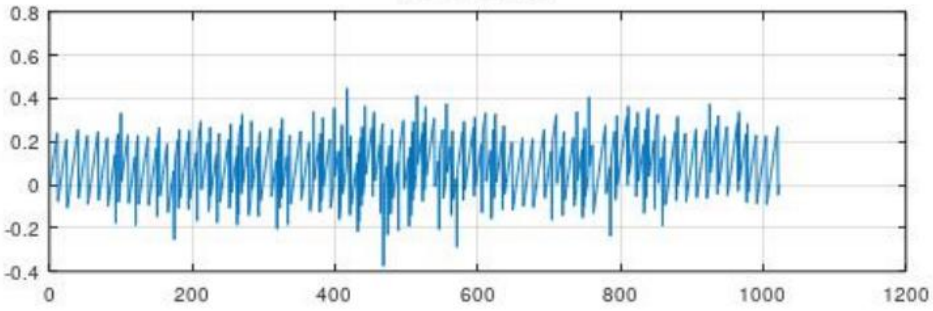

Figure 15: INL Analysis of a DAC.

2.2.2 Frequency Domain Analysis

As explained in [12], in high-speed converters, time domain representation is useful to understand the overall behaviour of the converter, however the frequency domain is best to measure its performance. The difference between these two domains can be illustrated as in Figure 16.

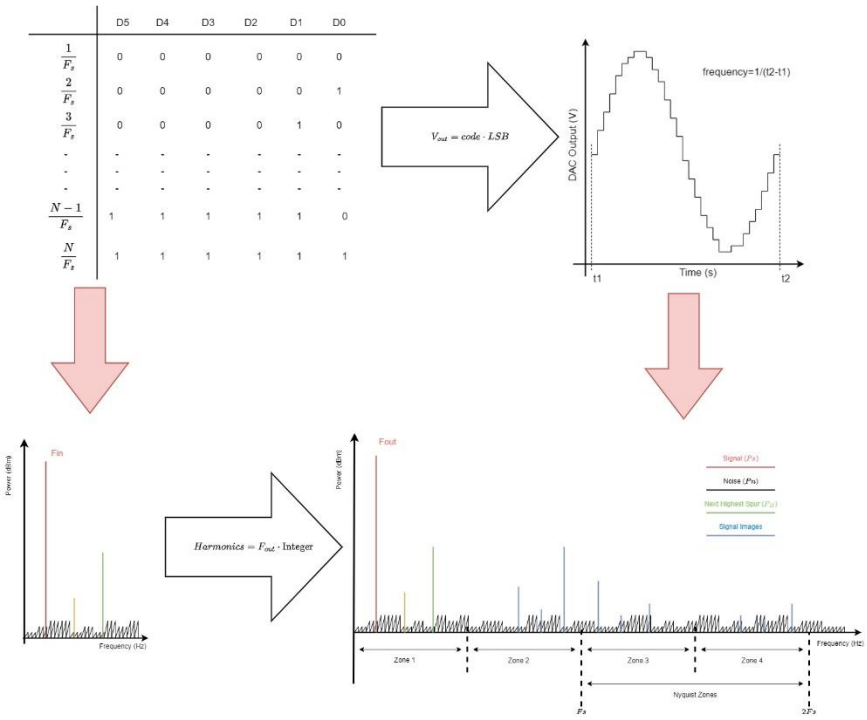

Figure 16: Difference between time and frequency domain.

Frequency domain plots are mostly described as FFT (Fast Fourier Transforms). Such are used to measure Signal Power (in dBm) across a linear frequency domain (Hz). These plots enable us to identify signal imperfections labelled as harmonics and noise.

Three of the first analysis to evaluate performance are SNR (Signal to Noise Ratio), SFDR (Spurious Free Dynamic Range) and SNDR (Signal to Noise-plus-Distortion Ratio).

SNR is calculated by the ratio between the RMS value of the fundamental output signal (P_S) and the RMS sum of the other spectral components (P_N). It is important to notice that the other spectral components considered to calculate SNR have to be below Nyquist frequency ($^1/_{F_S}$) and do not include neither DC component of the signal or the first six harmonics as explained in [12]. Such is calculated according to equation 1.

$$SNR = 10log_{10}\left(^{P_S}/_{P_N}\right)(dB) \quad (1)$$

SFDR represents the ratio between the RMS value of the fundamental output signal (P_S) and the RMS of the next higher power harmonic (P_H). SFDR can be calculated with equation 2.

$$SFDR = 10log_{10}\left(^{P_S}/_{P_H}\right)(dB) \quad (2)$$

The representation of the components to calculate SNR and SFDR can be demonstrated in a frequency domain plot as shown in Figure 17.

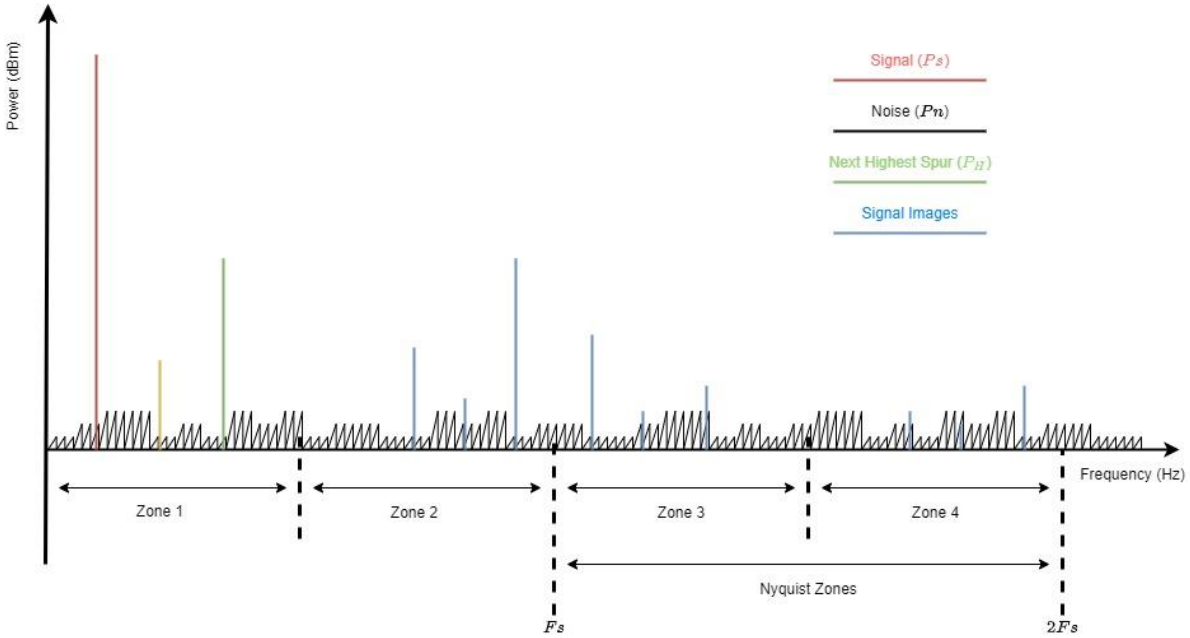

Figure 17: Single Tone DAC Performance Terminology and plot representation.

Lastly SNDR represents the ratio between the RMS value of the fundamental output signal (P_S) and the sum of the RMS value of the noise interferences (P_{noise}) and distortions to the signal (P_{distor}). Such is calculated by equation 3. Like SNR, SNDR only takes into consideration spectral components within Nyquist frequency.

$$SNDR = 10log_{10}\left(\frac{P_S}{P_{noise} + P_{distor}}\right)(dB) \tag{3}$$

Knowing the SNDR, we can calculate the ENOB (Effective Number of Bits) representing the number of bits the converter can convert maintaining the performance and behaviour of an ideal converter. The ENOB is calculated by the equation 4.

$$ENOB = \frac{SNDR - 1.76}{6.02}(bit) \tag{4}$$

2.2.3 DAC Architectures

There are three main different DAC architectures: resistive DAC's, switched capacitors DAC's and current steering DAC's.

2.2.3.1 Resistive DAC

Resistor DACs are mostly defined by the use of resistors for the conversion, outputting a signal characterized by voltage. There are three main approaches for resistor DACs: string resistor DAC, binary weighted resistor DAC and R-2R ladder resistor DAC.

2.2.3.1.1 String Resistor DAC

In a string resistor DAC architecture there are N resistors, being N the number of bits of the input code. These resistors are commonly connected between the reference voltage and ground dividing the reference voltage by the number of codes in each node. The voltage output comes from one node at a time controlled by switches as represented in Figure 18.

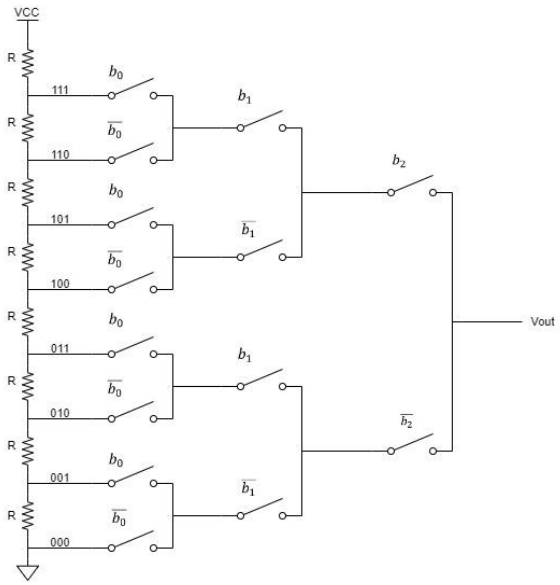

Figure 18: Example of a 3-bit string resistor DAC.

2.2.3.1.1 Binary Weighted Resistor DAC

Binary weighted resistor DACs take advantage of the implementation of an AMPOP as presented in Figure 19, reducing the number of resistors to N+1, being N the number of bits. Therefore, considering an ideal AMPOP, making the sum of the currents of each bit controlled by a group of switches and, through the OPAMP, being "translated" into voltage.

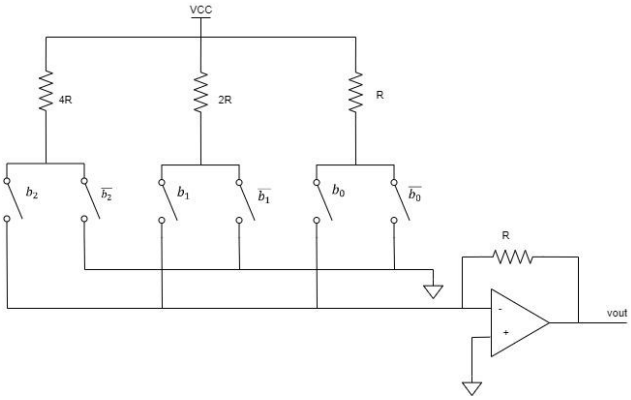

Figure 19: Example of 3-bit binary weighted resistor DAC.

2.2.3.1.2 R-2R Ladder Resistor DAC

R-2R Ladder Resistor DACs brings an interesting fusion between string resistor DACs and binary weighted DACs proposing a new architecture that, resourcing to AMPOP and converting the sum of the currents provided by each bit, has to an initial string of resistors as shown in Figure 20. These makes the number of necessary resistors to 2N+1, being N the number of bits. The output of this topology is calculated by the equation 5.

$$V_{out} = \sum_{i=0}^{n_{bits}-1} \frac{V_{ref} \times b_i}{2^{n_{bits}-i}} \tag{5}$$

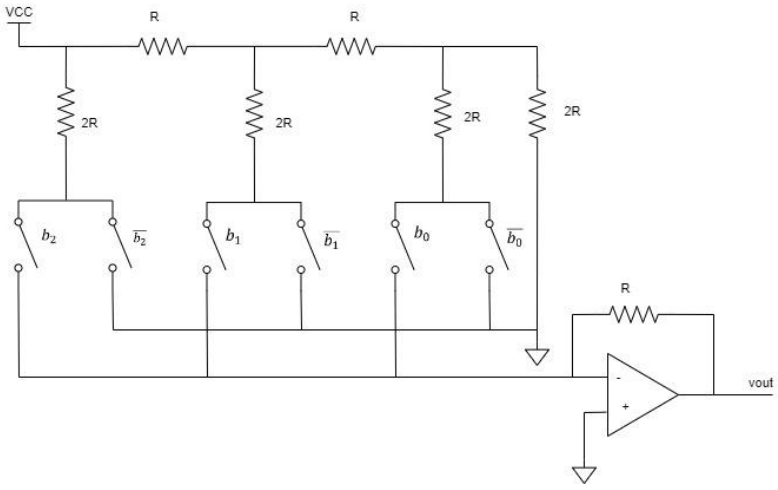

Figure 20: Example of 3-bit R-2R resistor DAC.

2.2.3.2 Switched Capacitor DAC

Switched Capacitor DACs are mostly characterized by the use, as implicit in the name, of capacitors and switches taking advantage of Law of Conservation of Energy. Usually

designed with a plate of capacitors connected to a comparator as represented in Figure 21. The number of capacitors is N being N the number of bits. The total charge for each stage is done by the sum of the capacitors active with the reference voltage.

There are different forms of application of the top plates separating the MSBs from the LSBs or not, as shown in Figure 21.

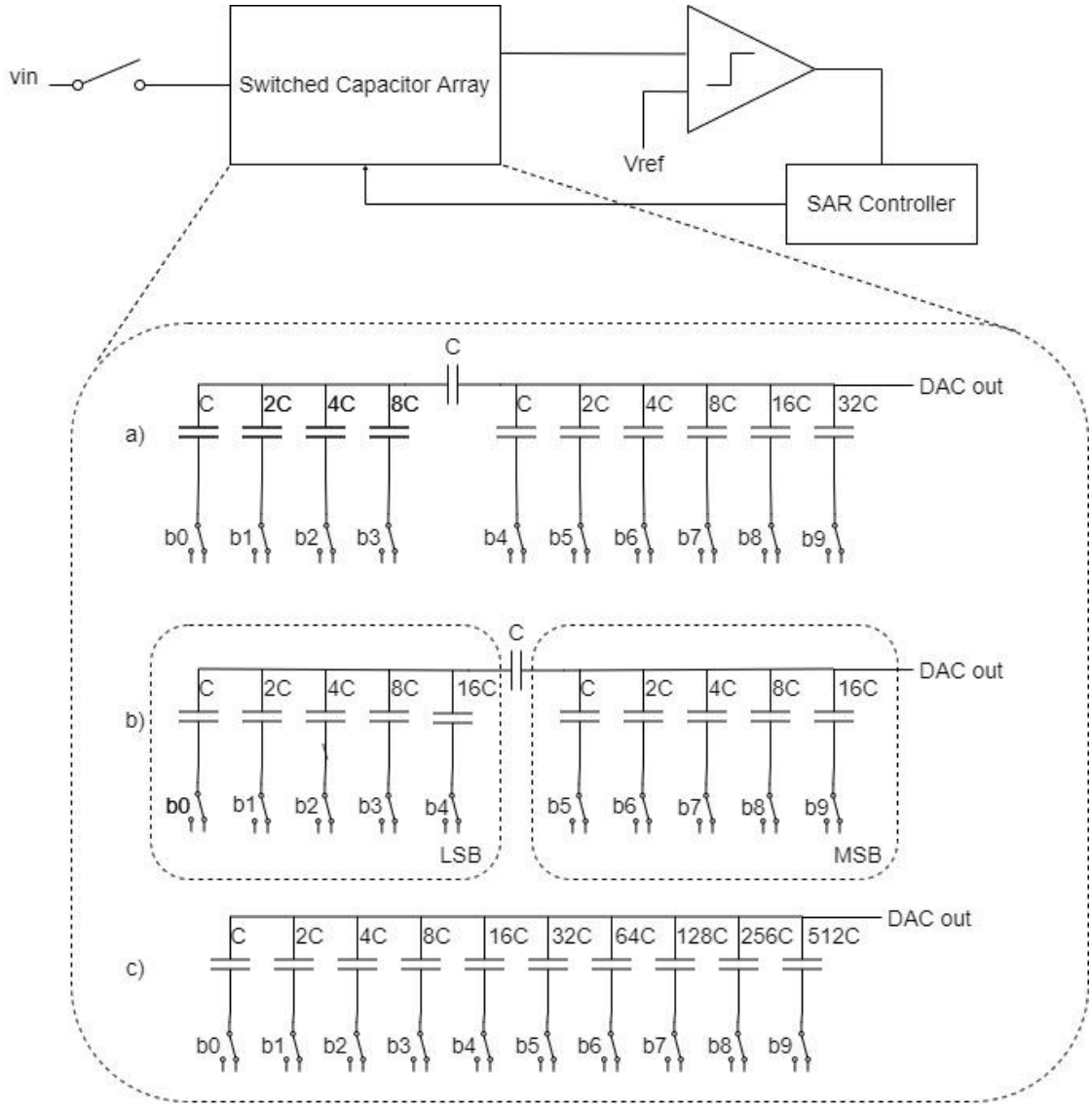

Figure 21: Different 10-bit Switched Capacitors DAC topologies (a) 6-4 split-capacitor DAC (b) 5-5 split-capacitor DAC (c) binary-weighted DAC.

2.2.3.3 Current Steering DAC

Current Steering DACs are built with an array of active current sources and switches. Since the current sources are always active, the currents must be steered in order to sum the currents corresponding to the input code and outputting that same sum. There are three main

types of implementations: binary implementation, unary implementation and segmented implementation.

2.2.3.3.1 Current steering DAC with Binary Implementation

The binary implementation is characterized by the array being composed of N current sources and N switches, being N the number of bits. Each current source provides a current twice as large as the less significant bit before as shown in Figure 22. The output current is calculated by the equation 6.

$$i_{out} = \sum_{i=0}^{n_{bits}-1} b_i \times 2^i \times I \tag{6}$$

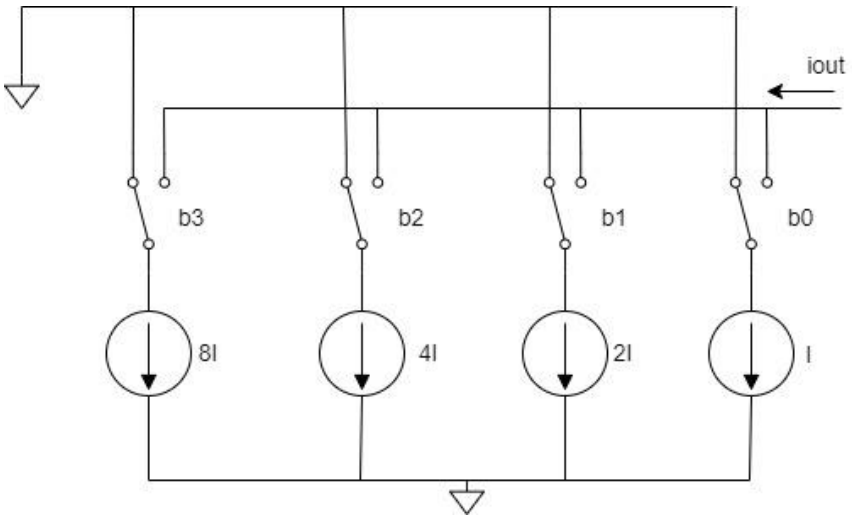

Figure 22: Example of 4-bit current steering DAC with Binary Implementation.

2.2.3.3.2 Current steering DAC with Unary Implementation

The unary implementation is characterized by the array being composed of 2^N current sources and 2^N switches, being N the number of bits. All current sources provide the same value of current, as shown in Figure 23. The output current is calculated by the equation (7).

$$i_{out} = \sum_{i=0}^{2^N-1} b_i \times I \tag{7}$$

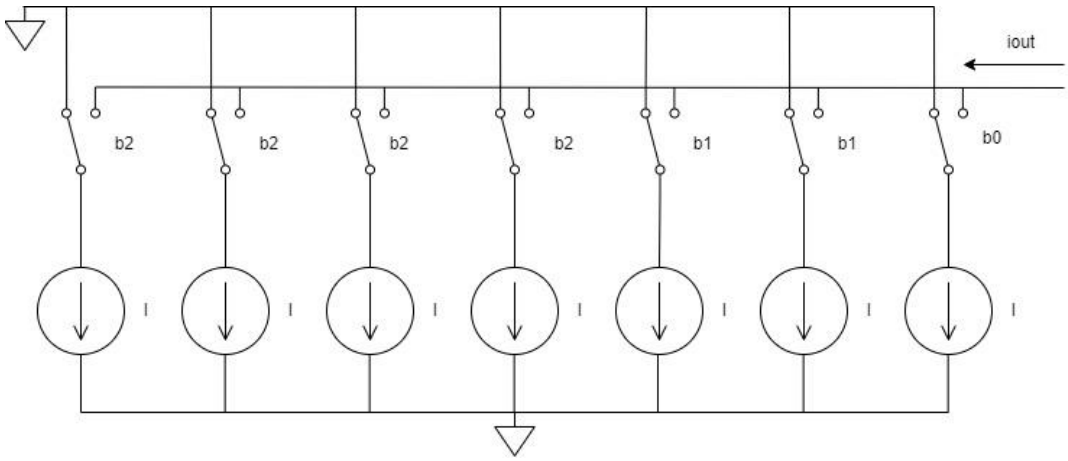

Figure 23: Example of 3-bit current steering DAC with Unary Implementation.

2.2.3.3.3 Current Steering DAC with a Segmented Implementation

The segmented implementation is a mix between binary implementation and unary implementation dividing the array in LSBs and MSBs as can be observed in Figure 24. As described in [18], the more binary bits used, the higher the DNL will be, so this implementation takes advantage of the less none-linearity of the unary implementation for the MSBs but reducing the power consumption and area of the circuit using binary implementation for the LSBs.

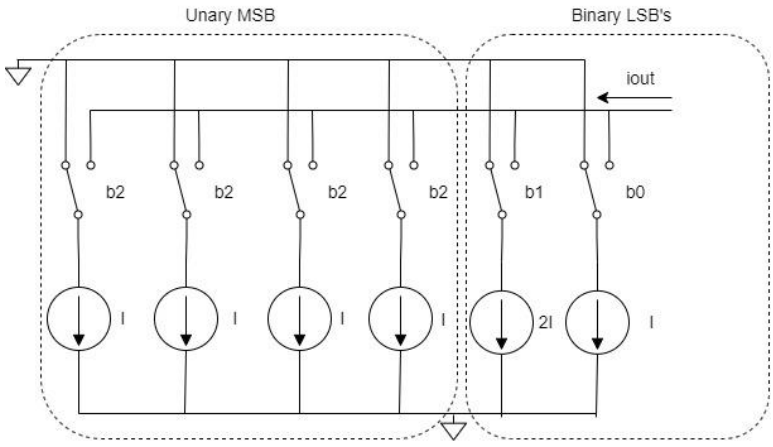

Figure 24: Example of 3-bit Current Steering DAC with a segmented implementation.

2.2.3.4 Comparison between Architectures

Within DACs, there may be many approaches with different results. In Table 1 there are present the results for five different approaches for resistor DACs, in Table 2 five different approaches for capacitor DACs and in Table 3 five different approaches for current steering DACs.

Table 1: Comparisons with State-of-the-Art Resistor DACs.

Parameter	[12]	[13]	[14]	[15]	[16]
Technology (µm)	0.5	0.18	0.35/0.5	0.35	0.35
Resolution (bits)	8	8	10	10+2	12
Output Rage(V)	0 to 3.3	0.3 to 2.1	0.2 to 4.7	1 to 17	0.1 to 3.2
INL (LSB)	0.0054	0.024	1.45	0.54	1.51
DNL (LSB)	0.0046	0.004	1.37	0.26	0.46
Area (mm^2)	2.6	0.0297	4.2	0.15	46.5
Current (µA)	190	65	1.2	-	2.4

Table 2 : Comparisons with State-of-the-Art Capacitor DACs.

Parameter	[17]	[18]	[19]	[20]	[21]
Technology (nm)	28	65	180	130	16
Resolution (bits)	5	8	8	11	8
Supply Voltage(V)	1	1.2	0.9	0.5	0.8
INL (LSB)	0.73	0.3	<1.4	0.89	1
DNL (LSB)	0.35	0.3	<0.75	0.78	-
Area (mm^2)	4.4	0.03	0.3	0.582	0.011
Power (mW)	0.015	1.83	1.6	0.00056	50

Table 3: Comparisons with State-of-the-Art Current Steering DACs.

Parameter	[22]	[23]	[24]	[25]	[26]
Technology (µm)	110	180	32	130	14
Resolution (bits)	6	6	10	12	12
INL (LSB)	0.7	0.0036	<0.4	2	2
DNL (LSB)	0.7	0.0023	<0.4	1	-
Area (mm^2)	0.46	-	-	3.99	0.093
Power (mW)	19.1	17.7	2.3	35	12.5
Sampling Frequency (GS/s)	1	3.1	1	0.08	1

Resistive DACs present good non-linearity mostly for smaller resolutions. As the resolution becomes greater, non-linearity problems become more preponderant. Another diminisher of this architecture, as explained in [18], is the fact that, for higher resolutions, the area increases dramatically added by the natural speed limitations of this architecture.

The first drawback of capacitive DACs is the difficulty in achieving higher speeds. This is due to the natural behaviour of switched capacitor architectures needing two phases to operate. Another problem of capacitive DACs, as referred in [27], is its nonlinear behaviour intrinsic to the capacitors used.

At last, the current steering DACs is shown to be more favourable for the problem in study, showing a better cost in terms of area, best speed performance and a more linear behaviour. One of its diminishes is the higher power consumption as can be observed in Table 3. Although the current project only requires a resolution of 4 bits, there is still a chance to try to increase it, corroborating the decision for this architecture.

2.2.4 Current Steering DAC Architectures

As analysed in Section 2.2.3.4, there are three different implementations of current steering DAC, being the two simplest the binary and unary implementations. The binary implementation has shown to have linearity problems increased by the number of bits of the converter. The unary implementation seems to significantly mitigate this problem, but at the cost of increasing massively its area. In the end, a segmented implementation shows itself as a reasonable trade-off between area and performance.

After choosing the implementation required for this project (segmented implementation), we must analyse the blocks that make part of it. Those blocks are: Current Source Array, Biasing circuit, Thermometer Decoder, Latency Equalizer, Latches and Drivers and the output CML Driver. These blocks can be observed in Figure 25 and Figure 5.

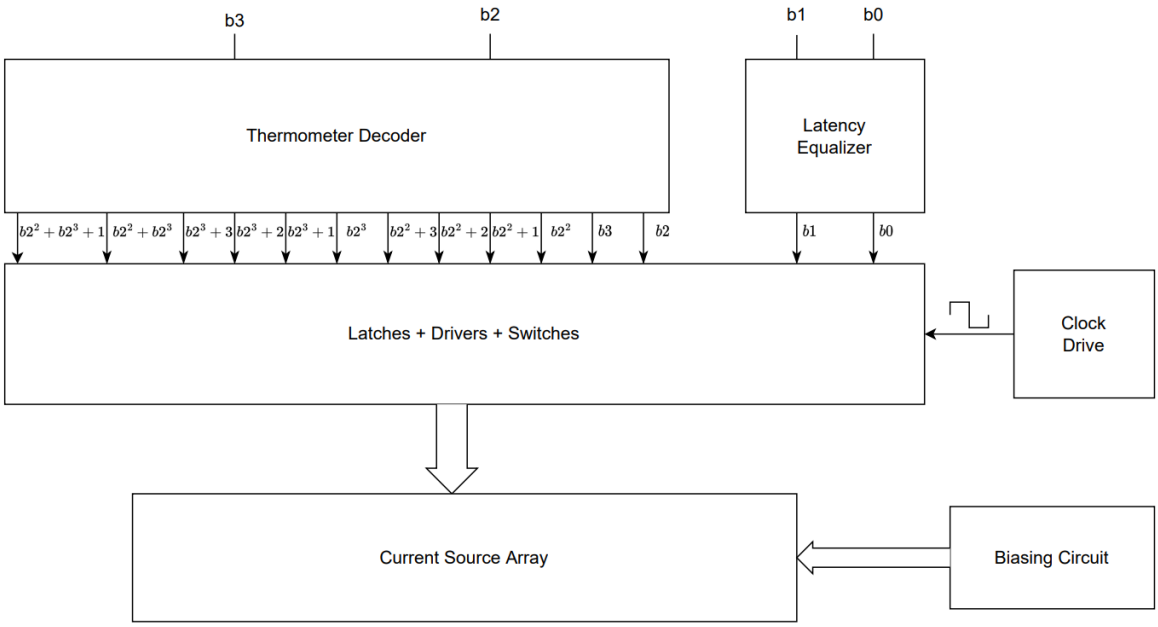

Figure 25: Basic block diagram of a 4-bit DAC with segmented implementation.

2.2.4.1 Blocks

2.2.4.1.1 Current Sources Array

The current source array block is made of all the current sources controlling the output current and being controlled by the drivers and latches. The generic representation of the array can be seen in Figure 23 at Section 2.2.3.3.2 as the individual implementation of a single current cell is observed in Figure 26. Considering that no two transistors are equal, random errors are to be expected. Those errors can be mitigated by resourcing to a cascode configuration and adding one or two transistors to the cascode, increasing its output impedance and approximating the current cell to an ideal current source. Is important to refer that both the switching and the cascode transistors must be working between saturation and turned off. The cascode must be at a constant polarization voltage (gate voltage) and the switching transistor controller by the switching voltage (gate voltage), being turned on or off.

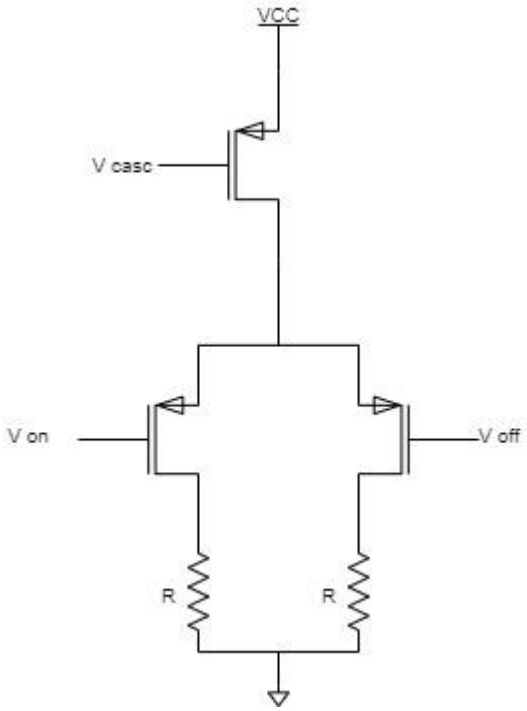

Figure 26: Example of a current cell.

2.2.4.1.2 Biasing Circuit

The functionality of a biasing circuit is to polarize the current source array, therefor defining its gate voltage and drain current, as explained in [27]. The simplest way to implement a biasing circuit is through a current mirror as illustrated in Figure 27.

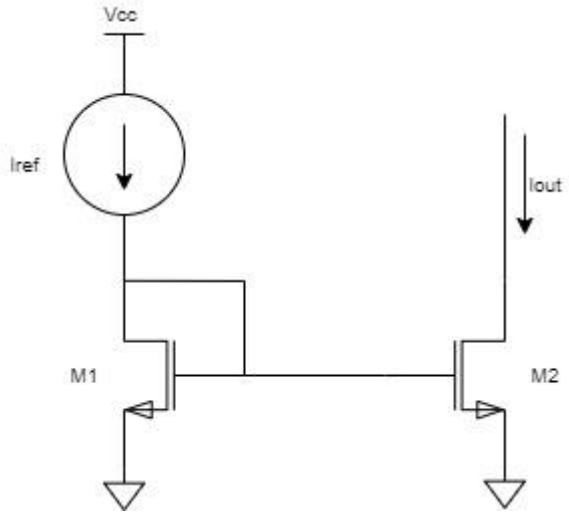

Figure 27: Simple schematic of a current mirror.

For the correct functioning of a current mirror, like in the source array block, all transistors must be working in saturation. A simple current mirror is defined by having an ideal current

source imposing a current to the first transistor. The first transistor will then polarize the second having them both drain currents characterized by the equations 8 and 9.

$$I_{D\_M1} \approx \frac{1}{2}\mu_n C_{ox}\left(\frac{W_{M1}}{L_{M1}}\right)\left(V_{GS\_M1} - V_{T\_M1}\right)^2 \quad (8)$$

$$I_{D\_M2} \approx \frac{1}{2}\mu_n C_{ox}\left(\frac{W_{M2}}{L_{M2}}\right)\left(V_{GS\_M2} - V_{T\_M2}\right)^2 \quad (9)$$

Through both transistors (considering they're ideal), sharing the same gate to source voltage, considering they are structurally the same (same $\mu_n C_{ox}$ and V_T) and knowing that $I_{D\_M1} = I_{ref}$ and $I_{D\_M2} = I_{out}$, we can conclude that the output current will only depend on the difference between their sizes demonstrated by equation 10.

$$I_{out} = I_{ref} \times \frac{W_{M2}/L_{M2}}{W_{M1}/L_{M1}} \quad (10)$$

At last, this project will be all made using the same technology (16nm), making the length of the transistor the same resulting in the simplest equation 11.

$$I_{out} \approx I_{ref} \times \frac{W_{M2}}{W_{M1}} \quad (11)$$

This first analysis was made considering some simplifications applicable in finFet technology due to the very short channel. If we took it into account, the real equations for the drain currents and, subsequentially, the output current are represented by the equations 12, 13 and 14.

$$I_{D\_M1} \approx \frac{1}{2}\mu_n C_{ox}\left(\frac{W_{M1}}{L_{M1}}\right)\left(V_{GS\_M1} - V_{T\_M1}\right)^2\left(1 + \lambda V_{DS\_M1}\right) \quad (12)$$

$$I_{D\_M2} \approx \frac{1}{2}\mu_n C_{ox}\left(\frac{W_{M2}}{L_{M2}}\right)\left(V_{GS\_M2} - V_{T\_M2}\right)^2\left(1 + \lambda V_{DS\_M2}\right) \quad (13)$$

$$I_{out} \approx I_{ref} \times \frac{W_{M2}\left(1 + \lambda V_{DS\_M1}\right)}{W_{M1}\left(1 + \lambda V_{DS\_M1}\right)} \quad (14)$$

As explained in [18], one solution to mitigate this problem is to implement a cascode transistor with its source connected to the second transistor's drain as shown in Figure 28.

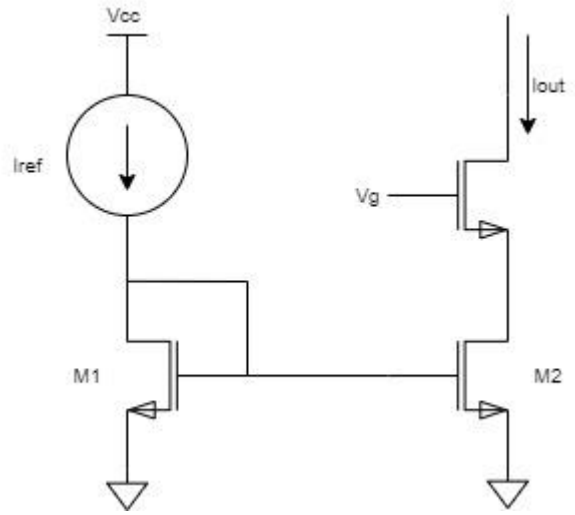

Figure 28: Schematic of a cascode current mirror.

The implementation of this third transistor allows the second transistor to be less influenced by channel length modulation due to the cascode topology, but in order to allow the drain to source voltages of the two first transistors to be the same, $Vg = V_{GS\_M3} + V_{DS\_M1}$, being $V_{DS\_M1} = V_{DS_{M2}} = V_{GS\_M2}$, resulting in an output current equation equal back to equation 11)

2.2.4.1.3 Thermometer Decoder

The thermometer decoder is important for controlling the switches, as explained in [10] and in Section 2.1.2, translating the digital inputs into thermometer code. In Figure 29 we can observe the codes graphical representation for a 3-bit decoder and in Figure 30 an example of a binary to thermometer decoder circuit.

000	001	010	011	100	101	110	111

Figure 29: Thermometer codes graphical representation.

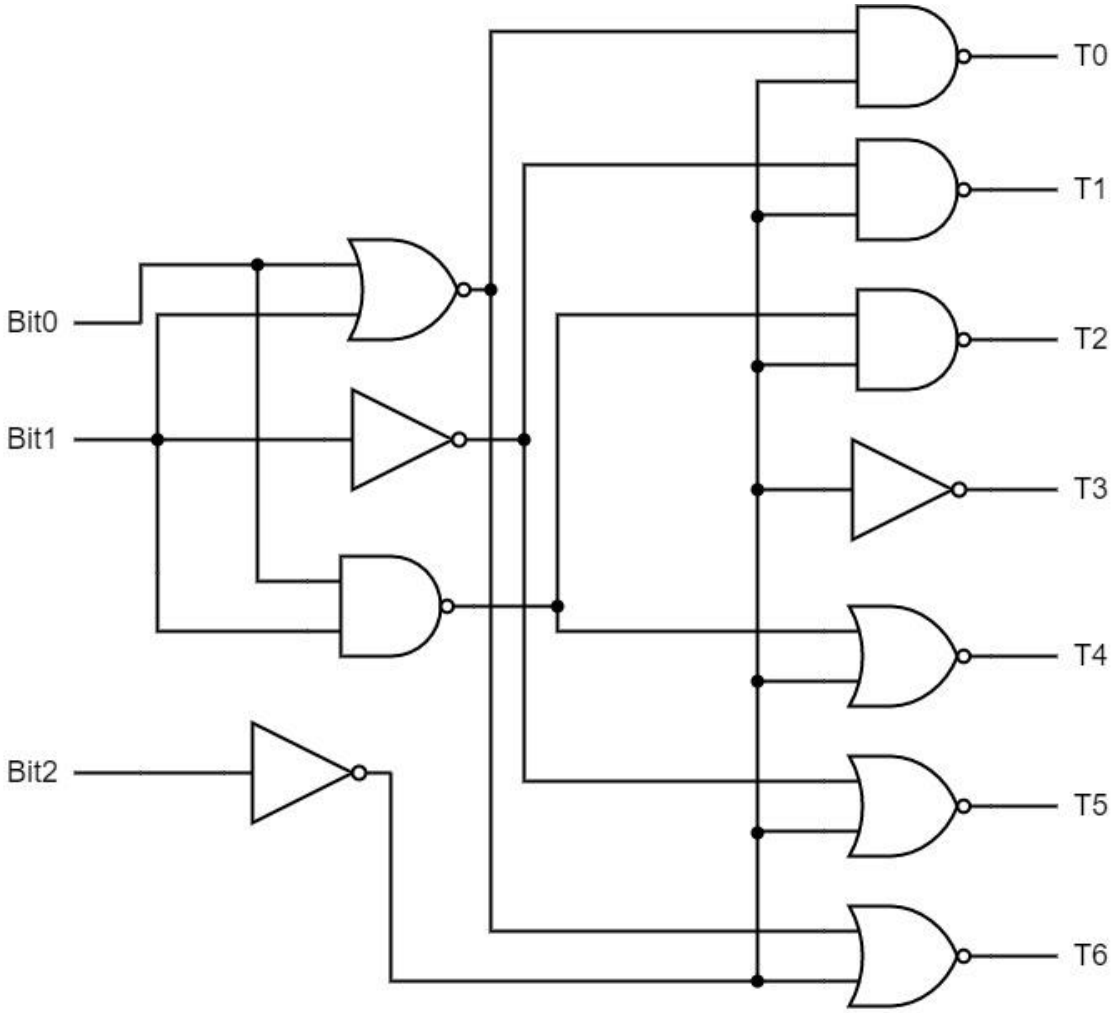

Figure 30: Circuit of a binary to thermometer 3-bit decoder.

As stated in [27] and [28], there are many implementations of a thermometer decoder:

- **Row-Column switching scheme**: As explained in [27], this implementation combines a row decoder with a column decoder. Both have to be optimized separately and, according to [], are not appropriate for 2-D error compensation.
- **Q2 Random Walk**: As explained in [28], this switching scheme is meant to divide current sources into regions resourcing to a two-step hypercritical switching scheme. This switching scheme shows better linearity due to linear error compensation in each region and allows to 2-D space optimization.
- **Custom made decoder**: Besides already existing schemes for thermometer decoders, a designer can always proceed with a custom decoder allowing to target specific optimization solutions for the project in question, mostly useful for high speeds. This

approach requires more effort to design, but allows the designer to verify time constrains and improve dynamic behaviour at every point of the circuit.

2.2.4.1.4 Latency Equalizer

In a segmented DAC, some of the bits go through the decoder (MSBs) and some of the bits don't (LSBs). Since the thermometer decoder brings some delay to the MSBs, a latency equalizer is needed to synchronize the LSBs with the MSBs. This block must be costume made to guarantee the same delay for all bits.

2.2.4.1.5 Latch, Driver and Shifter

The last block to be analyzed are the latches and drivers. The drivers are used to control the switches in each current cell guaranteeing that both switch transistors are not simultaneously on or off. A simple example of a driver can be observed in Figure 31.

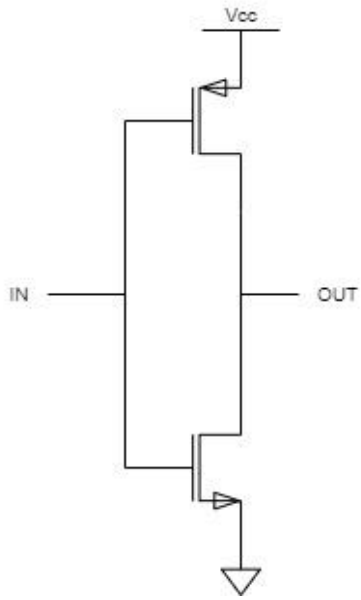

Figure 31: Example of a driver.

The level shifter, as explained in [18], is important to convert the voltages from the digital logic circuits correspondent to the input bits into the appropriate voltages for the analog systems. An example of a level shifter can be seen in Figure 32.

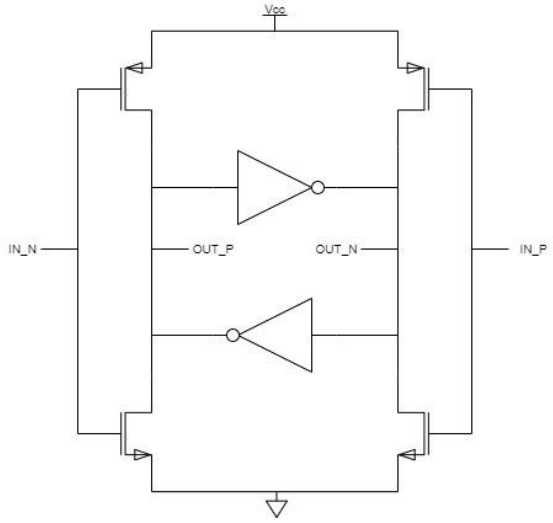

Figure 32: Example of a level shifter.

In between the level shifter and the driver, latches are needed to assure the synchronization and shape of the signal, as explained in [27]. The first latch is meant to receive the output of the shifter when the clock signal is "high" and the second latch gives its own output to the driver when the clock signal is "low". An example of latch can be seen in Figure 33.

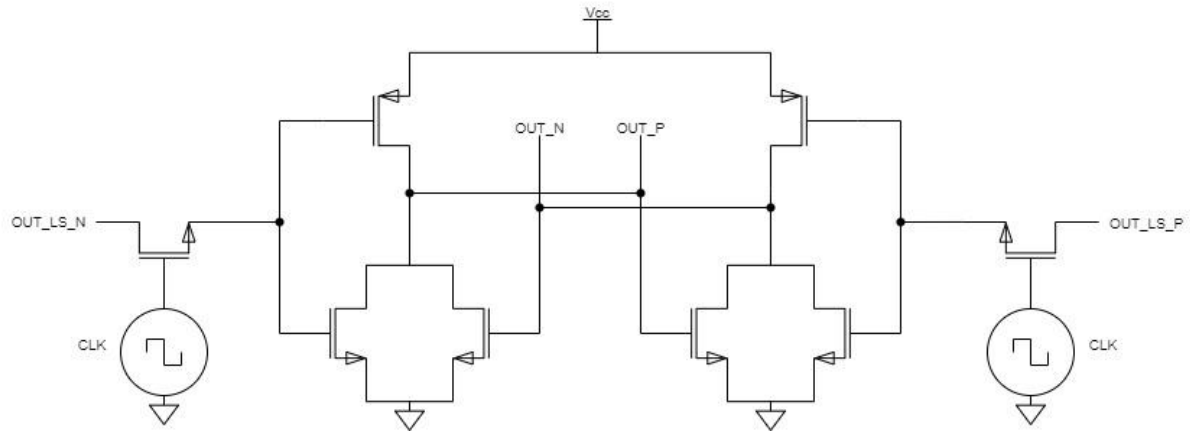

Figure 33: Example of a latch.

2.2.4.1.6 CML Driver

As referred in Section 2.1.2, the last block to be analysed is the CML output driver. As said in [29], CML driver is one of the most important components of a transmitter. In this project, the driver is to be designed in order to accommodate an output impedance of 50Ω in order to correspond to the load impedance of the channel.

The simplest structure of an output driver is based on a differential structure as presented in Figure 34.

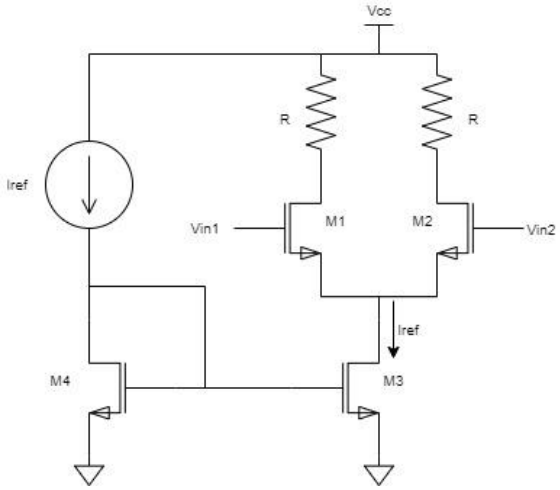

Figure 34: Simple single-stage structure of a CML driver.

However, as explained in [29], in order to increase driving ability and minimize delay, cascade drivers are shown to be a more interesting option. In this case more stages are needed to divide the total delay. An example of a two-levels CML cascade buffer can be observed in Figure 35.

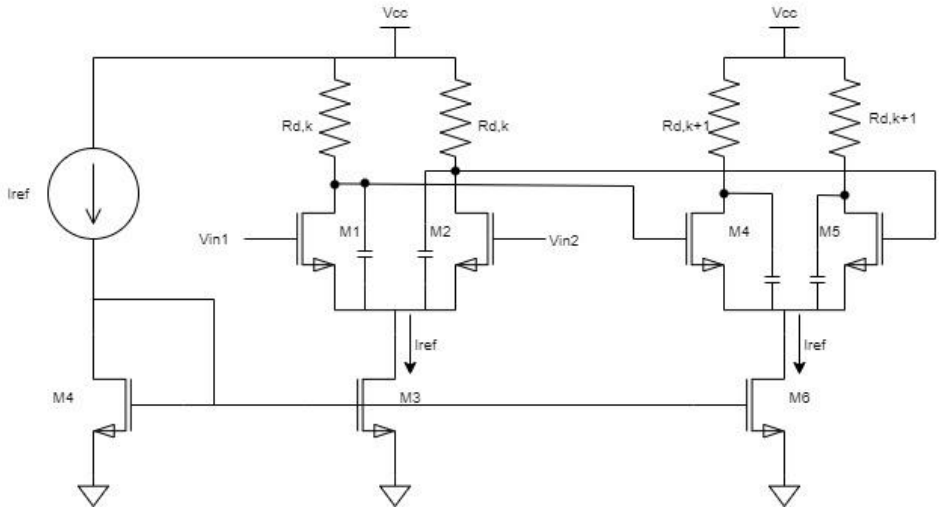

Figure 35: Example of a two-levels CML cascade.

2.2.5 Compensation and Calibration Techniques for Current Steering DACs

Compensation and calibration techniques, as stated in [30], have as main objective to improve static and dynamic linearity of the converter.

2.2.5.1 Compensation Techniques

According to [30], compensation techniques are used to minimize the error of the DAC's output when in correlation to the input bits. Some of these techniques go through:

- "Resampling the output signal", [30];
- "Altering the sampling clock", [30];
- "Modifying the cell structure", [30];
- "Dynamically rearranging the switching sequence", [30].

One of the most interesting compensation techniques studied in [30], due to its simplicity and results, is Always-on-Cascoding. Taking as reference the circuit presented in Figure 36, this technique is only based in keeping the transistors $M_{5,6}$ always bleeding a small current, therefore not allowing them to switch between ON and OFF states. This aims to reduce the output time constant error and improve SFDR.

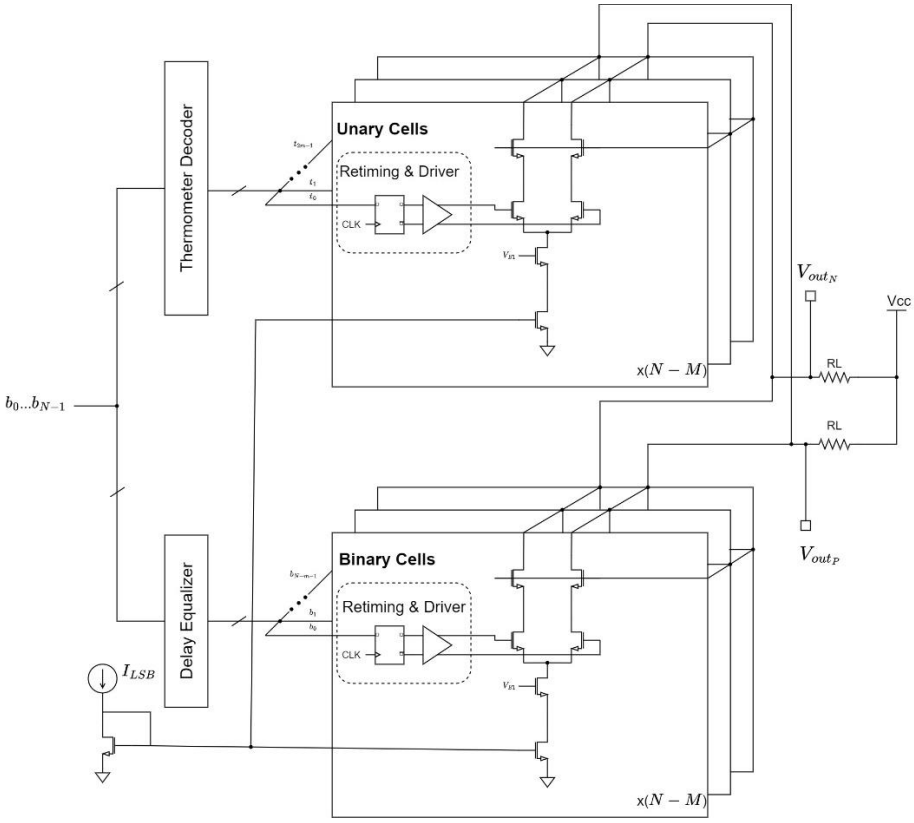

Figure 36: Example of a segmented DAC architecture (adapted from [30])

2.2.5.2 Calibration Techniques

As explained in [30], calibration techniques aim to solve three main problems: output voltage mismatch errors, delay mismatch errors and duty cycle mismatch errors. Through

correcting these problems, the DAC's linearity is to be significantly improved. In this report we will focus in amplitude and delay calibration.

2.2.5.2.1 Amplitude Calibration

As stated in [30], one of the most modern solutions for amplitude calibration is to implement a circuit of switched current sources in parallel with the current cell's transistor as illustrated in Figure 37. This aims to minimize the difference between the current of the current cell and the reference current. These circuit is called Cal-DAC.

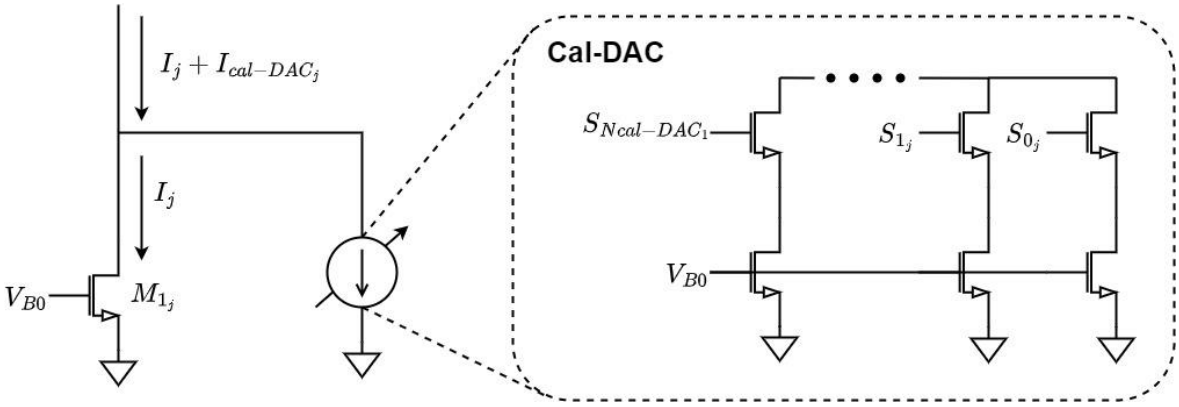

Figure 37:Example of Cal-DAC architecture (adapted from [30])

2.2.5.2.2 Delay Calibration

For delay calibration, following the same thought as for amplitude calibration, one solution is to apply to each current cell a specialized circuit. In this case is proposed by [30], the implementation of a tunable digital delay line between the retiming flip-flop and driver.

2.3 Technology: 16nm CMOS

As described by Moore's Law and corroborated by the past years, the number of transistors in chips has been consistently increased. In line with the increase of silicon density, the transistor size has been consistently decreased over the past years. In this work, there will be used 16nm CMOS (Complementary Metal Oxide Semiconductor) FinFET (fin field-effect) transistors technology for the development of the converter.

2.3.1 FinFET technology

FinFET technology has become more of a standard replacing the conventional MOSFET (metal-oxide-semiconductor field-effect transistors) due to the better performance and power efficiency, as described in [31], opposed to the MOSFET which is described to have reached too much power leakage for little gain in performance, being referred in the same article a benefit of 40% to 50% in performance and a reduction of 50% in power consumption for 16nm and 14nm FinFET technology over 28nm processes.

Today, FinFET technology is manufactured in two main types as explained in [31]: Dual-gate FinFET and Tri-gate FinFET.

2.3.1.1 Dual-gate FinFET

The Dual-gate FinFET is mostly differentiated for using an ultra-thin layer of silicon sitting on top of an insulator. That provides the means to trim excess of silicon and reducing the electrical field from the gate to the fin, as explained in [31]. The structure of the Dual-gate FinFET is presented in Figure 38.

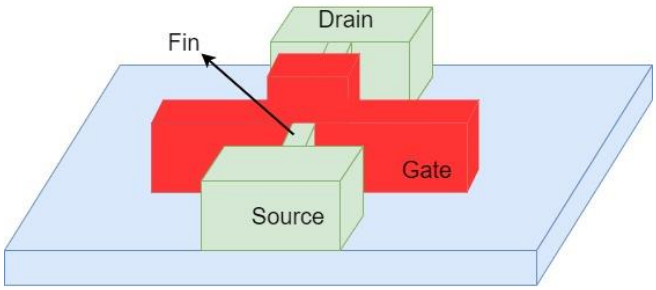

Figure 38: Dual-gate FinFET structure (adapted from [31])

2.3.1.2 Tri-gate FinFET

In the Tri-gate FinFET, the gate wraps around the three sides of the transistor as demonstrated in Figure 39. That change enables transistors to be packed closer together resulting better performance and better energy efficiency, according to [31].

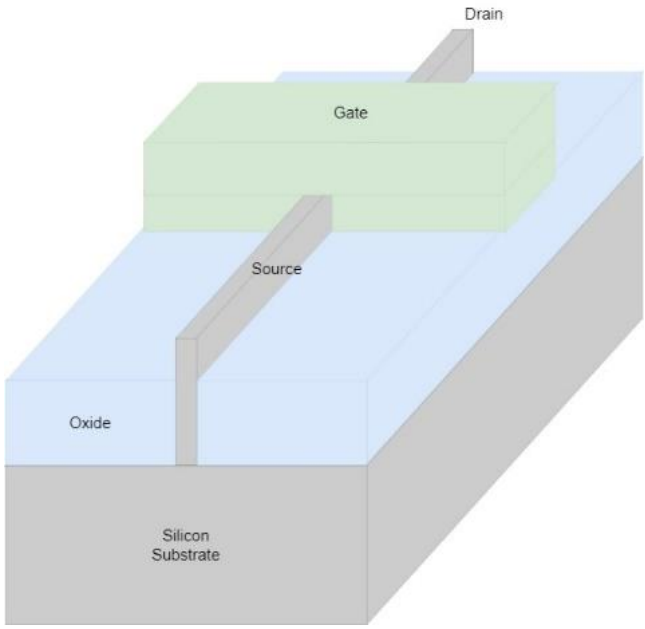

Figure 39: Tri-gate FinFET structure (adapted from [31])

2.3.2 Benefits of FinFET Technology

As explained in [32] and observed in Sections 2.3.1.1 and 2.3.1.2, FinFET technology is three-dimensional, contrasting to conventional MOSFET technology which is planar. This change of structure provides the possibility for better electrostatic control between the drain and the source.

Other benefits of FinFET technology over MOSFET are:

1. "maintaining a steep subthreshold slope", [32].
2. "better performance with bias voltage scaling", [32].
3. "good matching due to low doping concentration", [32].

2.3.3 Challenges and Drawbacks of FinFET Technology

Along with the benefits, FinFET technology brings some new challenges to the table. The first possible drawback, as described in [9] is due to the continual downscaling of transistors resulting in reduced contact area, therefore increasing contact resistance.

As explained in [6], the increased downscaling of the transistors does not only bring challenges to design along with characterization and validation models, but another concern is what is called Corner Effects. One approach to design may be to decrease the width of the

transistor which shows good results in order to reduce short channel effects, but this approach, and as above explained too, may very well increase parasitic resistance between the drain and the source. Another problem is due to three-dimensional structure and the proximity of the gates between transistors reducing, so the sharing of the charge occurs in the corner region of the gates as explained in [31], which can result in premature inversion at the corners. One of the ways to solve this problem, was reduce the oxide thickness and reduce the doping concentration, however, that results in increasing sub-threshold current.

Another concern of FinFET technology is the extraction of FinFET Parasitics as described in [31]. Due to the three-dimensional structure the parasitics can be interpreted as represented in Figure 40. In result, the transistors cannot be modelled only attending to its length and width.

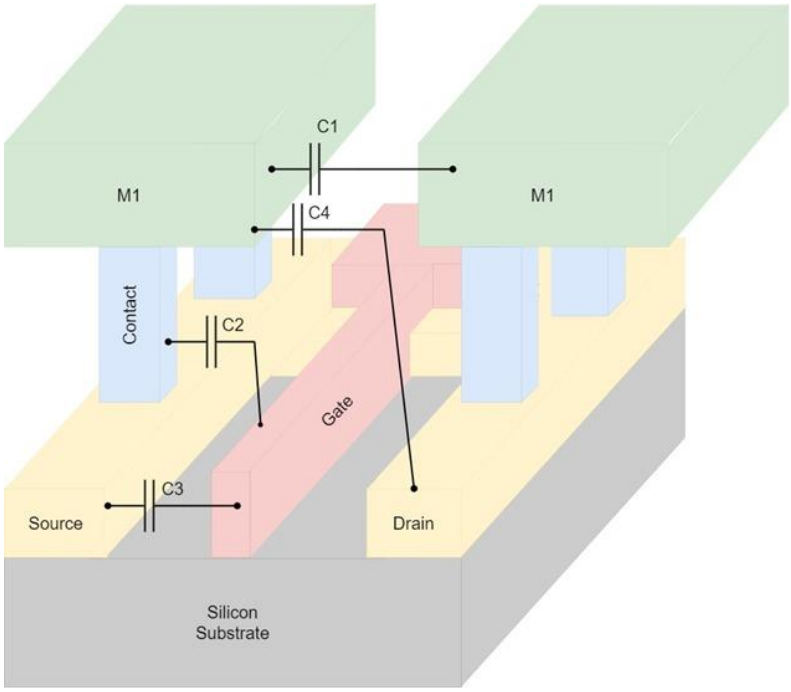

Figure 40: FinFET parasitic capacitances (adapted from [31])

3

DAC DESIGN FOR SERDES

3.1 Design Guidelines

Our design objective is to develop a 4-bit high frequency Current Steering SerDes driver. As presented in Figure 41, this project will be main composed of three main blocks: Digital Input Circuit, 4-bit segmented 2-2 Current steering DAC.

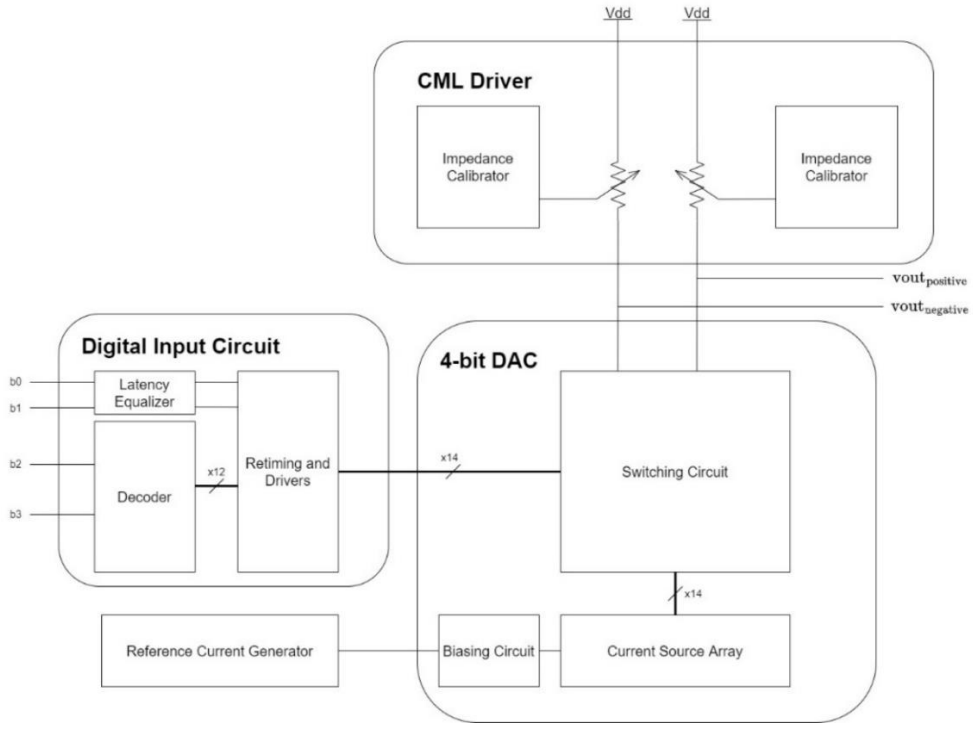

Figure 41: Simplified block diagram of the proposed solution.

The Digital Input Circuit will receive the four input bits where the LSBs will go through a Latency Equalizer and the MSBs will go to a Decoder. The outputs of these two modules will proceed to a Retiming circuit to synchronize all inputs for the Switching Circuit and gate Drivers.

As main requirements for the project the supply voltage cannot exceed 1.2V, the output swing must have a minimum of 0.8V and the frequency of the output signal must reach 10GHz which is equivalent to 20 Gbits/s.

Since the output is to be differential, it is expected to swing between -0.4V and 0.4V. According to equation 15, our LSB voltage will be of 50mV resulting in an ideal conversion represented in Figure 42.

$$LSB = \frac{OS}{2^{nbits}} \tag{15}$$

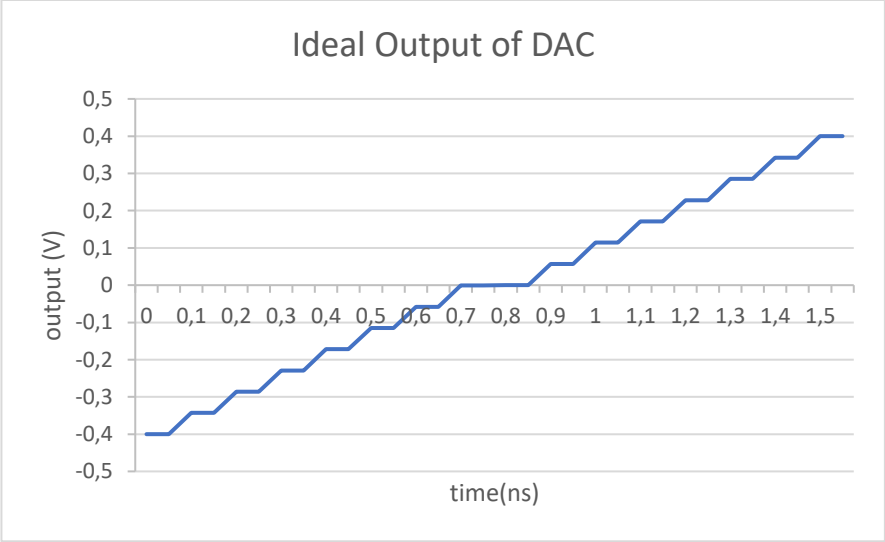

Figure 42: Ideal DAC response for 10GHz sampling.

3.2 Current Source Array

3.2.1 Biasing Circuit

The biasing circuit is as presented in Figure 43 to increase the swing voltage of the output. This architecture allows to reduce the Vds of the transistor N5, therefor increasing the output voltage swing. Analysing Figure 43 we deduce the equation 16, 17 and 18.

$$V_{GS1} = \sqrt{\frac{2I_D(n+1)^2}{\mu_n C_{ox}(W/L)}} + V_{th} = (n+1)\sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}} + V_{th} = (n+1)V_{eff} + V_{th} \quad (16)$$

$$V_{GS2} = \sqrt{\frac{2I_D(n)^2}{\mu_n C_{ox}(W/L)}} + V_{th} = n\sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}} + V_{th} = nV_{eff} + V_{th} \quad (17)$$

$$V_{DS3} = V_{GS1} - V_{GS2} = (n+1)V_{eff} + V_{th} - nV_{eff} - V_{th} = V_{eff} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}} \quad (18)$$

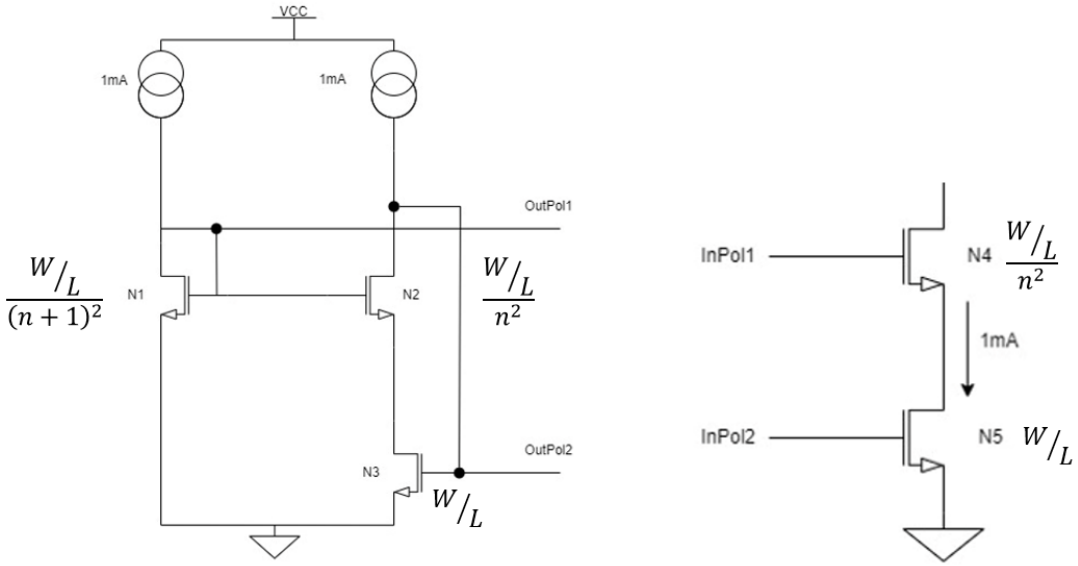

Figure 43: Schematic of a wide swing current mirror.

The n value chosen was 2, so not to increase to much the size of the N5 but still being able to maintain a good mirroring. This way we can reduce the size of N4 and, therefore, decrease the parasitic capacitances of the output node of the current source and resulting in the dimensioning presented in Table 4.

Table 4: Transistor dimensioning of the biasing circuit.

Transistor	Fingers	Fins	Multiplicity
N1	1	5	4
N2	1	5	15
N3	1	5	60

3.2.2 1LSB

All the current sources are constituted by two modules: the current mirror and the switching circuit. The current mirror is a simple cascode for a more accurate mirroring composed of two transistors being the top transistor smaller and the bottom transistor bigger in order to reduce the parasitic capacitances at the output node and still maintaining a good mirroring as explained in Section 3.2.1. Both transistors must work on saturation. The switching circuit is composed by two transistors working as switches and 200Ω resistors between any active components and the output node working as a secondary ESD protection. Due to the minimal acceptance width for the technology of resistors and maximum current density allowed on them, for the 1 LSB circuit, the switching circuit is composed by four identical circuits in parallel as represented in Figure 44.

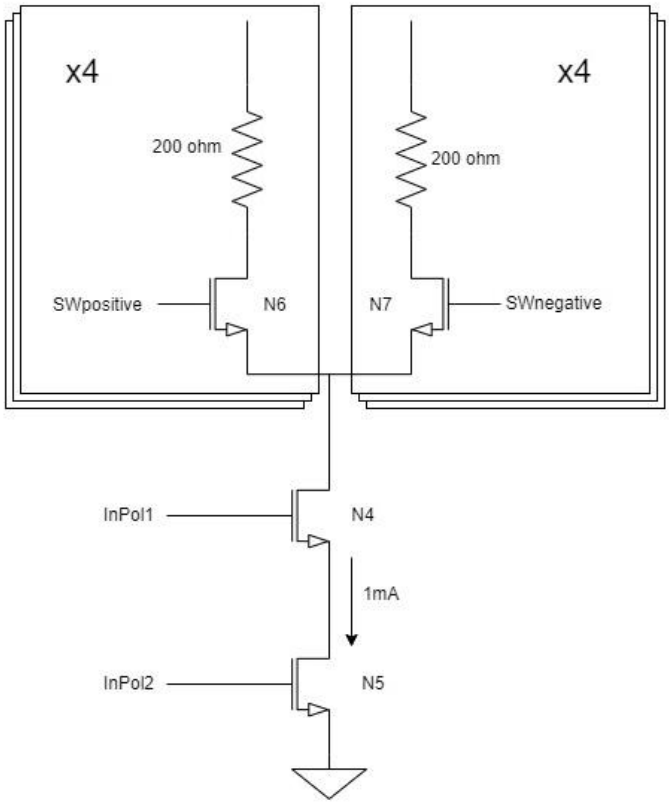

Figure 44: Schematic representation of the 1LSB module.

The polarization of the cascode was made to match the transistors N4 to N2 and N5 to N3, therefor giving to the dimensions presented in Table 5. As presented in Figure 45, the sum of the Vds's of transistors N4 and N5 is 0.05V, the lost voltage at the protection resistors is 0.05V and the pretended output swing is 0.8V, resulting in a pretended Vds of N6 is 0.2V.

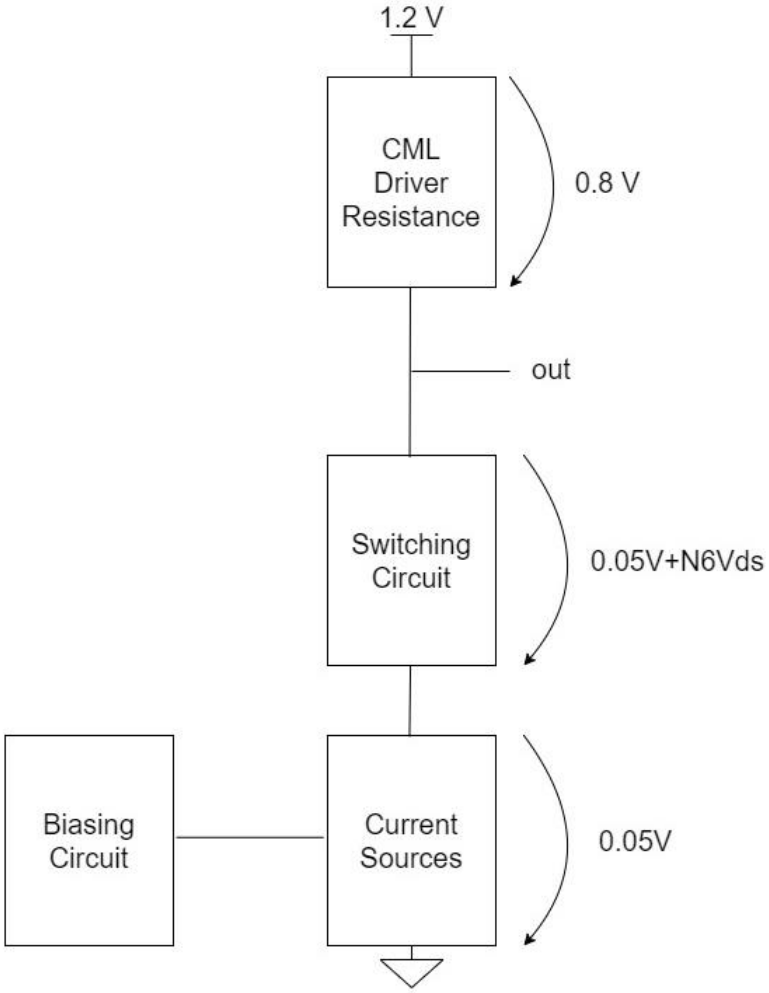

Figure 45: Block Diagram for the sizing of the switching circuit transistors.

Table 5: Transistor dimensioning of current sources and switching circuit for 1LSB module.

Transistor	Fingers	Fins	Multiplicity
N4	1	5	15
N5	1	5	60
N6	8	1	5
N7	8	1	5

After the dimensioning the transistors, a Monte Carlo analysis was made resorting to 100 iterations and an ideal reference current flowing through the biasing circuit and obtaining the results presented by the Figure 46.

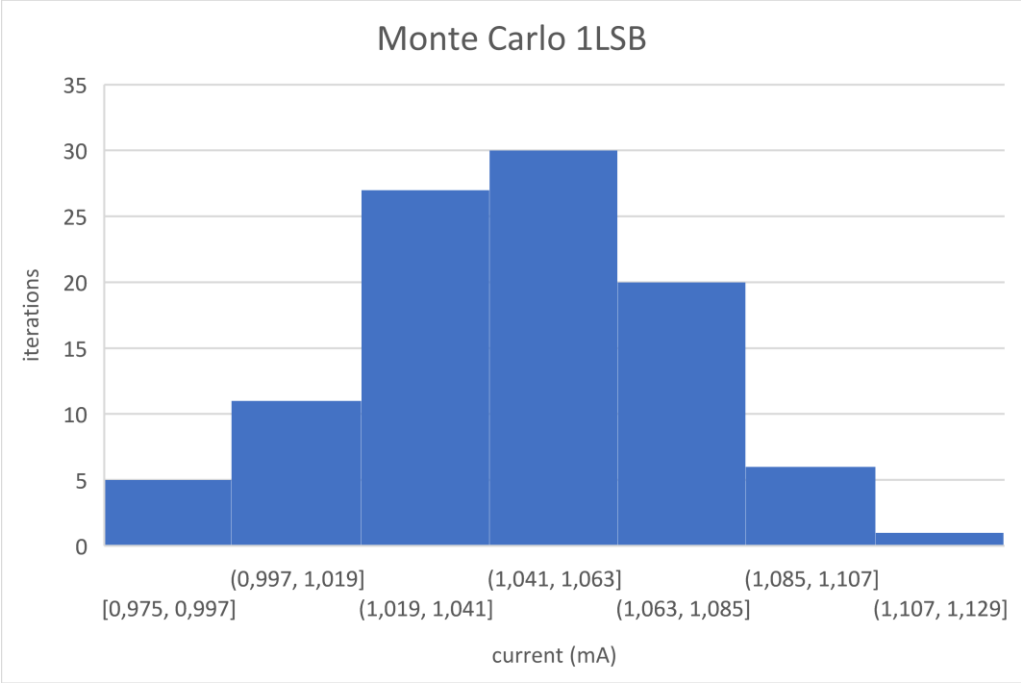

Figure 46: Monte Carlo analysis of the output current of the 1LSB module.

Analysing the histogram in Figure 46 we can interpret the results presented in Table 6.

Table 6: Results from the Monte Carlo analysis of the output current of the 1LSB module.

μ (mA)	σ (mA)	3σ (mA)	$\left({}^{3\sigma}/_{\mu} \times 100\right)$(%)
1.05	0.0285	0.0855	8%

3.2.3 2LSB

The implementation of the 2LSB module is similar to the 1 LSB but scaling the cascode transistors to double the size and using 8 switching circuits in parallel instead of 4 to respect the limitations above discussed. Therefor resulting in the dimensions presented at Table 7.

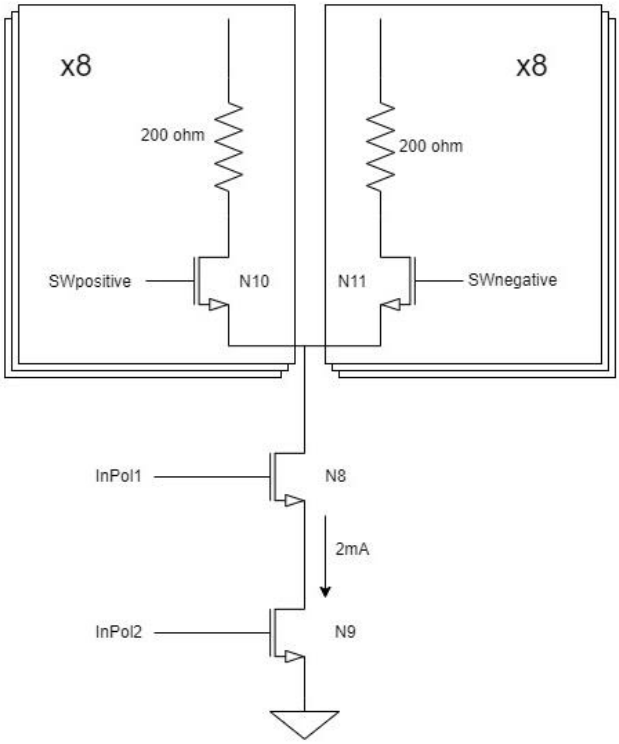

Figure 47: Schematic representation of the 2LSB module.

Table 7: Transistor dimensioning of current sources and switching circuit for 2LSB module.

Transistor	Fingers	Fins	Multiplicity
N8	1	5	30
N9	1	5	120
N10	8	1	5
N12	8	1	5

After the dimensioning the transistors a Monte Carlo analysis was made resorting to 100 Iterations and obtaining the results presented by the Figure 48.

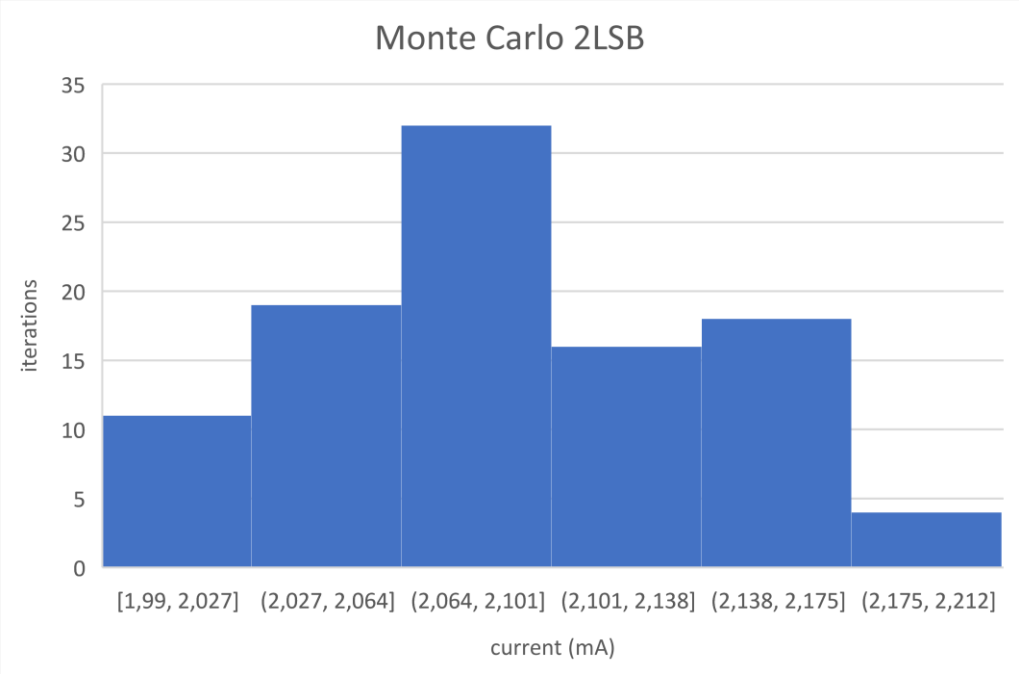

Figure 48: Monte Carlo analysis of the output current of the 2LSB module

Analysing the histogram in figure 48 we can interpret the results presented in Table 8.

Table 8: Results from the Monte Carlo analysis of the output current of the 2LSB module.

μ(mA)	σ(mA)	3σ(mA)	$(3\sigma/\mu \times 100)$(%)
2.09	0.0496	0.1488	7.2%

3.2.4 4LSB

Since we opted for a segmented approach, the 4LSB module is unary and made of four 1LSB modules in parallel as presented in Figure 49.

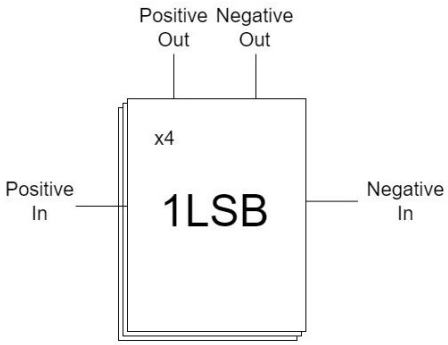

Figure 49: Simplified block representation of the 4LSB module.

The Monte Carlo analysis, resorting to 100 Iterations, allowed us to obtain the results presented by the Figure 50.

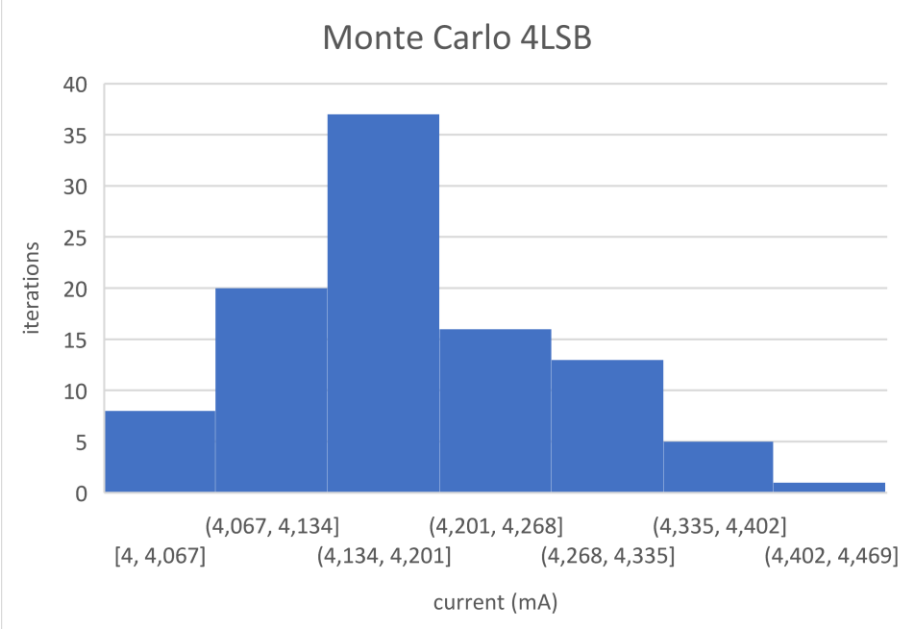

Figure 50: Monte Carlo analysis of the output current of the 4LSB module.

Analysing the histogram in Figure 50 we can interpret the results presented in Table 9.

Table 9: Results from the Monte Carlo analysis of the output current of the 4LSB module.

μ(mA)	σ(mA)	3σ(mA)	$\left({}^{3\sigma}/_{\mu} \times 100\right)$(%)
4.19	0.0891	0.267	6.4%

3.2.5 8LSB

Similar to the 4LSB module, the 8 LSB module is also unary made or two 4LSB modules in parallel as presented in Figure 51, which is equivalent to eight 1LSB modules in parallel.

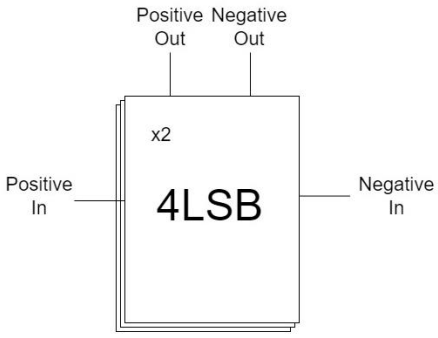

Figure 51: Simplified block representation of the 8LSB module.

The Monte Carlo analysis, resorting to 100 Iterations, allowed us to obtain the results presented by the Figure 52.

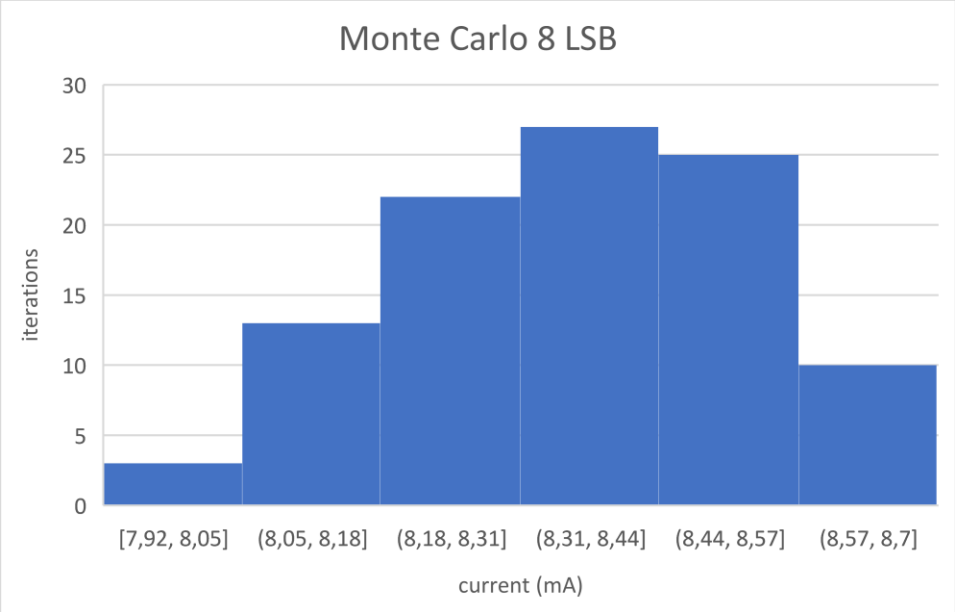

Figure 52: Monte Carlo analysis of the output current of the 8LSB module.

Analysing the histogram in Figure 52 we can interpret the results presented in Table 10.

Table 10: Results from the Monte Carlo analysis of the output current of the 8LSB module.

μ(mA)	σ(mA)	3σ(mA)	$\left({}^{3\sigma}/_{\mu} \times 100\right)$(%)
8.37	0.166	0.498	5.9%

3.2.6 Results

Analysing the results of the four modules we can establish the real LSB current do be 0.91mV instead of the ideal 1mA, resulting in an error of 9%. However, if we consider the real error $\left({}^{3\sigma}/_{\mu} \times 100\right)$(%), the maximum error is 8% which is below the 10% considered maximum for this project. At the end, the characteristic of the DAC is presented at Figure 53.

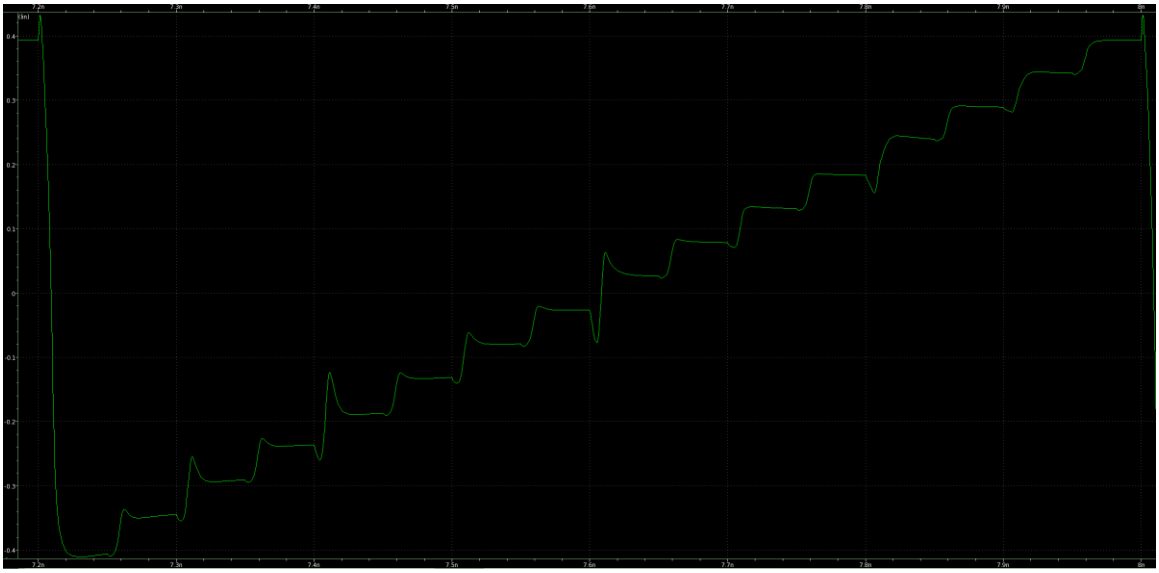

Figure 53: DAC response for 10GHz sampling.

From the values taken from Figure 53, we can conclude the real LSB voltage to be 53.5mV resulting in an output voltage swing of 0.803V and an output from -0.41V to 0.393V. In Figures 54, we can observe the INL and DNL analysis of the converter obtaining a maximum DNL of 0.1582 LSB and a maximum INL of 0.2042 LSB.

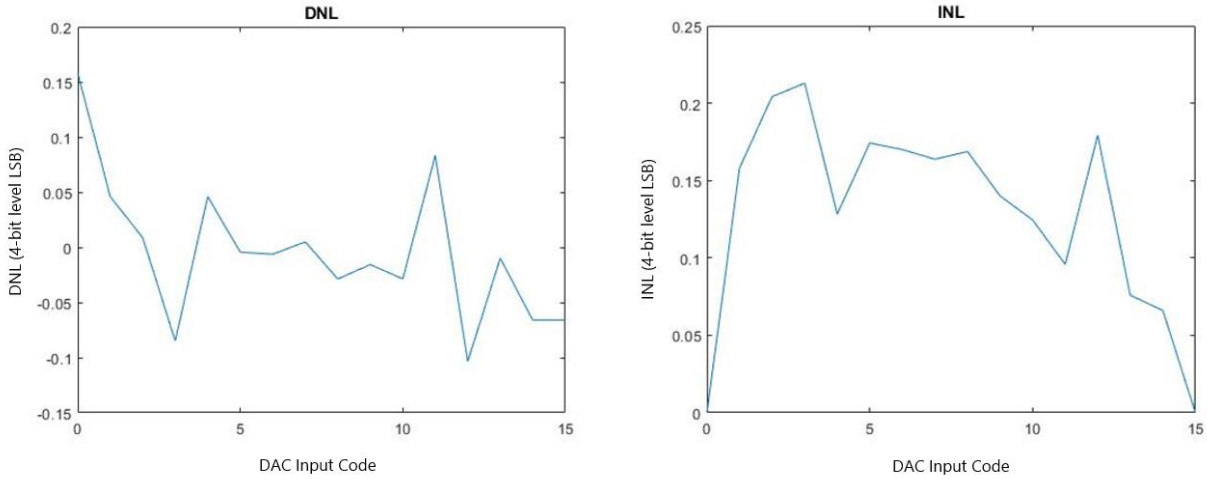

Figure 54: a) INL analysis of the DAC; b) DNL analysis of the DAC.

3.3 CML Driver

A typical CML Driver is as presented in Figure 55, composed by two switching transistors and two resistors connected do the transmission line.

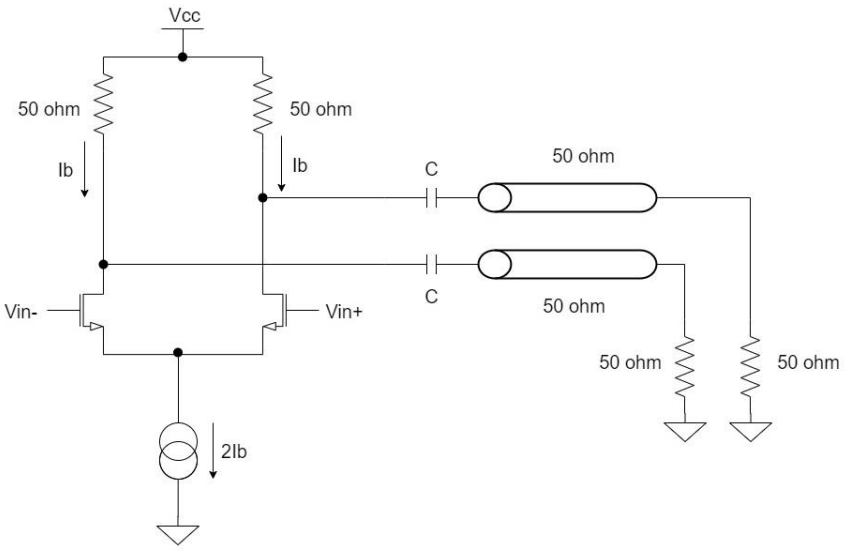

Figure 55: Schematic representation of a typical CML Driver.

However, since in Sections 3.1.2 to 3.1.5 we decided to include the switching transistors on the Current Source modules, our CML Driver can be represented as in Figure 56.

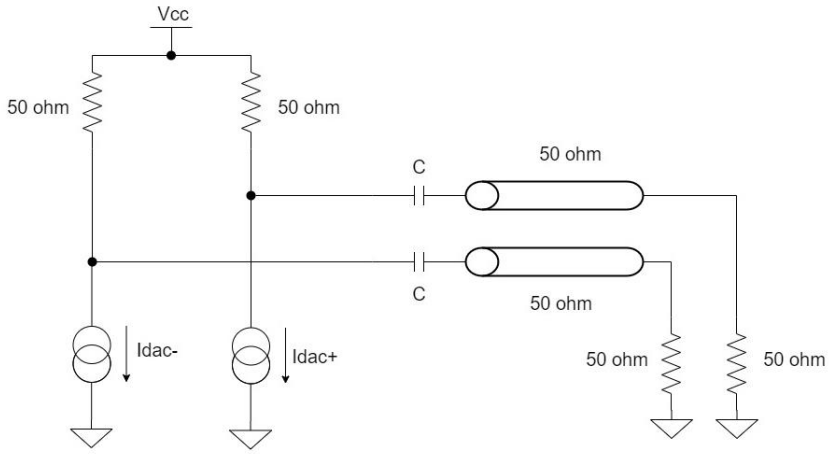

Figure 56: Schematic representation of the CML Driver implemented.

Since the project is meant for high frequencies, the CML Driver behaviour can be interpreted as presented in Figure 57, being this representation used for test benching in this project.

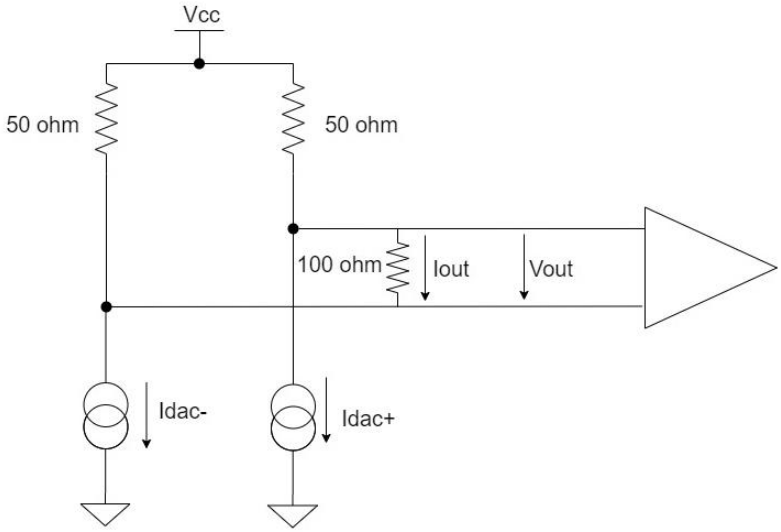

Figure 57: Equivalent schematic representation of the CML Driver implemented for high frequencies.

One of the most important analysis of the converter is the Corner Analysis to identify its behaviour in different circumstances such as: different types of behaviour of the transistors and the resistors and the difference of temperature in which the converter is working. So, the

different corners to be analysed are as presented in Table 11. The results for the characteristic of the converter can be seen in Figure 58 and the deviation of resistance values for the resistors of the CML Driver can be seen in Figure 59.

Table 11: Corners utilised for corner analysis.

	Corners	Typical
LVT MOS	Fast-fast, slow-slow, fast-slow, slow-fast	Typical-typical
Resistors	High, low	Typical
Temperature	-40, 125	25

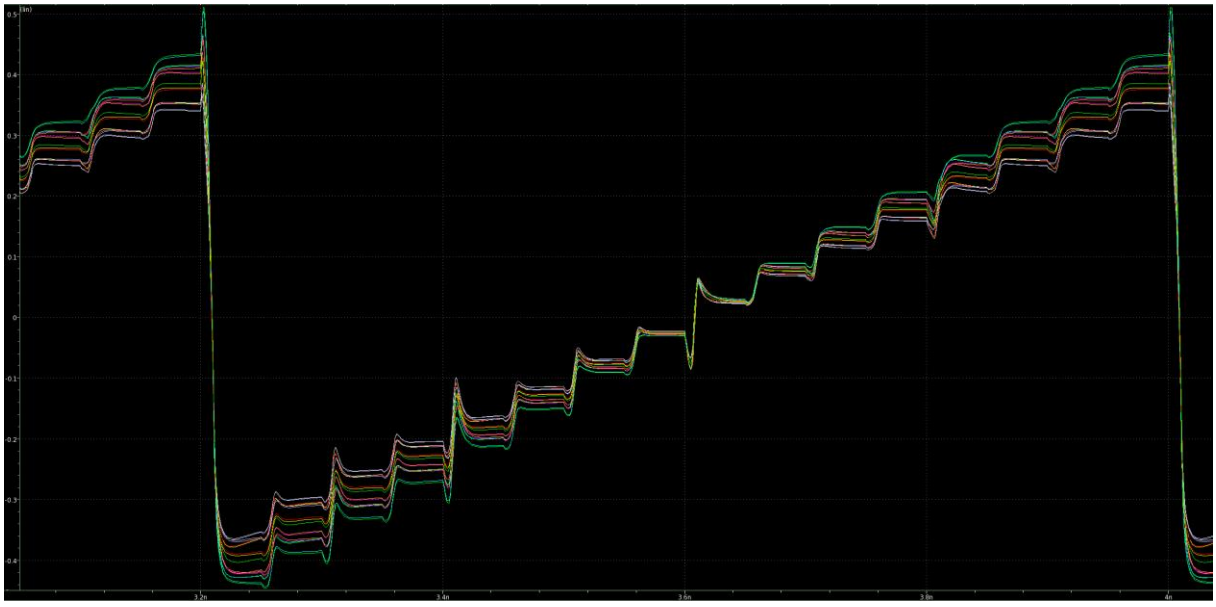

Figure 58: DAC response for 10GHz sampling and 17 corners.

As we can observe, the deviation between corners can reach up to 2 LSB so output impedance calibration shows to be necessary.

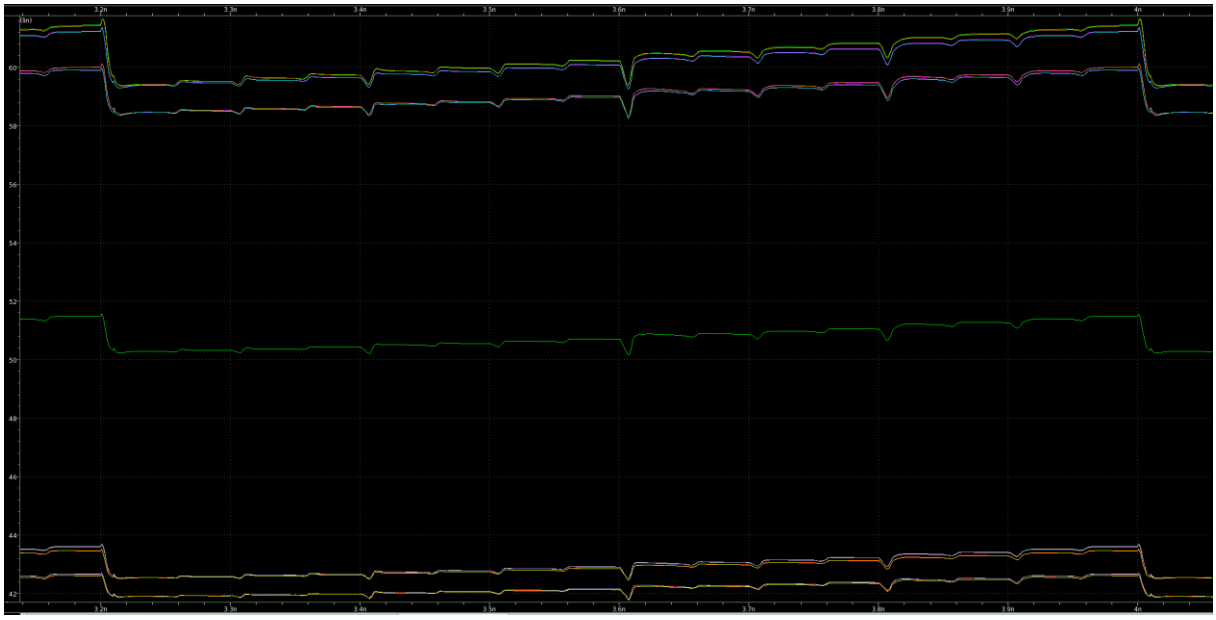

Figure 59: Output impedance of the DAC for 17 corners.

Table 12: Results of output impedance for 17 corners.

Corners	Best Corner	Worst Corner
Output Impendance	51Ω	62 Ω

Also, we can observe that the resistances of the CML Driver deviate from around 42 Ω and 62Ω giving an error of 12 Ω. However, the maximum error allowed is 3.3Ω according to equation 19.

$$R_{maximum_{error}} = \frac{V_{LSB}}{I_{DAC\_max}} = \frac{50mV}{15mA} = 3.3\Omega \quad (19)$$

3.3.1 Calibrator

The chosen CML Driver Resistance Calibrator is composed to an ideal 50 Ω resistor, two variable resistors, a comparator and a SAR Logic Module as shown is Figure 60.

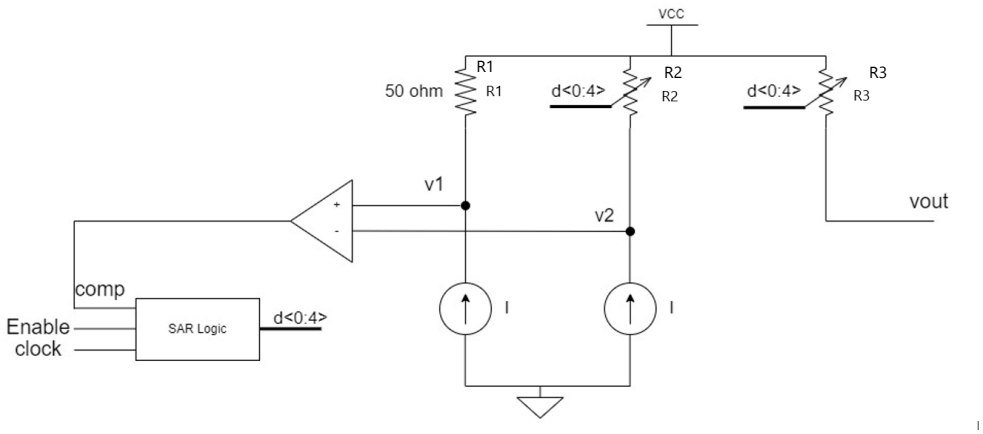

Figure 60: Simplified schematic representation of the CML Driver impedance calibrator.

Fistly, R1 and R2 resitors have the same current flowing creating the voltages v1 and v2. These voltages are compared and the result sent to the SAR Logic Unit, outputting a 5 bit result (d<0:4) which Is used to calibrate R2. This loop repeats until v1=v2, which menas R1=R2. This same calibration Is replicated In R3, which Is the real resistance of the CML Driver.

The variable resistor is made of six arrays of resistors in parallel controlled by switching transistors which are controlled by the bits from the SAR Logic Unit as represented in Figure 61.

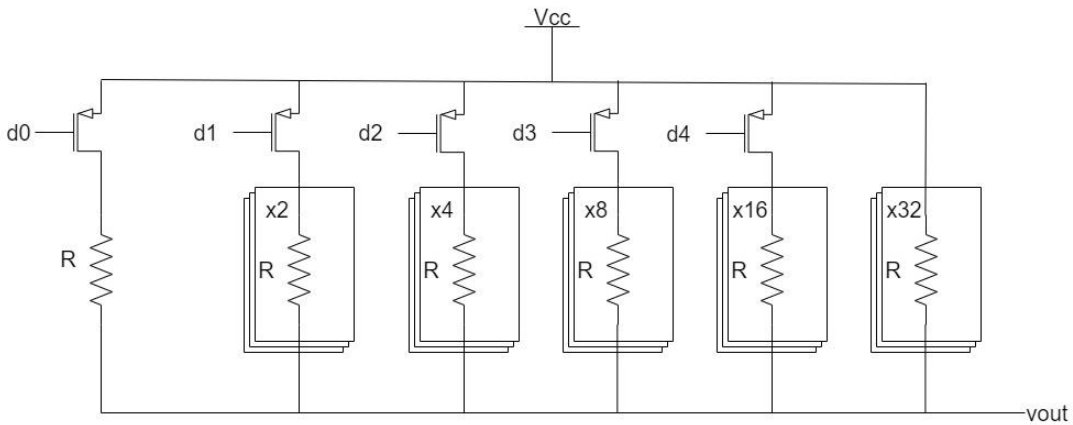

Figure 61: Schematic representation of the variable resistor of the CML Driver.

In way to have the 50 Ω resistance when the calibrator code is in the middle (code=10000), in order to be able to calibrate from lower or higher resistance values, the R value was established as presented by equation 20.

$$\frac{R}{16} // \frac{R}{32} = 50\Omega \Leftrightarrow \frac{\frac{R}{16} \times \frac{R}{32}}{\frac{R}{16} + \frac{R}{32}} = 50\Omega \Leftrightarrow \mathrm{R} = 2.4\mathrm{k}\Omega \quad (20)$$

However, to respect maximum current density allowed by the technology, each resistor was made do be two resistors in parallel with the value of $4.8\mathrm{k}\Omega$.

Other Important design decision was the number of bits of the calibrator in order to guarantee every bit was used. According to equations 21, 22 and 23, the less significant bit has an effect of 2.3Ω which is close to the error allowed of 3.3Ω.

$$R // \frac{R}{32} = 72.7\Omega \quad (21)$$

$$\frac{R}{32} = 75\Omega \quad (22)$$

$$75\Omega - 72.7\Omega = 2.3\Omega \quad (23)$$

Table 13: Corners utilised for corner analysis.

Parameters	Corners	Typical
High voltage MOS	Fast-fast, slow-slow, fast-slow, slow-fast	Typical-typical
Low Vt MOS	Fast-fast, slow-slow, fast-slow, slow-fast	Typical-typical
Resistors	High, low	Typical
Temperature	-40, 125	25

Table 14: Results of calibrated output impedance for 65 corners.

Corners	Best Corner	Worst Corner
Output Impendance	50.01Ω	51.92Ω

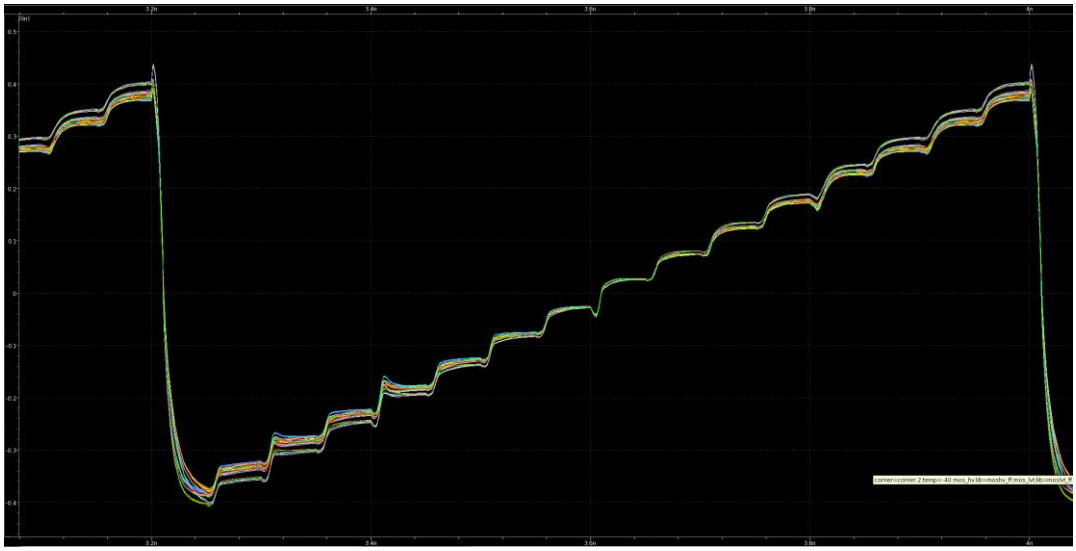

Figure 62: DAC response for 10GHz sampling and 65 corners after impedance calibration.

We can observe in Figure 62, that the corners become closer to each other resulting in a deviation lower than 1 LSB from the two extreme corners. The behaviour of the calibrator can be shown in figure 63, where we observe all the resistors starting uncalibrated (code 00000 of the SAR Logic Unit) and then converging to the 50 Ω desired.

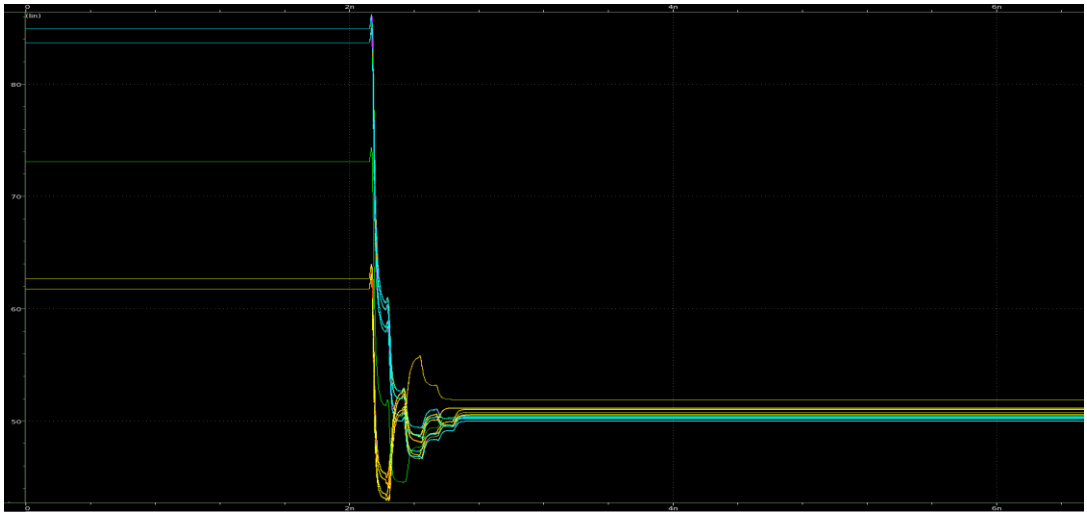

Figure 63: Output impedance during calibration for 65 corners.

3.4 Retiming and Drivers

As presented in Figure 36, Section 2.2.51, before the bits activate the gates of the switching transistors, they go through a retiming and driver modulo composed by a flip flop type D and a driver. The flip flop also allows to get the inverted bit for the negative switch.

The flip flop is composed by NAND modules and an INV module as presented in Figure 64 and each modules CMOS design presented in Figure 65.

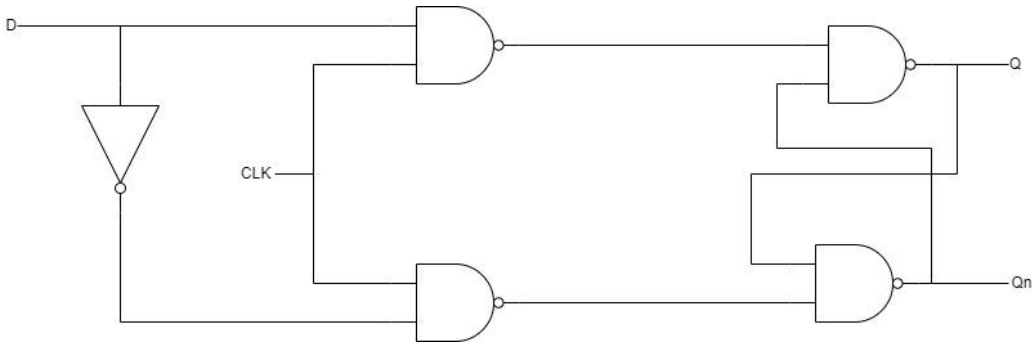

Figure 64: Schematic representation of a Flip Flop D.

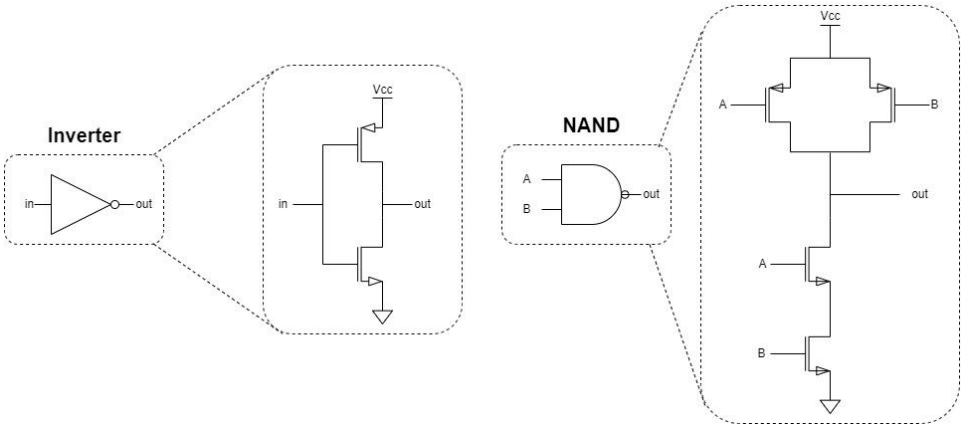

Figure 65: Schematic representation of Inverter and NAND modules.

We can observe the results of the outputs b0, b1, t0 and t11 in Figure 66, beavering according to Table 15, which are the codes utilized to test the circuit in order to get the characteristic of the converter.

Table 15: Expected outputs retiming circuit.

Bit 0	Bit 1	Bit 2	Bit 3	B0	B1	T0	T11
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

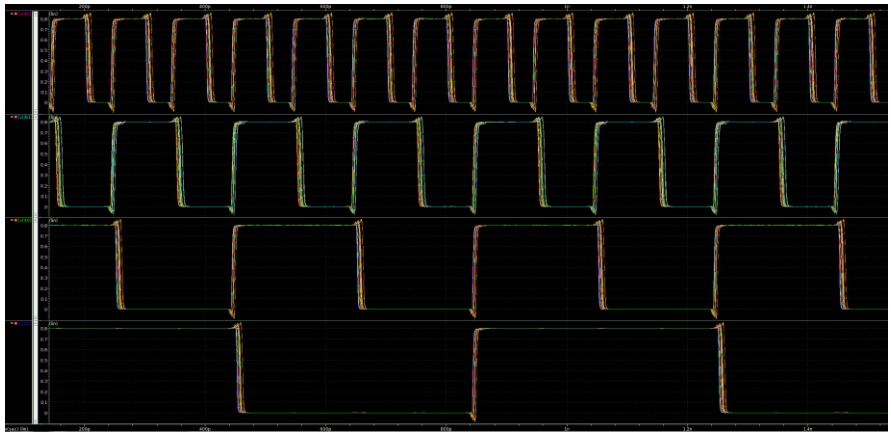

Figure 66: Output voltages of signals b0, b1, t0 and t11 of the retiming and drivers module.

3.5 Reference Current Generator

The reference current generator used is based on a V-I converter presented in [34] as presented in Figure 67. It is composed by a Operational Transconductance Amplifier (OTA) which polarizes two transistors (M1 and m2), a resistor a then two cascode current mirrors (NMOS and PMOS).

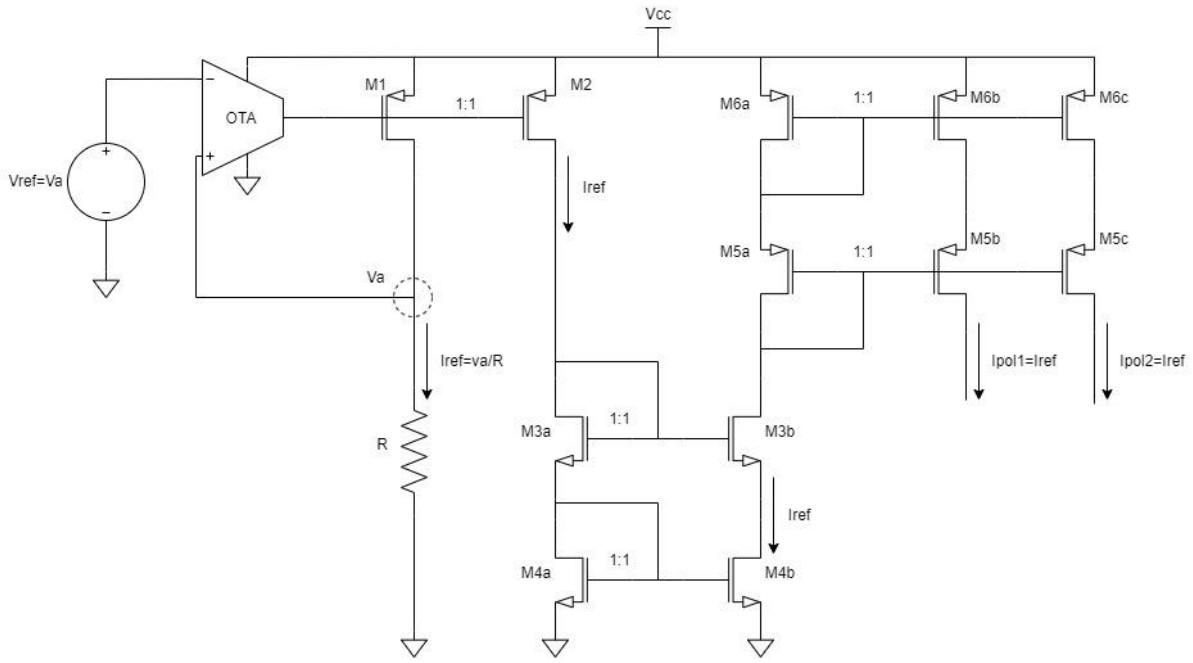

Figure 67: Schematic representation of the reference current generator.

The OTA forces the two inputs to have the same value (Vref and Va) due to its high input impedance. Then, with a fixed Va, the resistor R defines the current in M1. Establishing the V_{DS} and the drain current of M1, therefor defining a polarization voltage from the OTA. This same polarization voltage polarizes M2 resulting in an equivalent drain current for M2. This current is mirrored by the fist cascode current mirror (M3 and M4) and the mirror again by the second cascode current mirror (M5 and M6).

However, as we can observe in figure 62, our output swing is below the 0.8V required. Since the models used in this work (low voltage threshold) allow us to have the transistors working on lower V_{DS} and still in saturation.

3.5.1 OTA

From analysing our circuit and utilization, we can deduce that the gain and bandwidth of the OTA is not much relevant. What is relevant is a good polarization of the transistors so the circuit may work properly and increasing the output and input impedances. So, the designed OTA for this work is as represented in Figure 68 proposed by [35].

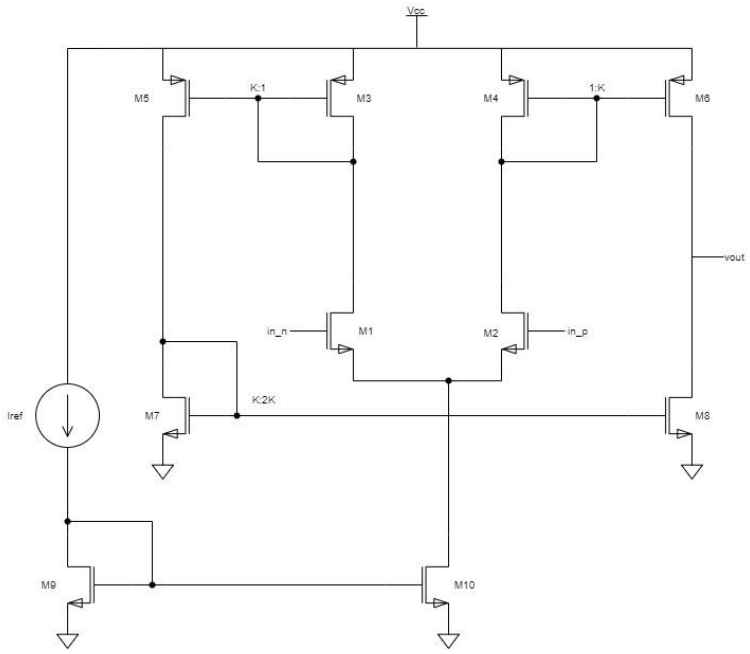

Figure 68: Schematic representation of the OTA circuit.

This architecture is governed by the equations 24, 25 and 26.

$$A_{v0_{OTA}} = \frac{g_{m1}}{g_{ds6} + g_{ds8}} \tag{24}$$

$$r_{out} = \frac{1}{g_{ds6} + g_{ds8}} \tag{25}$$

$$GBW_{OTA} = K\frac{g_{m1}}{2\pi C_{out}} \tag{26}$$

3.5.2 Results

As we can observe in Figure 69 and Table 16, resourcing to a Monte Carlo analysis with 100 iterations, the standard deviation error considering 3σ, is below the 10% maximum recommended and with a mean above the value of 1LSB (1mA).

In Figure 70 we can observe the 16 extreme corners of a corner analysis with 221 corners. From these results we can observe a clear difference between corners utilizing a fast-fast model for LVT transistors and corners utilizing a slow-slow model for LVT transistors. This allows us to conclude a clear sensibility of the circuit for LVT processes.

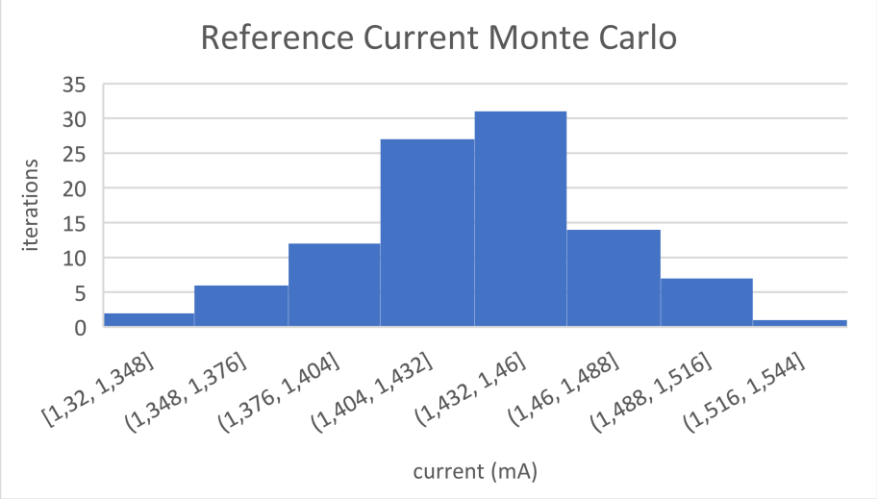

Figure 69: Monte Carlo analysis of the output current of the reference current generator.

Table 16: Results from the Monte Carlo analysis of the output current of reference current generator.

μ (mA)	σ (mA)	3σ (mA)	$\left({}^{3\sigma}/_{\mu} \times 100\right)$(%)
1.4	0.0376	0.1128	8%

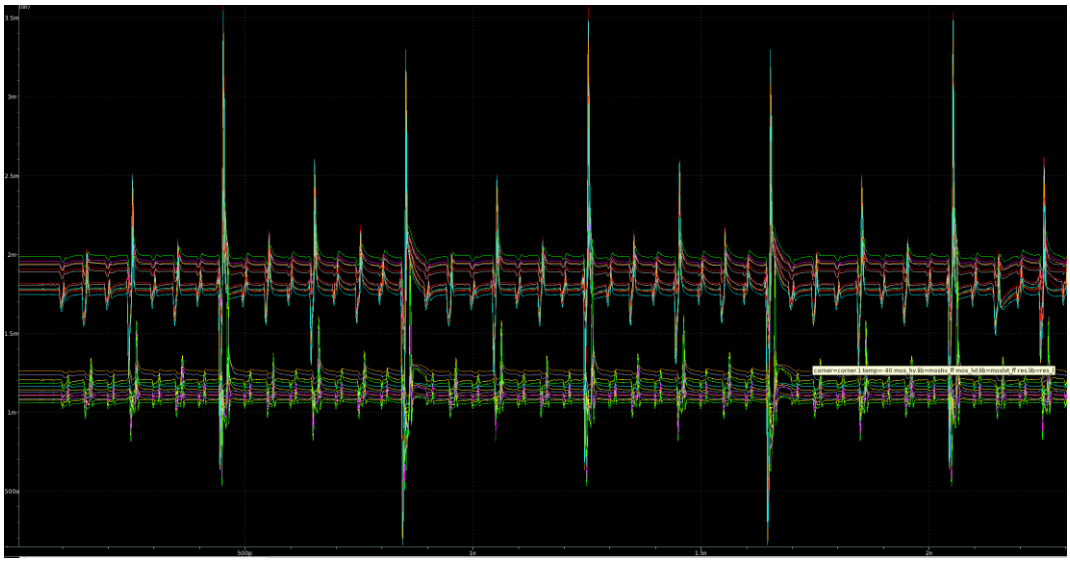

Figure 70: Output current of the reference current generator for the 32 extreme corners.

3.6 Decoder and Latency equalizer

The final module to be conceived is the decoder. The objective is to develop the decoder and the latency equalizer. The decoder will read the two MSBs (bit 2 and bit 3) and convert them into twelve outputs (t0 to t11) connecting to the unary current sources. The latency equalizer is a simple circuit to make sure all bits arrive at the same time to the laches and drivers. Both these circuits can be illustrated as in Figure 71.

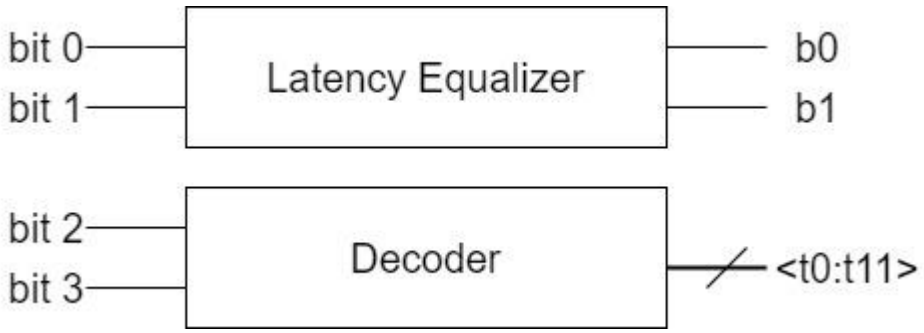

Figure 71: Simplified block diagram for the decoder and latency equalizer module.

To develop the decoder, a truth table was used as presented in Table 17 and resulting in equations 27, 28 and 29.

Table 17: Truth table of the decoder.

Bit3	Bit2	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0	0	0	0	0
1	0	1	1	1	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1

$$t_0 = t_1 = t_2 = t_3 = (B_2 \cdot B_3) \tag{27}$$

$$t_4 = t_5 = t_6 = t_7 = B_3 \tag{28}$$

$$t_8 = t_9 = t_{10} = t_{11} = (B_2 + B_3) \tag{29}$$

For simplification on implementation, only NAND, NOR and INV logic gates will be used resulting in the circuit presented in Figure 72.

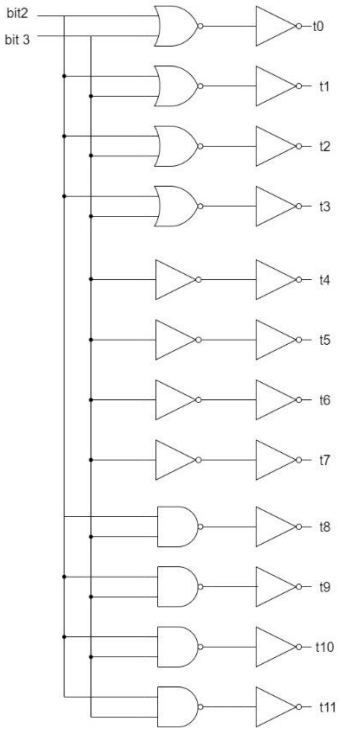

Figure 72: Schematic representation of the decoder.

The results of the decoder can be observed in Figure 73, where we can observe the bits 2 and 3 changing according to Table 18 and then the outputs of t0, t4 and t8 working as expected.

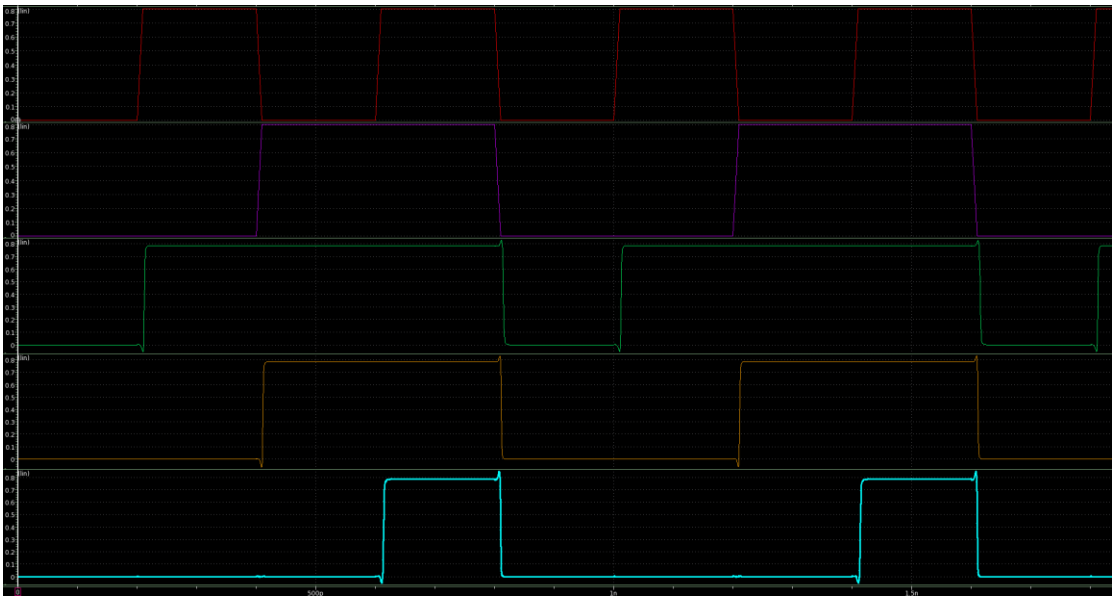

Figure 73: Output voltages of the decoder for signals t0 (green), t4 (orange) and t8 (blue).

The latency equalizer is only composed of two inverters so the latency of the LSBs are approximate to the latency of the MSBs. The latency equalizer can be represented as in Figure 74.

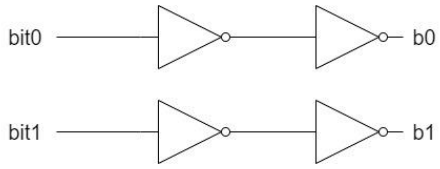

Figure 74: Schematic representation of the latency equalizer.

3.7 Design Final Results

3.7.1 Time Domain Analysis

For analysing the results, the two primary methods use will be Monte Carlo Analysis with 100 iterations and a reference temperature of 25^oC and Corner Analysis with 225 corners so to evaluate every possible variation regarding the process and the behaviour of the circuit with a variation of temperature between -40^oC and 125^oC.

The first analysis is the Monte Carlo analysis of the current sources of 1LSB and 2 LSB and then also the sum of all current sources when all bits are active. The results of this analysis are presented in Tables 18, 19 and 20 with its graphical representation in Figures 75, 76 and 77.

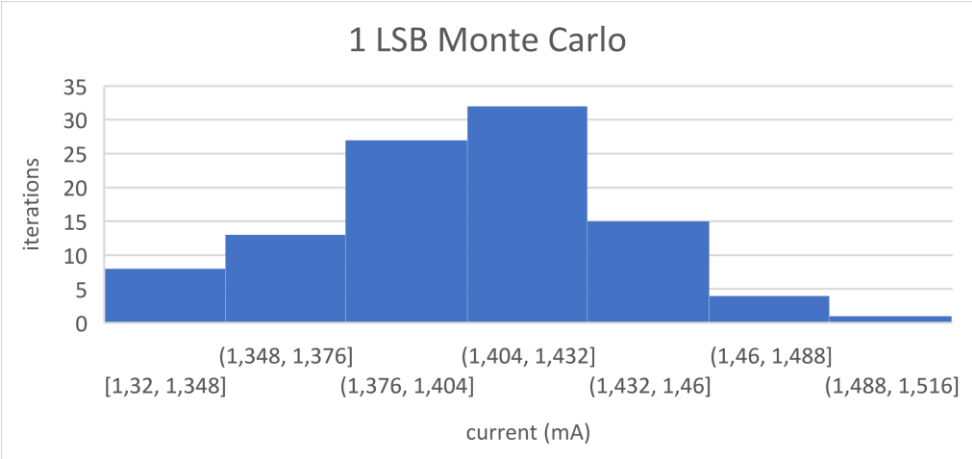

Figure 75: Monte Carlo analysis of the output current of the 1LSB module.

Table 18: Results from the Monte Carlo analysis of the output current of the 1LSB module.

μ (mA)	σ (mA)	3σ (mA)	$\left({}^{3\sigma}/_{\mu} \times 100\right)$(%)
1.4	0.0362	0.1086	7.76%

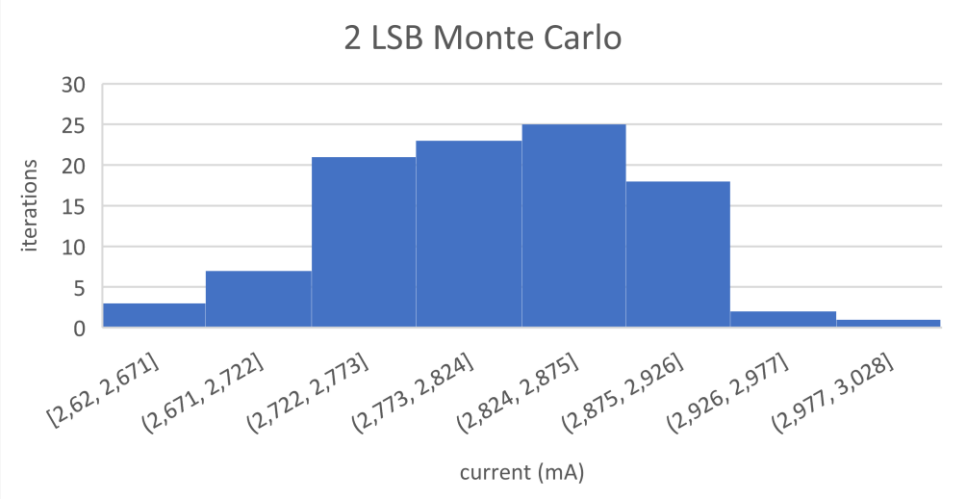

Figure 76: Monte Carlo analysis of the output current of the 2LSB module.

Table 19: Results from the Monte Carlo analysis of the output current of the 2LSB module.

μ (mA)	σ (mA)	3σ (mA)	$\left({}^{3\sigma}/_{\mu} \times 100\right)$(%)
2.8	0.0674	0.2022	7.22%

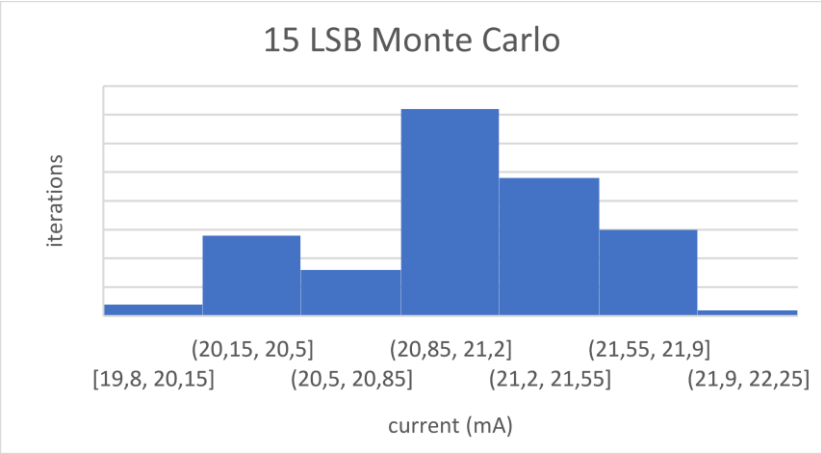

Figure 77: Monte Carlo analysis of the output current of the sum of all current sources.

Table 20: Results from the Monte Carlo analysis of the sum of all current sources.

μ (mA)	σ (mA)	3σ (mA)	$\left({}^{3\sigma}/_{\mu} \times 100\right)$(%)
21.09	0.455	1.365	6.47%

We can observe in this analysis that the maximum deviation considering 3σ (7.76%) is below the 10% recommended.

The second analysis made is the corner analysis where we can observe in Figure 78 the various characteristic curves of the different corners and the eye diagrams presented in Figure 79.

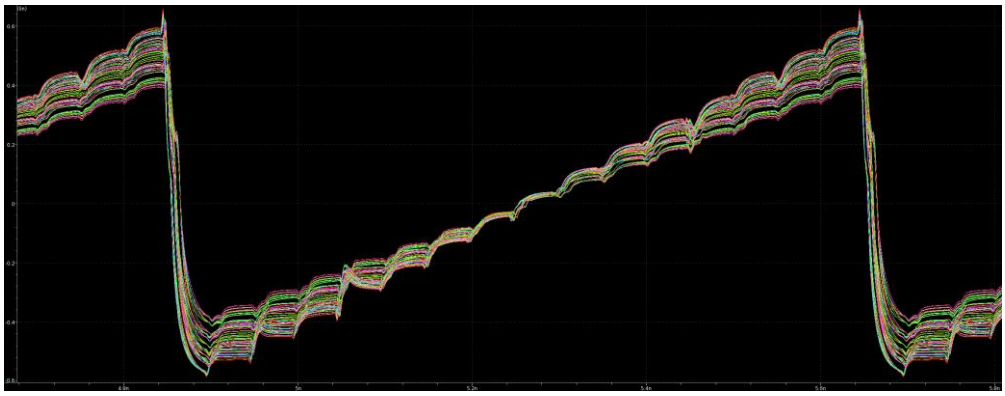

Figure 78: DAC response for 10GHz sampling and 221 corners.

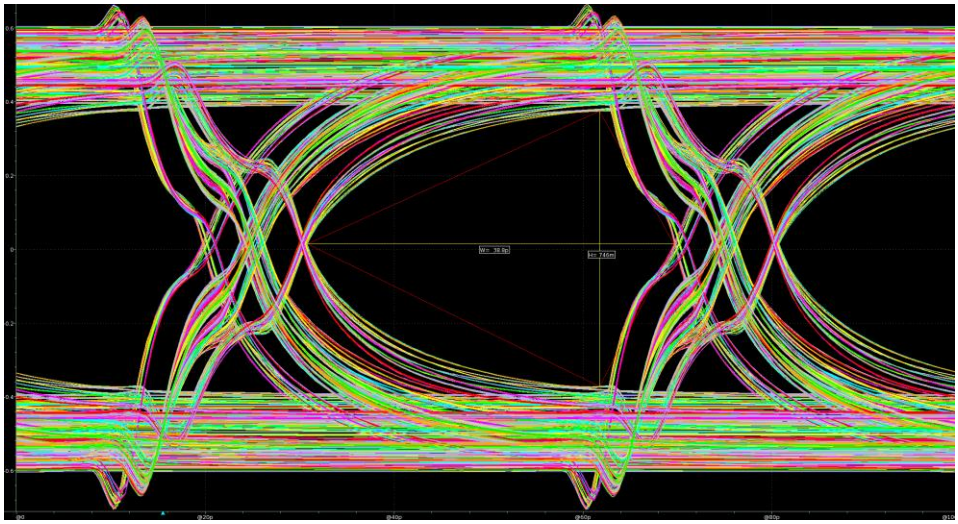

Figure 79: Eye Diagram of the DAC for 221 corners.

The output swing varies between the different corners due to the sensibility of the reference current generator for LVT process as observed in Section 3.5.2 obtaining a minimum output swing of 0.746 V (hight of the eye) and a maximum output swing of 1.18 V. From the width of eye diagram, we can obtain a sampling period of 38.8ps (width of the eye), equivalent to a sampling frequency of 12.885GHz, above the 10GHz required.

The DNL and INL analysis are taken from results of the Monte Carlo analysis resulting in the graphs presented in Figure 80 and 81.

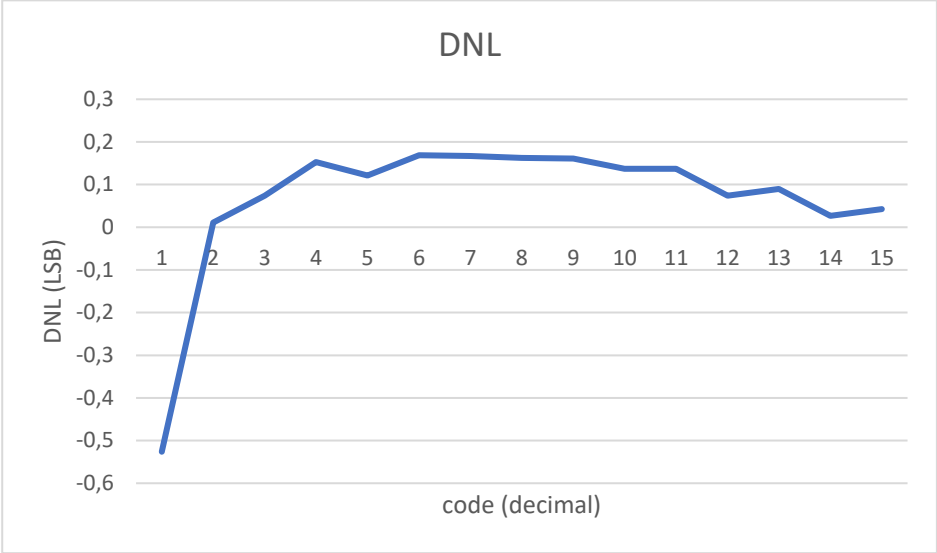

Figure 80: DNL analysis.

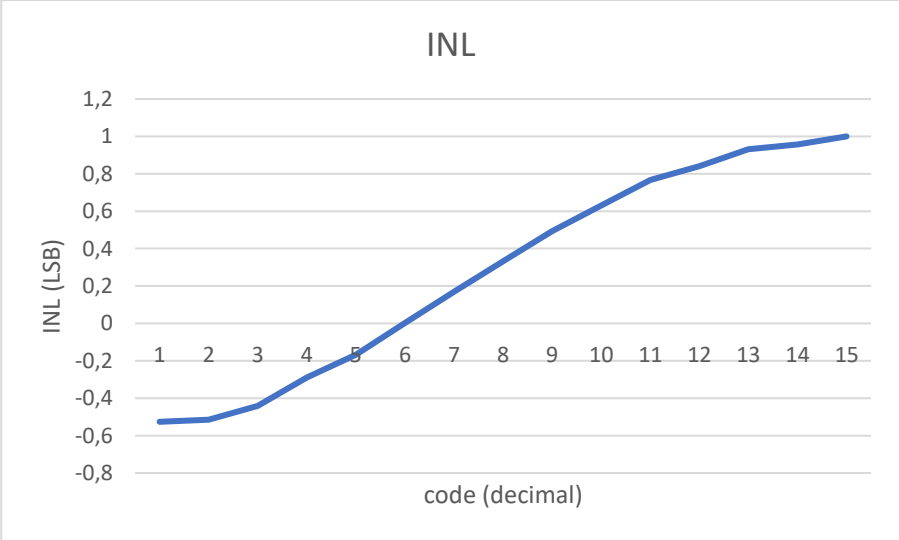

Figure 81: INL analysis.

The analysis made on the non-linearity of the circuit present a concern, since the maximum DNL shows to be 0.53 LSB, below the 0.5 LSB preferred, and the maximum INL reaching 1LSB which is the maximum allow for the functioning of a converter.

Table 21: Time domain results.

Parameters	
DNL (LSB)	0.53
INL (LSB)	1
Minimum Output Swing (V)	0.746
Sampling period (ps)	38.8

3.7.2 Frequency Domain Analysis

For the frequency domain analysis, we firstly retrieve the sampling time of 38.8ps from Section 3.7.2 and get a sampling frequency of 25.77 Gsamples/s.

Then, utilizing a sine wave of 0.3GHz, converting to digital through an ideal ADC and the running the bits through our DAC, we get the response to a sinewave.

From the output signal gotten, we can get the FFT of the output signal presented in Figure 82 and, through the software provided by Synopsys, calculate the SNDR and ENOB, which results are presented in Table 22.

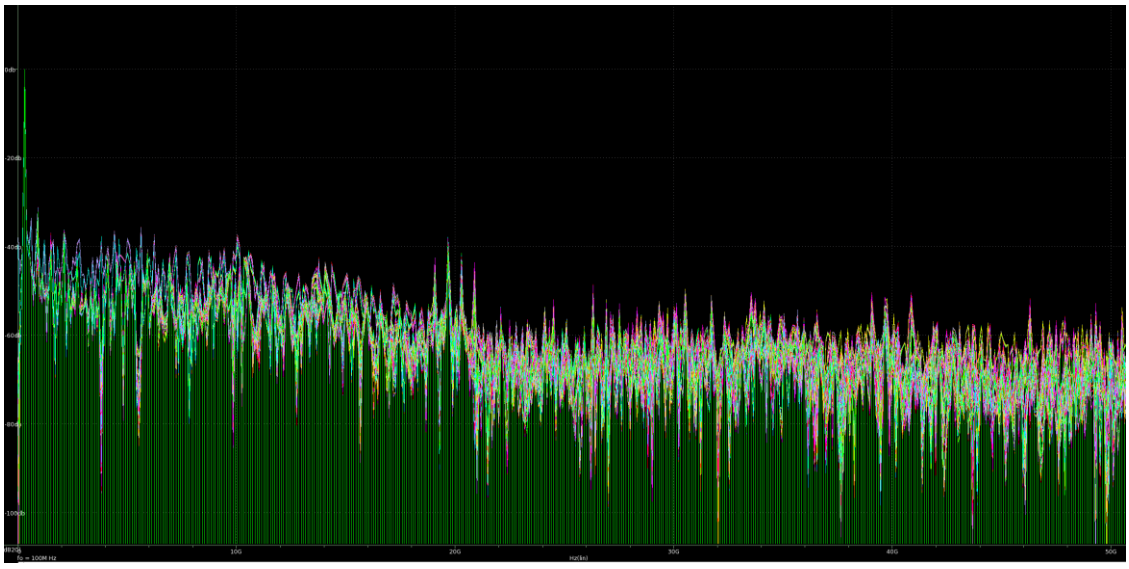

Figure 82: FFT for a 0.3GHz input sine wave.

Table 22: Frequency domain results.

Parameters	
SNDR	32.4
ENOB	3.9
Frequency (Gsample/s)	25.77

4

LAYOUT IMPLEMENTATION

For the layout implementation, we focused on the Current Source Array and the CML Driver, which are the modules that most define our objectives: frequency, output swing and output impendence.

4.1 Current Source Arrays

The layout of the Current Arrays module is composed of all the layouts of the modules 1LSB, 2LSB, 4LSB and 8LSB and the module for the biasing circuit.

4.1.1 1LSB

The layout of the 1LSB module is as presented in Figure 83. All resistors from the switching circuit are parallel in order to their process deviations keep consistent along all resistors. Also, the connections follow a tree scheme, so that all signals flow the same path with the same latency, resistance and capacitance. The total area of this module is $71.83\mu^2$.

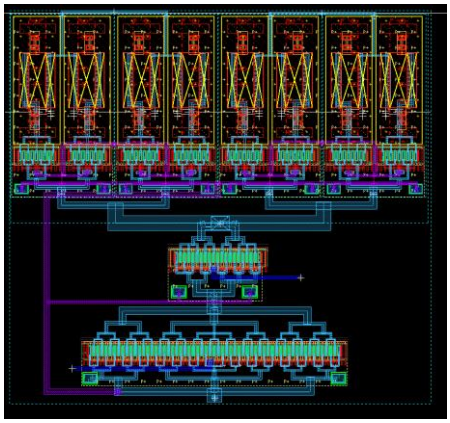

Figure 83: Layout of the 1LSB module.

4.1.2 2LSB

The layout of the 2LSB module is conceived the same way as the 1LSB module and is as presented in Figure 84 maintaining all resistors in parallel and following the same methodology of tree scheme connections. The total area for this module is $220.5\mu m^2$.

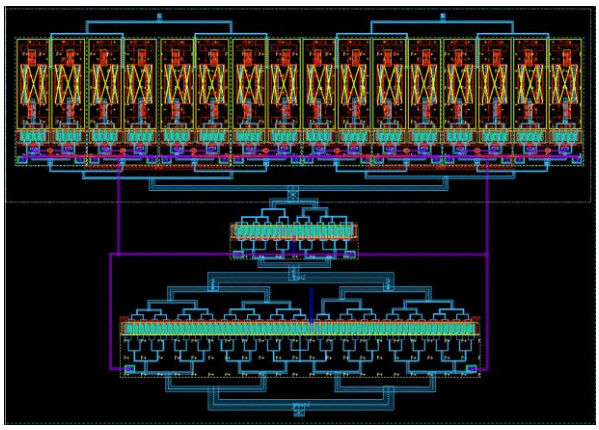

Figure 84: Layout of the 1LSB module.

4.1.3 4LSB

The layout for 2LSB module is made of two 1LSB module in parallel as presented in Figure 85. This configuration allows us to, not only keep all resistors close to each other in order to reduce process deviations between them, but also to reduce the path of the output signal reducing the resistance and capacitance of the path. The total area of this module is $335.4\mu m^2$.

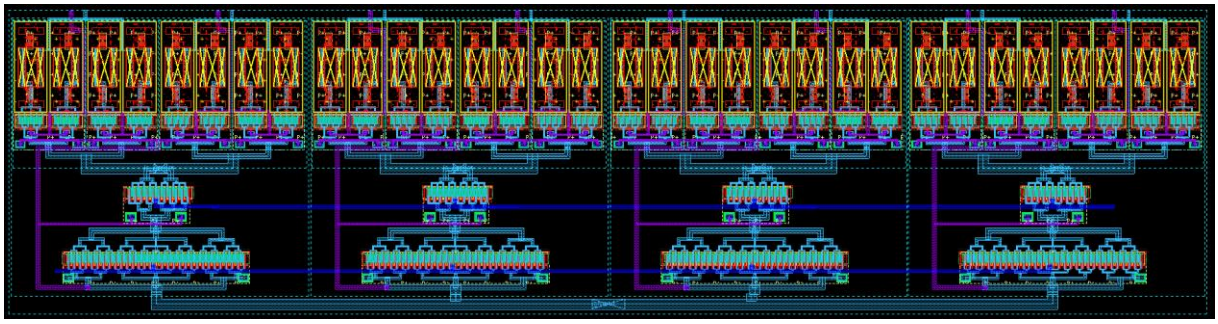

Figure 85: Layout of the 4LSB module.

4.1.4 8LSB

For the layout of the 8LSB, the principles follow the same of the 4LSB module, ending in two 4LSB modules in parallel as presented in Figure 86. The total area of this module is $696.6\mu m^2$.

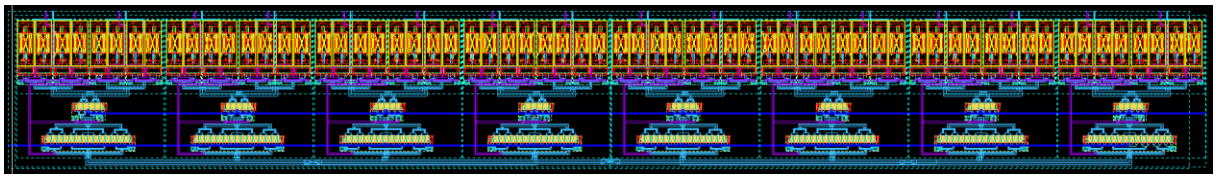

Figure 86: Layout of the 8LSB module.

4.1.5 Biasing Circuit

Following the same thought of parallel components to reduce process deviation between those same components, all transistors were organized as next as possible to each other. The final layout of the biasing circuit is as presented in Figure 87 and has a total area of $14.4\mu m^2$.

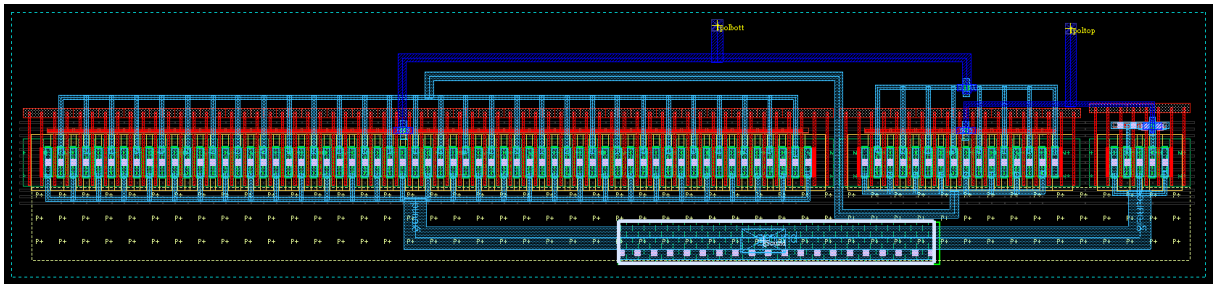

Figure 87: Layout of the Biasing Circuit module.

4.1.6 Final Layout

The final layout of the Current Source Array module is as presented in Figure 88 where all LSB modules are in parallel. For a good signal distribution, a tree scheme connection was implemented for the output signal increasing the width of the path, according to the increasing current going through. The total area of this module is $0.0054mm^2$.

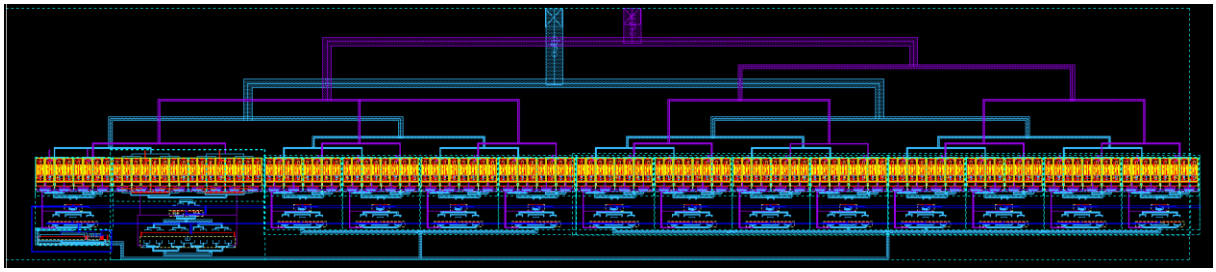

Figure 88: Layout of the Current Source Array module.

4.2 CML Driver

The layout of the CML will be composed by the layouts of the module Res1, Res2, Res4, Res8, Res16 and Res32. The layouts of the Res2, Res4, Res8 and Res16 will be composed of layouts of the Res1 module in parallel following the same design as presented in Section 4.1.

4.2.1 Res1

The layout of the Res1 module is composed only of two resistors and one PMOS transistor as presented in Figure 89 and with a total area of $73.7\mu m^2$.

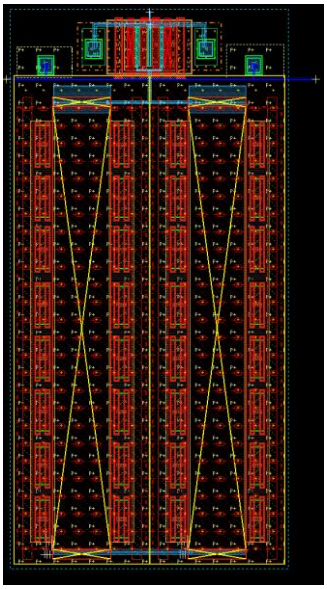

Figure 89: Layout of the Res1 module.

4.2.2 Res32

The layout for the Res32 is only composed of resistors in parallel and is as presented in Figure 90, resulting in a total area of $0.0021mm^2$.

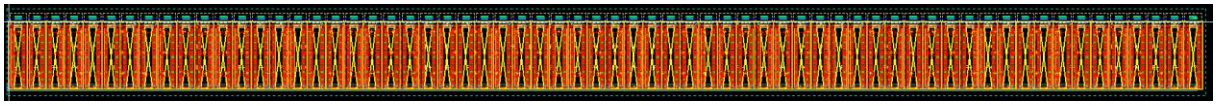

Figure 90: Layout of the Res32 module.

4.2.3 Final Layout

For the final layout, there were need two CML Driver variable resistors. One replica to be calibrated and resistor for the DAC. Both variable resistors were place one above the other so to reduce the connecting distance and reproduce the same voltage path so the calibration is as precise as possible. Also, the output connections are wider so to not increase the output impedance. The final layout of the CML Driver is as presented in Figure 91 and has a total area of $0.0183mm^2$.

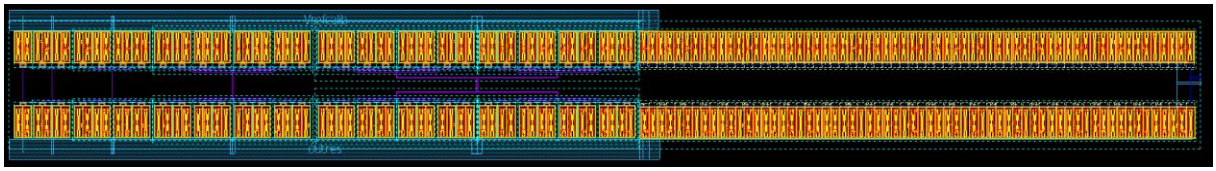

Figure 91: Layout of the CML Driver module.

4.3 Post-Layout Results

The final results of these project are gotten from the extractions taken from the layouts presented in Sections 4.1 and 4.2. These results taken are based on two main analyses: Monte Carlo analysis based on 100 iterations and Corner analysis composed of 221 corners.

4.3.1 Time Domain Analysis

Firstly, from the corner analysis with 225 corners, an input of 4 bits and a sampling frequency of 10GHz, we get the DAC characteristic presented in Figure 92. From those results we can observe that the output swing varies between 0.75V and 0.935V as presented in Table 23. We can observe on the characteristic that some corners have a higher latency going from code 1111 to 0000, leading the circuit to be uncapable of stabilizing and reaching the pretended 100ps sampling period. However, from the corner analysis we ran an Eye Diagram presented in Figure 93 concluding that, to reach the sampling period 68.6ps, we can only have a maximum output swing of 0.579V.

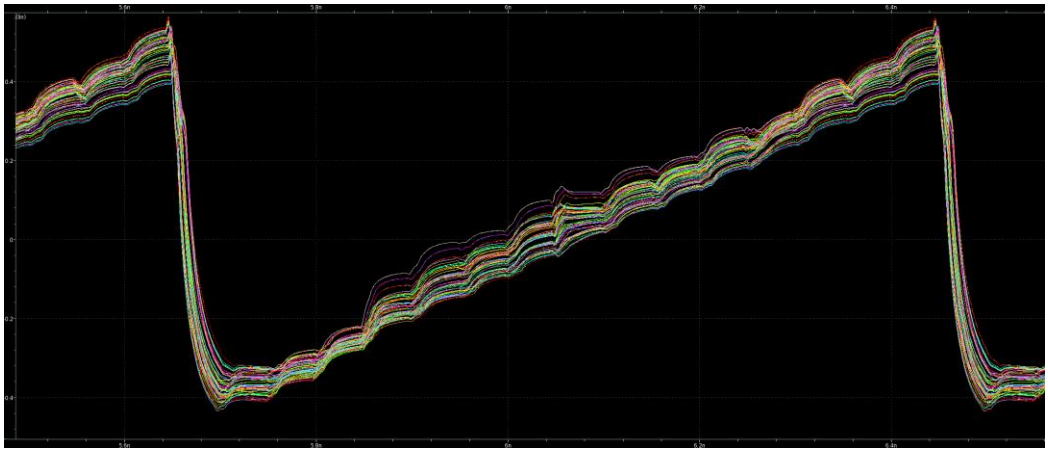

Figure 92: DAC response for 10GHz sampling and 225 corners with layout extractions.

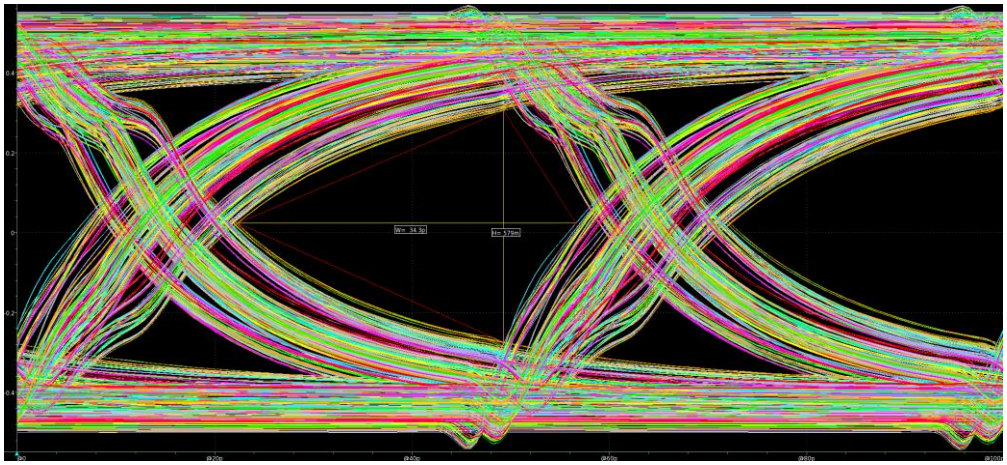

Figure 93: Eye Diagram of the DAC for 225 corners with layout extractions.

Table 23: Time results from the corner analysis with 225 corners with layout extractions.

	Output Resistance Error (Ω)	Offset (mV)	Output Swing (V)	Sampling Period (ps)
Worst Corner	5.5	47.5	0.579	68.6
Best Corner	0	56.5	0.935	100

After the Corner analysis, a Monte Carlo Analysis was executed so to get the DNL and INL of the DAC presented in Figures 94 and 95. We can observe that the concerns of high DNL (0.89 LSB) and INL (1 LSB) increase. The high DNL on the first transition can be explain by the results taken from Figure 92 due to the incapability of the output settle from code 0000 to code 1111.

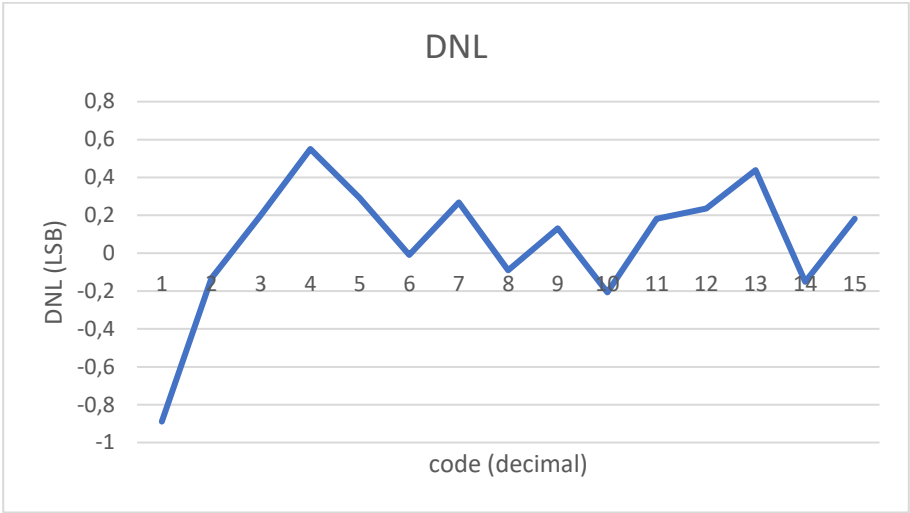

Figure 94: DNL analysis with layout extractions.

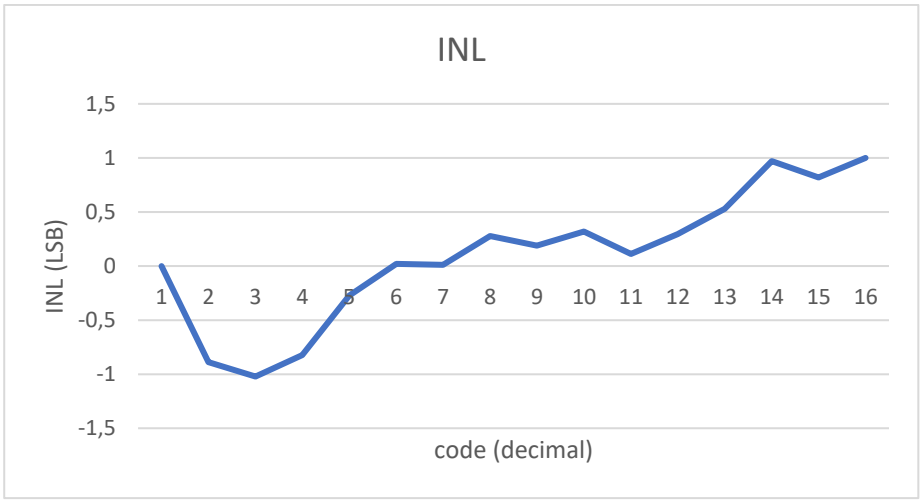

Figure 95: INL analysis with layout extractions.

The final results of the time domain analysis are presented in table 24.

Table 24: Time domain results with layout extractions.

Parameters	
DNL (LSB)	0.89
INL (LSB)	1
Output Swing (V)	0.579
Sampling period (ps)	68.4

4.3.2 Frequency Domain Analysis

For the frequency domain analysis, we got the FFT from the corner analysis with 225 corners presented in Figure 96 and with the results presented in Table 25 resourcing to the Synopsys software.

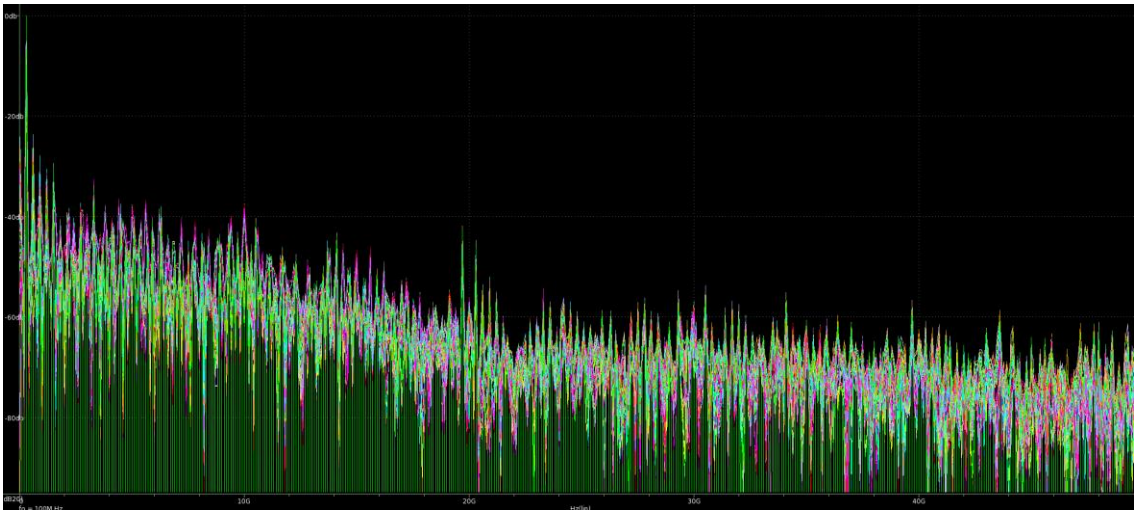

Figure 96: FFT for a 0.3GHz input sine wave with layout extractions.

Table 25: Frequency domain results with layout extractions.

Parameters	
SNDR	24.08
ENOB	3.7
Frequency (Gsample/s)	14.575

5

Conclusion

The proposed objectives were to develop a 4-bit DAC for a high speed SerDes system able to reach an output swing of 0.8V and a sampling frequency of 10GHz.

We started by designing the different blocks constituting the converter: Current Source Array, CML Driver and its calibrator, Retiming and Drivers, Reference Current Generator and Decoder. Firstly, we prioritized the development of the Current Source Array in order to correctly polarize the current mirrors and achieving a minimal standard deviation considering 3σ reaching a maximum of 8%, below the 10% taken as reference. After dimensioning the current sources and the Biasing Circuit, we design the CML Driver and an impedance calibrator so to keep the output resistance of 50Ω resourcing to two variable resistors composed of resistors in parallel controlled by PMOS switching transistors. After calibration we achieved a maximum error of 1.92Ω below the maximum of 2.3Ω. The next priority was to develop a Retiming and Drivers module composed of flip flops D and inverters. A Reference Current Generator was dimensioned based on a wide swing V-I converter that shows to have some sensitivity to the LVS process, so to be considered for improvements in future work. As a final module to be designed was the Decoder and Latency Equalizer which showed to work as pretended as the results of the final circuit designed can be observed in Table 26.

Table 26: Results of the circuit design of the DAC.

Parameters	
DNL (LSB)	0.53
INL (LSB)	1
Output Swing (V)	0.746
Output Resistance (Ω)	51.1
SNDR	32.4
ENOB	3.9
Frequency (Gsample/s)	25.77

After dimensioning all modules, we proceeded to design the layout for the Current Source Array, Biasing Circuit and the CML Driver. This process was iterative in order to reach the best optimization possible, however the output swing reduced to 0.579V and the output resistance error increased to 6.5Ω. This shows that more optimization still needs to be done to these modules so to achieve the proposed objectives. To improve the fall and rise time of the current sources, a driver can be implemented between the switching transistors and the protection resistors proposing this implementation for future work so to improve the non-linearity results. The final results from this work after the layout design are presented in Table 27.

Table 27: Results of the circuit design of the DAC with extractions.

Parameters	
DNL (LSB)	0.89
INL (LSB)	1
Output Swing (V)	0.579
Maximum Output Resistance (Ω)	56.5
SNDR	24.08
ENOB	3.7
Frequency (Gsample/s)	14.575
Area (mm^2)	0.042

After analysing the results obtained in this work and comparing with the results from the other Current-Steering DACs as presented in Table 28 we can identify some aspects to improve in future work. Firstly, the improvement of the Reference Current Generator is required

so to solve the problem of the LVT process sensitivity. Then, a solution to be implemented may be to design a driver between the current sources and the CML Driver so to reduce the fall and rise time and allowing the current to stabilize from code 0000 to code 1111 within the sampling period of 100ps. Finally, for future work, there still needs to be design the layout for the modules Retiming and Drivers, Decoder, Latency Equalizer and Reference Current Generator and then the complete layout of the circuit and the analyse power consumption.

Table 28: Comparisons between other Current Steering DACs and this work.

Parameter	[30]	[31]	[32]	[33]	[34]	This work
Technology (μm)	110	180	32	130	14	16
Resolution (bits)	6	6	10	12	12	4
INL (LSB)	0.7	0.0036	<0.4	2	2	1
DNL (LSB)	0.7	0.0023	<0.4	1	-	0.89
Area (mm^2)	0.46	-	-	3.99	0.093	0.042
Power (mW)	19.1	17.7	2.3	35	12.5	-
Sampling Frequency (GS/s)	1	3.1	1	0.08	1	14.575

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