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Implementation of a Sigma Delta Modulator for a Class D Audio Power Amplifier

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To my long-time companion, Cátia

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Abstract

Sigma-Delta Modulators ($\Sigma\Delta$M) have gain a lot of ground over the last several years as one of the premier solutions in signal conversion, for low frequency, high-resolution applications. $\Sigma\Delta$Ms use negative feedback to reduce the quantization error, where a filter circuit is placed before the quantizer in order to define the frequency band where the quantization error is attenuated.

This filter is traditionally built using ideal integrator stages, implemented with operational amplifiers (Op-Amps) in an integrator configuration. These Op-Amps require a large DC gain and bandwidth in order for the behaviour of the integrator circuits to be close to the ideal integrator behaviour. If the $\Sigma\Delta$M is built using discrete components in a Continuous-Time (CT) design, it is difficult to find fully differential Op-Amps, resulting in a circuit that uses a single ended topology with all the disadvantages associated.

This thesis focuses on the design of a 3rd Order CT-$\Sigma\Delta$M where the integrator stages of the filter are implemented with Bipolar-Junction Transistors (BJT) differential pairs. By replacing the Op-Amps with differential pairs, it is possible to build an equivalent filter circuit for the $\Sigma\Delta$M using lossy integrators. The finite gain and bandwidth of the differential pairs can be accommodated during the filter design process. Both 1-bit and 1.5-bit quantization are studied, as well as the effect of spreading of the zeros of the CT-$\Sigma\Delta$M along the signal bandwidth.

Electrical simulations show that it is possible to achieve an SNDR of around 62 dB for 1-bit quantization, 75 dB for 1.5-bit quantization and 78 dB with the spreading of the zeros, creating local resonator stages, for a sampling frequency of 1.28 MHz. These results are corroborated by experimental results, where an SNDR of around 58 dB is achieved for 1-bit quantization and 72 dB for 1.5-bit quantization and local feedback.

Keywords: Audio, Bipolar-Junction Transistors, Continuous-Time Sigma-Delta ($\Sigma\Delta$), Class D Amplifier, Differential Pair.

Resumo

Os Moduladores Sigma-Delta ($\Sigma\Delta$M) têm ganho muito terreno nos ultimos anos como uma das principais soluções em conversão de sinal, para aplicações de alta resolução a baixa frequência. Os $\Sigma\Delta$M usam realimentação negativa para reduzir o erro de quantificação, através de um filtro que é colocado antes do quantificador de maneira a definir a faixa de frequências onde o erro de quantificação é atenuado.

Este filtro é tipicamente feito através de andares de integração ideais, implementados com amplificadores operacionais (Amp-Ops) numa configuração de integrador. Estes requerem um elevado ganho DC e largura de banda para que o comportamento dos integradores seja próximo do ideal. Se o $\Sigma\Delta$M é feito com componentes discretos num *design* em Continuo (CT), é dificil encontrar Amp-Ops completamente diferenciais, resultando num circuito com uma topologia "single-ended"com todas as desvantagens associadas.

Esta tese foca-se no *design* de um CT-$\Sigma\Delta$M de 3ª ordem onde os andares de integração do filtro são implementados com pares diferenciais baseados em transistores de junção bipolar (TJB). É possivel construir um filtro equivalente para o $\Sigma\Delta$M usando integradores com perdas substituindo os Amp-Ops por pares diferenciais. O ganho e largura de banda finita dos pares diferenciais é acomodado durante o processo de *design* do filtro. Ambas as quantificações de 1-bit e 1.5-bit são estudadas, bem como o efeito da distribuição dos zeros do CT-$\Sigma\Delta$M através da banda do sinal.

Através de simulações eléctricas conclui-se que é possivel alcançar uma SNDR de cerca de 62 dB para uma quantificação de 1-bit, 75 dB para 1.5-bit e 78 dB para 1.5-bit e com distribuição dos zeros. A frequência de amostragem usada é de 1.28 MHz. Estes resultados são corroborados por resultados experimentais, onde é obtida uma SNDR de cerca de 58 dB para uma quantificação de 1-bit e 72 dB para 1.5-bit e realimentação local.

Palavras-chave: Audio, Transistores de Junção Bipolar, Sigma-Delta ($\Sigma\Delta$) em Continuo, Amplificadores Classe D, Pares Diferenciais.

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Abbreviations

ΣΔM	**S**igma **D**elta **M**odulator
A/D	**A**nalog/**D**igital
ADC	**A**nalog-to-**D**igital **C**onverter
BJT	**B**ipolar-**J**unction-**T**ransistor
BTL	**B**ridge-**T**ied-**L**oad
CIFF	**C**ascade of **I**ntegrators **F**eed**f**orward
CIFB	**C**ascade of **I**ntegrators **F**eed**b**ack
CMRR	**C**ommon-**M**ode **R**ejection **R**atio
CRFF	**C**ascade of **R**esonators **F**eed**f**orward
CRFB	**C**ascade of **R**esonators **F**eed**b**ack
CT	**C**ontinuous **T**ime
D/A	**D**igital/**A**nalog
DAC	**D**igital-to-**A**nalog **C**onverter
DC	**D**irect **C**urrent
DR	**D**ynamic **R**ange
DT	**D**iscrete **T**ime
EMI	**E**lectro**m**agnetic **I**nterference
FFD	**F**lip-**F**lop **D**-type
FFT	**F**ast **F**ourier **T**ransform
GBW	**G**ain **B**andwidth **P**roduct
IC	**I**ntegrated **C**ircuit

KCL	**K**irchhoff's **C**urrent **L**aw
NTF	**N**oise **T**ransfer **F**unction
OpAmp	**O**perational **A**mplifier
OSR	**O**vers**s**ampling **R**atio
PCB	**P**rinted **C**ircuit **B**oard
PDM	**P**ulse **D**ensity **M**odulation
PSSR	**P**ower **S**upply **R**ejection **R**atio
PWM	**P**ulse **W**idth **M**odulation
SC	**S**witched **C**apacitor
SNDR	**S**ignal-to-**N**oise-plus-**D**istortion **R**atio
SNR	**S**ignal-to-**N**oise **R**atio
STF	**S**ignal **T**ransfer **F**unction
THD	**T**otal **H**armonic **D**istortion

1

Introduction

1.1 Background and Motivation

Over the years, there is a growing concern with the energy efficiency of electronic appliances, due to the global sustainability issue. Audio amplifiers are one example where the efficiency can be improved. They amplify input audio signals in order to drive output elements with suitable volume and power levels, with low distortion.

Class D amplifiers, due to their output power devices operating as switches, can reach an efficiency of 100% in theory [1], [2]. Thus, Class D amplifiers pose themselves as the best solution in terms of efficiency for audio power amplifiers.

In order to generate the digital control signal for the power output devices of a Class D amplifier, it is necessary to convert the input analog signal into a digital signal. Thus, an Analog-to-Digital Converter (ADC) is employed. Sigma-Delta Modulators ($\Sigma\Delta$M), given their native linearity, robust analog implementation and reduced anti-aliasing filtering requirements, are the best option for low frequency, high-resolution applications [3], [4].

Continuous-Time (CT) implementations of $\Sigma\Delta$M have come a long way in recent years and present some advantages over pipeline ADCs, which many thought were the only conversion technique available for high dynamic performance, sub-100 mega-samples per second applications. Some of these advantages are the inherent anti-aliasing filtering (reducing/eliminating the need for an external Anti-Aliasing Filter) and low power operation.

The main goal of this thesis is to study and develop a CT-$\Sigma\Delta$M for use in a Class D full-bridge audio power amplifier, where the CT integrators are based on bipolar-junction-transistor (BJT) differential pairs. By relying on simple gain blocks instead of operational amplifiers to build the loop filter, a simpler overall circuit with lower power

dissipation is obtained. The non-ideal effects, such as the low gain and finite bandwidth of the differential pairs, are embedded in the loop filter transfer function. Although this leads to a more difficult design process, this problem can be solved through the use of a optimization procedure based on genetic algorithms, proposed in [5].

Since these Differential Pairs and most of the circuit will be designed using discrete components, BJTs are used instead of MOSFETs, largely in part due to their high transconductance, robustness against electrostatic discharge and lower cost.

1.2 Thesis Organization

Besides this introductory chapter, this thesis is organized in four more chapters:

Chapter 2 - Class D Audio Amplifiers and Data Conversion Fundamentals

In this chapter, a brief theoretical overview of Class D Audio Amplifiers and Signal Conversion is presented. The main building blocks of the former, as well its advantages and disadvantages, are described. In regards to the latter, the sampling and quantization concepts are explained, ultimately leading to the Nyquist-Shannon Theorem. The theory behind quantization noise and oversampling is presented as background to the topic presented next in this chapter, $\Sigma\Delta$ Modulation. Finally, the last section of this chapter focus on the analysis of several $\Sigma\Delta$M architectures. The constituting blocks are shown and their signal and noise transfer functions are determined. Also, the 1.5-bit quantization advantages are exploited.

Chapter 3 - Implementation of the $\Sigma\Delta$M

After selecting the appropriate architecture at the end of chapter 2, its implementation is explained in this chapter. Two different integrator stages are proposed, through the use of Operational Amplifiers (OpAmps) or Differential Pairs. In each case, a thorough analysis is made, equations are drawn and the advantages/disadvantages of each implementation are presented. Next, the design of the ADC is realized, through the implementation of the quantizer and the encoding logic. Finally, electrical simulations are performed and the overall performance of several $\Sigma\Delta$Ms is evaluated.

Chapter 4 - Measured Prototypes and Experimental Results

In Chapter 4, the performance of two $\Sigma\Delta$Ms where their integrator stages are implemented with BJT differential pais is evaluated through two prototypes and the experimental results obtained. The main difference between these two prototypes is the use of 1-bit quantization in one and 1.5-bit quantization on the other. Considerations are drawn over the results obtained.

Chapter 5 - Conclusions and Future Work

In the fifth and last chapter, a discussion of the obtained results is performed and

conclusions revolving around this work are drawn. Further possible work suggestions related to this thesis are advised.

1.3 Main Contributions

The main contribution behind this thesis is the implementation of a robust and high-performance CT-$\Sigma\Delta$M based on simple circuitry, recurring to BJT Differential Pairs to implement the integrator stages.

This is done instead of using traditional OpAmps in an integrator configuration, which are more expensive and sometimes not very efficient. The finite gain and bandwidth of these differential pairs are accommodated during the design process.

Also, by designing the integrator stages based on differential pairs, a fully-differential topology can be obtained from scratch without the use of a balun circuitry.

A paper resulted from the developed research work:

- Nuno Pereira, João L. A. de Melo and Nuno Paulino. "Design of a 3rd Order 1.5-Bit Continuous-Time Fully Differential Sigma-Delta ($\Sigma\Delta$) Modulator Optimized for a Class D Audio Amplifier Using Differential Pairs", presented at the 4th Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS 2013), Caparica, April 2013. - [6].

2

Class D Audio Amplifiers and Data Conversion Fundamentals

This chapter provides a theoretical overview of the relevant aspects addressed in this thesis. A brief presentation of Class D audio amplifiers is made. Afterwards, the main concepts behind signal conversion in general and $\Sigma\Delta$M in particular are addressed (Sampling/Oversampling, Quantization, etc). Finally, an analysis of several $\Sigma\Delta$M architectures is performed as well as the use of 1.5-bit quantization.

2.1 Class D Audio Amplifiers

Audio amplifiers are used to amplify input audio signals in order to drive output elements (like speakers) with suitable volume and power levels, with low distortion. These amplifiers must have a good frequency response over the range of frequencies of the human ear (20 Hz to 20 kHz).

Power is dissipated in all linear output stages, because the process of generating the output signal unavoidably causes non-zero voltages and currents in at least one output transistor. The amount of power dissipation strongly depends on the method used to bias the output transistors.

Traditional Class A audio amplifiers have a maximum efficiency of about 25% (50% if inductive coupling is used), which is considerably low. Class B audio amplifiers can reach an efficiency of 78.5% (theoretically), but have known disadvantages (cross-over distortion being the main one). The combination of both, Class AB audio amplifiers, can reach a similar efficiency, while practically eliminating the crossover [7].

In a Class D amplifier, the output transistors are operated as switches. They are either

fully on (the voltage across it is small, ideally zero) or fully off (the current through it is zero). This leads to very low power dissipation, which results in high efficiency (ranging from 90% to 100% [1], [2]).

The basic block diagram of a Class D amplifier is shown in Fig. 2.1.

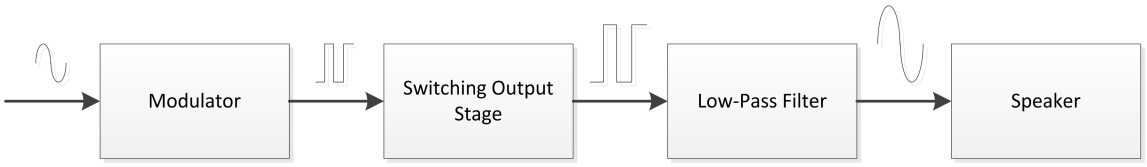


Figure 2.1: Class D amplifier block diagram.

The input audio signal is modulated into a digital control signal which drives the power devices in the output stage. This signal can be modulated, normally, using pulse-width modulation (PWM) or pulse-density modulation (PDM). The output stage can be implemented using a Half-Bridge or a Bridge-Tied-Load (BTL) topology, illustrated in Fig. 2.2 and Fig. 2.3. Class D amplifiers are often operated in a bridged configuration to increase the output power without increasing the power supply voltages. The last stage, the low pass filter, is used to remove the high frequency PWM/PDM carrier frequency, thus retrieving the sinusoidal audio signal.

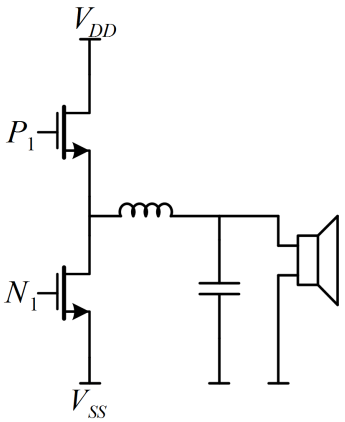


Figure 2.2: Half-Bridge Output Stage.

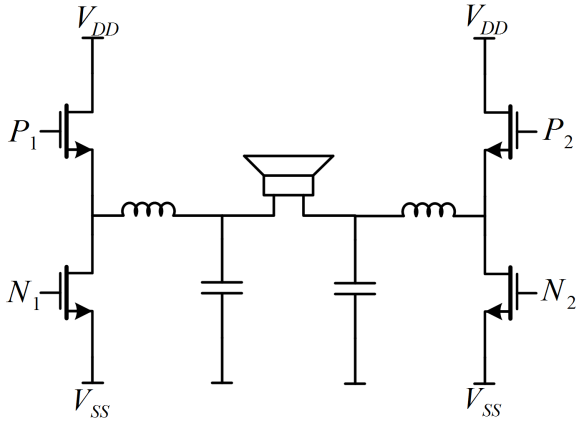


Figure 2.3: Bridge-Tied-Load Output Stage.

In a BTL amplifer, both sides of the speaker load are driven in opposite phase. Thus, a single supply can be used, while doubling the voltage swing across the load, yielding four times more output power than a Half-Bridge amplifier. Since this is a balanced operation, even order distortion is cancelled. However, a BTL amplifier needs twice the number of power switches and inductors [2].

Concerning the Half-Bridge amplifier, since it is a single-ended circuit the output signal contains a Direct-Current (DC) component with a $\frac{V_{cc}}{2}$ amplitude that might damage the speaker due to the high output power. Moreover, in the Half-Bridge Class D amplifier the energy flow can be bi-directional, which leads to the *Bus pumping* phenomena that causes the bus capacitors to be charged up by the energy flow from the load back to

the supply. This occurs mainly at low audio frequencies and can be limited by adding large decoupling capacitors between both supply voltages (V_{cc} and V_{ss}, the latter being typically ground) [8].

Considering both topologies, the BTL output stage is often used as the primary solution for high quality audio applications since it provides superior audio performance and output power. Nevertheless, neither topology can reach a power efficiency of 100% in reality since there is always switching and conduction losses that need to be considered and that limit the output stage's power efficiency.

A problem called *shoot-through* can reduce the efficiency of class-D amplifiers and lead to potential failure of the output devices [2], [8]. This results from the simultaneous conduction of both output stage complementary transistors (when one is being "turned off" and the other is "turned on"), during which a low impedance path between V_{cc} and V_{ss} is created leading to a large current pulse that flows between the two. This is caused by each transistor's response time, which is never immediate. The power loss that comes from shoot-through is given by

$$P_{ST} = I_{ST} \cdot (V_{cc} - V_{ss}) \tag{2.1}$$

, where I_{ST} is the average current that flows through both transistors. This can be eliminated by driving the output stage transistors with non-overlapping signals, avoiding simultaneous conduction.

The high switching frequency used in class-D amplifiers is a potential source of RF interference with other electronic equipment. The amplifiers must be properly shielded and grounded to prevent radiation of the switching harmonics. In addition, low-pass filters must be used on all input and output leads, including the power supply leads [2].

Another concern related to the use of Class D audio amplifiers is their Power Supply Rejection Ratio (PSRR). Due to the very low resistance that the output stage transistors have when connecting the power supplies to the low-pass filter, there is little to no isolation to any noise or voltage variation from these sources. If this problem is not properly addressed, the output signal will present a considerable level of distortion. A way of taming this problem is through the use of feedback directly from the output stage [9].

The pulses from the modulator and output stage contain not only the desired audio signal but also significant high-frequency energy (originated in the modulation process). As stated before, the low-pass filter removes this high frequency, allowing the speaker to be driven without such energy, thus minimizing the electromagnetic interference (EMI). If the modulation technique used is PWM, EMI is produced within the AM radio band. However, if PDM is employed (by a $\Sigma\Delta$M) much of the high-frequency energy will be distributed over a wide range of frequencies. Therefore, $\Sigma\Delta$M present a potential EMI advantage over PWM [8].

2.2 Signal Conversion Fundamentals

In this section, the ADCs theoretical behaviour will be presented. Most of the information presented is also valid for Digital-to-Analog Converters (DACs). Both sample an input signal at a certain sampling frequency and convert it to a bitstream. For ADCs, the input signal is analog and the resulting bitstream is the digital representation of the analog signal. In the DACs case, the input signal is digitally represented by an N bit word, which is converted into a bitstream (that is a digital representation of the input signal as well) that is then applied to a filter that recovers the analog version of the input signal.

Signal conversion in ADCs is performed when an analog input signal is transformed into a digital output signal. Since an analog signal can assume infinite values in a finite time interval and it is impossible to process infinite samples, it is necessary to acquire a finite number of values. This is done by *sampling* the analog signal (usually with a constant sampling period T_s) and *quantizing* its amplitude (so that it assumes one of a finite number of values) [4]. A representation is shown in Fig. 2.4, where x(t) is the input signal, s(t) the sampling function and y(t) the output signal. The output signal is a result of the product of the input signal by the sampling function (Eq. 2.2).

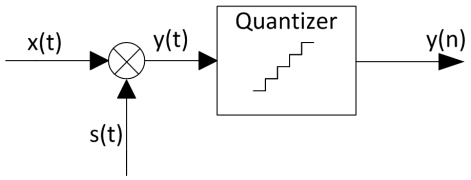


Figure 2.4: Sampling and Quantizing the x(t) input signal.

$$y(t) = x(t) \cdot s(t) \tag{2.2}$$

This sampling function is a periodic pulse train (Eq. 2.3), where $\delta(t)$ is the Dirac delta function and T_s is the sampling interval.

$$s(t) = \sum_{n=-\infty}^{+\infty} \delta(t - nT_s) \tag{2.3}$$

The Fourier transform of a periodic impulse train is another periodic impulse train. Thus,

$$S(j\omega) = \frac{2\pi}{T_s} \sum_{k=-\infty}^{+\infty} \delta\left(\omega - k\frac{2\pi}{T_s}\right) \tag{2.4}$$

From Eq. 2.2, since the multiplication procedure in the time domain is equivalent to convolution in the frequency domain, it is possible to write Eq. 2.5.

$$Y(j\omega) = \frac{1}{2\pi} X(j\omega) \bigotimes S(j\omega) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} X\left(j\omega - \frac{jk2\pi}{T_s}\right) \tag{2.5}$$

Fig. 2.5 and 2.6 illustrate the sampling process in the time and frequency domain respectively. Concerning Fig. 2.5, x(t) represents the input signal, s(t) the sampling function (Dirac pulses) and y(t) the sampled signal. In regards to Fig. 2.6, the spectrum of the input signal X(f), the sampling signal S(f) and the sampled output Y(f) are shown.

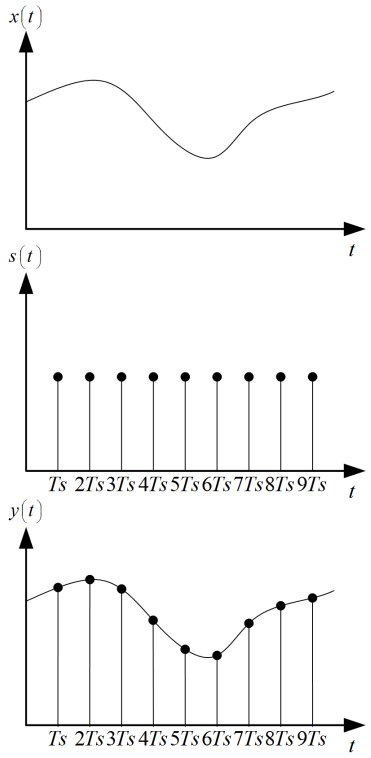


Figure 2.5: Sampling process in the time domain.

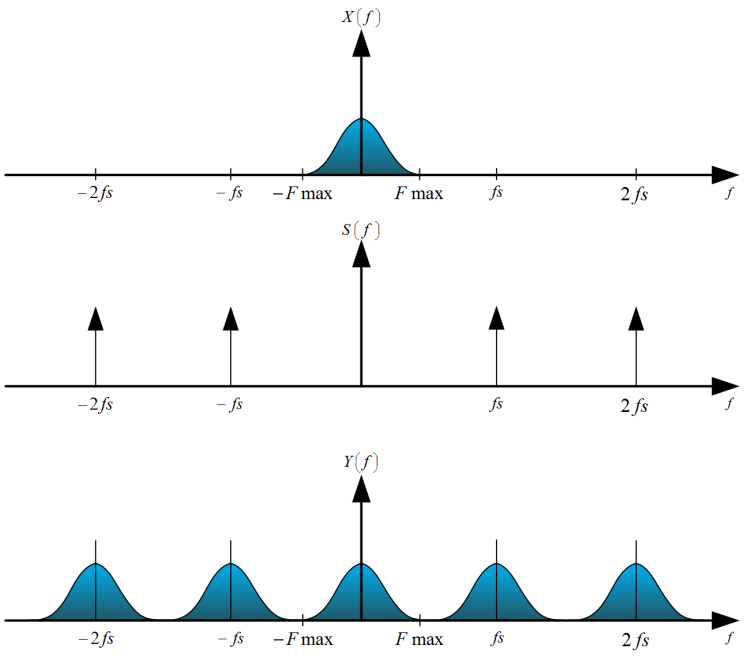


Figure 2.6: Sampling process in the frequency domain.

The spectrum separation between each spectral repetition of the input signal depends directly on the sampling frequency ($f_s = \frac{1}{T_s}$), as Eq. 2.5 shows. Thus, smaller sampling frequencies narrow the gap between each spectral repetition. If f_s is too low, an effect called *aliasing* occurs (shown in Fig. 2.7). This refers to a high-frequency component in the spectrum of the input signal apparently taking on the identity of a lower frequency in the spectrum of a sampled version of the signal (espectral overlap). Fig. 2.7 shows that it is impossible to recover the original input spectrum without distortion, due to *aliasing* [3], [10], [11].

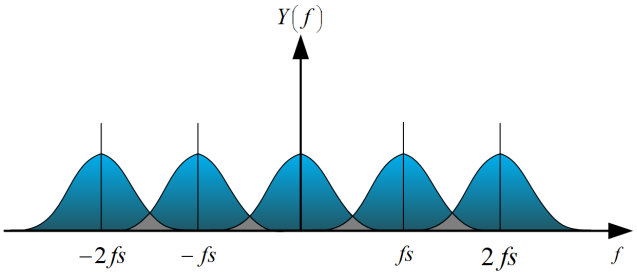


Figure 2.7: Aliasing Effect.

In order to avoid this effect, as stated by the *Nyquist-Shannon Theorem* [3], a signal can be sampled with no loss of information if the sampling frequency (f_s) is at least two times higher than the maximum signal frequency (B)[1]. This sampling frequency is called the Nyquist Frequency (f_N):

$$f_N = 2 \cdot B \tag{2.6}$$

It is possible to recover the original signal through the use of an ideal low pass filter with a cut-off frequency of B.

Data converters that use $f_s = 2 \cdot B$ are called Nyquist converters, while converters that use sampling frequencies that are greater than two times the maximum signal frequency ($f_s \gg 2 \cdot B$) are called Oversampling converters. The latter will be further explored in section 2.4.

Data converters in general have common performance metrics, which are usually are classified into two categories: static and dynamic. The latter can be further subdivided into spectral, frequency domain and power metrics [12]. Those most used to evaluate the overall performance of a ΣΔM and used in this work are briefly discussed below.

- **Signal-to-Noise Ratio (SNR)**: The SNR of a converter is given by the ratio of the signal power to the noise power at the output of said converter, for a certain input amplitude. It doesn't take into account the harmonically related signal components.
- **Signal-to-Noise-and-Distortion Ratio (SNDR)**: The SNDR of a converter is the ratio of the signal power to the noise and all distortion power components. Thus, it

[1]This can be enforced if a low pass pre-alias filter is used, prior to sampling, to attenuate the high-frequency components of the signal that lie outside the band of interest.

takes into account several of the harmonics (at least the 2nd and the 3rd harmonic) that lie inside the band of interest.

- **Dynamic Range (DR)**: The range of signal amplitudes over which the structure operates correctly, i.e. within acceptable limits of distortion. It is determined by the maximum amplitude input signal and by the smallest detectable input signal.
- **Total Harmonic Distortion (THD)**: Ratio of the sum of the signal power of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency. The harmonic distortion generated by a specific nth harmonic can also be determined and is given by the ratio between the signal power and the power of the distortion component at that nth harmonic of the signal frequency.

2.3 Quantization Noise

The Nyquist-Shannon Theorem ensures that if the sampling frequency is at least two times the signal bandwidth, no distortion will be introduced. The same cannot be said about quantization. While sampling concerns time, quantization deals with amplitude [11].

After the samples of the analog input signal are acquired (through sampling), they must then be converted into a digital signal. This is done through the quantizing process. It has a staircase characteristic (shown in Fig. 2.8) and the difference between two adjacent quantized values is called *step size* (Δ). For large input values the quantizer output may saturate. The conversion range for which the quantizer doesn't overload is referred as the full scale (FS) range of the quantizer. A quantizer with a number N of bits, can represent up to 2^N amplitude levels, resulting in a Δ given by

$$\Delta = \frac{FS}{2^N} \tag{2.7}$$

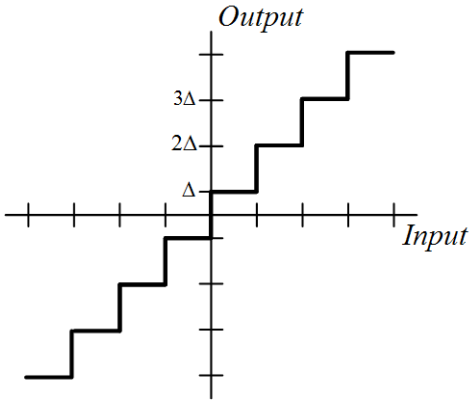


Figure 2.8: Quantizing Characteristic.

All input values will be rounded off to the nearest corresponding amplitude level, when applied to a quantizer with such characteristic (Fig. 2.8). Since these amplitude

levels cannot possibly be exactly equal to each input value, there is always some error associated with the quantizing process [4], [10], [11]. This error is called *Quantization Error* (q_e)[2]. Also, since the input and output range of the quantizer are not necessarily equal, the quantizer can show a non-unity gain k.

From Fig. 2.8, it's apparent that this quantization error has a maximum value of $\frac{\Delta}{2}$ and the total range of variation of this error is distributed over a range of values that go from $-\frac{\Delta}{2}$ to $+\frac{\Delta}{2}$ [4], [11]. Since the quantization error is considered a random process, uncorrelated with the input signal, it can be regarded as white noise, spread across the considered range with equal likelihood.

The average power of q_e (P_{q_e}) can thus be determined by averaging q_e^2 over all possible values of q_e, as follows

$$P_{q_e} = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} q_e^2 \, dq_e = \frac{\Delta^2}{12} \tag{2.8}$$

From Fig. 2.8, the higher the resolution of the quantizer, the smaller Δ is. Thus, by increasing the number of bits (N) of the quantizer, the noise power decreases. Specifically, for each additional bit in the quantizer, the noise power decreases by 6.02 dB [3], [4], [11]. Hence the SNR is increased by 6 dB.

When a signal is sampled at a frequency f_s, the quantization noise distribution is uniform along the frequency range $[-\frac{f_s}{2}; +\frac{f_s}{2}]$, since it is considered white noise. Thus, the spectral noise power distribution is given by Eq. 2.9.

$$E(f) = \frac{\frac{\Delta^2}{12}}{f_s} = \frac{\Delta^2}{12 \cdot f_s} \tag{2.9}$$

It is clear from Eq. 2.9 that an increase of the sampling frequency will result in the quantization noise being spread over a wider band, thus reducing the noise in the band of interest, as shown in Fig. 2.9. This is one of the major advantages of using a sampling frequency higher than the Nyquist Frequency (in other words, using oversampling).

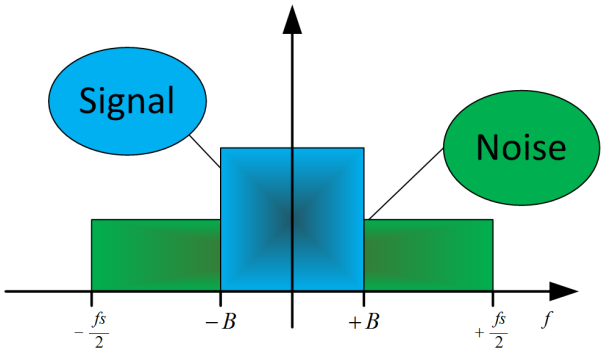


Figure 2.9: Spectral Density of Quantization Noise when using Oversampling.

[2]If the input signal exceeds the valid input range of the quantizer, the result is a monotonously increasing quantization error.

2.4 Oversampling

In many applications, such as digital audio, high resolution and linearity is required. Most standard Nyquist converters cannot provide the accuracy needed, and those that do, are too slow for signal-processing applications. Oversampling converters are capable of trading conversion time for resolution, by using simple high-tolerance analog components. Nevertheless, they require fast and complex digital signal processing stages [4], [11].

This tradeoff becomes acceptable since high-speed digital circuitry can be easily manufactured in less area, while high-resolution analog circuitry is harder to realize due to low power-supply voltages and poor transistor output impedance caused by short-channel effects [3].

For an input signal bandlimited to B, oversampling occurs when f_s is higher than two times B ($2B$ being the Nyquist frequency). The ratio between f_s and the Nyquist frequency is called Oversampling Ratio (OSR) [11] and is given by

$$OSR = \frac{f_s}{2B} \tag{2.10}$$

From Eq. 2.10, $f_s = 2 \cdot B \cdot OSR$. Applying it to Eq. 2.9 leads to Eq. 2.11,

$$E(f) = \frac{\frac{\Delta^2}{12}}{2 \cdot B \cdot OSR} = \frac{\Delta^2}{24 \cdot B \cdot OSR} \tag{2.11}$$

Eq. 2.11 shows that if the OSR is doubled (i.e., sampling at twice the rate), the spectral noise power decreases by 3 dB.

As seen in section 2.1, to recover the information from the sampled signal, a low pass filter is used to remove the spectral repetitions. This low-pass filter requires a sharp cut-off frequency response when Nyquist converters are used, since they cause the spectral repetitions to be very close to each other. This is another advantage of Oversampling converters: by using greater sampling frequencies, the spectral repetitions are more distant from one another. Therefore, simpler filters can be used.

Since the audio band is composed by low frequencies (ranging approximately from 20 Hz to 20 kHz), the use of Oversampling converters applied to audio applications should not pose a problem since today's electronics maximum frequency can be very high (up to GHz). However, due to the parasitics of the output stage, f_s should not be very high (above 2 MHz) in order to achieve high efficiency.

2.5 Continuous-Time (CT) Sigma-Delta Modulators (ΣΔM)

The block diagram of a generic ΣΔM is shown in Fig. 2.10. It's composed of a certain filter (typically designated as the *loop filter*) with a $H(s)$ transfer function, followed by the quantizer and a feedback loop.

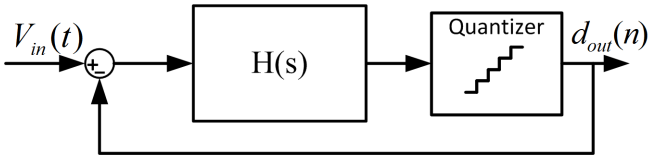


Figure 2.10: Block diagram of a generic CT-ΣΔM.

In the last decades most of the work regarding ΣΔM has been realized in discrete-time (DT) circuits, through a switched-capacitor (SC) implementation. DT-ΣΔM are used due to the design ease of SC filters and the high degree of linearity obtained in the circuits realized. However, the design of CT-ΣΔM is also feasible. In fact, ΣΔM was first proposed in the 1960s [13] through a CT implementation. CT-ΣΔMs can be distinguished from their discrete-time counterparts by the following:

- **Sampling Operation**: In CT-ΣΔM, the sampling operation takes place inside the ΣΔ loop, whereas in the DT-ΣΔM a sample-and-hold circuit is placed before the input of the converter. Therefore, all the non-idealities of the sampling process are included, when using a CT-ΣΔM. However, as it will be shown next, the errors inside the loop of a CT-ΣΔM are filtered out. Moreover, the use of a CT-ΣΔM can result in some kind of implicit antialiasing filtering, making unnecessary the use of a pre-alias filter. In regards to the DT case, every error that the sample-and-hold circuit generates adds to the input signal. Concerning clock jitter, CT-ΣΔMs are more susceptible to timing errors and the resulting SNR can be degraded, unlike DT-ΣΔMs who use SC circuits to realize the loop filter. However, the sampled noise may be aliased if the switch and capacitance time constant are much smaller than the sampling period. Therefore, the gain-bandwidth product (GBW) of the loop filter amplifiers in a DT-ΣΔM realization limits the sampling frequency used.

- **Filter Realization**: As it will be explained ahead in this section, the loop filter is typically implemented with integrators (which can be DT or CT). While in DT implementations, based on SC circuits, the gain is determined by a capacitor ratio and is very precise, CT integrator gains typically depend on a RC or gmC product. These are subject to large process dependent variations, that may lead to mismatches and in worst case an unstable system. Also, the non-linearity of the passive/active components used contributes to the harmonic distortion at the modulator output. In CT-ΣΔMs, the first stage generally defines the overall accuracy of the system.

- **Quantizer Realization**: In both DT and CT implementations, the non-idealities of the quantization process are averaged out, since the quantizer resides within the

feedback loop. However, the decision time of the quantizer has a different influence for each implementation: CT-ΣΔMs ideally need a very fast quantization since the result is needed right away to generate the correct CT feedback signal. DT systems, on the flip side, allow this decision time to last until half of a sampling period.

- **Feedback Realization**: In the DT system the feedback signal is applied by charging a capacitor to a reference voltage and discharging it onto the integrating capacitance, while in the CT realization the feedback waveform is integrated over time. Therefore, CT-ΣΔMs are sensitive to every mismatch on the feedback waveform that may occur due to clock jitter or loop delay, for example. Nevertheless, there are a set of solutions to overcome this problem [14], [15].

These differences and many more that distinguish DT and CT-ΣΔMs are presented and exploited in literature [4], [11], [12]. Table 2.1 highlights the main ones.

Table 2.1: Main differences between CT and DT ΣΔMs.

	CT-ΣΔM	DT-ΣΔM
Sampling Frequency	Not very sensitive to the amplifiers GBW	Limited by the GBW of loop filter amplifiers
Power Consumption	Lower	Higher
Anti-aliasing	Inherent	External filter needed
Sampling Errors	Shaped by the loop filter	Appear directly at the ADC output
Clock Jitter	Sensitive	Robust
Process Variations	Sensitive	Accurate

In order to analyse the theoretical behaviour of a CT-ΣΔM, a linear model of the block diagram presented in Fig. 2.10 is shown in Fig. 2.11. Since quantization is a non-linear operation (thus impossible to include directly in the model), the model is shown having two independent inputs, the quantized input signal and the quantization error (the latter is perceived as noise).

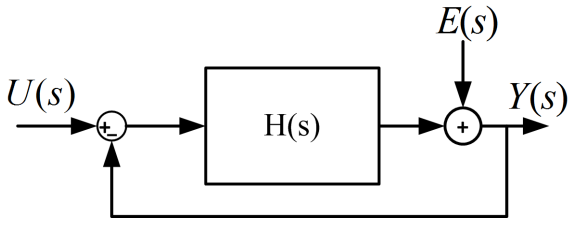


Figure 2.11: Linear Model representation for the ΣΔM.

Two separate transfer functions can be derived from Fig. 2.11. STF concerns the signal transfer function, while NTF represents the noise transfer function.

$$S_{TF}(s) = \frac{Y(s)}{U(s)} = \frac{H(s)}{1 + H(s)} \tag{2.12}$$

$$N_{TF}(s) = \frac{Y(s)}{E(s)} = \frac{1}{1 + H(s)} \tag{2.13}$$

Eq. 2.13 shows that when $H(s)$ goes to infinity, NTF goes to zero. This is due to the feedback loop, capable of averaging out the quantization error, since it is fed back negatively. Therefore, it's possible to greatly attenuate the noise over the frequency band of interest, while leaving the signal itself unaffected, by choosing $H(s)$ such that it has a large gain over the signal band. This process is called *noise-shaping* [3]. The use of noise-shaping applied to oversampling signals is commonly referred to as ΣΔ modulation. It refers to the process of calculating the difference (Δ) between both the output and the input signal and integrating (Σ) it [3], [11].

To perform noise-shaping, $NTF(s)$ should have a zero at dc (i.e., s = 0) so that it has a high-pass frequency response. Since the zeros of NTF correspond to the poles of $H(s)$, letting $H(s)$ be a continuous-time integrator (having a pole at s = 0) allows the NTF to present such response, as shown in Eq. 2.14 and 2.15. For a single stage ΣΔM, this results in a noise-shaping with a +20 dB/dec slope.

$$S_{TF}(s) = \frac{1}{s + 1} \tag{2.14}$$

$$N_{TF}(s) = \frac{s}{s + 1} \tag{2.15}$$

Eq. 2.14 and 2.15 also show that the use of integrators allows the STF to have unitary gain. Thus, the quantization noise is reduced over the frequency band of interest and the signal is left largely unaffected. Therefore, a greater SNR/SNDR can be achieved, as desired. A ΣΔM can be implemented through a cascade of integrator stages. For each stage, the noise-shaping slope increases by +20 dB/dec [4].

To design the NTF of the loop filter, several noise-shaping functions can be used. The most common are the Butterworth High-Pass response and the Inverse Chebyshev High-Pass Response (although others could be used, like pure differentiators [11]).

Intuition would lead to think that in order to nearly eliminate the noise from the frequency band of interest, all that is needed to do is to add further integrator stages. However, this cannot be done in a direct fashion.

Through all the advantages that ΣΔM bring, as all systems employing feedback they present some *stability* issues that need to be addressed. These issues are justified, since each integrator stage adds a -90 degrees phase shift. Thus, ΣΔMs can become unstable whenever the loop filter order is larger than 2.

Unfortunately, there is no certain solution for the stability issues of the ΣΔMs, since

they include a quantizer, which is non-linear element. Therefore, circuit designers usually follow a *rule of thumb* (Lee's Criterion), which states that the peak frequency response gain of the NTF should be less than 1.5 [4], [11]. In mathematical terms,

$$\left|N_{TF}(e^{j\omega})\right| \leq 1.5 \tag{2.16}$$

, for $0 \leq \omega \leq \pi$. This *rule* is not mandatory, as its value may range from 1.3 to 1.8 depending but not limited to the order of the modulator.

Another way of performing a stability analysis of the system is through the use of the root-locus graph. As with any CT system, the poles must be positioned on the left-half of the complex plane and should not cross over to the right-half of the imaginary axis. Each integrator stage of the ΣΔM adds a pole at the origin. It's shown in [12], [16] that each of these poles move directly into the right-half plane, if a linear model is used and the quantizer is modelled as $ke^{s\theta}$ (where k is the quantizer gain and θ the phase shift), for any value of k and θ.

Hence, to stabilize the ΣΔM, a zero (or more than one) can be introduced in the loop filter transfer function to counter the -90 degrees phase shift that each pole of each integrator stage causes. This allows the ΣΔM to be stable for a certain quantizer gain k where the poles are placed in the left-half plane, and can be achieved through feedforward or feedback compensation which can be implemented through several architectures (that in turn implement the noise-shaping functions). These are explored in section 2.6. Also, the amplitude of the input signal should not be too large since it may push the poles to non-stable regions [4], [11], [16].

2.6 Analysis of the ΣΔM Architecture

In this section, the design of the loop filter of the ΣΔM through several architecture options is presented. Both feedforward and feedback techniques are described, and a comparison between the two is made. Although both techniques provide the same NTF, they have different signal transfer characteristics. As seen in section 2.5, the NTF determines how much of the quantization noise is attenuated, thus determining the overall SNDR of the converter. Furthermore, the increase of the quantizer's resolution by 0.5 bit (from traditional 1-bit to 1.5-bit quantization) is discussed and its major advantages presented.

2.6.1 Feedforward Summation

The first topology that is subject of analysis is one in which a cascade of several integrators is put together, where a fraction of the output of each integrator stage is added to the output of the last stage, by means of a weighted feedforward path. It is commonly known as a cascade of integrators with feedforward (CIFF) structure.

The block diagram of a n^{th} order ΣΔM with distributed feedforward is shown in Fig. 2.12. The STF of this structure is given by Eq. 2.17, while the NTF is given by Eq. 2.18.

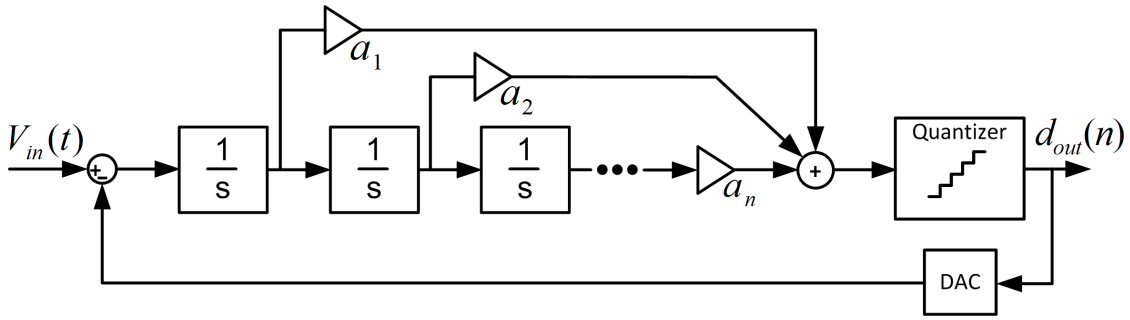


Figure 2.12: Block diagram of a n^{th} order ΣΔM with distributed feedforward.

$$STF = \frac{\sum_{i=1}^{n} a_{n-i+1} \cdot s^{i-1}}{s^n + \sum_{i=1}^{n} a_{n-i+1} \cdot s^{i-1}} \tag{2.17}$$

$$NTF = \frac{s^n}{s^n + \sum_{i=1}^{n} a_{n-i+1} \cdot s^{i-1}} \tag{2.18}$$

In this topology, only the error signal is fed into the loop filter, which consists mainly on quantization noise. Therefore, the first integrator can have large gain to suppress the subsequent stage's noise and distortion [4].

From Eq. 2.18, the zeros of the NTF are all placed at dc. To implement such architecture Butterworth high-pass filters are used, since Inverse Chebyshev NTFs have stopband zeros at non-zero frequencies and thus cannot be used. The cut-off frequency of this filter function is selected in order to limit the maximum gain of the NTF and eliminate the instability of the ΣΔM.

A drawback of adding zeros to the STF is that it will create peaking at a certain frequency due to the resulting filter characteristic [16]. If input signals with these frequencies are applied to this structure, the modulator could overload due to the gain of this peaking. Possible solutions to this issue are the use of a pre-filter or the modification of the NTF such that flat STFs are obtained [11], [12].

2.6.2 Feedforward Summation and Local Resonator Feedback

In the previous structure the NTF zeros are all placed at dc, which limits the effectiveness of noise-shaping only to low frequencies. However, a much better performance can be achieved if these zeros are optimally distributed inside the signal bandwidth, as shown in [11].

This can be achieved by adding a negative-feedback term around pairs of integrators in the loop filter, creating local resonator stages, which allows to move the open-loop

poles (that become the NTF zeros when the loop is closed). This structure is commonly known as a cascade of resonators with feedforward summation (CRFF).

The block diagram of a n^{th} order ΣΔM with distributed feedforward is shown in Fig. 2.13. The general transfer function of a resonator is given by Eq. 2.19, where k_u is the unity-gain frequency of the integrators.

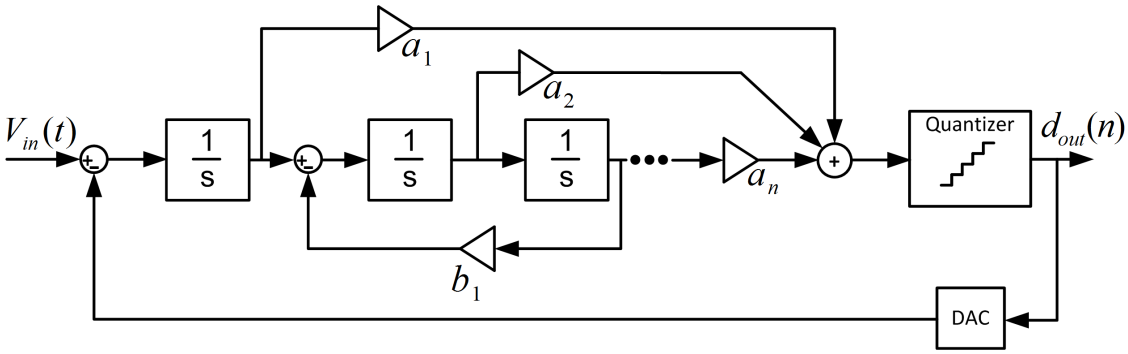


Figure 2.13: Block diagram of a n^{th} order ΣΔM with distributed feedforward and local resonator feedback.

$$H(s) = \frac{k_u \cdot s}{s^2 + {k_u}^2} \tag{2.19}$$

In this case, it is possible to implement the inverse Chebyshev NTF, by picking the stopband edge frequency of the filter. With the zeros spread across the signal bandwidth a better SNR/SNDR can be obtained, when compared to the Butterworth alignment, as the filter presents greater attenuation over the frequency band of interest. From inspection, the NTF of odd order ΣΔMs have always one zero placed at dc, while the NTF of even order ΣΔMs have none, when using this architecture since odd order ΣΔMs have always a plain integrator beyond the cascade of resonators. Typically, this integrator is the input stage of the loop filter in order to minimize the input-referred contributions of noise sources from following stages, as stated in the previous subsection.

In this architecture the drawback of high frequency peaking of the feedforward architecture is alleviated. However, the local resonator coefficients scale with OSR^{-2}. Therefore, they rapidly decrease with the OSR and this technique is more viable for low OSR. The resonators themselves are unstable, due to their pole locations. But since they are inside a stable feedback system local oscillations are prevented. The NTF magnitude response will exhibit one or more notches in its frequency response [4], [11], [12].

2.6.3 Distributed Feedback

In the previous subsections, 2.6.1 and 2.6.2, feedforward was used to improve stability and provide a higher performance for the ΣΔM. Onwards, alternative methods recurring to feedback paths are presented. These paths also create the zeros of the NTF, as in the previous subsections. The structure presented in Fig. 2.14 is a group of cascaded integrators with distributed feedback (CIFB), with each integrator stage receiving a fraction of

the output from the DAC, by means of a weighted feedback path.

The block diagram of a n^{th} order ΣΔM with distributed feedback is shown in Fig. 2.14. The STF of this structure is given by Eq. 2.20, while the NTF is given by Eq. 2.21.

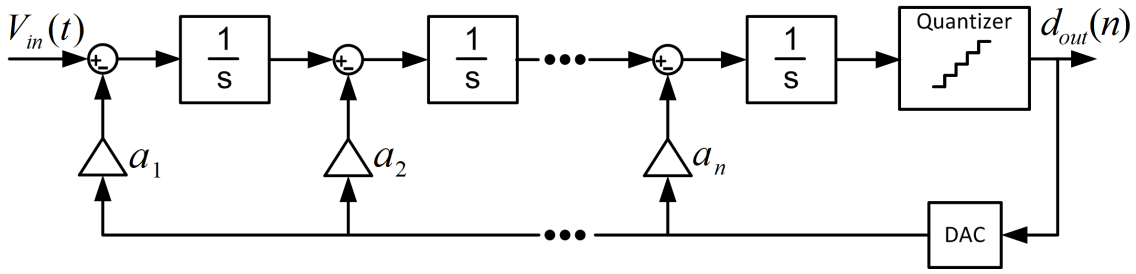


Figure 2.14: Block diagram of a n^{th} order ΣΔM with distributed feedback.

$$STF = \frac{1}{s^n + \sum_{i=1}^{n} a_i \cdot s^{i-1}} \tag{2.20}$$

$$NTF = \frac{s^n}{s^n + \sum_{i=1}^{n} a_i \cdot s^{i-1}} \tag{2.21}$$

While in the CIFF and CRFF structures only the error signal was fed into the loop filter, in the distributed feedback topology the entire output signal (including the input signal and the quantization noise) is fed back to every internal node of the filter.

As in the CIFF structure (subsection 2.6.1), all zeros of the NTF lie at $s = 0$ (dc). Again, the NTF can be seen as a Butterworth high-pass filter and the STF as a Butterworth low-pass filter (note that the STF has no zeros in this structure). As in the CIFF structure, the cut-off frequency of this filter function is selected in order to limit the maximum gain of the NTF and eliminate the instability of the ΣΔM.

One of the downsides of this architecture is that the integrator outputs contain significant amounts of the input signal as well as filtered quantization noise [11].

In this architecture the STF is somewhat dependent of the NTF: by determining the latter, the former is automatically fixed. To overcome this, feedforward paths can be added between the input node and each integrator's summing junction. This is depicted in Fig. 2.15. The STF of this structure is given by Eq. 2.22, while the NTF is given by Eq. 2.23.

$$STF = \frac{\sum_{i=1}^{n} b_{n-i+1} \cdot s^{n-i}}{s^n + \sum_{i=1}^{n} a_i \cdot s^{i-1}} \tag{2.22}$$

$$NTF = \frac{s^n}{s^n + \sum_{i=1}^{n} a_i \cdot s^{i-1}} \tag{2.23}$$

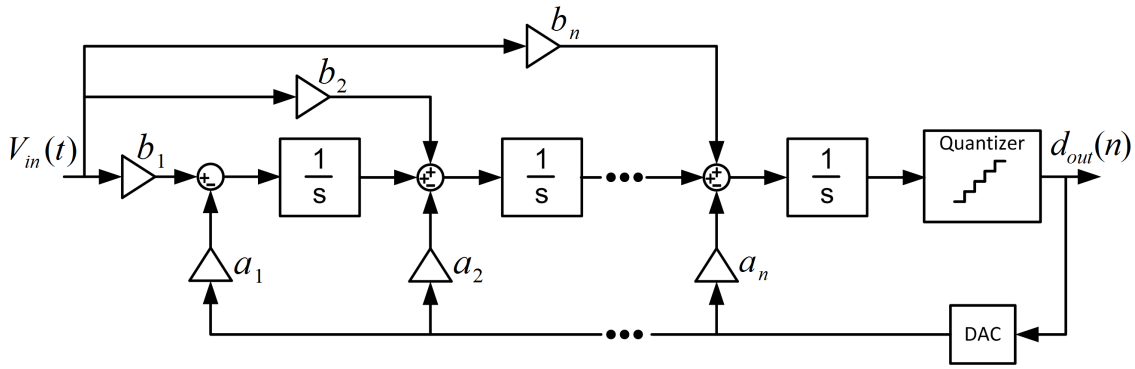


Figure 2.15: Block diagram of a n^{th} order ΣΔM with distributed feedback and distributed feed-forward inputs.

Eq. 2.22 shows that the addition of these paths allows the STF to be independent from the NTF, by properly choosing the values of the b coefficients. Notice that the order of the numerator of Eq. 2.22 is 1 less than the denominator. The zeros of Eq. 2.22 can be placed in a way that it cancels some of the poles, allowing the STF to have a lower roll-off rate [11]. The NTF is exactly the same for both structures (Fig. 2.14 and Fig. 2.15).

2.6.4 Distributed Feedback and Local Resonator Feedback

As in the CRFF structure, local resonator stages can be added to the CIFB structure in order to shift the NTF zeros away from dc and spread over the signal band. Again, this will improve the SNR/SNDR of the modulator. This structure is commonly known as a cascade of resonators with distributed feedback (CRFB).

The block diagram of a n^{th} order ΣΔM with distributed feedback and local resonator feedback is shown in Fig. 2.16.

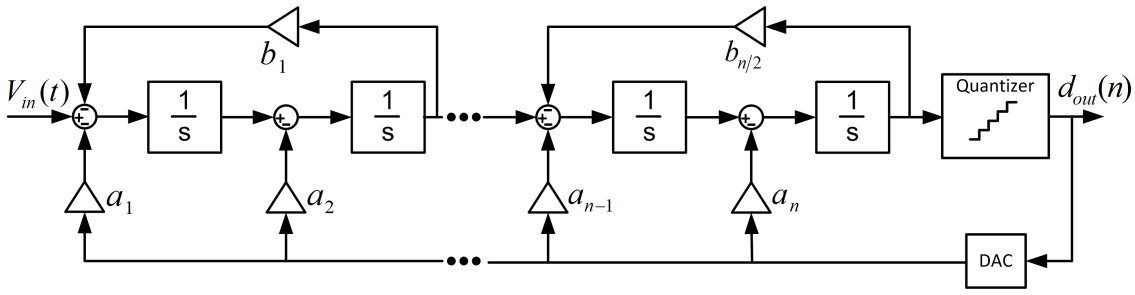


Figure 2.16: Block diagram of a n^{th} order ΣΔM with distributed feedback and local resonator feedback.

The filter coefficients are determined using the same method as in the CRFF structure, i.e. considering the NTF as a representation of a Chebyshev type II filter and choosing its stopband edge frequency.

2.6.5 Comparison between Feedforward and Feedback compensation

As seen in the previous subsections (2.6.1-2.6.4), both feedforward and feedback compensation yield similar results, since both are capable of improving the stability of the loop while the SNR/SNDR of the modulator can be improved by adding local resonator stages. Yet, these topologies are not entirely equal since some differences exist between the two.

The feedforward summation topology only feeds the quantization noise into the loop filter while the distributed feedback topology feeds both the input signal and the quantization noise. Also, the dissipated power of the feedforward compensation is less than in the feedback compensation due to lower internal signal swings.

However, while the STF of an n^{th} order CIFF structure has n poles and n-1 zeros, the STF of an n^{th} order CIFB structure has only n poles. Thus, the former can be interpreted as a first order lowpass filter and the latter as a n^{th} order lowpass filter, meaning that the CIFB structure can provide much stronger filtering for high frequency signals.

Also, due to the non-ideal compensation of STF poles and zeros, the CIFF STF shows peaking at a certain frequency. In contrast, the CIFB STF has no zeros and this peaking is practically non-existent.

Therefore, for the reasons stated above, the architecture chosen for the loop filter is the feedback compensation (both the CIFB and the CRFB structures) since it presents no peaking and provide much stronger filtering. Also, the addition of local resonator stages allows the distribution of the NTF zeros along the signal bandwidth in such a way that the filter presents greater attenuation over the frequency band of interest.

2.6.6 1.5-bit Quantization

As stated in section 2.1, Class D amplifiers typically achieve a power efficiency of at least 90%. However, these efficiency values are obtained through tests that assume ideal situations, where a maximum amplitude signal is applied to the load. Thus, there is a maximum power transfer to the load and the ratio between transferred power and total power consumption leads to a very high power efficiency. When subjected to non-ideal situations, i.e. the input signal's amplitude is not maximum, the power efficiency decreases due to the reducing of power delivered to the load and the impact of switching losses that remain mostly unaltered.

For input signals of zero or near zero amplitude, the power transferred to the load is roughly non-existent but the switching activity remains high. In this case, a very low power efficiency is obtained. Since under normal working conditions the input signal's amplitude may vary from low to high levels, the resulting average Class D power efficiency will be lower than the maximum efficiency obtained through ideal conditions.

Several solutions can be employed to tackle this issue: reducing the power device's parasitic capacitances and conduction resistances, the use of a smaller switching frequency, among others [8]. However, most of them consist in some sort of trade-off where

a slight increase in efficiency leads to a decrease in another important factor or the proposed solution although feasible is not viable.

Still, there is an option that has not yet been discussed: the use of multi-bit quantization instead of traditional 1-bit quantizers. This can reduce unnecessary switching of the output stage power devices, due to the existence of a number of other quantization levels besides the two levels that 1-bit quantization provide.

However, the number of quantization levels that a Class D amplifier can provide is limited by the number of amplitude levels that the output stage can represent. The Half-Bridge circuit can only represent two amplitude levels, those being when the load is connected to either supply voltage (V_{cc} and V_{ss}), making multi-bit quantization impossible. Fortunately, the BTL circuit can provide three levels (1.5-bit), the third being when the load is connected to the same potential on both terminals. This state is generally denominated the *zero-state*, since zero power is transferred to the load.

1.5-bit quantization in general and the zero-state in particular ease the representation of zero/near-zero amplitude input signals, significantly reducing switching activity for both high and low amplitude signals. Therefore, greater power efficiency can be achieved.

Multi-bit quantization exhibits far more advantages than only a power efficiency improvement. For multi-bit quantizers, the loop filter is inherently more stable since the quantizer gain (k) is well-defined (i.e. it can be approximated to be unity) and the no-overload range of the quantizer is increased, improving the linearity of the feedback in the modulator.

Also, as stated in section 2.3, the higher the resolution of the quantizer, the lower the quantization noise is [3], [4], [11], [12]. This will improve the SNR/SNDR of the circuit.

In the particular case of the 1.5-bit quantizer, going from two to three levels leads to the decrease of the quantization error by a factor of two (6 dB). Also, the input range of the modulator is increased by 1.6 dB. A total improvement of around 7.6 dB of the SNDR can be achieved [17].

3

Implementation of the ΣΔM

This chapter presents the design of the ΣΔM architecture chosen in chapter 2. Each constituting block of the circuit is analysed and its influence in the performance of the ΣΔM is investigated.

3.1 Integrator Stages

This section deals with the implementation of the integrator stages of the ΣΔM. Two different approaches, the use of active RC-Integrators or BJT-based Differential Pairs, are studied. There are more approaches that can be used to implement an integrator circuit, such as gmC-Integrators and LC-Resonators, which will not be studied in the development of this thesis.

3.1.1 Integrator Stages using Active RC-Integrators

Active RC-Integrators, shown in Fig. 3.1, poise themselves among the commonly used integrator structures in CT-ΣΔM due to their linearity, low sensitivity to parasitic components, large signal swing and overall power consumption [16]. It's transfer function is given by Eq. 3.1.

$$\frac{V_o(s)}{V_{in}(s)} = -\frac{1}{sRC} \tag{3.1}$$

When the input nodes of this structure meet virtual ground conditions (i.e. the amplifier's gain is high), the input resistors perform a linear V/I conversion. The linearity results are as good as the linearity of these resistors and the finite gain of the amplifier.

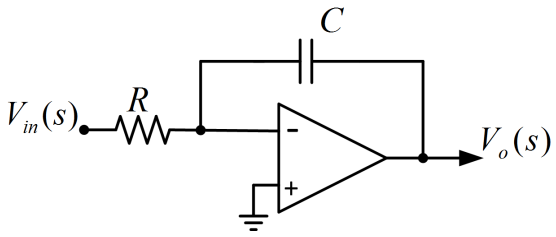


Figure 3.1: Single-Ended Active RC-Integrator.

Distortion can also result from the amplifier's non-linear transfer function and from the matching (or lack thereof) of the input resistors in the fully differential case. The linearity of the integration capacitor is not generally cause for concern, for two main reasons: the inherent linearity of the capacitor is better than that of the resistor and the capacitor itself creates a negative feedback loop around the amplifier, which further reduces distortion [16]. Therefore, the performance of this structure can be improved through the increase of the resistor area or an increase of the DC gain.

3.1.1.1 Sizing of the Active RC-Integrator Stages

In order to design an electrical circuit equivalent to the previously selected architecture, the NTF must be defined (i.e. it's coefficients must be known). A simple method of converting the mathematical model to an electrical circuit is proposed in [18] and shown in Fig. 3.2.

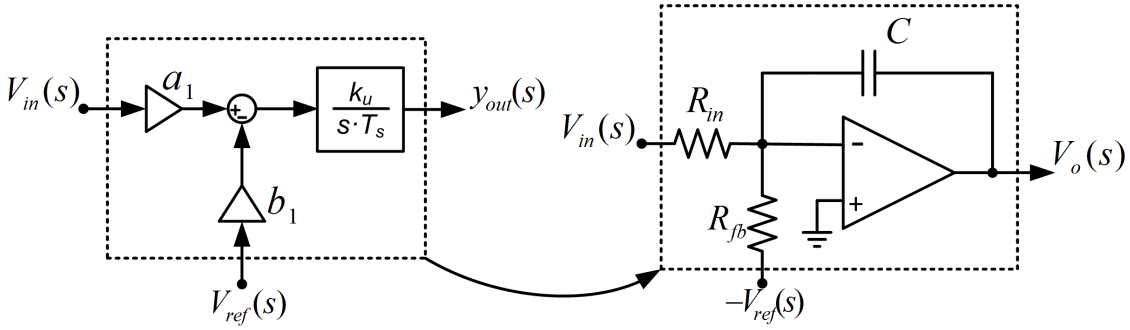


Figure 3.2: Conversion from the Mathematical model to an electrical circuit [19].

, where $T_s = \frac{1}{F_s}$ is the sampling period and k_u represents the unity-gain frequency of the integrator. The values of the a_1 and b_1 coefficients are determined when defining the NTF.

Analysing Fig. 3.2, the $y_{out}(s)$ equation can be written as:

$$y_{out}(s) = \frac{a_1 \cdot k_u}{s \cdot T_s} \cdot V_{in}(s) - \frac{b_1 \cdot k_u}{s \cdot T_s} \cdot V_{Ref}(s) \tag{3.2}$$

, while the $V_o(s)$ equation is given by:

$$V_o(s) = \frac{1}{s \cdot R_{in} \cdot C} \cdot V_{in}(s) - \frac{1}{s \cdot R_{fb} \cdot C} \cdot V_{Ref}(s) \tag{3.3}$$

By considering an ideal operational amplifier and equating Eq. 3.2 and Eq. 3.3, the expressions that give the value of the R_{in} and R_{fb} resistors are obtained:

$$R_{in} = \frac{T_s}{a_1 \cdot k_u \cdot C} \tag{3.4}$$

$$R_{fb} = \frac{T_s}{b_1 \cdot k_u \cdot C} \tag{3.5}$$

The same line of thought can be applied to the other integrator blocks of the modulator. The values of the components can be obtained through this approach, assuming a certain value for the capacitors.

3.1.2 Integrator Stages using Differential Pairs

ΣΔMs work by using negative feedback to reduce the quantization error, where a filter circuit is placed before the quantizer in order to define the frequency band where the quantization error is attenuated. This filter is traditionally built using ideal integrator stages, which are implemented with OpAmps in an integrator configuration, like the one shown in section 3.1.1. These OpAmps require large DC gain and bandwidth in order for the behaviour of the integrator circuits to be close to the ideal integrator behaviour.

This can result in a complex OpAmp circuit that is difficult to design and can dissipate a lot of power. Also, it is difficult to find fully differential OpAmps as discrete components and if the ΣΔM is built using such components, the resulting circuit will most likely be designed in a single ended topology with all the disadvantages associated. By replacing the OpAmps with differential pairs, it is possible to build an equivalent filter circuit for the ΣΔM using lossy integrators. The finite gain and bandwidth of the differential pairs can be accommodated during the filter design process.

A BJT differential pair is constituted by two coupled common-emitter stages through their emitter node, biased by a current source tied to it. Due to its symmetry, the differential output voltage of this circuit does not depend on the input common-mode voltage, leading to a high common-mode rejection ratio (CMRR). However, although the output is independent from the input common-mode voltage, the differential pair's transistors must be biased to operate in the active region. This imposes limits to the input dynamic range [20]. If exceeded, the circuit will cease to behave like its small-signal model and present non-linearities, leading to distortion.

The integrating differential pair circuit is presented in Fig. 3.3. Both capacitors $C_{1,2}$ perform the integration operation, while resistors $R_{C1,2}$ define both the gain and the output common mode DC voltage. Resistors $R_{fb1,2}$ add the feedback signal (a portion of the output signal of the loop filter) to the input signal (V_{in}). Both input resistors ($R_{b1,2}$) limit the voltage applied to the base of the BJT, ensuring that it is low enough to prevent saturation. Also, the current gain of each transistor (here designated as β) must be taken into account. The I_{EE} current source is implemented by a basic BJT current mirror.

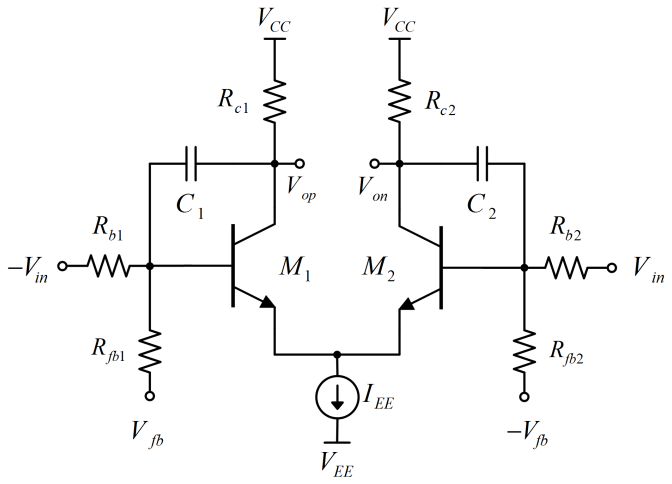


Figure 3.3: Schematic of the integrator Differential Pair (NPN version).

One of the downsides of the BJT Differential Pair is that if several of them are connected in a cascade manner, the output common mode DC voltage will increase up until the point where the BJTs will be unable to behave as desired (in the active region). This would render the Differential Pair useless when connecting several of them in cascade.

Therefore, a complementary version of the NPN version of the BJT Differential Pair is needed, based on PNP BJT's, as shown in Fig. 3.4. Through proper sizing, an increase of the output common mode DC voltage of the NPN Differential Pair is cancelled by the decrease of the output common mode DC voltage of the PNP Differential Pair, thereby preventing saturation.

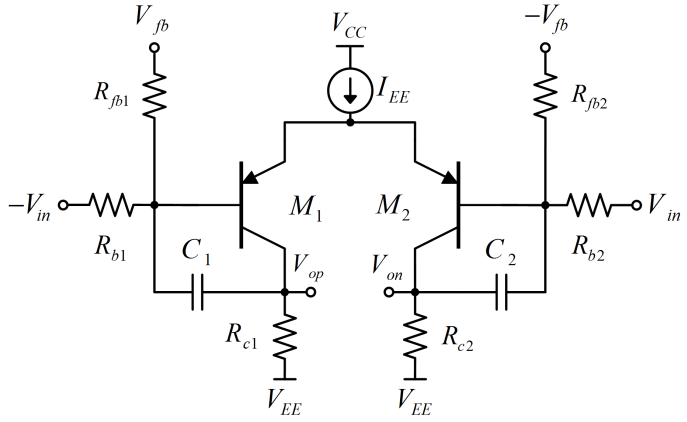


Figure 3.4: Complementary Version of the Differential Pair (PNP version).

In the next subsections, the output voltage expression of the BJT Differential Pair is derived. Three expressions are obtained, each concerning the model used to represent the transistor: one where the transistor's output impedance is neglected, another where it is not and another for the local resonator stage (due to the inclusion of another resistor in the model). Since these expressions are obtained through small signal modelling, they are valid for both NPN and PNP versions of the Differential Pair.

3.1.2.1 Model neglecting r_o

The expression of the output voltage $V_o = V_{op} - V_{on}$ (from Fig. 3.3) can be obtained by applying Kirchhoff's current law (KCL) to the small signal model (hybrid-pi model), when considering the linear behaviour, as shown in Fig. 3.5. KCL states that the algebraic sum of currents in a network of conductors meeting at a certain point is zero.

For the sake of simplicity, here the transistor's output impedance (r_o) is considered infinite, therefore neglected.

Considering the five nodes of the circuit (V_x, V_y, V_{op}, V_{on} and V_z), the equations stated in Eq. 3.6 are obtained. The R_{ee} resistor represents the output impedance of the current source.

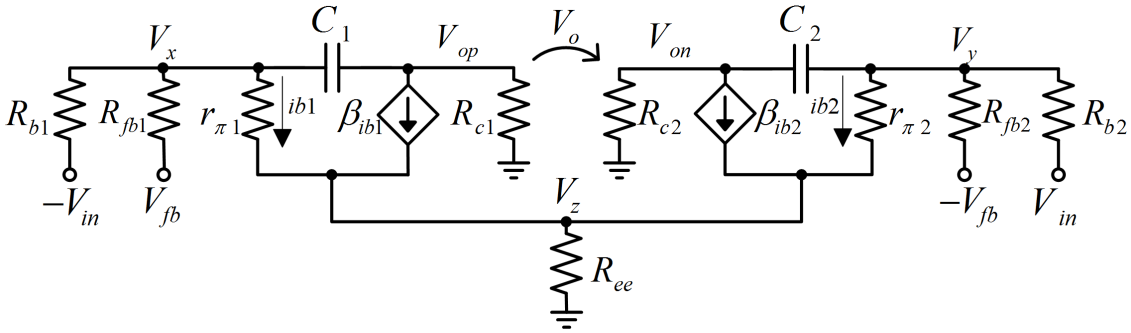


Figure 3.5: Small signal model of the integrator Differential Pair.

$$\begin{cases} -\dfrac{-V_{in}-V_x}{R_{b1}} - \dfrac{V_{fb}-V_x}{R_{fb1}} + (V_x - V_{op})\cdot s\cdot C_1 + \dfrac{V_x - V_z}{r_{\pi 1}} = 0 \\ -\dfrac{V_{in}-V_y}{R_{b2}} - \dfrac{-V_{fb}-V_y}{R_{fb2}} + (V_y - V_{on})\cdot s\cdot C_2 + \dfrac{V_y - V_z}{r_{\pi 2}} = 0 \\ -(V_x - V_{op})\cdot s\cdot C_1 + \dfrac{\beta\cdot(V_x - V_z)}{r_{\pi 1}} + \dfrac{V_{op}}{R_{c1}} = 0 \\ -(V_y - V_{on})\cdot s\cdot C_2 + \dfrac{\beta\cdot(V_y - V_z)}{r_{\pi 2}} + \dfrac{V_{on}}{R_{c2}} = 0 \\ -\dfrac{(\beta+1)\cdot(V_x - V_z)}{r_{\pi 1}} - \dfrac{(\beta+1)\cdot(V_y - V_z)}{r_{\pi 2}} + \dfrac{V_z}{R_{ee}} = 0 \end{cases} \tag{3.6}$$

Considering that $R_{b1} = R_{b2} \rightarrow R_b$, $R_{fb1} = R_{fb2} \rightarrow R_{fb}$, $R_{c1} = R_{c2} \rightarrow R_c$, $C_1 = C_2 \rightarrow C_{int}$ and $r_{\pi 1} = r_{\pi 2} \rightarrow r_\pi$, it is possible to obtain the output voltage of the integrator differential pair by combining the equations above (Eq. 3.6). This output voltage is given by Eq. 3.7.

$$V_o = \frac{2R_c(V_{fb}R_b - V_{in}R_{fb})(sC_{int}r_\pi - \beta)}{R_{fb}r_\pi(1 + sC_{int}R_c) + R_b(r_\pi + sC_{int}R_c r_\pi + R_{fb}(1 + sC_{int}(\beta R_c + R_c + r_\pi)))} \tag{3.7}$$

, assuming V_{in} and $-V_{in}$ are signals in phase opposition (as are V_{fb} and $-V_{fb}$). In these conditions, even order harmonics (2^{nd}, 4^{th} and so forth) tend to be cancelled when the

differential output is retrieved, reducing distortion and intermodulation, since they appear with the same phase shift on both output branches of the differential pair. Thus, the quality of the circuit will be determined by the 3^{rd} order harmonic (and subsequent odd harmonics)[1].

A look into Eq. 3.7 shows that capacitors $C_{1,2}$ behave like Miller capacitors, introducing an additional zero to the circuit. However, if f_s of the ΣΔM is low, this zero does not pose itself as a problem, since its value is much higher than f_s.

3.1.2.2 Model considering r_o

In the previous subsection, the transistor output impedance was assumed infinite. Here, $V_o = V_{op} - V_{on}$ is obtained considering the effect of r_o, which is modelled with a resistor between the transistor's collector and emitter.

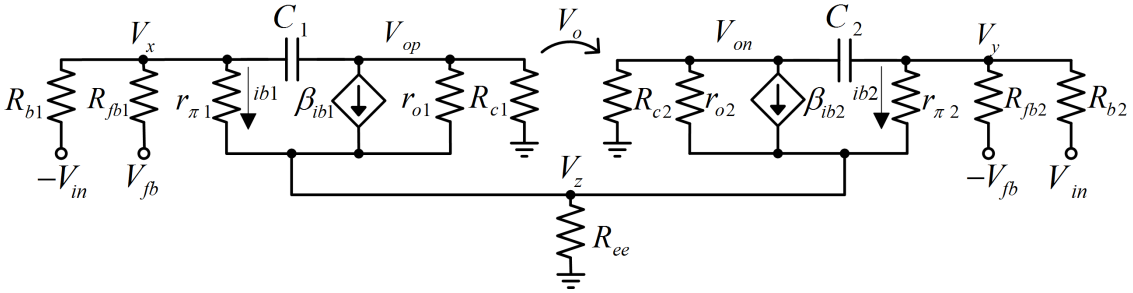


Figure 3.6: Small signal model of the integrator Differential Pair considering r_o.

Again, considering the five nodes of the circuit, the equations stated in Eq. 3.8 are obtained.

$$\begin{cases} -\dfrac{-V_{in}-V_x}{R_{b1}} - \dfrac{V_{fb}-V_x}{R_{fb1}} + (V_x - V_{op})\cdot s\cdot C_1 + \dfrac{V_x - V_z}{r_{\pi 1}} = 0 \\ -\dfrac{V_{in}-V_y}{R_{b2}} - \dfrac{-V_{fb}-V_y}{R_{fb2}} + (V_y - V_{on})\cdot s\cdot C_2 + \dfrac{V_y - V_z}{r_{\pi 2}} = 0 \\ -(V_x - V_{op})\cdot s\cdot C_1 + \dfrac{\beta\cdot(V_x - V_z)}{r_{\pi 1}} + \dfrac{(V_{op}-V_z)}{r_{o1}} + \dfrac{V_{op}}{R_{c1}} = 0 \\ -(V_y - V_{on})\cdot s\cdot C_2 + \dfrac{\beta\cdot(V_y - V_z)}{r_{\pi 2}} + \dfrac{(V_{on}-V_z)}{r_{o2}} + \dfrac{V_{on}}{R_{c2}} = 0 \\ -\dfrac{(\beta+1)\cdot(V_x - V_z)}{r_{\pi 1}} - \dfrac{(V_{op}-V_z)}{r_{o1}} - \dfrac{(\beta+1)\cdot(V_y - V_z)}{r_{\pi 2}} - \dfrac{(V_{on}-V_z)}{r_{o2}} + \dfrac{V_z}{R_{ee}} = 0 \end{cases} \tag{3.8}$$

Making the same assumptions as before ($R_{b1} = R_{b2} \to R_b$, $R_{fb1} = R_{fb2} \to R_{fb}$, $R_{c1} = R_{c2} \to R_c$, $C_1 = C_2 \to C_{int}$, $r_{\pi 1} = r_{\pi 2} \to r_\pi$ and $r_{o1} = r_{o2} \to r_o$), it follows that the V_o voltage is given by Eq. 3.9.

[1] One could also use emitter degeneration to reduce distortion, but this would decrease the voltage gain of each BJT. Since BJT Differential Pairs are being used to replace high-gain OpAmps, this would result in a performance drop.

$$\begin{aligned} V_o =& (2R_c r_o(V_{fb}R_b - V_{in}R_{fb})(sC_{int}r_\pi - \beta))/ \\ & (R_{fb}r_\pi(R_c + r_o + sC_{int}R_c r_o) + R_b(r_o(R_{fb} + r_\pi + sC_{int}R_{fb}r_\pi) \\ & + R_c(r_\pi + sC_{int}R_{fb}r_o r_\pi + R_{fb}(1 + sC_{int}(r_\pi + r_o(1+\beta)))))) \end{aligned} \tag{3.9}$$

Comparing Eq. 3.7 and Eq. 3.9 it follows that the r_o resistor slightly decreases the voltage gain of the differential pair. Since in a typical circuit $r_o \gg R_c$, the gain reduction due to r_o can be neglected.

3.1.2.3 Model for a resonator stage

When designing a CT-ΣΔM in a CRFB structure, the integrator Differential Pair will have another resistor connected to the base of each BJT. This additional resistor, along with the signal from the next integrator stage, allows spreading the zeros along the signal bandwidth as explained in section 2.6. The small signal model is presented in Fig. 3.7.

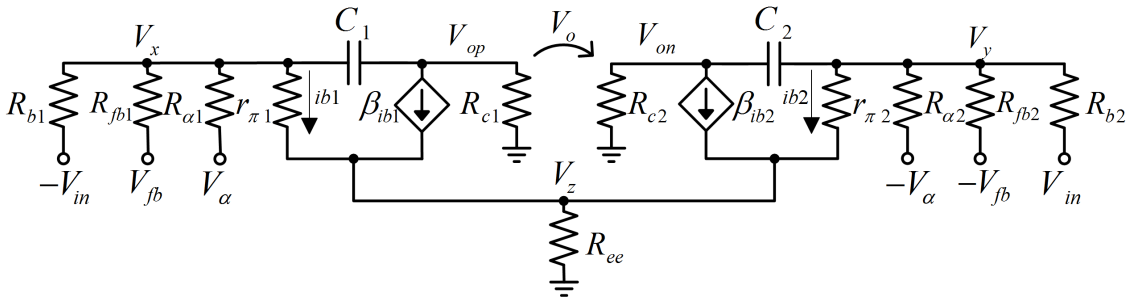


Figure 3.7: Small signal model of the integrator Differential Pair with Resonator resistor.

As before, considering the five nodes of the circuit, the equations stated in Eq. 3.10 are obtained.

$$\begin{cases} -\dfrac{-V_{in}-V_x}{R_{b1}} - \dfrac{V_{fb}-V_x}{R_{fb1}} - \dfrac{V_\alpha - V_x}{R_{\alpha 1}} + (V_x - V_{op})\cdot s\cdot C_1 + \dfrac{V_x - V_z}{r_{\pi 1}} = 0 \\ -\dfrac{V_{in}-V_y}{R_{b2}} - \dfrac{-V_{fb}-V_y}{R_{fb2}} - \dfrac{-V_\alpha - V_y}{R_{\alpha 2}} + (V_y - V_{on})\cdot s\cdot C_2 + \dfrac{V_y - V_z}{r_{\pi 2}} = 0 \\ -(V_x - V_{op})\cdot s\cdot C_1 + \dfrac{\beta\cdot(V_x - V_z)}{r_{\pi 1}} + \dfrac{V_{op}}{R_{c1}} = 0 \\ -(V_y - V_{on})\cdot s\cdot C_2 + \dfrac{\beta\cdot(V_y - V_z)}{r_{\pi 2}} + \dfrac{V_{on}}{R_{c2}} = 0 \\ -\dfrac{(\beta+1)\cdot(V_x - V_z)}{r_{\pi 1}} - \dfrac{(\beta+1)\cdot(V_y - V_z)}{r_{\pi 2}} + \dfrac{V_z}{R_{ee}} = 0 \end{cases} \tag{3.10}$$

Making the same assumptions as before ($R_{b1} = R_{b2} \to R_b$, $R_{fb1} = R_{fb2} \to R_{fb}$, $R_{c1} = R_{c2} \to R_c$, $C_1 = C_2 \to C_{int}$, $r_{\pi 1} = r_{\pi 2} \to r_\pi$ and $R_{\alpha 1} = R_{\alpha 2} \to R_\alpha$), it follows that the V_o voltage is given by Eq. 3.11.

$$\begin{aligned} V_o =& (2R_c(V_{fb}R_bR_\alpha + V_\alpha R_bR_{fb} - V_{in}R_{fb}R_\alpha)(sC_{int}r_\pi - \beta))/ \\ & (R_{fb}R_\alpha r_\pi(1 + sC_{int}R_c) + R_b(R_\alpha r_\pi(1 + sC_{int}R_c) \\ & + R_{fb}(r_\pi + sC_{int}R_cr_\pi + R_\alpha(1 + sC_{int}(r_\pi + R_c(1 + \beta)))))) \end{aligned} \tag{3.11}$$

3.1.2.4 Sizing of the Differential Pair Integrator Stages

After selecting the desired loop filter architecture and having both the STF and the NTF transfer functions determined, the value of their coefficients must be obtained. This was done by two different ways: by analytical sizing and through the use of a genetic algorithm tool.

- **Analytical Sizing**: The first step in this method is to determine the ideal NTF intended for the loop filter (Butterworth/Inverse Chebyshev High-Pass response, etc.) and obtain its coefficients. Afterwards, the output signal of the generic integrator stage is replaced by the V_o equation that was obtained before and a new transfer function of the loop filter is evaluated. This is equated to the generic transfer function of the selected loop filter's architecture that was obtained previously. Thus, equations that relate each coefficient of the latter transfer function to the constituting components (capacitors and resistors) of the Differential Pair are obtained. These equations have several degrees of freedom and in order to size the filter, some component values have to be assumed, like the R_b resistors and the capacitor values. As stated before, the R_c resistors define the output common mode DC voltage. Assuming that the Differential Pair is evenly matched, half of the biasing current will flow through each of its branches. Therefore, the equation that defines the value of the R_c resistors is known and depends only on the supply voltage and the biasing current value. Also, the input impedance of the transistor (r_π resistor) can be estimated through the following :

$$r_\pi = \frac{2\beta V_T}{I_{EE}} \tag{3.12}$$

, where V_T represents the thermal voltage (and at room temperature is estimated to be about 25 mV). Depending on the BJT chosen to implement the Differential Pair, the current gain (β) for both the NPN and the PNP can also be estimated. After making all of these assumptions, the value of the feedback resistors (R_{fb}) can be obtained. With the circuit sized, pole-plotting is performed to verify the stability. Both the STF and the NTF can be plotted to confirm the correct design of the modulator. In order to prevent the BJT from saturation, the signal gain between each integrator stage can be observed and if it is very high, the input resistors (R_b) value should be increased. A more detailed description of this method, together with a practical example, is presented in Appendix A.

- **Genetic Algorithm**: Although fairly accurate, the previous sizing method is very time-consuming and requires care when handling the design equations. In order to optimize the sizing procedure, a genetic algorithm tool was used, proposed in [5]. It uses the design equations to obtain the optimal component values (capacitors and resistors in this case) and evaluates the overall performance of the ΣΔM. Not only is this method faster than the previous, it also takes into account several details like thermal noise and maximum voltage swing, something that the previous method did not. It also picks the design solution that is the most insensitive to component variations, by running Monte Carlo simulations.

3.2 1.5-bit ADC for a Fully Differential Integrator Stage

This section deals with the implementation of the 1.5-bit ADC of the ΣΔM. To achieve 1.5-bit quantization (three levels), the integrator output voltages must be compared with a certain threshold voltage, as stated in Eq. 3.13.

$$\Delta V_o - V_t > 0 \tag{3.13}$$

Typical 1.5-bit quantizers for single-ended architectures use two comparators, like in [18]. For a fully differential architecture, a replica of this structure would result in the use of at least four comparators. Also, this architecture can pose a problem in terms of the common-mode output voltage of each comparator. In the interest of reducing the number of comparators used, and surpass the common-mode issue, the circuit in Fig. 3.8 was designed.

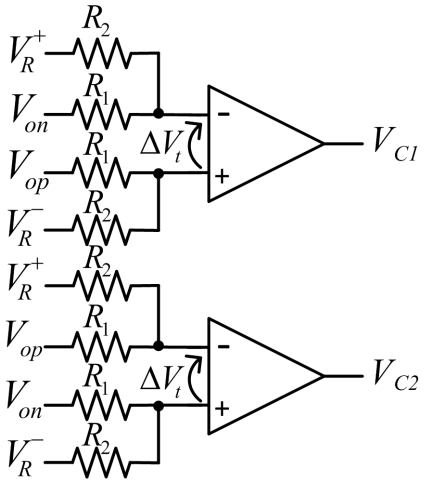


Figure 3.8: 1.5-bit ADC for a Fully Differential Architecture.

The threshold voltage is generated through a voltage divider between the V_o voltages (V_{op} and V_{on}) and two reference voltages (here denoted as $V_R{}^+$ and $V_R{}^-$). Concerning the upper part of the ADC, the threshold voltages are given by Eq. 3.14 and Eq. 3.15 (applying the superposition theorem).

$$V_t{}^+ = V_{op} \cdot \frac{R_2}{R_1 + R_2} + V_R{}^- \cdot \frac{R_1}{R_1 + R_2} \tag{3.14}$$

$$V_t{}^- = V_{on} \cdot \frac{R_2}{R_1 + R_2} + V_R{}^+ \cdot \frac{R_1}{R_1 + R_2} \tag{3.15}$$

Combining Eq. 3.14 and Eq. 3.15, Eq. 3.16 is obtained:

$$\Delta V_t = V_t{}^+ - V_t{}^- = \Delta V_o \cdot \frac{R_2}{R_1 + R_2} - \Delta V_R \cdot \frac{R_1}{R_1 + R_2} \tag{3.16}$$

Rearranging the right side of Eq. 3.16, it follows that,

$$\frac{R_2}{R_1 + R_2} \cdot \left(\Delta V_o - \Delta V_R \cdot \frac{R_1}{R_2} \right) \tag{3.17}$$

, where the expression within parenthesis is similar to Eq. 3.13. Thus,

$$\Delta V_R \cdot \frac{R_1}{R_2} = V_t \tag{3.18}$$

From Eq. 3.18, it is possible to obtain a relationship (Eq. 3.19) between R_1 and R_2, for a given V_t, $V_R{}^+$ and $V_R{}^-$:

$$R_1 = \frac{V_t}{\Delta V_R} \cdot R_2 \tag{3.19}$$

The $V_R{}^+$ and $V_R{}^-$ voltages can be the positive and negative power supply used in the circuit, in order to reduce the number of independent voltage sources used. The V_t voltage is determined by the Genetic Algorithm proposed in [5], where its optimal value is the one where the best possible SNDR value is obtained. The ADC codification is given by Table 3.1 and a representation of the state variation over time is shown in Fig. 3.9.

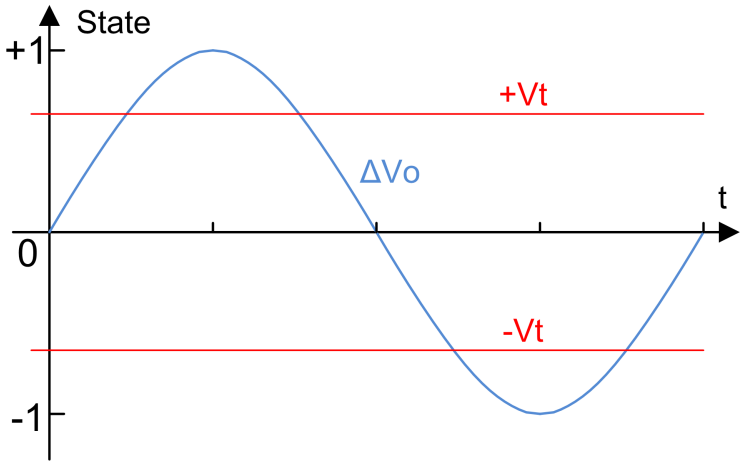


Figure 3.9: State Variation over time.

Table 3.1: ADC codification.

Condition	State
$\Delta V_o > +V_t$	+1
$+V_t > \Delta V_o > -V_t$	0
$\Delta V_o < -V_t$	-1

As stated, this circuit is also capable of effectively rejecting the common-mode. This can be shown by Eq. 3.20, based on Eq. 3.16.

$$\frac{V_t^+ + V_t^-}{2} = \frac{V_{op} + V_{on}}{2} \cdot \frac{R_2}{R_1 + R_2} - \Delta V_R \cdot \frac{R_1}{R_1 + R_2} \tag{3.20}$$

Dividing the right side of Eq. 3.20 by R_2, and considering that $R_2 \gg R_1$, it follows that the output common-mode voltage of the 1.5-bit ADC will be equal to the input common-mode voltage.

3.3 Encoding Logic for the 1.5-bit Quantizer

The output of the comparators can be encoded to 1.5-bit representation using only two D-type Flip-Flops (FFD), where the comparator voltage applied to the D-input, in a certain clock cycle, is retrieved at the Q output in the following clock cycle, as shown in Fig. 3.10. The logic codification of the 1.5-bit quantizer is shown in Table 3.2.

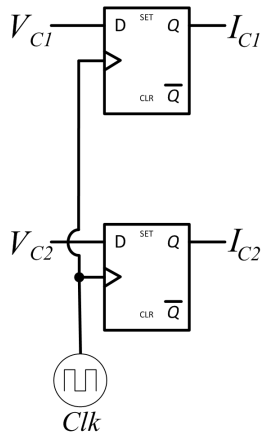


Figure 3.10: Original Encoding Logic.

Table 3.2: Original Logic Codification.

V_{C1}	V_{C2}	State	I_{C1}	I_{C2}
0	0	0	0	0
0	1	-1	0	1
1	0	+1	1	0
1	1	x	x	x

Although simple and capable of performing the required 1.5-bit codification, a problem arises when connecting this encoding logic to the output stage. Since this is a Class D audio power amplifier, its output power devices operate as switches, as stated in chapter 2, and will most likely be implemented by transistors. These transistors may introduce errors due to excessive use, when the bit stream coming from the encoding logic is the same for long periods of time.

To shorten this possibility, another encoding logic is designed, where when the considered bit stream occurs, the switches alternate between the "on" and "off" state between each clock period. This can be achieved through the use of a 1-bit counter, made with another FFD, where its state toggles on every clock period, by wiring the $\overline{Q}$ output to the D input of the considered FFD.

This 1-bit counter should only be used when both outputs of the 1.5-bit quantizer equal 0. Therefore, a NOR (or, in alternative, an XNOR) gate should be used, combining the two outputs of the quantizer. Furthermore, the output of this NOR gate should be connected to the input of an AND gate together with the main clock of the circuit (which defines the sampling frequency). The output of this second AND should then be used as the clock of the 1-bit counter.

By naming each switch of the output stage from SW_1 to SW_4 (as seen in Fig. 3.11), it's possible to set up a truth table (shown in table 3.3) with three inputs (both outputs of the quantizer and the output of the 1-bit counter) and four outputs (from 1 to 4, each connecting to the correspondent switch). This way, boolean equations can be retrieved and the desired encoding logic can be designed.

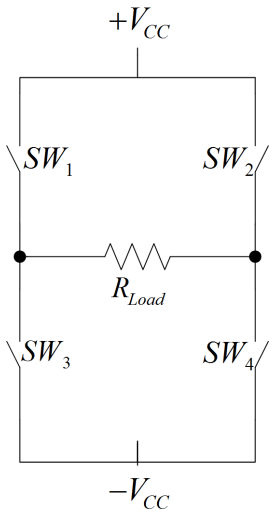


Figure 3.11: Simplified Model of Output Stage.

Table 3.3: New Logic Codification.

I_{C1}	I_{C2}	Q	SW_1	SW_2	SW_3	SW_4
0	0	0	1	1	0	0
0	0	1	0	0	1	1
0	1	0	1	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	1	0
1	0	1	0	1	1	0
1	1	0	x	x	x	x
1	1	1	x	x	x	x

Recurring to a Karnaugh map, it's easy to obtain the correspondent boolean expressions of each switch. Thus:

$$\begin{aligned} SW_1 &= I_{C1} \cdot (\overline{I_{C2}} + Q) \\ SW_2 &= I_{C2} \cdot (\overline{I_{C1}} + Q) \\ SW_3 &= I_{C2} \cdot (\overline{I_{C2}} + \overline{Q}) \\ SW_4 &= I_{C1} \cdot (\overline{I_{C1}} + \overline{Q}) \end{aligned} \tag{3.21}$$

These boolean expressions (Eq. 3.21) comprise several logic operations (AND, OR and NOT). In order to avoid having a wide array of different integrated circuits, all these expressions can be achieved through the use of the NAND logic equivalent. So, the proposed new encoding logic is the one presented in Fig. 3.12:

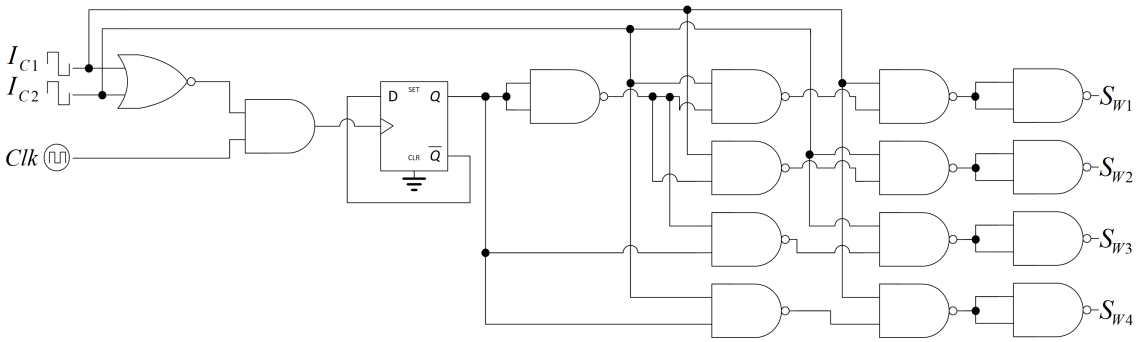


Figure 3.12: Proposed New Encoding Logic - NAND equivalent.

3.4 Feedback Circuitry for a Fully Differential Architecture

In a fully differential architecture, the feedback path can be simply implemented by a pair of resistors (one for each voltage of the differential signal) placed between the circuit output and the input of each integrator stage (when in a feedback structure). This resistor's value is the one that gives the proper feedback coefficient after designing the loop filter, as stated in section 2.6. This single feedback is used in the 1-bit architecture, as shown in Fig. 3.13. Table 3.4 presents the Common Mode Currents and Voltages. Notice that the feedback voltages (denoted before as V_{fb} and $-V_{fb}$) have been replaced by the feedback signal coming from the encoding logic.

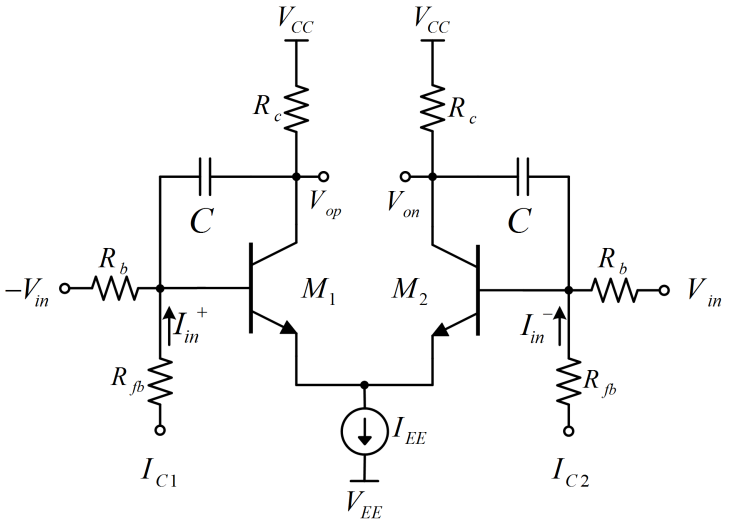


Figure 3.13: Feedback Circuitry for 1-bit Quantization.

Table 3.4: Common Mode Currents and Voltages for 1-bit quantization feedback.

State	I_{C1}	I_{C2}	I_{in}^{+}	I_{in}^{-}	V_{CM}
-1	0 V	5 V	$\frac{V_{CMin}-0}{Rfb}$	$\frac{5-V_{CMin}}{Rfb}$	2.5 V
+1	5 V	0 V	$\frac{5-V_{CMin}}{Rfb}$	$\frac{V_{CMin}-0}{Rfb}$	2.5 V

However, in a 1.5-bit architecture ideally there should be no current flowing in the feedback path when in the zero-state. With a single feedback path, there will always be a current flowing in one way or another. The solution to overcome this is to place a second pair of resistors in parallel with the original feedback resistors, as shown in Fig. 3.14. The other alternative was to design a more complex DAC.

To have near non-existent current flow in the feedback path when in the zero state, this second pair of resistors should be connected to the complementary opposite of the original feedback signal used. The downside is that two more feedback paths are necessary (increasing the total to four), instead of the original two. Table 3.5 presents the Common Mode Currents and Voltages.

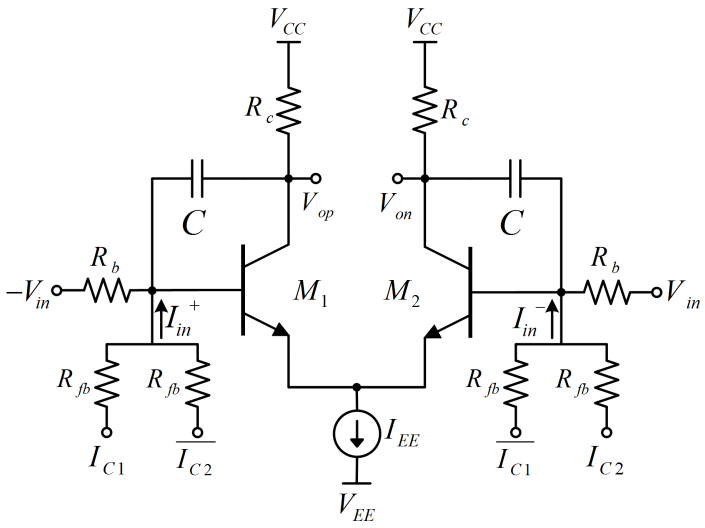


Figure 3.14: Feedback Circuitry for 1.5-bit Quantization.

Table 3.5: Common Mode Currents and Voltages for 1.5-bit quantization feedback.

State	I_{C1}	$\overline{I_{C1}}$	I_{C2}	$\overline{I_{C2}}$	I_{in}^{+}	I_{in}^{-}	V_{CM}
-1	0 V	5 V	5 V	0 V	$\frac{2\cdot(V_{CMin}-0)}{Rfb}$	$\frac{2\cdot(5-V_{CMin})}{Rfb}$	2.5 V
0	0 V	5 V	0 V	5 V	0 A	0 A	2.5 V
+1	5 V	0 V	0 V	5 V	$\frac{2\cdot(5-V_{CMin})}{Rfb}$	$\frac{2\cdot(V_{CMin}-0)}{Rfb}$	2.5 V

During the development of this thesis, possible feedback circuitry for a single-ended implementation were also studied. These were not included in the final design of the CT-ΣΔM, but are nonetheless interesting to consider. Therefore, they are presented and described in Appendix B.

3.5 Simulation Results of the ΣΔM with Differential Pairs

When designing the modulator, one must choose the order and the sampling frequency value of the circuit. Since the main goal is to design an audio amplifier, the signal bandwidth doesn't need to surpass the 20 kHz mark. To reduce the EMI of the amplifier and avoid non-ideal effects in the output power devices a low sampling frequency value should be used. For an ideal 3rd order ΣΔM with an OSR of 32, it is possible to achieve an SNDR value of around 95 dB [4], [11]. However, this value could drop to 65 dB due to the limitations imposed by stability. Nevertheless, an OSR of 32 and a signal bandwidth of 20 kHz yields a sampling frequency of 1.28 MHz.

This section deals with the electrical simulation of several ΣΔM architectures. The simulator considered was LTSpice. In order to establish a comparison between CT-ΣΔMs where the integrator stages are based on traditional Active RC-Integrators (high gain/bandwidth OpAmps) and integrator stages based on differential pairs (the proposed architecture in this work), a 3rd Order 1.5-bit CT-ΣΔM in a CRFB structure using Active-RC Integrators is initially considered. This ΣΔM is sized with the same Genetic Algorithm Tool and its performance is evaluated. Regarding the CT-ΣΔMs where the integrator stages are based on differential pairs, initially the analytical sizing procedure was used to determine the component values of the 1-bit architecture. The Genetic Algorithm Tool was then used to size the 1.5-bit architecture. The supply voltages used were of ± 5 V. The symbolic view shown in Fig. 3.15 is used to ease the representation of the Integrator Differential Pair in a block diagram.

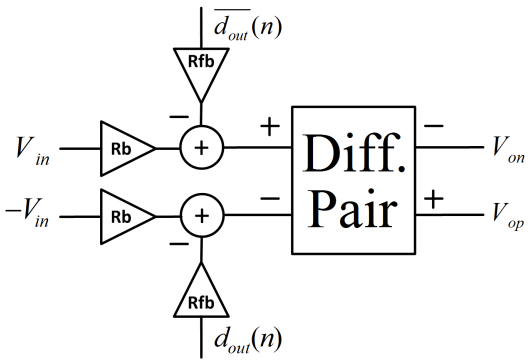


Figure 3.15: Symbolic View of the Integrator Differential Pair.

3.5.1 Simulation Results for a 3rd Order 1.5-bit CT-ΣΔM in a CRFB structure using Active-RC Integrators

A 3rd Order CT-ΣΔM with the NTF zeros spread across the signal bandwidth and with a 1.5-bit quantization scheme was considered, since this is the architecture that yields the best theoretical results [4], [11]. It has three integrator stages (although the last two form a local resonator stage), each one comprised by an Active-RC Integrator.

Rail-to-Rail OpAmps with a open loop gain of around 90 dB, a Gain Bandwidth Product (GBW) of 180 MHz and with high Slew Rate (90 V/μs) were used. The 1.5-bit quantizer is realized by two comparators and the V_t voltage is selected as the one that yields the best possible SNDR value, by the Genetic Algorithm Tool. The output of these comparators is then encoded to 1.5-bit representation using two FFDs.

A block diagram of this circuit is represented in Fig. 3.16.

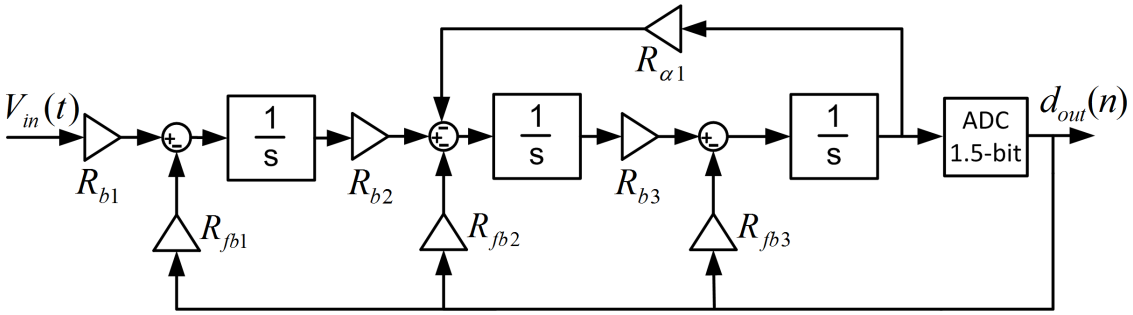


Figure 3.16: 3rd Order 1-bit CT-ΣΔM (CIFB).

For this topology, the Genetic Algorithm Tool provides the passive component values presented in Table 3.6.

Table 3.6: Component Values of the 3rd Order 1.5-bit ΣΔM using Active-RC Integrators.

Component	Value	Units
C	1	nF
R_{b1}	6.365	kΩ
R_{b2}	0.966	kΩ
R_{b3}	2.05	kΩ
R_{fb1}	15.91	kΩ
R_{fb2}	8.445	kΩ
R_{fb3}	8.950	kΩ
$R_{\alpha 1}$	56.231	kΩ

After the simulation is concluded, the output bitstream is converted to a txt file so that FFT analysis can be performed using a computational software like MATLAB®.

For a input sine wave with amplitude of 1 V_{rms} and 2 kHz frequency, the output spectrum shown in Fig. 3.17 was obtained. The noise floor is around -120 dB. Quantization noise is shaped and has a +60 dB increase per decade as expected, starting from 20 kHz. An SNDR of around 80 dB is obtained with a THD+N of around -86dB.

These results should be kept in mind, as they will be used to establish a comparison with the performance of a CT-ΣΔM when Differential Pairs are used to realize each integrator stage, as shown in the next section.

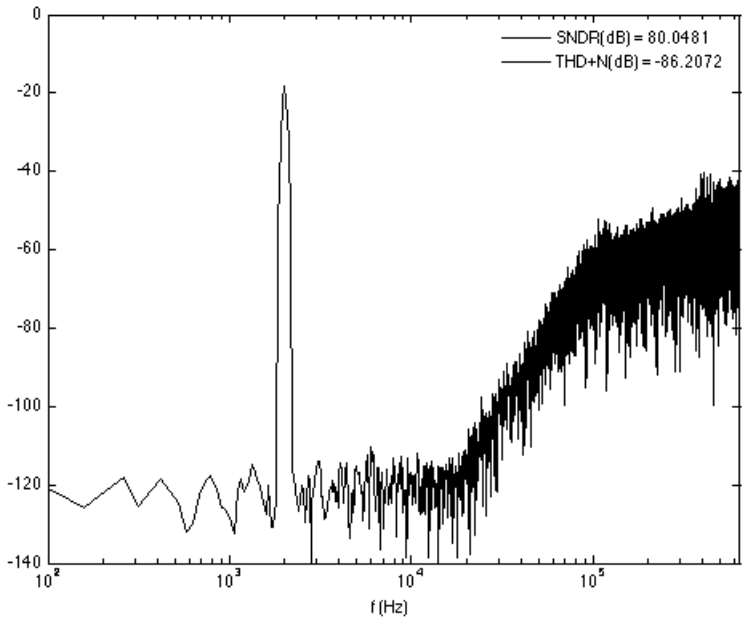


Figure 3.17: Output Spectrum of the 1.5-bit CRFB architecture obtained with electrical simulations when using Active-RC Integrators (2^{16} points FFT using a Blackman-Harris window).

3.5.2 3rd Order 1-bit CT-ΣΔM in a CIFB structure using Differential Pairs

The first architecture that is subject to analysis is the 3rd Order 1-bit ΣΔM in a CIFB structure. It has three integrator differential pair stages and the 1-bit quantizer is realized by a single comparator. The output of the comparator is then encoded to 1-bit representation using a single FFD. A block diagram of this circuit is represented in Fig. 3.18.

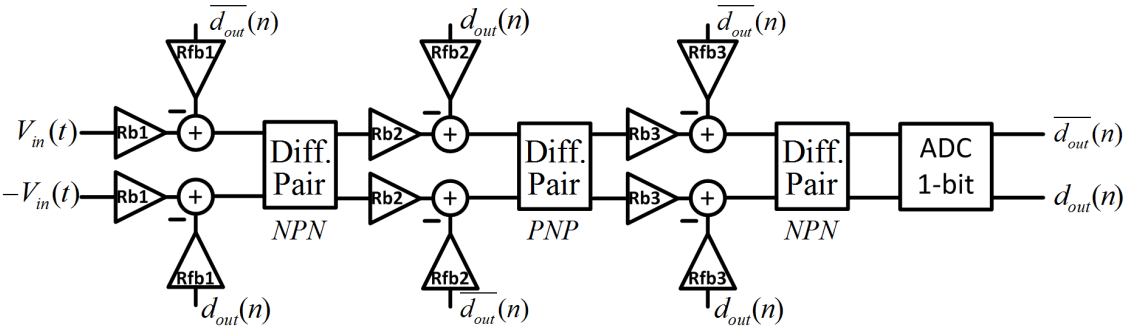


Figure 3.18: 3rd Order 1-bit CT-ΣΔM (CIFB).

As explained in section 3.1.2.4, the 3rd Order 1-bit ΣΔM was initially sized assuming values for certain components/factors and obtaining the values of the feedback resistors, for a NTF designed as a Butterworth high-pass filter with a cut-off frequency of 140 kHz, which is around a tenth of the sampling frequency. So, for a biasing current I_{EE} of 10 mA, a thermal voltage V_T of 25 mV and a current gain β of 400 for the transistors (both NPN and PNP), it follows that the input impedance of the transistor (r_π) should be around 2

kΩ. Furthermore, for the output common mode voltage of the NPN and PNP stages to be around 2.5 V (half of the positive supply voltage) and 0 V respectively, the collector resistors (R_C) should value 500 Ω and 1 kΩ accordingly. Finally, by picking the values of the input resistors (R_b) and setting the capacitor value to 0.47 nF[2], the value of the feedback resistors is obtained. The passive component values of the modulator are given in Table 3.7.

Table 3.7: Component Values of the 3rd Order 1-bit ΣΔM in a CIFB structure through Analytical Sizing.

Component	Value	Units
C	0.47	nF
R_{b1}	100	kΩ
$R_{b2} = R_{b3}$	2	kΩ
R_{fb1}	140.237	kΩ
R_{fb2}	29.255	kΩ
R_{fb3}	12.220	kΩ
R_{Cnpn}	500	Ω
R_{Cpnp}	1	kΩ

Note that the value of the input resistors of the first stage is much larger than the rest, due to the large voltage swing of the input signal.

After the simulation is concluded, the output bitstream is converted to a txt file so that FFT analysis can be performed using a computational software like MATLAB®.

For a input sine wave with amplitude of 1 V_{rms} and 2 kHz frequency, the output spectrum shown in Fig. 3.19 was obtained. The noise floor is around -100 dB. Quantization noise is shaped and has a +60 dB increase per decade as expected. An SNDR of around 61.45 dB is obtained with a THD+N of around -66dB. The measured SNDR as a function of the input level is shown in Fig. 3.20, following that the DR is of about 63 dB.

[2]This value presented itself as the most suitable for reducing the inherent noise of the circuit board.

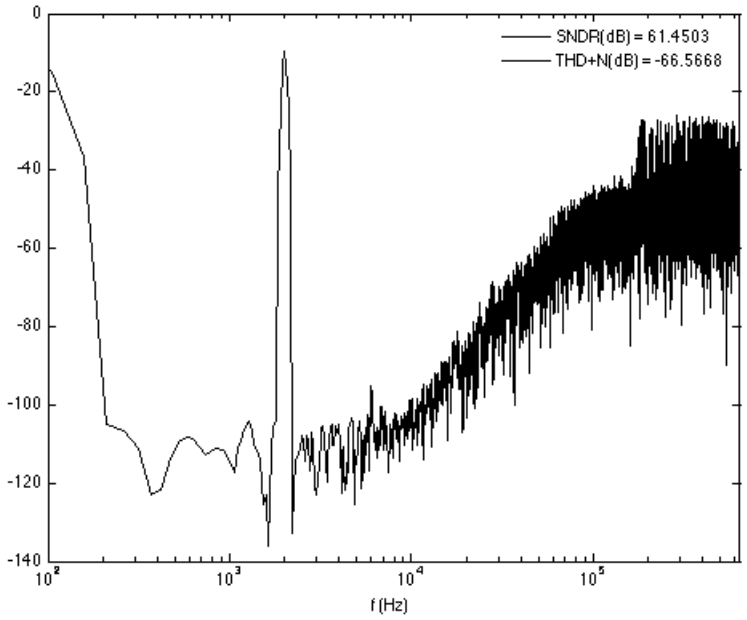


Figure 3.19: Output Spectrum of the 1-bit CIFB architecture obtained with electrical simulations (2^{16} points FFT using a Blackman-Harris window).

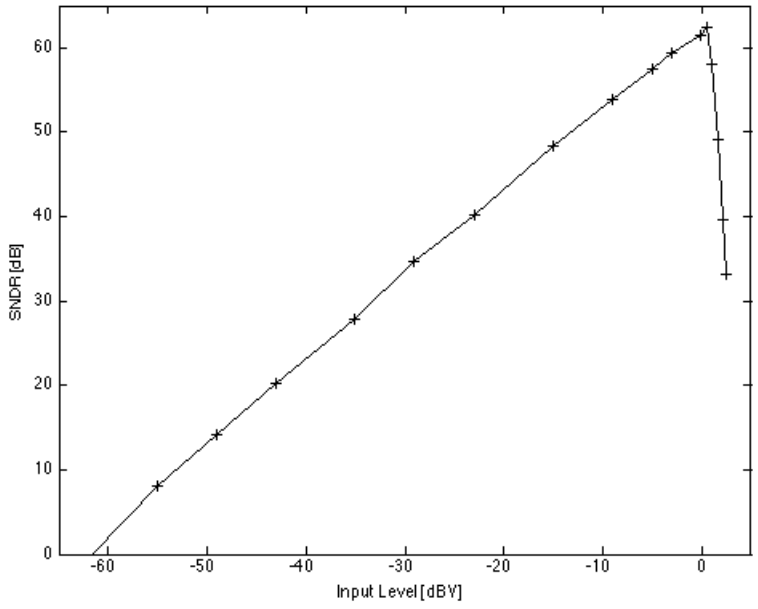


Figure 3.20: Measured SNDR as a function of Input Level of the 1-bit CIFB architecture.

3.5.3 3rd Order 1-bit CT-ΣΔM in a CRFB structure using Differential Pairs

As seen in section 2.6, local resonator stages allow for the distribution of the zeros of the NTF along the signal bandwidth. Therefore, the effectiveness of noise-shaping is extended beyond low frequencies. The following architecture is the 3rd Order 1-bit ΣΔM in a CRFB structure. It is composed of an initial integrator stage followed by a local resonator stage. A block diagram of this circuit is shown in Fig. 3.21. Notice the inclusion of another feedback loop that originates the local resonator stage.

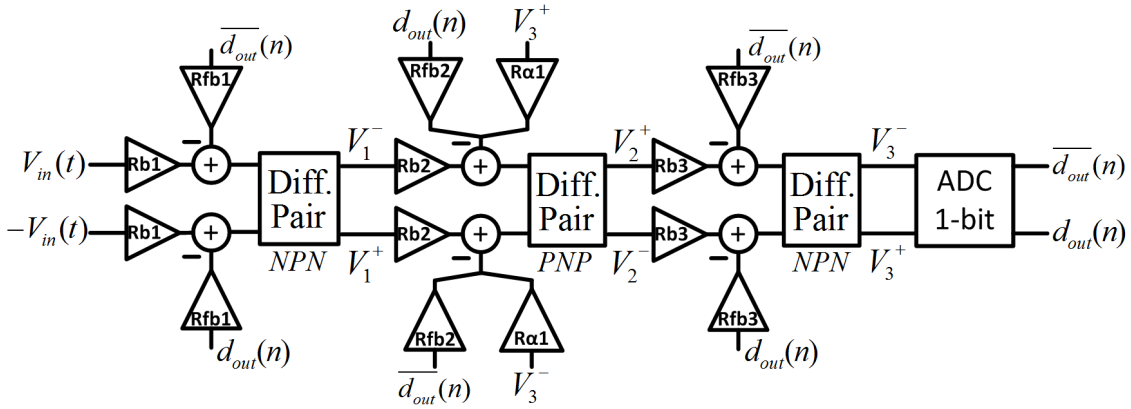


Figure 3.21: 3rd Order 1-bit CT-ΣΔM (CRFB).

To size the components of this architecture, the analytical sizing procedure was once again employed. However, although the TF of the proper Chebyshev type II filter can be determined by specifying a stopband edge frequency of 20 kHz and its coefficients retrieved, the computing software used to determine the values of the feedback resistors (Mathematica®) proved itself unable to determine the value of the local resonator feedback resistor (probably due to insufficient memory or another unknown reason). Therefore, the solution found was to use the same feedback resistors as in the CIFB structure and, by a backtracking process, determining the value of the local resonator feedback resistor that shifts the zeros from DC to the signal bandwidth and shapes the quantization noise so that it has a +60 dB increase per decade, starting from 20 kHz. This resistor value was found to be about 162 kΩ. All of the other components have the same value as in the CIFB structure (Table 3.7), as stated before.

For a input sine wave with amplitude of 1 V_{rms} and 2 kHz frequency, the output spectrum shown in Fig. 3.22 was obtained. Fig. 3.22 shows that the in-band noise floor of the 3rd Order 1-bit ΣΔM is around -100 dB. Quantization noise is shaped and has a +60 dB increase per decade starting from roughly 20 kHz, due to the zero spreading. An SNDR of around 64.5 dB is obtained with a THD+N of around -68 dB. Thus, the zero spreading is able of improving the overall performance of the ΣΔM by around +3 dB. The measured SNDR as a function of the input level is shown in Fig. 3.23, following that the DR is of about 65 dB.

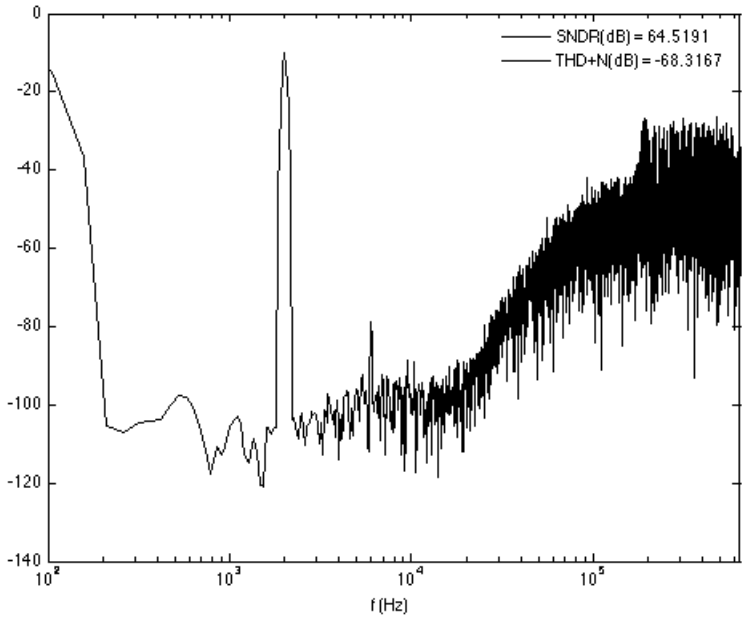


Figure 3.22: Output Spectrum of the 1-bit CRFB architecture obtained with electrical simulations (2^{16} points FFT using a Blackman-Harris window).

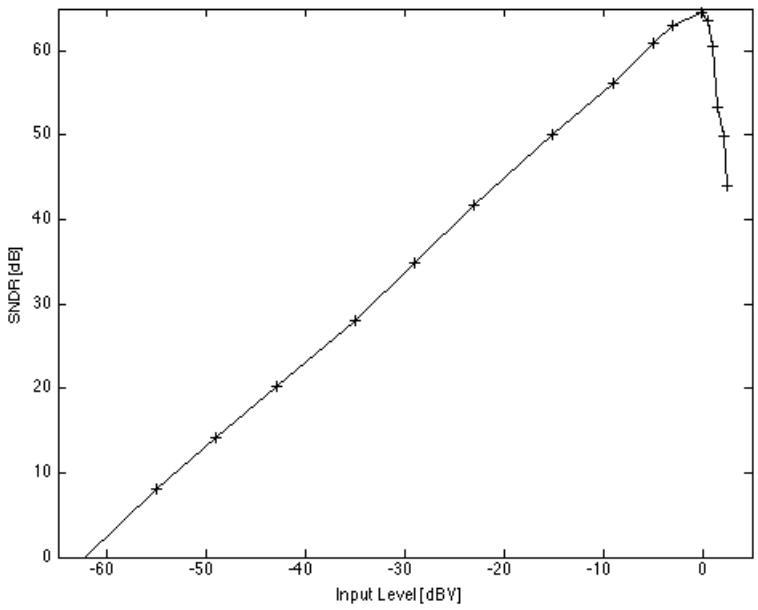


Figure 3.23: Measured SNDR as a function of Input Level of the 1-bit CRFB architecture.

3.5.4 3rd Order 1.5-bit CT-ΣΔM in a CIFB structure using Differential Pairs

As seen in section 2.6.6, another way of improving the SNDR of the ΣΔM is to use a 1.5-bit quantizer, thereby reducing the quantization error (thus improving the linearity of the feedback) in the modulator yielding a more stable loop. Thus, a larger cut-off frequency can be used. Furthermore, for near-zero input signals there is low switching activity. The 1.5-bit quantizer used is the one described in section 3.2. A block diagram of this circuit is shown in Fig. 3.24.

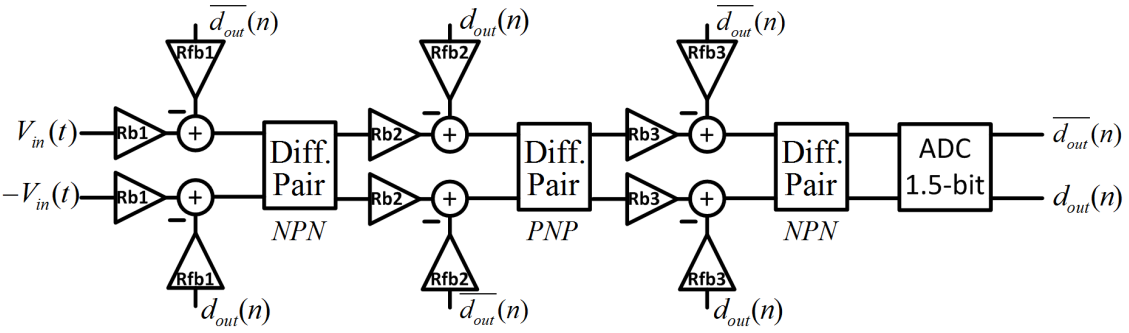


Figure 3.24: 3rd Order 1.5-bit CT-ΣΔM (CIFB).

For this topology, the Genetic Algorithm provides the passive component values presented in Table 3.8.

Table 3.8: Component Values of the 3rd Order 1.5-bit ΣΔM in a CIFB structure.

Component	Value	Units
C	0.47	nF
R_{b1}	69.565	kΩ
R_{b2}	2.131	kΩ
R_{b3}	2.100	kΩ
R_{fb1}	162.832	kΩ
R_{fb2}	104.904	kΩ
R_{fb3}	57.950	kΩ
R_{Cnpn}	500	Ω
R_{Cpnp}	1	kΩ
R_1	46.6	Ω
R_2	5k	kΩ

For a input sine wave with amplitude of 1 V_{rms} and 2 kHz frequency, the output spectrum shown in Fig. 3.25 was obtained. Fig. 3.25 shows that the in-band noise floor of the 3rd Order 1.5-bit ΣΔM is around -100 dB. Quantization noise is shaped and has a +60 dB increase per decade, although it begins still inside the audio band (roughly 20 kHz). An SNDR of around 75 dB is obtained with a THD+N of around -79 dB. The measured SNDR as a function of the input level is shown in Fig. 3.26, following that the DR is of about 72 dB.

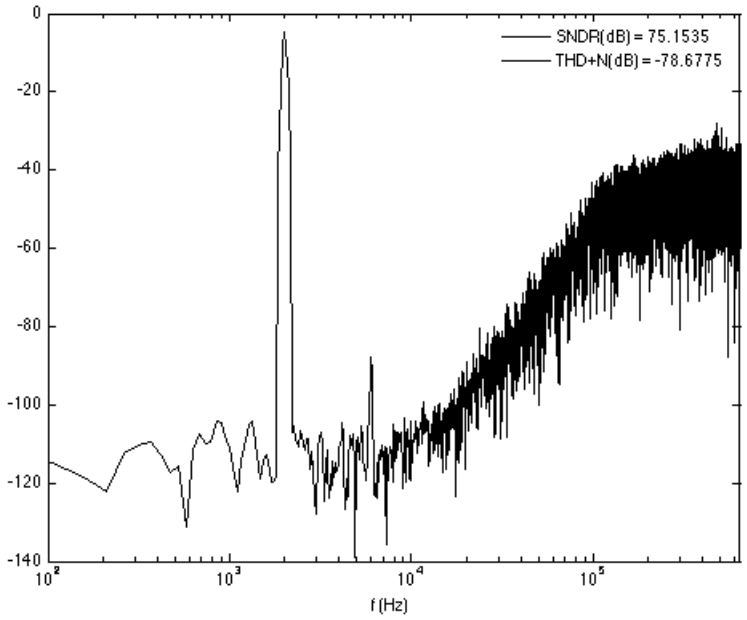


Figure 3.25: Output Spectrum of the 1.5-bit CIFB architecture obtained with electrical simulations (2^{16} points FFT using a Blackman-Harris window).

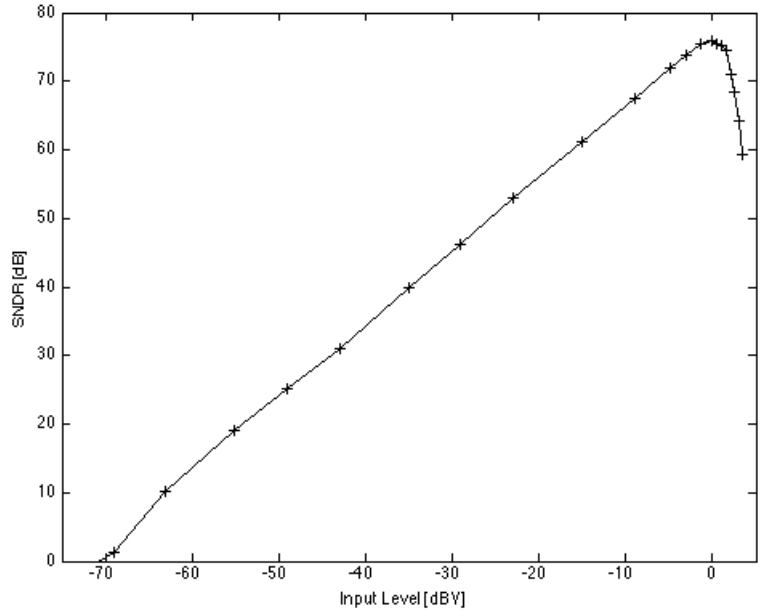


Figure 3.26: Measured SNDR as a function of Input Level of the 1.5-bit CIFB architecture.

3.5.5 3rd Order 1.5-bit CT-ΣΔM in a CRFB structure using Differential Pairs

Again, a local resonator stage is used (CRFB structure) in order to improve the overall performance of the ΣΔM. Together with 1.5-bit quantization, this is the architecture that yields the best overall results among those studied and implemented. A block diagram of this circuit is shown in Fig. 3.27.

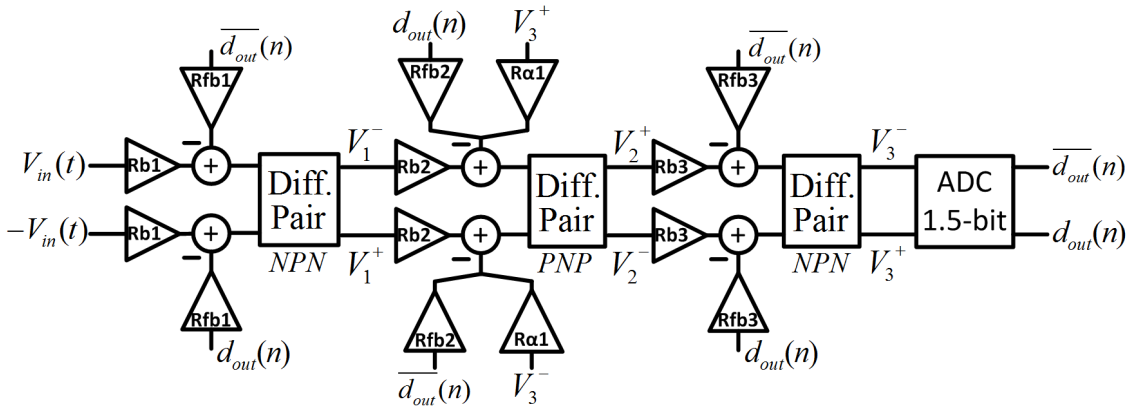


Figure 3.27: 3rd Order 1.5-bit CT-ΣΔM (CRFB).

In this architecture, the Genetic Algorithm provides the passive component values presented in Table 3.9.

Table 3.9: Component Values of the 3rd Order 1.5-bit ΣΔM in a CRFB structure.

Component	Value	Units
C	0.47	nF
R_{b1}	85.007	kΩ
R_{b2}	1.904	kΩ
R_{b3}	2.269	kΩ
R_{fb1}	164.320	kΩ
R_{fb2}	127.518	kΩ
R_{fb3}	68.910	kΩ
$R_{\alpha 1}$	216.613	kΩ
R_{Cnpn}	500	Ω
R_{Cpnp}	1	kΩ
R_1	38.1	Ω
R_2	5k	kΩ

With this sizing, for a input sine wave with amplitude of 1 V_{rms} and 2 kHz frequency, the output spectrum shown in Fig. 3.28 was obtained.

Fig. 3.28 shows that the in-band noise floor of the 3rd Order 1.5-bit ΣΔM is around -100 dB. Again, quantization noise is shaped and has a +60 dB increase per decade. When compared to Fig. 3.25, it follows that the distribution of the zeros along the signal bandwidth lead to an increase of the SNDR value of about +3 dB, to 78 dB, due to reduced

distortion (particularly HD3) and the noise being shaped further away from the audio band.

The measured SNDR as a function of the input level is shown in Fig. 3.29, following that the DR is of about 68 dB.

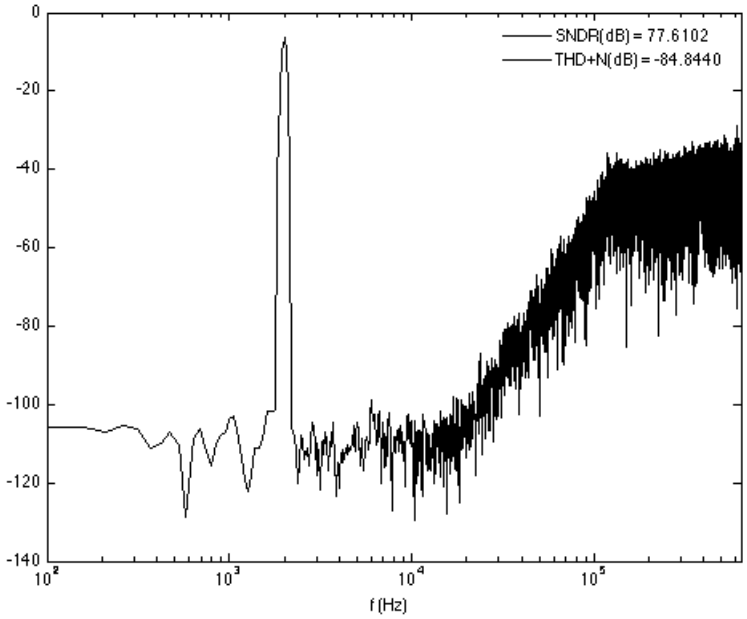


Figure 3.28: Output Spectrum of the 1.5-bit CRFB architecture obtained with electrical simulations (2^{16} points FFT using a Blackman-Harris window).

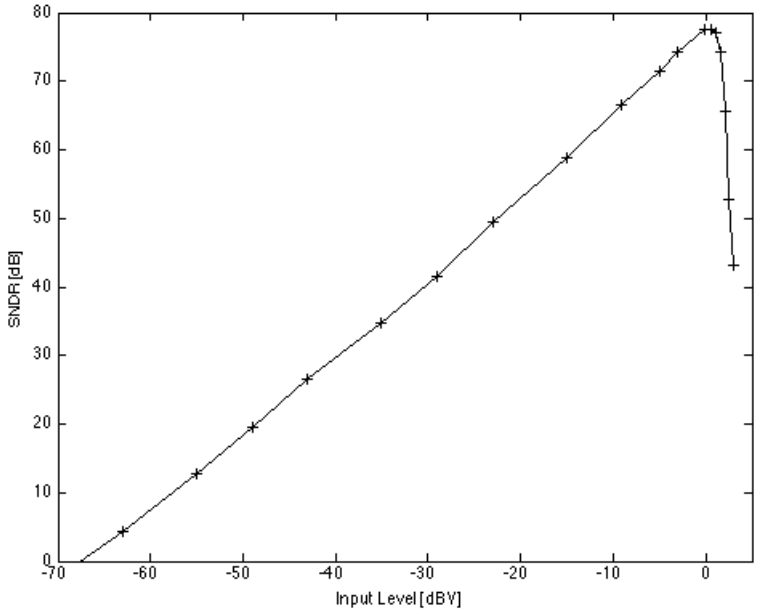


Figure 3.29: Measured SNDR as a function of Input Level of the 1.5-bit CRFB architecture.

By recalling the results obtained for a ΣΔM when Active-RC Integrators were used (Fig. 3.17), it follows that there was a decrease of no more than 3 dB. Thus, it is safe to assume that replacing high gain and bandwidth OpAmps by Differential Pairs, who behave like lossy integrators, can be done as long as their finite gain and bandwidth is accommodated during the filter design process.

4

Measured Prototypes and Experimental Results

This chapter presents the layout of the prototypes manufactured and the experimental results obtained. Two PCBs were designed, one for 1-bit quantization and another for 1.5-bit quantization. The layout was performed with the aid of the program EAGLE®. Both boards were designed in such a way that they could implement both the CIFB and the CRFB structure. To do so, a jumper was placed in between the local resonator feedback path.

4.1 3rd Order 1-bit CT-ΣΔM in a CIFB structure

The PCB layout of the 3rd Order 1-bit CT-ΣΔM is presented in Fig. 4.1. The 1206 package was used for both the resistors and capacitors. BC109 BJTs are used for the NPN differential pair(s) and current mirror(s), while BC179 are the BJTs chosen to implement the PNP differential pair(s) and current mirror(s). Both BJTs are manufactured in a TO-18 package. These were chosen due to their high current gain and low noise.

Each current mirror was implemented as a LED current source and has a variable resistor (potentiometer) that adjusts the current flowing through each Differential Pair stage. The comparator was implemented by LT1720 single-supply comparators with rail-to-rail outputs, while the FFD was implemented by a Quadruple FFD with clear (Ref: CD74AC175). The clock signal (f_s = 1.28 MHz) was applied to a SMA connector. Decoupling capacitors of 100 nF were used.

At first, the component values listed in Table 3.7 that were given by the Analytical Sizing procedure were used. Their nominal values are presented in Table 4.1.

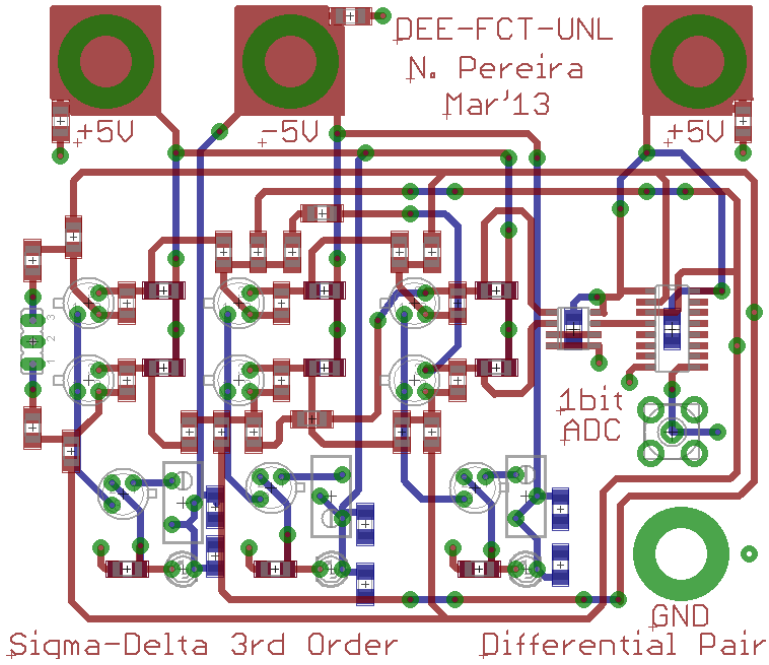


Figure 4.1: PCB layout of the 3rd Order 1-bit CT-ΣΔM.

Table 4.1: Component Values of the 3rd Order 1-bit ΣΔM in a CIFB structure through Analytical Sizing.

Component	Theoretical Value	Nominal Value	Units	Error (%)
C	0.47	0.47	nF	0
R_{b1}	100	99.8	kΩ	0.2
$R_{b2} = R_{b3}$	2	1.99	kΩ	0.5
R_{fb1}	140	137	kΩ	2.14
R_{fb2}	29.255	29.4	kΩ	0.15
R_{fb3}	12.220	12.4	kΩ	1.47
R_{Cnpn}	500	499	Ω	0.2
R_{Cpnp}	1	0.998	kΩ	0.2

The 3rd Order 1-bit CT-ΣΔM PCB after manufacturing and soldering the components is shown in Fig. 4.2.

After properly connecting the supply voltages and the clock signal onto the PCB and shunting both inputs, the DC operating point of the circuit was adjusted, by regulating the value of the potentiometers of each current mirror (Fig. 4.3). Afterwards, an input sine wave of 1 V_{rms} amplitude and 1 kHz frequency was applied to the circuit. The experimental setup is shown in Fig. 4.4. The test equipment used is described as follows: the input signals were produced with a Audio Precision ATS-2 audio analyser and the output signals were read with a probe and a Tektronix TDS3052 oscilloscope. The clock signal was produced by a Wavetek CG635 signal generator and the supply voltages were produced by a Tektronix PS2521G power supply.

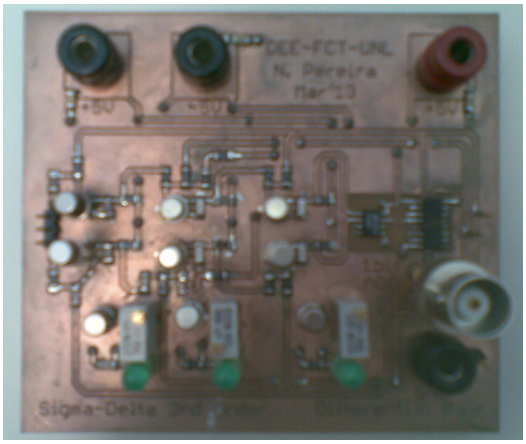


Figure 4.2: Manufactured 3rd Order 1-bit CT-ΣΔM PCB.

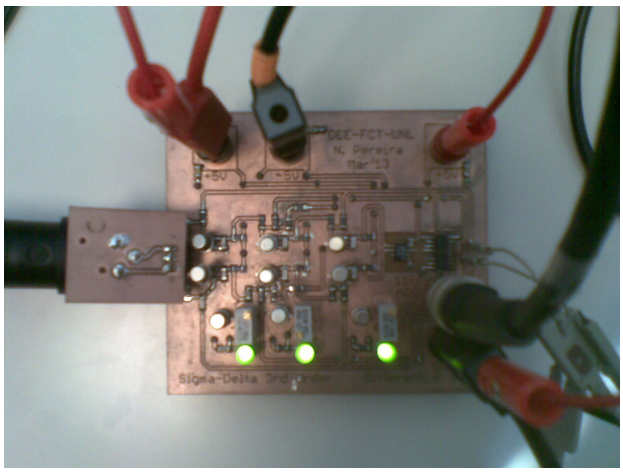


Figure 4.3: Connecting the input signal to the 3rd Order 1-bit CT-ΣΔM PCB.

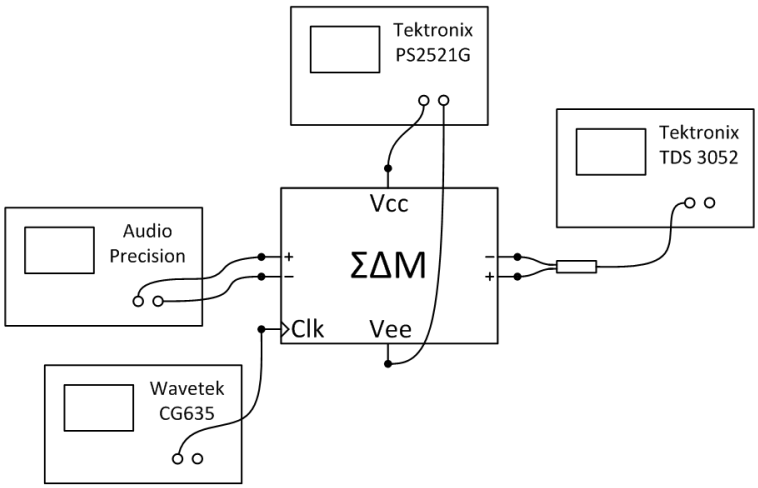


Figure 4.4: Experimental Setup for the 3rd Order 1-bit CT-ΣΔM PCB.

The bitstream signal was retrieved and converted to a txt file so that an FFT analysis could be performed, using a computational software like MATLAB®, in order to obtain the SNDR and THD+N value. The output spectrum is shown in Fig. 4.5. A series of

tests was also performed in order to trace the SNDR vs Input Signal curve. To do so, sine waves with different amplitudes were applied to the circuit. For instance, Fig. 4.6 shows the output spectrum when an input sine wave with 0.5 V_{rms} amplitude is applied. The SNDR vs Input Signal curve is shown in Fig. 4.7.

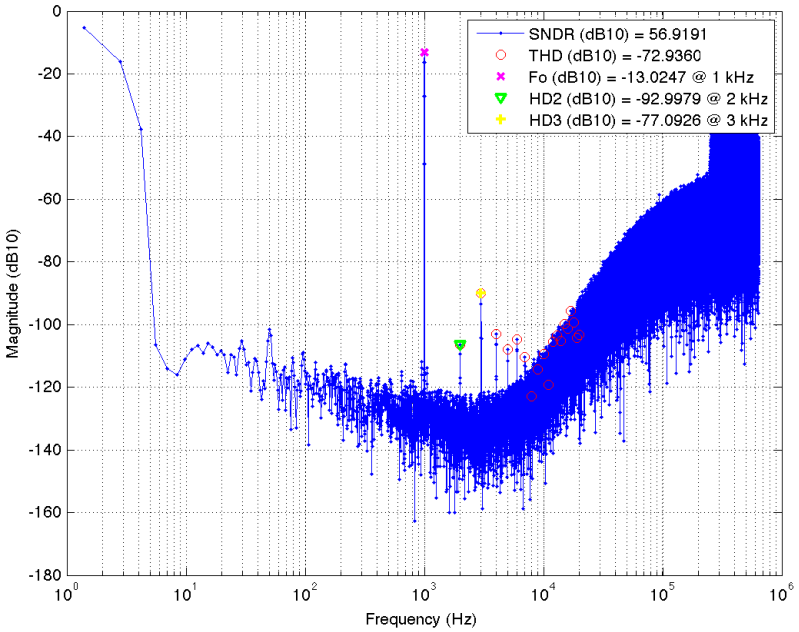


Figure 4.5: Output Spectrum of the 1-bit CIFB architecture obtained through experimental measurements for an input sine wave with 1 V_{rms} amplitude (2^{16} points FFT using a Blackman-Harris window).

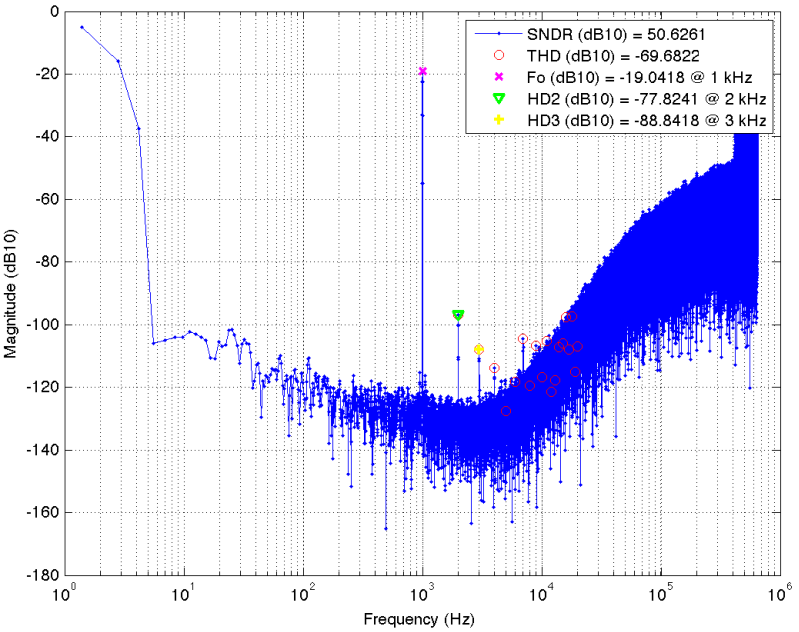


Figure 4.6: Output Spectrum of the 1-bit CIFB architecture obtained through experimental measurements for an input sine wave with 0.5 V_{rms} amplitude (2^{16} points FFT using a Blackman-Harris window).

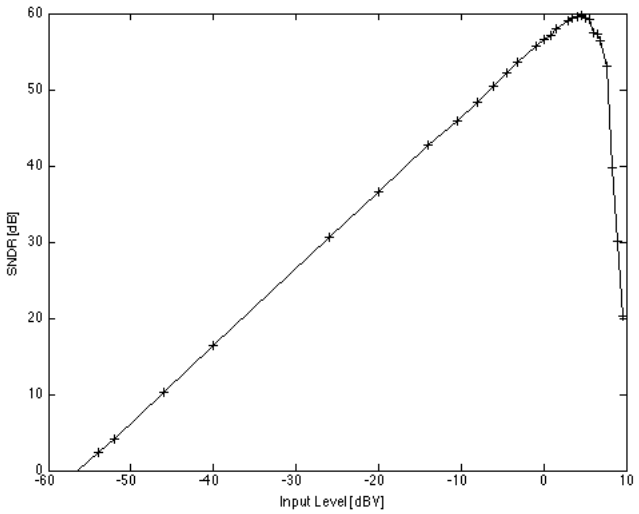


Figure 4.7: Measured SNDR as a function of Input Level for the 3rd Order 1-bit CT-ΣΔM in a CIFB structure.

Fig. 4.5 shows that the in-band noise floor of the 3rd Order 1-bit ΣΔM is around -110 dB. Quantization noise is shaped as expected and has a +60 dB increase per decade. The resulting SNDR is of around 57 dB, which is slightly lower than the simulation results obtained for the same circuit (about -4 dB), as seen in Fig. 3.19. This may be due to the inherent noise of the PCB and component mismatches. From Fig. 4.7, it follows that this ΣΔM has a DR of around 60 dB.

4.2 3rd Order 1-bit CT-ΣΔM in a CRFB structure

The next step was to solder a pair of resistors in the local resonator feedback path in order to shift the zeros placement. The same transistors, comparator and FFD were used. The component values of this architecture are listed in Table 4.2.

Table 4.2: Component Values of the 3rd Order 1-bit ΣΔM in a CRFB structure through Analytical Sizing.

Component	Theoretical Value	Nominal Value	Units	Error (%)
C	0.47	0.47	nF	0
R_{b1}	100	99.8	kΩ	0.2
$R_{b2} = R_{b3}$	2	1.99	kΩ	0.5
R_{fb1}	140	137	kΩ	2.14
R_{fb2}	29.255	29.4	kΩ	0.15
R_{fb3}	12.220	12.4	kΩ	1.47
$R_{\alpha 1}$	162	161.2	kΩ	0.49
R_{Cnpn}	500	499	Ω	0.2
R_{Cpnp}	1	0.998	kΩ	0.2

After redoing the procedures stated before (shunting both inputs, adjusting the DC operating point, etc), an input sine wave of 1 V_{rms} amplitude and 1 kHz frequency was applied. Again, the bitstream signal was retrieved and used to obtain the SNDR and THD+N value. The output spectrum is shown in Fig. 4.8. Another series of tests was performed in order to trace the SNDR vs Input Signal curve shown in Fig. 4.10. For a sine wave with 0.5 V_{rms} amplitude, the obtained output spectrum is shown in Fig. 4.9.

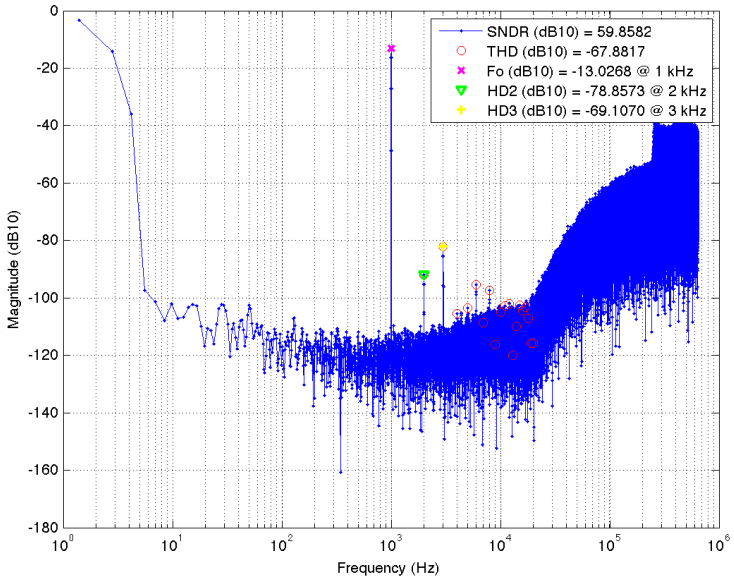


Figure 4.8: Output Spectrum of the 1-bit CRFB architecture obtained through experimental measurements for an input sine wave with 1 V_{rms} amplitude (2^{16} points FFT using a Blackman-Harris window).

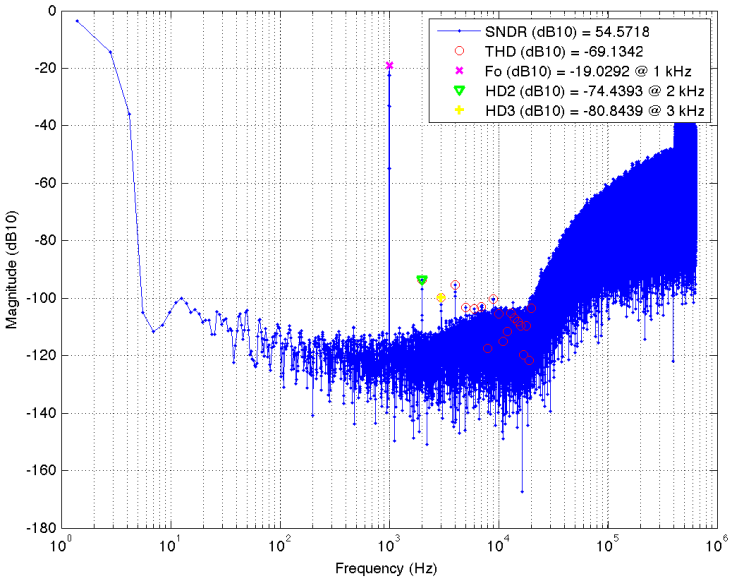


Figure 4.9: Output Spectrum of the 1-bit CRFB architecture obtained through experimental measurements for an input sine wave with 0.5 V_{rms} amplitude (2^{16} points FFT using a Blackman-Harris window).

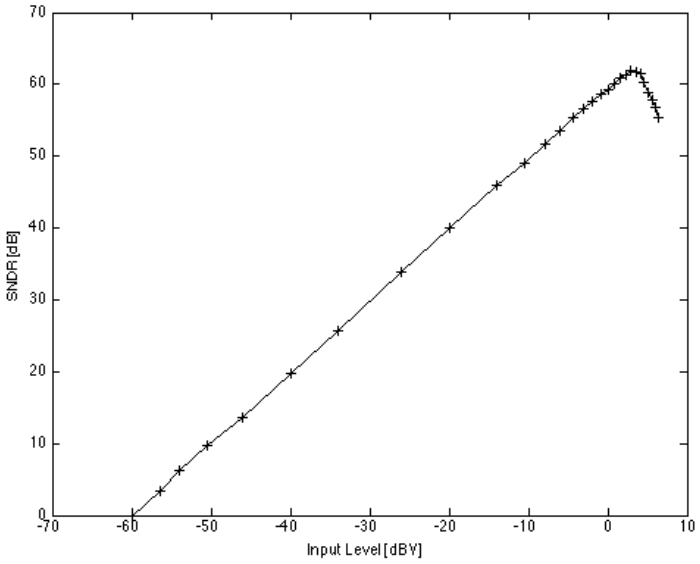


Figure 4.10: Measured SNDR as a function of Input Level for the 3rd Order 1-bit CT-ΣΔM in a CRFB structure.

Fig. 4.8 shows that the in-band noise floor of the 3rd Order 1-bit ΣΔM in a CRFB structure is around -100 dB. Quantization noise is shaped as expected and has a +60 dB increase per decade, starting from ± 20 kHz. This shows that the local resonator feedback is capable of shifting the zeros from DC to the signal bandwidth. Therefore the resulting SNDR is of around 60 dB, which is a slight improvement (about +3 dB) over the performance obtained for the CIFB architecture, as seen in Fig. 4.5. Also, from Fig. 4.10, it follows that this ΣΔM has a DR of around 62 dB.

4.3 3rd Order 1.5-bit CT-ΣΔM in a CRFB structure

The PCB layout of the 3rd Order 1.5-bit CT-ΣΔM is presented in Fig. 4.11. Again, the 1206 package was used for both the resistors and capacitors. The component values of this architecture are listed in Table 4.3.

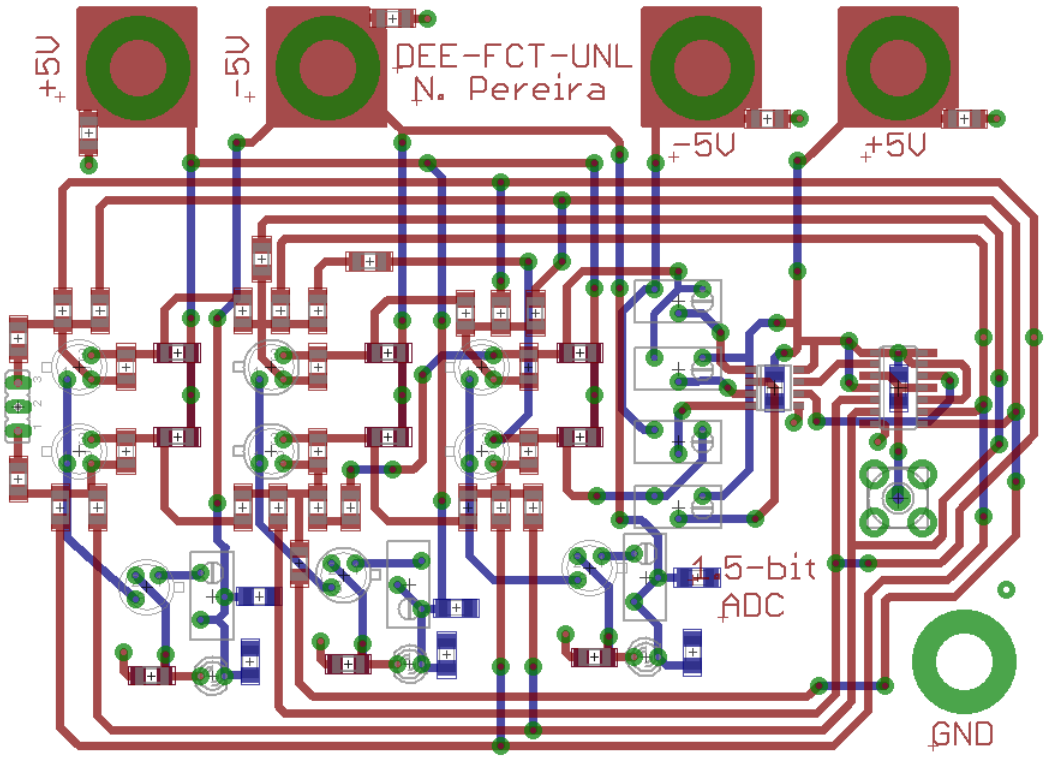


Figure 4.11: PCB layout of the 3rd Order 1.5-bit CT-ΣΔM.

Table 4.3: Component Values of the 3rd Order 1.5-bit ΣΔM in a CRFB structure sized through a Genetic Algorithm.

Component	Theoretical Value	Nominal Value	Units	Error (%)
C	0.47	0.47	nF	0
R_{b1}	85.007	84.8	kΩ	0.24
R_{b2}	1.904	1.910	kΩ	0.32
R_{b3}	2.269	2.262	kΩ	0.31
R_{fb1}	164.320	164.8	kΩ	0.29
R_{fb2}	127.518	127.7	kΩ	0.14
R_{fb3}	68.910	69.4	kΩ	0.71
$R_{\alpha 1}$	216.613	215.4	kΩ	0.56
R_{Cnpn}	500	499	Ω	0.2
R_{Cpnp}	1	0.998	kΩ	0.2
R_1	38.1	38.3	Ω	0.52
R_2	5	4.98	kΩ	0.4

The 3rd Order 1.5-bit CT-ΣΔM PCB after manufacturing and soldering the components is shown in Fig. 4.12.

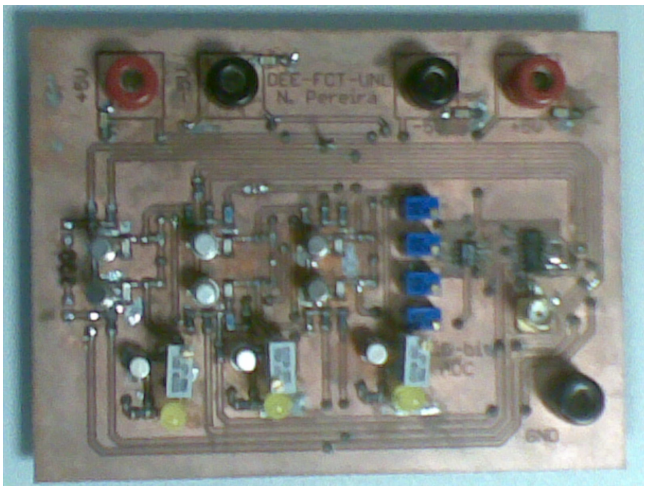


Figure 4.12: Manufactured 3rd Order 1.5-bit CT-ΣΔM PCB.

After performing the same preliminary steps as with the 1-bit CT-ΣΔM PCB, an input sine wave of 1 V_{rms} amplitude and 1 kHz frequency was applied to the circuit. The bitstream signal was retrieved and used to obtain the SNDR and THD+N value. The output spectrum is shown in Fig. 4.13. A series of tests was also performed in order to trace the SNDR vs Input Signal curve shown in Fig. 4.15. For a sine wave with 0.5 V_{rms} amplitude, the obtained output spectrum is shown in Fig. 4.14.

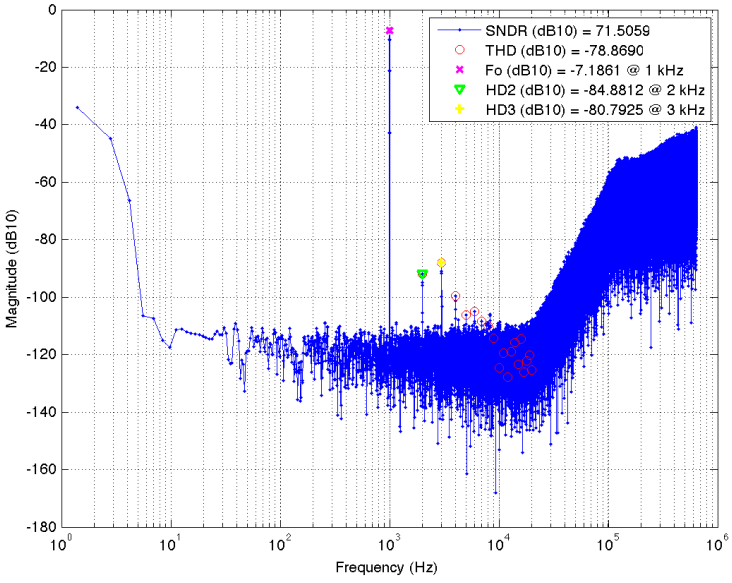


Figure 4.13: Output Spectrum of the 1.5-bit CRFB architecture obtained through experimental measurements for an input sine wave with 1 V_{rms} amplitude (2^{16} points FFT using a Blackman-Harris window).

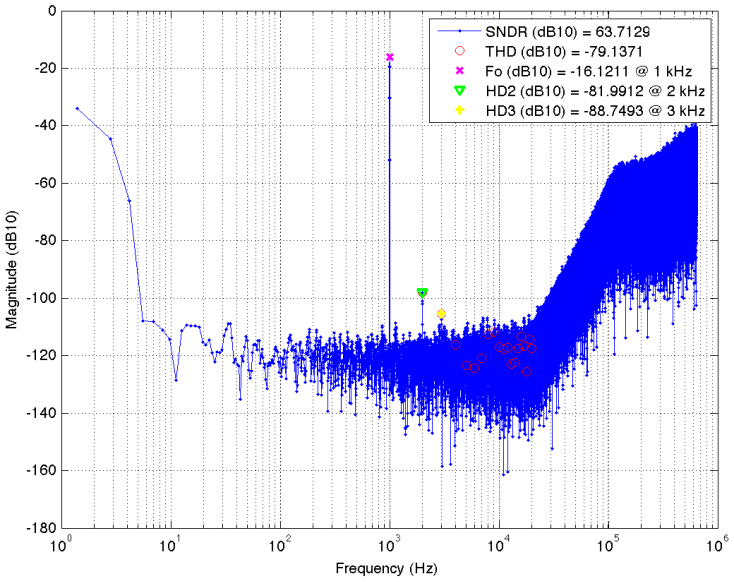


Figure 4.14: Output Spectrum of the 1.5-bit CRFB architecture obtained through experimental measurements for an input sine wave with 0.5 V_{rms} amplitude (2^{16} points FFT using a Blackman-Harris window).

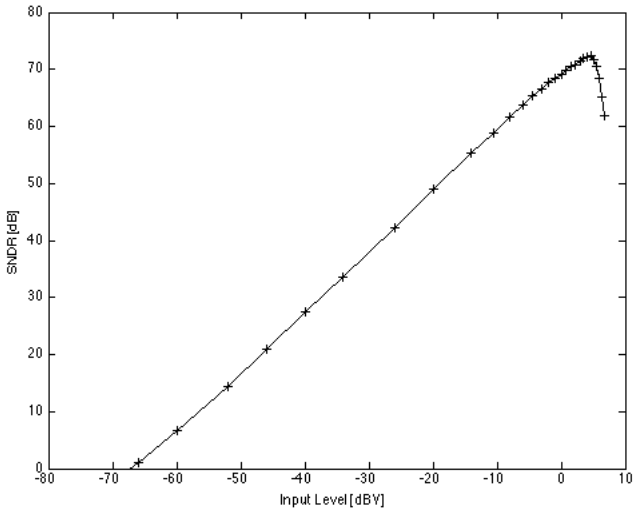


Figure 4.15: Measured SNDR as a function of Input Level for the 3rd Order 1.5-bit CT-ΣΔM in a CRFB structure.

Fig. 4.13 shows that the in-band noise floor of the 3rd Order 1.5-bit ΣΔM in a CRFB structure is around -100 dB. Quantization noise is shaped and has a +60 dB increase per decade, starting from ± 20 kHz. The resulting SNDR is of around 72 dB, which is slightly lower than the simulation results obtained for the same circuit (about -6 dB), as seen in Fig. 3.28. As before, this may be due to the inherent noise of the PCB and component mismatches. Also, the 2nd harmonic is clearly visible, which may indicate that the differential pairs are not perfectly balanced. Fig. 4.15 shows that this ΣΔM has a DR of about 73 dB.

4.4 Comparison between Theoretical and Experimental Results

Table 4.4 presents a comparison between the Theoretical Results obtained through electrical simulations and the Experimental Results provided by both PCBs, for the different ΣΔMs considered.

Table 4.4: Theoretical vs Experimental Results.

Architecture	Theoretical Result	Experimental Result
3rd Order 1-bit ΣΔM (CIFB)	SNDR = 61.45 dB THD+N = -66.57 dB	SNDR = 56.92 dB THD+N = -72.94 dB
3rd Order 1-bit ΣΔM (CRFB)	SNDR = 64.52 dB THD+N = -68.32 dB	SNDR = 59.86 dB THD+N = -67.88 dB
3rd Order 1.5-bit ΣΔM (CRFB)	SNDR = 77.61 dB THD+N = -84.84 dB	SNDR = 71.51 dB THD+N = -78.87 dB

As Table 4.4 shows, the experimental results are fairly close to the theoretical performance. The differences may be explained by the inherent noise of the PCBs, manufactured single-handedly by a machine owned by the Electrical Engineering Department, and component mismatches.

It should be stated that the PCBs were subjected to a series of tests and soldering of components, particularly different BJT's, that may have inadvertently degraded its quality.

Nevertheless, the results validate the theoretical work performed and show that Integrator Differential Pairs, with their low gain and bandwidth, are capable of properly replacing OpAmps with high gain and bandwidth, without degrading the performance of the ΣΔMs in a considerable fashion.

5

Conclusions and Future Work

5.1 Conclusions

The objective of the work presented in this thesis was to design and implement a $\Sigma\Delta$M for a Class D audio amplifier in a fully-differential topology where the loop filter's integrator stages were based on BJT Differential Pairs. In order to do so, several steps were taken which are summarized next.

In the second chapter, after presenting the fundamental concepts behind Class D audio amplifiers and Data conversion, where the advantages of $\Sigma\Delta$Ms were described, analysis on several $\Sigma\Delta$M architectures was made. The advantages/disadvantages of Feedforward and Feedback techniques were described. It was shown that although both provide the same NTF, the Feedback structure provided much stronger filtering and nearly no peaking at high frequencies. Also, the introduction of local resonator stages led to the distribution of the NTF zeros along the signal bandwidth which resulted in a greater attenuation over the frequency band of interest.

Furthermore, the use of 1.5-bit quantization over traditional 1-bit architectures showed that it was possible to improve the SNDR of the circuit by around 7.6 dB. Concerning the output stage, the addition of a third quantization level significantly reduces switching activity and a greater power efficiency can be achieved since in this third state zero power is transferred to the load.

In the third chapter the design of the $\Sigma\Delta$M is presented. Two possible solutions for the implementation of the integrator stages are shown, Active-RC Integrators and Integrator Differential Pairs. The former is one of the most common solutions for the integrator stages of the $\Sigma\Delta$M, mainly due to its linearity and power consumption. The latter composes the main contribution behind this work, where BJT Differential Pairs replace

the commonly used Active-RC Integrators in a CT design. Their main advantages are the inherent fully differential topology, a high CMRR and having a similar performance as the Active-RC Integrators despite their lower gain and bandwidth. Two different ways of sizing the loop filter are proposed, one where the design equations are used and certain assumptions of component values are made (Analytical Sizing) and another where a Genetic Algorithm Tool is used to find the component values while taking into consideration factors like RC mismatches and maximum voltage swing.

Also, a 1.5-bit ADC that relies only on two comparators is designed, capable of generating three different voltage levels and effectively rejecting the input common-mode voltage. These voltage levels are encoded to 1.5-bit representation using only two FFD. However, an alternative encoding logic is proposed capable of alternating the output stage's switches state whenever the bitstream is the same for long periods of time. Also, for 1-bit quantization the feedback circuitry consists only in single feedback resistors, while if 1.5-bit quantization is performed two resistors in parallel are used. This is necessary to ensure that in the zero-state no current is flowing in the feedback path.

Simulation results are shown at the end of the third chapter, for several $\Sigma\Delta$Ms. A 3^{rd} order $\Sigma\Delta$M with an OSR of 32 was considered. Since this $\Sigma\Delta$M is to be used as an audio amplifier, the signal bandwidth considered was of 20 kHz. As a result, a sampling frequency of 1.28 MHz was used. This relatively low sampling frequency value also helps in reducing the EMI of the amplifier and avoid non-ideal effects in the output power devices.

For a 1-bit CIFB structure, an SNDR value of 61.45 dB was obtained, together with a THD+N of -66.5 dB. This $\Sigma\Delta$M has a DR of about 63 dB. With local resonator stages (CRFB structure), the SNDR value was of 64.5 dB, a +3 dB increase when considering the CIFB structure. The DR was of about 65 dB. These performances could hopefully be improved if the Genetic Algorithm Tool was used to size the components, instead of the analytical sizing. This was done when sizing the 1.5-bit quantization structure (for both the CIFB and CRFB architectures). As expected, the results were improved. For the CIFB structure, simulations of the modulator show that it has a SNDR value of 75.2 dB and a DR of about 72 dB, with a THD+N of -78.7 dB. Finally, for a 1.5-bit CRFB structure, a SNDR value of 77.6 dB, DR of about 68 dB and a THD+N of -84.8 dB were obtained. This shows that both the increase of the resolution of the quantizer and the spreading of the zeros along the signal bandwidth improve the overall performance of the $\Sigma\Delta$M.

These results also show that a $\Sigma\Delta$M with integrator stages implemented by Integrator Differential Pairs is capable of reaching a performance fairly similar to that of $\Sigma\Delta$M with integrator stages implemented by Active-RC Integrators, with high gain and bandwidth. This is possible as long as the finite gain and bandwidth of the Differential Pairs is accommodated during the filter design process.

Finally, in chapter 4 the experimental results are presented. Three architectures were implemented: 3^{rd} Order 1-bit CT-$\Sigma\Delta$M in a CIFB structure and in a CRFB structure and 3^{rd} Order 1.5-bit CT-$\Sigma\Delta$M in a CRFB structure. The component values of the former two

were found through Analytical Sizing while the latter was sized through a Genetic Algorithm Tool. The experimental results obtained for these architectures were fairly close to those obtained through simulations, therefore validating the work done theoretically. The 3rd Order 1-bit CT-ΣΔM in a CIFB structure yielded an SNDR of around 57 dB while for the CRFB structure, the obtained SNDR was of about 60 dB (+3 dB increase due to the implementation of the local resonator stage). Both are about -4 dB below the theoretical results. Regarding the 3rd Order 1.5-bit CT-ΣΔM in a CRFB structure, the SNDR obtained was of around 72 dB (around -6 dB below the theoretical results). These slight disparities may be due to the inherent noise of the PCBs (which weren't manufactured by a specialized factory but instead by a PCB machine owned by the Electrical Engineering Department) and component mismatches.

5.2 Future Work

Following the work done in this thesis, space for further improvement was found. Some of these possible improvements are describe below.

5.2.1 Implementation of the remaining architectures

Since the experimental results obtained validated what was done theoretically, it is expected that other architectures like the 3rd Order 1-bit CT-ΣΔM sized by the Genetic Algorithm Tool (the results of which were not presented) or the 3rd Order 1.5-bit CT-ΣΔM in a CIFB structure present experimental results close to those simulated.

5.2.2 Optimizing the Sizing Procedure in order to minimize power consumption

The current consumption of each integrator stage is of around 10 mA. One major improvement that could be performed is to use the Genetic Algorithm Tool to size a ΣΔM taking into consideration low power consumption, regardless of the order or quantization scheme. However, a major performance drop should be prevented.

5.2.3 Designing a ΣΔM together with a Class D Audio Amplifier

The ΣΔMs designed in this work are expected to work together with a Class D output stage in a bridged configuration. Therefore, it is necessary to design and implement an output stage, connect it to the ΣΔM and see if the results are the ones expected or if further improvements are necessary.

Analytical Sizing of the CT-ΣΔM implemented with Differential Pairs

This appendix explains the procedure taken to determine the feedback resistor values of a CT-ΣΔM implemented with Differential Pairs through an Analytical Sizing. The software used to do such were Mathematica® and MATLAB®, and the commands presented follow each programs syntax.

A.1 Design of a CIFB structure

The first step taken is the determination of the loop filter's generic NTF. This can be obtained through several ways, although the easiest might be the use of a software tool, such as MATLAB®. The feedback resistor values are obtained based on the coefficients that are present in the NTF.

In a CIFB structure the NTF is typically designed to be a Butterworth High-Pass filter. To design it, the order N must be specified as well as the desired cut-off frequency w_p in rad/s. Since the NTF presents a high-pass response and will be implemented in continuous, the terms 'high' and 's' must be used, respectively.

The correspondent MATLAB® command is shown in Table A.1, where A and B represent the denominator and numerator coefficient values, respectively.

Table A.1: Obtaining the CT Butterworth High-Pass filter Transfer Function through Matlab.

[B,A] = butter(N,w_p,'high','s')
NTF = tf(B,A)

The next step is to obtain the TF of the ΣΔM implemented with Differential Pairs. This TF can be split into two, in order to obtain both the STF and the NTF. The latter's coefficients (which in reality are expressions that combine all of the components used in the circuit) are then equalled to the coefficients that MATLAB® provided. The final step is to assign values to most of the components in the circuit, except the feedback resistors.

For a common mode output voltage of V_{npn} V and V_{pnp} V for the NPN and PNP stages respectively and for a certain I_C collector current, it follows that the R_c resistors should be sized according to Eq. A.1.

$$R_{Cnpn} = \frac{V_{cc} - V_{npn}}{I_C} \qquad R_{Cpnp} = \frac{V_{pnp} - V_{ee}}{I_C} \tag{A.1}$$

, where V_{cc} and V_{ee} are the positive and negative power supply, respectively. Since the Differential Pair is composed of two coupled common-emitter stages, the voltage gain is known and depends on the BJT transconductance and the R_c resistor[1] given by Eq. A.2.

$$|A_v| = g_m R_c \tag{A.2}$$

, where $g_m = \frac{I_C}{V_T}$. V_T represents the thermal voltage (and at room temperature is estimated to be about 25 mV). This voltage gain should not be too small, otherwise the noise shaping at low frequencies will be reduced and the overall performance of the modulator may be affected significantly [18].

The input impedance of the transistor (r_π resistor) can also be estimated through Eq. A.3.

$$r_\pi = \frac{\beta V_T}{I_C} \tag{A.3}$$

, where β represents the current gain at low frequencies. Although there is no sure-fire

[1] This is valid only if a emitter degeneration resistor is not present.

way of determining its value, it can be estimated and the average value can be found on a datasheet.

The base resistors (R_b) have no direct method for its sizing. However, to prevent BJT operation outside of the linear region (due to a small dynamic range) the R_b resistors of the first stage should be considerably high when compared to the base resistors of the following stages. Finally, the integrating capacitors value are assigned.

With all of these components sized, a computing software (it can be either Mathematica® or MATLAB®) can solve the equations in order to determine the optimal values for the feedback resistors.

A.2 Design of a CRFB structure

If a CRFB structure is used, an Inverse Chebyshev type II filter is desired. The procedure is slightly the same as in the Butterworth filter design, where the order N of the filter must be specified but in this case the stopband edge frequency w_s (in rad/s) must be defined. Also, the stopband ripple should be R dB down from the peak passband value. Other than that, the terms 'high' and 's' are used again.

The correspondent MATLAB® command is shown in Table A.2.

Table A.2: Obtaining the CT Inverse Chebyshev High-Pass filter Transfer Function through Matlab.

[B,A]=cheby2(N,R,w_s,'high','s')
NTF = tf(B,A)

The main difference here is that a fourth equation is drawn, one that takes into account the numerator of the NTF. Without it, the spreading of the zeros along the signal bandwidth would not occur. The remaining procedure is the same and the value of the resistor that is placed between two consecutive integrator stages is obtained.

A.3 Design Example: 2nd Order 1-bit CT-ΣΔM

Take as an example the design of a 2nd Order 1-bit CT-ΣΔM with coincident zeros, which has a maximum SNDR value of around 55 dB [4], [11], when an OSR of 32 and a

f_s of 1.28 MHz is used.

The first step is to determine the loop filter's NTF. Thus, the filter's order N is 2, and a cut-off frequency of 100 kHz (around a tenth of f_s) is selected. The correspondent MATLAB® command is shown in Table A.3. Notice the '2*pi' factor, that converts the cut-off frequency from Hz to rad/s.

Table A.3: Obtaining the CT Butterworth High-Pass filter Transfer Function through Matlab.

```
[B,A] = butter(2,2*pi*100e3,'high','s')
NTF = tf(B,A)
```

The resulting NTF is presented in Eq. A.4.

$$NTF(s) = \frac{s^2}{s^2 + 8.886e05s + 3.948e11} \tag{A.4}$$

In order to obtain the values of the feedback resistors (R_{fb}), the value of the input resistors (R_b) is assumed. Also, considering that the output common-mode voltage should be around 2.5 V for the NPN integrator stage and 0 V for the PNP integrator stage, the R_C values are 500 Ω and 1 kΩ respectively. The passive component values of the modulator are given in Table A.4.

Table A.4: Component Values of the 2nd Order 1-bit ΣΔM in a CIFB structure through Analytical Sizing.

Component	Value	Units
C	0.47	nF
R_{b1}	80	kΩ
R_{b2}	2	kΩ
R_{fb1}	115.130	kΩ
R_{fb2}	24.301	kΩ
R_{Cnpn}	500	Ω
R_{Cpnp}	1	kΩ

For a input sine wave with amplitude of 1 Vrms and 2 kHz frequency, the output spectrum shown in Fig. A.1 was obtained.

Fig. A.1 shows that the in-band noise floor of the 2nd Order 1-bit ΣΔM is around -100 dB. Quantization noise is shaped and has a +40 dB increase per decade, as expected for

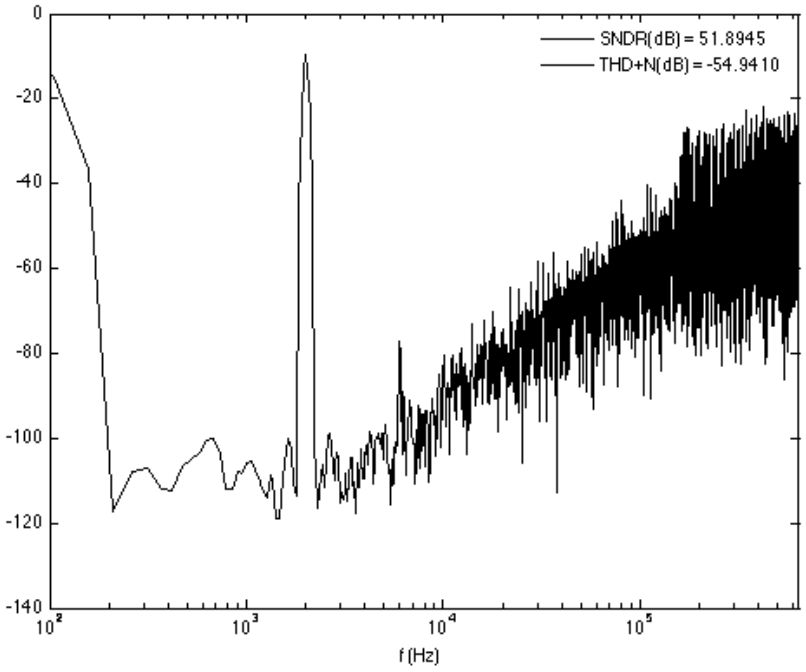


Figure A.1: Output Spectrum of the 2nd Order 1-bit CT-ΣΔM CIFB architecture obtained with electrical simulations (2^{16} points FFT using a Blackman-Harris window).

a 2nd Order ΣΔM. Since the zeros are not optimally distributed inside the signal bandwidth, the increase of quantization noise still inside the desired bandwidth leads to a decrease of the overall performance. Nevertheless, an SNDR of around 52 dB is obtained which is fairly close to the maximum expected (55 dB), for such ΣΔM.

B

Feedback circuitry for Single-Ended Architectures

B.1 Tri-State

In a single-ended architecture, the feedback of the $\Sigma\Delta$M can be realized by a differential amplifier, which picks both voltages from the output stage and convert it to a single-ended voltage of $\pm$ 1 V. This circuit, by proper design, can also level-shift the voltages from the output stage to the ones desired at the feedback.

Another way of achieving this is through the use of a tristate buffer. This will also provide the output required by the feedback circuitry, while being able to work without an output stage. The main idea behind this design is that the state of "high-impedance" can be used to represent the zero-state condition, while the logic signals "0" and "1" translate into -1 V and +1 V. This output voltages are reached through the positive and negative supply voltages applied to the tristate buffer. Since the supply voltages used are +5 V and -5 V, the desired output voltages ($\pm$ 1 V) are attained through the use of two resistors (ex: 1 kΩ and 4 kΩ), that compose a simple voltage divider.

To implement this feedback circuit, the logic behind the enable control input and the

data input must be properly designed. The tristate buffer should only be disabled when one of the I_C signals (at the output of the FFDs) opposes the other. If the enable is active low, this can be obtained by using an NOR logic gate. In the case where the enable control input is active high, an OR logic gate should be used.

Having the enable control input defined, the logic behind the data input can be designed through a truth table (Table B.1) composed of three inputs (both I_C signals and the enable input) and one output (the signal desired at the output of the tristate buffer). It should be noted that since there are two feedback paths (y_{out} and $\overline{y_{out}}$), the data input connections will alternate for each case. Thus, Table B.1 refers to the case where the y_{out} feedback path is considered.

I_{C1}	I_{C2}	$\overline{Enable}$	Out
0	0	0	0 or Z
0	0	1	x
0	1	0	-1
0	1	1	x
1	0	0	+1
1	0	1	x
1	1	0	x
1	1	1	x

Table B.1: 3-State Logic Codification for y_{out} feedback path.

From Table B.1, it follows that the desired output is obtained by the conjunction (AND Gate) of one of the I_C signal and the negation (NOT Gate) of the other I_C signal.

With the logic behind the data and the enable input defined, it is possible to reach the desired tristate feedback circuit, presented in Fig. B.1.

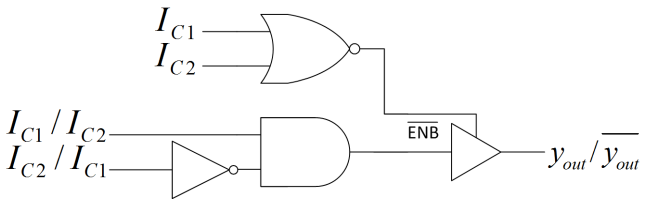


Figure B.1: 3-State Logic.

B.2 Transformer

Another way of converting both output voltages into a single feedback signal can be through the use of what is called a balun transformer. In its most common form, it consists in a pair of wires (commonly called the primary and the secondary) and a toroid core.

It works by converting the electrical energy of the primary into a magnetic field which is then converted back to a electric field by the secondary. These kind of baluns can provide a fairly good bandwidth but are generally limited to frequencies below 1.5 GHz. In addition to conversion between balanced and unbalanced signals, some baluns also provide impedance transformation. The higher the ratio used in this impedance transformation, the lower the bandwidth.

In the CT-$\Sigma\Delta$M case, each feedback voltage is applied to one of the primary terminals (balanced). Thus, the currents are equal in magnitude and in phase opposition. For the secondary, one of the terminals is connected to electrical ground and the other carries the single-ended feedback signal (unbalanced). This is shown in Fig. B.2.

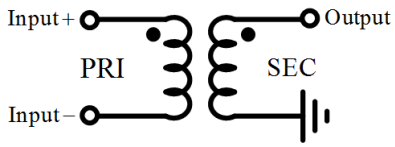


Figure B.2: Balun Transformer.

With the proper turns ratio, the output voltage can achieve the desired voltage levels. For instance, if the output stage provides +20 V and 0 V and the feedback signal should range from 0 V to +5V, a turns ratio of 4:1 should be used. The input and output voltages are presented in Fig. B.3.

The output voltage appears as a near-perfect square wave. This is due to the fact that the inductor values used were of at least 1 mH. For smaller values, the transition from 0 V to $\pm$5 V will present spikes (as shown in Fig. B.4), that may damage the circuit. This is due to the fact that a low inductance acts as a very low value resistor and a surge of current will occur.

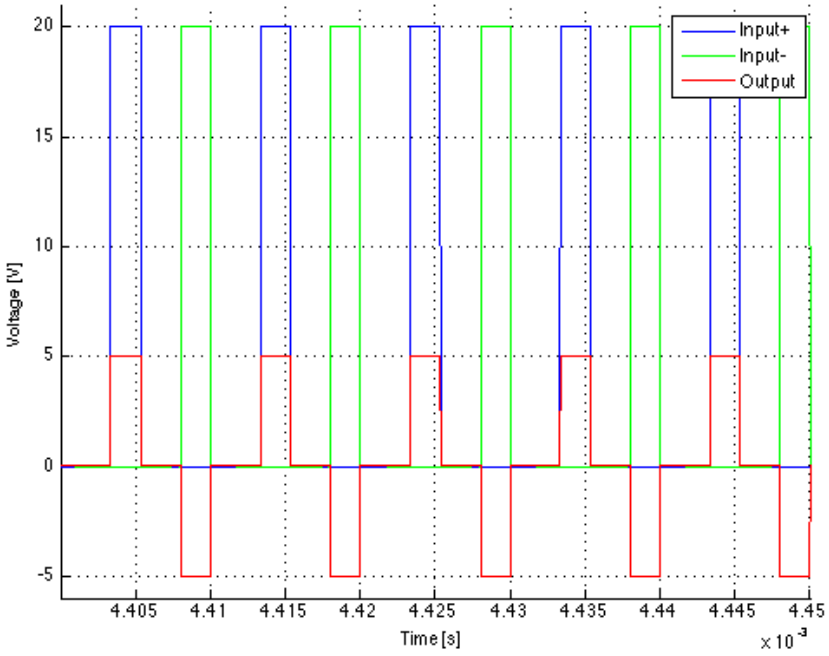


Figure B.3: Balun Transformer Behaviour.

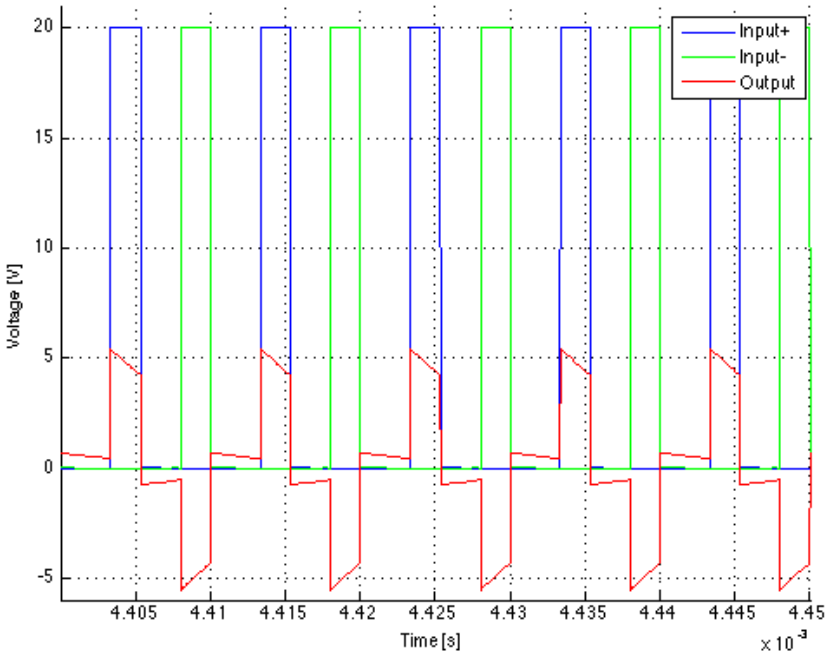
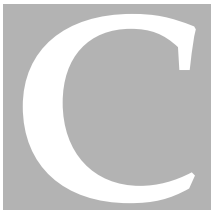


Figure B.4: Spikes that might occur when using a Balun Transformer.



Bibliography

[1] R. Cellier, G. Pillonnet, A. Nagari, and N. Abouchi. "An review of fully digital audio class D amplifiers topologies". In: *Circuits and Systems and TAISA Conference, 2009.* 2009, pp. 1 –4.

[2] M. Berkhout, L. Breems, and E. van Tuijl. "Audio at low and high power". In: *Solid-State Circuits Conference, 2008.* 2008, pp. 40 –49.

[3] T. Carusone, D. Johns, and K. Martin. *Analog Integrated Circuit Design*. John Wiley & Sons, 2011.

[4] R. Schreier and G. Temes. *Understanding Delta-Sigma Data Converters*. John Wiley & Sons, 2004.

[5] J. L. A. de Melo, B. Nowacki, N. Paulino, and J. Goes. "Design methodology for Sigma-Delta modulators based on a genetic algorithm using hybrid cost functions". In: *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on*. 2012, pp. 301 –304.

[6] N. Pereira, J. L. A. de Melo, and N. Paulino. "Design of a 3rd Order 1.5-Bit Continuous-Time Fully Differential Sigma-Delta ($\Sigma\Delta$) Modulator Optimized for a Class D Audio Amplifier Using Differential Pairs". In: *Technological Innovation for the Internet of Things*. Springer, 2013, pp. 639–646.

[7] A. Sedra and K. Smith. *Microelectronic Circuits*. Oxford University Press, USA, 2007.

[8] E. Gaalaas. *Class D Audio Amplifiers: What, Why and How*. 2006. URL: http://www.eetimes.com/design/audio-design/4015786/Class-D-Audio-Amplifiers-What-Why-and-How.

[9] B. Adams. *Sigma-Delta - New Algorithms and Techniques*. URL: http://www.cscamm.umd.edu/programs/ocq05/adams/adams_ocq05.pdf..

[10] S. Haykin. *An introduction to analog and digital communications*. John Wiley, 1989.

[11] S. Norsworthy, R. Schreier, G. Temes, and I. C. . S. Society. *Delta-Sigma data converters: theory, design, and simulation*. IEEE Press, 1997.

[12] F. Gerfers and M. Ortmanns. *Continuous-Time Sigma-Delta A/D Conversion: Fundamentals, Performance Limits and Robust Implementations*. Springer Series in Advanced Microelectronics. Springer, 2005.

[13] H. Inose, Y. Yasuda, and J. Murakami. "A Telemetering System by Code Manupulation – $\Delta\Sigma$ Modulation". In: *IRE Trans on Space Electronics and Telemetry* (1962), pp. 204–209.

[14] W. Gao, O. Shoaei, and W. Snelgrove. "Excess loop delay effects in continuous-time delta-sigma modulators and the compensation solution". In: *Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on*. Vol. 1. 1997, 65–68 vol.1.

[15] V. Vasudevan. "Analysis of Clock Jitter in Continuous-Time Sigma-Delta Modulators". In: *Circuits and Systems I: Regular Papers, IEEE Transactions on* 56.3 (2009), pp. 519–528.

[16] L. Breems and J. Huijsing. *Continuous-Time Sigma-Delta Modulation for A/D Conversion in Radio Receivers*. The Springer International Series in Engineering and Computer Science. Springer, 2001.

[17] R. Van Veldhoven. *Robust Sigma Delta Converters*. Analog Circuits and Signal Processing. Springer London, Limited, 2011.

[18] J. de Melo and N. Paulino. "A 3rd order 1.5-bit continuous-time (CT) Sigma-Delta ($\Sigma\Delta$) modulator optimized for Class D audio power amplifier". In: *Mixed Design of Integrated Circuits and Systems (MIXDES), 2010 Proceedings of the 17th International Conference*. 2010, pp. 531 –535.

[19] J. de Melo and N. Paulino. "Design of a 3rd order 1.5-bit continuous-time (CT) Sigma-Delta (SD) modulator optimized for Class D audio power amplifier". In: *International Journal of Microelectronics and Computer Science*. Vol. 1. 2. 2011.

[20] M. de Medeiros Silva. *Circuitos com transistores bipolares e MOS*. Fundação Calouste Gulbenkian, Serviço de Educação, 2003.