NOVA SCHOOL OF
SCIENCE & TECHNOLOGY

TIAGO MIGUEL RAMINHAS CARAPINHA

BSc in Electrical and Computer Engineering

DESIGN OF A COMPARATOR AND AN AMPLIFIER IN CMOS USING STANDARD LOGIC GATES

EVERY BRILLIANT DAY SHOULD BE LIVED FOR THOSE WHO PASSED AWAY

MASTER IN ELECTRICAL AND COMPUTER ENGINEERING

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"Even the smallest person can change the course of the future."

- Galadriel, The Lord of the Rings

ABSTRACT

Using standard logic gates in CMOS, or standard-cells, has the advantage of full synthesizability, as well as the voltage scalability between technologies. In this work a general purpose standard-cell-based voltage comparator and amplifier are presented.

The objective is to design a general purpose standard-cell-based comparator and amplifier in 130 nm CMOS by optimizing the already existing topologies with the aim of improving some of the specifications of the studied topologies.

Various simulation testbenches were made to test the studied topologies of comparators and amplifiers, in which the results were compared. The top performing standard-cell comparator and amplifier were then modified. After successfully designing the comparator, it was used in the design of an opamp-less Sigma-Delta modulator (ΣΔM).

The proposed comparator is an OR-AND-Inverter-based comparator with dual inputs and outputs, achieving a delay of 109 ps, static input offset of 591 µV, and random offset of 10.42 µV, while dissipating 890 µW, when clocked at 1.5 GHz.

The proposed amplifier is a single-path three-stage inverter-based operational transconductance amplifier (OTA) with active common-mode feedback loop, achieving a DC gain of 63 dB, 1444 MHz of unity-gain bandwidth, 51° of phase margin while dissipating 1098 µW, considering a load of 1 pF.

The proposed comparator was employed in the ΣΔM with a standard-cell based edge-triggered flip-flop. The ΣΔM, with a sampling frequency of 2 MHz and a signal bandwidth of 2.5 kHz, achieved a peak SNDR of 69 dB while dissipating only 136.7 µW.

Keywords: Standard-cell design, fully synthesizable, Comparator, Operational Transconductance Amplifier, Inverter-based, Sigma-Delta Modulator, 130 nm CMOS.

RESUMO

Utilizando portas lógicas básicas em CMOS oferece a vantagem de um circuito completamente sintetizável, tal como o escalamento de tensão entre tecnologias. Neste trabalho são apresentados um comparador de tensão e um amplificador utilizando portas lógicas.

O objetivo deste trabalho é desenhar um comparador e um amplificador utilizando portas lógicas através do estudo e otimização de topologias já existentes com a finalidade de melhoramento de algumas das especificações das mesmas.

Foram realizados vários bancos de teste para testar as topologias estudadas de comparadores e amplificadores, em que os resultados foram comparados. As topologias de comparadores e amplificadores de portas lógicas com melhor performance foram então modificadas. Após o comparador ter sido projetado com sucesso, foi utilizado na projeção de um modulador *Sigma-Delta* (ΣΔM) *opamp-less*.

O comparador proposto é um *OR-AND-Inversor* com duas entradas e saídas, que apresenta um atraso de 109 ps, *offset* estático na entrada de 591 µV, *offset* aleatório de 10.42 µV, enquanto dissipando 890 µW, utilizando uma frequência de relógio de 1.5 GHz

O amplificador proposto é um amplificador operacional de transcondutância *single-path three-stage inverter-based* com um *loop* ativo de realimentação do modo-comum, que apresenta um ganho DC de 63 dB, 1444 MHz de ganho-unitário de largura de banda, 51º de margem de fase e dissipando 1098 µW, considerando uma carga de 1 pF.

O comparador proposto foi aplicado no ΣΔM com um *flip-flop edge-triggered* baseado em portas lógicas. O ΣΔM, com uma frequência de amostragem de 2 MHz e uma largura de banda de 2.5 kHz, apresentou um SNDR máximo de 69 dB enquanto dissipando apenas 136.7 µW.

Palavras-Chave: Portas lógicas, completamente sintetizável, Comparador, Amplificador Operacional de Transcondutância, baseado em Inversores, Modulador Sigma-Delta, 130 nm CMOS.

CONTENTS

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ACRONYMS

AC	Alternate current
ADC	Analog-to-digital converter
BW	Bandwidth
C_L	Load capacitance
C_M	Miller capacitor
CM	Common-mode
CMFB	Common-mode-feedback
CMOS	Complementary metal–oxide–semiconductor
CMR	Common-mode input range
CMSL	Common-mode stabilization loop
CT	Continuous time
CT-SDM	Continuous-time ΣΔ modulator
ERBW	Effective resolution bandwidth
DAC	Digital-to-analog converter
DC	Direct current
DM	Differential-mode
DR	Dynamic range
DT	Discrete-time
DT-SDM	Discrete-time ΣΔ modulator
DVC	Dynamic voltage comparator
ENOB	Effective number of bits
FFC	Feedforward-compensated
FFT	Fast Fourier Transform
FT	Fourier Transform
FOM	Figure of merit
GBW	Gain-bandwidth product
I9BSSA	Inverter 9 based single-stage amplifier
I_D	Drain current
Inv	Inverter

MC	Miller-compensated
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOS	Metal-Oxide semiconductor
MOSCAP	MOS capacitor
N/A	Not available
OAI	OR-AND-Inverter
OTA	Operational transconductance amplifier
OS	Output swing
OSR	Oversampling ratio
P_D	Power consumption
PM	Phase margin
PMOS	p-channel metal-oxide semiconductor
PSD	Power spectral density
PVT	Process, voltage, and temperature
R_M	Miller resistor
RMS	Root-Mean-Square
RRDVC	Rail-to-rail dynamic voltage comparator
SAR	Successive-approximation
SADLC	Strong-Arm dynamic-latch comparator
SC	Switched-capacitor
SNDR	Signal-to-noise-and-distortion ratio
SP3SIB	Single-path three-stage inverter-based
SR	Set-Reset
UGBW	Unity-gain bandwidth
V_{CM}	Common-mode voltage
VCVS	Voltage controlled voltage source
V_{DD}	Supply voltage

SYMBOLS

A_{DC}	DC gain of the amplifier
C	Capacitor
C_{db}	Drain-bulk capacitance
C_{gd}	Gate-drain capacitance
C_{gs}	Gate-source capacitance
gds	Transistor's conductance
gm	Transistor's transconductance
p	Pole
R	Resistor
V_{diff}	Differential voltage
V_{DSat}	Drain-source voltage in saturation
V_{gs}	Gate-source voltage
V_{ref}	Voltage reference
$\Sigma\Delta$	Sigma-Delta (modulator)

1

INTRODUCTION

Each year semiconductor technology is suffering from size scaling into the nanoscale, allowing more density on integrated circuits. This requires lower supply voltages (V_{DD}) and reduces gate length, which results in a higher device intrinsic speed.

Characteristics such as more speed, more power efficiency, higher gain, higher bandwidth, and less noise sensitivity are some of the main aspects that are highly explored in state-of-the-art technology.

Technology scaling, together with the desire for high-speed digital circuits, turns the attention to CMOS standard logic. In CMOS, using standard logic gates, or standard-cells, has the advantage of them being fully synthesizable, as well as the voltage scalability between technologies. This offers advantages such as a compact layout, good trade-off performance between power consumption, noise, and speed, as well as rail-to-rail output range [1].

Comparators are devices that compare two electrical signals and determine if they are the same or different. They typically have two input terminals for the signals being compared and an output terminal that indicates the result of the comparison. Comparators can be designed to compare different types of variables, such as voltage, current, or frequency. Voltage amplifiers are devices that increase the amplitude or the power of an electrical signal. They take an input signal and produce an output signal that is a larger, more powerful version of the original. Amplifiers can be designed to amplify different types of signals, such as audio, video, or radio frequency signals.

Comparators and amplifiers are, therefore, a fundamental building block in modern electronic circuits and are the basic active blocks of any active filter, signal converter, analog block, or mixed-signal circuit. Switched-capacitor (SC) circuits, Sigma-Delta modulators, analog-to-digital converters (ADCs) such as the successive-approximation (SAR) ADC, oscillators, are some examples of commonly used circuits that use amplifiers and comparators.

In this work a general purpose standard-cell based voltage comparator and an operational transconductance amplifier are proposed.

This work is structured in 6 chapters.

In chapter 2, the study and comparison of standard-cell based operational transconductance amplifiers and voltage comparators topologies is made as well as a sigma delta modulator topology.

Chapter 3 presents the design methodology followed in this work.

In chapter 4, a general purpose standard-cell based voltage comparator and operational transconductance amplifier are proposed, as well as the theoretical analysis of the amplifier and its expected results are presented in chapter 5.

The next chapter, chapter 5, the simulation results of the proposed topologies are presented and discussed and the implementation of the proposed voltage comparator in the Sigma-Delta modulator described in chapter 2.

Finally, the conclusions, limitations and future proposals are presented in chapter 6.

1.1 Motivation

Facing the different state of the art topologies that are present, the aim of a topology that performed better in some way is desired. Standard-cell topologies may not be capable yet to compete, performance-wise, with non-standard-cell topologies. However, its scalability and simplicity offer a great advantage over the latter. So, the aim for simpler, good performing topologies is growing.

1.2 Objectives

The objective of this work is to design a general purpose standard-cell-based comparator and an amplifier in 130 nm CMOS by optimizing the already existing topologies with the aim of improving some of the specifications of the studied topologies.

To achieve this, a comparison between the proposed topologies and the current standard-cell state of the art topologies available is made by testing each of the studied standard-cell topologies to find the performance specifications of each, the overall better performing topology is chosen to be optimized in some way. The main specifications that will be accounted for in this work, for comparison are the following. For the comparators, a smaller delay, random offset, and power dissipation (P_D) are the main goals. Regarding the amplifiers, a larger direct current (DC) gain and unity-gain bandwidth product (UGBW), but at the expense of a smaller P_D, aiming for a better figure-of-merit (FOM). For the modulator, the aim is a better signal-to-noise and distortion-ratio (SNDR), effective-number-of-bits (ENOB), P_D, and FOMs.

Afterwards, the proposed comparator is implemented in an opamp-less Sigma-Delta modulator to prove its working condition and demonstrate its behavior when fully integrated in a CMOS circuit.

2

State of the Art in Comparators and Amplifiers in Standard Cells

As the CMOS technology advances there has been a significant development in both comparators and amplifiers whose topologies use all standard logic. Each topology, or design approach, has its advantages that depend on its final purpose. In this chapter are presented some of the different topologies studied from the literature that implement voltage comparators and OTAs in standard cells.

2.1 Voltage Comparators

The comparator is the most basic circuit that connects the analog and digital worlds, moving signals through them by comparing two inputs and producing relevant outputs. This makes comparators one of the fundamental components in most ADCs. Speed, power consumption, area, offset, and input range are some of the important specifications in a comparator. [2]

2.1.1 Fully Synthesizable, Rail-to-Rail Dynamic Voltage Comparator for Operation down to 0.3 V

Based on the dynamic voltage comparator (DVC) from [3] that incorporated a pair of cross-coupled NAND3 gates which [4] connected to a single-input Set-Reset (SR) Latch through inverter gates, as depicted in Figure 2.1, the author then implemented a similar topology using NOR3 gates. With limited common-mode input range (CMR), [4] combined both these topologies resulting in a Rail-to-Rail dynamic voltage comparator (RRDVC).

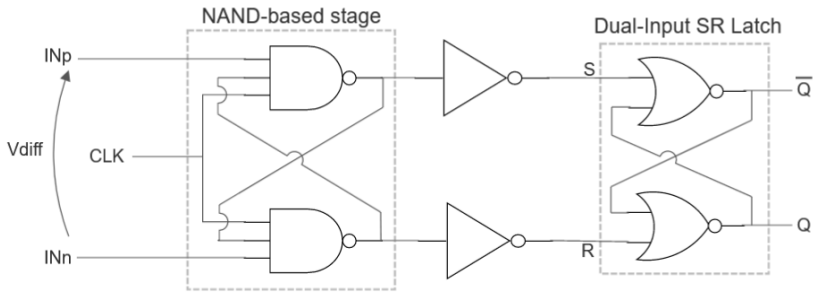
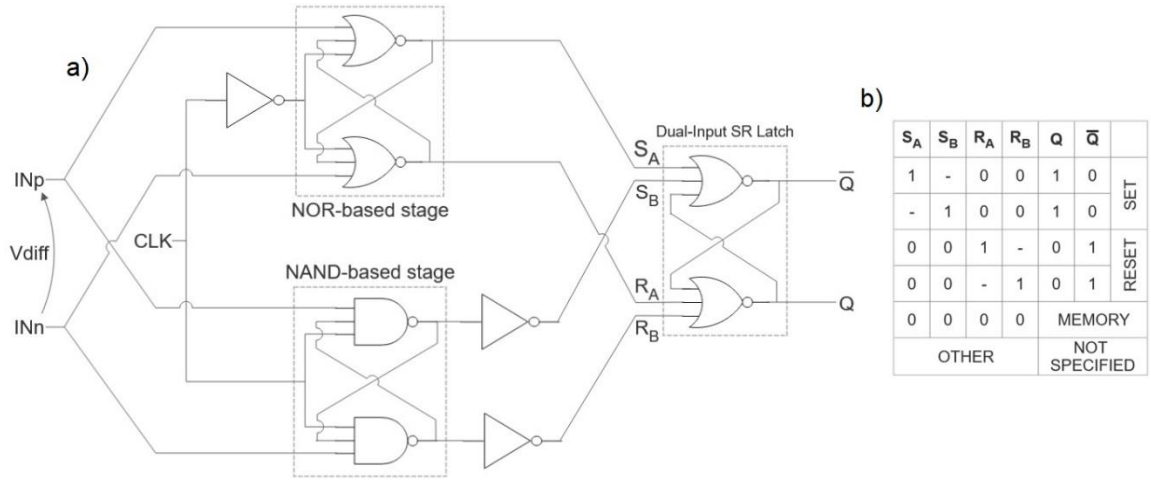


Figure 2.1 — NAND-based Input Stage with SR Latch.

The proposed RRDVC incorporates a NOR-based and a NAND-based input stages followed by a dual-input SR Latch. Here, the NOR-based stage detects the bottom half (0 - $\frac{V_{DD}}{2}$, closer to ground) and the NAND-based stage detects the top half ($\frac{V_{DD}}{2}$ - V_{DD}, closer to V_{DD}) of the CMR, Figure 2.2 a). These cross-coupled NOR3 and NAND3 input stages then drive the SR Latch containing two "set" inputs, S_A and S_B, and two "reset" inputs, R_A and R_B, which result in the OR truth table in Figure 2.2 b).

This is possible since when the common-mode (CM) input is in the bottom half, the NAND gates fail as their outputs stick to the precharge value (e.g., V_{DD}) and the NOR gates work correctly to generate the expected values of S_B and R_B. Here, the SR latch generates the correct output despite the values of the NAND gates (that are stuck at V_{DD}). The opposite occurs when the CM input is in the top half, where the NOR gates are stuck at ground, and the SR latch generates the output based on the S_A and R_A inputs resulting from the NAND gates. [4]



S_A	S_B	R_A	R_B	Q	$\bar{Q}$	
1	-	0	0	1	0	SET
-	1	0	0	1	0	
0	0	1	-	0	1	RESET
0	0	-	1	0	1	
0	0	0	0	MEMORY		
OTHER				NOT SPECIFIED		

Figure 2.2 — Fully synthesizable RRDVC in [4]: a) gate-level structure, b) truth table of the SR Latch.

This structure was designed in 40 nm CMOS technology and studied using three different supply voltages, 0.9 V, 0.6 V and 0.3 V, each limiting the CMR. All three had a different

impact on the delay, power, and input offset voltage of the proposed DVC, as shown in Figure 2.3, Figure 2.4, and Figure 2.5, respectively.

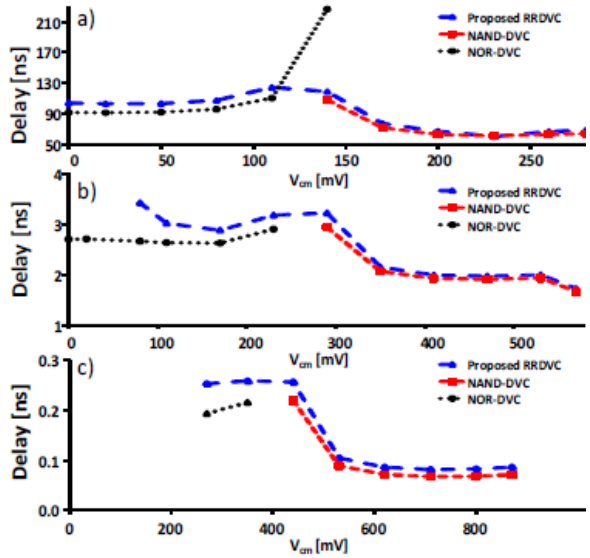


Figure 2.3 — Propagation delay vs. CM input voltage for the RRDVC, NAND and NOR DVCs with V_{diff}=5 mV, and a) V_{DD}=0.3 V, b) V_{DD}=0.6 V, c) V_{DD}=0.9 V [4].

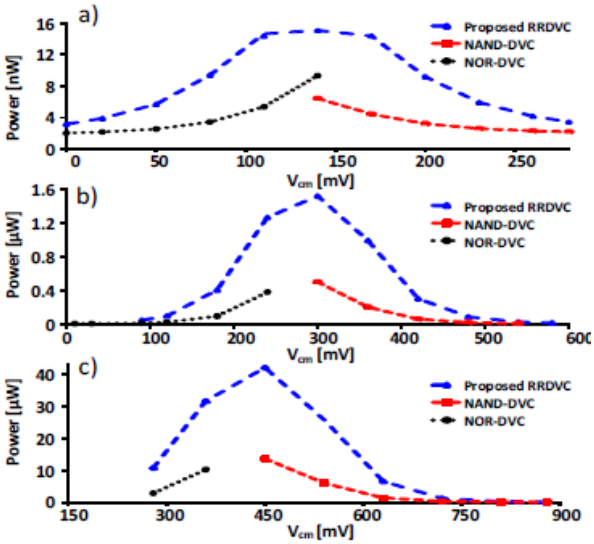


Figure 2.4 — Power consumption vs. CM input voltage for the RRDVC, NAND and NOR DVCs with V_{diff}=5 mV, and a) V_{DD}=0.3 V, b) V_{DD}=0.6 V, c) V_{DD}=0.9 V [4].

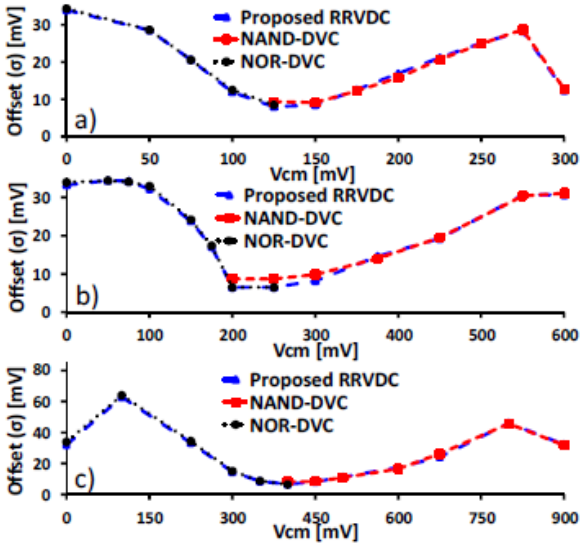


Figure 2.5 — Input offset voltage deviation vs. CM input voltage for the RRDVC, NAND and NOR DVCs with a) V_{DD}=0.3 V, b) V_{DD}=0.6 V, c) V_{DD}=0.9 V [4].

2.1.2 An All-Standard-Cell-Based Synthesizable SAR ADC With Nonlinearity-Compensated RDAC

A NAND comparator can be roughly yet simply interpreted as a group of clock switches, a preamplifier, and a latch. [5]

Proposing an OR-AND-Inverter (OAI)-based comparator as an improvement to the four-input NAND-based comparator. This NAND-based comparator, Figure 2.6, works by comparing V_P +$Vdac_P$ with V_N +$Vdac_N$ and contains the 2nd-stage latch, composed by the two NAND2 gates, which helps with the comparator gain during comparison and help to reset the outputs outside the comparison time. This topolgy has the issue of a limited input range where if an input experienced low voltage, when the sampling phase ends (high-to-low clock, CLK) the reset of the NMOS transistor is cut off. This results in a drain voltage difference from the drain node (n_x) maintaining residue charges with uncertain value, which can be unexpectedly amplified in the next comparison by the latch, resulting in an error output. [5]

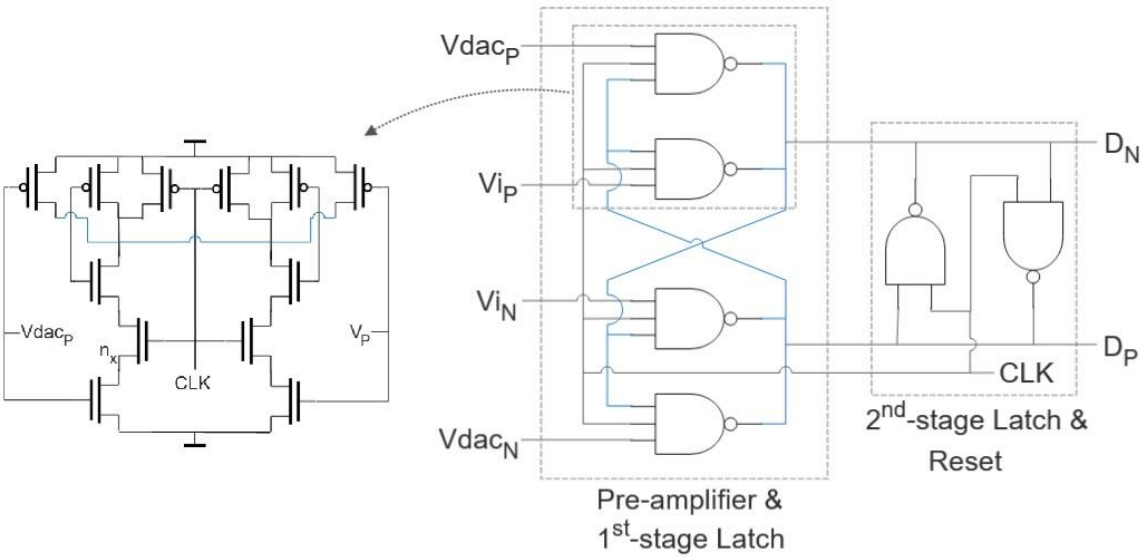


Figure 2.6 — Four-input NAND-based comparator in [5].

To add a reset path for the NMOS transistors n_x, the NAND topology was replaced by an improved topology from [6], the OAI topology, Figure 2.7, where n_x is reset after each comparison (CLK becomes low).

This change resulted in the probability of the error output being significantly reduced.

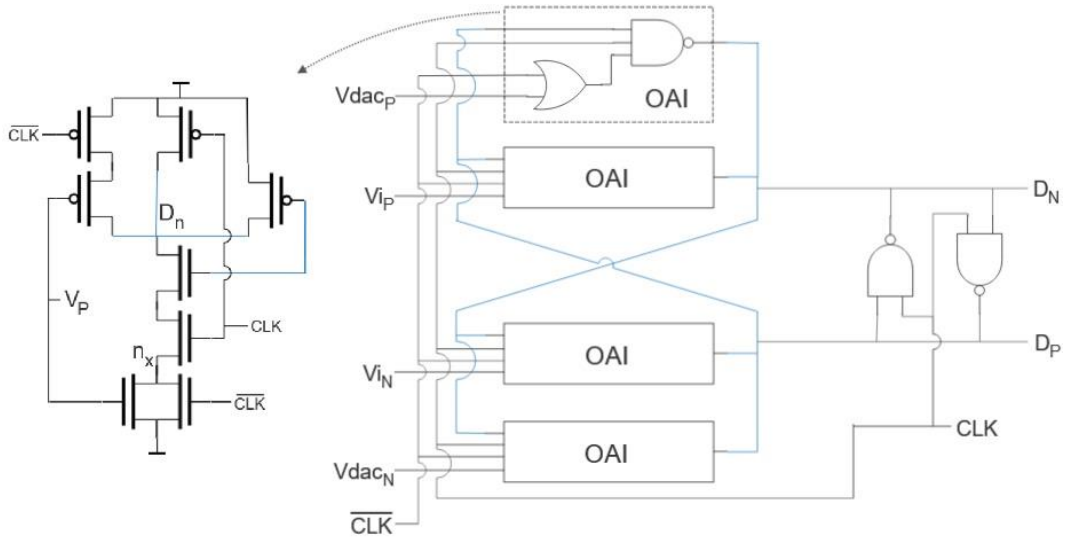


Figure 2.7 — OAI-based comparator in [5].

2.1.3 A 6-bit, 29.56 fJ/conv-step, Voltage Scalable Flash-SAR Hybrid ADC in 28 nm CMOS

A low power, high-speed comparator is proposed using a chain of inverters following a common-mode-feedback (CMFB) circuit, Figure 2.8. The CFMB, with the output connected to the bulk of the PMOS in the inverters, allows for compensation and correction of the common-mode voltage (V_{CM}) node variations caused by the process, voltage, and temperature (PVT), allowing for a fixed V_{CM}. By connecting a chain of these inverters in cascade, the input offset voltage of the comparator decreases. [7]

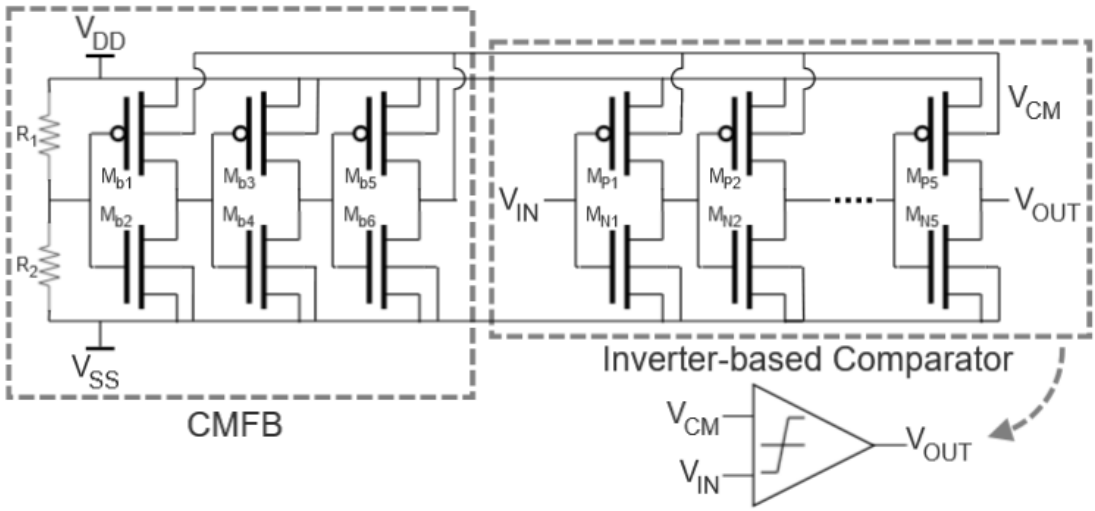


Figure 2.8 — Transistor level representation of the inverter-based comparator and CMFB circuit.

2.1.4 Design of Low Power High Speed Low Offset and Area Efficient Dynamic-Latch Comparator for SAR-ADC

A modified Strong-Arm dynamic-latch based comparator (SADLC) is proposed, designed using 180 nm CMOS technology and a supply V_{DD} of 1.8 V.

This topology incorporates a pair of cross-coupled inverters (M_6 with M_7, and M_9 with M_{10}) in the output, Figure 2.9, that determine which of the outputs, V_{OUT}- or V_{OUT}+, goes to V_{DD} and which goes to ground, depending on the difference between the reference voltage V_{ref} and V_{in} on each of the inputs, e.g. if $|V_{in+} > V_{in-}|$ the discharge rate of the V_{OUT}- node is faster, therefore connecting the V_{OUT}+ node to V_{DD}, being then latched high. [2]

Even though the SADLC is not a comparator based on logic gates, it presents what a state-of-the-art comparator is capable of in terms of its specifications such as speed power consumption and offset, as presented in Table 2.1. These values will serve as a comparison to the previously referenced comparators.

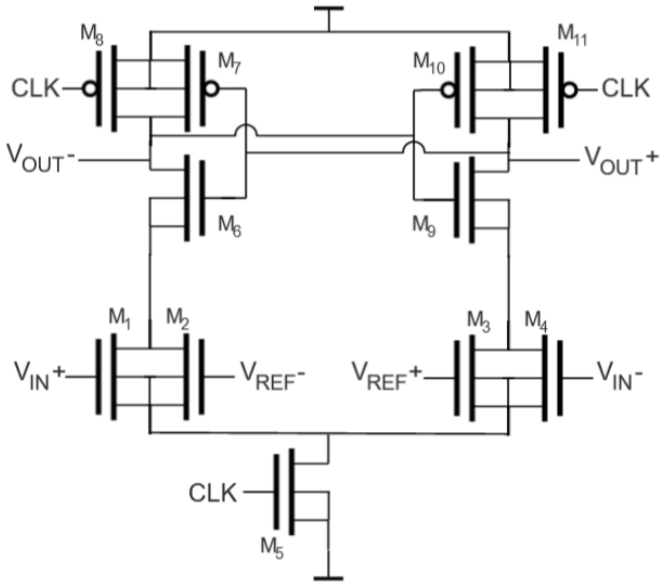


Figure 2.9 — Transistor level representation of the Strong-Arm dynamic-latch comparator.

2.2 Operational Transconductance Amplifiers (OTAs)

In a conventional inverter, assuming that both transistors are operating in the saturation region, its input is amplified by the two transistors. Inverter-based amplifiers usually rely on a cascade, multiple-stage, topology. Its gain varies depending on the CMOS technology being used. [8]

Improved DC gain, output swing (OS), slew rate, bandwidth and power consumption are the main go-to requirements for an amplifier.

2.2.1 An inverter-based OTA used in a 1.9 mW 250 MHz Bandwidth Continuous-Time ΣΔ Modulator

In the loop filter of the ΣΔ modulator presented in [9], pseudo differential inverter-based operational transconductance amplifiers (OTAs) are being used, as depicted in Figure 2.10.

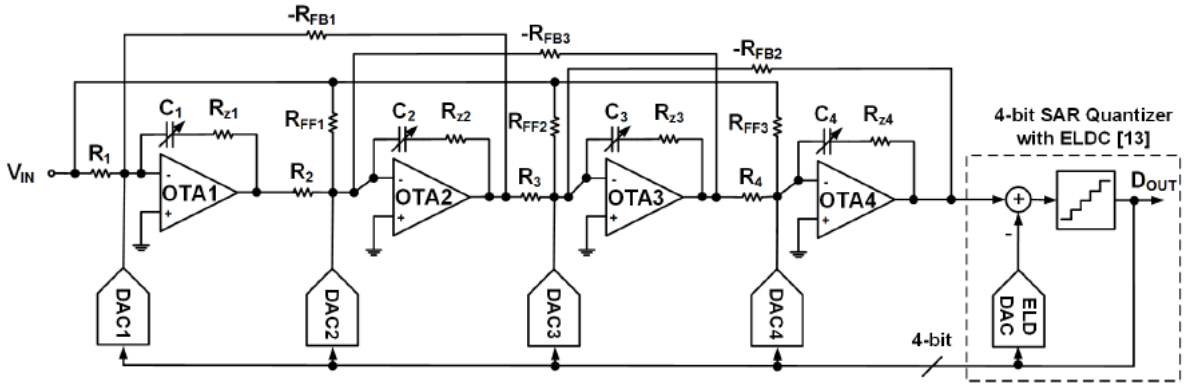


Figure 2.10 — Single-ended continuous-time ΣΔ modulator presented in [9].

This approach was chosen for its high bandwidth and as a mean of re-using the supply current. Here, OTA 1, OTA 2, and OTA 4 are implemented as single-stage inverter-based, while OTA 3 is implemented as a three-stage multi-path inverter-based amplifier, as seen in Figure 2.11. High bandwidth and supply current re-use are some of the benefits for using inverters for the analog amplifiers. [9]

OTA 3 consists of a high-gain path containing inverters 1-3 and a high-speed path using inverter 4, also a RC network (composed of a Miller resistor (RM) and a Miller capacitor (CM)) is used to boost the phase margin and split the poles. Each OTA used in this modulator has a CMFB circuit, as represented in Figure 2.11. In these, the input VCM are controlled with RL1 while the output CM is sensed by the two resistors (RL2) and amplified by the inverters in the CMFB. The CMFB loop is stabilized using the capacitors CL1 and CL2. [9]

The UGBW of the integrators containing the OTAs is limited to avoid clipping of the integrators. Maximizing the UGBW of the first integrator relaxes the thermal noise requirements of the second, third, and forth integrators.

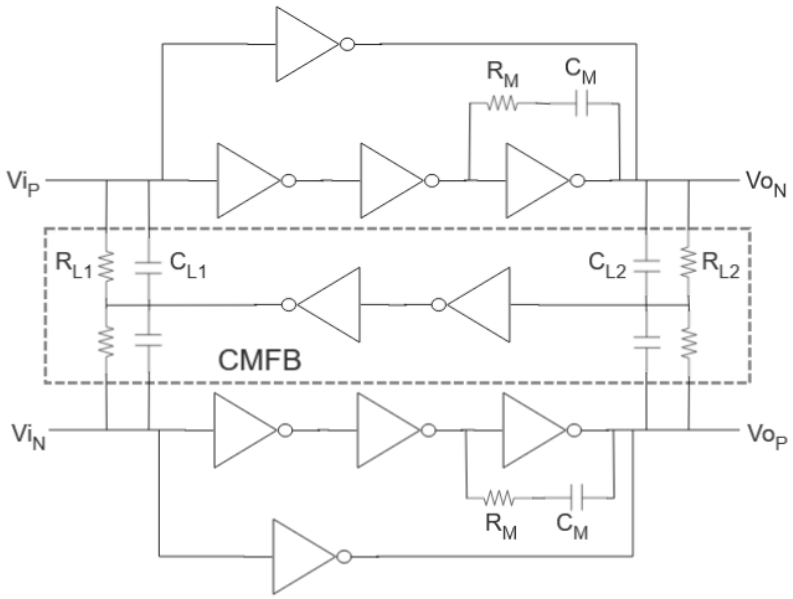


Figure 2.11 — Three-stage inverter-based amplifier used in OTA 3.

OTA 1/2/4 consume five times less power than OTA 3, which dissipates only 500 µW with a 1.1 V power supply.

2.2.2 Inverter-Based Subthreshold Amplifier Techniques and Their Application in 0.3-V ΔΣ Modulators

A Miller-compensated (MC) OTA and a feedforward-compensated (FFC) OTA presented for the discrete-time ΣΔ modulators (DT-SDM) and continuous-time ΣΔ modulators (CT-SDM), respectively, were proposed in [10]. Both OTAs are inverter-based, two-stage, with frequency compensation.

Each stage of the MC-OTA uses the inverter-based amplifier in Figure 2.12, however, the second stage has C_M for frequency compensation (splits the poles of the two-stage amplifier), as shown in Figure 2.13 a). Driving this capacitor, however, consumes extra current, affecting the power efficiency. [10]

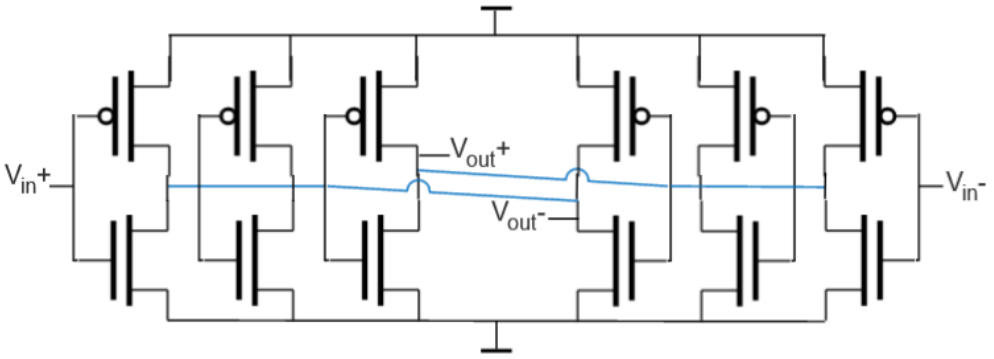


Figure 2.12 — Inverter-based cross-coupled pseudo-differential structure [10].

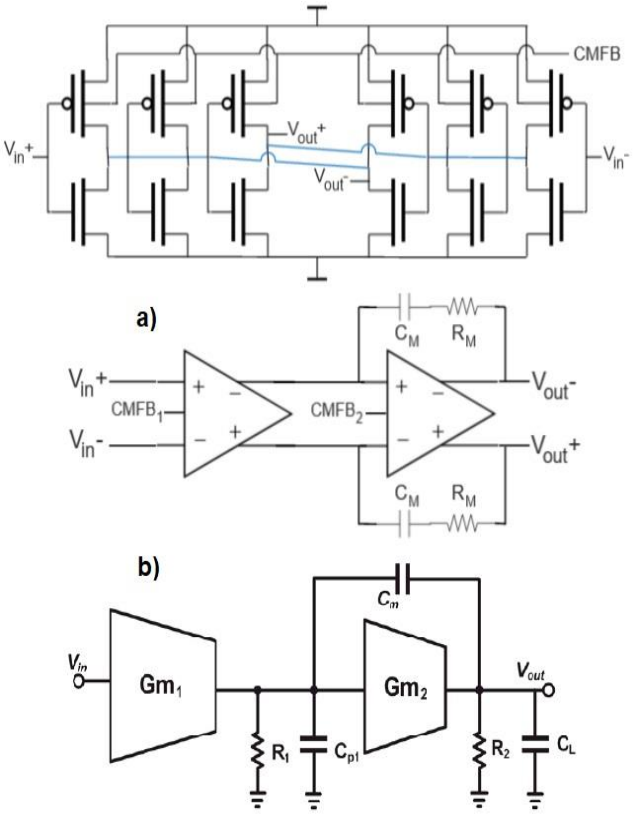


Figure 2.13 — Presented two-stage MC-OTA in [10]: a) schematic, b) simplified small-signal model.

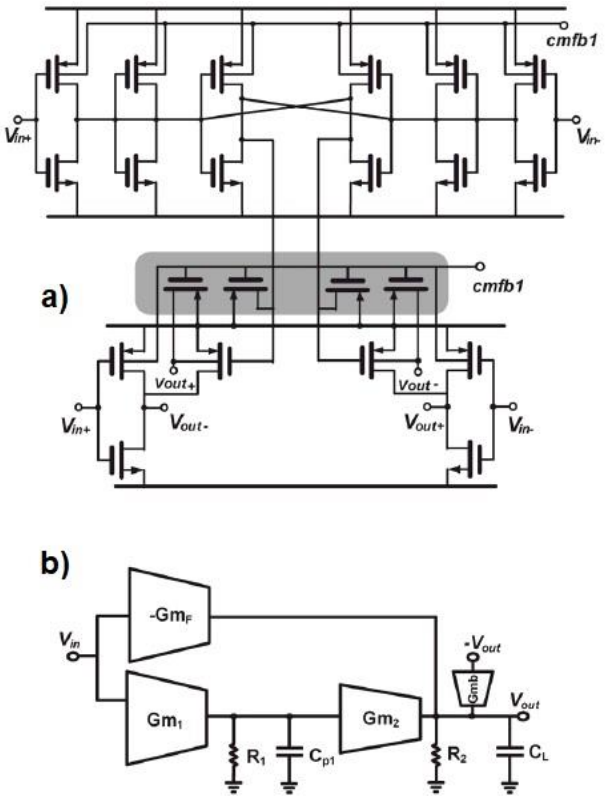


Figure 2.14 — Presented two-stage FFC-OTA: a) schematic, b) simplified small-signal model [10].

As an alternate, more complex, option, the FFC-OTA model, presented in Figure 2.14 a), is based on the pole-zero cancellation, increasing UGBW and power efficiency. For noise and robustness considerations, this FFC-OTA also uses the amplifier in Figure 2.12 for its first stage. In the second stage, a single PMOS with cross-coupled gain enhancement through the bulk terminals is used. A single inverter is used in the feedforward path [10].

An inverter-based solution is presented for the CMFB circuit, in Figure 2.15, where the bulk of PMOS transistors of the amplifier are used for the CMFB control [10].

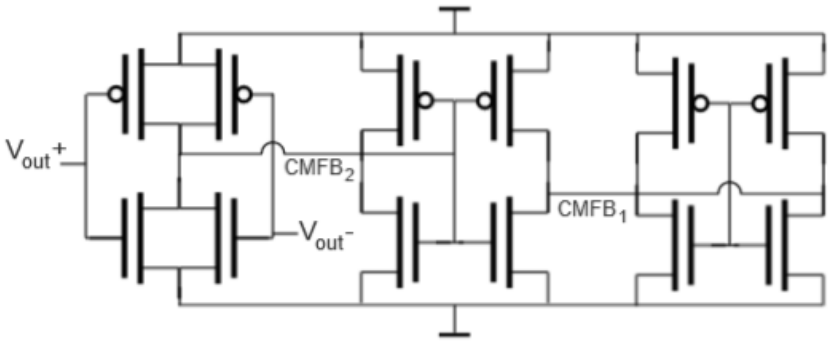


Figure 2.15 — Inverter-based common-mode feedback circuit [10].

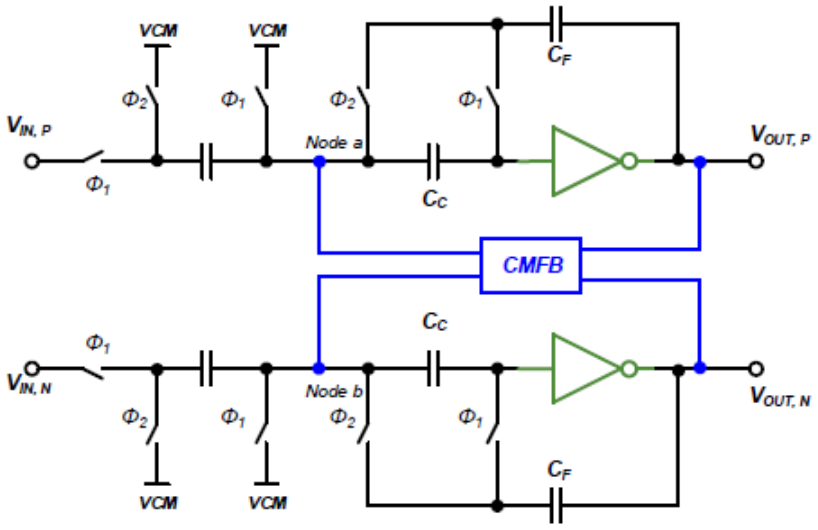
The FFC-OTA shows a superior performance compared to the MC-OTA due to its capacitor-free compensation. UGBW, phase margin, slew rate and overall FOM are improved over the latter, at the cost of more complexity [10].

2.2.3 Trade-offs and Limitations in Energy-Efficient Inverter-based CMOS Amplifiers

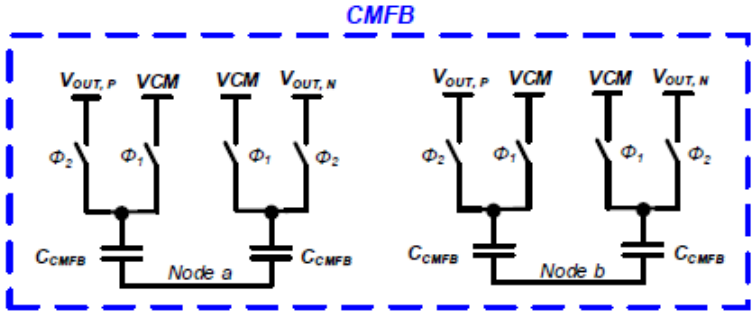
Three discrete-time (DT) inverter-based amplifiers were presented in [11], containing a single inverter, a three-stage inverter with a multipath and a three-stage inverter. These were designed using SC circuits.

Here, [11] proposed a circuit adapted from the Inverter-based SC Integrator presented by [12], in Figure 2.16, and containing the same CMFB circuit, but with its single Inverter replaced by a cascade of three Inverters, as proposed in the OTA 3 by [9], Figure 2.11, without a multipath (dropping the high frequency path), as depicted In Figure 2.17.

Maintaining the passive CMFB circuit of [12] also presented a good advantage concerning power consumption by reducing the number of unity Inverters that would be used with the CMFB circuit in [9].



(a)



(b)

Figure 2.16 — a) Inverter-based SC Integrator, b) passive CMFB circuit [11].

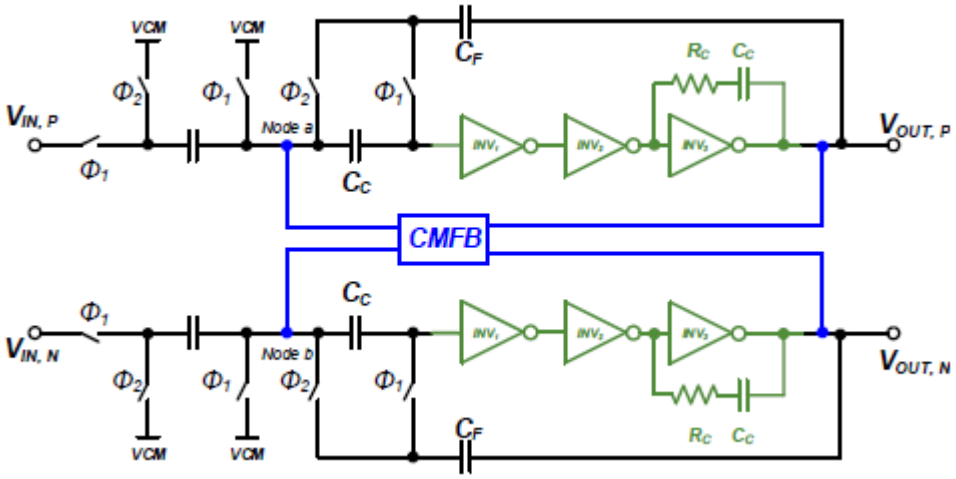


Figure 2.17 — Single-path three-stage pseudo-differential Inverter-based OTA [11].

This way, [11] proposed a circuit with a DC Gain much higher than the one achieved by [12] with a single Inverter and greater to the one achieved in the OTA 3 by [9], but also with a UGBW above 1 GHz, and not compromising the stability of the circuit with a high enough phase margin (PM). This circuit, out of the three, also presented the best compromise between linearity versus OS, the number of unity Inverters and power consumption.

2.2.4 Ultra-Low-Voltage Inverter-Based Amplifier with an efficient Common-Mode Stabilization Loop

[1] proposed an ultra-low voltage single stage amplifier topology consisting only of inverter gates, Figure 2.18. The main inverters (Inv1 and Inv2) process the differential input signal while the other seven inverters (Inv3 - Inv9) implement the common-mode stabilization loop (CMSL).

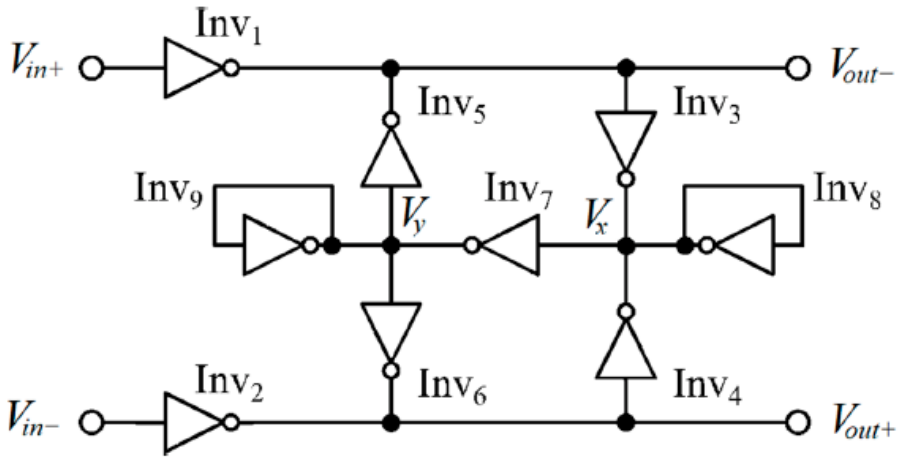


Figure 2.18 — Inverter 9 based single stage amplifier [1].

Here the CMSL serves the purpose of reducing the CM to CM gain close to unity in order to maintain the differential output range as well as making the amplifier usable in SC applications.

The pairs of inverters present in this amplifier (Inv1 and Inv2, Inv3 and Inv4, Inv5 and Inv6) were maintained identical for symmetry reasons. Inv8 and Inv9 are unity-gain-connected inverters.

The CMSL works with Inv3 and Inv4, being loaded by Inv8, extracting a signal that is proportional to the CM voltage at the output (V_x). V_x is then inverted by Inv7, loaded by Inv9, originating V_y which then drives the inverters Inv5 and Inv6. Inv5 and Inv6 are responsible for injecting CM currents into the output nodes, finally closing the CMSL.

With small signals, the output differential-mode (DM) voltage does not affect the node V_x due to the symmetry between Inv3 and Inv4. However, due to the non-linear behavior of Inv3 and Inv4, with larger signals (large differential voltages on the output) V_x may be

affected. This means that the CMSL operation is affected making the output CM dependent on the DM of the output. The output DM voltage changes are not significant due to the action of Inv5 and Inv6 being symmetrical. This results in the CMSL not having a significant impact on the DM to DM gain and the range of the DM, other than the lower output DM resistance of the amplifier caused by the output resistances of Inv5 and Inv6. Sizing the latter inverters to a higher channel length compared to inverters Inv1 and Inv2 diminishes the previous problem.

It is worth noting that with the use of ultra-low supply voltages the circuits tend to suffer more from PVT variations.

The low DC gain of the amplifier is due to the single-stage topology and minimum channel lengths, which offered a tradeoff between bandwidth and power consumption.

2.3 Sigma-Delta (ΣΔ) Modulators

A ΣΔ modulator and the decimation filter compose the two main blocks of a ΣΔ ADC. Its order is determined by the number of integrators in the modulator. There are two topologies best known for high-order modulators, the feedforward topology, and the feedback topology. The feedback topology works as an oversampled tracking system with negative feedback [13], but the feedforward topology presents advantages such as a decreased sensitivity to the nonlinearities of the integrator, allowing the use of a lower oversampling ratio (OSR), granting the use of the modulator in wideband applications [14]. [15]

Second-order ΣΔ modulators, for their increased dynamic range, are probably the most common category of modulators. [13]

Out of all the active components that constitute a time-based ΣΔ modulator, the ones that consume most of the power are the operational amplifiers that make for the integrators in the active loop filter. This way, replacing this active loop filter with a passive network would consume less power. [16]

2.3.1 A 0.4-V 410-nW Opamp-Less Continuous-Time ΣΔ Modulator for Biomedical Applications

[17] proposed a 2^{nd} order opamp-less CT-SDM using a passive loop-filter composed by two cascaded RC circuits, Figure 2.19, which lets the circuit obtain a second order noise shaping and therefore save power [18].

The only active block in the circuit is the dynamic comparator, and even though there is lack of gain in the loop-filter that would otherwise be provided by an active integrator, the comparator provides the required gain to the loop.

The CMOS inverters used in the feedback loop, being used as digital-to-analog converters (DACs), help to improve the comparator drive the resistors R2 and R'2. It is important to

note that both these inverters are responsible for about 50% of the overall power dissipation of the modulator.

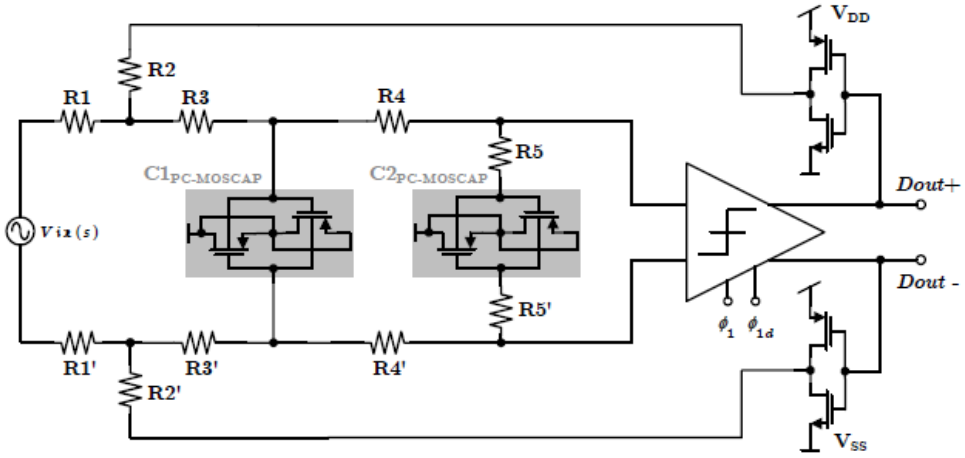


Figure 2.19 — 2nd order opamp-less CT-SDM with passive loop filter [17].

To enhance the attenuation of the quantization noise, the two poles of the loop-filter should be close to zero. This will result in excessive ringing in the closed-loop system when feedback is applied to the loop-filter. To control this, a zero is added to the circuit by the R5 resistor that is in series with the capacitor of the second RC circuit.

As an improvement to the modulator in [18], both capacitors in the loop-filter RC circuits were replaced by parallel compensated depletion-mode MOS capacitors (MOSCAPs), as depicted in Figure 2.19. These help to obtain a small area, since in most CMOS technologies these have a higher capacitance per area compared to metal-insulator-metal (MIM) capacitors and metal-oxide-metal (MOM) capacitors, therefore reducing the final cost of the circuit.

2.4 Comparator and amplifier specifications - A comparison

In conclusion, as depicted in Table 2.1 and Table 2.2, different topologies meet different specifications.

While comparing these topologies, it's important to consider the different CMOS technologies being used and, regarding the amplifiers, take into account that the load capacitance (C_L) is an important characteristic that influences the results.

The authors' non-disclosure on some of the obtained specifications results in a more challenging comparison, and any conclusions regarding this subject will be considered preliminary. The simulations scheduled for the next phase of the project will allow a more accurate and thorough comparison and an update of the Table 2.1 and Table 2.2.

For the comparators, shown in Table 2.1, and starting with the CMR the results are very different since the CMR strongly depends on V_{DD}. The delay on the inverter-based topologies, [2] and [7] is substantially smaller than the other topologies. [4] presents the best results in

terms of power consumption in its 0.3 V and 0.6 V voltage supply topologies but, in terms of comparison, [2] shows a lower power consumption, considering its supply voltage of 1.8 V. As for input offset voltage, [2] has the lowest offset.

For the amplifiers, shown in Table 2.2, even though [11] has a higher DC gain, gain-bandwidth product (GBW), and OS, since this is an OTA that operates in DT, the comparison cannot be made since the objective of this thesis is a continuous time (CT) OTA. Hence, regarding Gain, the FFC-OTA in [10] shows the best result. For GBW and Power dissipation, [9] presents, by far, the best result. Phase margin is higher in [10], particularly in the FFC-OTA. The OTA from [10] also presents, by far, the best FOM of the studied CT amplifiers.

Table 2.1 — STUDIED COMPARATOR SPECIFICATIONS.

Comparator	[2]	[4]			[3]*	[5]	[7]
Type	Strong-Arm Dynamic Latch	RRDVC NAND/NOR input stage and Dual-Input SR latch			NAND DVC	OAI (OR-AND-Inverter)	Inverter-based
CMOS [nm]	180	40	40	40	40	65	28
V_{DD} [V]	1.8	0.9	0.6	0.3	0.6	1.2	0.9
CMR [V]	N/A	0.2 - 0.9	0.1 - 0.6	0 - 0.3	0.4 - 0.6	2.2	N/A
Delay [ns]	0.0934	0.25	3	100	2	N/A	0.094
Power [µW]	4.72	40	1.50	0.015	0.50	160	N/A
Random Offset [mV]	6	60	40	28	40	N/A	14
Area [µm2]	N/A	62	62	62	35	N/A	N/A

N/A – not avaliable.

*The specification values from [3] are the ones simulated by [4].

Table 2.2— Studied Amplifier Specifications.

Amplifier	[9]	[10]	[10]	[11]	[1]
Type	OTA inverter-based (OTA 3)	Miller-Compensated OTA (two stage)	Feedforward-Compensated OTA (two stage)	DT Single Path 3 Stage Inv-based OTA (Circuit3)	I9BSSA
CMOS [nm]	40	130	130	130	180
V_{DD} [V]	1.1	0.3	0.3	1.2	0.5
DC Gain [dB]	38	46.2	49.8	57.9	25.2
GBW [MHz]	162	2.45	9.1	1360	0.132
Slew Rate [V/µs]	N/A	2.4	3.8	N/A	N/A
PhaseMargin [°]	N/A	52	76	62.9	87
OutputSwing [V]	N/A	0.1	0.1	0.63	N/A
Power [µW]	500	1801	1800	616	0.279
C_L [pF]	1	2	2	1	10
FOM [GBW*CL/Power] [MHz*pF/mW]	324	2.72	10.11	2207	4.73

N/A – not avaliable.

3

Design Methodology for Comparators and Amplifiers

When designing components, it is important to run simulations in order to confirm or improve their performance. These simulations were performed using the Cadence 6 ADE XL tool. Here, various simulations were put together to achieve the least effort and time consumption each time a circuit was modified.

In the first part of this chapter are presented the various testbenches prepared to test the topologies. After, the simulation results of the state of the art topologies are presented and discussed.

3.1 Simulation Testbenches

Three sets of testbenches were prepared: one set for the comparators, another for the amplifiers, and another for the modulator. This chapter presents the methodology used to test each studied topology, as well as the proposed topologies.

3.1.1 Voltage Comparators Testbench

In this chapter, the tests run in the voltage comparators are presented. These tests were simulated with the schematics presented in the Appendix, Figure A.0.1 and the voltage sources in Figure A.0.2.

3.1.1.1 Behavior and power dissipation

To test the correct functioning of the comparators a transient simulation was run, featuring a triangular waveform with maximum amplitude (rail-to-rail) and slow period (e.g. 100 ns) and a fixed voltage serving as threshold (if the comparator is designed to accept two inputs) as inputs in order to compare them. In this test it is also possible to check the current that the circuit is consuming in order to obtain its power. Since the current is always alternating,

due to the switching inside the comparator, the needed current value is the root-mean-square (RMS) of the current passing through the voltage source, then multiplied by V_{DD}.

3.1.1.2 Systematic offset and Random offset

Systematic offset (static)

To determine the systematic offset of the comparators, also referred as static input offset, (the offset that is constant in every decision of the comparator for a certain V_{ref}) a transient simulation was run but the triangular waveform in the input has a much lower frequency than the previous one (e.g. 1 µs) and its maximum and minimum voltages are very close to the threshold voltage of the comparator (e.g. 5% of the maximum amplitude). This way an accurate reading of the comparator's behavior can be obtained and analyzed.

If the comparator incorporates a clock, then the frequency of the input triangular wave must be a prime number relative to the clock frequency. This way the simulation will be able to test the behavior of the comparator when the input wave voltage is climbing and falling both during clock LOW and clock HIGH.

The final offset value of the comparator is obtained by calculating the mean of all the offset values corresponding to the different states of the comparator.

No offset cancellation techniques are presented in this work.

Random offset

Various techniques can be used to correct for the systematic offset; however, these do not apply to random offset.

In comparators the random offset is always present, either because of hysteresis, metal-oxide semiconductor (MOS) transistor mismatch, or because of some clock scheme to improve certain aspects of the circuit, and in these situations the offset is more complicated to analyze. The solution is to run various Monte-Carlo simulations (also using ADE XL) in order to find the standard deviation of the offset value.

To analyze the random offset the width of each transistor was randomized with a value that is within the standard deviation of one percent of the original (mean) value. A sample of 30 values from a Gaussian distribution, with the previously mentioned characteristic of 1% of standard deviation, was applied to the width of each transistor in order to approach a random result on the simulations.

Finally, for each comparator, the standard deviation value was calculated from the sample of the 30 offset values. This resulting standard deviation value is the random offset, measured in the same unit of the systematic offset.

3.1.1.3 Comparison time

To determine the time of comparison a transient simulation was run, and the reference input waveform included both easy decisions (V_{ref} = 50 mV) and hard decisions (V_{ref} = 5 mV)

above and below the set threshold of the comparator. The comparison time is then measured from when the comparison starts (clock HIGH) until the exit of the comparator reaches 90% of V_{DD}. Conventionally, the final comparison time of the comparator is the highest of all the decisions tested.

3.1.2 Operational Transconductance Amplifier (OTA) Testbench

This chapter presents the tests performed in all the studied amplifiers, except for the tests in chapters 3.1.2.3, 3.1.2.4, and 3.1.2.5 which were just for the proposed amplifier.

3.1.2.1 DC Operating Bias Points

To test the transistors functionality a DC simulation was run in order to confirm every transistor was in the saturation region. In this simulation it was also possible to calculate the power consumption of the amplifiers as well as determine the operating points of the transistors.

This test was made according to the schematic in the appendix, Figure A.0.3.

3.1.2.2 AC analysis

An alternate current (AC) simulation was run in order to obtain the frequency response of the amplifier (magnitude and phase).

A bias point was established by applying the input signal DC level at $V_{DD}/2$.

A C_L of 1 pF was used and a PM greater than 45º was required to not compromise the stability of the system.

This test was made according to the schematic in the appendix, Figure A.0.3.

3.1.2.3 Settling-Time

To observe the stability of the amplifier as well as calculating its settling time, a transient simulation was run. The testbench consisted of an inverting montage to the amplifier with unity gain ($R_a = R_b = 100$), where voltage-controlled voltage source (VCVS) were used as ideal buffers with unity gain before the feedback resistors.

The input signal used was a step with 100 mV_{diff} with CM voltage of $V_{DD}/2$.

This test was made according to the schematic in the appendix, Figure A.0.4.

3.1.2.4 Slew-Rate

The time domain response of the circuit in unity gain configuration, same as in 3.1.2.3, in response to a square wave with an amplitude of 200 mV_{diff} and a period of 20 ns. The period of the square wave was kept small in order to have a good visual definition of the amplifier's response.

This test was made according to the schematic in the appendix, Figure A.0.4.

3.1.2.5 AC Noise

A new testbench was made to determine the input referred thermal noise of the amplifier.

No inductors were used in the feedback loop since these would create an open loop at high frequencies. Instead, VCVS were used as ideal buffers with unity gain before the feedback resistors in the inverting montage with unity gain ($R_a = R_b = 10$ K).

An AC noise simulation was run between the frequencies of 1 Hz and 10 GHz. The resulting noise power spectral density (PSD) is then integrated in a band of frequencies where the flicker noise would not be present, resulting in the thermal noise of the amplifier.

This test was made according to the schematic in the appendix, Figure A.0.5.

3.1.3 Sigma-Delta Modulator Testbench

Similar to [17], this modulator was tested for a main differential input voltage signal of 220 mV. The sampling frequency used was Fs = 2 MHz with an OSR of 1024 (1), resulting in an input frequency of Fin = 976.5625 Hz which is close to the 1007.08 Hz input frequency used in [17].

$$OSR=Fs/(2*Fin) \quad (1)$$

The modulator was tested for various input signal frequencies above the base frequency of 976.5625 Hz with the purpose of finding the effective resolution bandwidth (ERBW) of the modulator, in this case with a differential input signal voltage of 220 mV. The ERBW of the modulator is the analog input frequency at which the SNDR drops by 3 dB from the base frequency value, giving the maximum bandwidth (BW) the converter is capable of handling.

The simulations for the modulator were performed using Cadence 6. These were transient simulations with 36 ms duration which, when sampled with a frequency of 2 MHz, resulted in over 2^{16} (65536) points.

The resulting points of the simulations, extracted between the comparator and flip-flop, were sent to Octave in which the Fourier Transform (FT) was calculated using the Fast Fourier Transform (FFT) algorithm and analyzed in order to calculate the signal-to-noise-and-distortion ratio (SNDR) of the modulator.

For calculating the dynamic range (DR) of the modulator other differential input voltages were tested until the FT did not present a noise shape with 40 dB/dec slope or presented 0 dB of SNDR.

The same simulations were then run when applying a transient noise with a frequency between 1 Hz and 20 MHz, in which the latter represents 10 times the sampling frequency used in the modulator. This simulation includes flicker noise, thermal noise and shot noise in

the simulations, which are no longer taken into consideration when the transient noise in the simulations is not applied.

The modulator test was made according to the schematic in the appendix, Figure A.0.6.

3.2 Electrical Simulations of prior art

Each of the circuits previously presented in chapter 2 have been redesigned in CMOS 130 nm technology and tested in order to decide which of the topologies had a better behavior.

Regarding the CMOS inverters used in comparators and amplifiers, both the PMOS and NMOS channel resistances need to be balanced in order to have a V_{gs} of $V_{DD}/2$, which was achieved by regulating the width of the channel of the transistors. Using Cadence 6 with the 130 nm CMOS technology these balanced values came out as W_N = 1.0 µm and W_P = 2.8 µm, and the minimum channel length $L_{N,P}$ = 120 nm, Figure 3.1, and its DC operating points for a V_{DD} = 1.2 V are shown in Figure 3.2. Every inverter, as well as other logic gates, used in this work has these values of channel length and width for PMOS and NMOS transistors.

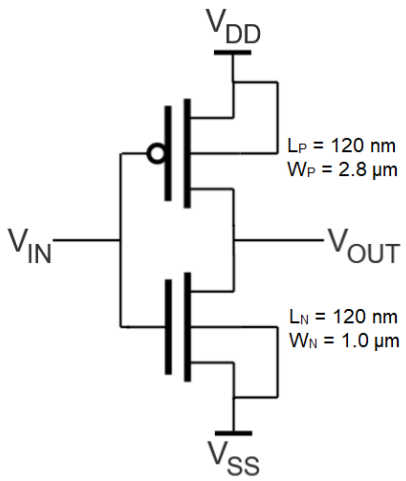


Figure 3.1 — Inverter schematic with channel sizes.

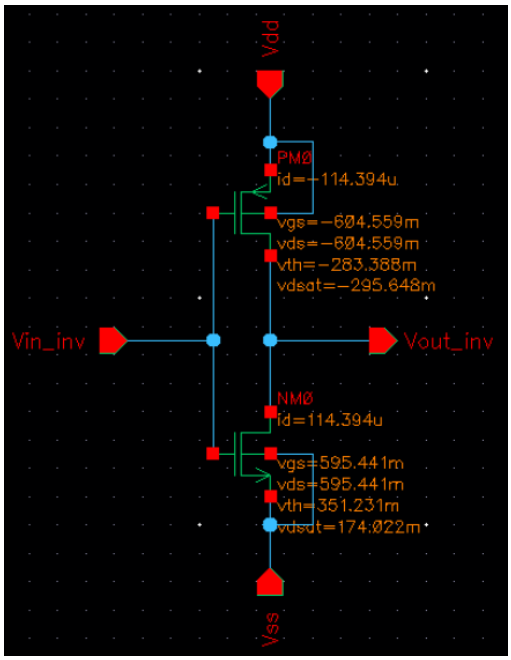


Figure 3.2 — Inverter schematic with DC Operating Points.

3.2.1 Simulations of Voltage Comparators

Starting with the comparators, no modifications were made to the designs in order to test them. The resulting specification values are presented in Table 3.1.

In the simulations of all the comparators that were studied, a frequency clock of 1.5 GHz, and a $V_{ref} = V_{DD}/2$ (600 mV) were used, with the exception of the NAND DVC which used a

V_{ref} = 900 mV due to the CM of the NAND3 gates being closer to V_{DD} where they generate the expected outputs [4] as previously discussed.

The topology that showed the overall best results was the SADLC, however, as previously discussed, this topology serves only as a reference to the others since it does not use standard-cells. This way, the OAI topology presented overall superior results relative to the other topologies and was used in the design of the comparator presented later in this thesis.

3.2.2 Electrical Simulations of OTAs

Regarding the amplifiers a few changes were made to some of the circuits concerning the CMFB and the frequency compensations.

In the MC-OTA, a 2nd order frequency compensation was necessary since this was a 2nd order amplifier, as depicted in Figure 2.13 a). This modification helped to increase the PM of the amplifier above the 45º minimum margin and remove the peaking in the amplifier's output. The CMFB of this amplifier was not tested and was instead replaced by an ideal voltage source of $V_{DD}/2$. The FFC-OTA was not simulated due to its increased complexity over the other topologies.

In Inverter 9 based single-stage amplifier (I9BSSA) every inverter used was in terms with the inverter presented in Figure 3.1.

The topology that showed the overall best results was the OTA 3 which presented the best DC Gain and power consumption of the three OTA tested. Even though OTA 3 did present a low UGBW compared to MC-OTA and lowest PM, it has the bigger FOM, as depicted in Table 3.2. Even though I9BSSA has the lowest FOM, it introduces an interesting approach as an inverter only OTA.

Table 3.1 — STUDIED COMPARATOR SPECIFICATIONS.

Comparator	[2]	[4]	[3]	[5]	[7]
Type	SADLC	RRDVC	NAND DVC	OAI	Inverter-based
CMOS [nm]	130	130	130	130	130
V_{DD} [V]	1.2	1.2 *	1.2	1.2	1.2
Delay [ns]	0.145	0.27	0.152 **	0.128	0.094
Power [µW]	344	1104	782 **	1125	1171
Static Input Offset [mV]	0.21	56	4 **	0.65	10.4
Random Offset [µV]	0.0057	84.27	71.87	14.57	320.85

* for V_{diff} = 0; ** for V_{ref} = 900 mV.

Table 3.2 — STUDIED AMPLIFIER SPECIFICATIONS.

Amplifier	[9]	[10]	[1]
Type	OTA inverter-based (OTA 3)	Miller-Compensated OTA	I9BSSA
CMOS [nm]	130	130	130
V_{DD} [V]	1.2	1.2	1.2
DC Gain [dB]	57	27	19
GBW [MHz]	569	1019	419
Phase Margin [°]	50	54	96
Output Swing [V]	1.260	1.192	1.260
Power [µW]	1370	3720	1538
C_L [pF]	1	1	1
FOM [GBW*C_L/Power] [MHz*pF/mW]	415	274	272

4

Proposed Topologies of a Comparator and an Amplifier

Keeping in mind the advantages, limitations, and simplicity of each topology, as well as the simulated results, a standard-cell based comparator and amplifier are proposed.

Considering the results discussed in chapter 3, two topologies for general purpose amplifier and comparator were chosen. The OAI for the comparator and, for the amplifier, the OTA in Figure 2.17 with the CMFB from Figure 2.11.

4.1 OR-AND-Inverter-based Comparator with Two Inputs

The chosen comparator was based on the OAI-based comparator by [5] with two of the four OAI groups removed in order to have two inputs and two outputs, Figure 4.1. This not only significantly decreases the layout area and P_D as well as slightly improves the comparator's specifications, as seen in Table 5.1, maintaining the advantages of the OAI-based topology from the voltage comparator studied in chapter 2.1.2.

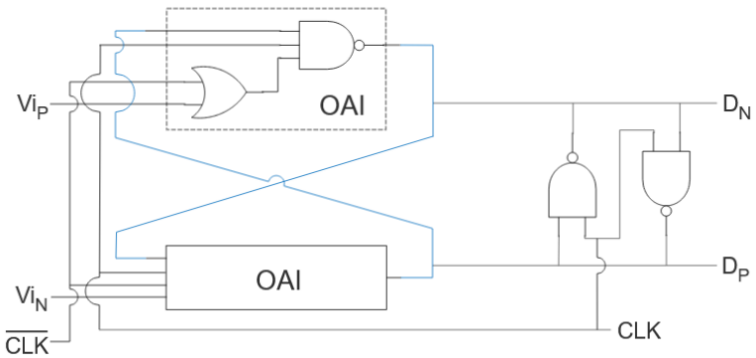


Figure 4.1 — Proposed OAI-based comparator with two inputs.

As previously mentioned, a NAND-based comparator can be roughly be interpreted as a latch in series with a preamplifier. [5] This design, in relation to the original in [5], does not

have the two V_{ref} inputs, however it works just like the original design with the same advantages of the OAI design over the NAND-based. The cross-coupled OAI nets compare V_{iP} with V_{iN} and the latch improves the gain of the comparison and later resets the outputs.

4.2 Single-Path Three-Stage Inverter-based OTA

The chosen amplifier was the Single-Path Three-Stage Inverter-based (SP3SIB) OTA from [11] with the CMFB loop from [9], Figure 4.2.

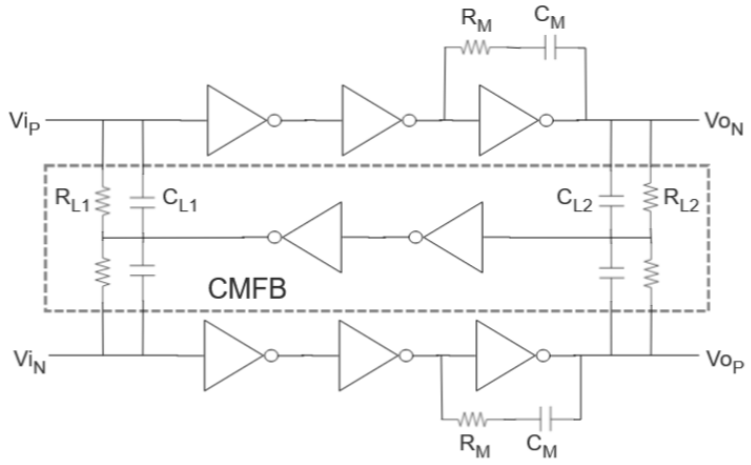


Figure 4.2 — Single-Path Three-Stage Inverter-based OTA with active CMFB.

The circuit proposed by [11], the SP3SIB OTA, presented a similarity to the OTA 3 proposed by [9] but without the high-speed path, and with SC both in the CMFB loop and the main stage. The SCs were not included in the simulations due to only requiring CT amplifiers in this work, as well as the CMFB. This way, only the three inverters and the 2nd order miller compensation were maintained from the circuit proposed by [11] and combined with the CMFB of [9].

The SP3SIB OTA was tested with and without the active CMFB of [9], Figure 4.2 and Figure 4.3 respectively, for the purposes of analyzing the impact the CMFB had in the AC analysis.

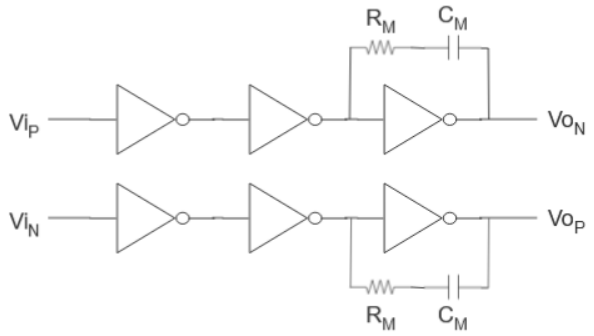


Figure 4.3 — Single-Path Three-Stage Inverter-based OTA without CMFB.

However, since this is a pseudo-differential topology, the outputs need to be maintained in the V_{CM} for them to not jump to either of the rails (V_{DD} or ground), so the chosen topology was the SP3SIB OTA with CMFB, Figure 4.2.

4.2.1 Common-Mode Feedback Loop (CMFB)

In order to fix the DC output of the amplifier in the desired level, a CMFB was added.

The passive component values were obtained through trial and error using typical values for these circuits, which were then adjusted.

The resistors cannot be too small, so the gain is not lost, or too large due to the high silicon area, which impacts costs. This way the values of the resistors are found in the k or dozens of k .

For the capacitors, these cannot have values larger than C_L value of the amplifier, 1 pF.

At the input of the amplifier the small resistors were added as well as the larger capacitors, and in the output the larger resistors and small capacitors were added in order to barely load the amplifier.

The values used for the resistors and capacitors were 20 k and 1 pF at the input, and 50 k and 100 fF at the output.

These values result in a good stability for the proposed amplifier, as depicted in Figure 5.8.

4.2.2 Theoretical Analysis for the Amplifier

In this chapter the theoretical analysis of the proposed amplifier is presented.

The equations and specifications that characterize the amplifier and its behavior are described below.

4.2.2.1 Circuit equations

The design of the proposed amplifier was studied considering various approximations in order to make its expressions less complex; however, this presented some error in the numeric results of each of its specifications.

For the theoretical analysis, only the pseudo-differential structure was studied, as the CMFB serves as to maintain the outputs from jumping to either of the rails, as previously explained. This CMFB circuit will create slight differences in the specifications of the amplifier.

These approximations consisted of analyzing a version of the amplifier only consisting of one of the cascaded inverters networks and ignoring the parasitic capacitance C_{gd}. Since this amplifier has a pseudo-differential structure, the former approximation has no impact on the expressions other than halving its gain and power consumption, while the latter simplifies all the expressions because the capacitance C_{gd} creates various feedback networks in the inverters resulting in high frequency zeros far over the UGBW frequency, therefore not being an

issue. This latter approximation does present some error in the numeric results but immensely simplifies the analysis of the amplifier.

Since this OTA consists of inverters, for the simplicity of the expressions, the following considerations will apply:

- $gm = gm_N + gm_P$
- $g = gds_N + gds_P$
- $C_{1,2} = C_{db_{1,2}} + C_{gs_{2,3}}$
- $C_3 = C_{db_3} + C_L$

The following expressions were obtained with the use of the software wxMaxima.

A. DC Gain

For this topology the DC Gain is the product of the gain of each of the cascaded inverters of one network then doubled because of the remaining inverter network:

$$A_{DC} = -2 * \frac{gm_1 * gm_2 * gm_3}{g_1 * g_2 * g_3} \quad (2)$$

B. Poles

This topology has four poles, one at the output of each of the inverters (p_1 after Inv_1, p_2 after Inv_2, and p_4 after Inv_3), and a low frequency pole, p_3, at the input of the last inverter caused by the feedback of the Miller compensation.

For the poles p_3 and p_4 the resistor R_M was not considered, and the channel admittances g_3 and g_2 were also not considered for the poles p_3 and p_4, respectively.

The expression of poles p_1 and p_2 are the following:

$$p_1 = \frac{g_1}{2\pi * C_1}\ [Hz]\ ;\ p_2 = \frac{g_2}{2\pi * C_2}\ [\text{Hz}] \quad (3)$$

For the pole p_3, considering $fp_3 << fp_4$ --> ($g_3 << sC_3$), therefore g_3 was not considered:

$$p_3 = -\frac{g_2}{2\pi * \left(C_M * \left(\frac{gm_3}{g_3} + 1\right) + C_2\right)}\ [\text{Hz}] \quad (4)$$

For the pole p_4, considering $fp_4 >> fp_3$ --> ($g_2 << sC_2$), therefore g_2 was not considered:

$$p_4 = \frac{-C_M * gm_3 - (C_M + C_2) * g_3}{2\pi * (C_M * (C_3 + C_2) + C_2 * C_3)}\ [\text{Hz}] \quad (5)$$

C. Zeroes

Since the C_{gd} of each transistor was not considered the zeros created by each of those parasitic capacitances were also not considered. This decision did not present an issue since these are high frequency zeroes located far over the UGBW frequency.

The only zero that was considered was the one created by C_M and has the following expression:

$$z = -\frac{gm_3}{2\pi * (C_M * R_M * gm_3 - C_M)} \text{ [Hz]} \quad (6)$$

D. Gain-Bandwidth Product

The resulting expression of A. GBW was obtained by multiplying the expression of the DC Gain and the expression of the lowest frequency pole (p_3):

$$\text{GBW} = -\frac{1}{2\pi} * \frac{2 * gm_1 * gm_2 * gm_3}{g_1 * g_3 * \left(C_M * \left(\frac{gm_3}{g_3} + 1\right) + C_2\right)} \text{ [Hz]} \quad (7)$$

E. Power Consumption

For this topology the expression for the power is obtained by the sum of current of each inverter (I_D) times V_{DD}. Theoretically, since the six inverters are equal so will their currents:

$$P_D = V_{DD} * (6 * I_D) \text{ [W]} \quad (8)$$

F. Output Swing

The OS is given by the expression:

$$\text{OS} = 2 * (V_{DD} - V_{DSat_P} - V_{DSat_N} - 0.1) \text{ [V]} \quad (9)$$

Here the 100 mV were given as a high possible margin of error and the doubling is because of the differential structure.

G. FOM

The FOM used is:

$$\text{FOM} = \text{GBW} * \frac{C_L}{P_D} \quad (10)$$

4.2.2.2 Physical parameters and specifications

The following values are the simulated physical parameters of the transistors, obtained in Cadence 6 with the 130 nm technology. These values were obtained through the DC simulation described in chapter 3.1.2.1.

- I_D: $114.394E-6\ [A]$
- V_{DSat_P}: $295.648E-3\ [V]$
- V_{DSat_N}: $174.022E-3\ [V]$

- gm_P: $593.052E-6\ [S]$
- gm_N: $664.265E-6\ [S]$
- gds_P: $72.4646E-6\ [S]$
- gds_N: $61.5862E-6\ [S]$

- gm_{P3}: $593.549E-6\ [S]$
- gm_{N3}: $663.902E-6\ [S]$
- gds_{P3}: $72.3831E-6\ [S]$
- gds_{N3}: $61.7217E-6\ [S]$

- C_{db_N}: $326.224E-18\ [F]$
- C_{db_P}: $1.37214E-15\ [F]$
- C_{gd_N}: $267.531E-18\ [F]$
- C_{gd_P}: $772.293E-18\ [F]$
- C_{gs_N}: $901.125E-18\ [F]$
- C_{gs_P}: $2.70095E-15\ [F]$
- $C_{db} = C_{db_N} + C_{db_P} = 1.698364E-15\ [F]$
- $C_{gd} = C_{gd_N} + C_{gd_P} = 1.039824E-15\ [F]$
- $C_{gs} = C_{gs_N} + C_{gs_P} = 3.602075E-15\ [F]$

- $C_{db_{N3}}$: $326.736E-18\ [F]$
- $C_{db_{P3}}$: $1.37018E-15\ [F]$
- $C_{gs_{N3}}$: $901.217E-18\ [F]$
- $C_{gs_{P3}}$: $2.70072E-15\ [F]$
- $C_{db_3} = C_{db_{N3}} + C_{db_{P3}} = 1.696916E-15\ [F]$
- $C_{gs_3} = C_{gs_{N3}} + C_{gs_{P3}} = 3.601937E-15\ [F]$

- R_M: $1.26E+3\ [\Omega]$
- C_M: $1.4E-12\ [F]$
- C_L: $1.0E-12\ [F]$

- $gm_1 = gm_2 = gm_N + gm_P = 1.257317E-3\ [S]$
- $gm_3 = 1.257451E-3\ [S]$
- $g_1 = g_2 = gds_N + gds_P = 1.340508E-4\ [S]$
- $g_3 = 1.341048E-4\ [S]$
- $C_1 = C_{db} + C_{gs} = 5.300439E-15\ [F]$
- $C_2 = C_{db} + C_{gs_3} = 5.300301E-15\ [F]$
- $C_3 = C_{db_3} + C_L = 1.001696916E-12\ [F]$

Replacing the previous values in the equations (2) to (10), will give the expected theoretical approximate values for the amplifier specifications:

$$A_{DC} = -2 * 824.892 \rightarrow 20 * log(2 * 824.893) = 64.35 \text{ dB}$$

$$p1 = 4.027 \text{ [GHz]}$$
$$p2 = 4.027 \text{ [GHz]}$$
$$p3 = 1.468 \text{ [MHz]}$$
$$p4 = 0.219 \text{ [GHz]}$$
$$z = 0.244 \text{ [GHz]}$$
$$\text{GBW} = 2.423 \text{ [GHz]}$$
$$P_D = 823.679 \text{ [}\mu W\text{]}$$
$$\text{OS} = 1.260 \text{ [V]}$$
$$\text{FOM} = 2944 \text{ [MHz} * \frac{\text{pF}}{\text{mW}}\text{]}$$

These values are theoretical and due to some error accounted for the previously mentioned approximations the simulated values will differ.

5

Simulation Results and Discussion

5.1 Simulation Results

In this chapter are presented the simulation results for the proposed voltage comparator, OTA, and ΣΔ modulator. The discussion of the results is presented in chapter 5.2.

5.1.1 Voltage Comparator

For the comparator, the tests referred in chapter 3.1.1 were made.

For every simulation figure shown in this chapter, the graphics present in red the varying input voltage, in yellow the reference input voltage, in green the sampling clock input, in light blue the non-inverting output, and in dark blue the inverting output of the comparator.

5.1.1.1 Behavior and power dissipation

The behavioral test is depicted in Figure 5.1, where the outputs, in blue, change in the moment both input voltages, yellow and red, cross each other, which shows the comparator is working as expected.

The RMS current obtained from the voltage source was 741.7 µA which resulted in a power dissipation of 890 µW.

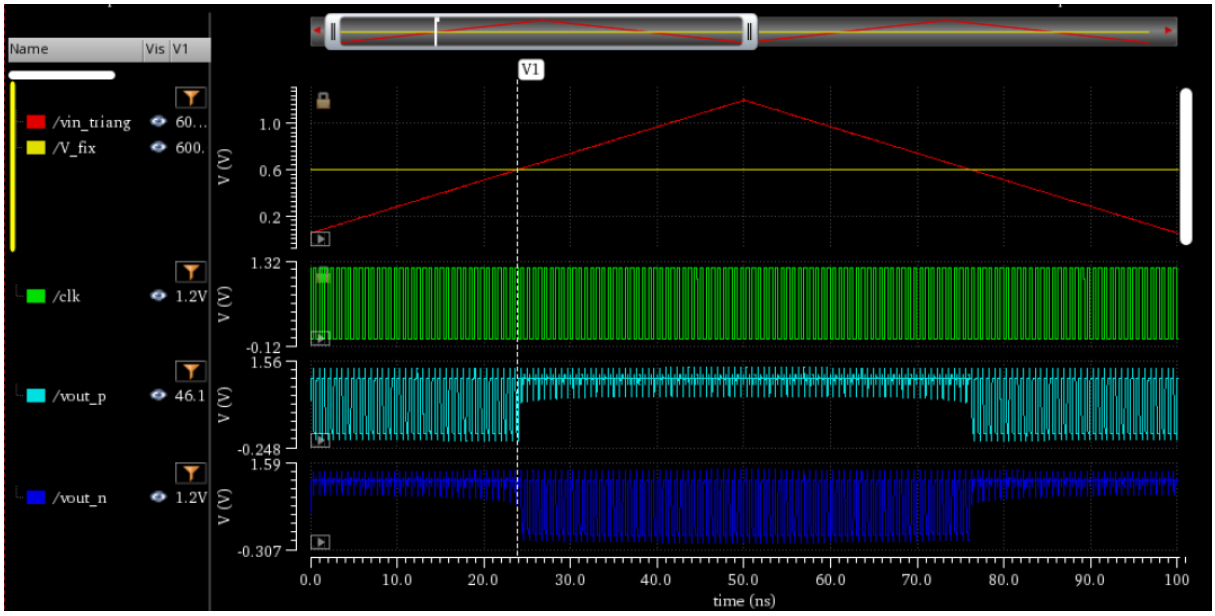


Figure 5.1 — Behavioral test of the OAI2 comparator.

5.1.1.2 Input Offset

The static input offset simulation is depicted in Figure 5.2 where the two values for the average are obtained by marking the moment the output of the comparator changes and verifying the varying input values, in red, relative to the reference input voltage, in yellow. The two static offset values are 587.8 mV and 594.4 mV. This results in a static offset of:

$$StaticOffset = \frac{0.5878 + 0.5944}{2} = 0.591\ mV$$

The random offset was calculated by a Monte-Carlo simulation as referred in section 3.1.1.2.

The resulting standard deviation value for this comparator was 10.42 µV.

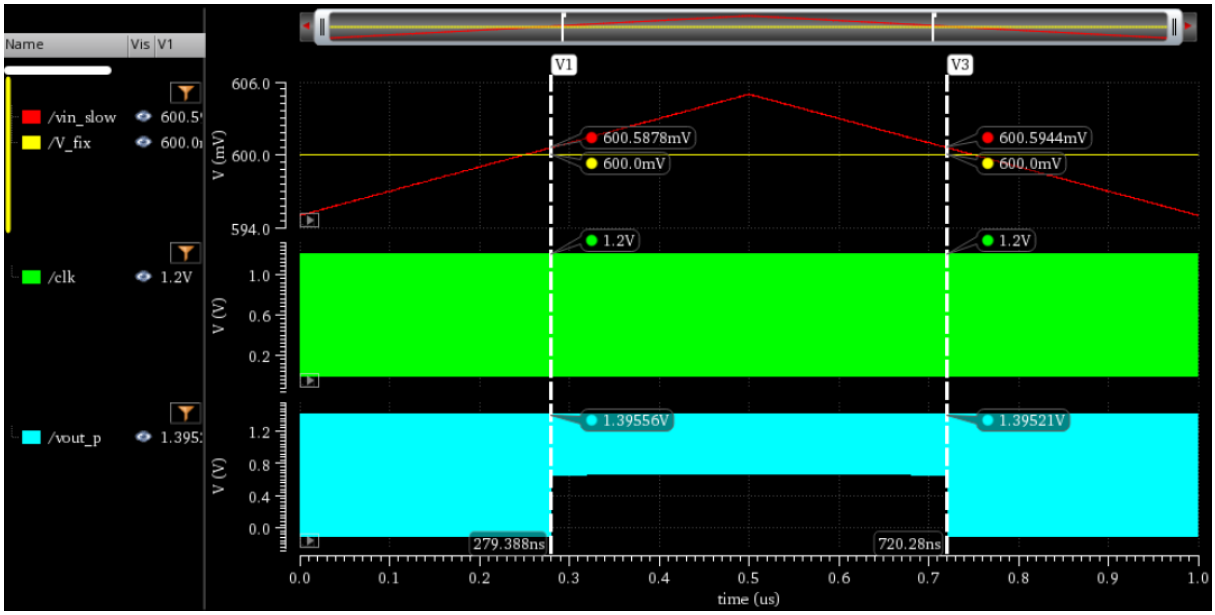


Figure 5.2 — Static Offset test of the OAI2 comparator.

5.1.1.3 Comparison time

The comparison time test is depicted in Figure 5.3 and more detailed in Figure 5.4. The latter, Figure 5.4, shows an augmented representation of the comparison time for the proposed comparator where the comparison time is larger, which is where the varying input voltage, in red, is closer to the reference voltage, in yellow.

The obtained value of this test is presented in the bottom value of Figure 5.4, for 108.59 ps in comparison time.

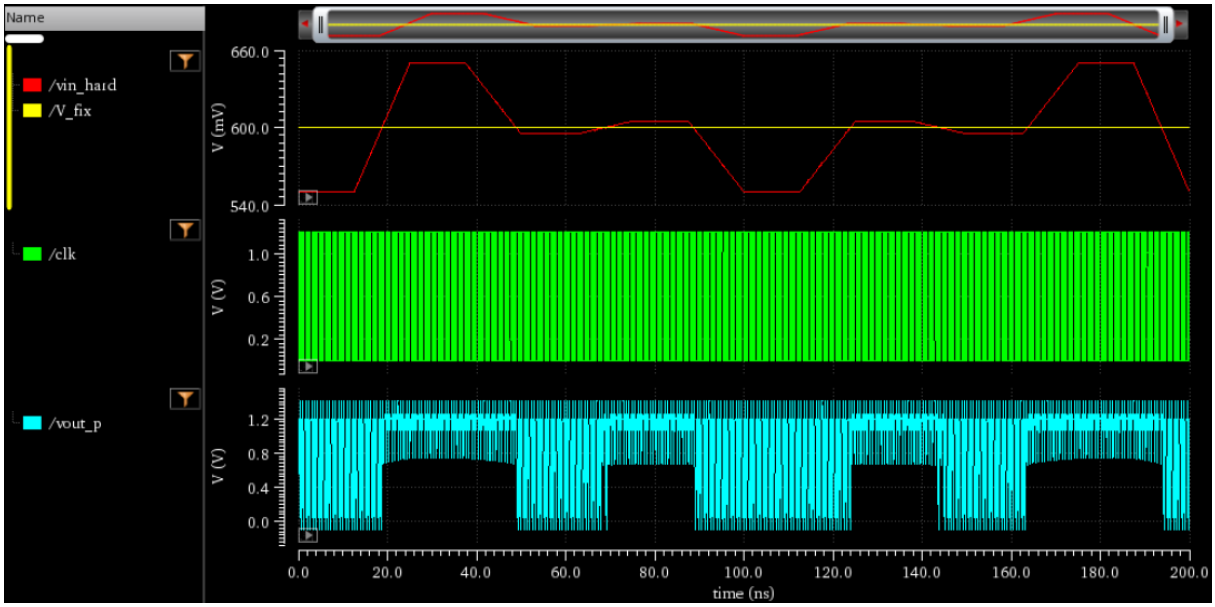


Figure 5.3 — Comparison time test of the OAI2 comparator.

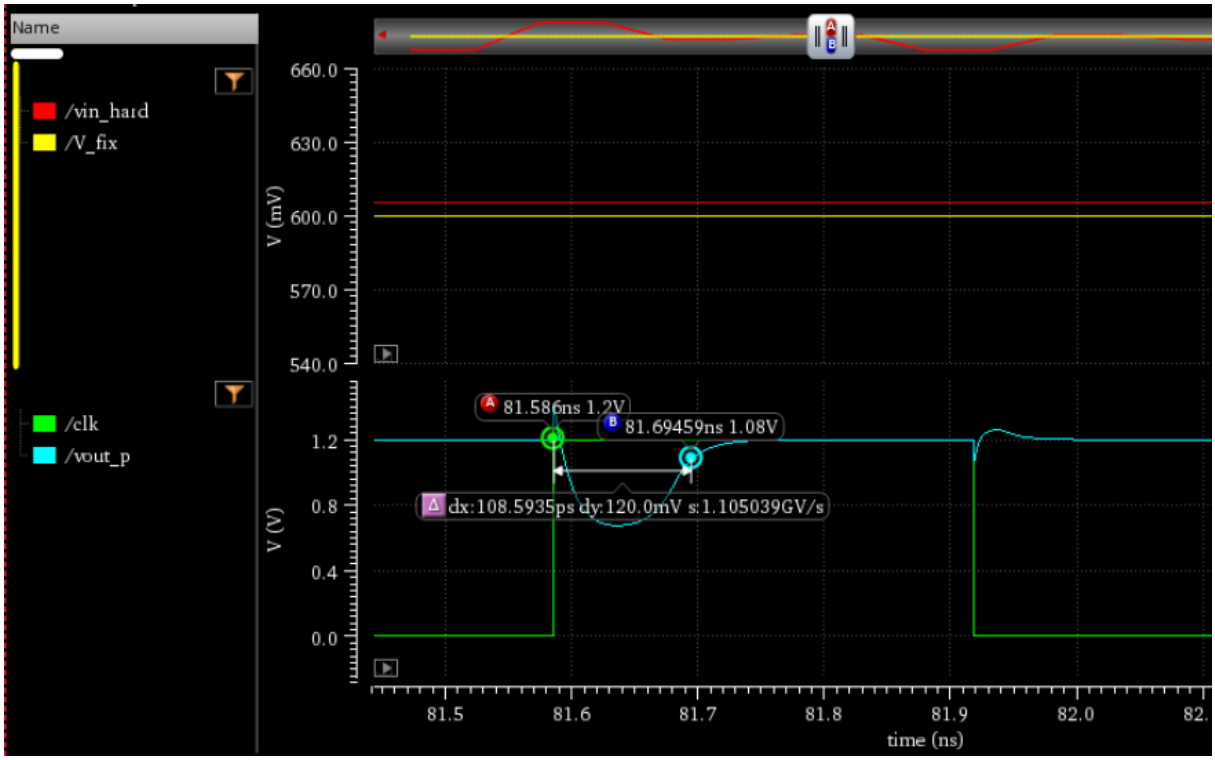


Figure 5.4 — Augmented representation of the comparison time value of the OAI 2 comparator.

The obtained performance results and specifications of the comparator are presented in the following table.

Table 5.1 — PROPOSED COMPARATOR SPECIFICATIONS.

Comparator	This work
Type	OAI 2 inputs
CMOS [nm]	130
V_{DD} [V]	1.2
Delay [ns]	0.109
Power [µW]	890
Static Input Offset [mV]	0.591
Random Offset [µV]	10.42

5.1.2 Operational Transconductance Amplifier

5.1.2.1 AC analysis

As previously mentioned the inverters have the channel dimensions of $L_{N,P}$ = 120 nm, W_N = 1.0 µm and W_P = 2.8 µm.

The dimensions of the frequency compensation components, R_M and C_M, of the feedback loop in the third Inverter were obtained through the simulation of various component values, Figure 5.5.

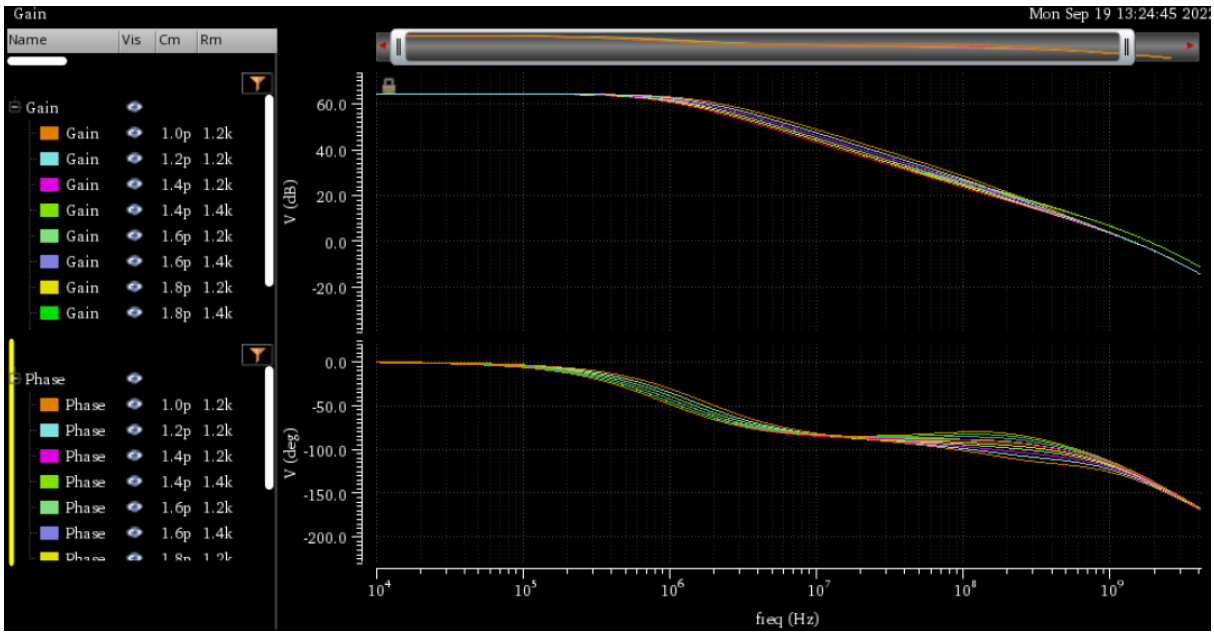


Figure 5.5 — Simulation of SP3SIB OTA for various values of C_M and R_M.

Considering a balance between a PM > 45º and a larger GBW, and to try and cancel the zero created by C_M in the RHP, the value of $R_M = 1/gm3$, the resulting values were R_M = 1.26 k and C_M = 1.4 pF, which resulted in the behavior represented in the AC analysis, Figure 5.6, where the DC Gain is presented on the top in red, and the phase on the bottom in green.

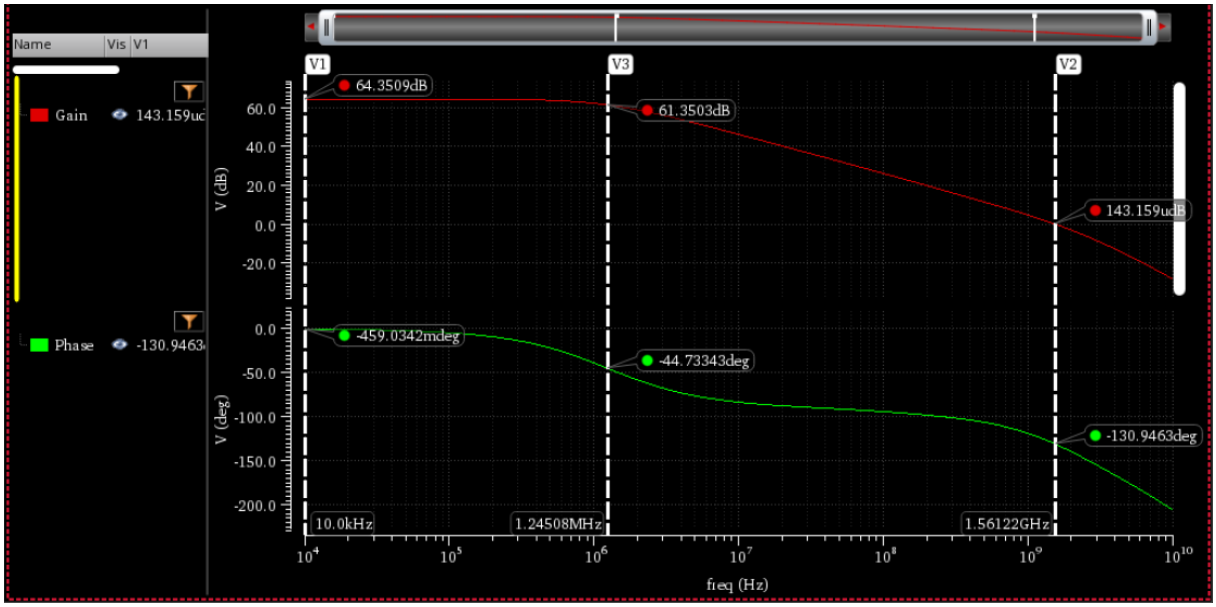


Figure 5.6 — AC simulation of SP3SIB OTA for R_M = 1.26 k and C_M = 1.4 pF.

This topology offered a 64 dB DC Gain, with a 1.561 GHz of GBW and 49º of PM which resulted in an FOM of 1894, in accordance with the expression (10).

After applying the CMFB loop to this amplifier, the resulting AC behavior slightly changed, Figure 5.7, with the DC Gain depicted on top in red, and the phase on bottom, in green.

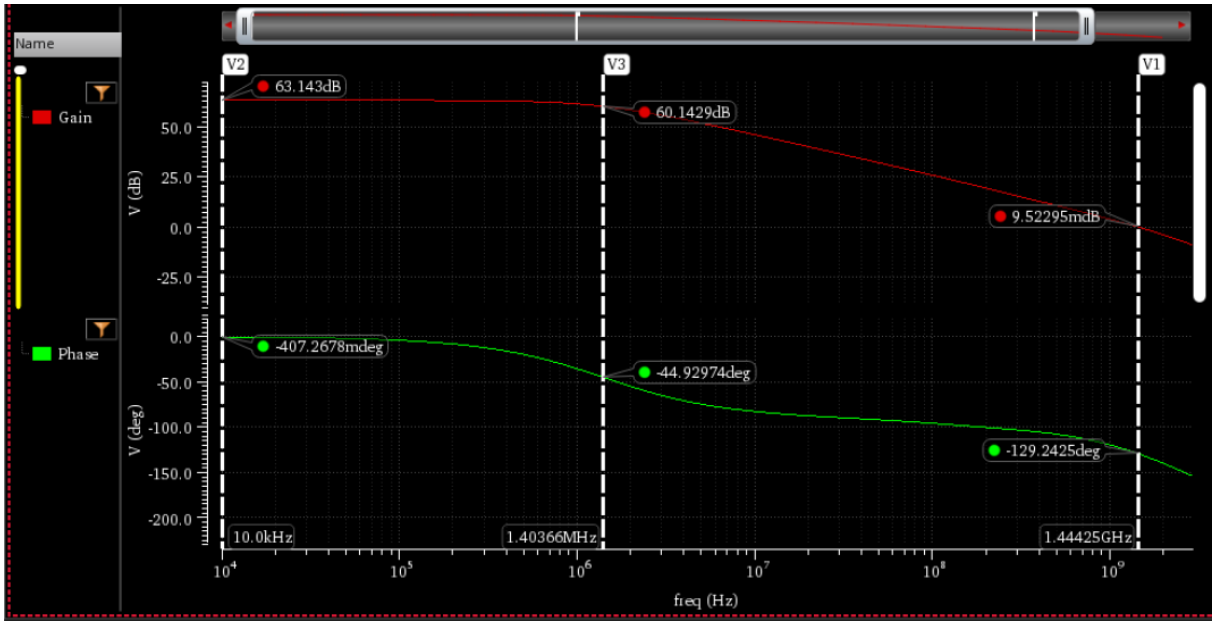


Figure 5.7 — AC simulation of the SP3SIB OTA with CMFB for R_M = 1.26 k and C_M = 1.4 pF.

This CMFB loop slightly decreased the DC Gain by roughly 1 dB, resulting in 63 dB of DC Gain, higher frequency for p3 as 1.403 MHz, a decreased the GBW frequency of 1.444 GHz, and an increased PM of 51º.

5.1.2.2 Settling-time

A transient simulation with an input step with an amplitude of 100 mV_{diff} was run, Figure 5.8, where the input signal is the step presented in red and the output is presented in green.

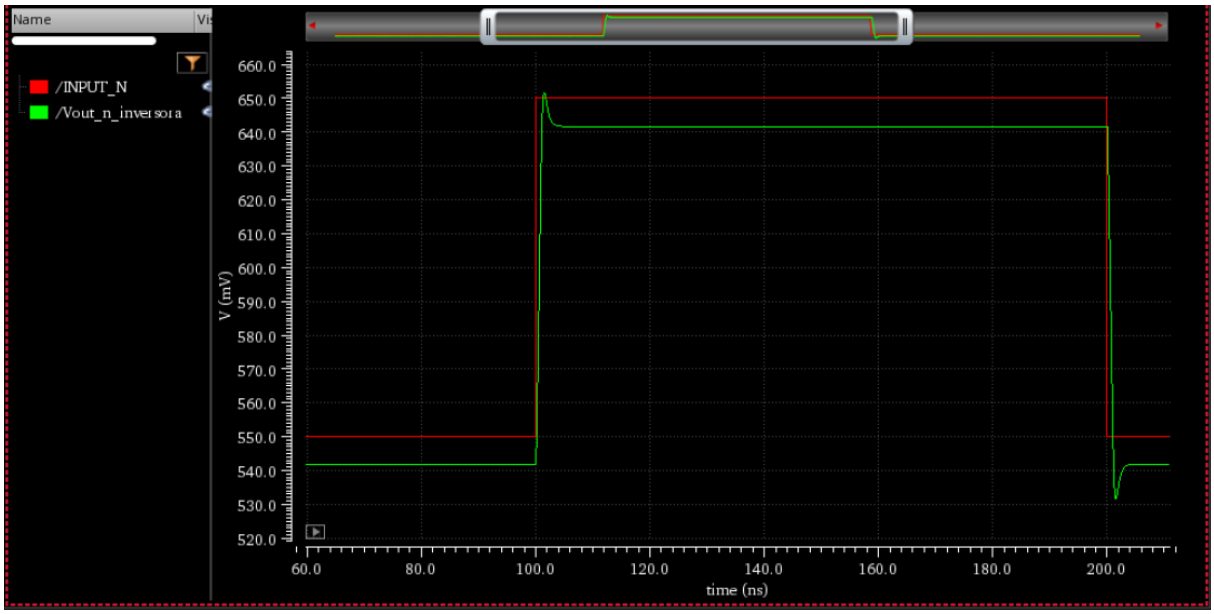


Figure 5.8 — Transient step simulation of the SP3SIB OTA, V_{IN} = 100 mV_{diff}.

The amplifier showed good response to the input signal with a small overshoot due to its 50º PM. The slight offset that can be seen in Figure 5.8 did not present an issue since it can be compensated if necessary.

The settling-time was calculated from the beginning of the input step until the output measured at a value of 0.1% of the input step high value (50 mV), as depicted in Figure 5.9. The amplifier presented a settling-time of 3.24 ns.

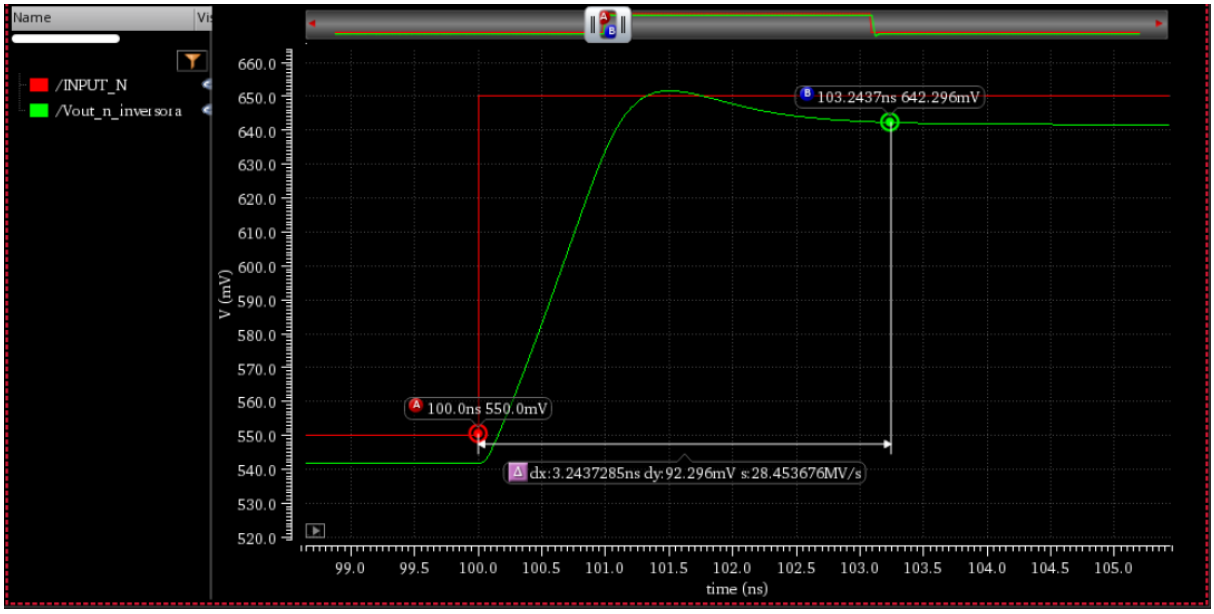


Figure 5.9 — Settling time of the SP3SIB OTA, V_{IN} = 100 mV_{diff}.

5.1.2.3 Slew-Rate

The positive and negative slew rates are depicted in Figure 5.10 and Figure 5.11, respectively, where the input signal is the step presented in red and the output is presented in green.

In Figure 5.10, the positive slew rate is presented in the third value, as 123.6686 MV/s, or 123.6686 V/µs.

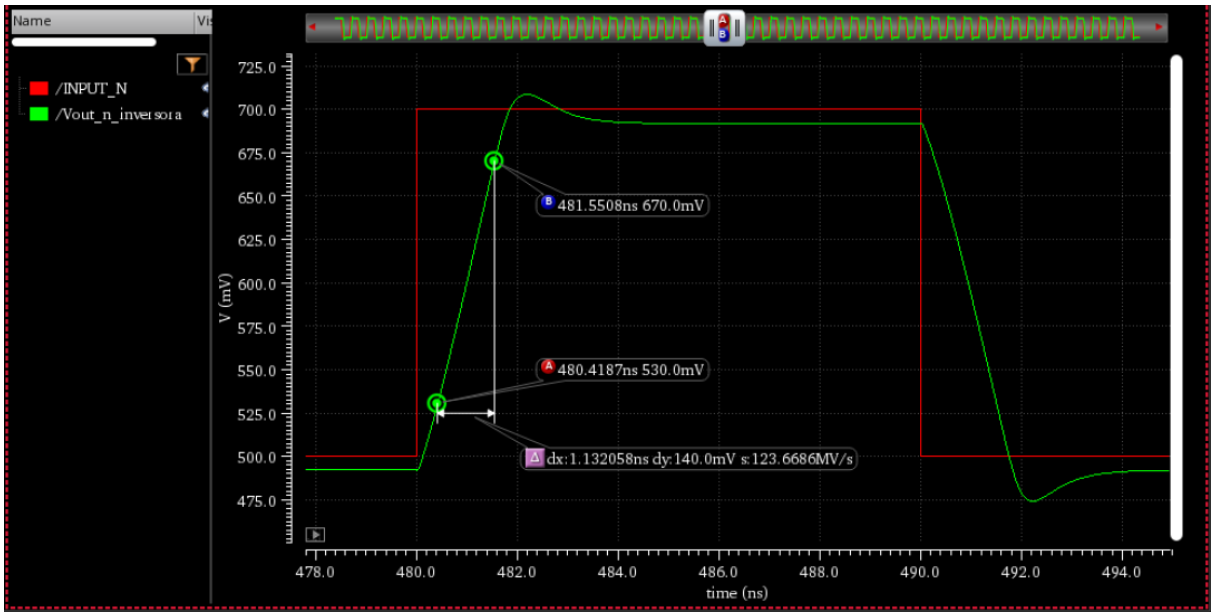


Figure 5.10 — Positive slew rate of the SP3SIB OTA.

In Figure 5.11, the negative slew-rate is presented in the third value, as 115.0247 MV/s, or 115.0247 V/µs.

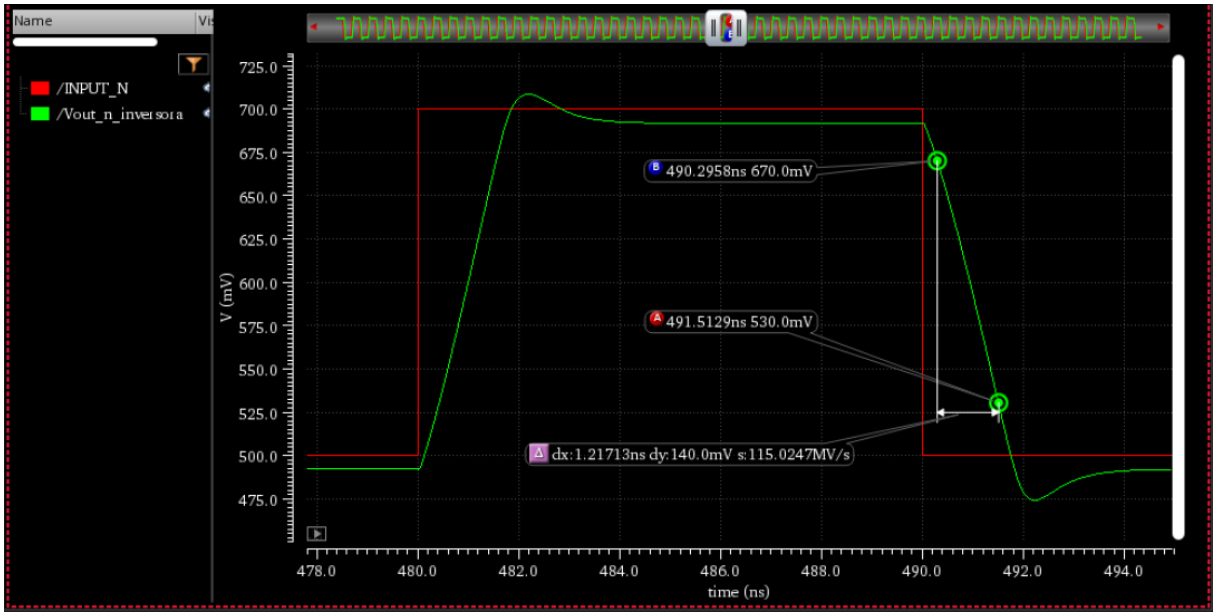


Figure 5.11 — Negative slew rate of the SP3SIB OTA.

The resulting values are the following:

- SR_+ = 123.6686 V/µs
- SR- = 115.0247 V/µs

and resulting in an average slew rate of:

- SR_{avg} = 119.35 V/µs

5.1.2.4 AC Noise

As previously stated in chapter 3.1.2.5, an AC noise simulation was run between the frequencies of 1 Hz and 10 GHz where the noise PSD of the input referred noise is plotted, Figure 5.12. Then, in order to just determine the thermal noise, the noise PSD was integrated between the frequencies of 1 MHz and 2 GHz to avoid the flicker noise.

The result of the integration was 633.4 nV^2 which, after making the square root of the value, ended with 795.9 µV of input referred thermal noise.

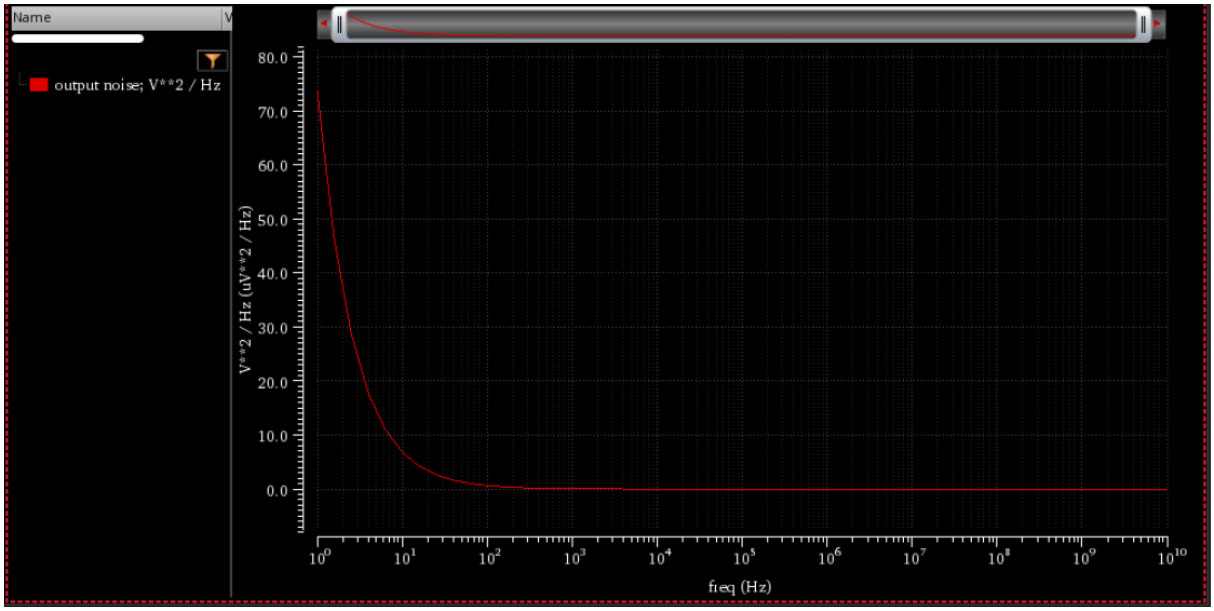


Figure 5.12 — Plot of the PSD of the SP3SIB OTA.

Table 5.2 presents the resulting specifications of the proposed amplifier.

Table 5.2 — PROPOSED AMPLIFIER SPECIFICATIONS.

Amplifier	This work	This work
Type	SP3SIB OTA w/ active CMFB	SP3SIB OTA wo/ active CMFB
CMOS [nm]	130	130
V_{DD} [V]	1.2	1.2
DC Gain [dB]	63	64
GBW [MHz]	1444	1561
Phase Margin [°]	51	49
Output Swing [V]	1.260	1.260
Power [µW]	1098	824
C_L [pF]	1	1
AC Noise [µV]	795.9	N/A
FOM [GBW*C_L/Power] [MHz*pF/mW]	1364	1894

N/A – not avaliable.

5.1.3 Sigma-Delta Modulator

As stated previously, the modulator in [17] offered good performance while having a low power dissipation due to its opamp-less topology, which revealed it to be an interesting option to work with and improve. So, the comparator in this topology was replaced for the one proposed in chapter 4.1.

The ideal capacitors replaced the MOSCAPs, just like the topology in [18], with the same capacitance value as the original sizing. The inverters in the feedback loop are the same as presented in 3.2. Regarding the comparator, unlike the one used in [17] which is not made from standard logic gates and contains a flip-flop from [19], the comparator from chapter 4.1 did not contain an edge-triggered flip-flop, therefore one from [20] was added after the comparator.

All the parameters used, as well as component values and input signals, were the same as in the literature ([17]), except that the supply voltage was set to 1.2 V, as described in 3.1.3.

A behavioral example of the resulting transient response simulation is depicted in Figure 5.13, in this case with an input signal amplitude of 220 mV_{diff}. Here, are presented in a small sample, from top to bottom: the sampling clock of the comparator in yellow, the inverting and non-inverting input voltages in red and blue, respectively, the output of the flip-flop in white, the input of the flip-flop (output of the comparator) in green, and the flip-flop sampling clock in purple.

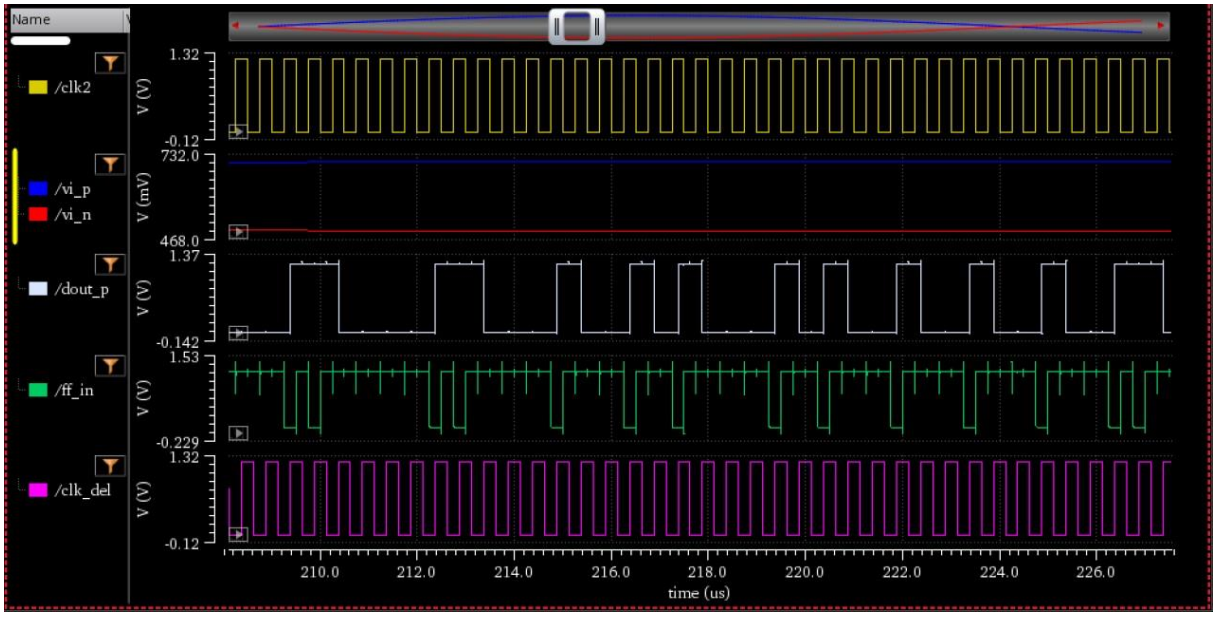


Figure 5.13 — Transient response simulation of the modulator for V_{diff} = 220 mV.

Without transient noise

The FFT of the ΣΔ modulator for an input signal amplitude of 220 mV_{diff} and with a reference of $V_{DD}/2$ can be seen in Figure 5.14. It presents a 40 dB/dec slope, as characteristic of the 2nd order modulators, and presents a calculated SNDR of 68.02 dB.

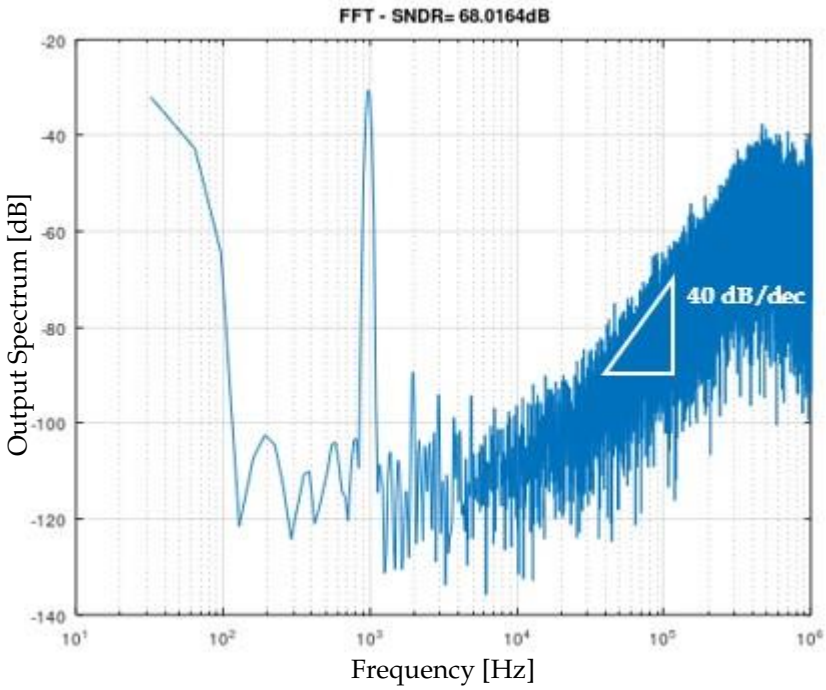


Figure 5.14 — FFT of the modulator for an input amplitude of V_{diff} = 220 mV.

To find the ERBW of the ΣΔ modulator, the modulator was tested for input signal frequencies increasing from 1.5 kHz. The SNDR of the modulator dropped around 3 dB from 68 dB at the 2.5 kHz input signal frequency, as depicted in Figure 5.15, resulting in a ERBW of 2.5 kHz.

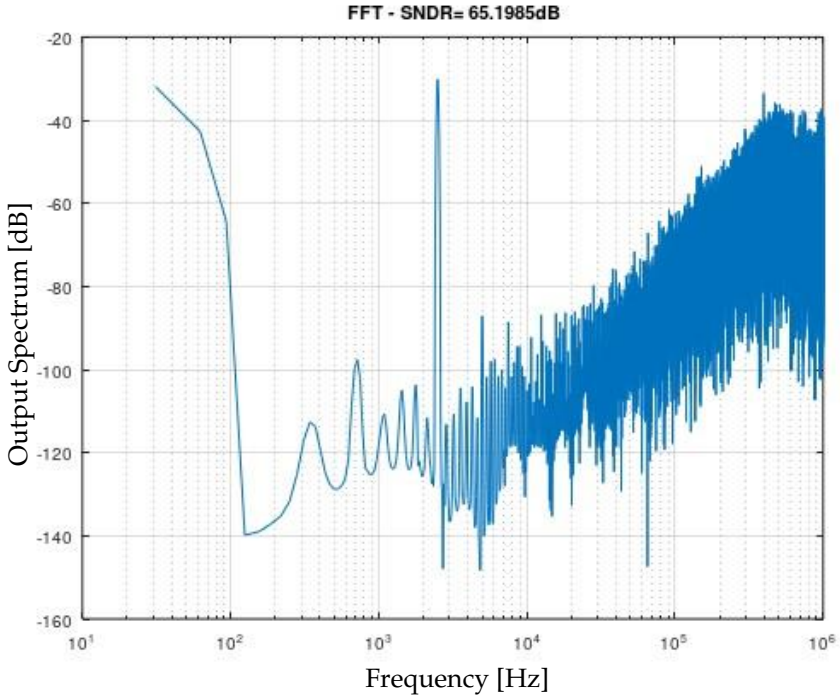


Figure 5.15 — FFT of the modulator for an input amplitude of V_{diff} = 220 mV with 2.5 kHz input frequency.

For the purpose of calculating the DR of the ΣΔ modulator, other differential input voltages were simulated. The modulator achieved around 0 dB of SNDR with a differential input of V_{diff} = 1 µV (-120.00 dBV), Figure 5.16, and until V_{diff} = 800 mV (-1.94 dBV), Figure 5.17, where beyond that amplitude the resulting FFT of the modulator no longer resembled the usual noise shape of 40 dB/dec, as can be observed with a V_{diff} = 890 mV (-1.01 dBV), Figure 5.18, resulting in a DR of 118 dB, Figure 5.22.

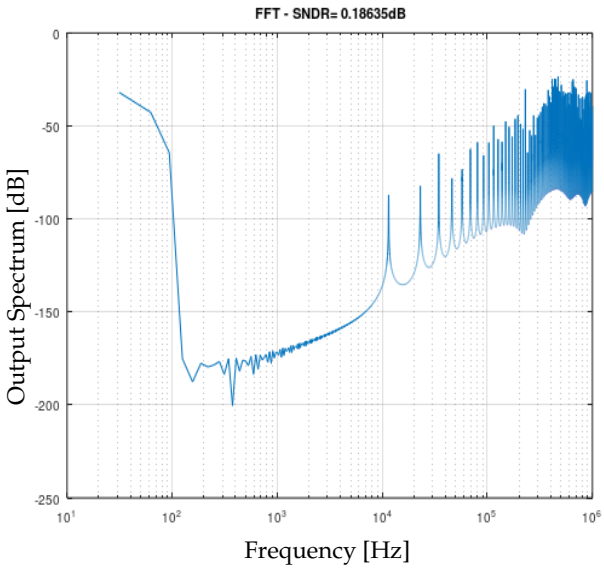


Figure 5.16 — FFT of the modulator for an input amplitude of V_{diff} = 1 µV.

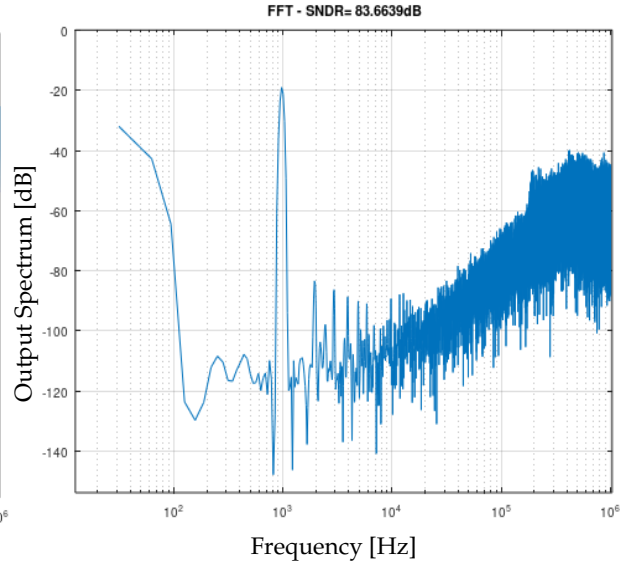


Figure 5.17 — FFT of the modulator for an input amplitude of V_{diff} = 800 mV.

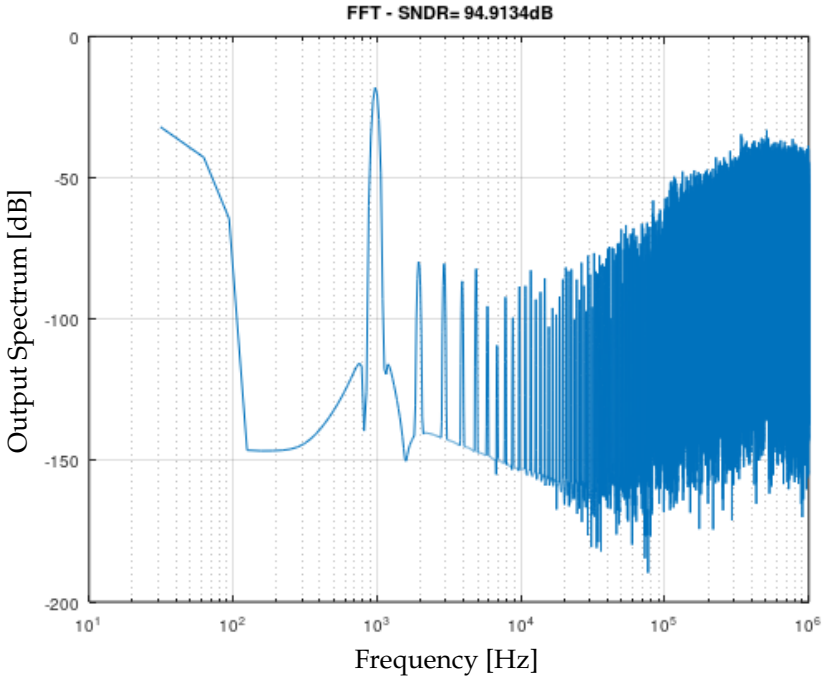


Figure 5.18 — FFT of the modulator for an input amplitude of V_{diff} = 890 mV.

The peak SNDR value of the ΣΔ modulator is 83.66 dB and was achieved with an input signal voltage of V_{diff} = 800 mV, as presented in Figure 5.22. This SNDR, using expression (11), corresponds to an ENOB of 13.60, meaning this modulator has a resolution of just over 13 bits.

$$ENOB = (SNDR - 1.76)/6.02 \quad (11)$$

The ΣΔ modulator tested for a power dissipation of 136.8 μW.

The FOMs of the modulator were calculated in accordance with the expressions (12) and (13).

$$\mathrm{FOM}_1 = DR + 10 * log\frac{BW}{P}\ [\mathrm{dB}] \quad (12)$$

$$\mathrm{FOM}_2 = \frac{P}{2 * BW * 2^{\mathrm{ENOB}}}\left[\frac{fJ}{Conv.-step}\right] \quad (13)$$

Resulting in the FOMs with the following values:

- $\mathrm{FOM}_1 = 191$ [dB]
- $\mathrm{FOM}_2 = 2196\ \left[\frac{fJ}{Conv.-step}\right]$

<u>With transient noise</u>

Regarding the simulations with transient noise, the resulting FFT for an input signal of V_{diff} = 220 mV are depicted in Figure 5.19 and present an SNDR of 58.3 dB.

The peak SNDR value of the modulator including transient noise is 69.82 dB and was achieved with an input signal voltage of V_{diff} = 900 mV, as presented in Figure 5.22. This SNDR, using expression (11), represents an ENOB of 11.306, meaning this modulator has a resolution of just over 11 bits.

As for the DR of the modulator when transient noise is present, the modulator achieved around 0 dB of SNDR with a differential input of V_{diff} = 100 μV (-80.00 dBV), Figure 5.20, and until V_{diff} = 900 mV (-0.92 dBV), Figure 5.21, for the same reason that was specified previously when no transient noise was present, resulting in a DR of 79 dB for the modulator when transient noise is present, Figure 5.22.

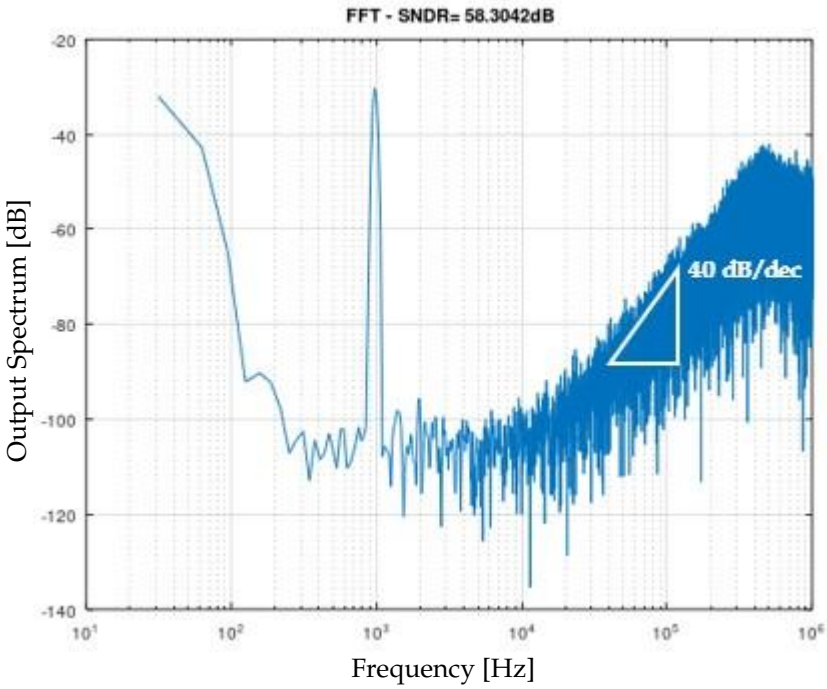


Figure 5.19 — FFT of the modulator for an input amplitude of V_{diff} = 220 mV with transient noise.

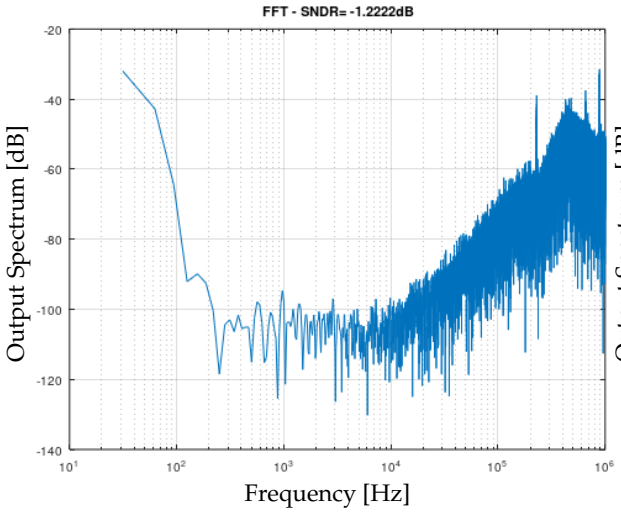


Figure 5.20 — FFT of the modulator for an input amplitude of V_{diff} = 100 µV with transient noise.

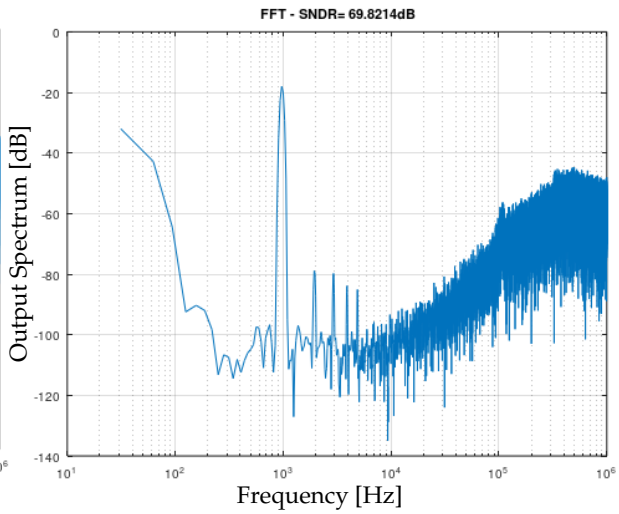


Figure 5.21 — FFT of the modulator for an input amplitude of V_{diff} = 900 mV with transient noise.

Resulting in the FOMs with the following values:

- $\mathrm{FOM}_1 = 152$ [dB]
- $\mathrm{FOM}_2 = 10798 \left[\frac{fJ}{Conv.-step}\right]$

The following graph shows the resulting SNDR of the modulator when varying the input signal amplitude.

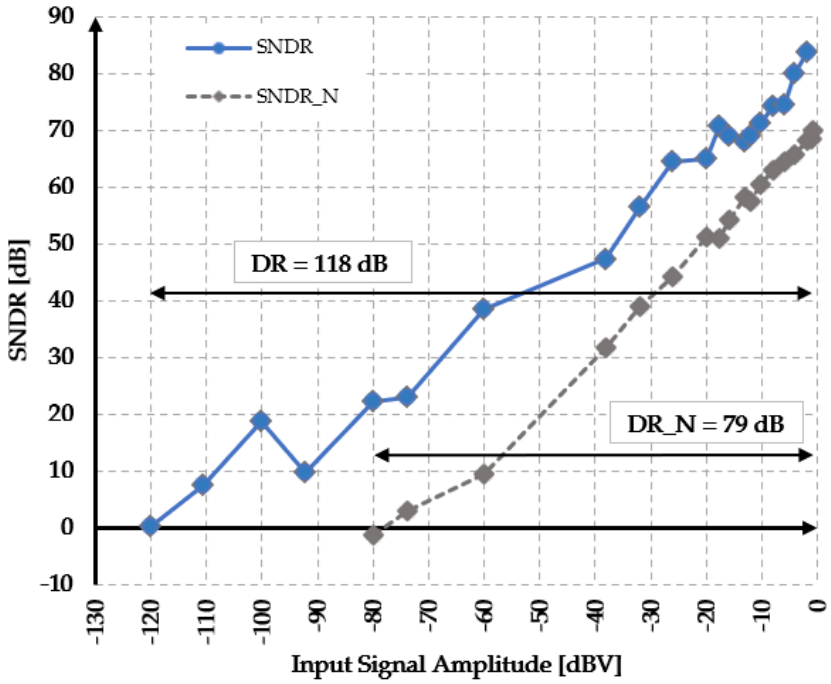


Figure 5.22 — SNDR versus input signal amplitude.

Table 5.3 — PROPOSED MODULATOR SPECIFICATIONS.

Modulator	This work	This work
Type	OAI opamp-less wo/ transient noise	OAI opamp-less w/ transient noise
CMOS [nm]	130	130
V_{DD} [V]	1.2	1.2
Signal Bandwidth [kHz]	2.5	2.5
Clock Frequency [MHz]	2	2
Peak SNDR [dB]	83	69
Power [µW]	136.8	136.7
ENOB	13.605	11.306
Dynamic Range [dB]	118	79
FOM_1 [dB] [DR+10log(BW/P)]	191	152
FOM_2 [fJ/Conv.-step] [P/(2*BW*2^ENOB)]	2196	10798

5.2 Discussion of results

The discussion of the results is presented considering the components that were proposed.

Comparator

The proposed comparator showed interesting results relative to the other standard-cell topologies studied. As expected, proposed design offered improved results over the OAI 4 topology proposed in [5], a 12% improved comparison time (delay), 27% improved power dissipation, and a 41% improved random offset, as seen in Table 5.4.

Relative to all the standard-cell topologies, the proposed comparator ended with the second best delay, the best being in the Inverter-based comparator, second best power consumption after the NAND DVC, but the best results in the static input offset and random offset, as depicted in Table 5.4.

Relative to the SADLC proposed in [2], the proposed comparator presented better delay, but not as good in the remaining specifications. As explained earlier in this work the SADLC is not a standard-cell topology but it is a state of the art comparator with excellent performance which, in this work, would serve as a base of comparison to the proposed comparator.

Amplifier

For the amplifier, the simulation results of the OTA without the CMFB, some of results of these simulations differ from the values expected from chapter 4.2.2. The DC Gain is exactly the expected result. The low frequency pole, p3, is located at the 1.24508 MHz which deviates from the expected value of 1.46881 MHz. This deviation originates a relative error of 18% which has an impact on the GBW frequency. These 18% are an acceptable error which may originate from the inexact V_{Dsat} values of the transistors in the theoretical analysis relative to the simulations as well as the considered approximations in chapter 4.2.2 and the stabilization of the circuit.

However, the CMFB circuit is necessary. The proposed topology showed the overall best results with the highest DC gain, GBW and lowest power dissipation, resulting in a FOM higher than the studied topologies, as depicted in Table 5.5.

ΣΔ Modulator

The results of the simulations run on the ΣΔ modulator show that it is working with the proposed comparator. The results for the tests run with transient noise are obviously worse than the ones without noise. The SNDR for the main studied input signal (V_{diff} = 220 mV) showed a 10 dB decrease when testing with noise, and the DR suffered a significant impact when the noise was present. These impacts where noticed in the FOMs. The power dissipation change was not significant when running the simulations with and without transient noise.

It is worth noticing that according to FOM_1 a higher value is better, and according to FOM_2 a lower value is better since that expression considers the energy spent per conversion-step.

The comparison of this modulator with the one in [17] is not fair since the proposed modulator uses a standard-cell based comparator which has performance limitations relative to the one in [17], but with the advantages described in chapter 1. Even so, relative to the modulator in [17], the proposed modulator showed better results in terms of SNDR, ENOB, and DR, however with the cost of a significant increase in power dissipation and BW.

Table 5.4 — PERFORMANCE COMPARISON FOR THE COMPARATORS.

Comparator	[2]	[4]	[3]	[5]	[7]	This work
Type	SADLC	RRDVC	NAND DVC	OAI	Inverter-based	OAI 2 in-puts
CMOS [nm]	130	130	130	130	130	130
V_{DD} [V]	1.2	1.2 *	1.2	1.2	1.2	1.2
Delay [ns]	0.145	0.27	0.152 **	0.128	0.094	0.109
Power [µW]	344	1104	782 **	1125	1171	890
Static Input Off-set [mV]	0.21	56	4 **	0.65	10.4	0.591
Random Offset [µV]	0.0057	84.27	71.87	14.57	320.85	10.42

* for $V_{diff} = 0$; ** for $V_{ref} = 900$ mV.

Table 5.5 — Performance Comparison For The Amplifiers.

Amplifier	[9]	[10]	[1]	This work
Type	OTA inverter-based (OTA 3)	Miller-Compensated OTA	I9BSSA	SP3SIB OTA w/ active CMFB
CMOS [nm]	130	130	130	130
V_{DD} [V]	1.2	1.2	1.2	1.2
DC Gain [dB]	57	27	19	63
GBW [MHz]	569	1019	419	1444
Phase Margin [°]	50	54	96	51
Output Swing [V]	1.260	1.192	1.260	1.260
Power [µW]	1370	3720	1538	1098
C_L [pF]	1	1	1	1
FOM [GBW*C_L/Power] [MHz*pF/mW]	415	274	272	1364

Table 5.6 — Performance Comparison For The Modulators.

Modulator	[17]	This work
Type	MOSCAP opamp-less	OAI opamp-less w/ transient noise
CMOS [nm]	130	130
V_{DD} [V]	0.4	1.2
Signal Bandwidth [kHz]	10	2.5
Clock Frequency [MHz]	2	2
Peak SNDR [dB]	58	69
Power [µW]	0.41	136.7
ENOB	9.342	11.306
Dynamic Range [dB]	64	79
FOM_1 [dB] [DR+10log(BW/P)]	168	152
FOM_2 [fJ/Conv.-step] [P/(2*BW*2^ENOB)]	32	10798

6

Conclusions and Future Work

The objectives of this work have been accomplished.

Starting with the comparator, the aim was for a reduced delay, random offset, and power dissipation than the studied state of the art comparators. The proposed comparator presented excellent results relative to the other studied, standard-cell, comparators.

For the amplifier, the proposed amplifier exceeded, in simulations, the studied topologies performance-wise which resulted in a larger FOM relative to the other studied amplifier topologies.

Finally, the proposed comparator has been employed in an opamp-less ΣΔ modulator with the objective of showing its working behavior when used in a working circuit, to which an edge-triggered flip-flop had to be added to the circuit. Here, the comparator worked flawlessly and achieved a similar performance. However, it achieved a much worse power dissipation, when compared with the comparator that was used in the prior art.

As referred in this work, using standard-cell-based topologies limits the performance of the components, but offers a good performance trade-off between the specifications. The proposed comparator and amplifier were a success objective-wise and the working modulator was also the final goal of this work.

For future works, an improvement of the ΣΔ modulator with the proposed comparator is suggested with the flip-flop proposed in [21], due to its compact topology which might offer a better response and improved power dissipation, improving the performance of the ΣΔ modulator.

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A

APPENDIX

A.1 - Schematics for the Comparator Testbench

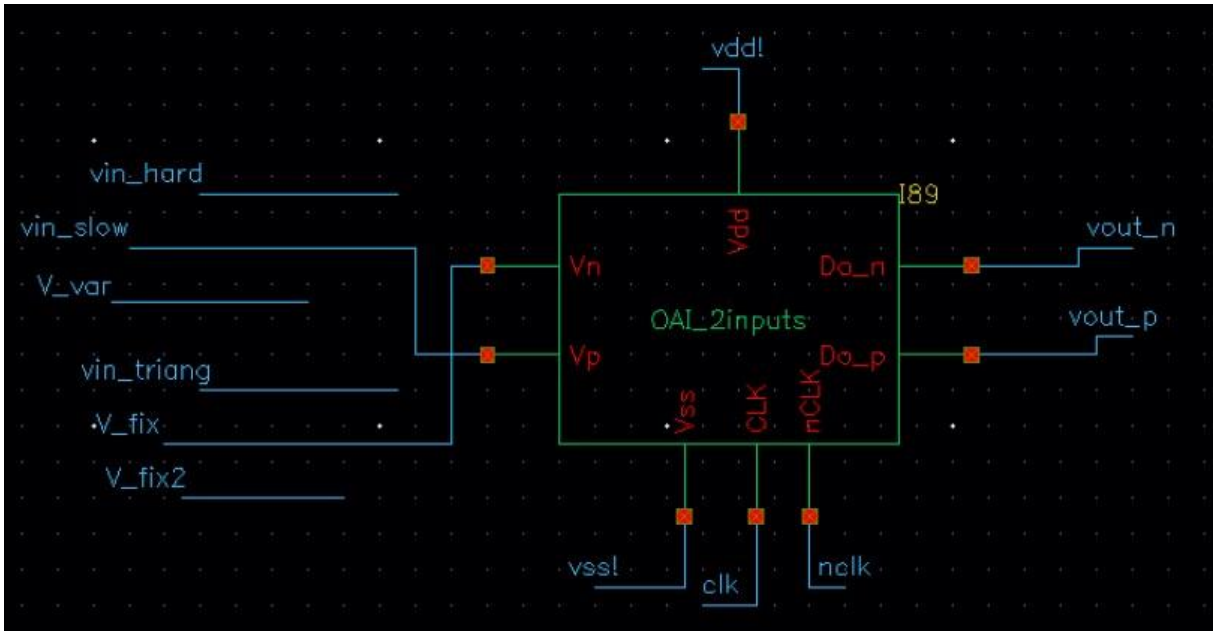

Figure A.0.1 — Testbench for the comparators.

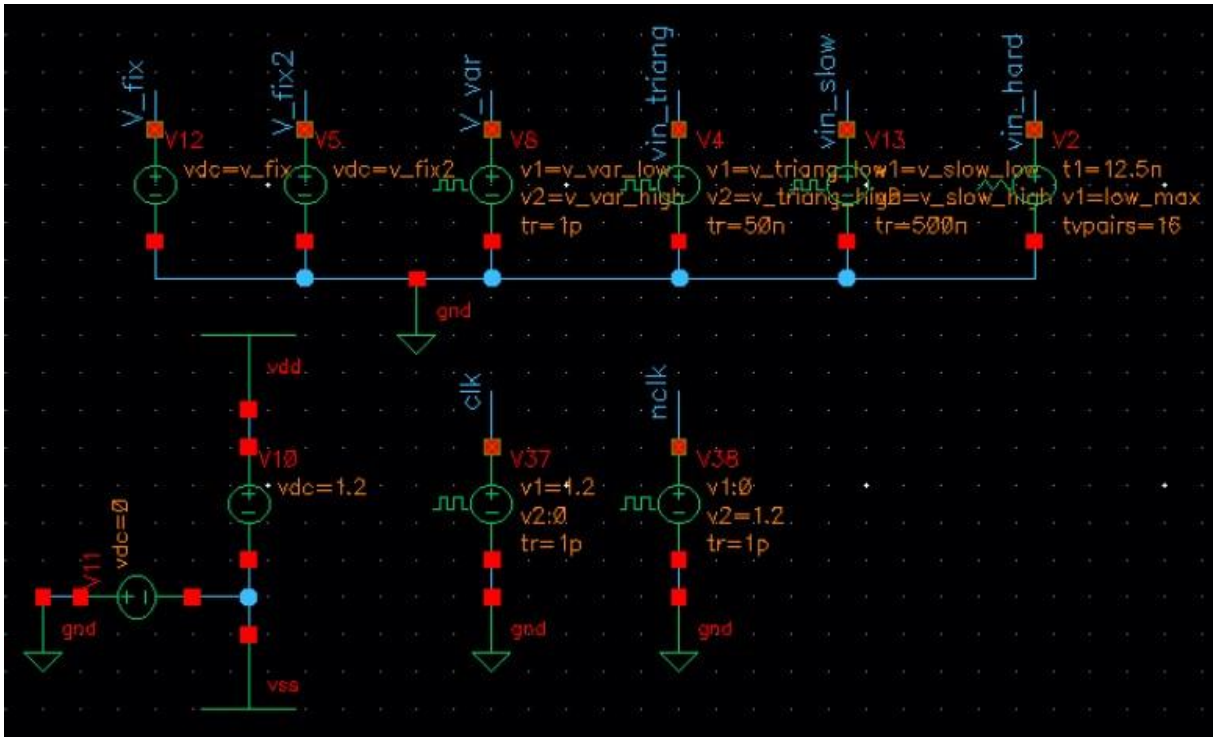

Figure A.0.2 — Ideal voltage sources for DC voltages, input signals and clock signals.

A.2 - Schematics for the Amplifier Testbench

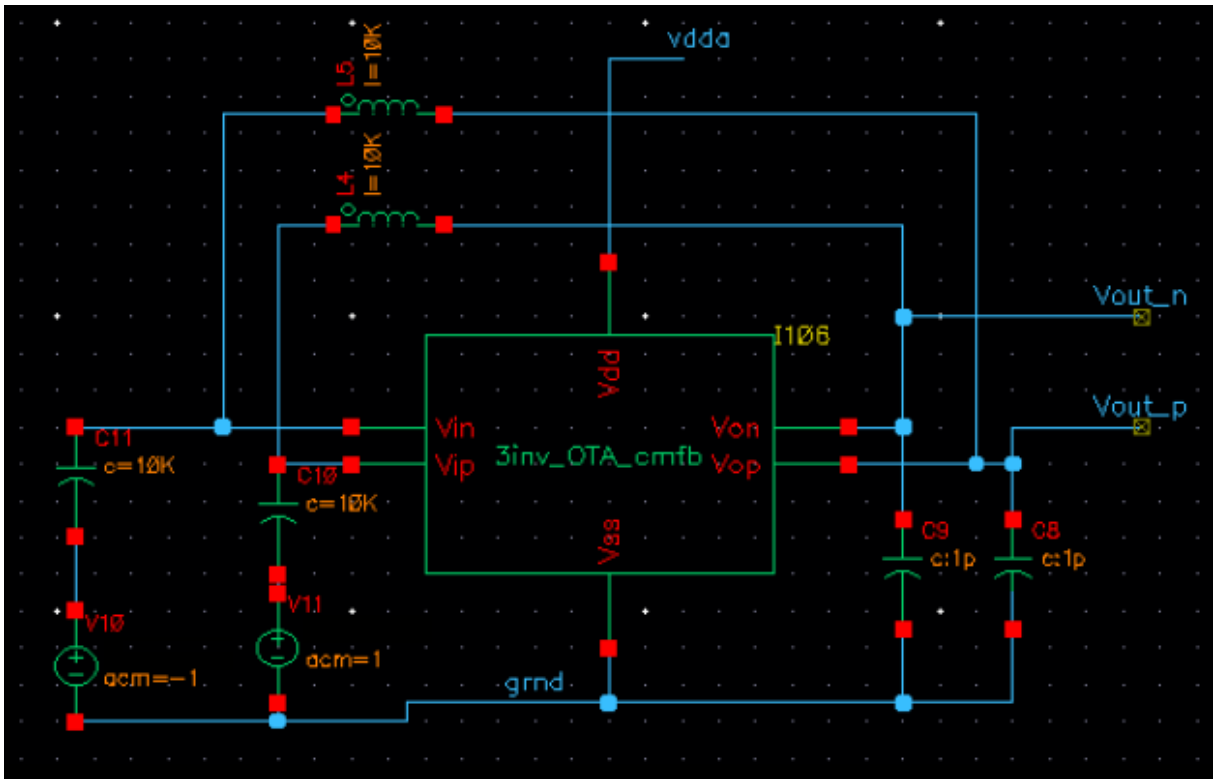

Figure A.0.3 — Differential AC analysis testbench.

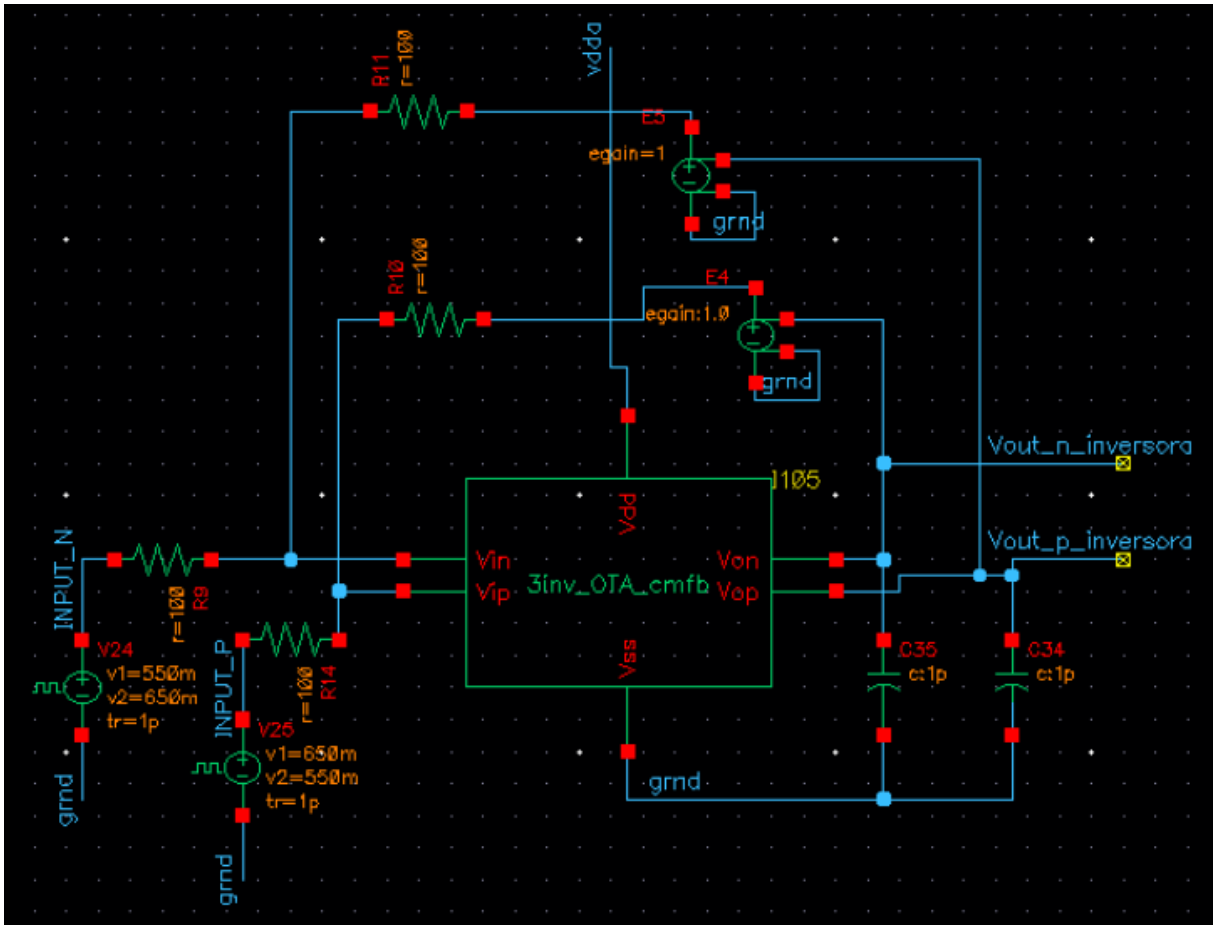

Figure A.0.4 — Differential transient analysis testbench.

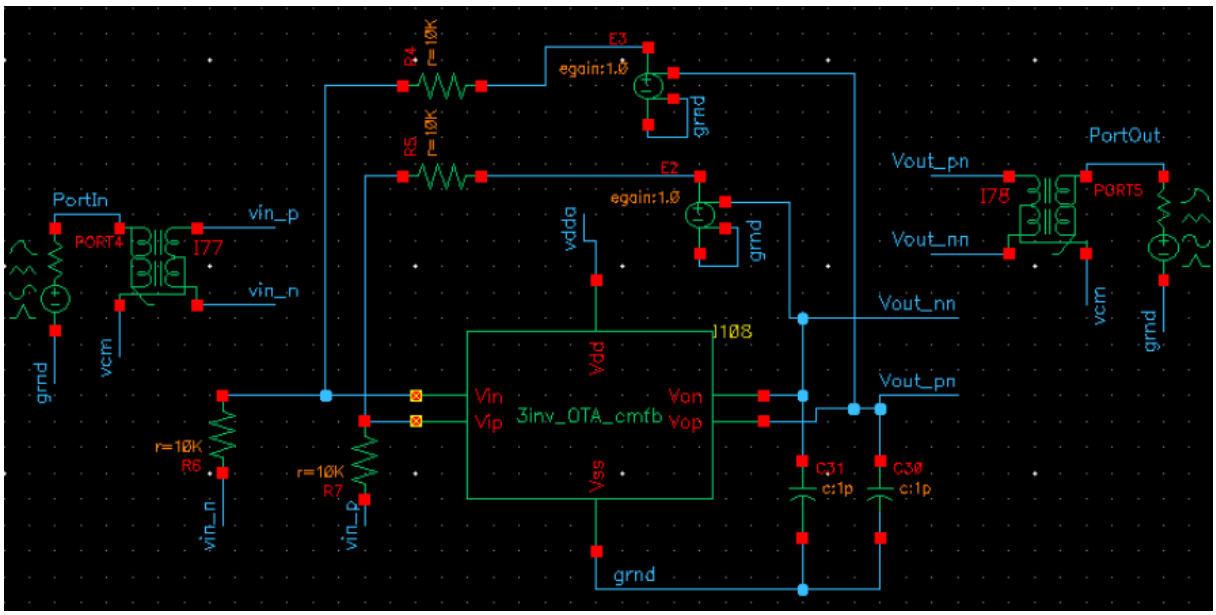

Figure A.0.5 — Differential AC Noise analysis testbench.

A.3 - Schematics for the Modulator Testbench

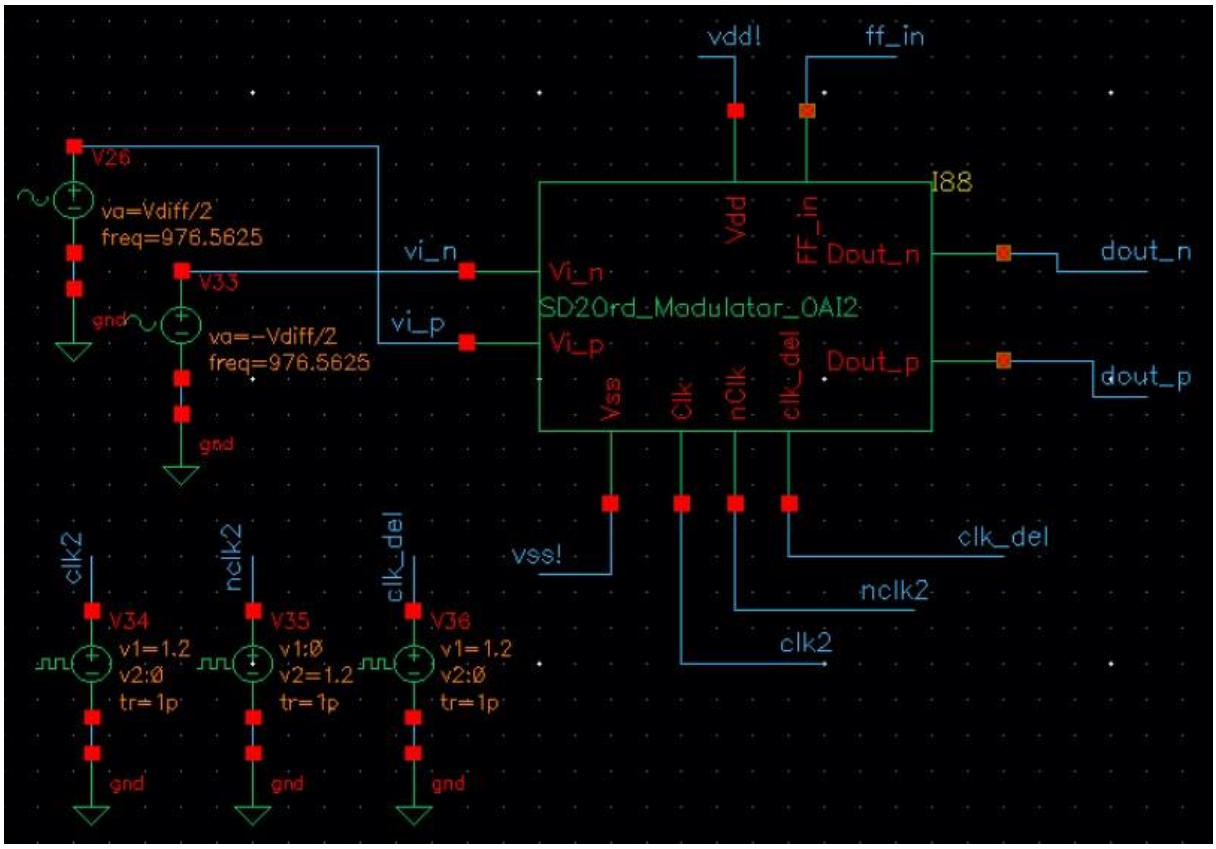

Figure A.0.6 — Modulator analysis testbench and clock sources.