NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

GIL LUZ GONÇALVES

Bachelor in Electrical and Computer Engineering

ACTIVE INDUCTOR FOR SERDES TX DRIVER TERMINATION

MASTER IN ELECTRICAL AND COMPUTER ENGINEERING

NOVA University Lisbon
November, 2021

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Acknowledgements

I would like to express my gratitude to NOVA School of Science and Technology from NOVA University of Lisbon and *Synopsys* for this opportunity to not only grow up as a future professional but also as a human being.

To give my thesis advisor, professor Luís Oliveira, a special thanks for choosing me as the right person to carry out this project and for all the guidance throughout its development.

I would also like to thank my supervisor in Synopsys, Eng. Rui Girão, for all the time put into my adjustment to this new environment and mention all the colleagues that helped me achieve the results accomplished in this thesis, those being the engineers José Brito, Joaquim Machado, João Baixinho, Sr. Mgr. Joaquim Machado and Dir. Ricardo Reis.

Additionally I would like to show appreciation for all the support i received from university colleagues and friends with special consideration to names such as Diogo Dias, Miguel Marcelo, Carolina Luís, Shazia Sulemane and Gonçalo Santos.

Finally, I would like to state my gratitude to my family for the investment they did on me and my education throughout all my life.

Abstract

As the technology keeps narrowing occupied silicon area, techniques to accomplish chip-to-chip data communication such as the SerDes aiming to achieve higher date transfer rates begin to look at passive inductors as an unreliable approach as these components consume large portions of chip area. The solution mentioned in this thesis revolves around using active components such as transistors to implement active inductors able to scale down with technology reducing die area and costs associated.

The objective of this thesis is to simulate active inductors in 16 nm FinFET technology and compare two of these component architectures when employed on a CML driver, with the most beneficial one, a CML driver with active loads comprised of inductors made of only a transistor and a resistance, being studied on more detail.

This CML driver with active loads ended up improving the bandwidth of the original CML driver from 6.5 GHz to 10.1 GHz while presenting a 50 Ω termination and a differential output swing of 976 mV.

Keywords: Active inductor, SerDes, CML driver, bandwidth improvement.

Resumo

À medida que a tecnologia continua a reduzir a área de silício, técnicas para realizar a comunicação de dados entre circuitos integrados, como os SerDes, com o objetivo de alcançar taxas de transferência de data mais altas, começam a olhar para bobinas passivas como uma abordagem pouco fiável, já que estes componentes consomem grandes porções de área de silício. A solução mencionada nesta tese gira em torno do uso de componentes ativos, como transistores, para implementar bobinas ativas capazes de serem reduzidas com a tecnologia, reduzindo a área de chip e os custos associados.

O objetivo desta tese é simular bobines ativas na tecnologia FinFET de 16 nm e comparar duas das arquiteturas destes componentes quando usadas num driver CML, com a mais benéfica, um driver CML com cargas ativas compostas por bobinas de apenas um transistor e uma resistência, sendo depois estudado com mais detalhe.

Este driver CML com cargas ativas acabou por estender a largura de banda do driver CML original de 6,5 GHz para 10,1 GHz, apresentando uma terminação de 50 Ω e uma saída diferencial de 976 mV.

Palavras-chave: Bobinas ativas, SerDes, driver CML, melhoria da largura de banda.

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Acronyms

CD	common-drain
CDR	clock and data recovery
CG	common-gate
CML	current mode logic
CMOS	complementary metal-oxide semiconductor
CS	common-source
CTLE	continuous time linear equalizer
DC	direct current
DTLE	discrete time linear equalizer
DTMOS	dynamic threshold metal oxide semiconductor field effect transistor
FFCS	feed-forward current source
FFP	feed forward path
FinFET	fin field-effect transistor
ft	transit frequency
I/O	input/output
MOSFET	metal oxide semiconductor field effect transistor
NMOS	n-channel metal-oxide semiconductor
OS	output swing
PMOS	p-channel metal-oxide semiconductor
PVT	process voltage and temperature

Q	quality factor
RF	radio frequency
SerDes	serializer desserializer
SRF	self resonance frequency
TX	transmitter
UWB	ultra-wideband
VHF	very high frequency

1

Introduction

1.1 Background and Motivation

Advances in integrated circuits technology have pushed further and further the data communication rates in high-speed I/O links resulting in a demand for higher bandwidths[1].

In order to achieve data rates in the orders of the gigabytes per second, standard circuitry design implements passive on-chip inductors with low power consumption, low noise and good linearity[2]. However, this spiral inductors end up occupying large chip area, for example 100 μm by 100 μm in case of a differential spiral inductor hitting 1.5 nH, posing a problem to the continuous scaling down of technology as the number of I/O pins required in the same chip keeps raising [3].

Active inductors based on CMOS technology appear as the solution to decrease the necessary area to implement high-speed communication between chips, becoming cheaper and providing large inductance values at higher frequencies allowing to achieve greater bandwidths.

Although they are considerably easy to design, employing active devices in order to obtain the two transconductances belonging to the gyrator-c model currently used as the main approach in their elaboration, active inductors still suffer with some problems such as noise and linearity making them not as attractive as their passive counterparts.

The mains focus of this work is to investigate active inductors including design techniques that allow to achieve better performances in circuits conceived to operate at high frequencies close to the 10 GHz mark.

1.2 Thesis Organization

This thesis is divided in 6 chapters, including this first one consisting of the introduction.

Chapter 2 is divided in 4 major parts including a brief breakdown of the elements consisting a SerDes, a description of the main uses of inductors in general alongside a

comparison between the passive and active inductors performances, an overview of the gyrator-c model applied in the design of active inductors ending in a presentation of the most common implemented architectures.

In chapter 3 is given a review of the state-of-the art active inductors focused on circuits aiming to work at high frequencies with techniques to improve their performance in terms of Q factor, linearity, bandwidth and noise, comparing them at the end.

Some of the mentioned active inductors discussed in both chapter 2 and 3 are then analyzed in chapter 4 with 16 nm technology improving the results found by the authors of the inductor circuits and allowing one to assess which circuits can present more advantages for the final circuit design.

The core of the thesis is presented in chapter 5 where a transmitter driver or TX driver will be first studied on its own before adding two active inductors performing inductive peaking. These two circuits will then be compared and the circuit that exhibits the best results is later on simulated in more detail.

The final chapter is reserved for conclusions where future developments of this thesis are suggested.

1.3 Original Contributions

This thesis was conceived in a business context derived from an internship in *Synopsys* and its main contributions consist in the study of active inductor topologies simulated with a smaller technology of 16 nm as well as the implementation of two circuits with different active inductors based on a regular CML driver [4]. The first circuit includes active loads similar to a CTLE with inductive peaking [5], a SerDes component as well, while the second one implements a non-gyrator type active inductor [6].

The results presented indicate that both designs allow the driver to achieve higher bandwidth through inductive peaking with the circuit that proves to be more advantageous being simulated in a more realistic test bench to evaluate the upsides and downsides of such circuit design.

2

SerDes and Active Inductors

In this chapter, an overview of the serializer/deserializer (SerDes) and active inductors will be provided. It will address the properties of the active inductors making a comparison with their passive counterparts and giving an insight on some of the most implemented active inductor architectures.

2.1 SerDes Concepts

2.1.1 Chip to chip data communication

A straightforward way to establish communication between chips is to connect the outputs of a chip into the inputs of another through a parallel data bus. This datapath is responsible for the transmission of several bits in a synchronous manner (as long as both chips share the same clock) requiring an even amount of outputs, inputs and bits transferred. This poses a problem as, with the scaling down of technology, chips are getting denser and with less space for I/O pins turning data transfer through multiple interconnections impracticable [7].

In order to reduce the number of I/O pins necessary to allow communication between chips, a serialization technique is put into practice. To perform serialization, the data is multiplexed at the output of the transmitter chip and demultiplexed at the receiver chip as shown in fig. 2.1. where n is the number of bits transferred and k the number of interconnections. This reduction of pins has an impact on the clock frequency as, in order to keep the same speed of data transfer, it is required a frequency increase by the ratio n/k. The best implementation of this serialization for large data rates consists on high-speed serializer/deserializer (HSS).

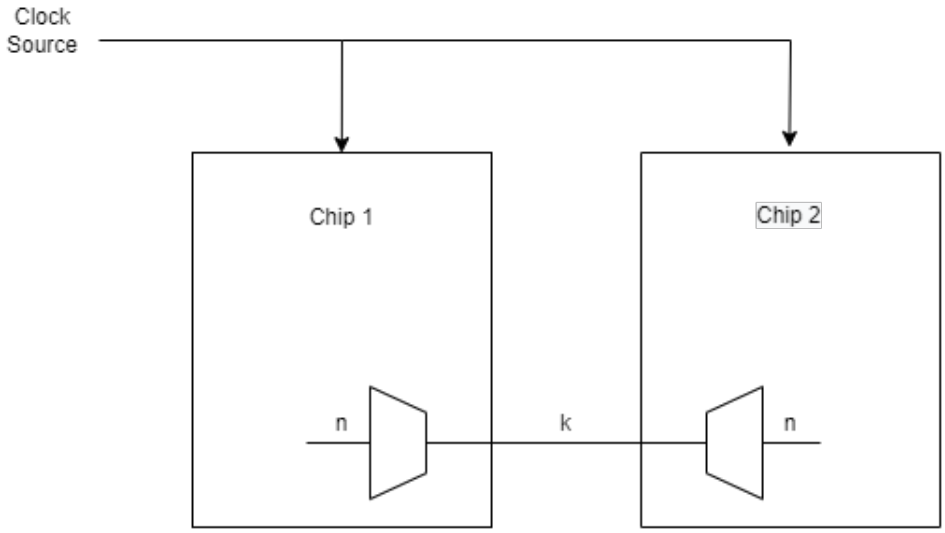


Figure 2.1: Data transfer with serialization [7].

2.1.2 High-speed SerDes

With the capability of handling data transfers at speeds over 2.5 Gbps, HSS devices are divided in 6 components, as showcased in fig. 2.2, those being the serializer and deserializer blocks, the equalizer, the clock and data recovery (CDR), the differential driver and finally the differential receiver.

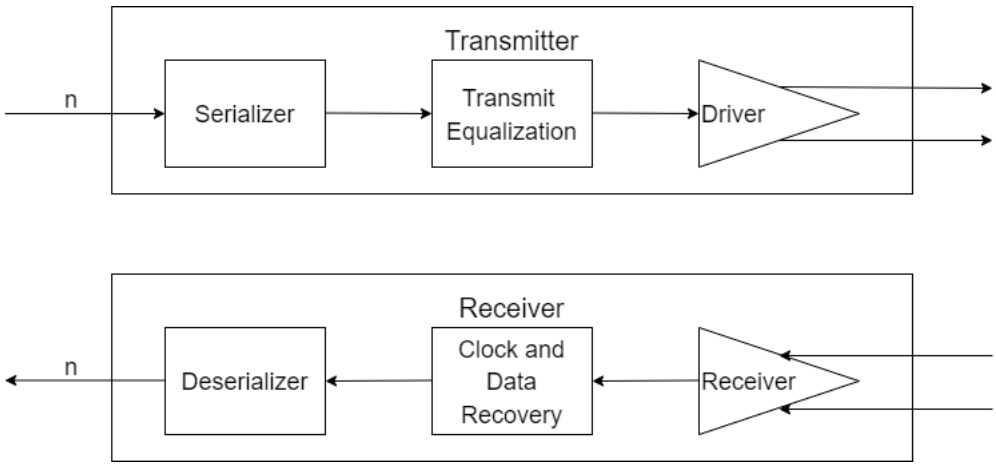


Figure 2.2: Composition of a SerDes [7].

Serializer and deserializer blocks

Ideally, the serializer block converts several bits, usually multiples of 8, into a single bit data signal. Nevertheless, wider datapaths are widely used, since the the equalizer, the component that follows the serializer, struggles to operate at high frequencies, this however complicates considerably its design. To maintain a single bit data transmission without requiring the equalizer to work a higher frequencies some implementations

perform the multiplexing in two stages, one before the equalizer and one after.

The deserializer block executes the exact opposite of the serializer dividing the data received back to the same bits as the ones converted by the serializer along with some information about the clock.

Equalizers

At certain frequencies the connection between the chips shows the same behaviour as a filter distorting the signal collected by the receiver. To avoid such concern, equalization is introduced in the transmitter chip with a transfer function opposite to that of the channel filter behaviour.

The most common equalizers integrated in SerDes are the feed forward equalizers (FFE) consisting on a series of flip-flops delaying the signal while implementing *taps*, each *tap* is associated with a certain weight also denominated filter coefficient responsible for countering the effects of signal distortion.

Clock and data recovery

Initially, in order to establish communication in a synchronous way, a single external clock was connected to both chips, this would require special consideration regarding the design of the SerDes as the delays associated to the devices would have to be taken into account [8]. Later on, a solution was found in source-synchronous setups, however this solution would add up more transmission lines that would require more I/O pins a problem already mentioned before.

The majority of HSS choose to adopt the CDR as a solution for this problems. It allows the receiver chip to obtain information on the clock based on the data received from the transmitter, this allows the synchronous communication to succeed without extra lines, thus reducing the noise.

Differential driver and receiver

The differential driver is the analog circuit responsible for transmitting a differential signal based on a true and complement signal generating elements [9] with means to reduce jitter. This is normally achieved with the help of flip-flops controlled by a clock working at baud rate [7].

On the other hand, a differential receiver is a comparator responsible for generating "0"and "1"with the true and complement legs of the differential signal it receives.

2.2 Inductors

2.2.1 Inductor applications

Inductors are currently included in high-speed communications for a variety of reasons aiming to improve the performance of the system [10]. The main employments of the inductors will be explained below.

LC oscillators

LC Oscillators are a good alternative to common ring oscillators as they introduce less phase noise, a sensitive characteristic in wireless communications. This is usually achieved with a passive fixed inductance and a tunable capacitor, in order to match the frequency desired, forming an LC tank.

Impedance matching

To maximise power transfer between channels and high-speed circuits it is important to reduce signal reflection and therefore achieve impedance matching where the output impedance of a certain circuit matches the input of the following one. Resistors are the most commonly used component for broadband communication systems as they allow an impedance matching for a large range of frequencies. Nonetheless, in narrowband wireless communications, frequency-dependent components such as inductors and capacitors are the most practical ones as they do not introduce as much noise as resistors do.

Phase shifting

As the name suggests, the purpose of phase shifting is to control the phase of a signal flowing through an uni-directional serial network. This is done with the help of a sequence of variable shunt capacitors called varactors. An example for the most common phase shifting circuitry is shown in fig. 2.3.

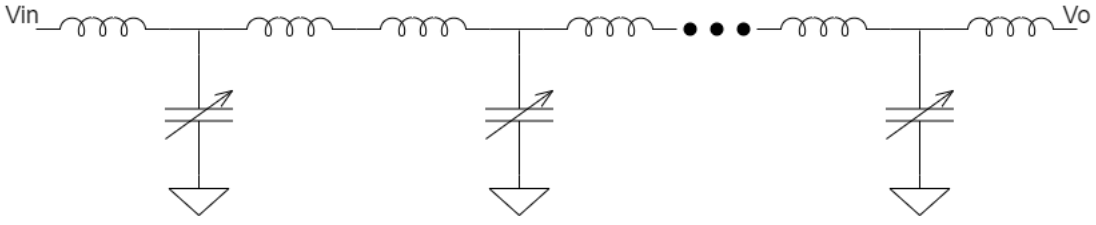


Figure 2.3: Phase shifting circuit [10].

Frequency selection

In narrow-band communications it is often required bandpass filters selecting frequencies for RF systems. These filters usually consist in lumped LC and surface acoustic wave (SAW) filters. Even though the second one is the most commonly used filter, it is not

compatible with CMOS technologies, (therefore not compatible with active components such as active inductors), therefore engineers attention has been turned to on-chip RF filters embedded in RF transceivers with ideas to compensate for high ohmic losses in spiral inductors.

Gain boosting

Traditionally, cascodes are the typical solutions to increase gain of a device, however MOSFETS' parasitic capacitances limit their use in high frequencies. An attractive replacement to perform the same operation is to resort to LC tanks. One example of this can be seen in low noise amplifiers as they rely on LC tank loads, as suggested in fig. 2.4, benefiting on their infinite impedance at high frequencies to boost their gain.

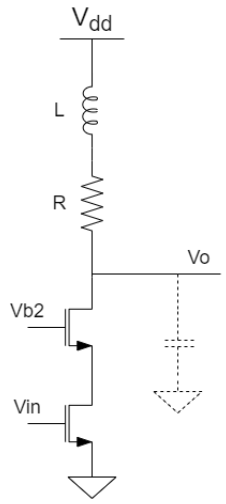


Figure 2.4: Example of gain boosting in a LNA [10].

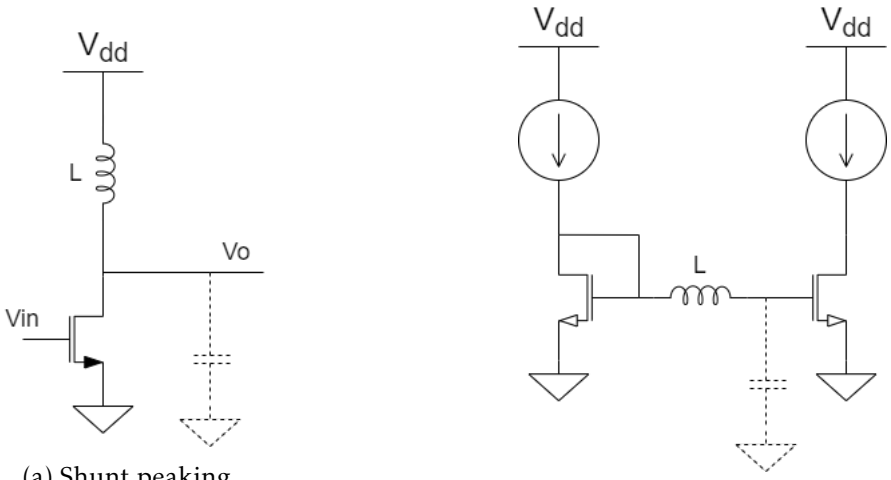
Power dividers

Power dividers such as the Wilkinson power divider [11], combine or separate the incident power at the output through a three branched network usually featuring transmission lines. In virtue of their usual length, efforts have been put into finding solutions to reduce their size, seeing as an alternative to lossy and limited passive inductors their active implementation.

Bandwidth improvement

Possibly the most critical application of inductors in SerDes, bandwidth improvement is an important requirement all around data communication circuits. There are currently three major approaches to enhance bandwidth those being inductive peaking, distributed amplification and current-mode signaling, however only the first two rely on inductors.

Inductive peaking The first approach includes inserting an inductor in a node with a high value of nodal capacitance. This inductance will resonate with the nodal parasitic capacitances forming an RLC circuit and enlarging the bandwidth when working at under-damped mode. This comes without affecting low-frequency gain of amplifiers as opposed to conventional microwave design techniques[12]. There are two different implementations of inductive peaking, series peaking and shunt peaking, both exhibited in fig. 2.5.



(a) Shunt peaking.

(b) Series peaking.

Figure 2.5: Inductive peaking [10].

Distributed Amplification Another technique to compensate the large nodal capacitance and improve bandwidth is achieved by dividing that large capacitor in smaller shunt capacitors separated by inductors. This distributed amplification is usually accomplished in MOSFETs when broken down in several fingers, which means dividing the transistor in smaller ones connected together (through inductors to increase the bandwidth) performing the same specifications. An example of this technique is depicted in fig. 2.6.

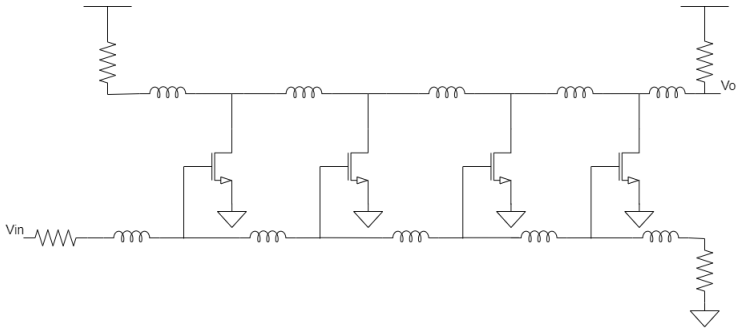


Figure 2.6: Example of distributed amplification applied to a MOSFET with four fingers [10].

2.2.2 Passive inductors

Spiral inductors still remain as the most employed inductors in integrated circuitry. These passive inductors are separated in two types, planar and stacked inductors. Planar inductors consist on a single metal strip rolled in a square shape. Their physical model can be represented in fig. 2.7 and it includes the inductor's inductance as well as all RC parasitics associated where R_s represents the resistance of the metal strip, C_s accounts for the capacitance generated by the overlap between the inductor and the underpass, C_{ox} depicts the oxide capacitance between the spiral and the silicon substrate and C_{si} plus R_{si} are representative of the capacitance and resistance of the silicon substrate[13].

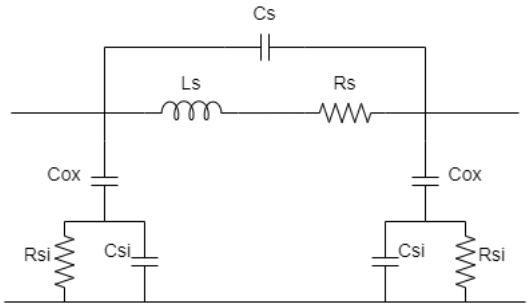


Figure 2.7: Physical model of a spiral inductor [13].

To increase the inductance of such components, which is usually small, these planar inductors are organized in stacked configurations improving the inductance by the sum of their inductance plus the mutual inductance between them.

2.2.3 Active inductors versus passive inductors

With the non-stopping scaling down of technology, active inductors, essentially made up of CMOS transistors, become an appealing upgrade compared to passive inductors. However some drawbacks such as noise and linearity contributions make them less popular[10][14]. Some of the advantages and disadvantages will be listed below.

Silicon area consumption Due to their low value of inductance, spiral inductors require many turns thus occupying a large proportion of silicon area. The active inductors however rely on CMOS transistors to be implemented and therefore occupy much less die area. This also allows the active inductor to scale down with technology while the passive counterpart is limited to a minimum size.

Tunability Active inductors also prove to be advantageous in this chapter as their inductance can be varied through transistor biasing whilst the spiral inductors are constrained to their number of turns.

Inductance and quality factor value As referred before, spiral inductors are limited to their number of turns and present a low inductance as well as quality factor values only improved through stacking and therefore occupying more silicon area. Active inductors however can present considerably high values with the simplest of designs.

Power consumption The first disadvantage in the use of active inductors resides in the power consumption required to produce inductance which is not necessary for passive inductors[14]. Apart from that, the voltage headroom required also presents a downside to active inductors.

Linearity Linearity is another major drawback when using active inductors as active devices have an hard time handling large signals, resulting in impedance fluctuations. Their usage is restricted to small signals, not allowing their implementation in circuits with large signal performance like power amplifiers.

Noise Possibly the main reason why active inductors are not popular, noise still remains a challenge in designs of active inductors as engineers have to dwell with the noise contributions of the CMOS transistors included in the circuit.

2.2.4 Properties of active inductors

The Gyrator-C model

To perform the same function as the passive counterpart, active inductors rely on active devices to achieve the same impedance. This is usually implemented with the gyrator-C model, depicted in fig. 2.8, incorporating a capacitor and two ideal transconductances, one negative and one positive, to successfully accomplish a positive imaginary impedance [15]. This can be confirmed by its transfer function,

$$\frac{V_{in}}{I_{in}} = \frac{sC}{G_{m1}G_{m2}} \tag{2.1}$$

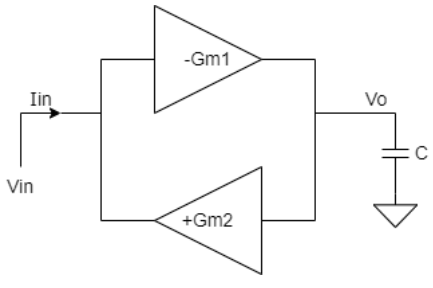


Figure 2.8: Gyrator-C model [15].

However, this is true assuming transconductors with infinite input and output impedances, in reality, active inductors are described with lossy single-ended gyrator-C or lossy floating gyrator-C models given in fig. 2.9 accompanied by their associated impedance described as:

$$Z_{in} = \frac{1}{sC_1 + G_{o1} + \frac{G_{m1}G_{m2}}{sC_2+G_{o2}}} \tag{2.2}$$

where G_{m1} and G_{m2} correspond to the transconductances, G_{o1} and G_{o2} to the output resistances and C_1 and C_2 to the parasitic capacitances.

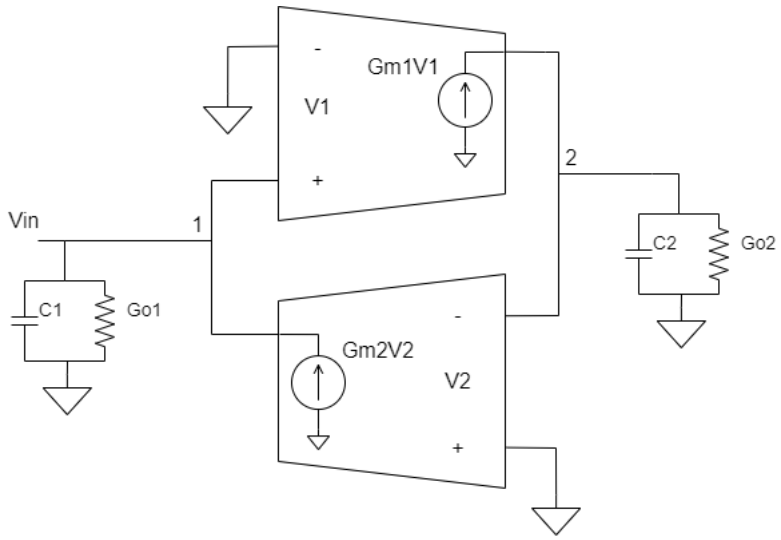


Figure 2.9: Lossy gyrator-C models[15].

This model can be furthermore simplified through a RLC equivalent circuit, fig. 2.10, whose terms relate to the gyrator-C model in the following manner:

$$Cp = C_1 \tag{2.3}$$

$$Rp = \frac{1}{G_{o1}} \tag{2.4}$$

$$Leq = \frac{C_2}{G_{m1}G_{m2}} \tag{2.5}$$

$$Rs = \frac{G_{o2}}{G_{m1}G_{m2}} \tag{2.6}$$

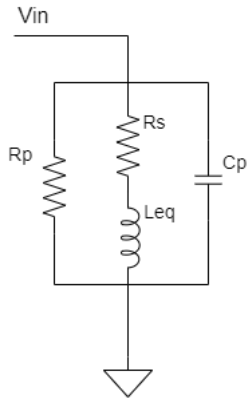


Figure 2.10: Equivalent RLC circuit for active inductors [15].

Frequency range

Active inductors only present an inductance behaviour in a limited frequency range exhibiting a resistive characteristic for lower frequencies below the zero frequency and a capacitive one for frequencies above the SRF [10]. This performance can be seen in fig. 2.11.

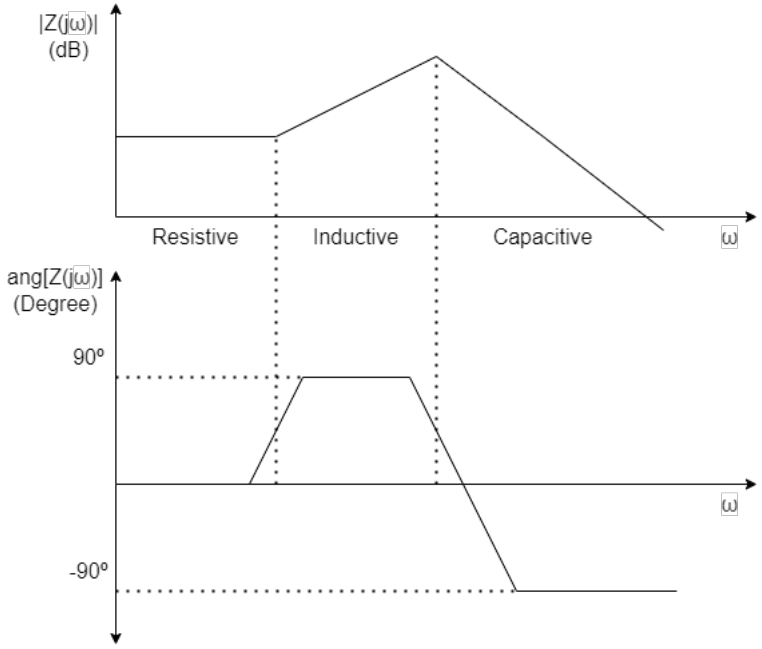


Figure 2.11: Active inductor frequency performance [10].

The pole (SRF) and zero frequencies can be obtained from the impedance of the inductor and can be expressed as:

$$\omega_p \simeq \omega_0 = \sqrt{\frac{1}{LC_p}} \tag{2.7}$$

$$\omega_z = \frac{R_s}{L} \tag{2.8}$$

Quality factor

The quality factor (Q) for every inductor is given by the ratio between the net magnetic energy stored and the ohmic losses over one oscillation cycle, namely, the impedance's imaginary and real parts. The quality factor associated to the gyrator-C can be described through:

$$Q = \frac{Im(Z_{in})}{Re(Z_{in})} = \frac{\omega L}{R_s} \frac{R_p}{R_p + R_s[1 + (\frac{\omega L}{R_s})^2]} [1 - \frac{(R_s)^2 C_p}{L} - \omega^2 L C_p] \tag{2.9}$$

The Q can then be divided in three terms. The first one is equivalent to $\frac{\omega L}{R_s}$ and is associated with the Q at low frequencies. The second one, given by $\frac{R_p}{R_p + R_s[1+(\frac{\omega L}{R_s})^2]}$, represents the effect of the finite impedance of transistors and the final one, $1 - \frac{(R_s)^2 C_p}{L} - \omega^2 L C_p$, is responsible for collapsing the Q at high frequencies.

One way to increase the Q of a certain active inductor is by adding a negative resistor circuit in order to reduce R_s thus achieving high Q value.

Linearity

The preceding described response of the active inductor is only valid for small input signals. As the signal voltage swing increases the circuit looses its linear response generating DC fluctuations and moving the operation point of the transistors integrating the inductor from the saturation region to the triode region reducing the transconductances from g_m to g_{ds} while proportioning some C variations[10].

2.3 Basic Active Inductor Architectures

In this section, some active inductor topologies implemented solely with transistors are discussed.

2.3.1 Thanachayanont-Payne CMOS Transistor-Only Active Inductor Topologies

As the following active inductor topologies are generated exclusively with two transistors they are suited to operate in very high frequencies close to their transit frequency (ft). In order to accomplish both transcoductances of the gyrator-C model, basic amplifiers are used, those being common-drain (CD), common-source (CS) and common-gate (CG), CS should be paired with either a CD or a CG as it presents a negative transconductance unlike the other two amplifiers [16].

2.3.1.1 Common-Source Amplifier Mixed with Common-Drain

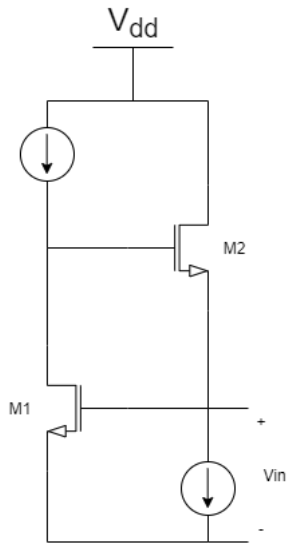


Figure 2.12: CS-CD active inductor.

The first configuration presented in fig. 2.12 features both CS and CD stages and obtains a high Q for wide bandwidth at the cost of not being able to function at low supply voltage as the minimum required is $2V_{gs} + V_{DSsat}$[17].

2.3.1.2 Common-Source Amplifier Mixed with Common-Gate

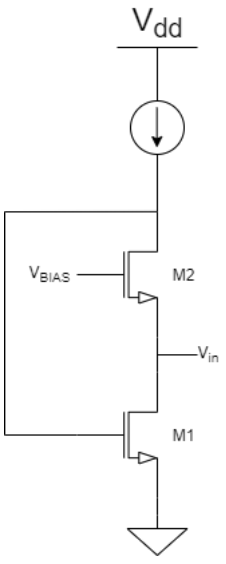


Figure 2.13: CS-CG(n-n) active inductor.

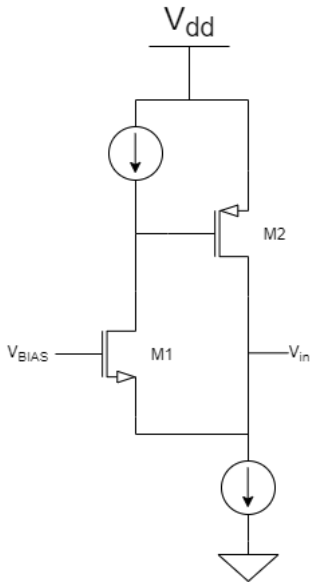


Figure 2.14: CS-CG(n-p) active inductor.

Compared to the last CS-CD configuration this CS-CG topology (fig. 2.13) offers less power consumption for the same supply voltage as both transistors share the same current. However, this circuit presents a low Q as the equivalent resistance, which is close to $frac1gm2$, tends to acquire low values. In an effort to raise the Q of the inductor, negative impedance circuits are added at the cost of reducing SRF and increasing power consumption as well as noise[18].

Another configuration can be used in order to achieve a more tunable active inductor. Using this configuration, the circuit is once again divided in two branches as evidenced in fig. 2.14 therefore increasing the current flowing in the circuit while slightly increasing the supply voltage.

2.3.1.3 High-Q VHF Active Inductor

The circuit presented in fig. 2.15 [16] is currently one of the most significant active inductors due to its simplicity, its particular attractiveness coming from the high Q value it achieves with the few transistors it includes.

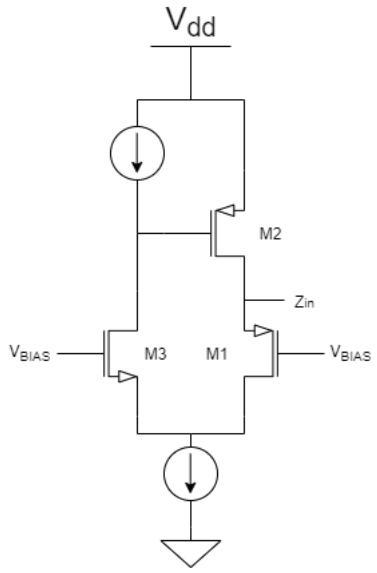


Figure 2.15: High-Q VHF active inductor.

This inductor is an adaptation from a simple CS-CG active inductor with p-mos devices prioritizing reduction of noise as well as negating the non-linear body effect over performance at high frequencies. It introduces a single CG, M3, as an attempt to increase the loop-gain therefore reducing the series resistance in order to achieve high Q.

Taking into account the RLC equivalent circuit of the active inductor, C_p corresponds to C_{gs3}, R_p is equal to $1/g_{ds2}$ and the overall impedance is expressed as:

$$Z_{in} = \frac{g_{ds3}g_{ds1} + (g_{ds1}C_{gs1} + g_{m1}C_{gs2})\omega + C_{gs1}C_{gs2}\omega^2}{g_{m3}\omega^2 C_{gs1}C_{gs2} + (g_{m3}g_{ds1}C_{gs1} + g_{m3}g_{m1}C_{gs2})\omega + g_{m1}g_{m2}g_{m3})} \tag{2.10}$$

The inductance and series resistor correspond, respectfully, to the imaginary and real part of Z_{in} given by:

$$Im(Z_{in}) = \frac{(\frac{g_{ds1}C_{gs1}}{g_{m1}g_{m2}g_{m3}} + \frac{C_{gs2}}{g_{m2}g_{m3}})j\omega}{(1 - \frac{C_{gs1}C_{gs2}}{g_{m3}}(\frac{\omega}{g_{m1}g_{m2}})^2)^2 + (\frac{g_{m3}g_{ds1}C_{gs1} + g_{m3}g_{m1}C_{gs2}}{g_{m1}g_{m2}g_{m3}})^2\omega^2} \tag{2.11}$$

$$Re(Z_{in}) = \frac{\frac{g_{ds1}g_{ds1}}{g_{m1}g_{m2}g_{m3}} + \frac{g_{m1}C_{gs1}}{g_{m3}}(\frac{C_{gs2}}{g_{m1}g_{m2}})^2(\frac{g_{m1}}{C_{gs1}} - \frac{g_{m2}}{C_{gs2}})\omega^2 + \frac{1}{g_{m3}}(\frac{C_{gs1}C_{gs2}}{g_{m1}g_{m2}})^2\omega^4}{(1 - \frac{\omega^2 C_{gs1}C_{gs2}}{g_{m1}g_{m2}})^2 + (\frac{g_{m3}g_{ds1}C_{gs1} + g_{m3}g_{m1}C_{gs2}}{g_{m1}g_{m2}g_{m3}})^2\omega^2} \tag{2.12}$$

whose approximations for lower frequencies correspond to:

$$L = \frac{C_{gs1}}{g_{m2}g_{m3}} \tag{2.13}$$

$$R_s = \frac{g_{ds1}g_{ds3}}{g_{m1}g_{m2}g_{m3}} \tag{2.14}$$

As mentioned before, this circuit reduces the series resistance of the common CS-CG by a factor of $\frac{g_{m3}}{g_{ds3}}$, increasing significantly the Q of the active inductor without adding any

negative impedance circuits thus guaranteeing greater bandwidth for the same power consumption. This Q can be altered through devices M2 and M3 by changing the gate voltages of both transistors therefore varying g_{m2} and g_{m3} which impacts the inductance as well as varying g_{ds2} and g_{ds3} with a direct effect on the series resistance.

2.3.2 Lin-Payne Active Inductor Topology

The next architecture is once more centered around the combination between a CS and CD implemented, respectfully, with a NMOS and a PMOS transistors[19]. This architecture is designed to work at a minimum supply voltage of 0.95 V ($V_{DSsat} + V_{GSp}$), however, the authors suggest increasing this value in order to compensate for the threshold voltage variations and to increase the voltage headroom of the transistors allowing the active inductor to handle large signals maximizing the dynamic range of the circuit displayed in fig. 2.17.

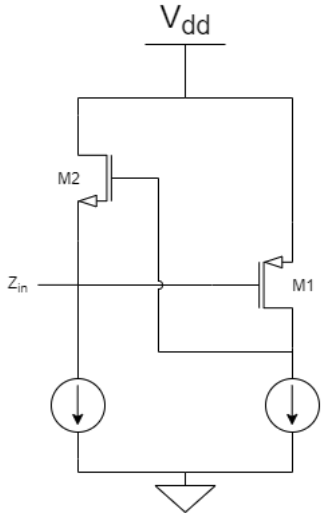


Figure 2.16: Lin-Payne active inductor.

In modern CMOS technologies the difference between the threshold voltages of the PMOS and NMOS transistors is significantly small resulting in a V_{DSsat2} lower than 50 mV implying that M1 is working in weak inversion reducing considerably the maximum frequency of such inductor [20]. This problem can be solved with the addition of a DC level shifter evidenced in fig. 2.17 through M3, increasing V_{DSsat2} and guaranteeing all transistors are working in the saturation region. The inductance impedance of this inductor deviates from the gyrator-C one and is expressed as:

$$Z_L(s) = s \cdot \frac{1}{g_{m1}} \cdot \frac{\frac{C_{gs2}g_{ds1}}{g_{m2}g_{m3}} + \frac{C_{gs3}g_{ds3}}{g_{m2}g_{m3}} - \frac{C_{gs2}g_{ds1}}{g_{m2}^2} + s^2\frac{C_{gs3}C_{gs2}}{(g_{m2}g_{m3})^2}(C_{gs2}g_{m3} + C_{gs3}g_{m2})}{(1 - s^2\frac{C_{gs2}C_{gs3}}{g_{m2}g_{m3}})^2 + s^2(\frac{C_{gs2}g_{m3}+C_{gs3}g_{m2}}{g_{m2}g_{m3}})^2} \tag{2.15}$$

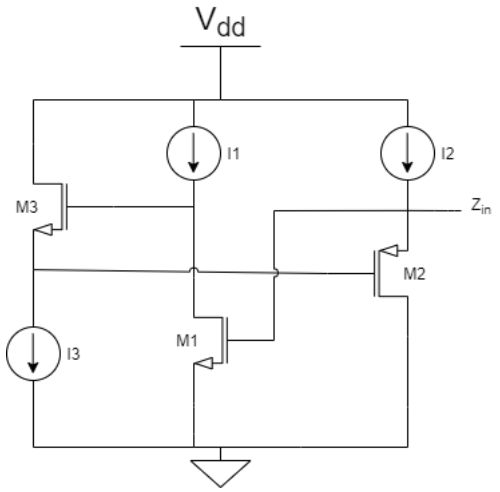


Figure 2.17: Improved Lin-Payne active inductor.

2.3.3 Yodprasit-Ngarmnil Active Inductor

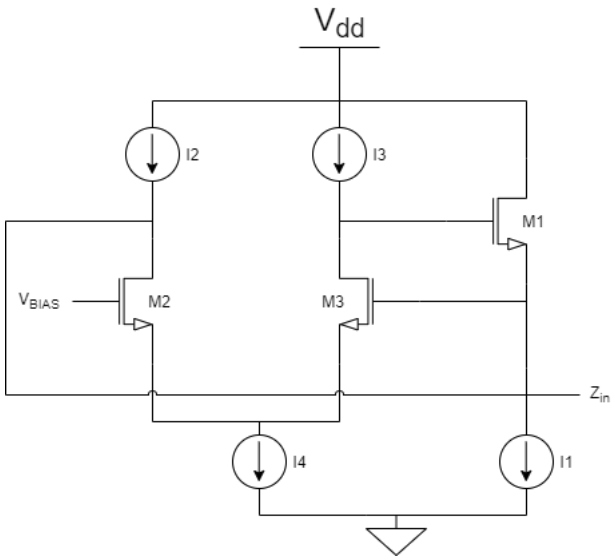


Figure 2.18: Yodprasit-Ngarmnil active inductor.

The following model implements a technique to reduce the ohmic loss of the inductor with the injection of a negative resistance and therefore increasing the Q of the circuit. This is achieved by replacing the CS transistor of a regular cascode active inductor with a differential pair of NMOS transistors as well as adding positive feedback into the circuit as shown in fig. 2.18 resulting in the introduction of a parallel resistance with value $\frac{-2}{g_{m2}}$ (considering $g_{m2} = g_{m3}$) significantly reducing the total resistance of the inductor while maintaining the same inductance value[21][22].

The final product has a Q resumed to

$$Q = \sqrt{g_{m2}g_{m2}C_{gs2}C_{gs2}}\frac{1}{C_{gs2}g_{ds2} + 2C_{gs1}g_{ds1}} \tag{2.16}$$

and can be easily tuned by varying $g_{m2,3}$ and $g_{ds2,3}$. Nevertheless, this has a direct impact on the inductance, therefore, cascodes are usually embedded in the differential pair facilitating the Q tunning.

2.3.4 High-Frequency Active Inductor

The last architecture features a compact active inductor offering many desirable specifications such as low voltage operation, high dynamic range, high Q, low noise and, most importantly, wide inductance band[23][24].

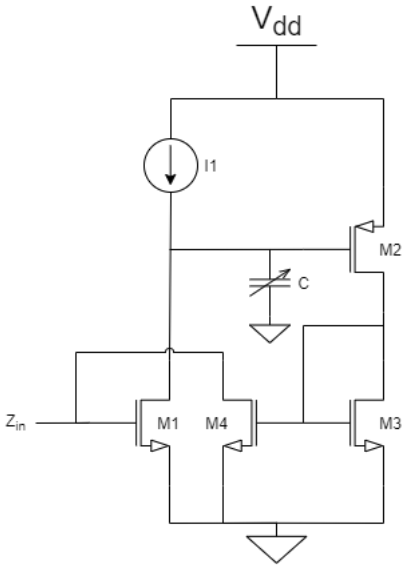


Figure 2.19: Compact high frequency active inductor.

This circuit, depicted in fig. 2.19, consists of two CS stages realized by transistors M1 and M2. Since it is based on the gyrator-c topology, the transconductance performed by M2 is inverted, in order to achieve a positive transconductance, through the current mirror composed by M3 and M4. This configuration relies on a minimum number of transistor drain terminals presenting low conductance values in critical nodes thus decreasing the series resistance of the inductor and enhancing the Q while improving the inductance value. Another advantage this design provides is the absence of body-effect in the transistors which would otherwise impact the transconductances of the related gyrator-c model.

The tunability of this inductor is proportioned by current biasing as well as by the varactor capacitance C introducing a dominant pole in the respective node improving the stability of the circuit. This circuit is also appealing in terms of noise since only M1 and M2 contribute directly to the input noise.

Reducing the size of the input transistor M1 results in a wider inductance band (due to the decrease of the input capacitance) as the inductance value remains unchanged

reaching SRF close to 10 Ghz, proving this topology to be suitable for RF applications.

2.4 State-of-the art Active Inductors

With the implementation of 5G, many communication systems assembled with integrated circuits require higher bandwidths, a problem engineers have been facing in recent years commonly adopting as a solution inductive shunt peaking[5]. As the passive inductors tend to have decaying performance at higher frequencies, dissipating a lot of magnetic energy as ohmic losses [25], engineers have turned themselves towards active approaches thus reducing chip area while adding noise and linearity problems into this systems.

This chapter will cover the most important active inductors developed in recent years designed to work at high frequencies while trying to minimize their inherent problems.

2.4.1 Active-Inductor-Based Termination Circuit for High-Speed I/O

As communication data rates between chips keep increasing, the parasitic capacitances at their boundaries become more impactful generating RC first-order filters in combination with the output resistance of the chip[2]. As the active inductors commonly used for bandwidth enhancement struggle to satisfy the required voltage headroom, the active inductor introduced in fig. 2.20 has been put forward.

The main structure of this inductor is formed with the PMOS transistor M1 and the active resistor M2, the advantage M1 offers is the nonexistence of body effect, this results in a lesser threshold voltage therefore allowing higher output swings when compared to NMOS inductors. This transistors are separated by a level shifter established with transistors M3 and M4 decreasing the voltage applied to the gate of transistor M1.

On perfect conditions the gain of the level shifter is equal to 1 and trough small-signal analysis the impedance of the inductor equates to:

$$Z_{in} = \frac{1 + j\omega(C_{gs}R)}{(g_m + g_{ds}) - \omega^2 RC_{gs}C_{ds} + j\omega(C_{gs} + RC_{gs}g_{ds})} \tag{2.17}$$

where all transistor parameters belong to M1 and R is the resistance of the transistor M2 working on deep-triode region. The approximated components of the equivalent RLC where R_p has been disregarded are the following:

$$L = \frac{RC_{gs}}{g_m + g_{ds}} \tag{2.18}$$

$$R_s = \frac{1}{g_m + g_{ds}} \tag{2.19}$$

$$C_p = C_{ds} \tag{2.20}$$

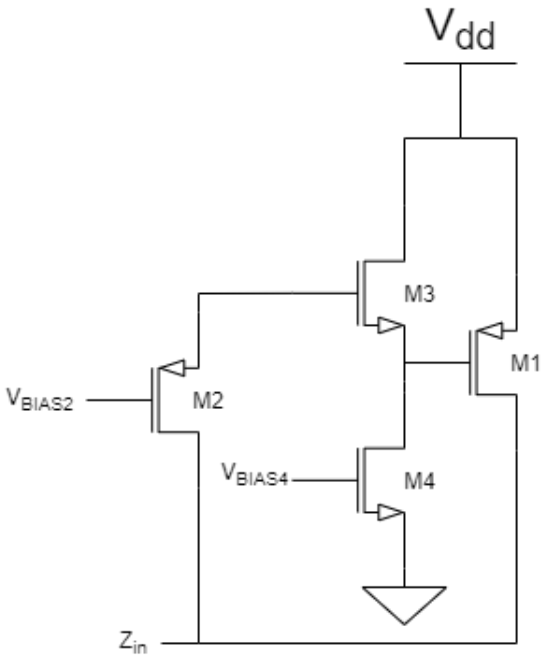


Figure 2.20: Active inductor for termination circuit.

The tunability of such inductor depends on the resistance value of M2 controlled by V_{g2} and bias current flowing through M1. As active inductors are very susceptible to linearity problems, and this inductor is no exception, a DC headroom voltage is applied to this circuit to ensure the g_m and g_{ds} oscillations are not excessive, allowing the inductor to handle large-signal swing. To achieve this without impacting the current-made-logic (CML) driver, the inductor extension responsible for alternating the tail current for data transmission (M_{diff1R} and M_{diff1L}), an additional differential current-source circuit containing the transistors M_{diff2R} and M_{diff2L} is appended

2.4.2 Low Voltage CMOS Active Inductor with Bandwidth and Linearity Improvement

In order to improve the bandwidth and linearity of the active inductor the following work, proposed by Priya Meharde *et al.* in [25], uses inductors to compensate the parasitic capacitances without affecting the low-frequency gain even showing better results in terms of noise performance.

Apart from the insertion of inductors, this circuit revolves around the idea of using a dynamic threshold MOSFET (DTMOS) to benefit from the device's high ft and transconductance as well as low supply voltage with the addition of a feed-forward current source technique (FFCS) to improve its linearity.

The DTMOS device

The DTMOS device is achieved by connecting the gate and body terminals of a MOSFET as depicted in fig. 2.20, this connection allows a forward body bias decreasing the threshold voltage of the MOSFET as the voltage between body and source terminals rises [26]. This configuration allows the transistor to work under low supply voltages while lessening the body effect.

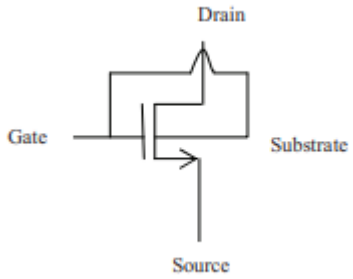


Figure 2.21: Dynamic threshold MOSFET[25].

Feed-forward current source technique

This technique aims to mimic an extra current arising from the drain current second order non-linearity, namely the most influential in linearity problems, and redirect it into the current source of the active inductor using "feed-forward". This will prevent V_{gs} offsets and diminish the effect of the extra current thus enhancing linearity[27].

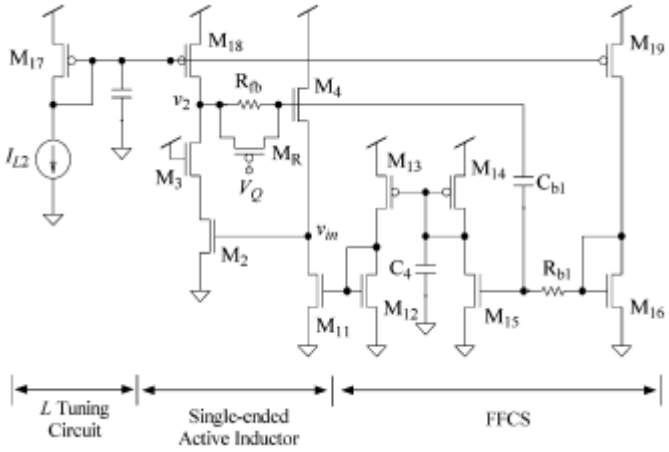


Figure 2.22: Feed-forward current source technique[27].

This is achieved in fig. 2.22 where the FFCS technique is applied to transistor M4. In this circuit, the extra current is duplicated by the transistor M15 and feed-forwarded into transistor M11 by means of current mirrors. This is only attainable if the V_{gs} of both M4

and M15 is the same, therefore the necessity of transistors M16 and M19 connected by a large resistor to not affect the performance of the active inductor.

Proposed active inductor

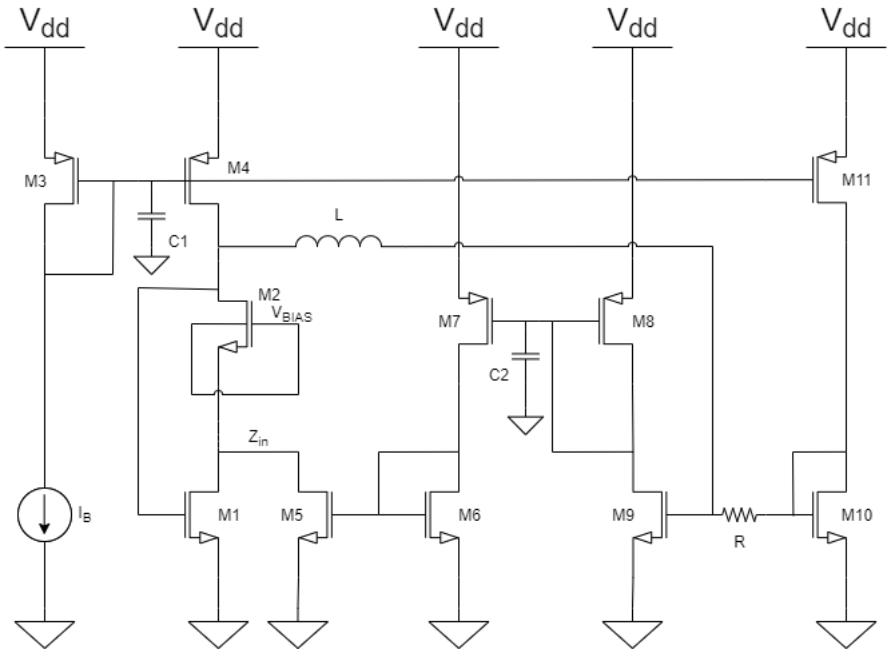


Figure 2.23: Active inductor with linearity and bandwidth improvement.

This circuit, displayed in fig. 2.23, is another variation of the NMOS CS-CG replacing the CG associated regular CMOS with a DTMOS. This substitution increased the non-inverting transconductance of the transistor M2 which resulted in an increment of its drain current thus increasing the resonant frequency of the inductor whose input impedance can be expressed as:

$$Z_{in} = \frac{C_{gs2}(C_{gs1} + g_{ds1} + g_{ds2})}{(C_{gs2} + \frac{C_{gs1}}{g_{m1}} + \frac{g_{ds1}+g_{ds2}}{g_{m1}})g_{m1}g_{m2} + C_{gs1} + g_{ds1} + g_{ds2}} \tag{2.21}$$

The inductance can be tuned by altering the current I_b in the current to voltage converter M3. The rest of the CMOS devices belong to FFSC circuit connected to the DTMOS device M2 as it is the most responsible for the linearity of the circuit. The L adjacent to this DTMOS transistor is a passive on-chip inductor carefully selected in order to not ruin the shunt peaking as its stray capacitance could possibly cause a detrimental effect regarding bandwidth.

2.4.3 CMOS High-Performance UWB Active Inductor

The two active inductors mentioned before present wide frequency ranges for low voltage operation and improved linearity, however, no efforts were put into noise reduction. On the other hand, the active inductor presented in fig. 2.24 is focused on achieving low noise results while reaching high SRF with bandwidth desirable for ultra-wideband (UWB) systems[28].

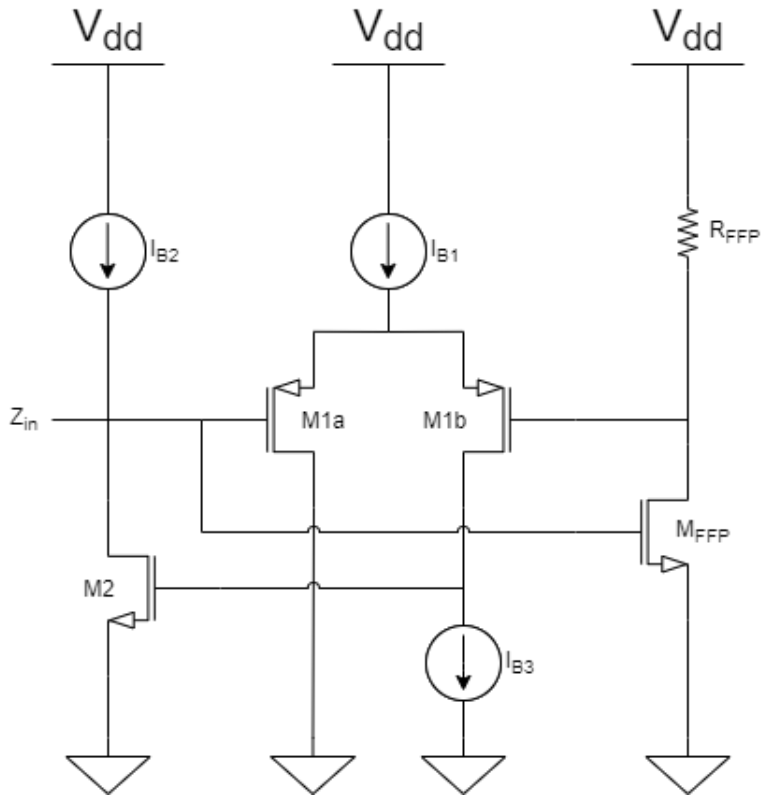


Figure 2.24: High-performance UWB active inductor.

This circuit incorporates two CS stages employing the gyrator-C model, the negative transconductance is obtained through a single transistor, M2, while the positive transconductance is achieved through the differential pair formed with transistors of the same size, M1a and M1b. It includes a feed forward path (FFP) as a technique to reduce both noise and loss. Since all transistors are configured as CS, one can expect low series resistance and therefore high Q.

Using an approximation consisting on considering g_m to be larger than $s \cdot c_{gs}$ for the desired range of frequencies, the RLC equivalent circuit can be described as follows:

$$L = \frac{2C_{gs2}}{g_{m2}g_{m1a}} \tag{2.22}$$

$$C_p = \frac{C_{gs1a}}{2} + C_{gsFFP} \tag{2.23}$$

$$R_p = \frac{1}{g_{ds2}} \tag{2.24}$$

$$R_s = \frac{2g_{ds1b}}{g_{m2}g_{m1a}} \tag{2.25}$$

The SRF of this inductor is calculated through 2.26 and can reach values above the 10 Ghz mark with some inductance cost proving to be suitable for bandwidth improvement at high-speed data communication systems.

$$SRF = \sqrt{\frac{1}{\frac{C_{gs1a}}{2} + C_{gsFFP}} \frac{g_{m2}g_{m1a}}{2C_{gs2}}} \tag{2.26}$$

Noise improvement

For noise calculation only the thermal noise is considered since the flicker noise is neglected at high frequencies. Representing the random motion of electrons, the channel current thermal noise in a CMOS transistor can be written by:

$$\overline{I_d^2} = 4kT\gamma(g_m) \tag{2.27}$$

where γ represents the channel excess noise factor, k the Boltzman constant, and T the temperature in Kelvin. Therefore, the total input referred noise current can be expressed as:

$$\overline{I_{n,in}^2} = 4kT\gamma(\frac{2}{g_{m1a}Z_{in}^2} + g_{m2}) \tag{2.28}$$

From 2.28 one can notice that reducing g_{m2} and increasing g_{m1a} improves the noise figure of the inductor. This last transconductance can be increased with extra bias current I_{BIAS1} or by enlarging the transistor channel width, however such methods result, respectfully, in more power consumption while being limited by the velocity saturation that would collapse g_{m1a} if the current reaches high values, and lower SRF due to the enlargement of parasitic capacitances. In order to improve the noise performance without the referred drawbacks the FFP is implemented. For performance evaluation, the effect of the transistor M2 is neglected since its contribution remains the same whether the circuit is benefiting from the FFP or not.

The equivalent transconductance of the differential pair and the corresponding output noise current are expressed as

$$G_m = \frac{g_{m1a}}{2} \tag{2.29}$$

$$\overline{I_{n,out}^2} = 4kT\gamma(g_{m1a}2) \tag{2.30}$$

With the addition of the FFP the equivalent transconductance is now represented by

$$G_m = \frac{(1 + R_{FFP} g_{mFFP}) g_{m1a}}{2} \tag{2.31}$$

resulting in the following output noise current where a_{FFP} is equivalent to the gain of the FFP ($a_{FFP} = g_{FFP} \times R_{FFP}$)

$$\overline{I^2_{n,out}} = 4kT\gamma(g_{m1a}2) + kt\gamma(\frac{a_{FFP}(a_{FFP} + \frac{1}{\gamma})g^2_{m1a}}{g_{m1FFP}}) \tag{2.32}$$

Comparing 2.29 with 2.31 it is possible to deduce that for the same equivalent gain, g_{m1a} with FFP is smaller than g_{m1a} without by a ratio of $1 + a_{FFP}$ meaning that both the bias current and aspect ratio of the correspondent transistor can be reduced by same ratio. Taking all this into account, the noise ratio (NR), for $\gamma = \frac{4}{3}$ can be approximated by

$$NR \simeq \frac{1}{1 + a_{FFP}} + \frac{a_{FFP}}{(1 + a_{FFP})\sqrt{12k(\frac{1}{1+a_{FFP}} + \frac{I_{FFP}}{I_{BIAS}}(1 + a_{FFP}) - 1)}} \tag{2.33}$$

where k corresponds to the ratio between the FFP and differential pair transistors aspect ratios. Increasing this ratio diminishes the noise but decreases the SRF, therefore there is a trade off when taking into account this approach.

2.4.4 Non-Gyrator Type Active Inductor

This work differs from the typical gyrator-c model as it includes a third current source compensating the current arising from the resistor component of the equivalent RLC circuit and aiming to achieve a pure inductive response[6].

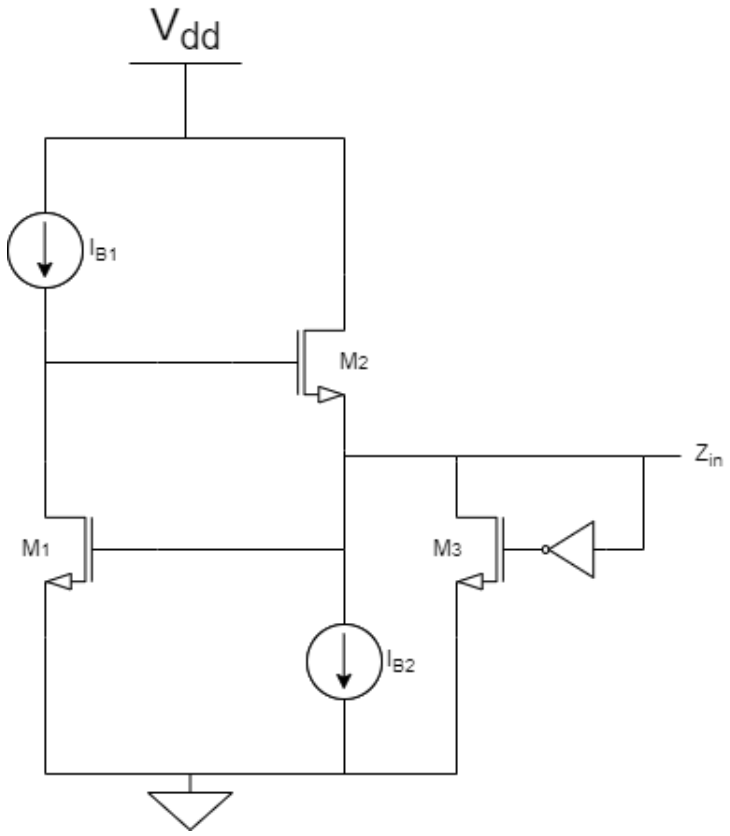


Figure 2.25: Active inductor with extra current source for resistance decrease.

This new technique is based on a regular two-transconductances active inductor generated through transistors M1 and M2 in which is added an extra current-source by means of a transistor M3 as depicted in fig. 2.25, whose admittance can be approximately described as:

$$Y_{in} = g_{m1} - g_{m3} + \frac{g_{m1}g_{m2}}{C_{gs2}s} + C_{gs1}s \tag{2.34}$$

Therefore achieving an input impedance that does not include a series resistor component. However, in order to attach this third transistor with negative gain a forth transistor has been added as a cascode of transistor m1 as shown in fig. 2.26 providing a $-\frac{g_{m1}}{g_{m6}}$ gain and achieving the final admittance of

$$Y_{in} = g_{m1} - \frac{g_{m1}g_{m3}}{g_{m6}} + \frac{g_{m1}g_{m2}}{C_{gs2}s} + C_{gs1}s \tag{2.35}$$

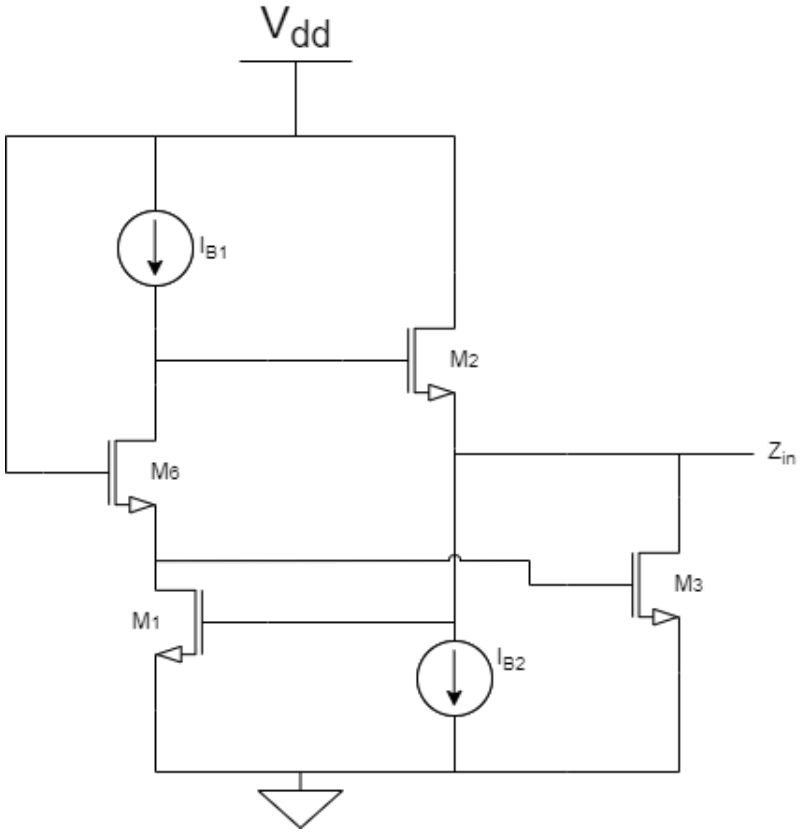


Figure 2.26: Non-gyrator type active inductor.

And since the series resistor effect is so substantially small this is an active inductor that achieves excellent Q that can be expressed as

$$Q = \left(\frac{1}{g_{m1}} - \frac{g_{m1}g_{m3}}{g_{m6}}\right)\sqrt{\frac{C_{gs1}}{C_{gs2}}}\sqrt{g_{m1}g_{mw}} \tag{2.36}$$

The tunability of this inductor mostly depends on the current of transistor m3 achieving Q as high as 4 for a SRF of 3 GHz and a maximum SRF of 5 GHz for Q above 1.

2.4.5 A tunable, power efficient active inductor-based 20 Gb/s CTLE in SerDes for 5G applications

The last work addressed in this state of the art features a Continuous Time Linear Equaliser (CTLE) implemented with simple active inductors performing inductive peaking around the frequency of 10 GHz [5].

CTLE

As previously discussed, the equalizer is responsible for adding some gain at higher frequencies compensating the channel bandwidth limitations. Equalizers can be separated between linear and non-linear equalizers, the first one associated with a finite

response as opposed to the second one. The linear equalizers are further divided between Discrete Time Linear Equalisers (DTLE) and CTLE. The difference lies in the dependency of clocks retrieved from the received data turning the DTLE a CDR dependent circuit. The CTLE however does not require a CDR circuit directly working on the high speed data.

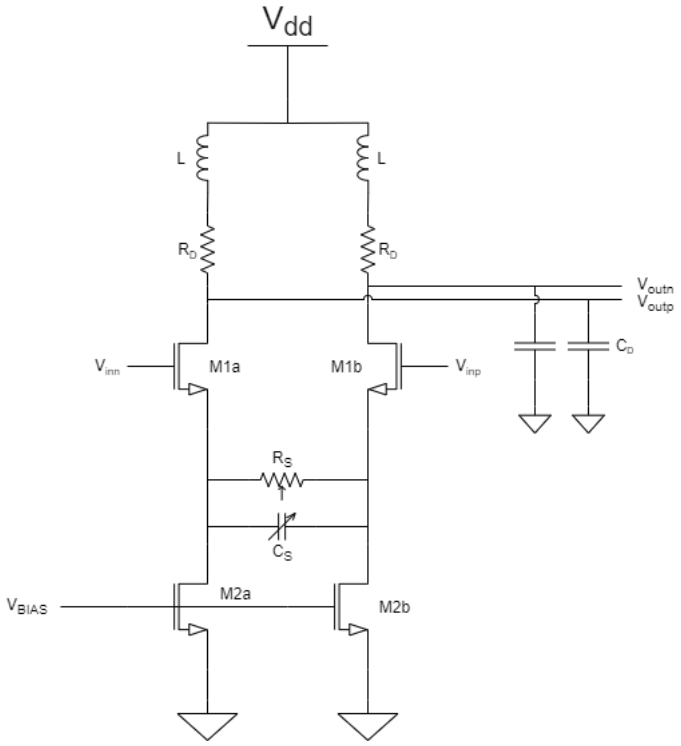


Figure 2.27: Continuous Time Linear Equaliser with passive inductor loads.

The active CTLE presented in fig. 2.27 forms one zero at:

$$\omega_z = \frac{1}{R_s C_S} \tag{2.37}$$

and two poles with the transfer function peaking at Nyquist frequency generating a -40 dB/decade slope afterwards. Those poles being located at:

$$\omega_{p1} = \frac{1 + \frac{g_m R_S}{2}}{R_S C_S} \tag{2.38}$$

$$\omega_{p2} = \frac{1}{R_D C_D} \tag{2.39}$$

The idea behind the usage of the active inductor in this circuit is to compensate one of the poles with a zero therefore enhancing the bandwidth of the CTLE without consuming as much on-chip area as a passive inductor would.

Active inductor based load

The active inductor implemented in the differential load depicted in fig. 2.28 has a very simple but effective design comprising a CS stage and a resistance formed by two transistors working in deep triode region (R_D). The impedance associated with this circuit is:

$$Z_{in} = \frac{sRC_{gs} + 1}{sRC_{gs} + g_m} \tag{2.40}$$

With a zero at ($\frac{1}{RC_{gs}}$) and pole at ($\frac{g_m}{RC_{gs}}$) from which, one can deduce the elements of a RL circuit:

$$R_p = R \tag{2.41}$$

$$L = \frac{RC_{gs}}{g_m - \frac{1}{R}} \tag{2.42}$$

$$R_s = \frac{1}{g_m - \frac{1}{R}} \tag{2.43}$$

However, to show an inductance characteristic, the condition $g_m > \frac{1}{R}$ must be obeyed at the desired frequency of 10 GHz[29].

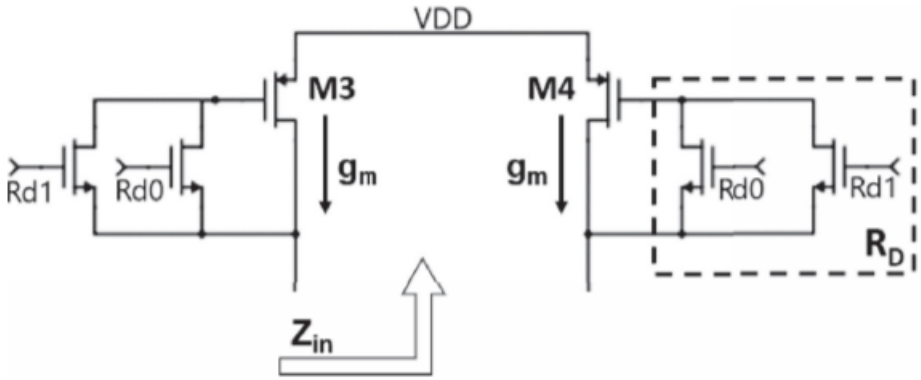


Figure 2.28: The active inductor based load impedance of the CTLE[5].

This active inductor based CTLE is designed with 28 nm CMOS technology allowing tunability between a range of 7 GHz to 20 GHz.

2.4.6 Comparison Between Discussed Active Inductors

To conclude the state-of-the art review, a comparison between performances of the previously addressed works whose SRFs are exhibited in table 2.1 will be given indicating the strengths and weaknesses in each design in table 2.2.

Table 2.1: Self-resonant frequencies of the explored works

Active inductors	[2]	[25]	[28]	[6]	[5]
Technology	90 nm	180 nm	180 nm	130 nm	28 nm
SRF	10 GHz	25 GHz	11.2 GHz	5 GHz	20 GHz

Table 2.2: Strengths and weaknesses of the covered inductors

Active inductors	Strengths	Weaknesses
[2]	Simplicity of design Low area consumption Low voltage operation Good linearity	Low inductance High noise Low Q
[25]	High bandwidth High SRF Good Linearity	High noise High area consumption High voltage operation High power dissipation Employs a passive inductor
[28]	High inductance value High bandwidth Low noise High tunability High Q	Bad linearity High voltage operation
[6]	Low series resistance value High Q High inductance value	Low SRF Can behave as an oscillator
[5]	High SRF Simplicity Low voltage operation	Low inductance value Low Q

3

Analysis of Active Inductors Topologies

Throughout this chapter analysis of some previously discussed active inductor topologies will be covered, giving an insight on their response to the different sizing of the elements that compose them.

These simulations were ran using *Synopsys* software with 16 nm technology that includes FinFETs with a minimum length of 14 nm resulting in a improvement of the results found by the authors of the topologies included in this chapter.

3.1 Thanachayanont-Payne Active Inductor Analysis

The first active inductor simulated is the one presented in fig. 2.12. In order to derive the expressions that allow one to create the equivalent RLC circuit, this design can be simplified using a small-signal model depicted in fig. 3.1, considering C_{gs} (parasitic capacitance between gate and source of a transistor) to be significantly larger than the other parasitic capacitances, therefore, rendering them irrelevant to the characterization of this inductor.

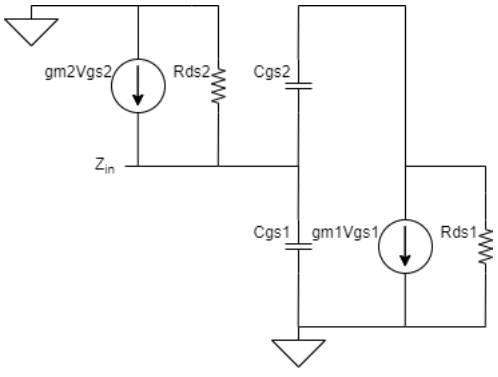


Figure 3.1: Small-signal model of Thanachayanont-Payne active inductor.

From fig. 3.1 one can derive the following input admittance expression:

$$Y_{in} = \frac{g_{m2}g_{m1}}{g_{ds1} + sC_{gs2}} + g_{ds2} + \frac{g_{m1}sC_{gs2}}{g_{ds1} + sC_{gs2}} + sC_{gs1} \tag{3.1}$$

From which, at lower frequencies way below the resonant frequency the usual components described in equations 2.3 to 2.6 can be extracted.

$$L = \frac{C_{gs2}}{g_{m1}g_{m2}} \tag{3.2}$$

$$C_p = C_{gs1} \tag{3.3}$$

$$R_p = \frac{1}{g_{ds2}} \tag{3.4}$$

$$R_s = \frac{g_{ds1}}{g_{m2}g_{m1}} \tag{3.5}$$

Through this RLC components it becomes obvious that the R_s can be decreased with the reduction of g_{ds1} (DC drain-source conductance). Since g_{ds1} is directly proportional to $\frac{I_{ds}}{L}$, where I_{ds} is the DC drain current of a transistor and L is its length, one can achieve higher Q factors with transistors with bigger lengths, however, this incurs a huge loss when it comes to the resonant frequency. Another way to reduce this resistance is by lowering the current flowing through transistor m1. This current variation also impacts g_{m1} resulting in an increase of the inductive component of the circuit, the Q can be further increased through the manipulation of the current and size of transistor m2 at the expense of SRF.

The tunability of this active inductor through current manipulation can be seen in figs. 3.2 and 3.2. These curves were obtained with transistors m1 and m2 both having a width of 200 nm for the minimum length.

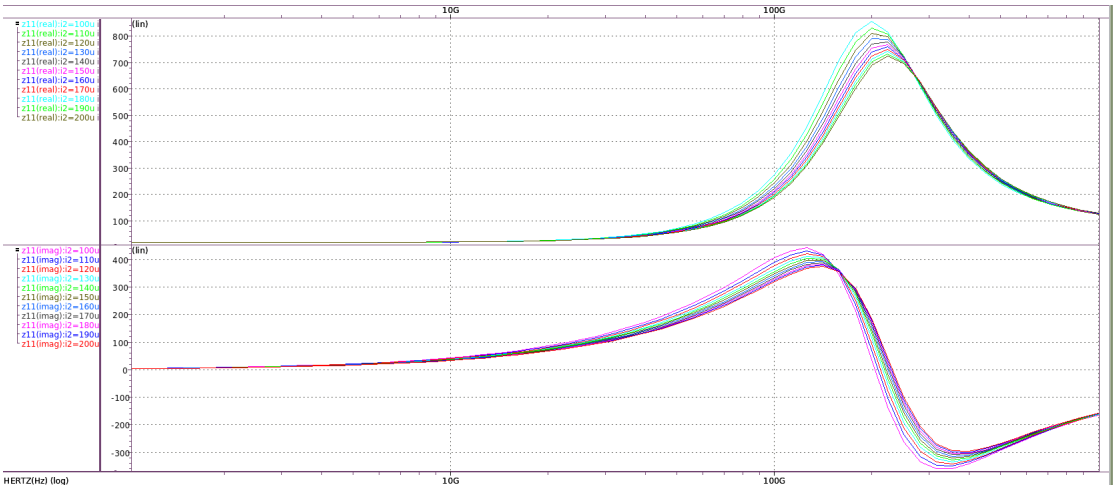


Figure 3.2: Variation of $Re(Z_{in})$ on top and $Im(Z_{in})$ on bottom with current on Thanachayanont-Payne active inductor.

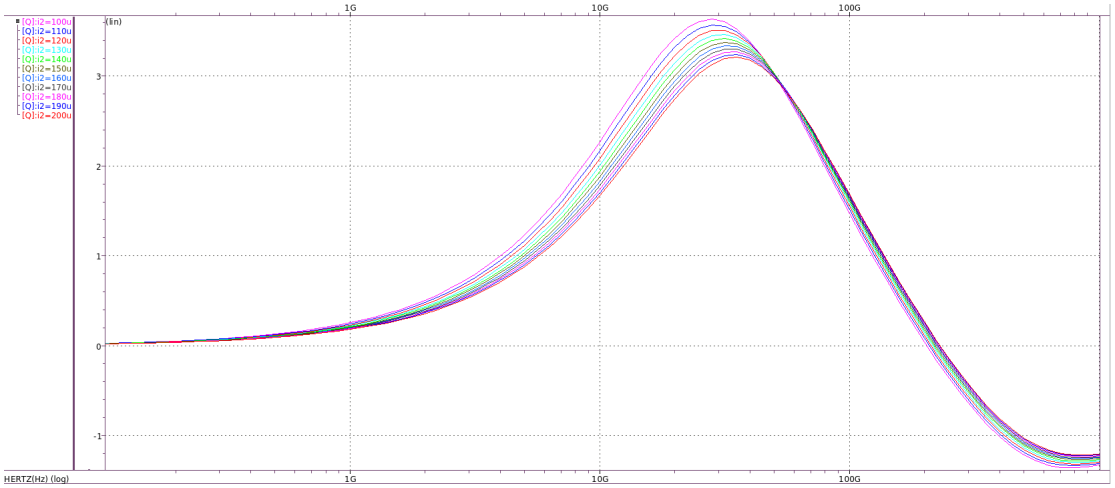


Figure 3.3: Variation of Q with current on Thanachayanont-Payne active inductor.

As previously explained the increase of the current in transistor m1 (I_2) from 100 µA to 200 µA resulted in a decrease of the $Re(Z_{in})$ as well as a smaller decrease of $Im(Z_{in})$ and consequently Q with an enhancement of more or less 50 GHz in SRF. To complete the simulation of this inductor the outcome of the change in size of transistor m2 can be watched in figs. 3.4 and 3.5.

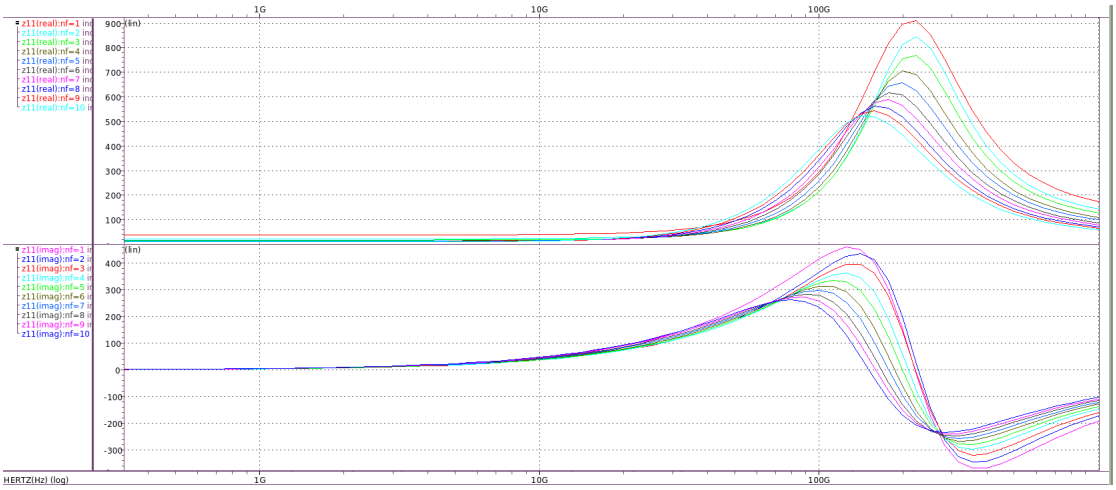


Figure 3.4: Variation of $Re(Z_{in})$ on top and $Im(Z_{in})$ on bottom with transistor m2 size on Thanachayanont-Payne active inductor.

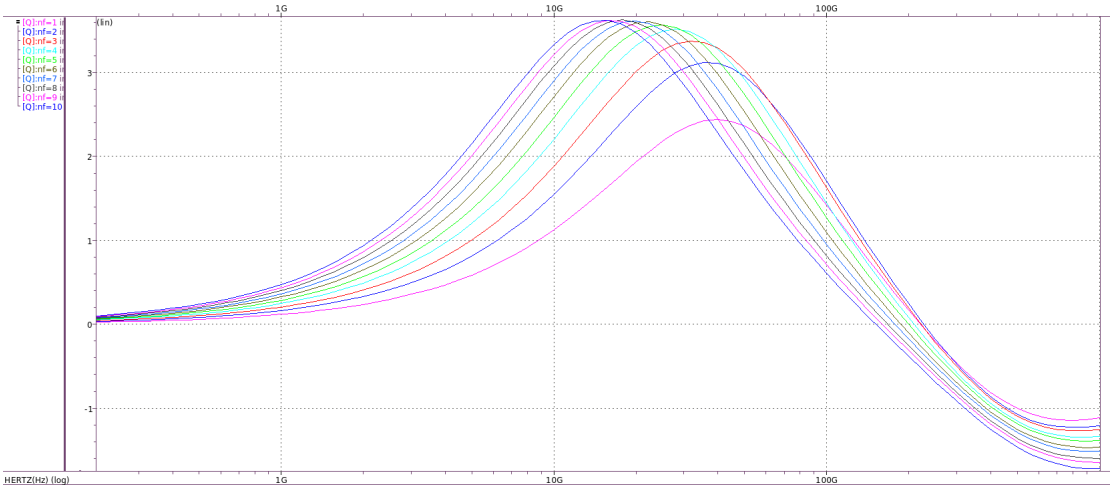


Figure 3.5: Variation of Q with transistor m2 size on Thanachayanont-Payne active inductor.

The examination of these simulations allows one to conclude that a larger transistor m2 results in a smaller inductance with a reduced SRF, however this allows to achiever better Q.

3.2 High-Frequency Active Inductor Analysis

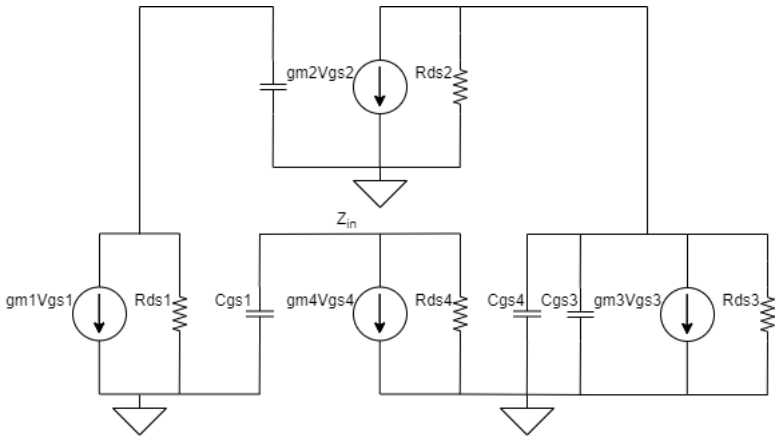


Figure 3.6: Small-signal model of high-frequency active inductor.

Similar to the inductor mentioned before this circuit (fig. 2.19) can be simplified, using the same transistor model, into a small-signal equivalent circuit to break it into the RLC components, fig. 3.6, considering C_{gs2} irrelevant in the presence of the varactor capacitance C, from which one can extract the following input admittance:

$$Y_{in} = sC_{gs1} + g_{ds4} + \frac{g_{m1}g_{m2}g_{m4}}{g_{m3}sC + s^2(C_{gs3} + C_{gs4})C + g_{ds1}g_{m3}} \tag{3.6}$$

Hence leading approximately to a circuit split into the components:

$$L = \frac{g_{m3}C}{g_{m1}g_{m2}g_{m4}} \tag{3.7}$$

$$C_p = C_{gs1} \tag{3.8}$$

$$R_p = \frac{1}{g_{ds4}} \tag{3.9}$$

$$R_s = \frac{g_{ds1}g_{m3}}{g_{m1}g_{m2}g_{m4}} \tag{3.10}$$

Compared to the sizing of the author in [23], this circuit had the input bias voltage reduced to 400 mV to comply with a supply voltage of 800 mV, the current was also changed to 400 µA in order to make a viable comparison with the preceding active inductor. Both this changes required an adjustment in the size of transistor m1, going from an aspect ratio of 33 (W_1=4 µm, L_1=0.12 µm) to 78 (W_1=1.25 µm, L_1=16 nm). The rest of the transistors kept the aspect ratios described in the article being proportionally shrunk to fit the minimum channel length of 16 nm.

The varactor plays an important role when it comes to the inductive value of the circuit as shown in expression 3.7 therefore influencing the Q of the inductor, however, despite bringing more stability to the circuit this capacitance has a detrimental effect on the SRF as shown in figs. 3.7 and 3.8.

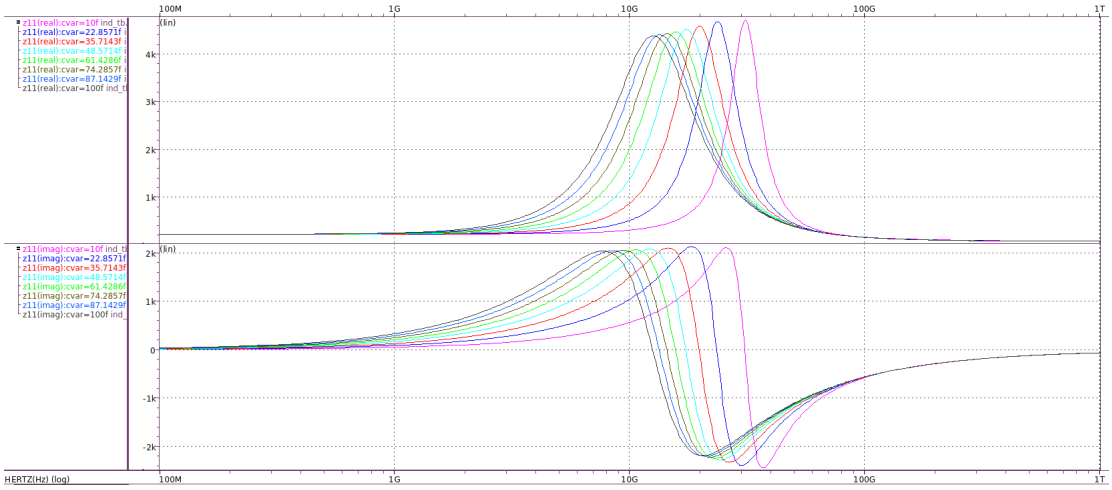


Figure 3.7: Variation of $Re(Z_{in})$ on top and $Im(Z_{in})$ on bottom with varactor's capacitance on high-frequency active inductor.

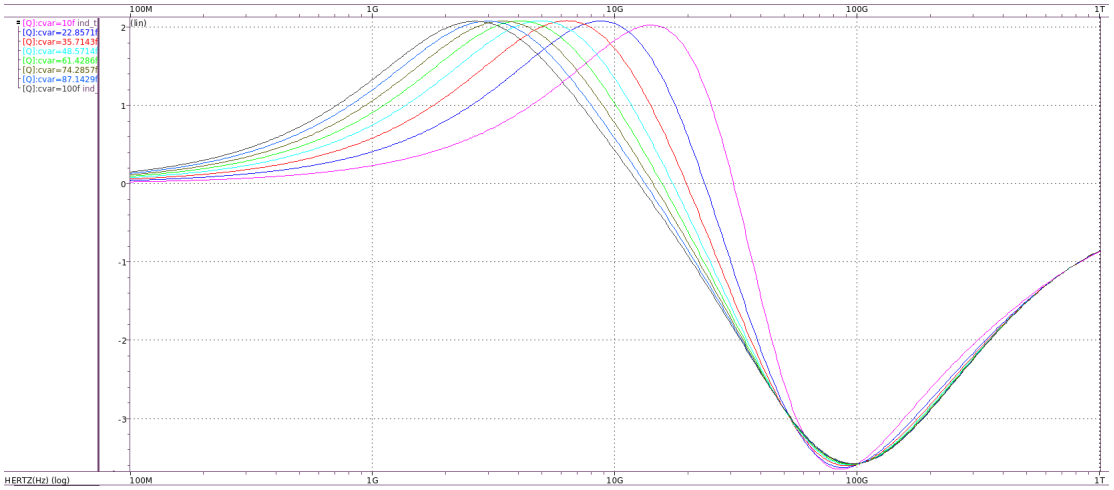


Figure 3.8: Variation of Q with varactor's capacitance on high-frequency active inductor.

An effective way to boost both inductance, Q and SRF of the circuit is by increment of the biasing current, figs. 3.9 and 3.10, hitting a quality factor and SRF inferior to the earlier active inductor but demonstrating higher values of inductance for the same power consumption.

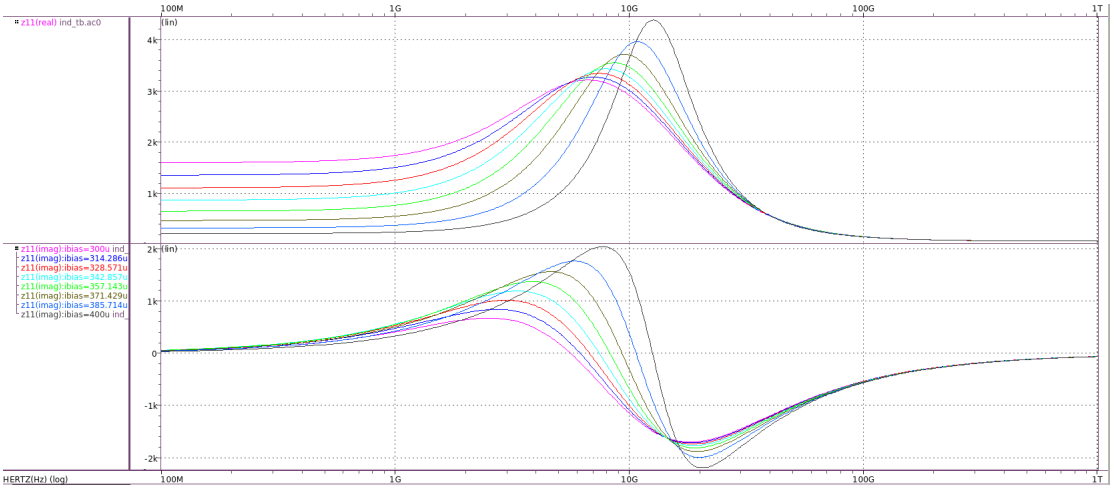


Figure 3.9: Variation of $Re(Z_{in})$ on top and $Im(Z_{in})$ on bottom with I_1 on high-frequency active inductor.

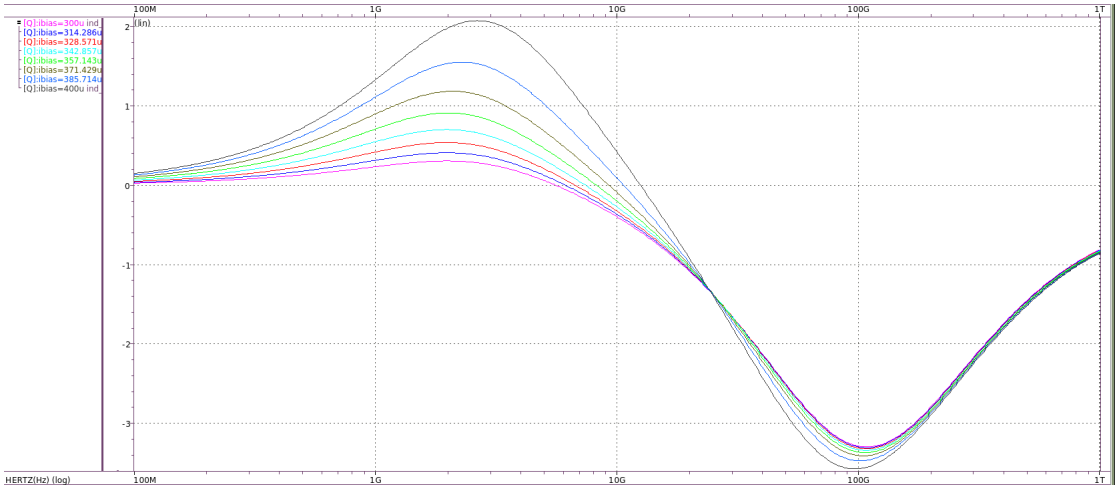


Figure 3.10: Variation of Q with I_1 on high-frequency active inductor.

3.3 Simple Active Inductor Analysis

The simplest active inductor design employed in section 2.4.5, portrayed in fig. 3.11, is actually the one achieving the best SRF results in the same conditions as the prior simulated circuits, however, the lack of Q and inductance values is noticeable.

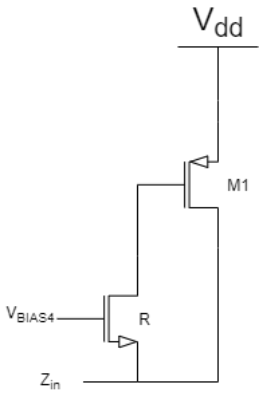


Figure 3.11: Simple active inductor circuit implemented in section 2.4.5.

When looking at expressions 2.42 and 2.43 it is evident that the sizing of transistor m1 has direct implications on both inductance and resistance characteristics of the circuit, nonetheless, it is only obvious that the second one reduces with the increment of m1's width while both C_{gs} and g_m rely on it indicating that the inductance and Q of said circuit have small variations. This can be seen in figs. 3.12 and 3.13.

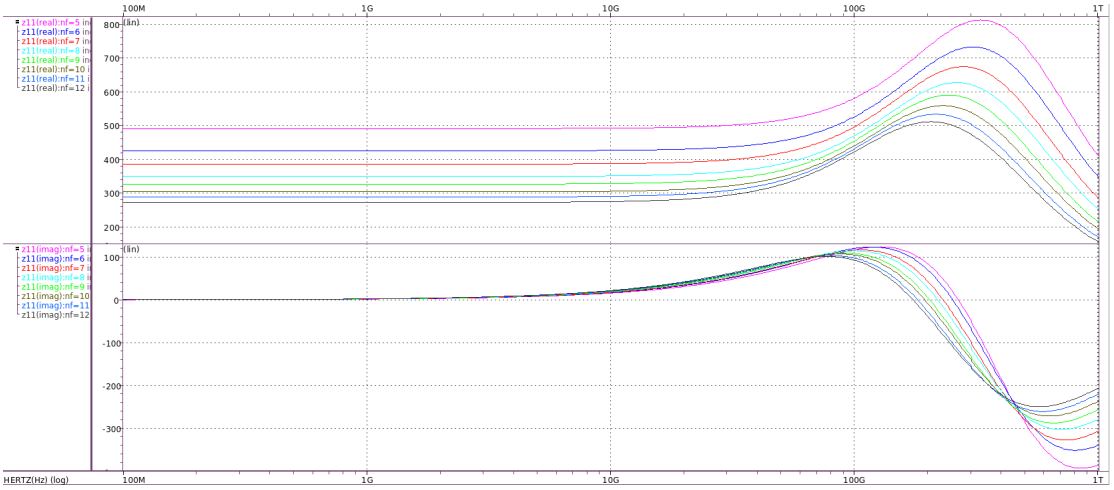


Figure 3.12: Variation of $Re(Z_{in})$ on top and $Im(Z_{in})$ on bottom with transistor m1 size on simple active inductor.

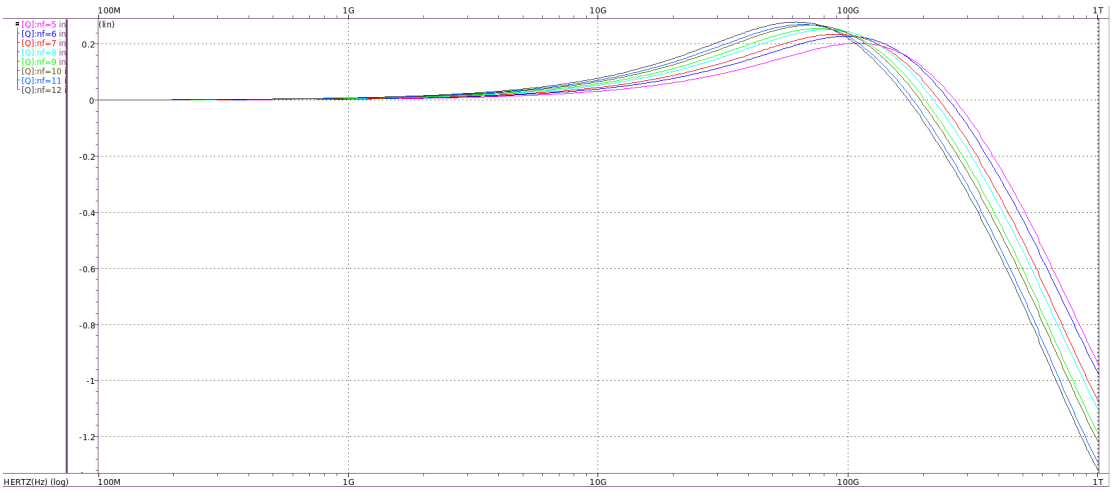


Figure 3.13: Variation of Q with transistor m1 size on simple active inductor.

On the other hand, the variation of the resistance value of R has no impact whatsoever in the overall resistance value at frequencies well bellow the SRF, fig. 3.14, working as a Q and inductance enhancer it also limits the bandwidth of the inductor seeing that it is inversely proportional to both zero and pole frequencies as shown in the simulation in fig. 3.15 ran on a transistor m1 whose width is equivalent to 900 nm.

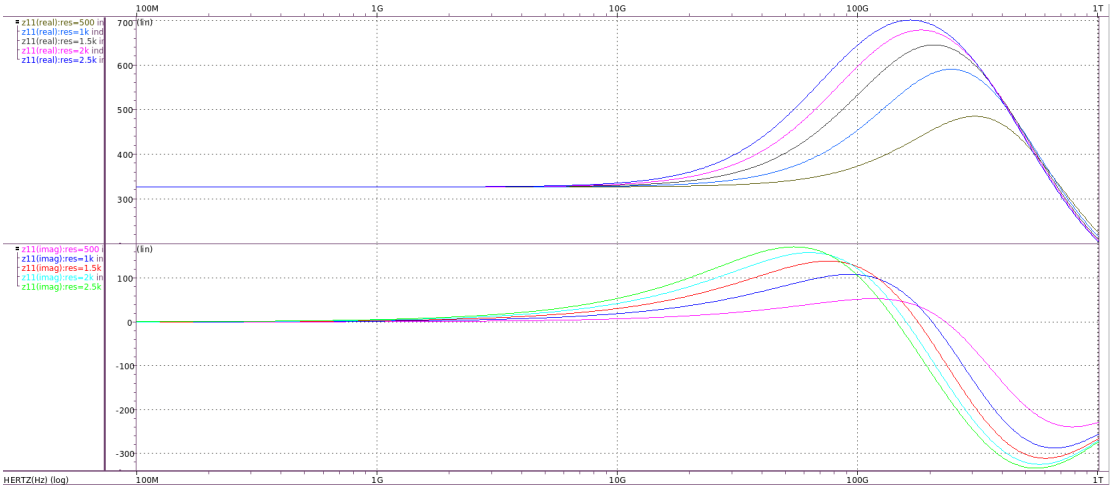


Figure 3.14: Variation of $Re(Z_{in})$ on top and $Im(Z_{in})$ on bottom with R value on simple active inductor.

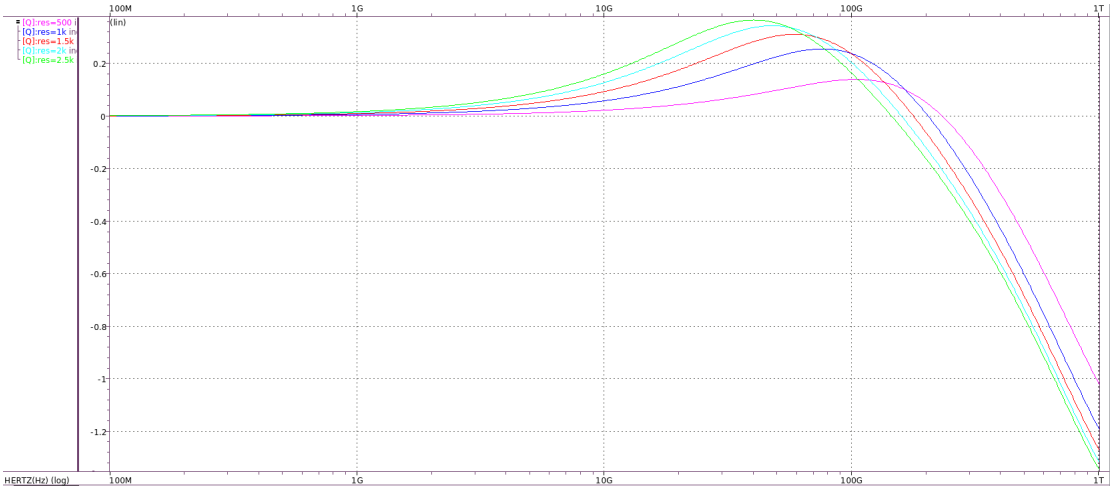


Figure 3.15: Variation of Q with R value on simple active inductor.

3.4 Non-Gyrator Type Active Inductor Analysis

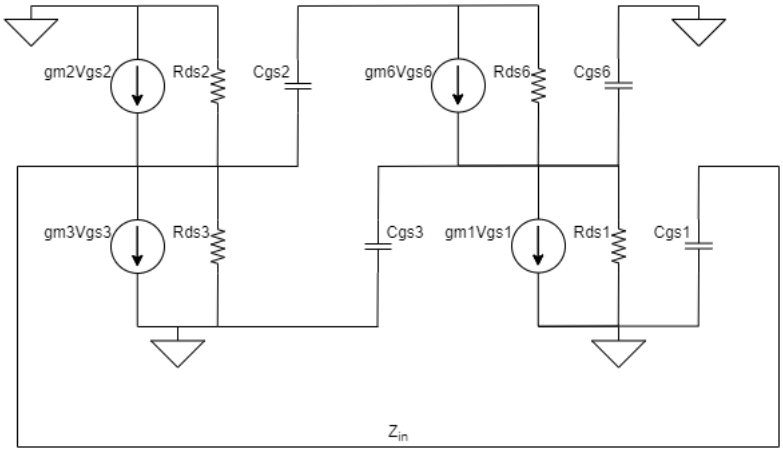


Figure 3.16: Small-signal model of non-gyrator type active inductor.

The final active inductor covered on this section, presented in fig. 2.26, is the most complex out of all the discussed circuits. Its simplified model, drawn in fig. 3.16, leads to the following input admittance:

$$Y_{in} = sC_{gs1} - \frac{g_{m3}g_{m1}(sC_{gs2}+g_{ds6})}{s^2C_{gs2}(C_{gs3}+C_{gs6})+g_{m6}sC_{gs2}} + (sC_{gs2}+g_{m2})(1+\frac{g_{m6}g_{m1}}{s^2C_{gs2}(C_{gs3}+C_{gs6})+g_{m6}sC_{gs2}} - \frac{sC_{gs2}}{sC_{gs2}+g_{ds6}}) \quad (3.11)$$

For low frequencies this expression ends up matching the expression 2.35 indicating that the circuit should exhibit a weak resistive response for frequencies lower than the SRF hence manifesting high Q. This phenomenon is derived from the existence of transistor m3 and one can see its influence looking at figs. 3.17 and 3.18.

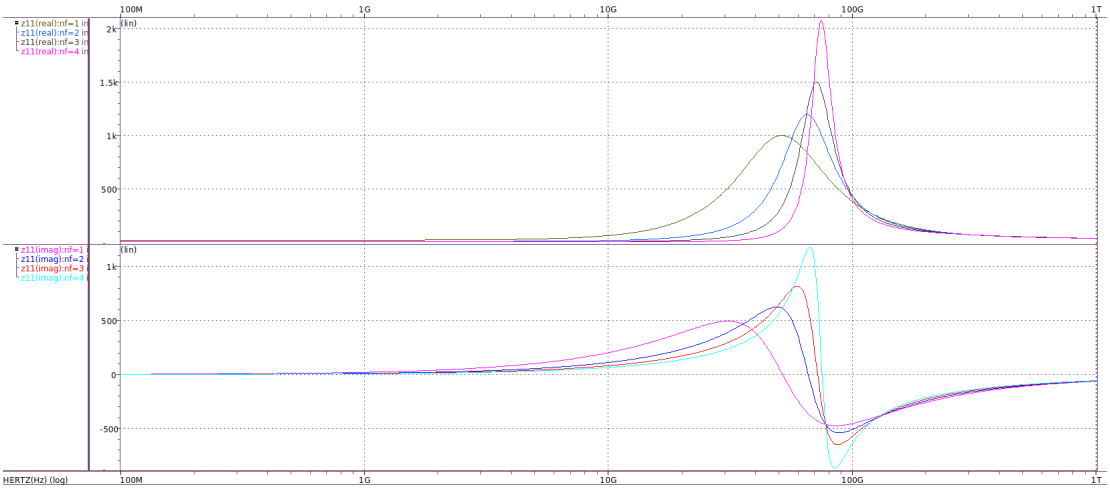


Figure 3.17: Variation of $Re(Z_{in})$ on top and $Im(Z_{in})$ on bottom with transistor m3 size on non-gyrator type active inductor.

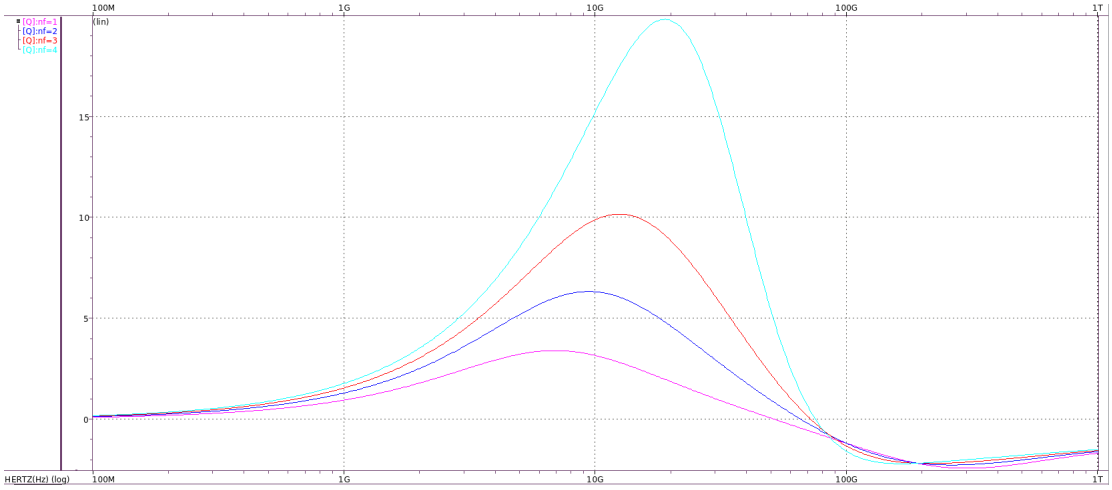


Figure 3.18: Variation of Q with transistor m3 size on non-gyrator type active inductor.

These responses were obtained using the aspect ratios of the author in [6], with an increase of the current consumed by the inductor, dividing this current in 50 µA for the m2 and m3 branch and 350 µA as a tunable biasing current that was later on varied from a range of 50 µA to 450 µA to produce figs. 3.19 and 3.20.

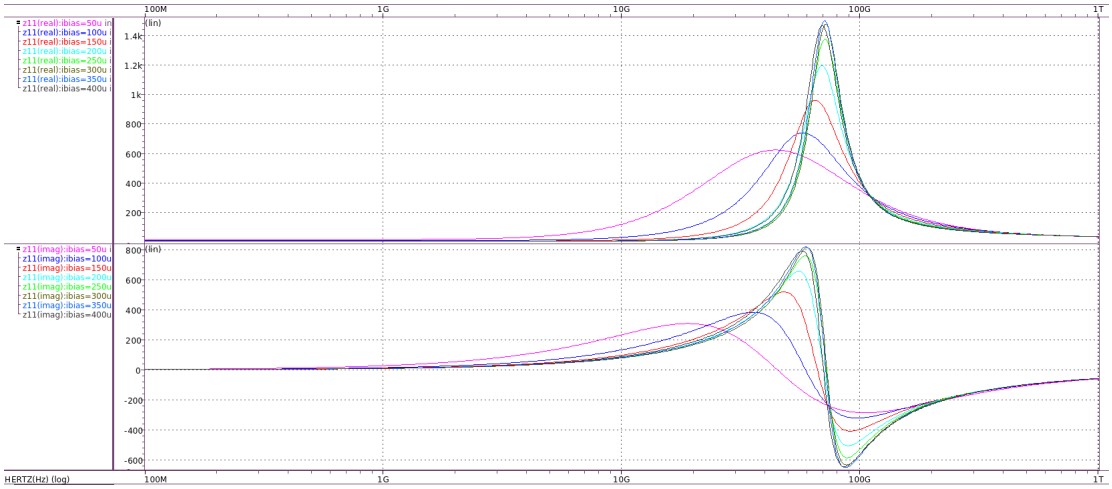


Figure 3.19: Variation of $Re(Z_{in})$ on top and $Im(Z_{in})$ on bottom with biasing current on non-gyrator type active inductor.

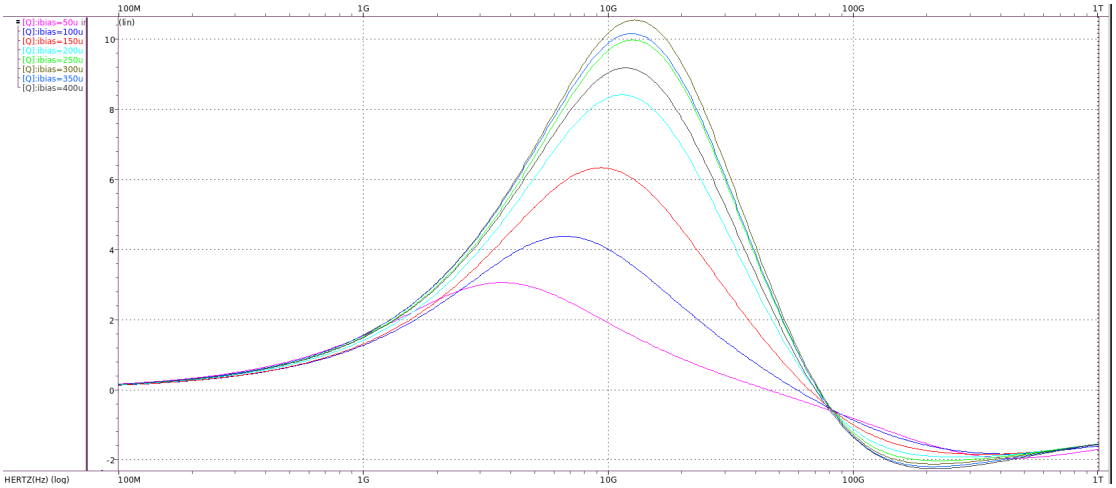


Figure 3.20: Variation of Q with biasing current on non-gyrator type active inductor.

As we can see in the results of this simulations this active inductor presents the best Q despite having an inductive bandwidth that does not reach the 100 GHz under ideal conditions.

4

TX Driver with Active Inductors

This chapter is devoted to the development of the main project consisting in the insertion of active inductors in an output driver to evaluate the benefits of this component. It is separated in three sections the first being an introduction to the driver that is going to serve as the study object, the second being a comparison between the proposed driver with active loads and a driver with a different active inductor included and the final section being the full circuit implementation and layout design of the covered driver.

4.1 The Current Mode Logic Driver

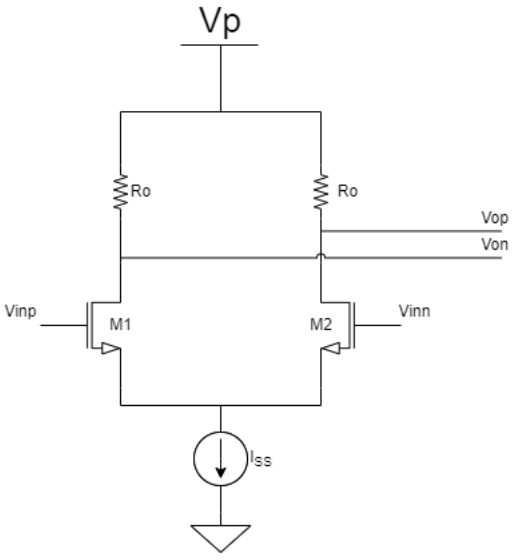


Figure 4.1: Circuit design of an ideal CML driver.

The chosen driver to implement an active inductor is a current-mode logic driver, or CML driver, due to its frequent use in high speed serial links powered with low supply voltages [4]. It is based on a simple differential architecture with passive loads that dictate both the output impedance of the driver and its output swing, fig. 4.1. The biasing of the circuit is independent from the inputs and can be achieved with the current-source

that provides the driver with a tail current, I_{ss}, that also defines, in conjunction with the passive loads, R_o, the differential output swing of the circuit:

$$OS = 2R_o I_{ss} \tag{4.1}$$

meaning that an input varying from 0V to V_p originates a single-ended output voltage comprised between V_p and $V_p - R_o I_{ss}$ respectively, fig. 4.2.

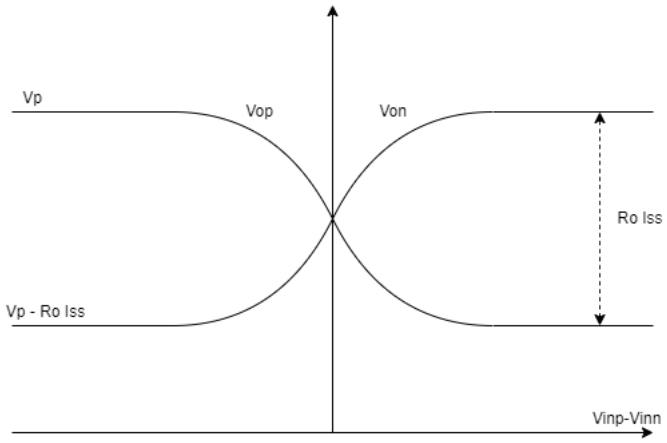


Figure 4.2: Transfer characteristics of the CML driver.

Despite being responsible for defining the output swing, the passive loads are set to 50Ω as they represent approximately the output impedance of the driver, such termination is desirable to match the usual impedance of the transmission line minimizing the reflection of electromagnetic waves and maximizing the energy transference. Another important characteristic influenced by the output resistances is the gain of the circuit that can be expressed as:

$$G = 2\frac{g_{m1,2}}{g_{ds1,2} + \frac{1}{R_o} + sC_o} \tag{4.2}$$

and given the fact that the drain resistance of a transistor is close to infinite one can simply the gain into

$$A_v = -2\frac{g_{m1,2}}{\frac{1}{R_o} + sC_o} \tag{4.3}$$

Where C_o corresponds to all the parasitic capacitances associated with the output node. In fig. 4.1 C_o is mainly constituted by the contribution of the small parasitic capacitance formed in between the terminals drain and gate of the transistor creating a pole in

$$\omega_p = \frac{1}{R_o C_o} \tag{4.4}$$

However, under real circumstances, the parasitic capacitances inherent to the datapath that succeeds the output node of the TX driver need to be taken into account.

For simulation purposes a capacitance of 0.5pF was introduced in the output node to simulate the described effect increasing C_o to the point where the influence of the transistor's parasitic capacitances becomes negligible limiting the driver to a bandwidth of

$$f_p = \frac{1}{2 * \pi * 50 * 0.5 * 10^{-12}} \simeq 6.4Ghz \tag{4.5}$$

with the improvement of this value via addition of active inductors being the objective of this thesis.

4.1.1 CML Driver with an ideal current source

An ideal current source requires no voltage headroom hence allowing the node that connects both transistor sources to have a constant voltage of 0V behaving like a virtual ground seeing that both transistors have identical sizes in this balanced differential pair. This allows the driver's inputs to receive a full rail-to-rail clock signal oscillating between 0V and power supply's 800mV voltage.

In order to achieve a differential 800mV output swing one can obtain through equation 4.1 a tail current equal to 8mA and in order to attain a gain close to 0dB, the output signal having the same amplitude as the input signal, g_m must be approximately 20mS obeying equation 4.3. As for the sizes of transistors m1 and m2, since the technology is so small, the models become very complex to estimate the transistor properties through calculations. An alternative approach was used, making a sweep of the width of a singular transistor biased with predetermined V_{gs} and V_{ds} in the simulation environment demonstrated in fig. 4.3.

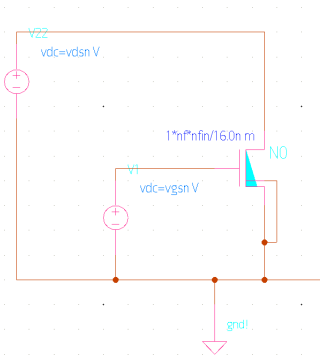


Figure 4.3: Simulation environment of a transistor.

From this environment one can extract the variation of threshold voltage, V_{th}, saturation voltage, V_{dsat}, I_{ds}, DC gate transconductance, g_m, and g_{ds} and notice that 14 number of fingers on a transistor with multiplicity of 2, corresponding to 7µm of width, give the closest g_m to the desired value.

Under all this conditions the driver exhibits the frequency response of fig. 4.4 limited by a bandwidth of 6.54GHz, frequency corresponding to a gain drop of 3dB, close to what was expected.

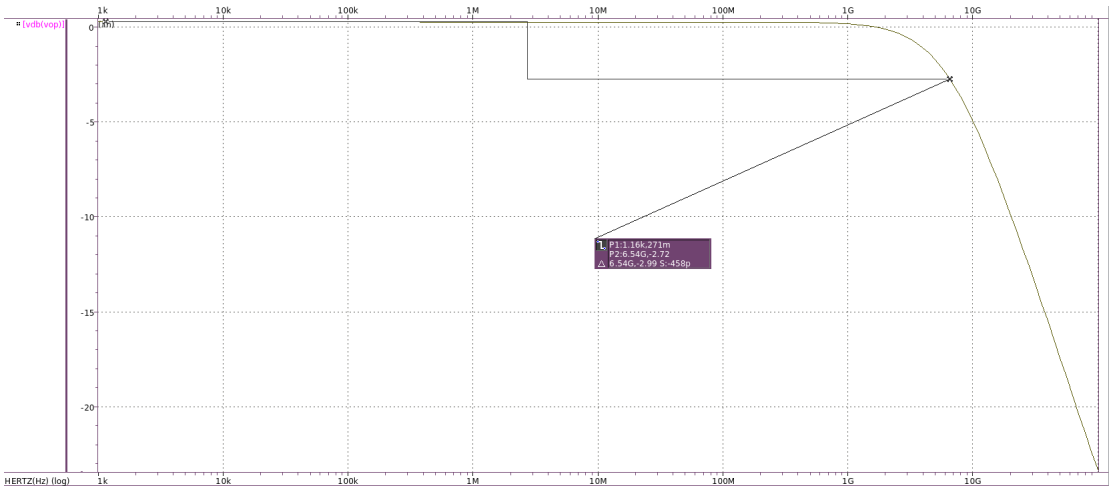


Figure 4.4: Frequency response of the ideal CML driver.

On the time domain, a clean output of 800mV peak-to-peak output with 1ns period is generated with a half period delay (since both transistors are in CS configuration which results in a 180° phase change) out of ideal pulse generators with a rectangular signal of frequency 1GHz producing fig. 4.5.

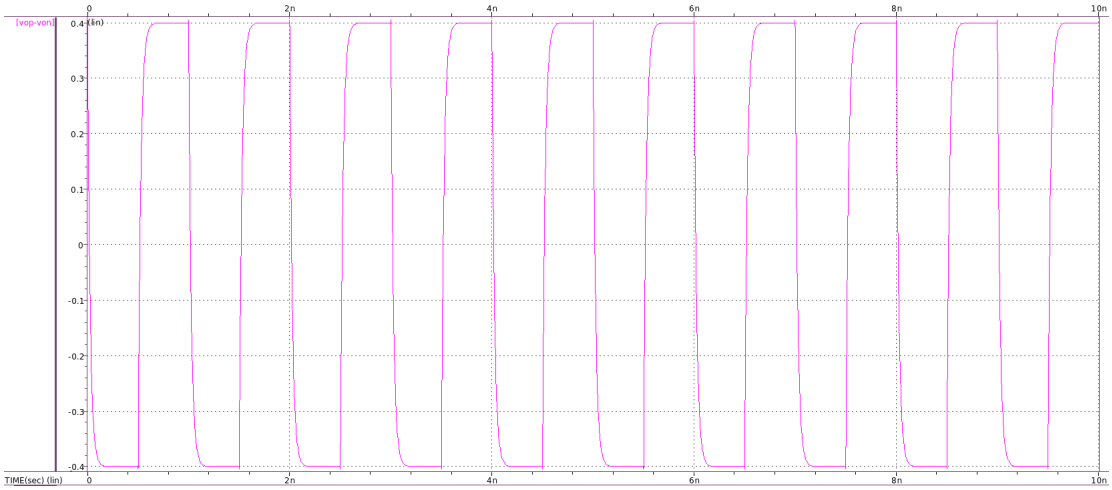


Figure 4.5: Time response of the ideal CML driver.

4.1.2 CML Driver with a real current source

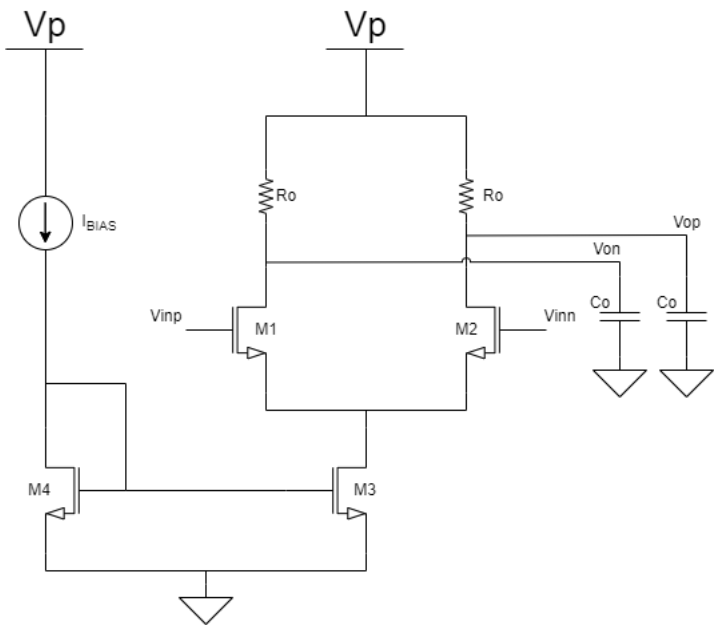


Figure 4.6: Circuit design of a CML driver biased with a current mirror.

As the ideal current source is replaced by a current mirror, fig. 4.6, some problems start to arise and the design of the driver becomes no longer trivial. This is due to the fact that by inserting a transistor m3 responsible for defining the current I_{ss} the node shared by m1 and m2 can no longer drop below the V_{ds} required for it to work on the saturation region.

This condition that all transistors must obey in order to achieve a proper operation of the CML driver is

$$V_{ds} > V_{gs} - V_{th} \tag{4.6}$$

ensuring at the same time that all transistors are on implying that

$$V_{gs} > V_{th} \tag{4.7}$$

For this conditions to be fulfilled the formerly 800mV input source must be limited to a smaller input swing having its DC voltage increased and giving the current mirror enough voltage headroom to keep it in the saturation region. However, given the high current of the circuit, m1 and m2 react with high V_{gs} creating a tendency for m3 to leave this region working close to the limit between saturation and triode.

The input signal is then limited between 800mV and 300mV which translates into a DC voltage increase of 150mV giving the DC operating points of the transistors organized in table **??**.

This upgrade to the CML driver will originate a similar response to the previous driver design as intended with the AC analysis shown on fig. 4.7.

Table 4.1: DC operating point of CML driver without active inductors

element	W[µm]	L[nm]	Ids[mA]	gm[mS]	Vgs[mV]	Vds[mV]	Vth[mV]
m1=m2	8.5	16	4.08	26.98	448.72	444.76	246.44
m3	4*17.68	16	8.16	107.16	313.3	151.28	247.97
m4	17.68	16	2.4	32.19	313.3	313.3	244.85

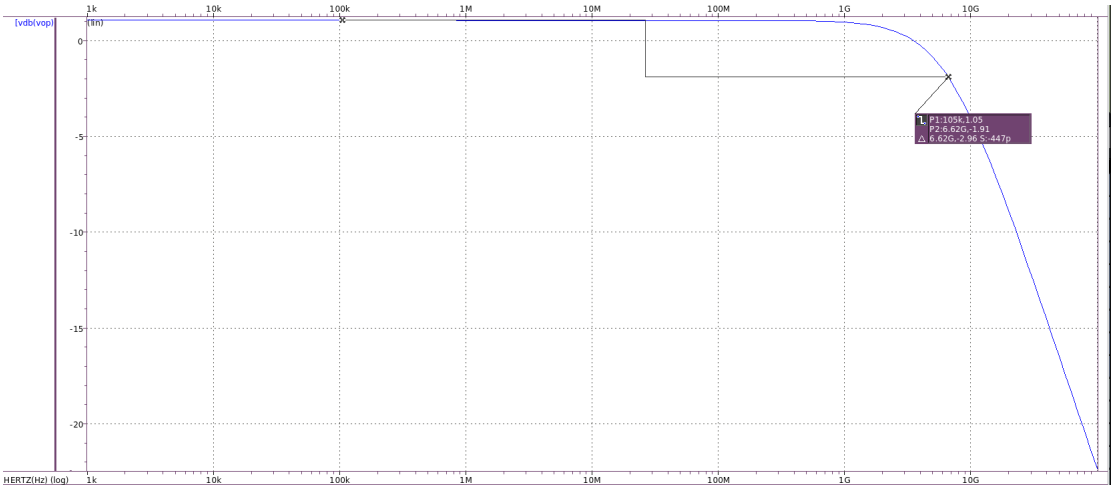


Figure 4.7: Frequency response of the CML driver.

4.2 CML Driver With Active Inductors

As mentioned before the aim of this work is to test the influence of active inductors on this CML driver. In this section two configurations will be presented, simulated and compared. The first one replaces the driver's resistive loads with active ones whose topology is described in sections 2.4.5 and 3.3 whilst the second one maintains the resistive loads introducing in the output node the active inductor described in sections 2.4.4 and 3.4.

4.2.1 Proposed CML driver with active loads

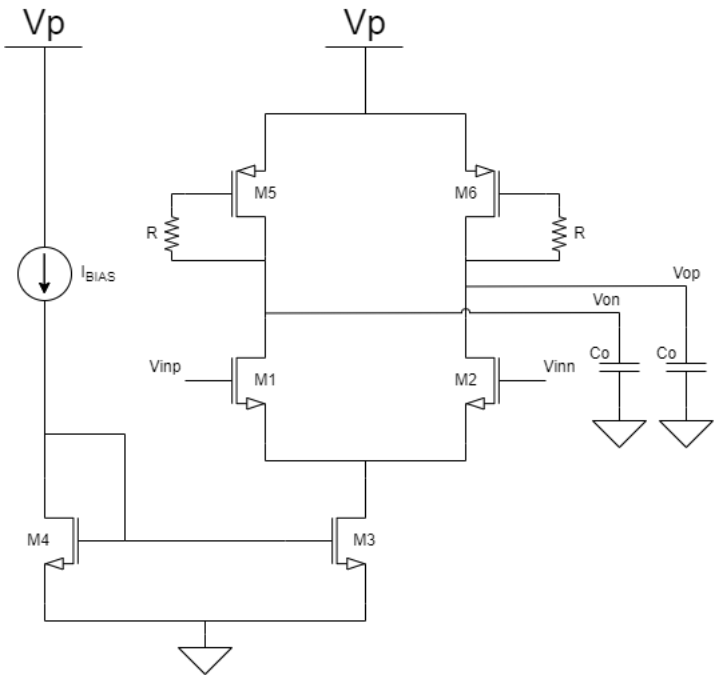


Figure 4.8: CML driver with active loads.

The idea behind the proper functioning of the circuit proposed in fig. 4.8 resides in the fact that the load can behave as a resistance at low frequencies and as an inductor at high frequencies. This implies that the size of the active element must be adequately sized in order to present a stable 50 Ω input impedance for frequencies below 6 GHz, frequency of the driver's pole that corresponds to its bandwidth, thereby maintaining the termination matching.

Based on equation 2.43 this impedance is achieved when the PMOS device demonstrates a g_m close to 20mS considering a R large enough to not interfere in this calculations, in this case a 1KΩ p-poly resistor was used.

Another requisite that the active load must comply is that the inductor's zero must match the driver's pole therefore guaranteeing the best bandwidth enhancement. In order to do so, a capacitor C was introduced in between the gate and source terminals of the transistor raising C_{gs}. The value of this capacitor can be derived from the inductor's zero equation:

$$f_z = \frac{1}{RC2\pi} \tag{4.8}$$

Matching this frequency to 6.4 GHz one finds that C must be sized to achieve a capacitance value of approximately 26 fF.

Proceeding to the sizing of the PMOS device another simulation environment similar to fig. 4.3 with a forced current I_{ds} of 4 mA and with both drain and gate terminals connected was utilized allowing one to obtain a desirable width of 6 µm.

A problem arises from this inductor as the current flowing through the PMOS device will force a certain V_{gs} therefore forcing the driver's DC output voltage. Under the established conditions this voltage is around 250 mV giving the driver active devices very little voltage headroom to work with. For this reason, the current supplied by the current mirror was reduced via an iterative process causing some changes around the active devices that compose this circuit including a reduction of the input DC voltage to ensure all transistors keep working in the saturation region.

The final sizes of the transistors as well as their DC parameters are displayed in table 4.2

Table 4.2: DC operating point of CML driver with active loads

element	W[µm]	L[nm]	Ids[mA]	gm[mS]	Vgs[mV]	Vds[mV]	Vth[mV]
m1=m2	15.03	16	3.69	32.92	380.97	206.56	246.92
m3	88.4	16	7.39	84.74	316.45	69.03	249.40
m4	17.68	16	2.5	32.87	316.45	316.45	244.79
m5=m6	5	16	-3.69	18.6	-524.41	-524.41	-235.12

This circuit design originates the following simulation results.

Frequency response

On fig. 4.9 it is represented the influence of the active inductor on the CML driver (represented as pink) as it adds a curvature to the AC signal at frequencies where the regular driver's response (represented as blue) starts to decay showing a bandwidth extension from 6.5 GHz to 10.1 GHz. Also important to denote that the circuit now presents a small gain of 2.89 dB before hitting a maximum of 5.1 dB at 4.5 GHz due to the inductive peaking.

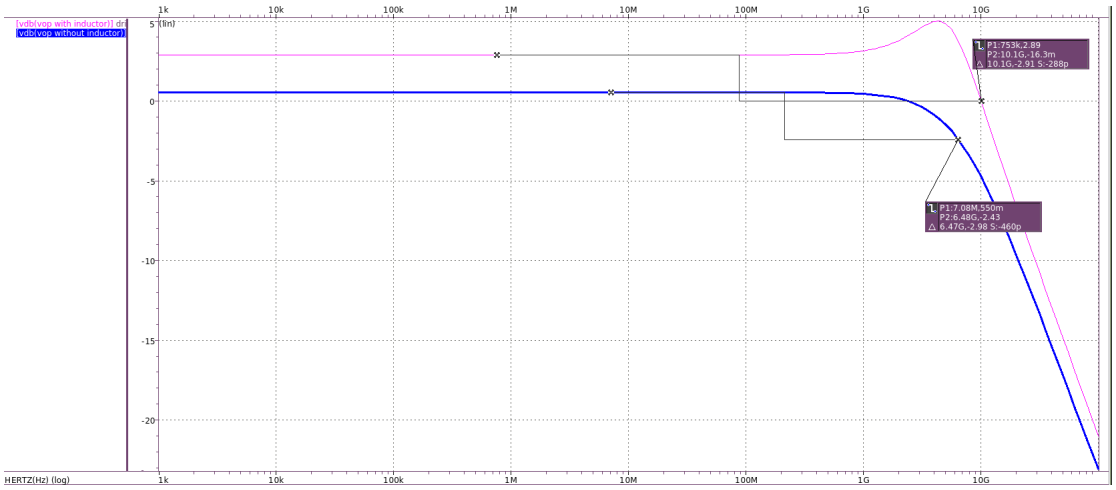


Figure 4.9: Frequency analysis comparison between CML driver with active loads as pink and original CML driver as blue.

To evaluate the robustness of the circuit to process voltage and temperature, PVT, variations the circuit was also submitted to a corners simulation testing the circuit in extreme situations. The process variations occur when a transistor has a set of characteristics turning the device slower or faster while the voltage variations account for the range of voltages provided by the power supplier. The circuit is simulated in four different extremes for process variations, ss, sf, fs and ff, with NMOS devices represented by the first letter being fast (f) or slow (s) and PMOS devices being represented by the second one with the range of process variations being determined by the foundry. To each of this cases is also verified a variation of +-10 % of the supply voltage V_p and a variation of temperature from -40 °C to 125 °C thereby giving origin to sixteen corners.

The sixteen corners are displayed in fig. 4.10. demonstrating a gain range between -1.85 dB and 4.24 dB with small implications on the bandwidth of the circuit that fluctuates between 9.95 GHz and 11.7 GHz.

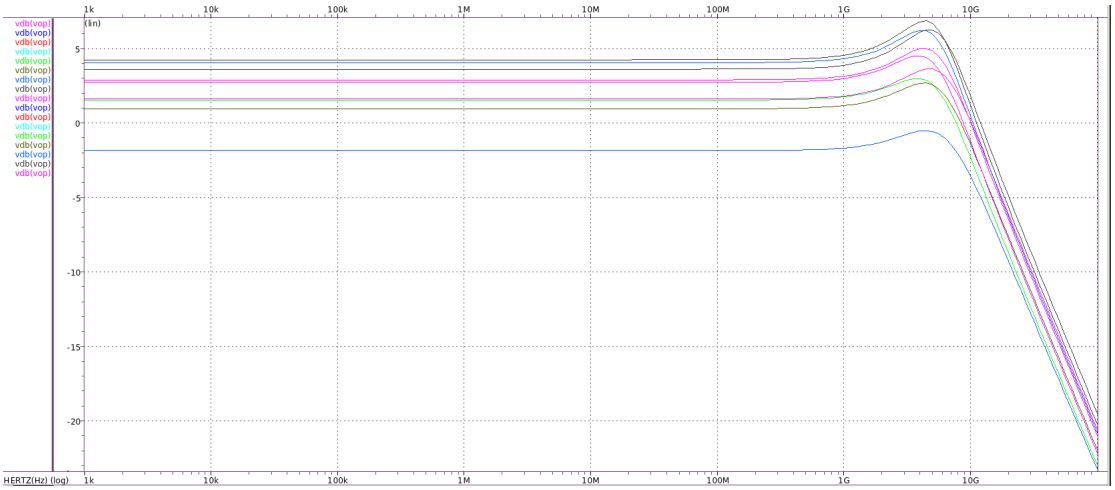


Figure 4.10: Frequency analysis for PVT variations of CML driver with active loads.

The output impedance of this circuit can be seen in fig. 4.11 proving this circuit to be well adapted to the transmission line exhibiting 50Ω at a frequency of 7.02 GHz before decaying to 33.9 Ω at the bandwidth frequency.

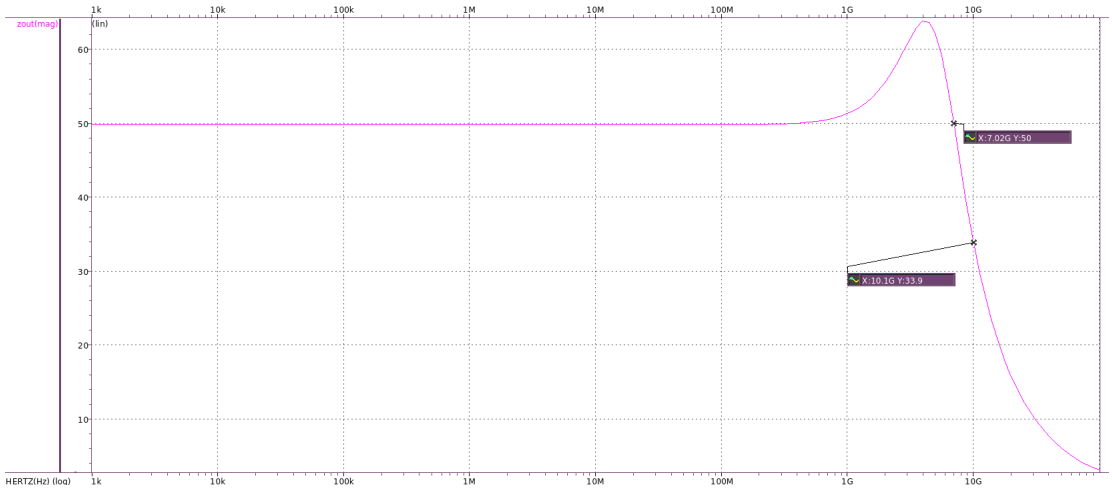


Figure 4.11: Termination evolution in frequency of CML driver with active loads.

The corners simulation of the termination is presented in fig. 4.12 showing a range of impedances between 42.4 Ω and 55.6 Ω.

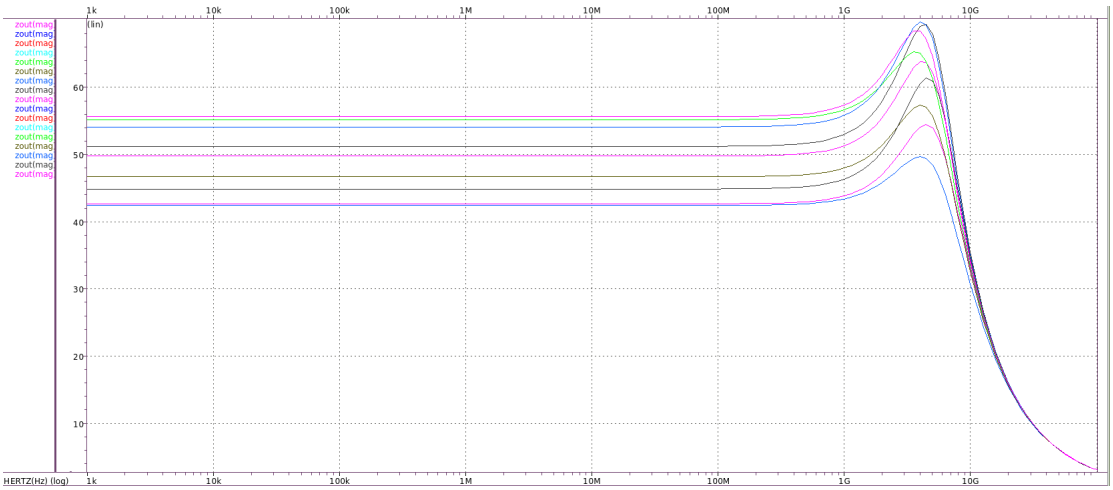


Figure 4.12: Termination evolution in frequency with PVT variations of CML driver with active loads.

Time response

Displayed in fig. 4.13 are the output signals of both output nodes Vop and Von at a frequency of 10 GHz which translates to a signal with a period of 100 ps, verifying a 400 mV peak-to-peak signal centered in 300 mV as expected.

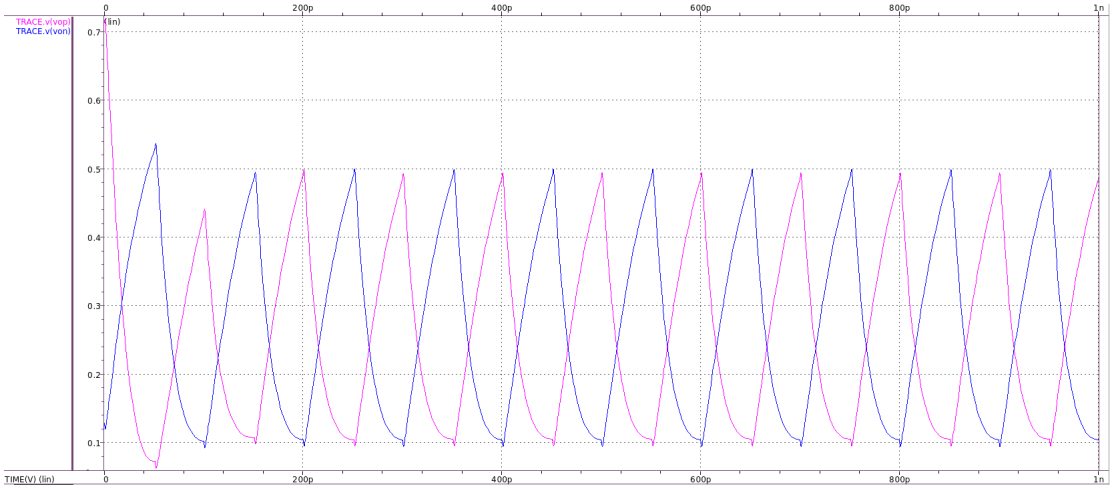


Figure 4.13: Single-ended outputs for 10 GHz of the CML driver with active loads.

This two signals group together to form the differential signal in fig. 4.14 with a differential output swing of 800 mV compared to the attenuated 600 mV of the original driver.

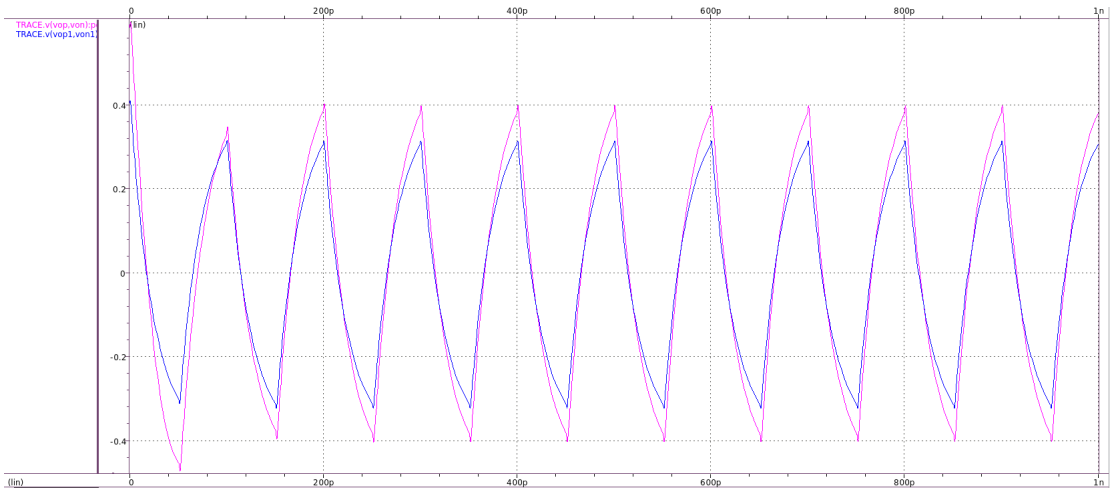


Figure 4.14: Comparison between differential outputs for 10 GHz of CML driver with active loads as pink and original CML driver as blue.

Repeating the corners simulation but in time domain allows one to notice from fig. 4.15 an output swing variation between 674 mV and 863 mV. This analysis in conjunction with the one made in the frequency domain imply that the circuit is robust enough to operate properly at all conditions.

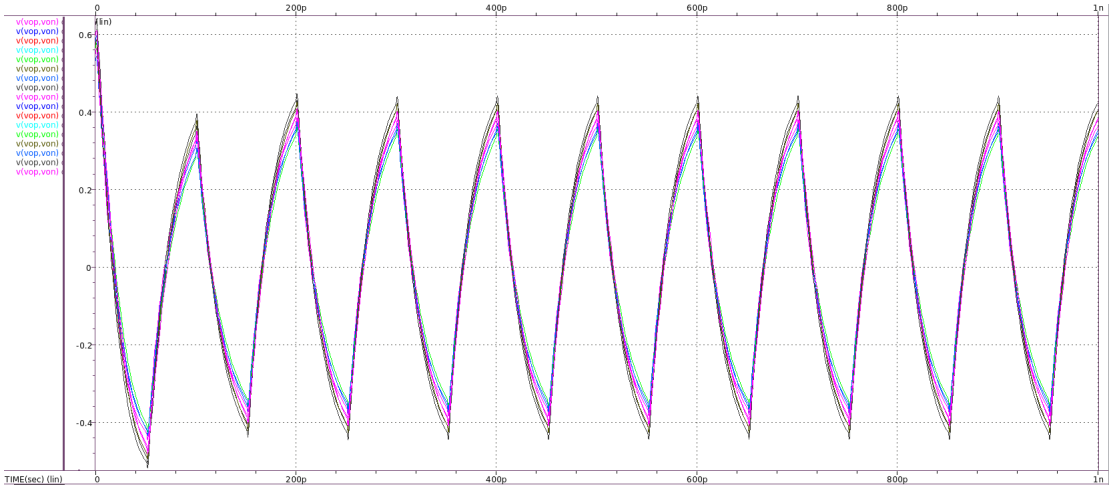


Figure 4.15: Differential output with PVT variations of CML driver with active loads.

4.2.2 CML driver with non-gyrator c type inductors

The second CML driver with inductive peaking of fig. 4.16 implements the non-gyrator type active inductor discussed in sections 2.4.4 and 3.4, fig. 4.17, nevertheless, changes had to be made in the design of both the driver and the active inductor.

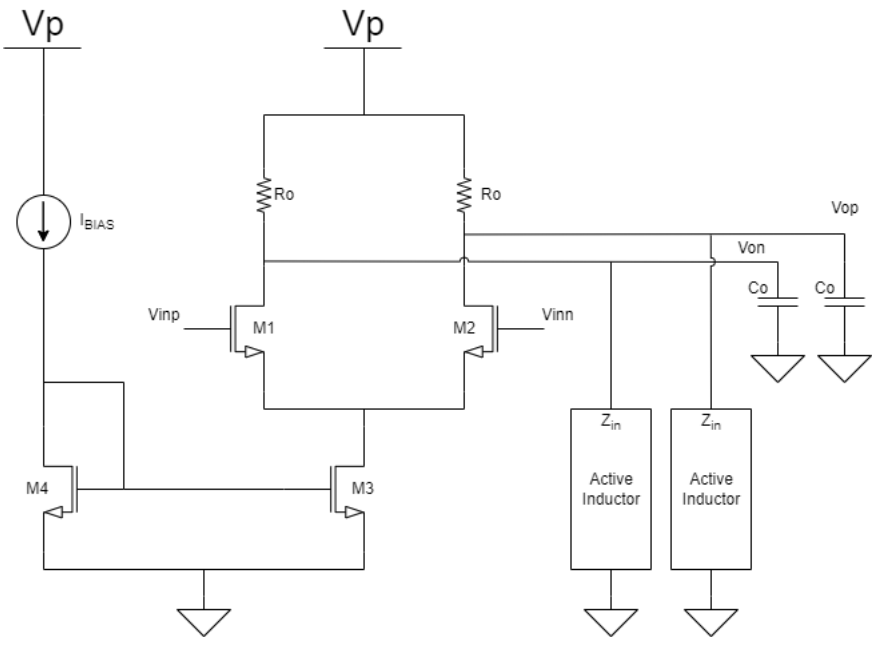


Figure 4.16: Circuit design of a CML driver with active inductors.

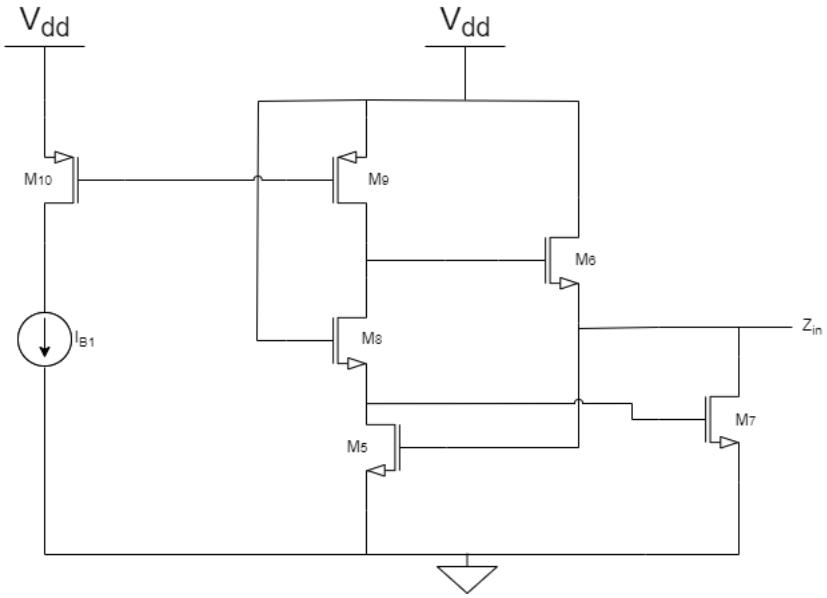


Figure 4.17: Circuit design of non-gyrator type active inductor.

The difference between the original driver and this one resides in the value of the resistance R_o as the output impedance is now categorized by the parallel of those resistances and the input impedance of the inductor meaning both impedances should correspond to 100 Ω at low frequencies.

The fact that R_o has been increased to 100 Ω affects the output swing of the driver that should be increased to 800 mV single-ended, nevertheless, such alteration is not so trivial as the reduced to 500 mV input, to give the current mirror enough voltage headroom for its proper operation as previously mention, will limit the output swing to the same value if the gain of the circuit maintains the 0dB value.

The first important aspect of the active inductor's design is the importance of establishing a DC voltage at the input node to match the driver's output voltage and achieve DC coupling for better performance of the inductor. In order to keep all transistors in the saturation region half of V_p (400 mV) was considered.

Another important change that has to be made to the previous sizing of the inductor circuit is that the resistance value of the inductor must be set to 100 Ω. This will be reflected in the current consumed that was reduced from a total of 400 µA to 125 µA giving rise to the parameter values of the transistors displayed in table 4.3.

Table 4.3: DC operating point of CML driver with non-gyrator type inductor

element	W[µm]	L[nm]	Ids[µA]	gm[mS]	Vgs[mV]	Vds[mV]	Vth[mV]
m1=m2	8.5	16	4066	25.62	458.83	301.94	249.42
m3	84.86	16	8132	96.62	316.45	91.17	239.19
m4	17.68	16	2500	32.87	316.45	316.45	244.79
m5	0.174	16	72.43	0.72	393.10	400.50	270.16
m6	2.68	16	52.40	1.26	201.79	406.9	243.93
m7	0.116	16	52.40	0.49	400.50	393.10	270.21
m8	0.216	16	72.43	0.64	399.50	194.39	258.72
m9	1.5	16	-72.43	1.36	-240.13	-205.11	-243.41
m10	1.5	16	-75	1.40	-240.13	-240.13	-242.46

Frequency response

In fig. 4.18 one can observe the effect of the active inductor as the bandwidth is extended to 9.6 GHz, also, this circuit presents a gain really close to 0 dB before reaching a maximum of 2.27 dB due to the inductive peaking effect caused by the inductor.

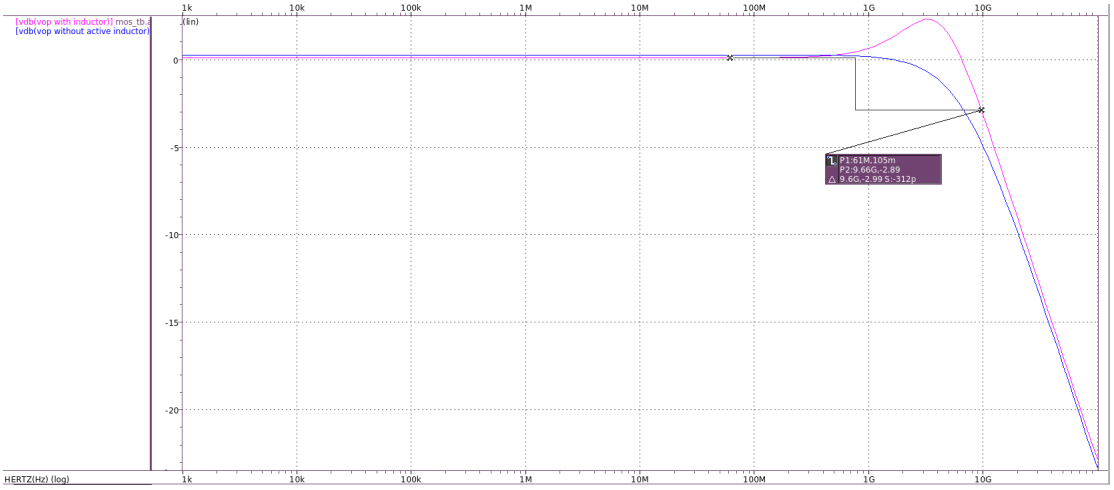


Figure 4.18: Frequency analysis comparison between CML driver with non-gyrator type active inductors as pink and original CML driver as blue.

However, after running the corners analysis of fig. 4.19, one can see that this circuit implementation fails in some situations. The failed corners are listed in table 4.4.

Table 4.4: List of failed corners

	Process	Voltage	Temperature
Corner n°1	ff	125°C	0.72V
Corner n°2	ff	125°C	0.88V
Corner n°3	fs	125°C	0.88V
Corner n°4	fs	-40°C	0.88V

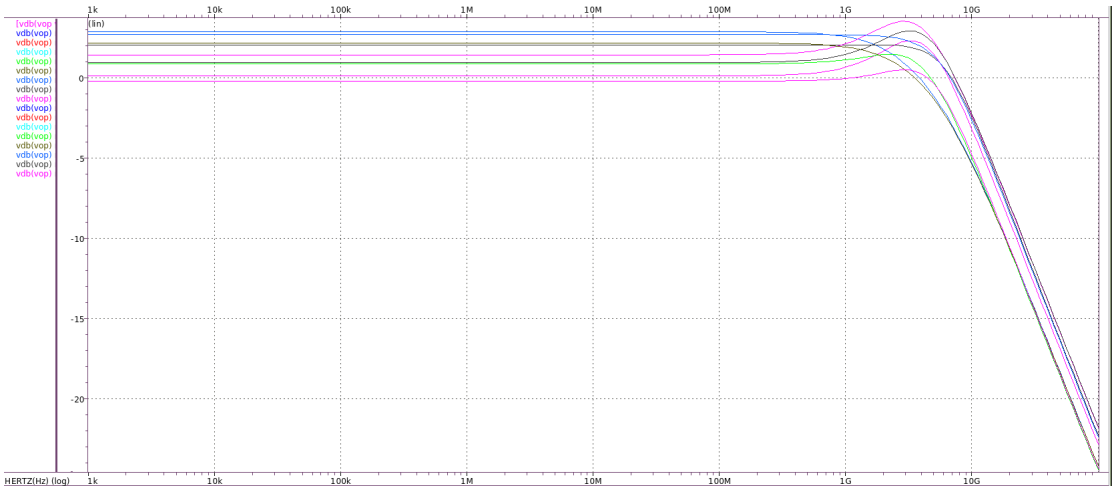


Figure 4.19: Frequency analysis for PVT variations of CML driver with non-gyrator type active inductors.

As for the output impedance, the result in fig. 4.20 shows a termination of 45.9 Ω for low frequencies demonstrating a slight deviation from the expected value hitting 61 Ω at 3GHz and 31.5 Ω at 9.66 GHz.

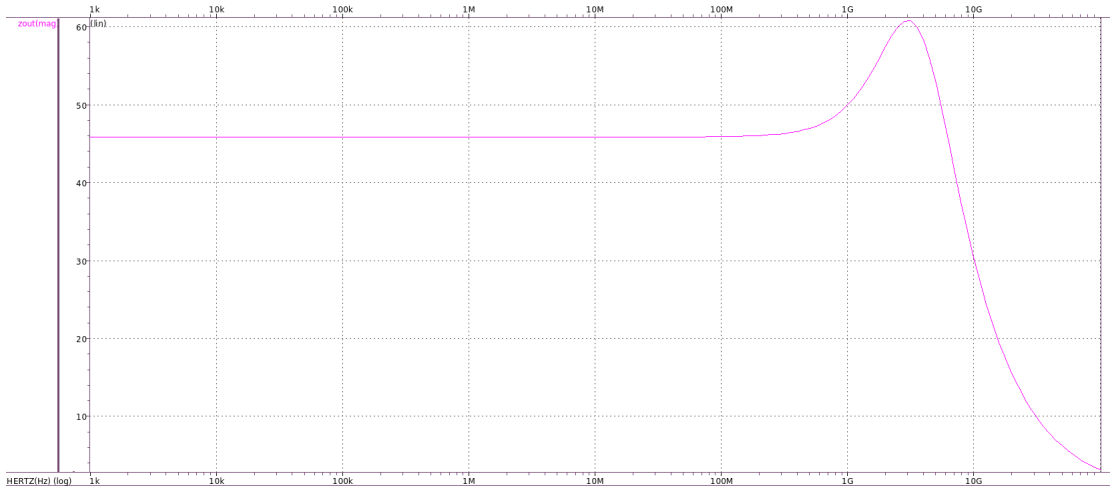


Figure 4.20: Termination evolution in frequency of CML driver with active loads of CML driver with non-gyrator type active inductors.

And as one would expect the same corners listed in table 4.4 gave terrible results once again in the corners simulation for the output impedance evidenced in fig. 4.21.

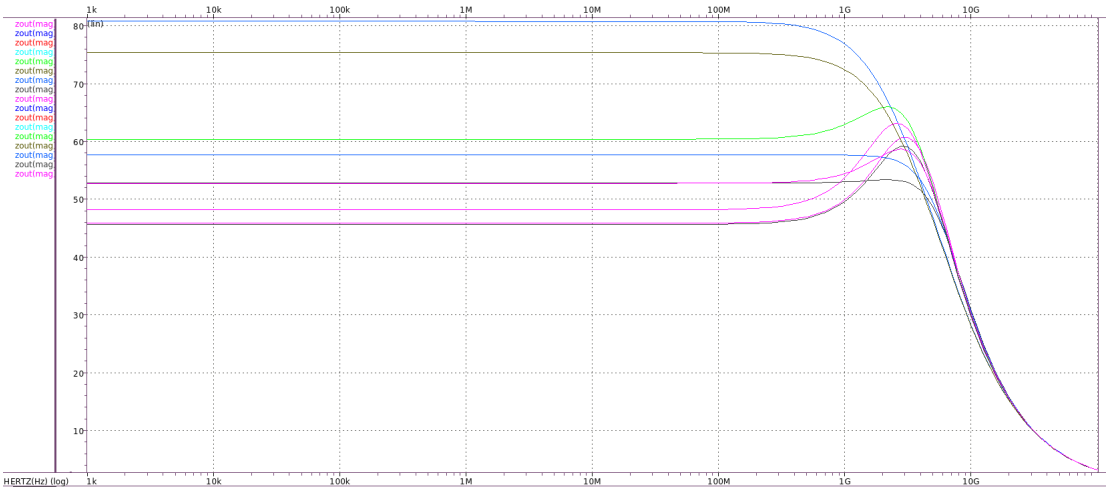


Figure 4.21: Termination evolution in frequency with PVT variations of CML driver with non-gyrator type active inductors.

Time response

In time domain, the obtained single-ended outputs displayed in fig. 4.22 show an unexpected output swing of 363 mV. This is most likely due to the V_{dsats} of the active inductor transistors that limit this value as the inductor's input node is shared with the driver's output node. This limitation also causes the differential signal in fig. 4.23 to be reduced to 726 mV peak-to-peak.

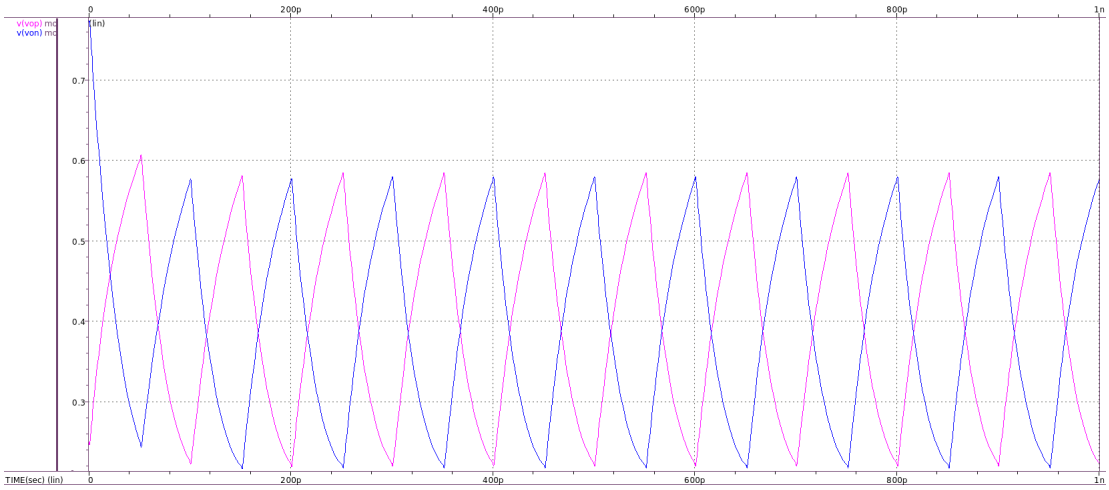


Figure 4.22: Single-ended outputs for 10 GHz of the CML driver with non-gyrator type active inductors.

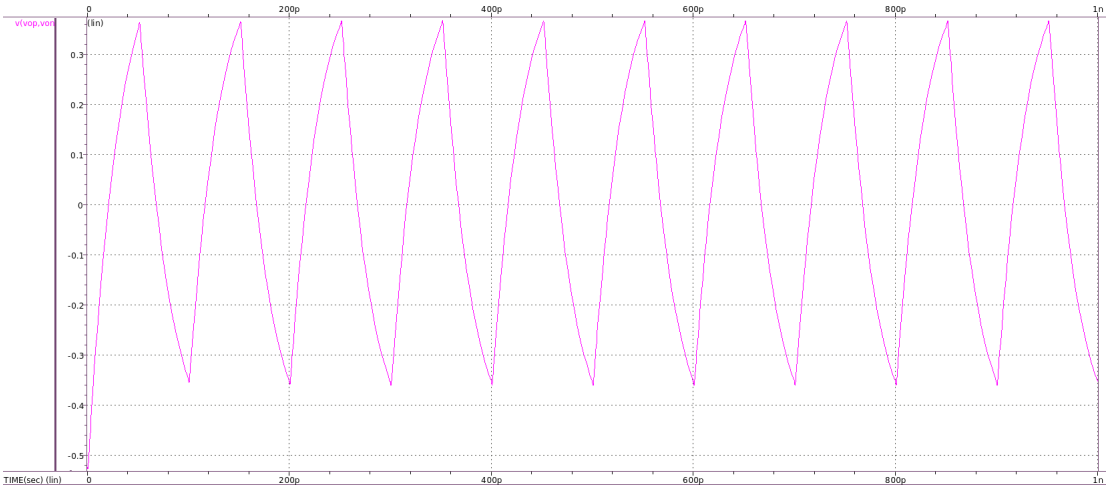


Figure 4.23: Differential output for 10 GHz of the CML driver with non-gyrator type active inductors.

Coinciding with the frequency simulations it does not come as a surprise that the four corners mentioned above result in a attenuated signal in time domain, this is demonstrated in fig. 4.24.

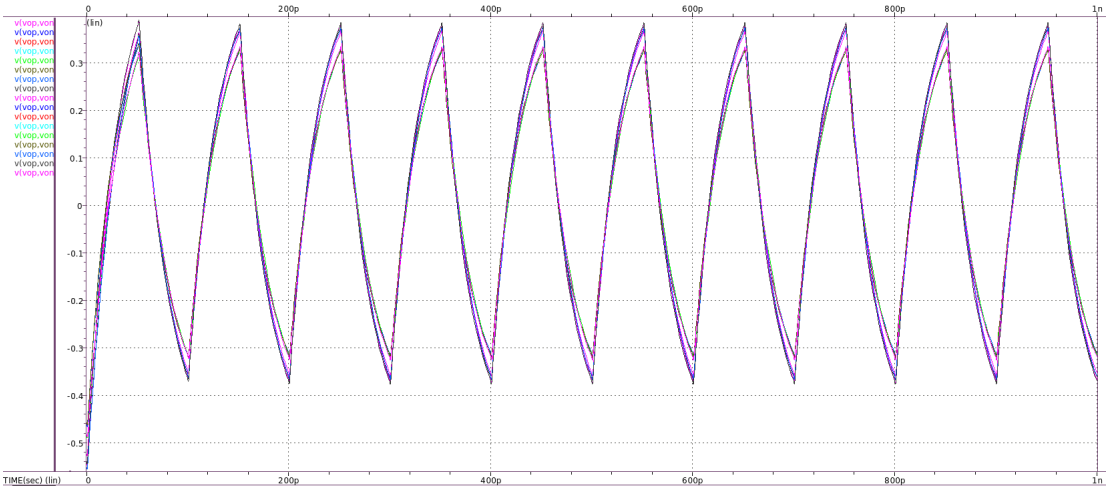


Figure 4.24: Differential output for 10 GHz with PVT variations of the CML driver with non-gyrator type active inductors.

4.2.3 Comparison between the simulated drivers

Looking at the performed simulations it becomes obvious that the implementation of the driver with active loads outperforms the driver with the non-gyrator c active inductor in almost every single aspect starting from the bandwidth achieving a small improvement of 500 MHz, moving on to the output impedance showing a value closer to the desirable 50 Ω and ending with an output swing at 10GHz closer to the 800 mV projected all while being more beneficial in terms of power dissipation as the current consumed in the first

circuit is limited to the 8 mA of the driver's current source whereas the second circuit counts with the increment of the current consumed by the active inductor.

Another important advantage the first circuit possesses is its robustness to PVT variations as these create DC voltage variations in the output node of the second circuit that compromise its performance rendering this circuit design not valid.

A summary of the differences of both drivers is presented in table 4.5:

Table 4.5: Comparison between simulated drivers

	CML driver with active loads	CML driver with active inductors
Bandwidth	10.1GHz	9.6GHz
Output Swing at 10GHz	400mV	363mV
Power Dissipation	7.9mA	8.2mA
Resilience	works in all corners	fails in 4 corners

4.3 Full Circuit Implementation and Simulation

As previously mentioned the input of the CML driver must be limited to a voltage range of 100 mV to 800 mV. This can be achieved with the help of a limiter circuit which in turn must be preceded by an inverter chain to achieve a more practical input signal.

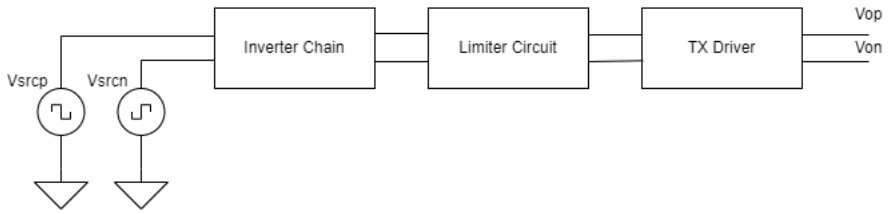


Figure 4.25: Sequence of circuits used to simulate the CML driver.

The full proposed circuit can be separated in three blocks presented in fig. 4.25 with the objective being to give a more realistic simulation of the CML driver with active loads. At the beginning of this string of blocks a random bit generator was used to create a stream of data together with an amplifier of gain -1 originating the complementary signal.

4.3.1 Limiter circuit

To achieve a signal with a limited voltage range another CML driver was used, however, unlike the driver that succeeds it, the termination does not require to be 50 Ω thereby allowing the fig. 4.6 circuit design to implement a larger R_o and achieve higher output swings.

Considering a resistance of 500Ω and by equation 4.1 one finds that the circuit must be biased with a total current of 1.4 mA therefore giving origin to the transistor characteristics registered in table 4.6.

Table 4.6: DC operating point of the limiter circuit

element	W[µm]	L[nm]	Ids[mA]	gm[mS]	Vgs[mV]	Vds[mV]	Vth[mV]
m1=m2	12.50	16	0.72	13.83	257.68	298.96	249.34
m3	11.92	16	1.43	18.67	316.44	142.32	250.78
m4	17.68	16	2.50	32.87	316.44	316.44	246.48

Unfortunately, by looking at transistor m3, one can notice that the V_{ds} surpasses the lower limit wanted in the output by 42 mV reducing the output swing by the same value, this is exhibited in fig. 4.26, however, the small DC voltage increase at the output node should not affect the performance of the TX driver.

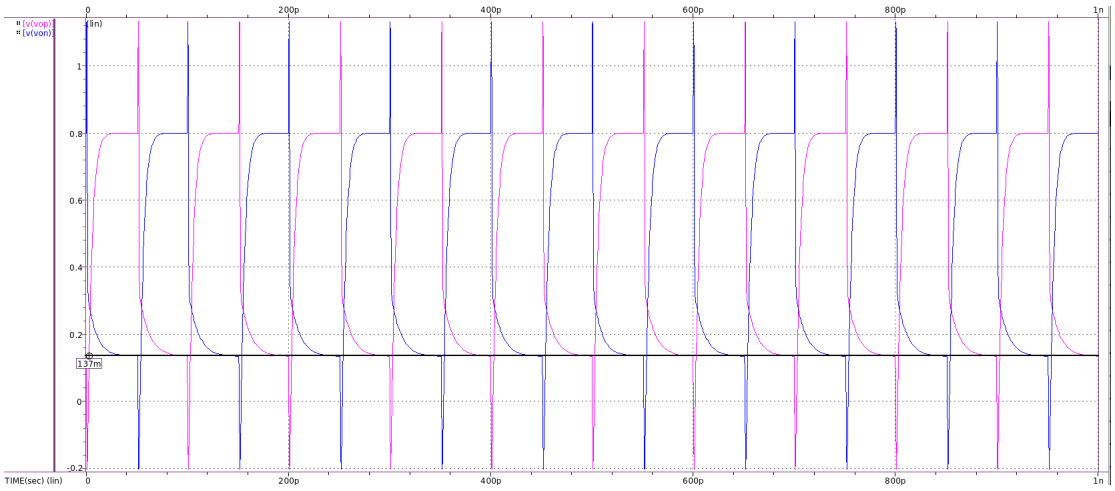


Figure 4.26: Limiter circuit outputs.

4.3.2 Inverter chain

Previous simulations were obtained with ideal signals from clock signal generators with infinite power thereby giving results that might not be trustworthy. To test the limiter circuit and the TX driver with a more realistic input signal a small inverter was placed after the voltage sources with conventionalized 1µm width NMOS and PMOS.

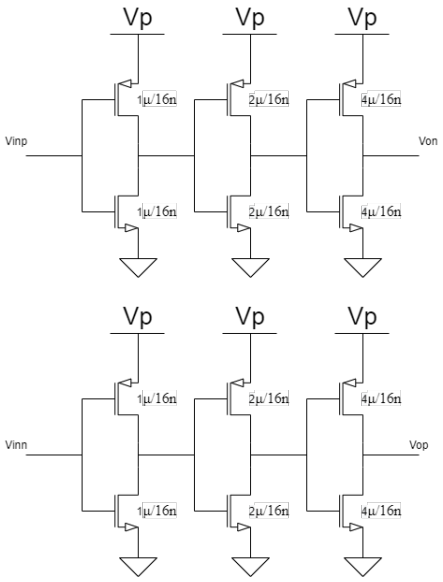


Figure 4.27: Inverter chain circuit design.

This inverter however is too small to drive a circuit as big as the limiter circuit. A chain of three inverters, fig. 4.27, was used instead allowing the circuit to achieve better performance at high frequency, with the third inverter being double the size of the second one and this one being double the size of the first one. This methodology comes from the fact that a small stage should be able to drive another stage twice as big.

4.3.3 Final results

To observe and evaluate the signal evolution at every stage of the block string that constitute the studied circuit a useful tool called eye diagram was employed.

The eye diagram overlaps the different sequences of logical zeros represented as the minimum voltage and ones represented as the maximum voltage over two periods. With this diagram one obtains a result that resembles an eye, giving information on the quality of the signal obtained. The more squared and opened is this eye the more perfect the signal is.

Taking as an example in fig. 4.28 the ideal data signal over time with each bit having a period of 1 ns originated by one of the sources at the beginning of the block chain.

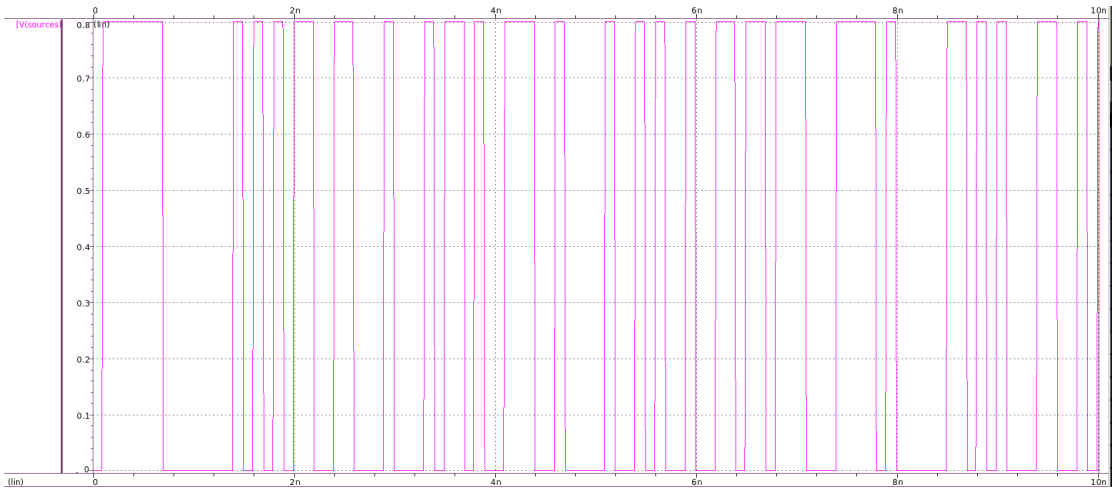


Figure 4.28: Signal generated by the voltage sources.

As ideal as it can be, it originates an eye diagram in fig. 4.29 with an invariable voltage amplitude of 800 mV and rise and fall times incredibly fast. Nevertheless, as it will be explained, the signal will suffer degradation throughout the outputs of the blocks causing the eye related to the final output to close.

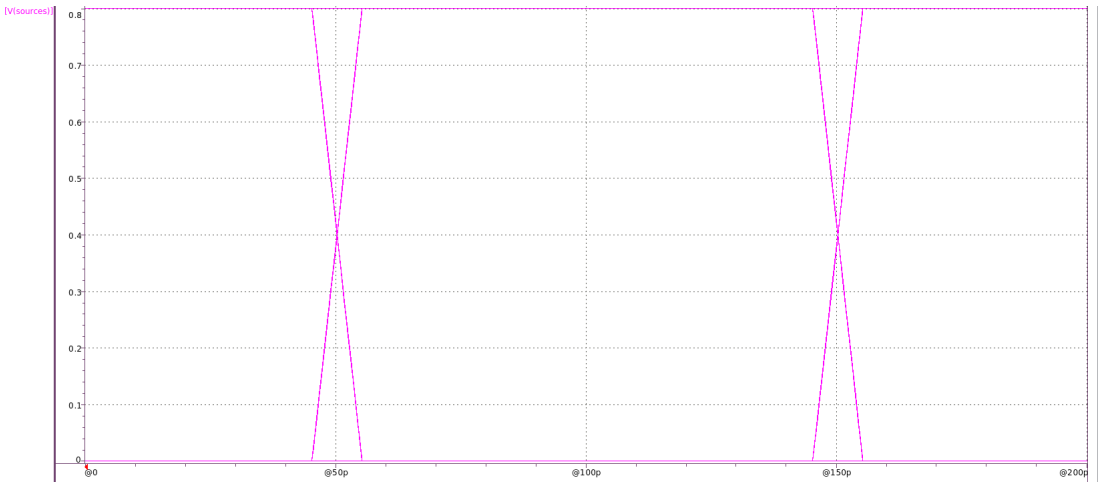


Figure 4.29: Eye diagram of the signal generated by the voltage sources.

The system will be simulated in two frequencies, the first one at 1 GHz will give the average outcome at lower frequencies corresponding to signals with 1 ns period, and the second one will depict the signal evolution at 10 GHz, 100 ps period, corresponding to the bandwidth of the final driver. The output of the driver will also be given for a frequency of 20 GHz to observe the attenuation for frequencies higher than the maximum frequency of operation.

1GHz simulation

Starting at the output of the inverter chain one can observe in fig. 4.30 an eye diagram close to perfection as this is the fastest circuit out of all involved. It has a differential swing of 1.6 V and perfect rectangle signal.

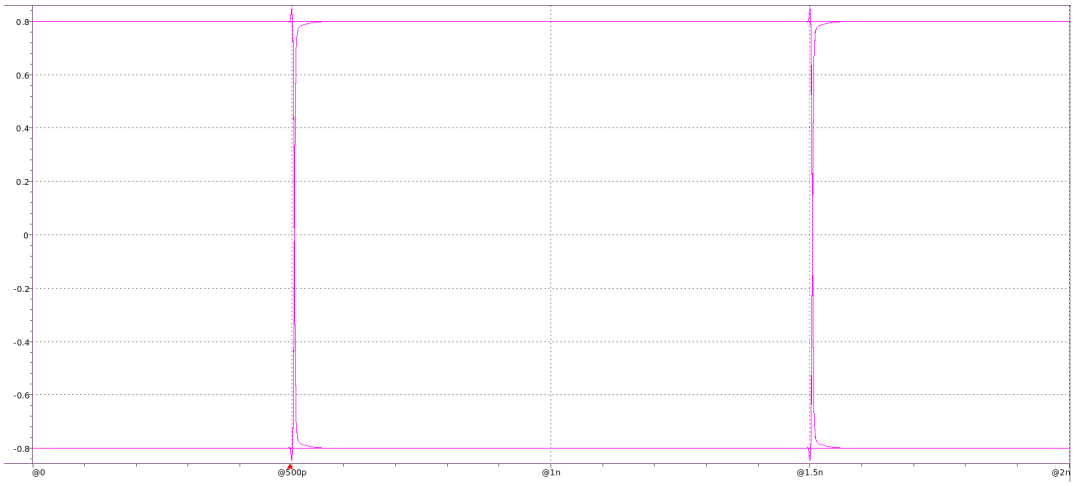


Figure 4.30: Eye diagram of the signal at 1 GHz at the output of the chain of inverters.

At the same frequency the limiter circuit starts to present, in fig. 4.31, a slower rise time keeping the rectangular shaped signal with differential swing of 1.33 V, 70 mV lower than desirable for the reasons previously discussed.

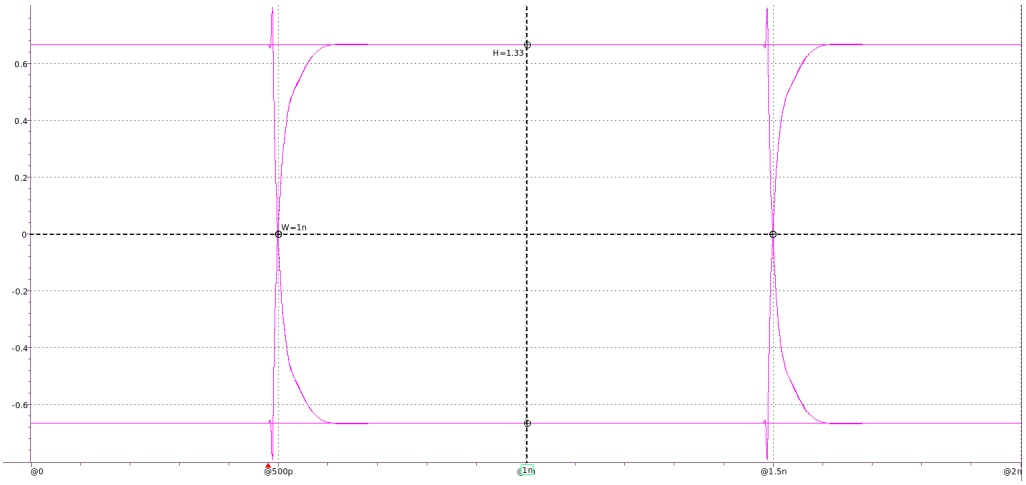


Figure 4.31: Eye diagram of the signal at 1 GHz at the output of the limiter circuit.

The final output in fig. 4.32 keeps the rectangular signal as one would expect for low frequencies while achieving an eye opening of 1.06 V, greater than the expected one which can only prove to be more beneficial.

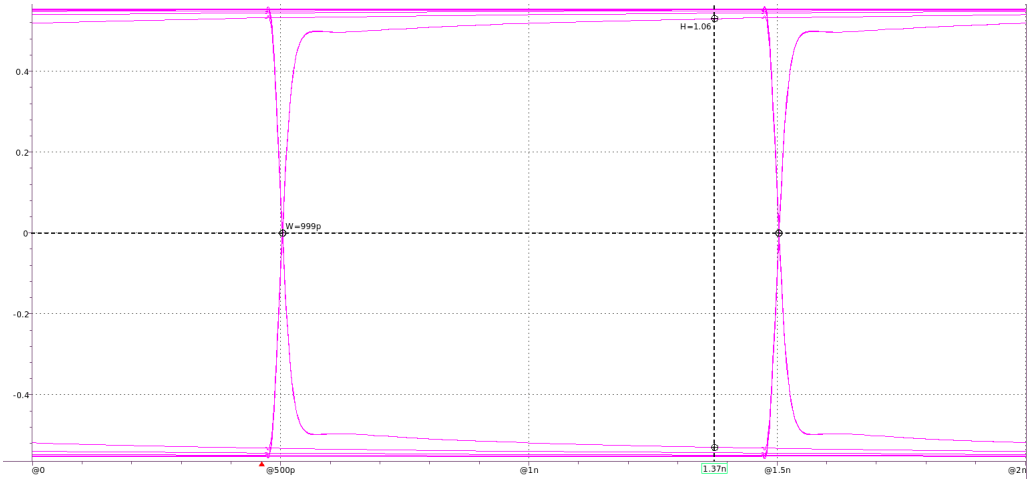


Figure 4.32: Eye diagram of the signal at 1 GHz at the output of the TX driver.

10GHz simulation

The figs. 4.33 and 4.34 show that the period alteration on the input signal barely caused any changes with the signal at the output of the inverters still close to a perfect one and the limiter output still keeping a 1.28 V differential swing even though the rise and fall times already start to condition the eye opening.

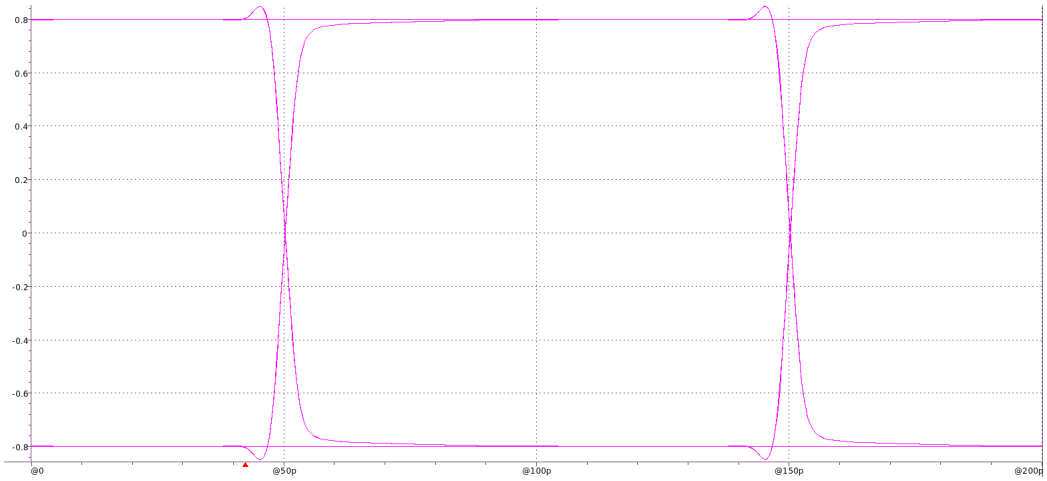


Figure 4.33: Eye diagram of the signal at 10 GHz at the output of the inverter chain.

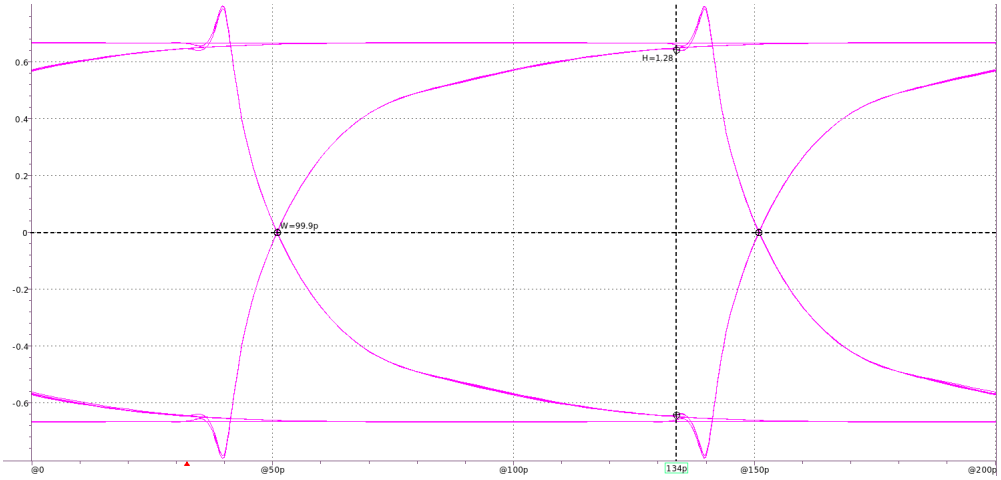


Figure 4.34: Eye diagram of the signal at 10 GHz at the output of the limiter circuit.

And finally the output of the entire circuit running at the maximum frequency is represented in fig. 4.35 where one can see a signal starting to loose the rectangular shape showing signs of attenuation since the eye opening has been restrained to 976 mV, 84 mV less than the previously obtained value. From the same simulation one can notice a slight time variation at which the signal intercepts 0 V.

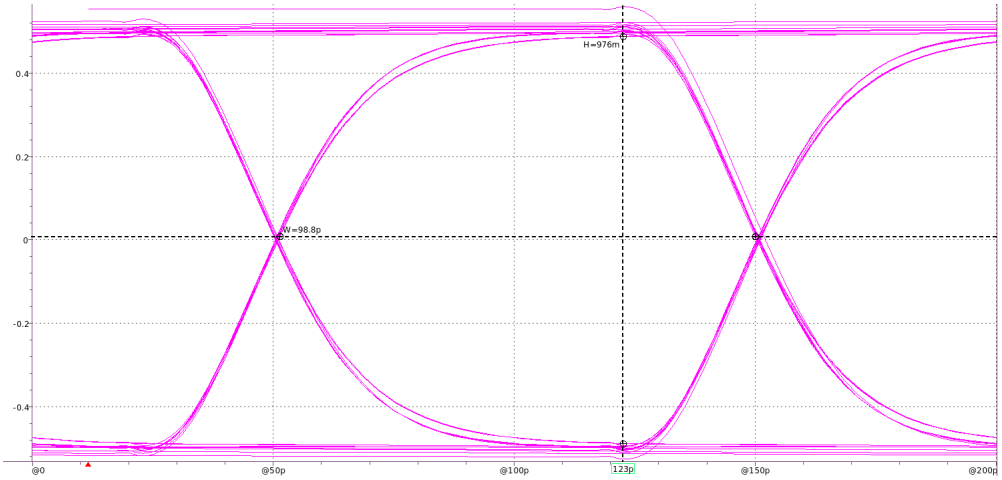


Figure 4.35: Eye diagram of the signal at 10 GHz at the output of the TX driver.

20GHz simulation

At 20 GHz, the eye diagram of the differential output of the circuit in fig. 4.36 exhibits an eye opening of 616 mV, almost half of the amplitude the driver achieves at low frequencies while displaying a 5 ps variation of zero crossing.

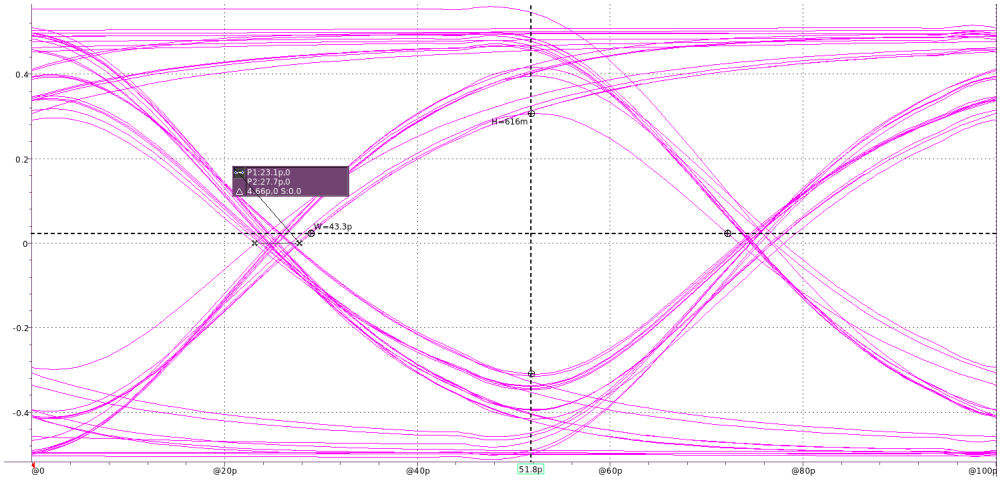


Figure 4.36: Eye diagram of the signal at 20 GHz at the output of the TX driver.

4.3.4 Layout

The final step to conclude the circuit implementation and simulation is to give a layout design of the CML driver without including the transistors used for current biasing of the circuit allowing one to later on design a more suitable current source.

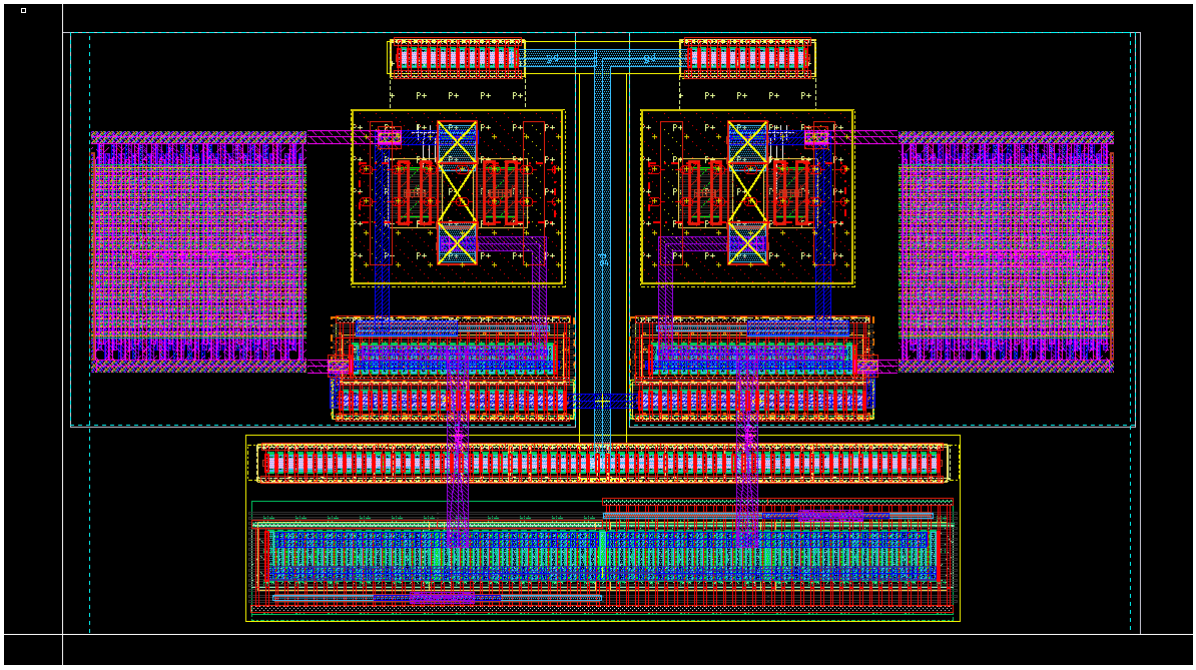


Figure 4.37: Layout of the CML driver with active loads.

The layout shown in fig. 4.37 can be separated in two mirrored active inductors separated through a placement border as white comprised of one transistor properly polarised with a bulk to avoid latch-up problems, a capacitance created with metals M1 to M7 and a poly resistance also polarised with its own bulk and the two gain transistors and respective bulks.

This design occupying a total area of 55.49 μm^2 was achieved with the help of checking tools such as the LVS, layout versus schematic, to ensure all connections correspond to the ones in the schematic of the circuit and DRC, design rule check, to ensure all rules associated with the technology, for example the distance between metals, are obeyed.

5

Conclusions and future work

5.1 Conclusions

In high-speed chip-to-chip communication implemented through SerDes it is becoming more and more important for the output and input drivers of this serialization technique to achieve higher speeds specially when they are limited by the parasitic capacitances inherent to the datapath that connects those drivers.

In this dissertation a method to increase the bandwidth of such drivers my means of inductive peaking with the help of active inductors was studied giving insight on the most commonly employed active inductor circuits theory and results. Later, a more detailed analysis was given with the simulation of a CML driver implementing the mentioned inductive peaking with two different active inductor topologies, one with simple active loads comprised of only a PMOS transistor and a resistance and the second one with a non-gyrator type inductors, making a comparison between the results of both designs.

The CML driver with active loads gave the best results in bandwidth, power dissipation, output swing and PVT variations robustness and was further simulated on a more realistic simulation environment as the findings showed a bandwidth increase from 6.5 GHz, the original bandwidth of the CML driver, to 10.1 GHz exhibiting a termination of 50 Ω while originating a differential signal with an output swing of 976 mV.

5.2 Future Work

Even though the CML driver's bandwidth was improved through inductive peaking the results could need some improvement.

The first possible improvement could be related to the bandwidth itself, aiming to enhance the bandwidth of the driver even further trying to reach the 20 GHz mark possibly with help of different active inductors apart from the covered ones.

Another improvement could be seen in the study of driver designs that implement the same active inductors but allow the circuit to have a rail-to-rail input and output signals therefore cutting off the necessity of the limiter circuit resulting in less power dissipation

and reduced chip area.

And last but not least, the layout design could be enhanced in other to minimize the chip area consumed and a post-layout parasitic extraction and simulation should be realized to understand the consequences of such design.

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