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Quadrature Generators based on Ring Oscillators and Shift Registers

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To my family, friends and lovely girlfriend.

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Abstract

Quadrature oscillators are key elements in modern radio frequency (RF) transceivers and very useful nowadays in wireless communications, since they can provide: low quadrature error, low phase-noise, and wide tuning range (useful to cover several bands). RC oscillators can be fully integrated without the need of external components (external high Q-inductors), optimizing area, cost, and power consumption.

The conventional structure of ring oscillator offers poor frequency stability and phase-noise, low quality factor (Q), and besides being vulnerable to process, voltage and temperature (PVT) variations, its performance degrades as the frequency of operation increases.

This thesis is devoted to quadrature oscillators and presents a detailed comparative study of ring oscillator and shift register (SR) approaches. It is shown that in SRs both phase-noise and phase error are reduced, while ring oscillators have the advantage of occupying less area and less consumption due to the reduced number of components in the circuit. Thus, although ring oscillators are more suitable for biomedical applications, SRs are more appropriate for wireless applications, especially when specification requirements are more stringent and demanding.

The first architecture studied consists in a simple CMOS ring oscillator employing an odd number of static single-ended inverters as delay cells. Subsequently, the quadrature 4-stage ring oscillator concept is shown and post-layout simulations are presented. The 3 and 4-phase single-frequency local oscillator (LO) generators employing SRs are presented, the latter with 50% and 25% duty-cycles. The circuits operate at 600 MHz and 900 MHz, and were designed in a 130 nm standard CMOS technology with a voltage supply of 1.2 V.

Keywords: Local oscillator, quadrature oscillator, multiphase generator, shift register, phase error, phase-noise.

Resumo

Os osciladores em quadratura são elementos fulcrais no que concerne aos mais recentes *transceivers* de rádio frequência (RF) e às comunicações sem fio de hoje em dia sobretudo graças às mais-valias que ostentam: baixos erro de quadratura e ruído de fase e ampla faixa de sintonização (útil para cobrir diversas bandas). Os osciladores RC podem ser totalmente integrados sem a necessidade de recorrer a componentes externos (indutores externos com elevado fator de qualidade [Q]), otimizando assim a área, custo e o consumo associados.

A estrutura convencional do oscilador em anel a par de uma pobre estabilidade de frequência e ruído de fase, apresenta um baixo fator de qualidade e além de ser vulnerável a variações de processo, tensão e temperatura (PVT do inglês *process*, *voltage and temperature*), o seu desempenho diminui à medida que a frequência de operação aumenta.

Esta tese é dedicada aos osciladores em quadratura, apresentando um detalhado estudo comparativo dos osciladores em anel e *shift registers* (SRs). Tanto o ruído de fase como o erro de fase são reduzidos nos SRs, ao passo que o oscilador em anel tem a vantagem de ocupar menos área e apresentar menor consumo, graças ao modesto número de componentes que possui. Assim, embora os osciladores em anel sejam mais adequados para aplicações biomédicas, os SRs são mais apropriados para aplicações *wireless*, sobretudo quando as especificações são mais rigorosas e exigentes.

A primeira topologia estudada consiste num simples oscilador em anel CMOS empregando um número ímpar de inversores como células de atraso. Posteriormente, o oscilador em anel de 4 estágios em quadratura é apresentado, bem como simulações pós-layout do mesmo. Relativamente aos SRs, desenvolveu-se geradores de 3 e 4 fases onde a arquitetura em causa é aplicada, o último com *duty-cycles* de 50% e 25%. Todos os circuitos operam a 600 MHz e 900 MHz e foram desenvolvidos na tecnologia padrão CMOS de 130 nm com uma tensão de alimentação de 1,2 V.

Palavras-chave: Oscilador em quadratura, gerador de fase, *Shift register*, erro de fase, ruído de fase.

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Acronyms

AC Alternating Current.

ADC Analog-to-Digital Converter.

AFE Analogue Front-End.

AM Amplitude Modulation.

ASCII American Standard Code for Information Interchange.

BER Bit Error Rate.

BPF BandPass Filter.

CAD Computer-Aided Design.

CD Critical Dimension.

CML Current-Mode Logic.

CMOS Complementary Metal-Oxide-Semiconductor.

D-FF D-type FlipFlop.

DC Direct Current.

DDR Double Data Rate.

DLL Delay-Locked Loop.

DRC Design Rule Checking.

DRM Digital Rights Management.

DSP Digital Signal Processing.

DTC Divide-by-Two Circuits.

EDA Electronic Design Automation.

FDK Foundry Design Kit.

FET Field-Effect Transistor.

FF Flip-Flop.

FM Frequency Modulation.

FoM Figure of Merit.

FPGA Field Programmable Gate Array.

GSM Global System for Mobile Communications.

I/O Input/Output.

IC Integrated Circuit.

IF Intermediate Frequency.

IP Intellectual Property.

IP_2 Second-order Intercept Point.

ISM Industrial, Scientific and Medical.

$\mathcal{L}$ Phase-noise.

LNA Low-Noise Amplifier.

LO Local Oscillator.

LPE Layout Parameter Extraction.

LPF Low-Pass Filter.

LSB Least Significant Bit.

LSI Large-Scale Integration.

LTI Linear Time-Invariant.

LTV Linear Time-Variant.

LVS Layout Versus Schematic.

MIM Metal-Insulator-Metal.

MIMCAP Metal-Insulator-Metal CAPacitor.

MOS Metal-Oxide-Semiconductor.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

NMOS Negative-channel Metal-Oxide-Semiconductor.

ODE Oscillator Design Efficiency.

PA Power Amplifier.

PAC Periodic AC.

PDK Process Design Kit.

PIPO Parallel-Input to Parallel-Output.

PISO Parallel-Input to Serial-Output.

PLL Phase-Locked Loop.

PMOS Positive-channel Metal-Oxide-Semiconductor.

Pnoise Periodic Noise.

PSD Power Spectral Density.

PSP Periodic S-Parameter.

PSS Periodic Steady-State.

PVT Process, Voltage and Temperature.

PXF Periodic Transfer Function.

Q Quality Factor.

QAM Quadrature Amplitude Modulation.

QDR Quadrature Data Rate.

QPSK Quadrature Phase-Shift Keying.

RF Radio Frequency.

SIPO Serial-Input to Parallel-Output.

SISO Serial-Input to Serial-Output.

SoC System-on-a-Chip.

SR Shift Register.

SSB Single-SideBand modulation.

TLR Topological Layout Rules.

UMC United Microelectronics Corporation.

VCO Voltage-Controlled Oscillator.

VLSI Very-Large-Scale Integration.

WMTS Wireless Medical Telemetry Service.

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

The demanding for wireless communications in the last years have changed the way wireless transmitters and receivers are made. This advance brought new requirements such as small devices and compact circuits with minimum area and at lower cost. This trend became a tremendous challenge up to the point where today it is possible to design a transceiver on one chip. In addition to overall system costs and area occupation, it is very important to reduce the voltage supply and power consumption [1–3]. Framed on the concept of System-on-a-Chip (SoC), one of the most attractive ways to achieve a high level of integration is using Complementary Metal-Oxide-Semiconductor (CMOS) technology. CMOS is the most widely used type of semiconductor as a result of high noise immunity and low static power supply drain, allowing the development of low cost and low power circuits able to operate at high frequencies.

This vision allowed Digital Signal Processing (DSP) to expand into wireless applications. Together with digital data transmission, DSP techniques have been at the heart of progress by using highly sophisticated modulation techniques, complex demodulation algorithms, error detection and correction, and data encryption, improving the accuracy and reliability of digital communications [4]. Given the simplicity in processing a digital signal compared to the analog one, an increasingly attempt to include as many blocks as possible of the transceivers to the digital domain has become a main interest.

The major strength of Analogue Front-End (AFE) of a modern wireless communication system lies in the responsibility of the interface between the antenna and the digital core. Moreover, the receiver AFE is one of the most critical components since the received signals are usually very weak and noisy due to the communication medium (air), resulting in stringent and demanding specifications of its key blocks shown in figure 1.1. Figure 1.1

gives a detailed description of a typical wireless transceiver: blocks (A) and (D) are part of the digital processor at the transmitter and receiver respectively, and the other blocks (B) and (C) are implemented in the AFE, where block (B) is designed at the transmitter and block (C) is applied at the receiver.

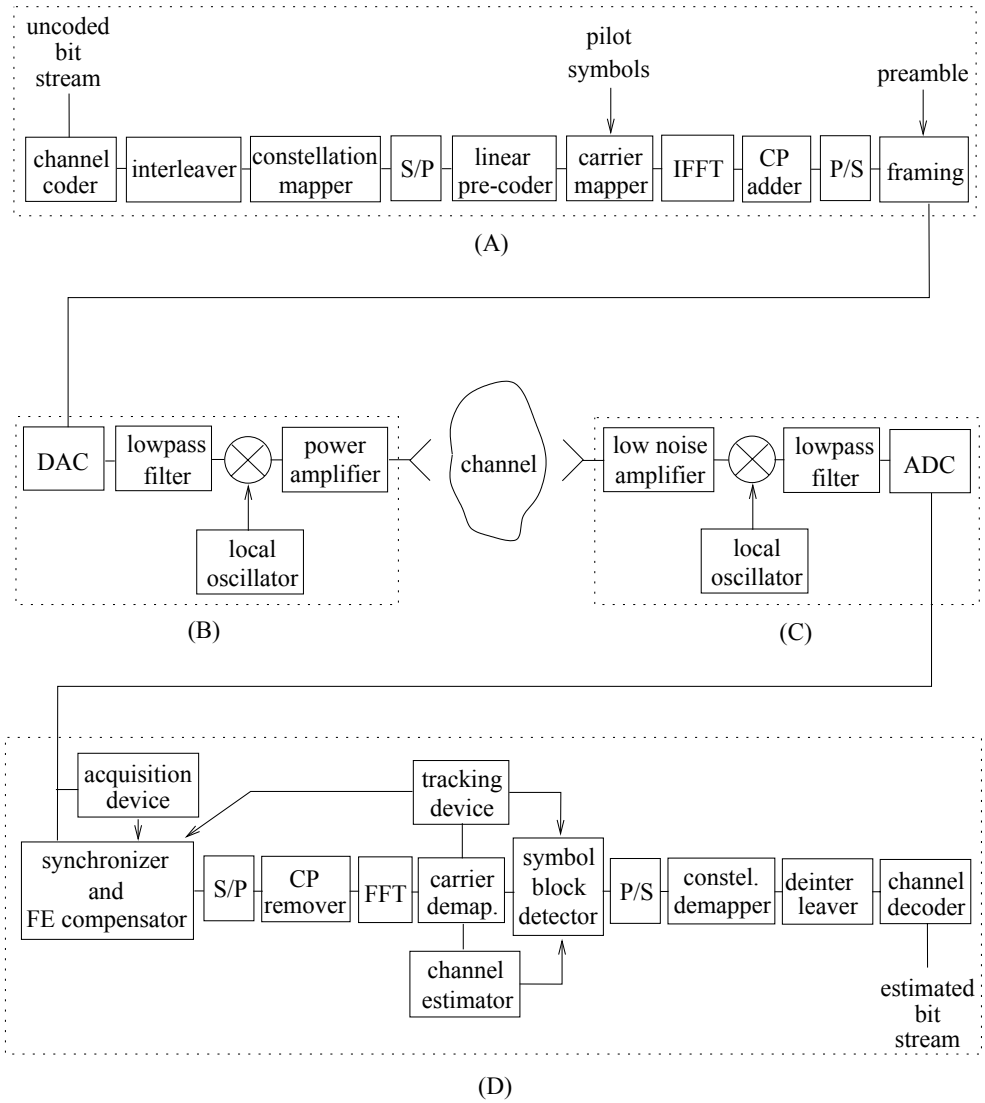

Figure 1.1: Wireless system block diagram: (A) transmit digital transceiver; (B) transmit analog front-end; (C) receive analog front-end; (D) receive digital transceiver [5].

There are two main receiver front-end architectures: the dominant heterodyne (or Intermediate Frequency (IF)) receiver - which uses one or more IFs and where the signal is downconverted from its carrier frequency to an IF - and the homodyne (zero-IF or direct-conversion) approach - which does not use IF so the IF is zero and where the signal is converted directly to the baseband frequency.

In the heterodyne receiver, the main handicap consists in the fact that, apart from the wanted signal, also an unwanted signal (image frequency signal) is downconverted

to the IF. These disturbances in the image frequency band have to be suppressed by an image reject filter before the mixing down to the IF. Conventional heterodyne receivers require filters with high Quality Factor (Q) which are difficult to comply for an integrated filter. Besides the implementation off-chip associated with high cost, a low IF causes the image frequency band to be so close to the desired frequency that an image-reject Radio Frequency (RF) filter is not feasible so a high IF is also indispensable. By these means, heterodyne receivers may have better performance than homodyne ones [3, 6].

Since the wanted RF signal is directly downconverted to baseband, the homodyne receiver does not require an image reject filter, a Low-Pass Filter (LPF) suffices. Nevertheless, the main drawback of the simplest receiver is the considerable sensitivity to parasitic baseband disturbances, Direct Current (DC) offsets, flicker noise and Local Oscillator (LO) leakage [2] which used to be relevant restrictions for a practical implementation, but are nowadays being overcome making this topology a viable alternative [3, 6]. To handle modern modulation schemes (for instance, Quadrature Amplitude Modulation (QAM)), a separation of In-phase (I) and Quadrature-phase (Q) components of the received signal is crucial to avoid possible cross-talk introduced by quadrature errors, which together with additive noise increases the Bit Error Rate (BER). These two components are used to cancel the image frequency, which is not necessary in homodyne receiver, and to obtain quadrature signals, so their importance is clearly recognized in modern transceivers.

A combination of the best features of each previously mentioned receiver compose the low-IF receiver [4, 7]. Unlike the homodyne architecture, the low-IF receiver eliminates DC offset, reduces the $1/f$ noise problem and avoids LO leakages issues [8]. Accurate quadrature signals, besides being used in the demodulation process, as it happens in heterodyne and homodyne architectures, are also used in image frequency cancelling instead of common external filters [9]. Along with component matching, they affect the quality of image-reject mixing contributing further to image rejection. Therefore, a LO with high accurate quadrature outputs is essential to remove image frequency signal.

The LO plays an important role in the RF front-end design. The main function of an oscillator is to generate LO phases I and Q for downconversion and upconversion operations. Therefore, besides the accuracy that the two quadrature output signals must have [10–14], the need for the oscillator to be fully integrated and tunable is quite relevant for the sake of front-end performance.

Due to the need of many modern transceiver architectures to have multiple phases of a certain output frequency, multiphase oscillators [15, 16] have been investigated. Their importance in clock and data recovery circuits is undeniable [17]. Several structures to generate quadrature signals are [18]:

1. A divide-by-two frequency divider following the oscillator running at the double the required LO frequency. This approach generally shows poor phase-noise and quadrature accuracy, as it requires 50% duty-cycle Voltage-Controlled Oscillator (VCO).

2. A VCO followed by a passive polyphase RC complex filter. An integrated polyphase networks is narrowband with poor quadrature accuracy. It also suffers from process variation on the RC time constants that lead to amplitude imbalance between the quadrature signals.

3. Two oscillators are forced to run in quadrature using transistor or transformer coupling. This technique provides wideband quadrature accuracy and superior phase-noise performance with a tradeoff of increased power, silicon area and reduced tuning range. By coupling two symmetric oscillators with each other, a quadrature VCO generates quadrature signals at high frequency.

Although the various ways to generate quadrature outputs, multiphase signals are an inherent feature of ring oscillators. Well known and so analysed as it is [19–30], this classic topology is popular due to its highly integration, low cost and small sizes. However, it suffers from poor phase noise/power tradeoff [31, 32], which has led to somewhat negligence today, encouraging us to use and investigate it in our own. Examples of some approaches are: (i) using an even number stage differential ring but it suffers from high phase noise [2]; (ii) employing an odd number of static single-ended as delay cells; (iii) the concept of adding feedforward paths to a ring with an even number of stages is also a possibility [22]. The latter two are described in this thesis.

Generating multiple phases is also a typical requirement for digital circuit design [33–40]. Recently, a significant effort has been made in the study of LO generators using the Shift Register (SR) technique [40, 41], where the same master clock drives N dynamic flip-flops to achieve low phase mismatch. Although a SR seems more attractive due to its wide working frequency range (flexibility), the input signal frequency has to be $N f_{LO}$ higher the clock frequency. This does not necessary lead to more power consumption and can even have advantages like less jitter than a equivalent Delay-Locked Loop (DLL) (assuming both are realized with Current-Mode Logic (CML)), higher Q and less area for the inductors. Furthermore, for flexible multiphase clock generation, SR is not only more flexible but often also better, in addition to allowing the use of latches with very small delay time [42].

The main goal of this work is to study either the ring oscillator and the SR architecture, making a solid comparison between these two multiphase generators, evaluating their relative advantages and disadvantages to investigate the most appropriate application for each of the LO generators. We focus on their key parameters that best characterize them, such as phase-noise and phase error, as well as on their discrepancies.

1.2 Main Contributions

To overcome poor frequency stability and phase-noise, vulnerability to Process, Voltage and Temperature (PVT) variations, low Q and performance degradation of ring oscillators as the increase of frequency of operation, the present dissertation brings a recent

architectural approach of a SR to design a multiphase clock generator, which is presented as a low phase-noise and low phase error solution suitable for wireless applications. The technique presented in [38] was taken into account in order to produce each dual D-type FlipFlop (D-FF).

Before using this attractive approach, a 3 and 4-stage ring oscillator concepts were explored and a layout of the latter was designed to validate the main schematic results.

During the development of this work, an opportunity to collaborate in a RF front-end receiver arose, leading to a publication titled "Wideband CMOS RF Front-End Receiver with Integrated Filtering" presented at 2015 Mixed Design of Integrated Circuits & Systems (MIXDES). Future publications can also be done after coupling the 4-phase single-frequency LO generator employing the SR architecture to the RF front-end since an ideal LO was previously used.

1.3 Thesis Outline

In addition to the introductory chapter, this thesis is organized into six more chapters, as follows:

Chapter 2 – Transceiver Architectures

Chapter 2 covers a broad review of RF transceiver architectures, such as the receiver and transmitter architectures. The key receiver architectures, including the low-IF, are presented, followed by the heterodyne and direct upconversion transmitters, respectively.

Chapter 3 – Oscillators

This chapter introduces some basic definitions usually employed in digital circuitry, such as the CMOS transistor model. Apart from a background of oscillator fundamental concepts and parameters, the main purpose of this chapter is to introduce the major single oscillator topologies, the LC and RC oscillators, where the ring oscillator structure is included.

Chapter 4 – Multiphase Generators

Chapter 4 introduces the open and closed-loop approaches where quadrature LO signals are obtained. In the closed-loop structures, the two-integrator and coupled oscillators are presented, while in open-loop approaches the shift register concept used in this work is highlighted.

Chapter 5 – Analysis of Multiphase Generators

In Chapter 5, the ring oscillator and shift register approaches are investigated. The same sizing was set purposely for a fair key parameters comparison. Each multiphase LO generator has two different topologies in order to produce 3 and 4 phase signals.

Moreover, the 4-phase clock generators employing SR with 50% and 25% duty-cycles are also presented here.

Chapter 6 – Simulation Results

The sixth chapter provides the schematic results of every ring oscillator and SR architecture. Furthermore, since a possible physical layout of the 4-stage ring oscillator was produced, the post-layout simulations are also presented. For a better understanding, the layout is presented hierarchically, i.e., from the most basic component to the final structure that composes the ring oscillator. Therefore, despite the comparison between both ring oscillator and shift register approaches, the schematic and post-layout of the 4-stage ring oscillator are also compared and the obtained results are discussed.

Chapter 7 – Conclusion and Future Work

The last chapter is devoted to draw the relevant conclusions. The most appropriate applications for each of the multiphase generators are also addressed here. Finally, some adjustments, optimization guidelines and future research suggestions are advised to ensure the best possible routing.

Chapter 2

Transceiver Architectures

In this chapter we review the basic transceiver (transmitter and receiver) architectures. We start by describing the advantages and disadvantages of the main conventional receiver approaches, namely, heterodyne, homodyne and low-IF. A special attention to the low-IF structure is given, since it consists in a combination of the best features of homodyne and heterodyne receivers. Then, section 2.2 presents the two elemental transmitter architectures: heterodyne and direct upconversion, respectively.

Receivers are characterized by performing low-noise amplification, downconversion and demodulation, while transmitters perform modulation, upconversion and power amplification. Nowadays, extensive researches are being made in the field of the receiver path, since integrability, interference rejection band selectivity are more demanding in receivers than in transmitters.

2.1 Receiver Architectures

The purpose of a communication system is to transmit the signal containing the information to the receiver. This system is composed by a transmitter, a receiver and a communication channel in which the signal is propagated. The transmitter's function is to process the message signal into a form suitable, known as a periodic signal called the carrier, for transmission over the communication channel. This process, denominated modulation, consists in the variation of, at least, one of its characteristics (amplitude, frequency or phase). As for the communication channel, its function is to provide a pathway between the transmitter's output and the receiver's input. Therefore, the receiver's job is to process the received signal and recover the appropriate original signal through a demodulation process. The reason why low frequency signals cannot be transmitted over long distances through the space is due to the short operating range they have, poor

radiation efficiency that characterize the low frequency signals, mutual interference causing erroneous interference air and the huge antenna requirement, since for a effective signal transmission, the sending and receiving antenna should be at least $1/4^{th}$ of the wave length of the signal.

In every wireless system, the receiver AFE is one of the most critical components since open space is used as the propagation channel and the received signals are usually very weak and noisy. Due to the strong attenuation during air transmission, signals are converted to high frequency for transmission and then downconverted to the baseband for reception. This is necessary since at high frequencies there is higher bandwidth and therefore the signals can carry more information and the antennas size is smaller. In summary, the receiver must be able to filter and amplify the received RF signal, downconvert it so the signal can be demodulated and processed by a digital system. The key blocks of a wireless receiver are the Low-Noise Amplifier (LNA), LO and the mixer, each one contributing to the system's overall signal gain/loss and noise figure [1, 43].

This section emphasizes three types of receivers, describing some of their characteristics, advantages and disadvantages.

2.1.1 Heterodyne Receiver

In 1917, Armstrong invented a further receiver principle, which is still used for a majority of wireless systems. The superheterodyne topology, also known as IF receiver, has that title because the designation heterodyne had already been applied in a different context (in the area of rotating machines) [2].

In this approach, shown in figure 2.1, the RF signal received by the antenna is filtered by a bandpass filter, where the influence of near interferers is minimized, then it is amplified by the LNA and downconverted to a lower IF through the mixer, to which the output of the LO is applied. Later, a bandpass filter at the IF called channel selection filter, isolates the desired signal from signals in adjacent channels. The signal demodulation is usually done in the digital domain and, therefore, it is necessary to include an Analog-to-Digital Converter (ADC), followed by a digital signal processor to perform the demodulation process [44].

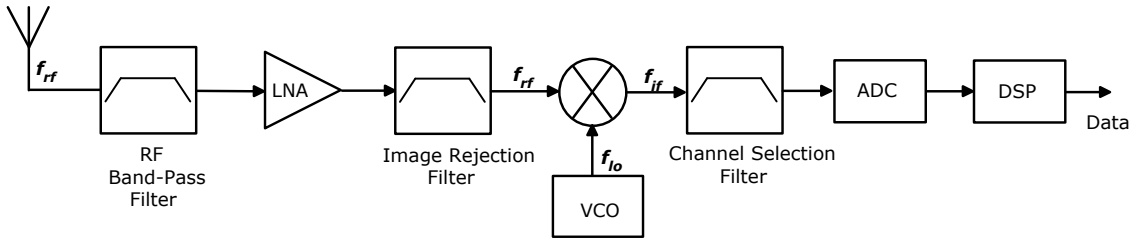

Figure 2.1: Superheterodyne receiver [44].

The main advantage of this architecture is that the IF is fixed, thus the desired RF frequency is selected by tuning the LO, making it easier to design the channel selection

filter, which should be very selective and with a high Q. On the other hand, the drawback of this receiver arises when a signal designated as image signal of frequency $f_{Im} = 2f_{LO} - f_{RF}$ appears at the mixer input, as shown in figure 2.2. After the multiplication, the image signal creates two more signals at frequencies $f_1 = f_{LO} - f_{RF}$ and $f_2 = 3f_{LO} - f_{RF}$, and so f_1 coincides with IF, overlapping the signal of interest and becoming impossible to separate both signals.

It is imperative to have an image rejection filter (IR BandPass Filter (BPF)) to reject the image produced in the downconversion, since two input frequencies can produce the same IF. Moreover, since the frequency difference between RF and image signals is $2f_{RF}$, increasing f_{RF} causes a relaxation in image rejection filter specifications. However, as f_{RF} increases, the channel selection filter must have tighter specifications for the same bandwidth due to the escalation of the Q, which is proportional to the centre frequency. Therefore, due to the required high Q of the filters, they need to be designed with discrete components which is not an acceptable solution for modern applications dominated by CMOS technology and where low-area and low-cost are indispensable, and so there is a compromise between IF and Q. In practice, high performance filters must be realized externally, which makes on-chip full integration impractical.

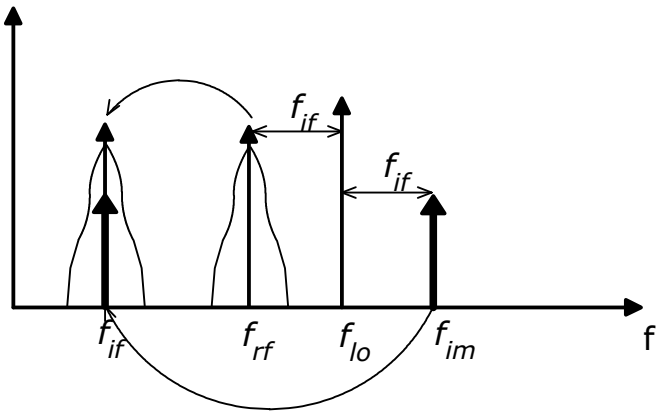

Figure 2.2: Image signal in superheterodyne receiver [44].

The heterodyne architecture described above has the advantage of handling modern modulation schemes that require IQ (in-phase and quadrature) signals to fully recover the information. However, the challenge nowadays is to obtain a fully integrated receiver on a single chip. This requires either direct conversion to the baseband or the development of new techniques to reject the image without the use of external filters. These two suggested approaches will be described next.

2.1.2 Homodyne Receiver

The homodyne receiver, known by other names such as direct-conversion or zero-IF, translates the input RF signal to baseband in a single downconversion (the IF is zero) using a LO with the same frequency as the RF signal. This avoids the use of an external

image rejection filter, and only a LPF is required after the mixer to do the proper channel selection. Finally, it allows the possibility of complete integration of the receiver on-chip.

Through the use of modern modulation schemes, the signal has information in the phase and amplitude, and the downconversion requires accurate quadrature signals. The block diagram of a simplified homodyne receiver is represented in figure 2.3(A) which is suitable for double-sideband Amplitude Modulation (AM) signals, since after the downconversion both sidebands are overlapped in baseband carrying the same information. However, for more sophisticated modulation schemes such Frequency Modulation (FM) or Quadrature Phase-Shift Keying (QPSK) the sidebands may carry different information, and to avoid loss of information after the downconversion, a quadrature architecture is shown in figure 2.3(B).

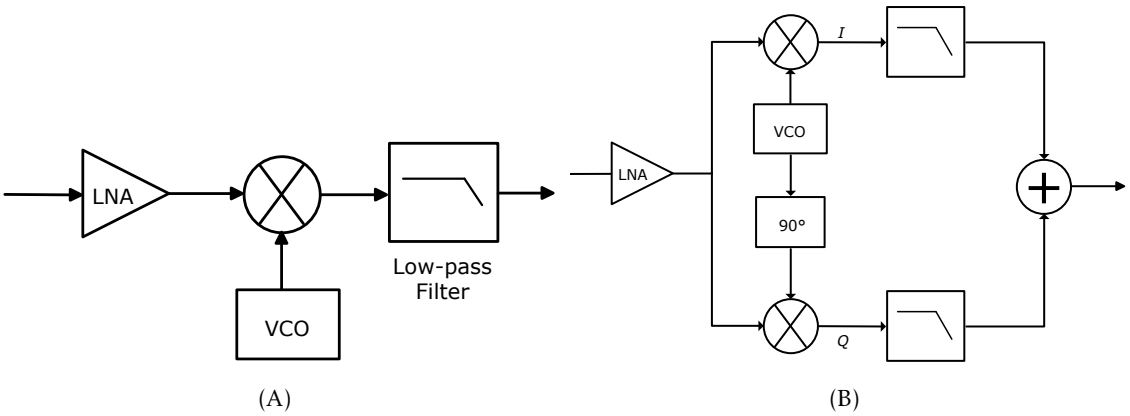

Figure 2.3: Homodyne receiver: (A) single inverter (B) quadrature receiver [44].

Despite its low complexity, this architecture presents several disadvantages described below, that prevent it from being applied in more demanding applications. These drawbacks are related to flicker noise, channel selection, LO leakage, quadrature errors, DC offsets and intermodulation:

1. **Flicker noise** – this type of noise from any active device has a spectrum close to DC. Therefore, it can corrupt substantially the low-frequency baseband signals, which is a severe problem in MOS implementation ($1/f$ corner is about 200 kHz).

2. **Channel selection** – at the baseband the desired signal must be filtered, amplified, and converted to the digital domain. Thus, the LPF must suppress the out-of-channel interferers. This filter should have high linearity and low-noise which makes it difficult to implement.

3. **LO leakage** – due to the device capacitances between the LO and RF ports of the mixer and capacitances or resistances between the LNA ports, the receiver will couple signal to the antenna that will be radiated, which can interfere with other

receivers using the same wireless standard. This effect can be minimized with the use of differential LO and mixer outputs to cancel common mode components.

4. **Quadrature error** – quadrature error and mismatches between the amplitudes of the I and Q signals corrupt the downconverted signal constellation (e.g., in QAM), resulting in imbalances in the gain and phase of the baseband I and Q outputs. Since modern wireless applications have different information in I and Q signals, this is the most critical aspect in direct-conversion receivers because it is very difficult to implement high frequency blocks with very accurate quadrature relationship.

5. **DC offsets** – as a result of LO leakage that appears at the LNA and mixer inputs, a DC component is generated at the output of the mixer (this process is known as LO "self-mixing") that can saturate the baseband circuits, preventing signal detection. Hence, this topology of receiver needs DC offset removal or cancellation to avoid the problems explained above.

6. **Intermodulation** – if two interferers exist near the channel of interest, after the mixing one of the interferers components is shifted near to the baseband and appears at the output together with the downconverted signal, leading to signal distortion. Thus, these kind of receivers must have a very high Second-order Intercept Point (IP_2). One solution is to implement differential LNAs and mixers, which would eliminate even-order harmonics.

This homodyne approach requires very linear LNAs and mixers, and high frequency oscillators with precise quadrature. All these requirements are hard to fulfil simultaneously.

2.1.3 Low-IF Receiver

The low-IF combines the best features of both types of receivers previously described, by using a mixed approach, which consists in using the homodyne receiver but instead of doing a direct-conversion to baseband the signal is shifted to a low IF. This relaxes the channel selection filter specifications and simultaneously avoids the baseband problems related to direct-conversion, in particular the flicker noise that strongly affects the baseband signal. However, it is still necessary to overcome the image issue associated with the non-direct conversion, which is solved applying a quadrature architecture that suppresses the image by generating a negative replica. This removal depends strongly on component matching and LO quadrature accuracy. There are two main rejection architectures, the Hartley and the Weaver [1, 3], as shown in figure 2.4.

The Hartley architecture (figure 2.4(A)) [45] mixes the RF signal with the quadrature outputs of the LO and, after the LPF, one of the resulting signals is shifted 90° and subtracted to the other signal. Assuming that a signal

$$x(t) = V_{RF}\cos(\omega_{RF}t) + V_{Im}\cos(\omega_{Im}t), \tag{2.1}$$

is placed at the input of the receiver, where V_{RF} and V_{Im} are, respectively, the amplitude of RF and image signals, and ω_{RF} and ω_{Im} are correspondingly the RF and image frequencies. After downconversion and filtering, the resulting signals at points 1 and 2 are, subsequently:

$$x_1(t) = -\frac{V_{RF}}{2}\sin([\omega_{RF} - \omega_{LO}]t) + \frac{V_{Im}}{2}\sin([\omega_{LO} - \omega_{Im}]t) \tag{2.2}$$

$$x_2(t) = \frac{V_{RF}}{2}\cos([\omega_{LO} - \omega_{RF}]t) + \frac{V_{Im}}{2}\cos([\omega_{LO} - \omega_{Im}]t). \tag{2.3}$$

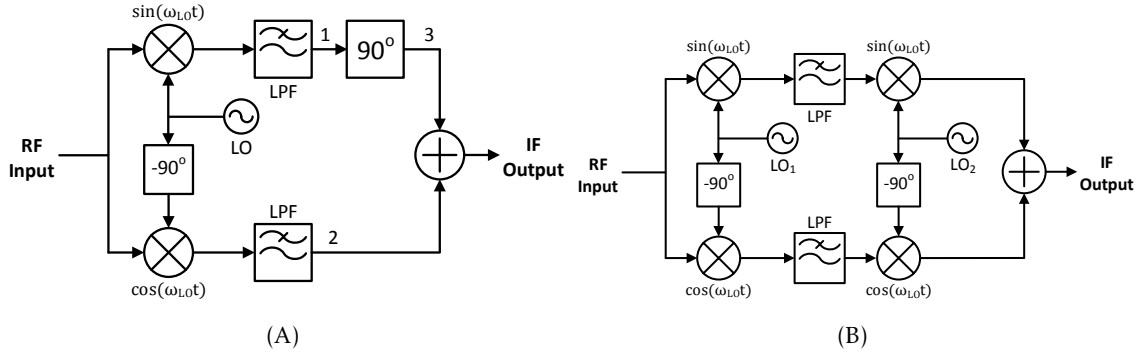

Figure 2.4: Image rejection architectures: (A) Hartley (B) Weaver [44].

Considering $\sin(\theta - \frac{\pi}{2}) = -\cos(\theta)$, after a 90° shift, the signal at point 3 (2.4(A)) is

$$x_3(t) = \frac{V_{RF}}{2}\cos([\omega_{RF} - \omega_{LO}]t) - \frac{V_{Im}}{2}\cos([\omega_{LO} - \omega_{Im}]t). \tag{2.4}$$

Finally, summing the signals $x_2(t)$ and $x_3(t)$ results in

$$x_{IF}(t) = V_{RF}\cos([\omega_{RF} - \omega_{LO}]t), \tag{2.5}$$

meaning that the desired signal is recovered (doubled in amplitude) and the image is suppressed. The main drawback of this architecture is the receiver sensitivity to the LO quadrature errors and the incomplete image cancellation due to the I/Q mismatches in the two signal paths that can occur.

In Weaver's approach (figure 2.4(B)) [46], the result is similar but the 90° phase shift is performed by a second mixing operation in both signal paths. Besides the problems of the Hartley architecture, this approach can also suffers from an image problem in the second downconversion if the signal is not converted to the baseband.

2.2 Transmitter Architectures

The three primary functions of RF transmitters are modulation, frequency translation/(up)conversion and power amplification, with the first two combines in some cases. Consequently, the key performance specifications are respectively modulation accuracy,

spectral emission and RF output power level. In transmitters, band selection and noise are not as critical as in receivers since a strong signal is locally available. Moreover, the variation of the signal level is small which relaxing requirements in terms of the dynamic range. Thus, due to their simplicity compared to receivers, there is a reduced diversity of transmitters approaches. They are: the heterodyne, that uses a sole IF and the direct upconversion which signal is straight converted to the RF band.

The generation of high output power leads to a high DC power consumption. In active operation, the power consumption of transceivers is mainly defined by the transmitter and not as much by the receiver. Nevertheless, a transmitter can be completely shut down after signal transmission to save power. Besides, modulation modes with both constant and variable signal amplitude can also be employed to transmit data [43]. The first scheme is more power efficient, whereas the latter one is the most often used, although it cannot be full integrated.

Transmitter design requires a solid understanding of modulation schemes because of their influence on the choice of such building blocks as upconversion mixers, oscillators and Power Amplifiers (PAs). The choice of a transmitter depends on the wanted and unwanted emission requirements and on the number of oscillators and external filters. Generally, the architecture and frequency planning of the transmitter must be selected in conjunction with those of the receiver to allow sharing hardware and possibly power [47].

2.2.1 Heterodyne Transmitters

Figure 2.5 shows the principle of heterodyne architecture. Since modern transmitters must handle quadrature signals, in this topology the baseband signals are modulated in quadrature to the IF, where it is easier to provide quadrature outputs with accuracy rather than at RF. The following IF filter rejects the harmonics of the IF signal and reduces the transmitted noise. Then, the IF modulated signal is upconverted, amplified thanks to the PA, and transmitted by the antenna.

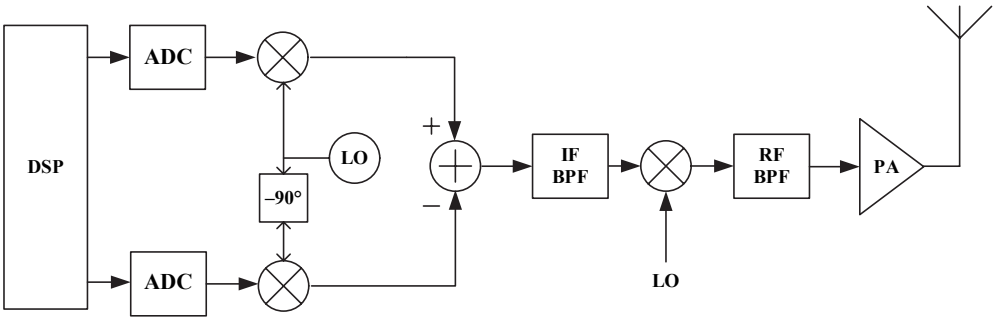

Figure 2.5: Heterodyne transmitter [3].

To suppress (50-60 dB) the unwanted sideband after the upconversion, an RF band-pass filter is necessary in order to meet spurious emission levels imposed by the standards.

This filter is typically passive and high-cost due to the off-chip components that compose it [1, 4]. As previously mentioned, this architecture does not allow full integration of the transmitter as a result of the off-chip passive elements in IF and RF filters.

2.2.2 Direct Upconversion Transmitter

In direct-conversion transmitters [48–50] (figure 2.6), the baseband signal is directly upconverted to RF. The RF output carrier frequency is equal to the LO frequency at the mixers input, and modulation and upconversion occur in the same circuit. A quadrature upconversion is required by modern modulations schemes. The simplicity of the architecture makes it attractive for high integration because there is no need to suppress any mirror signal generated during the upconversion. As in the receiver, the LO frequency is the carrier frequency [4]. The direct-conversion topology nonetheless suffers from an injection pulling [51] of the LO, whereby the oscillator frequency tends to shift towards the frequency of an external stimulus. This issue arises because the PA output is a modulated waveform having a high power and a spectrum centered around the LO frequency. The resulting spectrum cannot be suppressed by a bandpass filter because it has the same frequency as the wanted signal. To avoid this effect it is required an isolation higher than 60 dB.

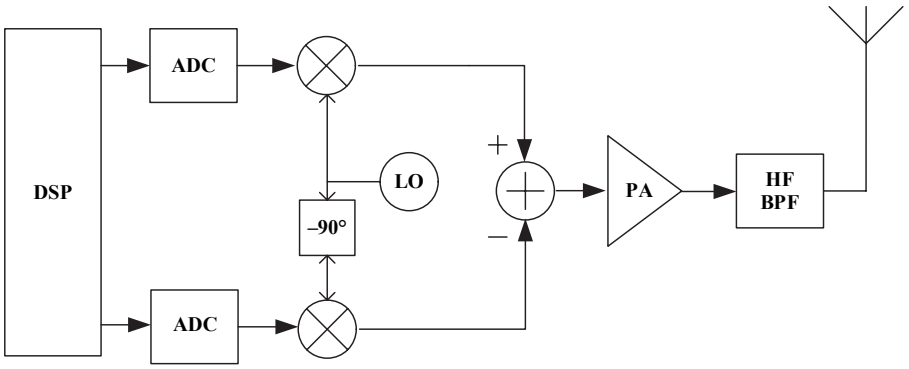

Figure 2.6: Direct upconversion transmitter [3].

A solution that settles the benefits of both heterodyne and direct upconversion was already proposed [52, 53], where the baseband signals are converted to a low IF and upconverted to the final carrier frequency through the use of an image-reject mixing technique to reject, avoiding the use of an RF filter after the upconversion. Therefore, it is possible to integrate the circuit with lower area and cost than with a conventional heterodyne approach.

CHAPTER 3

OSCILLATORS

In many transceivers, oscillators are one of the most important blocks in both the transmit and receive paths, since the quality of a up and downconversion depends on the quality of the oscillator produced signals. The requirements for oscillators used in receivers are more stringent than requirements for transmit oscillators. In addition to frequency stability, receiver LOs must have low Single-SideBand modulation (SSB) phase-noise required for adjacent channel selectivity and low wideband noise required for good receiver sensitivity and must be free of spurious modulation. Transmitter oscillators do have one unique requirement, called load pull, which is a measure of how much the oscillator frequency transmitter turn-on. In some applications, the oscillator's output harmonic content, current consumption, operation over extended temperature range, fast turn-on and turn-off times and easy modulation capability may be additional requirements [54].

Basically, an oscillator generates the LO periodic output signal at a specific or tunable frequency by converting a given DC level into a periodic signal without the interference of external signals. Interestingly, in most systems, one input of every mixer is driven by a periodic signal, hence the need for oscillators. Thus, oscillators can be roughly classified in two major categories [55, 56] (figure 3.1):

1. **quasi-linear oscillators** – based on the fulfilment of the Barkhausen criterion and characterized by sinusoidal output, such as the classical Wien-bridge, phase-shift oscillators [57] and LC oscillators. These oscillators are known by their good phase-noise performance, since Q is normally much higher than one. However, besides its large area of occupation due to the inductors, the LC oscillator itself cannot generate quadrature signals.

2. **strongly non-linear oscillators** – based on the use of non-linear devices (Schmitt-triggers and comparators), such as the astable multivibrator or the relaxation oscillator. Typically realized by RC-active circuits, this is a primary advantage since only resistors and capacitors are used together with the active devices (inductors, which are costly elements in terms of chip area, are not needed). On the other hand, relaxation oscillators present high phase-noise.

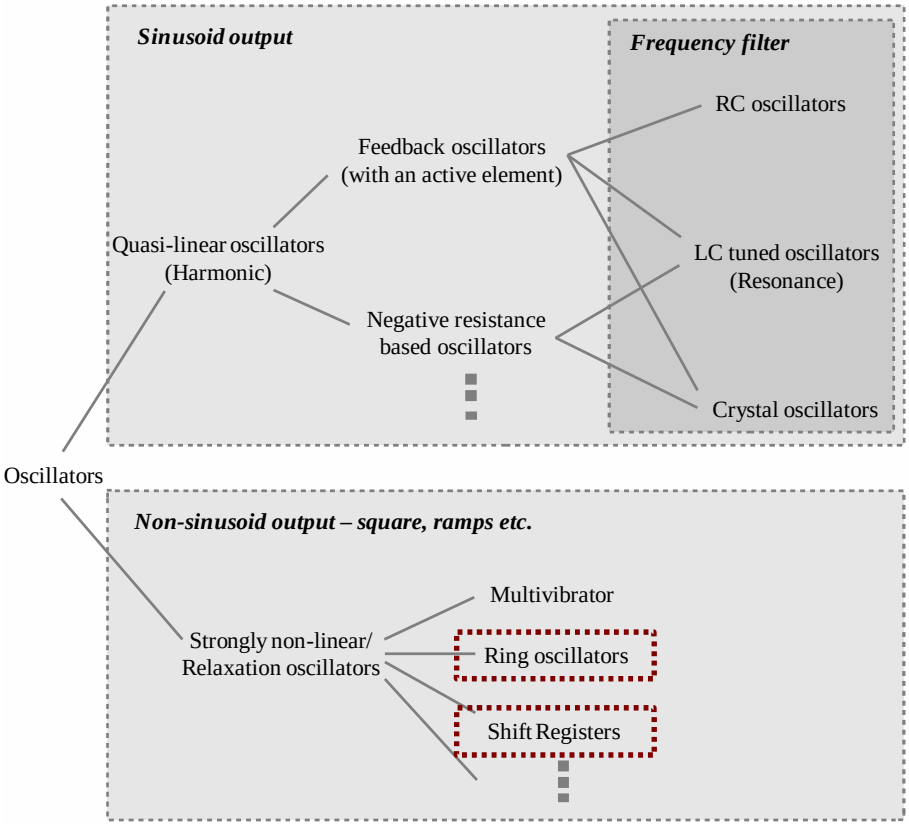

Figure 3.1: Classification of oscillators [58].

This chapter is organized as follows: first, a review of some basic concepts is introduced, where a description of the CMOS transistor model and the oscillator fundamentals are presented. Then, the oscillators are overviewed and characterized. The most used single oscillator topologies, the LC oscillator and the RC oscillator are also presented here [3, 59, 60]. We give a special attention to the conventional ring oscillator due to its importance and use throughout this work.

3.1 Basic Concepts

3.1.1 Performance

From a system designers perspective, the performance of a digital circuit expresses the computational load that the circuit can manage. For instance, a microprocessor is often

characterized by the number of instructions it can execute per second. This performance metric depends both on the architecture of the processor – for instance, the number of instructions it can execute in parallel –, and the actual design of logic circuitry. While the former is crucially important, it is not the focus of this work. When focusing on the pure design, performance is most often expressed by the duration of the clock period (clock cycle time), or its rate (clock frequency). The minimum value of the clock period for a given technology and design is set by a number of factors such as the time it takes for the signals to propagate through the logic, the time it takes to get the data in and out of the registers, and the uncertainty of the clock arrival times. At the core of the whole performance analysis, however, lays the performance of an individual gate.

The propagation delay t_P of a gate defines how quickly it responds to a change at its input(s). It expresses the delay experienced by a signal when passing through a gate. It is measured between the 50% transition points of the input and output waveforms, as shown in figure 3.2 for an inverting gate.[1] Since a gate displays different response times for rising or falling input waveforms, two definitions of the propagation delay are necessary. The t_{PLH} defines the response time of the gate for a LOW to HIGH (or positive) output transition, while t_{PHL} refers to a HIGH to LOW (or negative) transition. The propagation delay t_P is defined as the average of the two.

$$t_P = \frac{t_{PLH} + t_{PHL}}{2}. \tag{3.1}$$

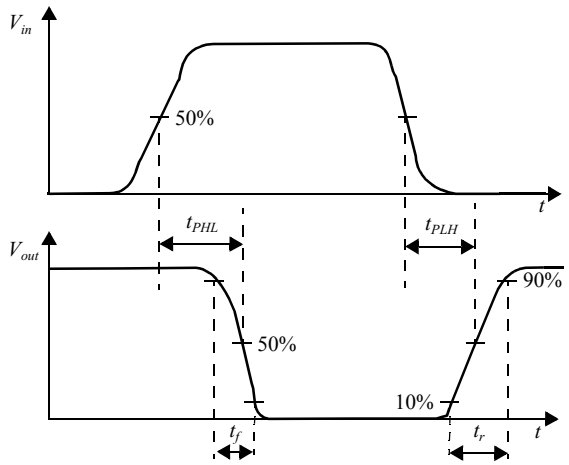

Figure 3.2: Definition of propagation delays and rise and fall times [61].

The propagation delay is not only a function of the circuit technology and topology, but depends upon other factors as well. Most importantly, the delay is a function of the slopes of the input and output signals of the gate. To quantify these properties, we introduce the rise and fall times t_r and t_f, which are metrics that apply to individual signal waveforms rather than gates (figure 3.2), and express how fast a signal transits

[1] The 50% definition is inspired the assumption that the switching threshold V_M is typically located in the middle of the logic swing.

between the different levels. The uncertainty over when a transition actually starts or ends is avoided by defining the rise and fall times between the 10% and 90% points of the waveforms, as shown in the figure. The rise/fall time of a signal is largely determined by the strength of the driving gate, and the load presented by the node itself, which sums the contributions of the connecting gates (fan-out) and the wiring parasitics.

When comparing the performance of gates implemented in different technologies or circuit styles, it is important not to confuse the picture by including parameters such as load factors, fan-in and fan-out. A uniform way of measuring the t_p of a gate, so that technologies can be judged on an equal footing, is desirable. The de-facto standard circuit for delay measurement is the ring oscillator, which will be presented in subsection 3.3.2 and applied in some structures that can be found in chapter 5.

Each cycle has an on-time (T_{on}) and an off-time (T_{off}) and considering all the work is done during on-time, the duration of these pulses and the number of cycles per second (frequency) are important. To describe the amount of "on-time", we use the concept of duty-cycle. Duty-cycle is defined as the proportion of time during which a component, device or system is operating. Abbreviated as D, the duty-cycle can be expressed as a ratio or as a percentage and is given by:

$$D = \frac{T_{on}}{T_{on} + T_{off}} = \frac{T_{on}}{T}, \tag{3.2}$$

where T is the period time of a completed cycle of pulse trains. If a digital signal spends half of the time on and the other half off, we would say the digital signal has a duty-cycle of 50% and resembles an ideal square wave. If the percentage is higher than 50%, the digital signal spends more time in the HIGH state than the LOW state and vice versa if the duty-cycle is less than 50%. Figure 3.3 illustrates these three scenarios.

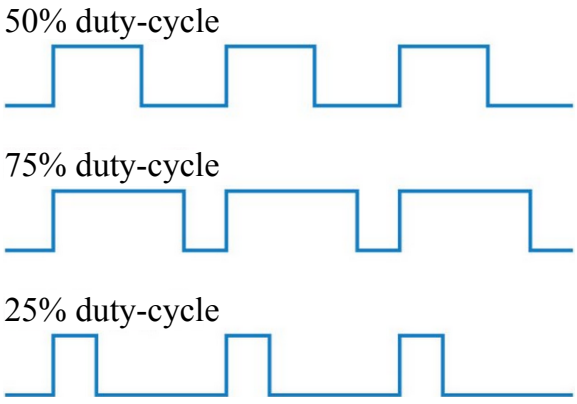

Figure 3.3: 50%, 75% and 25% duty-cycle examples.

3.1.2 MOS Transistor Overview

The Field-Effect Transistor (FET) is a device which uses an electric field through the oxide to control the transistor gate by turning it on and off, determining whether a current

flows between the drain and source or not. There are several types of FETs, of which the most widely used by far is the Metal-Oxide-Semiconductor (MOS) transistor. A large part of the sucess of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) transistor is due to the fact that it can be scaled to increasingly smaller dimensions, resulting in higher performance.

As a result of functionality per unit area (which in turn forces down the scale of the technology), substantially infinite input resistance and favourable operation as switches, MOS transistors are well-suited for designing digital circuits [62], where CMOS is the leading technology allowing the use of complementary devices such as Negative-channel Metal-Oxide-Semiconductor (NMOS) and Positive-channel Metal-Oxide-Semiconductor (PMOS). Due to its simplicity, versatility, low fabrication cost and the ability to improve performance consistently while decreasing power consumption, CMOS technology is usually preferred rather than any other, representing the majority of the manufactured Integrated Circuit (IC) in the world.

The signals of interest in analog ICs are often of the form:

$$v_{GS}(t) = V_{GS} + v_{gs}(t), \tag{3.3}$$

where V_{GS} is the fixed bias point and $v_{gs}(t)$ represents the small signal. Hence, the simplified incremental model of MOS transistor (when it is in saturation or active mode) must be considered, which can be represented as a voltage-controlled current source, as shown in figure 3.4, given by

$$i_d = g_m v_{gs}, \tag{3.4}$$

where i_d is the current that passes through the drain, g_m is the transconductance and v_{gs} is the voltage between gate and source terminals.

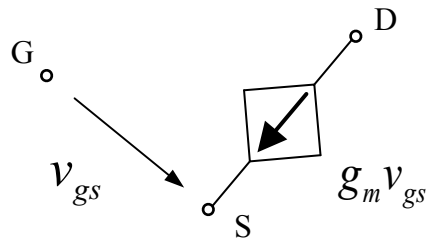

Figure 3.4: Simplified MOS transistor incremental scheme ($\lambda = 0$) [62].

MOS Capacitance Model

Any two conductors separated by an insulator form a parallel-plate capacitor. To analyse the main characteristics of a MOS transistor in its transitive work regime (Alternating Current (AC)), the parasitic capacitances must be considered because of their influence on the speed of operation of the MOS device and the MOS digital circuits. Based on physical structure of MOS, its parasitic capacitances can be classified into two major groups:

the gate capacitive effect (between the gate and the induced channel) and junction capacitances drain-body and source-body. The gate capacitance (approximate channel as connect to source) is the capacitance per area from gate across the oxide and is given by

$$C_{gs} = C_{ox} W L, \tag{3.5}$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$. How this gate capacitive effect manifests itself depends on the operation mode of the transistor. Finally, source and drain have undesirable capacitances to body (across reverse-biased diodes) called diffusion capacitance because it is associated with source/drain diffusion.

These two capacitive effects can be modelled by including capacitances in the MOS model between its four terminals gate (G), drain (D), source (S) and bulk (B) as shown in figure 3.5. Thus, there will be five capacitances, where the subscripts indicate the terminals [57, 63–67]:

1. C_{gs} – the gate-source capacitance models the effect of the charge under the gate.

2. C_{gd} – this capacitance models the effect of the gate-oxide overlap over the drain region. The C_{gd} and C_{gs} are overlap capacitances and voltage-dependent.

3. C_{db} and C_{sb} – depletion capacitances between drain-substrate and source-substrate, respectively.

4. C_{gb} – in addition to C_{gs} and C_{gd}, these parasitic capacitances depend on bias conditions since they are also voltage-dependent and distributed. They result from the interaction between the gate voltage and the channel charge.

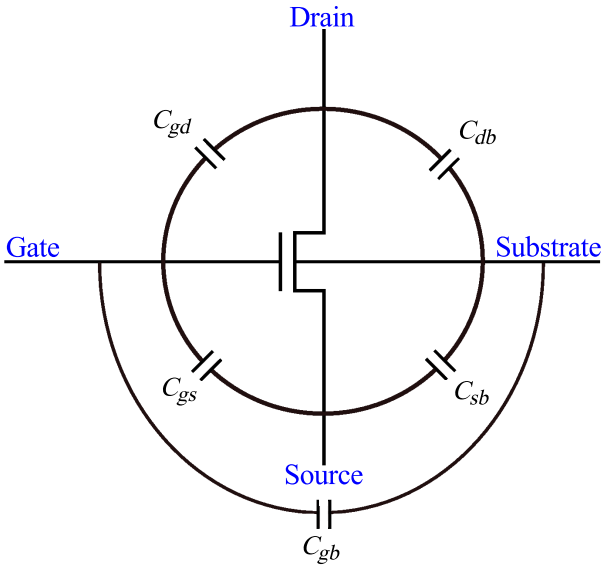

Figure 3.5: MOS capacitances [68].

The dynamic performance of digital circuits is directly proportional to these capacitances. Note that many of these capacitances are non-linear in that the capacitance varies with the voltage across the capacitance. A MOS transistor high-frequency, small-signal model is shown in figure 3.6.

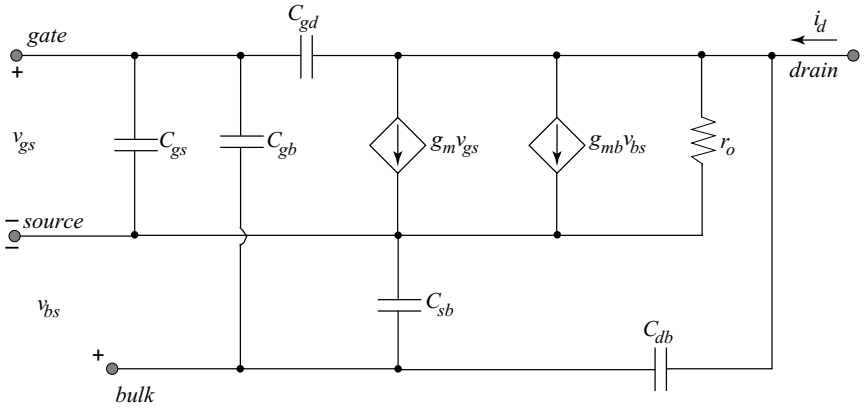

Figure 3.6: MOS high-frequency small-signal model [69].

This leads us to analyse the small-signals injected in the terminals of the transistor for each of the three different regions where the MOS transistor can operate, depending on the voltages at the terminals.

High-frequency Small-signal Analysis in the Active/Saturation Region

A high-frequency model of a MOS in the active region is shown in figure 3.7. Most of the capacitors in the small-signal model are related to the physical transistor. When MOS is operating in saturation mode, the channel has tapered shape and is pinched off at or near the drain end, thus the channel will not be uniform. Due to the change in V_{GS}, the gate-source capacitance C_{gs} is approximately given by [63]

$$C_{gs} \approx \frac{2}{3} W L C_{ox}, \tag{3.6}$$

where the 2/3 factor arises from the calculation of channel charge and inherently comes from integrating the triangular distribution assumed in figure 3.8 in the square-law regime.

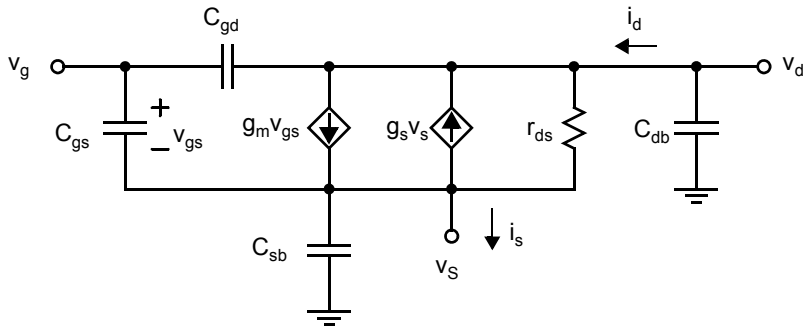

Figure 3.7: Small-signal model for a MOS transistor in the saturation region [70].

When accuracy is important, an additional term should be added to equation (3.6) to take into account the overlap between the gate and source junction, which should include the fringing capacitance due to boundary effects. This additional component is given by

$$C_{ov} = WL_{ov}C_{ox}, \tag{3.7}$$

where L_{ov} is the effective overlap distance and is usually empirically derived (usually taken larger than its actual physical overlap to more accurately give an effective value for overlap capacitances). Thus,

$$C_{gs} = \frac{2}{3}WLC_{ox} + C_{ov}, \tag{3.8}$$

when higher accuracy is needed.

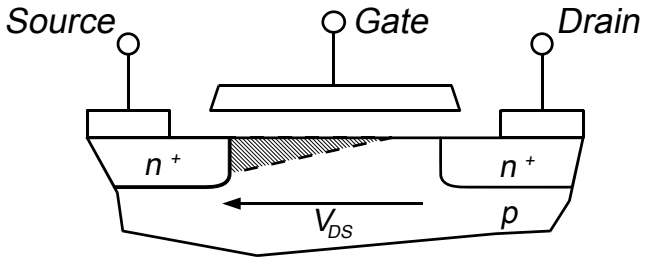

Figure 3.8: Cross section of a MOS operating in the saturation region.

The capacitance C_{gd}, known as the Miller capacitance, is important when there is a large voltage gain between gate and drain. It is primarily due to the overlap between the gate, the drain and fringing capacitance. Its value is given by

$$C_{gd} = WL_{ov}C_{ox}. \tag{3.9}$$

High-frequency Small-signal Analysis in the Triode/Linear Region

The accurate small-signal modelling of the high-frequency operation of a transistor in the triode region is nontrivial (even with the use of a computer simulation). A moderately accurate model is shown in figure 3.9, where the gate-to-channel capacitance and the channel-to-substrate capacitance are modelled as distributed elements. However, the I-V relationships of the distributed RC elements are highly non-linear because the junction capacitances of the source and drain are non-linear depletion capacitances, as is the channel-to-substrate capacitance. Besides, if V_{DS} is not small, then the channel resistance per unit length should increase as one moves closer to the drain. This model is much too complicated for use in hand analysis.

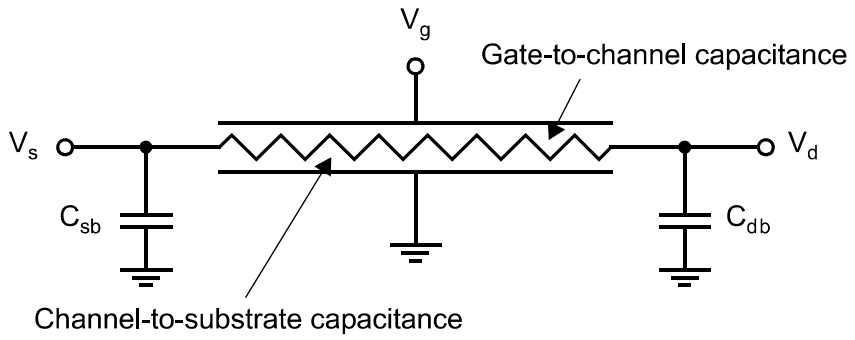

Figure 3.9: Distributed RC model for a transistor in the triode region [70].

A simplified model often used for small V_{DS} is shown in figure 3.10, where the resistance r_{ds} is the small-signal drain-source resistance. Here, the gate-channel capacitance has been evenly divided between the source and drain nodes:

$$C_{gs} = C_{gd} = \frac{1}{2}WLC_{ox} + C_{ov}. \tag{3.10}$$

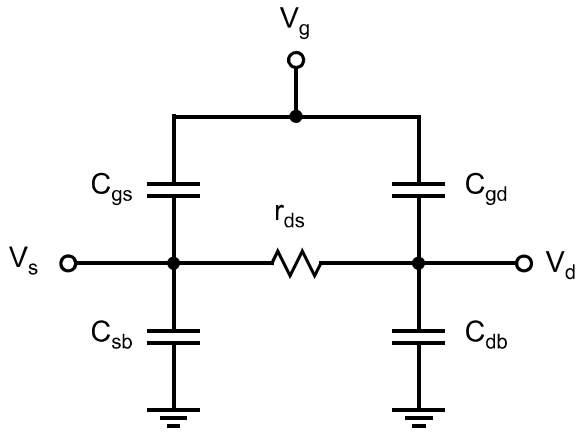

Figure 3.10: Simplified triode-region model valid for small V_{DS} [70].

High-frequency Small-signal Analysis in the Weak-inversion/Cut-off/Subthreshold Region

When the transistor turns off, the small-signal model changes considerably. A reasonable model is shown in figure 3.11. The most significant difference is that r_{ds} is now infinite. Another major difference is C_{gs} and C_{gd} which are now much smaller. Since the channel has disappeared, these capacitors are now due to only overlap and fringing capacitance. Thus,

$$C_{gs} = C_{gd} = WL_{ov}C_{ox}. \tag{3.11}$$

Their reduction does not mean that the total gate capacitance is necessarily smaller. The capacitor C_{gb} is highly non-linear and dependent on the gate voltage. If the gate voltage has been very negative for some time and the gate is accumulated, then

$$C_{gb} = WLC_{ox}. \tag{3.12}$$

If the gate-to-source voltage is around 0 V, then C_{gb} is equal to C_{ox} in series with the channel-to-bulk depletion capacitance and is considerably smaller, especially when the substrate is lightly doped. Another case where C_{gb} is small is just after a transistor has been turned off, before the channel has had time to accumulate. Because of the complicated nature of correctly modelling C_{gb} when the transistor is turned off, the equation (3.12) is usually used for hand analysis as a worst-case estimate.

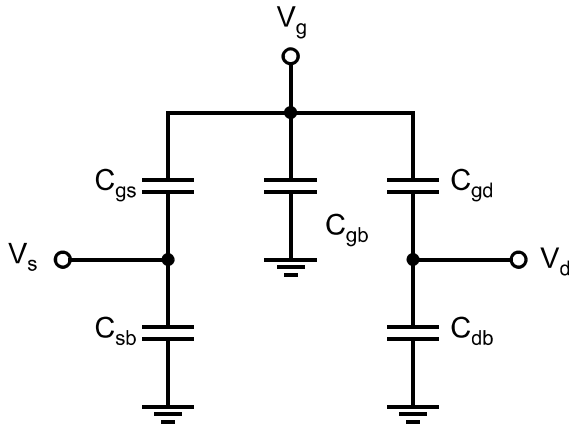

Figure 3.11: Small-signal model for a MOS that is turned off [70].

The sum of the three parasitic capacitances is then dependent of gate voltage. This sum has the maximal value of WLC_{ox} in the weak-inversion mode and the minimal value of $(1/2)WLC_{ox}$ in triode region.

3.1.3 Noise

Noise is an inevitable random process which limits the minimum signal level that a circuit can process with acceptable quality. Thus, it should be taken into account as other circuit parameter since it trades with power dissipation, speed and linearity [71]. Besides its responsibility for the degradation of the circuit performance, noise is frequently due to external interferences or to intrinsic material physical characteristics and its instant value cannot be foreseen at any time. Moreover, it is one of the most critical parameters in oscillators since they operate under large signal conditions [72–74]. Furthermore, the nonlinear noise is converted into different frequencies [43].

Figure 3.12 illustrates the different types of noise, the most commonly encountered in the context being white and pink (or $1/f$). Their color names are generally associated with the broad characteristic of their power spectrum. Note that white noise contains an equal amount of energy in all frequency bands, in contrast of $1/f$ noise which energy decreases as the frequency increases.

Following a general description of noise phenomenon and its effects, this subsection ends introducing thermal and flicker noise, the two main noise sources present in CMOS transistors.

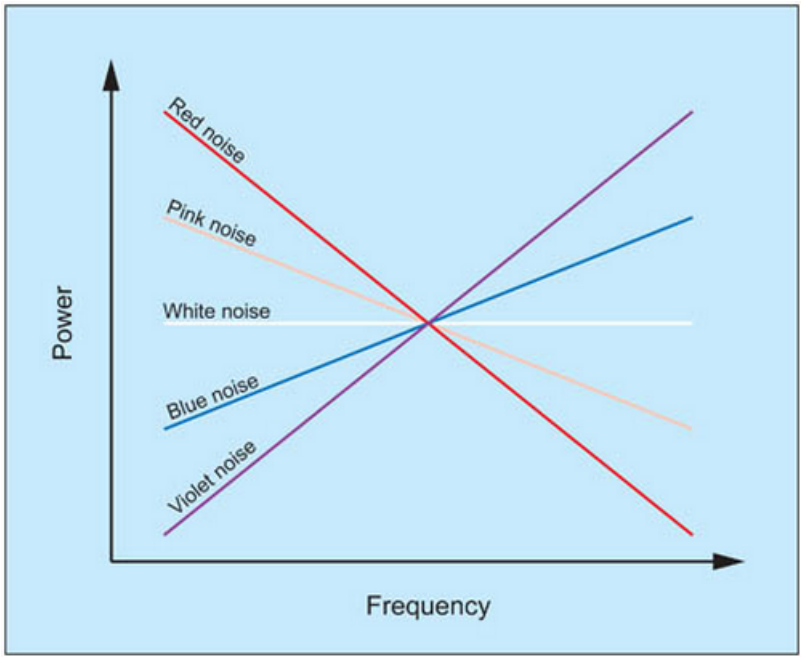

Figure 3.12: Types of noise [75].

Thermal Noise

Every ohmic resistor exhibits thermal noise caused by charge carriers generating a variation of current. This type of noise has a white (flat) spectrum that is proportional to absolute temperature [70]. As the temperature increases, the random motion of electrons increase and so does the corresponding noise level. The thermal noise power can be quantified by

$$P = kT\Delta f, \tag{3.13}$$

that is proportional to the material temperature T in Kelvin, where k is the Boltzmann's constant and Δf is the bandwidth that system covers. Usually it is assumed Δf=1 for notation simplicity, which means that noise is expressed per unit bandwidth. The spectral density generated in a resistor

$$\overline{V_n^2} = 4kTR\Delta f, \tag{3.14}$$

can be modelled as a voltage source with a Power Spectral Density (PSD) of $\overline{V_n^2}$ in series with a noiseless resistor (Thevenin equivalent) or as a current source with a PSD of $\overline{I_n^2}$ associated with a resistor in parallel (Norton equivalent) [1, 55, 76].

MOS transistors also exhibit thermal noise due to carrier motion through the channel, and it can be represented by a current source connect between the drain and source terminals.

The equations of thermal noise are defined depending in which regime the transistor is operating. If the device is operating in the triode region (where the drain-source conductance for $V_{DS} = 0$ V is $g_{d0} >> g_m$, and g_m is the transconductance), the noise

generated is [77]:

$$\overline{I_n^2} = 4kT\gamma g_m \Delta f, \tag{3.15}$$

where γ is the excess noise factor and has a value of unity for this bias condition ($\gamma = 1$). If the transistor is saturated [63], γ assumes the value of 2/3 for long-channel transistors and higher values for short-channel devices [78], and therefore:

$$\overline{I_n^2} = 4kT\gamma g_{d0} \Delta f. \tag{3.16}$$

Another source of thermal noise in MOS transistors is related with the gate resistance. Despite being more negligible than the noise due to channel carrier motion, this effect is becoming more important for new technologies, as the gate length is scaled down [1].

Flicker Noise

Flicker noise is a low-frequency noise present in all active devices, although only occurs when a DC current is flowing, and has origin in a phenomenon at the interface between the gate oxide (SiO_2) and the silicon substrate (Si). As a charge carriers move at the $SiO_2 - Si$ interface, some are randomly trapped and released introducing "flicker" noise in the drain current [71]. Beyond this phenomenon, other mechanisms are believed to generate flicker noise [63]. This type of noise is proportional to $1/f$, so it is dominant at low frequencies, and it is modelled more easily than the thermal noise as a voltage source in series with the gate, resulting in the following PSD:

$$\overline{V_{nf}^2} = \frac{K_f}{C_{ox} W L f^{\alpha_f}}, \tag{3.17}$$

where K_f is a process dependent constant, which is bias independent, C_{ox} is the gate oxide capacitance, W is the transistor channel width, L is the transistor channel length and the exponent α_f can assume values between 0.7 and 1.2 [63]. Note that a cleaner fabrication process results in power values for K_f. Therefore, for p-channel devices K_f is lower than for n-channel, and thus, PMOS transistors have less flicker noise than NMOS. Since flicker noise is well modelled as having a $1/f$ spectral density, figure 3.13 shows the power spectrum of flicker and thermal noise. The $1/f$ noise corner frequency f_c can be obtained by converting the flicker noise voltage (equation (3.17)) to current and equating the result to the thermal noise current expressed in equation (3.15) [1], so

$$\overline{f_c} = \frac{g_m K_f}{4kT\gamma g_m \Delta f C_{ox} W L f^{\alpha_f}}. \tag{3.18}$$

Nowadays, the corner frequency in MOS technologies is relatively constant and falls in the range of tens or hundreds of megahertz [1].

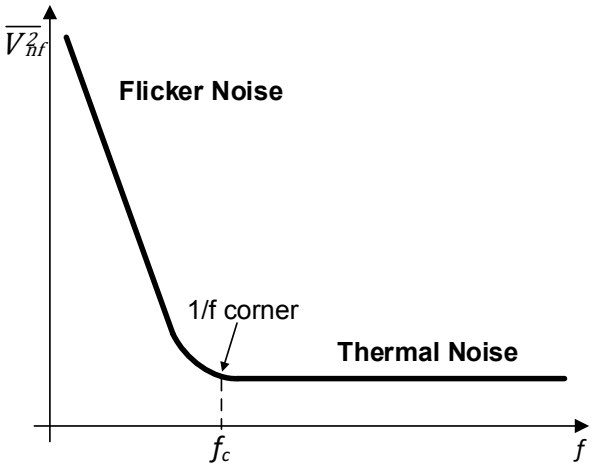

Figure 3.13: Power spectrum of flicker and thermal noise [79].

3.2 Oscillator Basic Concepts

An oscillator used in a RF transceiver must satisfy two sets of requirements: (i) system specifications (e.g., the frequency of operation, Q, phase-noise and the "purity" of the output), and (ii) "interface" specifications (e.g., the drive capability or output swing). In this section, a few of them will be considered, along with some basic principles and their role in the overall system.

3.2.1 Barkhausen Stability Criterion

At the core of any oscillator circuit is a loop that causes a positive feedback at a selected frequency. Figure 3.14 illustrates the generic closed-loop system representation. The mathematical condition for a circuit to oscillate can be established by combining the transfer functions of the amplification stage $A(j\omega)$ with the feedback stage $\beta(j\omega)$ to the closed-loop transfer function:

$$H_{CL}(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{A(j\omega)}{1 - A(j\omega)\beta(j\omega)}. \tag{3.19}$$

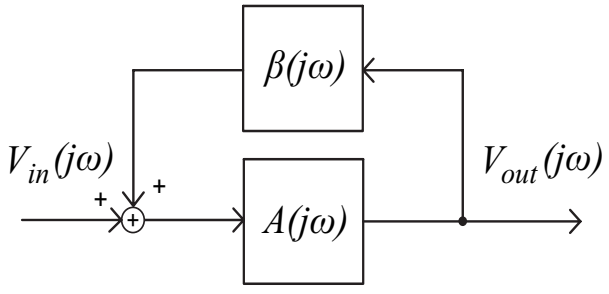

Figure 3.14: Basic oscillator configuration [3].

Oscillation will occur when the transfer function has a pair of complex conjugate poles over the imaginary axis. This happens when the denominator is equal to zero ($1 \pm A\beta = 0$) and therefore the closed-loop gain will be infinite and the corresponding time response will be sinusoidal. Analysing the open-loop gain $A\beta = 0$, it is possible to derive the conditions that ensure oscillation. The loop gain must be unity (amplitude condition) and according to the polarity of the feedback network this value may be either -1 or 1 which leads to the phase condition:

$$|A(j\omega_0)\beta(j\omega_0)| = 1 \tag{3.20}$$

$$\arg(A[j\omega_0]\beta[j\omega_0]) = 2k\pi. \tag{3.21}$$

This is known as the Barkhausen criterion, which presents the necessary conditions concerning the loop gain for steady-state oscillation with frequency ω_0 and k being an integer including zero. Although the Barkhausen criterion gives the necessary conditions for stable oscillations, the same is not valid for start-up. For the oscillation to start, triggered by noise, when the system is switched on, the loop gain must be larger than one, $|A(j\omega)\beta(j\omega)| > 1$ [55].

Note that the Barkhausen criterion is only valid for oscillators with a linear behaviour, such as the LC oscillators, considering they have a quasi-linear behaviour. In our case, this criterion cannot be applied since the objects of study in this work are based on RC oscillators, which present a strongly non-linear behaviour.

3.2.2 Quality Factor

Related to the total oscillator phase-noise and usually defined within the context of second order systems, the quality factor (Q) is the most common figure of merit for oscillators. However, there are three possible definitions of Q [1]:

1. While it can be defined in many ways, its most fundamental description measures the ratio of stored vs. lost energy per unit time. Consider that ω can assume the value of 2π for a sinusoid, while the same is not true for a square wave.

$$Q = \omega \frac{\text{Maximum energy stored in a period}}{\text{Energy dissipated in a period}}. \tag{3.22}$$

   Note that this definition is quite general and does not specify what type of system is required and which elements store or dissipate energy. However, this general definition is the only applicable to the case studies of this work, which was not taken into account because the RC oscillator presents a low Q, being at most one (since energy is stored on the capacitor in half-period and dissipated in the resistor on the other half), so it makes no sense to analyse it. In LC oscillators, the Q factor is $Q > 1$.

   This definition is usually applied to general RLC circuits and relates the maximum energy stored (in C or L) and the energy dissipated (by R) in a period. Considering

for instance a RLC series resonant circuit (resonant circuits are widely used when bandpass characteristics are required for interstage matching or filtering), the energy is stored in the inductor and the capacitor, and the maximum energy stored in the inductor and the capacitor is the same. At resonance, the reactances cancel out leaving just a peak voltage V_{rms} (root-mean-square voltage) across the loss resistor R. Thus, $I_{rms} = V_{rms}/R$ is the maximum current which passes through all elements.

The energy and stored in an inductor (W_L) is:

$$W_L = \int_0^T i(t) L \frac{di(t)}{dt} dt = L I_{rms}^2. \tag{3.23}$$

The energy dissipated in a resistor (W_R) per cycle (in the period T_0) is:

$$W_R = R I_{rms}^2 T_0. \tag{3.24}$$

Then, the value of Q is:

$$Q = \omega_0 \frac{L I_{rms}^2/2}{R I_{rms}^2/2} = \frac{\omega_0 L}{R}. \tag{3.25}$$

It is also possible to use the energy stored in the capacitor:

$$W_C = \int_0^T v(t) C \frac{dv(t)}{dt} dt = C V_{rms}^2. \tag{3.26}$$

Since the root-mean-square voltage in the capacitor is $V_{rms} = \omega_0 I_{rms}/C$, the value of Q is:

$$Q = \omega_0 \frac{C V_{rms}^2/2}{R I_{rms}^2/2} = \frac{1}{\omega_0 RC}. \tag{3.27}$$

2. In 1965, David B. Leeson considered a single resonator network with -3 dB bandwidth BW and resonance frequency ω_0 [60]. The following expression of Q is suitable for measuring the performance of filters and can be used in oscillators if we consider the resonator circuit as second order filter. As an example, the Q of a BPF is given by:

$$Q = \frac{\omega_0}{BW}. \tag{3.28}$$

In this case, ω_0 represents the filter center frequency and BW the filter bandwidth, which is $BW = \omega_2 - \omega_1$. Frequencies $omega_1$ and $omega_2$ are the frequencies in which the magnitude response of the filter drops 3 dB relatively to its maximum value (at w_0), as shown in figure 3.15.

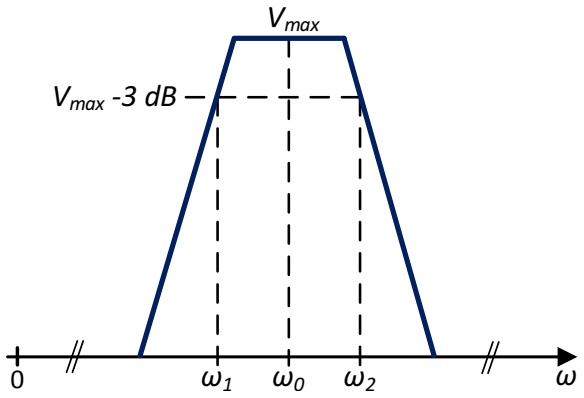

Figure 3.15: BPF frequency response and BPF Q factor [79].

The Q is a parameter that measures the filter sharpness (or selectivity) and as higher the Q is, the better is the filter. This means that a high-Q BPF can block undesired signals that are closer to the band of interest, comparing with a low-Q BPF.

3. In the third definition of Q the oscillator considered as a feedback system and the phase of the open-loop transfer function $H(j\omega)$ is evaluated at the oscillation frequency ω_{osc}, which is not necessarily the resonance frequency [26]. In a single RLC circuit, the oscillation frequency is the resonance frequency, but with coupled oscillators the oscillation frequency can be different. The oscillator Q is defined as:

$$Q = \frac{\omega_0}{2}\sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\theta}{d\omega}\right)^2}, \tag{3.29}$$

where A is the amplitude and θ is the phase of $H(j\omega)$. This definition, called open-loop Q, was proposed in [26], and takes into consideration the amplitude and phase variations of the open-loop transfer function. This Q definition is often applied to a single resonator, as shown in figure 3.16. Furthermore, it is also very useful to calculate the oscillator Q, which has its maximum value at the resonance frequency.

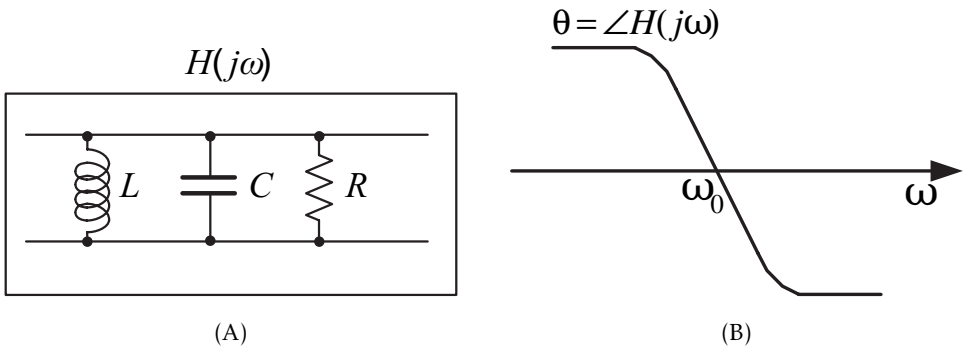

Figure 3.16: Definition of Q based on open-loop phase slope: (A) parallel RLC circuit (B) the phase of the parallel RLC circuit [3].

3.2.3 Phase-noise

Definition

In modern transceiver applications the most important difference between ideal and real oscillators is the phase-noise. An ideal oscillator produces a perfectly-periodic output of the form

$$x(t) = A\cos(\omega_0 t). \tag{3.30}$$

The zero crossings occur at exact integer multiples of $T_0 = 2\pi/\omega_0$. In reality, however, the noise of the oscillator devices randomly perturbs the zero crossings. To model this perturbation, we write

$$x(t) = A\cos(\omega_0 t + \phi_n(t)), \tag{3.31}$$

where $\phi_n(t)$ is a small random phase quantity that deviates the zero crossings from integer multiples of T_0. Figure 3.17 illustrates the two waveforms in the time domain. The term $\phi_n(t)$ is the phase-noise.

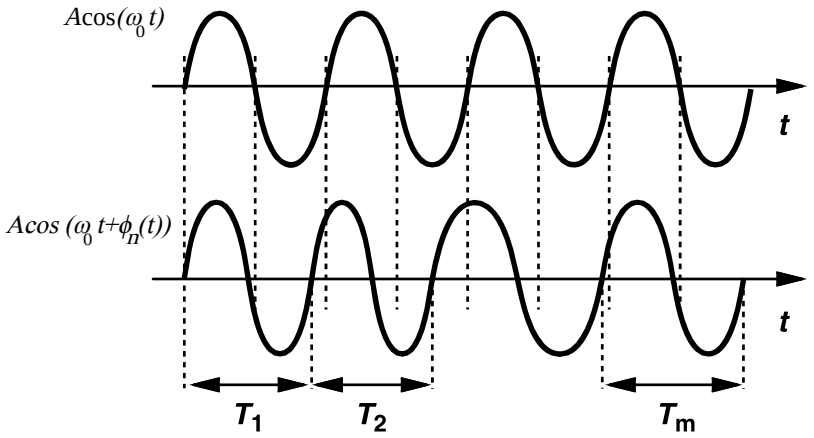

Figure 3.17: Output waveforms of an ideal and a noisy oscillator [1].

The noise generated at the oscillator output causes random fluctuation of the output amplitude and phase. This means that the output spectrum has bands around ω_0 and its harmonics (figure 3.18). With the increasing order of the harmonics of ω_0 the power in the sidebands decreases [80].

The noise can be generated either inside the circuit (due to active and passive devices) or outside (e.g., by power supply). Effects such as non-linearity and periodic variation of the circuit parameters make it very difficult to predict phase-noise [26]. The noise causes fluctuations of both amplitude and phase. Since, in practical oscillators there is an amplitude stabilization scheme, which attenuates amplitude variations, phase-noise is usually dominant. The oscillator noise can be characterized either in the frequency domain (phase-noise), or in the time domain (jitter). The first is used by analog and RF designers, while the second is used by digital designers [25, 26, 80].

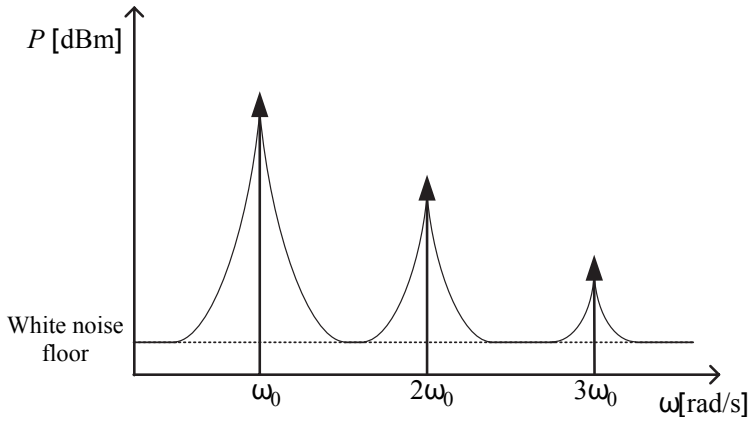

Figure 3.18: Spectrum of oscillator output with phase-noise [3].

There are several ways to quantify the fluctuations of phase and amplitude in oscillators. They are often characterized in terms of the single sideband noise spectral density $\mathcal{L}(\omega)$, expressed in decibels below the carrier per hertz (dBc/Hz). This characterization is valid for all types of oscillators and is defined as:

$$\mathcal{L}(\omega_m) = \frac{P(\omega_m)}{P(\omega_0)}, \tag{3.32}$$

where $P(\omega_m)$ is the single sideband noise power at a distance of ω_m from the carrier (ω_0) in a 1 Hz bandwidth and $P(\omega_0)$ is the carrier power.

The advantage of this parameter is its ease of measurement. This can be done by using a spectrum analyser (which is a general-purpose equipment, but will introduce some errors) or with phase or frequency demodulators with well known properties (which are dedicated and expensive equipment). Note that the spectral density (equation (3.32)) includes the both phase and amplitude noise, and they cannot be separated. However, practical oscillators have an amplitude stabilization mechanism, which strongly reduces the amplitude noise, while the phase-noise is unaffected. Thus, the equation (3.32) is dominated by the phase-noise and $\mathcal{L}(\omega_m)$ is simply known as phase-noise.

Leeson-Cutler Phase-noise Equation

The semi-empirical model proposed in [60, 81, 82], also known as the Leeson-Cutler phase-noise model, is based on the assumption that the oscillator is a Linear Time-Invariant (LTI) system. It predicts the phase-noise behaviour as follows [83]:

$$\mathcal{L}(\omega_m) = 10\log\left\{\frac{2FkT}{P_s}\left(1+\left[\frac{\omega_0}{2Q_L\omega_m}\right]^2\right)\left(1+\frac{\omega_{1/f^3}}{|\omega_m|}\right)\right\}, \tag{3.33}$$

where:

F – empirical parameter, called excess noise factor. A detailed study of this parameter, which includes non-linear effects for LC oscillators, was done in [84].

k – Boltzmann's constant;

T – absolute temperature;

P_S – average power dissipated in the resistive part of the tank;

ω_0 – oscillation frequency;

Q_L – effective quality factor of the tank with all the loadings in place (also known as loaded Q);

ω_m – offset from the carrier;

ω_{1/f^3} – corner frequency between $1/f^3$ and $1/f^2$ zones of the noise spectrum (represented in figure 3.19).

The first term $2FkT/P_s$ represents the noise floor. The second term $(\omega_0/2Q\omega_m)^2$ refers to the loaded Q factor. Unloaded $Q = Q_u = \omega_0/BW$, where BW is the bandwidth. Therefore, $1/Q_L = 1/Q_u + 1/Q_E$, where Q_E is dominated by the coupling and the device gain (g_m). Finally, the third term $\omega_{1/f^3}/|\omega_m|$ refers to phase perturbations and flicker effects.

A different model to predict the oscillator phase-noise was presented in [83]. This is a Linear Time-Variant (LTV) model, which, according to the authors, gives accurate results without any empirical or unspecified factor.

In figure 3.19, a typical asymptotic output noise spectrum of an oscillator is shown. The $1/f$ noise is not included, assumed to be dominated by the $1/f^2$ noise. This model can be divided into three different regions [80], considering the SSB spectral density:

(1) In the region close to the carrier frequency, with frequencies between ω_0 and ω_1 there is a -30 dB/decade slope due to the $1/f$ noise of the active devices.

(2) A region $\omega_1 - \omega_2$ with a -20 dB/decade slope is due to FM of the oscillator by its white noise sources.

(3) For frequencies far away from the carrier, the noise of the oscillator is due to white-noise sources from circuits, such as buffers, which are connected to the oscillators, so there is a constant floor in the spectrum.

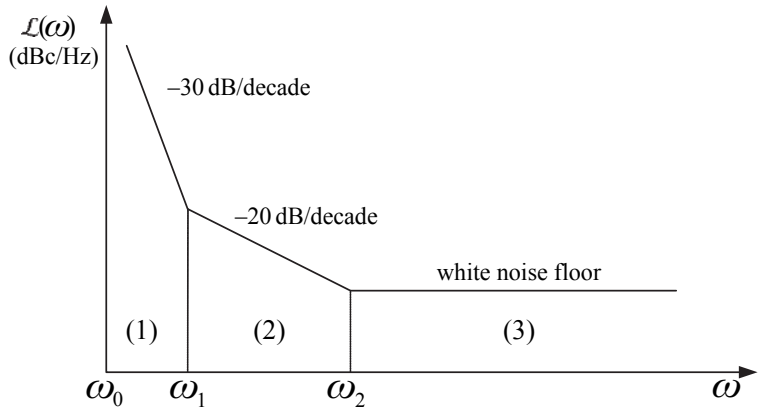

Figure 3.19: A typical asymptotic noise spectrum at the oscillator output [3].

Although the Leeson-Cutler Phase-noise Equation is very intuitive and simple to use, it is difficult to gain insight beyond increase P_s and increase Q_L. The following equation is the foundation for the oscillator Figure of Merit (FoM):

$$\text{FoM} = \mathcal{L}(f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log(P_s). \tag{3.34}$$

Role of Phase-noise in Wireless Communications

The exponential growth of the wireless communications has augmented the demand for more communication channels. This demand is usually hard to satisfy because the number of available channels is limited by the receiver's capability to accurately tune to a specific channel without being affected by the adjacent interfering channels. As shown in figure 3.20, an interfering signal can modulate the phase-noise of the LO and generate an interfering tone at the intermediate frequency. Thereafter, this interfering tone will be indistinguishable from the desired signal and thus cannot be removed by filtering. Since the phase-noise of the LO determines the power of this interfering tone, it is of great practical significance. This phenomenon will limit the immunity against adjacent interferer signals:

1. In the receiver path we want to downconvert a specific channel located at a certain distance from the oscillator frequency; due to the oscillator phase-noise, not only the desired channel is downconverted to an intermediate frequency, but also the nearby channels or interferers, corrupting the wanted signal (figure 3.21). This effect is called "reciprocal mixing" [26, 80].

2. In the case of the transmitter path the phase-noise tail of a strong transmitter can corrupt and overwhelm close weak channels [80] (figure 3.22), As an example, if a receiver detects a weak signal at ω_2, this will be affected by a close transmitter signal at ω_1 with substantial phase-noise.

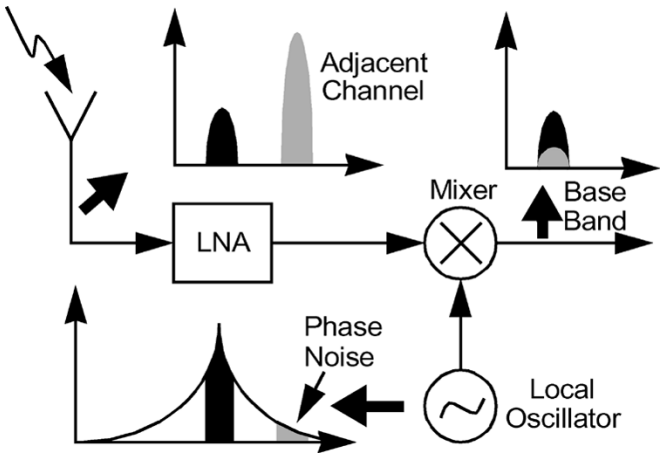

Figure 3.20: Phase-noise effect on RF systems [24].

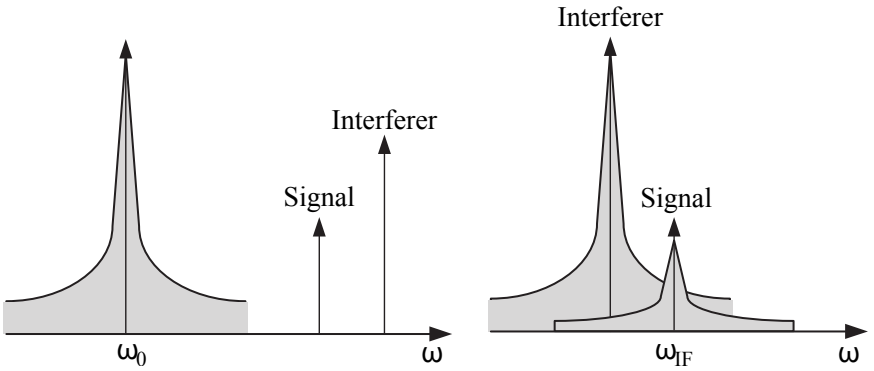

Figure 3.21: Phase-noise effect on the receiver and the undesired downconversion [3].

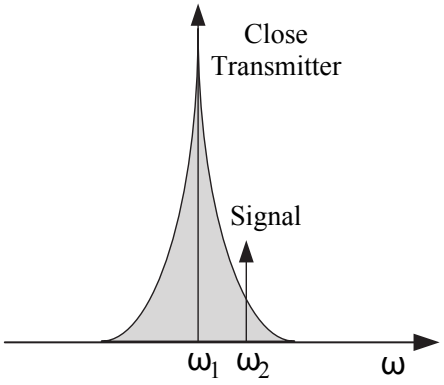

Figure 3.22: Phase-noise effect on the transmitter path [3].

3.2.4 Figure of Merit

Figure of Merit (FoM) is a characteristic that gives an overall perspective of the device, system or method (in our case the oscillator), relative to its alternatives. Usually used in literature for benchmark comparison, it takes into account not only the phase-noise $\mathcal{L}(f)$ but also the power consumption P_{DC} given by $P_{DC} = I_{core}V_{DD}$, and the frequency of the oscillator f_0, as can be seen in equation (3.35). Assuming a $1/f^2$-slope of the noise spectrum as described by the Leeson's oscillator model [60], the following relation is reasonable [85]:

$$\text{FoM} = \mathcal{L}(f) + 10\log\left(\frac{P_{DC}}{P_{ref}}\left[\frac{\Delta f}{f_0}\right]^2\right), \tag{3.35}$$

where P_{ref} is the reference power of 1 mW and Δf is the offset from the fundamental frequency f_0.

The minimum phase-noise for the relaxation and ring oscillators is given in equations (3.36) and (3.37), respectively [24].

$$\mathcal{L}_{relax}(f) \approx \frac{3.1kT}{P_{DC}}\left(\frac{f_0}{\Delta f}\right)^2 \tag{3.36}$$

$$\mathcal{L}_{ring}(f) \approx \frac{7.33kT}{P_{DC}}\left(\frac{f_0}{\Delta f}\right)^2. \tag{3.37}$$

There is also a FoM concerning the layout area (equation (3.38)), where A_{chip} is the circuit area in mm^2 and A_{ref} is a reference area ($1mm^2$) [86, 87].

$$\text{FoM}_A = \mathcal{L}(f) + 10\log\left(\frac{P_{DC}A_{chip}}{P_{ref}A_{ref}}\left[\frac{\Delta f}{f_0}\right]^2\right). \tag{3.38}$$

The FoM of an oscillator provides a qualitative insight on the relations between design parameters, allowing a designer to further optimize the circuit.

There is another FoM that allows further analysis of the oscillator performance, called Oscillator Design Efficiency (ODE) [86, 88]. This benchmark compares the phase-noise with a first order estimation of the best phase-noise case achievable (equation (3.39)). Although its use in LC oscillators, the ODE has been modified specifically for N-stage ring oscillators [86], such as the two-integrator oscillator (equation (3.40)).

$$ODE_{LC} = \mathcal{L}(f) - 10\log\left(\left[\frac{kT}{2P_{DC}Q^2}\frac{\Delta f}{f_0}\right]^2\right) \tag{3.39}$$

$$ODE_{ring} = \mathcal{L}(f) - 10\log\left\{\left(\frac{N^2kT}{4P_{DC}\left[\frac{\pi}{2}\right]^2}\frac{\Delta f}{f_0}\right)^2\right\}. \tag{3.40}$$

3.3 Single Oscillator Topologies

As the title suggests, in this section the most common single oscillator topologies are presented, namely the quasi-linear LC and strongly non-linear RC oscillators. Their advantages and disadvantages are also exposed, as well as a few examples of each topology.

In RC oscillators, the relaxation oscillator and ring oscillator are presented, considering they are usually realized by RC-active circuits. Quadrature RC oscillators are used in many modern transceiver architectures, as they can be fully integrated (do not require external components), have low area (similar to that of a single a single integrated inductor) and low cost, have a wide tuning range (useful to cover several bands), and they are able to provide quadrature (I/Q) signals with low quadrature error.

The structure and principle of ring oscillator are carefully analysed, since in Chapter 4 several types of this architecture will be applied, along with different stages to generate multiphases.

3.3.1 LC Oscillator

The LC oscillator is a type of oscillator where a LC (inductor-capacitor) tank circuit is used to guarantee the phase shift for oscillation, notwithstanding the use of dielectric resonators, crystals or striplines oscillators as resonator element. This pure reactance

feedback circuit is also termed as LC resonant circuit or LC tuned circuit, where the resonance is provided by a parallel LC combination. Although inductors consume a lot of area when compared to inductorless oscillators, it is a must in RF design to use inductors because of two primary reasons [1]. They are as follows:

- The resonance of inductors with capacitors allow for higher operational frequency and lower phase-noise, since Q is normally much higher than one (current is exchanged between the capacitor and inductor).
- The inductor sustains a very small DC voltage drop which aids in low supply operation.

Considering the second-order resonant LC tank quasi-linearity and sustained oscillations, the Barkhausen criterion can be applied, where the oscillation will occur at the frequency for which the amplitude of the loop gain is one and the phase is zero. The LC oscillator model is represented in figure 3.23: the transfer function is $H(j\omega) = g_m$, $\beta(j\omega)$ is the impedance of the parallel RLC circuit and the frequency of oscillation ω_0 is the resonant frequency of the tank.

$$\beta(j\omega) = \frac{R}{1 + j\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)Q}, \tag{3.41}$$

where the Q and the frequency of oscillation are respectively

$$Q = R\sqrt{\frac{C}{L}} \tag{3.42}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}. \tag{3.43}$$

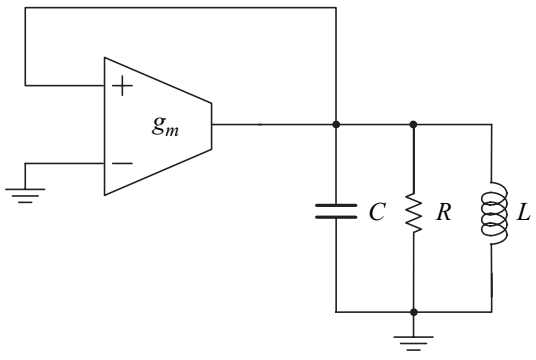

Figure 3.23: LC-oscillator behavioural model [3].

At the resonance frequency (ω_0) the inductor and capacitor admittances cancel and the loop again is $|H(j\omega_0)\beta(j\omega_0)| = g_m R = 1$: the active circuit has a negative resistance, which compensates the resistance of the parallel RLC circuit. This condition is necessary but not sufficient, because for the oscillation to start, the loop gain must be higher than 1, $g_m > 1/R$.

In figure 3.24, a typical LC oscillator, used in RF transceivers, is shown. This is known as LC oscillator with LC-tank, and it is also called differential CMOS LC oscillator, or negative g_m oscillator. The inductors provide a DC bias voltage to the transistor gates and drains ensuring they are in saturation. The cross-coupled NMOS transistors (M) generate a negative resistance, which is in parallel with the lossy LC tank (figure 3.25).

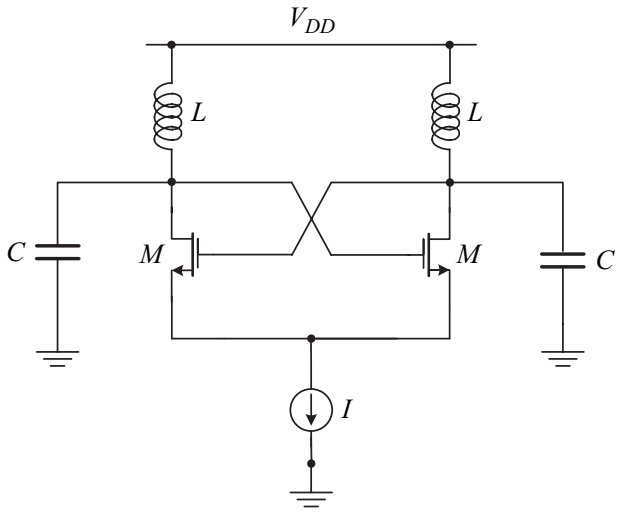

Figure 3.24: CMOS LC oscillator with LC tank [3].

In figure 3.25, the small-signal model of the differential pair is shown. Since the circuit is symmetric, the controlled sources have the currents shown in figure 3.25 and the equivalent resistance of the differential pair is:

$$R_x = \frac{v_x}{i_x} = -\frac{2}{g_m}. \tag{3.44}$$

Thus, the differential pair realizes a negative resistance (figure 3.25) that compensates the losses in the tank circuit.

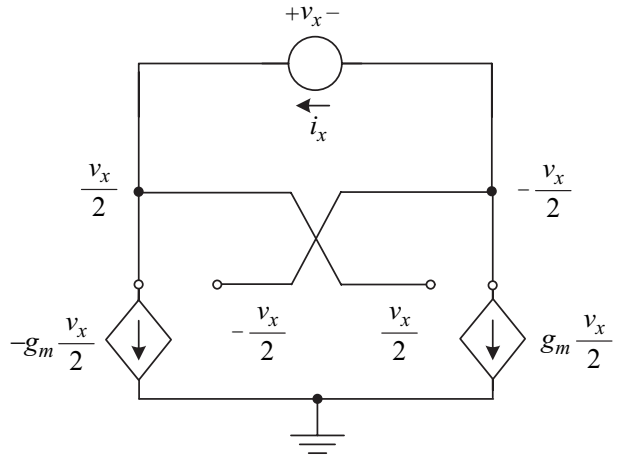

Figure 3.25: Equivalent resistance of the differential pair [3].

Despite its good phase-noise characteristics and its ease of implementation, the LC oscillator presents some drawbacks. First, it has low frequency tuning capability since the feedback network parameters are fixed ($\omega_0 = 1/\sqrt{LC}$). Moreover, the integration in CMOS technology would require large area consumption, which as we know is not desirable. Finally, modern receivers require quadrature outputs, which this oscillator alone is not able to provide. The solution lies in coupling an additional oscillator, which will increase even more the area used as well as it will degrade the frequency response due to the additional parasitic capacitances.

3.3.2 RC Oscillator

There has been a major interest in the latest years over the study and design of RC oscillators. RC oscillators, such as ring and relaxation oscillators, are especially known for their ease of integration and large tuning ranges. Besides they occupy far less area than a LC oscillator, the main difference is that now the feedback network is formed by a capacitor and a resistor, and that is the reason why RC oscillator presents lower Q. Furthermore, RC oscillators are normally much noisier than LC oscillators, given a certain power budget. Nevertheless, the main advantage of RC oscillators is that only resistors and capacitors are used together with the active devices.

The capacitor is used to convert the DC current into voltage (as shown in equation (3.45)) and the resistor is used for biasing. In this subsection, the two most common RC oscillator topologies are highlighted: the relaxation oscillator and the ring oscillator. Generally, beyond the performance of ring oscillator is better than relaxation oscillators, relaxation oscillators do not have in principle particular advantages at high frequencies.

$$v(t) = \frac{1}{C}\int_{t_0}^{t} i(\tau)d\tau + v(t_0). \tag{3.45}$$

Relaxation Oscillator

One of the most used high frequency oscillators is the relaxation or first-order RC oscillator (since its behaviour can be described in terms of first order transients) [10, 89], mainly in applications with relaxed phase-noise requirements [11], typically part of a Phase-Locked Loop (PLL). Relaxation oscillators do not require inductors and can be implemented in a standard low-cost technology, without RF options. A circuit level implementation is represented in figure 3.26. It operates by alternately charging and discharging the capacitor between two threshold voltage levels that are set internally. Since this is not a linear oscillator, the oscillation frequency cannot be determined by the Barkhausen criterion.

In a first-order analysis, the relaxation oscillator frequency depends only on resistor (R) and capacitor (C) values, where the resonant frequency is given by:

$$f = \frac{1}{8RC}, \tag{3.46}$$

which makes it suitable to guarantee the wanted oscillation frequency. At these high frequencies the oscillation is approximately sinusoidal [90]. The amplitude is dependent on the current (I) and R. The circuit only oscillates if the I is high enough to make the loop gain higher than one. The source current determines the amplitude of the modulated pulses [91].

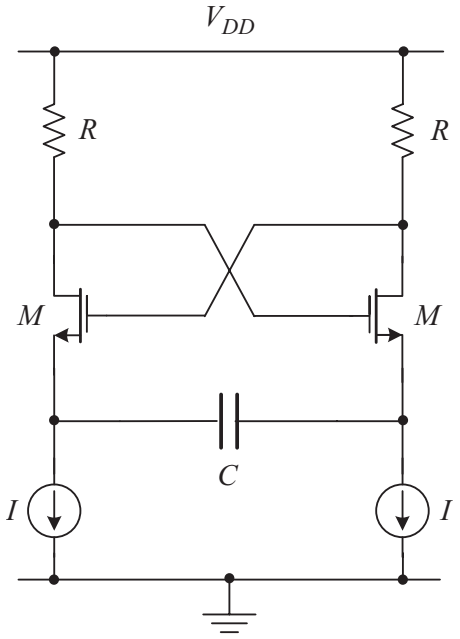

Figure 3.26: A conventional relaxation oscillator [3].

An advantage emerges when designing this type of oscillator in CMOS technology. The capacitor can be achieved just by the presence of the MOS parasitic capacitances thus reducing the area required for implementation.

Quadrature relaxation oscillators are often needed for receiver architectures since they can be fully integrated (because they do not have inductors), consequently have low area, have higher tuning range (useful to cover several bands) and are able to provide I/Q signals with low quadrature error. However, these oscillators have not been popular in RF design because they present poor phase-noise, and have noisy activate and passive devices [3, 92].

Ring Oscillator

The ring oscillator at RF has raised interest among CMOS IC designers because it is simple, fast and readily yields output phases in quadrature. A ring oscillator is realized by placing an odd number of open-loop inverting amplifiers in a feedback loop for periodic variation of the stage voltages (figure 3.33). The simplest type of amplifier that can be used is a simple digital inverter, as shown in figure 3.27(A). The oscillation frequency is determined by the number of the delay stages and the average propagation delay of the delay stages of the oscillator:

$$f_0 = \frac{1}{N(t_{PLH} + t_{PHL})}, \tag{3.47}$$

assuming the inverters are identical and N is the number (odd) of inverters in the ring oscillator. The sum of the low-to-high (LH) and high-to-low (HL) delays is used to calculate the period of the oscillation because each inverter switches twice during a single oscillation period. Thus, the switching behaviour of the inverter can be generalized by examining the parasitic capacitances and resistances associated with the inverter. Consider the inverter shown in figure 3.27 with his equivalent digital model. When V_{in} is high and equal to V_{DD}, the NMOS (M_1) transistor is on, while the PMOS (M_2) is off. A direct path exists between V_{out} and the ground node, resulting in a steady-state value of 0 V. On the other hand, when the input voltage is low (0 V), M_1 and M_2 are off and on, respectively. This yields to a high output voltage and to conclude that the gate clearly functions as an inverter. The effective input capacitance of the inverter is

$$C_{in} = \frac{3}{2}(C_{ox1} + C_{ox2}) = C_{inn} + C_{inp}. \tag{3.48}$$

The effective output capacitance of the inverter is simply

$$C_{out} = C_{ox1} + C_{ox2} = C_{outn} + C_{outp}. \tag{3.49}$$

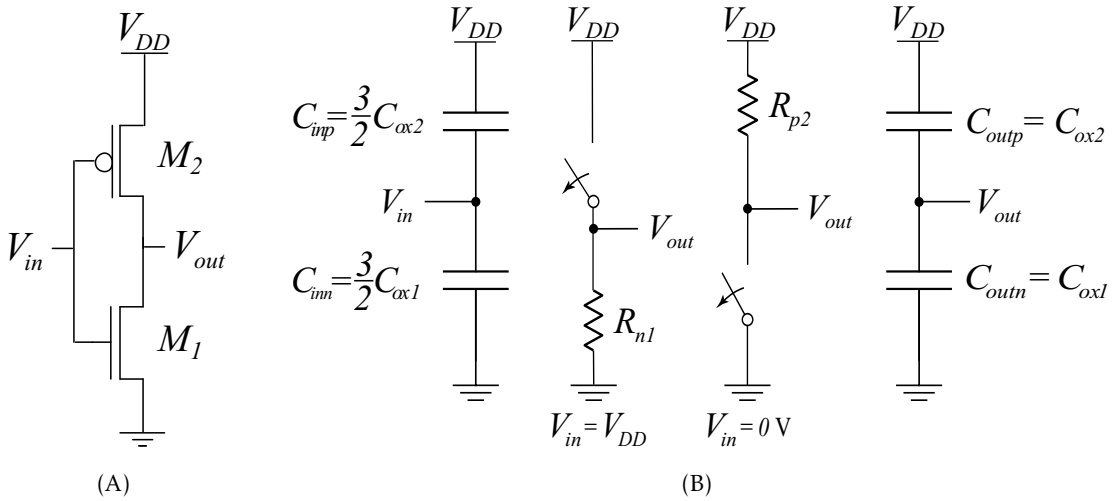

Figure 3.27: CMOS inverter switching characteristics using the digital model: (A) CMOS inverter circuit (B) Switch models of CMOS inverter.

The intrinsic propagation delays of the inverter are

$$t_{PLH} = 0.7 R_{p2} C_{out} \tag{3.50}$$

$$t_{PHL} = 0.7 R_{n1} C_{out}. \tag{3.51}$$

The propagation delays for an inverter driving a capacitance load are

$$t_{PLH} = 0.7R_{p2}C_{tot} = 0.7R_{p2}(C_{out} + C_L) \tag{3.52}$$

$$t_{PHL} = 0.7R_{n1}C_{tot} = 0.7R_{n1}(C_{out} + C_L). \tag{3.53}$$

where C_{tot} is the total capacitance on the output of the inverter, that is, the sum of the output capacitance of the inverter, any capacitance of interconnecting lines and the input capacitance of the following gate(s).

When identical inverters are used, the capacitance on the inverter's input/output is the sum of an inverter's input capacitance with the inverter's output capacitance:

$$C_{tot} = C_{out} + C_{in} = (C_{oxp} + C_{oxn}) + \left(\frac{3}{2}[C_{oxp} + C_{oxn}]\right) = \frac{5}{2}(C_{oxp} + C_{oxn}). \tag{3.54}$$

The delay is then calculated using

$$t_{PLH} + t_{PHL} = 0.7(R_p + R_n)C_{tot}. \tag{3.55}$$

Concerning the dynamic power dissipation, consider the CMOS inverter driving a capacitance load shown in figure 3.28. Each time the inverter changes states, it must either supply a charge to C_{tot} or sink the charge stores on C_{tot} to ground. If a square pulse is applied to the input of the inverter with a period T and frequency f_{clk}, the average amount of current that the inverter must pull from V_{DD}, recalling that current is being supplied from V_{DD} only when the PMOS device is on, is

$$I_{avg} = \frac{Q_{Ctot}}{T} = \frac{V_{DD}C_{tot}}{T}. \tag{3.56}$$

The average dynamic power dissipated by the inverter is

$$P_{avg} = V_{DD}I_{avg} = \frac{C_{tot}V_{DD}^2}{T} = C_{tot}V_{DD}^2 f_{clk}. \tag{3.57}$$

Notice that the power dissipation is a function of the clock frequency, voltage power supply and load capacitance. A great deal of effort is put into reducing the power dissipation in CMOS circuits. One of the major advantages of dynamic logic is its low power dissipation.

Although it is not the case, the N-stage ring oscillator can theoretically produce ideal sinusoidal waveforms. In this case the oscillator works completely in linear mode. On the other hand, when all transconductors have the limiting transfer characteristic defined in equation (3.58), and the output voltage is much larger than V_{lim}, the oscillator works in strongly non-linear mode. In this mode the transconductors in the oscillator are fully switching and deliver $-I_{lim}$ or I_{lim} with a 50% duty-cycle.

$$I_{out}(V_{in}) = \begin{cases} I_{lim} = g_m V_{lim}, & \text{if } V_{in} \geq V_{lim}, \\ g_m V_{in}, & \text{if } -V_{lim} < V_{in} < V_{lim}, \\ -I_{lim} = -g_m V_{lim}, & \text{if } V_{in} \leq -V_{lim}. \end{cases} \tag{3.58}$$

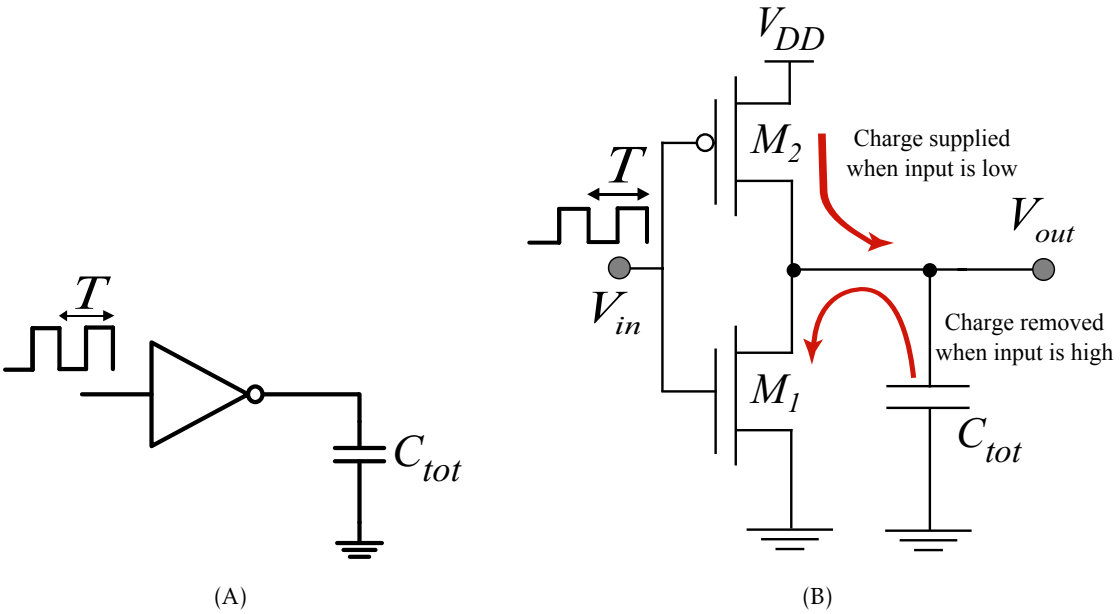

Figure 3.28: Dynamic power dissipation of the CMOS inverter: (A) Inverter standard block diagram (B) Dynamic power dissipation process [93].

In the case of static inverter oscillator, a large voltage gain exists when the input of each static inverter stage of the ring oscillator falls into the transition region of the voltage-transfer characteristic curve of the inverter, i.e, $V_{IL} \leq V_{in} \leq V_{IH}$, as shown in figure 3.29. To find the voltage gain expression in this region, a small-signal analysis of the inverter must be done (figure 3.30).

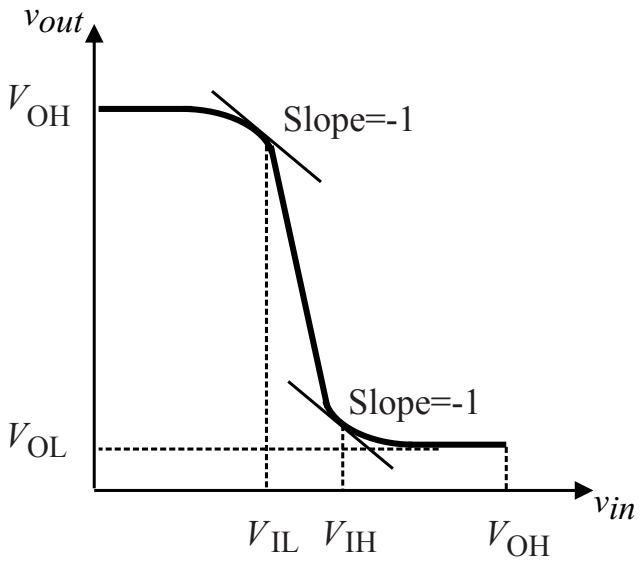

Figure 3.29: Voltage-transfer characteristic of the CMOS inverter [94].

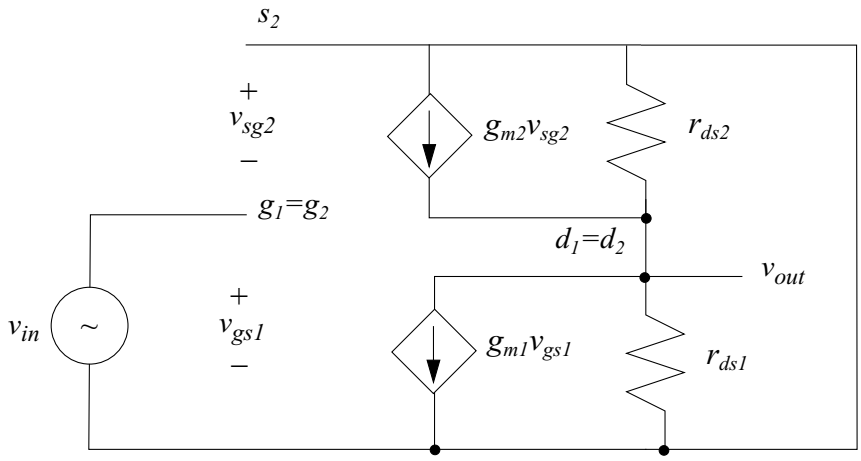

Figure 3.30: Small-signal model of the CMOS inverter [69].

Since $v_{in} = -v_{sg2}$, it is possible to simplify the small-signal circuit as follows:

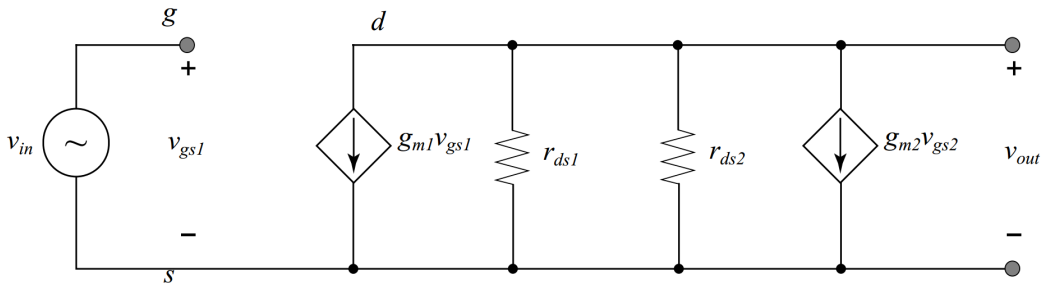

Figure 3.31: Simplified small-signal model of the CMOS inverter [69].

Therefore, the voltage gain is given by

$$A_v = \frac{v_{out}}{v_{in}} = -(g_{m1} + g_{m2})(r_{ds1} // r_{ds2}), \tag{3.59}$$

where g_{m1} and g_{m2} are the transconductances of NMOS and PMOS transistors, respectively, and r_{ds1} and r_{ds2} are the output resistors of NMOS and PMOS transistors, respectively. Considering $g_{ds} = 1/r_{ds}$ and the high-frequency small-signal model (figure 3.32), the voltage gain in this case is given by

$$A_v(s) = \frac{-g_{m1} - g_{m2} + sC_{gd1}}{g_{ds1} + g_{ds2} + s(C_{gd1} + C_{db1} + C_{gd2} + C_{db2} + C_L)}. \tag{3.60}$$

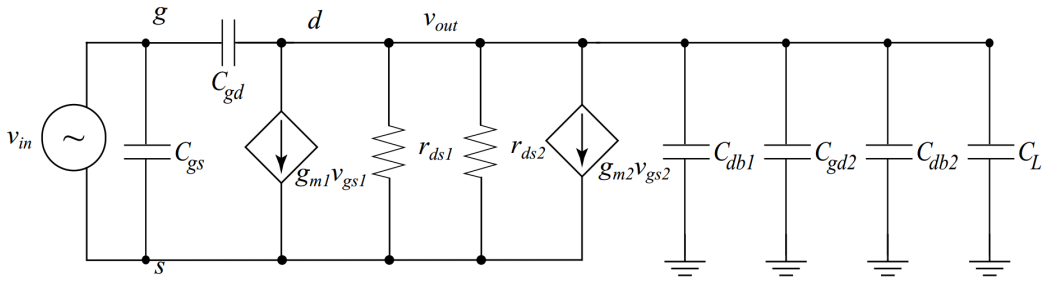

Figure 3.32: High-frequency small-signal model of the CMOS inverter.

The single-pole frequency is

$$\omega_{pole} = \frac{1}{RC} = \frac{G}{C} = \frac{g_{ds1} + g_{ds2}}{C_{gd1} + C_{db1} + C_{gd2} + C_{db2} + C_L}. \tag{3.61}$$

Finally, the inverter output impedance is given by

$$r_{out} = r_{ds2} // r_{ds1} = \frac{1}{g_{ds1} + g_{ds2}}. \tag{3.62}$$

Alternatively, the oscillation frequency can be determined by looking at the open-loop transfer of the RC oscillator, calculating the gain and phase characteristics, and seeing at which frequency the oscillation conditions are met. This linear analysis can accurately predict the actual oscillation frequency if the oscillator works in the linear region. For oscillators with active devices working in the moderate or strongly non-linear region, linear analysis will predict a higher oscillation frequency than the actual (large signal) oscillation frequency. Nevertheless, linear analysis is a convenient starting point and provides insight into the basic parameters determining the frequency [55].

Once the frequency of an oscillator is determined, the tuning possibilities can be determined by investigating the oscillator components that determine the oscillation frequency. For the ideal N-stage ring oscillator, capacitive and resistive tuning can be used to vary the oscillation frequency. Theoretically, variation of C and R are both completely equivalent tuning methods; the stage delay in the ring oscillator is varied. However, variation of C is less common compared to resistive tuning [86].

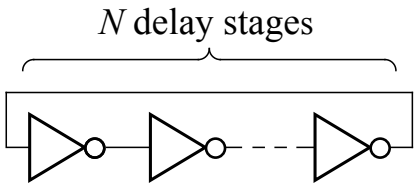

Figure 3.33: Ring oscillator with N delay stages [95].

The minimum number of stages for a ring oscillator is two or three if single-ended inverter gates are used. An example of a two-stage ring oscillator is the two-integrator oscillator. Like any even-stage ring oscillator, a two-stage ring oscillator provides quadrature signals. Unfortunately, quadrature outputs require a ring with an even number of stages, which has a stable, static operating point (also called "latch-up") and does not oscillate. For the single-ended ring oscillator, an odd number of stages is required to avoid latch-up (figure 3.33). On the other hand, the differential implementation can utilize an even number of stages by simply configuring one stage such that it does not invert, (e.g., swapping the feedback lines).

A behavioural model of a minimum of $N \geq 3$ stages ring oscillator is shown in figure 3.34. The resistor in the RC-network in each stage is noiseless in this ideal model and due to its presence, the phase shift in each stage will always be less than -90°. At least three

phases are provided by this ring oscillator, and in the case of perfect matching, the phase relation of the output signals is correct-by-construction. For an even number of stages, quadrature signals will be available [86].

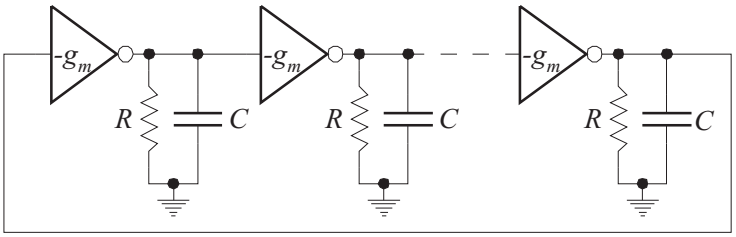

Figure 3.34: Linear model of an ideal N-stage ($N \geq 3$) ring oscillator [96].

Another commonly debated question concerns the optimum number of inverter stages in a ring oscillator to achieve the best jitter and phase-noise for a given f_0 and P. According to equation (3.63), for single-ended oscillators, the phase-noise and jitter in $1/f^2$ region are not strong functions of the number of stages for single-ended CMOS ring oscillators. However, if the symmetry criteria are not well satisfied, and/or the process has large $1/f$ noise, the equation (3.64) predicts that a larger N will reduce the jitter. In general, the choice of the number of stages must be made on the basis of several design criteria, such as $1/f$ noise effect, the desired maximum frequency of oscillation, and the influence of external noise sources, such as supply and substrate noise, that may no scale with N [97].

$$\mathcal{L}(\Delta\omega) \approx \frac{8}{3\eta}\frac{kT}{P}\frac{V_{DD}}{V_{char}}\frac{\omega_0^2}{\Delta\omega^2}, \tag{3.63}$$

where η is a proportionality constant (typically close to 1), k is the Boltzmann's constant, T is the absolute temperature, P is the total power dissipation and V_{char} is the characteristic voltage of the device.

$$f_{1/f^3} = f_{1/f}\frac{3}{2\eta N}\frac{(1-A)^2}{(1-A+A^2)}, \tag{3.64}$$

where A represents the asymmetry of the waveform and is defined as

$$A = \frac{f_r}{f_f}, \tag{3.65}$$

where f_r and f_f are the maximum slop during the rising and falling edge, respectively. As a special case, if the rise and fall times are symmetric, $A = 1$.

One significant advantage of the ring oscillator topology is that it needs only compact transistors and resistors and no bulky inductors as required for the analogue amplifier based approaches. However, due to the minimum number of three stages, the corresponding maximum oscillation frequency f_0 is bounded by

$$f_0 = \frac{1}{T} \leq \frac{1}{2Nt_P} = \frac{1}{6t_P}, \tag{3.66}$$

implying that the speed is determined by the parasitics of at least three transistors. Thus, the maximum oscillation frequency of ring oscillators is typically lower than the frequency achievable with the analogue amplifier based topologies [43].

At high frequencies, ring oscillators are preferred to relaxation oscillators in practice due to their simplicity, equal or better noise properties and their multiphase character. They are also very compact and easy to integrate, compared to on-chip LC oscillators. Furthermore, ring oscillators have wide tuning range and relatively power efficient, and it is easy to get multiphase output. However, as is often true in engineering, the simplest circuits bundle so many non-linear effects that they are quite difficult to analyse. Ring oscillators have poor frequency stability, low Q, poor phase-noise, its performance is vulnerable to PVT variations and extremely high frequencies are difficult to achieve [58].

Due to their integrated nature, ring oscillators have become an essential building block in many digital and communication systems. In many applications, it is necessary to control the frequency of the oscillator. An example of such a circuit is the VCO, whose oscillation frequency is a function (typically non-linear) of a control voltage [61]. Ring oscillators are used as a VCOs in applications such as clock recovery circuits for serial data communications [98, 99], disk-drive read channels [100], on-chip clock distribution [101], and integrated frequency synthesizers [102, 103].

Several ring oscillators structures have been proposed so far [19–30]. In this work, we present an architecture, which refines and extends a previously published model [22] to more accurately capture the process of quadrature outputs production.

Chapter 4

Multiphase Generators

Recently, a large amount of efforts has been dedicated in the analysis and design of multiphase generators. Considerable attention has currently been devoted to oscillator topologies generating multiphase signals in quadrature or multiphase signals in general. This interest is driven by several applications. For instance, the availability of I/Q LO references is essential for the implementation of fully integrated image-reject receivers [104]. In frequency synthesizers, fractional-N dividers [98] and frequency multipliers based on edge combination [105] require multiphase clock. Moreover, multiphase sampling clock can be used in high-speed samplers in order to reduce the maximum clock frequency. All these applications typically require accurate phase delay among the outputs. In fractional-N PLLs employing multiphase oscillators, phase errors between the phases raise the fractional spurs at the output [16]; in image-reject receivers, phase inaccuracy between the I/Q references limits the image rejection [106].

Multiphase clock generation has two important features: the frequency and the resolution. By resolution we mean the lowest time interval between two phases of the multiphase oscillator output. High frequencies with a high resolution are often required in multiphase clocks. The inverter ring oscillators are usually used to produce such a clock generator. The main drawback we face with inverter rings for implementing multiphase clocks is the exponential frequency drop with respect to the number of phases. In inverter ring oscillators, the frequency is only determined by the number of stages and the stage delay. Moreover, their resolution is limited to the stage delay and the only way to obtain more output phases is to add more stages, which decrease the maximum frequency and do not improve the resolution. Consequently, inverter ring oscillators cannot be used in applications requiring high resolution or high-speed multiphase clocks [107]. Furthermore, ring oscillators suffer from a strong phase-noise/power tradeoff.

After introducing the concept of producing multiphases through ring oscillators, the

closed-loop and open-loop approaches are presented, along with the SR architecture.

4.1 Closed-loop Approaches

All the conventional quadrature generating circuits reviewed have open-loop architectures, in which the errors are propagated to the output. In this section, the closed-loop architectures are presented, which have better quadrature, namely the two-integrator oscillator. This oscillator is very interesting because it can have either linear or non-linear behaviour. Finally, the coupled LC and RC oscillators will be analysed.

4.1.1 Two-Integrator Oscillator

Integrated wireless systems capable of operating with different frequency bands and different telecommunications standards are of great interest. In this subsection, the two-integrator oscillator is presented. Unlike the previous LC and relaxation oscillators, it generates quadrature outputs without the need of a coupling circuit, but as a result it only works with quadrature outputs.

Basically, the two-integrator oscillator consists in a two-stage ring oscillator [108] and like any even stage ($N = 2, 4$, etc.) ring oscillator, a two-stage ring oscillator provides quadrature signals. However, although the operating is similar to RC oscillators, the structure is different: the memory block (Schmitt-trigger) is substituted by another integrator.

At a high level model the two-integrator oscillator can be seen as two stages, each with an ideal integrator and an amplifier. These two stages are in cascade, and the output of the second stage is inverted and fed back to the first stage, as shown in figure 4.1. Depending on the amplifier, the oscillator has two types of behaviour: non-linear and quasi-linear [3, 86].

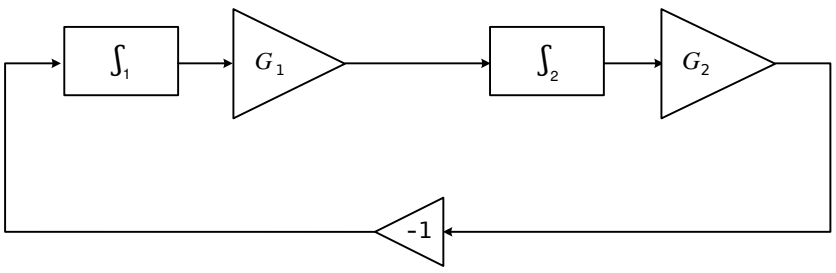

Figure 4.1: High level study of two-integrator oscillator [109].

Concerning the circuit level (figure 4.2), each integrator is implemented by a differential pair (transistors M) acting as a current buffer and a capacitor (C), whose impedance $1/j\omega C$ allows the integrator to produce a phase shift of $-90°$. The oscillator frequency is controlled by I_{tune}. The signal inversion made by the cross wired connection between the two stages produces an extra phase shift of $-180°$, which guarantees that the oscillator

only works with quadrature outputs. There is an additional differential pair (transistors M_r) with cross-coupled outputs used for loss compensation due to R to make the oscillation possible (a negative resistance is created in parallel with C) and amplitude stabilization due to the non-linearity (the current source I_{level} controls the amplitude).

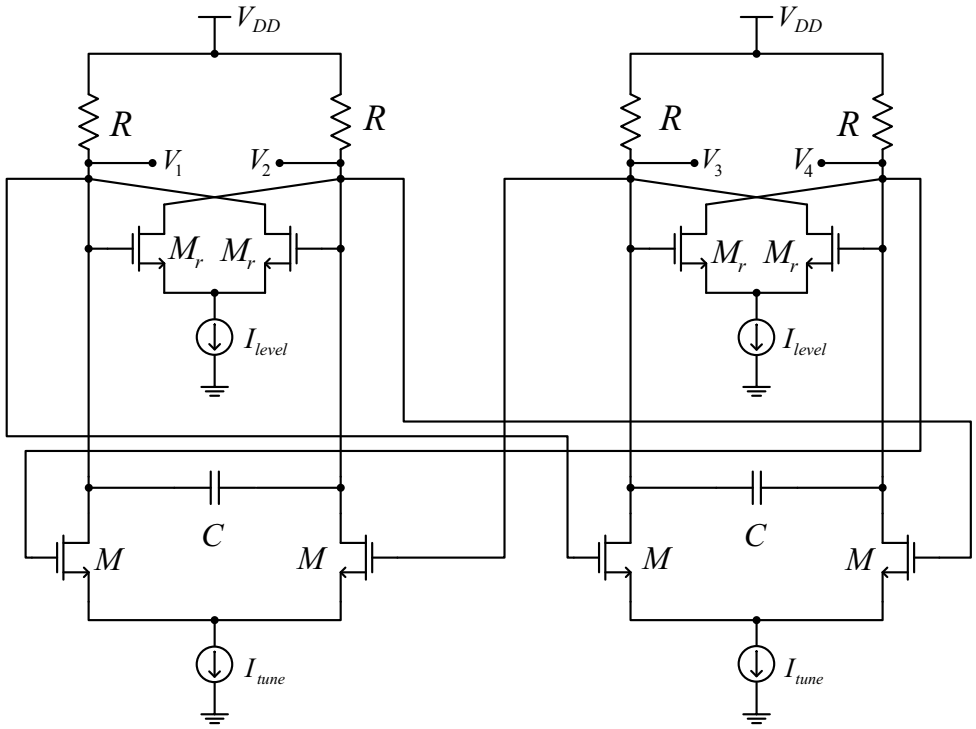

Figure 4.2: Two-integrator oscillator implementation [3].

For the oscillator to have a non-linear behaviour, the differential pair composed of transistors M_r must be in the saturation region. When increasing the current I_{level}, the transconductance $g_m = 2I_D/V_{DSsat}$ also increases, making the slope steeper and saturating the outputs more easily (equation (4.1)). In the saturation state, the output will form a square wave depending on the value of the input signal (if it is positive or negative). Then, the square wave is integrated, resulting in a triangular wave.

Transistors M that compose the differential pair determines in which way the current flows through the capacitor, depending on the voltage at its terminals. These transistors will change their operating regions, according to the signal at the gate. In theory both transistors work as a switch, when one is open the other is closed, so all the current flows through the latter one. In practice both transistors are conducting, as shown in figure 4.3, but there is more current in one of them.

Since the current is constantly changing, the capacitor is charging in different directions repeatedly thus producing the oscillation frequency, given by equation (4.2). The differential pair constituted by transistors M_r has the same behaviour delivering $-I_{lim}$ and I_{lim} with a 50% duty-cycle. In this case, the amplitude is $V_{out} = RI_{level}$.

$$I_{out}(V_{in}) = \begin{cases} I_{lim} = g_m V_{lim}, & \text{if } V_{in} \geq V_{lim}, \\ g_m V_{in}, & \text{if } -V_{lim} < V_{in} < V_{lim}, \\ -I_{lim} = -g_m V_{lim}, & \text{if } V_{in} \leq -V_{lim}. \end{cases} \tag{4.1}$$

$$\omega_0 = \frac{I_{tune}}{2CV_{out}}. \tag{4.2}$$

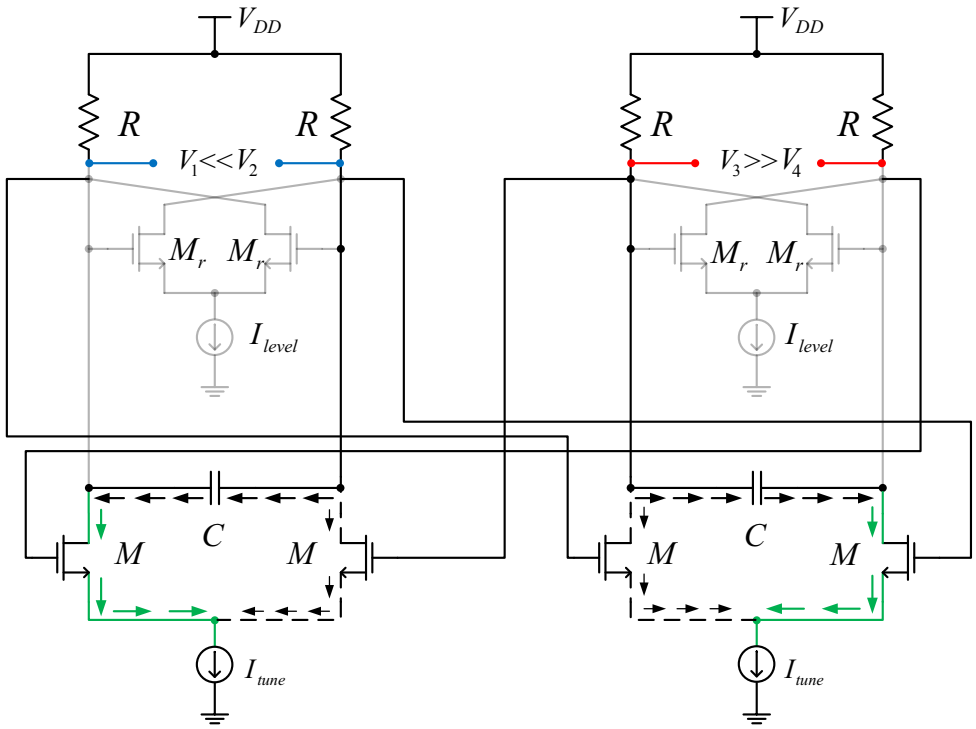

Figure 4.3: Current flow in the two-integrator oscillator circuit [109].

When the current I_{level} reaches a certain value, the differential pair independently of the input will always saturate. This behaviour is close to the one of a Schmitt-trigger, so it is possible to introduce a saturated amplifier in the high level model and thus obtaining the structure shown in figure 4.4. The outputs of each integrator determine the input signal of the other integrator. The waveforms are square at the amplifier outut and triangular at the integrator output, as well as in relaxation oscillators.

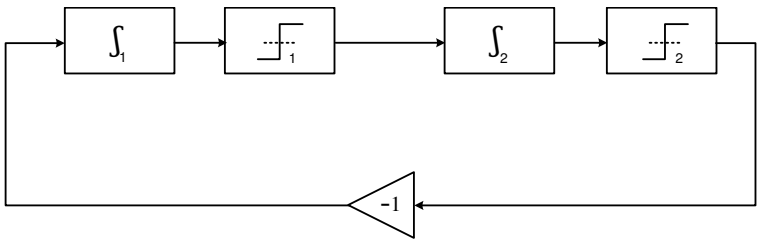

Figure 4.4: Two-integrator oscillator high level model with non-linear behaviour [109].

To obtain a perfect square wave at the amplifier an infinite number of harmonics is mandatory. This generation of unwanted harmonics causes a degradation of phase-noise. Thus, to achieve the best performance, the two-integrator oscillator should have a quasi-linear behaviour. In this behaviour both the differential pairs operate in the linear region, producing sinusoidal outputs. The amplifier can be replaced in the high level model by a soft-limiter, as shown in figure 4.5.

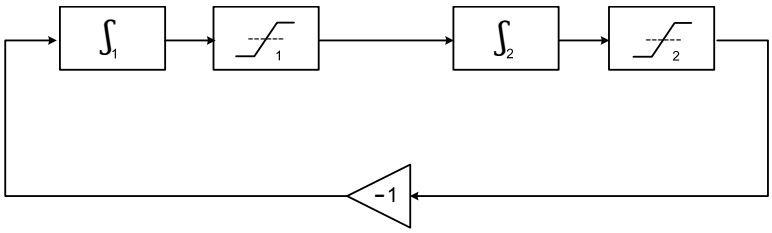

Figure 4.5: Two-integrator oscillator high level model with linear behaviour [109].

The resistor is used to obtain a current on the circuit and limit the amplitude signal. However, it also introduces noise and creates an unwanted real part on the poles. To compensate that, a differential pair of transistors M_r is employed [3, 86] from figure 4.3. Through the small-signal model (figure 4.6), it is possible to collect the equivalent impedance of the differential pair given by equation (4.3). The cross wire cancels the real part of the poles, to theoretically obtain only the imaginary part. To compensate the real part, we can increase the current I_{level} to consequently augment the g_m. If a over-compensation occurs, the oscillator will have a non-linear behaviour. On the other hand, if a balanced compensation takes place, the differential pair avoids saturation effects.

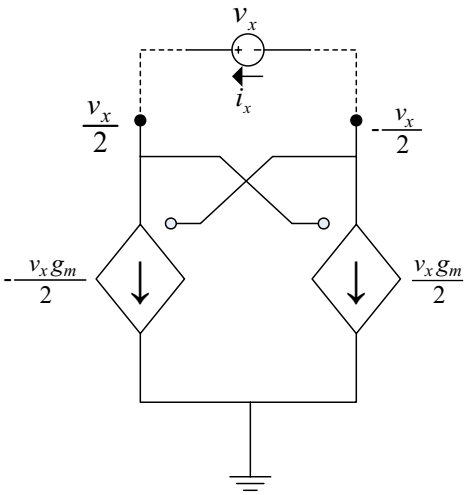

Figure 4.6: Small-signal model of differential pair composed of transistors M_r [109].

$$r_x = \frac{v_x}{i_{ix}} = -\frac{2}{g_m}. \tag{4.3}$$

Figure 4.7 illustrates a transconductance change due to a continuous variation of Transistor T_r v_{gs}. This transconductance is equivalent to a slope, since $g_m = \partial i_d / \partial v_{gs}$. As mentioned before, the role of g_m is to cancel the real part caused by the resistors, since their value is always changing. Therefore, the poles will always be between the stable and unstable region. This is one of the noise source that contributes to the oscillator phase-noise, since in practice it is impossible to obtain a constant frequency at the output.

A practical approach of the two-integrator oscillator in linear operation is represented in figure 4.8. The resistors R_{eq} model not only all the resistors in one stage, but also possible losses in the circuit.

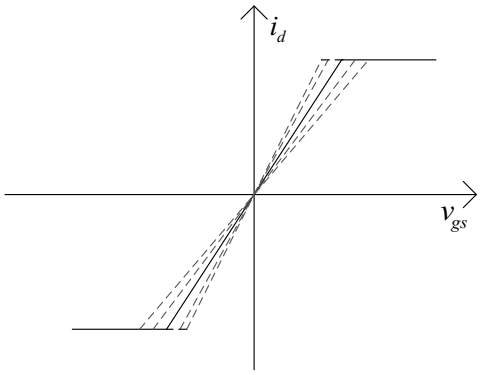

Figure 4.7: Small-signal analysis of transconductance [109].

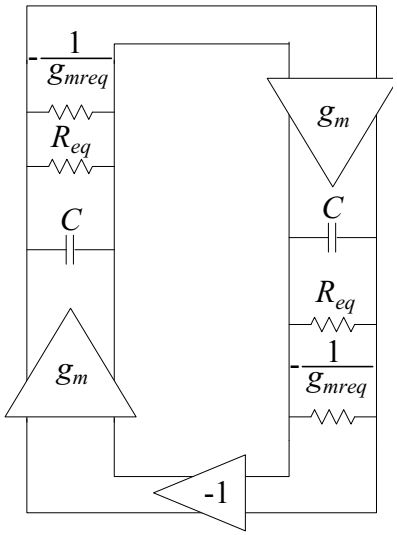

Figure 4.8: Two-integrator oscillator linear model [109].

From the model in figure 4.8, it is possible to obtain the oscillator frequency using the loop gain of the oscillator. Assuming that the real part is cancelled ($R = 1/g_{mreq}$), the loop gain is given by:

$$|H(j\omega)| = \frac{g_m^2}{\omega^2 C^2}. \tag{4.4}$$

Since the gain has to be one for oscillation and to satisfy the amplitude condition $|H(j\omega)| = 1$ of Barkhausen criterion, the oscillation frequency is:

$$\omega_0 = \frac{g_m}{C}. \tag{4.5}$$

This is the reason why the two-integrator oscillator has a wide tuning range, since with a simple manipulation of the I_{tune} current value, the transconductance g_m can be changed, allowing a sweep over a large range of frequencies.

Considering the current in the differential pair is equal to the source current, the oscillator amplitude is given by $V_{out} = RI_{level}$. When working with a non-linear behaviour, we will have the maximum output amplitude possible. In the linear behaviour, the amplitude is limited by the slope of the amplifier. To achieve a optimum point, the current I_{level} must be close to saturation [86]. However, this brings some disadvantages: the power consumption increases, the FoM worsens and there is a risk of entering into the non-linear region.

4.1.2 Coupled Oscillators

In this subsection two different types of coupled oscillators are introduced. First, the coupled LC oscillator, followed by the coupled RC oscillator. The idea is simple: obtain quadrature outputs by connecting two symmetrical oscillators. In the case of the coupled LC oscillator [13, 110], this can be done introducing two differential pairs acting as soft-limiters [3]. Figure 4.9 shows the coupled version of the LC oscillator circuit. A cross coupled connection to give a $-180°$ phase shift is also needed to fulfil the negative feedback loop phase condition of the Barkhausen stability criterion.

While the gates of transistors M_c connect to the outputs of a singular LC, the drains connect to the outputs of the other oscillator. When one pair senses the voltage variation at the gate, it varies the current injected in the other oscillator. The oscillation frequency will be synchronized in both oscillators and the outputs will have a phase shift of 90°.

Although single LC oscillator presents low phase-noise, when coupled they demonstrate some phase-noise degradation [111–113]. Moreover, there is the difficulty of implementing them with a low voltage supply and the large area the circuit occupies. To give a perspective of how significant is the circuit area, a RC oscillator can occupy the same layout area as an inductor.

LC oscillators need a strong coupling to synchronize both outputs with a phase difference of 90°. To increase the coupling, the gates size of coupling transistors should be increased. However, the parasitics on those transistors will increase and consequently, the oscillation frequency decreases, degrading the phase-noise. This drawback enables coupled LC oscillators to have a similar phase-noise performance to that of coupled RC oscillators [3].

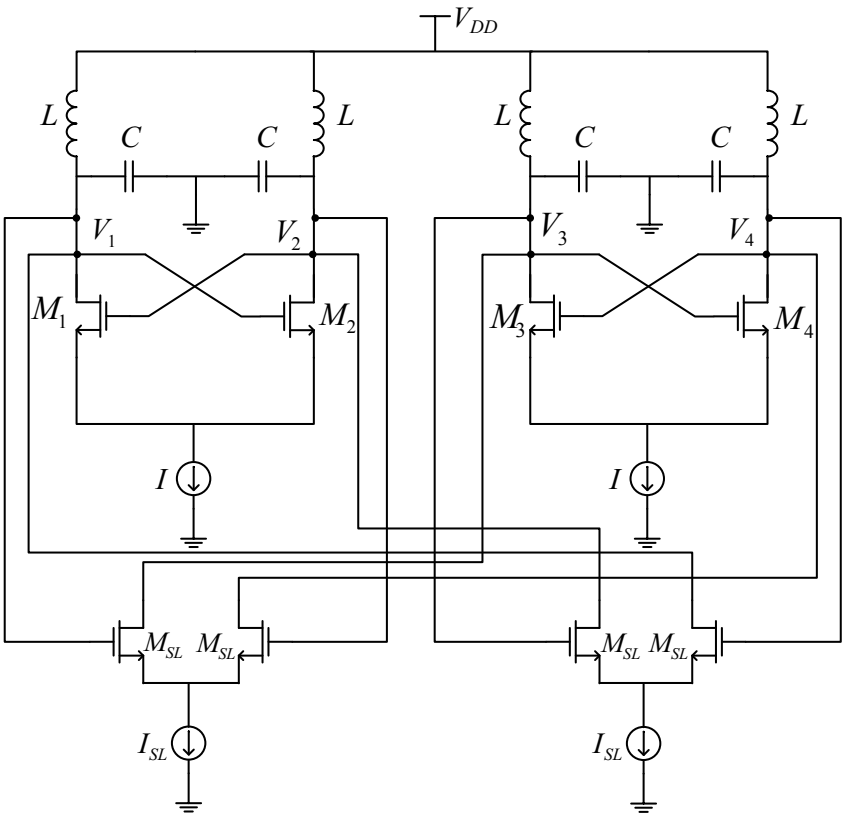

Figure 4.9: Coupled LC oscillator circuit [109].

In the coupled RC oscillator, the connection is made using a soft-limiter at the output of the integrator and increasing its gain a square wave signal is obtained at the output. Unlike the Schmitt-trigger that only changes when a threshold is reached, the soft-limiter saturates when the triangular wave goes above zero. Therefore, we obtain a square wave with a 90° difference from Schmitt-trigger output.

Figure 4.10 shows a high level block diagram of the coupled RC oscillator. The output of the soft-limiter is used to synchronize the other RC oscillator. Its square signal is added to the triangular output signal of the other integrator and then the resulting signal is processed by the Schmitt-trigger, creating a feedback structure. This way both outputs have always a 90° phase shift and the same frequency.

The resulting wave of the signal addition assumes an important part on the overall noise. This signal has a steeper slope and defines each oscillator state transitions, which means the switching times are less sensitive to noise [3]. As previously mentioned, the higher the gain of the soft-limiter, the more square the output becomes and thus, increases the slope, making the oscillator less sensitive to noise.

At circuit level the soft-limiter is implemented by a differential pair, as shown in figure 4.11. This coupling method has the same features as the one presented on LC oscillators, but in this case the gates are connected to the capacitor terminals. When the voltage at the gate varies, the current on the other oscillator also changes. To demonstrate how it influences the output amplitude, an oscillator will be analysed when transistor M_1 is off

and M_2 is on. Although in single LC oscillator the transistor M_1 has a voltage equal to V_{DD} and the transistor M_2 branch has a voltage of $V_{DD} - 4RI$, in the coupled version the outputs will be (with the current i_{sl1} lower than i_{sl2}):

$$\begin{cases} v_1 = V_{DD} - Ri_{sl1} \\ v_2 = V_{DD} - 2RI - Ri_{sl2}. \end{cases} \tag{4.6}$$

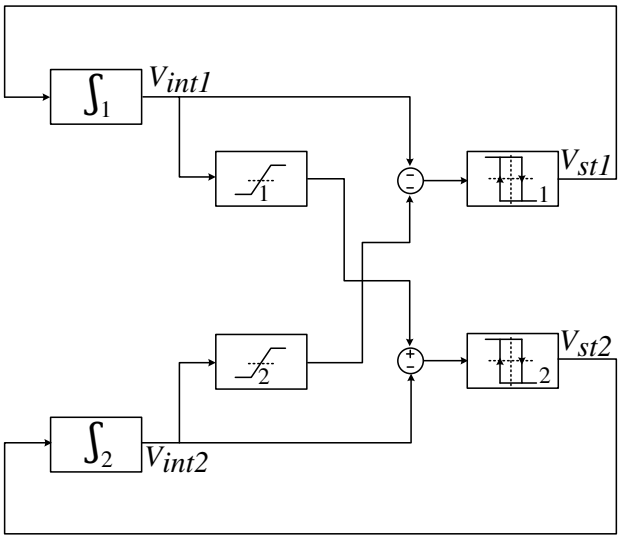

Figure 4.10: Coupled RC oscillator high level model [109].

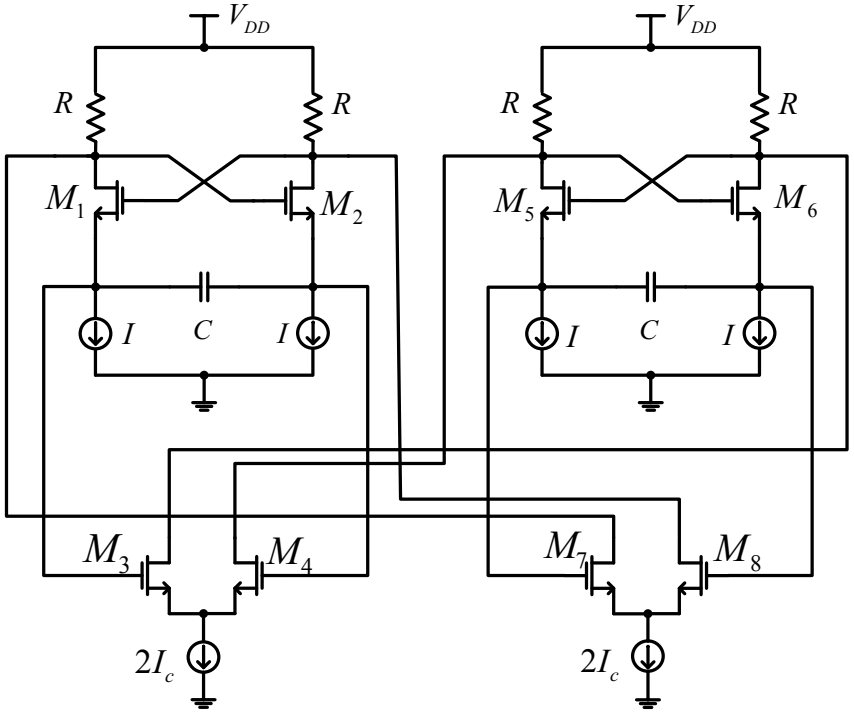

Figure 4.11: Coupled RC oscillator circuit [109].

When coupling two symmetrical oscillators, one of the new differential pairs must be cross coupled to guarantee the synchronization of both oscillators and, if in the quasi-linear behaviour, maintain the Barkhausen conditions. Coupling will also introduce a few changes in the single RC oscillator performance. It brings new noise sources due to the new active elements, but the advantages it provides are more significant. The phase-noise improves, notwithstanding the frequency reduction.

The decrease of the voltage supply combines with the need of using low power circuits. From equation (4.6), it is possible to deduce how troublesome is to implement coupled oscillators, since introducing the new differential pairs demand the best of care concerning the voltage supply. New coupling techniques have been developed to solve this problem: instead of using a current and a differential pair, the coupling is made using capacitors, which reduces not only the power consumption, but also some noise sources.

In recent years, coupled RC oscillators have become a subject of many studies due to their good performance, low area and quadrature outputs. Coupled LC oscillators have the same performance as RC ones but occupy a larger area. The goal is to attain a single chip transceiver and this oscillator type combined with CMOS technology allows that. Many RC architectures have been developed and some are being restudied in order to reduce power consumption, improve phase-noise and increase tuning frequency.

4.2 Open-loop Approaches

In modern transceivers, accurate quadrature is required for modulation, demodulation and for image rejection. The common methods of generating In-phase (I) and Quadrature (Q) signals with a phase difference of 90° employ open-loop structures [1] which are reviewed in this section. This requirement raises an important matter on mismatches because the error rate in detecting the baseband signal increases [1, 3]. The oscillator assumes a critical role on quadrature outputs, because of the required low quadrature error.

The best known approach RC-CR network is shown, followed by other techniques that can be found in the literature, such as the frequency division, among others. Finally, the SR concept used throughout this work is introduced.

4.2.1 RC All-pass Filter

The RC all-pass phase shifter consists of a pair of RC networks and differential amplifiers with component values chosen to yield a transfer function that has constant magnitude for all frequencies, i.e., an all-pass response. Figure 4.12 is an example of an RC all-pass phase shifter. The relative RC time constants between the two networks are designed in such a manner that the phase difference between their output signals is 90° at the center frequency [114]. Second and higher order RC networks (figure 4.12) are usually employed to achieve this 90° phase shift over a broader range of frequencies. An

interesting property of these networks is that most of the design parameters depend on ratios between component values as opposed to their absolute values [115]. This makes them less sensitive to process variations, albeit the centre frequency still shifts with any change in component value. While the broadband performance of RC all-pass filters is a definite plus, they are particularly large and complicated to design [114].

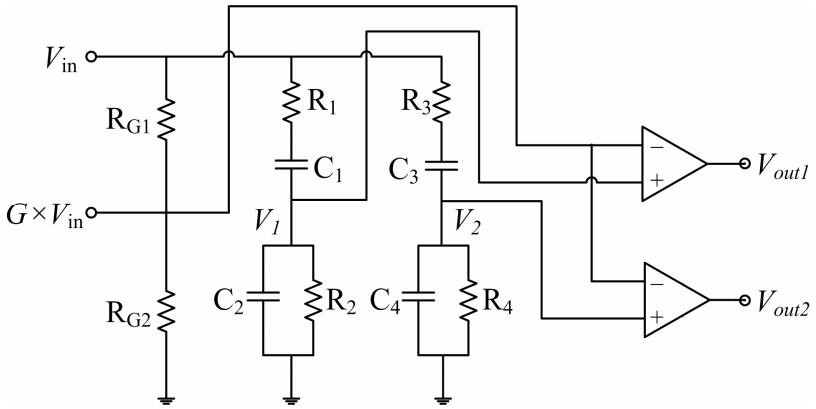

Figure 4.12: RC all-pass phase shifter diagram [116].

RC-CR Network

The RC-CR network [117–119] is the simplest technique in which the input signal is shifted by +45° in the CR branch and by −45° in the RC branch (figure 4.13. The two outputs are in quadrature (90°) for all frequencies which is desirable, but the amplitudes are not constant, since they are only equal at the cutoff/pole frequency $\omega = \omega_{pole} = 1/RC$ [2]. Therefore, the phase difference between the two outputs is not sensitive to process variations but the amplitude match certainly is. The design procedure is simply to set the pole frequency to the carrier frequency. However, if the value of either R or C changes (with temperature and with process), so does the frequency at which there are quadrature signals with equal amplitude [1]. Much effort has been made to minimize this problem by using limiter stages based on differential pairs (e.g., differential amplifiers) [1] or using variable gain amplifiers [2] to achieve an amplitude match over a wide frequency range, but several stages need to be cascaded which consumes a lot of DC power, diminishing the main advantage of RC-CR networks [117, 120].

The phase shift of V_{out1} is zero at DC and by increasing the frequency decreases asymptotically to −90°. The phase shift of V_{out2} is +90° at DC and decreases with the frequency towards 0°. The phase shift of each branch changes with the frequency, but the phase difference of two outputs is always 90°. This approach provides a good quadrature relationship, but the amplitude of the outputs changes significantly with the frequency. The I and Q branches have, respectively, a low-pass and a high-pass characteristic. On the other hand, at the pole frequency there is a 3 dB attenuation, which is a significant loss. Moreover, this network generates thermal noise, which cannot be ignored.

In the circuit of figure 4.13, the mismatch of resistors and capacitors originates a deviation θ from the 90° phase difference. Assuming relative mismatches α for the resistance and β for the capacitances, we can express θ in the neighbourhood of ω as:

$$\theta = \frac{\pi}{2} - \{\arctan(\omega RC[1+\alpha][1+\beta]) - \arctan(\omega RC)\}. \tag{4.7}$$

Using the trigonometric relationship

$$\arctan(A) - \arctan(B) = \frac{A-B}{1+AB}, \tag{4.8}$$

we obtain

$$\theta = \frac{\pi}{2} - \arctan\left(\frac{\omega RC[1+\alpha][1+\beta] - \omega RC}{1+[\omega RC]^2[1+\alpha][1+\beta]}\right). \tag{4.9}$$

If $\alpha \ll 1$ and $\beta \ll 1$ (small mismatches), and taking into account $\omega \approx 1/RC$:

$$\theta \approx \frac{\pi}{2} - \arctan\left(\frac{\alpha+\beta}{2}\right) \tag{4.10}$$

$$\theta \approx \frac{\pi}{2} - \frac{\alpha+\beta}{2}. \tag{4.11}$$

For typical values $\alpha = \beta = 10\%$, equation (4.11) gives 5.73° worst-case quadrature error.

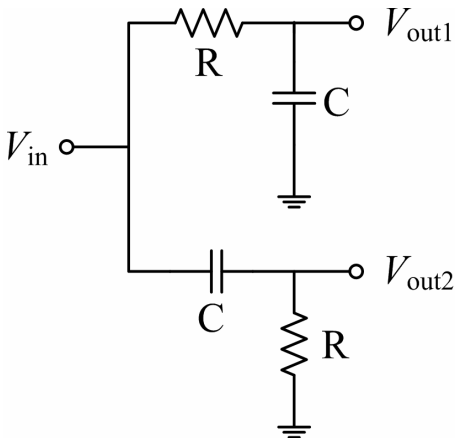

Figure 4.13: RC-CR circuit as a quadrature generator [116].

As depicted in figure 4.13, the circuit is entirely passive and therefore consumes zero DC power, a definite plus in portable low-power applications. Nevertheless careful circuit and device layout techniques, such as common-centroid layout for example, are available to reduce component mismatch and tolerances for satisfactory model-to-hardware correlation. Furthermore, an additional design cycle may be used to adjust the performance if deemed feasible.

4.2.2 RC Polyphase Filter

An RC-CR network with two or more stages is known as a polyphase filter [121–125]. A single RC-CR stage provides (without mismatches) an amplitude error below 0.2 dB over a 10% bandwidth. A properly designed 2-stage RC-CR network can give the same gain error with a higher bandwidth. We can use more stages in order to cover the required bandwidth. However, a polyphase filter has significant attenuation and high noise [2].

The RC polyphase filter is a symmetric RC network with inputs and outputs connected in relative phases, as shown in figure 4.14 [122]. Each RC (CR) branch leads to a $-45°(+45°)$ phase shift at the cut-off frequency of $1/RC$. Therefore, the differential inputs are shifted $\pm 45°$ towards each other at this cut-off frequency and combines at the outputs (with 0 dB gain) to form the differential quadrature signals.

The RC polyphase network can be viewed as low-pass (RC) and high-pass (CR) filter sections connected together at the outputs, with their low and high pass frequency responses combining together for an overall all-pass response. Thus, in contrast to the RC-CR network, a 90º phase difference only appears at the cut-off frequency $1/RC$ while the amplitudes are matched irrespective of frequency. A result of this is that the phase difference is now sensitive to process variations and the frequency at which quadrature signals exist will shift if the value of R or C changes. Most efforts to counter this problem have focused on cascading several stagger-tuned stages of the polyphase filter whose cut-off frequencies are logarithmically spaced out for a wideband equiripple response [122–125]. Doing so gives rise to a large footprint and possibly substantial signal loss as each stage loads the previous one. Careful circuit and device layout techniques, such as common-centroid layout for example, may nonetheless by used to reduce component mismatch and tolerances for satisfactory predictability. Furthermore, an additional design cycle may be employed to adjust the performance if possible.

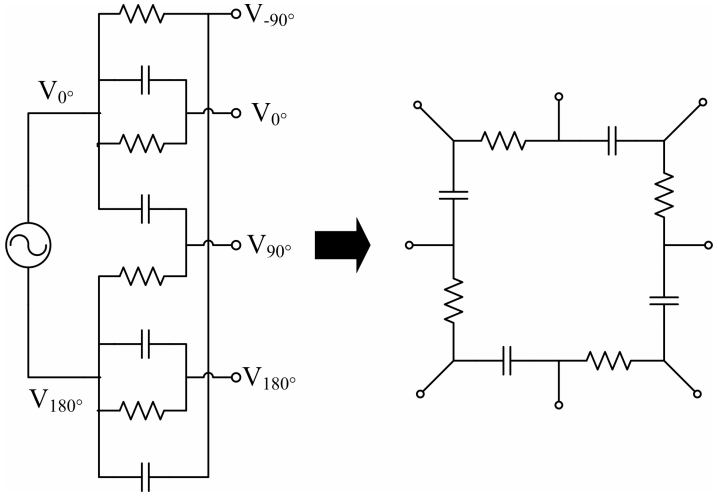

Figure 4.14: RC polyphase network as a symmetric RC network [116].

4.2.3 Frequency Divide-by-two Circuits

Frequency Divide-by-Two Circuitss (DTCs) [126–128] is a simple technique to generate quadrature carriers in which two latches are cascaded in a negative feedback loop to form a master-slave Flip-Flop (FF) with each stage exhibiting a 90° phase shift for the required loop total of 180°, as shown in figure 4.15. Thus, the master-slave FF is used to divide by two the frequency of a signal with double of the desired frequency. If the inputs are precisely complementary and the two latches match perfectly (with V_{in} having 50% duty-cycle), then the outputs of the latches are in quadrature [1].

In practice, device mismatches result in phase imbalances and additional imbalances occur as the input differential signals are not exactly 180° out of phase especially at high frequencies. Despite efforts for overcoming these problems to generate an accurate 90° phase shift, the latches usually consume a significant amount of DC power. In addition, generating an oscillator signal at twice the frequency could entail more DC power or might be impractical altogether if the desired LO frequency is very high, for example 60 GHz [1].

The use of a carrier with twice the desired frequency has two main disadvantages: there is an increase in the power consumption and the maximum achievable frequency is reduced. Mismatches in the signal paths through the latches and deviations of the input duty-cycle from 50% contribute to the phase error. To reduce the quadrature error, two dividers can be used, but this requires an input signal with four times the required frequency [2].

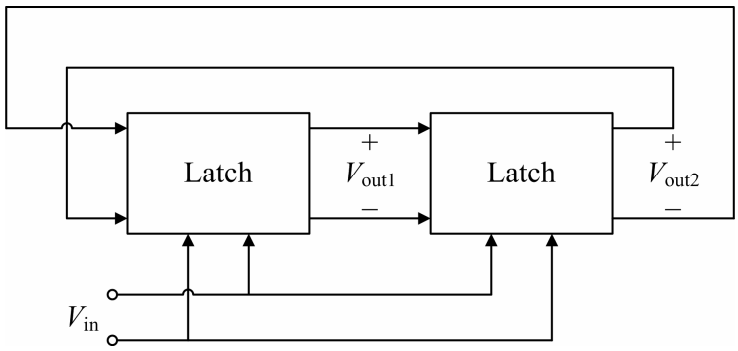

Figure 4.15: Quadrature generation using a divide-by-two circuit [116].

4.2.4 Shift Register

Normally based on logic circuits, one of the major challenges in digital electronics is manipulate data providing a means to store and access binary data. Shift Registers (SRs) are a type of sequential logic circuit (figure 4.16) that can be used to store or transfer data in the form of binary numbers [129]. Unlike combinational logic, this sequential logic is not only affected by present inputs, but also by prior history. SR produces a discrete delay of a digital signal or waveform. A waveform is synchronized to a clock, a repeating

square wave, is delayed by N discrete clock times, where N is the number of shift register stages [130].

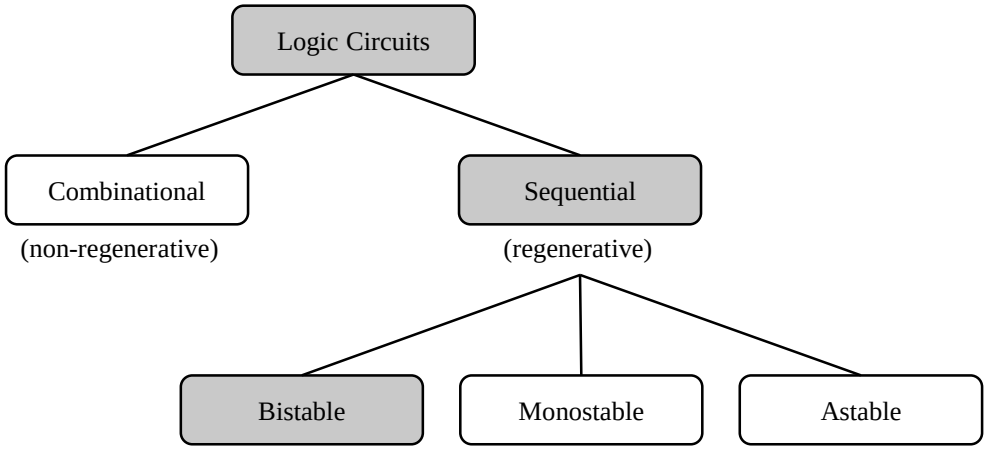

Figure 4.16: Classification of logic circuits based on their temporal behaviour [66].

Bistable circuits have, as their name implies, two stable states or operating modes and will remain in either state unless perturbed to the opposite state. On the other hand, monostable circuits have only one stable operating point, and even if they are temporarily perturbed to the opposite state, they will return to the single stable state. Finally, astable circuits have no stable operating point which the circuit can preserve for a certain time period, and oscillate between several states. The ring oscillator examined in subsection 3.3.2 is a typical example of an astable regenerative circuit.

Among these three main groups of regenerative circuit types, the bistable circuits are by far the most widely used and the most important class. All basic latch and FF circuits, registers and memory elements used in digital systems fall into this category.

In the following, SR consists of several FFs connected in a chain so that the output from one FF becomes the input of the next FF. Most of the registers possess no characteristic internal sequence of states. Every FF is driven by a common clock, and all are set or reset simultaneously.

The fundamental single-bit memory element of digital electronics is called a FF. It is a storage circuit that changes states on the rising and falling edge of a clock signal. Most FFs in CMOS IC design are based on cross-coupled inverters. It differs from a latch in that it has a control signal (clock) input and stores the input state and outputs the stored state only in response to the clock signal (synchronous, unlike latch which output only changes as soon as the input changes [asynchronous]). If a FF accepts its inputs at low to high (high to low) transition, it is a positive-edge (negative-edge) triggered. FFs are often said to be edge-triggered because it is the edge of the clock signal that triggers the FF. When used in clock-driven computer circuits, edge-triggering is an important characteristic since it helps circuit designers maintain better control over the timing in circuits that contain hundreds or perhaps thousands of FFs. By connecting several FFs

together, they may store data that can represent the state of a sequencer, the value of a counter, an American Standard Code for Information Interchange (ASCII) character in a computer's memory or any other piece of information. A set of N FFs can store any binary number in the range 0 to $(2^N - 1)$ or $-(2^{N-1})$ to $+(2^{N-1} - 1)$, depending on whether we choose to represent the number as unsigned or signed.

An important timing value for a FF is the propagation delay t_P (see subsection 3.1.1 for more details), which is the time a FF takes to change its output after the clock edge. The time for a low to high transition t_{PLH} is sometimes different from the time for a low to hgh transition t_{PHL}. Therefore, when cascading FFs which share the same clock (as in a SR), it is relevant to ensure that the t_P of a preceding FF is longer than the hold time (t_H) of the following FF, so data present at the input of the succeeding FF is properly "shifted in" following the active edge of the clock. This relationship between t_P and t_H is normally guaranteed if FFs are physically identical. Furthermore, for correct operation, it is easy to verify that the clock period has to be greater than the sum $t_{SU} + t_H$, where t_{SU} is called the setup time.

Also known as a data or delay FF, D-FF, which truth table is shown in table 4.1, is not only one of the most commonly used FFs, but also the simplest storage device as it takes the state of D input at the moment of a positive edge at the clock (or negative if the clock is active low) and delays it by one clock cycle and subsequent changes on the D input will be ignored until the next clock event. Figure 4.17 shows the timing diagram of a positive edge-triggered D-FF. The unknown state of Q before the first rising clock edge is indicated by the pair of lines at both low and high levels.

Table 4.1: D-type flip-flop truth table.

Clk	**D**	**Q**
0	0	Q
0	1	Q
1	0	0
1	1	1

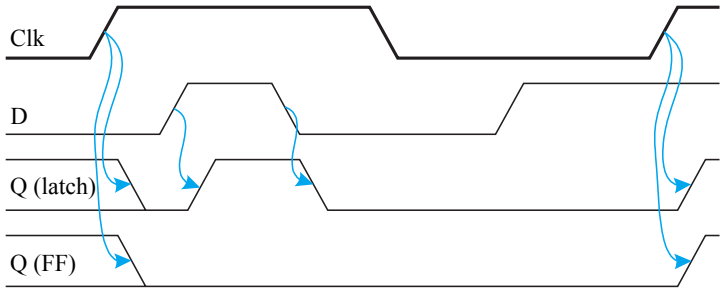

Figure 4.17: Latch and flip-flop timing diagrams [131].

The number of clock pulses required to shift all bits of a register completely in or completely out of the register is equal to the number of FFs in the register. SRs allow such data transfers and are capable of storing a N-bit word due to the N number of FFs they incorporate. The stages in a SR are delay stages, typically D-FF or type JK FFs. Generally, SRs operate in one of four different modes (figure 4.18) with the basic movement of data through a SR being:

1. **Serial-Input to Parallel-Output (SIPO)** – the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.

2. **Serial-Input to Serial-Output (SISO)** – the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.

3. **Parallel-Input to Serial-Output (PISO)** – the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.

4. **Parallel-Input to Parallel-Output (PIPO)** – the parallel data is loaded simultaneously into the register and transferred together to their respective outputs by the same clock pulse.

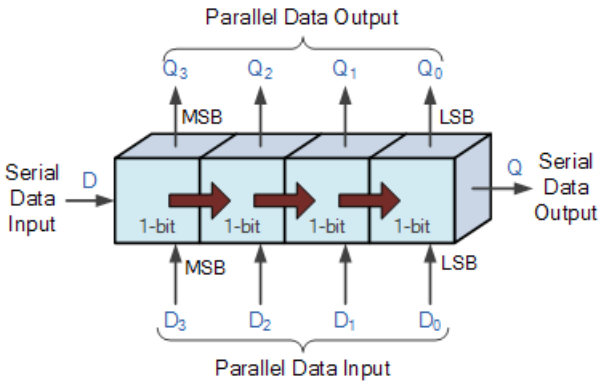

Figure 4.18: Shift register data movement [132].

Serial-In means the device reads in the data bit by bit, and Parallel-Out means all the output bits are presented simultaneously. Moreover, the directional movement of the data through a SR can be either to the left, (left shifting) to the right, (right shifting) left-in but right-out, (rotation) or both left and right shifting within the same register thereby making it bidirectional. In this work, the SISO SR is used and therefore this approach deserves to be substantiated in detail.

This type of SR acts as a temporary storage device or it can act as a time delay device for the data, with the amount of time delay being controlled by the number of stages in the register (4, 8, 16, etc.) or by varying the application of the clock pulses. The SISO SR is designed such that at the negative edge of each clock cycle, the data present at the

input is loaded into the first FF. At each subsequent negative edge of the clock, the data in the predecessor FF will be loaded into the successor FF. This continues until the clock stops. This means the data would be shifted out from the last FF and lost, unless stored.

For instance, let us consider the entry of five bits 11010 into a 5-bit register shown in figure 4.19, beginning with the Least Significant Bit (LSB). Assuming that the register is initially clear, the 0 is put onto the data input line, making $D = 0$ for FF_0. When the first clock pulse is applied, FF_0 is reset, thus storing the 0. Table 4.2 shows the entry of the five bits, which are indicated in bold.

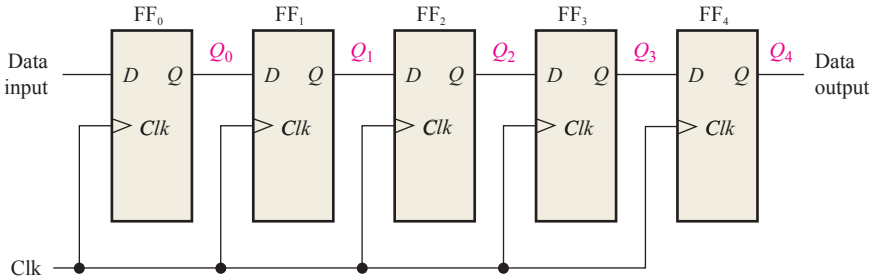

Figure 4.19: 5-bit SISO shift register [133].

Table 4.2: Shifting a 5-bit code into a SISO shift register.

Clk	FF_0 (Q_0)	FF_1 (Q_1)	FF_2 (Q_2)	FF_3 (Q_3)	FF_4 (Q_4)
Initial	0	0	0	0	0
1	**0**	0	0	0	0
2	**1**	**0**	0	0	0
3	**0**	**1**	**0**	0	0
4	**1**	**0**	**1**	**0**	0
5	**1**	**1**	**0**	**1**	**0**

Next the second bit, which is a 1, is applied to the data input, making $D = 1$ for FF_0 and $D = 0$ for FF_1 because the D input of FF_1 is connected to the Q_0 output. When the second clock pulse occurs, the 1 on the data input is shifted into FF_0, causing FF_0 to set, and the 0 that was in FF_0 is shifted into FF_1. The third bit, a 0, is now put onto the data-input line, and a clock pulse is applied. The 0 is entered into FF_0, the 1 stored in FF_0 is shifted into FF_1, and the 0 stored in FF_1 is shifted into FF_2. Then, the fourth bit, a 1, is put onto the data-in, and a clock pulse is applied. That bit enters into FF_0, the 0 stored in FF_0 is shifted into FF_1, the 1 stored in FF_1 is shifted into FF_2, and the 0 stored in FF_2 is shifted into FF_3. The last bit, a 1, is now applied to the data input, and a clock pulse is applied. This time the 1 is entered into FF_0, the 1 stored in FF_0 is shifted into FF_1, the 0 stored in FF_1 is shifted into FF_2, the 1 stored in FF_2 is shifted into FF_3, and the 0 stored in FF_3 is shifted into FF_4. This completes the serial entry of the five bits into the SR, where they can be stored for any length of time as long as the FFs have DC power.

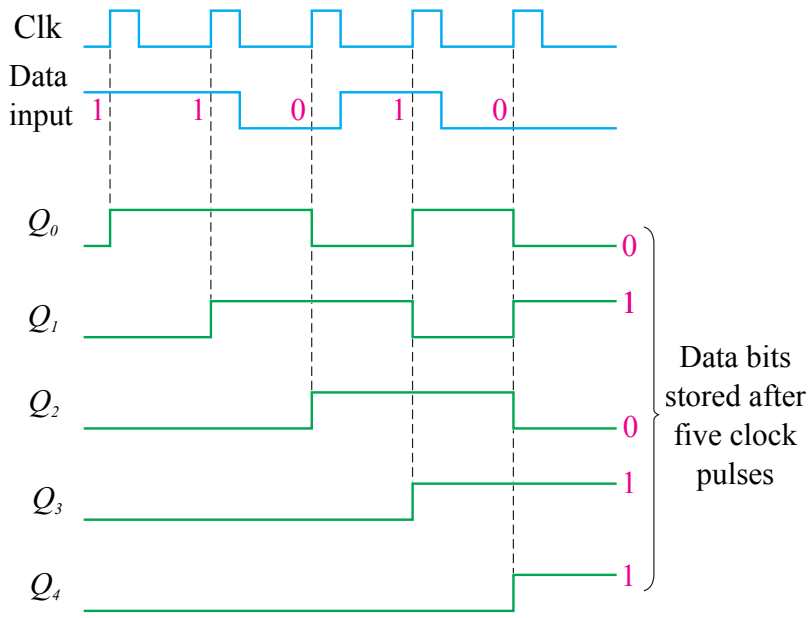

Figure 4.20: Data bits stored after five clock pulses [133].

To get the data out of the register, the bits must be shifted out serially to the Q_4 output, as table 4.3 illustrates. After Clk_5 in the data-entry operating just described, the LSB, 0, appears on the Q_4 output. When clock pulse Clk_6 is applied, the second bit appears on he Q_4 output. Clock pulse Clk_7 shifts the third bit to the output, Clk_8 shifts the penultimate bit to the output, and Clk_9 shifts the last bit to the output. While the original five bits are being shifted out, more bits can be shifted in. All zeros are shown being shifted in, after Clk_{10}. Note that in table 4.3 data bits are indicated in bold.

Table 4.3: Shifting a 5-bit code out of a SISO shift register.

Clk	**FF$_0$ (Q_0)**	**FF$_1$ (Q_1)**	**FF$_2$ (Q_2)**	**FF$_3$ (Q_3)**	**FF$_4$ (Q_4)**
Initial	**1**	**1**	**0**	**1**	**0**
6	0	**1**	**1**	**0**	**1**
7	0	0	**1**	**1**	**0**
8	0	0	0	**1**	**1**
9	0	0	0	0	**1**
10	0	0	0	0	0

With the widespread use of CMOS circuit techniques in digital integrated circuit design, a large selection of CMOS-based sequential circuits have also gained popularity and prominence, especially in Very-Large-Scale Integration (VLSI) design. Although their design is quite straightforward, direct CMOS implementations of conventional circuits such as latches or FFs tend to require a large number of transistors [66], as we will see in chapter 5. However, FFs are used in event detect, data synchronizer, frequency

divider, SR, asynchronous ripple counters, synchronous parallel counters and in state machines applications (e.g., D-FF are used in finite state machines). For instance, a Field Programmable Gate Array (FPGA) is an IC which contains edge-triggered FFs.

SRs can also be found in many applications. Here is a list of a few [134]:

1. **Digital delay lines** – if a single-bit data stream is fed serially into a SR and then read out serially from the output of one of the register's FFs, then the effect is that of delaying the data stream. For a clock period T, then if the data is read from the Nth stage of the register, the data is delayed by $(N-1)T$.

2. **Sequence generator** – if a binary pattern is fed into a SR it can then be output serially to produce a known binary sequence. Moreover, if the output is also fed back into the input (to form a SISO connected to itself), the same binary sequence can be generated indefinitely. When a SISO SR is connected to itself, this is usually referred to as a re-entrant SR, dynamic SR, ring buffer or circulating memory. Variations on this type of circuit are used for data encryption, error checking and for holding data during DSP.

3. **Ring counters** – SRs can be used to produce a type of simple counter whose advantage (in addition to the simplicity) is that they can operate at very high speeds since there is no need for any external control or decoding circuitry (necessary for most counters). Such counters are formed by simply using a re-entrant SR (the serial output is fed back to the serial input) which is (usually) loaded with a solitary high value. The register is then clocked and the output, taken from any one of the FFs, simply goes high every time the single stored bit arrives at that FF (i.e., after N clock cycles giving what is known as a mod-N counter). A second type of counter can be produced by connecting the $\overline{\text{Q}}$ output from the last FF of a SISO back to the input and then loading a single 1. This is usually referred to as one of the following: twisted ring, switched tail, Johnson or Moebius[1] counter. A mod-$2N$ twisted ring counter requires N FFs.

Despite the many applications where SRs can be found, our aim is to build a multiphase single-frequency clock generator with low phase mismatch using the SR concept. Multiphase clocking is an important technique that can be used to reduce device count in Large-Scale Integration (LSI) and VLSI circuits [76]. Typical applications are the microprocessors and Double Data Rate (DDR) and Quadrature Data Rate (QDR) memories to achieve a higher operation frequency than that of the main internal clock. To achieve high-speed interfaces, a multiphase clock generator is required to obtain a low power consumption, a fast-locking time, wide frequency range and clock synchronization [135]. Currently, several multiphase clock generators have been proposed for high-speed interfaces [136–141]. In high-speed serial link applications [142–145], multiphase clocks are used to process data streams at a bit rate higher than the internal clock frequencies.

[1] A Moebius strip is a loop made from a strip of paper with a single twist in, meaning it only has one side.

The multiphase clock previously mentioned is generated by the SISO SR which chain shifts the clock phase to produce N-phase clocks. In this work, the 3 and 4-phase single frequency clock generator are presented in chapter 5, the latter with 50% and 25% duty-cycles. UCLA and Broadcom® have recently presented in [34] a similar SR used in an inductorless wideband receiver. This increasing interest in SRs has led to extensive researches and investigations, as can be seen in [33–37, 40, 41].

CHAPTER 5

Analysis of Multiphase Generators

Recently, there has been a proliferation of modern transceiver architectures to achieve full integration and low cost, covering the widest range possible of the spectrum, from tens of MHz up to several GHz. This has lead to the development of quadrature oscillators, since quadrature errors affect strongly the overall performance of RF front-ends. Therefore, it is very important to have a reliable and efficient wave generator with stable frequency and phase, and accurate quadrature outputs. With this in mind, two approaches are introduced. First, the multiphase ring oscillator, described by its highly integration, low cost and small size, but its performance degrades as the frequency of operation increases, offering also poor frequency stability and phase-noise. Then, the contemporary SR approach, which although occupies a larger area when compared to the ring oscillator topology, its phase-noise and phase error are significantly lower. Therefore, the SR use has become very popular and motivated much of the research effort around this brand new concept, in order to achieve the best possible results.

This is the main chapter of this thesis, and it is devoted to present these two contrasting approaches.

5.1 Multiphase Ring Oscillators

5.1.1 3-stage Ring Oscillator

Without loss of generality, consider the oscillator of figure 5.2 which shows the 3-stage ring oscillator structure employing an odd number of static single-ended inverters (figure 5.1) acting as delay cells. The inverters are connected to form a closed-loop ring. It is important to note that this oscillator may operate either in the linear or non-linear regimes. Assuming its linear regime, each inverter in the loop needs a finite propagation delay τ_{inv} to charge or discharge the parasitic capacitances (where the capacitance C_{gs}

assumes to be the dominating capacitance) connected to the output node [146]. Since $\tau_{inv} = RC$, where R is the resistance of the output node and C expresses the transistors parasitic capacitances connected to the same node, the challenge is to settle the value of the last parameter given its dependence on W and L values of the transistors and the region in which they are operating.

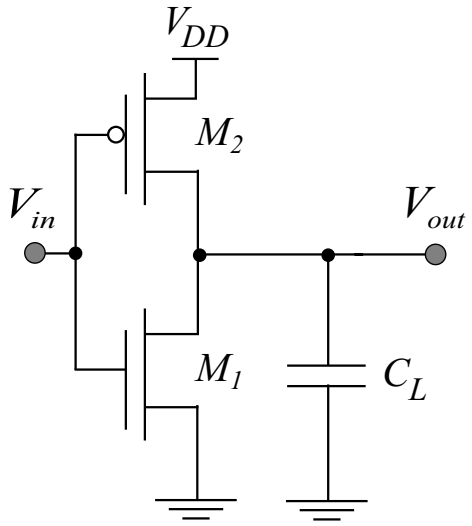

Figure 5.1: CMOS inverter circuit.

Considering the complementary inverter structure in saturation mode, the current that flows through the NMOS transistor is the same that passes through the PMOS transistor ($I_{D1} = I_{D2}$), where

$$I_D = \frac{K_{1,2}}{2}\frac{W}{L}\left(V_{GS} - V_{T1,T2}\right)^2 = \frac{K_{1,2}}{2}\frac{W}{L}V_{DSsat}^2. \tag{5.1}$$

Thus, a technique widely used in this type of oscillators to vary the oscillation frequency is varying the current that passes into each inverter block. Current consumption in static CMOS inverters is mainly due to charging and discharging the node capacitances. The lower the current, the longer the transition time.

The oscillation frequency of the ring oscillator depends on the propagation delay τ_{inv} per stage and the number of stages used [147]. To achieve a self-sustained oscillation, the ring must provide a phase shift of 2π and have at least a unity voltage gain. This means that for the 3-stage ring oscillator, the oscillating signal must travel through each of the three ($N = 3$) delay stages twice to have a total delay of 6τ and arrive at the initial state. Accordingly, the oscillation frequency can be expressed as

$$f_0 = \frac{1}{2\tau_{chain}} = \frac{1}{2N\tau_{inv}} = \frac{1}{6\tau_{inv}}, \tag{5.2}$$

which relies on the number of stages N, the time constant of the inverters chain τ_{chain} and the delay time of the inverters τ_{inv} which depends on circuit parameters. Therefore, adding pairs of inverters to the ring oscillator increases the total delay and thereby decreases the oscillation frequency.

Although not intended, the most basic CMOS ring oscillator (N=3) provides sinusoidal outputs. It follows by symmetry that if all the stages are identical, then as the sine wave traverses each stage of the ring its amplitude remains unchanged, and it experiences a phase lag of 120°. The only way to overcome this handicap is to increase the number of stages for $N > 3$ in order to get square waveforms at the output.

Unfortunately, quadrature outputs require a ring with an even number of stages, which has a stable, static operating point (also called latch-up) and does not oscillate. Therefore, there are two methods to solve this problem. The first is true differential signalling by using CML delay cells with a tail current source. The second is to add feedforward inverters between nodes with opposite-phase signals (see subsection 5.1.2).

The CML tail current source offers common mode rejection and forces the differential signals of an N-stage differential oscillator (that has $2N$ stages if seen as single-ended system) into opposite phase. Latch-up is prevented. For a large frequency range, delay interpolating techniques [100, 148] or advanced load circuits and self-biased techniques [149] are necessary. However, CML delay cells draw a constant bias current and energy is wasted during the time when no transition takes place. Moreover, signal swing is limited and phase-noise performance normalised to power consumption is suboptimal.

Ring oscillators with static, single-ended CMOS inverters offer large signal swings. Current consumption is lower because it is limited to the switching time interval. Therefore, the theoretical limit of the phase-noise FoM is better for full-swing single-ended ring oscillators than for CMOS ring oscillators [25].

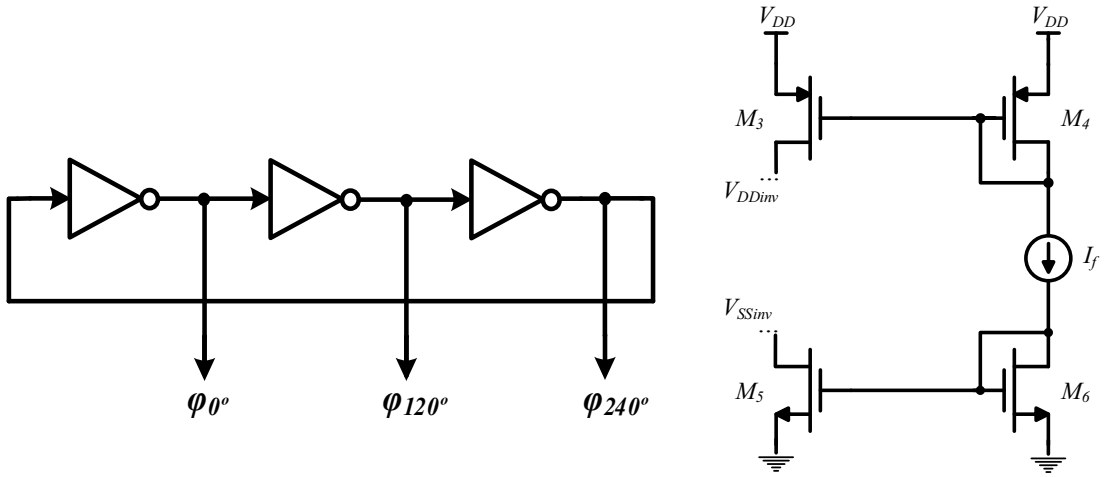

Figure 5.2: 3-stage single-ended ring oscillator.

Regarding the design of the CMOS inverter, assuming $K_1 = \mu_1 C_{ox} \cong 500\ \mu\text{AV}^{-2}$ and $K_2 = \mu_2 C_{ox} \cong 150\ \mu\text{AV}^{-2}$, the ratio K_R is defined as

$$K_R = \frac{K_1}{K_2} = \frac{\mu_1 C_{ox} (W/L)_1}{\mu_2 C_{ox} (W/L)_2} = \frac{\mu_1 (W/L)_1}{\mu_2 (W/L)_2}, \tag{5.3}$$

assuming that the gate oxide thickness t_{ox}, and hence, the gate oxide capacitance C_{ox} have

the same value for both NMOS and PMOS transistors. Therefore,

$$\frac{(W/L)_1}{(W/L)_2} = \frac{\mu_2}{\mu_1} \approx \frac{150}{500}. \tag{5.4}$$

Hence,

$$(W/L)_2 \approx 3\,(W/L)_1\,. \tag{5.5}$$

Considering the transistors length constant, we finally conclude that

$$W_2 \approx 3W_1. \tag{5.6}$$

It should be note that the numerical values used in equation (5.4) for electron and hole mobilities are typical values, and that exact μ_1 and μ_2 values will vary with surface doping concentration of the substrate and the tub. Regardless, the PMOS transistor has low mobility and in order to have a symmetric inverter as much as possible, the equation (5.5) should be satisfied. The main idea is that the rise and fall times of the output voltage signals are the same and therefore this can only be achieved by sizing the PMOS three times the NMOS size. As a matter of fact, the sizing of CMOS transistors clearly affects the rise and fall times and it is important to note that asymmetrical rise and fall times would lead to duty-cycle variations which consequently leads to jitter issues.

Considering the criterion set out from equation (5.5), the table 5.1 shows the chosen transistors dimensions. Notice that the adopted sizing will also be considered not only in the following ring oscillator, but also in the SR approaches for a fair comparison in chapter 6. Finally, it was estimated a benchmark relative to rise and fall times of the output signals of 100 ps, representing a value much less than 1 ns which corresponds to the period of a 1 GHz frequency, i.e., the frequency in which the oscillator could operate with a safety margin since 600 and 900 MHz frequencies were considered. Moreover, a load capacitance C_L in of 100 fF was also considered in order to have more current, without compromising the frequency since $f = 1/RC$. Considering it is possible to approximate the inverter transient response to an RC model, its response is clearly dominated by this output capacitance of the gate. Note that the propagation delay t_P (defined in subsection 3.1.1) is determined by the time it takes to charge/discharge the load capacitance C_L, so it is important to look upon this capacitance.

Table 5.1: Ring oscillator parameters.

Transistor	***W*** **(**μ**m)**	***L*** **(**μ**m)**	***NF***	***M***
M_1	5	0.12	2	1
M_2	5	0.12	6	1
M_3	6	0.24	10	1
M_4	6	0.24	10	1
M_5	5	0.24	4	1
M_6	5	0.24	4	1

5.1.2 4-stage Ring Oscillator

To avoid latch-up in an even-numbered static CMOS inverter ring, additional circuitry has to be added. In [99], a method to increase the operating frequency of ring oscillators with an odd number of delay cells by creating feedforward paths is presented. In figure 5.3, the concept of adding feedforward paths to a ring with an even number of stages is shown. Based on [22], several modifications had to be made in order to obtain quadrature and square waveforms at the outputs. A circuit acting as a current source was added to ensure enough current to guarantee the proper functioning of the oscillator and its inverters. Considering the purpose of controlling the current flow through the inverter and the 1.2 V voltage supply, the average value ideally continues to be 0.6 V, which means the output wave should be centered in that voltage level. The transistors that compose this current source should be designed with large size to ensure current passes through. Therefore, at least two times the technology minimum was considered ($L = 2L_{min} = 240$ nm).

In addition to the output capacitances of 10 fF, a buffer composed of four CMOS inverters was incorporated to each output to buffer the LO signal before providing it to the mixer, producing a limiting function since waveforms similar to a sinusoid were obtained without it. According to the requirements for the signal waveform, the signals were either directly applied to the loads or drivers were connected between the oscillator and the load circuits. This buffer converts the signal of the core to a square wave signal, where the duty-cycle requirement for this signal is usually 50%. The inverters which set this buffer contain exactly the same dimensions as the inverters composing the oscillator itself. L_{min} should be used to increase W/L.

In addition to the cascaded combination of the four main delay stages, feedforward inverters are placed between nodes with opposite phases so a pair of them can act as a negative-G_m cell or as a regenerative circuit [20], forcing the two signals involved to opposite levels. The feedforward inverters take over the job that is done by the tail current source in a CML oscillator. There is a threshold value for the strength of the feedforward inverters relative to the strength of the main inverters to sustain a stable oscillation.

In contrast to a ring with an odd number of inverters, now two transitions are travelling through the ring. Therefore, the oscillation frequency is given by

$$f_0 = \frac{1}{\tau_{chain}} = \frac{1}{N\tau_{inv}} = \frac{1}{4\tau_{inv}}. \tag{5.7}$$

As there is a rising and a falling transition at any time, the single-ended quadrature ring oscillator draws a nearly constant supply current and minimises switching noise on the supply lines.

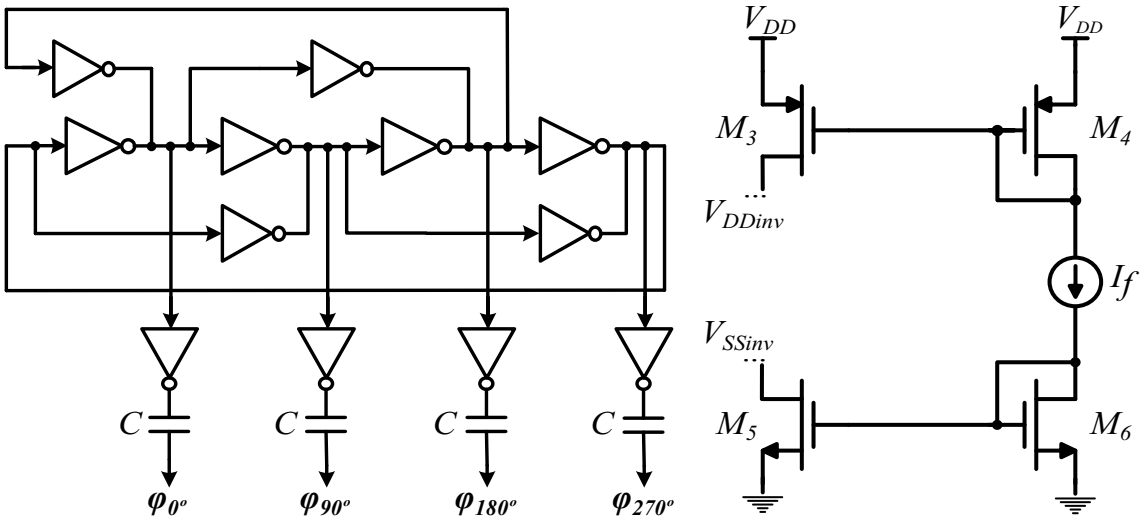

Figure 5.3: Quadrature 4-stage ring oscillator concept employing feedforward paths.

5.2 Multiphase Shift Registers

5.2.1 3-phase Shift Register

SRs are a very meaningful part of digital logic as they allow data transfers within the register from one FF to another for each clock pulse. The most basic structure is the SISO SR using D-FFs driven by a common clock.

One of the most interesting things to do with Boolean gates is to create memory with them. The FF shown in figure 5.4(B) consists in four NAND gates along with a single inverter where every schematic was designed with CMOS transistors. As is known, all circuits are possible to be implemented with NAND or NOR gates. However, the structure that required fewer logic gates was the one composed of NAND gates. Furthermore, NAND is a better gate for design because at the transistor level the mobility of electrons is normally three times that of holes compared to NOR and thus the NAND is a faster gate. Additionally, the gate-leakage in NAND structures is much lower. These are enough reasons for preferring the architecture of the single D-FF shown in figure 5.4(B). Figure 5.4(A) shows the 2-input NAND gate used in D-FF structure.

Considering figure 5.4(A), PMOS transistors M_7 and M_8 are in parallel, but there are states in which only one of them conducts and therefore, they should have the same sizing of inverter's PMOS present in figure 5.4(B). As for the NMOS transistors (M_9 and M_{10}), the worst case occurs when $A = B = 0$, leading them to operate in series and consequently, it is necessary to duplicate the W/L value (assuming $N = 2$ since there are two inputs: D and clock) concerning inverter's W/L ratio [62]. The dimensions of the transistors in a NAND logic gate with N inputs are then:

$$(W/L)_{nNAND} = N\,(W/L)_{nINV} \tag{5.8}$$

$$(W/L)_{pNAND} = (W/L)_{pINV} = \frac{\mu_n}{\mu_p}(W/L)_{nINV}. \tag{5.9}$$

Hence, the transistors dimensions of a NAND gate with two inputs ($N = 2$) assuming $\mu_n/\mu_p = 3$ are given by:

$$(W/L)_{nNAND} = 2(W/L)_{nINV} \tag{5.10}$$

$$(W/L)_{pNAND} = (W/L)_{pINV} \cong 3(W/L)_{nINV}. \tag{5.11}$$

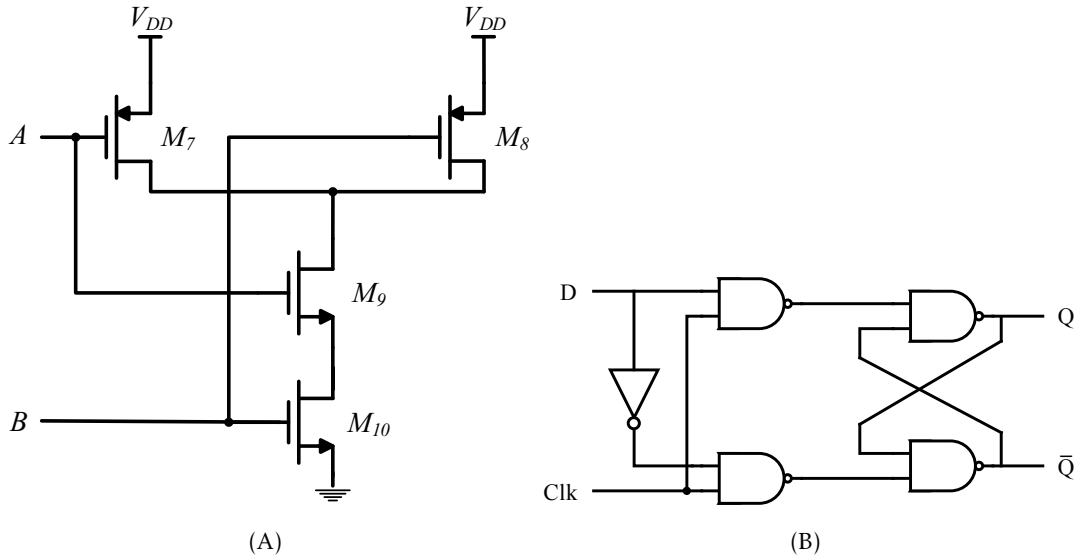

Figure 5.4: (A) 2-input NAND gate using MOSFET transistors (B) Single D flip-flop structure.

Table 5.2 shows the transistors dimensions used in SR approaches. For a proper operation of the D-FF, its D input signal must be stable before the clock starts to switch. When the clock switches, the logic value on the D node is transferred to the Q output. This means the timing of the FF output is determined by the clock, so the D input signal only acts as an "enabler" of a transition. Therefore, to D-FF works properly, it must be designed with two master/slave connected as latches as shown in figure 5.5, where the first latch is only an "enabler" [38].

Table 5.2: Shift register parameters (CMOS 130 nm).

Transistor	***W* (μm)**	***L* (μm)**	***NF***	***M***
M_1	5	0.12	2	1
M_2	5	0.12	6	1
M_7	5	0.12	6	1
M_8	5	0.12	6	1
M_9	5	0.12	2	1
M_{10}	5	0.12	2	1

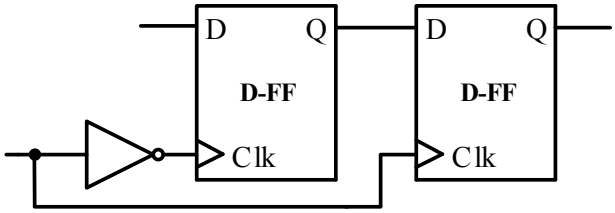

Figure 5.5: Dual D flip-flop structure.

Figure 5.6 shows the designed multiphase generator employing SR which shifts the clock phase to produce 3-phase clocks (0°, 120° and 240°). The last dual D-FF consists in a dummy block placed at proper node to ensure all logic blocks drive the same load capacitance [37]. Note that either D and clock inputs are generated from ideal sources.

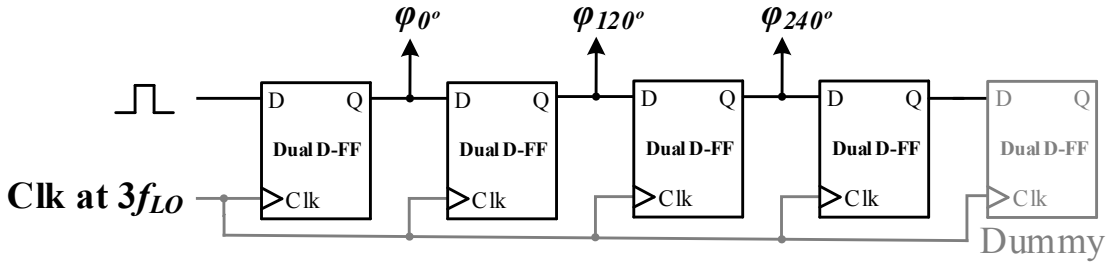

Figure 5.6: 3-phase shift register block diagram.

The main contribution of the presented circuit is not the introduction of a new SR and dual D-FF architectures, but rather a new implementation of their combination.

5.2.2 4-phase Shift Register with 50% Duty-cycle

In this case, four quadrature outputs are generated from the 4-phase SR concept. Figure 5.7 shows the designed LO generator which shifts the clock phase to generate 4-phase clocks (0°, 90°, 180° and 270°) with 50% duty-cycle. Compared to the previous case, an extra dual D-FF was added to the chain to ensure another output and consequently another phase.

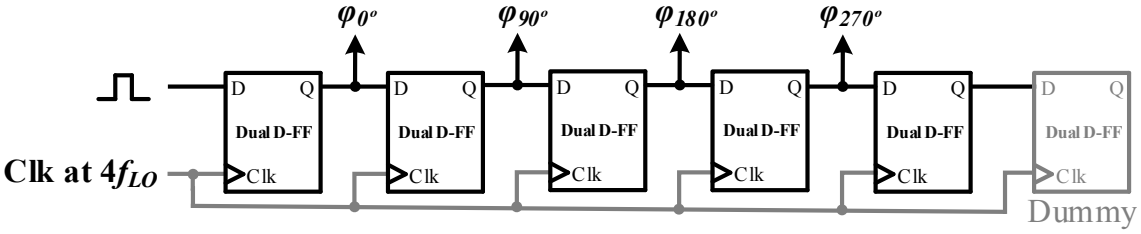

Figure 5.7: Quadrature 4-phase shift register with 50% duty-cycle.

This quadrature 4-phase SR structure can perfectly be coupled for instance, to the RF front-end receiver presented in appendix C or any RF front-end receivers. This architecture is able to replace any type of generator, providing better results with regard to

phase-noise and phase error.

5.2.3 4-phase Shift Register with 25% Duty-cycle

The SR architecture able to generate 4-phase clocks (0°, 90°, 180° and 270°) with 1/4 duty-cycle is shown in figure 5.9. To produce the desired duty-cycle, it was necessary to resort to Boolean algebra in order to understand how the circuit had to behave. Table 5.3 shows that a combination of NAND and AND logic gates is enough to achieve the 25% duty-cycle. These logic gates have exactly the same size as the logic gates previously designed, which are shown in table 5.4. Once again, the last dual D-FF ensures all logic blocks drive the same load capacitance and either D and clock inputs are generated from ideal sources.

Table 5.3: Truth table of the quadrature 4-phase shift register with 25% duty-cycle.

Boolean logic \ **Period**	$T/4$	$T/2$	$3T/4$	T
$Q_1 \barwedge Q_2$	1	0	1	1
$Q_1 \cdot (Q_1 \barwedge Q_2)$	1	0	0	0
$Q_2 \barwedge Q_3$	1	1	0	1
$Q_2 \cdot (Q_2 \barwedge Q_3)$	0	1	0	0
$Q_3 \barwedge Q_4$	1	1	1	0
$Q_3 \cdot (Q_3 \barwedge Q_4)$	0	0	1	0
$Q_4 \barwedge Q_1$	0	1	1	1
$Q_4 \cdot (Q_4 \barwedge Q_1)$	0	0	0	1

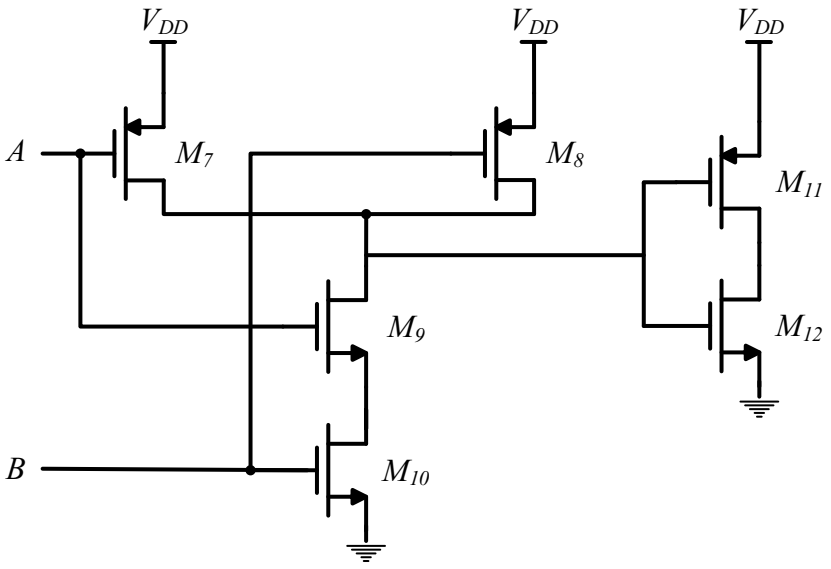

Figure 5.8: 2-input AND gate using MOSFET transistors.

Table 5.4: Parameters of the quadrature 4-phase shift register with 25% duty-cycle (CMOS 130 nm).

Transistor	W (μm)	L (μm)	NF	M
M_1	5	0.12	2	1
M_2	5	0.12	6	1
M_7	5	0.12	6	1
M_8	5	0.12	6	1
M_9	5	0.12	2	1
M_{10}	5	0.12	2	1
M_{11}	5	0.12	6	1
M_{12}	5	0.12	2	1

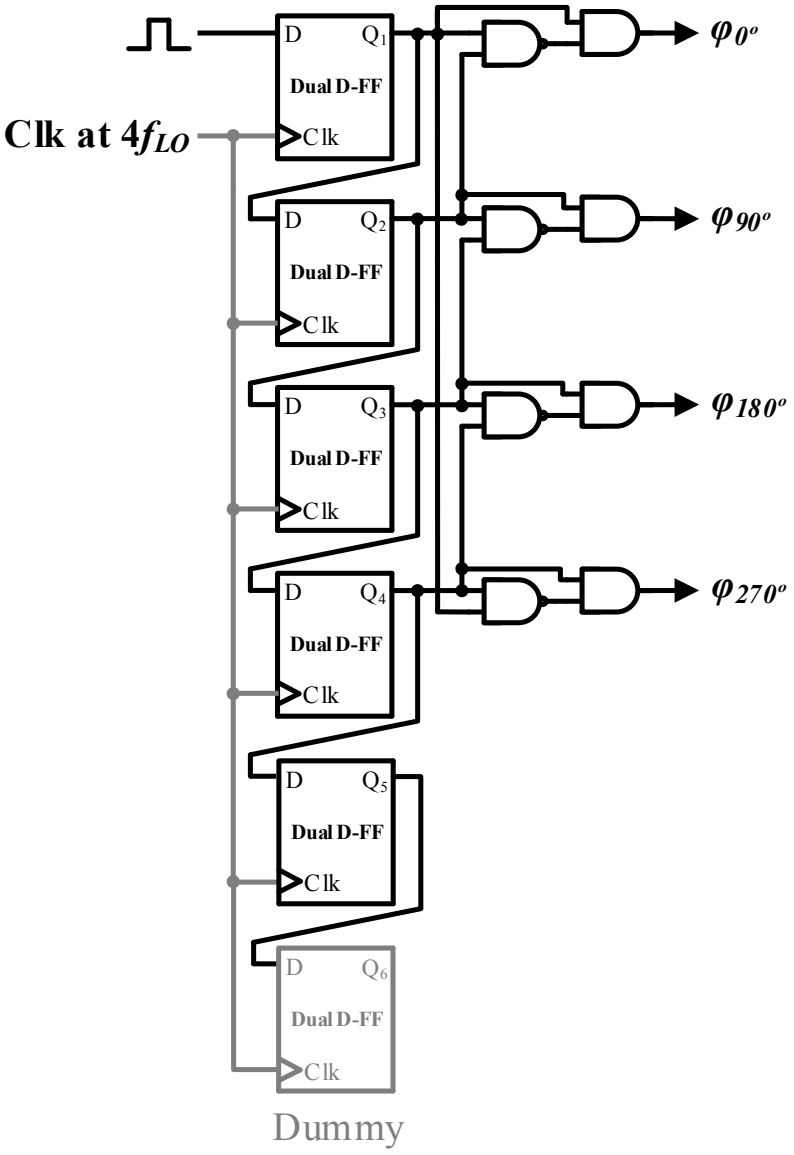

Figure 5.9: Quadrature 4-phase shift register with 25% duty-cycle.

CHAPTER 6

Simulation Results

This chapter is devoted to present the results obtained for the methods and systems described in the previous chapter. We start by introducing the circuit simulations realized throughout this work, followed by the test benches of each of the circuit blocks used in our circuits. The schematic simulations are then presented. First, the simulation results of the 3-stage CMOS ring oscillator and 3-phase LO generator employing SR are exposed. Afterwards, the results of the 4-phase ring oscillator and SR architectures are revealed, the latter with 50% and 25% duty-cycle approaches. Finally, the layout design and post-layout simulations of the 4-stage ring oscillator are also presented. Subsequently, a detailed discussion and a solid comparison are made in order to verify and validate the entire circuits.

Powered by a 1.2 V voltage supply, all circuits were produced and simulated in Cadence® Spectre RF using its provided analyses (transient, phase-noise, Periodic Steady-State (PSS) and Monte Carlo simulations). We also establish two single frequencies to test all the important features of our circuits: 600 MHz and 900 MHz. The reason why these frequencies were chosen is due to the fact that they belong to a frequency range of Wireless Medical Telemetry Service (WMTS) and Industrial, Scientific and Medical (ISM)/Global System for Mobile Communications (GSM) spectra respectively. Lastly, the same sizing was employed in any of the oscillators in order to disclose the advantages and drawbacks of each topology.

The technological process used is the United Microelectronics Corporation (UMC) L130E[1] MixedMode/RFCMOS - 1P8M2T[2] - 1.2 V, which has a Foundry Design Kit (FDK)

[1] Although it is a 130 nm process, the minimum transistor channel length of this technology is 120 nm.

[2] 1P8M2T means single-poly layer and eight metal (copper) layers, of which the top two are thicker (generally these thicker metals are used to build high quality inductors for RF applications).

or Process Design Kit (PDK) available through the Europractice IC service[3]. The design is fully customized, i.e., we do not use automatic place and route of IC standard cells neither use third partiers Intellectual Properties (IPs) IC cells, except for Input/Output (I/O) pads, for which we use Faraday IPs. Finally, we employ design tools from Cadence® Design Systems and from Mentor Graphics® Corporation. These Computer-Aided Design (CAD) tools are available from Europractice software service and the design tools used with the corresponding versions are shown in table 6.1.

Table 6.1: CAD tools and corresponding versions used.

Tool	Version
Cadence® Hierarchy Editor	05.01.000-s062
Library Manager	1.9
Virtuoso® Analog Design Environment	5.10.41.500.6.137
Virtuoso® Front to Back Environment	5.10.41.500.6.137
Virtuoso® Schematic Editor	5.10.41.500.6.137
Virtuoso® Spectre Circuit Simulator	7.1.1.187.isr11
WaveScan Waveform Tool	5.10.41.500.6.137

6.1 Schematic Simulations

6.1.1 3-stage Ring Oscillator

Fundamental frequency f_{LO} = 600 MHz

The DC operating point of the 3-stage ring oscillator (figure 5.2) for a fundamental frequency of 600 MHz is presented in table 6.2. All transistors are operating in the active region as they should be. Moreover, note how the current I_D is perfectly split along the current mirror presented in the circuit.

Figure 6.1 shows the output waveforms of the 3-stage ring oscillator structure designed for a fundamental frequency of 600 MHz. In this case sinusoidal outputs were obtained. To prevent this from happening, a buffer composed of single inverters should be used at the outputs.

The phase-noise curve for the same fundamental frequency is shown in figure 6.2. At 10 MHz offset the oscillator presents a phase-noise value of −118.6 dBc/Hz.

Considering that the 1st harmonic corresponds to the chosen fundamental frequency, the phase error relative to mismatches is shown in figure 6.3. 500 Monte Carlo runs considering variations of 3σ were done. The histogram reveals a minimum phase error (mean value [μ]) of 0.7255° with a standard deviation σ of 9.27°.

[3]Further details in `http://www.europractice-ic.com/technologies_UMC.php?tech_id=013um` (visited on 08/28/2015).

Table 6.2: DC operating point of the 3-stage ring oscillator for a fundamental frequency of 600 MHz (Inst: Instance, Trans: Transistor, Reg: Region, Inv: Inverter, CS: Current source, Act: Active).

Inst	Trans	g_m(mS)	I_D(mA)	V_{DS}(mV)	V_{DSsat}(mV)	Reg	g_{ds}(mS)	r_{ds}(mΩ)
Inv	M_1	1.11	0.06	408.1	75.2	Act	0.08	11.81
Inv	M_2	0.98	-0.06	-330.3	-80.8	Act	0.11	9.46
CS	M_3	2.40	-0.18	-196.9	-140.5	Act	0.08	12.18
CS	M_4	2.46	-0.19	-403.1	-140.7	Act	0.05	18.44
CS	M_5	2.78	0.18	264.1	110.2	Act	0.12	8.48
CS	M_6	2.97	0.19	379.4	110.7	Act	0.10	10.16

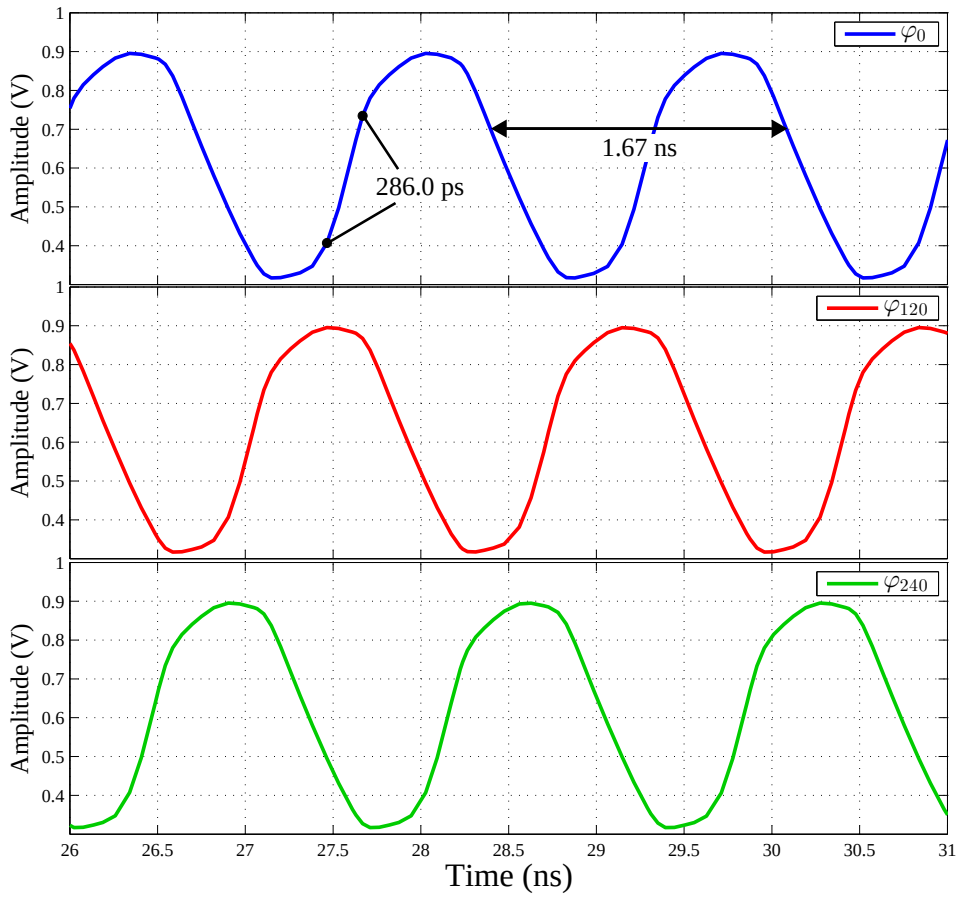

Figure 6.1: Oscillator transient response (f_{LO} = 600 MHz).

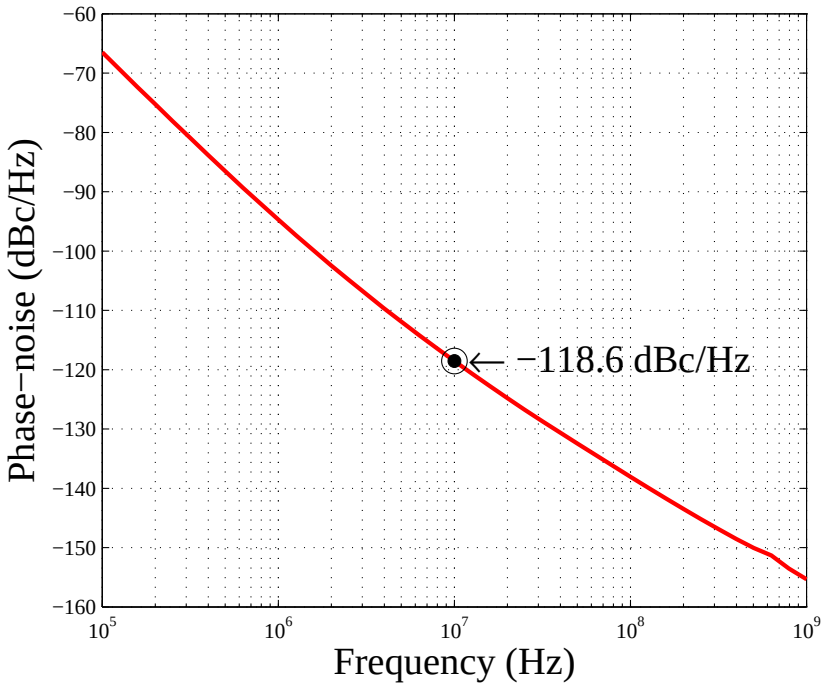

Figure 6.2: Oscillator phase-noise (f_{LO} = 600 MHz).

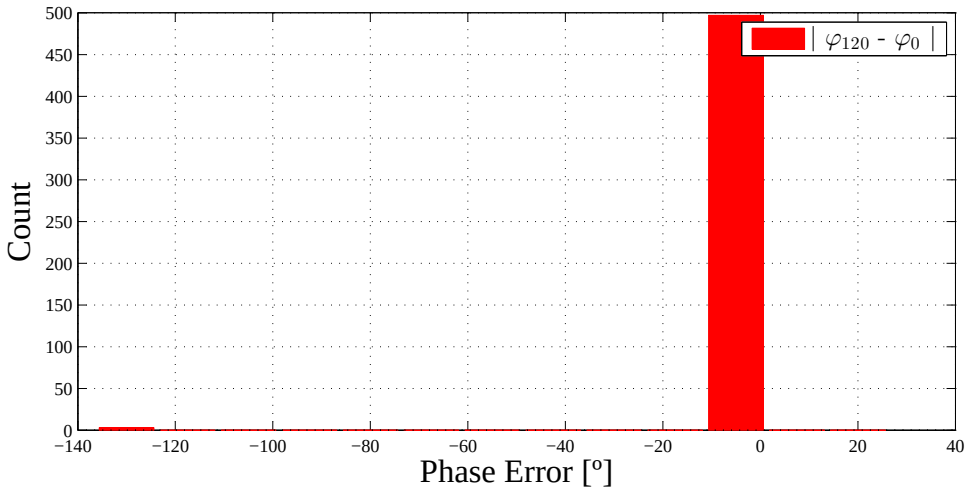

Figure 6.3: Phase error histogram ($\mu = 0.7255°$, $\sigma = 9.27°$).

Fundamental frequency f_{LO} = 900 MHz

Table 6.3 shows the DC operating point of the 3-stage ring oscillator shown in figure 5.2 for a fundamental frequency of 900 MHz.

Figure 6.4 shows the output waveforms of the 3-stage ring oscillator structure designed for the same fundamental frequency. At the outputs sinusoidal waveforms were obtained. A buffer should be used to prevent this from happening.

The phase-noise curve is shown in figure 6.5, where a phase-noise of −118.5 dBc/Hz at 10 MHz was obtained.

Finally, the phase error with regard to mismatches is shown in figure 6.6, where 500 Monte Carlo runs considering variations of 3σ were done. The histogram reveals a minimum phase error of 0.0074° with a standard deviation of 0.11°.

Table 6.3: DC operating point of the 3-stage ring oscillator for a fundamental frequency of 900 MHz (Inst: Instance, Trans: Transistor, Reg: Region, Inv: Inverter, CS: Current source, Act: Active, Tri: Triode).

Inst	Trans	g_m(mS)	I_D(mA)	V_{DS}(mV)	V_{DSsat}(mV)	Reg	g_{ds}(mS)	r_{ds}(mΩ)
Inv	M_1	1.64	0.10	431.8	85.5	Act	0.13	7.98
Inv	M_2	1.47	-0.10	-357.5	-97.6	Act	0.18	5.46
CS	M_3	2.95	-0.29	-162.2	-177.8	Tri	0.45	2.20
CS	M_4	3.38	-0.32	-446.1	-178.1	Act	0.06	17.69
CS	M_5	3.72	0.29	247.4	132.7	Act	0.21	4.85
CS	M_6	4.10	0.32	414.1	133.6	Act	0.15	6.57

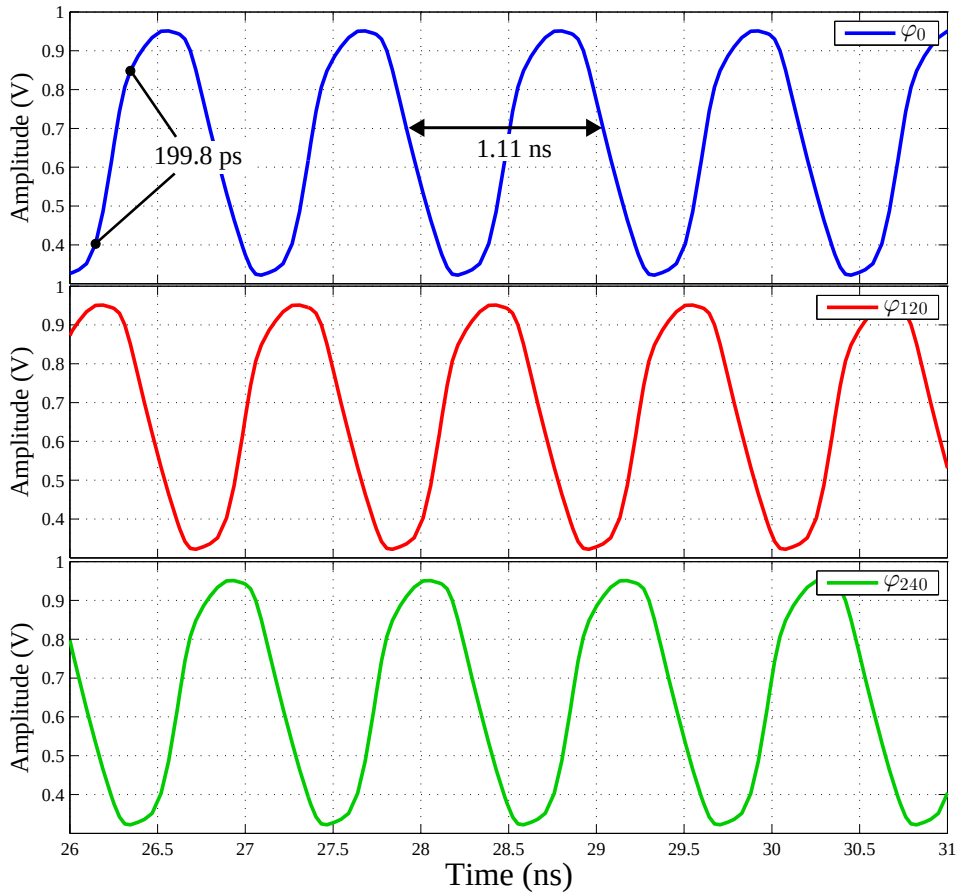

Figure 6.4: Oscillator transient response (f_{LO} = 900 MHz).

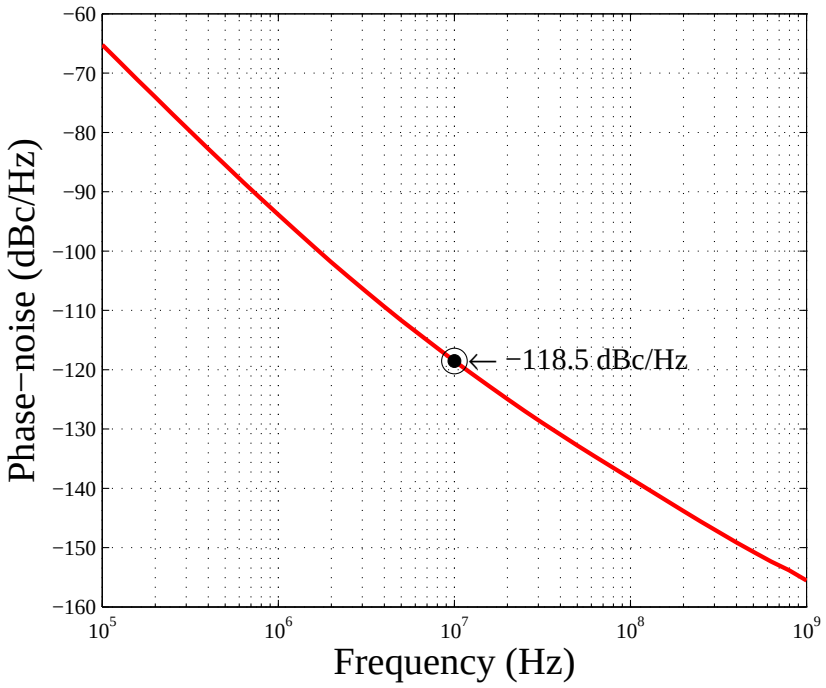

Figure 6.5: Oscillator phase-noise (f_{LO} = 900 MHz).

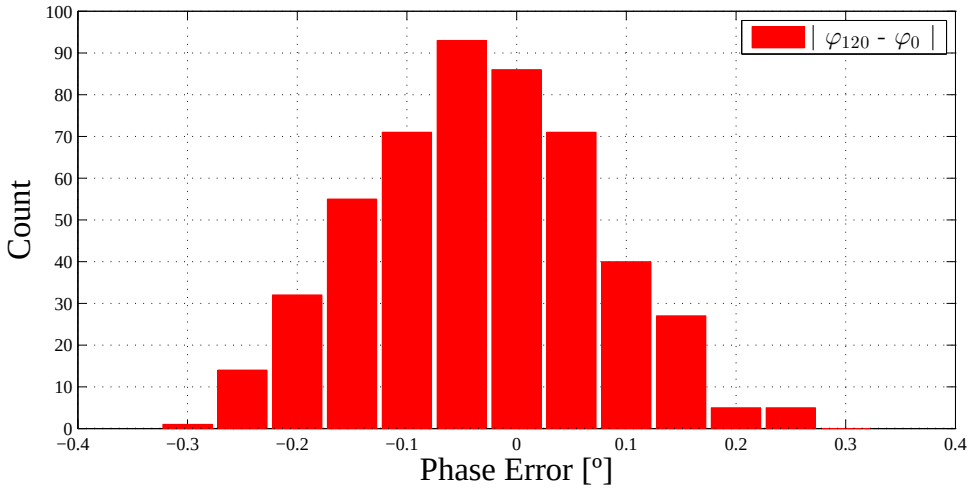

Figure 6.6: Phase error histogram ($\mu = 0.0074°$, $\sigma = 0.11°$).

6.1.2 3-phase Shift Register

Fundamental frequency f_{LO} = 600 MHz

Figure 6.7 illustrates the phase output waveforms of the 3-phase SR architecture shown in figure 5.6 for a fundamental frequency of 600 MHz. As intended, this generator presents non-overlapping square waveforms with fast rise/fall times, demonstrating how good this SR approach really is.

Afterwards, we present the phase-noise curve for the same fundamental frequency in figure 6.8. At 10 MHz offset, the generator presents a phase-noise value of −173.7 dBc/Hz, considering an ideal clock-phase generator.

Considering that the fundamental frequency is given by the 1st harmonic, the phase error due to mismatches is shown in figure 6.9. 500 Monte Carlo runs considering variations of 3σ were done. The histogram reveals a minimum phase error (μ) of 0.0002° with a σ of 0.03°.

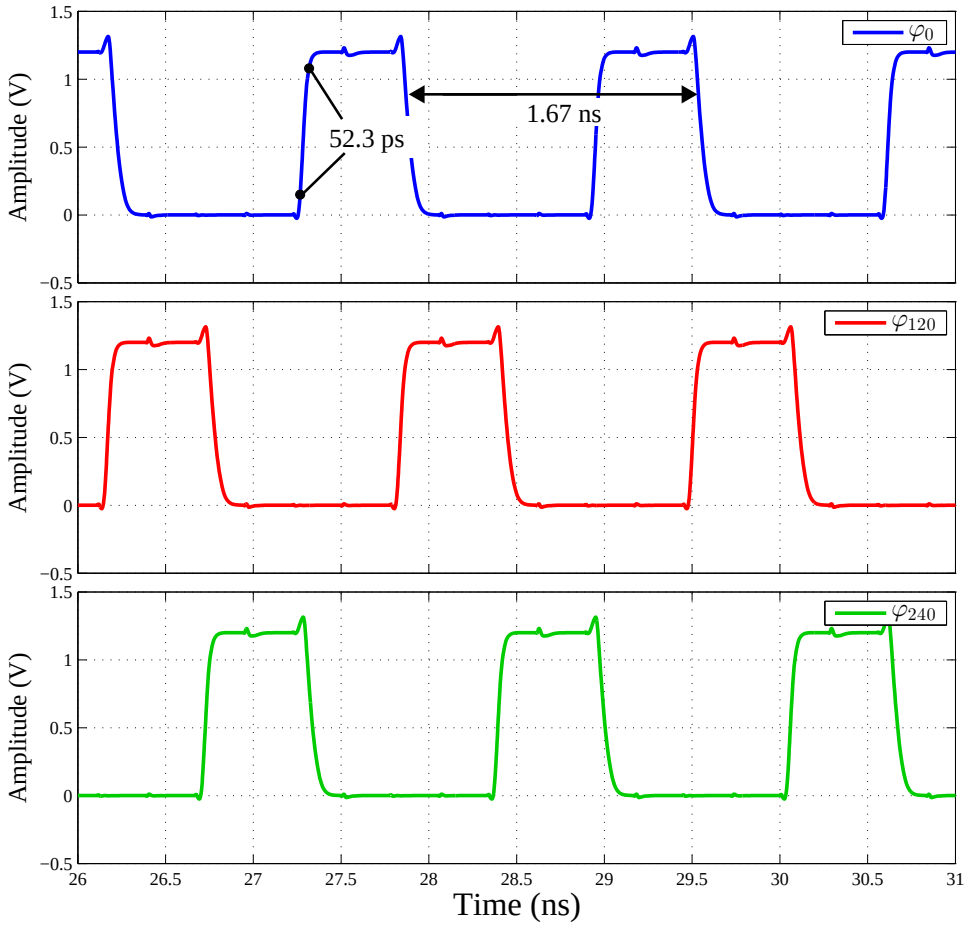

Figure 6.7: Generator transient response (f_{LO} = 600 MHz).

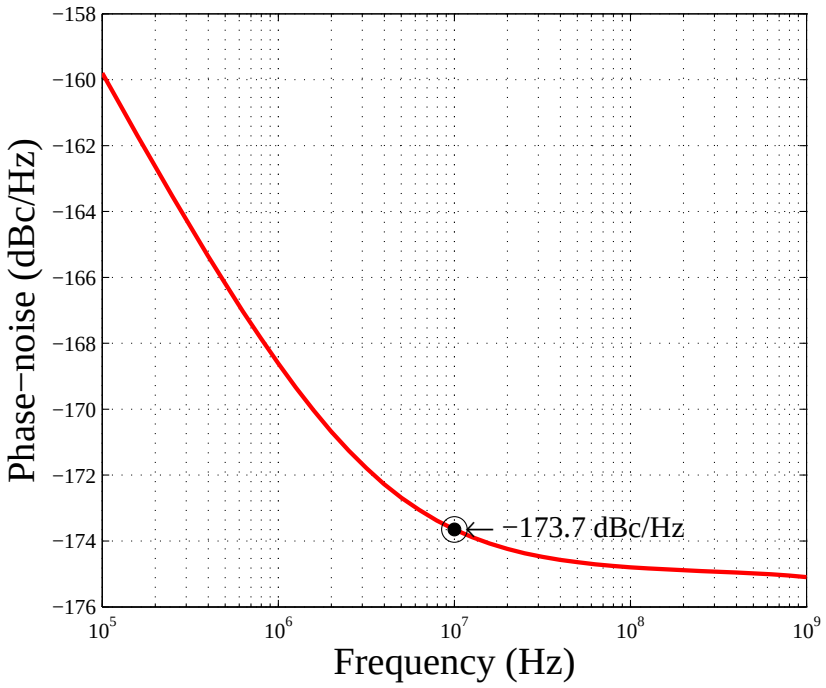

Figure 6.8: Generator phase-noise (f_{LO} = 600 MHz).

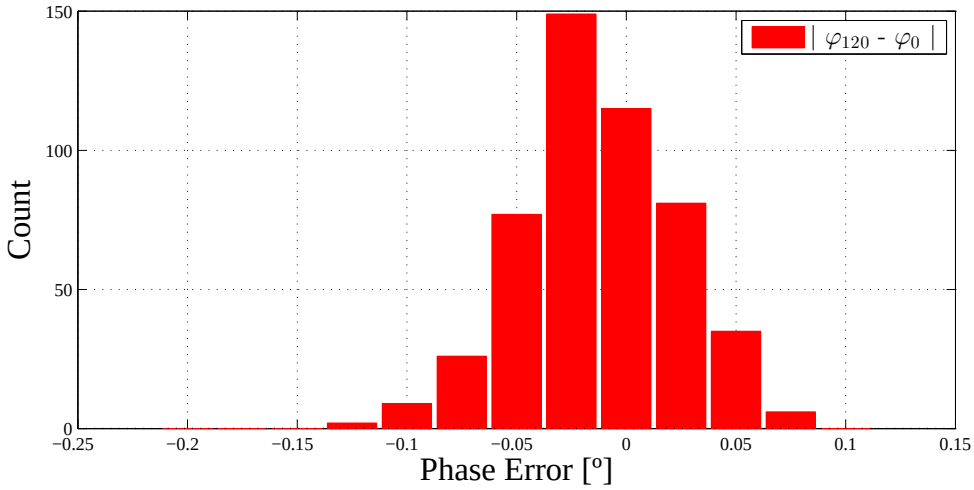

Figure 6.9: Phase error histogram (μ = 0.0002°, σ = 0.03°).

Fundamental frequency f_{LO} = 900 MHz

Figure 6.10 shows the phase square output waveforms of the 3-phase SR approach (figure 5.6) for a fundamental frequency of 900 MHz. As intended, each signal presents non-overlapping waves with fast rise/fall times, demonstrating how good this SR architecture is. The phase-noise curve for the same fundamental frequency is shown in figure 6.11. In this case, at 10 MHz offset the generator presents a phase-noise value of −172.3

dBc/Hz, considering an ideal clock. Figure 6.12 presents the histogram of the phase error due to mismatches. 500 Monte Carlo runs considering variations of 3σ were done. The histogram reveals a minimum phase error of 0.0008° with a standard deviation of 0.05°.

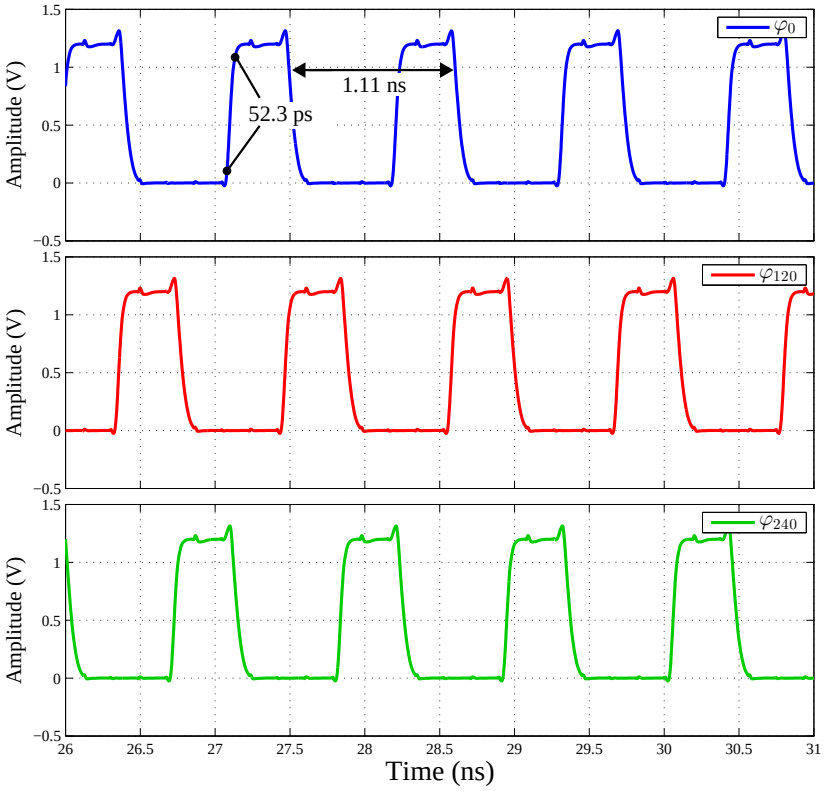

Figure 6.10: Generator transient response (f_{LO} = 900 MHz).

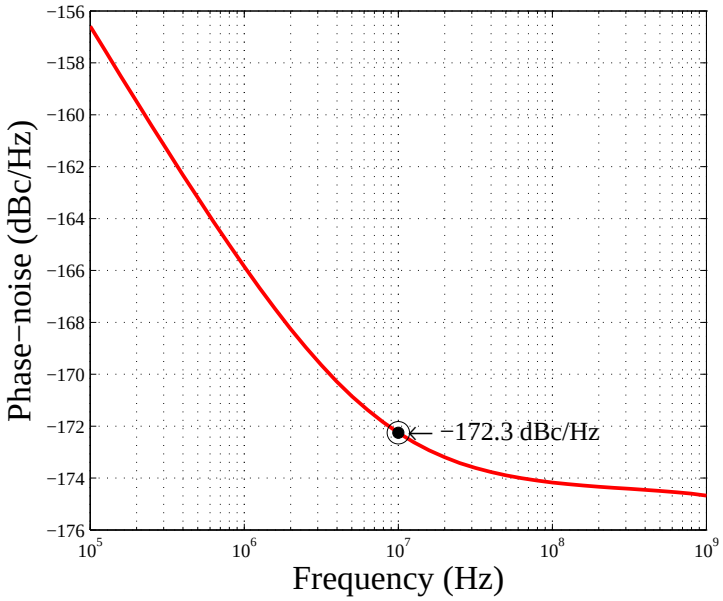

Figure 6.11: Generator phase-noise (f_{LO} = 900 MHz).

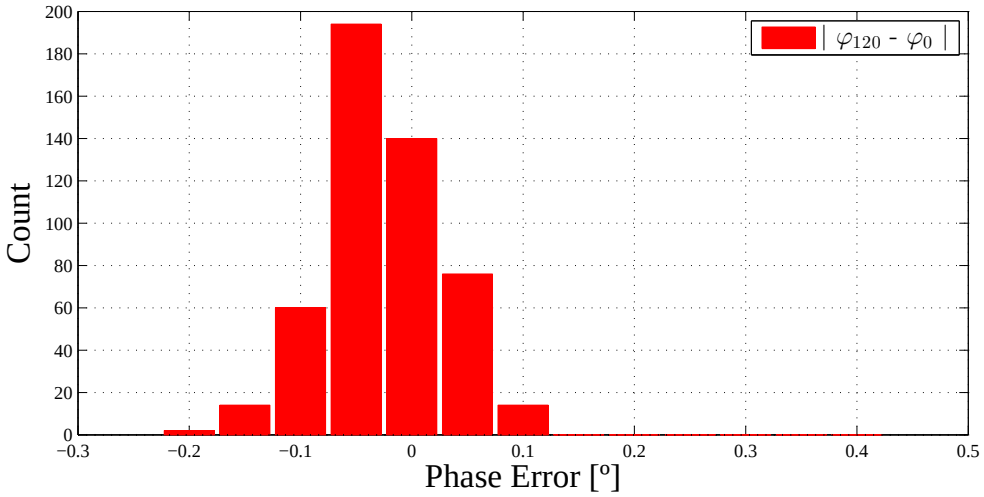

Figure 6.12: Phase error histogram ($\mu = 0.0008°$, $\sigma = 0.05°$).

6.1.3 4-stage Ring Oscillator

Fundamental frequency f_{LO} = 600 MHz

The DC operating point of the 4-stage ring oscillator shown in figure 5.3 for a fundamental frequency of 600 MHz is presented in table 6.4. Furthermore, figure 6.13 illustrates the output waveforms of the 4-stage ring oscillator structure designed for a fundamental frequency of 600 MHz. Each output presents a square waveform as we wanted.

Afterwards, the phase-noise curve for the same fundamental frequency is shown in figure 6.14. At 10 MHz offset the oscillator presents a phase-noise value of −124.5 dBc/Hz.

Considering that the 1st harmonic corresponds to the chosen fundamental frequency, the phase error due to mismatches is shown in figure 6.15. 500 Monte Carlo runs considering variations of 3σ were done. The histogram reveals a minimum phase error of 0.0056° with a standard deviation of 0.62°.

Table 6.4: DC operating point of the 4-stage ring oscillator for a fundamental frequency of 600 MHz (Inst: Instance, Trans: Transistor, Reg: Region, Inv: Inverter, CS: Current source, Act: Active, Tri: Triode).

Inst	Trans	g_m(mS)	I_D(mA)	V_{DS}(mV)	V_{DSsat}(mV)	Reg	g_{ds}(mS)	r_{ds}(mΩ)
Inv	M_1	1.31	0.07	415.2	79.1	Act	0.10	10.09
Inv	M_2	1.60	-0.07	-341.3	-87.3	Act	0.15	6.83
CS	M_3	4.15	-0.87	-212.2	-304.8	Tri	1.94	0.51
CS	M_4	6.14	-1.04	-590.1	-305.2	Act	0.16	6.20
CS	M_5	5.85	0.87	230.0	212.4	Act	0.99	1.01
CS	M_6	7.28	1.04	532.8	213.7	Act	0.40	2.52

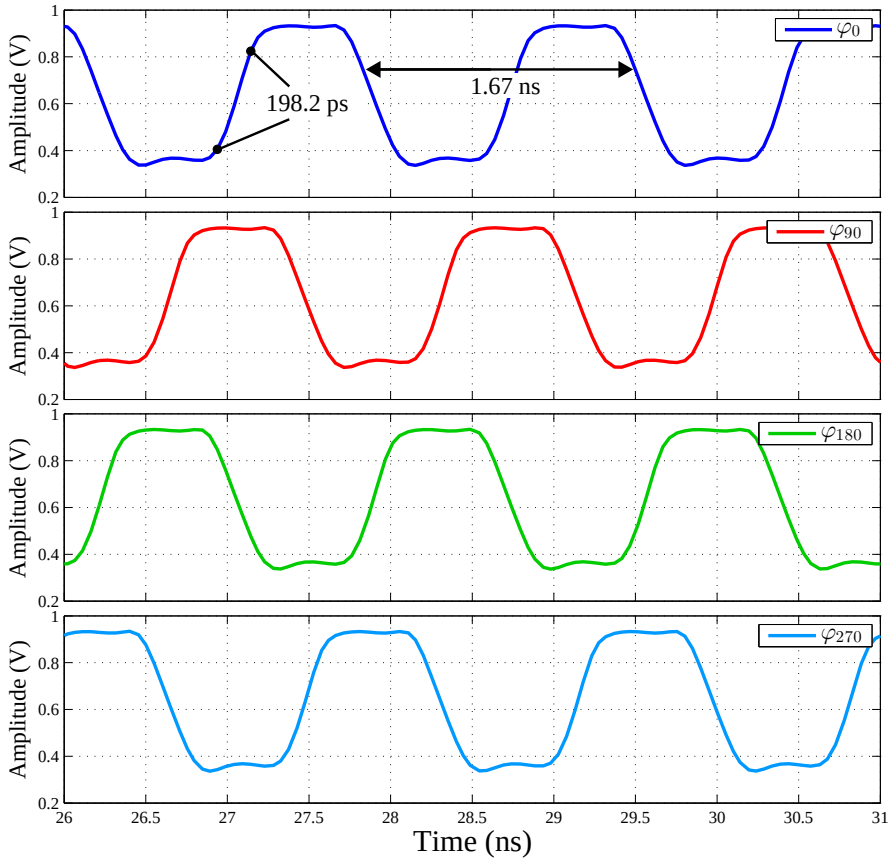

Figure 6.13: Oscillator transient response (f_{LO} = 600 MHz).

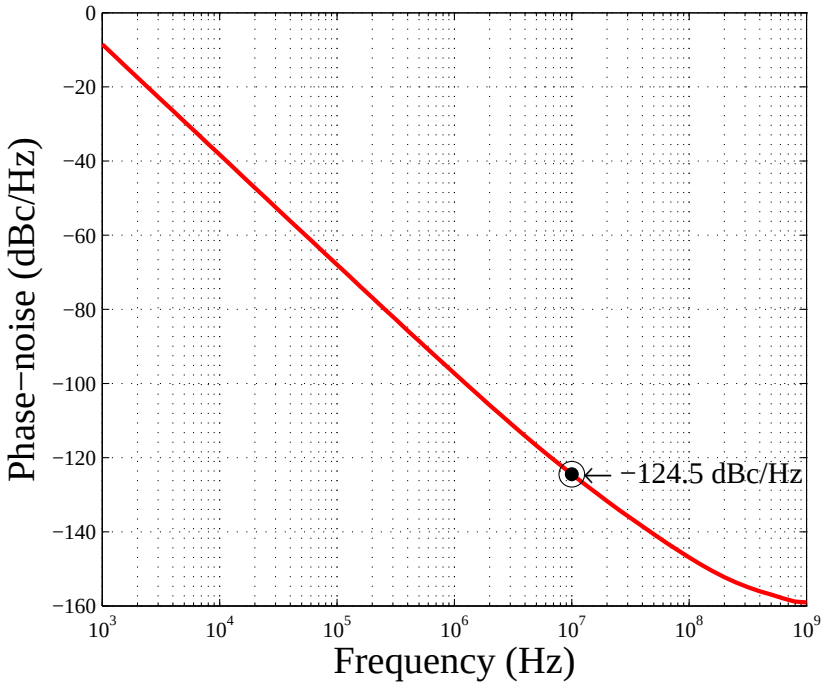

Figure 6.14: Oscillator phase-noise (f_{LO} = 600 MHz).

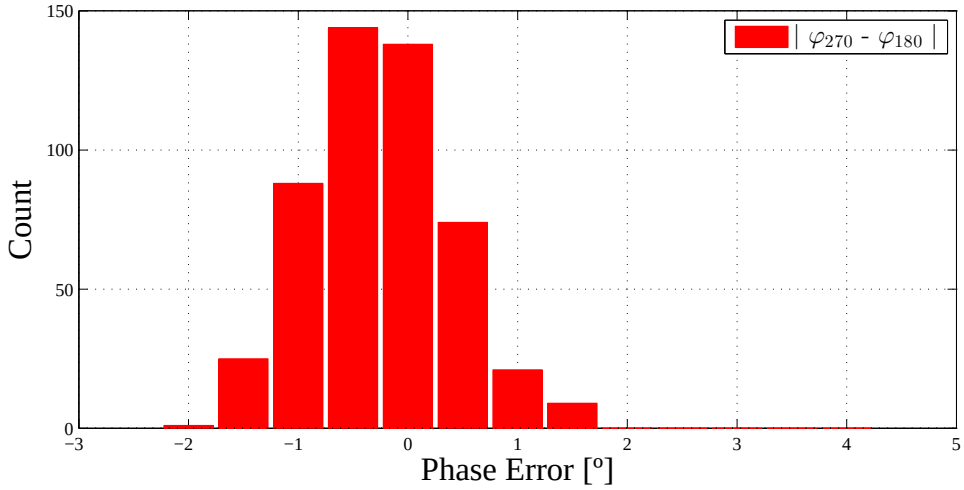

Figure 6.15: Phase error histogram ($\mu = 0.0056°$, $\sigma = 0.62°$).

Fundamental frequency f_{LO} = 900 MHz

Table 6.5 presents the DC operating point of the 4-stage ring oscillator shown in figure 5.3 for a fundamental frequency of 900 MHz.

The output waveforms of the 4-stage ring oscillator are shown in figure 6.16. Although the frequency has increased compared to the previous case, we continue to have a similar behaviour, i.e., each output presents a square waveform as intended.

The phase-noise curve is shown in figure 6.17. For a fundamental frequency of 900 MHz at 10 MHz offset the oscillator produces a phase-noise of −124.6 dBc/Hz.

Finally, figure 6.18 illustrates the phase error histogram, where 500 runes considering variations of 3σ were contemplated. The Monte Carlo histogram presents a phase error value of 0.0086° with a $\sigma = 0.47°$.

Table 6.5: DC operating point of the 4-stage ring oscillator for a fundamental frequency of 900 MHz (Inst: Instance, Trans: Transistor, Reg: Region, Inv: Inverter, CS: Current source, Act: Active, Tri: Triode).

Inst	Trans	g_m(mS)	I_D(mA)	V_{DS}(mV)	V_{DSsat}(mV)	Reg	g_{ds}(mS)	r_{ds}(mΩ)
Inv	M_1	1.85	0.11	435.0	89.5	Act	0.14	7.18
Inv	M_2	1.67	-0.11	-366.7	-104.1	Act	0.21	4.84
CS	M_3	3.85	-1.36	-209.3	-410.9	Tri	4.24	0.24
CS	M_4	7.78	-1.92	-712.2	-411.2	Act	0.28	3.58
CS	M_5	5.30	1.36	185.4	274.8	Tri	3.85	0.26
CS	M_6	9.05	1.92	633.3	276.4	Act	0.62	1.60

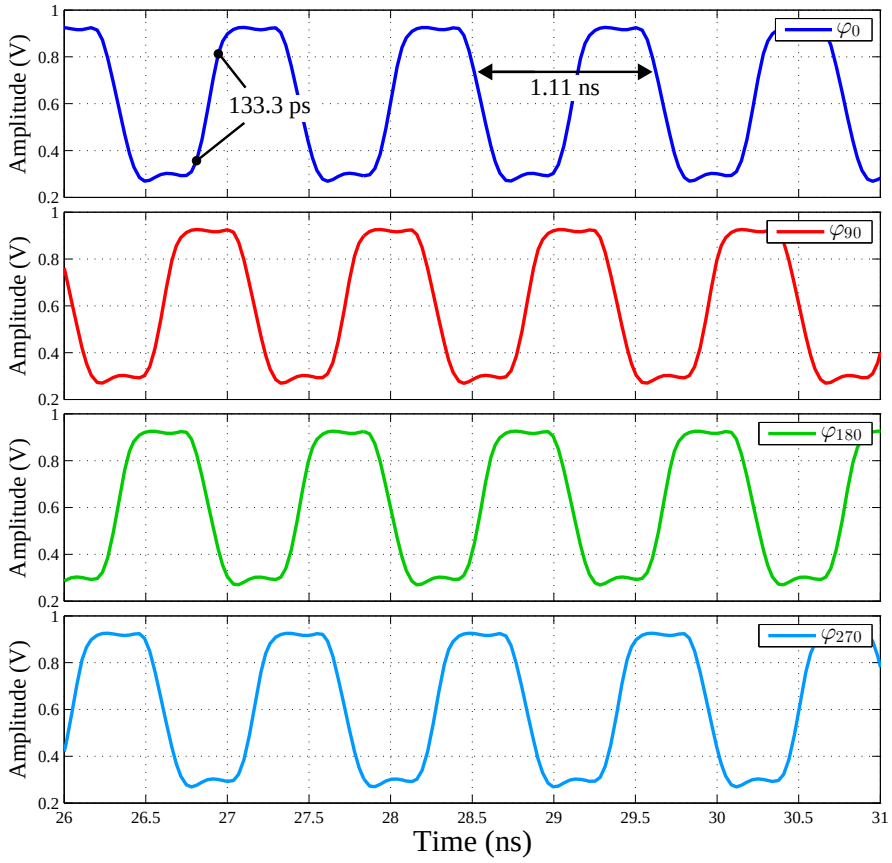

Figure 6.16: Oscillator transient response (f_{LO} = 900 MHz).

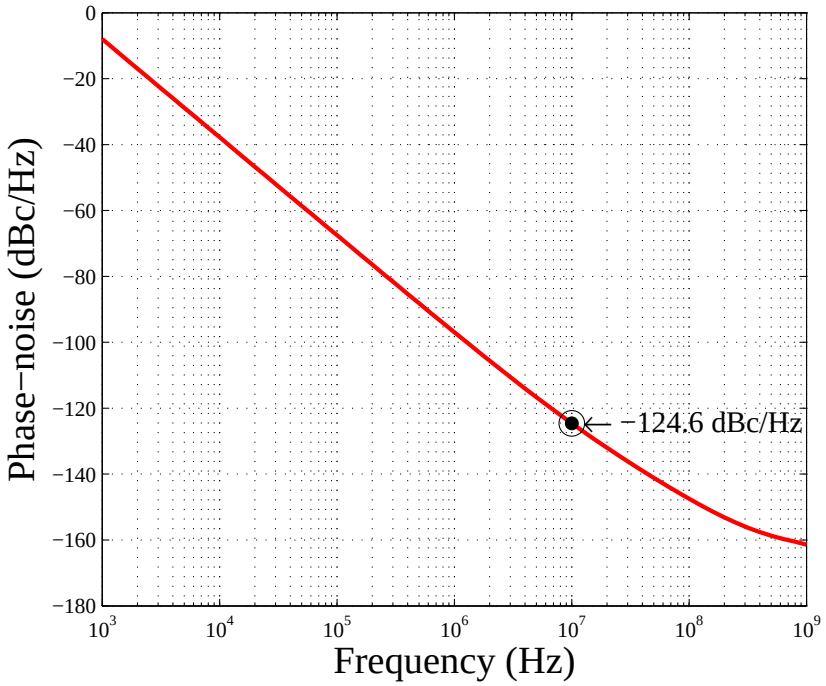

Figure 6.17: Oscillator phase-noise (f_{LO} = 900 MHz).

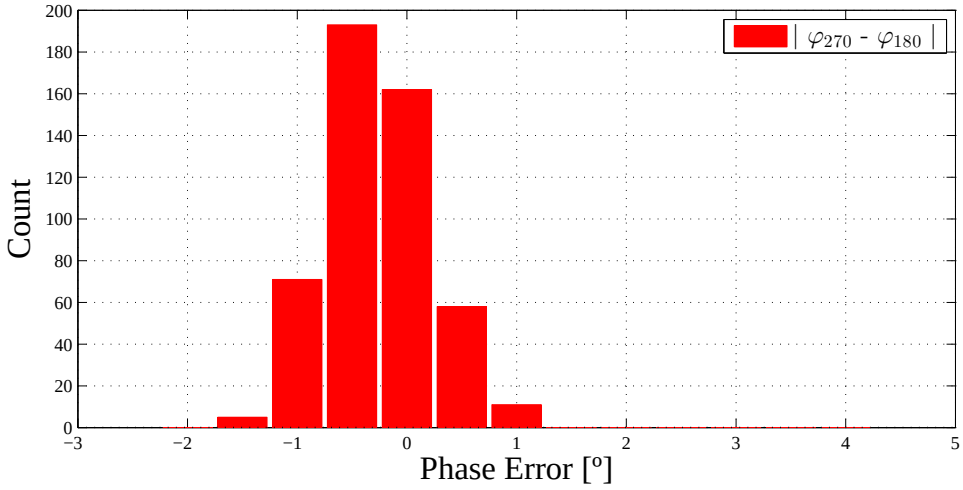

Figure 6.18: Phase error histogram ($\mu = 0.0086°$, $\sigma = 0.47°$).

In section 6.3.1, the layout of this structure will be developed. Therefore, these schematic results will be later compared with those obtained from post-layout simulations.

6.1.4 4-phase Shift Register with 50% Duty-cycle

Fundamental frequency f_{LO} = 600 MHz

Figure 6.19 illustrates the phase output waveforms of the 4-phase SR with 50% duty-cycle (figure 5.7) for a fundamental frequency of 600 MHz. In this case, each output presents a square waveform as intended.

In figure 6.20 we present the phase-noise curve for the same fundamental frequency. At 10 MHz offset the generator presents a phase-noise value of −174.7 dBc/Hz, considering an ideal clock-phase generator.

Considering that the 1st harmonic corresponds to the chosen fundamental frequency, the phase error due to mismatches is shown in figure 6.21. 500 Monte Carlo runs considering variations of 3σ were done. The histogram reveals a minimum phase error of 0.0010° with a standard deviation of 0.03°.

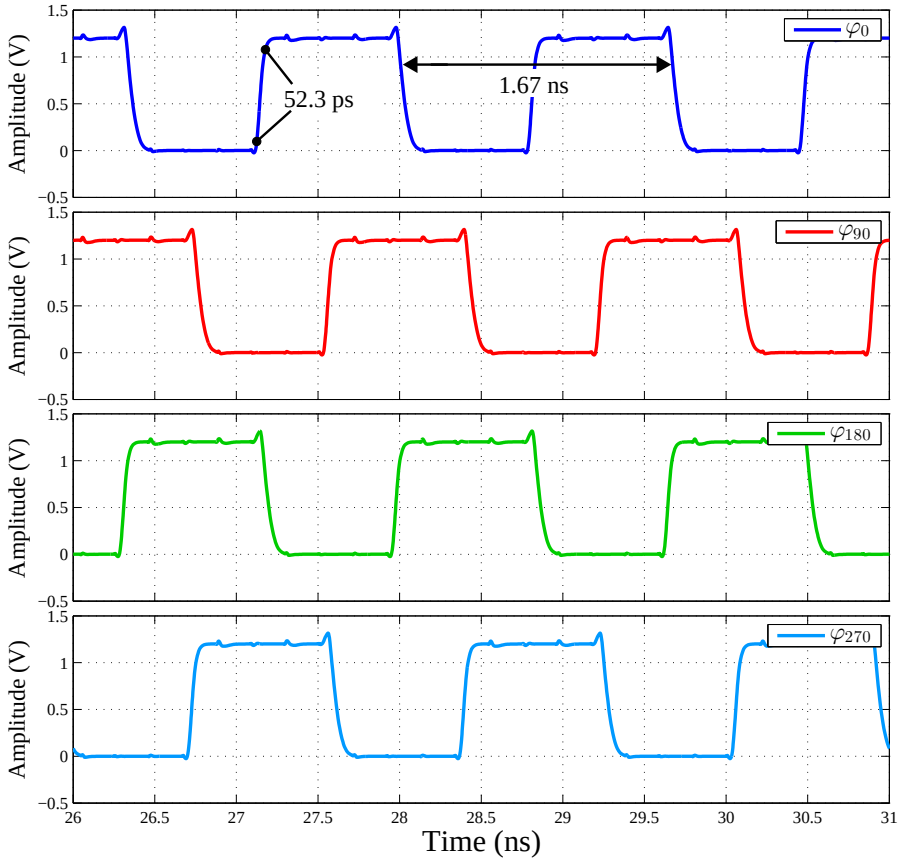

Figure 6.19: Generator transient response (f_{LO} = 600 MHz).

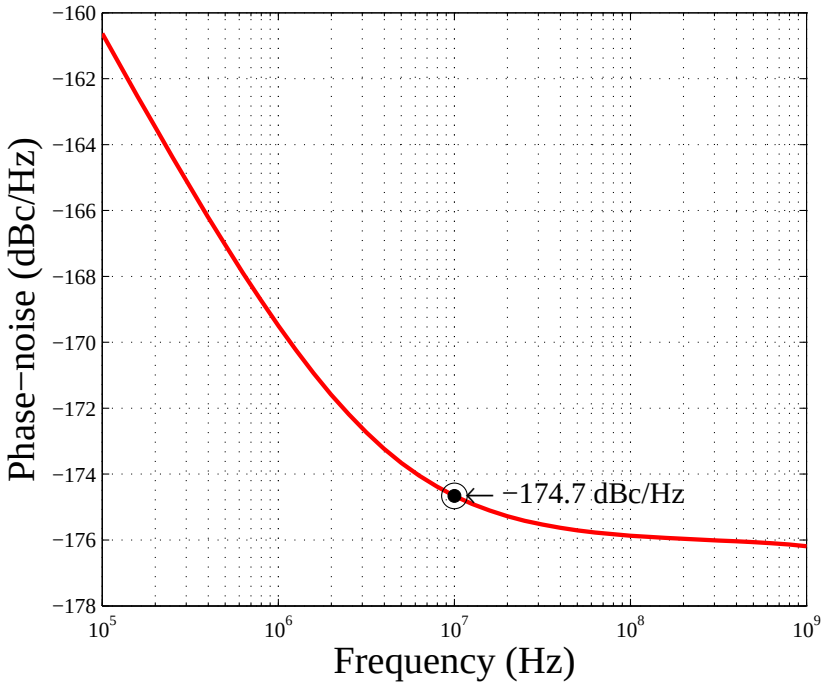

Figure 6.20: Generator phase-noise (f_{LO} = 600 MHz).

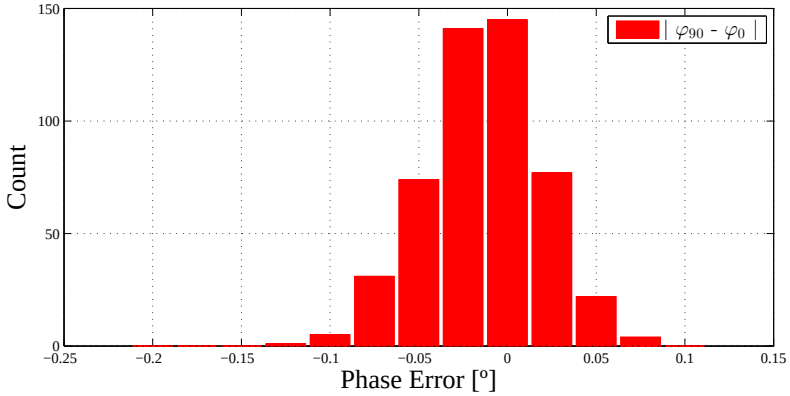

Figure 6.21: Phase error histogram ($\mu = 0.0010°$, $\sigma = 0.03°$).

Fundamental frequency f_{LO} = 900 MHz

The phase output waveforms of the 4-phase SR with 50% duty-cycle (figure 5.7) for a fundamental frequency of 900 MHz are presented in figure 6.22. As intended, this generator provides a square waveform in each of its outputs. Figure 6.23 shows the phase-noise curve for the same fundamental frequency. At 10 MHz offset the generator presents a phase-noise value of −172.3 dBc/Hz, regarding an ideal clock-phase generator. Considering that the fundamental frequency is given by the 1st harmonic, the phase error due to mismatches is shown in figure 6.24. 500 Monte Carlo runs considering variations of 3σ were done. The histogram reveals a minimum phase error of 0.0012° with a standard deviation of 0.06°.

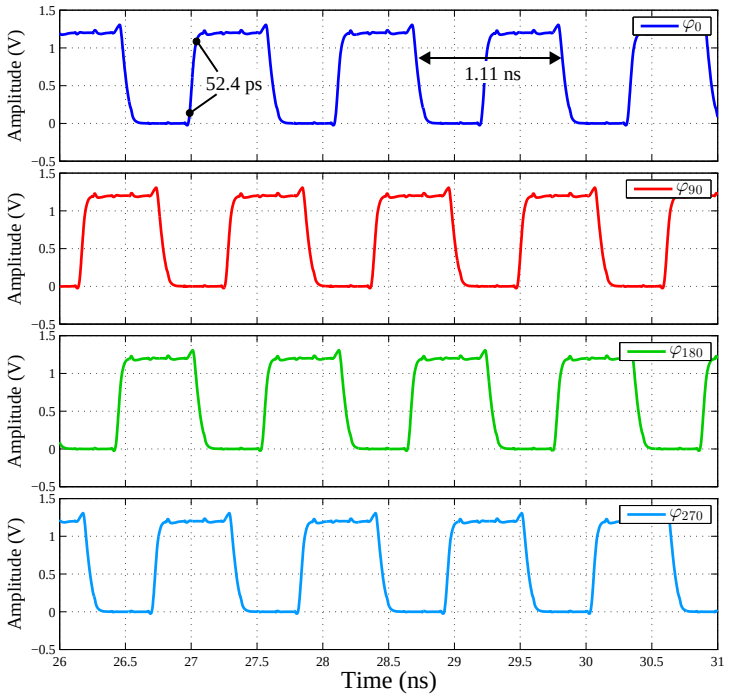

Figure 6.22: Generator transient response (f_{LO} = 900 MHz).

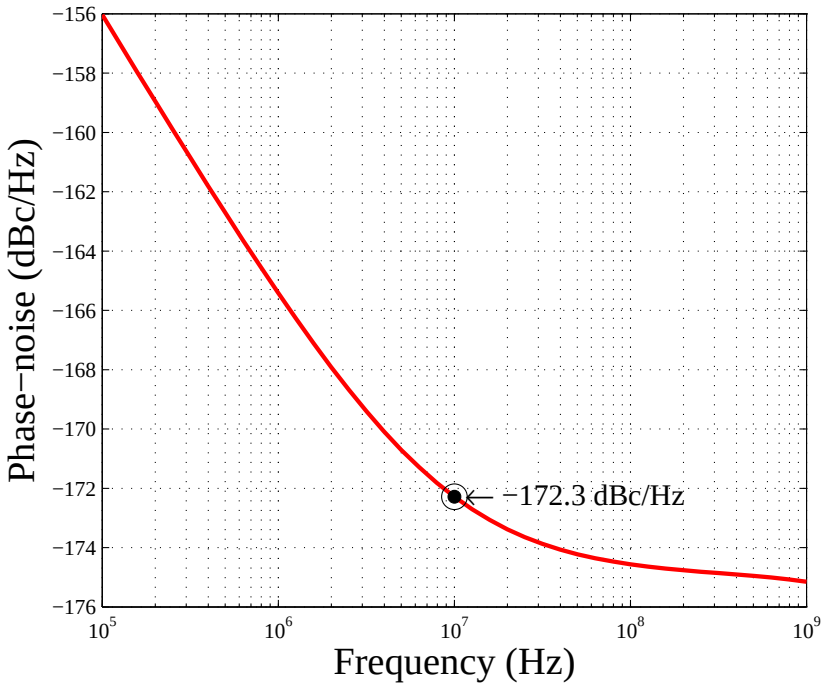

Figure 6.23: Generator phase-noise (f_{LO} = 900 MHz).

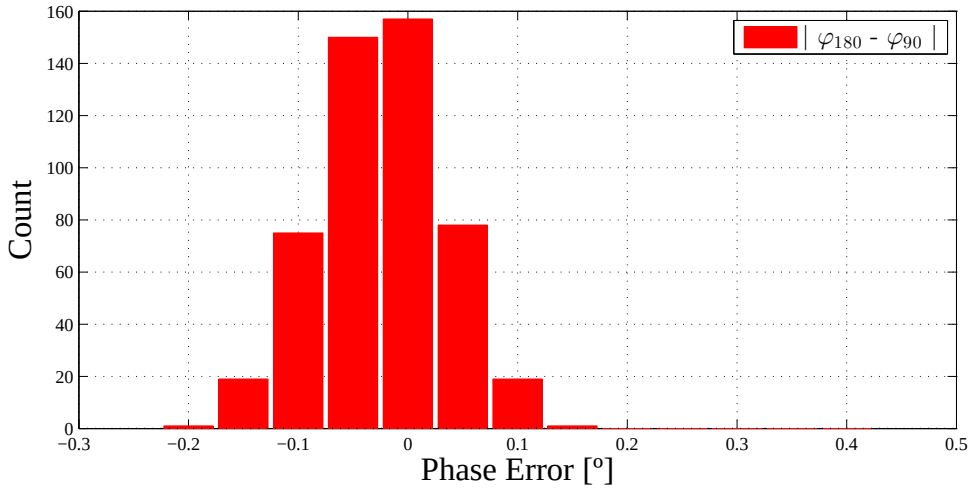

Figure 6.24: Phase error histogram (μ = 0.0012°, σ = 0.06°).

6.1.5 4-phase Shift Register with 25% Duty-cycle

Fundamental frequency f_{LO} = 600 MHz

Figure 6.25 presents the phase output waveforms of the quadrature 4-phase SR with 25% duty-cycle (figure 5.9) for a fundamental frequency of 600 MHz. As intended, the generator produces non-overlapping square waves with fast rise/fall times, demonstrating how good this SR approach is. The phase-noise curve for the same fundamental

frequency is shown in figure 6.26. At 10 MHz offset the generator presents a phase-noise value of −172.0 dBc/Hz due to the use of an ideal clock-phase generator. Considering that the 1st harmonic corresponds to the chosen fundamental frequency, the phase error due to mismatches is shown in figure 6.27. 500 Monte Carlo runs considering variations of 3σ were done. The histogram reveals a minimum phase error of 0.0011° with a standard deviation of 0.04°.

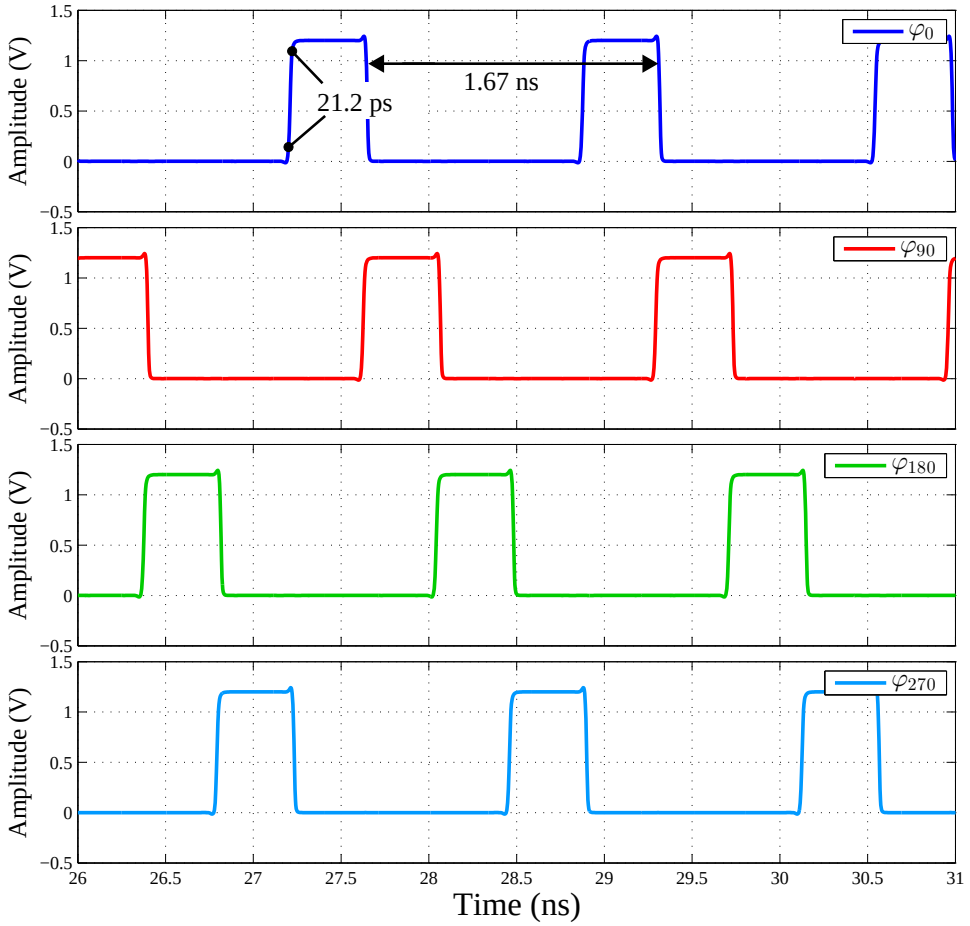

Figure 6.25: Generator transient response (f_{LO} = 600 MHz).

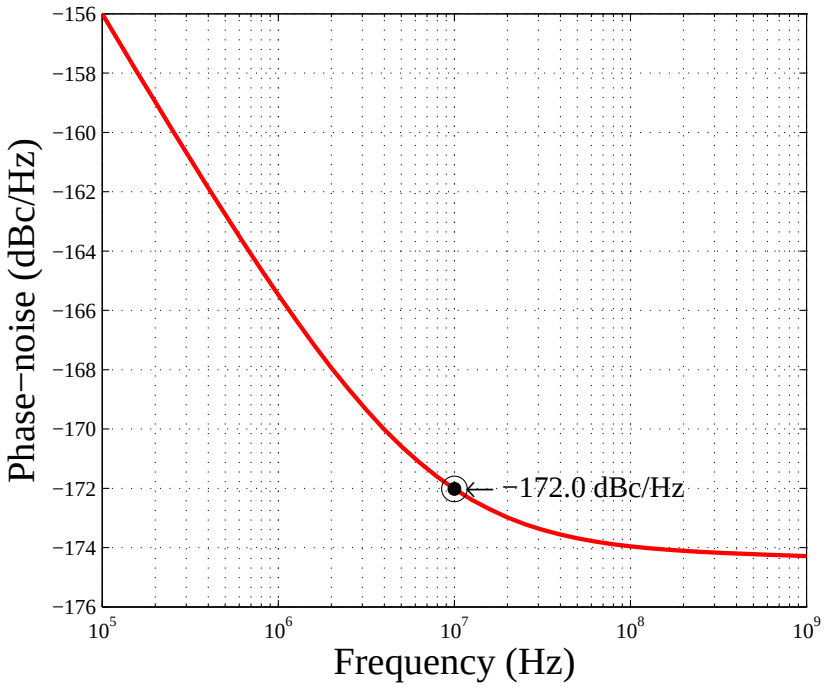

Figure 6.26: Generator phase-noise (f_{LO} = 600 MHz).

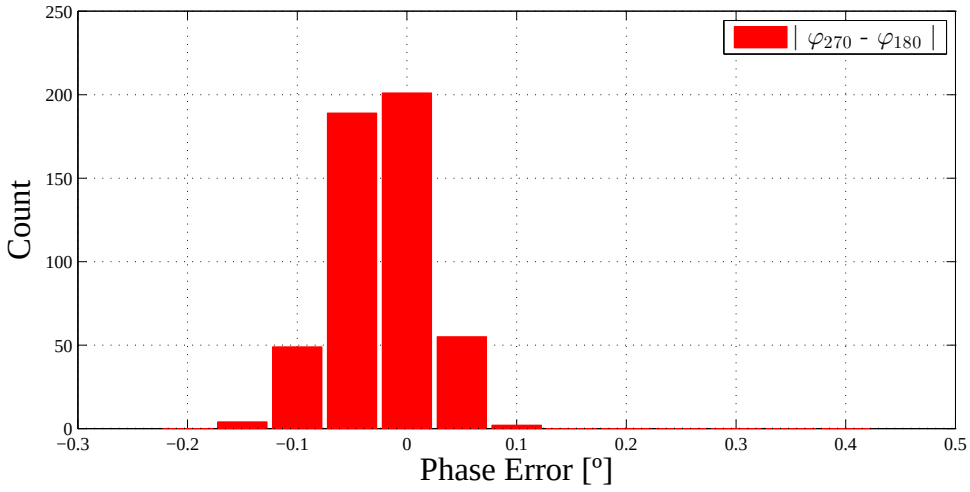

Figure 6.27: Phase error histogram (μ = 0.0011°, σ = 0.04°).

Fundamental frequency f_{LO} = 900 MHz

The phase output waveforms of the quadrature 4-phase SR with 25% duty-cycle (figure 5.9) for a fundamental frequency of 900 MHz are presented in figure 6.28. As intended, the generator provides non-overlapping square waves with fast rise/fall times, demonstrating how good this SR architecture really is. Figure 6.29 shows the phase-noise curve for the same fundamental frequency. At 10 MHz offset the generator presents a

phase-noise value of −169.8 dBc/Hz, since an ideal clock-phase generator was applied. Considering that the fundamental frequency is given by the 1st harmonic, the phase error due to mismatches is shown in figure 6.30. 500 Monte Carlo runs considering variations of 3σ were done. The histogram reveals a minimum phase error of 0.0019° with a standard deviation of 0.06°.

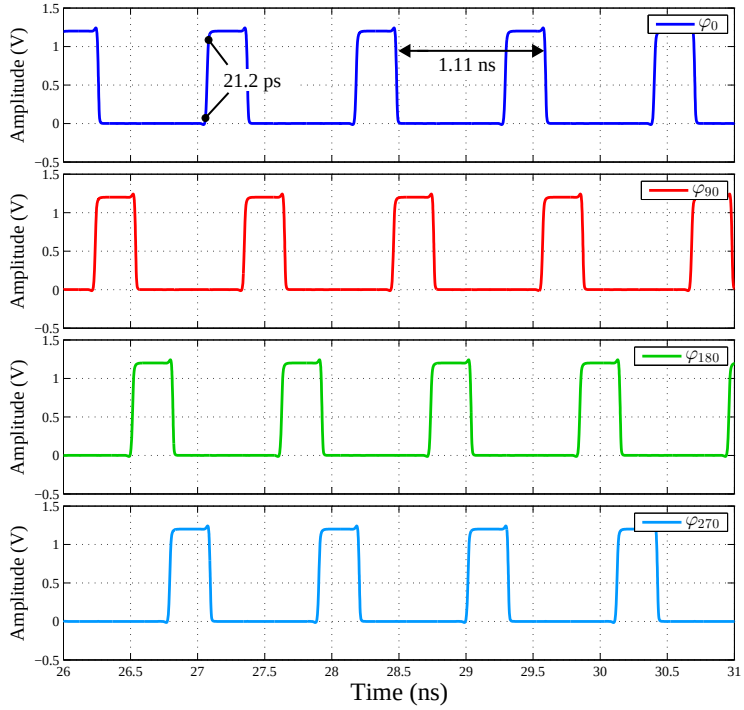

Figure 6.28: Generator transient response (f_{LO} = 900 MHz).

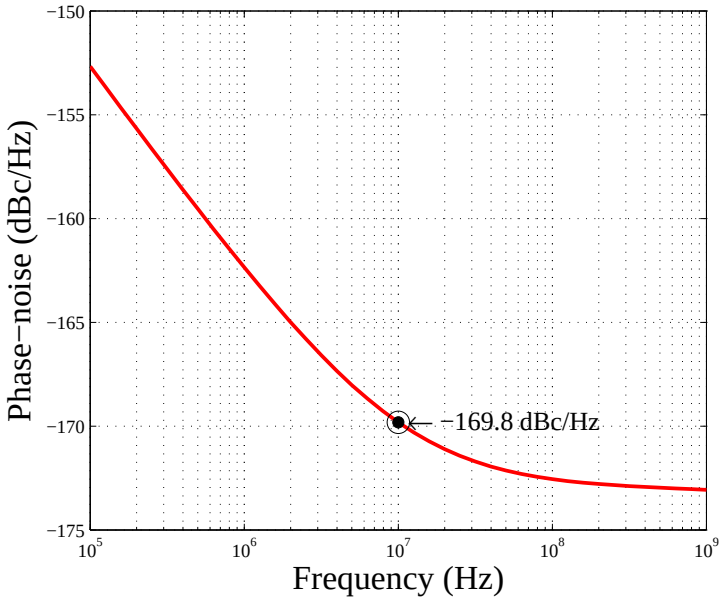

Figure 6.29: Generator phase-noise (f_{LO} = 900 MHz).

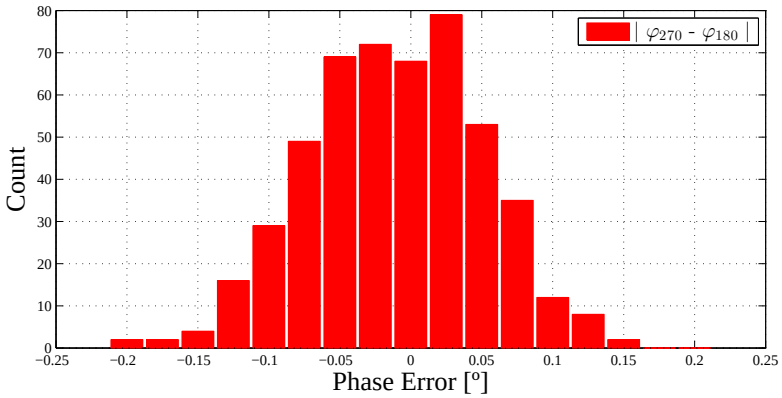

Figure 6.30: Phase error histogram ($\mu = 0.0019°$, $\sigma = 0.06°$).

6.2 Layout Design

In this section, a possible physical layout of the 4-stage ring oscillator is presented. For a better understanding of all the elements that set up the proposed layout, it was decided to present it hierarchical, i.e., as the same way as it was designed: starting with the most basic components such as the transistors, following the inverter assembly and the design a posteriori of the oscillator core, which comprises eight single-ended inverters. Subsequently, we proceeded to the design of the current source which feeds the same core, followed by assembling the two main blocks and adding the four capacitors that compose the buffer.

The physical design (layout) was completely submitted to physical verifications, such as the Design Rule Checking (DRC) rules (to check whether the layout is manufacturable or not), the Layout Versus Schematic (LVS) check (to check whether the schematic and layout match well) and the Layout Parameter Extraction (LPE) (to confirm if the extracted layout still delivers the same performance parameters than those achieved with the electrical schematic) in order to verify if the layout design was correct and robust [93, 131, 150]. These classes of Electronic Design Automation (EDA) were done using Calibre Interactive. Note that, taking the electrical schematic as a reference point, the extracted layout abstraction is a step closer to the physical IC. Hence, the simulations results coming from this abstraction level are valuable and more realistic due to the inclusion of RC parasites. Subsequently the extracted simulations, the post-layout results are compared with the schematic simulation results from subsection 6.1.3.

6.2.1 Layout Considerations

RF circuits are very critical/sensitive to parasitic effects. To get robust and predictable performance, a careful layout strategy must be adopted to minimize the wiring differences and the signal path shall be carefully arranged by following considerations. First,

associated with the metal layers (ME) are parasitic capacitances and resistance, which shall be avoided. Therefore, it is very important to decide which metal layers to use. Another suggestion is to not use layers with high resistivity to create long paths. Even though the gate terminal of CMOS transistors has high impedance, there is always leakage and transient currents. For instance, a very narrow and long path has a very high resistance, so there will be a voltage drop if too much current passes there. On the other hand, the parasitic capacitance in a node where a high-frequency signal passes must be taken into account so the signal does not become much slower. Afterwards, the distance between two paths or components shall be larger to avoid mutual inductance or parasitic capacitance. Moreover, to avoid the coupling noise from noisy substrate, the top metal layer is used for signal path. The last consideration is that the path shall be as short and straight as possible. If there is a branch on the path, the distance of two paths shall be designed to the same to avoid phase variation.

In the component arrangement, the circuit layout shall be as symmetrical as possible to mitigate any process variations between the components present in the circuit. In addition, signal paths shall have the same length to avoid possible phase errors. Furthermore, the usage of maximum finger number of transistor is suggested by [151]. Larger finger number leads to lower process variation and better model fitting. Moreover, although both RF CMOS transistors used can support an odd number of fingers, it is recommended to use even finger number to reduce drain junction capacitance. The corner section *tt* (typical n-ch MOSFET and typical p-ch MOSFET) was applied in both transistors and regarding their biasing coverage, these transistors can achieve a voltage up to V_{DD} with a frequency up to 18 GHz, and they cover a temperature range from -55 °C to 125 °C.

The architecture and layout of both devices employ double-side gate contacts to reduce gate resistance. Dummy poly gates are also applied at each side to improve the poly Critical Dimension (CD) uniformity of poly fingers. In addition, the pick-ups of source and drain use $ME_1 - ME_3$ metal stacks to improve current handling capabilities. Finally, the space between Poly gate and S/D contacts is 0.12 μm.

All blocks that compose the circuit have been carefully placed in the same position. Therefore, it was decided that inverters were aligned vertically in order to design a circuit as organized as possible and at the same time occupying the smallest area possible. Furthermore, with rare exceptions to keep the circuit logically structured, odd metals (ME_1, ME_3, etc.) are laid out horizontally while even metals (ME_2, ME_4, etc.) are laid out vertically. In addition, at least two contacts/vias in each ohmic contact were used.

It is important to know the basic aspects of the layout rules associated with the technology employed (e.g., the minimum width of routing metals, the minimum distance between them, the minimum distance between adjacent diffusion regions, etc) to make a manufacturable place and route. For this purpose, the Topological Layout Rules (TLR) of the technology should be consulted. This document is provided with the FDK. Moreover, it is relevant to examine the layout rules, I/O latch-up rules, antenna rules, current density each metal trace and via can carry reliably and also the manufacturing grid, which

is the minimum layout grid allowed by the technology. For the technology used in this work, this grid is 10 nm.

6.2.2 Hierarchical Layout

1.2V Pwell RF NMOS

In this work, the cell name of the UMC Digital Rights Management (DRM) 1.2V Pwell RF NMOS used was the N_12_RF, which has four terminals: drain (D), gate (G), source (S) and bulk (B). The model range is limited as follows:

$$\begin{cases} 0.9 \leq WF \leq 7.2\ (\mu\text{m}) \\ 0.12 \leq LF \leq 0.36\ (\mu\text{m}) \\ 4 \leq NF \leq 16 \\ M \geq 1, \end{cases} \tag{6.1}$$

where WF is the gate finger width, LF is the gate finger length, NF is the gate finger number and M is the MOS multiplier. Figure 6.31 illustrates the layout of the 1.2V Twin Well RF NMOS, considering its adopted sizing for this work:

$$\begin{cases} WF = 2.5\ \mu\text{m} \\ LF = L_{min} = 120\ \text{nm} \\ NF = 4 \\ M = 1. \end{cases} \tag{6.2}$$

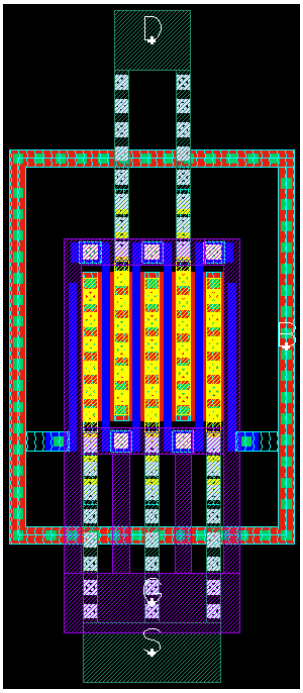

Figure 6.31: Layout of the 1.2V Twin well RF NMOS used.

Figure 6.32 shows the subcircuit model topology of 1.2V Twin Well RF NMOS.

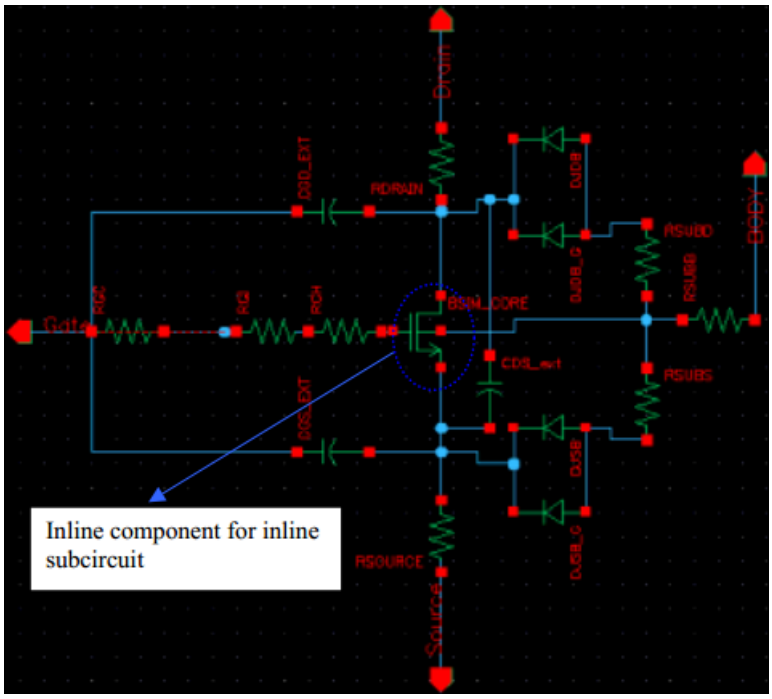

Figure 6.32: Subcircuit topology of 1.2V Twin Well RF NMOS [151].

1.2V Nwell RF PMOS

The cell name of the UMC DRM 1.2V Nwell RF PMOS used was the P_12_RF. This device is composed of five terminals: drain (D), gate (G), source (S), bulk (B) and p-substrate (PSUB). Its model range is:

$$\begin{cases} 1.6 \leq WF \leq 9.6\ (\mu\text{m}) \\ 0.12 \leq LF \leq 0.36\ (\mu\text{m}) \\ 2 \leq NF \leq 32 \\ M \geq 1. \end{cases} \tag{6.3}$$

Figure 6.33 exposes the layout of the 1.2V RF PMOS used, considering the following transistor sizing:

$$\begin{cases} WF = 5\ \mu\text{m} \\ LF = 120\ \text{nm} \\ NF = 6 \\ M = 1. \end{cases} \tag{6.4}$$

Figure 6.34 illustrates the subcircuit model topology of the 1.2V RF PMOS.

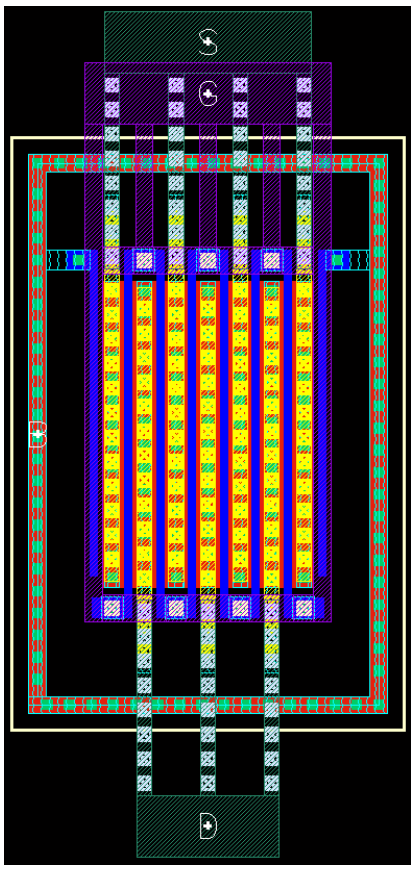

Figure 6.33: Layout of the 1.2V RF PMOS used.

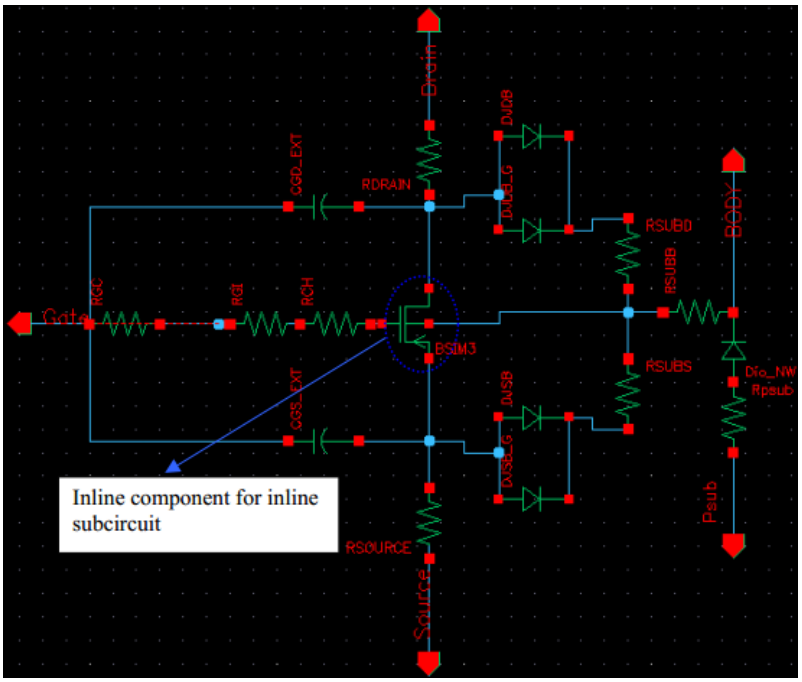

Figure 6.34: Subcircuit topology of 1.2V RF PMOS [151].

MIM Capacitor

The chosen capacitor was the MIMCAPS_MML_130E. This Metal-Insulator-Metal (MIM) capacitor has been successfully developed for 0.13 μm Mixed mode technology and is suggested to be put between last two layers metal for lower parasitic capacitance and less substrate loss. Moreover, it is composed of plus and minus terminals, with a model range of:

$$\begin{cases} 3.9 \leq W \leq 100\ (\mu\text{m}) \\ 3.9 \leq L \leq 100\ (\mu\text{m}) \\ Ca = 1\ \text{fF}/\mu\text{m}^2 \\ Cf = 0.114\ \text{fF}/\mu\text{m}, \end{cases} \tag{6.5}$$

where W and L are the capacitor width and length, respectively. Ca is the area component of the parasitic capacitance (specific capacitance) and Cf is the fringing capacitance per unit length. Figure 6.35 shows the layout of the MIM capacitor employed, considering the following sizing:

$$\begin{cases} W = 3.9\ \mu\text{m} \\ L = 3.9\ \mu\text{m} \\ C_{tot} = 16.9884\ \text{fF}, \end{cases} \tag{6.6}$$

where C_{tot} is the total capacitance value, which assumes the minimum capacitance value provided by the chosen MIM capacitor.

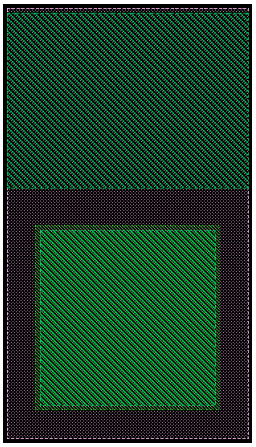

Figure 6.35: Layout of the MIM capacitor used.

It was decided to use this capacitor instead of MIMCAPS_RF for three main reasons: (i) the MIMCAPS_MML_130E enables a closer capacitance than that which was used in the schematic. In the schematic, 10 fF capacitors are used at each one of the outputs and while the minimum value provided by MIMCAPS_RF is 104.56 fF, MIMCAPS_MML_130E presents a minimum value of 16.9884f F, as previously mentioned; (ii) a solution could be connect several MIMCAPS_RF in series. However, regarding also its capacitance

value, this option would occupy a significant area as shown in figure 6.36, since a single MIMCAPS_RF has either 10 μm in length or width, meaning a die area occupancy of nearly three times more that a standard MIMCAPS_MML_130E could involve; (iii) from the beginning it was stipulated this circuit would not be manufactured, implying a non-requirement in using only RF elements, such as the MIMCAPS_RF.

Metal-Insulator-Metal CAPacitors (MIMCAPs) are well-known for having a remarkable linearity [152], but it exhibits higher sensitivity to process variations [153] (about ±15% variation over process corners [154]). Moreover, they can be placed over active devices and therefore not occupying a large area. It would be possible to place an entire circuit under a considerable MIMCAP and not use any extra area.

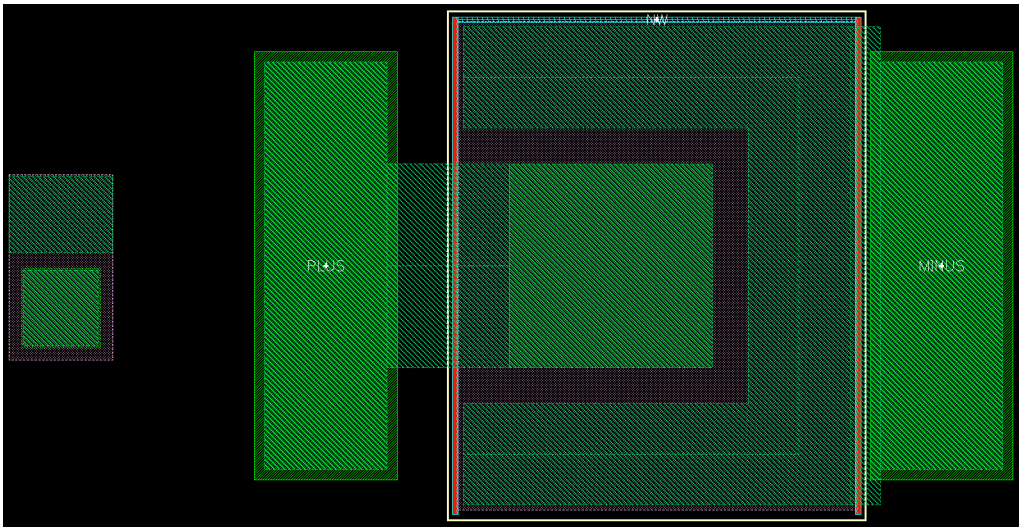

Figure 6.36: Layout of MIMCAPS_MML_130E and MIMCAPS_RF capacitors respectively side by side.

CMOS Inverter

Figure 6.37 illustrates the designed CMOS inverter, which position where transistors are aligned vertically will be maintained through the oscillator design. As discussed in subsection 3.3.2, the top device is a PMOS while the bottom MOSFET is a NMOS type. Both gates are connected to the input line. On the other hand, the output line connects to the drains of both MOSFETs.

In the CMOS inverter schematic, the drains of both devices are tied to the out node, while the sources (and bulks, or substrates) of the PMOS and NMOS are connected to V_{DD} and V_{SS}, respectively. In the layout, it is possible to treat the drain and source terminals interchangeably. Therefore, we connected the source terminal of the NMOS transistor to the drain of the PMOS and called that node out. This is only possible because the MOS transistors are physically symmetrical, despite manufacturing imperfections. This node permuting capability is a feature of the FDK.

Besides the *out* node, the *in* node of the inverter (i.e., the gate of the PMOS and NMOS transistors) was also created, in addition to V_{DD} and V_{SS}. Finally, *ro_c* and *ro_b* nodes are connected to the current source (subsection 6.2.2) so the inverter can be fed by it.

Note that the PMOS transistor, although respecting the mobility criterion, seems wide than the NMOS because there is a surrounding white edge. This edge is, in fact, a Nwell layer, which defines the Nwell of the PMOS transistor, since the technology has a p-type substrate. Hence, the bulk terminal of PMOS transistor is tied to the Nwell, whereas that of the NMOS is tied to the substrate.

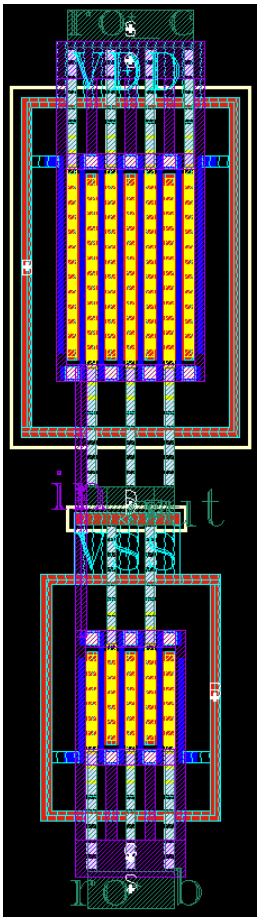

Figure 6.37: Layout of the designed CMOS inverter.

Oscillator Core and Buffer

The oscillator core consists in eight single inverters, while four inverters placed at each one of the oscillator outputs compose the buffer. This buffer is needed to control the output matching by ensuring that square waves are obtained. Furthermore, a buffer is always necessary to drive the existing capacitances in the receiver, i.e., to buffer the LO signal before providing it to the mixer. Figures 6.38 and 6.39 show the schematic and layout of the 4-stage ring oscillator, respectively. In the layout, it is possible to verify that not only all V_{DD} and V_{SS} were respectively connected, but also *ro_c* and *ro_b* outputs

which will later connect to the current source that follows.

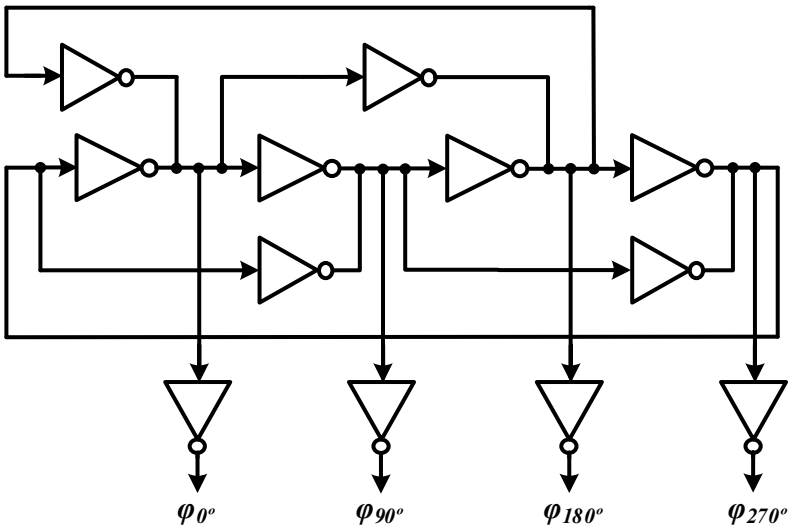

Figure 6.38: Oscillator core and buffer schematic.

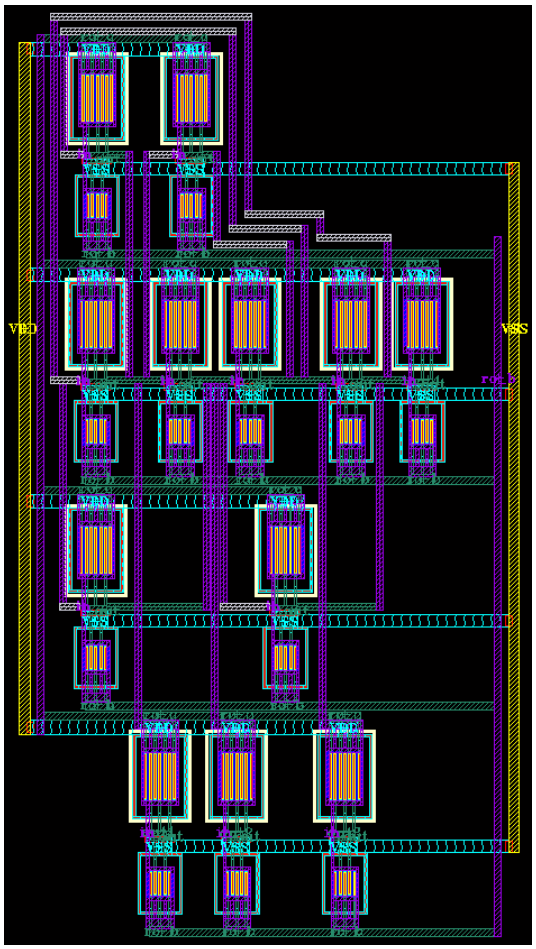

Figure 6.39: Layout of the designed oscillator core and buffer.

Current Source

The produced layout of the current source is shown in figure 6.40. It consists in a double current source with two PMOS transistors on top and two NMOS transistors below acting as a bias circuit to guarantee the proper functioning of the oscillator and its inverters. Considering the purpose of controlling the current flow through the inverter and the 1.2 V voltage supply, the average value continues to be 0.6 V. Although a current mirror is more insensitive to process variations, its transistors should be designed with large size to ensure current passes through so at least two times the technology minimum was considered ($L = 2L_{min} = 240$ nm).

Concerning the layout itself, besides the two ro_c and ro_b inputs previously explained, the current source has two outputs, idc_c and idc_b which will connect to an ideal current source. Note that this current source could be replaced for example by a simple non-ideal current source, a Cascode current mirror or a Wilson current mirror.

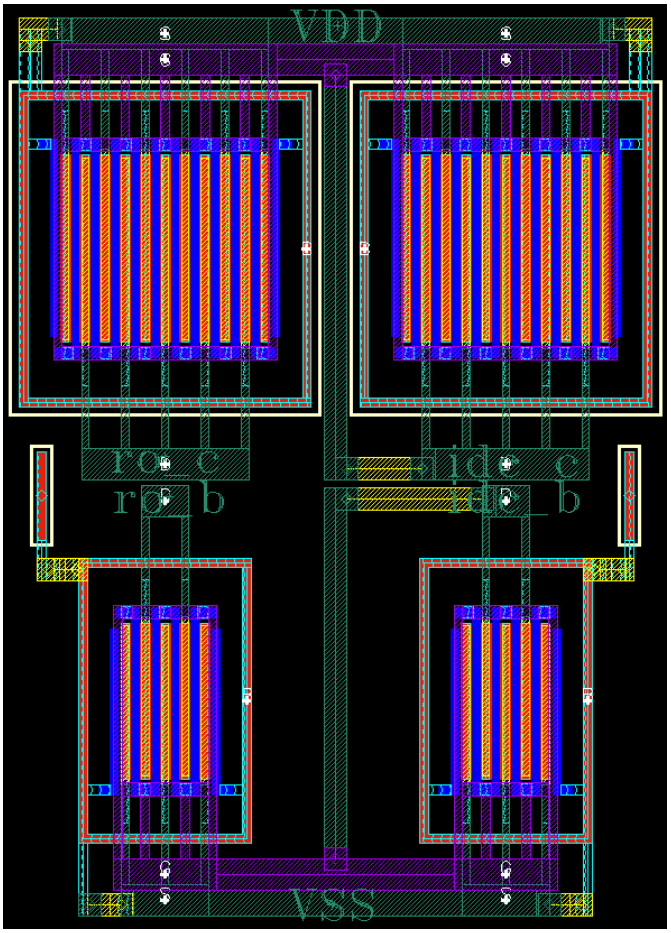

Figure 6.40: Layout of the designed current source.

4-stage Ring Oscillator

The final layout is shown in figure 6.41. All components described above constitute the 4-stage ring oscillator. Note that in this case the MIM were already incorporated to each output of the oscillator. Note also how the oscillator core's and buffer's $V_{DD}s$ and $V_{SS}s$ are connected respectively to current source V_{DD} and V_{SS}. The same goes for *ro_c* and *ro_b*. The entire circuit occupies a die area of 7.19x10^3 μm^2.

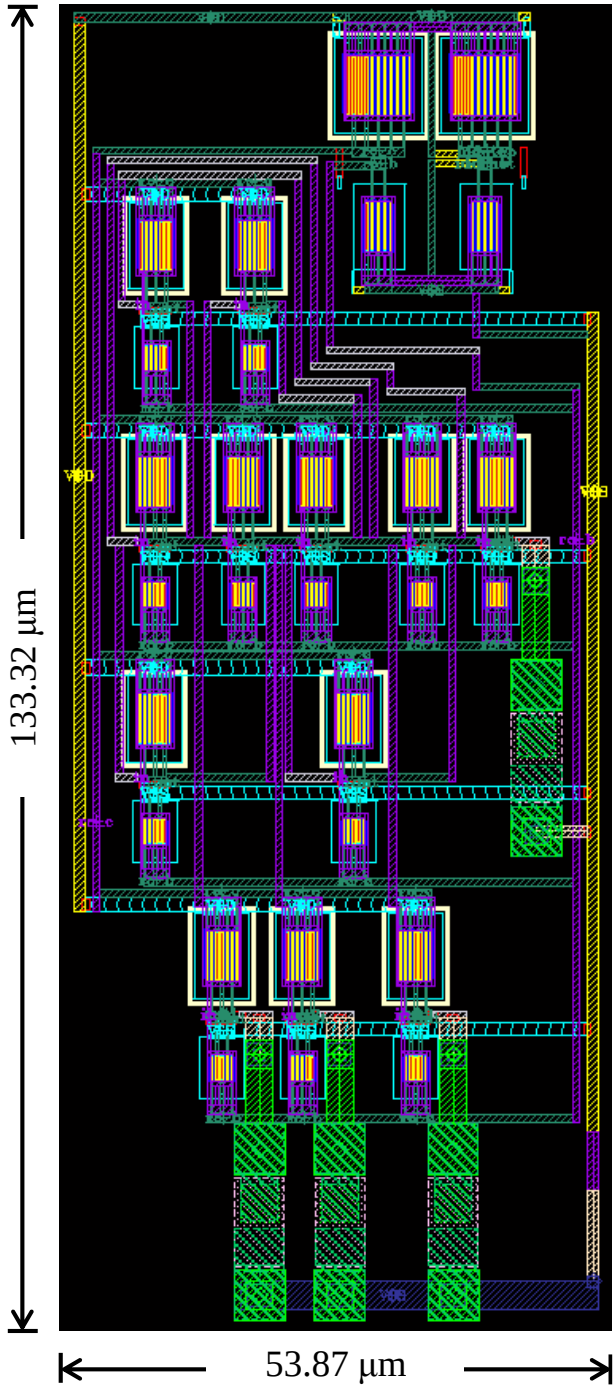

Figure 6.41: Layout of the designed 4-stage ring oscillator.

6.3 Post-layout Simulations

6.3.1 4-stage Ring Oscillator

After having the layout done, we verified if it was manufacturable (i.e., if it complied with DRC rules), if it really represented the corresponding electrical schematic (i.e., LVS check) and if the extracted layout including parasitics still delivered the same (or close) performance parameters than those achieved with the electrical schematic (i.e., we had to extract the parasitics through LPE).

Once the previous steps have been successfully completed, the extracted simulations (also known as post-layout simulations or simply post-simulations) can be done to confirm if the performance results of our circuit (4-stage ring oscillator) are close or not to those obtained using the schematic view. For a fair and accurate comparison, the post-simulations are exactly the same as the ones done in pre-layout (transient, phase-noise, PSS and Monte Carlo simulations). The idea was to fix the current value obtained from schematic simulations of the controlled current source I_f and notice how the remaining oscillator parameters change, namely the frequency of operation.

The simulation results for the fundamental frequency of 1.1 GHz are presented, followed by the results for the frequency of 1.6 GHz. As in the schematic simulations, for each of the fundamental frequencies a transient response was done in order to verify the oscillator output waveforms, proceeded by the phase-noise curve where an offset 10 MHz was considered as a benchmark value. Finally, the phase error value was obtained using the Monte Carlo simulation, which provides not only the mean value (μ), but also the standard deviation (σ) of the respective histogram.

Fundamental frequency f_{LO} = 1.1 GHz

Figure 6.42 illustrates the output waveforms of the 4-stage ring oscillator structure designed (figure 6.41) for a fundamental frequency of 1.1 GHz. The designed oscillator provides square waveforms in each of its outputs as we wanted.

Afterwards, we present in figure 6.43 the phase-noise curve for the same fundamental frequency. In this case, at 10 MHz offset the oscillator presents a phase-noise of −119.3 dBc/Hz.

Considering that the fundamental frequency is given by the 1st harmonic, the phase error due to mismatches is shown in figure 6.44. 500 Monte Carlo runs considering variations of 3σ were done. The histogram reveals a minimum phase error (μ) of 1.1851° with a standard deviation of 21.43°.

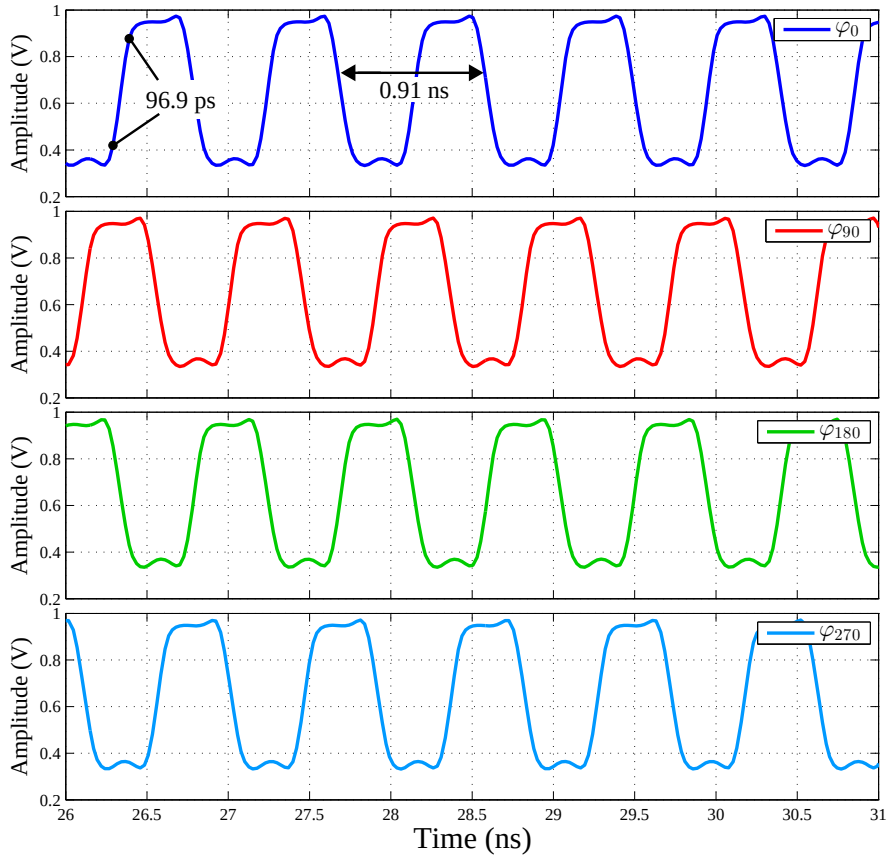

Figure 6.42: Oscillator transient response (f_{LO} = 1.1 GHz).

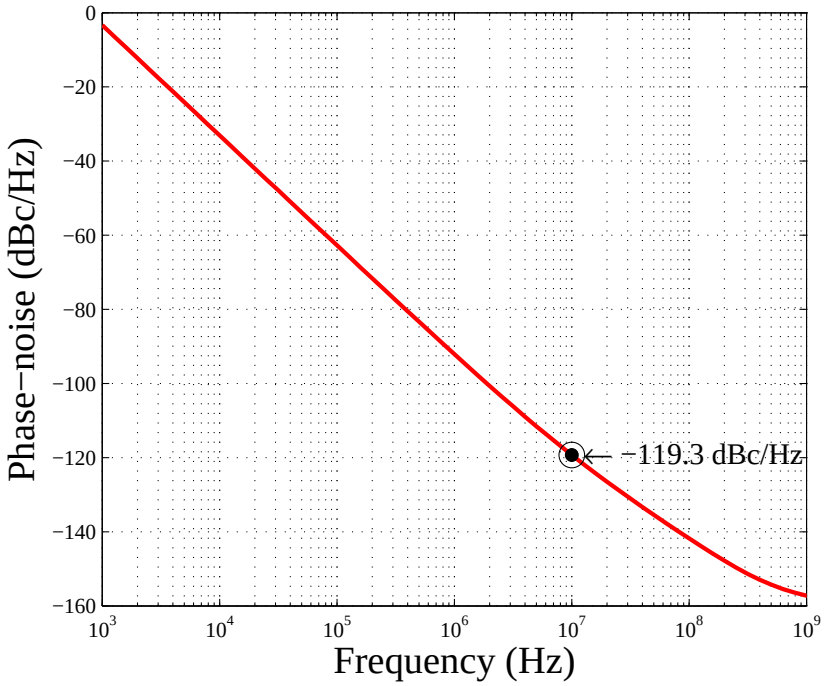

Figure 6.43: Oscillator phase-noise (f_{LO} = 1.1 GHz).

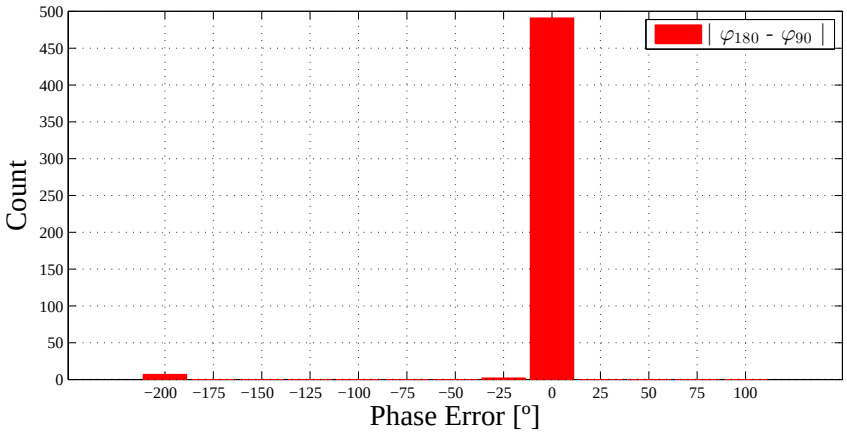

Figure 6.44: Phase error histogram ($\mu = 1.1851°$, $\sigma = 21.43°$).

Fundamental frequency $f_{LO} = 1.6$ GHz

Figure 6.45 shows the output waveforms of the designed ring oscillator shown in figure 6.41 for a fundamental frequency of 1.6 GHz. Although the frequency has increased compared to the previous case, we continue to have a similar behaviour, i.e., each output presents a square waveform as intended. The phase-noise curve is shown in figure 6.46. For a fundamental frequency of 1.6 GHz at 10 MHz offset, the oscillator produces a phase-noise of −120.7 dBc/Hz. Lastly, the phase error due to mismatches is shown in figure 6.47. Taking into account that only 1st harmonic matters, 500 Monte Carlo runs considering variations of 3σ were also contemplated here. In this case, the histogram reveals a minimum phase error of 0.8702° with a standard deviation of 11.56°.

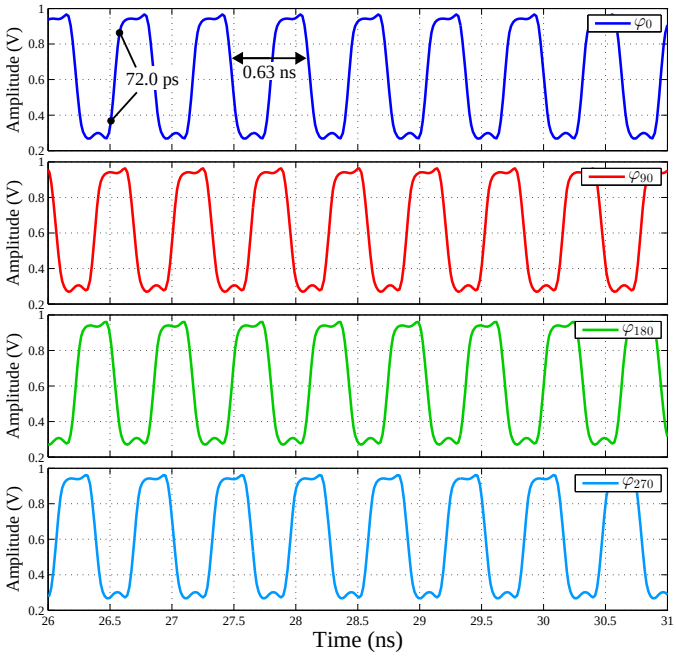

Figure 6.45: Oscillator transient response ($f_{LO} = 1.6$ GHz).

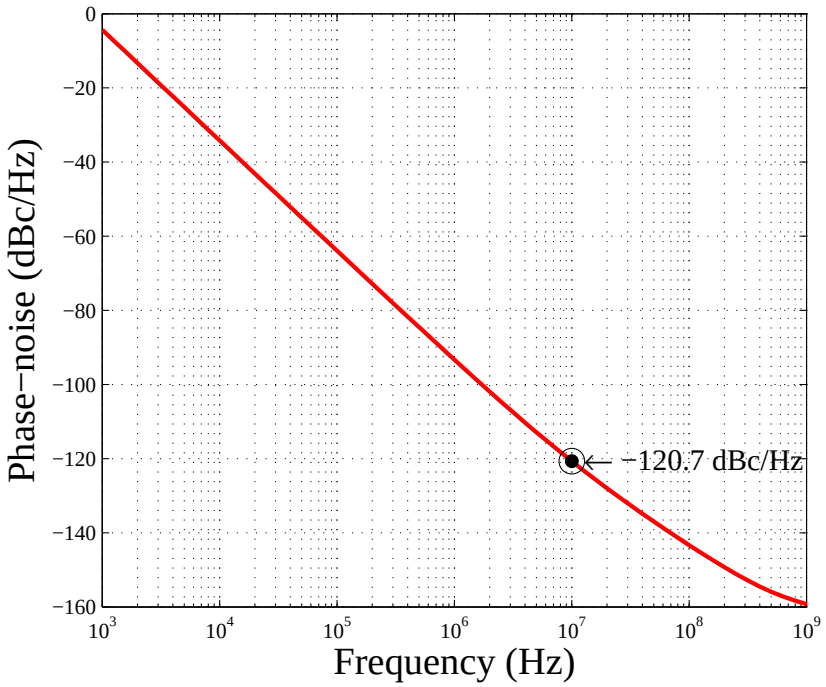

Figure 6.46: Oscillator phase-noise (f_{LO} = 1.6 GHz).

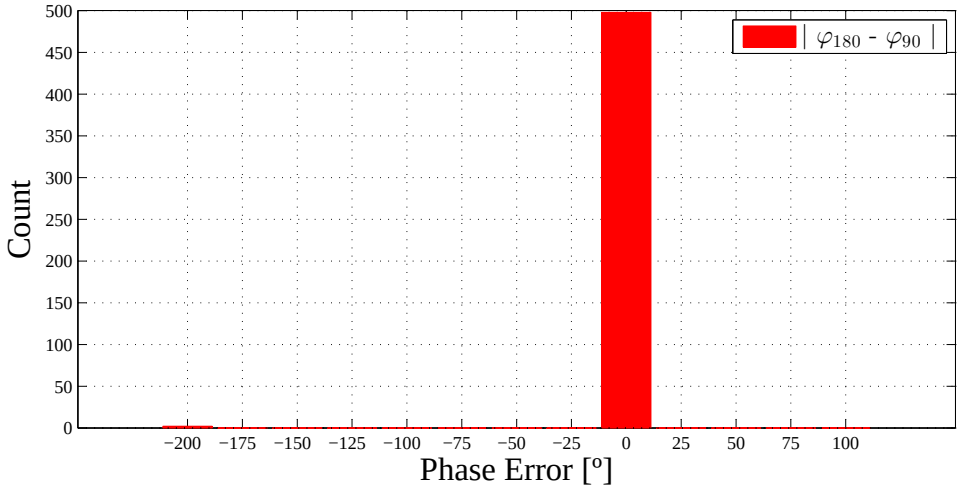

Figure 6.47: Phase error histogram (μ = 0.8702°, σ = 11.56°).

6.4 Analysis of Results and Discussion

Table 6.6 shows the pre- and post-layout results of the designed 4-stage ring oscillator. The schematic results were previously presented in subsection 6.1.3, while layout results were presented in the previous subsection. The idea was to fix the current value obtained from schematic simulations of the controlled current source I_f and notice how

the remaining oscillator parameters change, namely the frequency of operation. Therefore, fundamental frequencies of 1.1 GHz and 1.6 GHz were obtained from post-layout simulations. Consequently, the achieved rise and fall times of the output waveforms are significantly lower than the benchmark value of 100 ps assumed. Note also that in the schematic 10 fF capacitors were used, whereas in the layout we employed capacitors of 17 fF (minimum value provided by the employed technology). In addition to changing the circuit response time, this modification has an impact not only on rise/fall times, but also on the required current (I_{DC}) and thus the associated power (P_{DC}). Notice that the power consumption value (P_{DC}) is calculated over the total current (I_{DC}) flowing through the oscillator multiplied by the V_{DD} voltage supply. Finally, unlike Phase-noise ($\mathcal{L}$), there is a considerable increase of phase errors as result of layout imperfections. Although we tried to design the 4-stage ring oscillator layout as similar as possible to the electrical schematic designing it as symmetrical as possible, and produce signal paths with the same length to avoid phase errors, alongside with the lower area possible, there are naturally layout defects that contribute to an increase of phase error. Nevertheless, the phase errors obtained show that the circuit is fairly robust with respect to mismatches, presenting phase errors below 2°. For best results regarding phase-noise and phase errors, the use of the SR architecture previously presented would be a viable alternative.

The DC operating point (operating region, DC current, V_{DSsat}, g_m and g_{ds}) of the 4-stage ring oscillator schematic for the different fundamental frequencies is shown in tables 6.4 and 6.5. The transient analyses show that these parameters were in fact contemplated and well sized. Furthermore, the post-layout waveforms remain nearly the same as in the schematic, so we can consider that precise and accurate square waves are also obtained here. However, in both cases their amplitude does not reach the 1.2 V level provided by the current source due to the voltage drop in each of the transistors that compose the inverters. Again, a SR circuit is a possible solution capable of preventing this drawback. Nevertheless, the concept may be optimized and layout designers would certainly be able to provide even better results than those obtained.

Table 6.6: 4-stage ring oscillator pre- and post-layout results (Circ.: Circuit).

Circ. View	f_{LO} **(GHz)**	**Rise/Fall Time (ps)**	$\mathcal{L}$ **@ 10 MHz (dBc/Hz)**	I_f **(mA)**	I_{DC} **(mA)**	P_{DC} **(mW)**	**Phase Error (°)**
Schematic	0.6	198.2	−124.5	1.04	2.00	2.40	0.0056
Layout	1.1	96.9	−119.3	1.04	1.98	2.38	1.5979
Schematic	0.9	133.3	−124.6	1.92	3.54	4.24	0.0086
Layout	1.6	72.0	−120.7	1.92	3.45	4.14	0.8702

Regarding the ring oscillator topologies, in the 3-stage approach sinusoidal outputs were obtained. To prevent this from happening, a buffer composed of single inverters should be used. This concept was applied in the 4-stage ring oscillator structure, and

square waveforms were obtained. Their performances can be compared with others in literature using the following FoM expression [85]:

$$\text{FoM} = \mathcal{L}(f) + 10\log\left(\frac{P_{DC}}{P_{ref}}\left[\frac{\Delta f}{f_0}\right]^2\right), \tag{6.7}$$

where $\mathcal{L}(f)$ is the measured phase-noise, P_{DC} is the power consumption, P_{ref} is the reference power of 1 mW and Δf is the offset from the fundamental frequency f_0. It has been shown in [26] that the theoretical limits of FoM are −165.3 dBc/Hz so the obtained values shown in table 6.7 of this work place this ring oscillator performance near that of state-of-the-art ring oscillators. What distinguishes these oscillators from the others presented recently is the low power consumption and low area. This proves the benefits of using a fully integrated CMOS circuit, since with a small area we achieve a good FoM result, as shown in table 6.7.

Table 6.7: Comparison of state-of-the-art RC oscillators (Diff.: Differential, SE: Single-ended, Relax.: Relaxation).

Ref.	**Oscillator Concept**	f_0 **(MHz)**	P_{DC} **(mW)**	Δf **(MHz)**	$\mathcal{L}(\Delta f)$ **(dBc/Hz)**	**FoM (dBc/Hz)**
[19]	2-stage Diff. Ring	973	79.20	1.0	−117	−158
[20]	3-stage SE Ring	926	6.81	0.1	−83	−154
[21]	4-stage SE Ring	913	18.95	0.6	−117	−167
[22]	4-stage SE Ring	762	1.44	4.0	−111	−155
[23]	4-stage Diff.	900	35.66	600.0	−117	−165
[24]	5-stage SE Ring	232	1.50	1.0	−119	−164
[25]	6-stage Diff. Ring	859	10.00	1.0	−104	−153
[26]	Relax. Diff.	920	10.00	5.0	−102	−151
This work	**3-stage SE Ring**	**900**	**0.75**	**10.0**	**−119**	**−159**
	4-stage SE Ring	**900**	**4.25**	**10.0**	**−125**	**−157**

To verify the conclusions concerning the 3 and 4-phase LO generators, tables 6.8 and 6.9 provide the parameters of ring oscillator and SR approaches. Although the ring oscillator structures produce less power consumption and occupy less die area, for the same transistors dimensions it is not possible to achieve the output amplitude of 1.2 V using the ring oscillator approach, which does not happen in SR architectures. Beyond that, rise and fall times of SRs are below 53 ps demonstrating how fast the circuit response is, whereas the ring oscillator topologies exceed the benchmark value of 100 ps. Concerning phase-noise and phase errors, better (and exceptional) results were obtained using the SR architectures. Thus, table 6.10 summarizes the advantages and disadvantages of both LO generators.

Table 6.8: 3-phase LO generators parameters (RO: Ring oscillator, CS: Current Source, SR: Shift register, tran: transistors).

Circuit	f_{LO} (MHz)	Rise/Fall Time (ps)	$\mathcal{L}$ @ 10 MHz (dBc/Hz)	I_f (mA)	I_{DC} (mA)	P_{DC} (mW)	Phase Error (°)	Die Area
RO CS	600	286.0	−118.6	0.19	0.38	0.45	0.7255	10 tran
SR	600	52.3	−173.7	–	8.63	10.36	0.0002	190 tran
RO CS	900	199.8	−118.5	0.32	0.63	0.75	0.0074	10 tran
SR	900	52.3	−172.3	–	12.91	15.49	0.0008	190 tran

Table 6.9: 4-phase LO generators parameters (RO: Ring oscillator, SR50%: Shift register with 50% duty-cycle, SR25%: Shift register with 25% duty-cycle, tran: transistors).

Circuit	f_{LO} (MHz)	Rise/Fall Time (ps)	$\mathcal{L}$ @ 10 MHz (dBc/Hz)	I_f (mA)	I_{DC} (mA)	P_{DC} (mW)	Phase Error (°)	Die Area
RO	600	198.2	−124.5	1.04	2.00	2.40	0.0056	28 tran
SR50%	600	52.3	−174.7	–	12.33	14.67	0.0010	228 tran
SR25%	600	21.2	−172.0	–	13.77	16.53	0.0011	268 tran
RO	900	133.3	−124.6	1.92	3.54	4.24	0.0086	28 tran
SR50%	900	52.4	−172.3	–	18.23	21.88	0.0012	228 tran
SR25%	900	21.2	−169.8	–	20.51	24.62	0.0019	268 tran

Table 6.10: Comparison of LO generators tradeoffs (perf.: performance).

LO generator	Advantages	Disadvantages
Ring oscillator	low power consumption circuit simplicity flexible design highly integration low cost small size wide tuning range	poor frequency stability low Q poor phase-noise sensitivity to PVT variations perf. degradation as f_{LO} increases
Shift register	low phase error low phase-noise wide frequency range fast rise/fall times data storage simple operation	large die area relatively power consumption signal frequency Nf_{LO} > Clk frequency N clocks to retrieve N data bits

Chapter 7

Conclusion and Future Work

7.1 Conclusion

The continuous demand for mobile equipment in recent years of wireless communications and higher portability, along with equipment low size and cost, has increased the interest in fully integrated transceivers with very accurate quadrature signals to satisfy the requirements of today's and future mobile communication systems. Quadrature generation is a very important part of the signal processing since quadrature errors affect strongly the overall performance of RF front-ends.

In this work we study and compare two types of quadrature generators: ring oscillators and SRs. Ring oscillators are characterized by their poor frequency stability and phase-noise performance when compared with SR concept. However, SR approaches require an oscillator at N times the operating frequency. We study in detail these two architectures in terms of their key parameters: oscillation frequency, amplitude, phase relationship, phase-noise and phase error. Based on this, ring oscillators proved to be useful in biomedical applications as result of the small area they occupy associated with a low power consumption. On the other hand, due to their low phase-noise and reduced phase error, SRs are more suitable for wireless applications.

Within these LO generators, we have implemented various topologies based on their multiphase recognition. SR generators prove to be a good solution, especially when specification requirements are more stringent and demanding, although ring oscillators have a better power consumption and occupy a smaller area. Associated with low phase-noise and reduced phase error, the use of SRs are now the first choice in the design of modern transceivers.

In this thesis the design and implementation of 3 and 4-stage ring oscillators employing static single-ended inverters as delay cells are presented. Several methods were

considered to obtain not only quadrature outputs, but also square waveforms at the outputs. For these purposes, circuits acting as current source and buffer were incorporated to provide the intended quadrature square signals. A technique used to increase the operating frequency by creating feedforward paths was also considered. Both topologies were validated through simulation and the concept of the 4-stage ring oscillator is compared with the results from the post-layout simulations. Thus, these multiphase generators are described as being fully integrated with a small area, reduced power consumption and wide tuning range, and their performance are compared with other RC oscillators proposed in recent years.

Recently, an increasing interest has been devoted to SR approaches, as they are now widely used in applications in which very low phase-noise and phase error are necessary. In this work we consider 3 and 4-phase topologies, the latter with 50% and 25% duty-cycles. Simulation results of both circuits implemented in a 130 nm CMOS technology are presented. We show that fast rise/fall times under 100 ps are achievable, together with phase-noise values of −170 dBc/Hz at 10 MHz offset (considering an ideal high frequency generator). Both circuits are robust with respect to mismatches, showing phase errors below 0.002°. Therefore, SR generators can be a suitable alternative to ring oscillators and we hope the advantages of a SR will be larger as technology advances.

7.2 Future Work

Some of the recommendations left that could be useful to supplement this work include:

- The layout design of both SR approaches (50% and 25% duty-cycles) and compare them with the analogous ring oscillator produced.
- The design of a 8-phase SR and its associated analysis.
- The application of differential signalling to certify possible improvements in the architectures present through this work.
- A meticulous study of circuits behaviour regarding the regions where transistors should operate.
- The optimization of the 4-stage ring oscillator die area taking into account precise and refined layout strategies.
- A further investigation of how can we reduce the existing number of components in the SR architectures conceived, and therefore the consumption associated.
- The inclusion of the 3 and 4-phase single-frequency LO generators employing SRs to RF front-end receivers.

- The manufacture of the oscillators in study to validate the obtained results through measurements.
- The design of the oscillators analysed in a lower CMOS technology to explore if a better compromise between cost, area, power and performance could be achieved.
- Investigate concrete applications for the oscillators of this work, namely in GSM, WMTS and ISM bands, which would require possible changes in our circuits, according to the specifications of each application.

The SR approach is a work in progress since it can still be improved, intending to a more competitive solution. This thesis hopefully will inspire more ideas and more circuits where this topology can be applied. The increasing interest in SRs is the proof of how much potential this configuration has, and therefore it must be contemplated.

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Appendix

Performance of the Individual Blocks

Simple simulations of the critical blocks are presented here. The purpose of this appendix is to verify if the response of all circuit blocks match with their truth tables. Therefore, this appendix is structured as follows: first, the simulation result of the only structure used in the ring oscillator topologies: the single-ended CMOS inverter. Then, the transient responses of the logic gates AND and NAND are presented. The single D-FF simulation is illustrated, followed by the response of the dual D-FF structure adopted.

A.1 CMOS Inverter

The function of a inverter logic gate (figure 5.1) is to output the opposite of the input as shown in table A.1. This logical negation can be noticed in figure A.1. Constructed using two complementary transistors in a CMOS configuration, the CMOS inverter is perhaps the most basic of all the logical gates in digital electronics since it outputs a voltage (V_{out}) representing the opposite logic-level to its input (V_{in}).

Table A.1: Inverter truth table.

A	$\overline{\mathbf{A}}$
0	1
1	0

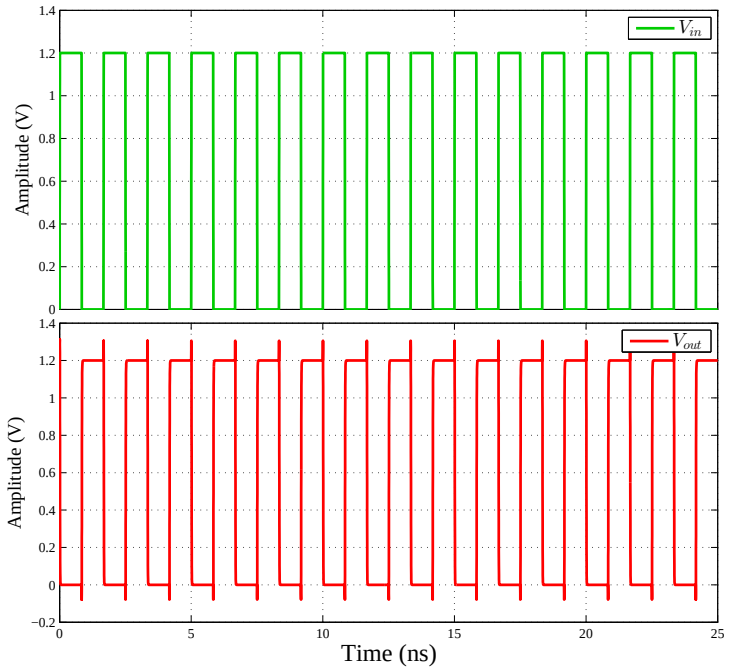

Figure A.1: Inverter transient response.

A.2 AND Logic Gate

The AND gate shown in figure 5.8 is a basic digital logic gate that implements logical conjunction. It gives a HIGH output (V_{out}) only if all its inputs (V_1 and V_2) are HIGH. If neither or only one input is HIGH, a LOW output results. This behaviour is coherent with what figure A.2 illustrates and also with the AND truth table (table A.2).

Table A.2: AND truth table.

A	B	A·B
0	0	0
0	1	0
1	0	0
1	1	1

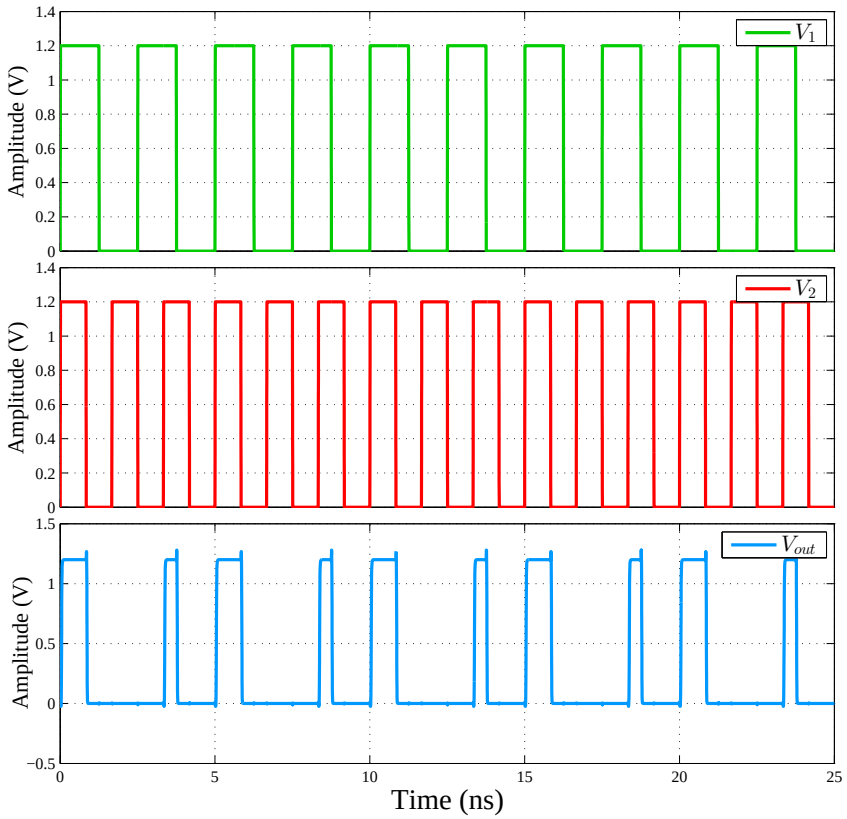

Figure A.2: AND transient response.

A.3 NAND Logic Gate

A NAND gate (figure 5.4(A)) is an inverted AND gate. This logic gate produces an output (V_{out}) which is false only if all its inputs (V_1 and V_2) are true. Thus, its output is complement to that of the AND gate. A LOW output results only if both the inputs to the gate are HIGH. If one or both inputs are LOW, a HIGH output results. While table A.3 shows the truth table of a NAND logic gate, figure A.3 illustrates the transient response of the designed NAND gate.

Table A.3: NAND truth table.

A	B	A·B
0	0	1
0	1	1
1	0	1
1	1	0

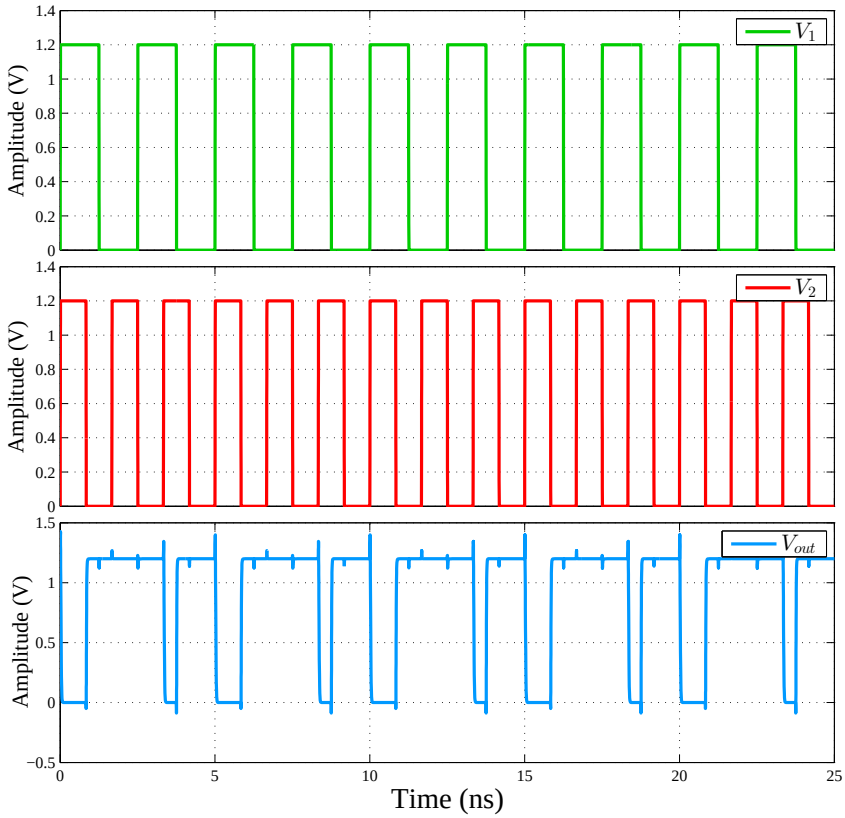

Figure A.3: NAND transient response.

A.4 Single D-FF

The D-FF presented in figure 5.4(B) captures the value of the *D*-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the *Q* output. At other times, the output *Q* does not change. Table A.4 and figure A.4 illustrate its behaviour. This type of FF can be viewed as a memory cell, a zero-order hold or a delay line.

Table A.4: D-type flip-flop truth table.

Clk	D	Q
0	0	Q
0	1	Q
1	0	0
1	1	1

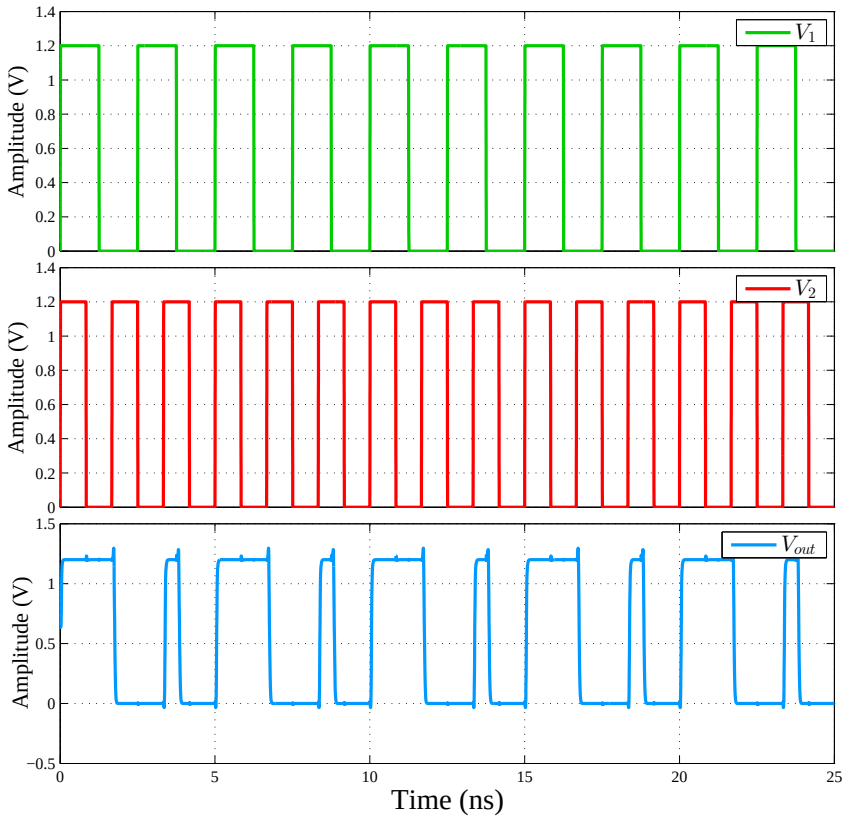

Figure A.4: Single D-FF transient response.

A.5 Dual D-FF

For a proper operation of the D-FF, its *D* input signal must be stable before the clock starts to switch. When the clock switches, the logic value on the *D* node is transferred to the *Q* output. This means the timing of the FF output is determined by the clock, so the *D* input signal only acts as an "enabler" of a transition. Therefore, to D-FF work properly, it must be designed with two master/slave connected as latches as exposed in figure 5.5, where the first latch is only an enabler [38]. Figure A.5 shows how it behaves.

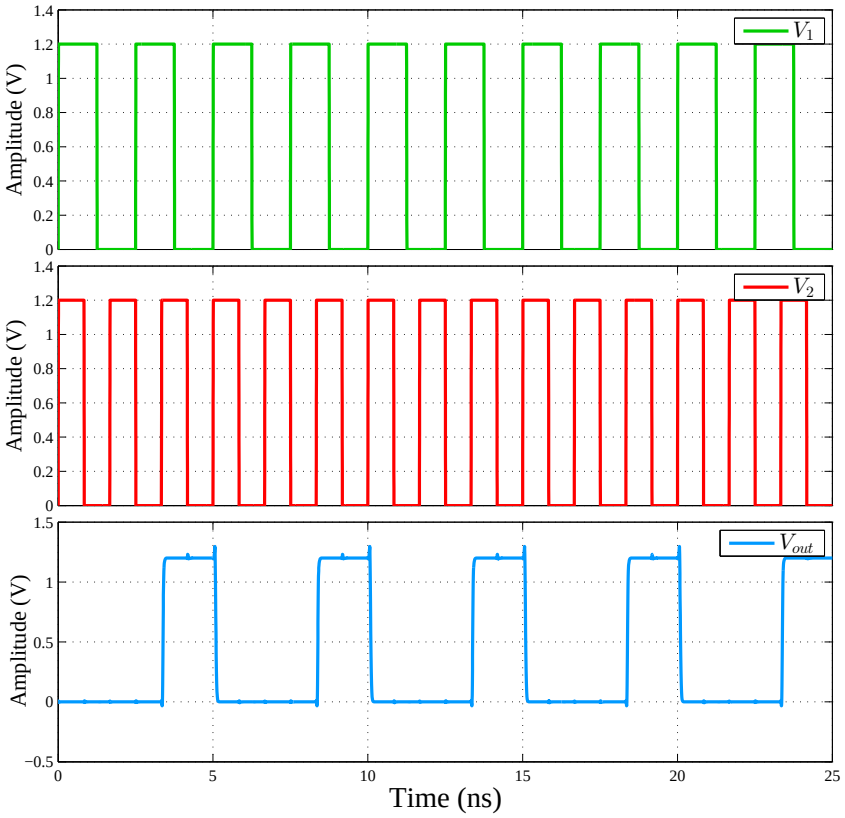

Figure A.5: Dual D-FF transient response.

Appendix B

Simulations Description

Circuit simulation plays a key role in the design process of today's electronic circuits. The field of circuit simulation has seen exciting development ever since the advent of ICs. Modern integrated circuits continually challenge circuit simulation algorithms and implementations with the various verification problems they pose. As a VLSI technology has advanced to the nano-scale regime, it is crucial to efficiently simulate all the important new physic effects coming shrinking devices to the design and verification of future VLSI systems.

Circuit simulation is basically a computer program predicting the behaviour of a real circuit. It replaces real components with idealized electrical models. Its practical feedback allows the designer to determine the correctness and efficiency of a design before the system is actually constructed. Consequently, the user may explore the merits of alternative designs without physically building the systems. By investigating the effects of specific design decisions during the design phase rather than the construction phase, the overall cost of building the system diminishes significantly.

Another benefit of simulators is that they permit system designers to study a problem at several different levels of abstraction. By approaching a system at a higher level of abstraction, the designer is better able to understand the behaviours and interactions of all the high level components within the system and is therefore better equipped to counteract the complexity of the overall system. This complexity may simply overwhelm the designer if the problem had been approached from a lower level. As the designer better understands the operation of the higher level components through the use of the simulator, the lower level components may then be designed and subsequently simulated for verification and performance evaluation. The entire system may be built based upon this "top-down" technique. This approach is often referred to as hierarchical decomposition and is essential in any design tool and simulator which deals with the construction

of complex systems.

This appendix presents a description of each of the simulations realized throughout this work, among which stand out the PSS and Pnoise, able to provide the phase-noise inherent in the oscillator, and the Monte Carlo analysis, which provides the phase error value associated with the oscillator.

B.1 DC Analysis

In most practical electronic circuits a constant steady state resulting from DC excitations is the most commonly used simulation mode. If system performance relies on instantaneous signal variations then usually there is a reference signal impressed by the energy sources. This reference signal provides a background for the time-varying signals. Furthermore, it is important to know the required power supply and its limits, the current consumption and to be sure that all devices are working in the safe region without exceeding their normal ratings.

Similarly, systems operating with time-varying signals of a larger dynamic range covering a wide range of non-linear characteristics of the system elements, require a sequence of DC simulations with an excitation changing gradually. This so-called DC sweep or multipoint DC analysis examines the dependence of responses on the excitations, assuming that the latter vary slowly enough to neglect reactive effects. The swept parameter can be circuit temperature, a device instance parameter, a device model parameter, a netlist parameter, or a subcircuit parameter for a particular subcircuit instance. Such analysis is useful for analog and digital (logic) circuits with large signals.

It is essential for a system designer to efficiently calculate the bias since the design process for ICs always starts with the DC analysis and verification of DC signals. Moreover, the DC analysis is an introduction to other types of circuit analyses, such as the transient analysis, which will be presented in the following subsection. DC analysis is automatically performed prior to a transient analysis to determine the transient initial conditions.

B.2 Transient Analysis

The transient analysis computes the transient response of the circuit over a specified time interval. The purpose of a transient response is to compute the behaviour of a structure subjected to time-varying excitation. The transient excitation is explicitly defined in the time domain.

Some circuits, such as oscillators or circuits with feedback, do not have stable operating point solutions. For these circuits, either the feedback loop must be broken so that a DC operating point can be calculated or the initial condition must be provided in the simulation input. If an initial condition is not specified, the analysis starts from the DC

steady-state solution. It is also possible to influence the speed of the simulation by setting parameters that control accuracy requirements and the number of data points saved.

Notwithstanding the possibility of setting transient analysis speed and accuracy parameters individually, three different numerical methods can be defined to control transient analysis accuracy: liberal, moderate and conservative. At liberal, the simulation is fast but less accurate. The liberal setting is suitable for digital circuits or analog circuits that have only short time constants. At moderate, the default setting, simulation accuracy approximates a SPICE2 style simulator. At conservative, the simulation is the most accurate but also slowest. The conservative setting is appropriate for sensitive analog circuits.

Although a transient analysis might provide a convergent DC solution, the transient analysis itself can still fail to converge. The convergence failure might be due to stated initial conditions that are not close enough to the actual DC operating point values.

B.3 PSS Analysis

PSS analysis is a large-signal analysis that directly computes the periodic steady-state response of a circuit at either a given fundamental frequency or the corresponding steady-state analysis period. With PSS, simulation times are independent of the time constants of the circuit, so PSS can quickly compute the steady-state response of circuits with long time constants, such as high-Q filters and oscillators.

Sweep frequency or other variables using PSS is also possible. After completing a PSS analysis, the Spectre® RF simulator can model frequency conversion effects by performing one or more of the periodic small-signal analyses: Periodic AC (PAC) analysis, Periodic S-Parameter (PSP) analysis, Periodic Transfer Function (PXF) analysis and Periodic Noise (Pnoise) analysis. This last analysis will be presented in the next subsection.

B.4 Pnoise Analysis

After the PSS analysis computes a periodic solution, this analysis linearises the circuit about the PSS and performs a small-signal analysis. The small-signal analysis computes the total-noise spectral density at the output.

The Pnoise analysis is similar to the conventional noise analysis (which linearises the circuit about the DC operating point and computes the total-noise spectral density at the output, where the output can be either a voltage or a current) except that it models frequency conversion effects. It can compute the phase-noise of oscillators as well as the noise behaviour of mixers, switched-capacitor filters, chopper-stabilized amplifiers, and other similar circuits.

First, the circuit is linearised using the PSS operating point. The periodically time-varying qualities of the linearised circuit create the frequency conversion. Then the Pnoise

analysis simulates the effect of a periodically time-varying bias point on component-generated noise.

Initially, PSS computes the response to a large periodic signal such as a clock or a LO. The subsequent Pnoise analysis computes the resulting noise performance.

In periodic systems, there are two effects that act to translate noise in frequency. First, for noise sources that are bias dependent, such as shot noise sources, the time-varying operating point modulates the noise sources. Second, the transfer function from the noise source to the output is also periodically time-varying and modulates the noise source contribution to the output.

B.5 Monte Carlo Analysis

Small random variations occur during the manufacturing of circuit devices, resulting in behavioural differences between identically designed devices. These variations, or device mismatches, are often dismissed as an unimportant or difficult aspect of circuit design. This is not surprising because it is challenging to analytically predict the behaviour of any non-trivial circuit due to the accumulation of the mismatch errors from individual devices. However, the physical aspects of device mismatch are well understood and quantitative models that accurately predict the device mismatch of individual devices exist [155–157]. Monte Carlo simulation can be used to investigate how the individual mismatches of a circuit may accumulate and affect the circuit as a whole. This is achieved by analysing a large set of circuit instantiations, whose circuit devices have each been individually randomized in accordance to the mismatch model of the particular device type [158].

Device mismatches are a result of manufacturing variations and can be observed lot to lot, wafer to wafer, die to die and device to device. Variations can be characterized in many different ways [155–157]. Unlike resistors, inductors and capacitors, modeling the variation of MOSFET devices is more difficult due to their non-linear and multi-terminal nature. MOSFET devices have multiple parameters that vary, a dependence on bias for the current and voltage errors, and an area dependence for their variations, which cannot be modelled by a simple substitution of device values. There has been extensive research done on modelling the mismatch behaviour of MOSFETs [155–157].

All existing components in a circuit have tolerances and so the combined effect of all the component tolerances may result in a significant deviation from the expected circuit response. What the Monte Carlo analysis does is to provide statistical data predicting the effect of randomly varying model parameters or component values (variance) within specified tolerance limits. The generated values follow a statistically defined distribution. The circuit analysis (DC, AC or transient) is repeated a number of specified times with each Monte Carlo run generating a new set of randomly derived component or model parameter values. The greater the number of runs, the greater the chances that every component value within its tolerance range will be used for simulation. It is not uncommon

to perform hundreds or even thousands of Monte Carlo runs in order to cover as many possible component values within their tolerance limits. Monte Carlo, in effect, predicts the robustness or yield of a circuit by varying component or model parameter values up to their specified tolerance limits.

The model parameter deviations from the nominal values up to the tolerance limits are determined by a probability distribution curve. By default, the distribution curve is uniform; that is, each value has an equal chance of being used. The other option is the Gaussian (or normal) distribution, which is the familiar bell-shaped curve shown in figure B.1, commonly used in manufacturing. Component values are more likely to take on values found near the center of the distribution compared to the outer edges of the tolerance limits [159].

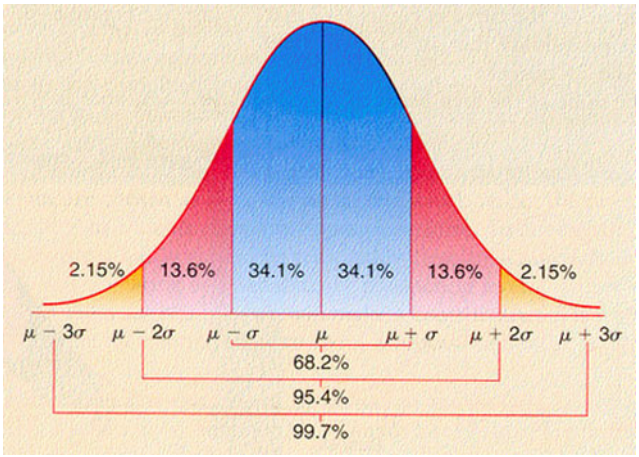

Figure B.1: Gaussian (or normal) distribution [160].

Appendix C

Published Paper

"Wideband CMOS RF Front-End Receiver with Integrated Filtering"

22nd International Conference *"Mixed Design of Integrated Circuits and Systems"* (MIXDES), 2015

Wideband CMOS RF Front-End Receiver with Integrated Filtering

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***Abstract*—A wideband CMOS receiver front-end for radio applications operating between 300 MHz and 900 MHz is presented. In order to obtain channel selection with image-rejection and out-of-band interferers attenuation, both low-noise amplifier (LNA) and mixer incorporate a N-Path signal processing technique. The effectiveness of this N-Path filtering is investigated by comparing distinct combinations of clock phases and respective duty cycle. Using a standard 130 nm CMOS technology and a supply voltage of 1.2 V, it was possible to obtain a voltage gain greater than 28 dB, a noise figure (NF) lower than 6.05 dB and IIP3 $>$ -1.54 dBm.**

***Index Terms*—RF CMOS, high-Q bandpass filter, noise cancellation, N-path filter, SAW-less, tunable LNA, passive mixer.**

I. Introduction

With the expansion of multi-standard radio communications, a greater importance is given to out-of-band interferers due to their negative impact on the receiver's performance. A narrowband receiver can solve this problem by using external filters, which are tuned for specific frequencies. However, in wideband receivers this method would require the use of several filters that are selected for each channel. An alternative to external filters is to embed passive filtering on the LNA [1]. This results in a tunable narrowband LNA able to operate over a wide range of frequencies. Interestingly, this technique can also be used on passive mixers, granting the same filtering advantages.

In this paper a wideband CMOS RF receiver analog front-end (AFE) with integrated filtering is presented, as shown in Fig. 1. It consists of a cascode balun-LNA with embedded N-path filtering. The N-path filter at the input of the LNA is single-ended, which also contributes to the input impedance matching. Also, a differential N-path filter is used to increase the out-of-band interferers attenuation. A current-driven passive mixer is connected to the LNA output to perform down-conversion of the RF signal to an intermediate frequency (IF) and to filter the RF signal.

Both filters and the mixer are controlled by a multi-phase clock generated by the local oscillator (LO). The performance of the N-path filters is very depended of the number of phases and duty cycle. Therefore, to optimize the trade off between out-of-band filtering, gain, noise and harmonic rejection, distinct phase schemes are investigated.

The paper is structured as follows. In Section II the N-path technique is reviewed and applied to high-Q bandpass filtering (BPF) and mixing. These high-Q BPFs are embedded in the LNA described in Section III. The full AFE is presented and studied in Section IV. Finally, section V discusses the overall obtained results.

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II. N-Path Filtering and Mixing

A N-path filter technique can be implemented by using the simple configuration shown in Fig. 2. The MOS transistor, acting as a switch, commutates the RF current to the baseband impedance Z_{BB}, which consists in a simple capacitor (C_{BB}) [2]. It can be proved [3] that this topology converts a low-pass baseband impedance to a high-Q BPF, with the center frequency set by the clock frequency. Moreover, due to the passive nature of the circuit it generates no flicker noise [1], [4].

Considering a M-phase clock, the input impedance of the N-Path filter of Fig. 2 is given by [5]

$$Z_{RF}(\omega) \cong R_{SW} + M \sum_{k=-\infty}^{\infty} |a_k|^2 Z_{BB}\left(f - f_{LO}\right) \qquad a_k = \frac{sin\left(k\pi/N\right)}{k\pi}. \tag{1}$$

Equation (1) assumes a duty cycle of T_{LO}/M, where T_{LO} is the clock period. In order to understand the better combination between the number of phases and the required duty cycle, four options have been used, as shown in Table I.

TABLE I
Tested LO parameters

	Number of Phases	Duty Cycle	Phase Ratio	Phase Delay
1	3	1/2	1:2:1	-60º, 0º, 60º
2		1/3		
3	4	1/4	1:1:1:1	0º, 90º, 180º, 270º
4		1/2		

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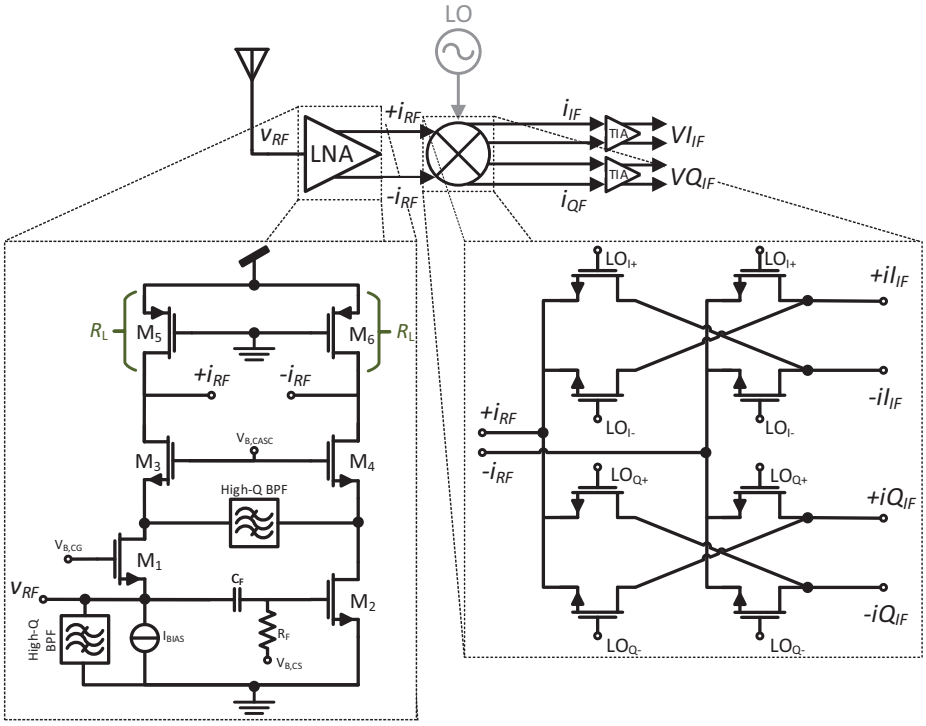

Fig. 1. RF receiver front-end.

A. *Single-ended input filter*

By applying (1) on the circuit of Fig. 2, and assuming that all the MOS switches are ideal, the filter input impedance Z_{RF} is given by the simplified expression [4], [6]

$$Z_{RF}(\omega) \cong R_{SW} + \frac{M}{\pi^2} sin^2 \frac{\pi}{M} \times \left[Z_{BB}\left(\omega - \omega_{LO}\right) + Z_{BB}\left(\omega + \omega_{LO}\right) \right]. \quad (2)$$

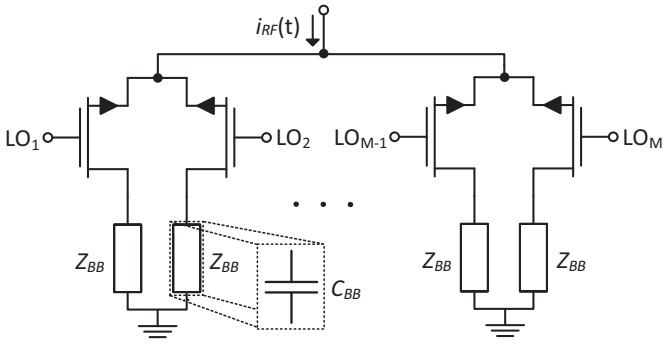

Fig. 2. Single-ended M-phase high-Q BPF.

Equation (2) shows a high-Q band pass frequency response around ω_{LO}, helping on filtering of out-of-band interferers. The single-ended version was designed and simulated in CMOS 130 nm technology. 5 pF capacitors were chosen as C_{BB} and the NMOS switches have a width of 3.6 μm and the minimum length allowed by the technology (120 nm). Fig. 3 shows the obtained filter results for different LO conditions, tested at 600 MHz.

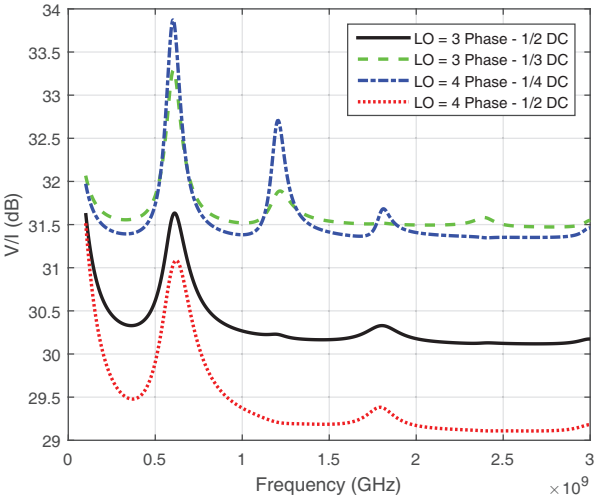

Fig. 3. Single-ended high-Q BPF MAG for multiple LO phases and duty cycle.

It was observed that the 4-phase LO with a $1/4$ duty cycle presents better bandpass results for the selected frequency, but it does not cancels the second harmonic, contrary to the 3-phase LO with a $1/3$ duty cycle. Both 3-phase with a $1/2$ duty cycle and 4-phase with a $1/2$ duty cycle do not have the same filter sharpness, but suppress the even harmonics.

By analysing the results of Table II and Fig. 4, it is possible to conclude that the same envelope filter response is shifted between 450 and 900 MHz for 4-phase with a $1/4$ duty cycle. Fig. 5 shows that the filter has a high input reflection behaviour for frequencies near f_{LO}, not interfering with the desired baseband signal.

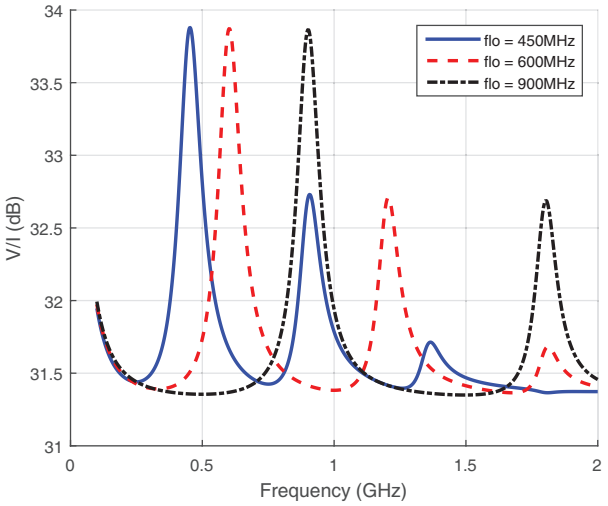

Fig. 4. Single-ended high-Q BPF MAG for multiple values of f_{LO} operating with 4-phase and $1/4$ duty cycle.

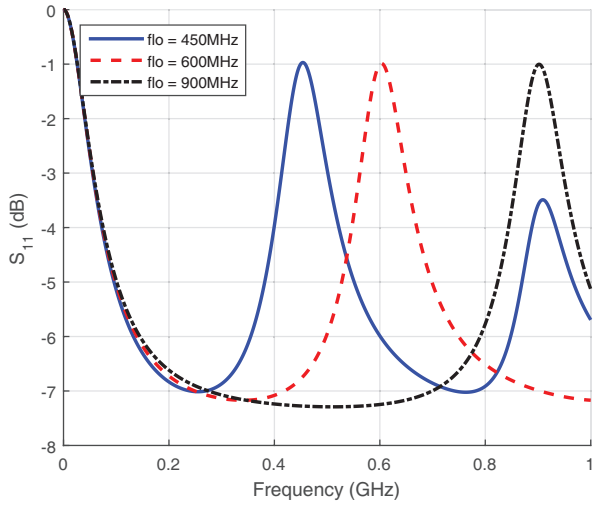

Fig. 5. Single-ended high-Q BPF S_{11} for multiple values of f_{LO} operating with 4-Phase and $1/4$ duty cycle.

TABLE II
PAC RESULTS OF SINGLE-ENDED HIGH-Q BPF WITH DIFFERENT LO CONFIGURATIONS

LO Configuration	PAC [dB]		
	450 MHz	600 MHz	900 MHz
3-phase $1/2$ duty cycle	31.64	31.6	31.57
3-phase $1/3$ duty cycle	33.29	33.28	33.27
4-phase $1/4$ duty cycle	33.87	33.87	33.86
4-phase $1/2$ duty cycle	31.08	31.02	30.97

B. Diferential input filter

On this version the number of switches are doubled but the Z_{BB} can be shared, as shown in Fig. 6. By analyzing the respective input impedance, expressed by (3), it is clear that the differential configuration also cancels all the even harmonics and has twice the input impedance, comparing with the single-ended version.

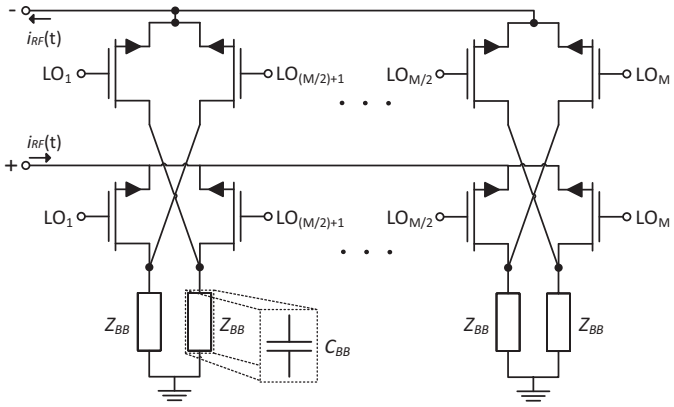

Fig. 6. M-phase differential high-Q BPF.

$$
\begin{aligned}
Z_{in}(\omega) = {} & 2R_{SW} \\
& + \frac{2M}{\pi^2}\sin^2\left(\frac{\pi}{M}\right) \\
& \quad \times [Z_{BB}(\omega-\omega_{LO}) + Z_{BB}(\omega+\omega_{LO})] \\
& + \frac{2M}{9\pi^2}\sin^2\left(\frac{3\pi}{M}\right) \\
& \quad \times [Z_{BB}(\omega-3\omega_{LO}) + Z_{BB}(\omega+3\omega_{LO})] \\
& + \frac{2M}{25\pi^2}\sin^2\left(\frac{5\pi}{M}\right) \\
& \quad \times [Z_{BB}(\omega-5\omega_{LO}) + Z_{BB}(\omega+5\omega_{LO})] \\
& + \ldots
\end{aligned}
\tag{3}
$$

The differential version was also simulated using the same component sizes and the same LO parameters as in the single-ended version. The obtained results are shown in Fig. 7. By comparing each topology it is easy to conclude that the 4-phase with a $1/4$ duty cycle has the best results, as can be confirmed in Table III and Fig. 8.

Because the filter sharpness increases with the size of the baseband capacitor C_{BB}, this version allows to get a sharper filter and to save chip area.

TABLE III
PAC RESULTS OF DIFFERENTIAL HIGH-Q BPF WITH DIFFERENT LO CONFIGURATIONS

LO Configuration	PAC [dB]		
	450 MHz	600 MHz	900 MHz
3-phase $1/2$ duty cycle	36.9	36.84	36.78
3-phase $1/3$ duty cycle	38.22	38.19	38.16
4-phase $1/4$ duty cycle	40.16	40.15	40.15
4-phase $1/2$ duty cycle	37.29	37.23	37.18

C. Current-driven Passive Mixer

The designed mixer is a doubled-balanced current-driven passive mixer, as shown in Fig. 1. Being a passive element, it

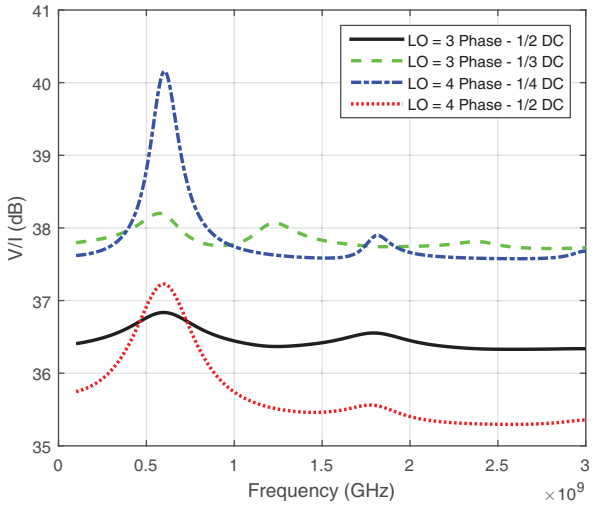

Fig. 7. Differential high-Q BPF MAG for multiple LO phases and duty cycle.

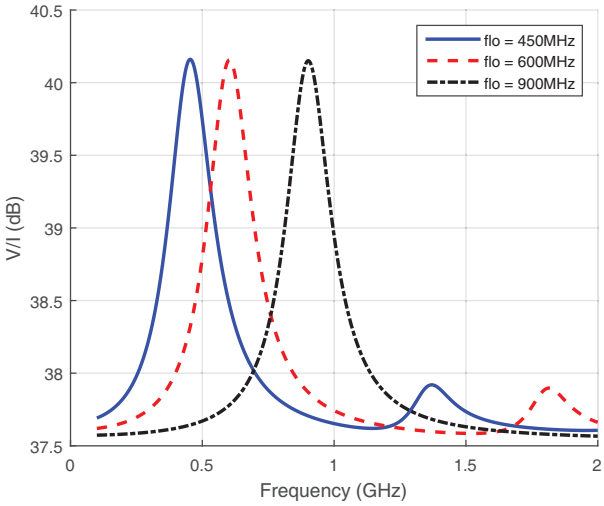

Fig. 8. Differential high-Q BPF MAG for multiple values of f_{LO} operating with 4-phase and $1/4$ duty cycle.

has a voltage gain lower than one and its noise contributions are low [2]. It has the same properties as the filters explained above, allowing to filter out-of-band blockers while converting the RF signal to an IF. Also, since the mixer is current-driven, it is very linear because there is no voltage variation in the signal path [7]. The mixer's output is connected to a TIA, with a transimpedance gain of A_{vi} = 100 kΩ, lowering the switches V_{DS} fluctuation and helping on the circuit's linearity.

The mixer's biasing was done by matching its input impedance to the LNA output impedance (1.4 kΩ), allowing a good linearity and maximizing its notch filter behaviour, as referred in [2]. The mixer was simulated for different LO parameters with worse results, proving that a 4-phase LO with $1/4$ duty cycle is the best option for getting good results for this mixer.

Fig. 9 shows the mixer's input impedance (using PSS and

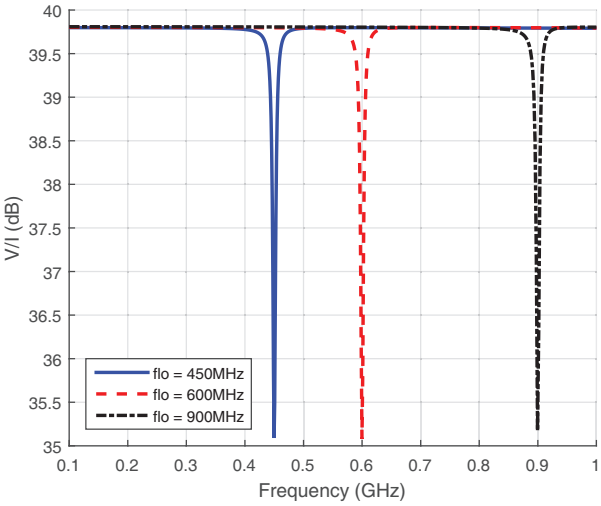

Fig. 9. Mixer's input impedance with f_{LO} = 900 MHz.

PSP analysis), where it is possible to verify that it is low for frequencies near f_{LO}. The mixer's noise figure (NF) was obtained using PSS and PNoise analysis. A minimum NF of 4.5 dB was achieved, as shown in Fig. 10.

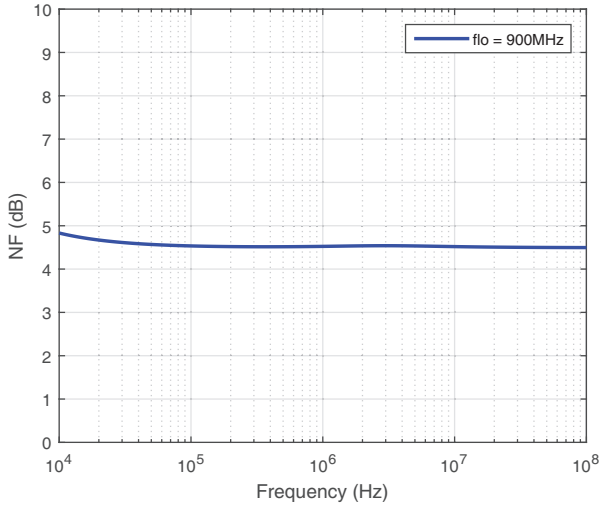

Fig. 10. Mixer's noise figure with f_{LO} = 900 MHz.

Regarding IIP3, PSS and PAC analysis were chosen, with an LO frequency of 900 MHz and two pure sine waves spaced apart 20 MHz, f_1 = 901 MHz and f_2 = 921 MHz. Using these simulation parameters it was possible to obtain an IIP3 around +17.6 dBm.

III. Balun-LNA with Embedded N-path Filtering

The designed LNA, based on [8], consists of a two stage balun with a differential cascode at the output, as shown in Fig. 1. The first stage is a common gate (CG), which grants a good input impedance matching for a wide frequency range. Besides the differential output guarantee a higher gain, it cancels the thermal noise produced at the CG by appearing in common

mode at the differential output, since the common source (CS) stage inverts the signal phase. A full noise cancellation is only possible if there is a good gain match between the two stages.

To increase the LNA performance the traditional resistors were replaced by two PMOS transistors, M_5 and M_6, operating at the triode region, as described in [3]. By using this technique it is possible to achieve a higher impedance with the same voltage drop, reducing the circuit's NF and increasing the voltage gain, as shown in (4).

$$A_v \approx g_{m,CG} \times R_L + g_{m,CS} \times R_L \approx 2 \times g_{m,CG} \times R_L \quad (4)$$

At the LNA input it was used a single-ended version of the high-Q BPF studied in Sec. II-A, and at its output the differential version, explained in Sec. II-B, was integrated in order to remove undesired signals outside of the desired channel. Since the LNA input impedance matching is given by the parallel of the CG transistor's input impedance with the single-ended filter's impedance, and the filter's impedance is ideally infinity [2], the filter has not much impact on signals at frequencies near to f_{LO}. For frequencies far from f_{LO}, the parallel is equivalent to R_{SW}, attenuating undesired out-of-band interferers. Considering that the LNA input impedance as an equivalent resistance R_{LNA}, the filter bandwidth is given by [8]

$$\omega_{3dB} \cong \frac{1}{M(R_{LNA} + R_{SW})C_{BB}}. \quad (5)$$

For the differential filter, it was used the 4-phase LO with a $1/4$ duty cycle and for the single-ended version all the topologies studied in Sec. II were simulated. The obtained results are shown in Table IV, from which it is possible to conclude that the best results for the LNA with integrated filtering were obtained for the 4-phase LO with a $1/4$ duty cycle.

TABLE IV
LNA SIMULATION RESULTS WITH DIFFERENT LO TYPES FOR THE SINGLE-ENDED BPF, WITH f_{LO} = 900 MHZ.

LO Configuration	Volt. Gain [dB]	NF [dB]	Z_{11} [Ω]	S_{11} [dB]
3-phase $1/2$ duty cycle	26.94	3.143	38.404	-15.86
3-phase $1/3$ duty cycle	27.96	2.624	47.4	-18.3
4-phase $1/4$ duty cycle	28.33	2.492	51.05	-17.69
4-phase $1/2$ duty cycle	26.78	3.239	37.06	-15.26

Knowing the best LO option, the LNA with integrated filtering was simulated for a frequency range between 300 MHz and 900 MHz. The obtained results are shown in Table V. These values show a LNA voltage gain of almost 30 dB and a NF lower than 2.26 dB, both at f_{LO}, with a power consumption of 3.6 mW. Outside the LO frequency the gain is attenuated by 6 dB, comparing with the gain at f_{LO}, and the NF shows values around 4.5 dB.

TABLE V
SIMULATION RESULTS OF THE LNA WITH FILTERING

Freq. [GHz]	Volt. Gain [dB]	NF [dB]	Z_{11} [Ω]	S_{11} [dB]	IIP_2 [dBm]	IIP_3 [dBm]
0.3-0.9	$>$ 28.3	$<$ 2.26	≈50	$<$ -17.7	$>$ 9.04	$>$ -11.78

Table VI shows the design parameters used to get the previous results. The bias voltages are 513 mV for M_1, 390 mV for M_2, and 897 mV for M_3 and M_4.

TABLE VI
LNA PARAMETERS

Transistor	W (μm)	L (μm)	Region	I_D (mA)	V_{DSsat} (mV)
M_1	115.2	0.12	active	1.51	97.99
M_2	230.4	0.12	active	1.53	78.67
M_3	11.2	0.12	active	1.52	219.35
M_4	11.2	0.12	active	1.52	219.63
M_5	6.92	0.12	triode	-1.52	-740.24
M_6	6.92	0.12	triode	-1.52	-740.40

IV. RF FRONT-END SIMULATION RESULTS

The presented receiver AFE contains all the key blocks studied below. Using the PSS and PNoise simulation, it was obtained a NF of 6.023 dB for the IF (1 MHz) and a NF below 6.9 dB for frequencies below 54 MHz, as shown in Fig. 11.

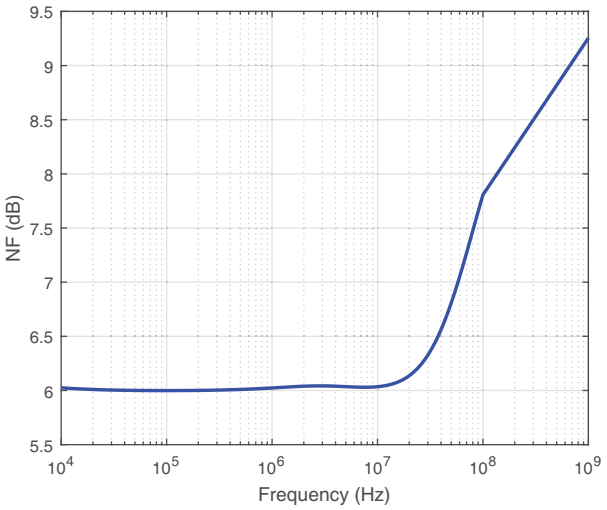

Fig. 11. AFE receiver's Noise Figure with flo = 900 MHz.

Both AFE's input impedance and input reflection (S_{11}) were obtained using PSS and PSP analysis on SpectreRF. Their results for different LO frequencies are shown in Fig. 12 and Fig. 13. In both results it is possible to verify that for higher LO frequencies the results are slightly worse, mainly due to the parasitic effects of the LNA and filters' transistors, which affect the AFE input impedance at high frequencies. However, it is possible to conclude that the receiver is adapted to the antenna's impedance for its entire working band, since the S_{11} parameter remains below -10 dB at f_{LO}.

TABLE VII
RECEIVER SIMULATION RESULTS FOR FREQUENCIES BETWEEN 300 MHZ AND 900 MHZ

Receiver Block	Volt. Gain [dB]	NF [dB]	Z_{11} [Ω]	S_{11} [dB]	IIP_3 [dBm]
LNA with Filtering	$>$ 29.52	$<$ 1.83	$\approx$46.1	$<$ -19.71	$>$ -9.23
LNA without Filtering	$>$ 28.3	$<$ 2.5	$\approx$50.9	$<$ -17.7	$>$ -11.48
Mixer	N/A	$<$ 4.5	N/A	N/A	$\approx$ 17.6
Receiver AFE	$>$ 28.3	$<$ 6.9	$\approx$45	$<$ -24	$>$ -1.54

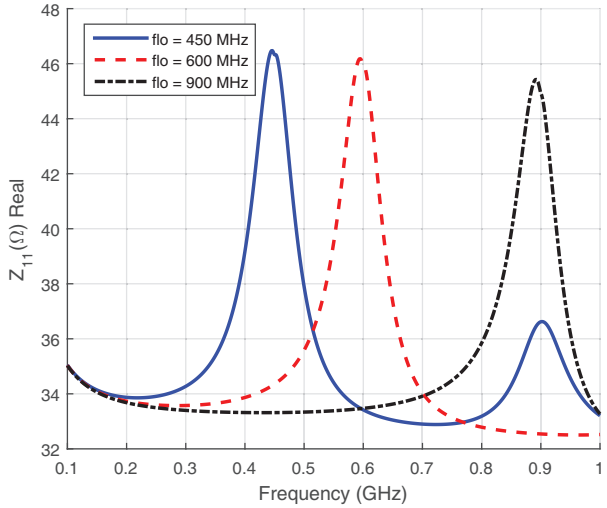

Fig. 12. Receiver AFE input impedance for multiple values of f_{LO}.

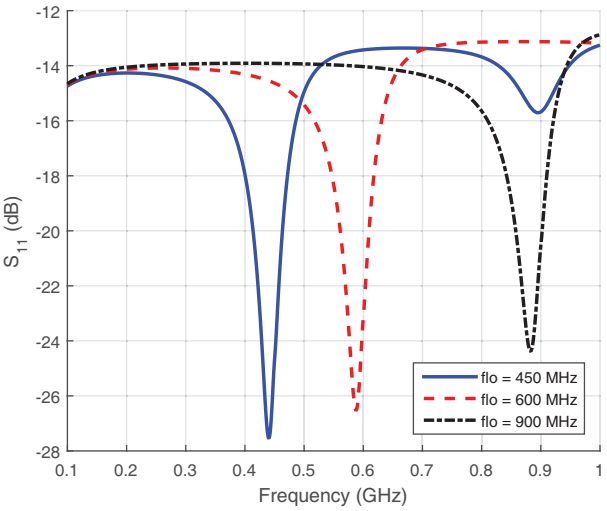

Fig. 13. Receiver AFE S_{11} for multiple values of f_{LO}.

By injecting two pure sine waves, one at 604 MHz as the RF signal and the second at 624 MHz, operating has an interferer at the receiver's input, and working with f_{LO} = 600 MHz, it was obtained an IIP3 = -1.54 dBm, showing a good linearity for the designed receiver. This simulation value was obtained using PSS and PAC analysis. Table VII shows the simulation results of each receiver's block and for the complete AFE.

V. CONCLUSIONS

In this paper a wideband CMOS receiver with integrated filtering, operating between 300 MHz and 900 MHz, was presented. The circuit was designed using CMOS 130 nm technology and a supply voltage of 1.2 V. By simulating different LO with 3 and 4 phases and with different duty cycles, it was verified that the N-Path technique is a good alternative to the traditional SAW filters. The best results were obtained for a 4-phase LO with $1/4$ duty cycle . By integrating both single-ended and differential filters on the LNA, it is possible to achieve a voltage gain of about 28.3 dB at f_{LO}, and to filter out-of-band interferers of about 6 dB, comparing with the desired signal. By adding an ideal TIA to the mixer's output, it was obtained a widely tunable receiver AFE, which is controlled by the LO frequency, with a NF below 6.9 dB for an IF lower than 54 MHz. The circuit has a power dissipation of 3.6 mW, and an IIP3 of -1.54 dBm.

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