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A Built-In Self-Test Technique for High Speed Analog-to-Digital Converters

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To the memory of my father

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During my PhD journey I received direct and indirect contributions, support, advices from many generous persons, to whom I would like to express my indebtedness. Since my memory is not perfect and it fades over time (not as much different as real capacitors and inductors lose their states), I would also like to sincerely apologize those forgotten. For those lucky, I would like to particularly thank:

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Abstract

As the conversion rate trend of analog-to-digital converters (ADCs) keeps increasing, from the present state of few gigasamples per second range, their testing is becoming progressively more challenging, time-consuming, and costly. Aware to this fact, in this PhD work we investigate a novel solution to this problem. Specifically, we propose to use two small area oscillators inserted into two synchronized phase-locked loops (PLLs) to generate high frequency sinusoidal and clock signals and, on the digital side, to employ straightforward digital signal processing (DSP) techniques to dynamically and functionally test high speed and moderate resolution ADCs. Using this built-in self-test (BIST) approach, the only off-chip component required is a low frequency and stable reference signal (e.g., produced by a ubiquitous crystal oscillator). The DSP techniques for output response analysis rely primarily on spectral computations, which nowadays are available in most system-on-a-chip environment through optimized fast Fourier transform algorithms; hence, reusing of the DSP resources is usually possible. The proposed concept was implemented in an integrated circuit featuring two PLLs for test stimuli generation and an 8-bit 500 MS/s ADC as the device under test, and was validated with silicon measurements. In a 0.13 μm CMOS technology, the area overhead introduced by the two PLLs is merely 0.052 mm^2.

KEYWORDS: Analog-to-digital converter (ADC), built-in self-test (BIST), high speed conversion, oscillator, phase-locked loop (PLL).

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Resumo

Seguindo a tendência do ritmo de amostragem de conversores analógico/digital (ADCs), que atualmente já adentra sobre a faixa de bilhões de amostras por segundo, o teste destes dispositivos está progressivamente se tornando mais complexo, demorado e custoso. Cientes desta problemática, neste trabalho de doutoramento investigou-se uma solução para tal questão. Especificamente, é proposta a utilização de dois osciladores compactos, controlados por duas malhas de captura de fase (PLLs) síncronas, para gerar sinais de sinusoide e de relógio de alta frequência e, na parte digital, empregar técnicas de processamento digital de sinais (DSP) simples para testar ADCs de elevado ritmo de conversão e moderada resolução dinamicamente e funcionalmente. Empregando esta abordagem de auto-teste (BIST), somente um componente externo para gerar um sinal de referência de baixa frequência e estável (e.g., por meio de um oscilador a cristal) é necessário. As técnicas de DSP para análise da resposta de saída recaem principalmente na computação do espectro, muito utilizada atualmente em sistemas completamente integrado em silício através de algoritmos de transformada rápida de Fourier otimizados. Portanto, a reutilização de recursos de DSP é geralmente possível. O conceito proposto foi implementado num circuito integrado, contendo duas PLLs para geração dos estímulos de teste e um ADC de 8-bit e 500 MS/s como dispositivo sob teste, e foi validado com medições em silício. Numa tecnologia CMOS de 0.13 μm, o incremento de área introduzido pelas duas PLLs é de apenas 0.052 mm^2.

Palavras-chave: Conversor analógico/digital (ADC), auto-teste (BIST), elevado ritmo de conversão, oscilador, malha de captura de fase (PLL).

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List of Abbreviations and Symbols

Abbreviations

AAC	Automatic Amplitude Control
ac	Alternating Current
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AMUX	Analog MUltipleXer
ATE	Automated Test Equipment
BIST	Built-In Self-Test
CAD	Computer-Aided Design
CMOS	Complementary Metal-Oxide-Semiconductor
CODEC	COder-DECoder
CP	Charge Pump
DAC	Digital-to-Analog Converter
dc	Direct Current
DDEM	Deterministic Dynamic Element Matching
DDS	Direct Digital Synthesis or Synthesizer
DfT	Design for Testability
DFT	Discrete Fourier Transform
DIB	Device Interface Board
DIFF/SE	DIFFerential-to-Single-Ended
DNL	Differential NonLinearity
DSP	Digital Signal Processing or Processor
DUT	Device Under Test
ENIG	Electroless Nickel Immersion Gold
ENOB	Effective Number Of Bits
ESD	ElectroStatic Discharge
FD	Frequency Divider
FF	Flip-Flop
FFT	Fast Fourier Transform
FSR	Full-Scale Range
GBC	Global Biasing Circuit
HABIST	Histogram-based Analog Built-In Self-Test
HBIST	Hybrid Built-In Self-Test
IC	Integrated Circuit

IDFT	Inverse Discrete Fourier Transform
I^2C	Inter-Integrated Circuit
IMD	InterModulation Distortion
INL	Integral NonLinearity
I/O	Input/Output
IP	Intellectual Property
IQ	In-phase and Quadrature-phase
LC	Inductor-Capacitor
LF	Loop Filter
LFSR	Linear Feedback Shift Register
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling
MADBIST	Mixed Analog-Digital Built-In Self-Test
MDAC	Multiplying Digital-to-Analog Converter
MOM	Metal-Oxide-Metal
MSB	Most Significant Bit
MUX	MUltipleXer
OBIST	Oscillation Built-In Self-Test
ORA	Output Response Analyzer
OTA	Operational Transconductance Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PFD	Phase/Frequency Detector
PG	Processing Gain
PLL	Phase-Locked Loop
ppm	Parts Per Million
PVT	Process, supply Voltage and Temperature
PWM	Pulse Width Modulation
RAM	Random-Access Memory
RC	Resistor-Capacitor
RF	Radio Frequency
rms	Root-Mean-Square
ROM	Read-Only Memory
rss	Root-Sum-Square
RZ	Return-to-Zero
SC	Switched-Capacitor
SFDR	Spurious Free Dynamic Range
SINAD	SIgnal-to-Noise And Distortion ratio
SiP	System-in-a-Package
SMA	SubMiniature version A
SNR	Signal-to-Noise Ratio
SoC	System-on-a-Chip
SPI	Serial Peripheral Interface

SPICE	Simulation Program with Integrated Circuit Emphasis
SSO	Simultaneous Switching Output
STG	Symmetrical Transmission Gate
TG	Transmission Gate
THA	Track-and-Hold Amplifier
THD	Total Harmonic Distortion
TI	Time-Interleaving
TSG	Test Stimulus Generator
UMC	United Microelectronics Corporation
VCO	Voltage-Controlled Oscillator
VCR	Voltage-Controlled Resistor
V/I	Voltage-to-Current
3D	Three-Dimensional

Symbols

f	Signal frequency ($f = 1/T$) [cycles per second, Hz]
f_s	Sampling frequency ($f_s = 1/T_s$) [samples per second, S/s]
G	Static gain of an ADC
N	Resolution of an ADC [bits, b]
N_p	Number of integer periods of a periodic continuous-time signal
N_s	Number of collected samples at ADC output
N_{seq}	Number of collected sequences, each one with length N_s
Q	Ideal code bin width of an ADC [e.g. volts, V]
$T[k]$	kth code transition level of an ADC [e.g. volts, V]
T	Signal period [seconds, s]
T_s	Sampling period [seconds, s]
V_{os}	Static offset of an ADC [e.g. volts, V]
$x(t)$	Continuous-time signal at time instant t
$x[n]$	nth sample of a discrete-time signal
$X[k]$	kth DFT spectral component
$X_{\text{os}}[k]$	kth one-sided spectral component
$X_{\text{osm}}[k]$	Magnitude of $X_{\text{os}}[k]$
$X_{\text{osmav}}[k]$	Averaged magnitude of $X_{\text{os}}[k]$
$X_{\text{osmrms}}[k]$	rms magnitude of $X_{\text{os}}[k]$
$X_{\text{win}}[k]$	kth windowed DFT spectral component
$W[k]$	kth code bin width of an ADC [e.g. volts, V]

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Chapter 1

Introduction

In this introductory chapter, we first discuss the motivations behind the research line pursued in this work in Sec. 1.1. Then, in Sec. 1.2, we give an overview of the proposed idea and state the main contributions. Finally, in Sec. 1.3, we present the organization of the chapters throughout this document.

1.1 Motivation

The evolution of the complementary metal-oxide-semiconductor (CMOS) technology has been uninterrupted, allowing more efficient implementations of conventional digital-domain functions, and favoring the migration of other-domain functions to the digital domain at each new technology node. This efficiency gain and the innate advantages of the digital circuits (e.g. flexibility, robustness against surrounding noise, "unlimited" accuracy, etc.) are the main reasons behind the "never-ending" CMOS technology downscaling.

Despite of the interesting characteristics of the digital domain for implementing a variety of functions, most signals found in nature (e.g. sound, temperature, electromagnetic fields, etc.) cannot be directly processed by digital means. Therefore, after being represented into analog electrical signals (voltages or currents), these signals need to be converted to and from the digital domain through analog-to-digital and digital-to-analog converters (ADCs and DACs), respectively. ADCs and DACs are the most fundamental mixed-signal components, since they make the interfaces between the analog and digital domains possible.

The ADC interface, similarly as the DAC one[1], assumes different forms depending on its specifications. For example, the ADC required to digitize the electrical signal representation of a human voice is completely distinct from the one required to digitize a high frequency modulated communication signal. Hence, there exist several ADC architectures and their design, fabrication, and test may vary considerably. The three key specifications of any ADC are the resolution, the conversion rate, and the dissipated power, which entail several trade-offs depending on the particular architecture chosen and the technology used.

For certain applications, commonly found in communication and measurement industries, high conversion rate (above 100 MS/s) ADCs play a crucial role in attaining faster

[1]DAC interfaces are outside the scope of this work.

data processing, transmission, and usage. With the advances of the CMOS technology and the development of novel design techniques, the conversion rates of CMOS ADCs are now well beyond the gigasamples per second (GS/s) range [1–3]. Although the conversion rates for these applications are the highest possible, they generally require only moderate ADC resolutions (usually below 12 bits) [4]. These high conversion rate and moderate resolution ADCs are the ones we are primarily concerned in this work.

To ensure that these ADCs meet the specifications, and hence are qualified to be used in the envisaged applications, they need to be tested after fabrication and occasionally during in-field operation. The production test costs of such components represent today a very significant fraction of their production cost [5, p. 42], and these costs are perhaps the fastest-growing portion of the total manufacturing cost [6, p. 19] [5, p. 43]. These high testing costs are mainly due to lengthy test applications by means of extremely expensive automated test equipments (ATEs), which are required to apply specific test stimuli to the devices under test (DUTs) and collect and analyze their responses in the fastest possible way.

Since the conversion rates are foreseen to keep increasing [7], interfacing the ADCs to the test instruments raises new problems due to parasitics, trace mismatches, and interferences of either the printed circuit board (PCB) and the instrument test probes. This scenario becomes even more challenging with the today's trends of system-on-a-chip (SoC), system-in-a-package (SiP), and the still recent three-dimensional (3D) chips [8,9], where the accessability of the ADCs for testing purposes through external equipments is becoming more and more restricted. Currently, this accessability problem can only be alleviated when an ADC and a DAC coexist into the same system, where the two can be combined to implement a fully digital test [10]. If it is not the case, however, the testing of such an ADC is extremely challenging.

1.2 Overview and Contribution

It is clear from the preceding discussion that today's testing of high speed and moderate resolution ADCs poses remarkable challenges in terms of cost (due to expensive equipment and lengthy test applications), reliability (due to DUT and ATE interfacing issues), and also feasibility (due to restriction of pins for accessing the DUT).

To cope with these challenges, in this work we explore the possibility of using a dedicated built-in self-test (BIST) approach for testing these high speed and moderate resolution ADCs, either embedded into complex systems or as standalone components. This BIST approach is based on two compact and easy-to-integrate oscillators that generate high frequency test stimuli (either analog input and clock) to the DUT. Currently, CMOS oscillators are able to reach oscillation frequencies in excess of 300 GHz [11]; hence, they naturally fit to the purpose of high frequency signals generation. Instead of using free-running oscillators for generating the analog input and clock test stimuli, we propose to synchronize the two oscillators with the aid of two phase-locked loops. This synchronization improves the phase noise of the generated signals and, more importantly, allows coherent sampling.

The use of coherent sampling has a direct and beneficial impact on the output response analysis of the DUT, since it simplifies a lot the processing of the output data in terms of

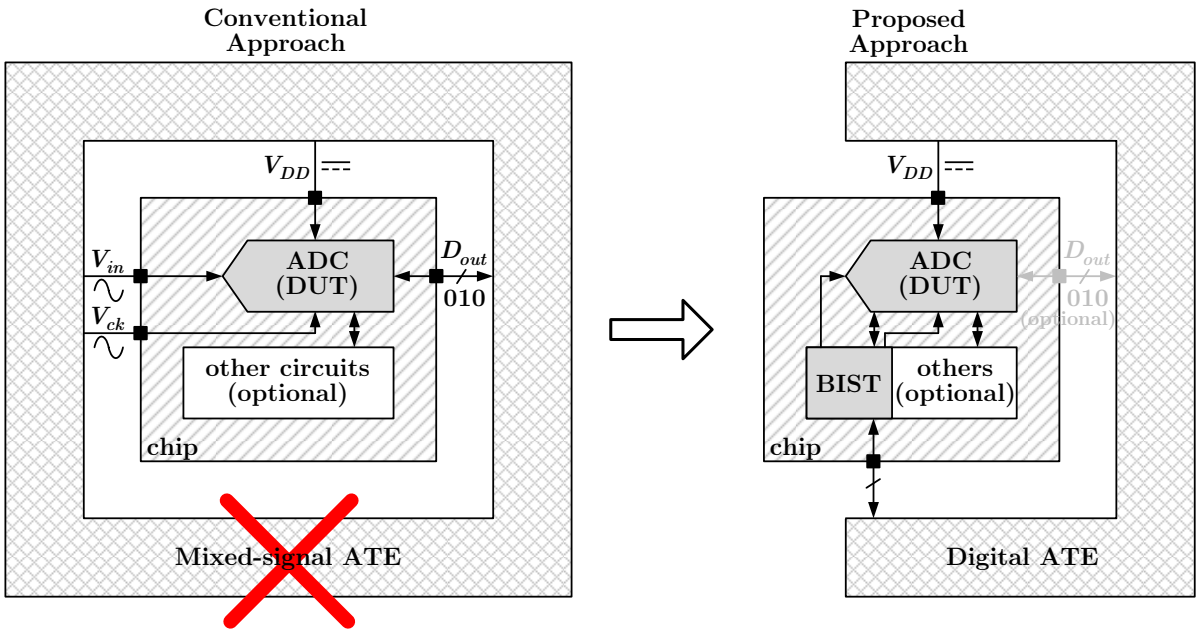


Fig. 1.1: Overview of the proposed idea.

execution time and complexity. Besides of that, and assuming spectral analysis is used to evaluate the raw output data, a coherent sampled signal translates directly to a coherent spectrum, which avoids undesirable artifacts like spectral leakage.

In the context of this work, we are primarily concerned about the ADCs' dynamic and functional performances, since ultimately they are what most matter in the testing of high speed ADCs [12, p. 241].

This fully integrated in CMOS technology BIST approach, which reduces test costs by avoiding the need of expensive mixed-signal ATEs, improves reliability by avoiding interfacing critical signals between the DUT and ATE, and enhances feasibility by carrying out the test procedure completely on-chip, is the main contribution of this work [13]. The conceptual overview of the proposed approach is shown in Fig. 1.1.

Even thought the DUT used in this work is based on a pipelined ADC topology, as it will be addressed later, the approach can be applied to other converter topologies with minimal effort, since it "sees" the device under test as an almost ideal "black box".

1.3 Chapters Organization

This dissertation is divided into eight chapters and one appendix. Following this introductory chapter, Chapter 2 introduces the basic concepts used throughout this work, namely: the static and dynamic performance metrics for ADCs and the standard test procedures used to determine them; the purpose of testing an integrated circuit; and the main differences between characterization and production tests and between structural and functional test approaches.

Chapter 3 deals specifically with the research question that guides this work. The investigated problem is detailed and preliminary observations, highlighting the strengths of built-in self-test methods, are given. Then, Chapter 4 is focused on the review of

structural and functional built-in self-test approaches, with emphasis on functional ones, which are further analyzed in terms of their applicability to static or dynamic performance testing. The chapter ends with a discussion of the reviewed solutions and identifies research gaps which are then considered within this work.

Chapter 5 presents the proposed built-in self-test architecture for high speed ADCs conceptually. It also indicates how the programmable parameters of the architecture could be selected based on the desired normalized analog input frequencies, desired clock frequencies, desired external reference frequency, and on the resolution of the ADC. Based on these parameters, a frequency map, which indicates all possible analog input and clock frequency combinations available to stimulate the device under test, is readily computed.

Chapter 6 contains the details of the proof-of-concept integrated circuit implementation. Special emphasis is given to the built-in self-test circuitry implementation, which may be ported to another ADC topology with minimal efforts, since the proposed approach considers the device under test as an almost ideal "black box" (except with regard to the interfacing input/output impedances). The device under test implementation, in this particular case a pipelined ADC, is also covered in this chapter.

Chapter 7 shows the silicon measurement results for distinct test scenarios, starting with the standalone ADC evaluation where the BIST circuitry is completely disabled. By means of on-chip configuration digital counters controlled by external push-button switches, other test modes are evaluated until the case where the BIST circuitry is fully operational. These results are compared and then confronted to those of other approaches available in the open literature. This chapter also discusses the implementation of the evaluation board and the test setup employed to make the measurements.

Chapter 8 summarizes the whole work and presents some suggestions for future research and development.

The dissertation is completed with Appendix A, which shows all system configuration possibilities.

Chapter 2

Basic Concepts

In this chapter, the background concepts related to this work are presented. First, in Sec. 2.1, the fundamental aspects of the A/D conversion are introduced since, throughout this work, we will deal with ADCs, in particular, with their testing. Secs. 2.2 and 2.3 discuss the most commonly used performance parameters for ADCs, classified into static and dynamic. Emphasis is given for dynamic parameters, since they are the most valuable in the context of high speed ADC testing. In Sec. 2.4, we briefly present the main need for evaluating a device, which is then complemented by Sec. 2.5, where two testing scenarios, characterization and production testing, depending on the device's development phase, are contrasted. The chapter ends with Sec. 2.6, which discusses the differences between functional and structural testing approaches, and points out why functional testing still maintains its predominance nowadays.

2.1 Analog-to-Digital Conversion Principle

The function of an ADC is to convert a continuous-time and continuous-amplitude signal into a discrete sequence of digital words. It needs, therefore, to perform time discretization by means of a sampler (sampling operation) and amplitude discretization through a quantizer (quantization operation). The model for an ideal ADC is illustrated in Fig. 2.1. In general, quantization and sampling are nominally uniform [14, p. 1].

The input-output transfer curve of an ideal ADC, under the assumption of uniform quantization, can be represented by a staircase function and fitted with a straight line

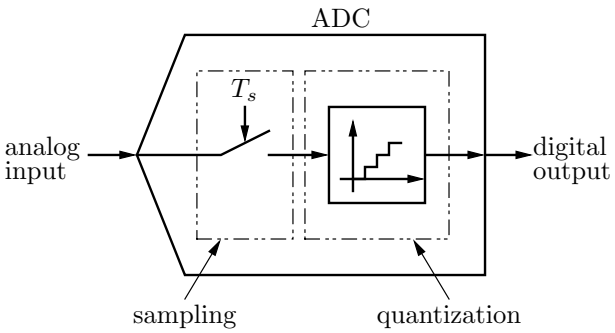


Fig. 2.1: Ideal ADC model showing sampling and quantization operations.

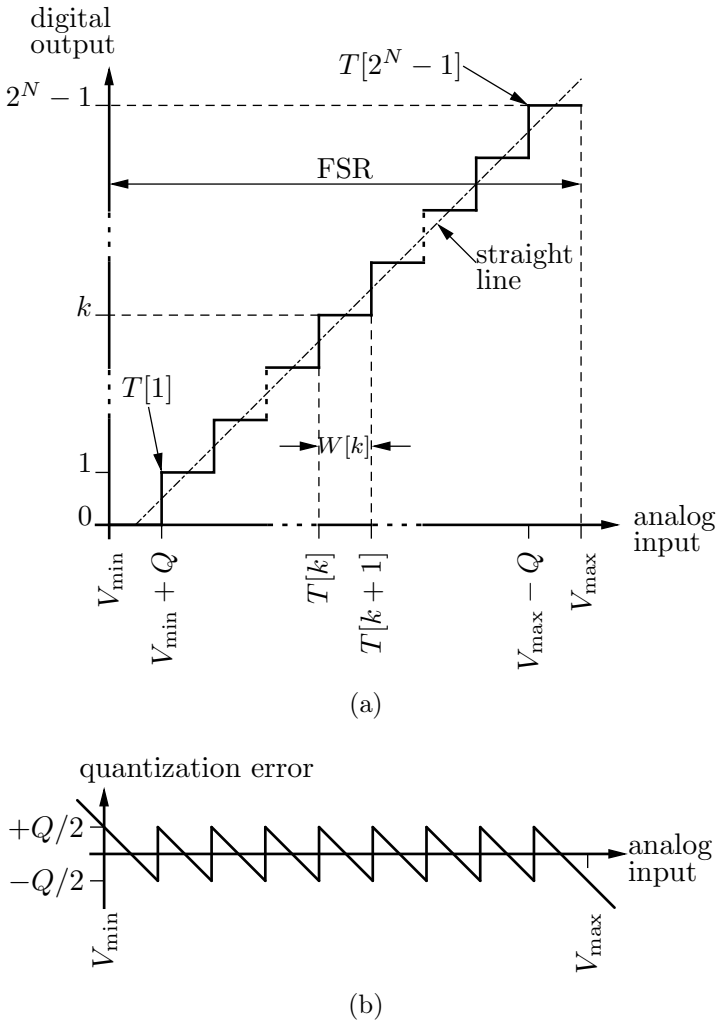


Fig. 2.2: Ideal ADC transfer curve, having full-scale range FSR and $(2^N - 1)$ transition levels, which correspond to an N-bit quantization (a) and resulting quantization error (b).

as shown in Fig. 2.2a. The transfer curve maps the sampled input signal of the ADC (represented as a voltage, in this example) to a corresponding digital output (here, represented with the unsigned coding scheme). The input signal can range from a minimum to a maximum value, $V_{\min}$ and $V_{\max}$, respectively, which is denoted as the input full-scale range (FSR) of the ADC. For a N-bit resolution ADC, the FSR is divided into 2^N equally sized code bins with nominal width Q, hence

$$Q = \frac{\text{FSR}}{2^N} = \frac{V_{\max} - V_{\min}}{2^N} \tag{2.1}$$

By convention, the lowest code bin is numbered 0, the next is 1, and so on up to the highest code bin, numbered $(2^N - 1)$ [14, p. 2]. Code bins are delimited by $(2^N - 1)$ code transition levels represented by $T[k]$. The actual kth code bin width is $W[k] = T[k+1] - T[k]$ for $k = 1, 2, \ldots, (2^N - 2)$. With this convention, therefore, the first and the last code bin widths are undefined. The code transition level $T[k]$ corresponds to the

analog input magnitude where half of the digital outputs are greater or equal to code k while the other half are below code k [14, p. 34].

Since ADCs do not have a one-to-one input-output mapping (i.e., several input voltages are mapped to the same digital output), an inherent error denominated by quantization error exists. Referring to Fig. 2.2a, this error represents the difference between the staircase function and the fitted straight line, and is plotted in Fig. 2.2b. For specific input voltages (e.g., a ramp signal or a sine signal mixed with appropriate noise) the quantization error can be treated as a continuous random variable uniformly distributed between $-Q/2$ and $+Q/2$. In this situation, it is easy to show that the root-mean-square (rms) value of the quantization error will be [15, pp. 83-85]

$$\text{rms quantization error} = \frac{Q}{\sqrt{12}} \tag{2.2}$$

Since the rms value of a full-scale input sine signal is $\text{FSR}/(2\sqrt{2})$, the maximum theoretical signal-to-noise and distortion ratio (SINAD) for an N-bit ADC is

$$\text{SINAD}_{\text{max}} = 20\log_{10}\left(\frac{\text{FSR}/(2\sqrt{2})}{Q/\sqrt{12}}\right) = 6.02N + 1.76 \text{ [dB]} \tag{2.3}$$

The analog-to-digital (A/D) conversion of an actual ADC has other errors in addition to the quantization error shown in Fig. 2.2b. These errors can be classified into static and dynamic depending on the time derivative of the input signal observed at consecutive sampling instants. If the observed time derivatives are small, it means that the input signal slowly varies in time and its effects on the A/D conversion will be equivalent to a constant signal. Static and dynamic errors can be evaluated through several metrics which are discussed in the next sections (Secs. 2.2 and 2.3).

2.2 Static ADC Performance Metrics and Corresponding Testing

In this section, the most common ADC static metrics, i.e., offset, gain, differential and integral nonlinearities (DNL and INL), are discussed. We mention them briefly, since for high speed ADCs these parameters do not lead to useful conclusions about the devices' performance. The only exception is the integral and differential nonlinearities derived by sine wave histograms, where the frequency of the sine signal can be practically increased to reveal some dynamic limitations of the ADC. In this case, we call dynamic DNL and INL to oppose to their static counterparts, and the frequency of the sine wave as well as the sampling frequency must be specified.

The static parameters inform how accurate are the code transition levels of the actual ADC transfer characteristic with regard to the ideal one (see Fig. 2.2a). Hence, the first procedure in deriving the static ADC metrics is to obtain all code transition levels $T[k]$ for $k = 1, \ldots, 2^N - 1$. For this purpose, there are basically three methods: the feedback loop, the ramp histogram, and the sine wave histogram [14, pp. 34-42].

For specific ADCs, e.g., very-high resolution or time-interleaved ADCs, the code transition levels are impractical or impossible to be defined. In these situations, there exist

an alternative method to obtain the ADC transfer curve by averaging the output codes related to a set of input signal levels. This method is explained in [14, pp. 42, 43].

2.2.1 Gain and Offset

The static gain G and offset V_{os} of an ADC are defined as the quantities by which the code transition levels $T[k]$ are multiplied and then added, respectively, in order to minimize the errors $\varepsilon[k]$ defined in Eq. (2.4). Note that the right side of Eq. (2.4) represents the ideal code transition levels, with T_1 corresponding to the ideal transition $T[1]$ (see Fig. 2.3). This definition of G and V_{os} leads to the minimum difference between the input and the output signals, after the latter is converted to input units.

$$G \times T[k] + V_{\text{os}} + \varepsilon[k] = Q \times (k-1) + T_1 \qquad k = 1, \ldots, 2^N - 1 \tag{2.4}$$

Depending on how $\varepsilon[k]$ is minimized, there are two definitions for gain and offset: terminal based and independently based [14, pp. 44, 45]. Terminal-based gain and offset are the values of G and V_{os} in Eq. (2.4) that set the error $\varepsilon[k]$ of the first and last code transition levels to zero , i.e., $\varepsilon[1] = \varepsilon[2^N - 1] = 0$. Hence, by measuring the code transition levels $T[1]$ and $T[2^N - 1]$, the terminal-based gain and offset are straightforwardly obtained.

When G and V_{os} in Eq. (2.4) are found by minimizing the mean squared value of $\varepsilon[k]$, the resulting gain and offset are denominated independently based. Using linear least-squares estimation techniques, the static gain and offset become, respectively, [14, p. 45]

$$G = \frac{Q\left(2^N - 1\right)\left(\sum_{k=1}^{2^N-1} kT[k] - 2^{(N-1)}\sum_{k=1}^{2^N-1} T[k]\right)}{\left(2^N - 1\right)\sum_{k=1}^{2^N-1} T[k]^2 - \left(\sum_{k=1}^{2^N-1} T[k]\right)^2} \tag{2.5}$$

and

$$V_{\text{os}} = T_1 + Q\left(2^{(N-1)} - 1\right) - \frac{G}{\left(2^N - 1\right)}\sum_{k=1}^{2^N-1} T[k] \tag{2.6}$$

Whichever of the two definitions is used, it must be clearly specified. The independently based approach is the most common in practice.

2.2.2 Differential Nonlinearity

The differential nonlinearity is defined as the difference between the real and ideal code bin widths, $W[k]$ and Q, respectively, divided by the ideal code bin width, after correcting for static gain. Mathematically, this becomes

$$\text{DNL}[k] = \frac{W[k] - Q}{Q} \qquad k = 1, \ldots, 2^N - 2 \tag{2.7}$$

Note that code bin widths $W[0]$ and $W[2^N - 1]$ are undefined, hence the corresponding DNLs do not exist. Furthermore, since we must adjust for static gain before computing

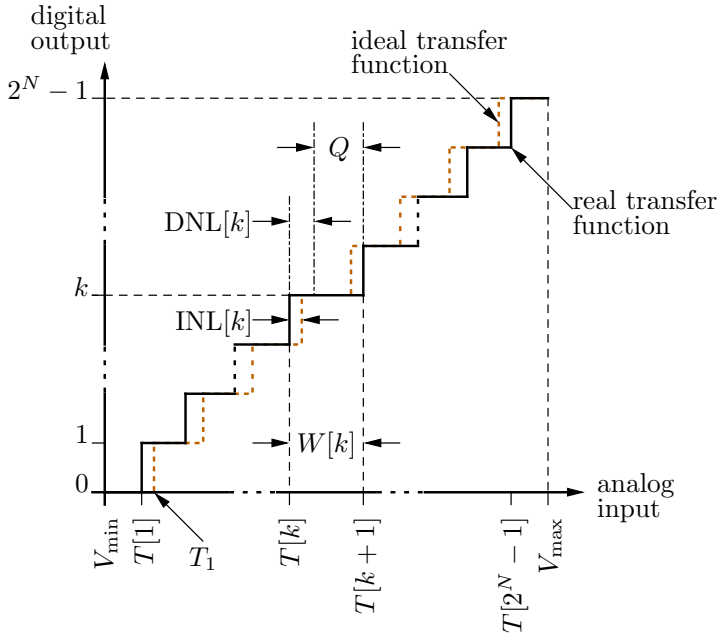


Fig. 2.3: Independently based DNL and INL definitions.

the DNL, we name the DNL according to the gain derivation procedure (i.e., terminal or independently based). The graphical representation of the kth independently based DNL value is shown in Fig. 2.3.

When the DNL is stated in a single value, it represents the maximum absolute value $|\mathrm{DNL}[k]|$ for all k. We say code k is a missing code when $\mathrm{DNL}[k] \leq -0.9$ [14, pp. 47, 48].

2.2.3 Integral Nonlinearity

The integral nonlinearity is the difference between the ideal and actual code transition levels, normalized to the ideal code bin width, after correcting for static gain and offset. When expressed in units of least significant bits (LSBs), the INL becomes

$$\mathrm{INL}[k] = \frac{\varepsilon[k]}{Q} \qquad k = 1, \ldots, 2^N - 1 \tag{2.8}$$

Similarly to the DNL, the INL may be terminal or independently based depending on the gain and offset estimation. Fig. 2.3 shows the kth independently based INL value.

A single INL value represents the maximum value of $|\mathrm{INL}[k]|$ for all codes k.

2.3 Dynamic ADC Performance Metrics and Corresponding Testing

Since the building blocks of any real ADC have finite bandwidths and can only process finite amplitude signals, generally swinging within a fraction of the supply rails (V_{DD} and V_{SS}), the behavior of the ADC changes as either the amplitude or frequency of the input signal increases. Moreover, particularly when the ADC core circuitry is surrounded by

other circuitry, there exist a high likelihood of interferences from these circuits, which also modify the ADC's behavior. These changes are associated with intricate dynamical phenomena which pose limits on the performance of the ADCs and are quantified through several metrics discussed within this section. Given that most ADC performance parameters are derived from spectral analysis, we begin explaining the discrete Fourier transform (DFT) and a sampling technique called coherent sampling. For each metric, we discuss the most commonly used testing approaches.

2.3.1 Discrete Fourier Transform and Coherent Sampling

Suppose an ADC is digitizing an input signal $x(t)$ with a sampling frequency f_s. After $N_s \times T_s$ seconds, where N_s and T_s $(= 1/f_s)$ are the number of digitized samples and sampling period, respectively, we have a sequence $x[n]$ with N_s samples. This time-domain sequence may be represented in the frequency-domain applying the DFT, which is defined as [16, p. 644]

$$X[k] = \sum_{n=0}^{N_s-1} x[n] e^{-j2\pi kn/N_s} \qquad k = 0, \ldots, N_s - 1 \tag{2.9}$$

If we want to recover the sequence $x[n]$ from its spectrum $X[k]$, we can apply the inverse DFT (IDFT) as follows [16, p. 644]

$$x[n] = \frac{1}{N_s} \sum_{k=0}^{N_s-1} X[k] e^{j2\pi nk/N_s} \qquad n = 0, \ldots, N_s - 1 \tag{2.10}$$

Note that a normalization factor $1/N_s$ is used in Eq. (2.10). This means that each spectral component $X[k]$ in Eq. (2.9) is scaled up by a factor N_s. This conclusion is easily confirmed if we calculate, for example, the direct current (dc) spectral component by means of Eq. (2.9), which is $X[0] = x[0] + x[1] + \cdots + x[N_s - 1]$, and compare it with the actual dc component value, which is the time average of $x[n]$, i.e., $(x[0] + x[1] + \cdots + x[N_s - 1])/N_s$.

The spectrum derived by Eq. (2.9) ranges from dc to $f_s(1 - 1/N_s)$ with increments of f_s/N_s, which is the frequency resolution of the DFT. Furthermore, the spectrum so obtained is two-sided represented meaning that $X[k] = X^*[N_s - k]$ for $k = 1, \ldots, N_s - 1$, where the symbol $*$ means complex conjugation. If N_s is an even integer, the spectral component $X[N_s/2]$ does not have complex conjugation. In this case, the two-sided spectrum may be converted to the one-sided one (i.e., ranging from dc to $f_s/2$) by multiplying the components $X[k]$ by a factor of two for $k = 1, \ldots, N_s/2 - 1$. Therefore, the one-sided spectrum comprises a set of $N_s/2 + 1$ spectral components as follows

$$X_{\text{os}}[k] = \begin{cases} X[k] & \text{for } k = 0 \\ 2 \times X[k] & \text{for } 1 \leq k \leq N_s/2 - 1 \\ X[k] & \text{for } k = N_s/2 \end{cases} \tag{2.11}$$

The magnitude of the one-sided spectrum after appropriate normalization is

$$X_{\text{osm}}[k] = \frac{|X_{\text{os}}[k]|}{N_s} \qquad k = 0, \ldots, N_s/2 \tag{2.12}$$

where $|x|$ means the absolute value of x. When N_s is an odd integer, slightly modifications are needed to make the two- to one-sided spectrum conversion, since now the component $X[N_s/2]$ does not exist. In this work, otherwise explicitly stated, we assume even integer N_s.

Even though the one-sided spectrum contains only half the spectral components of the two-sided spectrum, both representations have the same spectral power. Hence, they can be used interchangeably, although the one-sided spectrum is the most used.

If we collect N_{seq} sequences $x[n]$, each one with N_s samples, and apply the DFT over each of these sequences, the resulting N_{seq} spectrums will be slightly different due to inherent random artifacts (e.g. random noise, random interferers, etc.) present either in $x(t)$ or introduced during the A/D conversion. Hence, the results obtained through the spectrums will vary accordingly, limiting the measurements' accuracy and repeatability. To reduce the spectral variance, the magnitudes of the spectrums can be averaged as follows [14, p. 52]

$$X_{\text{osmav}}[k] = \frac{1}{N_{\text{seq}}} \sum_{n=1}^{N_{\text{seq}}} X_{\text{osm}_n}[k] \qquad k = 0, \ldots, N_s/2 \tag{2.13}$$

where $X_{\text{osm}_n}[k]$ represents the kth one-sided spectrum magnitude related to the nth sequence. Eq. (2.13) is an ensemble average and represents the one-sided averaged magnitude spectrum. By concentrating on a given spectral component $X_{\text{osm}_n}[k]$, as n ranges from 1 to N_{seq}, the magnitudes fluctuate around a mean value with a certain standard deviation. It can be shown that this standard deviation is approximately $\sqrt{N_{\text{seq}}}$ times higher than that obtained observing the fluctuations over several realizations of $X_{\text{osmav}}[k]$[1]. Therefore, the spectral magnitudes given by Eq. (2.13) are more accurate than those given by Eq. (2.12).

The spectral magnitudes of Eqs. (2.12) and (2.13) may be represented in rms values. For Eq. (2.12), for instance, this becomes

$$X_{\text{osmrms}}[k] = \begin{cases} X_{\text{osm}}[k] & \text{for } k = 0 \\ X_{\text{osm}}[k]/\sqrt{2} & \text{for } 1 \leq k \leq N_s/2 - 1 \\ X_{\text{osm}}[k] & \text{for } k = N_s/2 \end{cases} \tag{2.14}$$

The average power of a real-value sequence $x[n]$, with N_s samples, may be written in terms of the rms spectrum as follows

$$\frac{1}{N_s} \sum_{n=0}^{N_s-1} x[n]^2 = \sum_{k=0}^{N_s/2} X_{\text{osmrms}}[k]^2 \tag{2.15}$$

where the Parseval's theorem [16, p. 707] is used.

Thus far, we have imposed no restrictions on the input signal $x(t)$ being digitalized by the ADC and then processed by DFT. However, the spectrum computed by the DFT will be correct only if the signal $x(t)$ can be frequency decomposed into integer multiples of the frequency resolution of the DFT, i.e., kf_s/N_s for $k = 0, 1, 2, \ldots$ This means that,

[1] This is strictly true only if the random artifacts corrupting the collect sequences $x[n]$ are uncorrelated.

when the DFT is applied, the spectral components of $x[n]$ will lie exactly on the DFT bins, i.e., kf_s/N_s for $k = 0, 1, \ldots, N_s - 1$. When this condition is satisfied, we say that signal $x(t)$ is coherently sampled.

For the special case of a sine signal $x(t) = A\sin(2\pi f_{\text{in}}t)$, with frequency f_{in} $(= 1/T_{\text{in}})$, being sampled by a sample rate f_s, coherent sampling is achieved with [17, p. 45] [18]

$$f_{\text{in}} = \frac{N_p f_s}{N_s} \tag{2.16}$$

where N_p is an integer number. Eq. (2.16) can be rearranged as follows: $N_p T_{\text{in}} = N_s T_s$, where N_p may be interpreted as the number of input periods sampled during the sampling interval $(N_s T_s)$.

The computation of the DFT, exactly as defined in Eq. (2.9), requires a high computational cost, specifically, N_s^2 complex multiplications and $N_s(N_s - 1)$ complex additions. In practice, however, there exist more efficient ways to compute the DFT, which are called fast Fourier transform (FFT) algorithms [16, chap. 9]. It can be shown that these algorithms reduce the implementation complexity of the DFT to $N_s \log_2 N_s$ complex multiplications and $N_s \log_2 N_s$ complex additions, if N_s is a power of two [16, p. 729]. Therefore, it is advisable and wise to collect a power of two number of samples to allow an efficient DFT computation. In this work, unless differently stated, we assume $N_s = 2^p$ with a positive integer value p.

Sampling the sine signal $x(t)$, with f_{in} defined as in Eq. (2.16), at instants $t = nT_s$, for $n = 0, 1, \ldots$, results

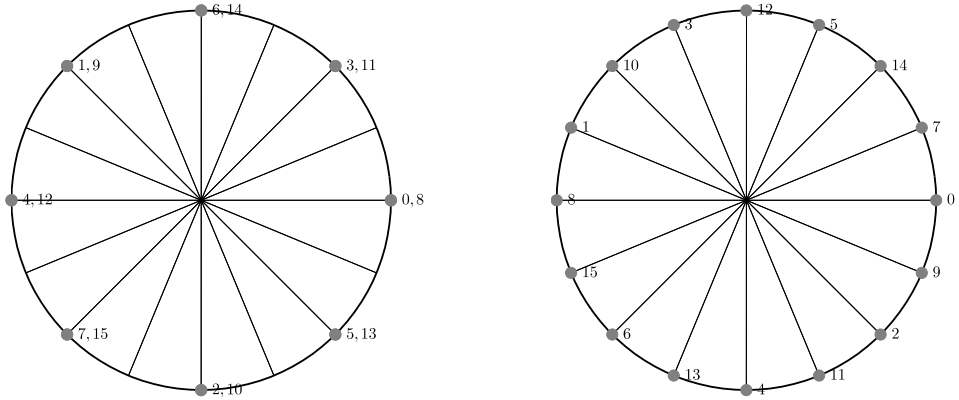
$$x[n] = A\sin\left(\frac{2\pi N_p n}{N_s}\right) \tag{2.17}$$

If we consider $N_s = 2^4 = 16$ and $N_p = 6$, for instance, and collect N_s samples, the sine signal will assume discrete-phase values of $2\pi(6/16)n$, $n = 0, 1, \ldots, N_s - 1$. Distributing these phases on a circle produces Fig. 2.4a, where the index n for each sample is shown. It is clear from Fig. 2.4a that the sequence $x[n]$ contains only 8 distinct values, since half of the samples overlap. In other words, the collected samples are somehow redundant. This occurs because N_p/N_s is not irreducible in this example, i.e., $N_p/N_s = 6/16 = 3/8$. Hence, the phases overlap after 8 samples, instead of $N_s = 16$. By considering N_p any odd integer, the ratio N_p/N_s is irreducible since N_s is a power of two. In general, N_p and N_s must be mutually prime. Fig. 2.4b shows the phases distribution when $N_s = 16$ and $N_p = 7$. Clearly, the N_s collected samples have distinct values.

From the ADC testing perspective, we want the minimum N_s that contains all possible ADC codes. Hence, N_p/N_s must be irreducible to avoid collecting redundant samples when the input signal is periodic. With this condition fulfilled and assuming an ideal ADC sampling a full-scale sinusoidal, the minimum N_s in order to get at least one sample from every ADC code is [13] [14, p. 30]

$$N_s > \pi 2^N \approx 2^{N+2} \tag{2.18}$$

The approximation in Eq. (2.18) gives some margin for nonidealities either in the ADC or in the input sinusoidal signal, though it cannot guarantee that all possible ADC codes are sampled in this nonideal scenario.



(a) (b)

Fig. 2.4: Phases distribution of a sine signal with reducible (a) and irreducible N_p/N_s (b). $N_s = 16$ for both cases and the circle is divided in N_s slices.

The number of samples, N_s, also influences the processing gain (PG) of the DFT, which is defined as [15, p. 88]

$$\mathrm{PG} = 10 \log_{10} \left(\frac{N_s}{2} \right) \ [\mathrm{dB}] \tag{2.19}$$

This gain defines how much the DFT noise floor is below the maximum signal-to-quantization noise ratio given by Eq. (2.3). As an example, Fig. 2.5 shows the one-sided magnitude spectrum obtained through Eq. (2.12) over $N_s = 4096$ samples. The samples are derived from a 10-bit ADC with a FSR of one, which is sampling a full-scale sine signal, i.e. $x(t) = (\mathrm{FSR}/2) \sin(2\pi f_{\mathrm{in}} t)$, with $f_s = 100$ MS/s. The frequency f_{in} is selected by Eq. (2.16) with $N_p = 483$ and N_s given by Eq. (2.18), thus ensuring coherent sampling. (Note that the Nyquist criterion [16, p. 160] is not obeyed if $N_p \geq N_s/2$. In this case, the ADC is undersampling the input signal, which is commonly denoted sub-sampling operation mode.)

If Eq. (2.16) is not satisfied, the ADC samples the input signal noncoherently. In this situation, the signal will not be concentrated on a single DFT bin; instead, it will be spread among several bins, which is commonly known as spectral leakage. Fig. 2.6a superimposes the coherent spectrum of Fig. 2.5 with a noncoherent spectrum obtained choosing $N_p = 483.5$. It is noticeable that the resulting spectrum is unsuitable for practical use.

To minimize the undesirable effects produced by noncoherent sampling, we can apply a window over the digitized sequence $x[n]$, and then compute the DFT. The purpose of any window is to progressively reduce the amplitude of the sequence $x[n]$ from its intermediate to its extremes samples. This idea originates from the fact that the DFT, even processing a single sequence $x[n]$ with N_s samples, implicitly assumes the sequence $x_c[n]$, formed by a contiguous arrangement of an infinity number of sequences $x[n]$, has no discontinuities between adjacent samples. When Eq. (2.16) is not fulfilled, these discontinuities are unavoidable. To reduce them, which are the cause of spectral leakage, the extreme samples of $x[n]$ are attenuated (see Fig. 2.7).

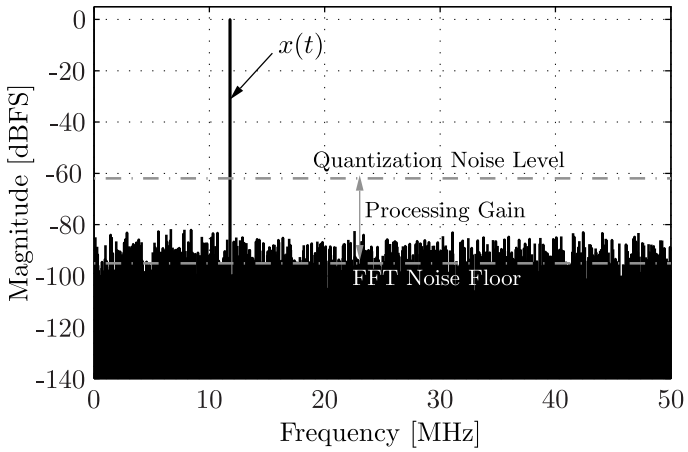


Fig. 2.5: Output spectrum (4096-point FFT) of 10-bit ADC with FSR = 1, f_s = 100 MS/s, and input signal $x(t) = 0.5 \times \sin(2\pi \times (483/4096) \times 10^8 t)$. The FFT noise floor is ~ 33 dB below the maximum theoretical SINAD for this converter, i.e. ~ 62 dB, due to processing gain.

The spectrum of a windowed sequence is derived as follows

$$X_{\text{win}}[k] = \sum_{n=0}^{N_s-1} w[n]x[n]e^{-j2\pi kn/N_s} \qquad k = 0, \ldots, N_s - 1 \tag{2.20}$$

which is similar to Eq. (2.9), despite now the sequence $x[n]$ is multiplied by the window $w[n]$.

Regarding the window selection, there are several options depending on the desired characteristics (see, e.g., [19, p. 55]). Perhaps the most used for ADC testing are the Flat Top and the Hann windows, which are defined, respectively, by Eqs. (2.21) and (2.22)

$$w[n] = 1 - 1.93\cos\left(\frac{2\pi n}{N_s - 1}\right) + 1.29\cos\left(\frac{4\pi n}{N_s - 1}\right) - 0.388\cos\left(\frac{6\pi n}{N_s - 1}\right) + 0.0322\cos\left(\frac{8\pi n}{N_s - 1}\right) \qquad n = 0, \ldots, N_s - 1 \tag{2.21}$$

$$w[n] = 0.5\left(1 - \cos\left(\frac{2\pi n}{N_s - 1}\right)\right) \qquad n = 0, \ldots, N_s - 1 \tag{2.22}$$

The Flat Top window changes almost negligibly the amplitudes of the signal $x(t)$, and since most measurements are based on spectrum magnitudes, this window is largely employed. However, the Flat Top window is not adequate for frequency discrimination, given that the energy of the components are spread over several DFT bins. In this particular case, the Hann window is more appropriate. Besides these two windows, there are many others, e.g., Hamming, Blackman, Blackman-Harris, etc. The windowed spectrum shown in Fig. 2.6b uses a Flat Top window.

2.3.2 Signal-to-Noise and Distortion Ratio

Suppose an ADC is digitizing an input sine signal whose noise and distortion are negligible compared to those introduced by the ADC itself and other signals driving the ADC, e.g.,

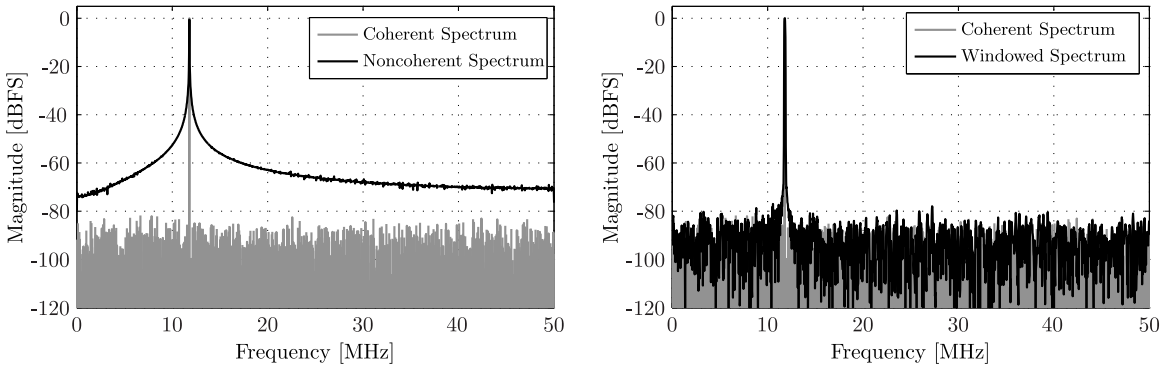


Fig. 2.6: Noncoherent (a) and windowed (Flat Top window) (b) spectrums both overlaid with the coherent spectrum.

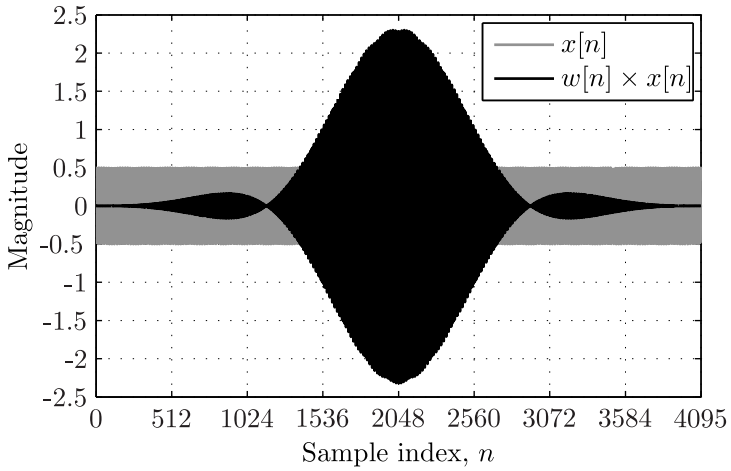


Fig. 2.7: Original $x[n]$ and windowed $w[n] \times x[n]$ sequences. The window attenuates the amplitudes of $x[n]$ at its extreme samples.

the clock signal. For each amplitude and frequency of the sine wave, the signal-to-noise and distortion ratio (SINAD) is computed as the ratio of the rms value of the sine signal to the rms value of the total noise at the ADC output. Mathematically, this becomes

$$\text{SINAD} = 20 \log_{10} \left(\frac{\text{rms signal}}{\text{rms total noise}} \right) \text{ [dB]} \tag{2.23}$$

The total noise is any deviation between the output of the ADC, converted to input units, and the input signal, except deviations caused by gain, phase, or dc level shifts. Therefore, the amplitude accuracy and dc offset of the sine signal do not affect the SINAD result. Nonetheless, random noise and distortion do affect it and, consequently, appropriate filtering may be required depending on the quality of the available sine wave generator. Also, the frequency stability of the generator is an important concern, and it should be able to generate a low phase noise signal.

The above outlined sine signal nonidealities must be insignificant contrasted to those introduced by the A/D conversion. If they are not, the ADC performance evaluation will

be misleading. Concerning the sine distortion, in practice, the amplitude of the dominant harmonic component of the sine signal should be at least 12 dB (or approximately 2 bits) below the amplitude of the dominant harmonic distortion of the ADC [14, pp. 69, 70]. A similar rule of thumb may be applied to the random noise corrupting the sine signal, i.e., 12 dB below the ADC rms quantization noise. For the frequency stability, a maximum limit may be found relating the time jitter standard deviation of the sine signal to its nominal period [14, pp. 68, 69].

The amplitude and frequency of the sine wave influence the SINAD, hence for each measurement their values must be clearly specified. The minimum amplitude that can be processed by the ADC is restricted by the ADC noise floor. As the amplitude of the sine signal increases, the SINAD also increases until the distortions become dominant. For greater magnitudes, the SINAD decreases sharply. The dependence on frequency is usually monotonic, with the SINAD decreasing as the frequency of the sine signal increases. The most informative SINAD value is obtained when either the frequency and amplitude of the sine signal are pushed close to the maximum allowed values, which rely on the ADC bandwidth and full-scale range.

There are, basically, two test methods used to derive the SINAD: one based on the frequency domain and other based on sine wave fitting. The frequency domain method uses the DFT to first derive the spectrum and then compute the rms values of the sine signal and the total noise. A coherent spectrum, when practically feasible, is preferable to a windowed spectrum, as explained in Sec. 2.3.1. Considering a one-sided rms magnitude spectrum (see Eq. (2.14)), the rms value of the total noise is given by

$$\text{rms total noise} = \sqrt{\sum_{f_k \neq 0, f_{\text{in}}} X_{\text{osmrms}}[f_k]^2} \tag{2.24}$$

where $f_k = k f_s/N_s$, $k = 0, \ldots, N_s/2$. In Eq. (2.24), we removed the dc and fundamental frequency (f_{in}) components, and the remaining rms spectral components are combined in a root-sum-square (rss) basis. The rms value of the sine signal is found as follows

$$\text{rms signal} = X_{\text{osmrms}}[f_{\text{in}}] \tag{2.25}$$

The SINAD is then obtained by substituting Eqs. (2.24) and (2.25) into Eq. (2.23).

If the measurement requires more accuracy, then the averaged spectrum defined by Eq. (2.13) can be applied. When a windowed spectrum is used to measure the SINAD, special attention must be paid to select the appropriate spectral components that form the rms signal and total noise values, since the energy of the signals are not confined in single DFT bins. In this situation, and depending on the characteristics of the window employed, adjacent bins should be considered for the dc and sine signal related spectral components [15, pp. 332, 333].

The sine fitting method is an alternative to the windowed spectrum to calculate the SINAD, since both approaches do not necessarily rely on the coherent sampling. Nevertheless, the fitting method entails more intensive computations than the DFT, specially when the latter is implemented using a FFT algorithm. This, in turn, entails more complex hardware/software implementations and longer testing procedures, which unavoidably limit the approach popularity. Following this method, the total noise rms

value is given by

$$\text{rms total noise} = \sqrt{\frac{1}{N_s}\sum_{n=0}^{N_s-1}\left(x[n]-\hat{x}[n]\right)^2} \tag{2.26}$$

where $x[n]$ is the digital output of the ADC and $\hat{x}[n]$ is its best fit sine wave. The sine wave rms value is simply the amplitude of the fitted sine divided by $\sqrt{2}$.

Two well-known approaches for sine wave fitting are the three- and four-parameters least-squares fitting. The former is used when the frequency of the sine is known a priori, but the offset, amplitude and phase are not. A discussion of both methods may be found in [14, pp. 28, 29].

2.3.3 Total Harmonic Distortion

Differently from the SINAD, the total harmonic distortion (THD) accounts only for the harmonic components present in the ADC total noise. The harmonic components are a result of ADC nonlinearity and intricate dynamic phenomena when it is digitizing a periodic signal.

When the ADC is digitizing a pure sine wave (see Sec. 2.3.2 for a discussion on the sine wave purity) with certain frequency and amplitude, the THD is computed as the ratio of the rms value of a specified set of harmonic components to the rms value of the sine wave. In decibels this becomes

$$\text{THD} = 20\log_{10}\left(\frac{\text{rms harmonics}}{\text{rms signal}}\right)\ [\text{dB}] \tag{2.27}$$

The set of harmonics considered in the THD must be stated when providing a THD measurement, as well as the amplitude and frequency of the input sine wave. Otherwise explicitly stated, in this work we consider the 2^{nd} to the 10^{th} harmonics, similarly as in [14, p. 52]. When a given harmonic component cannot be distinguished from the ADC noise floor, it can be ignored from the THD computation.

Depending on the ADC bandwidth and full-scale range, the most useful THD value is obtained when the input sine wave assumes the highest amplitude and frequency allowed. This setup usually leads to the worst THD, since normally it worsens as either the amplitude and frequency of the sine signal increase.

The computation of the rms value of the harmonic components with enough accuracy needs an unambiguous spectrum, which is readily achieved with a coherent spectrum. When a windowed spectrum is used instead, special care must be given to the THD measurement, as discussed in [14, pp. 53, 54]. Furthermore, an averaged spectrum should be used whenever practical.

Considering an one-sided rms and coherent spectrum, the rms value of the harmonics is given by

$$\text{rms harmonics} = \sqrt{\sum_{l=2}^{10} X_{\text{osmrms}}[f_{\text{h}l}]^2} \tag{2.28}$$

where $f_{\text{h}l} = l f_{\text{in}}$ represents the frequency (folded or not) of the lth harmonic. The rms value of the sine signal is given by Eq. (2.25).

2.3.4 Signal-to-Noise Ratio

To derive the SINAD the ratio of the rms values of the sine signal to the total noise is used. If we remove from the total noise the harmonic components used in the THD measurement, then the signal-to-noise ratio (SNR) results

$$\text{SNR} = 20\log_{10}\left(\frac{\text{rms signal}}{\text{rms non-harmonic noise}}\right) \text{ [dB]} \tag{2.29}$$

The rms value of the total noise excluding the harmonics, i.e., the non-harmonic noise, is

$$\text{rms non-harmonic noise} = \sqrt{\sum_{f_k \neq 0, f_{\text{in}}, f_{\text{hl}}} X_{\text{osmrms}}[f_k]^2} \tag{2.30}$$

where the frequencies f_{hl} are the same used in Eq. (2.28). The rms value of the sine signal is given by Eq. (2.25).

2.3.5 Spurious Free Dynamic Range

For an ADC digitizing a pure sine signal, the spurious free dynamic range (SFDR) is defined as the ratio of the sine wave amplitude to the largest amplitude in the whole spectrum after removing the dc and the sine wave spectral components. Mathematically, and considering an one-sided magnitude spectrum (see Eq. (2.12)), the SFDR turns to be

$$\text{SFDR} = 20\log_{10}\left(\frac{X_{\text{osm}}[f_{\text{in}}]}{\max_{f_k \neq 0, f_{\text{in}}}\left(X_{\text{osm}}[f_k]\right)}\right) \text{ [dB]} \tag{2.31}$$

where $f_k = kf_s/N_s$, $k = 0, \ldots, N_s/2$. The function $\max_{f_k \neq 0, f_{\text{in}}}\left(X_{\text{osm}}[f_k]\right)$ finds the maximum spectral component in the spectrum disconsidering the dc and the fundamental frequencies.

As for the other dynamic parameters discussed so far, the SFDR also depends on the amplitude and frequency of the sine signal. Consequently, the chosen amplitude and frequency must be specified with any SFDR measurement.

2.3.6 Effective Number of Bits

The effective number of bits (ENOB) performance parameter compares how close a real ADC is of an ideal ADC in terms of total noise. For a pure sine wave of specified amplitude and frequency, the ENOB is defined as follows

$$\text{ENOB} = N - \log_2\left(\frac{\text{rms total noise}}{\text{rms quantization error}}\right) \tag{2.32}$$

where N is the resolution of the ADC in bits. In Eq. (2.32), the rms value of the total noise is given by Eq. (2.24) or (2.26), and the rms value of the quantization error is given by Eq. (2.2).

The ENOB may be related to the SINAD as follows [14, pp. 67, 68]

$$\text{ENOB} = \log_2\left(\text{SINAD}\right) - \log_2\left(\sqrt{1.5}\right) - \log_2\left(\frac{X_{\text{osm}}[f_{\text{in}}]}{\text{FSR}/2}\right) \tag{2.33}$$

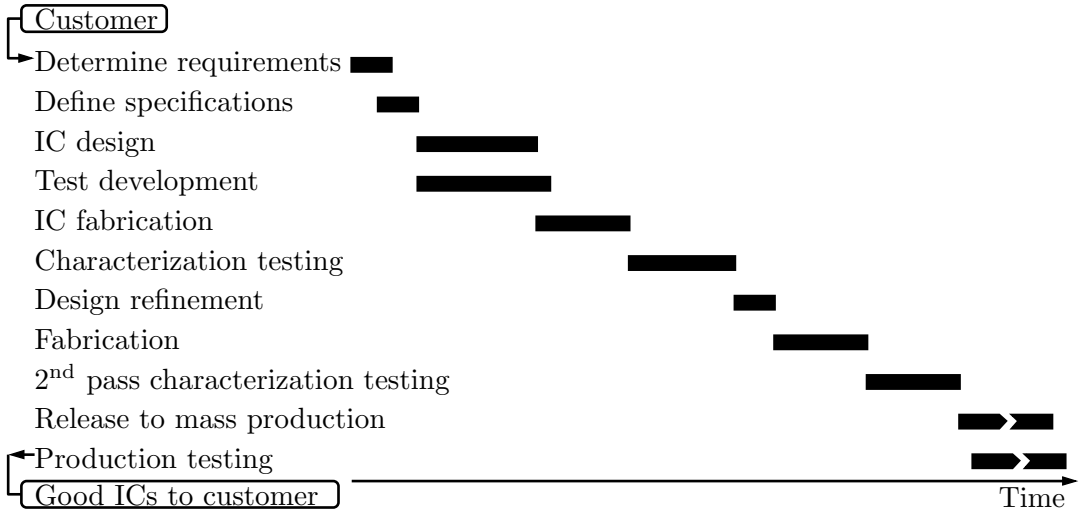


Fig. 2.8: Development cycle of an IC.

where the SINAD is given by Eq. (2.23) (after converting to linear scale), $X_{\text{osm}}[f_{\text{in}}]$ is the amplitude of the digitized sine wave, and FSR is the full-scale range of the ADC.

In this section, we presented the most common dynamic metrics for evaluating an ADC as well as the test methods used to derive them. This coverage is sufficient for the purposes of this work; however, more dynamic metrics do exist. A more complete treatment can be found in the IEEE standard 1241-2010 [14]. We have noted that most test methods rely on a spectrum derived through DFT and coherent sampling.

2.4 Role of Testing

To better understand the purpose of testing an integrated circuit (IC), for example, an ADC, we firstly need to comprehend the development and production cycle of such a device. This cycle is divided in several phases, which are defined according to the business model of the IC manufacturer. For instance, a manufacturer having a vertically integrated business may deploy a development cycle beginning with the requirements for a specific device and finalizing with the concerns of in-field application for it [20, pp. 2–7]. Here, instead of this holistic approach, we consider a reduced version starting with costumer's requirements and ending with good packaged devices shipped to the customer, as illustrated in Fig. 2.8.

The development begins with the customer's requirements for the IC with a target application in mind. For instance, the IC may be used for a telecommunication transceiver, a high frequency oscilloscope, a medical equipment, etc. Based on the requirements, a set of specifications is defined, which can be grouped by categories [5, p. 7]. Functional specifications relate to the input-output characteristics of the IC, e.g. offset, gain, linearity, noise, etc. Most of the parameters discussed in Secs. 2.2 and 2.3 are functional properties. Operating specifications define supply voltages, power dissipation, operating frequency, etc. The target fabrication (e.g., CMOS, bipolar, etc.) and packaging technologies as well as die area are defined in the physical specifications. Environmental specifications define temperature, humidity, etc. ranges under which the IC will possibly

operate and the reliability needed under several environmental conditions. Furthermore, other characteristics such as production volume, cost, price, etc. are also specified.

Before proceeding in the IC development flow, the requirements and specifications should be checked against their feasibility. To this end, requirements and specifications are audited, which is a form of avoiding an unrealizable specification to reach the design phase [5, p. 8].

With the specifications defined and audited, the IC design takes place. The most recurrent design methodologies for mixed-signal ICs are the top-down and bottom-up methodologies, with their own strengths and weaknesses [21, 22]. In a top-down design, without going into many details, for example, the design starts with a high-level behavioral modeling of the architecture. Behavioral model simulations, although not as accurate as electrical simulations, are much faster and allow the designer to evaluate several design choices and ideas which were not feasible otherwise. In the next step, the functionality of model is mapped to electrical circuits, which are then sized to meet the specifications, and more accurate electrical simulations are performed. The electrical and behavioral results are verified for agreement. If there exist a high correlation, the circuits are then laid out; if not, the circuits are resized and simulated again. After the layout is done, electrical simulations verify the conformance of post-layout simulation results with circuit-level (in the absence of parasitics) results. If the results are in accordance, then the IC is sent to fabrication.

Note that throughout the design phase several verifications are executed when changing from one abstraction level to the next (e.g. from model to electrical circuits to physical layout). These verifications permit to identify a design error early in the design cycle, thus avoiding waste of time and cost, and precluding as much as possible an erroneous design to reach the fabrication step.

Concurrently to the IC design, the test development occurs. This involves the definition of all testability issues, the elaboration of a test plan and the design of the hardware (e.g., PCB) and software required for testing.

The layout data allows to generate the photomasks used for IC fabrication. The fabrication process entails a sequence of steps which involve, for example, epitaxial growth, photoresist deposition, patterning through the exposure of photomasks to ultraviolet light, etching, ion implantation, oxidation, metallization, etc. (see [23, pp. 87–104] for details).

Unfortunately, the fabrication is not a perfect process. Impurities and material imperfections, malfunction equipments, and human errors are some caused of defective ICs. The main reason for testing is to detect these defects, which cause an out of specification, or bad, IC [5, p. 8]. The testing gives no answer about what exactly went wrong. This answer is obtained through diagnostic analysis (diagnosis). The defects can be group into catastrophic or non-catastrophic (or soft). In the former, which may be a short or open trace, for example, the IC is not functional at all. In the latter, the specifications may vary slightly from one IC to another, and this may be caused by extra parasitic capacitance on a specific trace, for instance.

When an IC is designed, fabricated, and tested for the first time, which is called a prototype, it is not directly released to mass production nor it is tested in the same way as it is under this manufacturing regime. The prototype is tested under diversified operational conditions and the worst-case ones are found. For example, the distortion of

an ADC may be evaluated under a range of temperatures as well as a range of supply voltages. After exhaustive measurements, the worst-case distortion results for specific temperatures and supply voltages. In essence, the characterization testing tries to uncover the performance limits of an IC.

Usually, the characterized performance of the prototype does not completely meet the intended specifications. In this situation, a design refinement is required. The redesign is then fabricated and tested, and, if the achieved performance is satisfactory, it is release to mass production. In complex ICs, however, more than a single redesign is commonplace.

In mass production, the lengthy and costly characterization testing is not economically viable. Hence, a simplified version, generally a subset of the characterization testing, is used. The aim of the production testing is to provide quality testing, where as much as possible defective ICs are detected and not shipped to the costumer, in a cost effective manner [20, p. 2].

The fraction of acceptable, or good, ICs among all produced parts is called the production process *yield*. The silicon area of the IC has a strong impact on the yield, since the likelihood of defect occurrence is proportional to the area. For complex ICs, yield values of about 60 % are quite typical in a mature manufacturing process [5, p. 46].

Not all defective ICs are rejected by means of testing, because the testing procedure is not perfect; there is a trade-off between test quality and cost. As a result, some bad ICs are actually shipped to the customer. The fraction of defective ICs among all ICs that pass the test, expressed in parts per million (ppm), is defined as the *defect level* and it is used as a metric for test quality [5, p. 47]. Defect levels lower than 100 ppm represent a high quality testing [5, p. 48].

2.5 Characterization versus Production Testing

As has been pointed out in Sec. 2.4, the characterization and production tests involve distinct levels of complexity. In addition, they are usually performed with different hardware setups as well as with different personnel interactions.

The characterization testing (also known as design debug or verification testing) for an ADC is usually carried out with bench equipment controlled by a personal computer (PC) [24], as illustrated in Fig. 2.9a. The device under test (DUT), in this case the ADC, is soldered onto a properly designed PCB. The DUT interfaces with a test stimulus generator whose purpose is to stimulated the ADC input with a known signal, e.g. a sine wave. The clock signal is usually derived from another signal synthesizer, or, optionally, from a crystal oscillator mounted directly onto the PCB. One or more power supplies provide the voltage and current levels needed to power up the ADC. The parameters of the signal generators and the power supplies can be controlled directly from the PC. After these parameters are configured, the ADC starts the conversion process and a data capture board collects the digitized samples which are firstly stored in a memory and then sent to the PC for analysis. The data capture board also serves as a bridge between the PC and ADC, providing the digital signals to operate the latter.

In order to appropriately collect the samples, the data capture board must run in the same time base with respect to the ADC. This is achieved sharing the clock signal, or other specific signal planned for this task. Sometimes, it is also important to synchronize

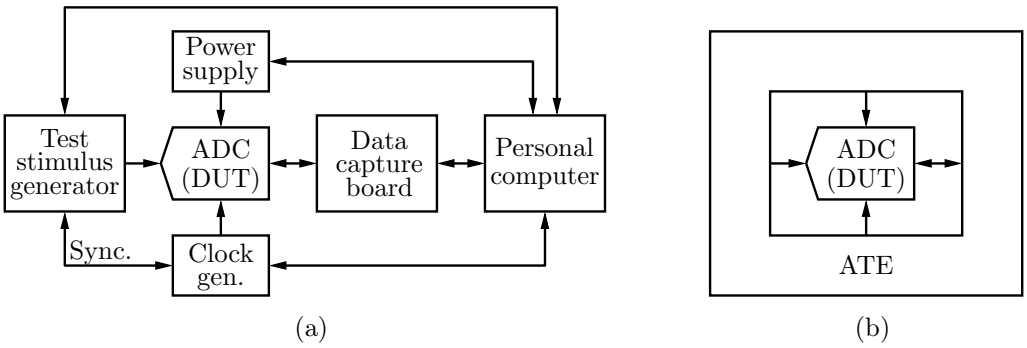


Fig. 2.9: Setup for characterization (a) and production (b) testing.

the analog input test stimulus generator with clock generator. This synchronization is done by connecting a cable between specific terminals usually available in such equipment.

The samples sent to the PC are analyzed through a custom or commercial software, and the performance parameters of the ADC are found. The evaluated performance allows to infer the correctness of the design and test procedure, which, depending on the results, may or not be changed.

The characterization testing usually involves the interaction of both design and test engineers, since the limits of the designed IC are being explored. Also, this type of testing is normally executed in the design laboratory over a small number of ICs, which allow, in any case, to reach statistically significant results. A successful characterization signals the beginning of mass production.

All produced ICs are tested in a more streamlined test procedure contrasted to the characterization tests, which is denominated production or manufacturing testing. In this case, the bench equipment shown in Fig. 2.9a are fully integrated into an automated test equipment (ATE), as illustrated in Fig. 2.9b, and the testing takes place in the manufacturing plant.

An ATE tester usually consists of three main parts: a test head, a workstation, and the mainframe [6, p. 11]. The test head contains all the sensitive measurement electronics, for example, signals drivers and receivers. The circuits in the test head connect to the device interface board (DIB) which, in turn, interface with the packaged IC (DUT) through a socket. Besides a temporary electrical connection between the DUT and the ATE, the DIB also contains specific local circuits such as buffers and loads. In essence, it has a similar role as the PCB has for characterization testing.

The workstation serves as the user interface to the ATE. Test and manufacturing engineers use the softwares provided by the ATE vendor to debug test procedures and to monitor the daily operation of the tester. The mainframe contains much of the tester's electronics, such as power supplies, measurement instruments, and computers to control the instruments. The mainframe may also contain a manipulator to position the test head precisely and a refrigeration unit to regulate the temperature of the test head electronics [6, p. 12].

The purpose of the ATE is to power up the DUT, apply test stimuli to and analyze the responses from it, and mark the DUT as good or bad.

ATE tester may be purchased from a variety of vendors, such as Teradyne, Advantest-Verigy, and LTX-Credence. The total cost of such equipment is approximately a function

of the number of pins and the additional capabilities available, e.g. mixed-signal circuits testing hardware. A mixed-signal ATE may cost a few millions dollars [5, p. 10].

When an IC pass production testing, it is not guaranteed that it will function within specifications for a long period of time. Some devices, indeed, will present abnormal operation within hours or days. To improve the reliability of such ICs, they undergo burn-in testing, also known as stress or accelerated life testing. In this particular form of testing, the devices are tested for a long period of time under an accelerated operation environment (e.g. with elevated temperatures and/or supply voltages).

With burn-in testing, bad ICs will actually fail and will not be shipped to the customer. The two most common failures detected by burn-in testing are infant mortality failures and freak failures. The former is isolated with a short-term testing (10 to 30 hours) and the latter with a long-term testing (100 to 1,000 hours) [5, p. 20]. The adoption of burn-in testing is essential for high reliability devices, where the additional testing costs are justifiable.

After the good tested ICs are delivered to the customer and before the customer integrates them into a system, some randomly selected, or even all, devices are tested again. This testing is known as incoming inspection or acceptance testing, and prevents that bad quality devices are assembled onto PCBs and then into systems.

Acceptance testing follows the reasoning of the *rule of ten* [5, p. 44], which says that the cost for detecting a faulty device increases by a factor of ten as we move to higher integration levels (from ICs to PCBs to systems).

Despite of being at the IC, PCB, or system level, the goals of testing are to discard defective devices and learn information (through diagnosis) to improve the fabrication process yield and reduce costs [5, p. 309].

2.6 Structural versus Functional Test Approaches

A mixed-signal device, as an ADC, can be either tested against its functional specifications or tested against structural defects caused during the manufacturing process. Both approaches have their advantages and drawbacks, and sometimes the best testing trade-offs are achieved mixing them.

The functional testing, also known as specification-oriented testing, regardless of being in the characterization or production levels, performs the minimum set of measurements on the DUT to ensure that the intended specifications are met, e.g., the total harmonic distortion of the tested device is bellow a specified value. This is done applying specific test stimuli to the DUT and analyzing its response. The responses, even for good quality devices, will vary around a nominal value due to noise, manufacturing parameters fluctuations, and measurement uncertainties. The allowed variation range, called tolerance box, will be used to qualify the tested IC as good or bad. If the performance parameter under evaluation is within the range of variation, the IC is classified as good, else it is assumed bad or, alternatively, sorted within another range of variation (which could fulfil the requirements for another application, for example).

Structural, or defect-oriented, testing, on the other hand, tries to detect structural changes in the DUT's circuit caused by manufacturing defects, which will probably lead to a malfunction device. In this sense, the test stimuli may be completely distinct from

the ones used in the actual application of the device, and they may be applied in different nodes as well. The key idea of structural testing is to identify whether specific modeled faults are present in the manufactured IC or not. Hence, fault modeling and fault simulations at the design level are crucial.

Similarly to defects in ICs, fault models for mixed analog/digital testing can be classified into two categories: catastrophic faults (or hard faults) and parametric faults (or soft faults) [25, p. 704]. Catastrophic faults can be either a short between two, or more, non-shorted designed traces or terminals, or a open terminal or trace. Parametric faults are fluctuations of a given design parameter (e.g. a resistor value) outside the tolerance limits. Although simple short and open models fit reasonably well for digital circuits, and are the main drivers behind the wide adoption of structural testing there, there is not such a consensus for fault modeling in mixed-signal circuits. For example, the resistance of a shorted trace should be modeled with 0.1, 1, or 10 Ω? Though likely irrelevant for a digital circuit, these values may directly affect the performance of a mixed-signal IC.

Additionally, does not exist currently a mapping relating structural modeled faults to the device functional specifications. This, together with the absence of well-accepted analog fault models, are the main reasons preventing structural testing to be widely used in mixed-signal ICs [5, p. 312]. Besides the modeling problem, analog fault simulation (i.e. test generation and evaluation) is very time consuming because of the large number of faults that may exist during manufacturing.

The opportunities offered by structural testing are shorter and faster, and thus more economic, test procedures. Also, following this approach it is possible to compute the fault coverage of the testing, which is a quantitative measure of test effectiveness. Nevertheless, as pointed out in [26, p. 302], the structural approach does not prove that the DUT meets functional specifications because of the many interdependencies between the circuit constituent elements.

Even though generally being more time consuming and costly, functional tests are still the dominant approach [5, p. 312]. This is mainly due to their independency over today's impractical analog fault models. In addition, functional testing also permits to calibrate and compensate the mixed-signal circuit performance [25, p. 740], which is not possible by means of structural testing.

Despite the today's dominance of functional testing over structural testing, the debate about which of the approaches is the best dates back to a long time and is still recurrent [26, p. 302] [25, p. 705]. Perhaps, as happens in other situations, the most viable solution may fall in the between of the two extremes.

Chapter 3

Research Question

In this chapter, in Sec. 3.1, the main problem addressed by this work is introduced in more detail. In Sec. 3.2, we present the research question that guides the work and, finally, in Sec. 3.3, we derive some preliminary observations.

3.1 Problem Introduction

Currently, the testing of high speed ($>$ 100 MS/s) and moderate resolution ($<$ 12-bit) ADCs poses a remarkable challenge for mixed-signal IC manufacturers, and the near future scenario tends to get worse with the trends towards higher conversion rates, higher resolutions, and more complex IC integration levels.

As we have seen in Sec. 2.5, the ADC under test interfaces with a socket soldered on a board, which, in turn, interfaces with the tester. The tester must provide quality test stimuli to the DUT and capture the DUT responses for analysis, ultimately qualifying the ADC as good or bad for a given set of functional specifications. The inaccuracies introduced by testing, e.g. noise and distortion extrinsic to the ADC, must be inferior to those introduced by the DUT itself. This ensures a high quality and reliable testing.

From the above test procedure, the following challenges become apparent. First, as the bandwidth and resolution of the ADCs keep increasing, the interfaces between the ADC and the tester become more and more complicated. The test stimuli and test responses should be sent to and received from the DUT without any corruption. This ideal condition is not fulfilled in practice because traces and cables parasitics and signals crosstalk between traces and cables corrupt the desired signals. In addition, most signal synthesizers generate single-ended signals, while most ADCs use differential ones, at least for the analog input signals, to cope with among other things the lower supply voltages which would otherwise severely degrade the ADC dynamic range. Hence, transformers, or even more tricky devices or circuits, mounted on the interfacing board (PCB or DIB) usually do the required single-ended to differential conversion. These differential signals are then carried to the ADC by means of two well-matched traces. However, any mismatch between these traces also corrupts the signals. Furthermore, the electrical connection between the DUT and the DIB through a socket, in production testing, does not perform as well as a DUT soldered directly onto the PCB, which leads to additional sources of error [6, p. 19].

Second, the signals generated for and captured from the DUT must be of acceptable

quality to result in a reliable test procedure. The interfacing problems discussed above add to this challenge, since they introduce unpredictable nonidealities. Therefore, the tester must generates low distortion and low noise signals. As an option, a filter may be interposed between the tester terminals and the transformer inputs to relax the requirements on the signal generators. However, high-order (i.e. high-quality) filters are bulky and hard to mount on the interfacing board, and usually lack flexibility (i.e. they are normally tuned to a particular frequency band). In addition to noise and distortion, time (or phase) synchronization between the analog input and clock signals is crucial to achieve, for example, coherent sampling (as discussed in Sec. 2.3). This avoids collecting redundant samples and, consequently, shorts the test application time. However, high speed signals interfaced between the DUT and the tester are complex to synchronize, and the circuitry present in the path of the signals contribute to additional phase noise (or timing jitter).

Third, high speed, low distortion, and low noise signal generators, if feasible and available in the tester, are very expensive. Advanced signal generators of this type may cost more than US$ 1M [5, p. 10]. Regarding the digital part of the tester, the cost increases proportionally to the number of probing pins with a cost rate of about US$ 3,000 per pin [5, p. 10]. If we add to the total tester's cost, the tester's depreciation and maintenance as well as the operating costs, the test procedure for an uninterrupted tester may cost as much as 5 cents/second [6, p. 19] [5, p. 11]. Usually, the testing time for a mixed-signal IC falls in the 3 to 6 seconds range [5, p. 12], therefore the production testing cost for such an IC may be as high as 30 cents. Since bad tested ICs are not sold, their test cost must be recovered from the sales of good ICs. If the process yield is 75 %, for example, then the test component of the sale price of a good mixed-signal IC is about $30/0.75 = 40$ cents [5, p. 11]. At a glance, this test cost per device seems not so high, however, multiplying this cost by tens or hundreds million fabricated devices, the total cost easily reaches a considerable and concerning amount. Therefore, the test application time and equipment costs must be reduced to lower testing costs.

With the proliferation of SoCs, with less intensity SiPs and, recently, 3D ICs, the controllability and observability of important signal nodes are becoming progressively more restricted. The number of input/output (I/O) pins do not increase linearly proportional to the number of transistors confined within the same IC. As a rough estimative, consider a square IC with lateral dimensions d. The number of pins, N_{pin}, is proportional to $4d$, while the number of transistors, N_t, is proportional to d^2. Hence, $N_{\text{pin}} \propto \sqrt{N_t}$ as defined by the Rent's rule [5, p. 13]. However, these levels of integration are of paramount importance to create higher value systems in the *More Moore* and *More than Moore* approaches [8, see "More-than-Moore" White Paper].

An ADC embedded into a SoC, SiP, or 3D IC cannot, in general, be tested following the approaches shown in Fig. 2.9, because it is unlikely that all needed I/Os will be externally accessible for the conventional test application. Hence, one alternative is to incorporate on-chip, along with ADC itself, testing circuitry to improve the ADC testability.

3.2 Research Question

Aware of the current and envisaged challenges related to the testing of high speed and moderate resolution ADCs, be it embedded into a system or in a stand-alone IC, in this work we pursue an answer for the following key question:

- *How a feasible, reliable, and low cost test for high speed and moderate resolution ADCs can be achieved?*

By answering this question, we will contribute to remove or alleviate some of the problems discussed in the previous section.

3.3 Preliminary Observations

In order to understand the fundamental reasons behind our approach, which is conceptually explained in Chapter 5, and also delimit a fertile research space for the literature review that follows in the next chapter, we provide some preliminary observations here. These observations are a result of a first effort (focusing) towards an adequate solution to the research question posed above.

The first relevant observation to highlight is the reliability and cost of the manufacturing processes, considered the CMOS process throughout this work, although most of the ideas are not restrict only to this particular case. As the CMOS technology evolves, the cost to integrate transistors and other devices on-chip decreases remarkably. Hence, more and more specific functionalities can be integrated on-chip very affordably. On the other hand, the reliability of the manufacturing process maintains high, allowing reliable function to be implemented on-chip as well.

The above trend has favored the implementation of test-related functions directly on-chip during the IC design phase. This practice, designated as design for testability (DfT), evolved firstly for purely digital ICs and then migrated to mixed-signal devices. Although there exist several DfT alternatives available today, the BIST solution, due to its inherent advantages, is the most appealing one [5, p. 44] [6, p. 19] [9, p. 97] [8, p. 36 of the Test & Test Equipment Chapter].

According to [27], BIST is "*any of the methods of testing an IC that uses special circuits designed into the IC. This circuitry then performs test functions on the IC and signals whether the parts of the IC covered by the BIST circuits are working properly*".

Since the BIST circuitry is integrated with the DUT, in this particular case an ADC, on the same IC, it naturally enhances the accessibility to internal nodes of an embedded ADC. The close proximity of the testing circuitry to the ADC itself removes most of the interfacing problems discussed in Sec. 3.1. Also, given that the essential test functionalities are integrated on-chip, more inexpensive testers can be used. Furthermore, the testing may be performed from time-to-time during field operation to verify if the device is still complying the intended requirements.

On the other hand, the BIST circuitry contributes to additional area, increases design time and effort, and may degrade the performance of the DUT due to intrusive test structures.

Table 3.1: Summary of advantages and disadvantages of BIST.

Advantages	**Disadvantages**
vertical testability (wafer to system)	area overhead
high diagnosis resolution	performance penalties
full-speed testing	additional design time & effort
reduced need for external test equipment	additional risk to project
reduced test development time & effort	
reduced manufacturing test time & effort	
reduced time-to-market	

A more in depth discussion about the advantages and drawbacks of BIST, including the ones shortly mentioned above, is found in [20, pp. 12–14]. Table 3.1 summarizes the key points.

Given the above observations, it becomes clear that a wise solution for the research problem considered in this work should incline towards some kind of BIST solution. We elaborate more on this in the next chapters.

Chapter 4

Literature Review

In this chapter, the open literature is reviewed to identify the strengths and weaknesses of existing BIST approaches for ADCs, and to demonstrate the novelty of our approach, which is considered in the following chapters. In Sec. 4.1, we review relevant structural (defect-oriented) BIST techniques applied to ADCs, and, in Sec. 4.2, we extend the analysis, with more emphasis, to functional (specification-oriented) BIST methods, given that they are the main focus of this work.

4.1 Structural Built-In Self-Test for ADCs

Although structural BIST approaches are not the focus of this work, it is still insightful to consider some relevant examples in this section. As we pointed out in Sec. 2.6, the lack of widely accepted analog fault models and means of relating structural faults to functional specifications are the main difficulties preventing ample adoption of these methods.

When an ADC and DAC coexist into the same IC (e.g. in a SoC system), we can connect the output of the DAC to the input of the ADC and implement an almost completely digital BIST approach, as shown in Fig. 4.1. The digital BIST circuitry includes a test stimulus generator (TSG), an output response analyzer (ORA), as well as a test controller. Depending on the state of multiplexer MUX_2, the input of the DAC is driven by the test stimulus or the normal input. In test mode, a digital test stimulus is applied to the DAC and its analog output is sent to the input of the ADC by appropriately configuring multiplexer MUX_1. The digitized signal is returned to the ORA through MUX_3 and then, after digital processing, the ORA decides whether the devices under test pass the test or not. It is also important to connect the output of TSG to the input of the ORA to test the digital part of the BIST circuitry before testing the DAC and ADC. This explains the need of multiplexer MUX_3. Given that the path of the test stimulus forms a loop from the TSG to the ORA, this approach is commonly referred as DAC/ADC loopback BIST, or simple DAC/ADC BIST [6, p. 572].

The only analog component required by the DAC/ADC loopback BIST approach is the analog muxtiplexer MUX_1, hence the operation and performance of the analog portion of the mixed-signal system is not affected substantially. Another important benefit of this approach is its almost all digital nature, which facilitates its implementation (following an automated digital design flow), and self-testing (using well-established digital BIST circuitry). Conversely, since the DAC may somehow compensate some imperfections

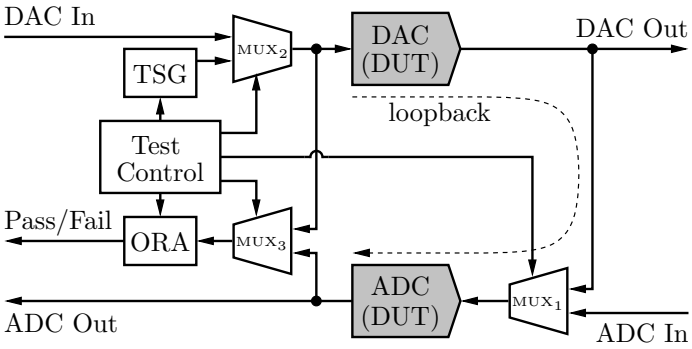


Fig. 4.1: DAC/ADC loopback BIST architecture.

of the ADC, this method is only useful for a coarse evaluation of the ADC or DAC. Furthermore, this method requires an DAC/ADC pair which, sometimes, is not available into the same chip.

One of the first proposals relying on the DAC/ADC loopback BIST technique is presented in [28], and is called hybrid built-in self-test (HBIST). Both the TSG and ORA are built with a linear feedback shift register (LFSR), as often found in the digital circuitry testing realm. The LFSR-based TSG generates pseudo-random digital patterns that look similar to white noise when passed through a DAC. The output of the ADC is applied to a LFSR-based ORA for signature analysis. However, contrary to digital circuits, it is unlikely that a fault-free mixed-signal circuit will produce exactly the same signature over consecutive executions of the BIST sequence due to noise (e.g. thermal, quantization, jitter, etc.) and process, supply voltage, and temperature (PVT) variations. Hence, the determination of fault-free signatures using traditional digital techniques is unpractical to mixed-signal circuits. To surpass this difficulty, it is proposed in [28] to eliminate the LSBs from the analysis. Nevertheless, the LSBs are the bits most sensitive to manufacturing process variation and, hence, contribute significantly to the testing quality [26, p. 306].

Improved ORA implementations as well as additional test stimuli, in addition to the widely used pseudo-random patterns, have also been proposed. In [29], for example, the ORA is implemented with a double precision accumulator that averages out the response deviations from the output of the ADC caused by noise and PVT variations. The ORA may also accumulate the absolute value of the difference between the input test stimulus and the output response. With these improvements, it is possible to determine a range of good circuit BIST signatures and, therefore, enhance the detection of faults. In addition to pseudo-random test stimuli, the work in [29] also implements ramp, saw-tooth, triangular, step, pulse, and DC waveforms, as well as frequency sweeps using a square wave. This diversified set of test stimuli permits a high fault coverage in a wide range of analog and mixed-signal circuits[1].

Since there is an intricate correspondence between fabrication faults and the output response of the DUT, it may happen, for example, that one fault compensates for another. In this situation, a range of good circuit BIST signatures may overlap with a range of

[1]For instance, after the DAC/ADC are tested, other analog circuits may be interposed between them for testing; however, this is outside the scope of this work.

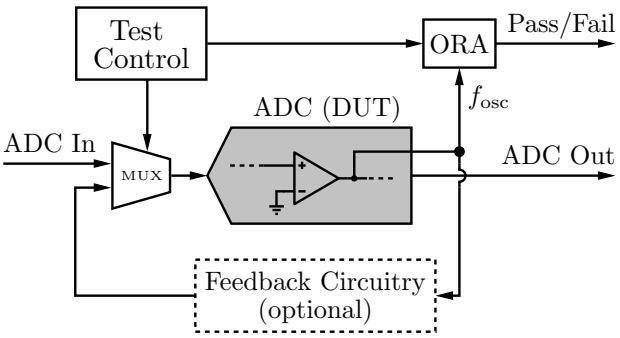


Fig. 4.2: Oscillation BIST architecture.

faulty signatures, compromising fault detection. This is an inherent problem associated with structural testing.

A radically different structural BIST approach, called oscillation built-in self-test (OBIST), is presented in [30] and shown in Fig. 4.2. The technique is an extension of the oscillation-based test methodology, proposed by the same authors [31], and because of its simplicity it has attracted considerable attention from the design and test community in the past years. The key idea of the method is to transform the DUT into an oscillator, measure its oscillation frequency, f_{osc}, and compare the measured oscillation frequency with a predetermined range (test signature). If the measured oscillation is within this range, the DUT is fault-free; otherwise, it is considered faulty. The ORA consists of a frequency-to-number converter, which is built using a level-crossing detector and a counter, and a digital comparator. A test controller directs the BIST sequence and configures the input multiplexer. For particular circuits, it is necessary to add some kind of feedback circuitry to sustain oscillation.

The range of good test signatures is found by means of fault modeling and simulation as well as Monte Carlo analysis over the tolerances of the component values (resistors, capacitors, transistors, etc.). As previously noted, some faults may compensate others having a negligible impact on the oscillation frequency. Likewise, some faults (e.g. parametric variations of a component) may be transparent to the oscillatory behavior of the DUT. However, despite these problematic scenarios, it has been shown high fault coverage for some ADC types [30, 31].

The main advantage of the OBIST is that no TSG is necessary. The test response is generated by the DUT itself (sometimes aided by extra circuitry to configure the DUT into an oscillator). The output response carrying the f_{osc} information can be treated as a digital signal. Hence, a very small area overhead and fully digital BIST is possible. In addition, given that the BIST circuitry is digital, it can be self-tested using digital methods prior testing the ADC. One of the weaknesses of the approach is how the DUT is modified, possibly adding extra elements, to achieve reliable oscillations. Without a well defined oscillatory behavior, the test results may be misleading. Additional circuitry, specially in critical signal paths, may deteriorate the performance of the ADC.

The OBIST approach has been applied with more intensity to integrating [31] and delta-sigma ($\Delta\Sigma$) [32, chap. 4] ADCs, perhaps motivated by the structure of these type of converters, which facilitates their reconfiguration into an oscillator. Recently, researchers begin to take other parameters of the oscillating signal (e.g. the amplitude) into consid-

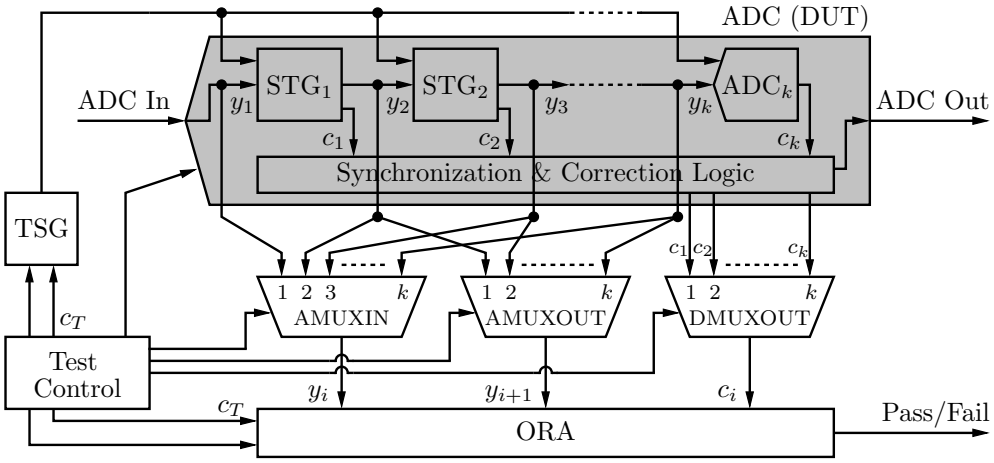


Fig. 4.3: Structural BIST architecture for pipelined ADCs.

eration to achieve more accurate and relaxed testing [32, p. 7].

Structural BIST specifically applied to pipelined ADCs is proposed in [33]. The approach relies on testing the pipelined stages separately in order to detect any fault within them that can lead to ADC malfunctioning. To this end, the analog input and output as well as the digital code of every stage must be accessible to the ORA. This accessability is enabled, respectively, by analog multiplexers AMUXIN and AMUXOUT and a digital multiplexer DMUXOUT, as shown in Fig. 4.3. For the ith pipelined stage, its analog input and output are represented by y_i and y_{i+1}, respectively, and its digitized code by c_i. Appropriate dc test stimuli, with coarse precision, need to be applied to the input of every stage under test. A test controller directs the state of the multiplexers, the reconfiguration of the stages, the on-chip TSG, and the ORA operation.

The technique is based on the reconfiguration of each stage under test as an ADC-DAC block and on the application of a set of dc analog stimuli corresponding to specific levels of the stage transfer characteristic. Considering the testing of the ith stage, first its multiplying digital-to-analog converter (MDAC) is converted into a DAC, called mDAC. A structurally similar DAC, called DACT, is available in the ORA. A dc test stimulus, associated with code c_T, is applied to the sub-ADC of the ith stage, which, in turn, generates code c_i for both the mDAC and DACT inputs. The outputs of mDAC and DACT, y_{i+1} and y_T, respectively, are compared using an analog window comparator also available in the ORA. When both values differ more than the tolerance level defined by the comparator window width, an output test signal will indicate the existence of faults in the MDAC. Faults in the ith sub-ADC are detected comparing codes c_i and c_T through a digital comparator present in the ORA.

The primary advantages of this approach are small area overhead and a TSG without stringent accuracy requirements, for example, it may be implemented with a simple resistive network. On the other hand, many circuit modifications are needed to apply the test and also critical signal nodes must be accessed for testing purposes. This adds parasitics and noise that surely will degrade the performance of the ADC, specially for high speed applications.

4.2 Functional Built-In Self-Test for ADCs

Contrary to structural testing methods, functional BIST techniques are more often employed by design and test engineers mainly because they evaluate specification-related performance parameters, instead of detecting particular manufacturing defects. Also, most functional techniques treat the ADC under test as a "black box", which contrasts with most structural BIST approachs, where internal signal nodes are accessed and, in some cases, even the circuitry of the DUT are modified during testing. Despite of these aspects, in general, functional self-test approaches require more elaborate and complex stimulus generators and output response analyzers. In this section, we firstly review, in Sec. 4.2.1, BIST approaches able to determine static performance parameters of an ADC, as discussed earlier in Sec. 2.2. Next, in Sec. 4.2.2, we survey BIST techniques related to the dynamic performance of ADCs. The dynamic performance parameters, as introduced in Sec. 2.3, are directly and more appropriately related with high speed ADC testing, the focus of this work.

4.2.1 Static Performance BIST Methods

As referred in Sec. 2.2, the static performance parameters of an ADC are related with the actual code transition levels of its transfer characteristic, which, in turn, are often found using feedback loop, ramp histogram or sine wave histogram testing. As a result, most of the BIST methods discussed below explore some features of these approaches.

The histogram-based analog built-in self-test (HABIST) presented in [34], and shown in Fig. 4.4, is an example where histograms are extensively employed to obtain offset, gain, noise, and distortion parameters of a DUT. For the case of an ADC, the method generates an expected histogram at the output of the converter for a known test stimulus, e.g. a sine or saw-tooth wave. The expected histogram may be generated using a CAD software, e.g. through a SPICE simulation, or experimentally evaluating a "golden ADC". This histogram is then stored in a memory on-chip as a template. The range of variation of offset, gain, noise, and distortion that will be tolerated when comparing the template histogram with the measured histogram of the DUT are derived simulating the manufacturing tolerance limits of the circuit parameters, for example, using a Monte Carlo analysis. These variations allow to determine acceptable test signatures for a given test stimulus. During test application, the same test stimulus used to obtain the template histogram and the range of variation for the performance parameters of interest stimulates the ADC, and a histogram is generated at its output. This histogram is then processed using a special algorithm and the template histogram. This process generates test signatures that describe the difference between the actual and template histograms. If these signatures are within predefined ranges, the DUT is classified as fault-free (or faulty if the predefined range refers to an unacceptable variation).

This approach also permits high level diagnosis if a library of fault symptoms exist. For example, suppose that the difference histogram has higher code counts in its extremes when stimulated by a sine wave. This indicates that clipping is occurring, and this may be associated with several imperfections of the DUT listed in a library. After the ADC is tested, it is also possible to reuse the tested ADC and the BIST circuitry to apply histogram-based testing to other analog circuits included into the same chip.

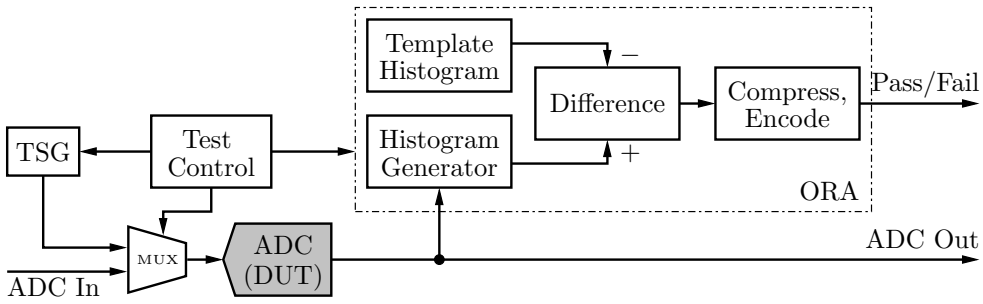


Fig. 4.4: HABIST architecture.

One advantage of the HABIST method is its capability to diagnose the causes of some testing abnormalities, although this is done heuristically. On the other hand, the algorithm to process the histograms and derive the test signatures, as well as the memory elements required on-chip to store the histograms, may entail a substantial area penalty.

One crucial requirement for histogram-based BIST is the availability of on-chip ramp or sine waves with high linearity. These test stimuli are the most common to derive histograms. Sine waves are usually generated with some oscillator circuit followed by a filter. However, for low frequencies, it may be more costly to integrate on-chip a sine wave generator than a ramp generator[2]. Therefore, several researchers have addressed the issue of on-chip slow ramp generation. For example, different adaptive schemes are used in [35, 36] to calibrate the ramp signal, achieving simulated linearities up to 15 bits for slow ramps. Although in both works it is claimed the proposed generators are highly insensitive to process variations, the much lower performance measured (e.g. only 11 bits in [35]) does not corroborate these arguments. Despite of this, ramp generators, specially for low frequencies, are widely used for BIST schemes aimed at testing the static linearity of ADCs.

Instead of accumulating an output histogram, which may be costly in terms of implementation hardware, some researchers proposed a simplified polynomial-fitting method to determine offset, gain, and second and third harmonic distortion [37]. Central to this method is a highly accurate test stimulus comprising a four-segment staircase-like exponential waveform proposed by the same authors in [38], as illustrated in Fig. 4.5b. This test stimulus is generated using a digital pulse width modulation (PWM) synthesizer, with only five different duty cycles, followed by a simple first order low-pass active filter (implemented off-chip). The ADC under test then digitizes the rising and falling edges of the exponentials (as shown by the shaded regions in Fig. 4.5b), which are evenly distributed over four equal segments of the full-scale range of the ADC. The samples from each of these segments are accumulated and combined in the ORA to produce four sums: S_0, S_1, S_2, and S_3, where $S_i = S_{\mathrm{r}i} + S_{\mathrm{f}i}$ for $i = 0, \ldots, 3$. These sums can be related to a third order polynomial of the form $y = b_0 + b_1 x + b_2 x^2 + b_3 x^3$, which is assumed sufficient to fit the transfer characteristic of the ADC, and the polynomial coefficients are used to estimate offset, gain, and harmonic distortion [37].

The primary advantages of this approach are its accuracy in the presence of noise

[2]For example, considering an LC oscillator, its oscillation frequency, f_{osc}, is $1/(2\pi\sqrt{LC})$. Hence, for generating lower frequencies we need larger LC tanks, which entail larger silicon area and fabrication cost.

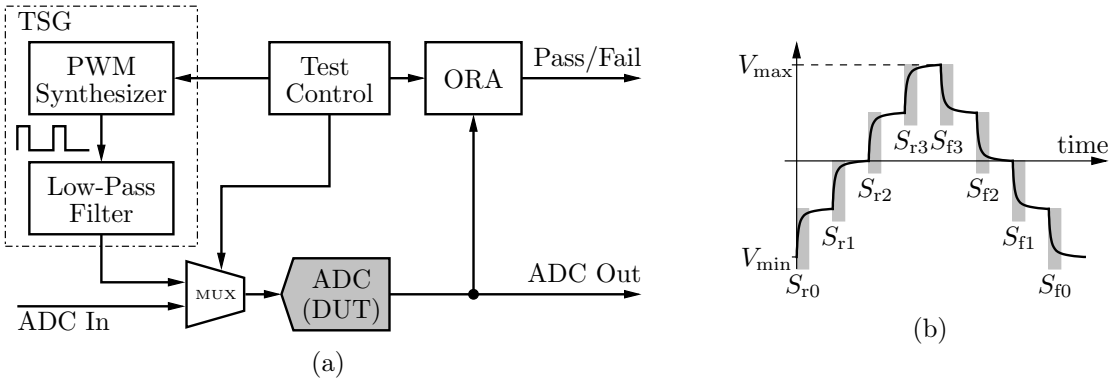


Fig. 4.5: Polynomial-fitting BIST architecture (a) and low-pass filtered test stimulus (b).

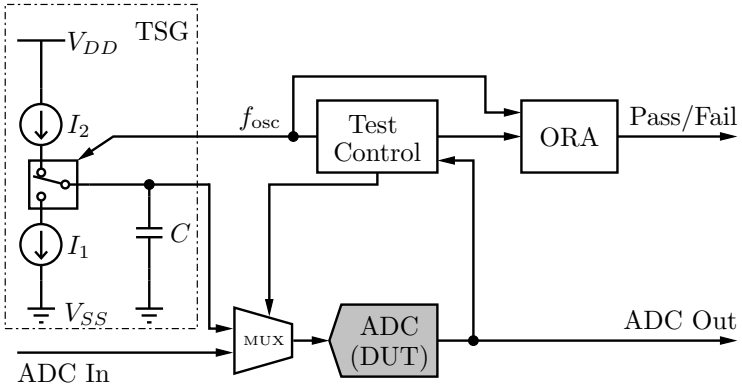


Fig. 4.6: OBIST architecture applied to functional testing.

and its simple implementation. On the other hand, the need for an accurate off-chip active filter is one drawback. In addition, this method is particular useful for $\Delta\Sigma$ ADCs, which are inherently noisy and have a monotonic transfer function. A more intricate A/D transfer characteristic cannot be suitably fitted by a simple third order polynomial.

The OBIST technique discussed in Sec. 4.1 for structural self-testing of ADCs can also be extended to functional DNL and INL testing of ADCs [30]. In this case, the method is independent of the internal structure of the DUT and hence it can be applied to any type of A/D converter. The approach is illustrated in Fig. 4.6 and it is similar to the traditional feedback loop testing. However, instead of using an accurate DAC (with greater accuracy than the ADC under test) in the feedback path and inferring the code transition levels of the ADC from the digital input of the DAC, the OBIST approach deduces the functional performance by evaluating the oscillation frequency f_{osc} of the control signal of the switch used to generate the test stimulus. Therefore, the implementation of the method entails less area overhead. The test controller monitors the output of the DUT and forces it to oscillate between two predefined codes by controlling a switch responsible for charging or discharging a capacitor C, with current sources I_2 and I_1, respectively. When steady oscillation is achieved, the ORA extract the value of f_{osc} and relates it with the DNL and INL of the converter. If the found values are within the tolerance ranges, the converter meets its nonlinearity specifications and is qualified as a good device regarding these performances.

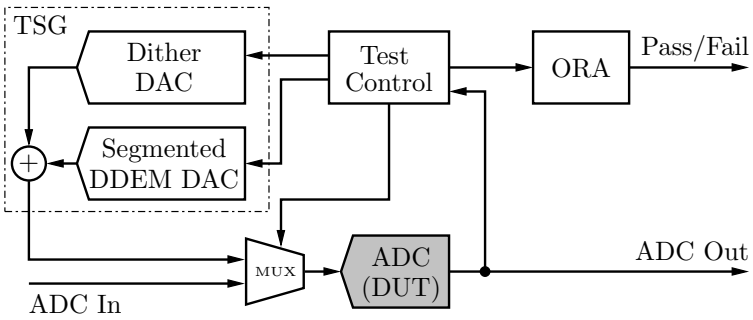


Fig. 4.7: BIST architecture using low accuracy DACs for test stimulus generation.

Although apparently much more straightforward than the conventional feedback loop testing, the OBIST technique still requires an accurate symmetrical triangular waveform at the input of the ADC under test. Hence, the current sources, which are probably the main source of error, must be well matched against PVT variations. Also, the integrating capacitor must be linear, i.e., its temperature and voltage dependence coefficients must be very small. If these requirements are not fulfilled, the positive and negative slopes of the test stimulus will be different and the results will become inaccurate. It is due to these weaknesses, certainly, that the functional OBIST have attracted much less interest than its structural counterpart.

The main bottleneck of integrating on-chip a traditional feedback loop testing for ADCs is the need for a high accuracy DAC. It is possible, however, to build a high accuracy DAC using low resolution and low accuracy ones incorporating special techniques. In [39], for example, deterministic dynamic element matching (DDEM) and dithering are combined to achieve a high accuracy DAC. As shown in Fig. 4.7, the output of a DDEM reconfigurable segmented current steering DAC is added to the output of a dither DAC to generate the test stimulus. With 7-bit linearity DACs it is possible to generate a test stimulus featuring about 15 bits of linearity [39].

These low accuracy DACs are used in a BIST scheme (shown in Fig. 4.7) to perform INL testing. During test application, INL values related to all ADC codes may be evaluated or, alternatively, INL values may be found to critical codes depending on the architecture of the ADC under test. The choice between the two approaches will affect the overall testing time. In either case, and for a predefined code, say code k, the test controller applies the digital codes to the dither as well as to the segmented DDEM DAC. The codes applied to the latter DAC also account to its reconfigurability through the DDEM technique. There are P reconfigurability options for the segmented DAC and N_d distinct input codes for the dither DAC. Therefore, for each code k, the test controller finds N_dP estimates for the digital input of the segmented DAC that correspond to code k. These estimates are found using binary search, to accelerate the searching process, and monitoring the output of the DUT. If the output is below code k, the binary search is interrupted, the estimate is stored, and a new estimate is found. After all estimates are derived, they are averaged to obtain the equivalent code transition level associated with code k. This averaged code is sent to the ORA for later use. This process is repeated for a preestablished set of ADC codes, and, finally, the INL profile is determined.

This technique, even though using low accuracy DACs, provides high accuracy measurements because of estimates average. However, there is a trade-off between test ac-

curacy and test application time, since increasing the number of estimates increases the overall searching process time. Hence, the best compromise must be identified considering the intended application.

Instead of using deterministic test stimuli (e.g. sine wave or ramp), some researchers also explored the possibility of using random noise to this end. In [40], for example, a white noise generator with a bandwidth of about 4 kHz is used as TSG to test the linearity of an ADC under test. The INL and DNL are obtained by means of spectral analysis, thus reducing the number of required ADC output samples with respect to a histogram testing. The spectral analysis is carried out in the ORA with a digital signal processor executing FFT. The same authors also propose to use this BIST approach to estimate the dynamic performance of the ADC, and some results with good agreement with conventional test methods are presented in [41], though apparently for low speed converters (about 10 kS/s).

Another noise-based BIST approach is proposed in [42]. The main differences with respect to [40] are the use of Gaussian noise for test stimulus and the ORA implementation, which is based on histograms and lookup tables to derive the DUT nonlinearities. The implemented noise generator has a bandwidth of about 10 MHz and hence the INL and DNL contain some dynamic effects of the A/D conversion.

The primary advantage of noise-based methods is the implementation simplicity of the TSG, which is robust against surrounding noise (critical in SoC applications, for example) and leads to a small area overhead. Also, coherent sampling is not required during testing. On the other hand, particularly in [40], a huge amount of samples is needed to achieve statistical significance for the measurements. Another shortcoming is the generation of noise with larger bandwidths, which may be challenging.

4.2.2 Dynamic Performance BIST Methods

Throughout Sec. 2.3 we discussed the dynamic performance parameters commonly used to characterize ADCs. It may be note that most test methods rely on accurate sine waves for test stimulus, and spectral analysis (mainly by means of FFT) or sine wave fitting for output response analysis. Sine waves are widely employed because it is relatively easier to synthesize a high frequency and accurate (pure) sine wave than other waveforms. Spectral analysis, among the techniques available for response evaluation, gives the richest set of information, thus it is quite usual. Hence, most of the BIST techniques presented next aim at providing feasible solutions for on-chip integration of sine wave generators and spectral analyzers.

The mixed analog-digital built-in self-test (MADBIST) method proposed in [43] exploits an intensive digital implementation of the test stimulus generator, since this block is one of the most challenging to be implemented in a fully on-chip BIST technique for ADCs. Although the approach was originally devised for $\Delta\Sigma$ ADCs to take advantage of existing hardware for testing purposes, it may be extended to other converter architectures as well. A simplified MADBIST approach intended for ADC testing is illustrated in Fig. 4.8. The TSG comprises a fully digital $\Delta\Sigma$-based oscillator which uses oversampling and noise shaping to generate a spectrally pure sine wave within the frequency band of interest. The amplitude, frequency, and phase of the sine wave can be easily adjusted digitally. The digital bitstream at the output of the oscillator, which has two levels, is

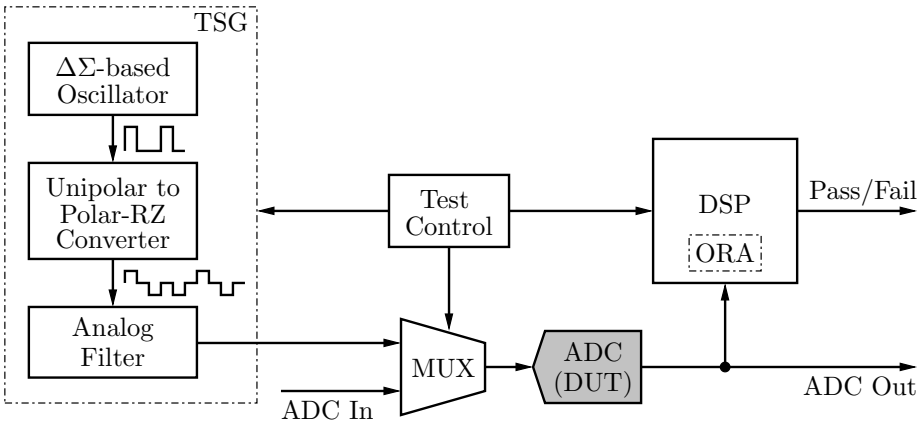


Fig. 4.8: Simplified MADBIST architecture for ADC testing.

converted to a polar return-to-zero (RZ) encoding in order to reduce the distortion of the generated test stimulus. The out-of-band noise of the polar-RZ encoded signal is removed by a simple and low accuracy analog filter, which may be the anti-aliasing filter preceding the ADC, if it is available on-chip (in Fig. 4.8 we consider a dedicated filter).

The proposed approach is able to test SINAD, frequency response, and gain tracking for a given ADC under test. For frequency response, the frequency of the test stimulus is swept within the band of interest while the amplitude is maintained constant. On the other hand, the frequency of the test stimulus is kept constant while the amplitude is varied to measure the gain tracking. In [43] three output response methods are considered: spectral analysis through FFT, sine wave fitting, and narrow-band filtering. The two former methods, with emphasis on spectral analysis, are mentioned in Sec. 2.3. The FFT approach returns a vast and rich content, however, its implementation demands the highest computational power of the three methods. Although the sine wave fitting technique alleviates the computational resources required relatively to an FFT processor, the simplest method is the narrow-band filtering.

The filtering approach uses a narrow-band bandpass response simultaneously with a notch response to separate the signal and noise. The method is based on a time-recursive implementation of an arbitrary transform (e.g. an FFT), and thus removes the need for on-chip sine and cosine values usually stored in a lookup table and the need for capturing all samples into a memory before computing an FFT or a sine wave fitting. The filtered sine signal emerges from the bandpass output, while the total noise emerges from the notch output. The bandpass and notch responses are centered at the input test stimulus frequency. Signal and noise powers are obtained by accumulating one sum and two squared-sums over consecutive samples [43]. One drawback of the narrow-band filter approach is that neither the bandpass nor the notch response are ideal, i.e. sharp enough to allow passing only the sine signal and the noise, respectively. Therefore, the actual bandpass response will pass the sine signal as well as some adjacent noise. Likewise, some amount of noise will not pass the notch filter. Consequently, these limitations lead to biased measurements. Another problem associated with the filter approach is that some time interval has to be reserved for the filter to reach steady state. Hence, initial samples must be discarded. Nevertheless, a judiciously placement of the filter poles can make the bias as well as the settling time of the filter negligible in practice [43].

Overall, the MADBIST approach benefits from its mostly digital implementation, which is robust against PVT variations and can be self-tested using digital methods. In addition, high test accuracy is possible and the approach may be extended to other on-chip analog and mixed-signal blocks. For instance, after successfully testing the ADC, it can be used as a calibrated device to test a DAC, and the two combined can test other analog circuits on-chip (this broad scenario is not illustrated in Fig. 4.8, where we focus on ADC testing). In contrast, the on-chip implementation of the technique entails a considerable area overhead, unless available on-chip resources can be reused [44]. The analog filter, though of low accuracy, may be of third order or more, thus leading to additional area if an anti-aliasing filter is not available on-chip. Furthermore, due to oversampling, high frequency test stimuli are not easy or even possible to generate.

Another limitation of the MADBIST method, when using a narrow-band digital filter as the ORA, is the impossibility of computing the THD, for example, since multi-tone measurements are needed in this case. Also, the possibility of generating multi-tone test stimulus would allow to measure the intermodulation distortion (IMD) and multi-tone frequency response of the ADC under test. With these concerns in mind, the MADBIST approach was extend in [45] to cover multi-tone test stimulus generation as well as multi-tone measurement of the DUT's output response. A multi-tone test stimulus is generated extending the idea of the digital $\Delta\Sigma$-based oscillator, i.e. by simultaneously generating multiple tones and summing the $\Delta\Sigma$ modulated bitstreams by time-interleaving. In the ORA side, multiple single stage narrow-band digital filters, each of which tuned for a particular test stimulus frequency, can be combined to produce a narrow-band multi-output digital filter. The number of filter outputs will be dictated by the number of tones considered at the output of the ADC. For instance, to measure the THD up to the fifth harmonic, a digital filter with five outputs is required. In this situation, the fundamental component of the sine wave emerging from one of the five narrow-band bandpass response outputs is related, in terms of signal power, to the four harmonic components coming from the remaining bandpass outputs.

Instead of using a $\Delta\Sigma$-based oscillator for test stimulus generation, which may be difficult to design and may represent a significant area overhead, it is possible to periodically reproduce a short optimized bitstream recorded from the output of a $\Delta\Sigma$ modulator [46]. In this case, a variety of test stimuli (e.g. single- and multi-tone sine waves, triangular waves, Gaussian pulses, etc.) can be generated, since the optimized bitstream for a particular signal is derived in software. The software generation, in contrast to traditional hardware modulators, benefits from several aspects. First, the complexity and stability issues associated with the order of the modulators are not a paramount concern. The complexity of designing a higher order modulator in software is almost similar to that of designing a lower order one. The software modulator does not need to be stable in the classical sense, only stable long enough to acquire a sufficient number of points to create the bitstream [46]. Second, when using a bandpass modulator to generate higher frequencies than a low-pass one, the center frequency is selected in practice to be $f_s/4$ to ease the hardware implementation. Conversely, software modulators can use any arbitrary center frequency, from dc to $f_s/2$. Finally, the finite-length bitstream can be optimized taking several performance parameters, e.g. SFDR, SINAD, etc., into account.

The basic circuit of the finite-length bitstream based TSG consists of a one-bit shift register with the output fed back to the input, a one-bit DAC, and an analog filter, which

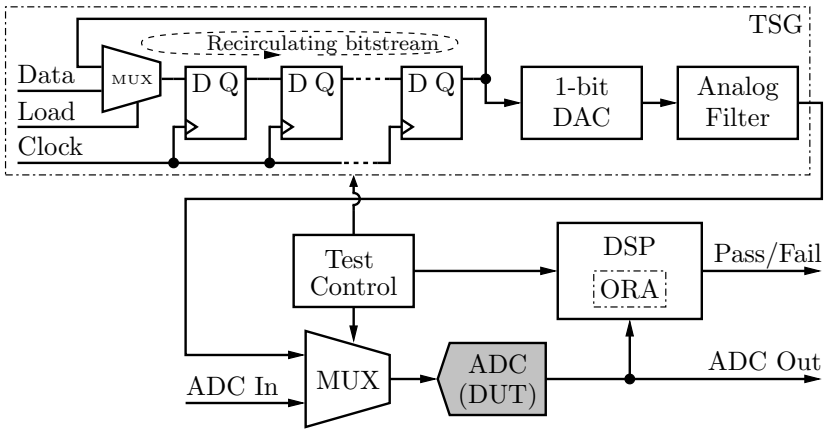


Fig. 4.9: Finite-length bitstream based test stimulus generator for BIST of ADCs.

may be an anti-aliasing filter, as previously observed. Fig. 4.9 shows the BIST circuitry for testing an ADC following this approach. The length of the bitstream N_{bs} is equal to the number of D-type flip-flops available in the shift register. Initially, the *Load* signal selects the *Data* signal as the input of the shift register. After N_{bs} consecutive rising transitions of the *Clock* signal, the shift register is loaded with the optimized bitstream derived in software. In the sequence, the *Load* signal connects the output of the shift register to its input through the multiplexer, and, for a continuously running clock, the bitstream recirculates periodically. This periodic bitstream is then converted to the analog domain with a simple one-bit DAC, filtered, and used as test stimulus to the ADC under test. The ORA may be implemented, for example, using a narrow-band multi-output digital filter, as mentioned earlier, built into a DSP.

Alternatively to the shift register implementation, the bitstream may also be stored in a random-access memory (RAM) and sent out continuously from the RAM [46]. This is particular useful when a RAM is available on-chip. In addition, the RAM based generator is more flexible than the shift register based one, which can only accommodate fixed length bitstreams. On the other hand, the shift resister implementation can achieve higher speeds of operation due to its simplicity.

As for the $\Delta\Sigma$-based oscillator, the finite-length bitstream approach trades off signal accuracy with signal bandwidth, since in both cases oversampling is employed. As a result, high frequency test stimuli are hardly achieved. Conversely, both approaches are implemented using intensive digital hardware, which is robust against PVT fluctuations and, most important, can be self-tested prior testing the DUT itself employing mature BIST methods commonly available to digital circuitry.

Given that a $\Delta\Sigma$ modulated bitstream would lead to prohibitive sampling frequencies for current CMOS technologies, specially for synthesizing high frequency test stimuli, other methods to circumvent this limitation were proposed. A read-only memory (ROM) used to store ideally digitized samples of an arbitrary test stimulus (e.g. a single- or multi-tone sine wave), followed by a DAC and an analog filter is proposed in [47] (see Fig. 4.10). The digital words/samples to be stored into the ROM are generated in software, where a desired test stimulus is digitized by an ideal ADC (a normal Nyquist ADC without using oversamling). The number of collected samples will be restricted by the ROM size. During on-chip test stimulus generation, the digital samples stored into the ROM are sent

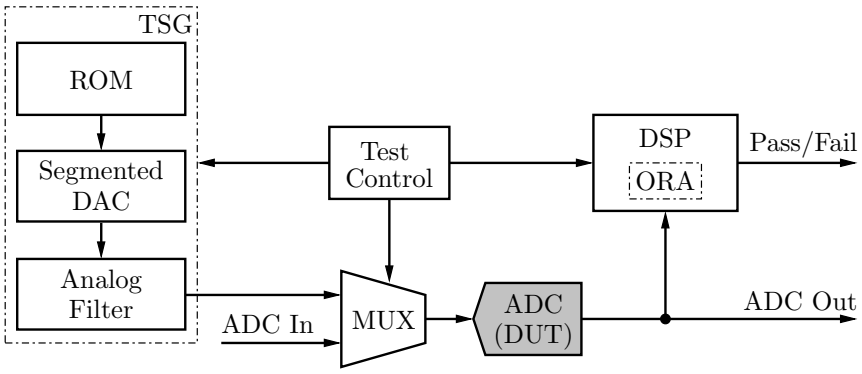


Fig. 4.10: Test stimulus generator based on ROM and DAC for ADC BIST.

out continuously and in a circular fashion (i.e. after the sample stored in the last register is sent out, the next sample will be that related to the first register). These output digital samples are then converted by a DAC. In [47], it is used a segmented current steering DAC to achieve higher conversion speeds. The area overhead of the DAC is reduced using a segmented design with two segments, which has minimal performance degradation. The analog signal emerging from the output of the DAC is filtered and buffered before driving the DUT. If a DSP is available on-chip, a FFT algorithm can be implemented for output response analysis.

The primary advantages of this approach are the flexibility of generating a variety of test stimuli and the capability of synthesizing high frequency stimuli (e.g. in the hundreds of MHz range), although featuring relatively low SFDRs (e.g. around 20 dB at 400 MHz using an 8-bit DAC). On the other hand, the DAC and the analog filter/buffer cannot be easily self-tested prior testing the ADC under test. This means that the test procedure will be somehow inaccurate. Furthermore, the multi-bit DAC, ROM, and analog filter lead to a large area, unless available on-chip resources can be reused. Another specific problem of this BIST architecture is the limited dynamic range at the input of the ADC under test, which is influenced by the dynamic range at the output of the DAC as well as the input and output dynamic ranges of the amplifier used to build the active filter.

An alternative to reduce the area overhead of the BIST circuitry is to reuse on-chip resources when they are available. Based on this philosophy, several BIST methods were proposed. In [48], for instance, a method for self-testing a DAC/ADC pair available in a speech coder-decoder (CODEC) is presented. The test approach is similar to the DAC/ADC loopback self-test discussed previously in Sec. 4.1, but now intended for functional dynamic performance parameters. A DSP, also available in the CODEC, generates the test stimuli and analyzes the output responses. The DSP generates a sine wave with specific amplitude and frequency, and the resulting digital values are stored in a RAM (also part of the CODEC). In the sequence, these data are sent to the DAC, which, during test mode, has its output connected to the input of the ADC by means of a multiplexer, and brought again to the digital domain through the ADC. The digitized samples are then stored in the same RAM and analyzed through a FFT processor. Next, the results are compared with pre-defined limits and the performance of the DAC/ADC pair is consider within specifications or not. To allow measuring the performance of the ADC separately, an off-chip calibrated DAC is used in place of the on-chip one.

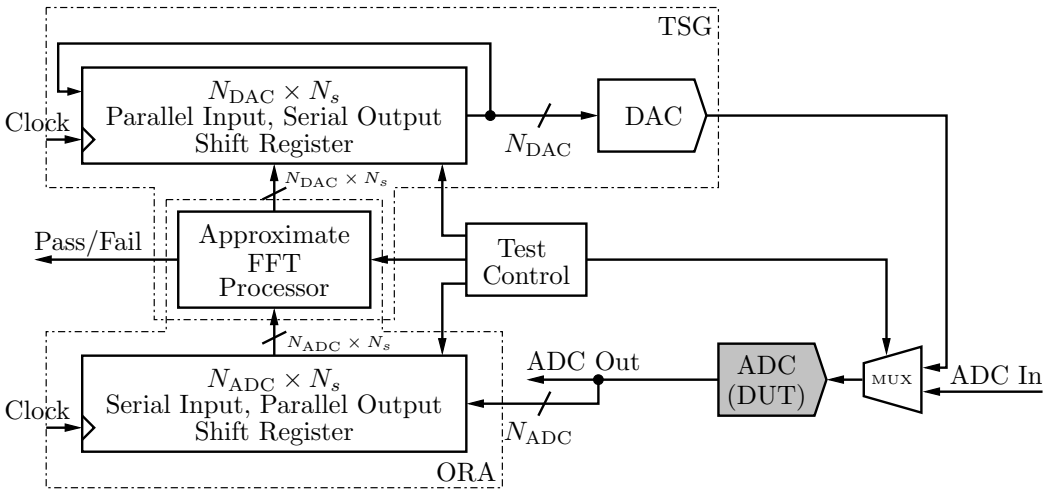


Fig. 4.11: FFT-based built-in self-test architecture.

With this approach it is possible to measure and evaluate the SINAD, frequency response, gain tracking, and other specific characteristics. An interesting conclusion derived in [48], after evaluating 2,000 DUTs, is that the correlation between the test results from the BIST circuitry and those obtained from a mixed-signal ATE is high. That is, the BIST circuitry is a proven alternative to ATEs. By reusing the on-chip resources for testing and releasing them to normal operation after the test procedure, the area penalty is considerably reduced, maybe slightly increasing the complexity of the DUT.

Since the FFT and its inverse differ in a scaling factor $1/N_s$ and a minus sign in the exponent of the kernel function $e^{-j2\pi kn/N_s}$ (cf. Eqs. (2.9) and (2.10) in Sec. 2.3.1), which result in slightly computation differences, some researchers proposed to use the same FFT processor for both test stimulus generation and output response analysis [49]. For stimulus generation, single- or multi-tone sine waves are straightforwardly generated by setting the real and imaginary values of each spectral component composing the signal in the frequency domain. The remaining components, of a total of N_s spectral components for a N_s-point FFT processor, are set to zero. The time domain digital signal is then obtained applying an inverse FFT by means of the FFT processor, which is similar to the FFT computation despite a scaling factor $1/N_s$ (the minus sign in the kernel function can be ignored). In the sequence, this signal is loaded into a shift register, as illustrated in Fig. 4.11. The output of the shift register is fed back to its input to create a circular shift register, thus periodically reproducing the stored signal. This periodic signal is converted to the analog domain by a DAC, and used to stimulate an ADC under test. Optionally, an analog filter may follow the DAC. With this approach, it is possible to generate $N_s/2$ single-tone sine waves or combine these single-tones into multi-tone signals. The minimum spacing between adjacent tones is f_s/N_s, where f_s is the sampling clock frequency.

For output response analysis, the output samples of the DUT are sent serially to another shift register. When the register is fully loaded, a N_s-point FFT is performed and the performance parameters of interest are computed and evaluated. Based on the evaluation, the ADC is considered functional or not.

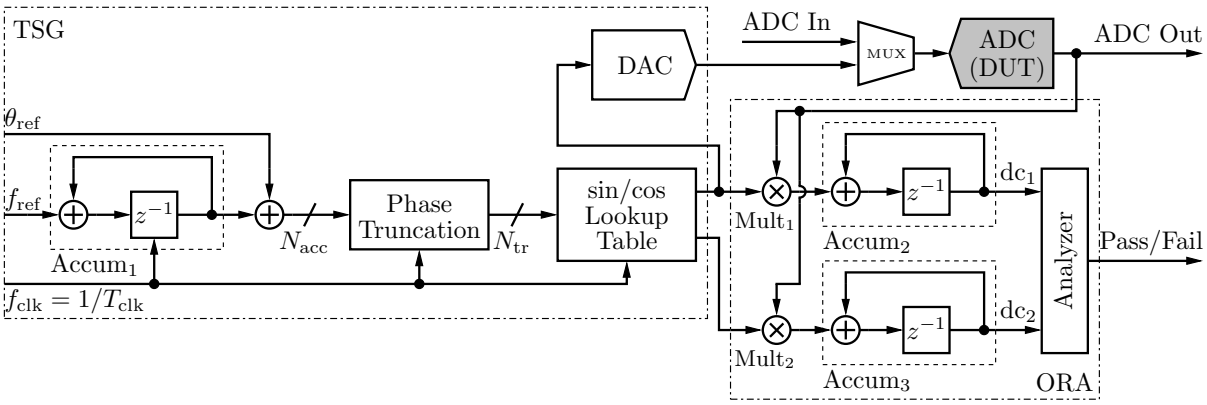


Fig. 4.12: DDS-based built-in self-test architecture.

Besides the need of a multi-bit DAC, which may or may not be available on-chip, the area overhead associated with a dedicated FFT processor is also huge. Hence, the same authors proposed an approximate FFT processor [50]. The basic idea is to approximate the exact kernel function with certain coefficients that allow to reduce multiplications to simple shift and add/subtract operations while computing the FFT. With this technique, the complexity of the arithmetic operators is reduced and the on-chip implementation of a FFT processor exclusively for testing purposes becomes practical. One drawback related to this method is the presence of spurious tones either in the generated signal and in the computed spectrum due to the employed approximations. However, the magnitude of these spurs can be reduced to some extent by increasing the number of approximated kernel coefficients.

Another well-known approach to generate sine waves is employing direct digital synthesis (DDS). In [51], for example, this idea is used as test stimulus generator to self-test several analog blocks in a transceiver, including the data converters. A simplified diagram of the proposed BIST technique is depicted in Fig. 4.12. The key block of a DDS is a lookup table where predefined sine/cosine values are stored. Based on truncated phase words, these stored values are appropriately selected and sent to a DAC to generate sine/cosine analog signals. The truncated phase words are produced by an accumulator, responsible for accumulating the desired frequency word f_{ref} to generate the corresponding phase values, an adder, which allows setting an initial phase θ_{ref}, and a truncate block, which may be straightforwardly implemented by choosing the most significant bits (MSBs) of N_{acc}. The synthesized signal, considering the sine values in a lookup table, is of the form: $\sin(2\pi f_t n T_{\text{clk}} + \theta_{\text{ref}})$, where $f_t = f_{\text{ref}} f_{\text{clk}}/2^{N_{\text{acc}}}$, f_{clk} is the clock frequency (the same as the DAC), and n are integer sample indexes. As a result, the frequency resolution of a DDS is $f_{\text{clk}}/2^{N_{\text{acc}}}$, and finer resolutions can be achieved by increasing the size of accumulator Accum$_1$.

On the ORA side, two multipliers and two accumulators combined with a simple analyzer are used to measure and evaluate the frequency response as well as the linearity of the DUT. A two's complement conversion is performed on the negative values entering the accumulators, Accum$_2$ and Accum$_3$, such that subtraction is accomplished by the adders present in the accumulators. Furthermore, the DDS input of the two multipliers (Mult$_1$ and Mult$_2$) is converted to a signed magnitude value to remove any dc offset that

could affect the accuracy of the test. The multipliers in the ORA serve as mixers to down-convert selected frequency components into dc signals. The dc levels are then compacted by the accumulators and further processed in the analyzer. This multiplier/accumulator output response analysis can be efficiently implemented in hardware, but, since only one frequency component is evaluated at a time, the resulting test time is significant.

Multi-tone test stimuli can be easily and efficiently generated by using multiple truncated phase generators and sharing the lookup table by time-interleaving its input and output. Also, it is proposed in [51] to up-convert the sine/cosine signals generated by the DDS to the radio frequency (RF) range using RF mixers and PLL available in the transceiver. In this case, high frequency analog circuits (e.g. low noise amplifiers) can be properly self-tested.

In contrast to PLLs, the DDS method offers finer frequency resolutions, faster frequency switching times, and wider frequency ranges. The former advantage, as discussed previously, is due to the dependence of the frequency resolution of the DDS on the number of bits of the phase accumulator; hence, increasing the size of the accumulator results in finer resolutions. Frequency switching time refers to the time needed to switch between two frequencies with well-defined (i.e. settled) outputs. Since DDSs do not employ feedback, their responses are much faster than PLLs. The last feature is due to the limited tuning range of the voltage-controlled oscillator (VCO) present in PLLs. On the other hand, the output spectrum of a PLL is usually more clean than that of the DDS. This is due to the finite number of DAC bits, truncated phase bits, and DAC nonlinearity present in the DDS. Furthermore, the DDS output frequency is limited by the maximum operation frequency of the DAC and the digital logic.

As we mentioned above, it is possible to up-convert in frequency a low frequency signal by mixing it with a high frequency one. This principle have been explored by several BIST approaches. In [52], for example, a low frequency generated test stimulus is mixed/multiplexed with a local dc signal to generate a high frequency stimulus (see Fig. 4.13). The low frequency test signal may be generated on-chip, employing one of the techniques discussed previously, or off-chip (although in this case it is not BIST). In the latter case, the external signal can be conveyed up to the multiplexer (close to the ADC under test) using a standardized low frequency analog bus (e.g. the IEEE 1149.4 analog test bus). The analog multiplexer can be implemented with relatively simple low impedance CMOS transmission gates. The multiplexing is performed synchronously to the ADC clock, though at a half rate ($f_s/2$). Consequently, every sample from the output of the ADC corresponding to the low frequency test stimulus will be followed by one dc sample.

In the ORA, a phase selector chooses between the alternating current (ac) (i.e. associated with the test stimulus) or dc samples to be stored into an N-bit register. The ac samples are then processed using a given methodology (e.g. FFT) and a pass or fail indication is generated.

If the local dc signal is chosen equal to the input common mode voltage of the ADC and maintained relatively constant, the test stimulus will change as much as half of the full scale range of the ADC between samples. As a result, the dynamic phenomena related to the ADC will be revealed. Although high accuracy (up to 16-bit) for high speed converters (100 MS/s) is achieved in [52] through simulations, more research is need to support these results.

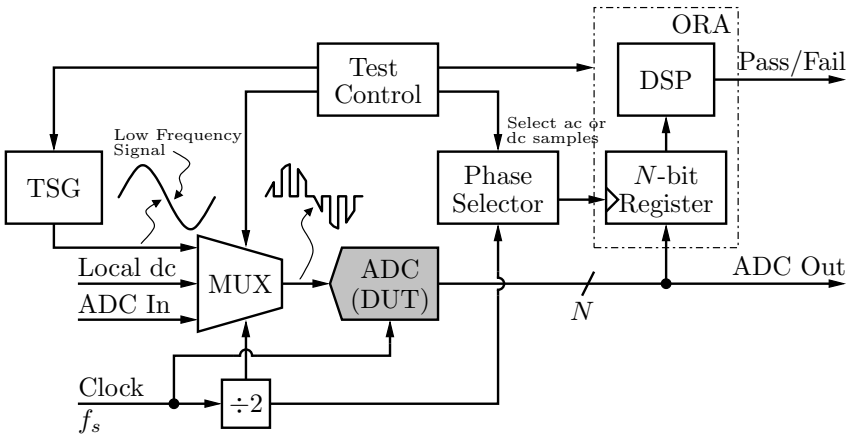


Fig. 4.13: Built-in self-test architecture with high frequency test stimulus generated by mixing.

An extensive research has been done to optimize the performance of on-chip oscillators in order to turn them practical for test stimulus generation. Two recent efforts in this direction are [53, 54]. In [53], a time-mode-based oscillator, employing digital harmonic cancelation circuitry to suppress low frequency harmonics and passive low-pass filter to suppress the high frequency ones, is proposed. The oscillator achieves a SFDR of about 74 dB at 10 MHz with a differential output swing of 228 mV_{pp}. In [54], two oscillators, one continuous-time and other discrete-time, are presented. The fastest, based on a continuous-time operational transconductance amplifier-capacitor (OTA-C) circuitry, achieves a SFDR of 70 dB at 40 MHz with a differential output swing of 175 mV_{pp}, and 56 dB for 590 mV_{pp} at the same frequency.

Although the aforementioned oscillators achieve low distortion, they are able to deliver the rated performance at relatively low frequencies and output swings. Hence, the challenge is to increase either the oscillation frequency and the output swing while keeping the distortion as low as possible. In addition, oscillators are the most versatile building blocks to synthesize high frequency signals. This means that they have an innate potential for stimulus generation, especially for high speed ADC testing. Conversely, free-running oscillators suffer from substantial phase noise. One way to remedy this problem is to insert the oscillator into a PLL with a "clean" external reference clock. Following this method, the close-in phase noise of the oscillator will be significantly attenuated up to the PLL bandwidth. In this work, we will follow this direction to address the built-in TSG problem.

4.3 Discussion

The BIST approaches for mixed-signal circuitries, including ADCs, may be broadly classified into structural (defect-oriented) or functional (specification-oriented). The structural methods have as the main advantage their implementation simplicity, which results in small area overheads and short test application times. Conversely, these techniques rely on fault modeling and simulation for test development and validation, which are extremely challenging (and sometimes even impractical) particularly for analog and mixed-signal

circuits. In addition, with the down-scaling of the CMOS technology, these problems are intensified, since new types of fault become possible. The functional methods, contrary to the structural ones, generally entail more complex BIST circuitry as well as test procedures. Despite of this, they are the most employed at moment, since they overcome the fault modeling issues and provide results that are directly related to the specifications of the device under test, which ensure the device is meeting its intended functions.

Functional BIST approaches may be inclined towards static or dynamic performance parameters of the DUT. In the particular case of ADCs, the difference between the approaches is the rate of change of the input signal with respect to adjacent sampling instants. If the input signal varies slowly, then the static performance is being evaluated. On the other hand, rapidly varying input signals reveal the dynamic imperfections of the ADC, which are crucial for the applications where high speed ADCs are used.

Hence, throughout this section, we discussed functional dynamic BIST approaches with more detail. It is clear that BIST implementations are usually divided into two separated problems: the TSG and ORA implementations. For dynamic BIST methods, a variety of TSGs are available today, such as $\Delta\Sigma$-based oscillators, $\Delta\Sigma$ finite bitstream based generators, ROM/RAM-based generators, FFT-based generators, DDS-based generators as well as many oscillator topologies. In general, although some techniques do exist to up-convert the test stimuli to higher frequency (e.g. by mixing), most available TSGs are not able to generate test stimuli with frequencies greater than about 100 MHz. For the ORA, there are FFT methods, sine wave fitting methods, narrow-band digital filtering, multiplier/accumulator methods, to mention some examples. Despite the available techniques, it is noticeable that the ORA implementation problem is much less investigated than the TSG one, maybe because the ORA is a purely digital implementation issue (i.e. easier to deal with) or because in some cases the digital hardware required for the output response analysis is readily available on-chip as part of the normal (i.e. non-test related) circuitry.

Overall, the available functional dynamic BIST methodologies do not consistently address the high speed ADC testing problem. Hence, in this work, we concentrate our efforts on this topic.

Chapter 5

Proposed Approach

In this chapter, in Sec. 5.1, a generic A/D converter BIST architecture is presented and succinctly discussed. Then, in Sec. 5.2, the ADC BIST architecture proposed in this work is conceptually described.

5.1 Generic ADC BIST Architecture

In the particular case of ADC testing, a generic BIST architecture may be as the one presented in Fig. 5.1. The test stimulus generator (TSG) and the output response analyzer (ORA) are the two very essential blocks of the BIST circuitry. The TSG synthesizes the test stimuli to excite the analog input of the ADC, while the ORA captures the ADC's output, processes it, and signals whether the DUT passed or failed the test. Another important block, which may be optionally integrated on-chip, is the clock generator. This circuit generates the time base for all circuits and has stringent requirements specially for high speed ADCs. The test controller, after initialized by an external signal (e.g. "BIST Start"), provides the controlling signals to all circuits in order to define the testing sequence. In particular, the controller configures the input multiplexer (MUX), which selects the input of the ADC between the test stimulus or its normal input. Besides the "BIST Start" and "Pass/Fail" I/O pins, the BIST may also incorporate a "BIST Done" pin to indicate that the test procedure is complete and that the BIST results are valid and can be read to determine the fault-free/faulty status of the DUT [20, p. 9].

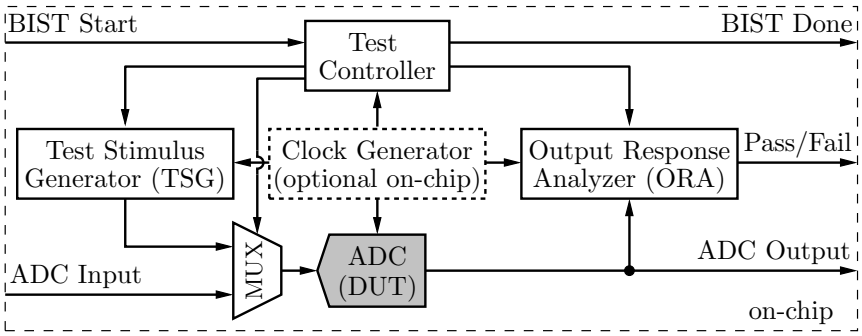


Fig. 5.1: Generic BIST architecture for an ADC.

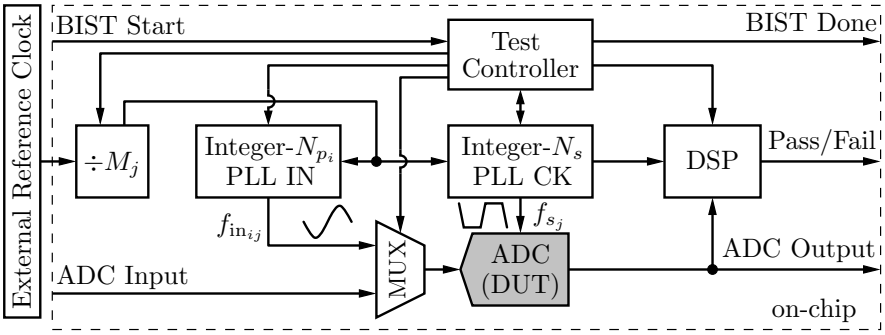


Fig. 5.2: Proposed BIST architecture for coherent testing of high speed ADCs.

5.2 Proposed ADC BIST Architecture

The ADC BIST architecture proposed in this work is conceptually illustrated in Fig. 5.2. It is composed of two integer-N PLLs (PLL IN and PLL CK) that share the same external reference clock to ensure signal synchronization. This synchronization is a prerequisite to achieve coherent sampling. PLL IN generates low distortion, high frequency, and low jitter sine wave signals, while PLL CK generates high frequency and low jitter square wave (nonlinear) clock signals, which are used to drive the ADC during the test procedure. The only off-chip component required is a stable and low frequency reference clock, which may be implemented, for example, by an inexpensive and ubiquitous crystal oscillator.

Under testing, the digitized samples are processed by a DSP (e.g. executing a FFT algorithm), in order to calculate the most important functional dynamic performances of the device under test, which are the most valuable metrics for a high speed ADC. The results may then be compared, for example, with different effective resolution thresholds (e.g. 6, 7, and 8 bits) up to the maximum resolution allowed by the self-testing system and, for each comparison, a pass or fail indication shown. With this, ADCs having different resolutions are sorted and it becomes possible to check the performance degradation during the ADC life time. A test controller takes care of the test application and sequence.

When the two PLLs are locked, the input and sampling frequencies of the ADC become, respectively,

$$f_{\text{in}_{ij}} = N_{p_i} \frac{f_{\text{ref}}}{M_j} \tag{5.1}$$

$$f_{s_j} = N_s \frac{f_{\text{ref}}}{M_j} \tag{5.2}$$

where f_{ref} is a stable external reference frequency and M_j and N_{p_i} $(i, j = 1, 2, \ldots)$ are integer programmable frequency divider values, which enable different frequencies for the input and sampling signals. From Eqs. (5.1) and (5.2) coherent sampling is achieved (cf. Eq. (2.16)).

The architecture parameters N_s, N_{p_i}, and M_j are selected according to the resolution of the ADC under test, the external reference frequency, the desired sampling frequencies $(\hat{f}_{s_j})$, and the desired normalized input frequencies $(\hat{f}_{\text{in}_i}/f_s)$. N_s is a power of two ideally

Table 5.1: Programmable parameters and frequency map for a 6-bit ADC (all frequencies are either in MHz or MS/s).

$f_{\text{ref}} \equiv 4$ MHz		$\hat{f}_{s_1} \equiv 250$	$\hat{f}_{s_2} \equiv 500$	$\hat{f}_{s_3} \equiv 1000$
$N \equiv 6$ bits	$N_s = 256$	$M_1 = 4$	$M_2 = 2$	$M_3 = 1$
		$f_{s_1} = 256$	$f_{s_2} = 512$	$f_{s_3} = 1024$
$\hat{f}_{\text{in}_1}/f_s \equiv 1/2$	$N_{p_1} = 127$	$f_{\text{in}_{11}} = 127$	$f_{\text{in}_{12}} = 254$	$f_{\text{in}_{13}} = 508$
$\hat{f}_{\text{in}_2}/f_s \equiv 1/4$	$N_{p_2} = 63$	$f_{\text{in}_{21}} = 63$	$f_{\text{in}_{22}} = 126$	$f_{\text{in}_{23}} = 252$
$\hat{f}_{\text{in}_3}/f_s \equiv 1/8$	$N_{p_3} = 31$	$f_{\text{in}_{31}} = 31$	$f_{\text{in}_{32}} = 62$	$f_{\text{in}_{33}} = 124$

given by Eq. (2.18). N_{p_i} $(i = 1, 2, \ldots)$ is given by

$$N_{p_i} = \left\{ \left(\frac{\hat{f}_{\text{in}_i}}{f_s} \right) N_s \right\} \tag{5.3}$$

where $\{x\}$ means the nearest odd integer value of x. Note that odd integer values for N_{p_i} ensure irreducibility with respect to N_s, since the latter is a power of two (this irreducible ratio is another requisite of coherent sampling). M_j $(j = 1, 2, \ldots)$ is given by Eq. (5.4), where $\langle x \rangle$ is nearest integer value of x.

$$M_j = \left\langle \frac{f_{\text{ref}} N_s}{\hat{f}_{s_j}} \right\rangle \tag{5.4}$$

As an example, Table 5.1 gives the architecture parameters and the resulting frequency map for a hypothetical 6-bit ADC with $f_{\text{ref}} = 4$ MHz, $\hat{f}_{s_j} = 250$, 500, and 1000 MS/s, and $\hat{f}_{\text{in}_i}/f_s = 1/2$, $1/4$, and $1/8$. We can see that the actual analog input and sampling frequencies are slightly different from the desired ones, but this is indeed required to guarantee coherent sampling (and it is not a limitation in this context).

In the next chapter, we show how the reconfigurable BIST architecture shown in Fig. 5.2, excluding the DSP part, can be efficiently integrated (e.g. with small area overhead) on-chip, thus becoming a very attractive solution for functional dynamic testing of current and future high speed ADCs.

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Chapter 6

Prototype Implementation

In this chapter, the proof-of-concept integrated circuit implementation is discussed. In Sec. 6.1, an overview of the implemented system is given. Then, in Sec. 6.2, emphasis is given to the circuits related to the built-in self-test integration. Finally, in Sec. 6.3, we briefly discuss the implementation of an 8-bit 500 MS/s pipelined ADC, which acts as the device under test in this work.

6.1 Implemented System Overview

Before moving into the description of the individual blocks, it is useful to take a look at the whole block diagram of the implemented system, with particular attention on which signals go in/out of the chip and also how the signals flow from one block to another.

This top view diagram is shown in Fig. 6.1. It is composed of two phase-locked loops (PLLs), one analog-to-digital converter (ADC), and some interfacing circuits like the configurable counters and the reference divider. One PLL generates a differential sinusoidal signal (*vipbist*/*vinbist*) to stimulate the analog input of the ADC, and hence it is denominated PLL IN. Another PLL generates a clock signal (*ckbist*) to clock the ADC, and it is called PLL CK accordingly. Both PLLs have some degree of configuration through the digital control bits that come from the configurable counters. Furthermore, each PLL has a one-pin external reference current that sets internally an independent reference current, which is then mirrored and distributed to the related circuits by means of a global biasing circuit (master current mirror). PLL IN also has an *amplctrl* pin whose purpose is to set the amplitude of the *vipbist*/*vinbist* externally.

The ADC accepts both externally or internally generated analog input and/or clock signals, which are selected according to the state of one of the configurable counters, and it produces an 8-bit digital output which is valid at the falling edges of *ckout* signal. The same external differential clock input that clocks the ADC in normal operation also serves to the reference clock for the PLLs (signal *ckref*). The ADC has an external pin (*vcme*) used to set the internal common-mode voltage (analog ground). Moreover, similarly to the PLLs, it also has a one-pin external reference current (*adciref*) that sets internally an independent reference current, which is then distributed to the related circuits.

The configurable counters let the user set, by means of external push-button switches, specific operation modes for the blocks. This allows, for example, to evaluate the device under test (DUT) under distinct scenarios.

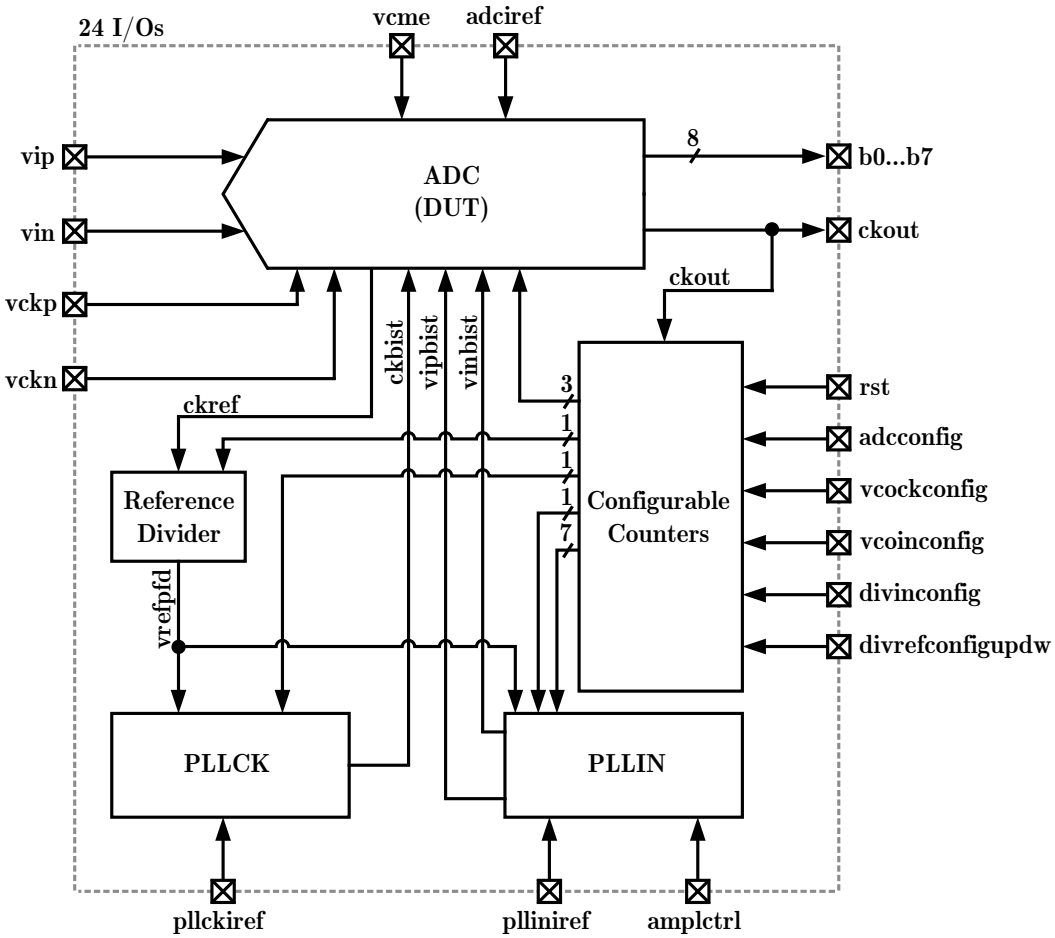

Fig. 6.1: Overview of the implemented system. Power supply and ground pins are omitted for simplicity.

The top layout view of the designed system is shown in Fig. 6.2. Implemented in a 0.13 μm CMOS technology from United Microelectronics Corporation (UMC), the integrated circuit fits on an area of 1525 μm $\times$ 1525 μm including the I/O ring cells.

The chip has a total of 48 pins, but six of them are not connected by default, i.e., they do not need to be wirebonded to the printed circuit board (in case of chip-on-board assembly) or to the selected package fixture. The detailed description of the pins is given in Sec. 7.2.1.

Most of the silicon area not occupied with active circuits is filled with bypass MOS capacitors, which help to stabilize the internal power supply lines. This issue is further discussed later within this chapter.

A Note on the Sizing of Digital Gates

Each digital gate on the logic schematics presented in this chapter carries a single number, below its name, which means the gate strength (the larger the number, the larger the gate drivability is). Otherwise differently stated, the digital gates sizing follows the procedure outlined next, which takes into account the drive strength. The main assumption behind this procedure is to ensure comparable rise (imposed by PMOS transistor branch(es)) and

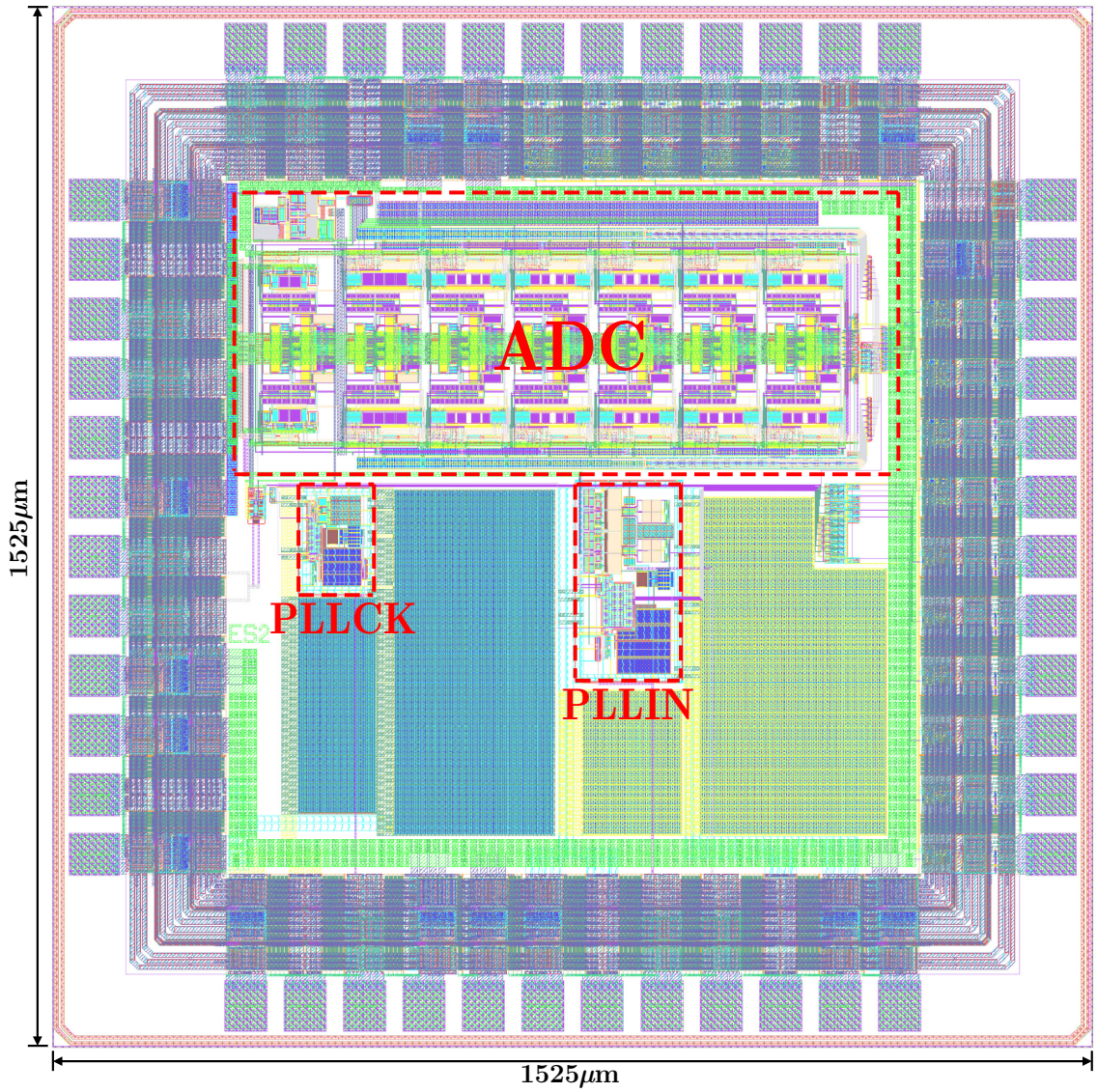

Fig. 6.2: Top layout view of the implemented system, which was implemented in a 0.13 μm CMOS technology and has dimensions, including the I/O ring, of 1525 μm $\times$ 1525 μm.

fall (imposed by NMOS transistor branch(es)) times for the output signal. The length of each transistor is the minimum allowed by the technology used, i.e., $L_{\text{min}} = 0.12$ μm. The width of each NMOS transistor, W_n, is given by $W_n = S \times NS_n \times W_{\text{min}}$, where S is the gate strength, NS_n is the number of NMOS transistors connected in series from the output node to the ground for the respective branch where the transistor being sized is connected, and W_{min} is the minimum transistor width allowed in the technology, i.e., $W_{\text{min}} = 0.16$ μm. The width of each PMOS transistor, W_p, follows the same idea, expect that a factor of three is added to compensate the slower holes mobility, hence, $W_p = 3 \times S \times NS_p \times W_{\text{min}}$. Also, the number of PMOS transistors in series is counted from the output node to V_{DD}. In order to avoid wide transistors, both NMOS and PMOS transistors are fingered. The number of fingers for NMOS transistors, NF_n, is given by

$NF_n = S \times NS_n/2$, and for PMOS ones is given by $NF_p = S \times NS_p/2$. Consequently, the width per finger of NMOS transistors is $2 \times W_{\text{min}} = 0.32$ μm, and of PMOS transistors is $3 \times 2 \times W_{\text{min}} = 0.96$ μm. To show how the above sizing methodology works, consider the following two examples. Firstly, considering a CMOS inverter with strength 4, it is built with a NMOS transistor with width $W_n = 0.64$ μm and number of fingers $NF_n = 2$, and a PMOS transistor with width $W_p = 1.92$ μm and $NF_p = 2$, since $NS_n = NS_p = 1$. As a second example, considerer a two-input NOR gate with strength 2. Since in this case we have two parallel NMOS transistors from the output node to ground, $NS_n = 1$ to both of them (as in the inverter case), and since we have two series PMOS transistors from the output node to V_{DD}, $NS_p = 2$ for both PMOS transistors. Hence, applying the sizing rules presented previously, the two-input NOR gate with strength 2 is built with two NMOS transistors with $W_n = 0.32$ μm and $NF_n = 1$ each, and two PMOS transistors with $W_p = 1.92$ μm and $NF_p = 2$ each.

6.2 BIST Circuitry: PLL IN, PLL CK, and Interfacing Circuits

In this section, we give a detailed description of the building blocks of the proposed built-in self-test architecture. We start with an overview description of the analog input phase-locked loop (PLL IN), since this block, besides of the usual particularities of PLLs, has other specific issues like the generation of low-distortion and amplitude-controlled sinusoidal signals. We then overview the clock phase-locked loop (PLL CK), which resembles a more conventional PLL. Following that, the specific building blocks used to build both PLL IN and PLL CK are addressed. Finally, we give the description of the essential interfacing circuits like the configuration logic block and the linear buffer that buffers the differential sinusoidal signal produced by PLL IN.

6.2.1 Analog Input Phase-Locked Loop (PLL IN) Overview

The block diagram of PLL IN is shown in Fig. 6.3. The topology is based on an integer-N charge pump PLL [55], which is composed of a phase/frequency detector (PFD), a main and an auxiliary charge pump (CP), a loop filter (LF), a two-integrator voltage-controlled oscillator (VCO), a linear buffer, a differential-to-single-ended (DIFF/SE) converter, and a programable frequency divider (FD).

The main function of PLL IN is to generate differential sinusoidal signals (*vipbist* and *vinbist*) based on a relatively low frequency (of few MHz) reference signal (*vrefpfd*). In this work, since the DUT is an 8-bit 500 MS/s ADC, the generated output frequencies are designed to be around approximately 250 and 500 MHz. With these frequencies, it is possible to stimulate the ADC with an analog input frequency close to its Nyquist frequency ($f_s/2$), which is the ultimate frequency to be considered when evaluating a high speed ADC. The frequency range around 500 MHz can be used to evaluate higher conversion rate ADCs, e.g., a 1 GS/s converter, if the DUT is upgraded.

Based on the selection procedure of the architecture parameters discussed in Sec. 5.2, and considering an external reference frequency of about $f_{\text{ref}} = 4$ MHz, we have that frequency divider N_{p_i} must have values of at least $N_{p_{1,2}} = \{63, 127\}$ in order to generate

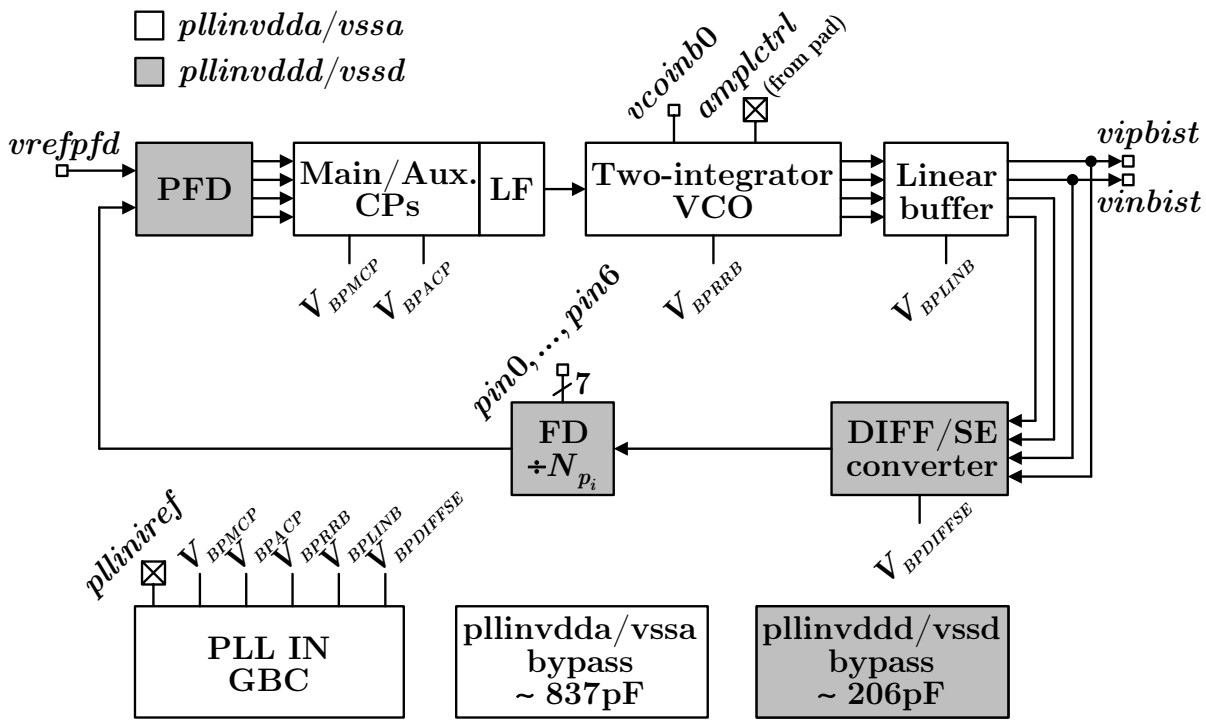

Fig. 6.3: Block diagram of the analog input PLL (PLL IN).

the intended frequency ranges. As a consequence, the frequency divider of PLL IN is programmable by means of the control bits $pin0, pin1, \ldots, pin6$, shown in Fig. 6.3 and addressed later in Sec. 6.2.6, allowing integer frequency division from 32 to 127.

In order to accommodate the two frequency ranges (i.e., around 250 and 500 MHz) without relying on considerable different VCO gains, the two-integrator VCO employs two discrete tuning characteristics, one for each frequency range. The selection between one discrete tuning curve or another is done through *vcoinb*0, which comes from the configuration logic block.

The amplitude of sinusoidal signals generated by the two-integrator VCO can be adjusted by means of the *amplctrl* signal, which is set through an external pin.

Another external pin, *pllinIref*, is used to provide an on-chip independent reference current to PLL IN. This reference current is then mirrored by a global biasing circuit (GBC) and distributed to the circuits of the PLL IN. This approach is important to distribute biasing signals separated by large distances in current domain[1] instead of in the voltage domain (the latter susceptible to IR drops and other sources of error).

Two separated power/ground domains (analog and digital) are used for PLL IN, as shown in Fig. 6.3. The digital domain is more noisy and it powers the DIFF/SE converter and the frequency divider, which operate at the maximum frequency of the PLL and, as a result, produce significant transient current impulses into the respective power/ground lines.

In this work, due to pin number restriction, the analog and digital power/ground

[1]In Fig. 6.3, the biasing signals are represented by voltages, but they are implicitly associated with the respective mirrored currents. Although this convention may lead to confusion, it simplifies the schematic net labeling by avoiding duplicate names on the same net.

domains are not completely isolated; they are connected together in the I/O pad ring. Consequently, some noise propagates from the digital domain to the analog one. In order to avoid strong current impulses propagation between power/ground domains, and to help stabilize the internal supply voltages, all "free" silicon area is filled with bypass capacitors. These capacitors are implemented with arrays of MOS transistors operating in strong inversion, which maximize the attainable capacitance density (about 12 fF/μm^2 in the technology used).

The top layout view of PLL IN and its associated floorplan is shown in Fig. 6.4. The PLL IN core occupies an area of 138 μm $\times$ 282 μm, which represents only a fraction of the whole layout, since most the area is filled with bypass capacitors.

In the layout, as it is clear analyzing its flooplan, the main PLL signals make a circular path, shortening the distance between adjacent blocks. Also, all blocks have some degree of substrate isolation through specifically laid out guard rings, specially the differential-to-single-ended converter and the frequency divider (the ones that are likely to inject more noise into the substrate). This substrate isolation is important because the technology used has a low resistivity substrate to efficiently cope with latch-up issues; hence, it is easy to happen noise propagation through the substrate, if preventive measures are ignored.

The power/ground lines are routed with wide (sometimes in parallel) metal traces, and to ease the distribution of these signals to the circuits, a power/ground ring is laid out around the PLL IN core.

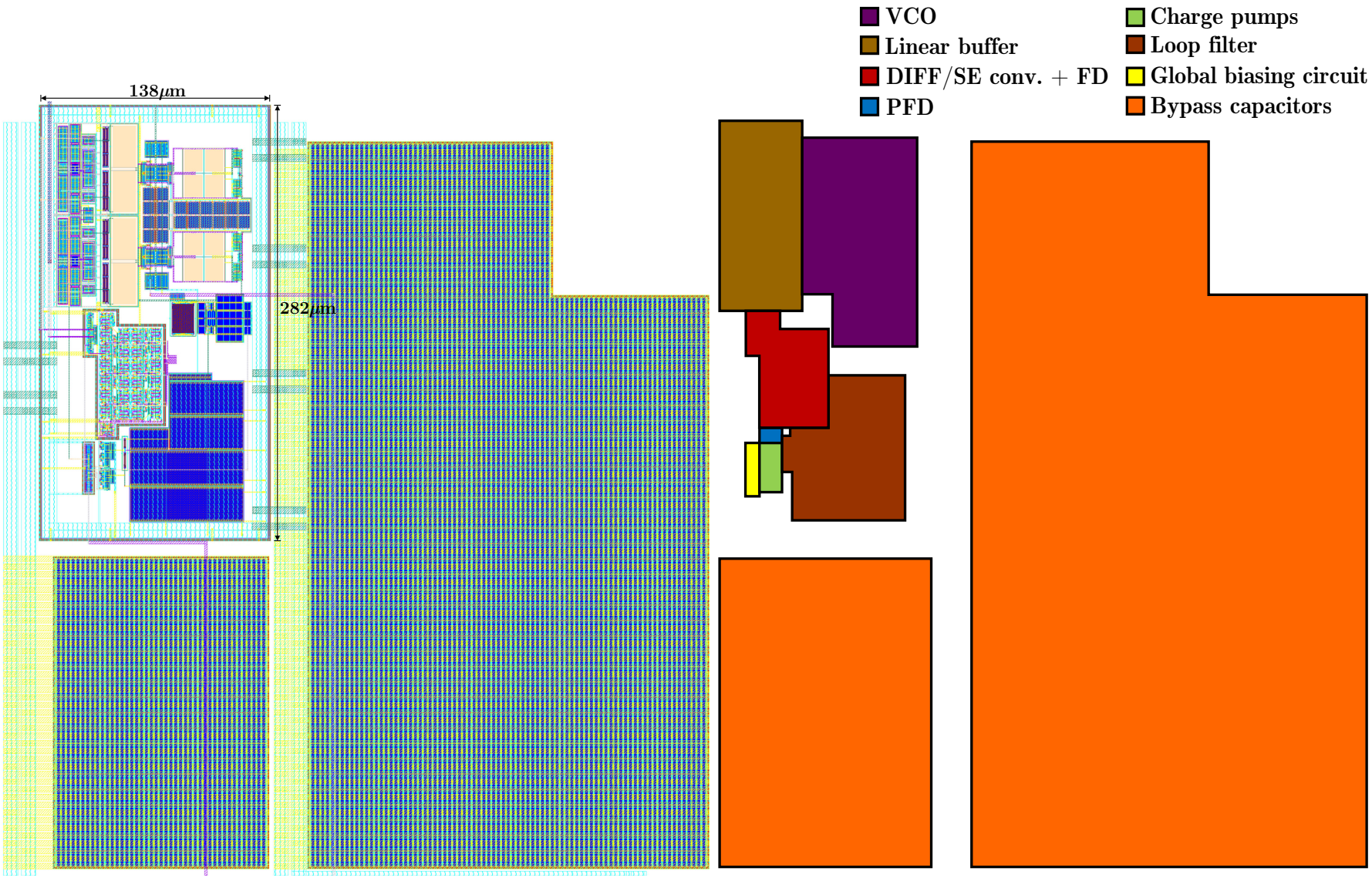

Fig. 6.4: Layout of the analog input PLL (left) and its floorplan (right). The PLL IN core occupies an area of 138 μm $\times$ 282 μm.

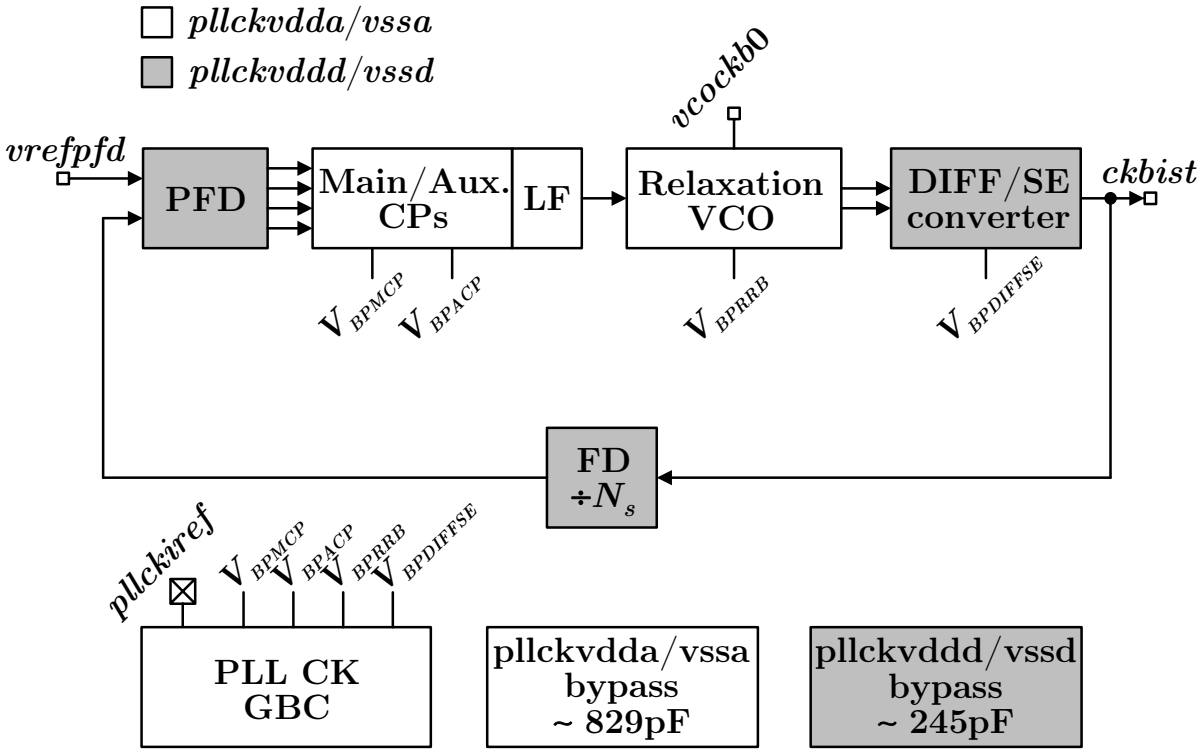

Fig. 6.5: Block diagram of the clock PLL (PLL CK).

6.2.2 Clock Phase-Locked Loop (PLL CK) Overview

The clock PLL is also based on an integer-N charge pump topology, as shown in Fig. 6.5. However, differently from the analog input PLL, it resembles a more conventional PLL used for ubiquitous clock generation.

The main function of PLL CK is to generate a low jitter and high frequency clock signal (*ckbist*) based on a relatively low frequency signal (*vrefpfd*), which is also shared with PLL IN. The sharing of *vrefpfd* allows both PLLs to operate in the same time base (i.e., synchronized) when they acquire lock state (i.e., enter steady state regime). This in turn enables the DUT to sample the analog input signal in a coherent fashion. Moreover, it is interesting to note that any phase noise on *vrefpfd* within the loop bandwidth of the PLLs appears correlated in the PLLs outputs; hence, this noise affects the system noise performance almost negligibly.

The clock frequencies generated by PLL CK should be as close as possible to the target sampling frequency of the ADC. In this work, since we are evaluating an ADC with a conversion rate of about 500 MS/s, we design one frequency range around 500 MHz and another around 1 GHz. The latter may be used to assess higher speed A/D converters, if the DUT is upgraded.

According to the procedure discussed in Sec. 5.2, the divider value of the frequency divider of PLL CK, N_s, should ideally be $N_s = 2^{8+2} = 1,024$ for an 8-bit ADC. To be able to generate the slowest frequency range around 500 MHz, this N_s value would require a reference frequency at the input of the PFD of about 500 kHz (≈ 500 MHz$/1,024$). This

would require a loop bandwidth for both PLLs of approximately 50 kHz[2], which is not desirable in this work because we are using relatively noisy (but extremely compact) RC oscillators to generated the intended signals.

As a result of the above limitation, in this work we use $N_s = 256$ to allow the loop bandwidth of the PLLs to be four times wider (i.e., approximately 200 kHz) than it would be possible with $N_s = 1,024$. Doing this way, we reduce the likelihood of collecting at least one sample from every ADC code, since the number of distinct discrete phase samples diminishes (refer to Sec. 2.3.1), but we allow the PLLs to suppress the close-in phase noise of the RC oscillators more effectively up to 200 kHz.

Since the frequency divider value of PLL CK is fixed ($N_s = 256$), and assuming the external reference of $f_{\text{ref}} = 4$ MHz is unchanged (as it would be in the case of a mounted-on-the-PCB crystal oscillator), we need an additional degree of freedom to generate frequencies either at 500 MHz and 1 GHz. This degree of freedom is achieved with the reference frequency divider (see Fig. 6.1), which allows the external reference frequency to be divided by $M_{1,2} = \{1, 2\}$.

Similarly to the two-integrator VCO of PLL IN, the relaxation VCO of PLL CK also embodies two discrete tuning curves for the same reasons discussed previously. The selection between these discrete tuning curves is achieved with the *vcockb*0 signal, which comes from a configurable counter (and it is configured externally by the user).

The PLL CK also has a dedicated external pin, *pllckiref*, that sets an independent reference current on-chip. This reference current is then mirrored with a global biasing circuit, shown in Fig. 6.5, and distributed to the needed circuits.

Furthermore, for the same reasons pointed out earlier in Sec. 6.2.1, the PLL CK also has two separated power/ground domains: one analog (more quiet) and one digital (more noisy). Again due to pins limitation, the analog and digital power/ground domains are isolated up to the I/O pad ring, where they are connected together through the specific I/O power/ground rings. To help improve the quality of the power/ground supply lines, many bypass capacitors are used. These capacitors, similarly to the ones employed in PLL IN, are implemented with MOS capacitors in order to integrate on-chip the maximum amount of bypassing capacitance.

The top layout view of PLL CK is shown in Fig. 6.6 alongside its floorplan. The PLL CK core occupies an area of merely 92 μm $\times$ 138 μm, which represents a tiny fraction of the whole layout area including the bypass capacitors.

As it may be seen from the floorplan of Fig. 6.6, the building blocks of PLL CK are arranged in a circular fashion that keeps the distance between adjacent blocks as short as possible. Also, some preventive measures like guard rings for substrate noise isolation, mainly for the differential-to-single-ended converter and the frequency divider, are employed. To ease the power/ground signals distribution, a low resistance power/ground ring is laid out around the PLL CK core.

[2]The loop bandwidth of a charge pump PLL is usually designed to be 1/10th (or even smaller) of the reference frequency at the PFD to ensure stability [56, p. 24].

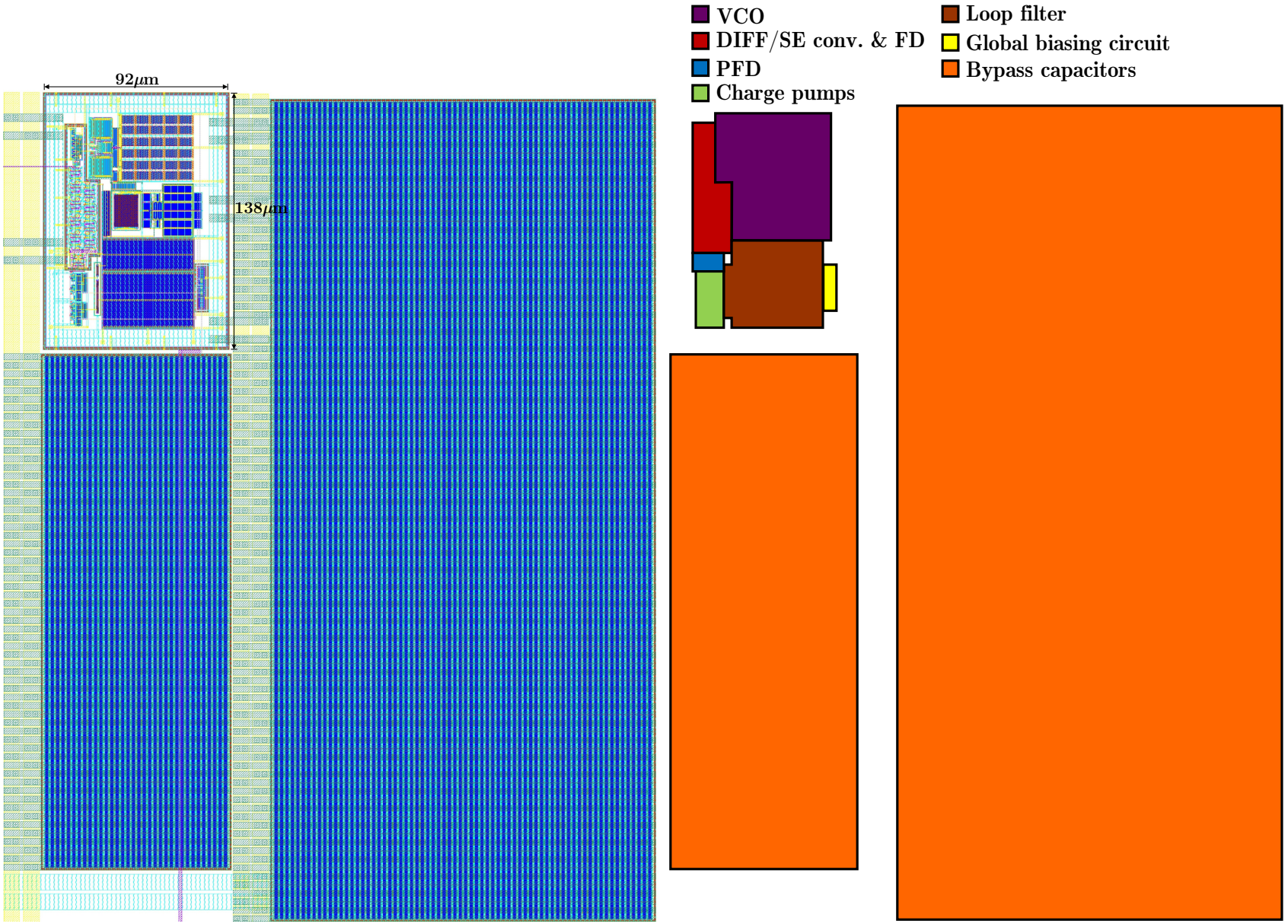

Fig. 6.6: Layout of the clock PLL (left) and its floorplan (right). The PLL CK core occupies an area of 92 μm $\times$ 138 μm.

Table 6.1: Comparison of fully integrated CMOS oscillators.

Oscillator Topology	Phase Noise	Output Distortion	Tuning Range/Linearity	Area
LC tank	Lowest	Low	Smallest/Low	Largest
Ring	Medium	High	Large/Medium	Small
Relaxation	Medium	High	Large/Medium	Small
Two-integrator	Medium	Low*	Large/Medium	Small

* When operated in the linear regime.

6.2.3 Voltage-Controlled Oscillators

As briefly mentioned in Secs. 6.2.1 and 6.2.2, the proposed BIST scheme requires an oscillator to generate low distortion sinusoidal signals at PLL IN and another to generate low jitter clock signals at PLL CK. In this section, we present the topologies chosen for these oscillators. Since these blocks are the most critical in the proposed self-testing scheme, we start with a brief comparison of oscillator topologies that are suitable to be fully integrated in CMOS technology.

Oscillators Comparison

There are a variety of oscillators topologies in the current literature and, probably, the most used in CMOS technology are listed in Table 6.1. The LC oscillator is widely used mainly because of its superior phase noise performance, the best among the topologies listed. However, for a practical BIST scheme, which must be as compact as possible, this oscillator has a remarkable drawback: the large area occupied by the integrated inductors. This single reason is sufficient to discard the use of this topology. Furthermore, if special RF options are not available (e.g., several metal layers with a thick top metal), the quality factor of the inductors are reduced and the phase noise performance is somewhat worsened. Another shortcoming of LC oscillators is the narrow tuning range, which would pose some restrictions when generating a variety of frequencies, as it is required by the proposed architecture.

The remaining three topologies shown in Table 6.1 may be classified as RC-type oscillators and, therefore, have relatively poor phase noise performance. However, if this phase noise is still adequate for the application, this class of oscillators offers a unique feature: they are extremely compact (occupy small silicon area) and are easily integrated in standard CMOS technologies.

It is well-know that the phase noise of an oscillator trades off with the power dissipation. In a BIST scheme, the power dissipation is not the main concern, since all the testing circuitry can be powered-down after the test procedure. Hence, it is possible to reduce the phase noise at the expense of higher power dissipation. Other useful properties of RC oscillators are wide tuning range and improved tuning linearity.

Among the RC oscillators presented, only the two-integrator oscillator can generate low distortion sinusoidal signals, since this topology can operate in linear regime [57, pp. 102-104]. Additionally, the two-integrator oscillator can be used in an efficient automatic amplitude control (AAC) loop that stabilizes the oscillator amplitude to a reference

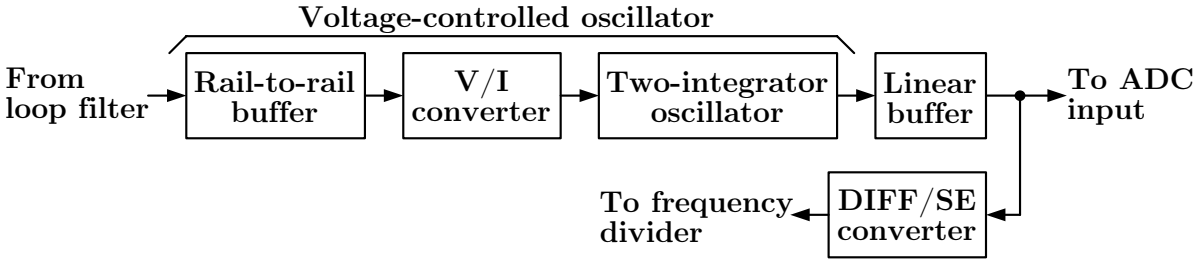

Fig. 6.7: Block diagram of the two-integrator VCO and related circuits.

(well-known) value after start-up [58] [59, pp. 34-36]. For these reasons, we have chosen the two-integrator oscillator topology to generate spectral purity sine waves at PLL IN. A more detailed discussion regarding this oscillator will be given below.

The implementation simplicity of ring and relaxation oscillators makes them the preferred choice to generate the clock signal. In [60], it is shown that practical ring oscillators have a slightly better phase noise performance than practical relaxation oscillators for a given power dissipation. Despite this known advantage, the relaxation oscillator is adopted here because, in addition to a "square" wave, this oscillator produces a "triangular" waveform which can be used for other applications (e.g., calibration of time-interleaved ADCs; but this is outside the scope of this work). Moreover, as previously mentioned, the phase noise can be improved by increasing the dissipated power in the oscillator. A more in-depth discussion regarding the relaxation oscillator is given later within this section.

Two-Integrator Voltage-Controlled Oscillator

The block diagram of the two-integrator voltage-controlled oscillator (VCO) and associated circuits is shown in Fig. 6.7. The two-integrator VCO is composed of three building blocks: an input rail-to-rail buffer, a voltage-to-current (V/I) converter, and a two-integrator oscillator core. A linear buffer follows the VCO and its purpose is to buffer the low distortion sinusoidal signals generated by the latter. This buffer is discussed in detail in Sec. 6.2.7, and it plays a crucial role in the interface between PLL IN and the ADC, since it drives the front-end track-and-hold amplifier (THA) of the ADC (which is a heavily nonlinear load). A differential-to-single-ended (DIFF/SE) converter translates the differential sinusoidal signal into a full-swing CMOS signal, which can then be used by the digital frequency divider. This DIFF/SE converter is intentionally placed after the linear buffer to avoid possible deleterious interferences (e.g., kick-back noise) into the two-integrator oscillator core.

The schematic of the two-integrator oscillator core, including the sizing of all devices, is shown in Fig. 6.8. The two integrators are realized by two differential pairs, transistors M_{3a-d}, and two switched-capacitor banks, $C_{1a,b}$. Two additional differential pairs, comprising transistors M_{4a-d}, with the outputs cross-coupled to the inputs, implement negative transconductance ($-G_m$) to compensate the losses due to resistors R_{1a-d}, and make sustainable oscillation possible. These additional pairs may also be used for amplitude control of the output signals, as it will be further discussed later. The schematic is completed with a filtering capacitor C_f, which reduces the distortion of the generated

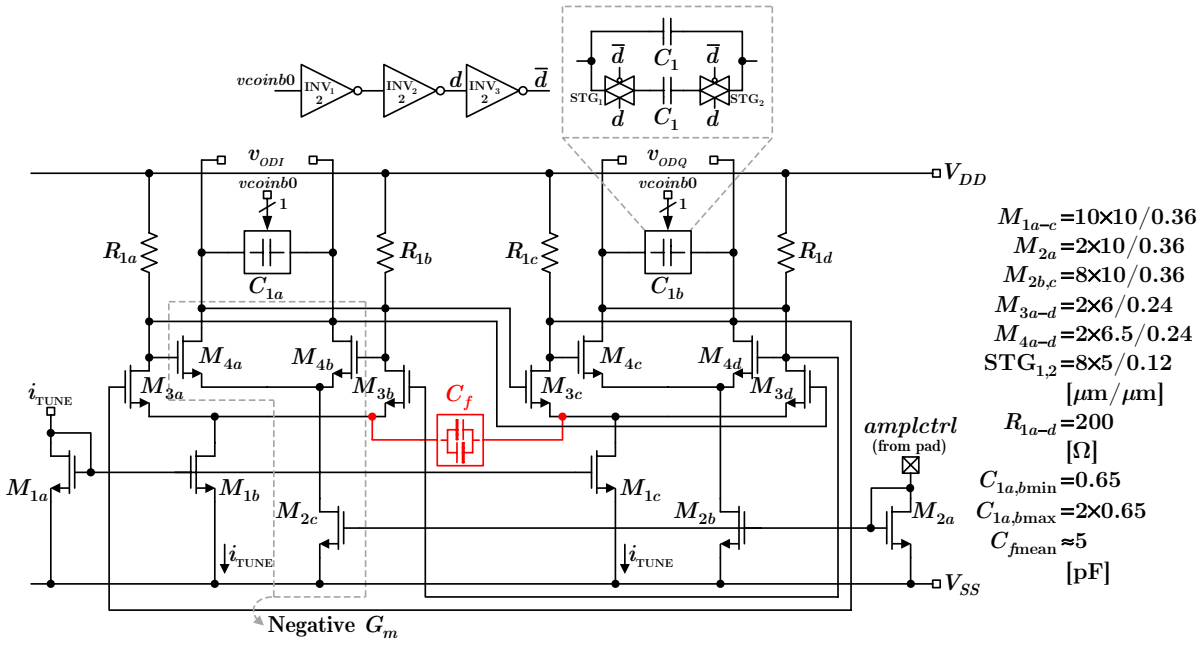

Fig. 6.8: Schematic of the two-integrator oscillator.

sinusoidal signals.

The two-integrator oscillator topology generates in-phase and quadrature-phase (IQ) signals, v_{ODI} and v_{ODQ}, respectively. In linear operation, the oscillation frequency is approximately given by [57, p. 106]

$$f_{\text{osc}} = \frac{g_{m3}}{2\pi C_1} \tag{6.1}$$

where g_{m3} is the transconductance of each integrator's differential pair and $C_1 = C_{1a,b}$ is the equivalent capacitance of each switched-capacitor bank. The transconductance g_{m3} can be varied by means of the currents i_{TUNE}. Hence, the two-integrator oscillator can be tuned by changing C_1 and/or i_{TUNE}.

In this work, in order to widen the tuning range without excessively increasing the VCO gain, K_{VCO}, we use a combination of discrete and continuous tuning modes [61]. A switched-capacitor bank controlled by *vcoinb*0 selects a given tuning characteristic (two discrete tuning curves available), and continuous variations within the selected characteristic are obtained by changing the magnitude of the current sources i_{TUNE}. The continuous tuning is performed in the current domain because in this way it is possible to achieve wider tuning range and better tuning linearity. In fact, high quality varactors are not offered in modern CMOS technologies [61].

The switched-capacitor banks are implemented with symmetrical metal-oxide-metal (MOM) capacitors and two symmetrical transmission gates (STGs)[3]. A simple CMOS inverter logic is used to control these STGs, which switch on or off one of the bank capacitors according to the state of *vcoinb*0 signal. When the capacitor is switched on, the slowest discrete tuning curve is selected; otherwise, the fastest discrete tuning curve is used by the VCO.

[3]A STG is composed of an NMOS and a PMOS transistor with the same aspect ratio W/L.

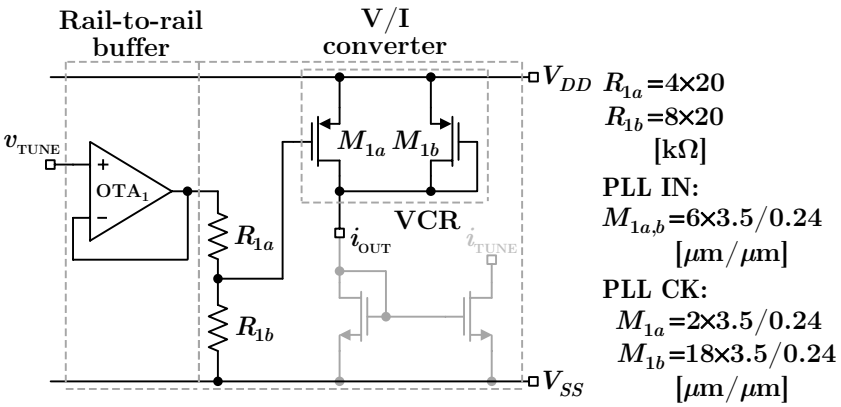

Fig. 6.9: Schematic of the V/I converter and rail-to-rail buffer. The schematic of OTA$_1$ is shown in Fig. 6.10. The voltage-controlled resistor has different sizing depending whether it is related to the two-integrator oscillator (PLL IN) or to the relaxation oscillator (PLL CK).

The output of the loop filter is a voltage, hence a V/I converter is needed to convert this voltage into the tuning current i_{TUNE}. The V/I converter used in this work is shown in Fig. 6.9. It is built around a PMOS voltage-controlled resistor (VCR) composed of transistors $M_{1a,b}$. The main function of the diode-connected transistor, M_{1b}, is to help linearize the V/I transfer characteristic.

Additionally, in a low voltage environment, it is important to use the entire voltage swing available by the charge pumps[4] to further minimize the K_{VCO}. Thus, an input rail-to-rail buffer as indicated in Fig. 6.9 is used. This buffer in conjunction with resistors $R_{1a,b}$[5] adjust the controlling voltage range for the VCR.

The detailed schematic of the rail-to-rail buffer is shown in Fig. 6.10. It is based on a simple operational transconductance amplifier (OTA) topology with complementary input differential pairs, transistors M_{1a-2b}, which allow input rail-to-rail swing. The output branch employs two common-source transistors, $M_{4b,5b}$, and consequently its maximum voltage swing is comparable to that of the charge pumps (hence the entire voltage swing can be used). With a load of 240 kΩ, the buffer has an open loop dc gain of about 40 dB and a dominant pole frequency around 100 kHz. Moreover, it is important to highlight that this buffer and the V/I converter (the latter with a slightly different sizing) are used as building blocks of PLL CK as well. With this building blocks reuse, which is a philosophy used throughout this work, we minimize the design effort needed to implement the proposed BIST scheme.

The simulated discrete tuning characteristics of the two-integrator VCO, according to the state of signal *vcoinb*0, are shown in Fig. 6.11. As discussed in Sec. 6.2.1, these two characteristics are centered around 250 and 500 MHz respectively. The slowest tuning curve has a K_{VCO} gain of about 125 MHz/V in its more linear region, while the fastest

[4]According to Fig. 6.24, the voltage swing available by the charge pumps is: $V_{DD} - V_{SS} - 2|V_{DS\mathrm{sat}}|$, where $V_{DS\mathrm{sat}}$ is the drain-to-source saturation voltage.

[5]Resistors $R_{1a,b}$ act as a 2/3 voltage divider, which maps a voltage range of [0 V, 1.2 V] at the output of the buffer into a maximum voltage range of [0 V, 0.8 V] at the output of the divider. This voltage mapping gives margin for the PMOS VCR to operate in strong inversion.

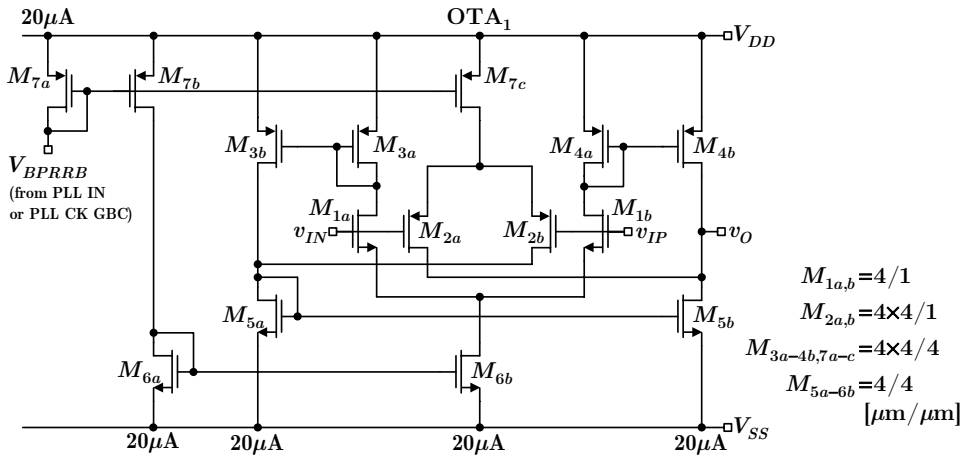

Fig. 6.10: Detailed schematic of the rail-to-rail buffer. The biasing voltage V_{BPRRB} (or more appropriately the mirror reference current) comes from the global biasing circuit (GBC) of PLL IN or PLL CK, depending each one is being considered.

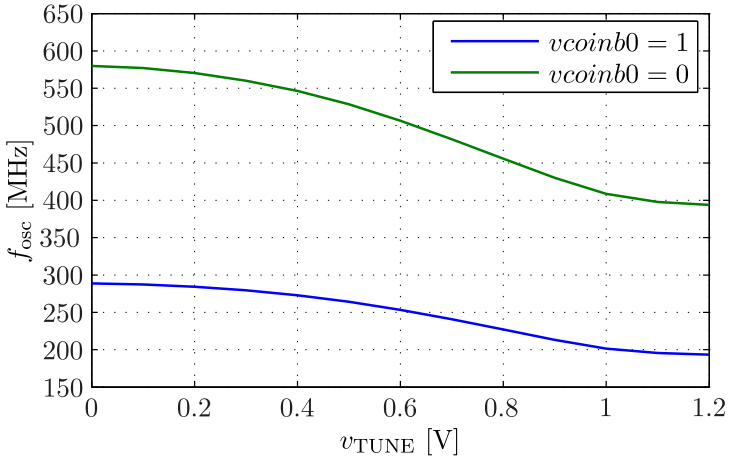

Fig. 6.11: Simulated discrete tuning characteristics of the two-integrator VCO.

curve has a VCO gain twice as high, i.e., about 250 MHz/V. This K_{VCO} difference follows direct from Eq. (6.1), since to implement the fastest discrete curve we halve the bank capacitances ($C_{1a,b}$) with respect to the slowest curve and, consequently, a factor of 2 appears in front of the referred equation.

To reduce the output distortion of the two-integrator oscillator, an extra capacitor C_f is placed between the drains of transistors $M_{1b,c}$, as shown in Fig. 6.8. According to simulations, this capacitor attenuates the amplitude of the dominant second harmonic present on these nodes by a low-pass filtering action. This causes the oscillator operation to be more linear and, consequently, the output distortion is improved. A somewhat related technique intended for phase noise reduction rather than for output distortion improvement is proposed in [62].

The filtering capacitor C_f is implemented with an array of N+/Nwell MOS varactors (i.e., a NMOS transistor inside an Nwell) that exhibit a smoother capacitance-voltage characteristic and lower channel resistance than a conventional NMOS transistor con-

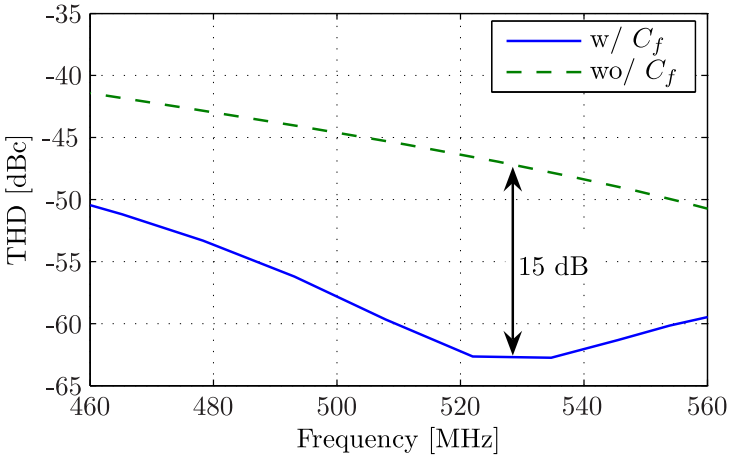

Fig. 6.12: Simulated output THD of the two-integrator oscillator with and without the filtering capacitor C_f versus frequencies of the fastest discrete tuning characteristic.

figured as a capacitor. This lower distributed channel resistance in turn improves the capacitor quality factor and enhances the filtering action in this particular application. Since a N+/Nwell MOS varactor is naturally asymmetrical, the whole array is divided by half and each of these half arrays are connected in opposite direction. This ensures a good layout symmetry, which is also observed in the whole VCO layout (including its loads).

The simulated THD of the two-integrator oscillator with and without the proposed filtering scheme is shown in Fig. 6.12. The total distortion is mainly caused by third and fifth harmonics, since the oscillator has differential outputs and its layout is carefully made symmetrical. Considering an output voltage swing of 500 $\mathrm{mV_{pp,diff}}$ and no filtering, the THD hardly exceeds -50 dB. Employing the proposed filtering scheme, with $C_f \approx 5$ pF, the THD improves substantially in all frequencies and reaches a maximum enhancement of 15 dB. These results are for the frequencies of the fastest discrete tuning curve, but similar conclusions apply to the slowest discrete tuning characteristic as well.

As mentioned previously, the cross-coupled differential pairs (transistors M_{4a-d}) may be used for amplitude control of the output signals of the two-integrator oscillator. When these pairs are incorporated into an automatic amplitude control (AAC) loop, the following benefits are derived: *i*) it may force the oscillator to operate in the linear regime resulting in less distorted output signals, and *ii*) it stabilizes the output amplitude to a known predefined value, which may be matched to the full-scale range of the ADC under test (assuming this range is small enough to ensure the two-integrator oscillator can still operate in linear regime).

There are several approaches to implement the AAC loop, but the essential functions are *a*) sensing and estimation of the output oscillation amplitude, *b*) comparison of this estimation with a predefined reference value (which produces an error), and *c*) injection of this error (usually amplified) into the gates of $M_{2b,c}$, which closes the negative feedback loop. In the same way that the AAC loop brings some interesting advantages, it can potentially "kill" the oscillation if the loop becomes unstable due to a bad design or due to an unpredicted manufacturing process shift. With these considerations in mind, in this work we chose a more conservative approach in order to avoid excessive risks, that is, we

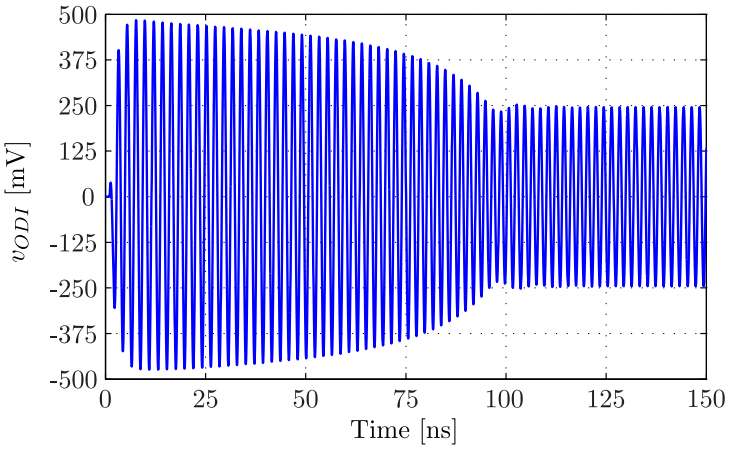

Fig. 6.13: Simulated start-up of the two-integrator oscillator showing the AAC response.

control the biasing of the cross-coupled differential pairs in open loop through an external signal *amplctrl*. Following this open loop approach, we can still force the oscillator to operate in linear regime and roughly set the oscillation amplitude to a given value, but this procedure is done interactively adjusting *amplctrl* and observing the resulting measured signals.

Even though the AAC loop is not integrated on-chip in this work, it is still useful to consider one implementation approach to see how it really behaves. One such elegant implementation method is proposed in [58] (one of the former for this particular oscillator topology). According to [58], the IQ output signals of the two-integrator oscillator may be expressed as

$$v_{ODI} = V_{od} \sin(\omega_{\text{osc}} t) \tag{6.2}$$

and

$$v_{ODQ} = V_{od} \cos(\omega_{\text{osc}} t) \tag{6.3}$$

where it is assumed, for simplicity, that the output signals have the same amplitude V_{od}. If these signals go through squarer circuits and are summed up, from Pythagoras' law follows that

$$V_{od}^2 \sin^2(\omega_{\text{osc}} t) + V_{od}^2 \cos^2(\omega_{\text{osc}} t) = V_{od}^2 \tag{6.4}$$

With the above procedure we have an estimation of the squared output amplitude. This value can then be compared with a reference voltage V_{ref}, also squared, and the result applied to the gates of transistors $M_{2b,c}$. If the negative feedback loop is stable, these transistors will force the output amplitude to approach V_{ref} after reaching the steady state regime.

The simulated start-up of the two-integrator oscillator with such an AAC loop is shown in Fig. 6.13, where it is possible to observe the AAC transient response. With V_{ref}^2 set to $(250\ \text{mV})^2$, the AAC loop stabilizes the differential output amplitudes, v_{ODI} and v_{ODQ}, to approximately 250 mV with less than 120 ns.

The output amplitudes of the two-integrator oscillator with an AAC loop versus the oscillation frequencies of the fastest discrete tuning curve are shown in Fig. 6.14. It is interesting to note that, due to the AAC loop, the amplitude varies less than approximately 1 mV within the entire frequency range.

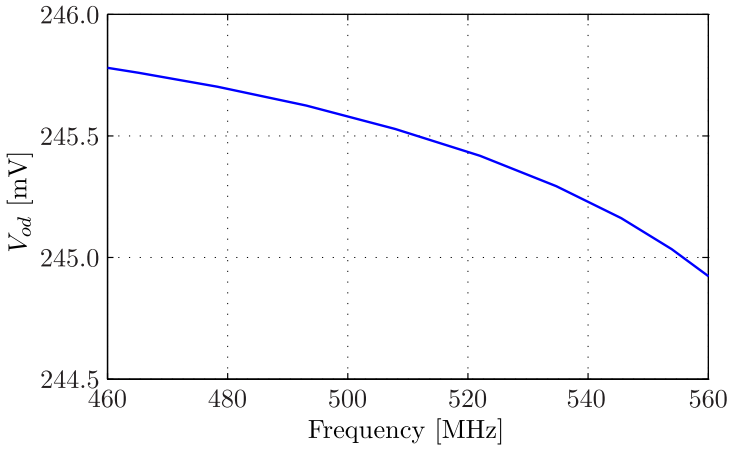

Fig. 6.14: Simulated output amplitude of the two-integrator oscillator versus frequencies of the fastest discrete tuning characteristic.

Before being applied to the digital frequency divider, the differential sinusoidal signals generated by the two-integrator VCO must be converter to a full-swing CMOS signal. This conversion is done with the DIFF/SE converter shown in Fig. 6.15, which is composed of a simple front-end amplifier followed by a CMOS inverter buffer. The amplifier ensures single-ended termination and some amount of pre-amplification, and the inverters buffer converters the resulting signal into a full-swing CMOS one (with fast rising/falling times).

As mentioned earlier, the DIFF/SE converter is connected after the linear buffer (cf. Fig. 6.7) to avoid injection of digital noise into the VCO outputs, which would be detrimental to the VCO operation. Furthermore, in order to equalize the loading of the preceding linear buffer (which has IQ outputs), the DIFF/SE converter uses a main structure for the in-phase output and a dummy structure for the quadrature-phase output. With this approach and careful layout, the loading of the linear buffer is made as symmetrical as possible.

Relaxation Voltage-Controlled Oscillator

The block diagram of the relaxation VCO is shown in Fig. 6.16, and overall it is considerably simpler than that of the two-integrator VCO. The relaxation VCO is also composed of three building blocks, i.e., a rail-to-rail buffer, a V/I converter, and a relaxation oscillator core. The former two blocks are topologically identical to the ones employed in the two-integrator design (i.e., Figs. 6.9 and 6.10), except that the V/I converter has a slightly different sizing to optimize the tunability of the relaxation oscillator. Since the generated output signal drives only a few standard digital gates, we do not need to worry about specific buffering issues. Consequently, a differential-to-single-ended converter immediately follows the relaxation oscillator core. This DIFF/SE converter, however, is different from the one used for PLL IN, as it will be explained later.

The schematic of the relaxation oscillator core is shown in Fig. 6.17. The oscillator is composed of a floating timing switched-capacitor bank, C_1, connected to a nonlinear structure that behaves like a Schmitt trigger. This nonlinear structure is formed by two current sources i_{TUNE}, obtained through $M_{1b,c}$, a cross-coupled pair of transistors, $M_{2a,b}$,

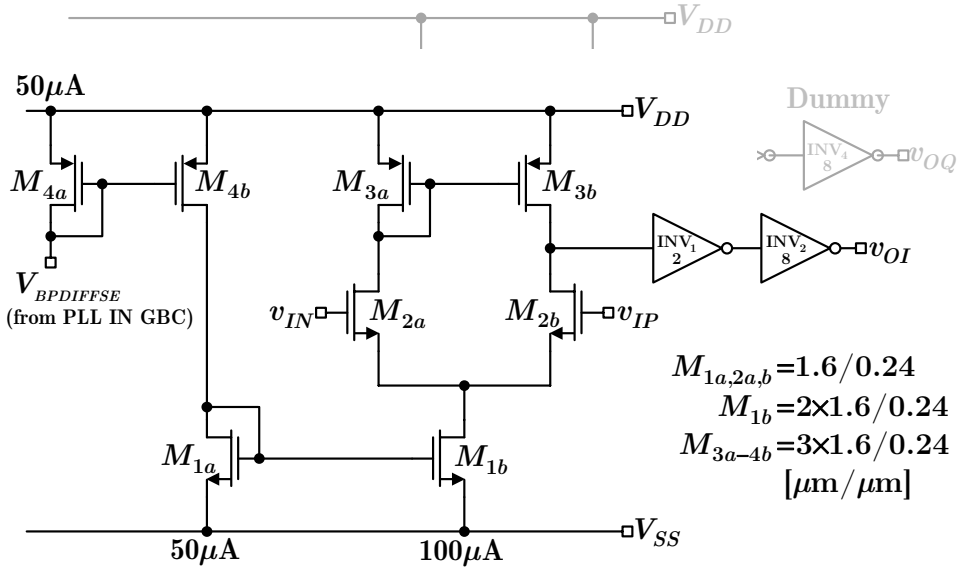

Fig. 6.15: Schematic of the differential-to-single-ended (DIFF/SE) converter employed in PLL IN. The biasing voltage $V_{BPDIFFSE}$ (or more appropriately the mirror reference current) comes from the global biasing circuit of PLL IN. A dummy structure is used to avoid asymmetrical loading of the linear buffer.

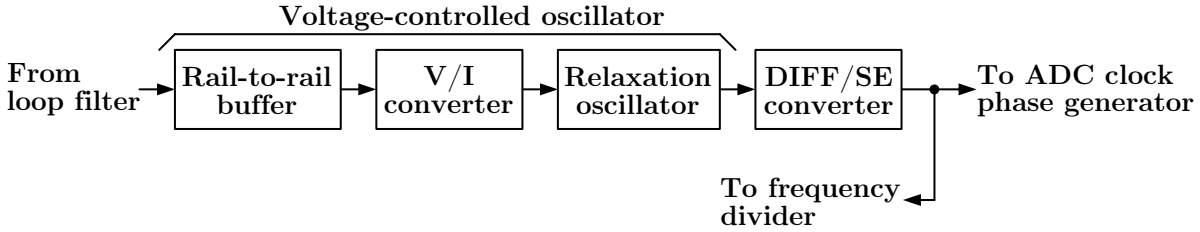

Fig. 6.16: Block diagram of the relaxation VCO and related circuits.

which steers the currents i_{TUNE} between the two branches, two load resistors, $R_{1a,b}$, and two diode-connected devices, $M_{3a,b}$, which clamp the output nodes and create a strong i_{TUNE} versus oscillation frequency dependence.

In oscillatory regime, the oscillation frequency is approximately given by [63]

$$f_{\mathrm{osc}} = \frac{i_{\mathrm{TUNE}}}{4C_1 V_{c1}} \tag{6.5}$$

where V_{c1} is the amplitude of the voltage swing across the floating timing capacitor. As a result, this oscillator can be practically tuned by changing C_1 and/or i_{TUNE}, since V_{c1} is usually not under direct control.

For the same reasons discussed for the two-integrator oscillator, we combine both discrete and continuous tuning for the relaxation oscillator tunability. The discrete tuning is performed by a switched-capacitor bank, C_1, controlled by *vcockb*0 signal (two discrete tuning curves are available, similarly to the two-integrator VCO). On the other hand, the continuous tuning is realized by the currents i_{TUNE}, which are generated by the V/I converter shown in Fig. 6.9.

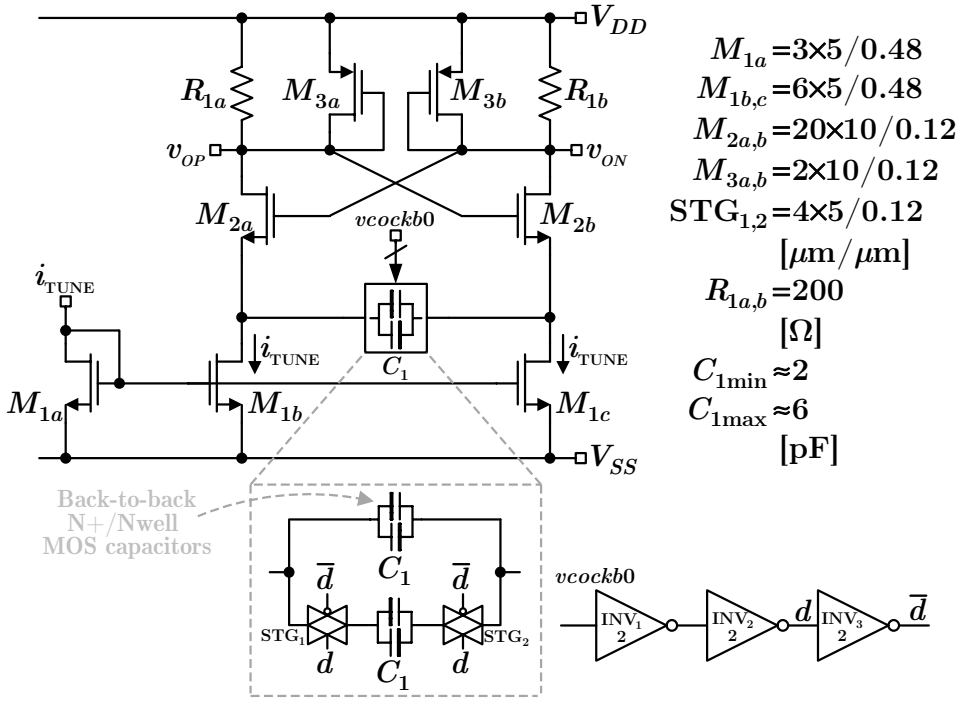

Fig. 6.17: Schematic of the relaxation oscillator.

The implementation of the switched-capacitor bank C_1 is similar to that of the two-integrator oscillator, despite that here N+/Nwell MOS varactors are used in place of MOM capacitors. This different choice is justified to achieve a higher capacitance per area density, since we need to integrate relatively larger capacitors for the relaxation oscillator than for the two-integrator oscillator[6]. N+/Nwell MOS varactors suffer from capacitance modulation due to the voltage magnitude across their terminals. This time-varying capacitance translates into output distortion, amongst other subtle effects. However, the distortion at the output of the relaxation oscillator is not an issue as it is in the case of the two-integrator oscillator.

As we already discussed elsewhere, the N+/Nwell MOS varactors are inherently asymmetrical. Hence, to keep the layout of the relaxation oscillator as symmetrical as possible, we divided the switched-capacitor bank C_1 by half and connected each half array in opposite (back-to-back) direction. Doing this, we avoid systematic unbalances that may compromise the performance of the relaxation VCO.

The simulated discrete tuning curves of the relaxation VCO are shown in Fig. 6.18. As discussed in Sec. 6.2.2, one of these curves is centered around 500 MHz and another is centered around approximately 1 GHz. The slowest curve has a maximum K_{VCO} of about 65 MHz/V in the linear region, while the fastest curve has a VCO gain of about 130 MHz/V.

The phase noise of the relaxation VCO operating in open loop (i.e., free-running)

[6]Apparently, this argument seems contradictory, since the relaxation oscillator operates usually at twice the speed of the two-integrator oscillator and, according to Eq. 6.5, the oscillation frequency is inversely proportional to the capacitance C_1. However, this comparison is not meaningful because the operation principles that govern both oscillators are completely distinct.

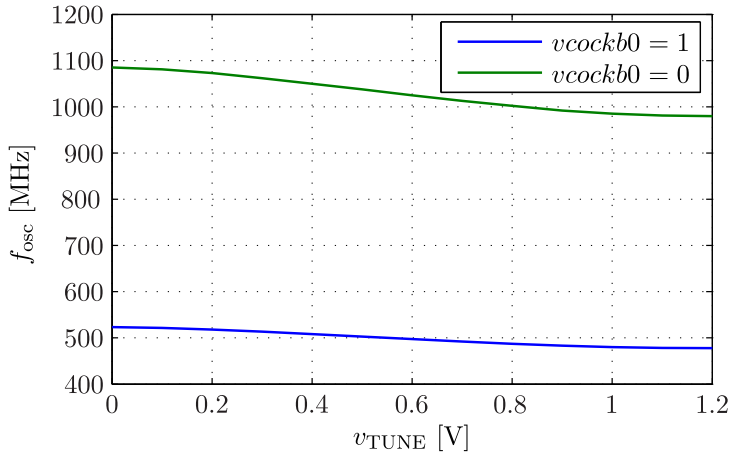

Fig. 6.18: Simulated discrete tuning characteristics of the relaxation VCO.

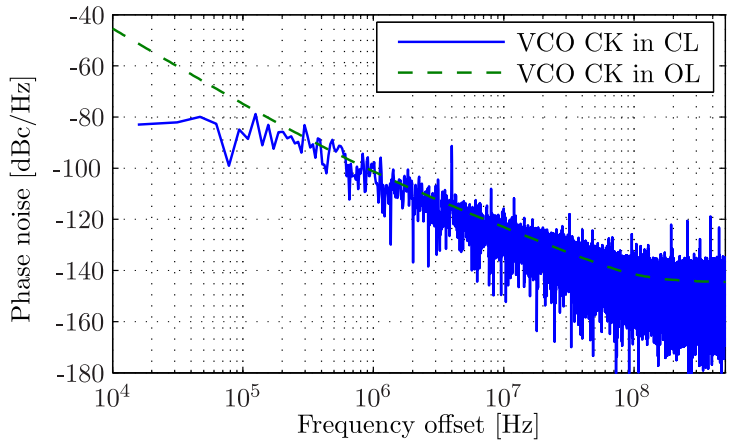

Fig. 6.19: Simulated phase noise of the relaxation VCO running in open loop and in closed loop (i.e., incorporated into PLL CK) at a fundamental frequency of 1,024 MHz.

at a fundamental frequency of 1,024 MHz is shown in Fig. 6.19, alongside with the corresponding phase noise when it is inserted into the PLL CK (i.e., in closed loop operation). Up to the PLL CK bandwidth, approximately 200 kHz, the VCO phase noise is significantly suppressed, and, at higher frequency offsets, the total phase noise is mainly limited by the own phase noise of the VCO. The resulting rms jitter integrated above 1 MHz is about 1.8 ps. This lower-end integration limit of 1 MHz allows estimating the rms jitter that would be present in an FFT of 1,024 points sampled at a conversion rate of 1,024 MS/s (which would lead to an FFT resolution of $(1,024\,\text{MS/s})/(1,024\,\text{pts}) = 1$ MHz and an observation time of 1 μs[7]). Close-in phase noise fluctuations with frequency offsets lower than this integration limit affect the clock signal transitions negligibly within the observation time [64, p. 14].

The differential output signal generated by the relaxation VCO must be converted to a full-swing CMOS digital signal before being applied to the digital frequency divider of PLL CK. As a result, a differential-to-single-ended converter as the one shown in

[7]The observation time is the time length spent to collect the desired amount of samples.

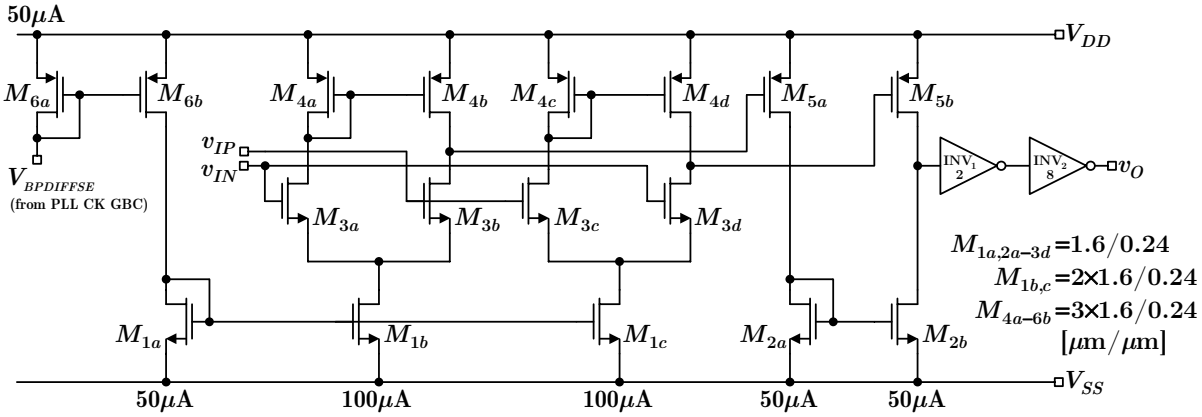

Fig. 6.20: Schematic of the differential-to-single-ended converter employed in PLL CK. The biasing voltage $V_{BPDIFFSE}$ (or more appropriately the mirror reference current) comes from the global biasing circuit of PLL CK.

Fig. 6.20 is used. This DIFF/SE converter is built with to symmetrically connected front-end amplifiers that equalize the propagation delays of v_{IP} and v_{IN} up to the CMOS inverters buffer, and, consequently, ensures a well-behaved close to 50 % output duty cycle [65]. This duty cycle is further improved in the clock phase generator of the ADC (using a divide-by-two D-type flip-flop), since it plays a crucial role in the DUT topology used in this work (i.e., a two-channel time-interleaved pipelined ADC).

To show a global picture of the simulated performance of the proposed BIST system (for a particular set of parameters), the output spectrum of the DUT when it is stimulated by the signals generated by PLL IN and PLL CK (both in lock state) is shown in Fig. 6.21. For this particular simulation, we use an external reference frequency of $f_{\text{ref}} = 4$ MHz, and frequency dividers values of $N_s = 256$, $N_{p_i} = 127$, and $M_j = 2$. Consequently, the synthesized analog input and clock signals have frequencies of $f_{\text{in}} = 127 \times 4/2$ MHz and $f_s = 256 \times 4/2$ MS/s, respectively. Moreover, the amplitude of the analog input signal is set to about 600 $\text{mV}_{\text{pp,diff}}$ through the *amplctrl* signal (refer to Fig. 6.8).

By observing the relevant spectrum content detailed in Fig. 6.22, we note that the worst spurious components are related to the reference spurs of the PLLs, $R_{1l,r}$, which have a magnitude of about −50 dBc and happen at $f_{\text{in}} \pm f_{\text{refpfd}}$[8]. Regarding the harmonics, the third harmonic is the strongest and has a magnitude of about −55 dB. Furthermore, it is clear from this spectrum that coherent sampling is being achieved by the proper synchronization of PLL IN and PLL CK.

The reference spurs in charge pump PLLs are caused by nonidealities mainly in the PFD and CP, which may create a significant ripple on v_{TUNE} even when the PLL is locked and, as a result, lead to a direct modulation of the output frequency of the VCO at multiples of f_{refpfd} around the fundamental frequency[9]. These nonideal issues are thoroughly considered in [66, pp. 562-567] and are further discussed later.

[8]The frequency f_{refpfd} is the frequency at the input of the phase/frequency detector, *not* the external reference frequency.

[9]The loop of a charge pump PLL is updated at a rate of $T_{\text{refpfd}} = 1/f_{\text{refpfd}}$, hence why the reference spurs appear at $f_{\text{in}} \pm k f_{\text{refpfd}}$, $k = 1, 2, ...$ The reference spurs for $k \geq 2$ are associated with the harmonics of aforementioned ripple, which usually have smaller impact.

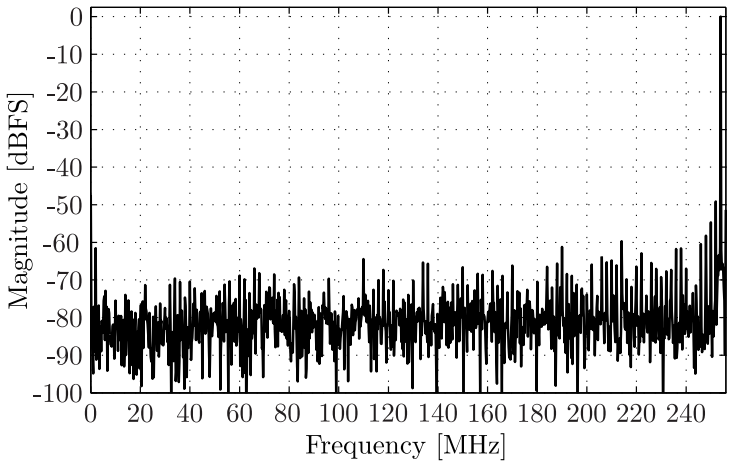

Fig. 6.21: Simulated spectrum (2,048 points FFT) at the output of the DUT when it is stimulated by the signals generated by PLL IN and PLL CK. For this particular simulation, the following parameters are being used: $f_s = 512$ MS/s, $f_{\text{in}} = 254$ MHz, and $V_{\text{in}} \approx 600$ $\text{mV}_{\text{pp,diff}}$.

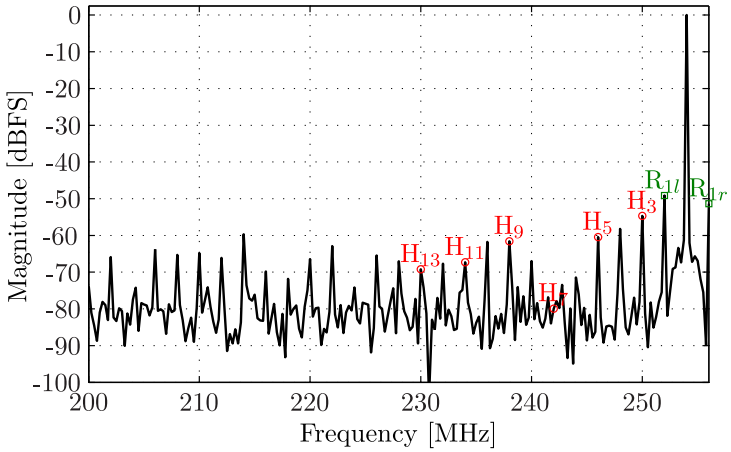

Fig. 6.22: Zoom in of the relevant spectrum content of Fig. 6.21.

6.2.4 Phase/Frequency Detector

The schematic of the sequential three-state phase/frequency detector (PFD) used in this work is shown in Fig. 6.23. It is employed either in PLL IN and in PLL CK, reducing the implementation design efforts.

This circuit is based on a dual D-type flip-flop (D-FF) structure and uses an asynchronous race-free design [67]. Compared to a more conventional NAND-based design, this PFD minimizes the perturbation in the loop filter voltage by reducing the simultaneous activation of the *up* and *dw* signals during steady state operation of the PLL. As a result, the reference spurs and jitter performance are improved.

The propagation delays of the *up* signal and its negated version $\overline{up}$ are equalized by means of a pair of transmission gate (TG) and CMOS inverter, TG_1 and INV_2 respectively. The TG is carefully sized to matched the equivalent delay introduced by the CMOS inventer. This equalization helps to avoid systematic imbalances in the operation

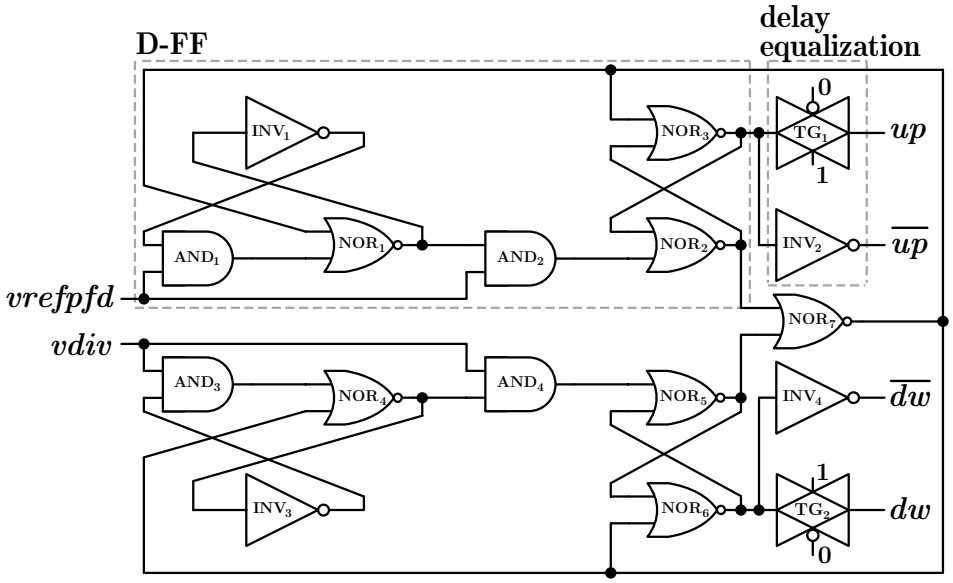

Fig. 6.23: Schematic of the phase/frequency detector employed either in PLL IN and PLL CK. The sizing in μm/μm for all NMOS and PMOS transistors are 0.16/0.12 and 0.48/0.12, respectively, except for the transmission gates, where they are 0.20/0.24 and 0.60/0.24, respectively.

of the charge pumps, which would otherwise increase the reference spurs of the PLL. The same idea is applied for the signals dw and $\overline{dw}$.

The layout of the PFD must be carefully made to ensure good matching between the up and dw logic-related paths, since a considerable layout asymmetry would lead to significant up/dw skew (which would adversely affect the charge pumps operation as well).

6.2.5 Charge Pumps and Loop Filter

The charge pumps (CPs) and the third-order passive loop filter (LF) are schematically shown in Fig. 6.24. The same circuits are used either in PLL IN and in PLL CK, with only a slightly difference in the sizing of the loop filter elements.

In order to reduce the total capacitance of the integrated loop filter, which is desirable to reduce its area overhead, a capacitance multiplication scheme as proposed in [68] is used. This scheme employs a main charge pump connected to the resistor side (R_1) of the loop filter as in a conventional design, and an auxiliary charge pump with a smaller current ($\beta < 1$) connected to the node between resistor R_1 and capacitor C_1'. Additionally, the up and dw switching signals of the two charge pumps are arranged in such a way that, when the main charge pump is sourcing current, the auxiliary one is sinking, and vice versa. With this arrangement, the entire current of the main charge pump flows through the resistor R_1, whereas only the current difference of the two charge pumps (i.e., $(1-\beta)I_{CP}$) flows into the capacitor C_1'. Hence, if we choose $\beta = 0.8$ as an example, the capacitance value of C_1' is only 20 % of the equivalent capacitor C_1 that would be required in a conventional design, since C_1' becomes $(1-\beta)C_1$. As a result, the layout

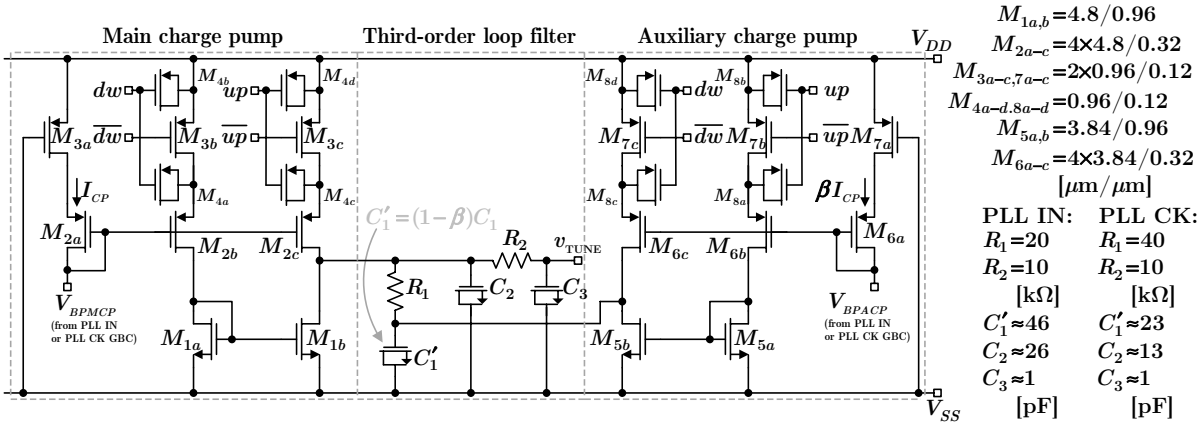

Fig. 6.24: Schematic of the charge pumps and third-order passive loop filter employed either in PLL IN and PLL CK. The biasing voltages V_{BPMCP} and V_{BPACP} (or more appropriately the mirror reference currents) come from the global biasing circuit of PLL IN or PLL CK, depending each one is being considered.

area needed to implement the LF is also reduced by the same factor.

The auxiliary charge pump is a scaled down version (by the factor β) of the main charge pump, and their topology is similar to the one proposed in [69]. Considering only the main charge pump for simplicity, this topology uses two PMOS (M_{2a-c}) and one NMOS ($M_{1a,b}$) current mirrors. Transistors $M_{3b,c}$ act as switches, turning on or off the intended current mirrors. In order to compensate the charge injection introduced by the PMOS switches, these switches include dummy devices (M_{4a-d}) operated in opposite signal phase. Device M_{3a}, always turned on, compensates the R_{on} resistance of the PMOS switches, such that the source terminals of the PMOS current mirrors' devices always "see" an equal impedance towards V_{DD}.

The layout of the charge pumps must be carefully made to achieve good matching among the current mirrors and good overall symmetry for the implemented compensation mechanisms to work effectively.

In this work, the nominal I_{CP} current of the main charge pump is 50 μA, while that of the auxiliary charge pump is 40 μA (i.e., the selected β is 0.8). The simulated up and down output currents of the main charge pump are shown in Fig. 6.25. It is possible to note that, due to the simple current mirrors used, with relatively low output resistance, it is impossible to exactly match the up and down currents through the entire (useful) output range. In fact, these currents are only matched around $V_{OMCP} = 0.6$ V. One alternative to improve the currents matching would be to use cascode current mirrors, but they would lead to another problem: reduced output voltage swing, which is a critical issue in a low-voltage (1.2 V) technology. Hence, even with a significant lower output resistance, we adopted the simple current mirrors in this work to maximize the achievable output voltage swing.

The employed passive loop filter has a third-order transfer function, with three poles

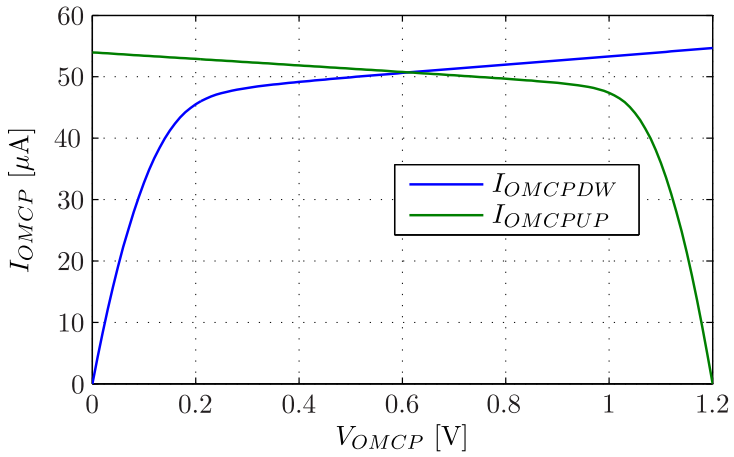

Fig. 6.25: Simulated up and down output currents of the main charge pump.

and one zero, given by

$$\frac{V_{\text{out}}}{I_{\text{in}}} = \frac{1}{s(C_1+C_2+C_3)} \frac{1+sR_1C_1}{\left[1+s\dfrac{R_1C_1(C_2+C_3)+R_2C_3(C_1+C_2)}{C_1+C_2+C_3}+s^2\dfrac{R_1R_2C_1C_2C_3}{C_1+C_2+C_3}\right]} \tag{6.6}$$

Ignoring R_2 and C_3, which are usually added to further suppress the undesirable ripple caused by imbalances in the PFD and CPs, and are sized to have a negligible impact on the dynamics of the PLL, this transfer function simplifies to

$$\frac{V_{\text{out}}}{I_{\text{in}}} \approx \frac{1}{s(C_1+C_2)} \frac{1+sR_1C_1}{\left(1+s\dfrac{R_1C_1C_2}{C_1+C_2}\right)} \tag{6.7}$$

which has a zero at $\omega_z = 1/(R_1C_1)$, two poles, one at $\omega_{p1} = 0$ rad/s and another at $\omega_{p2} = (C_1+C_2)/(R_1C_1C_2)$, and a dc gain of $K_{LF} = 1/(C_1+C_2)$.

The selection of the above loop filter parameters dictates most of the dynamic properties of the PLL, including its stability. Consequently, special attention must be given to this selection. In this work, we optimized the loop filter parameters following the design approach proposed in [70], and the final parameters sizing for both PLL IN and PLL CK, considering a closed loop bandwidth of about 200 kHz[10] and a Butterworth filter response for both of them, is given in Fig. 6.24.

The on-chip implementation of the loop filters, even with the adopted multiplication capacitance scheme discussed earlier, still requires a considerable capacitance amount (tens of pF). Hence, in order to reduce the occupied silicon area as much as possible, the LF capacitors are implemented with MOS devices configured as capacitors. In the technology used, these devices offer the highest capacitance per area efficiency, i.e., about 12 fF/μm^2 when operating in strong inversion.

[10]For a justification about this loop bandwidth choice, refer to the discussion on loop bandwidth presented in Sec. 6.2.2.

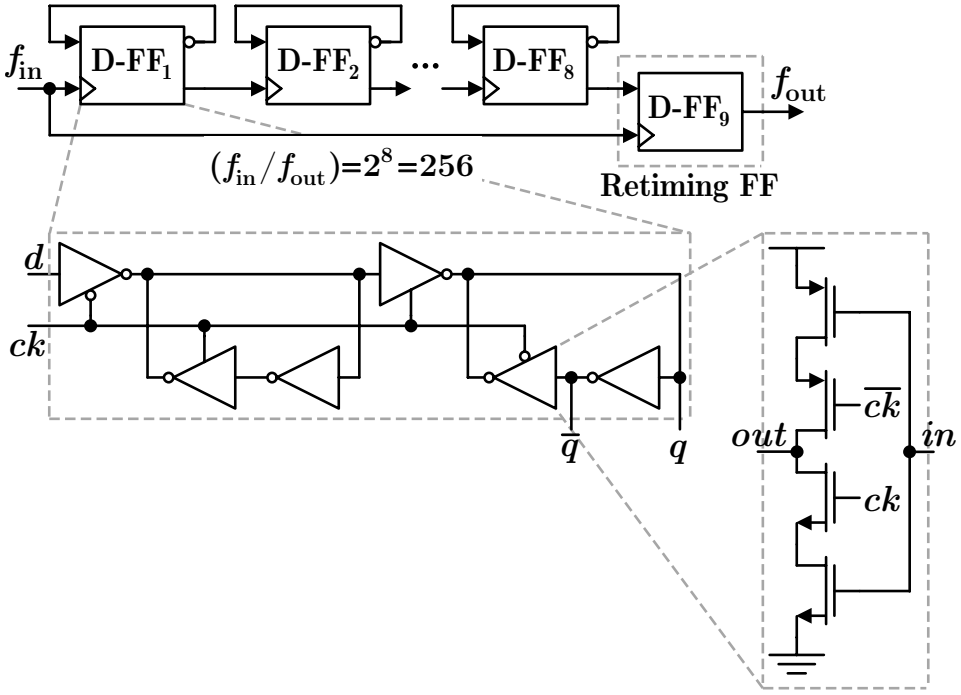

Fig. 6.26: Schematic of the N_s frequency divider of PLL CK.

6.2.6 Frequency Dividers

The proposed BIST architecture, according to Fig. 5.2, requires one fixed frequency divider (for PLL CK) and two programmable frequency dividers (one for PLL IN and another for the external reference signal).

The fixed frequency divider for PLL CK implements a division by a power of two ($N_s = 256$), hence it can be straightforwardly implemented by cascading divide-by-two D-type flip-flop (D-FF) stages, as shown in Fig. 6.26. A well-known problem associated with asynchronous dividers like this is jitter accumulation as the input signal pass through the dividing stages. To remedy this undesirable effect, a retiming D-FF is usually placed at the output and it is clocked by the cleanest signal available (usually the input signal). With this approach, the only jitter source of the whole frequency divider is that of the retiming D-FF.

Fig. 6.26 also shows the schematic of the D-FF used. It is based on two static latches formed by standard CMOS inverters and clocked inverters. Due to the relative low switching frequencies used in this work, dynamic latches, although smaller, are not suited.

The programmable frequency divider for PLL IN (N_{p_i}) is based on a modular structure consisting of a chain of 2/3 divider cells connected like a ripple counter [71], as it is shown in Fig. 6.27. This modular design avoids the presence of long delay loops (each cell interacts adjacently only), and facilitates the layout because cells are identical. Each 2/3 divider cell is built using four D-FFs and three AND gates. The implemented divider has division ratios in the range of 32 to 127 and is programmable through the binary word $pin0, pin1, \ldots, pin6$. For the same reasons discussed above, a retiming FF is employed at the divider output.

The programable frequency divider for the external reference frequency (M_j) is simply

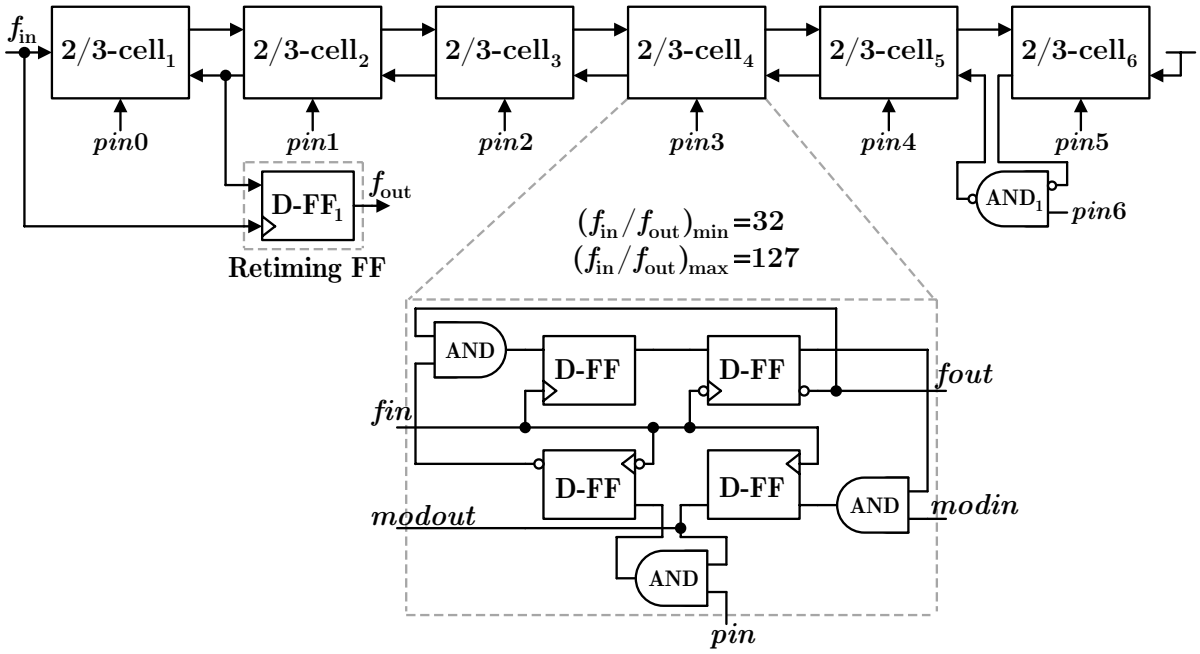

Fig. 6.27: Schematic of the N_{p_i} programable frequency divider of PLL IN.

implemented by a divide-by-two D-FF followed by a multiplexer, since its purpose is to let the external reference signal to pass without any division or to divide it by two.

The transistors used to build the above frequency dividers are sized with the minimum W/L aspect ratio allowed by the technology[11] to reduce both the peak and the average currents. Since this minimum sizing does not lead to a strong drivability, when required, appropriate CMOS inverters buffers follow the frequency dividers.

Also, since the frequency dividers N_s and N_{p_i} operate at the maximum speed of the respective PLLs, they are usually one of the dominant sources of substrate noise. Consequently, protection guard rings are used around their layouts to attenuate substrate noise propagation to adjacent sensitive circuits.

6.2.7 Interfacing Circuits

In this section, we describe the essential interfacing circuits, starting with the description of the linear buffer that follows the two-integrator VCO and drives the THA of the ADC under test. We then discuss the configurable counters, which are used for system configuration. Besides of these interfacing circuits, analog and digital multiplexers are needed to interface the analog input and clock signal generated by the BIST system, respectively. Since these multiplexers are embedded into the ADC circuitry, they are addressed in Sec. 6.3.2.

[11]Specifically, the size of the NMOS transistors is 160 μm/120 μm and of the PMOS ones is 480 μm/120 μm. The width of the PMOS transistors is three times that of the complementary NMOS ones to compensate the lower holes' mobility.

Linear Buffer

The linear buffer that drives the front-end track-and-hold amplifier (THA) of the ADC is, by far, the most challenging interfacing circuit. The main reason for this is the nature of the THA input impedance: it is a heavily nonlinear, switched load. Together with the CMOS technology used, which is not suitable to the design of this type of buffers [72,73], we ends up with a great design challenge.

In CMOS technology, a source follower stage is generally used for buffering analog signals. The simplest source follower is composed of an NMOS transistor (or a PMOS one, in case of a PMOS source follower) and a current source connected to its source terminal. The output signal is derived at the source of the NMOS transistor, and it is level-shifted by V_{GS} (gate-to-source voltage) with respect to the gate terminal; hence, the name "source follower".

Despite of its simplicity, the simple source follower has a considerably high output resistance, which makes it unsuitable to the application considered in this work. As a result of this limitation, improved topologies are proposed in the literature. In this work, we closely consider the "super source follower" [74, pp. 212-214] and the "modified super source follower" [75] topologies.

The super source follower (see top left-side of Fig. 6.28) uses an additional transistor (M_2) and an extra current source (I_2) with regard to the simple source follower. This additional transistor implements a negative feedback loop around M_1, reducing the output resistance R_o by a factor of approximately $g_{m2}r_{ds1}$, where g_{m2} and r_{ds1} are the small-signal transconductance and drain-to-source resistance of M_2 and M_1, respectively. Since intrinsic gains ($g_{m2}r_{ds1}$) in the order of 20 or more are readily implemented in the CMOS technology used, the output resistance with regard to the simple source follower is reduced by a factor of 20 or more.

One of the limitations of the super source follower is the available input/output voltage swings. For the NMOS implementation shown in Fig. 6.28, the maximum input swing is not V_{DD} (as it would be in the simple source follower), but $V_{DD} - V_{DS\text{sat}}$ instead, where $V_{DS\text{sat}}$ is the drain-to-source voltage required to keep the MOS transistors in saturation. This restriction happens because, with the addition of M_2, the voltage at node v_X must be $V_{DD} - V_T - V_{DS\text{sat}}$ to keep M_2 saturated (V_T is the threshold voltage of the MOS transistors). Consequently, and since the NMOS and PMOS transistors have roughly the same V_T in the technology used, the maximum allowed voltage at the gate of M_1 that keeps M_1 saturated is $V_{DD} - V_{DS\text{sat}}$ (which comes directly from the well-known square-law saturation rule of $V_{DS} \geq (V_{GS} - V_T)$).

In this work, the input full-scale range of the ADC is 0.8 $V_{\text{pp,diff}}$ and its input common-mode voltage is centered around $V_{DD}/2 = 0.6$ V. The ADC can only tolerate input common-mode voltage variations of about 600 ± 50 mV without significant performance penalties (see Sec. 7.4.4, specially Figs. 7.17 and 7.18). That is, we are not allowed to set the output common-mode voltage of the linear buffer deliberately, since, to give some margin for manufacturing process shifts, it needs to be nominally 0.6 V.

Considering the output swing of the super source follower shown in bottom left-side of Fig. 6.28, which is derived from typical V_T and $V_{DS\text{sat}}$ values, we note that centering it around 0.6 V requires the input common-mode level to be increased to 1.0 V, since both levels are separated by $V_{GS1} = V_T + V_{DS\text{sat}} = 0.4$ V. This in turn restricts the

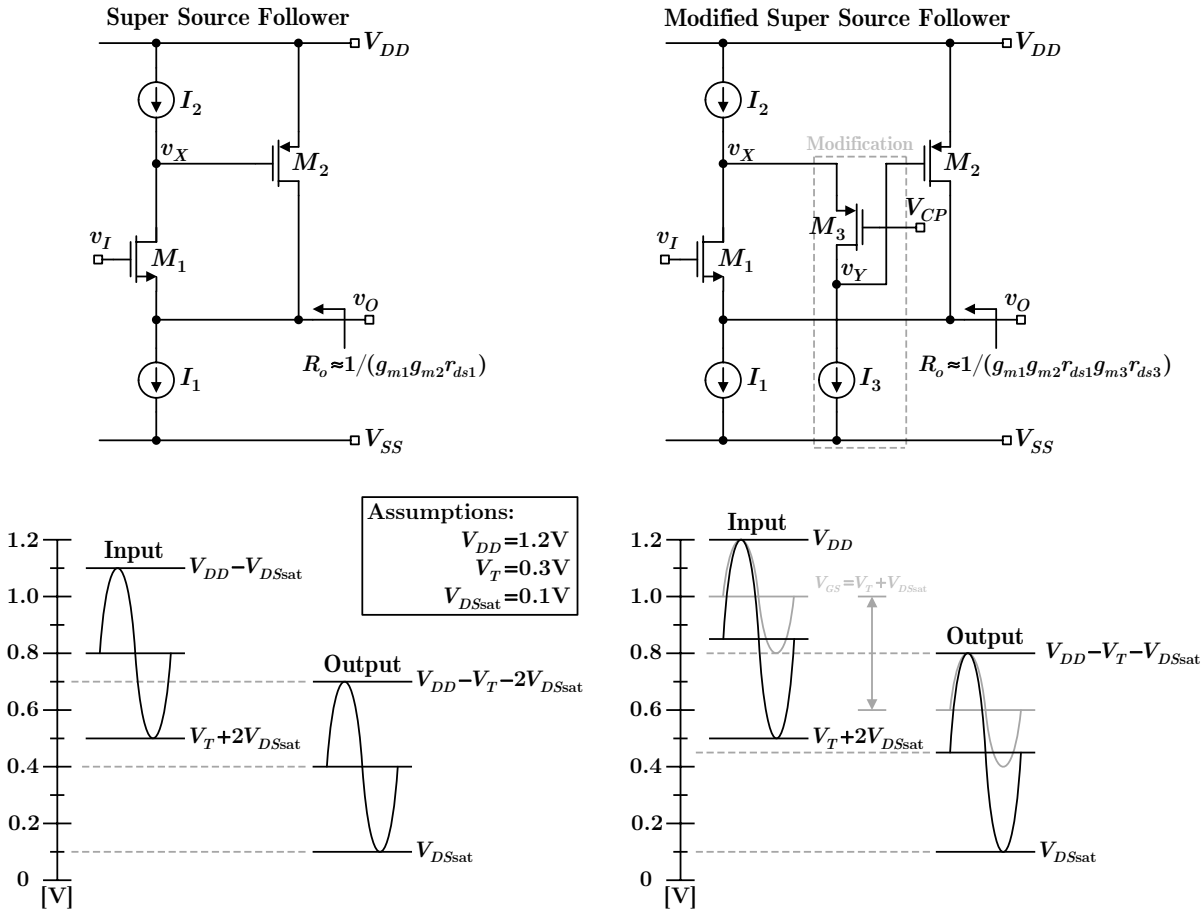

Fig. 6.28: Output resistance and maximum input/output voltage swings comparison between the super source follower (left) and the modified super source follower (right).

maximum input voltage swing (and the output swing as well) to about 0.2 V_{pp}. And, consequently, it would lead to a maximum peak-to-peak differential output voltage (when using two complementary super source followers in a pseudo-differential configuration) of only 0.4 $V_{pp,diff}$.

It is clear from the above discussion that, even with a significant improved output resistance with respect to the simple source follower, the super source follower has voltage swing limitations that make it unsuitable for the application considered here. Therefore, a modified version of the super source follower, which overcomes these swing limitations, is analyzed below.

The modified super source follower [75] is shown in the top right-side of Fig. 6.28. With respect to the super source follower topology, it adds an additional stage, composed of M_3 and I_3, between the drain of M_1 and the gate of M_2. This extra stage breaks the swing limitations of the super source follower and, additionally, improves even more the output resistance. Specifically, the input/output voltage swings become equivalent to those of the simple source follower, and the output resistance becomes $R_o \approx 1/(g_{m1}g_{m2}r_{ds1}g_{m3}r_{ds3})$, i.e., it is improved by a factor of $g_{m3}r_{ds3}$ with respect to the super source follower.

As it is shown in light gray in the bottom right-side of Fig. 6.28, the modified topology may fulfill both the output voltage swing (0.8 $V_{pp,diff}$) and the output common-mode

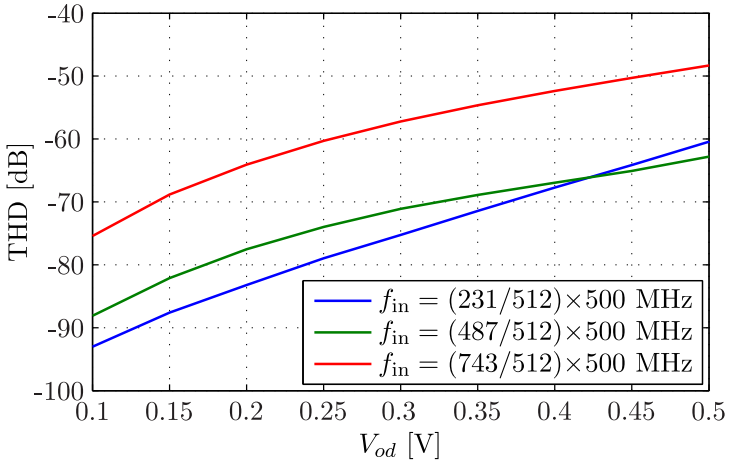

Fig. 6.29: Simulated THD of the linear buffer versus output differential amplitudes and three distinct input frequencies.

voltage (0.6 V) required by the ADC used in this work.

The benefits of the modified super source follower topology come with an increase in design complexity, since now the circuit behaves as a third order system, with one dominant pole at v_Y and two nondominant poles at v_O and v_X (the latter at a higher frequency in most practical cases). Despite of this extra complexity, it is still feasible to design such a follower in the employed CMOS technology.

The complete schematic of the modified super source follower used in this work, together with its sizing, is shown in Fig. 6.30. To achieve differential signaling, two complementary followers are used in a pseudo-differential configuration. In order to set a biasing voltage of 1 V at the input of the followers, which would lead to an output common-mode voltage of about 0.6 V, a high-pass RC network, composed of C_{1a} and $R_{1a,b}$ for the positive path and C_{1b} and $R_{1c,d}$ for the negative one, is used.

The biasing signals are generated by a local biasing circuit, which receives a reference current from the global biasing circuit (GBC) of PLL IN. Moreover, to avoid loading the two-integrator VCO asymmetrically, which could compromise its performance, a dummy structure of the followers is used for the quadrature-phase output of the two-integrator VCO.

The layout of the proposed linear buffer is done with special care for the two pseudo-differential followers to work as close as possible of an equivalent true-differential circuit. Such care includes laying out the two complementary paths (positive and negative) as symmetrical as possible.

The simulated THD of the linear buffer driving the THA operating at 500 MS/s for different output differential amplitudes and three input frequencies is shown in Fig. 6.29. We note that the THD degrades as both V_{od} and f_{in} increase, as expected. For $f_{\text{in}} = (487/512) \times 500$ MHz and $V_{od} = 0.4$ V $= 0.8$ $V_{\text{pp,diff}}$ (i.e., the maximum output voltage swing demanded by the linear buffer), the THD is about -67 dB.

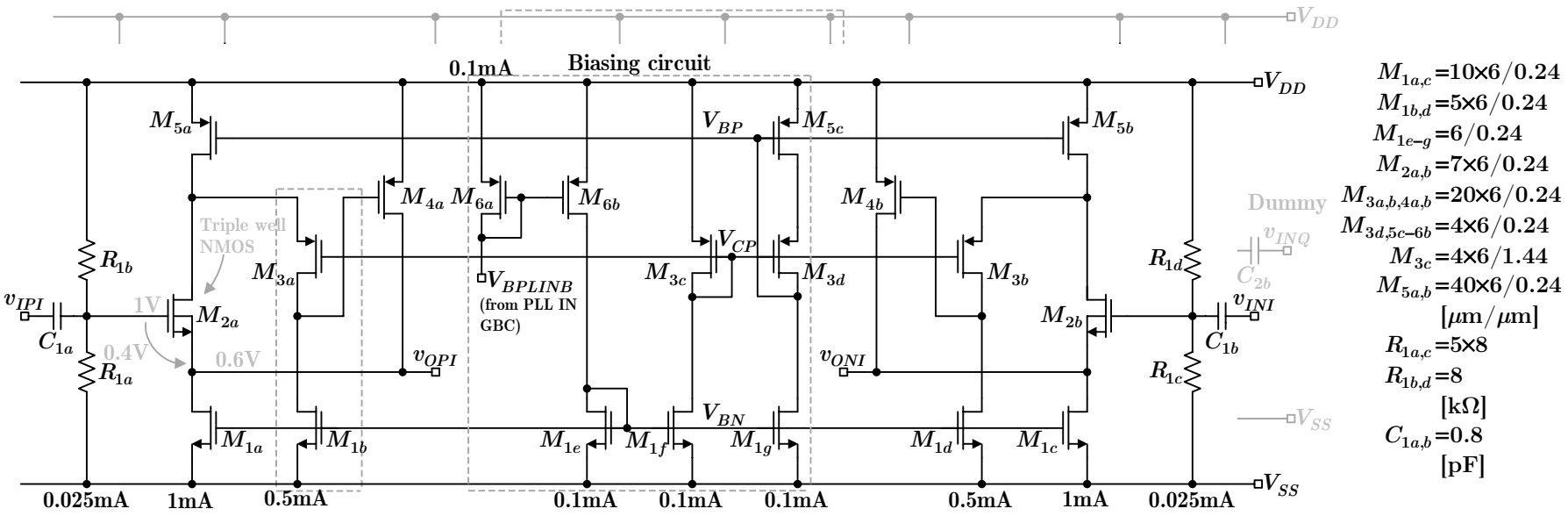

Fig. 6.30: Schematic of the pseudo-differential linear buffer that drives the ADC input. The biasing voltage V_{BPLINB} (or more appropriately the mirror reference current) comes from the global biasing circuit of PLL IN. A dummy structure is used to symmetrically load the two-integrator VCO.

Configurable Counters

The simplified schematic of the implemented configuration logic is shown in Fig. 6.31. The configurable counters are implemented with simple asynchronous counters, which react upon the transitions of the respective external control signals. One of these counters (the DIV IN counter) is slightly more complex than the others, since it implements up and down counting. This up/down feature is added to avoid long wrap around loops, since it is a 7-bit counter with $2^7 = 128$ possible states.

The noisy digital output drivers of the ADC change state on the rising transitions of the *ckout* signal, which create a bounce on the power supply of the digital I/O cells. Since the implemented counters are asynchronous, they could react to these bounces and originate false toggles that could inadvertently change their internal states. To overcome this potential issue, all external control signals are synchronously sampled on the falling edges of *ckout*. With this approach, we give half *ckout* period for the I/O power supply recover from the transient bounces and, consequently, we significantly reduce the likelihood of false toggles.

An external rst signal allows forcing a known state to all configurable counters. This signal is also synchronously sampled on the falling edges of *ckout* for the same reasons pointed out above.

A detailed discussion on the operation of these configurable counters and how their states affect the system configuration is given in Appendix A.

6.3 DUT Circuitry: High Speed Pipelined ADC

In this section, we give an overview of the high speed ADC (DUT) implemented, which is based on a pipeline architecture. After this overview, we discuss specific small changes in the ADC needed to interface it with the proposed BIST scheme.

6.3.1 Pipelined ADC Overview

One of the key features of the BIST approach proposed in this work is its great independence with regard to the DUT architecture, since it "sees" the ADC as "black box". That is, the BIST circuitry does not demand complex changes in the DUT to be successfully implemented. This property, besides of extending the feasibility of the proposed self-test scheme to virtually all high speed ADC architectures, has the merit of not compromising the performance of the DUT in normal operation (i.e., after the BIST execution), since during that regime the BIST circuitry is "transparent" to the ADC. Specially in high speed ADCs, adding intrusive circuits for functions other than the essential ones is particularly not attractive, given that these unwelcome circuits may change the load, couple extra noise, etc.

With the above feature, any high speed ADC architecture chosen to function as the DUT in this work would certainly lead to the same overall conclusions, given the specific interfacing issues were properly addressed. In this work, however, we choose the pipeline ADC architecture because *i*) it is indeed a very common high speed architecture in CMOS technology [76, chap. 3], and *ii*) it is the architecture more familiar to the author.

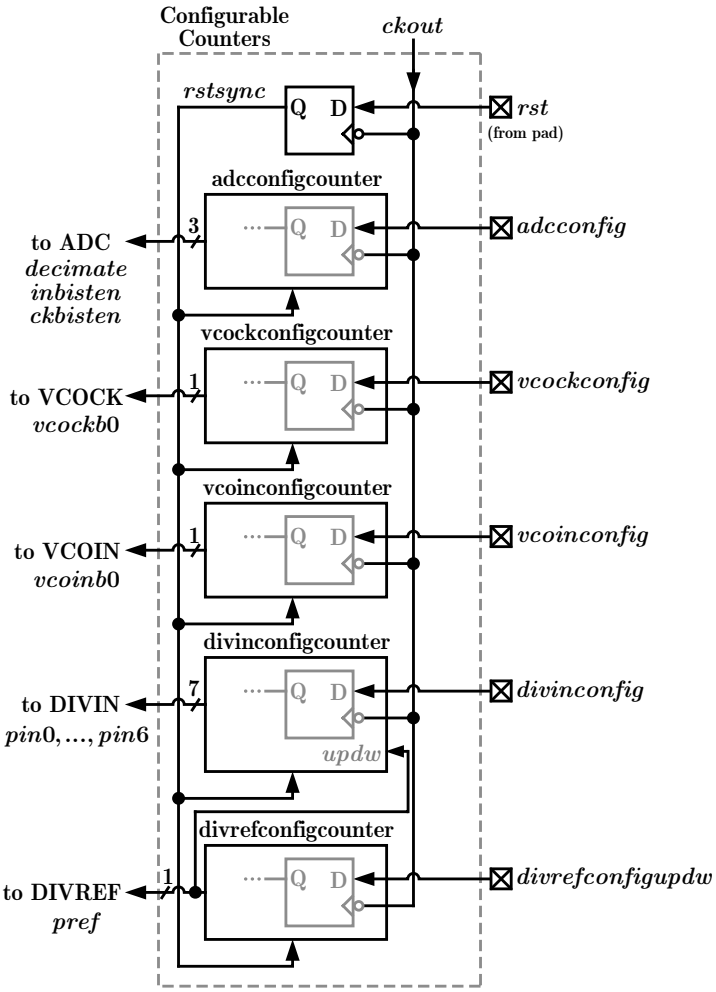

Fig. 6.31: Simplified schematic of the configurable counters.

With the pipeline architecture in mind, the main design goals were to achieve the highest A/D conversion speed with a resolution of about 8 bits in a 0.13 μm CMOS technology, which would allow to experimentally verify the limitation of the proposed BIST technique[12]. The power dissipation per conversion, usually an important specification, plays an irrelevant role in this context (after all we are not proposing a novel state-of-the-art ADC). The architectural highlights of the designed A/D converter are briefly considered next.

The block diagram of the implemented 8-bit resolution pipelined ADC is shown in Fig. 6.32. The analog/mixed-signal core of the ADC is composed of a track-and-hold amplifier (THA), six 1.5 bit pipeline stages, and a back-end 2-bit flash ADC. On the other hand, digital core is composed of a synchronization logic, a digital correction logic, a 2:1 8-bit multiplexer, an 8-bit output register, a digital output buffer, and a decimation logic. The auxiliary circuits include an internal clock circuitry, a clock distribution tree, a reference voltages generator/buffer, a global biasing circuit (GBC), and bypass capacitors.

[12]Note that this approach is opposite to what is normally the case, i.e., the BIST scheme with higher accuracy than the DUT. Since in this work we are exploring the virtues/bondaries of the proposed idea, we proceeded differently than the usual application.

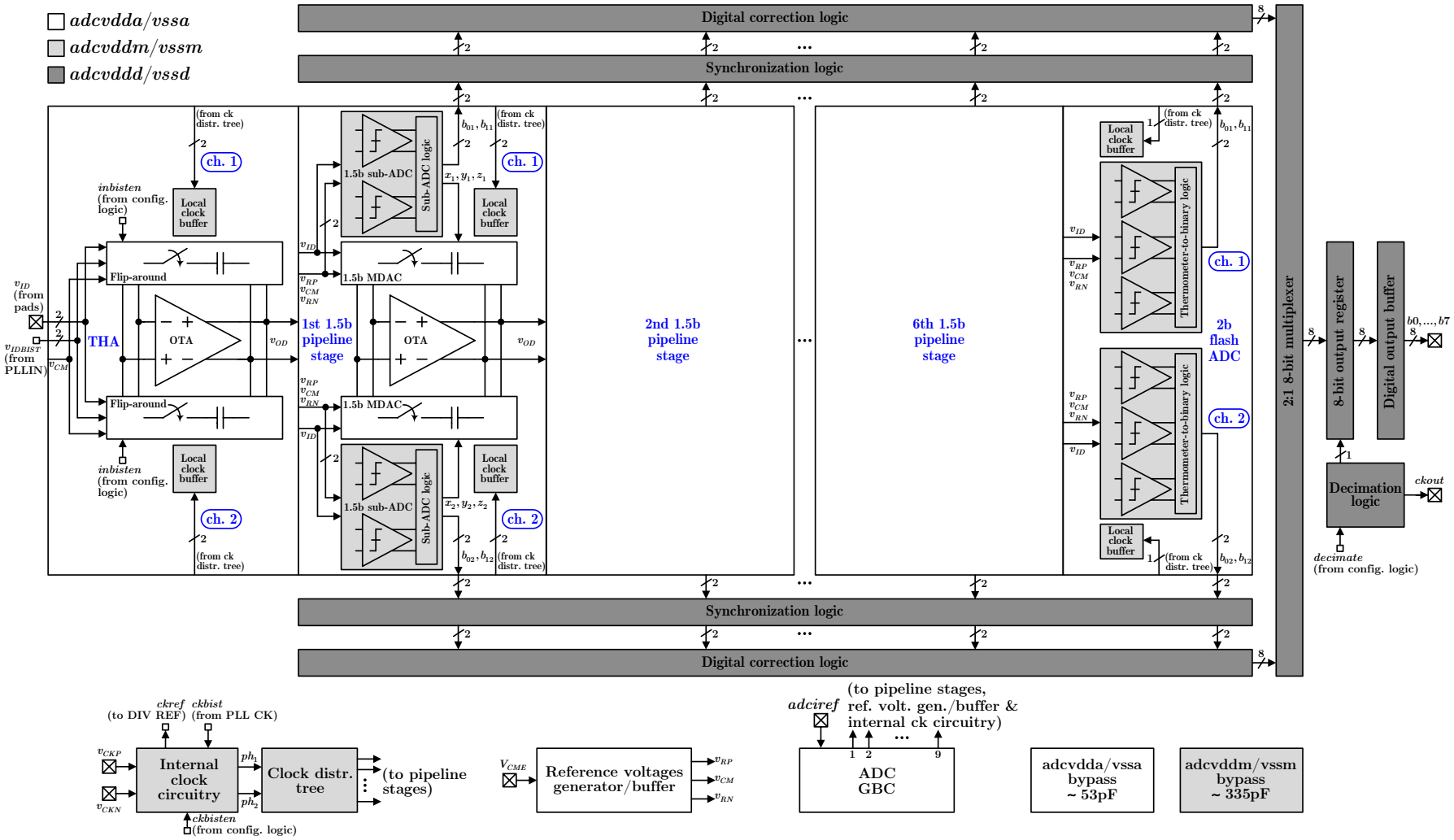

Fig. 6.32: Block diagram of the 8-bit two-channel time-interleaved pipelined ADC.

To maximize the attainable A/D conversion speed in the employed technology, without excessively increasing the design complexity, a two-channel time-interleaving approach is used. Instead of duplicating the whole A/D conversion channel, only some elements are duplicated while others are shared between the two channels. Specifically, in the implemented design the shared elements are the power- and area-hungry operational transconductance amplifiers (OTAs). Such sharing technique is also termed "double-sampling" in the literature [77].

With a two-channel time-interleaved converter, each A/D conversion channel operates at half the full ADC speed. This allows a time slot for settling the OTAs, which are usually the building blocks that limit the maximum conversion speed, to be twice as larger than that of a single channel converter operating at same f_s. Each OTA operates such that, when one of channel is sampling (i.e., not needing the OTA), the other channel is using it for amplification, and vice versa.

Besides of the advantages above, the time-interleaving approach also has its weaknesses, such as the introduction of spurious tones in the output spectrum of the ADC due to inter-channel offset, gain, and timing mismatches. Timing mismatch is particularly critical in high speed ADCs, since it becomes challenging to fulfil the tight timing requirements demanded in the front-end track-and-hold: ideally, the adjacent sampling instants should have a phase difference of exactly 180° (in a two-channel time-interleaved converter), but, due to manufacturing process mismatches, a time skew usually exists between channels. The manifestation of these shortcomings is noticeable in the measurements presented in Sec. 7.4.1.

The track-and-hold amplifier, which is further consider later in Sec. 6.3.2 with regard to the interfacing issues with the proposed BIST scheme (i.e., whether it samples signal v_{ID}, provided externally, or v_{IDBIST}, provided internally by PLL IN), is based on a flip-around topology [78], where the positive (or negative) path sampling capacitor is connected between the non-inverting output and inverting input (or inverting output and non-inverting input) of the OTA during amplification phase. Since this topology has an ideal feedback factor, β, of one (neglecting the input parasitic capacitance of the OTA), it dissipates less power to achieve higher speeds and has lower noise than other usual implementations. However, as explained in [78], assuming the OTA has limited input common-mode range (as is the case of the OTA topology used in this work), the analog input common-mode voltage needs to be accommodated within this range, otherwise the performance of the OTA will drop considerably. This is one of the main weaknesses of this THA, and it should be addressed carefully when determining the common-mode voltages, as it was done, for instance, in Sec. 6.2.7 for the linear buffer.

The signal held at the output of the THA is processed by a chain of six topologically-identical 1.5-bit pipeline stages in a discrete-time fashion (cf. Fig. 6.32). Each channel within one of these stages is built with a switched-capacitor (SC) 1.5-bit multiplying digital-to-analog converter (MDAC), which interacts with the shared OTA to implement the intended function, a 1.5-bit sub-ADC, which is composed of two latched comparators and some simple encoding logic, and a local clock buffer. The 1.5-bit MDAC, besides of implementing a three-level DAC characteristic, also implements a multiply-by-two function (i.e., a gain of two is applied to the input signal). The 1.5-bit sub-ADC generates

a 1.5-bit output[13], b_{01}, b_{11} for channel 1 and b_{02}, b_{12} for channel 2, with half-bit redundancy. This redundancy helps to relax the design of the latched comparators, and it means that each 1.5-bit pipeline stage contributes effectively with one bit in the final ADC resolution. Moreover, the sub-ADC generates the required x, y, z encoding for the proper operation of the MDAC. The local clock buffer receives two clock phases, ph_1 and ph_2, from the clock distribution tree, generates other clock phases when required (e.g., negated and earlier versions[14]), and then buffers all clock phases before sending them to the required clock-driven circuits.

Together with the front-end THA, the 1st pipeline stage has the more stringent demand in terms of performance, since, as the analog input signal goes through the pipeline, gain is added to it and, consequently, it becomes less susceptible to usual nonidealities. In other words, the design of the front-end THA and 1st pipeline stage requires much more care than the following pipeline stages, which are usually a scaled down copy of the 1st pipeline stage.

The analog/mixed-signal core of the ADC is completed with a 2-bit flash ADC, which contributes with two bits in the overall resolution. Each channel of this flash ADC is composed of three latched comparators followed by a thermometer-to-binary encoding logic. Additionally, as in other stages, a local clock buffer per channel is also used.

The digital core of the ADC starts with a synchronization logic, whose purpose is to align the output bits associated with the same sample processed throughout the pipeline stages. This alignment is achieved with a chain of D-type flip-flops (a digital delay line) for each pipeline stage output, with longer delays for the first stages. After synchronization, the output bits go through a correction logic, composed of seven 1-bit full adders (per channel), to achieve the final 8-bit representation of the sampled analog input signal. This digital correction logic makes use of the pipeline stages' half-bit redundancy to compensate (or "correct") specific imperfections occurred during the A/D conversion (e.g., the ones introduced by offset of the latched comparators).

The above synchronization and correction takes place for each channel individually. As so, the corrected 8-bit digital output per channel is at half the full speed of the ADC, with a phase difference of 180°. In order to combine the digital data of the two channels into a single 8-bit digital signal at full speed (i.e., f_s), a 2:1 8-bit multiplexer is employed.

Since sampling frequencies in excess of 500 MS/s are achieved with the ADC implemented in this work, and given that the output buffers use CMOS-level signaling (3.3 V), it is unfeasible to send the digital data off-chip at full speed. Doing so, and assuming the output buffers had the demanded drive strength (refer to Sec. 7.2.1), these buffers would create a lot of digital noise that would strongly degrade the overall performance of the ADC.

Since the use of different signaling options suited for high frequencies, like low-voltage differential signaling (LVDS), were not a choice due to the restricted number of the I/O pins[15], we implemented a decimation logic whose purpose is reduce the output data rate

[13] A 1.5-bit digital signal is represented by two bits, but has only three possible states instead of four.

[14] The earlier clock phases are used for bottom plate sampling, a well-known technique employed in SC circuits that reduces signal-dependent charge injection.

[15] For example, an LVDS driver uses two pins instead of one, since a current is sourced/sinked to/from an external resistor. Therefore, the number of output pins would double with respect to the CMOS signaling case considered.

by a factor of 15. (Note that, for a two-channel time-interleaved ADC, it is a must to decimate by an *odd* number; otherwise, data of only one of the channels would be sent off-chip.) Hence, even with an actual (internal) $f_s = 500$ MS/s, the data sent off-chip is at $f_s/15 \approx 33$ MS/s.

The decimation logic, based on the state of the *decimate* signal from the configuration logic (which is under control of the user), controls the latching (strobing) instants of an 8-bit output register, composed of eight parallel D-FFs, imposing the desired data rate. When *decimate* signal is logic high, the output is decimated by 15, conversely, when it is logic low, the data is sent off-chip at full speed[16]. The same signal used to strobe the output register is buffered and sent off-chip as *ckout*. Since the output register is strobed at the rising edge of *ckout*, the ideal edge for collecting the output data off-chip is the falling edge of *ckout*, giving sufficient time for the outputs to stabilize.

While the decimation per se does not affect the performance of the ADC, it can indirectly contribute to some metrics, since the observation time for collecting a given data set is increased by the same amount of the decimation factor. For instance, if the jitter of the clock signal used to drive the ADC accumulates over time, the larger observation time will lead to higher SNR than would be the case when collecting the same length data set at full speed. This specific issue is also discussed in Sec. 6.2.3, since it is an important argument within this work.

The digital core is completed with an 8-bit digital output buffer that buffers the output bits up to the output drivers at the I/O ring (which are the "true" buffers for the external load, and also embody specific functionalities like the 1.2 V to 3.3 V CMOS level shifting).

Some auxiliary circuits are included on-chip to make possible the realization of the ADC. Firstly, an internal clock circuitry, which is further consider in Sec. 6.3.2 since it entails some interfacing issues with the proposed BIST scheme, is used. This clock circuitry receives an ac-coupled external differential signal (v_{CKP} and v_{CKN}) and generates two non-overlapped clock phases, ph_1 and ph_2. In order to save pins, the external reference signal for the PLLs (*ckref*) is also generated by this block. Moreover, according to the state of *ckbisten* (under control of the user), the generated clock phases may rely on the clock generated by PLL CK (i.e., *ckbist*) instead of v_{CKP}/v_{CKN}. Specifically, when *ckbisten* is logic low, the clock phases ph_1 and ph_2 reflect the external clock signal provided at pins v_{CKP} and v_{CKN}. Conversely, when *ckbisten* is logic high, the clock phases ph_1 and ph_2 reflect the internal clock signal provided by PLL CK.

The reason for using differential signaling instead of a full-swing CMOS signal for the input of the internal clock circuitry is the same as the one mentioned earlier of the output bits (i.e., strong digital noise generation and coupling), with the aggravating fact that any noise on the clock signal (or coupled from it to other sensitive signals, e.g., the analog input) translates almost directly into the output spectrum of the ADC, restricting the ADC performance. Indeed, for high speed ADCs, the clock signal path should be treated with the same special care as that of the analog input path, since both paths may deteriorate the performance of the ADC if treated negligently.

The differential clock signal provided externally is of sinusoidal shape which "smoothly" goes through the bond wires inductance and its amplitude is limited to few hundreds mil-

[16]This full speed feature is added mainly for debugging purposes at low data rate.

livolts to not cause any strong perturbation to sensitive internal signals. On-chip, after crossing the bond wires and related interfacing issues between the PCB and the chip, this differential clock is converted to a full-swing CMOS signal and used with normal CMOS logic gates.

Since the analog/mixed-signal core of the designed ADC is relatively big (see Fig. 6.33), distributing the required high speed clock phases is considerably challenging. Hence, a second auxiliary circuit, a clock distribution tree, is employed. With this tree, composed of CMOS inverters with distinct drive strengths, the distribution of ph_1 and ph_2 up to the vicinity where they are used is significantly simplified. Close to the target circuits, these clock phases are locally regenerated (in case other specific clock phases are needed) and buffered, before being applied to the target.

A third auxiliary circuit employed is a reference voltages generator and buffer, which internally generates and buffers the voltages V_{RN}, V_{CM}, and V_{RP} (used throughout the pipeline stages) based on an external voltage V_{CME} (which ideally equals V_{CM}, i.e., the internal analog ground, at the buffer output). This internal buffer is implemented to avoid deterioration on the reference voltages due to the nature of the load driven by these voltages, that is, a switched-capacitor load (larger than approximately 1 pF in worst-case). This switched load, directly interacting with the bond wires inductances (in the case an internal buffer is not used), would lead to significant bounces on the reference voltages, which would deteriorate the performance of the ADC as well.

The above bounce issue could be alleviated by employing large on-chip bypass capacitors on the reference voltages provided externally, but this solution would entail a significant area, much larger than the solution using an internal buffer. Hence, given that in this design we are not primarily concerned with the power dissipation, we implemented the reference voltages buffer on-chip.

A fourth auxiliary circuit used in the ADC design is a global biasing circuit (GBC), similarly as used in the design of the PLLs. This GBC distributes the required biasing signals (reference currents) in the current domain, which is attractive when distributing biasing signals to physically distant circuits. Then, locally, these biasing signals are mirrored to the required MOS transistors with well-matched current mirrors.

The ADC design employs three different power supply domains: analog, mixed-signal, and digital, which are progressively more noisy following this order. The appropriate separation of these power domains when selecting which domain to use for each building block plays a crucial role in the overall performance of the ADC. This power domain separation is judiciously done (with the aid of simulations) and it is clearly indicated in different gray tonalities in in Fig. 6.32. Basically, the cleaner analog domain is used by the OTAs (and related SC networks), the reference voltages generator/buffer, and the global biasing circuit. The mixed-signal domain is used by all clock circuitry (including clock distribution tree and local clock buffers), and by the latched comparators (and adjacent encoding logic). Finally, the noisy digital domain is used for all the digital core of the ADC, which starts with the synchronization logic and ends with the 8-bit digital output buffer.

The analog and mixed-signal domains employ bypass capacitors to help on the stabilization of the voltages to impulsive currents drained by the respective loads. Furthermore, due to pins restriction, the analog and mixed-signal power and ground voltages are ohmically connected together in the I/O ring. Hence, they are separated only up to the

I/O ring.

The top layout view of the designed ADC is shown in Fig. 6.33, and the corresponding floorplan appears in Fig. 6.34. The ADC core occupies an area of about 990 μm$\times$365 μm, most of it occupied by the analog/mixed-signal core, of which the OTAs layout takes most of the silicon space.

As indicated in the floorplan of Fig. 6.34, there is a vertical symmetry axis which is strictly observed in the layout of the two time-interleaved channels: one channel is laid out above this symmetry axis and the other below it, with OTAs laid out in the middle of the channels. Considering the channel layout of one of the pipeline stages, closer to the shared OTA (most sensitive circuit) is laid out the related SC networks, and then more distant are the latched comparators, with the associated encoding logic, and the local clock buffer.

The clock distribution tree is laid out in a C-like structure at the outer sides of the analog/mixed-signal core. Even thought the tree layout is made fully symmetrical, since the corresponding buffers of the two channels are separated by a significant distance (about 300 μm), this C-like arrangement makes these buffers prone to significant process mismatches. Together with the mismatch of the local clock buffers, which are also separated more or less by the same distance, these process mismatches originate timing mismatch in the clock phases responsible for controlling the sampling switches in the THA. As discussed previously, this timing mismatch is one of the main nonidealities in a high speed time-interleaved ADC, which compromise the performance with the introduction of spurious tones.

A possible solution would be to lay out the clock distribution tree in the middle of the two channels (with very good matching), but that approach would entail other shortcomings as well. For example, it could potentially couple noise to the sensitive underneath OTAs, which are also laid out in the middle of the channels. Furthermore, in the designed layout, the analog power and ground lines run above the OTAs layout (using low resistance top layers metal). Hence, to lay out the clock distribution tree there, these lines should be separated. Also, to avoid coupling to the OTAs and to these analog lines, appropriate shielding should be used.

The digital core circuitry is conveniently arranged adjacent the back-end pipeline stages, since, as mentioned before, these stages do not need the stringent performance required in the front-end stages.

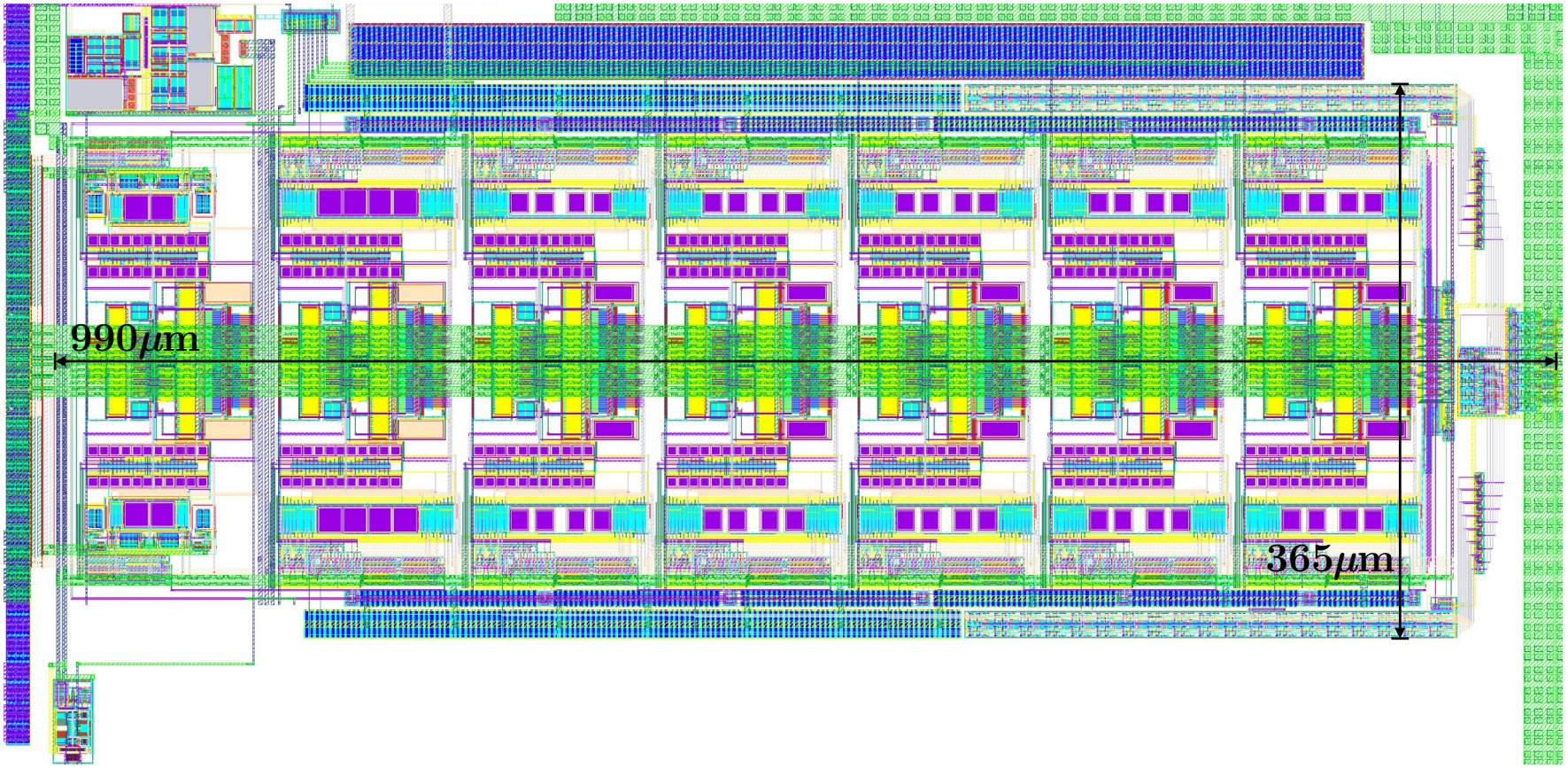

Fig. 6.33: Layout of the 8-bit two-channel time-interleaved pipelined ADC. The ADC core occupies an area of 990 μm $\times$ 365 μm.

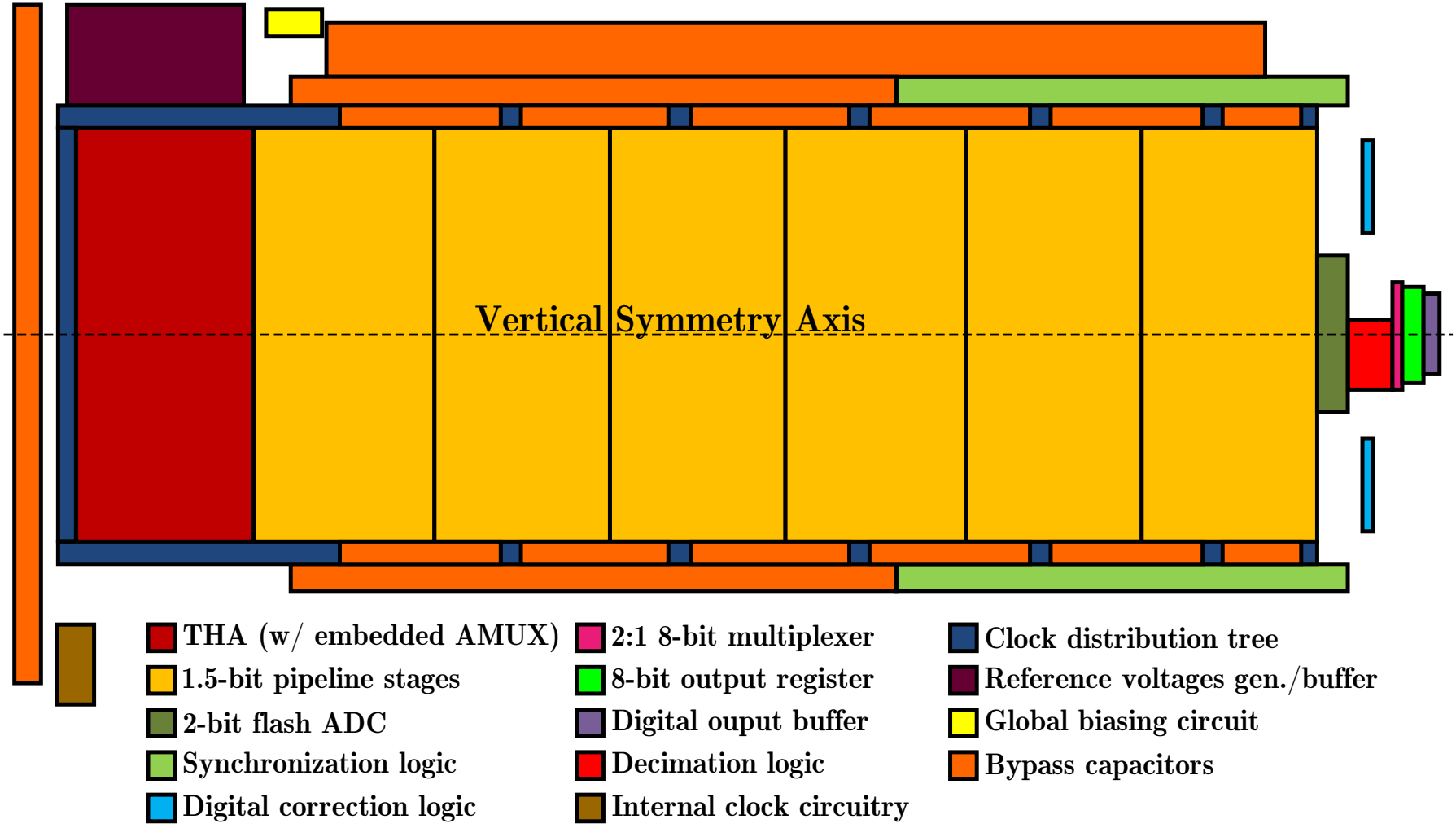

Fig. 6.34: Floorplan of the 8-bit two-channel time-interleaved pipelined ADC.

6.3.2 Interfacing Issues

Previous, in Sec. 6.2.7, we already discussed some interfacing circuits required to integrate the proposed BIST architecture with the designed ADC (DUT). In this section, we discuss specific interfacing issues in the track-and-hold amplifier and in the internal clock circuitry, which are also required to successfully interface the BIST scheme with the designed DUT.

With regard to the THA, the interfacing issues involve the use of additional switches and some basic logic elements, as highlighted in red in Fig. 6.35. Particularly, each channel requires two extra bootstrapped switches [79], four local CMOS AND gates (one per each bootstrapped switch), and one CMOS inverter (which generates $\overline{inbisten}$).

With the above small and straightforward changes, the THA operates as follows. When *inbisten* is logic low, the THA samples v_{IP} and v_{IN} provided externally, since the other bootstrapped switches are disabled (i.e., in high impedance mode). When *inbisten* is logic high, the bootstrapped switches associated with v_{IPBIST} and v_{INBIST} are enabled and, conversely, the signal provided internally by PLL IN is sampled.

In fact, this type of analog multiplexer (AMUX) can be efficiently implemented in any SC network, which are very common in ADC designs.

With respect to the internal clock circuitry, only an additional digital multiplexer (MUX) is needed, as shown in red in Fig. 6.36. Then, according to the state of *ckbisten*, the MUX output is *ckext*, provided externally, or *ckbist*, provided internally by PLL CK. Moreover, the internal clock circuitry also generates the reference signal for both PLLs, i.e., *ckref* signal, which pass through the reference divider before reaching the phase/frequency detectors of the PLLs.

Besides of the extra multiplexer, the internal clock circuitry is composed of a differential clock amplification circuit, a differential-to-single-ended (DIFF/SE) converter, a differential D-type flip-flop, and a two-phase non-overlapped clock generator. The amplifiers A_1 and A_2 of the amplification circuit are built with a differential pair with resistive loads. A front-end resistive network adjusts the common-mode voltage of the ac-coupled differential clock input. The DIFF/SE is built with CMOS inverters, where the back-to-back inverters (INV_3 and INV_4) work as a latch forcing one output towards V_{DD} and the other towards V_{SS}, and vice versa. These back-to-back inverters must have a drive strength weaker than INV_1 and INV_2, otherwise they could retain the latched states indefinitely. A differential D-type flip-flop [80] is used to adjust the duty cycle to be exactly 50 %, which is straightforwardly achieved by dividing the clock frequency by two. The duty-cycle-adjusted differential clock is then applied to a NOR-based two-phase non-overlapped clock generator, which generates the clock phases ph_1 and ph_2. These clock phases are distributed to the pipeline stages by means of a clock distribution tree.

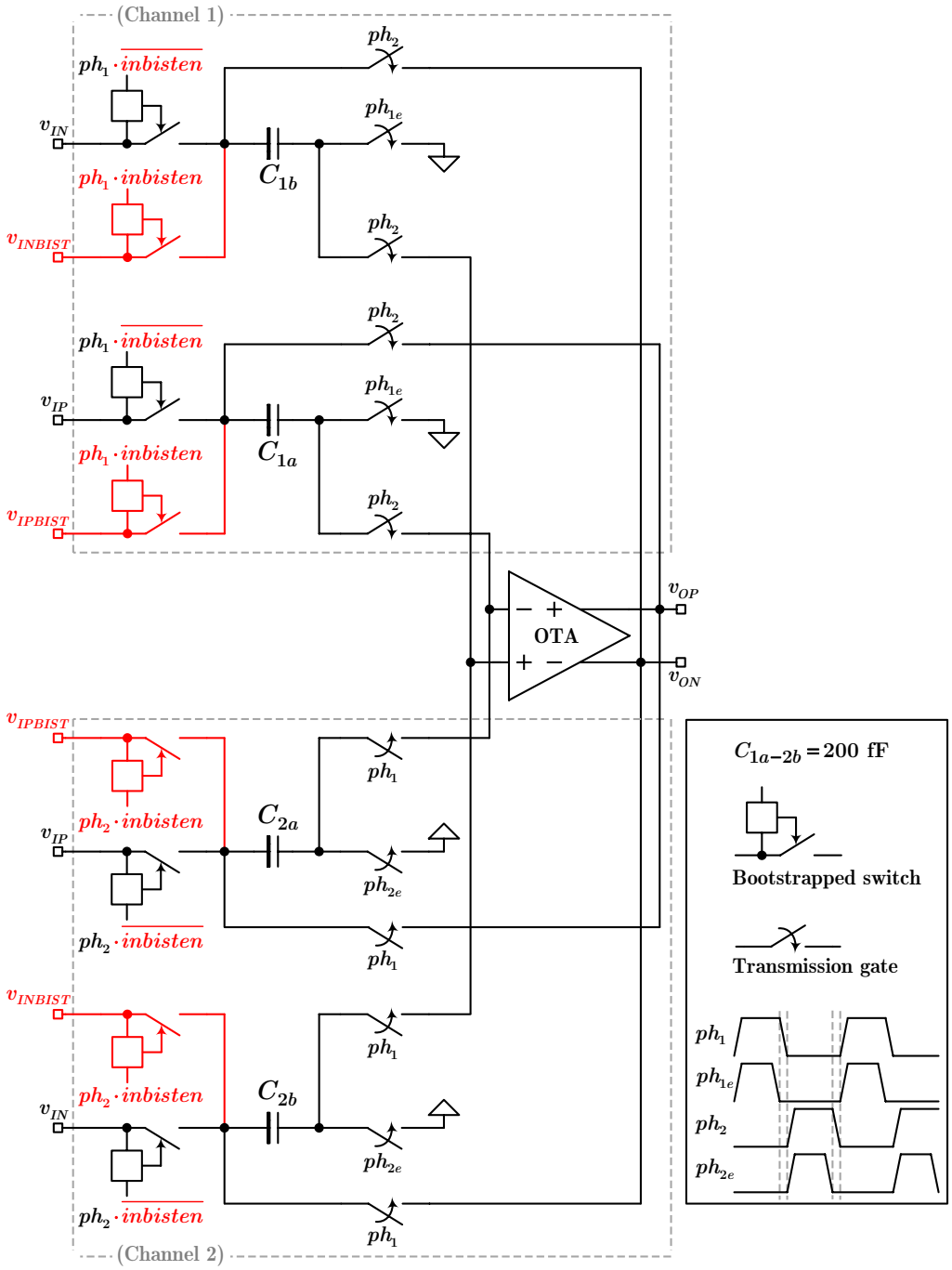

Fig. 6.35: Simplified schematic of the track-and-hold amplifier. Parts in red are the additional elements required to interface with the proposed BIST scheme.

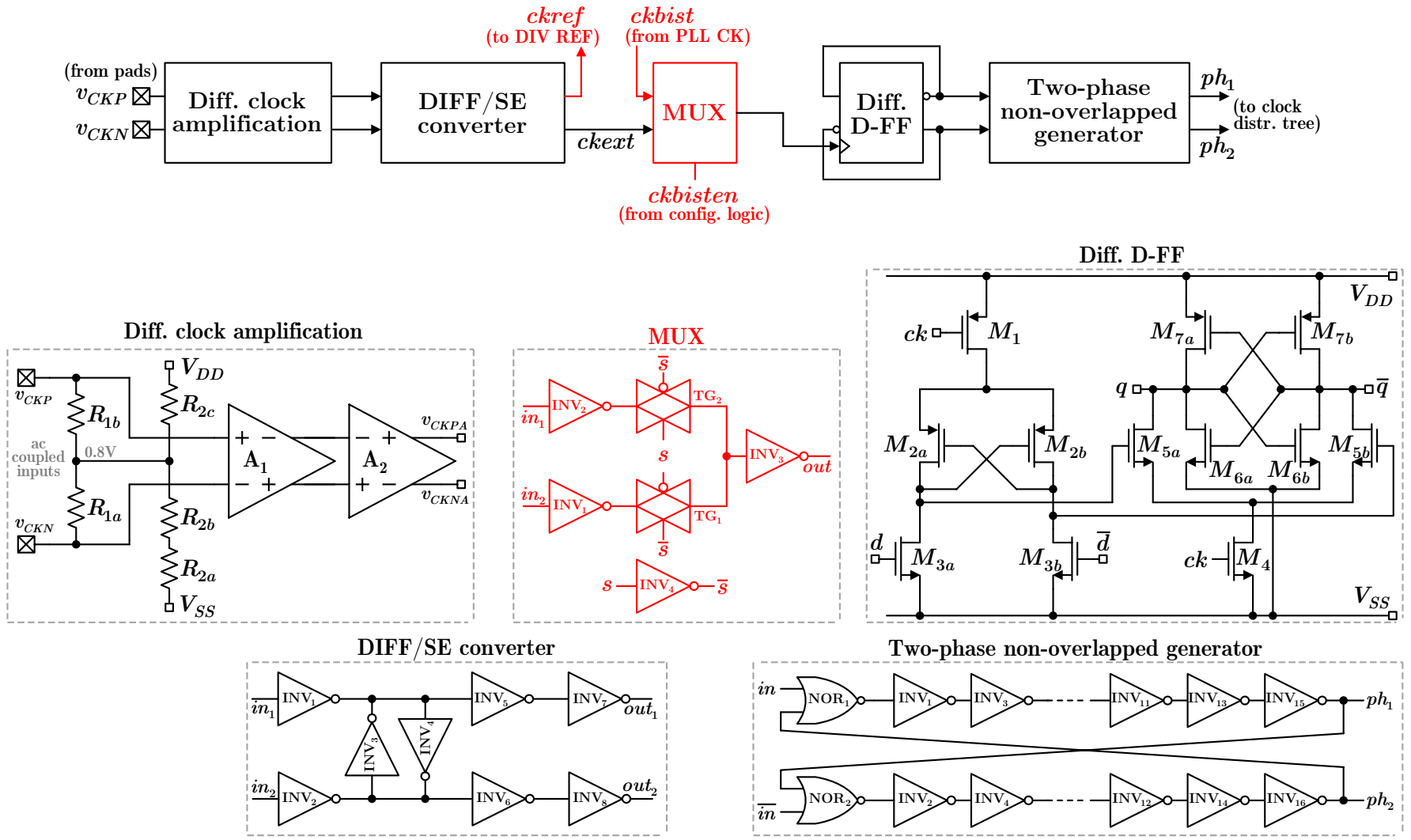

Fig. 6.36: Simplified schematic of the on-chip clock circuitry. Parts in red are the additional elements required to interface with the proposed BIST scheme.

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Chapter 7

Experimental Results

In this chapter, the main experimental results of the designed prototype are presented. First, in Sec. 7.1, we discuss the evaluation board where the designed chips are mounted and wire-bonded for characterization. In Sec. 7.2, we highlight the chip-on-board process used to mount the chips on the board. In Sec. 7.3, we present the evaluation setup employed to collect the experimental results. Then, in Sec. 7.4, we show the key experimental results and, finally, in Sec. 7.5, we discuss and compare the achieved results with other works available in the open literature.

7.1 Evaluation Board

The evaluation board of an integrated circuit involving high-frequency and/or high-resolution signals demands special care to avoid masking the actual performance of the chip. For instance, an unbalanced pair of traces carrying a high-frequency differential signal may create a significant distortion, which could mask the true distortion of the circuit under evaluation.

With the above observation in mind, in this section we present the electrical schematic and the board layout of the evaluation board, discussing the most critical aspects to take into consideration. We also discuss the technology used to manufacture the board and the bill of materials employed for board assembly.

The electrical schematic of the test board may be roughly divided in two parts: one containing input/output analog and digital signals and another containing power and biasing signals (or circuits).

The circuitry for the input/output analog and digital signals is shown in Fig. 7.1. This is composed of the analog input circuit, clock circuit, data output circuit, configuration switches, and bypass capacitors. Of these, the most critical are the analog input and clock circuits, as discussed next. The data output circuit does not pose the same challenges because the data are decimated before sending off-chip, resulting in a maximum frequency of only a few tens of MS/s.

7.1.1 On-board Analog Input Interface Circuitry

The key purpose of the analog input circuit is to provide a low noise and low distortion (sinusoidal) differential signal at the inputs *vip*/*vin* of the DUT. Besides of a differential

component, since the inputs *vip*/*vin* are dc coupled, the analog input circuit also has to provide a well-defined common-mode component.

For ensuring a low noise signal, it is of paramount importance to start with the selection of a high-quality signal generator, particularly one with a very low phase noise profile. This feature is commonly available in most RF signal generators, as further discussed in Sec. 7.3. RF signal generators, however, usually have two limitations regarding the applicability as the signal source for the analog input considered in this work: *i*) while providing state-of-the-art noise figures, the harmonic distortions of this kind of generators are as high as −30 dBc (particularly for the second and third harmonics), and *ii*) these generators have only single-ended output.

Consequently, in order to turn a RF generator into a suitable signal source for the analog input signal considered in this work, the two issues above must be properly addressed. The high harmonic distortion issue can be remedied by using passive filters, specially band-pass ones (more in Sec. 7.3), of narrow bandwidth (i.e., high order) to attenuate the harmonics till the aimed levels. This, in effect, is an affordable solution, since these passive filters are not too expensive. The single-ended output issue can be overcome in the board level using some single-ended-to-differential converter element or circuit.

With the above considerations, the analog input circuit (refer to Fig. 7.1) begins with a SMA female RF connector, $X1$. This kind of connector is suitable to connect to commercially available passive filters, which normally have 50 Ω impedance, directly or using a piece of an RF cable (also with 50 Ω impedance).

In order to ensure a well-terminated design, i.e., $Z_{\text{source}} = Z^*_{\text{load}}$, which maximizes the power transfer from the source to the load, but also affects the input signal level needed to achieve the input full-scale range of the ADC, a termination resistor, $R1$, is used. Since, as it will be discussed below, a RF transformer is used in the analog input path, and since the load impedance seen at the transformer's secondary is reflected back to its primary according to the transformer impedance ratio, $R1$ may or may not be installed on the board to ensure good termination. Furthermore, other subtle phenomena, like transformer losses, also influence a well matched 50 Ω termination, as discussed in [81].

The role of $R5$, $R18$ and $R19$, which by default are 0 Ω resistors, is to reserve a footprint space to install ferrite bead (or low-Q) inductors. These elements may be used to cancel out the capacitive reactances in the signal path to achieve a better impedance matching, if desired. Ideally, the impedance should become purely resistive. However, it is impractical to match the capacitive and inductive reactances for a broad range of frequencies. Therefore, in practice, the capacitive and inductive reactance terms are matched for the center frequency of the frequency band of interest.

The capacitor in series with the transformer primary, $C2$, acts as a dc-blocking element, since the primary winding of the transformer can carry only a small dc current safely. With significant dc currents, the transformer core may saturate resulting in a reduced transformer bandwidth or other performance degradation. An unsafe dc current into the primary of the transformer could be caused, for instance, by an offset voltage generated in the RF signal generator. Typically, a value of 0.1 μF is suitable for the blocking capacitor, since this large capacitance value originates an insignificant impedance within the bandwidth of interest of this work, i.e., from few to hundreds of MHz. In addition, since this blocking capacitor appears in series with the reflected impedance at the primary

of the transformer, it has negligible impact on the impedance matching.

The key element in the analog input circuit is the RF transformer, $T1$. This approach for driving an ADC competes, nowadays, with high-frequency differential amplifiers. Both solutions have their advantages and their drawbacks. For example, RF transformers are more suitable for larger bandwidth and lower noise. On the other hand, high-speed amplifiers allow a flatter band pass characteristic and more flexible gain adjustment. A detailed discussion on the two approaches is given in [82]. In this work, in view of the simplicity and low noise features of passive RF transformers, this solution is chosen.

The fundamental function of the RF transformer within the scope of this work is to convert a single-ended signal into a differential one. In addition, the selected transformer has a center-tap in the secondary that permits to set the dc level in its secondary outputs, which is useful when the analog input of the ADC is dc coupled.

The single-ended-to-differential conversion of the transformer is effective within the transformer bandwidth. With the Mini Circuits ADT1-1WT model, the -3 dB bandwidth is slightly less than 800 MHz, specifically from 0.4 to 800 MHz. The single-ended-to-differential conversion is also susceptible to nonlinearity, especially at high frequencies (above 100 MHz). The amplitude and phase imbalances of the transformer give an indication of this nonlinearity. Commonly, the phase imbalance dominates and it causes even-order distortions, mainly a second harmonic [82]. The above Mini Circuits transformer has very good amplitude and phase imbalances, which result in negligible distortions within the effective bandwidth.

The dc level required at the inputs *vip*/*vin* and the common-mode voltage of the ADC, which is internally buffered, is set by a resistive divider, $R7$ and $R8$, connected to the transformer's secondary center tap. In order to vary the input common-mode voltage, if desired, it is possible to replace the fixed resistor $R8$ with a variable one. A 0.1 μF capacitor, $C5$, connected to ground, creates a low cut-off frequency, low-pass filter which helps stabilize the center tap voltage.

Small-series resistors, $R22$ and $R23$, with a differentially connected capacitor, $C18$, damp out the charge injection introduced by the ADC[1]. This RC combination also forms a low-pass filter which attenuates broadband noise [82]. With values of 33 Ω and 4.7 pF, the -3 dB low-pass bandwidth is about 500 MHz.

Resistor $R29$ reserves a footprint space to install an impedance matching resistor, if required.

7.1.2 On-board Digital Input/Output Interface Circuitry

Most of the preceding discussion presented to the analog input circuit is applied to the clock circuit as well, since both circuits have several similarities. However, differently from the analog input circuit, the clock circuit does not need to provide a low distortion signal to the DUT. Furthermore, since the clock inputs are ac coupled, there is no need to set the common-mode level for the differential clock signal externally.

[1]Switched-capacitor ADCs with unbuffered analog input (as is the case of this work when the analog input is provided externally) suffer from charge injection into the sampling capacitors being reflected back onto the signal source. This, in turn, may cause settling delays for the passive filters in the drive circuit [82].

With the above consideration, the same RF transformer model is used to make the single-ended-to-differential conversion for the clock signal. In addition, since no particular common-mode level is needed in secondary outputs, the center tap of the transformer is ac coupled to ground with a 0.1 μF capacitor, $C6$.

Resistors $R16$ and $R17$ reserve footprint spaces to install current limiting resistors, if required as a protection mechanism for the diodes that follow.

A pair of back-to-back Schottky diodes, $D1$, clips the clock signal to roughly 0.8 $V_{pp,diff}$ in case of large clock swings. This preserves the fast rise and fall times of the differential clock, which helps minimize clock jitter.

Two ac-coupling capacitors, $C13$ and $C14$, of 0.1 μF each, make sure only the ac components of the differential clock signal reach the DUT.

The clock circuit is completed with resistor $R28$, which reserves a footprint space for an impedance matching resistor, if required.

With regard to the data output circuit, it receives 3.3 V CMOS digital signals from the DUT and then conveys these signals to a set of logic analyzer probe leads (more details in Sec. 7.3). As stated previously, the output data are decimated on-chip to reduce the frequency to a few tens of MS/s at maximum. Each logic analyzer probe lead has a typical input capacitance of only 1.5 pF.

The relatively low data rate in conjunction with small probe leads input capacitances minimize the transient current of the output drivers of the DUT. To help minimize this transient current even more, which is beneficial to generate less digital noise, series resistors, $R36$ to $R44$, are placed between the output drivers of the DUT and the probe leads connector, $JP18$. These series resistors interact with the input capacitance of the probe leads and the parasitic capacitance of the PCB traces creating a low-pass filter that smooths the rising and falling edges of the output digital signals [15, pp. 743, 744].

A set of configuration switches (push-buttons), $S1$ to $S6$, permits to configure the system according to distinct testing scenarios, as explained in Appendix A. The configuration circuit in the PCB is very simple because each input digital driver has an enabled pull-down resistor, leading to a normally low logic level, unless the corresponding push-button is pressed. Furthermore, each input driver has a Schmitt trigger circuit enabled, which turns the digital inputs more insensitive to noise. The robustness against noise is enhanced even more with on-chip synchronous sampling, on the clock edges opposite to those related to the output data updates (i.e., after the supply of the output drivers has partially, or completely, settled).

Many bypass capacitors, of 0.1 μF each, are used to help stabilize the supply and biasing signals. These capacitors are placed as close to the DUT as possible, in order to avoid most of the parasitic inductances of the PCB traces, and hence improving the bypassing effectiveness.

7.1.3 Power Supplies and Biasing Circuitry

The circuitry for the power and biasing signals is shown in Fig. 7.2. This is composed of a set of adjustable power supplies and a set of adjustable biasing current circuits.

Five power supply domains are available: 1.2 V analog, 1.2 V digital and 3.3 V I/O supplies for the ADC, 1.2 V analog supply for PLL CK, and 1.2 V analog supply for PLL IN.

The power supplies are built around low dropout linear regulators (model ADP1708 from Analog Devices), which provide high power supply rejection and achieve excellent line and load transient response with a small 4.7 μF ceramic output capacitor. These linear regulators are powered up by a single 4 V bench power supply (more in Sec. 7.3). The supply voltages are independently adjusted to the desired levels with a set of variable resistors, $R15$, $R27$, $R32$, $R35$, and $R47$.

If for some reason it is desirable to bypass the linear regulators and power the supply domains using external and dedicated power supplies, a set of jumpers ($JP4$, $JP10$, $JP14$, $JP15$, and $JP17$) permit to disconnect the linear regulators from the power domains.

After being regulated by the linear regulators, each supply voltage goes through a ferrite bead and a set of bypass capacitors (some of these very close to the DUT). The role of the ferrite beads is to enhance the bypass capacitors effectiveness [83], since, at high frequencies, the ferrite bead model approaches a purely resistive impedance with a significant value. For example, the ferrite beads, $L1$ to $L5$, have an impedance (almost purely resitive) of about 50 Ω at 100 MHz. At these high frequencies, the bypass capacitors have a much lower impedance path, ensuring that most of the transient currents will flow through these capacitors. At low frequencies, the ferrite bead model approaches a purely inductive impedance, with a very small equivalent series resistance (as small as 15 mΩ for the ferrite beads used in this work). This low series resistance at low frequencies ensures a small IR drop across the ferrite beads.

The biasing circuits are simply a set of variable resistors ($R3$, $R9$, $R12$, and $R20$) which set the intended reference currents to the internal current mirrors. Internally, there is a global current mirror for the ADC, one for PLL CK, and another for PLL IN, hence three separate reference currents are needed. An extra biasing current, adjusted by $R20$, is needed to control the amplitude of the sinusoidal signal generated by PLL CK (in this case, it is also possible to enable a resistive divider through $JP8$ and monitor a reference voltage instead of a reference current, if desired).

To ease the adjustment of the reference currents, without employing an ammeter, a set of precision resistors ($R4$, $R10$, $R13$, and $R21$) is used. Each of these precision resistors is connected in parallel to a two-pin connector, which allows easy voltage measurement through a voltmeter. Hence, the reference currents are set by measuring the voltage across the resistors and dividing this voltage to the corresponding resistor values[2], instead of measuring the current directly.

Similarly to the supply voltage signals, all biasing signals are bypassed with a set of capacitors. Again, some of these capacitors are placed very close to the DUT.

[2]Note that the resistor values are purposely chosen to be a power of ten to turn the division straightforward.

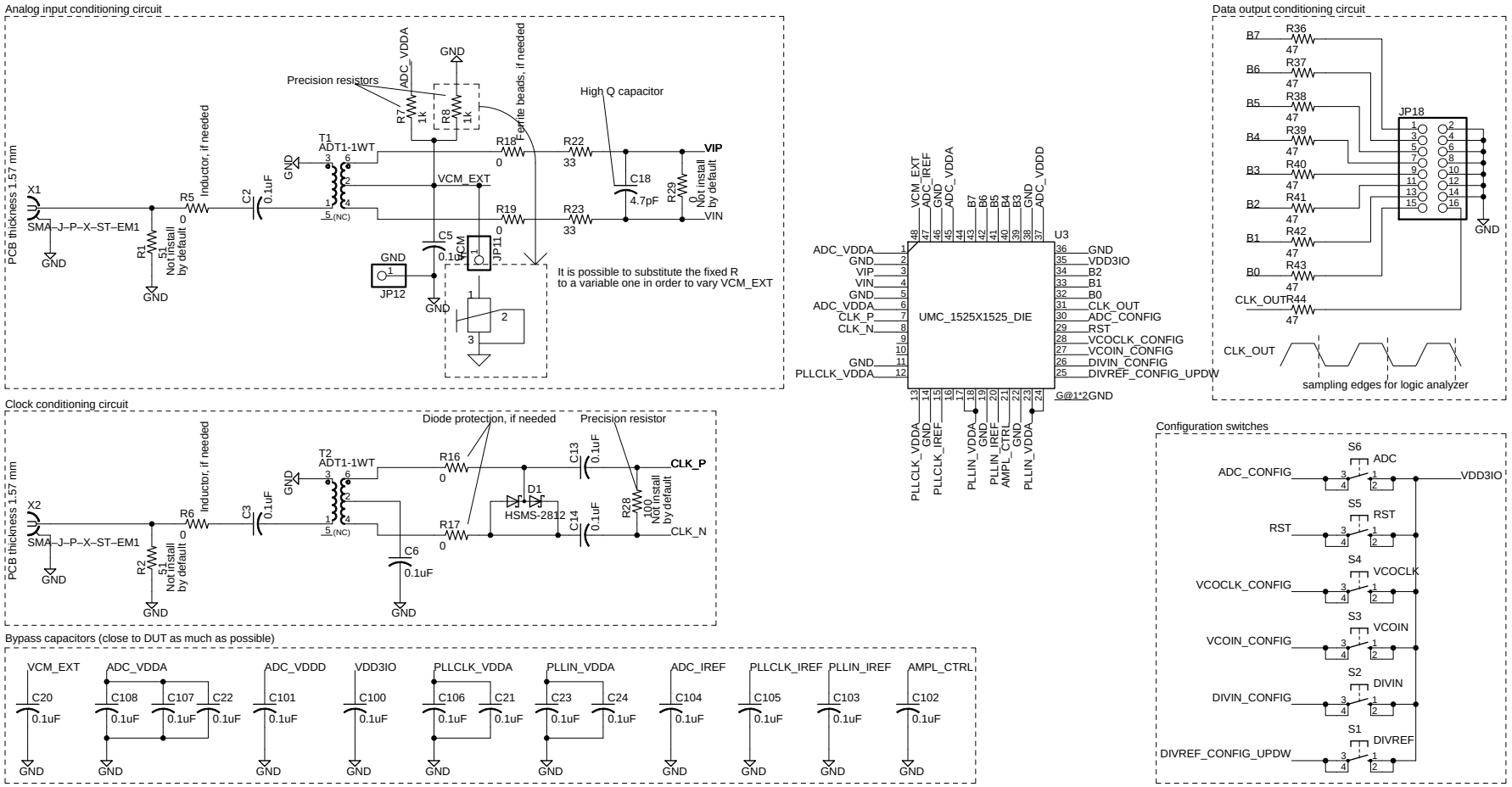


Fig. 7.1: Test board schematic: input/output analog and digital signals circuitry.

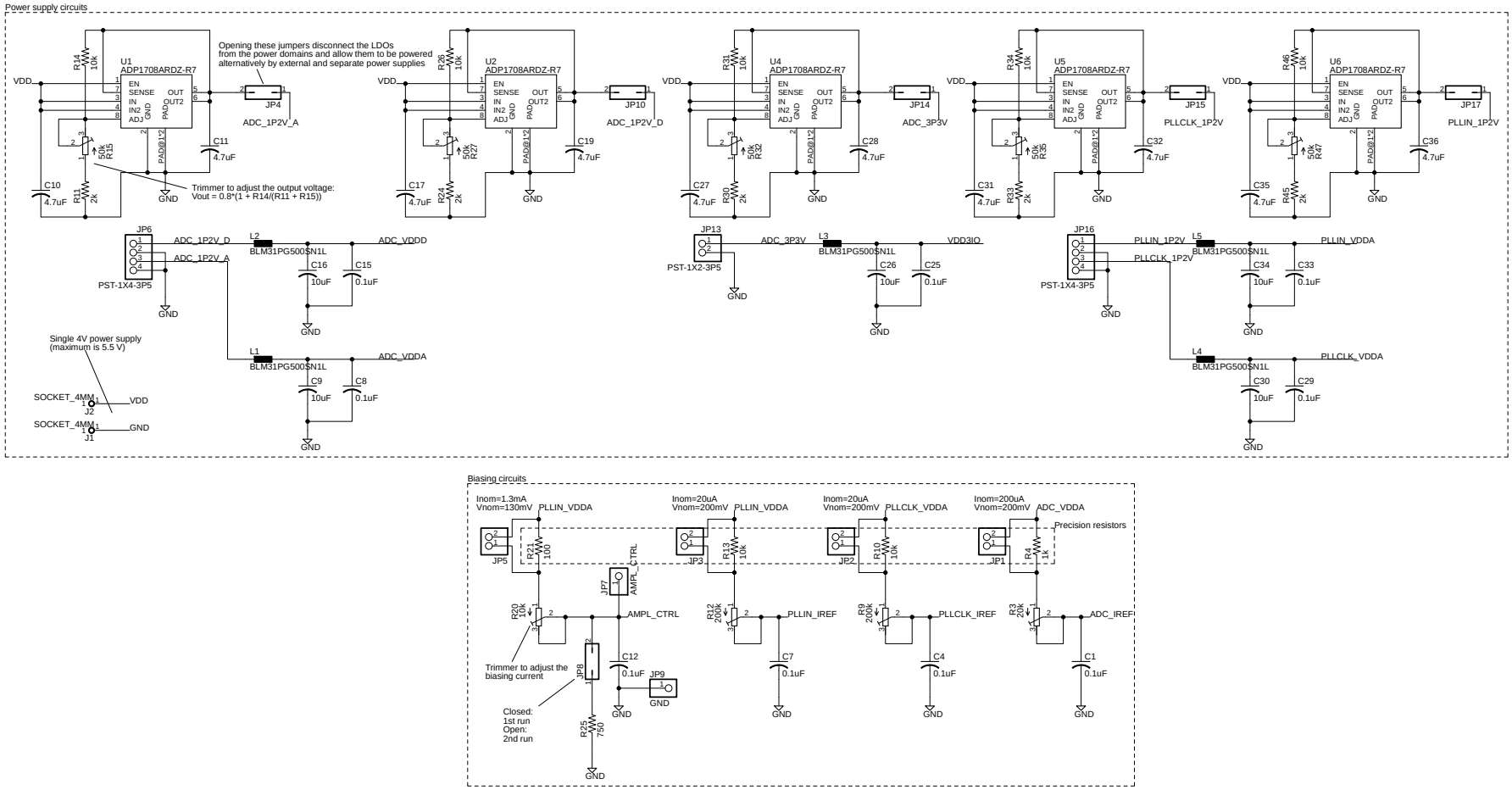


Fig. 7.2: Test board schematic: power supplies and biasing circuitry.

7.1.4 Printed Circuit Board Layout

The test board is laid out in a standard six-layer technology (from Eurocircuits company), as shown in Fig. 7.3. Top and bottom layers are used for signal routing, and the four internal layers for power and ground planes.

Instead of using separate ground planes (e.g., for analog and digital circuits), a common ground plane, on layers 2 and 5, is used, as shown in Figs. 7.3c and 7.3g. This approach simplifies the design considerably and, given that the noise-sensitive signals, like the analog input and clock, are carefully keep apart from the noisy ones, like the digital outputs, the ground plane effectiveness is maintained.

Owing to the careful arrangement of the I/O pins of the DUT, a physical separation between sensitive and noisy signals is possible. In this work, the most sensitive signals are routed in the left-half of the board, while the noisy ones are routed in the right-half.

The power plane shown in Fig. 7.3d contains the three power domains for the ADC: analog, digital, and I/O, while the power plane in Fig. 7.3h contains the power domains for PLL CK and PLL IN. It is important to note that the ground and power planes are intentionally adjacent layers, thereby creating a significant interplane capacitance. This capacitance is distributed in nature and sums up with the discrete bypass capacitors, improving the bypassing effectiveness.

Special care was taken while routing the high-frequency signals. Firstly, the analog input and clock traces are sized with approximately 50 Ω characteristic impedance. Secondly, the differential analog input and clock traces are as much symmetrical as possible. Finally, the digital outputs traces, even though less critical than the former ones, are delay-equalized with meanders ("zigzag" traces).

Preferably, the analog input and clock traces (or components) are laid out perpendicular to each other to minimize the (inductive) coupling between them. This rule is not fully observed here. However, even though most of the analog input and clock paths run in parallel, they are physically separated by a significant distance. Hence, the coupling is minimal.

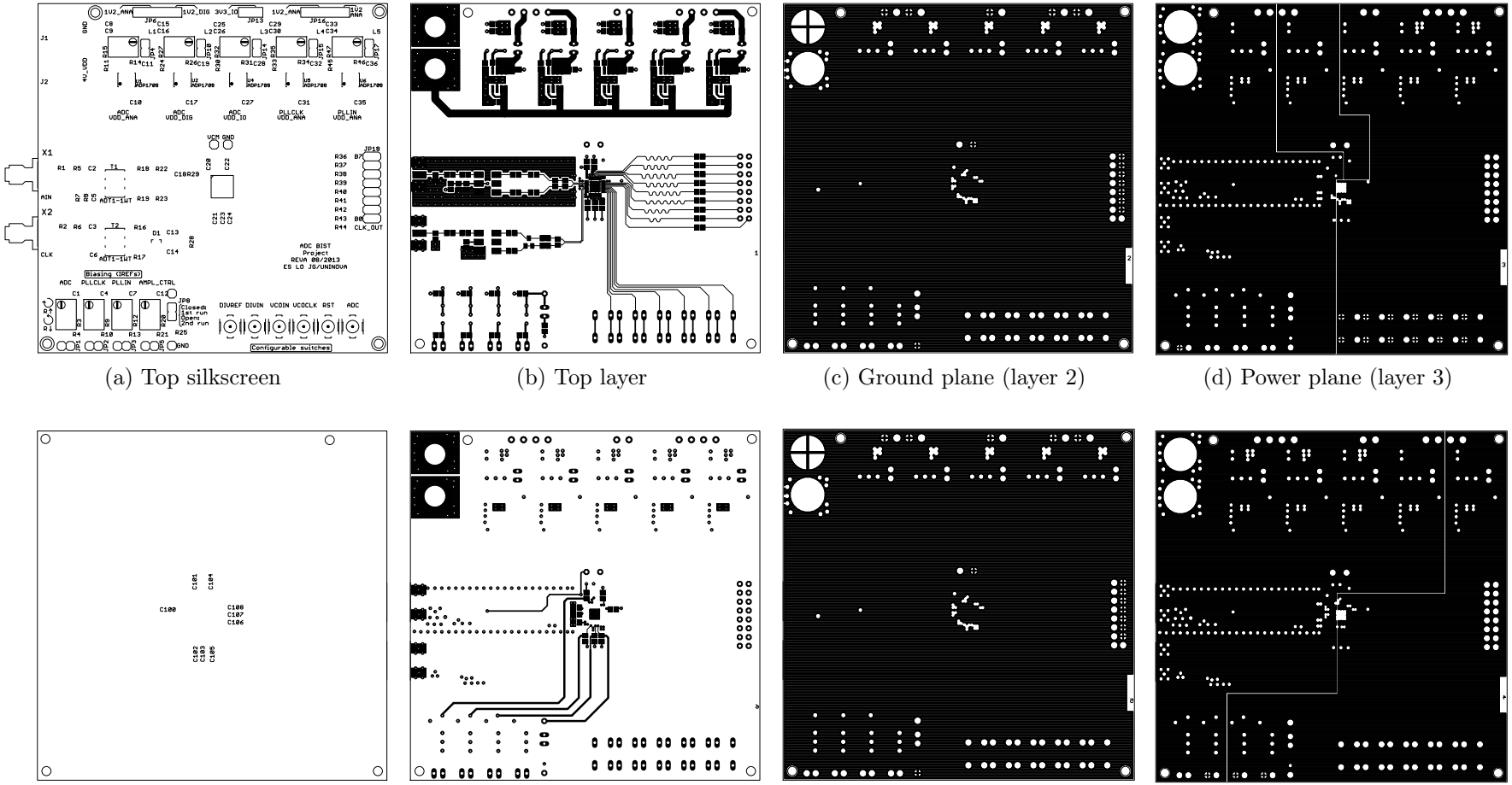
As said before, several bypass capacitors are placed as much close to the DUT as possible. This rule is clearly observed in Figs. 7.3b and 7.3f for capacitors $C20$ to $C24$ (top layer) and $C100$ to $C108$ (bottom layer).

One important aspect that directly influences the wire bonding during the chip-on-board process is the surface finish of the PCB (over the pads where the wire bonding will be executed). In this work, to minimize this influence, we adopt a chemical Nickel/Gold selective (also known as ENIG[3] after solder mask) as surface finishing. This surface finishing adds 3–6 μm of nickel onto the copper and then adds a very thin gold layer (0.06–0.10 μm) onto the top of that. This copper/nickel/gold build up makes the pads more solderable and less prone to oxidation, significantly easing the wire bonding.

The discrete components required to assemble a complete PCB are listed in Table 7.1[4]. An effort was done to use the minimal number of components and, given their types, to use the same component family/series and manufacturer. This simplifies the purchase of the components and their eventual substitution, in case they do not meet the intended quality.

[3]ENIG stands for Electroless Nickel Immersion Gold.

[4]These components are easily acquired in any major distributor like Digi-Key, Farnell, etc.



(a) Top silkscreen (b) Top layer (c) Ground plane (layer 2) (d) Power plane (layer 3)

(e) Bottom silkscreen (f) Bottom layer (g) Ground plane (layer 5) (h) Power plane (layer 4)

Fig. 7.3: Test board layout. PCB has six layers and actual dimension of 10 cm by 10 cm.

Table 7.1: Bill of materials.

Qty	Parts	Description	Value	Mfg	Mfg Part Number
6	S1, S2, S3, S4, S5, S6	SWITCH TACTILE SPST-NO 0.05A 24V	B3F-1000	Omron Electronics	B3F-1000
5	U1, U2, U4, U5, U6	IC REG LDO ADJ 1A 8SOIC	ADP1708ARDZ-R7	Analog Devices	ADP1708ARDZ-R7
2	T1, T2	RF XFMR / SURF MOUNT RoHS5	ADT1-1WT	Mini Circuits	ADT1-1WT
1	D1	DIODE SCHOTTKY GP LN 20V SOT-23	HSMS-2812	Avago Technologies	HSMS-2812-TR1G
5	L1, L2, L3, L4, L5	FERRITE CHIP 50 OHM 3500MA 1206	BLM31PG500SN1L	Murata Electronics	BLM31PG500SN1L
1	C18	CAP CER 4.7PF 250V NP0 0805	4.7pF	Murata Electronics	GQM2195C2E4R7BB12D
29	C1, C2, C3, C4, C5, C6, C7, C8, C12, C13, C14, C15, C20, C21, C22, C23, C24, C25, C29, C33, C100, C101, C102, C103, C104, C105, C106, C107, C108	CAP CER 0.1UF 16V 10% X7R 0805	0.1uF	Murata Electronics	GRM219R71C104KA01D
10	C10, C11, C17, C19, C27, C28, C31, C32, C35, C36	CAP CER 4.7UF 10V 10% X7R 0805	4.7uF	Samsung	CL21B475KPFNNNE
5	C9, C16, C26, C30, C34	CAP CER 10UF 10V 10% X7R 0805	10uF	Samsung	CL21B106KPQNFNE
6	JP4, JP8, JP10, JP14, JP15, JP17	CONN HEADER VERT SGL 2POS GOLD		3M	961102-6404-AR
4	JP1, JP2, JP3, JP5	CONN HEADER VERT SGL 2POS GOLD		3M	961102-6404-AR
4	JP7, JP9, JP11, JP12	CONN HDR BRKWY .100 VERT GOLD		TE Connectivity	5-146858-1
1	JP18	CONN HEADER VERT DUAL 16POS GOLD		3M	961216-6404-AR
1	JP13	TERM BLOCK HEADER 2POS 3.5MM BLK		Phoenix Contact	1945096
2	JP6, JP16	TERM BLOCK HEADER 4POS 3.5MM BLK		Phoenix Contact	1945119
1	R20	TRIMMER 10K OHM 0.5W PC PIN	10k	Bourns	3299W-1-103LF
1	R3	TRIMMER 20K OHM 0.5W PC PIN	20k	Bourns	3299W-1-203LF
5	R15, R27, R32, R35, R47	TRIMMER 50K OHM 0.5W PC PIN	50k	Bourns	3299W-1-503LF
2	R9, R12	TRIMMER 200K OHM 0.5W PC PIN	200k	Bourns	3299W-1-204LF
7	R5, R6, R16, R17, R18, R19, R29	RES 0.0 OHM 1/8W JUMP 0805 SMD	0	Panasonic	ERJ-6GEY0R00V
2	R22, R23	RES 33 OHM 1/8W 1% 0805 SMD	33	Panasonic	ERJ-6ENF33R0V
9	R36, R37, R38, R39, R40, R41, R42, R43, R44	RES 47 OHM 1/8W 1% 0805 SMD	47	Panasonic	ERJ-6ENF47R0V
2	R1, R2	RES 51 OHM 1/8W 1% 0805 SMD	51	Panasonic	ERJ-6ENF51R0V
2	R21, R28	RES 100 OHM 1/8W 1% 0805 SMD	100	Panasonic	ERJ-6ENF1000V
1	R25	RES 750 OHM 1/8W 1% 0805 SMD	750	Panasonic	ERJ-6ENF7500V
3	R4, R7, R8	RES 1K OHM 1/8W 1% 0805 SMD	1k	Panasonic	ERJ-6ENF1001V
5	R11, R24, R30, R33, R45	RES 2K OHM 1/8W 1% 0805 SMD	2k	Panasonic	ERJ-6ENF2001V
7	R10, R13, R14, R26, R31, R34, R46	RES 10K OHM 1/8W 1% 0805 SMD	10k	Panasonic	ERJ-6ENF1002V
2	X1, X2	CONN SMA JACK 50 OHM EDGE MNT		Samtec	SMA-J-P-H-ST-EM1
1	J1	SOCKET, 4MM, BLACK, PK5, BIL 30		Hirschmann	930166100
1	J2	SOCKET, 4MM, RED, PK5, BIL 30		Hirschmann	930166101

7.2 Chip-on-Board Assembly

The silicon chips received from the foundry (United Microelectronics Corporation, UMC) are directly mounted on the printed circuit boards using a chip-on-board technology. One of the benefits of this approach is less parasitic influences between the chip and test board interconnections, since package-related parasitics are eliminated.

This section addresses the details of the chip-on-board process followed in this work. Before that, however, a brief discussion regarding the I/O ring is given.

7.2.1 I/O Pad Ring

The I/O pad ring is shown in Fig. 7.4 and it is composed of a set of IP (Intellectual Property) cells provided by Faraday Technology Corporation. These I/O cells, besides featuring handy functions like buffering, pull down and pull up, comparison with hysteresis, etc., also have embedded ESD (ElectroStatic Discharge) protection. This last feature is of fundamental importance, specially when the chips are handled in a non-rigidly controlled ESD environment, as it is the case of the test facilities used in this work.

To ensure an effective ESD protection, the I/O ring must be continuous. This conti-

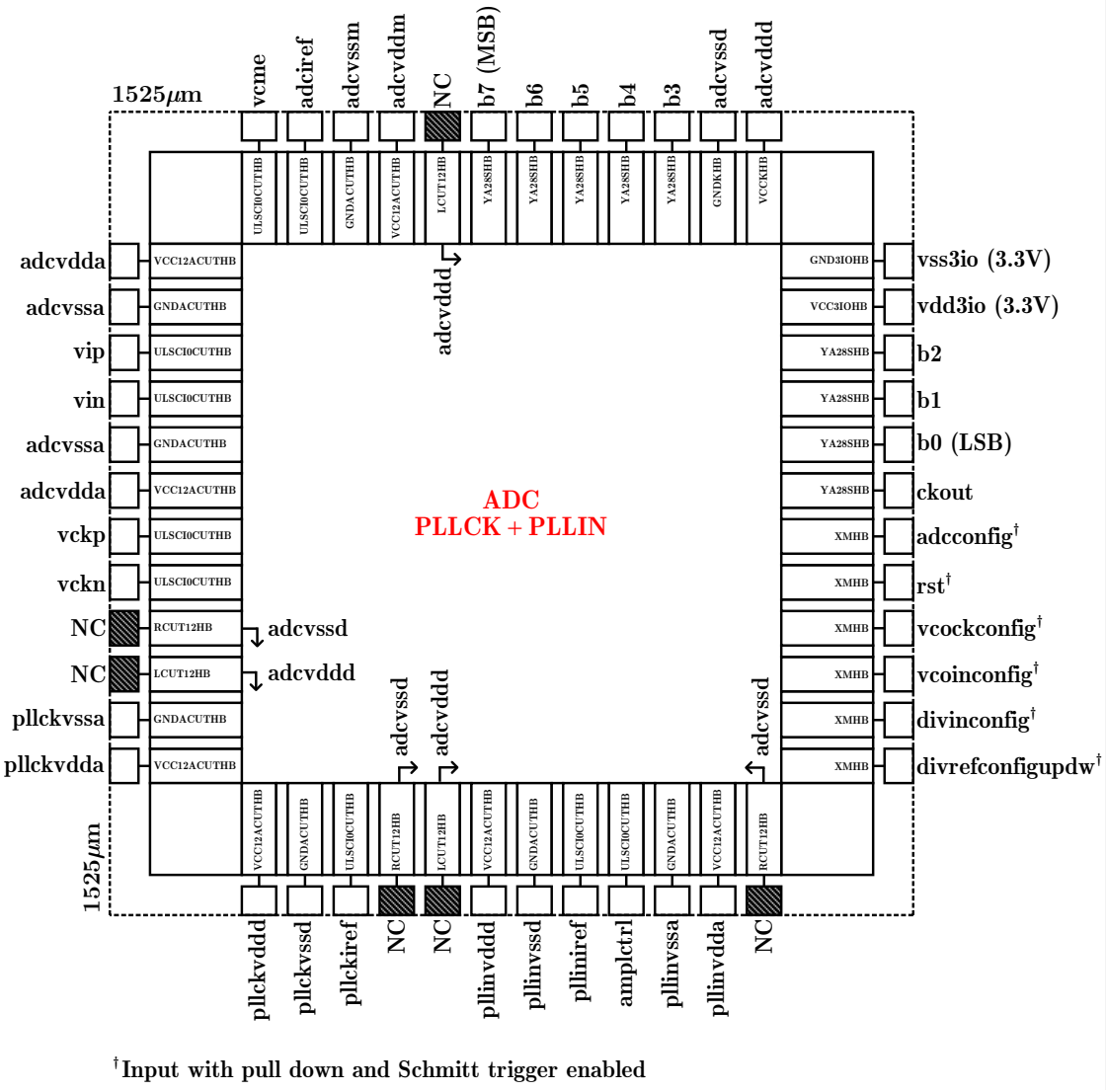


Fig. 7.4: Pads distribution around the I/O ring. Bonding pads named 'NC' are 'not connected' during wire bonding.

nuity is achieved with specific corner cells and fillers, which are placed between adjacent I/O cells. This ring continuity is also important to distribute power to the I/O buffers by means of power and ground metal rings (i.e., thick traces of low-resistance, stacked and interconnected metals).

The power and ground rings that power up the digital I/O buffers are generally very noisy. To minimize that this noise propagates to other sensitive sections of the I/O ring, where the I/O cells that convey noise-sensitive signals to or from the chip are, special cut cells can be used to cut the ring at specific places. This, in effect, separate the power supply domains.

In the I/O ring shown in Fig. 7.4, three sensitive ring sections are present: one for the sensitive signals of the ADC, one for PLL CK, and another for PLL IN. It is important

to note that, even though different power and ground names within the same sensitive ring section are present in Fig. 7.4 (e.g., *adcvdda*/*adcvddm* and *adcvssa*/*adcvssm*), they pertain to the same power/ground domain. In other words, these power supplies (e.g., *adcvdda* and *adcvddm*) and grounds (e.g., *adcvssa* and *adcvssm*) are connected together through the I/O ring.

To ensure that the introduced cut cells that break the I/O ring continuity do not compromise the ESD protection, these cells are connected to the VCCKHB/GNDKHB cells with very low resistance lines. This keeps the implemented ESD protection mechanism fully functional.

The digital I/O buffers are powered by specific power and ground cells, VCC3IOHB and GND3IOHB. The substantial power drained by these buffers, specially for the output buffers, demands a judicious selection of the maximum number of I/O buffers that can be powered by a single VCC3IOHB/GND3IOHB pair. This number is usually called I/O-to-power/ground (I/O-to-P/G) ratio. If the resulting I/O-to-P/G ratio is less than the required number of I/O buffers, then more than a single pair of VCC3IOHB/GND3IOHB should be used.

Two approaches are usually employed to determine the I/O-to-P/G ratio. One is based in the current-carrying capacity (CCC) of the VCC3IOHB/GND3IOHB cells. Another, usually more stringent (i.e., leading to a smaller I/O-to-P/G ratio), is based on the simultaneous switching output (SSO) noise[5] required to minimize timing push-out and avoid false toggles.

The current-carrying capacity approach involves, besides the determination of the current-carrying capacity of VCC3IOHB and GND3IOHB, the determination of the capacitive load of each output buffer (C_L) and the maximum signal switching frequency (f_{sw}). Then, the I/O-to-P/G ratio becomes $\text{CCC}_{\text{min}}/(C_L V_{DD} f_{\text{sw}})$[6]. As an example, if we have $\text{CCC}_{\text{min}} = 150$ mA, $C_L = 10$ pF, $V_{DD} = 3.3$ V, and $f_{\text{sw}} = 67$ MHz (a typical parameters set for this work), then the I/O-to-P/G ratio is 67. Hence, up to sixty-seven 3.3 V output buffers, each driving a load of 10 pF at 67 MHz, could be connected to a single VCC3IOHB/GND3IOHB pair.

On the other hand, the simultaneous switching output noise approach relies on timing push-out criteria, magnitude of the parasitic inductances associated with the I/O power and ground pads, drive strength of the output buffers, etc. The I/O-to-P/G ratio is then usually provided in the datasheet of the respective I/O power and ground cells. For instance, a VCC3IOHB/GND3IOHB pair, each possessing an interconnect parasitic inductance of 4 nH, can power up to 14 output buffers, each featuring a drive strength of 8 mA and fast slewing option, while ensuring a SSO push-out criterion of 30 % and no false toggles.

Since only nine 3.3 V output buffers, each with 8 mA drive strength and fast slewing option, are required in this work, both I/O-to-P/G ratio definitions are fulfilled. This in turn ensures well-behaved and reliable digital output signals.

[5]The SSO noise is caused by the output buffers switching at the same time, which creates a strong transient current demand on the I/O power supplies and, consequently, a bounce on the I/O supply voltages (mainly due to the interaction with the finite inductances of the bond wires interconnecting the I/O power and ground pads to the printed circuit board).

[6]The CCCs of VCC3IOHB and GND3IOHB may be slightly different, so the minimum one, CCC_{min}, should be used in calculations.

The digital input buffers, XMHB cells in Fig. 7.4, are also sensitive to the I/O power supply and ground noise. In order to turn these buffers less sensitive to this noise, they have internal Schmitt trigger circuits enabled.

The pads are carefully distributed around the I/O ring to ensure appropriate separation of sensitive signals. Digital-related pads, less sensitive to noise, are distributed in the right and top sides of the ring. Since the top side also contains sensitive pads of the ADC, the switching activity of the digital pads are taken into account during the pads distribution. As so, the most significant bit, $b7$, which has less switching activity among the output bits, is placed adjacent to the sensitive pads. The description of each pad is given in Table 7.2.

Given the above contextualization about the I/O ring, we discuss next the details of the chip-on-board process.

7.2.2 Chip-on-Board Process

The chip-on-board assembly is divided in three steps: die attach, wire bonding, and encapsulation. In the first step, the silicon die is glued onto the PCB. Next, in the wire bonding, the metallic interconnections between the chip pads and PCB are made. Finally, an encapsulant material is deposited over chip and bond wires to prevent contamination or accidental damages.

In this work, the adhesive used for die attach is the Ablestik ABLEBOND 2025D, from Henkel. This is a thermally conductive/electrically non-conductive adhesive with silica filler. This adhesive is heat cured, can withstand with high temperatures, and has good adhesion to a variety of substrates.

After die attach, the wire bonding between the die bonding pads and the printed circuit board pads is executed with a ball bonding process using gold wire of 23.5 μm diameter. The finished wire bonding of one sample is shown in Fig. 7.5a. The maximum bond wire length, occurring on the die corners, is about 2 mm.

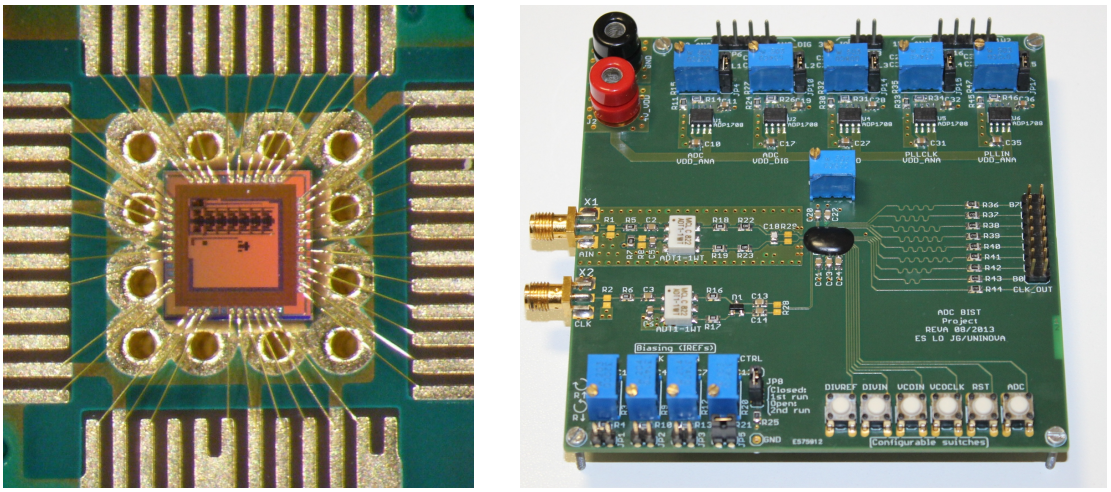
The wire bonded silicon die is encapsulated using a glob top encapsulation. The encapsulant material used for this purpose was Hysol FP4460, also from Henkel. This is a heat cured, black (and opaque), epoxy compound. The resulting glob top encapsulation for one sample appears in the center of a completely assembled PCB shown in Fig. 7.5b.

7.3 Test Setup

As summarized in Table A.1 of Appendix A, the three relevant evaluation modes available for the prototype are: *i*) ADC stimulated with external analog input and clock (this mode assesses the standalone ADC performance); *ii*) ADC stimulated with external analog input and internal clock (this mode gives the impact of PLL CK on the ADC performance); and *iii*) ADC stimulated with internal analog input and clock (this mode assesses the performance of the whole BIST system, i.e., ADC + PLL CK + PLL IN). A fourth evaluation mode, which combines the performance of the ADC and PLL IN also exists, however, in this mode, the sampling frequency of the ADC is restricted to a few MHz only. Hence, this last mode is not relevant in the high-speed-testing context of this work.

Table 7.2: Description of the chip pads.

Pad name	**Description**
adcvdda	1.2 V analog supply for ADC.
adcvssa	Analog ground for ADC.
adcvddm	1.2 V mixed-signal supply for ADC. Connected to *adcvdda* in the I/O ring.
adcvssm	Mixed-signal ground for ADC. Connected to *adcvssa* in the I/O ring.
adcvddd	1.2 V digital supply for ADC.
adcvssd	Digital ground for ADC.
vdd3io	3.3 V digital I/O supply.
vss3io	Digital I/O ground.
adciref	Reference current for ADC. Nominally 200 μA.
vcme	External common-mode voltage. Nominally 0.60 V.
vip/vin	Positive/negative analog input.
vckp/vckn	Positive/negative clock input.
$b0 \ldots b7$	Digital output bits, from LSB to MSB.
ckout	Clock output for synchronous sampling.
rst	Digital input for chip reset.
adcconfig	Digital input for ADC configuration.
vcockconfig	Digital input to configure the voltage-controlled oscillator of PLL CK.
vcoinconfig	Digital input to configure the voltage-controlled oscillator of PLL IN.
divinconfig	Digital input for PLL IN divider configuration.
divrefconfigupdw	Digital input for reference divider configuration. It also affects the up/down direction of PLL IN divider.
pllckvdda	1.2 V analog supply for PLL CK.
pllckvssa	Analog ground for PLL CK.
pllckvddd	1.2 V digital supply for PLL CK. Connected to *pllckvdda* in the I/O ring.
pllckvssd	Digital ground for PLL CK. Connected to *pllckvssa* in the I/O ring.
pllckiref	Reference current for PLL CK. Nominally 20 μA.
pllinvdda	1.2 V analog supply for PLL IN.
pllinvssa	Analog ground for PLL IN.
pllinvddd	1.2 V digital supply for PLL IN. Connected to *pllinvdda* in the I/O ring.
pllinvssd	Digital ground for PLL IN. Connected to *pllinvssa* in the I/O ring.
plliniref	Reference current for PLL IN. Nominally 20 μA.
amplctrl	Amplitude control for the voltage-controlled oscillator of PLL IN. Nominally 0.75 V.
NC	Do not connect.



(a) (b)

Fig. 7.5: Photograph of a wire bonded die before glob top encapsulation (a) and of a completely assembled test board (b). Die dimensions are 1525 μm $\times$ 1525 μm.

The three test modes above may be evaluated with the test setup shown in Fig. 7.6, which represents the simplified block diagram of the actual bench setup illustrated in Fig. 7.7. The setup as shown in Fig. 7.6 represents the evaluation mode where both the analog input and clock are generated externally, i.e., the most demanding in terms of test equipments resources. For other test modes, some of the test equipments are disabled or used for different purposes. For example, during the whole BIST system evaluation, the external analog input generator, Marconi 2041, is disabled, and the external clock generator, R&S SMB100A/SMB-B112, is used as an external reference clock for the phase-locked loops instead of an external clock for the ADC.

In the test setup, the evaluation board is power up with a single programmable power supply, Tektronix PS2521G (not shown in Fig. 7.6 for simplicity), which delivers 4 V to the adjustable voltage regulators on the evaluation board. The output voltages of these voltage regulators are adjusted on-board to the desired levels with variable resistors. Another set of on-board variable resistors is used to adjust the reference biasing currents.

The high-quality (i.e., very low phase noise) external analog input, needed in test modes *i*) and *ii*) mentioned above, is provided by an RF signal generator, Marconi Instruments 2041. In order to remove the harmonics of the generated signal (intrinsic to this kind of generator), the analog input is band-pass or low-pass filtered before being applied to the test board. In this work, the following Mini-Circuits passive filters were used: SBP-10.7, SLP-100+, SLP-250+, SLP-550+, and SLP-750+.

The external clock signal, both for ADC clocking or for the reference clock of the PLLs, is provided by another RF signal generator, Rohde & Schwarz SMB100A/SMB-B112. This generator also has an outstanding phase noise profile. For instance, the integrated rms jitter in the bandwidth of 100 Hz to 2 GHz at 1 GHz is merely 210 fs.

When used simultaneously, both RF signal generators are synchronized. Thus, the phase noise of both signal generators is correlated within the bandwidth of their reference PLLs (usually in the range of a few Hz up to 100 Hz) and, as a result, this phase noise does not contribute to the measurements.

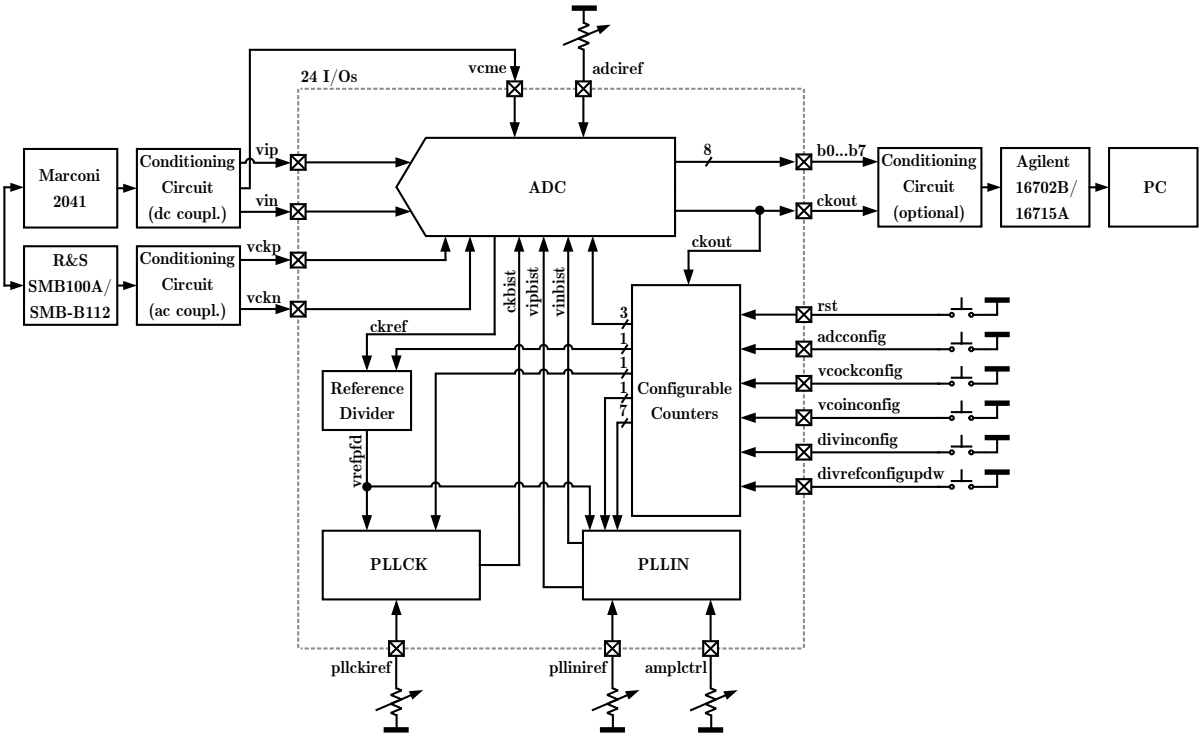


Fig. 7.6: Test setup. Power supplies and grounds are omitted for simplicity.

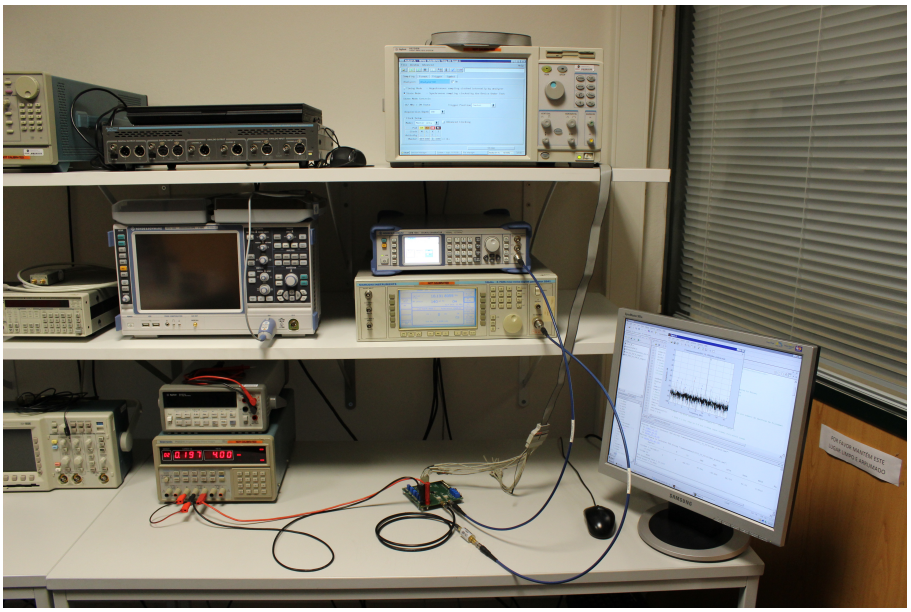


Fig. 7.7: Photograph of the actual test setup.

The ADC output data are captured with a logic analyzer, Agilent 16702B/16715A, which uses a flying lead probe with 17 channels (16 data + 1 clock). Each channel has an input capacitance as low as 1.5 pF. The captured data are then remotely transferred to a personal computer and processed in MATLAB.

A set of on-board push-button switches allows the configuration of the system and the selection of the desired test mode, as thoroughly explained in Appendix A.

7.4 Measurement Results

In this section, the key experimental results are presented. First, the standalone performance of the ADC, where both the analog input and the clock are provided externally, is presented. Next, we show the performance of the ADC when PLL CK is enabled, i.e., when the analog input signal is provided externally and the clock signal is provided internally, on-chip. Following that, the whole ADC BIST performance is presented, where the analog input and the clock are both generated internally by PLL IN and PLL CK, respectively. Finally, some complementary measurements are provided.

7.4.1 DUT with External Analog Input and Clock

In this first evaluation scenario, we concentrate on the standalone performance of the ADC, where the converter is stimulated with external analog input and clock. This evaluation gives a baseline performance which can then be contrasted with the other evaluation scenarios, where the analog input and/or clock are generated on-chip.

The results are presented in terms of the performance metrics discussed in Sec. 2.3, specifically SINAD, SNR, THD, SFDR, and ENOB. Additionally, since the ADC topology under consideration is based on a time-interleaving (TI) array, it is also interesting to analyze in separate the spurious tones caused by time-interleaving. For a two-channel TI array, spurious tones appear at dc, $f_s/2$, and $f_s/2 - f_{\text{in}}$. The former two are due to offset mismatches and, since they are very small and appear at unimportant parts of the spectrum[7], they are not taken into consideration here. On the other hand, the spur appearing at $f_s/2 - f_{\text{in}}$ and caused by timing and gain mismatches is carefully considered.

We can write the relative magnitude of the time-interleaving spur at $f_s/2 - f_{\text{in}}$, in logarithmic scale, using this equation

$$\text{TI} = 20\log_{10}\left(\frac{\text{rms TI spur}}{\text{rms signal}}\right) \text{ [dB]} \tag{7.1}$$

If we remove the TI spur of Eq. (7.1) from the SNR, we get a redefined metric called SNR_{woTI} (the suffix "woTI" clearly emphasizes that the TI spur was subtracted). Then, the SINAD can be rewritten as

$$\text{SINAD} = -10\log_{10}\left(10^{\frac{-\text{SNR}_{\text{woTI}}}{10}} + 10^{\frac{\text{THD}}{10}} + 10^{\frac{\text{TI}}{10}}\right) \text{ [dB]} \tag{7.2}$$

[7]For example, the dc component of the spectrum does not influence any of the metrics used throughout this section. Hence, it is, in any case, irrelevant in this context.

which is a decomposition in terms of TI spur, harmonic distortions, and all other noise sources. From Eq. (7.2), we can easily compute $\text{SINAD}_{\text{woTI}}$ by removing the last term, i.e.,

$$\text{SINAD}_{\text{woTI}} = -10\log_{10}\left(10^{\frac{-\text{SNR}_{\text{woTI}}}{10}} + 10^{\frac{\text{THD}}{10}}\right) \text{ [dB]} \tag{7.3}$$

With the definitions above, we can determine wether the SINAD (or ENOB) is being limited by the timing/gain time-interleaving spur, by the harmonic distortions or by the remaining sources of noise (quantization noise, jitter, etc.).

Otherwise stated differently, the THD values presented account up to the 13^{th} harmonic. Furthermore, the even harmonics are insignificant with respect to the odd ones to due the use of differential signaling and very symmetrical and careful layouts.

All results presented are derived from coherent spectra and no averaging is applied. Although an averaged spectrum improves the accuracy of the measurement (as explained in Sec. 2.3.1), it demands much more samples. And, since in the built-in self-test scenario we aim to reduce the number of samples, which is beneficial in the point of view of processing resources and time devoted to compute the spectrum, we avoid averaging to keep consistency throughout the reported results.

The measured SINAD, SNR, THD, TI spur, and ENOB versus sampling frequency for three distinct and randomly selected die samples are shown in Figs. 7.8 and 7.9. In Fig. 7.8, despite for the TI spur curves, the remaining performance curves agree very well among the three evaluated samples. The discrepancy among TI spur curves originates from gain/timing inter-channel mismatches of the ADC that vary from die-to-die[8]. Sample 3 has the worst inter-channel mismatch (i.e., the highest TI spur values), while Sample 2 has the best inter-channel matching.

With a full-scale, relatively low-frequency analog input tone, the SINAD of the ADC keeps flat up to about 500 MS/s. For higher sampling frequencies, the SINAD starts to drop quickly. The same holds for the ENOB curves shown in Fig. 7.9, which present an ENOB of about 7 bits up to 500 MS/s, i.e., roughly one bit lower than the designed resolution of the ADC.

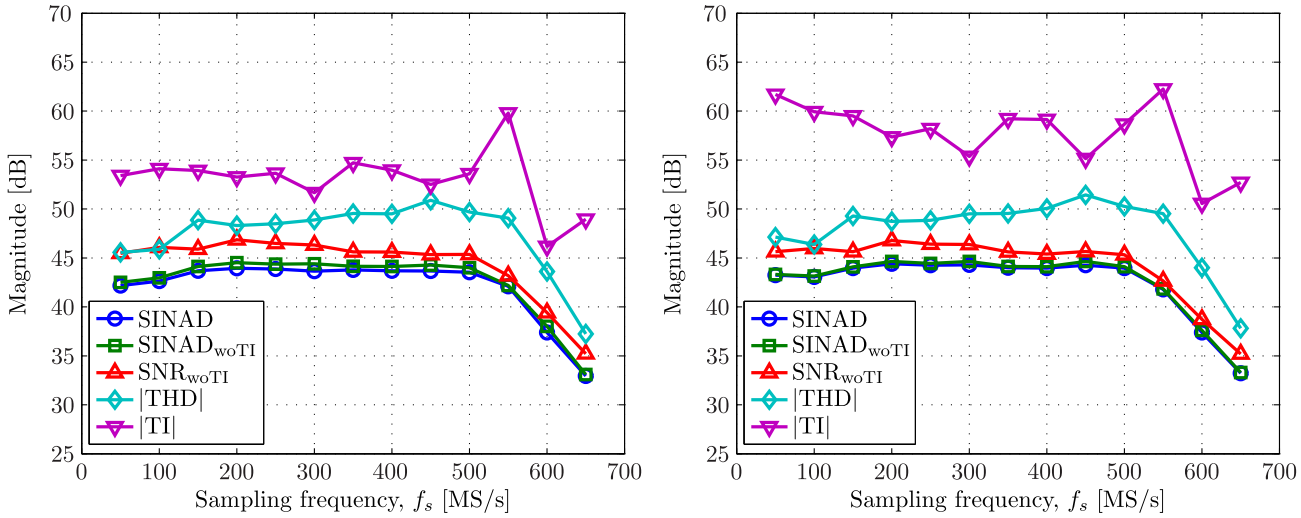
It is possible to observe only a slightly difference between the ENOB and $\text{ENOB}_{\text{woTI}}$ curves in Fig. 7.9, which shows, for this particular case, that the TI spur has small impact. Indeed, considering that the TI spur is dominated by the timing mismatch (as it is in this work), its effect is minimal when the analog input frequency is low. As soon as the analog input frequency starts to increase, the TI spur worsens.

The measured SINAD, SNR, THD, TI spur, and ENOB versus analog input frequency for the same three samples are shown in Figs. 7.10 and 7.11. For frequencies f_{in} above 250 MHz, the ADC operates in sub-sampling.

In Fig. 7.10, we note that ignoring the TI spur impact the remaining curves agree very well (compare $\text{SINAD}_{\text{woTI}}$, SNR_{woTI}, and THD curves pertaining to the three samples). Including the impact of the TI spur, we note that the SINAD of Sample 3 is limited by this spur at high analog input frequencies. For Samples 1 and 2, despite of the stronger contribution of the TI spur as the analog input frequency increases, this spur has negligible influence on the overall performance (i.e., SINAD and $\text{SINAD}_{\text{woTI}}$ curves are very close to each other).

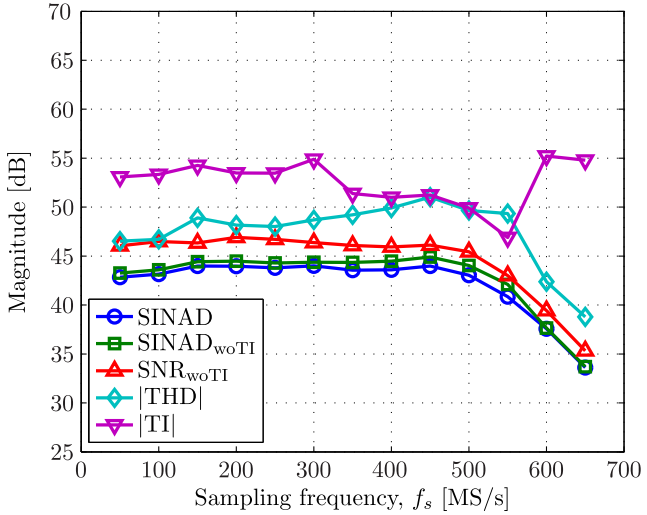
[8]Further discussion of these mismatches are outside the scope of this work, since they are a particularity of the ADC (DUT) topology used.

In Fig. 7.11, we note for Sample 3, which has the stronger inter-channel timing/gain mismatch, an ENOB versus $\text{ENOB}_{\text{woTI}}$ difference as high as 1.5-bit when $f_{\text{in}} = 600$ MHz, clearly showing the strong impact of the TI spur as the analog input frequency increases.



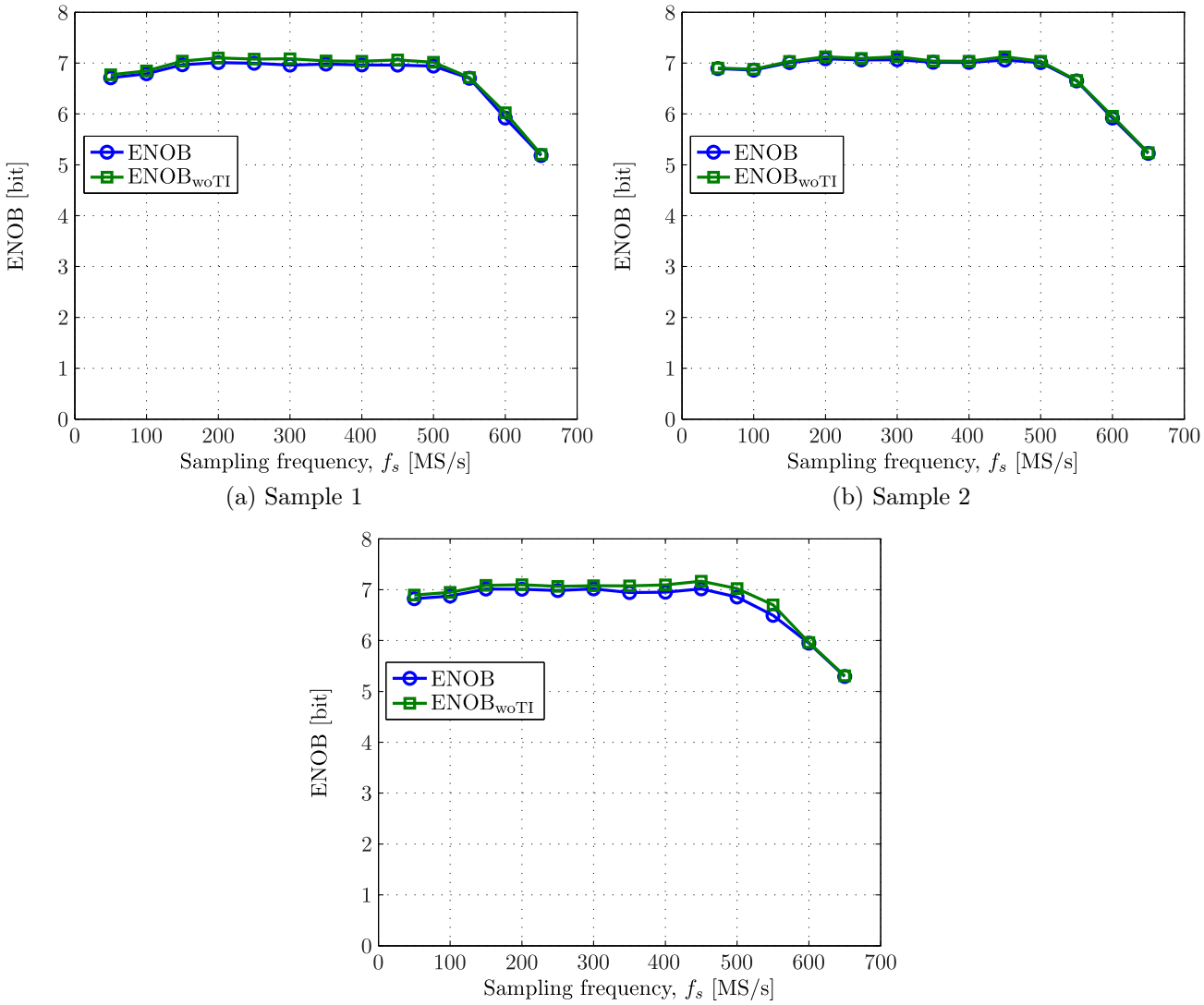
(a) Sample 1

(b) Sample 2



(c) Sample 3

Fig. 7.8: Measured SINAD, SNR, THD, and TI spur versus f_s at $f_{\text{in}} \approx 10$ MHz and $V_{\text{in}} \approx -0.1$ dBFS for three different samples. Subscript "woTI" indicates that the corresponding metric has the time-interleaving spur impact removed.

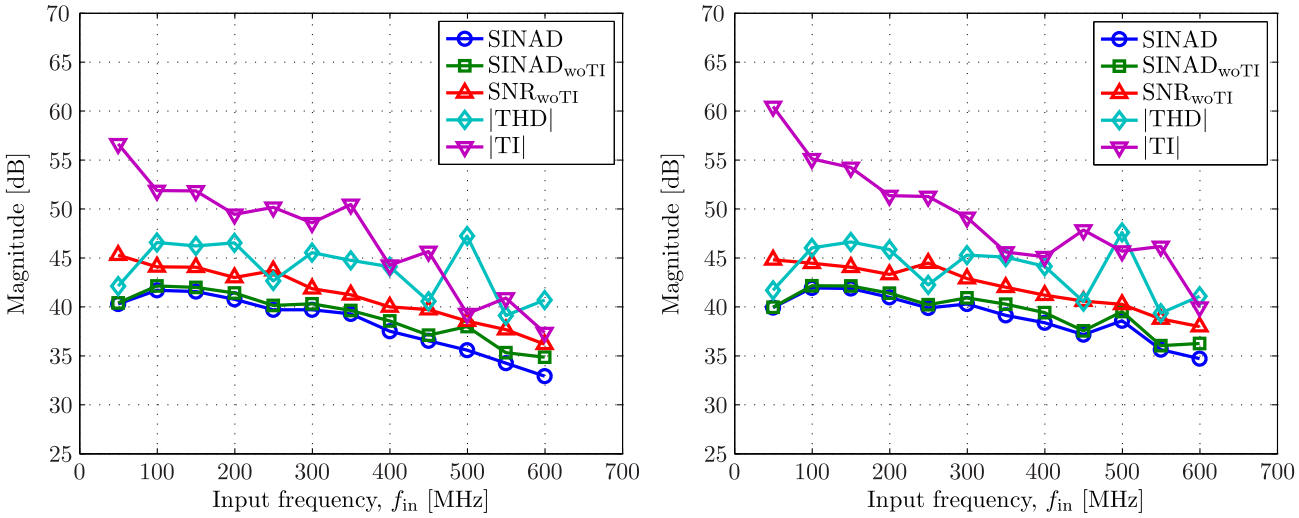


(a) Sample 1

(b) Sample 2

(c) Sample 3

Fig. 7.9: Measured ENOB versus f_s at $f_{\text{in}} \approx 10$ MHz and $V_{\text{in}} \approx -0.1$ dBFS for three different samples. Subscript "woTI" indicates that the corresponding metric has the time-interleaving spur impact removed.

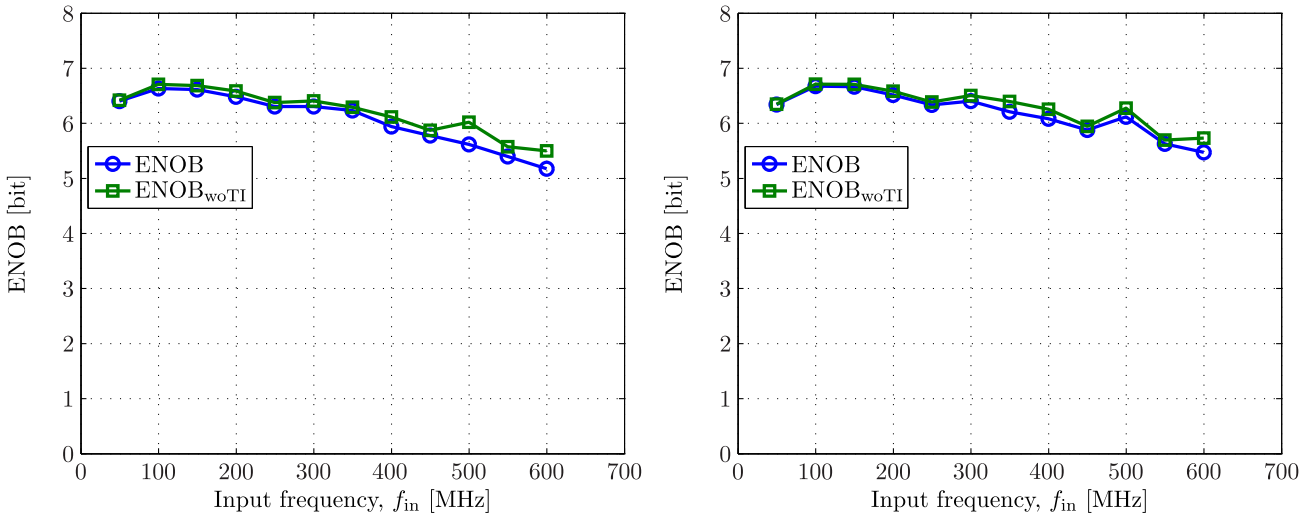


(a) Sample 1

(b) Sample 2

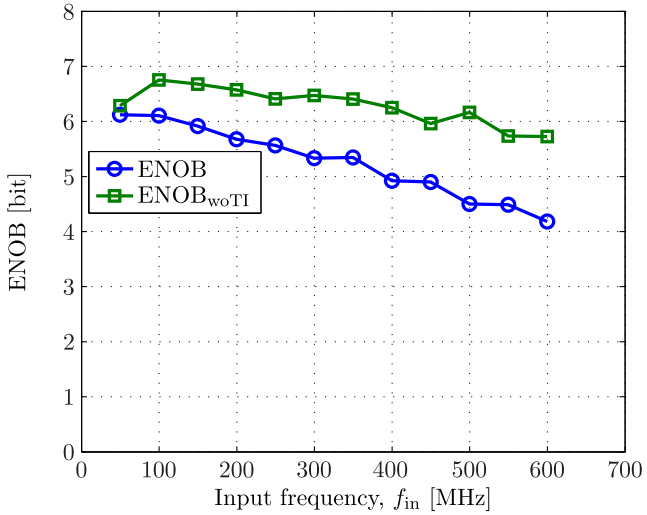
(c) Sample 3

Fig. 7.10: Measured SINAD, SNR, THD, and TI spur versus f_{in} at $f_s = 500$ MS/s and $V_{\text{in}} \approx -0.1$ dBFS for three different samples. Subscript "woTI" indicates that the corresponding metric has the time-interleaving spur impact removed.



(a) Sample 1

(b) Sample 2



(c) Sample 3

Fig. 7.11: Measured ENOB versus f_{in} at $f_s = 500$ MS/s and $V_{in} \approx -0.1$ dBFS for three different samples. Subscript "woTI" indicates that the corresponding metric has the time-interleaving spur impact removed.

7.4.2 DUT with External Analog Input and Internal Clock

In this second evaluation scenario, we report the measurement results when the analog input signal for the ADC is provided externally and the clock signal is provided internally by means of PLL CK.

As it is shown in Sec. 7.4.4, the measured slowest and fastest locking ranges of PLL CK, according to the selected discrete tuning curve of the voltage-controlled oscillator, are centered around 470 MHz and 1 GHz, respectively. Since the performance of the ADC drops quickly as sampling frequency goes above 500 MS/s, as discussed in the previous section, the locking range around 1 GHz is not meaningful here. Consequently, the useful clock frequencies synthesized by PLL CK span approximately 30 MHz around 470 MHz (cf. Fig. 7.19).

In view of the above locking range constraint, we configure PLL CK to generate a clock signal with frequency 464.64 MS/s. This configuration involves setting an external reference frequency, f_{ref}, of 3.63 MHz, which is divided by 2 internally and then applied to the phase/frequency detector of the phase-locked loop. Given that PLL CK is an integer PLL with fixed frequency divider of 256, the generated frequency becomes $256 \times 3.63/2$ MS/s $= 464.64$ MS/s.

It is important to highlight that the selected f_{ref} (i.e., 3.63 MHz) leads to a value very close to the center frequency of the locking ranges around 470 MHz of the three measured samples (cf. Fig. 7.19). This means that even with a somehow narrow 30 MHz locking range span, there is a reasonable overlapping among the locking ranges of the measured samples. Hence, the same f_{ref} can be used throughout the samples to lock PLL CK. In practical terms, this would allow to use a single, cheap, low phase noise crystal oscillator (with a fixed frequency) on the PCB to produce the desired external reference frequency. In this work, however, f_{ref} is provided by an RF signal generator to allow flexibility in the characterization.

The output clock generated by PLL CK has deterministic spurs at $f_{\text{in}} \pm k f_{\text{refpfd}}$ ($k = 1, 2, \ldots$), where f_{refpfd} represents the reference frequency applied to the phase/frequency detector of the phase-locked loop[9]. These spurs happen because the PLL feedback loop is updated at a rate equal to f_{refpfd} when the PLL is in lock state. These periodic updates modulate the tuning voltage of the voltage-controlled oscillator and produce the so-called reference spurs, as indicated in Fig. 7.12. In this figure, only the first-order reference spurs (happening at $f_{\text{in}} \pm f_{\text{refpfd}}$) are significant. Furthermore, we denote left and right reference spurs for those occurring at $f_{\text{in}} - k f_{\text{refpfd}}$ and $f_{\text{in}} + k f_{\text{refpfd}}$, respectively[10].

Following the same reasoning behind the separation of the TI spur from the other performance metrics, we can also analyze the impact of the reference spurs in separate. The suffix "woTI&R" following a given performance metric indicates that, besides the TI spur subtraction, the first-order reference spurs are also removed. Higher-order reference spurs are not taken into account because they are usually considerably smaller than the first-order ones, so their impact is insignificant.

The measured SINAD, SNR, THD, TI spur, and ENOB versus f_{in} at $f_s = 464.64$ MS/s

[9] Do not confuse the external reference frequency, f_{ref}, with the reference frequency at the input of the phase/frequency detector, f_{refpfd}. They differ by the reference divider value.

[10] In Fig. 7.12, the first-order left (right) reference spur occurs in the right (left) side of the fundamental. This apparently incorrect labels placement is due to the spectrum folding caused by the decimation.

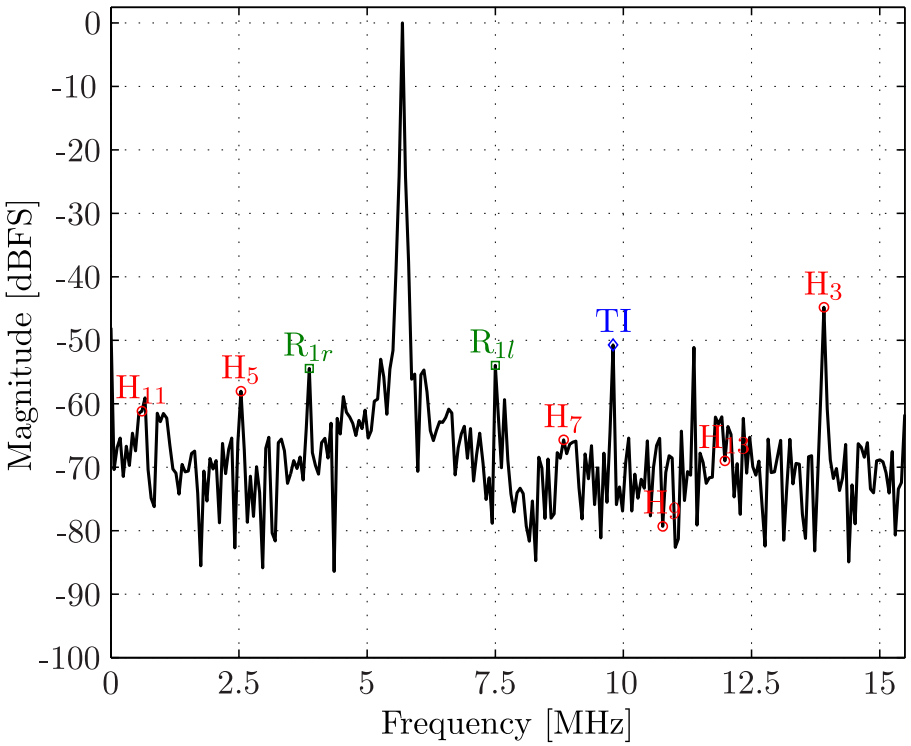


Fig. 7.12: Measured output spectrum (512 points) of Sample 1 at $f_s = 464.64$ MS/s ($= 256 \times 3.63/2$ MS/s), $f_{\text{in}} = 56.265$ MHz ($= 31 \times 3.63/2$ MHz) and $V_{\text{in}} \approx -0.1$ dBFS. The frequency axis accounts for an output data decimation of 15. Label TI represents the time-interleaving spur, H_i represents the ith harmonic, and $\text{R}_{1l,r}$ represents first-order left and right reference spurs.

and $V_{\text{in}} \approx -0.1$ dBFS for Sample 1 are shown in Fig. 7.13. The left-side graphs (Figs. 7.13a and 7.13c) represent the setup where both the analog input and clock are provided externally, whereas the right-side graphs (Figs. 7.13b and 7.13d) represent the setup where the analog input is provided externally and the clock internally. With these side-by-side graphs, we can easily observe the impact introduced by the nonidealities of the clock generated by PLL CK.

Besides of the undesirable reference spurs mentioned above, which occur at deterministic frequencies of the spectrum, the clock generated by PLL CK is also affected by random phase fluctuations, also know as time jitter. These fluctuations, in contrast with the reference spurs, are more or less equally spread all over the spectrum.

Despite of the distinct occurrences on the spectrum (deterministic vs stochastic), both the reference spurs and the phase noise manifest themselves in a stronger way as the analog input frequency increases.

By comparing Figs. 7.13a and 7.13b, we note that the greatest performance discrepancy occurs on the SNR_{woTI} metric. In Fig. 7.13a, with an external and cleaner clock, the SNR_{woTI} is approximately flat for all analog input frequencies up to the Nyquist frequency. In Fig. 7.13b, however, it is noticeable that the reference spurs and phase noise on the clock generated by PLL CK are deteriorating SNR_{woTI} considerably as the analog input frequency increases. It is also interesting to observe that the impact of the reference

spurs becomes more significant at higher input frequencies.

Given that the reference spurs occur at well-known frequencies, we can ignore them for the purpose of evaluating the actual performance of the ADC under test. In any case, we know a priori that these spurs are not introduced by the ADC, but by the clock synthesized by PLL CK. Using this argument, we can see in Fig. 7.13d that the $\text{ENOB}_{\text{woTI\&R}}$[11] is only about 1-bit worse than the baseline ENOB of Fig. 7.13c for the highest analog input frequency. In another perspective, we can say that the quality of the clock generated by PLL CK allows evaluating a 500 MS/s ADC with an ENOB upper limit of approximately 5.5-bit at the Nyquist frequency.

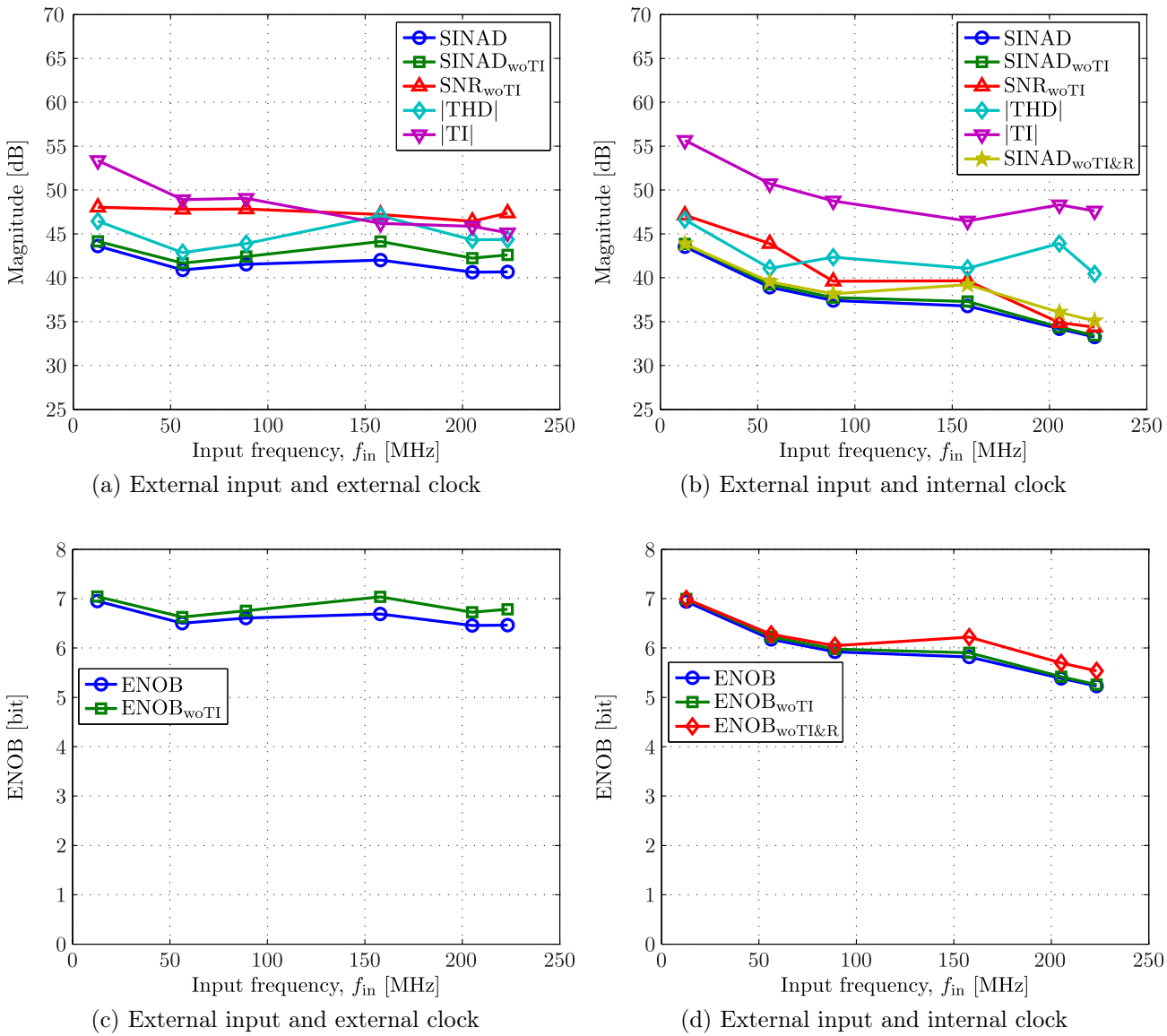
Analyzing the corresponding measurements for Samples 2 and 3, shown respectively in Figs. 7.14 and 7.15, similar conclusions may be drawn. For Sample 3, the minimum $\text{ENOB}_{\text{woTI\&R}}$ is about 5-bit (cf. Fig. 7.15d), i.e., slightly less than the other two samples.

It is also important to mention that the results presented in Figs. 7.13, 7.14, and 7.15 are derived from a 512-point FFT spectrum[12]. Furthermore, the output data sent off-chip is decimated by a factor of 15, since the digital outputs are CMOS-level signals which cannot be read at full-speed (i.e., 464.64 MS/s) due to the amount of noise produced by the output digital drivers. This means that, with decimation, the acquisition (observation) time is increased from $(512-1)\times T_s$ to $15\times(512-1)\times T_s$ and, given that slower phase noise fluctuations will influence in the sampling instants too, the impact of the phase noise on the SNR will be stronger. Said in other words, assuming an application where the ADC performance is computed on-chip at full-speed, the impact of the clock phase noise on the SNR would be weaker.

In summary, the measurements of this section show that the quality of the internally generated clock allows evaluating the performance of a Nyquist-rate ADC up to an ENOB of about 5-bit when sampling at 500 MS/s an analog input signal with $f_{\text{in}} \approx f_s/2$.

[11] The $\text{ENOB}_{\text{woTI\&R}}$ ignores both the time-interleaving and the reference spurs, but, since the reference spurs are dominant in this context, it is equivalent of ignoring only the reference spurs.

[12] The minimum ideal record length to get at least one sample from every output code in a 8-bit resolution ADC is $2^{8+2} = 1,024$ samples (cf. Eq. (2.18) in Sec. 2.3.1). Here, however, we use only 512 samples because *i*) we want to reduce the amount of samples for DSP processing and *ii*) the designed frequency ratio for coherent sampling is $f_{\text{in}}/f_s = N_p/256$ (imposed by the frequency divider value of PLL CK), hence the samples' phases ideally repeat after each adjacent set of 256 samples. Therefore, unless of nonidealities in the A/D conversion or in the sinusoidal analog input or in the clock, collecting more samples does not bring much more useful information.



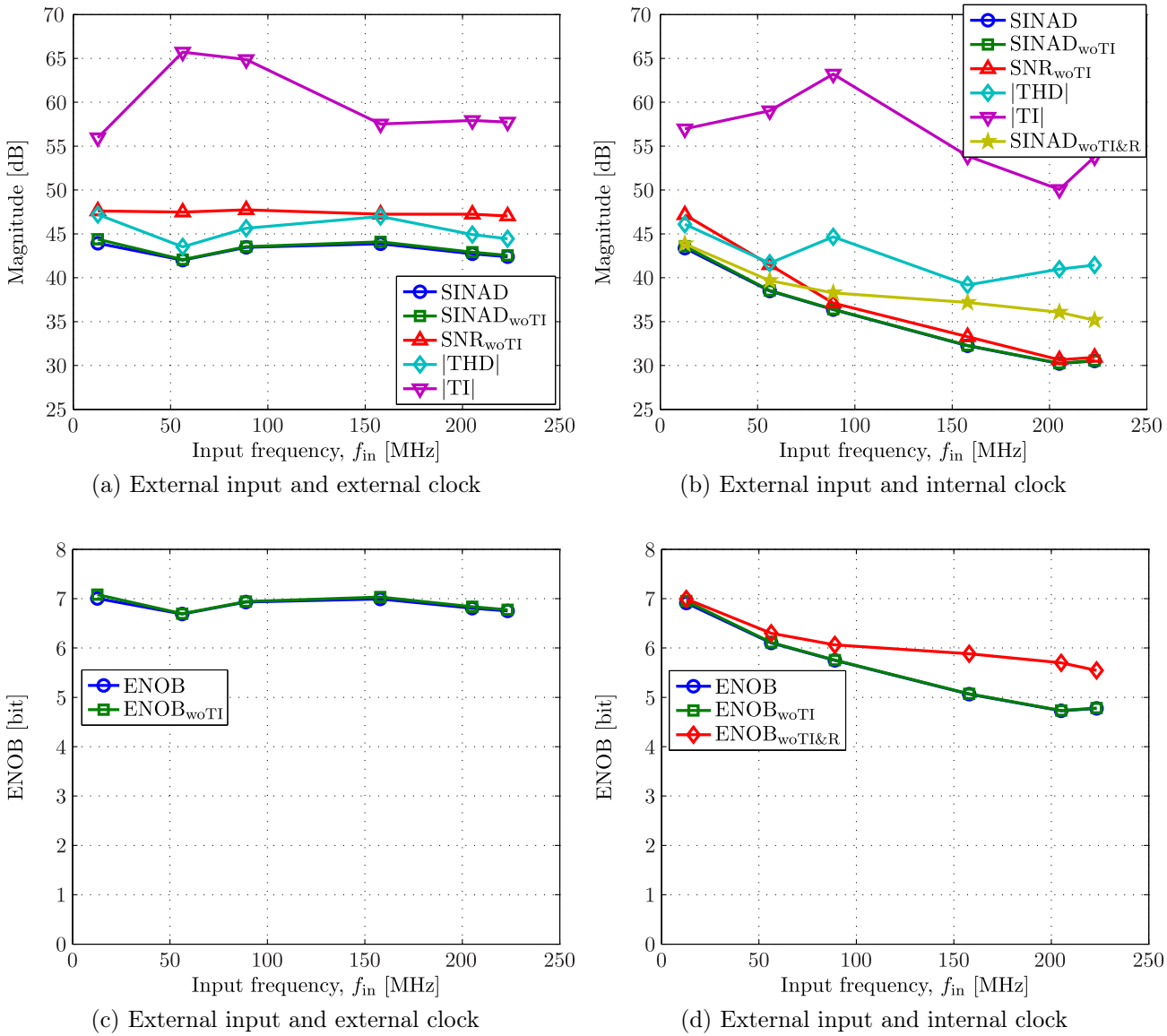
(a) External input and external clock

(b) External input and internal clock

(c) External input and external clock

(d) External input and internal clock

Fig. 7.13: Measured SINAD, SNR, THD, TI spur, and ENOB versus f_{in} at $f_s = 464.64$ MS/s ($= 256 \times 3.63/2$ MHz) and $V_{\text{in}} \approx -0.1$ dBFS for Sample 1. Subscript "woTI&R" indicates that, besides time-interleaving spur impact removed, the impact of the reference spurs is also subtracted.



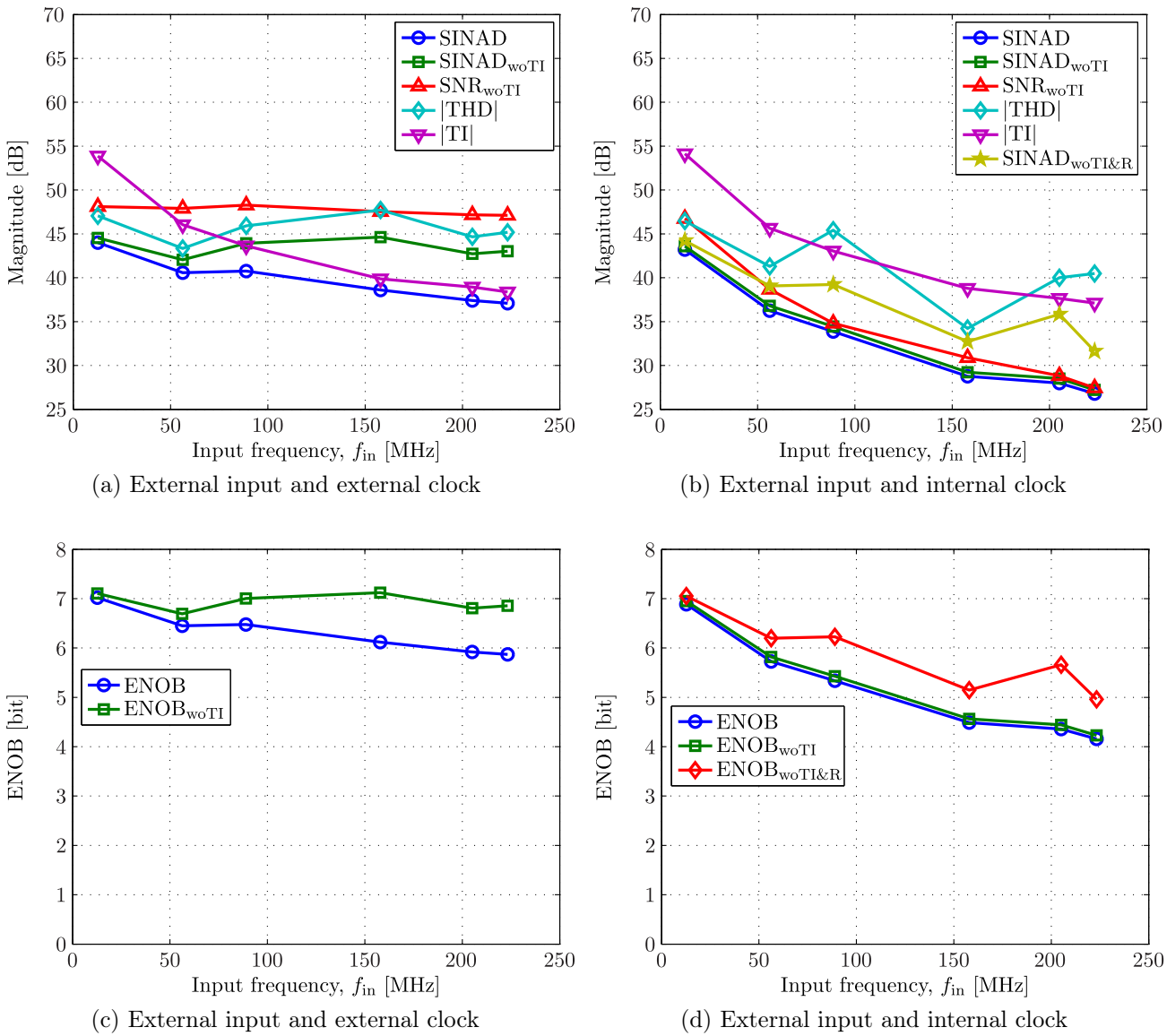
(a) External input and external clock

(b) External input and internal clock

(c) External input and external clock

(d) External input and internal clock

Fig. 7.14: Measured SINAD, SNR, THD, TI spur, and ENOB versus f_{in} at $f_s = 464.64$ MS/s ($= 256 \times 3.63/2$ MHz) and $V_{in} \approx -0.1$ dBFS for Sample 2. Subscript "woTI&R" indicates that, besides time-interleaving spur impact removed, the impact of the reference spurs is also subtracted.



(a) External input and external clock

(b) External input and internal clock

(c) External input and external clock

(d) External input and internal clock

Fig. 7.15: Measured SINAD, SNR, THD, TI spur, and ENOB versus f_{in} at $f_s = 464.64$ MS/s ($= 256 \times 3.63/2$ MHz) and $V_{in} \approx -0.1$ dBFS for Sample 3. Subscript "woTI&R" indicates that, besides time-interleaving spur impact removed, the impact of the reference spurs is also subtracted.

7.4.3 DUT with Internal Analog Input and Clock

In the last evaluation scenario, we report the measurement results when both the analog input signal and the clock signal are provided internally by means of PLL IN and PLL CK, respectively. This test mode evaluates the complete BIST system.

Similarly as it happens for the locking ranges of PLL CK, PLL IN also has two distinct locking ranges, one centered around approximately 230 MHz and another centered around 500 MHz. The center frequencies of these locking ranges are intentionally twice as slow as the respective center frequencies of the locking ranges of PLL CK (i.e., 470 MHz and 1 GHz) to enable the stimulation of the ADC with an analog input frequency very close to the Nyquist frequency which, for a high-speed Nyquist-rate ADC, is the most revealing setup (where usually the converter exhibits the worst performance).

The selection between the slowest or the fastest locking range of PLL IN is achieved by controlling the discrete tuning curve of its voltage-controlled oscillator. Although not shown in the complementary measurements of Sec. 7.4.4[13], the PLL IN locking range centered around 230 MHz spans a range of frequencies of nearly 30 MHz while the one centered at 500 MHz spans a range of about 60 MHz.

Using the same external reference frequency of the previous section, i.e., $f_{\text{ref}} = 3.63$ MHz, and setting the reference divider to divide by two, the clock frequency generated by PLL CK becomes $f_s = 256 \times 3.63/2$ MS/s $= 464.64$ MS/s. The frequency divider value of PLL IN could be any odd integer that keeps PLL IN in lock state given the reference frequency above. Here, we set the frequency divider of PLL IN to 125, and then the analog input frequency becomes $f_{\text{in}} = 125 \times 3.63/2$ MHz $= 226.875$ MHz. Note that the frequencies f_s and f_{in} are chosen to lie very close to center of their respective locking ranges, giving margin to process variations that slightly shift up or down the locking ranges from one die to another.

The amplitude of the sinusoidal signal generated by PLL IN directly influences the THD of the analog input signal provided to the ADC. This argument holds because the voltage-controlled oscillator produces stronger distortions as the oscillation amplitude increases, and also because the linear buffer that follows the VCO and drives the track-and-hold stage of the ADC gets more nonlinear as the input signal enlarges.

Since in this work the distortion of the VCO dominates and it gets more significant as the output differential amplitude of the VCO becomes larger than $V_{\text{in}} = 600$ $\text{mV}_{\text{pp,diff}}$, we set the analog input amplitude to approximately this level. This adjustment is made through the *amplctrl* pin, which internally controls the output oscillation amplitude of the VCO. Given that the input full-scale range of the ADC is nominally 800 $\text{mV}_{\text{pp,diff}}$, this level of V_{in} corresponds to -2.5 dBFS. If we were not constrained by the distortion of the VCO, we would choose a larger analog input level, e.g., -0.1 dBFS (corresponding to 790 $\text{mV}_{\text{pp,diff}}$ in this particular case), in order to exercise almost all output codes of

[13]Due to I/O pins limitation, it was not implemented an observation point in the prototype capable of reading the output frequency of PLL IN directly. Hence, differently than the case of PLL CK, where the output clock (*ckout* signal in Fig. 7.6) serves to this purpose, the output frequency of PLL IN is inferred observing the output spectrum: first, assuming that both PLL IN and PLL CK are locked, the output spectrum should have a coherent look, without spectral leakage, and second, since we know the frequency divider value of both PLLs and the reference frequency applied to them, we know exactly where frequency f_{in} should lie in the spectrum. If the output spectrum is not coherent and/or f_{in} lies on an unpredicted FFT bin, we know that PLL IN is out of its locking range.

the ADC.

Given the above contextualization, we show in Fig. 7.16 the measured output spectra for Sample 1 not only for the current evaluation scenario, but also for the previous two evaluation modes. For a fair comparison, we use the same frequencies and amplitude for all cases, and we only change the sources of the analog input and clock signals: in Fig. 7.16a the analog input and clock are both provided externally by signal generators, in Fig. 7.16b the analog input is provided externally by a signal generator whereas the clock is provided internally by PLL CK, and in Fig. 7.16c the analog input and clock are both provided internally by PLL IN and PLL CK, respectively.

The spectrum of Fig. 7.16a serves as a baseline reference for comparison. We note in this spectrum, besides of the fundamental tone, a set of odd harmonic distortions, dominated by the third harmonic (−48.3 dB), and the TI spur (−44.4 dB), which is the strongest spurious tone in the spectrum.

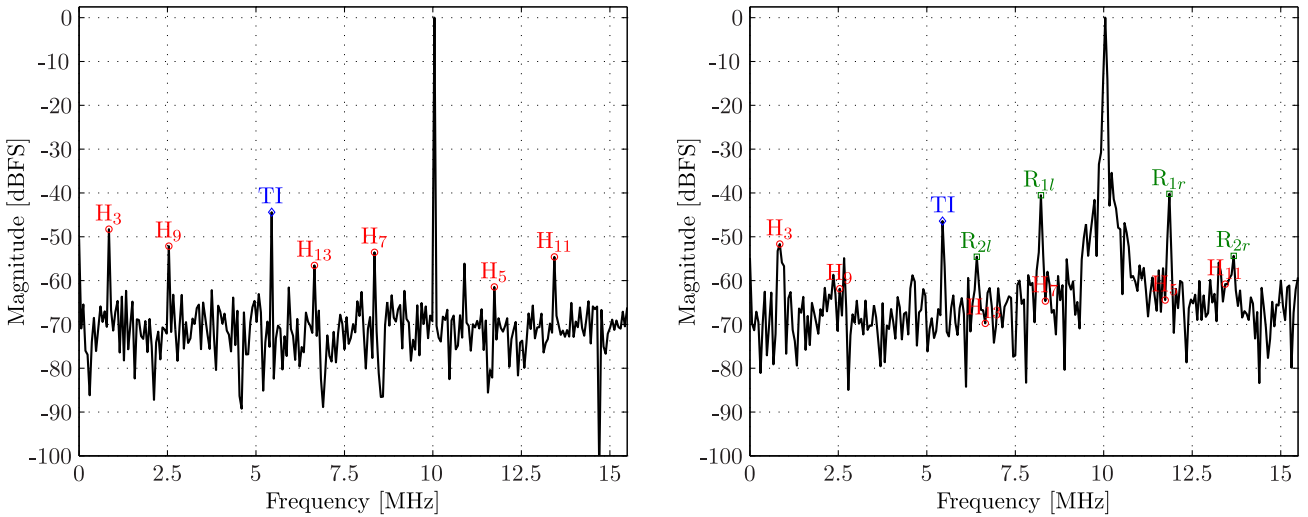
When we change the source of the clock signal from the external signal generator to the internal PLL CK, in Fig. 7.16b, we see that the third harmonic and the TI spur are still visible, while the other odd harmonics are somehow masked in the spectrum. This masking is partly due to the strong reference spurs, $R_{1,2l,r}$, which potentially mask adjacent tones, and partly due to increased noise floor caused by the incremented clock jitter.

If we neglect the reference spurs following the same reasoning discussed in Sec. 7.4.2, then the spectrum of Fig. 7.16b is dominated by the third harmonic (−51.7 dB) and the TI spur (−46.4 dB). The largest discrepancy with the corresponding values of Fig. 7.16a (baseline reference) is about 3.4 dB.

When both the analog input and clock are generated internally by PLL IN and PLL CK, in Fig. 7.16c, we observe that the reference spurs are somehow amplified, but the dominant harmonic and the TI spur are still showing up in the spectrum. Specifically, the third harmonic level is −41.4 dB and the TI spur is −42.2 dB. Comparing with the baseline performance, we have a 6.9 dB difference in the third harmonic level and a 2.2 dB difference in the TI spur level. The larger discrepancy in the third harmonic level is mainly due to the increased distortion introduced by the VCO of PLL IN (even thought we are using a $V_{\text{in}} \approx -2.5$ dBFS to reduce this impact).

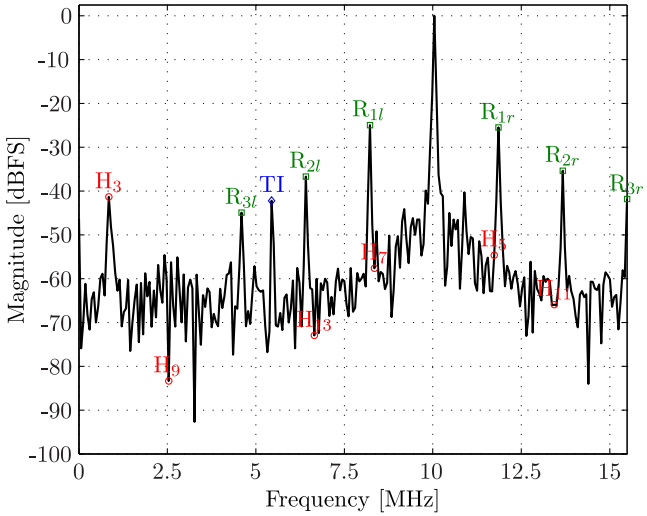
Similar conclusions can be drawn analyzing the output spectra of Samples 2 and 3, which are not shown here for sake of brevity.

In summary, provided that we disregard the reference spurs (since we know exactly where they appear and also know they are merely an artifact introduced by the PLLs and not by the ADC (DUT) itself), we can say that the quality of the analog input and clock signals produced by the PLLs of the built-in self-test scheme proposed in this work allows us evaluating an ADC with a SFDR as high as about 41.4 dB when sampling an almost-Nyquist-frequency tone at about 500 MS/s.



(a) External input and clock

(b) External input and internal clock



(c) Internal input and clock

Fig. 7.16: Measured output spectra (512 points) of Sample 1 at $f_s = 464.64$ MS/s ($= 256 \times 3.63/2$ MHz), $f_{\text{in}} = 226.875$ MHz ($= 125 \times 3.63/2$ MHz) and $V_{\text{in}} \approx -2.5$ dBFS for the three test scenarios. The frequency axis accounts for an output decimation of 15.

7.4.4 Complementary DUT Measurements

Some complementary measurement results are presented in this section. Even though these results are not essential to support the main conclusions of this work, they bring additional details and help justify the parameters selection made in the previous measurements.

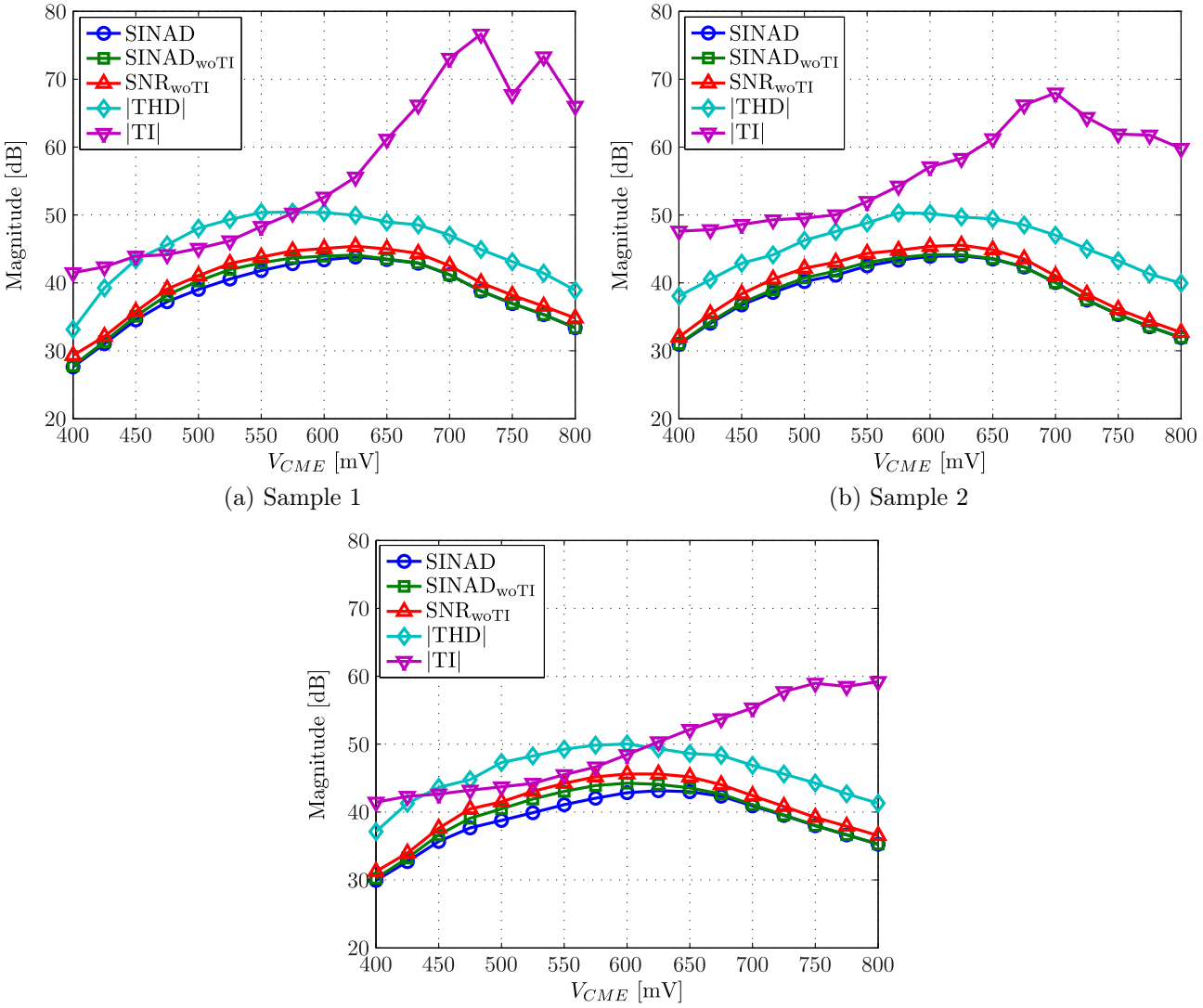
Figs. 7.17 and 7.18 show how the measured SINAD, SNR, THD, TI spur, and ENOB of three different die samples evolve as we change the external common-mode voltage, V_{CME}. For these measurements, $f_s = 500$ MS/s, $f_{\text{in}} \approx 10$ MHz and $V_{\text{in}} \approx -0.1$ dBFS are used.

Besides of setting the internal common-mode (i.e., the analog ground V_{CM}), the voltage V_{CME} (cf. Fig. 7.6) also influences the level setting of the ADC positive and negative reference voltages, V_{RP} and V_{RN}, respectively. Ignoring the nonidealities, we have $V_{RN} = 2/3V_{CME}$, $V_{CM} = V_{CME}$, and $V_{RP} = 4/3V_{CME}$. Hence, as we increase (decrease) the voltage V_{CME} from its nominal value of $V_{DD}/2 = 0.6$ V, so as increase (decrease) the difference between V_{RP} and V_{RN}. And, since $2 \times (V_{RP} - V_{RN})$ sets the maximum differential input full-scale range of the ADC, we need to adjust V_{in} accordingly to span the full-scale range as we change the voltage V_{CME}. The results shown in Figs. 7.17 and 7.18 account for this V_{in} adjustment.

Observing Fig. 7.17, we note that the key performance metrics, except the TI spur, do not vary significantly when 550 mV $\leq V_{CME} \leq$ 650 mV. Hence, the converter can tolerate V_{CME} variations of about 100 mV around its nominal value of 600 mV without significant performance penalties. The measured ENOB results shown in Fig. 7.18 indicate that the optimum performance for the three evaluated samples occurs indeed when V_{CME} is slightly above its nominal value, specifically, when $V_{CME} \approx 625$ mV.

It is interesting to observe the TI spur curves in Fig. 7.17. For all samples, the TI spur level has a considerable decrease as the V_{CME} voltage increases[14]. This behavior is partly explained because as we increase V_{CME} the full-scale range of the ADC is actually increasing. Then, when we reach $V_{CME} \approx 700$ mV, the full-scale range starts to saturate and consequently the TI spur level starts to deteriorate again.

[14]Please note that we are plotting the absolute value of the TI spur in Fig. 7.17, but, according to the definition of Eq. (7.1), the TI spur is always a negative (in dB sense) value.

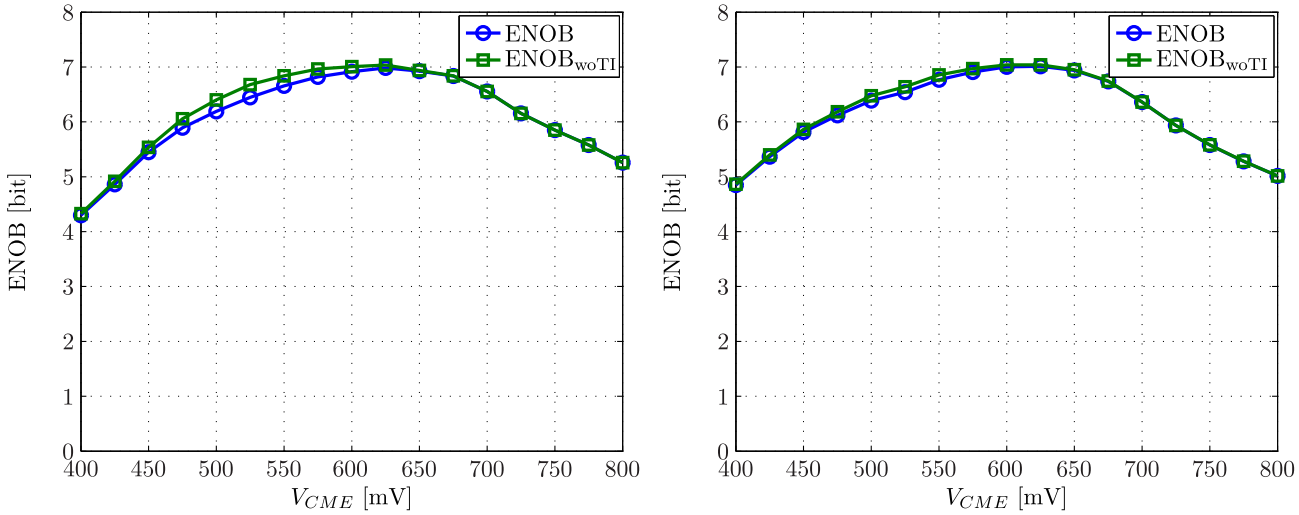


(a) Sample 1

(b) Sample 2

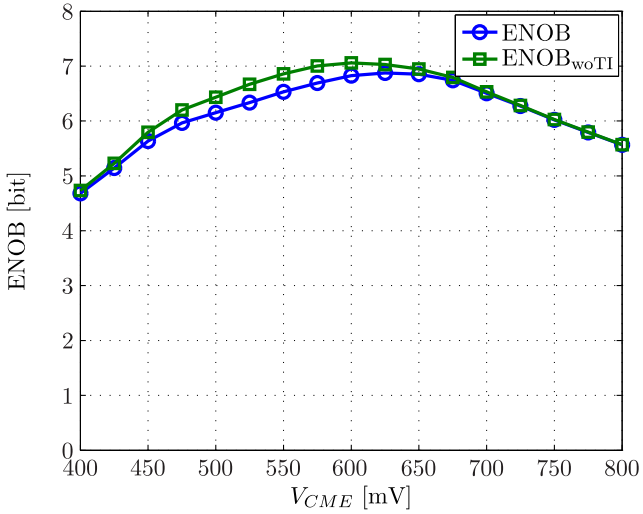
(c) Sample 3

Fig. 7.17: Measured SINAD, SNR, THD, and TI spur versus V_{CME} at $f_s = 500$ MS/s, $f_{\text{in}} \approx 10$ MHz and $V_{\text{in}} \approx -0.1$ dBFS for three different samples. Subscript "woTI" indicates that the corresponding metric has the time-interleaving spur impact removed.



(a) Sample 1

(b) Sample 2



(c) Sample 3

Fig. 7.18: Measured ENOB versus V_{CME} at $f_s = 500$ MS/s, $f_{\text{in}} \approx 10$ MHz and $V_{\text{in}} \approx -0.1$ dBFS for three different samples. Subscript "woTI" indicates that the corresponding metric has the time-interleaving spur impact removed.

Table 7.3: Summary of the key frequencies (in MHz) of the slowest locking range of PLL CK.

	Sample 1	Sample 2	Sample 3
$f_{\text{ckavg,min}}$	449.01	449.36	456.99
$f_{\text{ckavg,max}}$	479.08	482.67	487.77
Δf_{ckavg}	30.07	33.31	30.78
$\overline{f}_{\text{ckavg}}$	464.04	466.01	472.38
$\overline{f}_{\text{ref}}$	3.63	3.63	3.69

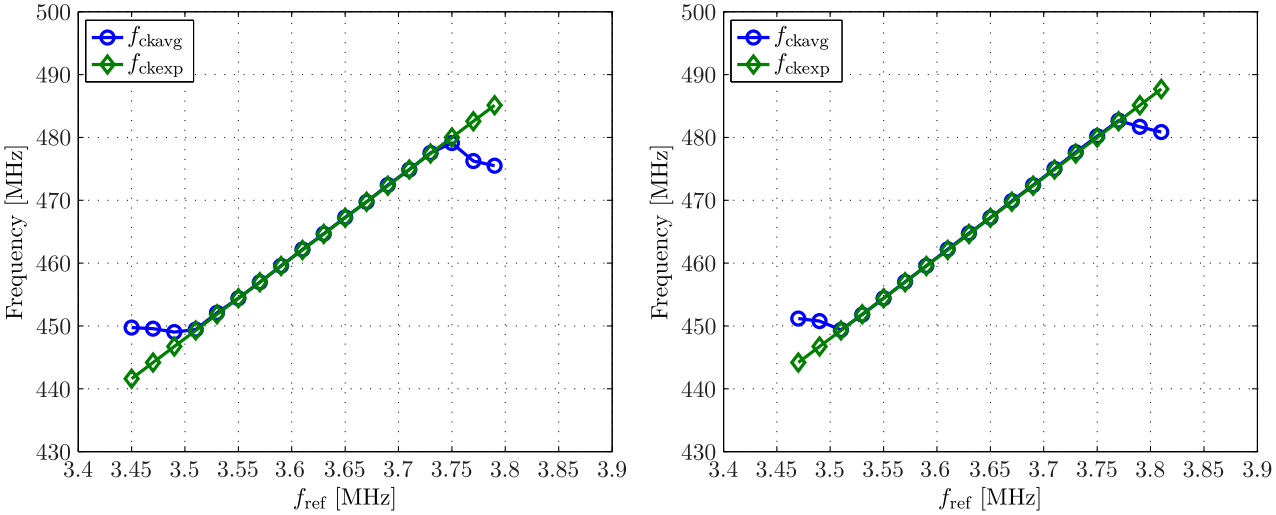
Table 7.4: Summary of the key frequencies (in MHz) of the fastest locking range of PLL CK.

	Sample 1	Sample 2	Sample 3
$f_{\text{ckavg,min}}$	952.65	961.05	965.79
$f_{\text{ckavg,max}}$	1021.50	1031.90	1036.70
Δf_{ckavg}	68.85	70.85	70.91
$\overline{f}_{\text{ckavg}}$	987.07	996.47	1001.24
$\overline{f}_{\text{ref}}$	3.85	3.89	3.91

The measured locking range of PLL CK when its voltage-controlled oscillator is set to the slowest discrete tuning curve is shown in Fig. 7.19. The output clock frequency, f_{ckavg}, is read after setting a given value for the external reference frequency, f_{ref}, and each data point on the curve represents the average of 10,000 clock periods captured by an oscilloscope (R&S RTO 1022). We use averaging here to enhance the accuracy of the measurements.

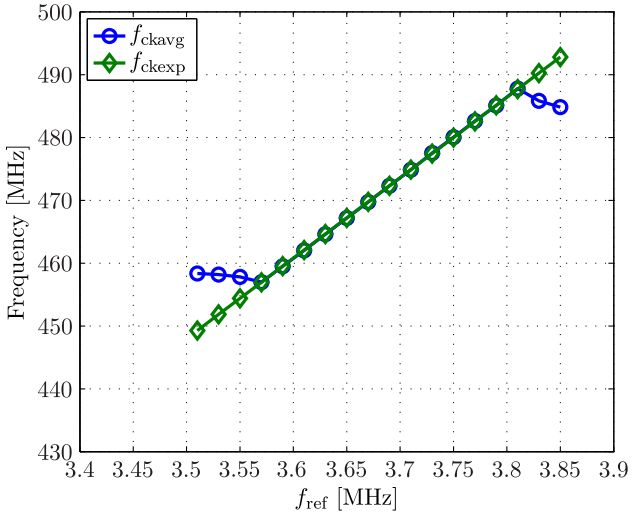
In order to compare die-to-die process variations, it is useful to identify the f_{ckavg} minimum, maximum, span range, and average (or center) frequencies. Also, the corresponding reference frequency average is equally important, since it is based on it that the external reference frequency is selected. Table 7.3 summarizes the key data for the locking ranges shown in Fig. 7.19. We can see that the locking ranges (Δf_{ckavg}) of the three samples span approximately 30 MHz. In addition, center frequencies ($\overline{f}_{\text{ckavg}}$) of these locking ranges are shifted by a maximum of 8.34 MHz. This $\overline{f}_{\text{ckavg}}$ spread, however, is not significant because the locking ranges of the measured samples still have a considerable overlapping. Hence, it is still possible to put PLL CK in lock state using a relatively large range of f_{ref} frequencies.

The measured locking range of PLL CK for the fastest discrete tuning curve is shown in Fig. 7.20, and the key details are summarized in Table 7.4. We can see that locking ranges of the three measured samples span about 70 MHz. Additionally, the locking ranges centers are shift by a maximum of 14.17 MHz. Even thought this spread is almost twice the one indicated above for the slowest discrete tuning curve, the impact is not worst because the locking ranges are more than twice as large as the ones indicated above. Hence, a good overlapping among the locking ranges is still present.



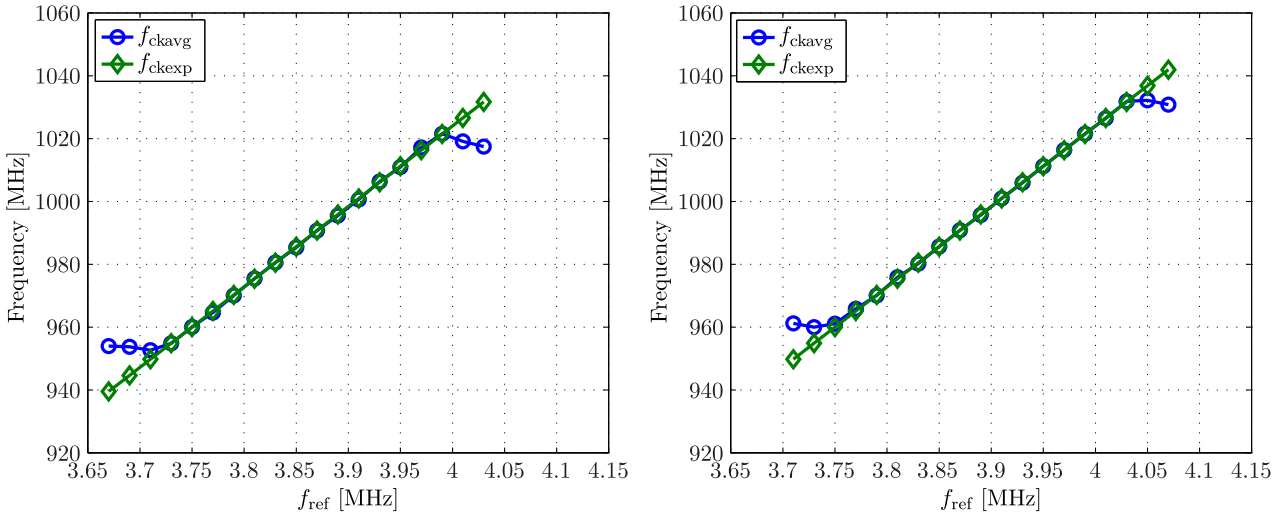
(a) Sample 1

(b) Sample 2



(c) Sample 3

Fig. 7.19: Measured locking range of PLL CK for the slowest discrete tuning curve. The expected output clock frequency, f_{ckexp}, represents the behavior of an ideal PLL with infinite locking range.



(a) Sample 1

(b) Sample 2

(c) Sample 3

Fig. 7.20: Measured locking range of PLL CK for the fastest discrete tuning curve. The expected output clock frequency, f_{ckexp}, represents the behavior of an ideal PLL with infinite locking range.

Table 7.5: Performance summary and comparison with prior works.

		This Work	[47]*	[53]*	[46]*
Technology	[μm]	0.13	0.13	0.13	0.8
Area	[mm^2]	0.052	0.51†	0.186	0.833
Power	[mW]	26.0	39.5	4.04	36.5
Supply Voltage	[V]	1.2	1.4	1.2	N/A
ADC Input Voltage	[mV$_{pp}$]	600	149	228	N/A
ADC Input Frequency	[MHz]	227	312	10	40
SFDR	[dB]	41.4§	25.3	74.1	65.4‡
ADC Clock Frequency	[MHz]	465	N/A	N/A	N/A
ADC Clock Jitter	[ps]	1.5**	N/A	N/A	N/A

* Do not deal with the clock signal generation.
† Area of the read-only memory not included.
‡ SFDR measured at 1 MHz frequency.
§ Ignoring PLLs reference spurs.
** Jitter rms integrated above 1 MHz and estimated from simulation.

7.5 Comparison and Discussion

The BIST scheme proposed in this work can be compared with other works available in the open literature, as shown in Table 7.5.

One of the key requisites of a BIST circuitry is small area overhead, since the extra silicon area impacts both in the overall cost and in the yield of the integrated circuits. As we can see in Table 7.5, our work has an almost fourfold area improvement compared with the most area-efficient implementation, even ignoring that those works do not deal with the clock signal generation. This improvement is achieved by a judicious selection of circuit topologies and techniques. For instance, instead of using area-hungry LC oscillators to build up the voltage-controlled oscillators of the phase-locked loops, we relied on simple RC oscillators. As another example, we use a capacitance multiplication scheme to reduce the capacitances, and consequently the silicon area, of the loop filters of the phase-locked loops.

The power dissipation of the BIST circuits is not very important because these circuits are only used during a fraction of the operation time of the remaining (core) circuits, usually in the course of the power-on or during idle time slots. After the self-test procedures, the BIST circuits are turned-off, dropping the power dissipated by these circuits to (almost) zero. Hence, even thought the BIST circuits proposed in this work dissipate a relatively considerable 26 mW, this is fine for the target application.

We compare the quality of the analog input signal provided to the device under test using the SFDR metric. Even though the measured SFDR of this work is worst than those of [46, 53], it is obtained for much larger analog input frequencies and amplitudes. For example, the SFDR of 74.1 dB reported in [53] is for an analog input frequency as low as 10 MHz and for a differential amplitude as small as 228 mV$_{pp}$. In general, it is unfeasible or very difficult to keep a high SFDR while increasing the analog input frequency and/or amplitude, since the circuits suffer from stronger distortions or other restricting artifacts (e.g., bandwidth). This argument is fully reflected in the SFDR of

25.3 dB reported in [47], where the input frequency is 312 MHz.

The main limitations of the generated analog input and clock signals of the proposed BIST scheme are the following:

- Distortions in the analog input signal. The sources of these distortions are the nonlinearity of the VCO of PLL IN, and also the nonlinearity of the buffer that follows this VCO and drives the front-end track-and-hold of the ADC.
- Phase noise (or jitter) in the analog input and clock signals. The source of this noise is mainly the noise present in the active devices that build the VCOs of PLL IN and PLL CK.
- Deterministic reference spurs. The sources of these spurs are nonidealities (mainly mismatch) in the charge pumps of both PLL CK and PLL IN.

These limitations can be alleviated by means of improvements in the sizing of the employed circuits, by enhancements in the circuit topologies, and by drawing even more careful layouts. Also, as discussed in the previous sections, some of these limitations are more severe than others. For example, the deterministic reference spurs are not much problematic, since they can be easily isolated from the actual performance of the ADC under test.

In this work, ignoring the reference spurs of the phase-locked loops, we achieve a worst-case (for three measured samples) SFDR as high as 41.4 dB for an analog input frequency of about 227 MHz and a differential amplitude of 600 mV_{pp}. Though these results represent the undertaken measurements, simulations of the proposed circuits reveal that it is possible to reach good SFDR values for higher frequencies as well [13].

The SFDR of the generated analog input signal is also dependent on the employed supply voltage, since reducing the supply voltage (which is the trend for newer CMOS technology nodes) equally reduces the voltage headroom available to keep the active devices operating in saturation. Put in other words, reducing the supply voltage increases the distortions of a given circuit topology maintaining the same signal swings, unless topology changes (if viable) are made.

The phase noise (or jitter) present both in the analog input and in the clock appears combined in the output spectrum, rising the noise floor, as previously shown in Sec. 7.4.3. In this work, in view of the prototype complexity and reduced number of I/O pins, it was not implemented observation points to experimentally quantify the jitter of PLL IN and PLL CK in separate. Hence, we qualitatively gain insight on the impact of the jitter of both PLLs observing the evolution of the output spectrum while changing the signal sources (as illustrated in Fig. 7.16).

By means of post-layout simulations, we can estimate the integrated rms jitter (above 1 MHz offset) of PLL CK as 1.5 ps, as indicated in Table 7.5. This result, however, cannot be contrasted with the other works, since those works only address the analog input signal generation.

Chapter 8

Conclusions

The testing of high speed data converters, particularly ADCs, is an important issue of today's mixed-signal circuits. Pushed by the ever-increasing digital signal processing data rates, the conversion speeds of data converters are progressively increasing as well to keep pace with this trend. This phenomenon, however, exacerbates the problems involved in the testing of these devices. In view of this open challenge, a fully integrated, low cost, and reconfigurable architecture for coherent self-testing of high speed ADCs is presented in this work.

The proposed built-in self-test solution is based on two synchronized PLLs, one to synthesize the analog input signal and another to synthesize the clock signal for an ADC under test. This synchronization is a key feature in the proposed approach, since it allows coherent sampling.

With coherent sampling, the digital output data of the converter are well-behaved and their spectrum is clear (unambiguous), in the sense that it is possible to distinguish the most relevant frequency components without worrying with spectral leakages, windowing, etc. Hence, with a reduced record length and a relatively low-complexity DSP hardware, it is feasible to do a reliable spectral analysis to assess the functional dynamic performance of the ADC.

Special techniques and circuits were proposed/adopted to implement compact and dedicated PLLs for this particular application. On the one hand, these techniques allowed to reduce the area of the BIST circuitry considerably and, in consequence, the extra cost and the penalty on the final yield. On the other hand, these techniques do not severely compromised the generation of relatively good quality analog input and clock signals, in terms of phase noise and distortion, thus enabling the assessment of a moderate resolution ADC. Even though the proof-of-concept is made with a moderate resolution converter, the idea proposed in this work can be extended to low and high resolution ADCs as well, given the necessary changes or enhancements are carried out.

The proposed BIST architecture for ADCs is reconfigurable. That is, it is possible to synthesize different analog input and clock frequencies by simply changing the frequency dividers values related to the PLLs. The attainable frequency ranges depend on the designed locking ranges of the PLLs. With this reconfiguration, it is feasible to evaluate the ADC under different scenarios.

To experimentally validate the proposed BIST methodology, the BIST circuitry, essentially comprised of two PLLs and interfacing circuits, alongside with a two-channel

time-interleaved pipelined ADC are implemented in a 0.13 μm CMOS technology. The ADC topology is irrelevant in this context, since the proposed self-test solution views the converter as a "black box"[1]. Nonetheless, a time-interleaved pipelined ADC topology was selected to reach a reasonable resolution and the highest conversion rate possible in the given technology, while do not complicating the ADC design so much. As a result, an 8-bit 500 MS/s ADC was implemented.

8.1 Suggestions for Future Work

For more developed a work is, it is never finished. There is always margins for improvements, since it is hard (not to say impractical for most of the times) to support that a given circuit or system is exhibiting its optimal performance, and for new investigations, since due to time constraints we need to concentrate our efforts on a limited exploration horizon.

Hence, this section serves to suggest some improvements that the author believes it is possible to reach and to indicate future research topics that would be worthwhile to pursue. These suggestions are:

- The phase-locked loops used to generate the test stimuli for the ADC under test exhibited stronger reference spurs than anticipated by simulations. We already discussed the causes of these stronger reference spurs; only to recapitulate, charge pumps' mismatch and leakage. Hence, more attention is deserved in the design of the charge pumps to reduce these problems.

- The phase-locked loops, which are the core of the proposed BIST system, are experiencing tremendous innovative improvements year-after-year, similarly as it take place for the A/D converters. One reason for these improvements is that the PLLs are an active research line, since they find widespread application. Another reason is certainly related to the advantages brought by the modern CMOS technologies, which allow room for novel concepts and ideas. Consequently, the BIST system proposed here can benefit directly from these achievements. For example, today all-digital PLLs are replacing the traditional charge-pump PLLs with the same or better performance while occupying a fraction of silicon area [84].

- As we discussed in the literature review, the BIST implementations are commonly divided into the test stimulus generator (TSG) and the output response analyzer (ORA). In this work, since we assume the ORA will be implemented reusing the hardware available, for example, in a system-on-a-chip embedded ADC or, in case of a standalone ADC, it will be implemented in a modern CMOS technology, where the cost of a few extra digital gates is minimal, we concentrate our efforts exclusively on the test stimulus generation. As a result, a possible future research line could be the investigation of new output response analysis methods, particularly those

[1]Even though the converter resembles a "black box" to the BIST circuitry, the input impedance of the converter (whether it is switched or not, whether it is capacitive or not, etc.) matters a lot when selecting the topology and designing the linear buffer that drives the ADC analog input. The converter's topology also affects the clock input, but generally in less extend and complexity.

related to spectral analysis, in order to benefit from the test stimulus generation proposed here.

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Appendix A

System Configuration

This appendix presents the configuration options available in the designed prototype. These options permit to configure the prototype in distinct operating modes, which allow evaluating the internal modules separately and/or with more flexibility in their parameters.

A set of on-chip counters controlled by external push-button switches enable the choice among different configurations. This approach reduces considerably the number of I/O pins while maintaining the implementation complexity low. Another more complex solution, which would lead to a reduced set of I/O pins, would be to use a serial interface bus, like SPI or I^2C.

We address bellow how the configurable counters behave when driven by the external switches and how they affect the system configuration. Before proceeding, however, we define some terms that will be used within this section:

- NL: Normally low logic state (set by means of an on-chip pull-down resistor).
- X: Do not care or unknown logic state.
- H: High logic state.
- L: Low logic state.
- L $\rightarrow$ H: Low-to-high (i.e., rising) logic state transition.

ADC Configurable Counter This counter controls the ADC multiplexers employed to select between decimated output or not, between external analog input or BIST analog input (i.e., generated by PLL IN), and between external clock or BIST clock (i.e., generated by PLL CK). Hence, a total of eight configurations are possible, as indicated in Table A.1.

The description of the signals associated with ADC configurable counter is as follows:

- *adcconfig*: A low-to-high logic transition in this signal increments the on-chip 3-bit counter by one.
- *rst*: Reset signal (activated high).
- $b0 \ldots b2$: Counter output bits (LSB to MSB).
- *decimate*: When selected (indicated by ✓), decimates the output of the ADC by a factor of 15.
- *inbisten*: When selected, the analog input signal of the ADC is provided by the on-chip BIST circuitry; otherwise, it comes from an external signal generator.

- *ckbisten*: When selected, the clock signal of the ADC is provided by the on-chip BIST circuitry; otherwise, it comes from an external signal generator.

VCO CK Configurable Counter This counter controls the capacitor bank used to tune VCO CK discretely. This voltage-controlled oscillator is the one associated with PLL CK, responsible for generating the clock signal on-chip. In the designed prototype, VCO CK has only two discrete tuning curves, consequently only one bit is sufficient to completely control this simple capacitor bank, as shown in Table A.2.

The description of the signals associated with the configurable counter of VCO CK is as follows:

- *vcoclkconfig*: A low-to-high logic transition in this signal toggles the logic state of the on-chip 1-bit counter.
- *rst*: Reset signal (activated high).
- *b*0: Counter output bit.
- *vcockb*0: When *vcockb*0 is logic low, the additional capacitor used for discrete tuning is switched off. Therefore, the fastest VCO tuning characteristic is selected. When *vcockb*0 is logic high, the discrete tuning capacitor is switched on and the slowest VCO tuning characteristic is selected.

VCO IN Configurable Counter This counter controls the capacitor bank used to tune VCO IN discretely. This voltage-controlled oscillator is the one associated with PLL IN, responsible for generating the analog input signal on-chip. In the designed prototype, VCO IN has only two discrete tuning curves (similarly as VCO CK), consequently only one bit is sufficient to completely control the corresponding capacitor bank, as shown in Table A.3.

The description of the signals associated with the configurable counter of VCO IN is as follows:

- *vcoinconfig*: A low-to-high logic transition in this signal toggles the logic state of the on-chip 1-bit counter.
- *rst*: Reset signal (activated high).
- *b*0: Counter output bit.
- *vcoinb*0: When *vcoinb*0 is logic low, the additional capacitor used for discrete tuning is switched off. Therefore, the fastest VCO tuning characteristic is selected. When *vcoinb*0 is logic high, the discrete tuning capacitor is switched on and the slowest VCO tuning characteristic is selected.

DIV IN Configurable Counter This counter is used to configure the integer frequency divider of PLL IN. Possible divider values range from 32 to 127. In order to ease the selection of a specific divider value with the 7-bit configurable counter, an up/down counter is used. Hence, the count direction (up or down) can be changed at any time avoiding a long wrap around. Table A.4 shows how the desired divider values are selected.

The description of the signals associated with this configurable counter is as follows:

- *divinconfig*: A low-to-high logic transition in this signal increments/decrements the 7-bit up/down counter by one, depending on the state of the internal *updw* control signal. If *updw* is low, the counter decrements. If *updw* is high, the counter increments.

- *divrefconfigupdw*: This signal controls the internal *updw* signal. After reset, internal *updw* is set to low. Afterwards, each low-to-high logic transition in *divrefconfigupdw* toggles the state of *updw* signal (this behavior is indicated by the dark gray rows of Table A.4).
- rst: Reset signal (activated high).
- $b0 \dots b6$: Counter output bits (LSB to MSB).
- $pin0 \dots pin6$: Programable divider word. The decimal representation of this word corresponds to the specific divider value. For example, $(1111111)_2 = (127)_{10} \mapsto \div 127$. Note that for $pin0 \dots pin6 = (0)_{10}$ to $(31)_{10}$ the corresponding divider value is shifted up by 32 (this feature is indicated by the light gray rows in Table A.4).

DIV REF Configurable Counter This counter is used to configure the reference frequency divider. Possible divider values are 1 or 2 only, as shown in Table A.5.

The description of the signals associated with this configurable counter is as follows:

- *divrefconfigupdw*: A low-to-high logic transition in this signal toggles the 1-bit counter. Note this signal is also used to control the direction (up or down) of the DIV IN counter.
- rst: Reset signal (activated high).
- $b0$: Counter output bit.
- *pref*: When *pref* is low, the external reference clock is directly applied to the PFD of both PLLs. When *pref* is high, the external reference signal is divided by two before being applied to the PFDs.

Table A.1: ADC decimation, analog input, and clock configuration.

External signals		Counter outputs			Internal control signals			Comments
adcconfig	*rst*	*b*0	*b*1	*b*2	*decimate*	*inbisten*	*ckbisten*	
NL	NL	X	X	X	X	X	X	Unknown eval.
X	H	0	0	0	✗	✗	✗	Standalone ADC eval.
1st L → H	L	1	0	0	✓	✗	✗	
2nd L → H	L	0	1	0	✗	✓	✗	ADC + PLL IN eval.
3rd L → H	L	1	1	0	✓	✓	✗	(f_s of few MHz only)†
4th L → H	L	0	0	1	✗	✗	✓	ADC + PLL CK eval.
5th L → H	L	1	0	1	✓	✗	✓	
6th L → H	L	0	1	1	✗	✓	✓	ADC + PLL CK +
7th L → H	L	1	1	1	✓	✓	✓	PLL IN eval.
8th L → H(repeat)	L	0	0	0	✗	✗	✗	Standalone ADC eval.
...								

† In this evaluation mode, the external clock serves simultaneously as the reference clock for PLL IN and for the ADC itself. Hence, the sampling frequency, f_s, is restricted to only a few MHz.

Table A.2: VCO CK discrete tuning configuration.

External signals		Counter output	Internal control signal
vcockconfig	*rst*	*b*0	*vcockb*0
NL	NL	X	X
X	H	0	Capacitor switched off
1^{st} L $\rightarrow$ H	L	1	Capacitor switched on
2^{nd} L $\rightarrow$ $H^{(repeat)}$	L	0	Capacitor switched off
...			

Table A.3: VCO IN discrete tuning configuration.

External signals		Counter output	Internal control signal
vcoinconfig	*rst*	*b*0	*vcoinb*0
NL	NL	X	X
X	H	0	Capacitor switched off
1^{st} L $\rightarrow$ H	L	1	Capacitor switched on
2^{nd} L $\rightarrow$ $H^{(repeat)}$	L	0	Capacitor switched off
...			

Table A.4: DIV IN division value configuration.

External signals			Counter outputs	Internal control signals
divinconfig	*divrefconfigupdw*	*rst*	$b0 \dots b6$	$pin0 \dots pin6$
NL	NL	NL	XXXXXXX	XXXXXXX $\mapsto \div$X
X	X	H	0000000	0000000 $\mapsto \div 32$
1st L $\rightarrow$ H	L(down count; default after reset)	L	1111111	1111111 $\mapsto \div 127$
2nd L $\rightarrow$ H	L	L	0111111	0111111 $\mapsto \div 126$
...	...	...	...	...
64th L $\rightarrow$ H	L	L	1111110	1111110 $\mapsto \div 63$
65th L $\rightarrow$ H	L	L	0111110	0111110 $\mapsto \div 62$
...	...	...	...	...
95th L $\rightarrow$ H	L	L	1000010	1000010 $\mapsto \div 33$
96th L $\rightarrow$ H	L	L	0000010	0000010 $\mapsto \div 32$
97th L $\rightarrow$ H	L(div. value shifted up by 32)	L	1111100	1111100 $\mapsto \div 63^{(\text{not } 31)}$
98th L $\rightarrow$ H	L	L	0111100	0111100 $\mapsto \div 62^{(\text{not } 30)}$
...	...	...	...	...
127th L $\rightarrow$ H	L	L	1000000	1000000 $\mapsto \div 33^{(\text{not } 1)}$
128th L $\rightarrow$ H	L	L	0000000	0000000 $\mapsto \div 32$
L	1st L $\rightarrow$ H(set up count)	L	0000000	0000000 $\mapsto \div 32$
129th L $\rightarrow$ H	L(div. value shifted up by 32)	L	1000000	1000000 $\mapsto \div 33^{(\text{not } 1)}$
130th L $\rightarrow$ H	L	L	0100000	0100000 $\mapsto \div 34^{(\text{not } 2)}$
131st L $\rightarrow$ H	L	L	1100000	1100000 $\mapsto \div 35^{(\text{not } 3)}$
...	...	...	...	...
255th L $\rightarrow$ H	L	L	1111111	1111111 $\mapsto \div 127$
L	2nd L $\rightarrow$ H(set down count again)	L	1111111	1111111 $\mapsto \div 127$
256th L $\rightarrow$ H	L	L	0111111	0111111 $\mapsto \div 126$
257th L $\rightarrow$ H	L	L	1011111	1011111 $\mapsto \div 125$
...				

Table A.5: DIV REF division value configuration.

External signals		Counter output	Internal control signal
divrefconfigupdw	*rst*	$b0$	*pref*
NL	NL	X	X
X	H	0	$0 \mapsto \div 1$
1st L $\rightarrow$ H	L	1	$1 \mapsto \div 2$
2nd L $\rightarrow$ H(repeat)	L	0	$0 \mapsto \div 1$
...			

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