NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ALEXANDRE MIGUEL AFONSO DE BRITO

BSc Electrical and Computer Enginnering

ANALYSIS AND PERFORMANCE EVALUATION OF HIGH EFFICIENCY AMPLIFIERS FOR 5G AND WI-FI WAVEFORMS

MASTER IN ELECTRICAL AND COMPUTER ENGINNERING

NOVA University Lisbon
September, 2022

NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ANALYSIS AND PERFORMANCE EVALUATION OF HIGH EFFICIENCY AMPLIFIERS FOR 5G AND WI-FI WAVEFORMS

ALEXANDRE MIGUEL AFONSO DE BRITO

BSc Electrical and Computer Enginnering

Adviser: Rui Dinis
Associate Professor, NOVA University of Lisbon

Co-advisers: Hugo Serra
Researcher, UNINOVA

João Oliveira
Associate Professor, NOVA University of Lisbon

Examination Committee

Chair: Paulo Montezuma
Associate Professor, FCT-NOVA

Rapporteur: Luis Bica Oliveira
Associate Professor, FCT-NOVA

Member: Hugo Serra
Researcher, UNINOVA

MASTER IN ELECTRICAL AND COMPUTER ENGINNERING
SPECIALIZATION IN RF ELECTRONICS AND MOBILE COMMUNICATIONS

NOVA University Lisbon
September, 2022

Analysis and performance evaluation of high efficiency amplifiers for 5G and Wi-Fi waveforms

This document was created with the (pdf/Xe/Lua)LaTeX processor and the NOVAthesis template (v6.9.15) [1].

Acknowledgements

The first big thanks naturally have to go to my family including my brother, my mom, my dad, and my aunts. Firstly, I have to thanks for all the investment made in my education that allowed me to be the best version of myself and create the best product out of myself. Secondly, their philosophies of never giving up have really shaped the way I am and behave.

I want to thank Hugo Serra for his support since the beginning and clearance in times of indecision. Hugo was a very inspiring person in this process, from the amount of knowledge he possess but also the easiness of transmitting knowledge. Hugo taught me how to use Cadence in a more professional way allowing me to level up my game on this software. Professor João Oliveira was very important to show the panorama and the state of the art of power amplifiers. The conversations with professor João always gave food for thought. I also want to thank Professor Rui Dinis for his rapid support and motivation throughout this journey.

I can't continue without giving props to my friends, José, Pedro, João, Gonçalo and Martim. Every time I was feeling under the weather or down because things weren't going the right way, they were always there for me and helped me to get on the right tracks again. Surely the best friendships life gave me. In a farewell style, I have to be grateful to have met great colleagues that share the same principles as I do and always strive for perfection. They aren't many so I can just name them here, João Faria, Pedro Capelo and Saul Neto. Having worked with them as a team really showed me what engineering is all about. I hope to work with them in the future!

"Success is not final, failure is not fatal, it is the courage to continue that counts" (Winston Churchill)

Abstract

The trend of wireless and mobile networks is to increase the capacity in terms of the number of users connected to the mobile network and the capacity in terms of bit rate. The main goal of 5G is to provide ultra-reliable, fast, and low-latency communications. The field of applications of 5G entails, for example, IoT, smart cities, and virtual reality. To achieve this level of massification, the mobile handsets have to be the most low-cost and compact and the base stations need to be the most power-efficient possible.

In order to achieve higher data rates and higher spectral efficiency, modulation schemes with high envelope fluctuations must be employed. Given this signal envelope fluctuation, state-of-the-art PA's are working at a point where it only outputs 10 W of 100 W. Now given the complexity and the number of base stations a mobile operator has, it is not hard to imagine the energy costs. With this scenario in hand, a new technique called Quantized Digital Amplifier (QDA) with promising efficiency results is exposed.

Moreover, the focus of the thesis leans on understanding the factors that condition the development of a power amplifier. With the development of an innovative design kit, the reader will understand the ins and outs of a class E power amplifier including a theoretical analysis of the losses due to real components. Based on this theoretical analysis and using a 130 nm CMOS technology, a class E cascode topology will be designed for four distinct output power levels. Namely, for a 12 mW output power level, a PAE of 46% was achieved.

Keywords: OFDM, QDA, Mobile Networks, Class E PA, 5G, Wi-Fi, Power Amplifiers, Power Electronics

Resumo

A tendência das redes sem fios e móveis é aumentar a capacidade em termos de número de usuários conectados à rede móvel e capacidade em termos de ritmo binário. O principal objetivo do 5G é fornecer comunicações confiávies, rápidas e de baixa latência. O campo de aplicações do 5G envolve, por exemplo, IoT, cidades inteligentes e realidade virtual. Para atingir esse nível de massificação, os telemóveis devem ser os mais baratos e compactos e as estações base precisam ser mais eficientes em termos energéticos.

Para alcançar ritmos binário cada vez mais altos e uma maior eficiência espectral, esquemas de modulação com altas flutuações da envolvente complexa devem ser empregues. Dada essa flutuação de envolvente, os amplificadores de potencia de última geração estão a operar num ponto de eficiência em produzem apenas 10 W de 100 W. Agora, dada a complexidade e o número de estações base que uma operadora móvel possui, não é difícil imaginar os custos de energia. Com este cenário em mãos, uma nova técnica chamada Quantized Digital Amplifier (QDA) com resultados promissores de eficiência é exposta.

Além disso, o foco da tese vai também passar pela compreensão de fatores que condicionam o desenvolvimento de um amplificador de potência. Com o desenvolvimento de um kit de design inovador, o leitor entenderá os prós e contras do design de um amplificador de potência em classe E, incluindo uma análise teórica das perdas devido a componentes reais. Com base nesta análise teórica e usando uma tecnologia CMOS de 130 nm, uma topologia de cascode classe E será projetada para quatro níveis de potência de saída distintos. Nomeadamente, para um nível de potência de saída de 12 mW, um PAE de 46% foi alcançado.

Palavras-chave: OFDM, QDA, Redes Móveis, Class E PA, 5G, Wi-Fi, Amplificadores de Potência, Electrónica de Potência

Contents

List of Figures

List of Tables

Acronyms

AC Alternating Current *(p. 93)*
ADSL Asymmetric Digital Subscriber Line *(p. 4)*
AM Amplitude Modulated *(pp. 24, 25)*

BPSK Binary Phase Shift Keying *(p. 28)*
BS Base Station *(pp. 1, 2)*

CMOS Complementary metal–oxide–semiconductor *(pp. 88, 92)*
CSV Comma Separated Values *(p. 99)*

DC Direct Current *(pp. 3, 21, 23, 26)*

FDM Frequency Divsion Multiplexing *(p. 5)*
FPGA Field Programmable Gate Array *(pp. 3, 32)*

GaN Gallium Nitride *(p. 88)*
GMSK Gaussian Minimum Shift Keying *(p. 1)*

IFFT Inverse Fast Fourier Transform *(p. 5)*
ISI Inter Symbolic Interference *(pp. 4, 6)*

LF PA Low Frequency Power Amplifier *(p. 24)*
LINC Linear Amplification with non linear components *(p. 24)*
LNA Low Noise Amplifier *(p. 12)*

MH Mobile Handset *(p. 1)*
MIMO Multiple-input/multiple-out *(p. 4)*

NovaTek NovaTek Microelectronics *(p. 86)*

OFDM Orthogonal Frequency Division Multiplexing *(pp. 1, 3–7, 28, 75)*
OPEX Operational Expenditure *(p. 2)*

PA Power Amplifier *(pp. 1–4, 9–11, 14, 20, 23–25, 29, 31, 32, 87, 88)*
PAE Power Added Efficiency *(pp. xi, xii, 3, 10, 29, 30, 39, 41, 56, 59, 64, 66–69, 71, 73–75, 78–88, 105, 109)*
PM Phase Modulated *(pp. 24, 25)*
PMEPR Peak-To-Mean Envelope Power Ratio *(pp. 7, 9, 20, 28)*
PSS Periodic Steady State analysis *(pp. 66, 67, 72)*

QDA Quantized Digital Amplifier *(pp. 2, 3, 28, 30, 59, 75, 87, 88)*

RF Radio Frequency *(pp. 24, 37, 43)*

SRF Self Ressonant Frequency *(p. 50)*
STM STMicroelectronics *(p. 86)*

TSMC Taiwan Semiconductor Manufacturing Company *(p. 86)*

UMC United Microelectronics Corporation *(pp. 51, 86)*

ZDVS Zero Derivative Voltage Switching *(pp. 33, 34)*
ZVS Zero Voltage Switching *(pp. 33, 34)*

1 Introduction

1.1 Motivation and Scope

Energy efficiency is an increasingly a growing topic when it comes to mobile networks. With the release of the fifth mobile generation, finding ways to efficiently use energy in mobile handsets and base stations is a growing field of study. 5G represents in a way the densification of mobile networks. It is estimated that by 2025 the number of global connections reaches 100 billion [2]. The biggest innovation of 5G relative to its predecessor, is the data rate and the field of application. Vehicle-to-vehicle communication augmented reality and remote surgical operations are some of the many fields that 5G intends to penetrate. A brief comparison between 4G and 5G can be seen in Table 1.1. The information from these table was extracted from [3]

Table 1.1: Comparison between existing solutions.

Parameters	**4G (LTE Advanced)**	**5G**
Speed (Mbps)	100	1000
Latency (mS)	200	1
Devices Connected (d/km^2)	10000	1 million
Base Station (BS) power consumption (kW)	6.877	11.577
Mobile Handset (MH) power consumption (W)	0.2	0.4

In the second generation, it was employed a Gaussian Minimum Shift Keying (GMSK) modulation. As a result, the envelope was constant hence there was no problem with Power Amplifier (PA) efficiency. However, with the growing need for data rate, data modulations with higher envelope modulation were employed, making the apparent nonexistent problem in 2G a growing concern for mobile operators. In 4G the problem reached new peaks with the implementation of Orthogonal Frequency Division Multiplexing (OFDM). OFDM is a modulation technique that allows spectral efficiency maximization, making then a better use of the spectrum (a scarce resource). One of the problems of OFDM is its

high envelope fluctuation. This problem decreases substantially the power efficiency of the PA. In light of the latency and devices-connected specifications of 5G, it is no surprise that energy efficiency is the make or break of this mobile technology. Energy consumption constitutes around 20% to 40% of the network Operational Expenditure (OPEX) [4]. From a base station point of view, there are many sources of energy consumption hence energy efficiency. The energy consumption of each element of the base station depends on the size of the base station [5].

The main goal of 5G is to have more devices connected and reduced latency, BS tend to get smaller and smaller. This results in the PA being the element of a BS with the most energy consumption. That is why solving the problem of energy efficiency is expected to make 5G a more efficient and sustainable technology. Despite this solution being the main topic of this thesis, there was research on other ways to increase the energy efficiency of a mobile network. For instance, it was studied in [6] that there is an unequal distribution of traffic. 80 % of the data traffic is conducted only by 30 % of the base stations. This happens because to guarantee the most coverage, sometimes base stations have to be placed in areas least populated. To overcome this problem recent advancements in the transceiver technology make it possible for a deep sleep state where energy consumption is drastically reduced [7]. To complement this, artificial intelligence solutions have been proposed to smartly turn ON and OFF the base station or transfer data traffic from one base station to the other.

With this in mind, researching new ways to maximize overall efficiency when subject to high envelope fluctuation signals is of paramount importance. A new solution called Quantized Digital Amplifier (QDA) is exposed and compared with other techniques. More specifically, this new solution is analyzed from a signal processing standpoint and it is deeply explored from an electronics standpoint.

1.2 Contributions of this work

This thesis exposes a new solution called QDA. This novel technique can potentially set a new record for the maximum efficiency achievable. By making a signal processing analysis and electronic analysis of the power amplifier, the reader can better understand the impact of this new solution and understand its advantages and disadvantages compared with other existing efficiency enhancement techniques.
Furthermore, with the development of an innovative PA design kit, a power amplifier can be designed, under the technology node restrictions, for any frequency and output power requirement. During this process, the reader will be able to understand practically all the intricacies behind the design and simulation of a power amplifier and start to get familiar with the challenges of integrated circuitry design.

1.3 Thesis Layout

This work starts by introducing OFDM. The advantages of this frequency division multiplexing technique will justify the need to use this technique in modern mobile communications. The disadvantages of this technique are explored and serve as a prelude for the next chapter. The next two sections outline the characterization of a power amplifier and the metrics to characterize it. With this information, understanding why overall efficiency is so low is a small step. With the familiarization with PAs characteristics, in the next section, the basic topologies of power amplifiers are outlined, such as linear and nonlinear amplifiers. At the end of this chapter, the reader will know the limitations of linear amplifiers and why non-linear amplifiers are the way to go.

With a low PA efficiency due to the input of a high envelope fluctuation signal, techniques to improve the linearity and maximum efficiency are exposed. Based on the advantages and disadvantages of the techniques presented, a new solution called QDA is exposed. The details and intricacies of this novelty technique are explored from a signal standpoint and an electronics standpoint. Also, the developed design for an initial QDA prototype is shortly presented and compared with existing techniques.

The thesis could end here but it would fail to address with some diligence and elegance the most important issue, the power amplifier. Despite its characterization being explored in previous chapters, what does it take to design one and more interestingly what does it take to design one fully integrated? After all, whoever wins the power efficiency race has to maximize the power amplifier performance and the power combining performance. Picking the power amplifier performance as a mission then the next chapters emerge. The class E power amplifier topology is studied considering a relatively small Direct Current (DC) bias inductor. This allows for the full integration on the chip of the PA. An innovative design kit will be developed in order to understand what are the factors that condition the development of PA, more specifically a class E PA. As a proof of concept four power amplifiers will be developed for different output power levels. Within this design, a methodology to get the best PAE given real components is proposed. This methodology requires some knowledge of impedance matching and integrated inductors. Last but not least, given the fact that a Field Programmable Gate Array (FPGA) does not have the power capability to turn on the PA fast enough, power amplifier drivers must be explored. This will be a relatively brief chapter where one driver topology is seen and designed.

2

Theoretical Background

2.1 Orthogonal Frequency Division Multiplexing

2.1.1 Introduction

Orthogonal Frequency Division Multiplexing (OFDM) is a modulation technique with spectral efficiency gains and good performance on fading channels. This concept is not new and was used in Asymmetric Digital Subscriber Line (ADSL) communications. With the hardware development and efficient algorithms implementation, nowadays it is widely used in 4G mobile communications and will be used in 5G due to its hardware simplicity and Multiple-input/multiple-out (MIMO) compatibility. The goal of this chapter is to illustrate the many advantages when compared to a single-carrier solution and the disadvantages. One can say with a high degree of confidence that the continuous investigation of efficiency enhancement techniques of power amplifiers is due to one of the major problems of OFDM. This chapter is organized as follows: First, a signal and schematic description of OFDM will be given. Then an explanation of the cyclic prefix and how it helps to eliminate Inter Symbolic Interference (ISI) will be given. Last but not least, as this thesis is focused on improving the overall Power Amplifier (PA) efficiency, one must understand where the high envelope fluctuation of OFDM comes from.

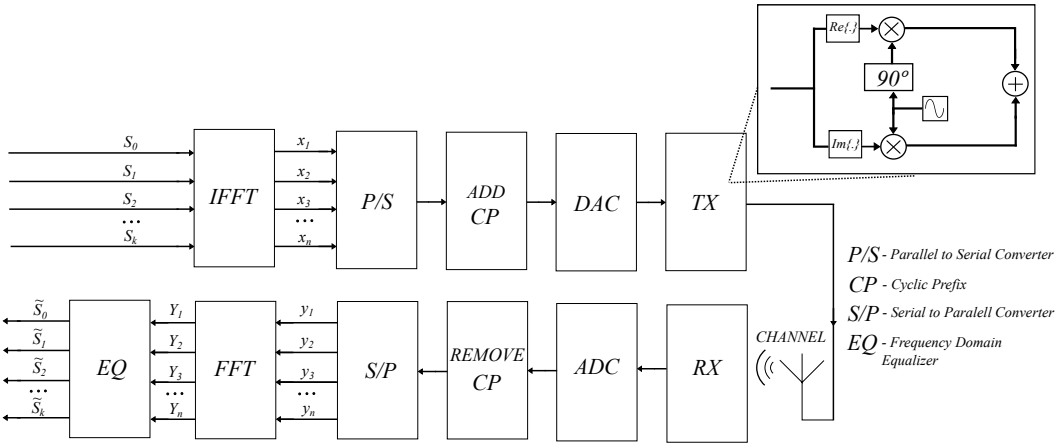


Figure 2.1: OFDM Transmitter and Receiver Schematic.

2.1.2 Signal Characterization

A generic frequency division multiplexing technique can be described, in the frequency domain, as follows

$$S(f) = \sum_{k=-\frac{N}{2}}^{k=\frac{N}{2}} S_k \cdot R(f - k \cdot F) \ , \tag{2.1}$$

where N represents the number of subcarriers, S_k the k_{th} symbol and F the spacing between consecutive carriers. In traditional Frequency Divsion Multiplexing (FDM), F must be bigger than signal bandwidth because of the spectral leakage one user might incur in another. This happens because the filters are not ideal. In OFDM, R is equal to the support signal. This can be better understood by observing Fig. 2.2. The particular choice of F makes the subcarriers orthogonal between each other. This means that the condition in equation (2.2) is met. Intuitively this means that at each integer multiple of F, all of the carriers are null except the one carrier centred in that value.

$$\int_{-\infty}^{\infty} R(f - kF) \cdot R^*(f - k'F) df = 0 \ , \ k \neq k' \ . \tag{2.2}$$

In the time domain, the OFDM signal is simply obtained by doing the inverse Fourier transform of equation (2.1) and then considering multiple OFDM symbols we get the following expression

$$s(t) = \sum_{l=0}^{\infty} \sum_{k=-\frac{N}{2}}^{\frac{N}{2}} S_k \cdot r(t) \cdot e^{j2\pi f_k (t - lT_{sym})} \ , \tag{2.3}$$

where $f_k = \frac{k}{T_{sym}}$. By analyzing equation (2.3), one possible hardware implementation would be to add $\frac{N}{2}$ IQ modulators in parallel. It is understandable that for a high number of subcarriers this implementation is prohibitive. Instead, if the signal is sampled at $t = l \cdot T_{sym} + nT$ where T is equal to T_{sym}/N, the continuous time signal in the equation in (2.3) can be re-written to a discrete version.

$$x_n = \sum_{k=0}^{\frac{N}{2}-1} S_k \cdot e^{j2\pi k \cdot \frac{n}{N}} \ . \tag{2.4}$$

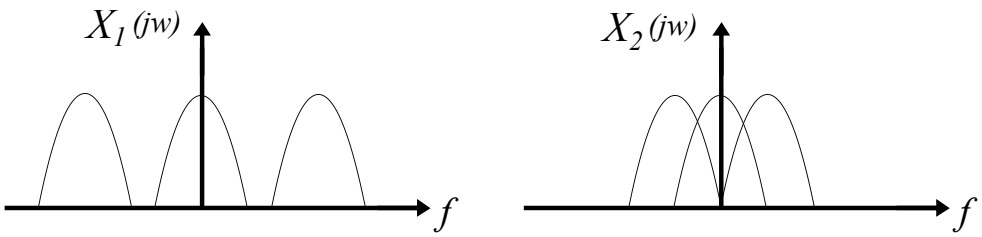
This is precisely the inverse Fourier transform. This means that hardware-wise, the implementation of OFDM at the receiver could be done using a relatively inexpensive Inverse Fast Fourier Transform (IFFT) block. At the transmitter side since there is orthogonality between subcarriers integrating the input signal with the k_{th} carrier will output the k_{th} symbol. In a discrete form, the integral becomes a summation and for a generic carrier,

we get equation 2.5.

$$\begin{aligned} Y[k] &= \sum_{n=0}^{N-1} y[n] \cdot e^{-j \cdot 2\pi k \cdot \frac{n}{N}} \\ &= \sum_{n=0}^{N-1} \left\{ \frac{1}{N} \sum_{i=0}^{N-1} S_i \cdot e^{j 2\pi i \cdot \frac{n}{N}} \right\} \cdot e^{-j \cdot 2\pi k \cdot \frac{n}{N}} \\ &= \frac{1}{N} \cdot \sum_{i=0}^{N-1} S_i \sum_{n=0}^{N-1} e^{-j \cdot 2\pi \cdot (i-k) \cdot \frac{n}{N}} \ . \end{aligned} \tag{2.5}$$

Note that $\sum_{n=0}^{N-1} e^{-j \cdot 2\pi \cdot (i-k) \cdot \frac{n}{N}}$ is the Fourier transform of the constant function, which is equal to $\delta(i-k)$. Replacing that in the expression above, we get.

$$Y[k] = \frac{1}{N} \cdot \sum_{i=0}^{N-1} S_i \cdot \delta(i-k) = S_k \ . \tag{2.6}$$



(a) (b)

Figure 2.2: (a) Traditional FDM ; (b) Orthogonal FDM

2.1.3 Cyclic Prefix

The duration of a OFDM symbol is N times greater than the input symbol time. This means that the OFDM signal suffers less inter-symbolic interference than a single carrier solution. To completely eliminate ISI, a guard interval with a time duration corresponding to the coherent time of the channel considered is used. Usually, a cyclic prefix is used where a set of final samples of each symbol is added to the beginning of the symbol. Using a cyclic prefix makes the convolution between channel samples and signal samples, a circular kind. This allows for the following relation

$$Y[k] = H[k] \cdot X[k] + Z[k] \ , \tag{2.7}$$

where H is the frequency component of the channel at the frequency k. X is the symbol value at the frequency k. This is quite useful because if the coherent band of the channel is lower than each carrier band, the equalization is quite simple.

2.1.4 Envelope characterization

Looking at equation (2.3) it is clear that at each time sample, the signal is the result of summing different sinusoids with different amplitudes and phases. This results in a signal

whose envelope fluctuates quite considerably. To measure this fluctuation a metric called Peak-To-Mean Envelope Power Ratio (PMEPR), defined by equation (2.8), is used.

$$PMEPR = \frac{R^2(P)}{\bar{P}} \ . \tag{2.8}$$

$\bar{P}$ is the average power and R(P) is the envelope value that is exceeded with probability P. The numerator of this metric could be replaced by the peak power of the OFDM signal. That would be the traditional form of this metric, so to speak. However, the peak power value grows with the number of sub-carriers and that leads to a high value of PMEPR. Additionally, the probability of the occurrence of a peak taking place is relatively low. As so, the contribution of the peak for the overall efficiency is almost insignificant. By using equation (2.9), an approximated peak envelope can be set. Beyond this envelope value, the probability can be as low as desirable. For example, a reasonable value for P is 10^{-3} [8]. For a high number of sub-carriers, the distribution of the complex envelope's real and imaginary parts approaches a Gaussian distribution. This implies that the envelope module has a Rayleigh distribution and the phase a uniform distribution. The probability density function of the Rayleigh distribution is given by the following

$$p\,(R) = \frac{R}{\sigma^2} \cdot e^{-\frac{R^2}{2 \cdot \sigma^2}} \ , \tag{2.9}$$

where R is the module of the complex envelope of the OFDM signal. σ^2 represents the average power. The probability of the envelope amplitude exceeding r is given by equation (2.10)

$$P = Prob\,(R > r) = \int_r^{+\infty} p(R)\, dR = e^{-\frac{X^2}{2 \cdot \sigma^2}} \ . \tag{2.10}$$

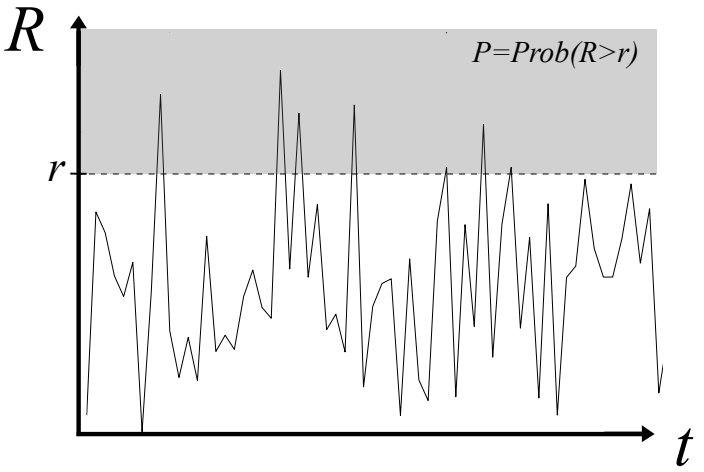


Figure 2.3: OFDM Envelope Fluctuation.

2.2 Power Amplifier Modelling

2.2.1 Introduction

The ideal power amplifier can be described with a linear function. Meaning that independently of the input power the output power will always be a scalar of the input power. However, in reality, all electronic components are non-linear. This is quite a bold statement but if one starts to see why we consider the components linear, one will conclude that it is a mere approximation. For instance, the small signal analysis of the transistor is nothing more and nothing less of a linearization around the quiescent point. There are two main types of non-linearity: strong and weak. The weak non-linearity is usually a non-linearity that can be expressed by a Taylor series with actually few coefficients. An example of this weak non-linearity is the quadratic current description of the transistor when the latter is in saturation. A strong non-linearity is applicable when either the Taylor series presents a prohibitive number of coefficients or when it is preferable to define the non-linearity as a piece-wise function. Usually, this type of non-linearity is tackled by using advanced techniques such as harmonic balance. A very good example is the current description when the transistor transients between the triode region and saturation region. In our case, only the weak non-linearity will be considered. The power series of a weak non-linear system can be described by equation (2.11)

$$y(t) = a_1 \cdot x(t) + a_2 \cdot x(t)^2 + a_3 \cdot x(t)^3 \ . \tag{2.11}$$

Working with power series can quickly become a cumbersome task. It has been shown that the interest is definitely the envelope and the phase of the input signal. As so, creating abstractions from the Taylor series is a must. To start with, let's analyze the Cartesian memoryless non-linear characteristic. The band-pass complex envelope can be described by the following equation

$$x(t) = R(t) \cdot e^{j \cdot \psi(t)} \ , \tag{2.12}$$

where $\psi(t) = \theta(t) + 2\pi \cdot f_c \cdot t$ It can be proven [8] that the output complex envelope of the non-linear system is obtained by applying a non-linear function to the real and imaginary part of the input complex envelope.

$$y(t) = g_I(R(t) \cdot cos(\psi(t))) + j \cdot g_Q(R(t) \cdot sen(\psi(t))) \ . \tag{2.13}$$

The complex envelope is a periodic function. As a consequence, it can be re-written as a Fourier series

$$y(t) = \sum_{l=-\infty}^{+\infty} c(R(t)) \cdot e^{j \cdot l \cdot \psi(t)} \ . \tag{2.14}$$

Admitting the existence of a filter that only keeps the fundamental component and removes all the other components the output of a non-linear system can be described as follows

$$y(t) = f(R) \cdot e^{j \cdot l \cdot \psi(t)} \ , \tag{2.15}$$

where $f(R) = 2 \cdot Re(c(R(t))) + 2 \cdot j \cdot Im(c(R(t)))$. In polar format f(R) can be described by equation (2.16)

$$f(R) = A(R) \cdot e^{j \cdot (\theta(R))} \ . \tag{2.16}$$

The amplitude of $f(R)$ represents the AM/AM conversion, and the phase represents the AM/PM conversion. The AM/PM conversion will be useful to characterize some PA circuits enhancements. As so, it is really important to know, based on a PMEPR value if the amplifier is going to distort the signal.

2.2.2 AM-AM Conversion

It is useful to quantify this compression effect in a general way, independent of the specific transistor in use. There are models that describe the variation of output phase with input amplitude called AM/PM models and models that describe the variation of output amplitude with input amplitude called AM/AM models. A very useful AM/AM model is the Rapp model that can be observed in Fig. 2.4. The AM/AM characteristic is described by equation (2.17).

$$A(r) = \frac{r}{\left(1 + \left(\frac{r}{S_{sat}}\right)^{2p}\right)^{\frac{1}{2 \cdot p}}} \ . \tag{2.17}$$

S_{sat} is the saturation value of the amplifier and p is a parameter that controls the non-linearity near the compression point.

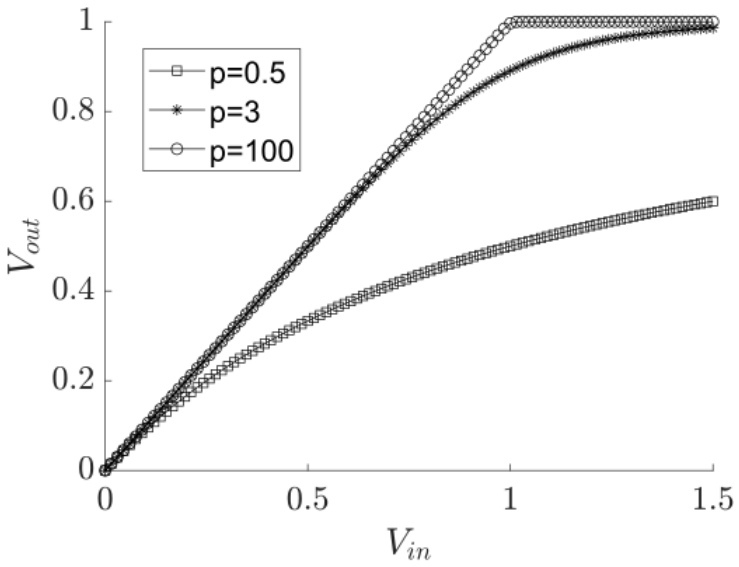


Figure 2.4: Rapp model for different values of p.

2.3 Metrics to rank a Power Amplifier

2.3.1 Drain Efficiency

This metric expresses the quotient between the output power and the power supplied by the power supply. It is quite useful when one wants to know how much of the energy supplied is actually being dissipated on the transistor or non-ideal components. The drain efficiency is given by the following formula

$$\eta = \frac{P_{out}}{P_{DC}} \, . \tag{2.18}$$

2.3.2 Power Added Efficiency

To complement the metric, drain efficiency, there is a metric called Power Added Efficiency (PAE). This is a more suitable metric to be used as a figure of merit of a PA topology. Because this metric tells us how much power we need to give to the gate of the transistor to get a specific output power. In other words, it is not only important to get a good drain efficiency, but it is also important to have a big gain in order to have a higher performance. These two factors can be expressed by the following equation

$$PAE = \frac{P_{out} - \frac{P_{out}}{G}}{P_{DC}} = \frac{P_{out}}{P_{DC}} \cdot \left(1 - \frac{1}{G}\right) \, , \tag{2.19}$$

where $G = \frac{P_{out}}{P_{in}}$. When the gain is relatively big, the power-added efficiency is equivalent to the drain efficiency. Also, there can be advantages in terms of the maximum value of PAE achievable if the drain efficiency drops slightly but the gain increases.

2.4 Basic Power Amplifier Topologies

2.4.1 Linear Power Amplifiers

The use of a linear Power Amplifier is not new and dates back to 1941 [9], where the optimum conditions of a linear PA were analyzed. This type of PA can be used in audio amplification such as HiFi audio where the good linearity of the power amplifier plays a crucial role in delivering a clean signal to the speakers. This type of amplifier is called linear because of the harmonic purity at the output. This term, as the reader will see, is better used in a specific class of linear power amplifiers.

In Linear Power Amplifiers, there are three major classes: A, B and C. The class A PA is best in terms of linearity as it will be explained. The figure of a generic linear PA can be observed in Fig 2.5. It consists of a transistor operating equivalently as a current source. Then it has a choke inductor which forces a DC voltage, in the drain port of the transistor, equal to V_{DD}. This doubles the maximum efficiency. Then there is the LC tank. This tank is working as a band-pass filter. For a high enough quality factor, only the fundamental harmonic is delivered to the output resistance R. This schematic is applicable to all the power amplifier classes. What changes is the gate polarization? If all of the input signals are above the threshold voltage then we have a class A regime. If the signal is centred at the threshold voltage then we have a class B regime. The class C regime happens when more than 50% of the input signal is below the threshold voltage. This section was inspired by Kazimierczuk's book [10].

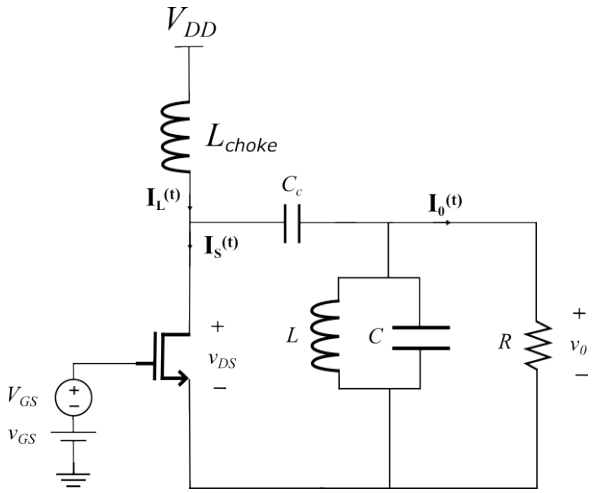


Figure 2.5: Linear Power Amplifiers.

2.4.1.1 Class A

This class of amplifiers is used when a high degree of linearity is required. The amplifier consists of a transistor, an LC tank at the output and a choke coil. The latter is extremely important as it doubles the maximum efficiency possible if, for example, we put a resistor instead of the coil. A DC decoupling capacity C_c is also used.

The transistor in this class is saturated hence it operates as a current source. The transistor is always on which means that the voltage applied to the gate of the transistor must be always greater than the threshold voltage. Unlike the Low Noise Amplifier (LNA) or the mixer where it is possible to apply a small signal regime and thus simplify the analysis, in this case, it will not be possible. This is due to the fact that we have a signal at the gate whose amplitude is frankly greater than the threshold voltage of the transistor. The LC tank, considering that it has a relatively high-quality factor, will only allow the flow of current whose frequency is equal to the input frequency. The LC tank at frequencies different than the resonant frequency will behave like a short circuit therefore no ac current can flow. On the other hand, at the resonant frequency, the LC tank behaves like an open circuit so ac current can flow.

The input voltage applied at the gate of the transistor can be expressed as $v_{GS} = V_{GS} + v_{gs} = V_{GS} + V_{gs} \cdot \cos(wt)$. The DC component of this voltage forces a DC regime on the transistor leading to a DC current through the drain-source channel. The sinusoidal voltage applied at the gate produces a sinusoidal current. If the quality factor of the tank is relatively high, the drain voltage and current can be expressed as follows

$$V_D = V_{DD} + v_D \cdot cos(w \cdot t) \ , \tag{2.20}$$

$$I_D = I_{DC} + i_D \cdot cos(w \cdot t) \ , \tag{2.21}$$

What values do i_d and v_d take? The answer must be such that allows maximization of the drain efficiency. The DC power given the power supply is evident by equations (2.20) and (2.21) and is given by

$$P_{DC} = V_{DD} \cdot I_{DC} \ , \tag{2.22}$$

Since the tank only allows to let the fundamental harmonic through, the output power is given as follows

$$P_{out} = \frac{1}{2} \cdot v_D \cdot i_D \ , \tag{2.23}$$

The drain efficiency is given by equation (2.24).

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{1}{2} \cdot \frac{v_D \cdot i_D}{V_{DD} \cdot I_{DC}} \ . \tag{2.24}$$

Since the goal is to maximize this value, one has to find a relation between the output voltage and current with the DC current and voltage. In terms of sinusoidal current, since the input gate voltage cannot fall below the threshold voltage, the maximum sinusoidal current amplitude is equal to I_{DC}. Relative to the output voltage, since the transistor needs

to stay in saturation, the maximum voltage is V_{DD} (assuming a really small saturation voltage). This being said, the maximum drain efficiency is effectively **50 %**. This means that in half of a period the energy is spent on the transistor in the form of heating and in the other half the energy is delivered to the load. In reality, the value is lower because the transistor in order to operate in saturation, its drain-source voltage must always be higher than the maximum saturation value. The drain efficiency can then be reformulated in the following equation

$$\eta_D = \frac{1}{2} \cdot \left(1 - \frac{2 \cdot (V_{GS} - V_{TH})}{V_{DC}}\right) < 50\% \ . \tag{2.25}$$

2.4.1.2 Class B

The class B amplifier has the same basic operation as class A in the way that the transistor works as a current source. In the following analysis, the quadratic model will be used to describe the transistor working in the class B regime.

In class B, the transistor is ON half of the time and OFF the other half. At first glance, this might not bring any clear advantages. It will be seen, that there is a way to change the harmonic value of the DC component and the fundamental to increase the ratio between the output power and DC power. Being OFF half of the time suggests that the input wave is half of the time below the threshold voltage. The input voltage is precisely given as follows

$$v_{GS} = V_{TH} + v_{gs} = V_{TH} + V_{gs} \cdot \cos(wt) \ , \tag{2.26}$$

Using the quadratic formula one can describe the current behaviour during a period by the following branch function

$$i_d(t) = \begin{cases} \frac{1}{2} \cdot K_n \cdot \frac{W}{L} \cdot \left[V_{TH} + V_{gs} \cdot cos(w \cdot t) - V_{TH}\right]^2 & \frac{-\pi}{2} \leq wt \leq \frac{\pi}{2} \\ 0 & \frac{\pi}{2} \leq wt \leq \frac{3\pi}{2} \end{cases}$$

Looking at the branch function, two observations are necessary. The first is that this branch function assumes an infinitesimal switch time between states. There is no such thing. Then, the current when the transistor is OFF despite being very small is not entirely 0. It is a good approximation to consider it as 0. For simplicity's sake, consider a new variable, I_{DM} whose value can be described in equation (2.27). This variable represents the maximum current through the drain-source channel of the transistor.

$$I_{DM} = \frac{1}{2} \cdot K_n \cdot \frac{W}{L} \cdot V_{gs}^2 \ . \tag{2.27}$$

With the description of the current in a branch even function, the value of the DC harmonic and the fundamental harmonic using the Fourier transform. are given as

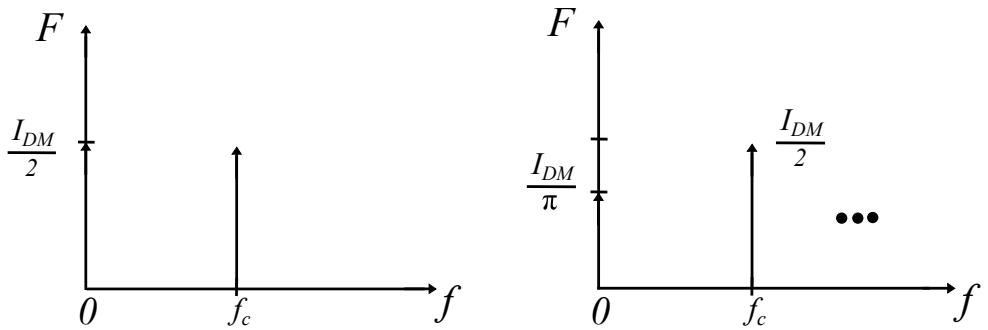
$$I_{DC} = \frac{1}{2 \cdot \pi} \cdot \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} id \ d\,(wt) = \frac{I_{DM}}{2 \cdot \pi} \cdot \left[\sin\,(wt)\right]_{-\frac{\pi}{2}}^{\frac{\pi}{2}} = \frac{I_{DM}}{\pi} \ , \tag{2.28}$$

$$I_m = \frac{1}{\pi} \cdot \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} id \cdot \cos\,(wt) \ d\,(wt) = \frac{I_{DM}}{2} \ , \tag{2.29}$$

With these two quantities, the drain efficiency can be calculated using equation (2.30)

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{1}{2}\frac{v_m \cdot i_m}{V_{DD} \cdot I_{DC}} = \frac{1}{2} \cdot \frac{V_{DD} \cdot \frac{I_{DM}}{2}}{V_{DD} \cdot \frac{I_{DM}}{\pi}} = \frac{\pi}{4} \, . \tag{2.30}$$

In comparison with the class A PA, despite the output current is the same the DC current is reduced which in turn increases the drain efficiency. Reminding the less attentive reader, in class A the output current can be expressed like the maximum drain current divided by two and the DC current follows suit. This harmonic relationship can be observed graphically in Fig. 2.6. Either in class A or in class B it is assumed that the output resistor is such that creates an output voltage whose amplitude is equal to V_{DD}. In reality, this never happens because the transistor when it is ON must be in saturation for the current description given above to be valid. Now, can we push this ratio up? Meaning, if the transistor is more time OFF than ON, does it brings benefits to the drain efficiency? This alluring question will be explored in the next subsection



(a) Class A (b) Class B

Figure 2.6: Comparison between class A and class B from a harmonic point of view.

2.4.1.3 Class C

It is now possible to generalize the results for when the transistor is more time OFF than ON. As mentioned earlier, the voltage applied to the gate is given by equation (2.31)

$$v_{GS} = V_{GS} + V_{gsm} \cdot cos(wt) \, . \tag{2.31}$$

Analyzing the equation (2.31), it is possible to see that the time the input voltage is above V_{TH} can be varied by changing the value of V_{GS} or V_{gsm}. With this idea in mind, one can define a quantity called conduction angle. The conduction angle, θ,is determined by finding the angle that causes the input gate voltage to be equal to V_{TH}.

$$\theta = 2 \cdot \cos^{-1} \frac{V_{TH} - V_{GS}}{V_{gsm}} \tag{2.32}$$

The conduction angle represents then the amount of angle that the input voltage is above V_{TH}. In other terms, the amount of time the transistor is ON, ϑ, can be found by doing the

following

$$\vartheta = \frac{\theta}{2 \cdot \pi} \cdot T \ , \tag{2.33}$$

where T represents the period of the input signal. This can also be seen graphically in Fig. 2.7. Bridging with the previous subsection, when $V_{TH} = V_{GS}$ the transistor is in a class B

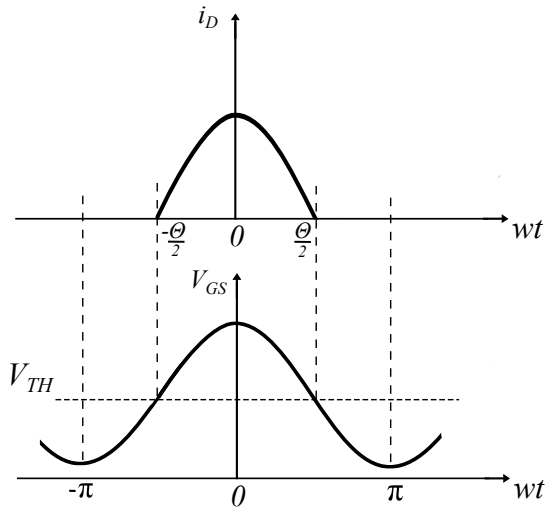


Figure 2.7: Gate input voltage and drain current of a class C Power Amplifier.

amplifier situation. When $V_{TH} - V_{GS} > 0$ the transistor is in a class C amplifier situation. Assuming a quadratic relationship between the drain current and the voltage applied to the gate, the drain current temporal evolution can be described as a branch function

$$i_d(t) = \begin{cases} I_{DM} \cdot \frac{\cos(wt) - \cos(\theta)}{1 - \cos(\theta)} & \frac{-\theta}{2} \leq wt \leq \frac{\theta}{2} \\ 0 & \frac{\theta}{2} \leq wt \leq 2 \cdot \pi - \frac{\theta}{2} \end{cases}$$

where the conduction angle is equal to θ and $I_{DM} = \frac{1}{2} \cdot K_n \cdot \frac{W}{L} \cdot V_{gs}$. The procedure to determine the fundamental harmonic and the value of the DC component follows the same rationale taken in the study of class B. Using the Fourier transform, the dc component of the drain current is given by

$$I_{DC} = I_{DM} \cdot \frac{sin(\frac{\theta}{2}) - \frac{\theta}{2} \cdot cos(\frac{\theta}{2})}{\pi(1 - cos(\frac{\theta}{2}))} = I_{DM} \cdot \alpha_0 \ . \tag{2.34}$$

In the same way, the fundamental harmonic amplitude can be obtained through the following equation

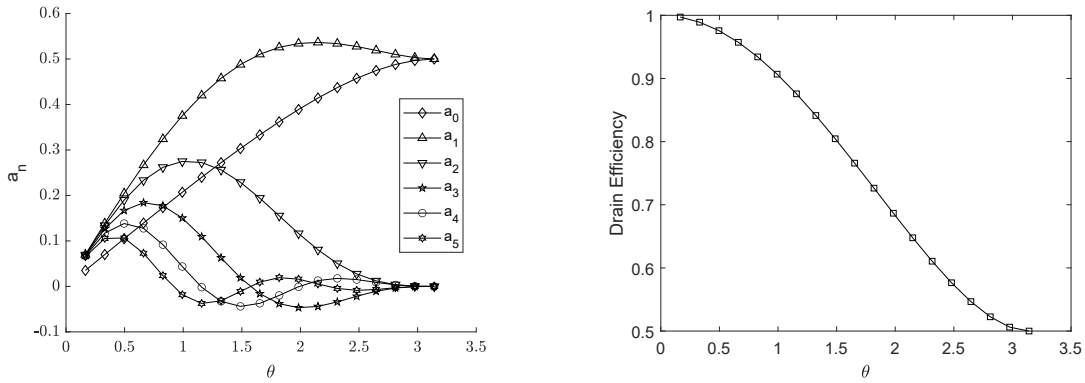
$$I_m = I_{DM} \cdot \frac{\frac{\theta}{2} - sin\left(\frac{\theta}{2}\right) \cdot cos\left(\frac{\theta}{2}\right)}{\pi\left(1 - cos\left(\frac{\theta}{2}\right)\right)} \ . \tag{2.35}$$

With these two quantities, the drain efficiency can be formulated as follows

$$\eta_D = \frac{P_0}{P_{DC}} = \frac{1}{2} \cdot \frac{\theta - \sin(\theta) \cdot \cos(\theta)}{\sin(\theta) - \theta \cdot \cos(\theta)} \ . \tag{2.36}$$

The normalized value of the harmonics for each conduction angle can be observed in Fig. 2.8 (a). As they are normalized, the ratio between the first harmonic and DC component

gives, for each conduction angle, a ratio which is directly proportional to the drain efficiency apart from a factor of 0.5. With that in mind, Fig. 2.8 (b) is given.



(a) Normalized harmonic values variation with the conduction angle

(b) Drain efficiency variation with the conduction angle

Figure 2.8: General view of Linear Power Amplifiers.

2.4.2 Non-Linear Amplifiers

As seen in previous chapters, linear power amplifiers have relatively low peak efficiency. Drain efficiency can be written as follows

$$\eta = 1 - \frac{P_D}{P_{DC}} \ . \tag{2.37}$$

The efficiency is intended to be 1, so the power consumed by the drain must ideally be 0. To know which criteria this occurs, the drain power definition is analyzed in equation (2.38).

$$P_D = \frac{1}{T} \cdot \int i_d\,(t) \cdot v_d\,(t)\ dt \ . \tag{2.38}$$

Power is 0 if the transistor draws current but does not create a potential difference across its terminals. With this idea in mind, topologies such as the class D or class E emerge. One of the class D advantages is that the maximum drain source voltage of each transistor is roughly the nominal supply voltage. On the other hand, this topology has some losses when the transistors turn ON and OFF and requires additional circuitry to generate the input waves. The next subsection explains the class E topology in further detail.

2.4.2.1 Class E

This class was first introduced by Nathan Sokal and his son Alan Sokal in 1975 [11]. To this day it is still widely used in power amplifier design. This happens because this amplifier's main goal is to reduce the power losses when the transistor switches on or when the transistor switches OFF. Compared to a class D amplifier, this alone represents an advantage because class D has losses both when the transistor turns ON and turns OFF.

There are two main class E topologies. The difference lies on where is the reduction of power losses. If it is when the transistor turns ON, then the topology is called class E voltage switching. If it is when the transistor turns OFF, then the topology is called class E current switching. In this thesis, only the first will be carefully designed.

The schematic of the class E voltage switching can be observed in Fig. 2.11. So how does this circuit works? To simplify the following analysis, consider the following restrictions: The on-resistance of the transistor is extremely small or null, the inductor (L1) is a choke inductor, and the quality factor of the output tank is high enough to guarantee only the fundamental harmonic to exist and the duty cycle is 50%.

When the transistor is ON, the voltage drop between the capacitor is 0 meaning that there is no charging and discharging of the capacitor. Consequently, all the sinusoidal current from the tank and the DC choke current flow through the switching transistor. When the transistor turns OFF, all the current now flows through the capacitor. Given the sinusoidal nature of the tank current, there will be some times when the capacitor is charging and other times when the capacitor will be discharging. The criteria for how this happens and at what time this happens is the definition of the turn-on condition. In other

words, when the transistor turns ON we want the voltage drop on the capacitor to be 0 so that there is no current flowing through the transistor. Besides that the capacitor must be fully discharged so that there are no charges going to the transistor channel, implying power losses. This happens if the voltage derivative is 0. A more illustrative explanation can be seen through the Fig.'s 2.9 and 2.10.

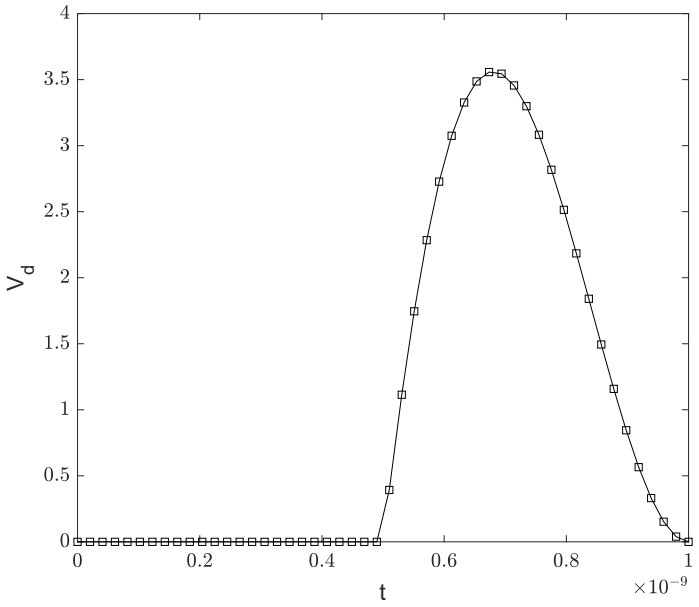
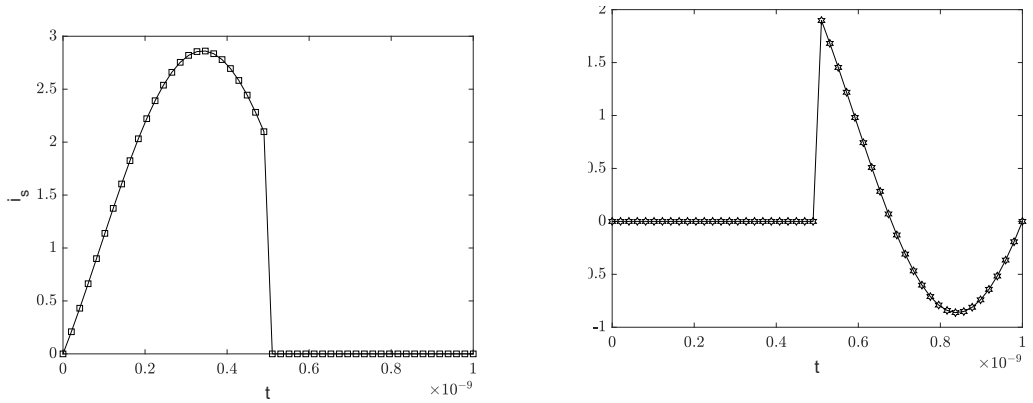


Figure 2.9: Time evolution of the voltage drop through the shunt capacitor.



(a) (b)

Figure 2.10: (a) Time evolution of the current through the switch ; (b) Time evolution of the current through the capacitor

At the turn ON time, if one wants the voltage derivative to be 0, then there must be a phase shift on the sinusoidal current of the tank. This entails an additional reactive part. In other words, the tank must be designed for a frequency bigger or lower than the working frequency. How to know which way to design it? Let's assume that the tank

current is given by the following.

$$i = I_m \cdot \sin(wt + \phi) \ . \tag{2.39}$$

Then the voltage drop at the output resistance comes naturally

$$v_r = V_{RM} \cdot \sin(wt + \phi) \ . \tag{2.40}$$

The voltage drop across the reactance is given as

$$v_l = \pm V_{LM} \cdot \cos(wt + \phi) \ . \tag{2.41}$$

The sign will be positive if the reactance is an inductor and negative if it is a capacitor. Looking at the resonant frequency formula one can conclude that if the additional reactance represents an inductor then the resonance frequency of the tank is lower than the working frequency. If the additional reactance represents a capacitor then the resonance frequency of the tank is higher than the working frequency.

$$f_t = \frac{1}{2 \cdot \pi \sqrt{LC}} \ . \tag{2.42}$$

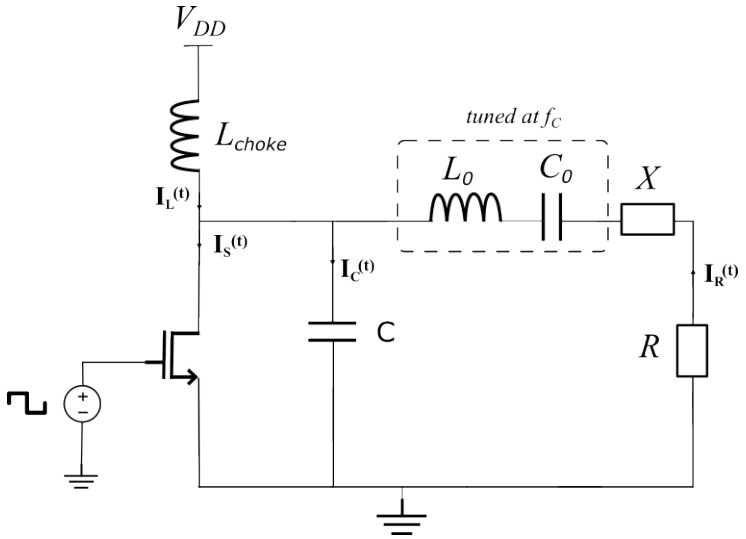


Figure 2.11: Class E schematic.

3

Power amplifier performance enhancement techniques

3.1 Power amplifier linearity enhancement techniques

3.1.1 Introduction

As it was seen the transfer function of a power amplifier is not linear. As a result, if the input signal power is closer to the compression point, there will be distortion. To fix this problem the power amplifier is configured to work in back-off, decreasing substantially the overall efficiency.

Linearization techniques allow to reduce the back-off needed hence increasing efficiency. There are many techniques to increase the Power Amplifier (PA) linearity. Pre-distortion, feed-forward, will be analyzed in the next section. Knowing a relatively accurate model of the power amplifier allows to apply a concept called pre-distortion. It is crucial to emphasize that this linearization technique improves linearity and as a consequence can improve the efficiency. For example, consider the response of a Rapp Model with a p parameters equal to 3 It is clear that the linear zone is only a small fraction of the input spectrum. As a result, a varying envelope signal with a high Peak-To-Mean Envelope Power Ratio (PMEPR) would surely be distorted. The problem could be fixed if a good estimation was made on the PA response. Would there be any way to increase efficiency with this method? Note that in saturation, no matter what the response of the pre-distorter may be, the signal would always saturate.

3.1.2 Pre-distortion

Pre-distortion, in short, is a technique that applies the inverse of the power amplifier transfer function. This block as it can be seen in the Fig.3.1 is right before the PA. Since the RF amplifier presents gain and phase compression, the inverse of the PA transfer function translates into a circuit that would exhibit a gain and phase expansion. The main drawback of distortion is that the transfer function of a power amplifier is time-dependent. This dependency arises from power supply variations, temperature variations, and the

intrinsic behaviour of the transistor. To overcome this problem, a feedback loop may be required to periodically adapt the pre-distortion transfer function. How to implement the pre-distorter block? One way could be by using a power amplifier whose Direct Current (DC) bias is relatively higher than the main power amplifier. That solution will degrade the overall efficiency despite linearizing the overall circuit. Another solution is using linear feedback. It can be shown that when an amplifier is configured in a negative feedback configuration, the coefficient related to the second-order non-linearity is attenuated by the gain product. One imminent problem with this approach is that the operational amplifier does not have a microwave bandwidth and drive capability. With the advancement of digital signal processing, the pre-distortion can be made digitally with look-up tables. For more information on digital pre-distortion consult [12].

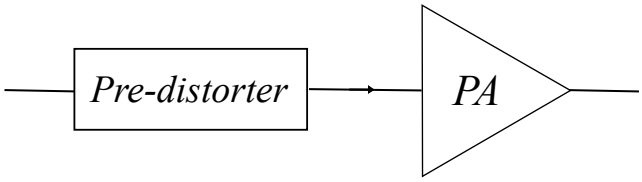


Figure 3.1: Pre-distortion concept.

3.1.3 Feed-Forward

Rather than pre-distorting the signal, if somehow the non-linearity of the power amplifier is measured, it could be subtracted to create an error-free technique. That is called feed-forward linearization. This technique consists on the cancellation of the distortion signal. The block diagram of a basic feed-forward linearization technique can be seen in Fig. 3.2. The output voltage of a power amplifier can be expressed in two parts. A useful part is a signal we want to transmit and an error voltage like it can be seen in equation (3.1)

$$v_p = A_{PA} \cdot v_{in} + v_d \ . \tag{3.1}$$

The block diagram of a basic feed-forward linearization technique can be seen in the figure below. The output of the error amplifier is given as follows

$$v_{eo} = A_{PA} \cdot (v_{in} + \frac{v_d}{A_{PA}} - v_{in}) = v_d \ . \tag{3.2}$$

The output can then be expressed using equation (3.3).

$$v_{out} = v_p - v_{eo} = A_{PA} \cdot v_{in} + v_d - v_d = A_{PA} \cdot v_{in} \ . \tag{3.3}$$

As it can be seen in equation (3.3) the distortion signal is perfectly cancelled. This technique also suppresses the noise added to the signal in the main power amplifier. The main disadvantage of this technique is the gain mismatch and the phase delay mismatch in the signal branches. If the error amplifier does not monitor the changes in A_v then the error voltage is not suppressed. The phase shifts can be compensated by the introduction of

delay elements in both branches. The delay elements introduce loss if they are passive or distortion if they are active. Also, the implementation of wide-band delay is a difficult task.

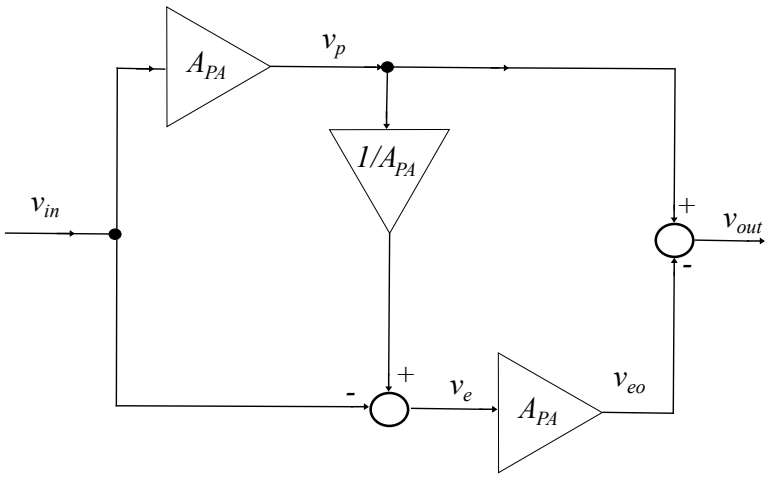


Figure 3.2: Feed-forward concept

3.2 Power amplifier efficiency enhancement techniques

3.2.1 Introduction

The linearization enhancement techniques can't increase the efficiency beyond the maximum efficiency of the power amplifier. This means that the use of linearization techniques represents some improvement but only to correct the non-linearity problem of the PA. That's where efficiency techniques come in. By putting the PA always operating in the maximum efficiency point, the best efficiency possible can be obtained for each and any signal input amplitude.

3.2.2 Envelope Tracking Technique

The main goal of envelope tracking is to adaptively change the bias level of the power amplifier so that this can operate at the highest efficiency possible. As it was seen earlier, in the linear class of amplifiers the max efficiency is relatively low. Adding to this, the input signal presents a variable envelope. This leads to compression of the output signal or a low long-term average efficiency. This technique tries to solve that problem by adaptively changing the DC bias point of the amplifier. This way, in theory, the amplifier can operate always at its maximum efficiency. As it was seen in the Class A section, the drain efficiency is given by the following expression.

$$\eta_D = \frac{P_{DS}(t)}{P_{DC}(t)} = \frac{1}{2} \cdot \left(\frac{V_{m(t)}}{V_{DC}(t)} \right)^2 . \tag{3.4}$$

Observing expression (3.4), it becomes clear that if the bias voltage tracks the variation of the input signal, the efficiency can be kept at its maximum. An example of an envelope-tracking circuit can be seen in the figure below. It consists of two paths. One contains a liner block and a delay block to compensate for the DC/DC converter delay. The other contains an envelope detector and a DC/DC converter. The challenge in this technique is to maximize the efficiency of the envelop detector and the DC/DC converter. The envelope detector can detect the instantaneous variation of the envelope amplitude or its average value. Depending on the choice, the bandwidth requirements of the DC/DC converter vary and the overall performance follows suit [13].

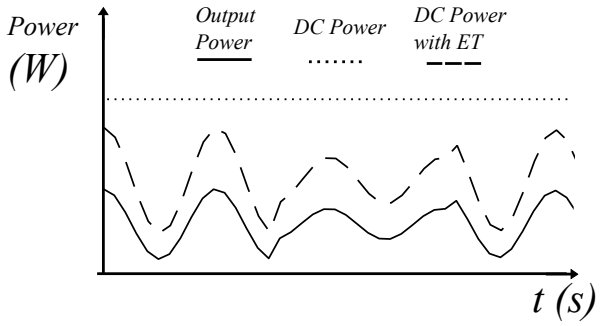


Figure 3.3: Envelope tracking concept.

3.2.3 Polar Modulation Technique

Polar modulation, also called envelope elimination and restoration, is an efficiency enhancement technique. It can be seen as an upgrade of envelope tracking as its maximum efficiency is higher. The polar modulation system consists of two branches. The first branch consists of an Radio Frequency (RF) limiter and an RF non-linear high-efficiency switching mode power amplifier. The other path consists of an envelope detector and a low-frequency power amplifier. The circuit associated with this technique can be observed in Fig. 3.4

At the input of this system is applied an Amplitude Modulated (AM) and Phase Modulated (PM) voltage.

$$v_{in} = V(t) \cdot \cos[w_c \cdot t + \theta(t)] \,. \tag{3.5}$$

The RF limiter as the name suggests, limits the input voltage, causing the following constant envelope, PM voltage.

$$v_{PM} = V_c \cdot \cos[w_c \cdot t + \theta(t)] \,. \tag{3.6}$$

The envelope detector is followed by a Low Frequency Power Amplifier (LF PA) which amplifies the AM component of the input signal. If the main PA is a class E, then one can express the output power in terms of the supply voltage in the following way

$$P_{out} = \frac{K_p}{R_{out}} \cdot V_{DD}^2 \,. \tag{3.7}$$

For a fixed output impedance and for an optimum point, R_{out} and K_p are fixed. The supply voltage will depend on the output of the upper branch which is equal to $v_m(t) \cdot A_v$.

The output voltage of the polar modulation can be expressed by equation (3.8)

$$V_{out} = |V_{out}| \cdot \cos[w_c \cdot t + \theta(t)] \quad \text{where} \quad |V_{out}| = K_p \cdot V(t) \tag{3.8}$$

The downside of this technique is that there is a difference in the phase shift of the two branches because of the AM/PM characteristic of the power amplifiers. Secondly, the RF limiter introduces phase distortion corrupting the signal phase. Also implementing the phase limiter in wide-band is challenging as obtaining an envelope amplifier with good efficiency for a relatively big bandwidth.

3.2.4 Outphasing Technique

This system consists of a signal component separator and a phase modulator, two identical nonlinear high-efficiency power amplifiers and RF power combiner. This technique is also called Linear Amplification with non linear components (LINC). The signal at the input of an outphasing power amplifier can be described by

$$v_i = V(t) \cdot \cos\left(w_c t + \phi(t)\right) = \cos\left[w_c t + \phi(t)\right] \cdot \cos([arcos\ V(t)]) \,. \tag{3.9}$$

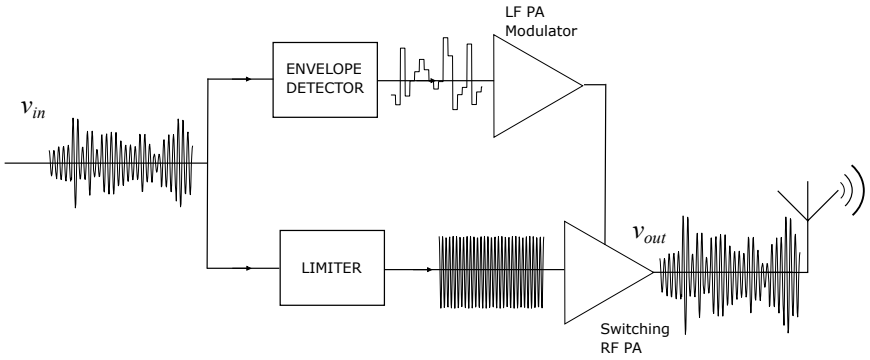


Figure 3.4: Polar Modulation circuit.

Using the trigonometric relationship

$$\cos(\alpha)\cos(\beta) = \frac{1}{2}\cdot\cos(\alpha+\beta) + \frac{1}{2}\cdot\cos(\alpha-\beta)\ , \tag{3.10}$$

the signal separator and PM block separate then the input signal in the two following signals.

$$v_1 = \frac{1}{2}\cdot\cos\left[w_c t + \phi(t) + \arccos V(t)\right]\ , \tag{3.11}$$

$$v_2 = \frac{1}{2}\cdot\cos\left[w_c t + \phi(t) - \arccos V(t)\right]\ . \tag{3.12}$$

Observing the output signals of the SP and PM block it is clear that the AM and PM information of the input signal is included in the output signals phase. The output signals have constant amplitude. This means that they can be amplified by non-linear high-efficiency switching mode power amplifiers. At the output of this system, there will be a sum of two sinusoidals. Using the trigonometric formula

$$\cos(\alpha)+\cos(\beta) = 2\cdot\cos\left(\frac{\alpha+\beta}{2}\right)\cdot\cos\left(\frac{a-\beta}{2}\right)\ . \tag{3.13}$$

The output signal of the system is given as follows.

$$\begin{aligned} v_0 = A_v\cdot(v_1+v_2) = A_v\Bigg\{ &\frac{1}{2}\cdot\cos\left[w_c t + \phi(t) + \arccos V(t)\right] + \\ &\frac{1}{2}\cdot\cos\left[w_c t + \phi(t) - \arccos V(t)\right]\ . \end{aligned} \tag{3.14}$$

The analysis above is only valid when the two branches are well balanced in terms of gain and phase. As there is always a mismatch between the two power amplifiers, at the output there will be a phase and gain error. This phase error produces spectral regrowth. Another problem with the outphasing is the combining stage. For instance, if the two branches are summed using a transformer each output impedance seen by the PA depends on the phase component resulting in a decrease in efficiency since the optimum point will drift. Chireix noted this problem and suggested the introduction of reactances to null the imaginary part [14]. Another issue is that there is needed outphasing for the quadrature and the in-phase components, amounting to 4 switching amplifiers.

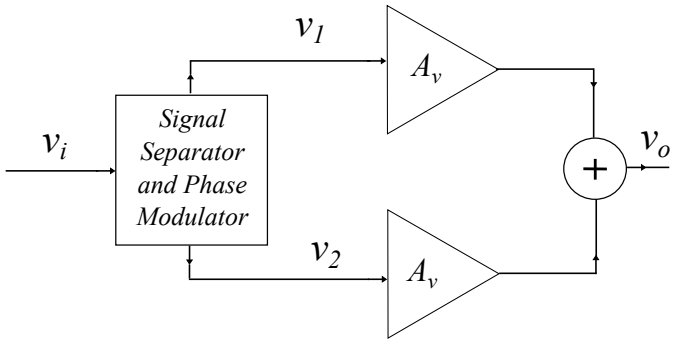


Figure 3.5: Outphasing circuit schematic

3.2.5 Doherty Technique

The main purpose of this system is to keep the amplifier working at maximum efficiency with the voltage input variation. A block diagram of this amplifier can be seen in Fig. 3.6 (a). The main power amplifier is called a carrier amplifier and the auxiliary power amplifier is called a peak amplifier. The main power amplifier is usually configured as AB or B class and the auxiliary amplifier is usually a class C amplifier. The main power amplifier is on until it saturates at high input power. When the main amplifier saturates, the auxiliary power amplifier is turned on and is responsible for the amplification of the high input power levels. The system maintains good efficiency under power back-off conditions [14].

For instance, the efficiency of power amplifiers whose conduction angle is lower than 180 degrees is given as follows.

$$\eta_D = \frac{1}{2} \cdot \frac{I_m^2 \cdot R}{V_{DC} \cdot I_{DC}} \ . \tag{3.15}$$

In class B, C or AB there is a relation between the peak current value and the DC current value and the output current amplitude.

$$I_m = I_{DM} \cdot \frac{\frac{\theta}{2} - \sin\left(\frac{\theta}{2}\right) \cdot \cos(\frac{\theta}{2})}{\pi \cdot (1 - \cos\left(\frac{\theta}{2}\right))} \ . \tag{3.16}$$

$$I_{DC} = I_{DM} \cdot \frac{\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2} \cdot \cos(\frac{\theta}{2})}{\pi \cdot (1 - \cos\left(\frac{\theta}{2}\right))} \ . \tag{3.17}$$

Replacing these two expression in the drain efficiency equation the following equation is obtained

$$\eta_D = \frac{1}{2} \cdot \frac{R}{V_{DC}} \cdot I_{DM} \cdot \kappa \ , \tag{3.18}$$

where $\kappa = \frac{\left(\frac{\theta}{2} - \sin\left(\frac{\theta}{2}\right) \cdot \cos\left(\frac{\theta}{2}\right)\right)^2}{(\pi \cdot (1 - \cos\left(\frac{\theta}{2}\right)) \cdot (\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2} \cdot \cos(\frac{\theta}{2})}$.The drain efficiency written this way clearly exposes the core understanding about the Doherty amplifier. The peak current value, I_{DM} is directly related to the gate source voltage applied to the power amplifier. Hence to

maximize the efficiency over a wide range of values of gate source voltage, the following condition must hold true.

$$R \cdot I_{DM} = V_{DC} \ . \tag{3.19}$$

To keep the validity of equation (3.19), the supply voltage can change leading to the envelope tracking solution. If it is the resistance that changes then the solution is called Doherty. The resistance is modulated by changing two independent current sources. This concept is illustrated in Fig. 3.6 (b). The current through the impedance R_L can be expressed through Kirchhoff's Current Law, like in equation (3.20)

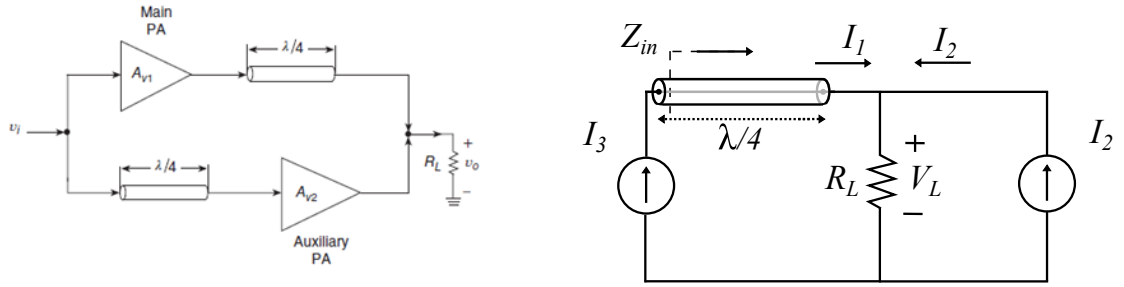
$$I_L = I_1 + I_2 \ . \tag{3.20}$$

The load impedance seen at the output of the transmission line is given by

$$R_1 = \frac{V_L}{I_1} = \frac{V_L}{I_L - I_2} = \frac{V_L}{I_L \cdot (1 - \frac{I_2}{I_1 + I_2})} = R_L \cdot (1 + \frac{I_2}{I_1}) \ . \tag{3.21}$$

The current I_1 can be seen as the output current of the main power amplifier and current I_2 as the output current of the auxiliary power amplifier. With this idea in mind, when the input gate source voltage is such that saturates the main PA, the auxiliary comes into play. In other words, the current I_1 will be saturated and I_2 will increase. Considering this behaviour, the reader can observe that the resistance seen by the main PA will increase instead of the desired behaviour of decrease. Another way to see this is that at the highest input voltage both currents are equal. This means that the main amplifier will see twice the output resistance when the current is at its highest. This surely will put the main amplifier working mainly in the triode region. To overcome this problem an impedance inverter is needed between the load R_L and the current source I_1.
The input impedance of a quarter-wave transmission line is given as follows.

$$Z_{in} = \frac{Z_0^2}{R_3} = \frac{Z_0^2}{R_L \cdot (1 + \frac{I_2}{I_1}.)} \tag{3.22}$$



(a) Circuit schematic

(b) Impedance modulation concept

Figure 3.6: Doherty Technique concepts

3.2.6 Quantized Digital Amplifier (QDA)

A new technique is now proposed and will be analyzed in future sub-sections. The Quantized Digital Amplifier (QDA) solution, in short, splits a high PMEPR signal into a constant envelope signal. This enables the use of highly efficient power amplifiers (Class E or D). The QDA consists of three main stages: the quantization stage, the amplification stage and the combining stage.

One of the goals of this technique is that it is fully-integrated into the existing technology. As so, the Orthogonal Frequency Division Multiplexing (OFDM) signal is firstly mixed with an intermediate frequency originating a band pass signal $x(t) = \bar{x(t)} \cdot \sin(2\pi f_i t)$. After that, the signal is sampled with a sampling frequency f_s, originating the time domain samples $x_n = x(nT_s)$.

3.2.6.1 Quantization Stage

After being sampled the signal goes through a uniform quantizer with 2^M, where M represents the quantization bits. These bits will be used to generate the control bits relative to the combining stage and to control the bank of M-1 digital-to-analog converters that follow the quantizer and are responsible to generate the different binary phase shift keying signals that will be amplified and combined.

Since the most significant bit is used to control the Binary Phase Shift Keying (BPSK) signal phase, and the 0 is represented by all the bits at 0, there are M-1 levels for the negative and positive signal parts. The clipping or saturation level of the quantizer was chosen to minimize the overall quantization distortion.

The normalized clipping level is represented by $s_M\sigma$, where $\sigma = \sqrt{\left|\overline{\bar{x}(t)^2}\right|}$ represents the standard deviation of the OFDM signal x(t). Based on the choice of this quantity, the signal-to-interference ratio can be minimized. In other terms, if a low clipping level is chosen, then the quantization distortion will come from the quantizer saturation. If a high clipping level is chosen, then the quantization distortion will come from the quantizer levels error. There is then an optimum level for the clipping level. Using this optimum level, the BER results in Fig. 3.7 can be obtained. This optimum normalized clipping level will also be useful when the overall efficiency of the amplifying stage is calculated.

3.2.6.2 Amplification Stage

In the amplification stage, the input signal of each amplifier stage is a constant envelope BPSK signal given by equation (3.23)

$$s_m(t) = A_m \cdot \sin(2\pi f_c t + \phi_m) \tag{3.23}$$

The most significant bit controls the phase of the BPSK signal. For positive values, ϕ_m is equal to 0 degrees and for negative values, ϕ_m is equal to 180 degrees. After the BPSK signal generation the signal enters the PA stage. Each amplifier has a different output

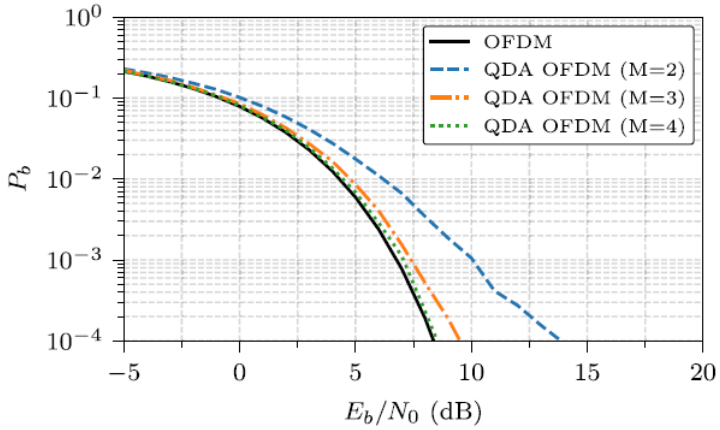


Figure 3.7: Simulated BER performance of a nonlinear OFDM system with 16-QAM modulation.[15]

power depending on the branch quantized level. For $m = 4$, an array of class-E PAs was implemented using the Qorvo TGF2977 transistor. The optimization process began with load-pull simulations at f=880 MHz where the gate and drain voltages, and the input power was swept to find the optimum input and output impedance points that maximize the Power Added Efficiency (PAE) for the desired output power of each power level of each amplifier. Table I shows the four PAs PAE and V_{DD} values at the desired output power level, with $V_{GG} = -2.7V$ the weighted average PAE of the 4 PAs is approximately 66.9 %.

Table 3.1: PA array performance.

PA #	V_{DD}	P_{in} (dBm)	P_{out} (dBm)	PAE (%)
1	12.29	10.3	25	69.7
2	8.26	9.1	22	66.4
3	5.64	8.6	19	64.4
4	3.21	6.2	16	63.4

3.2.6.3 Combining Stage

In the smart power combining stage, M-1 sections of the Wilkinson power combiner are used in a ladder structure. This type of combiner can be observed in Fig. 3.8.

The Wilkinson power combiner is a combiner that guarantees impedance matching at each port meaning isolation between ports. The disadvantage of this class of power combiners is the potential input power loss. In other words, if the inputs have different amplitudes or different phases, there will be losses through the isolation resistance. The truth table of the smart combiner can be observed in Table 3.2. If there is no power at both inputs the combiner is in an idle state. If there is at least power at one of the inputs, the

input power is bypassed to avoid losses in R_{isol}. Last but not least, if there is power at both inputs then the signals are combined.

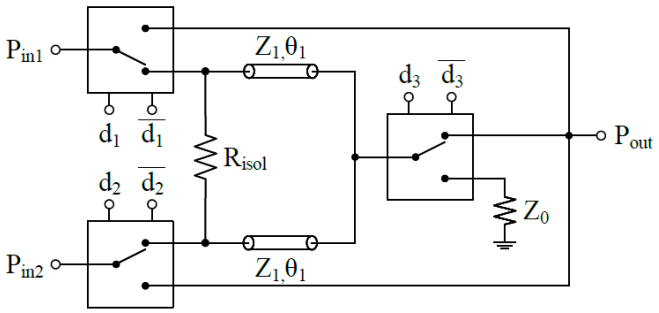


Figure 3.8: Schematic of the digitally controlled Wilkinson power combiner. [15]

Table 3.2: Smart combiner control bits.

Combiner State	P_{in1} (mW)	P_{in2} (mW)	d_1	d_2	d_3
Idle	$= 0$	$= 0$	1	1	0
Bypass P_{in1}	$\neq 0$	$= 0$	0	1	0
Bypass P_{in2}	$= 0$	$\neq 0$	1	0	0
Combine	$\neq 0$	$\neq 0$	1	1	1

3.2.7 QDA comparison with existing solutions

To better understand the novelty of the QDA solution, Table 3.3 compares it with existing solutions.

Table 3.3: QDA comparison with existing solutions.

Parameters	***[15]***	***[16]***	***[17]***	***[18]***	***[19]***	***[20]***
Frequency	880 MHz	2.4 GHz	2.4 GHz	1.95 GHz	1.9 GHz	32 GHz
Technology	Discrete GaN	-	Sim.	GaN/CMOS	40 nm CMOS	28 nm CMOS
Technique	QDA	PM	PM	Outphasing	Doherty	Doherty
Output Power	21.8 dBm	19 dBm	10 dBm	42 dBm	23.4 dBm	19.6 dBm
Gain	14.35 dB	6.5 dB	16 dB	24 dB	21.3 dB	18 dB
Max PAE	69.7%	-	-	-	-	32 %
Average PAE	31.3 %	28 %	-	-	23.3	22%
Drain efficiency	-	36%	41.3%	42 %	-	32 %

PM-Polar Modulation ; Sim.-Simulation

4

Class E design methodology foundations

4.1 Introduction

In chapter 3, the fundamentals of class E were seen. In the explanation of this Power Amplifier (PA) class, a choke inductor was considered. This might not be the optimal case because usually, the higher the inductor value, the lower the quality factor is. To analyze this circuit, two methods can be used, the harmonic balance or differential equations that are defined based on Kirchhoff laws. The harmonic balance method considers the circuit as being in a permanent regime. In the non-linear node (transistor drain node for example), there can be defined a number of harmonics. From there, equations can be defined and an iterative solution can be determined. For sake of being easier to understand the intermediary steps and as a preference to obtain a compact design kit, the differential equations were the way to go. A careful analysis of this topology allows to have a consistent design and potentially saves time in optimization or avoids unnecessary iterations.

In [21], a Class E design kit, assuming a finite DC feed inductance, is presented, and derived. Furthermore, a design example is given and complemented with a design kit explanation. To follow up, in [22], a survey about this design kit is introduced and a much more detailed explanation of the design kit is given, and design examples are conferred. Relative to the design kit considering the transistor on-resistance there is not much. Mustafa, in [23], derived the design kit considering the transistor on-resistance. However, the design kit exposed in that article is incomplete, despite the analysis of the latter being relevant and helpful. What's more, is that there is no article explaining the symbiosis between the design kit and an actual design and careful analysis of the design kit considering the transistor on-resistance. This indeed does not make much sense for discrete transistors but for integrated transistors where the transistor width is a variable this design kit might have a significant relevance. The goal of this design kit development and the post design is to investigate what are the challenges of developing a mobile handset PA. In addition to that, find if there is any advantage in using the design kit

considering the transistor on-resistance since an optimization process is almost certain.

Once the design kit is derived, the goal now centres on designing 4 class E PAs for different output powers. Before that, however, it is necessary to understand what are the disadvantages and limitations of this topology. The main disadvantage of this topology, the maximum drain voltage, will be explored. Then an attentive study on the impact of the supply voltage on the circuit performance will be done in order to understand if there is an advantageous relation between the output power and the supply voltage.

As it will be seen in the design kit derivation, one can only restrict the output power or the resistance but not both at the same time. Since our design is specified in terms of output power, the output resistance is a direct consequence of that. By reason of that, impedance transformation mechanisms will have to be analyzed in order to boost or drop the impedance for class E optimum conditions. Moreover, the design will have to account for the parasite resistances of the components, especially the inductors. Because of that, there is an optimum output resistance based on the characteristics of the components. The developed design kit will have a dependency on the transistor on-resistance. However, it does not express any relation between the transistor on-resistance and the transistor width. For the technology used that relation will be expressed by parametrization methods.

Last but not least, the input of a power amplifier, for certain output powers, cannot be directly connected to an Field Programmable Gate Array (FPGA). Power drivers are then important pillars in connecting a very low power output source to a very power hungry power amplifier input. By the end of this chapter, the reader should understand the necessary the trade-offs and the intricacies needed to design a class E power amplifier for any output power specification.

4.2 Analysis of the class E considering transistor on-resistance

In this analysis, the transistor on-resistance is considered. This opens doors to eventually find a trade-off between the size of the transistor and the value of the input power, for instance. In addition to that, once we have a power loss component, a theoretical drain efficiency can be explored. This might give us some light on whether the choke inductor assumption is good for situations where we can change the transistor width. The following study considers a transistor on-resistance. Also, it considers a 50% duty cycle. The schematic of the circuit can be observed in Fig. 4.1.

When the transistor is ON the current balance in the drain node of the transistor is given as follows

$$I_L + I_R - I_C - I_S = 0 \ , \tag{4.1}$$

where the inductor current is given as

$$I_L = \frac{1}{L} \cdot \int (V_{DD} - V_{C_{on}}(t)) \quad dt = \frac{V_{DD}}{L} t - \frac{1}{L} \int V_{C_{on}}(t) \quad dt + i_0 \ , \tag{4.2}$$

where i_0 corresponds to the initial current of the inductor L. The current through the capacitor is, opposite to the other analysis, not null and given by the following expression

$$I_C = C \cdot \frac{d\, V_{C_{on}}(t)}{dt} \,. \tag{4.3}$$

The current through the transistor, assuming that it can be modelled as a on-resistance on the deep triode region is given by equation (4.4)

$$I_S = \frac{V_{C_{on}}(t)}{r_{on}} \,. \tag{4.4}$$

Assuming a high enough tank quality factor, the current through the tank only contains a harmonic. As so it can be expressed as follows

$$I_R = I_R \cdot \sin(wt + \theta) \,. \tag{4.5}$$

Replacing (4.5), (4.4), (4.3) and (4.2) in (4.1) and deriving once, we obtain the following differential equation

$$C \cdot \frac{d^2 V_{C_{on}}(t)}{dt} + \frac{1}{r_{on}} \frac{d\, V_{C_{on}}(t)}{dt} + \frac{1}{L} V_{C_{on}}(t) - \frac{V_{DD}}{L} - w \cdot I_R \cdot \cos(wt + \theta) = 0 \,. \tag{4.6}$$

Similarly to the analysis ignoring the on-resistance, some variables are considered in order to simplify the design.

$$q = \frac{1}{w \cdot \sqrt{L \cdot C}} \,. \tag{4.7}$$

$$p = \frac{w \cdot L \cdot I_R}{V_{DD}} \,. \tag{4.8}$$

Additionally, new variables are defined due to the introduction of the transistor on-resistance.

$$m = w \cdot r_{on} \cdot C \,. \tag{4.9}$$

$$a = \frac{-1 + \sqrt{1 - 4 \cdot q^2 \cdot m^2}}{2 \cdot m} \,. \tag{4.10}$$

$$b = \frac{-1 - \sqrt{1 - 4 \cdot q^2 \cdot m^2}}{2 \cdot m} \,. \tag{4.11}$$

With this variables transformation, we arrive at a very (compact) description of the drain voltage during the transistor ON time,

$$V_{d_{on}}(t) = V_{DD} + c_1 \cdot e^{a \cdot w \cdot t} + c_2 \cdot e^{b \cdot w \cdot t} + \frac{m \cdot p \cdot q^2 \cdot V_{DD} \cdot \left[sin(\theta + w) + m \cdot (-1 + q^2) \cdot cos(\theta + w \cdot t) \right]}{1 + m^2 \cdot (-1 + q^2)^2} \,. \tag{4.12}$$

To determine the constants c_1 and c_2, the continuity of the voltage and current shall be considered. The Zero Voltage Switching (ZVS) and Zero Derivative Voltage Switching (ZDVS) conditions must be fulfilled. This can be expressed, mathematically, as

$$V_C(T) = 0 \,, \tag{4.13}$$

$$\frac{dV_c}{dt} = 0 \, . \tag{4.14}$$

The constants c_1 and c_2 can be consulted in the appendix D. Since we derived the current equation, the initial inductor current disappears. However to keep the validity of the current equation this initial current must be set. Admitting that the optimum conditions at turn-on are satisfied, this initial inductor current can be given by equation (4.15).

$$i_0 = -i_m \cdot \sin(\theta) \, . \tag{4.15}$$

When the transistor is OFF, assuming a relatively large off resistance, the current balance in the drain transistor node is given as

$$I_L + I_R - I_C = 0 \, . \tag{4.16}$$

The current on the inductor, resistor and capacitor is equivalent to when the transistor is ON.For review, consult equations (4.2),(4.3) and (4.4). The second order equation, when the transistor is OFF, can be given as

$$L \cdot C \cdot \frac{d^2 V_C\,(t)}{dt} + V_C\,(t) - V_{DD} - \; L \cdot w \cdot I_R \cdot \cos\,(wt + \theta) = 0 \, . \tag{4.17}$$

Solving this differential equation and using the same variable transformation, (4.7) and (4.8), we obtain the following equation

$$V_{d_{off}}(t) = V_{DD} + c_3 \cdot cos(q \cdot w \cdot t) + c_4 \cdot sin(q \cdot w \cdot t) - \frac{p \cdot q^2 \cdot V_{DD} \cdot cos(\theta + w \cdot t)}{1 - q^2} \, . \tag{4.18}$$

Similarly, to find the constants c_3 and c_4, the ZVS and ZDVS conditions are used. This are translated by equations (4.13) and (4.14). The reader may wonder why using the same conditions. Once the circuit reaches a permanent stage, the circuit dynamics become periodic. As a result, the turn ON conditions must be met in the circuit description when the transistor is on and also when it is off. The constants c_3 and c_4 are then given by the equations (D.3).

What remains to do is to guarantee the continuity of voltage and current between the on and off transition of the capacitor and inductor, respectively. These conditions can be described by equations (4.19), (4.20).

$$V_{C_{on}}(\frac{\pi}{w}) = V_{C_{off}}(\frac{\pi}{w}) \, . \tag{4.19}$$

$$I_{L_{on}}(\frac{\pi}{w}) = I_{L_{off}}(\frac{\pi}{w}) \, . \tag{4.20}$$

With equations (4.19) and (4.20) the value of p and θ can be described with a q dependency. To present p and θ in a compact form, the following auxiliary variables (a_1,b_1,d_1,a_2,b_2,c_3), described in annex D. With these auxiliary variables, p and θ can be defined in terms of q

$$p = -\frac{\sqrt{d_2^2\left(a_1^2 + b_1^2\right) - 2a_1 \cdot a_2 \cdot d_1 \cdot d_2 + a_2^2 d_1^2 - 2 \cdot b_1 \cdot b_2 \cdot d_1 \cdot d_2 + b_2^2 d_1^2}}{\sqrt{(a_2 \cdot b_1 - a_1 \cdot b_2)^2}} \, , \tag{4.21}$$

$$\theta = \tan^{-1}\left(\frac{(a_2 \cdot b_1 - a_1 \cdot b_2)(b_1 \cdot d_2 - b_2 \cdot d_1)}{\sqrt{(a_2 \cdot b_1 - a_1 \cdot b_2)^2}\sqrt{d_2^2\left(a_1^2 + b_1^2\right) - 2a_1 \cdot a_2 \cdot d_1 \cdot d_2 + a_2^2 d_1^2 - 2b_1 \cdot b_2 \cdot d_1 \cdot d_2 + b_2^2 d_1^2}}, \right.$$
$$\left. \frac{(a_2 \cdot b_1 - a_1 \cdot b_2)(a_2 \cdot d_1 - a_1 \cdot d_2)}{\sqrt{(a_2 \cdot b_1 - a_1 \cdot b_2)^2}\sqrt{d_2^2\left(a_1^2 + b_1^2\right) - 2a_1 \cdot a_2 \cdot d_1 \cdot d_2 + a_2^2 d_1^2 - 2b_1 \cdot b_2 \cdot d_1 \cdot d_2 + b_2^2 d_1^2}}\right) . \tag{4.22}$$

With this solution, the derivation of the design kit is the final step. Similar to the analysis ignoring the transistor on-resistance, the variables of the design will be the same. What changes is the way of describing them. Starting with K_L, this variable can be derived using the circuit power conservation. From all the energy supplied by the source, some is dissipated in the transistor and some is delivered to the output resistance.

$$\frac{{I_R}^2}{2} \cdot R + P_{switch} = I_0 \cdot V_{DD} \ . \tag{4.23}$$

Where I_0 represents the average supply current. To compute this quantity, note that when the transistor is off, no DC current is generated since there is no linear term in the voltage equation. Besides, when the transistor is on, all the DC current flows through the transistor since there is no linear term in the voltage equation. This means that the average supply current can be described by equation (4.24).

$$I_0 = \frac{w}{2\pi \cdot R_{on}} \int_0^{\frac{\pi}{w}} V_{C_{on}} \, dt \ . \tag{4.24}$$

To calculate P_{switch}, considering that the transistor only has a considerable resistance during its on time, one can use the formula (4.25).

$$P_{switch} = \frac{w}{2\pi \cdot R_{on}} \cdot \int_0^{\frac{\pi}{w}} V_{C_{on}}(t)^2 \, dt \ . \tag{4.25}$$

Replacing (4.24) and (4.25) in (4.23) we get

$$\frac{{I_R}^2}{2} \cdot R \cdot \frac{2\pi \cdot R_{on}}{w} = \int_0^{\frac{\pi}{w}} V_{C_{on}} \, dt \cdot V_{DD} \ - \ \int_0^{\frac{\pi}{w}} {V_{C_{on}}}^2 \, dt \ . \tag{4.26}$$

Using equation (4.8), we can replace I_R by the following

$$I_R = \frac{p \cdot V_{DD}}{w \cdot L} \ . \tag{4.27}$$

Applying (4.7) in (4.27) and squaring it, we get equation (4.28).

$${I_R}^2 = \frac{p^2 \cdot {V_{DD}}^2 \cdot q^2 \cdot C}{L} \ . \tag{4.28}$$

Replacing (4.28) in (4.26) we obtain

$$\frac{p^2 \cdot {V_{DD}}^2 \cdot q^2 \cdot C}{2 \cdot L} \cdot R \cdot \frac{2\pi \cdot R_{on}}{w} = \int_0^{\frac{\pi}{w}} V_{D_{on}} \, dt \cdot V_{DD} \ - \ \int_0^{\frac{\pi}{w}} {V_{D_{on}}}^2 \, dt \ . \tag{4.29}$$

Noting that $m = w \cdot R_{on} \cdot C$, the equation (4.29) can be re-written as

$$\frac{p^2 \cdot {V_{DD}}^2 \cdot q^2}{2 \cdot L} \cdot R \cdot \frac{2\pi \cdot m}{w^2} = \int_0^{\frac{\pi}{w}} V_{D_{on}}\, dt \cdot V_{DD} \; - \; \int_0^{\frac{\pi}{w}} {V_{D_{on}}}^2\, dt \; . \tag{4.30}$$

Putting $w \cdot L$ and R in evidence, we have the following relation

$$K_L = \frac{w \cdot L}{R} = \frac{m \cdot \pi \cdot p^2 \cdot {V_{DD}}^2 \cdot q^2}{w \left(\int_0^{\frac{\pi}{w}} V_{D_{on}}\, dt \cdot V_{DD} \; - \; \int_0^{\frac{\pi}{w}} {V_{D_{on}}}^2\, dt \right)} \; . \tag{4.31}$$

Given the q definition, K_C can be obtained from K_L by simply doing

$$K_C = \frac{1}{q^2 \cdot K_L} \; . \tag{4.32}$$

From the definition of K_L, one can write equation (4.35).

$$K_L = \frac{V_{DD} \cdot p}{R \cdot I_R} \; . \tag{4.33}$$

Equation (4.27) can be re-written by

$$I_R = \sqrt{\frac{2 \cdot P_{out}}{R}} \; . \tag{4.34}$$

Replacing (4.34) in (4.35), we reach at equation (4.35).

$$K_L = \frac{V_{DD} \cdot p \cdot \sqrt{R}}{R \cdot \sqrt{2 \cdot P_{out}}} \; . \tag{4.35}$$

Picking equation (4.35) , squaring it and putting in evidence $\frac{P_{out} \cdot R}{{V_{DD}}^2}$, the definition of K_p becomes clear by equation (4.36).

$$K_P = \frac{P_{out} \cdot R}{{V_{DD}}^2} = \frac{p^2}{2 \cdot {K_L}^2} \; . \tag{4.36}$$

Relative to the K_x, it can be obtained by taking the real and imaginary Fourier coefficient of the fundamental harmonic present at the drain voltage. The real and imaginary coefficients represent the voltage drop of the output resistance and additional reactance X, respectively

$$V_R = \int_0^{\frac{\pi}{w}} \frac{V_{d_{on}}(t)}{\pi} \cdot sin(w \cdot t + \varphi)\, dt \; + \int_{\frac{\pi}{w}}^{\frac{2\pi}{w}} \frac{V_{d_{off}}(t)}{\pi} \cdot sin(w \cdot t + \varphi)\, dt \; , \tag{4.37}$$

$$V_X = \int_0^{\frac{\pi}{w}} \frac{V_{d_{on}}(t)}{\pi} \cdot cos(w \cdot t + \varphi)\, dt \; + \int_{\frac{\pi}{w}}^{\frac{2\pi}{w}} \frac{V_{d_{off}}(t)}{\pi} \cdot cos(w \cdot t + \varphi)\, dt \; , \tag{4.38}$$

$$K_X = \frac{V_x}{V_R} \; . \tag{4.39}$$

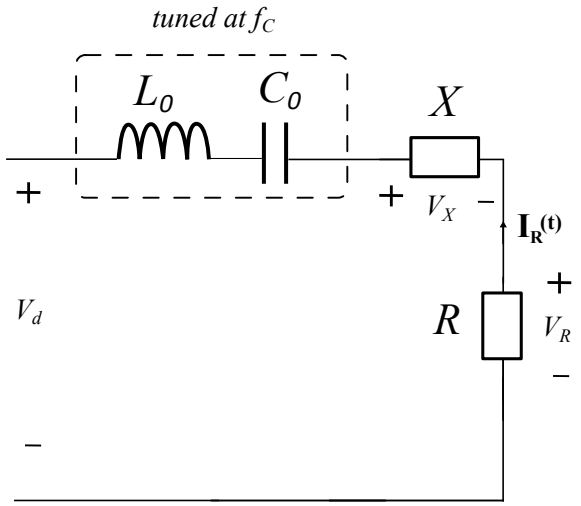


Figure 4.1: Class E schematic.

The design kit is all defined. To see if there is any advantage in considering a non choke inductor, a theoretical drain efficiency needs to be defined. Since there is now a power loss component, the drain efficiency can be defined by equation (4.40).

$$\eta = \frac{V_{DD} \cdot I_0 - P_{switch}}{V_{DD} \cdot I_0} = 1 - \frac{P_{switch}}{V_{DD} \cdot I_0} \ . \tag{4.40}$$

In Fig. 4.2 the reader can observe the drain efficiency variation with q and m. Assuming that the optimal conditions are met, using a design with a Radio Frequency (RF) choke is not clearly a good choice. The design kit can be seen in Fig. 4.3 for $m = 0.02$.

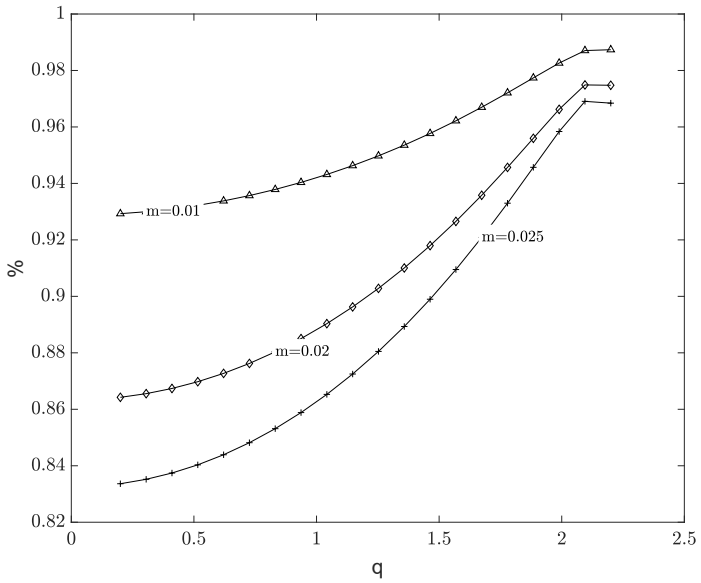


Figure 4.2: Drain efficiency for different values of m.

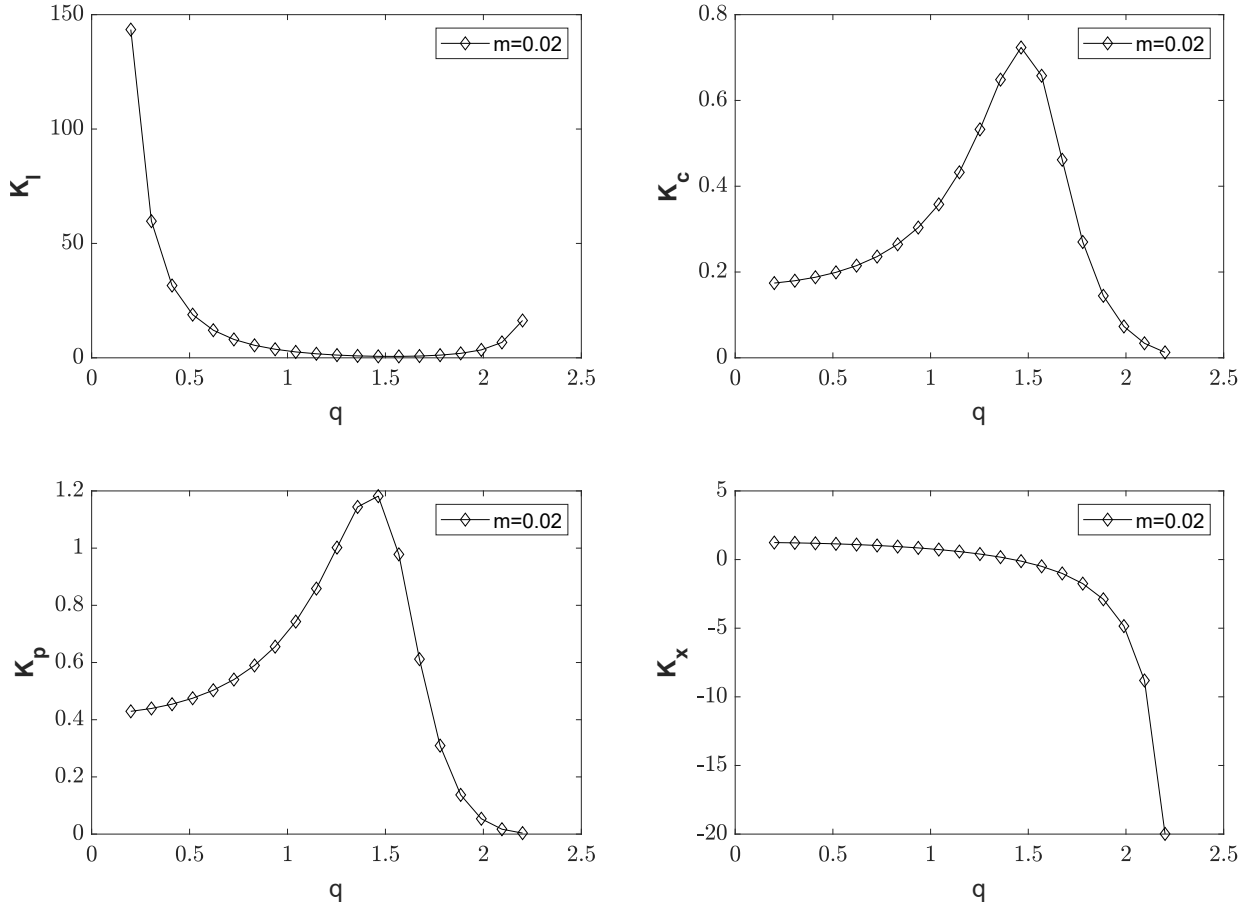


Figure 4.3: Design kit for $m = 0.02$.

4.3 Maximum drain voltage

One of the major problems of this topology is the maximum drain voltage. This maximum is always reached at ¾ of the period because if the transistor turns ON at zero voltage and zero derivative voltage, all the energy supplied by the capacitor is given back. In other words, when the transistor is OFF, the drain voltage is symmetric around ¾ of the period. The variation of the maximum voltage with q and m can be observed in Figure 4.4. Note that the maximum voltage does not change much with q but rather with m. This suggests that the transistor on-resistance influences the maximum voltage the most. Also, these results were obtained considering a supply voltage of 1.2 V. Naturally, the maximum voltage depends on the supply voltage. The tendency of the maximum voltage increase with the m increase is notorious. It is corroborated by the approximated curve that corresponds to an analysis scenario where the transistor on-resistance was ignored.

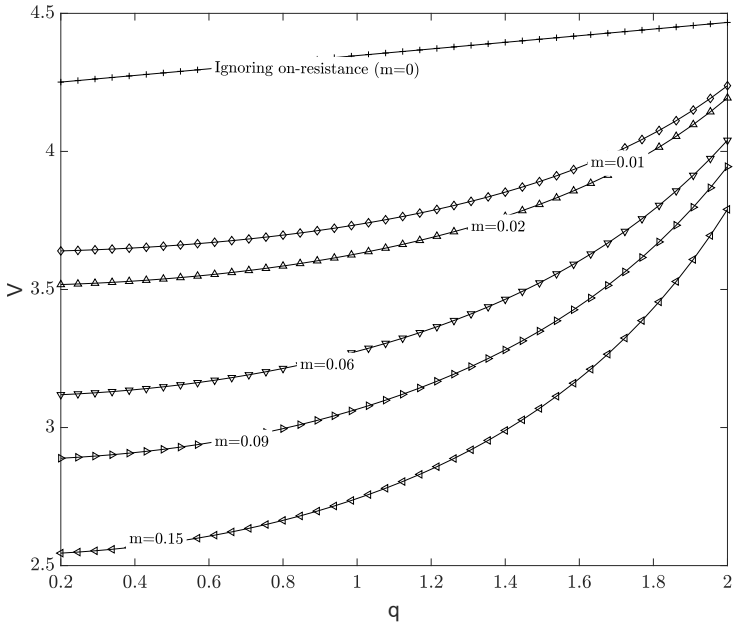


Figure 4.4: Variation of the maximum voltage with q and m.

The immediate solution could be to use a very high m. That unfortunately brings the inherent disadvantage of a substantial low Power Added Efficiency (PAE). This solution will be better analyzed in the design section. Another solution could be to try a completely different topology like the class DE [24]. The solution explored in this thesis is the cascode solution. In small signals, the cascode solution brings the advantage of increasing the output impedance consequently increasing the gain. Also, it provides good isolation between the output and input.

In a large signal approach, the cascode solution is quite handy to reduce the drain-source voltage stress. To maintain the optimum conditions the resistance value has to be divided between the two transistors. For example, let's say the optimum resistance is R, meaning that each transistor can have, for instance, $\frac{R}{2}$. The transistor on-resistance on

each transistor dropped while the transistor width practically doubled. This is the price to pay for dropping the maximum voltage on each transistor. Relative to the transistor's regions, when the common source transistor is on, both transistors operate in the triode region. When the common source transistor is off, the common gate transistor is saturated. What will be the source voltage of the common gate transistor? The short answer is that it will be enough so that the gate source voltage is above the threshold voltage. As so, the selection of the gate voltage of the common gate transistor is crucial for two main reasons. The first reason is transistor on-resistance. The second is that since the common gate transistor needs to be on, the following relation can be deduced

$$V_{s2} \approx V_{g2} - V_{TH} \ . \tag{4.41}$$

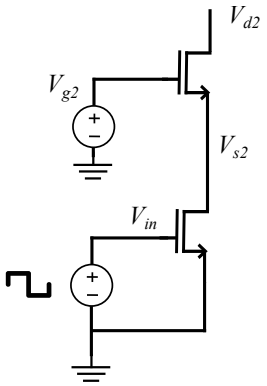
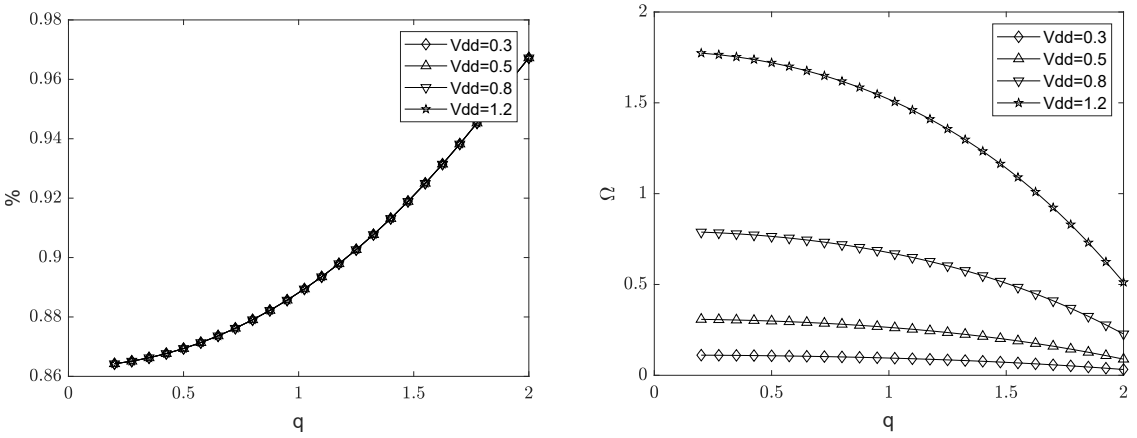


Figure 4.5: Cascode schematic.

4.4 Effect of V_{DD} on PAE

As it was seen in the derivation of the design kit, the parameters only depend on q and m. This means that the drain efficiency, for instance, does not change with the variation of the supply voltage as it can be seen in Fig. 4.6 (a). Nevertheless, the on-resistance decreases. This makes sense because the drain efficiency does not change with the supply voltage, which is the same as saying that for a given q and m the power loss is the same. So, to counter the decrease of the supply voltage, the on-resistance has to decrease. This behaviour is depicted in Fig. 4.6 (b).

The effect of V_{DD} can be seen from another perspective. As it can be seen in Fig. 4.7 the maximum voltage drops as the supply voltage drops. Because of this reduction, the first harmonic of the drain voltage will be lower. Assuming that the output power is the same, the output resistance has to be lower and the output current has to be larger. If the output current is larger it is reasonable to assume that the capacitor current increases. The same goes for the inductor by the Kirchhoff laws. By the continuity principle, the current will also be larger when the transistor is on. If this happens, the supply power remains the same because the inductor current increases in the same proportion that the supply



(a) Drain Efficiency. (b) On Resistance.

Figure 4.6: Variation of V_{DD} for m=0.02 .

voltage dropped. If this is true, then the power loss in the transistor has to be kept the same. For this to happen, since the current increases the on-resistance has to decrease. This rationale is supported by the design kit. Let's consider a design coordinate of (q,m) equal to (2,0.02). The relevant obtained simulated values are illustrated in Table 4.1.

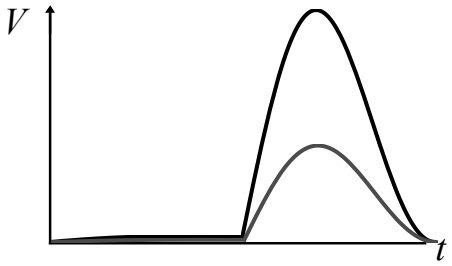


Figure 4.7: Class E voltage variation with time for different V_{DD} values.

Table 4.1: Class E performance for different V_{DD} values.

Parameters	V_{DD} **= 0.5**	V_{DD} **= 1.2**
Output Power (mW)	40.23	39.96
Input power (mW)	3.076	0.699
Supply Power (mW)	45.31	45.87
PAE (%)	82.0	85.6
On-resistance Ω	0.089	0.504
Output Resistance Ω	0.302	1.742

So far, there seems to be no need to adjust the supply voltage to the required output power. This is because the supply current changes in conformity with the required output resistance. To understand if there is a consequence relation between the output power and supply voltage, the transistor on-resistance needs to be fixed. Keeping the transistor

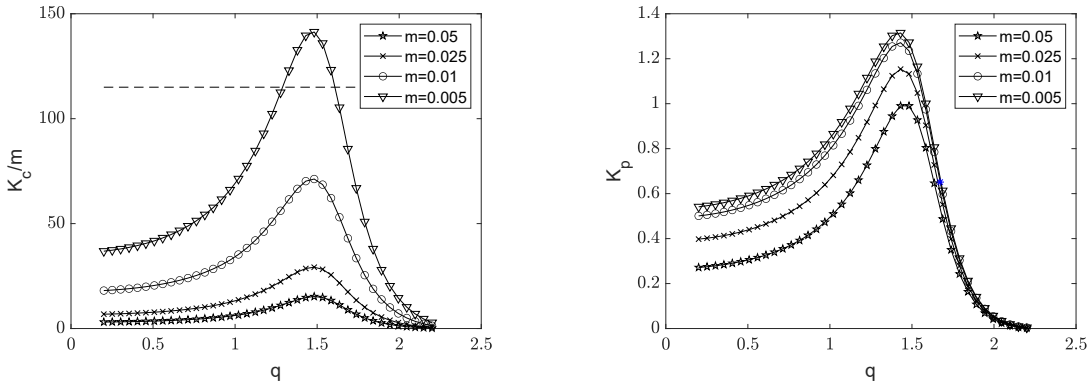
on-resistance constant, means that equation (4.42) must be satisfied.

$$\frac{K_c}{m} = \frac{R_{out}}{r_{on}} \ . \tag{4.42}$$

From equation (4.42), the design variables q and m are defined. From there the design function K_p has a fixed value. Besides that, the output resistance value is defined, which means that the following equation holds true

$$\frac{P_{out}}{{V_{DD}}^2} = \frac{K_p}{R_{out}} = const \ . \tag{4.43}$$

As a proof of concept, let's assume an output resistance of 23 Ω and a transistor on-resistance of 0.5. Computing the ratio $\frac{K_c}{m}$, the design variables q and m can be found, as it can be seen in Fig. 4.8 (a). The desired point crosses two points of the curve. The highest q value was chosen to guarantee an inductor as the additional tank reactance. Then with those two design variables the value of the variable function K_p can be found, as it can be seen in Fig. 4.8 (b). The optimum K_p has a value equal to 0.9087. Knowing the output resistance, the relation between the output power and the squared supply voltage can be evaluated. This relation is expressed in equation (4.44). This relation can be observed graphically for different output power values in Fig. 4.9



(a) Condition of K_c over m.

(b) Design function K_p.

Figure 4.8: Impact of constant on-resistance.

$$\frac{P_{out}}{{V_{DD}}^2} = 0.0399 \ . \tag{4.44}$$

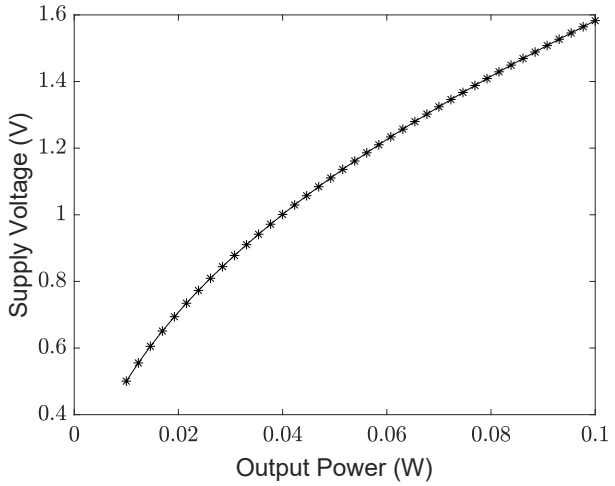


Figure 4.9: Supply voltage variation with output power.

4.5 Impedance matching

4.5.1 Introduction

Impedance matching is a cornerstone in RF design. This term is present in almost every RF circuit. The most basic case is optimal power transfer. In power amplifiers, particularly, this technique has almost a certain use. For example, in class A topology, to generate the maximum output voltage swing, the output resistor must be carefully chosen. In some cases, it might coincide with the characteristic impedance of 50 Ω. But it is not always the case. In this chapter let's consider impedance matching to a single tone. This is the desired case in most situations. Specifically, the wave present at the input of the antenna is usually a sinusoidal carrier wave with a narrow-band envelope. This implies a resonant tank at the output of the power amplifier. In the simplest case, the optimum resistor is 50 Ω and the tank has the following format. There can be two types of tank configurations. A tank in series or in parallel. The choice depends on the application. Assume that the following analysis considers a series tank. In order to design a tank, two questions must be answered. What is the resonant frequency of the tank? And what is the quality factor of the tank? The first is of a short answer and can be resolved with equation (4.45).

$$f_c = \frac{1}{2 \cdot \pi \cdot \sqrt{LC}} \,. \tag{4.45}$$

The second question has more to it than meets the eye. In physical terms, the quality factor Q tells us how much of all the energy supplied to a reactive component (for example) is lost. Meaning that the reactive component will store some of this available energy and the remaining energy will be lost. Equating this ratio, we get the traditional definition of a quality factor given by equation (4.46).

$$Q_L = 2\pi \cdot \frac{\textit{Maximum instantaneous energy stored at } f_c}{\textit{Total energy lost per cycle at } f_c} \,. \tag{4.46}$$

If one develops (4.46) by assuming a sinusoidal permanent regime, it arrives at the alternative definition of quality factor expressed by equation (4.47).

$$Q_L = \frac{X_T}{R_T} \ , \tag{4.47}$$

where R_T represent the series resistor and X_T the reactance which can be from a capacitor or inductor. The equation (4.47) can have many interpretations. One of them is assessing the quality of a real component. For example, in inductors the higher the quality factor the lower the parasitic resistance becomes. This will have some relevance in the section of the L network. The other interpretation is defining the quality factor of the tank itself. Expanding equation (4.47) we get the following equation

$$Q_L = \frac{2\pi \cdot f_c \cdot L_T}{R_T} \ , \tag{4.48}$$

where L_T represents the series inductor. Differently, using equation (4.45) and replacing in (4.48) we get

$$Q_L = \frac{1}{R_T \cdot 2\pi \cdot {f_c}^2 \cdot C_T} \ . \tag{4.49}$$

The good characterization of the tank quality factor allows one to know the bandwidth of the tank. In other words, the range of frequencies around the working frequency where the tank behaviour is assumed to be "constant". More rigorously, the bandwidth is defined as the frequencies where the gain of the tank drops -3 dB. The bandwidth can be defined by means of equation (4.50).

$$BW = \frac{f_c}{Q_L} \ . \tag{4.50}$$

The higher the tank quality factor, the less bandwidth the tank has, meaning more harmonic selectivity.

As a proof of concept, assume a working frequency of 1 GHz and a desired quality factor

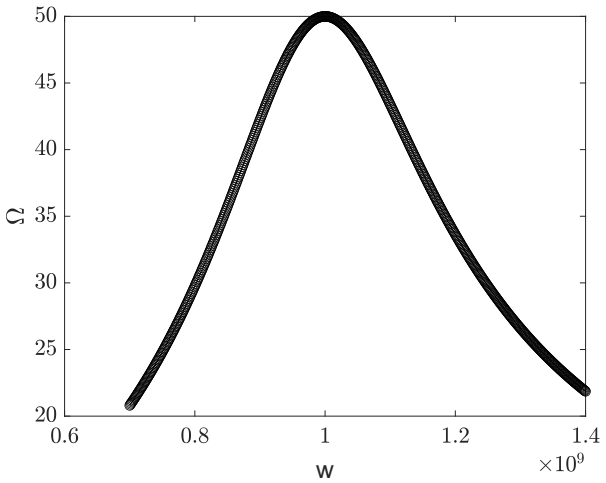


Figure 4.10: Tank impedance evolution with the frequency.

of 10. With this, the value of L_T and C_T can be found. Considering the output resistance equal to 50 ohm the inductor value can be found using equation (4.48)

$$L_T = \frac{Q_L \cdot R_T}{2\pi \cdot f_c} = \frac{10 \cdot 50}{2\pi \cdot 1 \cdot 10^9} = 79.57\ nH\ . \tag{4.51}$$

Now using equation (4.45) the value of the series capacitor can be calculated.

$$C_T = \frac{1}{(2 \cdot \pi \cdot f_c)^2 \cdot L_T} = \frac{1}{(2 \cdot \pi \cdot 1 \cdot 10^9)^2 \cdot 79.57 \cdot 10^{-9}} = 0.318\ pF\ . \tag{4.52}$$

With a basic understanding of the quality factor, apprehending the concept of impedance transformation is easier. In the next section, impedance transformation will be explored and with that understood, specific cases such as the L network can be studied.

4.5.2 Impedance Transformation

In the previous subsection 4.5.1, the foundations of the resonant tank and quality factor were given. A tool to analyze and transform a series tank to a parallel tank will be examined. This subsection was inspired by the book [25]. Suppose the following series tank is depicted in Fig. 4.11. The complex impedance can be given as

$$z_{in} = r + j \cdot x\ . \tag{4.53}$$

Now, consider a parallel tank. Its complex impedance is given by equation (4.54)

$$Z_{in} = \frac{1}{\frac{1}{R} + \frac{1}{X}}\ . \tag{4.54}$$

How can we then transform a series tank into a parallel tank? Well, we equate both impedances as equal and see what is the relation between the real parts and imaginary parts. By doing this we arrive at the following relations

$$R = r \cdot \frac{R^2 + X^2}{X^2}\ , \tag{4.55}$$

$$X = x \cdot \frac{R^2 + X^2}{R^2}\ . \tag{4.56}$$

Note that this transformation is narrowband. In other words, in the DC regime whereas in the series tank there will be no current since the capacitor is open-circuited, in the parallel tank there will be current through the inductor. Besides that, it is assumed that the reactive components have a single value. This works fine for a narrowband approximation.
This transformation implies that the series quality factor is equal to the parallel quality factor. Intuitively, a small series resistor means that all the energy is stored by the reactive components. This is equivalent to saying that we have a big parallel resistor.

$$Q_s = Q_p = \frac{x}{r} = \frac{R}{X}\ . \tag{4.57}$$

Given the quality factor equivalence, equations (4.55) and (4.56) can be re-written as

$$R = r \cdot \left(Q^2 + 1\right)\ , \tag{4.58}$$

$$X = x \cdot (1 + Q^{-2})\ . \tag{4.59}$$

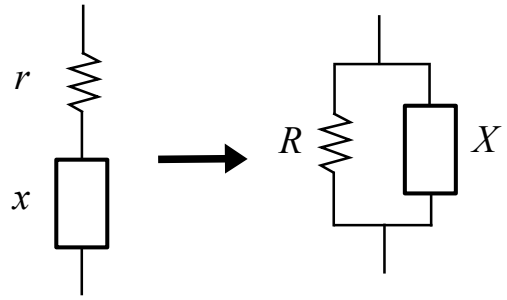
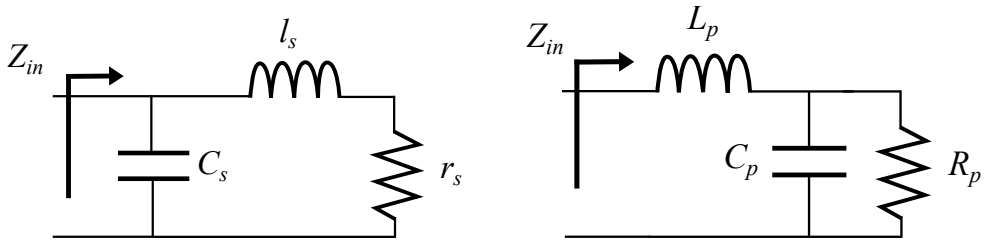


Figure 4.11: Impedance Transformation.

4.5.3 L network

Now that a tool to analyze impedance transformation circuits was presented, a specific case can be studied. The L network, named due to its format, it's an impedance transformation network whose aim is to increase or decrease the impedance seen at the input. The two main networks are depicted in Fig. 4.12. The rationale behind this network is trying to discriminate the resonant tank and see what is the real part of that transformation.



(a) Impedance Boost. (b) Impedance Drop.

Figure 4.12: L networks.

4.5.4 Impedance Boosting

4.5.4.1 Ideal Scenario

In light of what was explained in subsection 4.5.2, it is quite straightforward to transform the series inductor and resistor to a parallel one. The parallel inductor and resistor value can be given at the expense of the series component value by equations (4.60) and (4.61).

$$R_s = r_s \cdot \left(Q^2 + 1\right) . \tag{4.60}$$

$$L_s = l_s \cdot (1 + Q^{-2}) . \tag{4.61}$$

Where the quality factor can be given by equation (4.62)

$$Q = \frac{2 \cdot \pi \cdot w \cdot l_s}{r_s} . \tag{4.62}$$

The resulting circuit can be observed in Fig. 4.13. This is basically a parallel tank. The transformed shunt inductor will resonate with the shunt capacitor. This means that the

shunt capacitor value must comply with the following equation

$$C_s = \frac{1}{(2\pi \cdot f_c)^2 \cdot L_s} \ . \tag{4.63}$$

The shunt capacitor will be resonant with the equivalent shunt inductor. This means that at the resonant frequency the imaginary part is 0. Consequently, the impedance seen from the input represents the transformed resistor.

$$Z_{in} = r_s \cdot \left(Q^2 + 1\right) \ . \tag{4.64}$$

To consolidate these concepts let's solve an example. Consider an output resistance of 50 Ω and a desired input resistance of 100 Ω. Using equation (4.64) it is easy to obtain the quality factor of the tank since we know the output resistance and relevant input resistance. The quality factor is then given by the following

$$Q = \sqrt{\frac{R_s}{r_s} - 1} = \sqrt{\frac{100}{50} - 1} = 1 \ . \tag{4.65}$$

With this value, since the series quality factor is equal to the parallel quality factor the inductor value can be found by using the definition of quality factor.

$$L_s = \frac{R_s}{Q \cdot 2 \cdot \pi_c} = 15.91 \ nH \ . \tag{4.66}$$

All that is left to do is to calculate the value of the shunt capacitor. This can be done by resorting to the definition of the resonant frequency.

$$C_s = \frac{1}{(2 \cdot \pi_c)_s^2} = 1.591 \ pF \ . \tag{4.67}$$

Note that L_s does not represent the physical inductor but the parallel equivalent. To find l_s, one can use the equation (4.61)

$$l_s = \frac{L_s}{1 + Q^{-2}} = 7.95 \ nH \ . \tag{4.68}$$

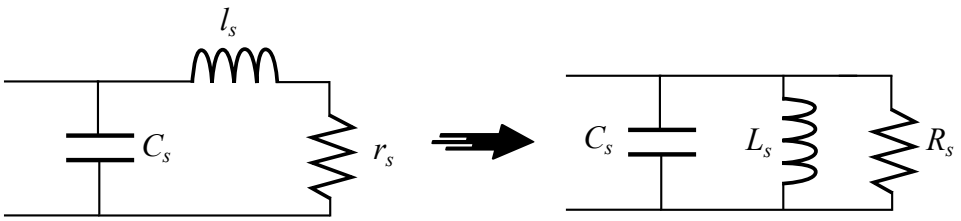


Figure 4.13: Impedance Boost.

4.5.4.2 Real Scenario

The analysis above considered that the only power loss would come from the output resistance. This starts to fail when real components are used. The matter becomes worse when integrated components, with low Q values, are used. To measure the quality of the real scenario impedance transformation a metric called insertion loss will be used. It can be expressed in the following way

$$IL = \frac{P_{out}}{P_{in}} \ . \tag{4.69}$$

In the following analysis, only the parasite resistance of the inductor will be considered because the quality factor of integrated capacitors is far bigger than integrated inductors. Note that, in this network, the parasite is in series with the output resistance. In resonance, the capacitor and equivalent inductor form an open circuit leaving only the series combination of the output resistance and parasite resistor. The current is common on both components meaning that the insertion loss comes down to the following

$$IL = \frac{V_{out} \cdot i_1}{V_{in} \cdot i_1} = \frac{\frac{R_{out}}{R_{out}+R_{loss}} \cdot V_{in}}{V_{in}} = \frac{R_{out}}{R_{out} + R_{loss}} \ . \tag{4.70}$$

Putting R_{out} in evidence one can obtain the following expression

$$IL = \frac{1}{1 + \frac{R_{loss}}{R_{out}}} \ . \tag{4.71}$$

The R_{loss} and R_{out} were obtained from the tank quality factor

$$R_{out} = r_{out} \cdot \left(1 + {Q_T}^2\right) \ , \tag{4.72}$$

$$R_{loss} = r_{loss} \cdot \left(1 + {Q_T}^2\right) \ . \tag{4.73}$$

Replacing (4.72) and (4.73) in (4.71), one obtains equations (4.74)

$$IL = \frac{1}{1 + \frac{r_{loss}}{r_{out}}} \tag{4.74}$$

Assuming that $r_{out} \gg r_{loss}$, the tank quality factor approximates to $\frac{2\pi \cdot L \cdot f}{r_{out}}$. Using (4.74) and dividing both resistances by $2\pi \cdot L \cdot f$, we arrive at the following expression

$$IL = \frac{1}{1 + \frac{r_{loss} \cdot \frac{1}{2\pi \cdot L \cdot f}}{r_{out} \cdot \frac{1}{2\pi \cdot L \cdot f}}} = \frac{1}{1 + \frac{Q_T}{Q_L}} \ . \tag{4.75}$$

Equation (4.75), expresses a very interesting result. Assuming that the intrinsic inductor quality factor, Q_L, does not change considerably then if we want a bigger input resistance the insertion loss is greater. This is one way of analysing the expression. The other is that if the matching ratio does not need to be big, more lossy components can be used saving some bucks.

4.5.5 Impedance Decrease

4.5.5.1 Ideal Scenario

Consider the circuit in Fig. 4.14. The process is similar to the impedance boosting case. This time, the opposite transformation will be used. The shunt capacitor and resistor will be transformed into a series circuit. The series capacitor and resistor can be given

$$r_p = \frac{R_p}{(1+Q^2)} \,, \tag{4.76}$$

$$c_p = C_p \cdot (1+Q^{-2}) \,, \tag{4.77}$$

The quality factor can be given by the following expression

$$Q = R_p \cdot 2\pi \cdot f_c \cdot C_p \,. \tag{4.78}$$

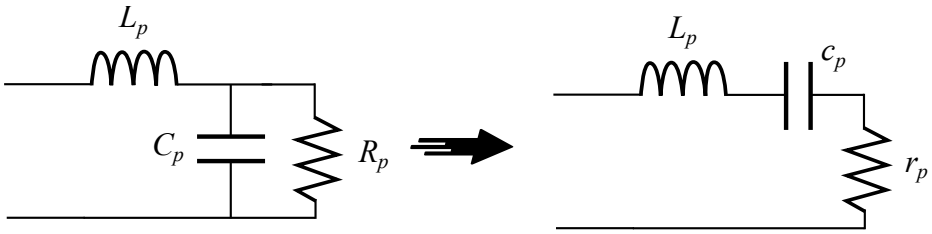


Figure 4.14: Impedance Drop.

4.5.5.2 Real Scenario

Despite the transformation being opposite to the impedance boost case, the parasite resistance and the output resistance are in series. This means that the insertion loss, assuming that $r_{out} \gg r_{loss}$, will have the same value

$$IL = \frac{1}{1+\frac{Q_T}{Q_L}} \,. \tag{4.79}$$

4.6 Optimum output resistance

4.6.1 Introduction

If the real components were ideal, this subsection would not be needed. Unfortunately, the real components have parasitic reactance and resistance. To aggravate the situation even more, in integrated circuits due to the nature of silicon and geometry, there are great losses, especially in inductors. The real capacitors also have losses, but when compared to the inductor losses, it is a needle in the haystack. The study of the inductor's losses is the primary subject of this section. A brief overview of all kinds of inductors will be given. Understanding the resistive losses in the inductor quantitatively allows two main goals: Know exactly the quality factor needed to transform a resistance and know exactly the optimum resistance that maximizes the tank efficiency. These two goals will guide the section workflow.

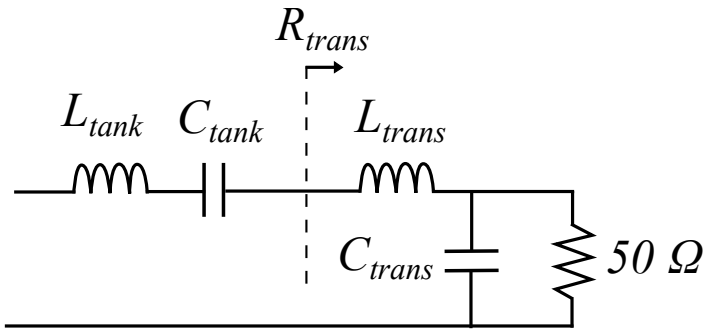


Figure 4.15: Tank output schematic.

4.6.2 Inductors Flavours

Monolithic on-chip inductors or also called planar spiral inductors are formed with metal layers on top of a substrate which is usually silicon. The metal layers can be implemented on one layer or to increase the inductance or the metal layers can be piled up in a spiral geometry. The geometry of the metal layers can change, resulting in different inductor geometries such as square, octagonal or circular. The difference between these geometries will be discussed further. The big disadvantage of on-chip inductors is definitely the low-quality factor which results in severe resistive losses. On the other hand, being integrated means that a monolithic chip can be built, making the mass production process cheaper.

There are three important metrics to bear in mind when characterizing an integrated inductor. The first is the maximum inductance value achievable for a given frequency. The second is the Self Ressonant Frequency (SRF) which, in short, is the frequency that separates the inductor from having an inductance or capacitive behaviour. Keeping this value far from the working frequency is a plus because the inductor is less sensitive to variations and the behaviour is quasi-static. Last but not least, the quality factor. This metric quantifies the amount of energy loss per cycle to resistive sources. In integrated inductors, the maximum quality factor is around 12 which is quite low when compared to discrete solutions which can achieve a quality factor of 100. The resistive losses come from the metal layer resistance, the skin effect that happens at higher frequencies where the electrons tend to flow only in the outer part of the metal layer increasing the resistance. Also since there are alternating currents in the metal layers there are ever-changing magnetic fields which induce currents in the adjacent turns and in the substrate. It is important to mention the quality factors mentioned throughout this section and the next. When one talks about the quality factor it can refer to the intrinsic quality factor of the component or to the quality factor of the band-pass filter. As it was mentioned there are different inductors geometries, square, octagonal, or circular. Each of these geometries has its cons and pros which are mainly involved with the metrics already discussed. Table 4.2 resumes the properties of each geometry

Table 4.2: Different inductors geometries.

Inductors Geometries	Quality Factor	Maximum L	SRF
Square Inductor	Bad	Very Good	Good
Octagonal Inductor	Good	Good	Good
Circular Inductor	Good	Good	Good

4.6.3 How to choose the right tank quality factor

Reminding the reader that the ultimate goal is to have the biggest bandwidth possible and the biggest tank efficiency what value should the quality factor take, the lowest possible, the highest possible or a middle term? This is indeed a very pertinent question. Relative to the bandwidth, the (-3 dB) bandwidth of the tank can be given by equation (4.80).

$$BW = \frac{f}{Q} \, . \tag{4.80}$$

where f is the central frequency and Q is the quality factor. If the highest bandwidth is desired, surely the lowest quality factor should be considered. Furthermore, the tank optimum resistance is given as follows

$$R_{out} = \frac{2\pi \cdot f \cdot L_{tank} - R_{parasite} \cdot Q}{Q} \tag{4.81}$$

Also, the tank efficiency is naturally given by the following equation

$$\varphi_{tank} = \frac{R_{out}}{R_{out} + R_{parasite}} \, . \tag{4.82}$$

Clearly, it can be seen that the lower the quality factor becomes, the better because the output resistance becomes very large and becomes relatively bigger than the inductor parasite resistance, $R_{parasite}$. Not everything is flowers and roses. In the analysis of the class E, it was assumed a single harmonic sinusoid at the output. This clearly becomes unfeasible if the quality factor is too low. This as it was stated, changes the conditions considered in the analysis but it also disrupts the harmonic purity at the output. As more and more harmonics appear at the output resistance the waveform gets further away from a sinusoid which is not definitely desirable. For this reasons, the initial chosen quality factor value was **4**

4.6.4 Inductor characteristics extraction

With the quality factor question settled, it is time to explain how the inductor characteristics were extracted. The software used was Cadence virtuoso and the inductor model was provided from United Microelectronics Corporation (UMC). Unfortunately, the inductor value cannot be swept directly as a manual optimization button must be pressed for the inductor value to change. This being said, to change the inductor value the parameters

that characterize the inductor must be swept. Namely, the outer diameter, the metal width, and the number of turns. After the sweep, there are a lot of points and a mess because a lot of inductance values are repeated in the process, or the quality factor changed dramatically from one point to another. To illustrate this mess of points, Fig 4.16 is a good aid.

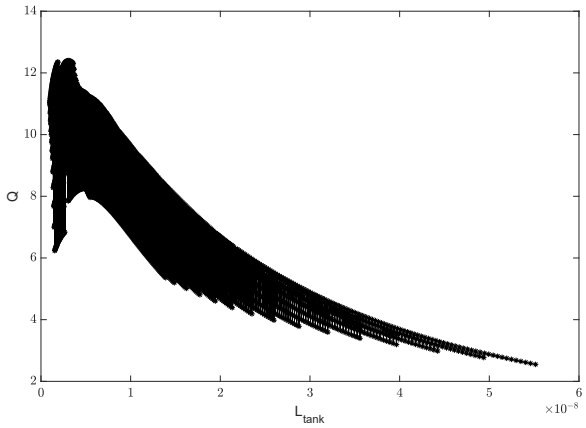
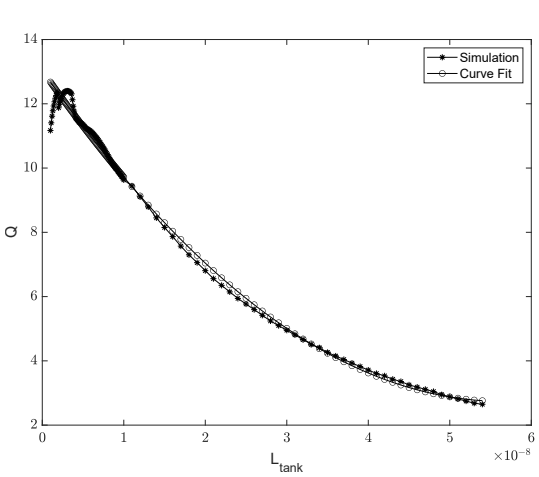


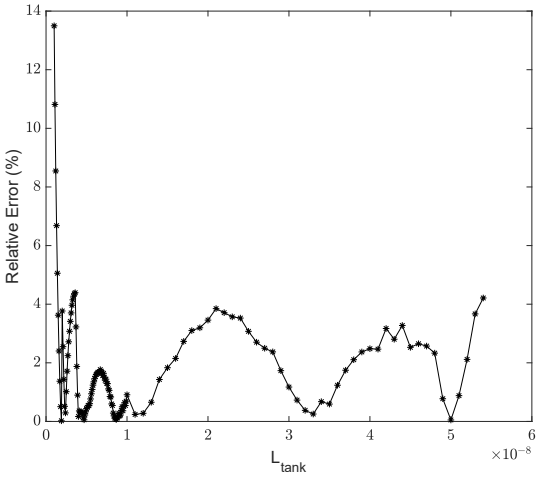
Figure 4.16: Quality factor variation with tank inductor in bulk.

This result is not workable, and no effective conclusions can be taken. To filter the data, the inductor value was rounded. What to do with all the inductor value redundancy? The criteria was to choose the best quality factor amongst the repeated inductor values. After this step, the relation between the quality factor and inductor values looks far cleaner as can be observed in Fig. 4.17. The curve fit was obtained in Matlab by using the function "fit", producing the relation between the quality factor and the inductor value expressed in equation 4.83.

$$Q_{curve\ fit} = 3.22 \cdot 10^{15} \cdot L^2 \ - \ 3.64{\cdot}10^{8} \cdot L \ + \ 13.04\ . \tag{4.83}$$



(a) Quality factor variation with inductor value.



(b) Relative error of parametrization.

Figure 4.17: Quality factor variation with tank inductor.

With this powerful curve description in hand, it is now possible to calculate the tank efficiency. Using the equation 4.81, and assuming a quality factor of **4** the necessary output resistance can be observed in Fig 4.18. Starting with the output resistance, it presents a quadratic behaviour which is corroborated by the curve fit of the quality factor relation with the inductor value. The reader may ask why there is no data from a certain tank inductor point. It could be that the inductor used does not achieve such inductance values. The explanation lies in the fact that at these points the tank inductor parasite resistance is so big that it complies with the quality factor alone. Adding an output resistance at these points would decrease the quality factor. In Fig. 4.19 a), the reader can see the parasite resistance dependency on the tank inductor. The theoretical and simulation curve is practically aligned except for a range of inductor values. This effect reflects on the tank efficiency as it can be stated in Fig. 4.19 b)

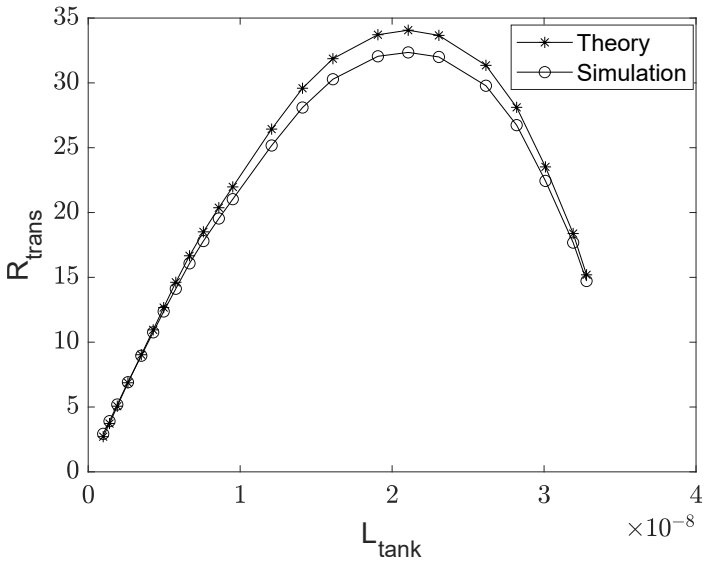
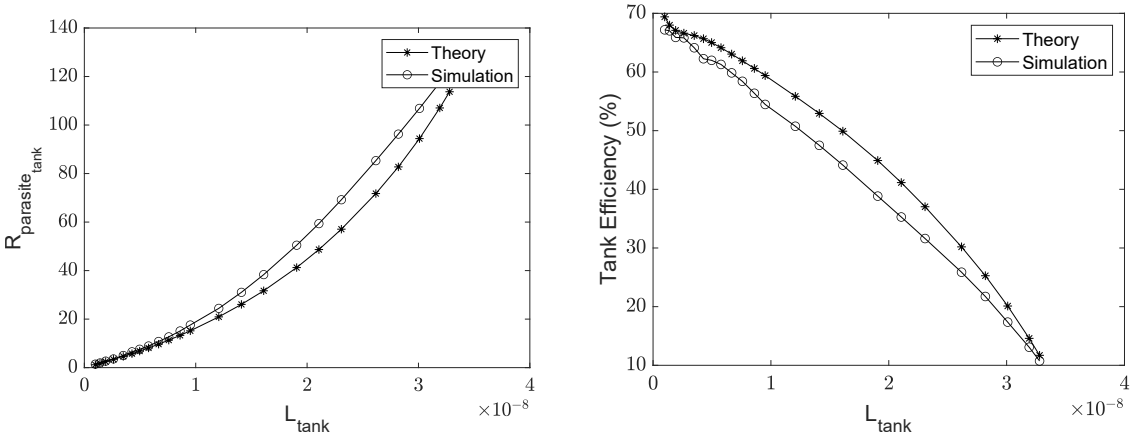


Figure 4.18: Transformation Resistance variation with the tank inductor.

One thing that cannot go unmentioned is the discrepancy between the theory and simulation data in Fig. 4.18. This transformation resistance is affected by the impedance transformation part of the tank. The explanation for the disparity can be found in Fig. 4.20. Note that for some transformation quality factor, the simulation transformation resistance is lower. The reason for this is unknown but nevertheless, it does not matter because these points do not correspond to optimum points. This behaviour is not supported by Fig. 4.21 (a) where a much more reasonable and logical behaviour takes place. The discrepancy can be explained by the parametrization where the parabolic behaviour was assumed linear (Fig. 4.17 (a)). This difference between simulation and theoretical results justifies the difference in impedance transformation efficiency as it is depicted in Fig. 4.21 (b). Note that in Fig. 4.20, the theoretical resistance ignoring the parasite resistance is pretty close to the theoretical one. This indicates that the parasite resistance is relatively small. This can be corroborated by looking once again at Fig. 4.21 (b) where the approximation curve



(a) Tank inductor parasite resistance variation with tank inductor value

(b) Tank efficiency variation with tank inductor value

Figure 4.19: Tank performance theoretical and simulation comparison.

using equation 4.79 is fairly close to the theoretical curve. This makes sense because the parasite resistance is considerably smaller than 50 Ω

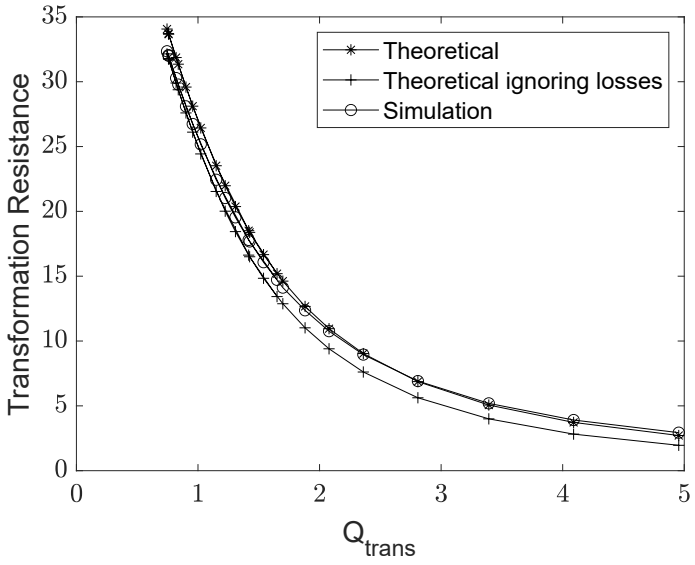
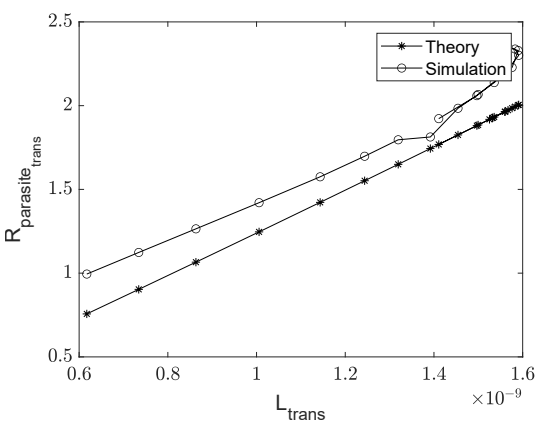
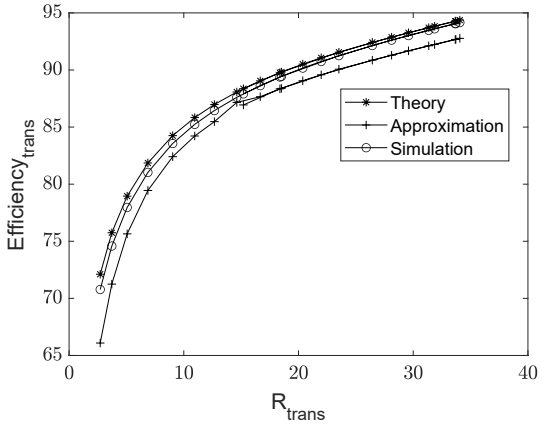


Figure 4.20: Transformation Resistance variation with impedance transformation quality factor.

The total efficiency is illustrated in Fig. 4.22. The simulation curve is below the theoretical one because the inductor tank parasite resistance is slightly higher as it can observed in Fig. 4.19 (a). The optimum resistance occurs for a total resistance of **22.74** with an efficiency of around **52 %**.



(a) Transformation inductor resistance variation with transformation inductor value



(b) Transformation efficiency variation with transformation resistance

Figure 4.21: Impedance Transformation performance theoretical and simulation comparison.

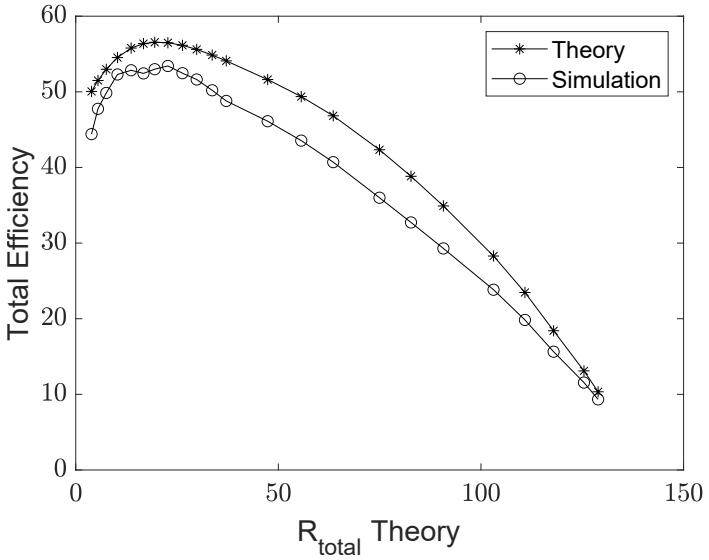


Figure 4.22: Total efficiency variation with theoretical total resistance.

4.7 Transistor on-resistance parametrization

The transistor for Vd_{sat} larger than 0, can have three relatively distinguishable regions. The saturation region, where the drain source voltage surpasses Vd_{sat}. In this region, the transistor can be approximated to a current source and a large parallel resistance. Then there is a triode region where the transistor is equivalent to a current source and a parallel resistance whose value will depend on the nominal drain source voltage. More interestingly to switching operations, there is the deep triode region. In this region, the transistor can be seen as a resistance. As so, the transistor on-resistance term, strictly speaking, is only valid when the values of the drain source voltage are substantially low.

From mathematical terms, the drain source current, in the triode region, is given by

$$I_D = \frac{W}{L} \cdot K_n \cdot \left[(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{{V_{DS}}^2}{2} \right] . \tag{4.84}$$

It is quite intuitive that for low values of V_{DS}, the expression turns into equation (4.85).

$$I_D = \frac{W}{L} \cdot K_n \cdot (V_{GS} - V_{TH}) \cdot V_{DS} . \tag{4.85}$$

For a fixed value of V_{GS}, the relation in (8.47) assumes a linear behaviour and a resistance can be interpreted

$$r_{on} = \frac{L}{K_n \cdot W \cdot (V_{GS} - V_{TH})} . \tag{4.86}$$

The details of the simulation steps can be found in the appendix B. In Fig. 4.23, the theoretical and simulated curve of the on-resistance can be observed for four different frequencies. The first observation is that the simulated curves don't differ much with the variation of the frequency which makes sense because the channel conditions don't change much as long as the operating frequency is far from the transition frequency. For low width values which is the same of saying for high resistance values, the simulated curves and theoretical curves are quite far apart. This happens because as the on-resistance increases, the drain voltage increases making the deep triode approximation less accurate. This won't pose an issue because, as it will be seen in the following chapters, the optimum point of PAE is obtained when the r_{on} falls in relatively small values. With this idea in mind, for on-resistance values lower than 6 Ω, the theoretical formula presents a relative error lower than 10 %, if a correction factor of **2.12** is applied. The relative error with this correction factor is depicted in Fig. 4.24 (b). This error would ideally be 0 but it is okay because as it will be seen in the design section, a small variation of transistor width is done to make sure the circuit is working at its optimum point. This analysis already helps a lot because there is a simple expression that relates the transistor width with its on-resistance

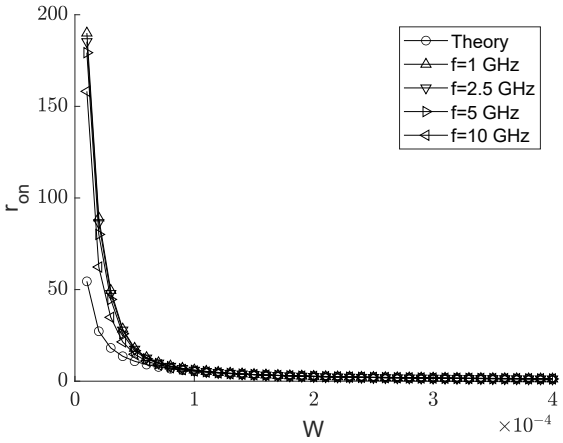
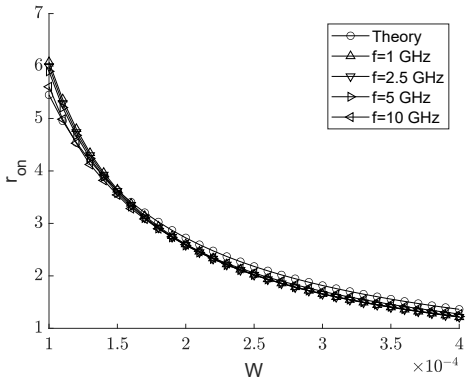
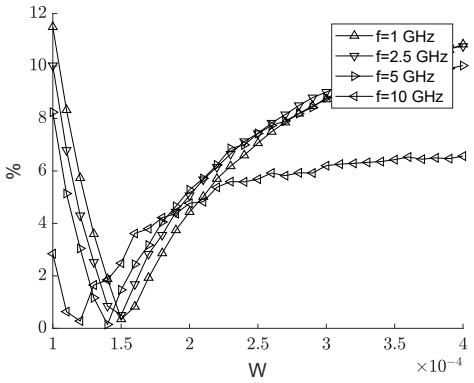


Figure 4.23: r_{on} variation with transistor width for different frequency values.



(a) r_{on} variation with transistor width for r_{on} lower than 6 Ω



(b) Relative Error between theoretical expression with correction factor and simulated values for r_{on} lower than 6 Ω

Figure 4.24: r_{on} optimum parametrization

4.8 Class D power driver

The class D schematic can be seen in Fig. 4.25. It is formed by a PMOS and NMOS transistor. This class can be used as a Power Amplifying stage or a Driver stage. As a driver stage, it is a simple and effective choice as it is quite easy to scale the driver based on the maximum output power of the FPGA. Besides that, its design is quite easy to understand. When this class is used as a driver, it works as an inverter. In other words, when a voltage equal to V_{DD} is present at the input and assuming that the output capacitor is charged, the NMOS transistor will discharge the output capacitor and lower the output voltage to 0. Similarly, when a voltage equal to 0 is present at the input, the PMOS transistor will charge the output capacitance increasing the output voltage to V_{DD}. It is important to mention that this is a very ideal working case. In practice, there might be a common mode as there can't be in nature an infinitely rapid jump from 0 to V_{DD}. Both transistors, take the NMOS for instance, will be initially in saturation and once the output voltage becomes sensibly $V_{DD} - V_{TH}$, the transistor starts to enter in the triode region. The analysis can become quickly cumbersome when including both regions. Instead, let's assume that the saturation approximation is good until the output voltage reaches half of the supply voltage. Let's call this time, the rise time. The time the transistor takes to reach the supply voltage is practically two times the rise time. Assuming that the transistor is in saturation until half of the supply voltage value, the rise time can be defined as

$$t_{rise} = \frac{V_{DD} \cdot C \cdot L}{W \cdot K_n \cdot (V_{GS} - V_{TH})^2}\ , \tag{4.87}$$

where C is the output capacitance, L is the transistor channel length and W is the transistor width. The goal of a driver design is to know the transistor width that produces a determined input power. This can be achieved indirectly using equation 4.87. By decreasing the rise time, which is the same as saying that the transistor width will be swept, one can see

the behaviour of the input power. This resumes the methodology used in designing a class D driver. The design starts by putting an inverter and sweeping the NMOS and PMOS transistor width. By looking at the relations between K_n and K_p, the PMOS transistor width can be defined from the NMOS transistor width. The sweeping will reveal mainly two regions. The first region where the driver input power is lower than the driver output power. The second region is the complete opposite. The first region is preferable since a gain bigger than 1 is a must since the goal of the driver is to breakdown the exigent PA input power to a more accessible input power that can be directly connected to a micro-controller for instance. Then inside the first region, the criteria to choose a final width is the PA output power maximization. After a width is chosen for the first inverter, the input power is evaluated. Is it small enough? If not, another inverter is added, and this process is repeated all over again until the driver input power is small enough. During this process, the PA output power drops which may require an additional design iteration on the PA.

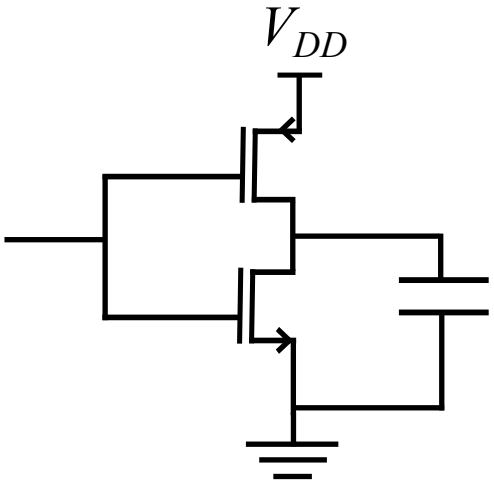


Figure 4.25: Inverter schematic.

5

Power amplification stage design for a QDA with four branches

5.1 Introduction

With the optimum resistance known, the design kit can be put to use to design 4 branches for a mobile version of the Quantized Digital Amplifier (QDA). In the next section, the actual design and optimization will be explained. Starting from a maximum output power restriction the output power of each branch will be derived. Then the design and optimization workflow which is common for all the branches will be explored. Once all the branches are optimized to the fullest, assuming the envelope distribution seen in chapter 2.1.4, the overall drain efficiency and Power Added Efficiency (PAE) will be derived. After that, as a proof of concept, two drivers will be designed for the last branch. Finally, some further optimizations will be applied to the last branch like using a 3.3V transistor to alleviate the drain source stress of the common gate transistor. This could be applied to all the branches but that would be applying the same concept already seen 4 times.

5.2 Four branches design and optimization

5.2.1 Introduction

If the reader reached here without skipping the QDA section, then it understands that the QDA amplifying stage is made up of several parallel power amplifiers. To know the output power of each power amplifier, one needs to know what is the maximum power of the amplifying stage. By consulting [26], the maximum output power considered was 180 mW. For a 4-branch amplifying stage, the minimum output power can be found as follows

$$P_{out} + 2 \cdot P_{out} + 4 \cdot P_{out} + 8 \cdot P_{out} = 0.180\ mW \tag{5.1}$$

$$P_{out} = \frac{0.180}{1+2+4+8} = 12\ mW \tag{5.2}$$

The output power of the other branches follows suit. The output power of each power branch is summarized in Table 5.1.In this calculation, it is assumed that the power losses in the combiner are 0 so the power seen in the table corresponds to the actual output power of each branch. The goal is to naturally obtain the desired output power for each

Table 5.1: Branch's Output Power.

Branch 1	12 mW
Branch 2	24 mW
Branch 3	48 mW
Branch 4	96 mW

branch with the highest efficiency possible. Besides that, to properly judge if the analysis of the class E is worth it, this latter will be compared with an analysis where the transistor on-resistance is 0. It is interesting to see if there is convergence as the output power increase in both designs. If not investigate the reason why. Moving on to the design part, the core question is what values to choose for q and m. Note that the output power on each design is fixed. This means that the output resistance is a consequence of q and m. The design strategy can be better understood by analysing Fig 5.1.

For high values of m, the transistor on-resistance is high which results in low input power. However, the power losses in the on-resistance are higher resulting in a low drain efficiency. For low values of m, the drain efficiency is high but the input power increase can result in undesirable PAE values. Relative to the q variable, for low values of q the additional reactance component is an inductor which is not good news for the overall efficiency. As the q increases the additional reactive component becomes a capacitor and the output resistance gets close to the desired value already seen in the previous chapter. The optimum q and m point lies somewhere in the middle.

This rather not precise decision especially on the value of m comes from the fact that the parametrization of the input power with the transistor width is something not that easy. The input power is not a linear matter because it does not only depend on the transistor parasitic capacitance's. In normal conditions, the turn ON voltage would be 0. This means the drain is already at 0 volt and the gate drain capacitance will be charged right away. When the drain-voltage is not 0, the transistor will have to discharge the parasitic capacitance, namely the drain-gate capacitance and then charge it afterwards. This means that the input power is not only a matter of the value of the parasitic capacitances but also on what are the conditions when the transistor turns on. This justifies the difficult task it is to have a clear relationship between the width of the transistor and input power.

Instead of trying to find a relation between those two entities a simpler strategy will be used. Since a careful study on the optimum output resistance was done, that variable is known prior to the design. This means that the only unknown variables are q and m.

The m was varied on a range of values and as consequence, the value of q can be found. In the simulation for each value of m, the performance is measured and conclusion are taken based on what is the m that maximizes the PAE for the desired output power.

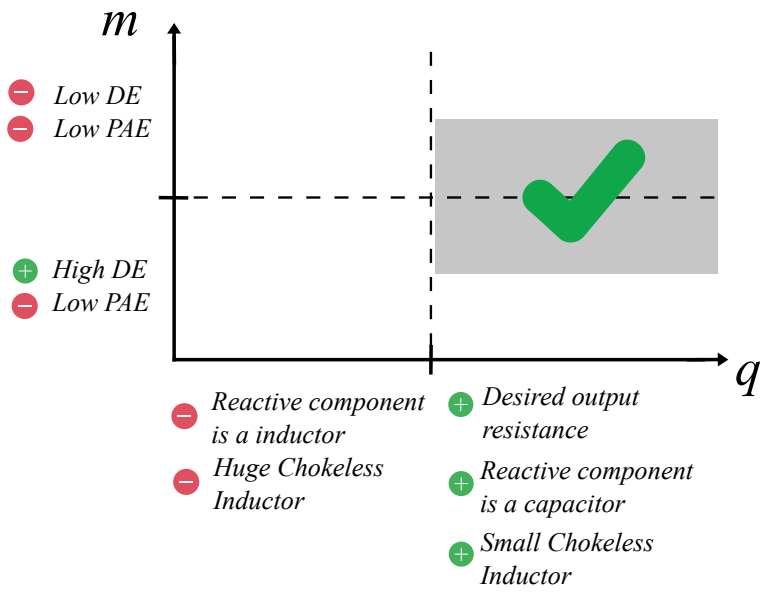


Figure 5.1: Design strategy for class E circuit.

Once the value of q is set and the range of values of m to test is decided, what is the next step? Obviously, the parameters of the circuit for each value of m will be introduced in the simulator. By doing only this, the reader can note that the output power will not coincide with the desired and the PAE will be quite far from what can be considered good. There are two reasons for this. The first is that the transistor on-resistance has some error associated and as so, the width of the transistor must be corrected.

With the r_{on} fixed, there is another problem which is the transistor parasitic capacitances. To account for the existence of parasitic capacitances the shunt capacitor value must be reduced until the desired output power is achieved. This refinement can be observed graphically in Fig. 5.2. Relative to the design considering the transistor on-resistance as ideal, the only step in the simulator was to find the best transistor width that maximized the PAE.

After the best q and m point is known, the tank efficiency will be studied in order to reinforce the idea that the chosen output resistance is indeed the best one possible for the desired quality factor. Another reason to study the tank efficiency again is that in the previous chapter, the tank was studied with a single harmonic at the input. It was not in the conditions the tank will be in class E case. This study despite having been applied to all the branches only will be discussed in the first branch section.

Due to the maximum voltage, a cascode solution is opted. Analysing this cascode solution from a theoretical standpoint can be future work, but in the meantime, global optimization is used. When the cascode solution is implemented, the PAE drops quite considerably due to the parasitic capacitances of an additional transistor. Besides that, the

common gate transistor switching between the triode region and saturation increases the power losses. The optimizer is Cadence's propriety so no further details are not available. The design steps are almost complete. The last step is to see the variation of output power and PAE when the input power changes. Using the ideal driver may not be the best option and a trade-off can be achieved where the drain efficiency does not change much to an input power change.

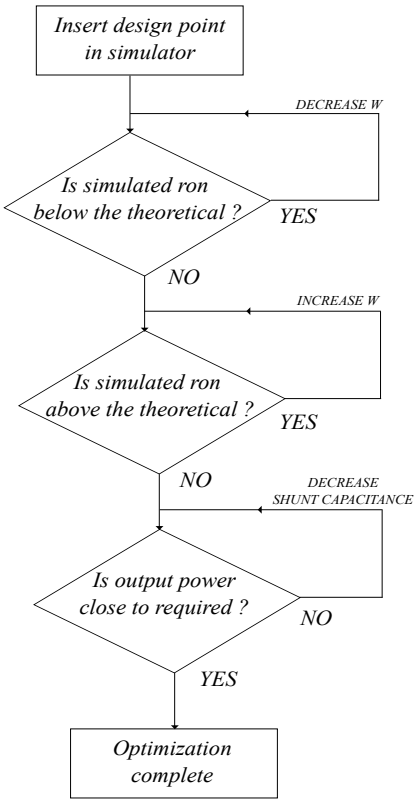


Figure 5.2: First iteration strategy.

5.2.2 First Branch

5.2.2.1 Design

For the first branch, we need 12 mW so, in light of the conclusions regarding the optimum resistance, the designed output power should be sensibly 23.1 mW. The design space can be seen in Fig. 5.3. Relative to the output resistance, the dotted line represents a resistance value of 22.74 Ω which corresponds to the optimum output resistance. For a q too low as it was mentioned in the introduction, the reactive component is positive which represents an inductor reactance, the chokeless inductor is prohibitively big. With all this in mind, the m was swept. The q value, for each m value, was adjusted to guarantee the optimum output resistance. The coordinates of (q,m) chosen can be seen in Table 5.2. For each of the q values, the circuit was also designed to admit the transistor on-resistance as being ideal.

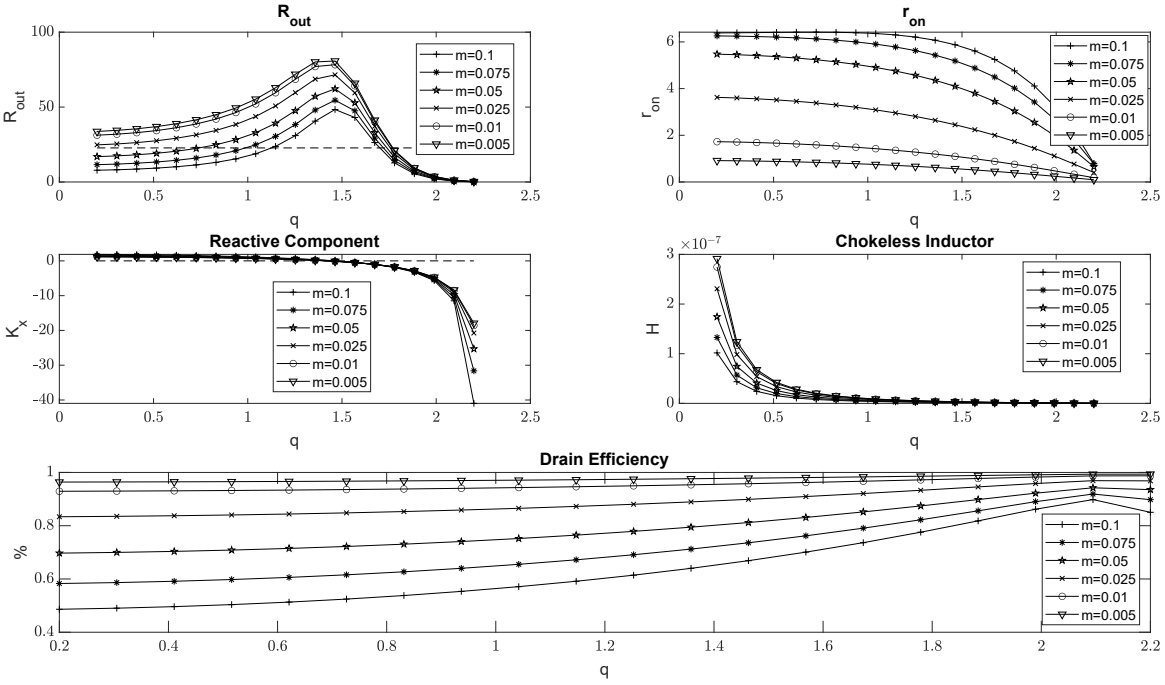


Figure 5.3: First Branch Design Space.

Table 5.2: Design variables coordinates (q,m) for the first branch.

q	1.6968	1.714	1.7324	1.7515	1.7637	1.768
m	0.1	0.075	0.05	0.025	0.01	0.005

5.2.2.2 Simulation

In Fig. 5.4 (a), the output power for different values of m can be observed. Note that the output power of the design considering a non-ideal transistor and ignoring the transistor on-resistance is independent of the design value, m. This occurs because the value of q between the design points is practically constant. Secondly, it is clear that the output power of that design is far from the goal. One could argue that the design kit ignoring the transistor on-resistance is faulty. This would be a plausible thought but, note the output power of that design with an ideal transistor. It is right on the desired output power. Even when the on-transistor resistance decreases the output power of that design with a real transistor shows no signs of convergence. This alone justifies a more careful analysis to see where the designs meet. This topic will be explored in section 5.6.

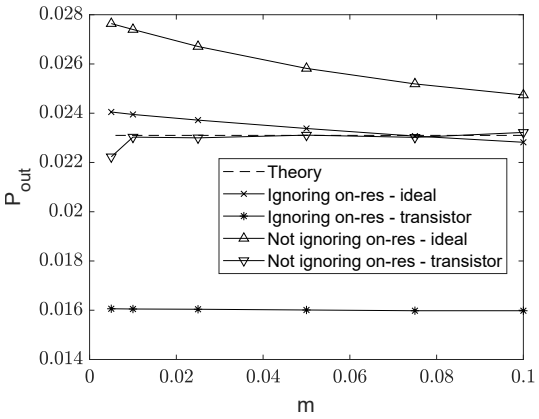
The output power of the design considering the on-resistance and assuming a real transistor follows relatively well the desired output power until a certain value of m. After that, it starts failing short. This happens because as the value of m decreases, the transistor width gets larger, increasing the parasitic capacitances. There will be a point than where the parasitic capacitances surpass or are equal to the necessary shunt capacitance.One

curious phenomenon is the fact that the output power in the design considering the on-resistance with the ideal transistor is relatively far from the goal. After all, being ideal should be as close as possible. A possible explanation can be given based on Fig. 5.4 (b) where the transistor power loss is depicted for the design considering the on-resistance. An immediate observation is that the optimization works because the transistor power loss in the case of the real transistor is relatively close to the theoretical loss. Except for smaller values of m but this can be justified by the parasitic capacitances that become dominant. Relative to the ideal transistor case, the power losses are far greater. This might indicate that a slight refinement needs to be done even in the ideal case. This idea is reinforced by looking at Fig. 5.5 where the drain voltage variation with time can be observed. Note that in the ideal case, in both designs, the turn ON condition is not met. This phenomenon is representative that maybe the current flowing in the switch might not be equal to the desired, making all the remaining currents follow suit. The reader could now ask why the design considering the on-resistance ideal follows so well the desired output power. The explanation lies in the fact that there is no path for losses. Due to this, in Fig. 5.6 (a), the DE of the design considering the transistor on-resistance with ideal transistor falls short and it is even below the PAE with the real transistor. This is naturally due to the power losses being lower in the latter but also the input power compared with the output power is substantially lower.

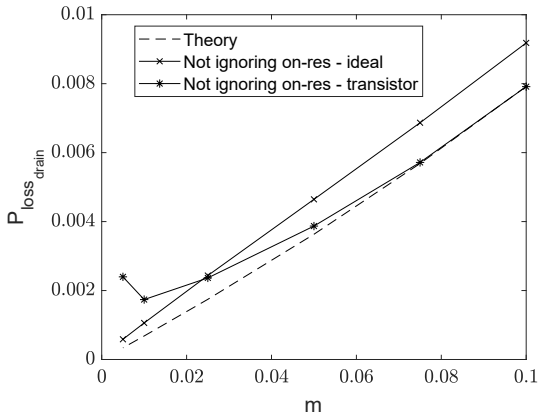
In Fig. 5.6 (b) one can see the PAE of the design ignoring the transistor on-resistance with an ideal / not-ideal transistor. It is here mainly to state that there is potential in these designs since their PAE are high. However, if the output power is not obtained in design considering a real transistor, additional work will have to be spent on optimizers.

Last but not least, in Fig. 5.7 the expected behaviour between input power and conduction resistance is remarked. As it was prospected in the design stage, there is a clear trade-off between the transistor on-resistance and the input power. The transistor on-resistance is inversely proportional to the transistor width and the input power is proportional to the transistor width. One thing to bear in mind is that the parasite capacitances does not tell the whole story. Just note for m=0.075 where the input power is lower where it, according to transistor width only, should be higher. This happens because of the turn ON conditions.

To conclude, the best point in terms of m is 0.025. The optimum components for this m value and after the optimization are resumed in Table 5.3



(a) P_{out} variation with m design variable.



(b) Transistor power loss variation with m design variable.

Figure 5.4: Output power and power losses in the first branch design .

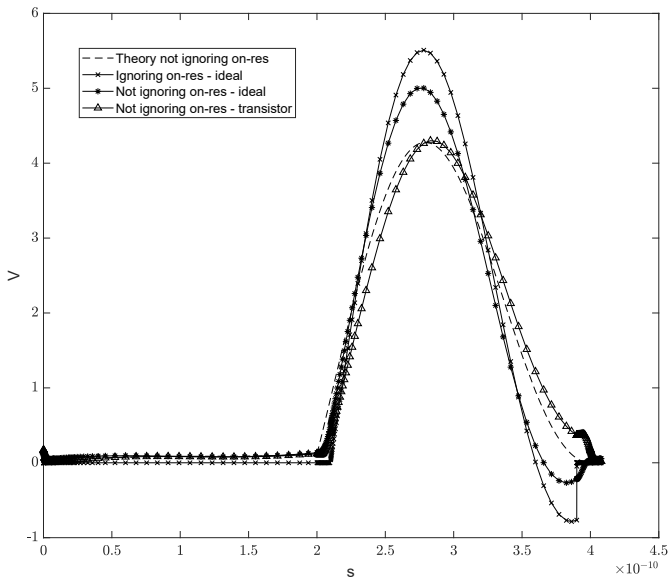
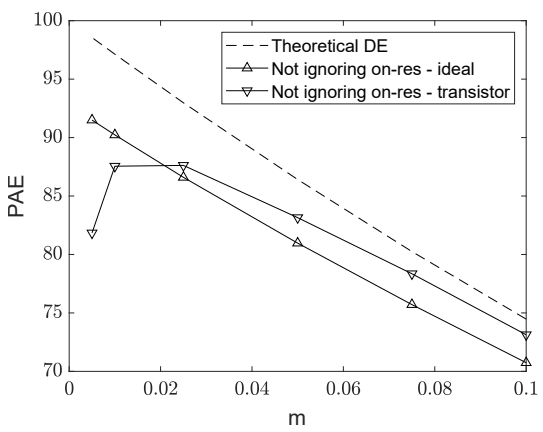


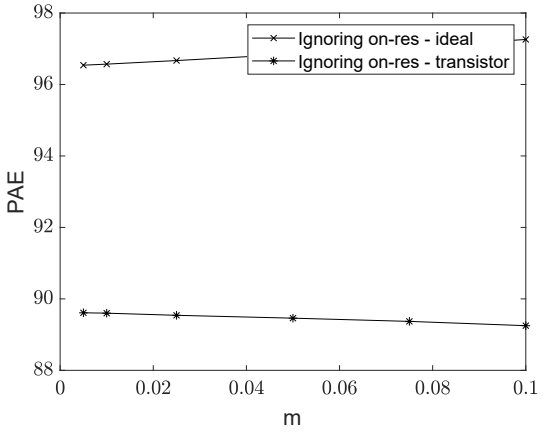
Figure 5.5: Time evolution of the drain voltage in the first branch for m=0.025.

Table 5.3: Components value before and after the first iteration.

Parameters	*Before first iteration*	*After first iteration*
Transistor Width	300 μm	280 μm
Shunt Capacitor	0.880 pF	0.760 pF
Choke Inductor	1.5018 nH	1.5018 nH
Tank Inductor	5.7647 nH	5.7647 nH
Tank Capacitor	0.703 pF	0.703 pF
Tank Additional Reactance	1.821 pF	1.821 pF
Output Resistance	22.76 Ω	22.76 Ω



(a) PAE of the designs accounting the transistor on-resistance.



(b) PAE of the designs considering the transistor on-resistance ideal.

Figure 5.6: PAE comparison on the first branch between the two design kits.

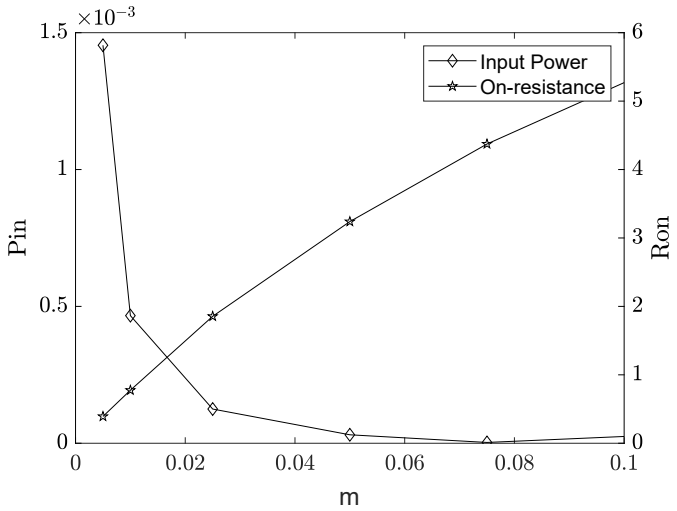


Figure 5.7: Input power and on-resistance variation with m design variable on the first branch

5.2.2.3 Tank Analysis

Now that a better idea between the different design's performance and the best design point in terms of PAE is known, a tank analysis will be performed to see if the efficiencies check right. When putting the real inductor, the imaginary part did not correspond to the original design, resulting in less input power at the tank input. To correct this, the value of the additional reactance was increased. The results obtained are shown in Table 5.4. Note that the theoretical results and the results from the AC have already been discussed in the previous chapter.

The Periodic Steady State analysis (PSS) simulation results are interesting enough. These results were obtained with the tank connected to the rest of the class E circuit, unlike the AC analysis. Possibly because of that, the results are slightly different. For instance, the tank inductor parasite resistance is lower, contributing to a higher tank efficiency. Note

that calculating the tank efficiency with the parasite resistance and the transformation resistance is going to give a slightly lower result. This might be because of the PSS analysis uncertainty. Nevertheless, the total efficiency result from the PSS analysis will be taken into account in the optimization stage in the output power restriction.

Table 5.4: First branch tank performance for different analysis

Parameters	*Theory*	*AC Simulation*	*PSS Simulation*
Inductor Tank $R_{parasite}$ (Ω)	8.118	8.960	7.692
Transformation Tank $R_{parasite}$ (Ω)	1.744	1.892	1.893
Transformation Resistance (Ω)	14.62	14.18	14.18
Total Resistance (Ω)	22.74	23.14	22.53
Tank Efficiency (%)	64.14	61.29	69.06
Transformation Efficiency (%)	88.07	86.66	86.87
Total Efficiency (%)	56.49	53.11	60.00

5.2.2.4 Optimization

Due to the prohibitive maximum voltage of the class E topology, the cascade solution must be employed. The cascade solution brings inherent problems. The first is that additional capacitances are introduced in a circuit which can disrupt the class E optimum conditions. Besides that, there is another gate consuming power. The solution, right off the bat, could be to duplicate the transistor width of the initial transistor and distribute it equally now in the common source and common gate transistor. That did not prove to be the best solution as the output power obtained was below the desired and the PAE dropped substantially. Because of that, a global optimizer will be used to search for the best solution possible. The constraints can be consulted in Table 5.5. Starting with the PAE, the value choice was based on the initial solution described above. The latter gave a PAE of 73 %. So, in order to push the optimizer, the PAE has a goal of maximization with a reference of 79 %. It is assumed that the maximum drain source voltage stress of the transistor is around twice the nominal voltage (1.2 V) [27]. For that reason, the common gate drain source voltage was restricted to 2.6 V. The reader will understand better the decision for this value at the end of this subsection. To finish the constraints, the desired output power is left. Based on the tank analysis subsection, the tank's total efficiency is around 60% resulting in a necessary tank input power of 20 mW. Because of the uncertainty of the PSS analysis, a 2 mW additional power was given to that value. This accounts for the tank losses in the inductor, but it does not account for the losses in the choke inductor parasitic resistance. As an approximation let's consider the current through the choke inductor in the first design. Using that approximated current and the approximated parasitic resistance value we get to a power loss of around 1.83 mW. Note that the higher the output power, the higher the current in the inductor hence more output losses. Let's add then a 2 mW

margin to that value. Summing everything up, the estimated necessary output power is around 24 mW. Using this value, a range of desired output power was defined and can be observed in Table 5.5.

Table 5.5: First branch optimizer Restrictions.

Parameters	*Specification*
Output Power	26 mW < ... > 23 mW
Maximum Voltage	< 2.6 V
Power Added Efficiency	max 79%

The output of the optimizer revealed some good design points candidates. The maximum PAE achieved was 78.7 % and the corresponding design parameters can be observed in Table 5.6. What makes a good design point candidate is that the PAE is maximized while keeping the maximum drain source voltage of the common gate transistor below twice the nominal voltage. Note that in the optimizer definition, this voltage was defined to be below 2.6. This can be justified by the fact that the choke inductor has a series parasitic resistance. This creates an additional voltage drop allowing the designer to be tolerant in the definition of this parameter. The output power should be such that in the final design minor changes are done to the circuit, preserving the good PAE achieved. With this idea in mind, the chosen candidate was number 3, for two reasons. The first reason is that between candidate points 2 and 3 the PAE does not differ much, and the maximum voltage is relatively lower in candidate 3, which is good to increase the longevity of the transistors. Candidate point 1 was discarded to detriment of the third because of the maximum voltage and also because of the output resistance which is further from the optimum resistance. The chosen design point has the values of the components described in Table 5.7

Table 5.6: First branch optimizer Best Results.

Design Points	*PAE(%)*	*Max. Voltage (V)*	*Output Power(mW)*	*Total Resistance(Ω)*
Best PAE point	78.7	2.763	28.66	21
Candidate Point 2	77.48	2.622	27.20	24
Candidate Point 3	77.31	2.505	26.28	23

The next step is to add the tank with the impedance transformation already and replace all ideal inductors with real ones. After this step, the obtained output power was 11.8 mW. This value was increased by increasing the additional tank reactance to 2.5 pF. The last step remaining is to replace the ideal capacitors with real ones. The final circuit specifications can be consulted in Table 5.8.

Table 5.7: First branch chose design point components description.

Component	*Value*
Common Source Transistor Width (μm)	390
Common Gate Transistor Width (μm)	270
Shunt Capacitor (pF)	1
Choke Inductor (nH)	1.2
Tank Capacitor (pF)	0.703
Tank Inductor (nH)	5.765
Additional Tank Reactance (pF)	2.3
Transformation Inductor (nH)	1.39
Transformation Capacitor (pF)	2.16
Output Resistance (Ω)	50

Table 5.8: Fist Branch final design parameters

Parameters	*Values*
Output power (mW)	12.08
Supply power (mW)	40.57
Bandwidth (MHz)	400
Total tank efficiency (%)	52.35
PAE (%)	28.50
Common source input power (μW)	522.5
Common gate input power (μW)	0.903
Total Resistance (Ω)	22.26
Maximum Drain Source voltage of CG	1.953
Maximum Drain Source voltage of CS	1.474

5.2.3 Fourth Branch

5.2.3.1 Design

In this branch, the selection of the optimum total tank resistance became more challenging. As a first approach, the resistance chosen was 7.5 Ω. For this resistance, the tank's total efficiency is, theoretically, around 50 %. Since the desired output power is 96 mW, the output power designed was 192 mW. The design space can be observed in Table 5.8. The design coordinates (q,m) can be consulted in Table 5.9

Table 5.9: Design variables coordinates (q,m) of the fourth branch.

q	1.552	1.577	1.585
m	0.025	0.01	0.005

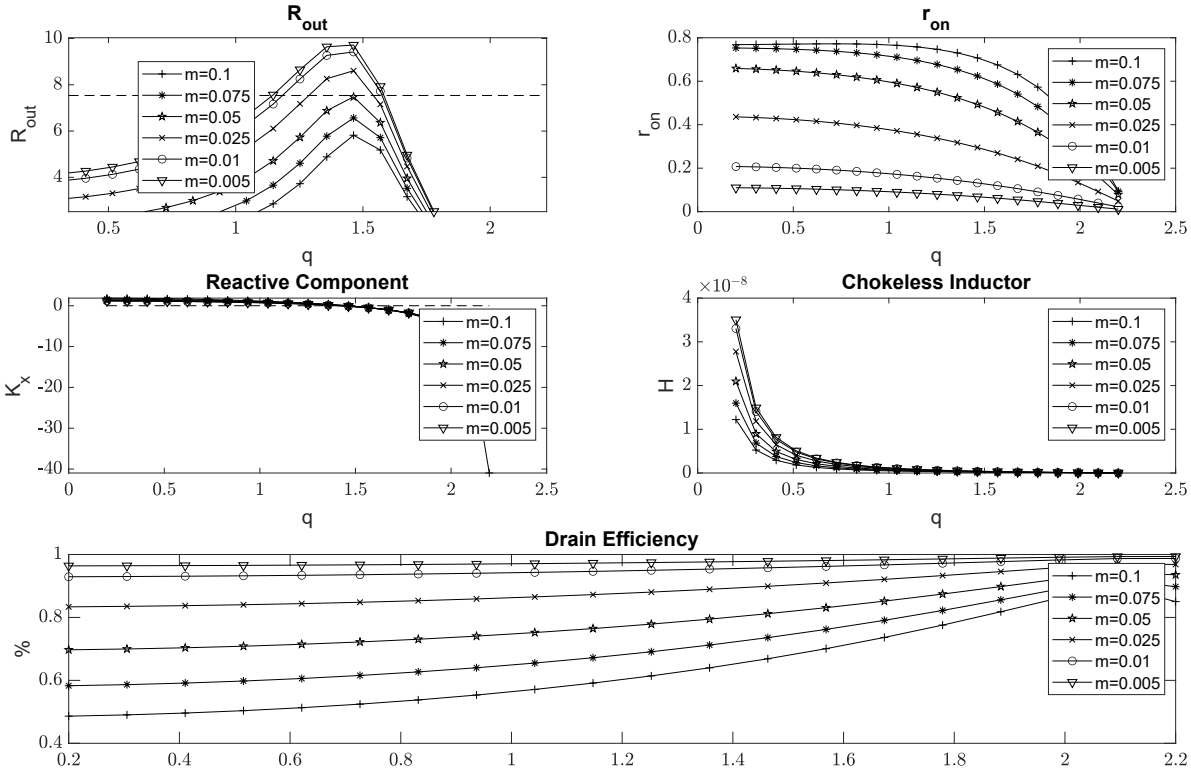
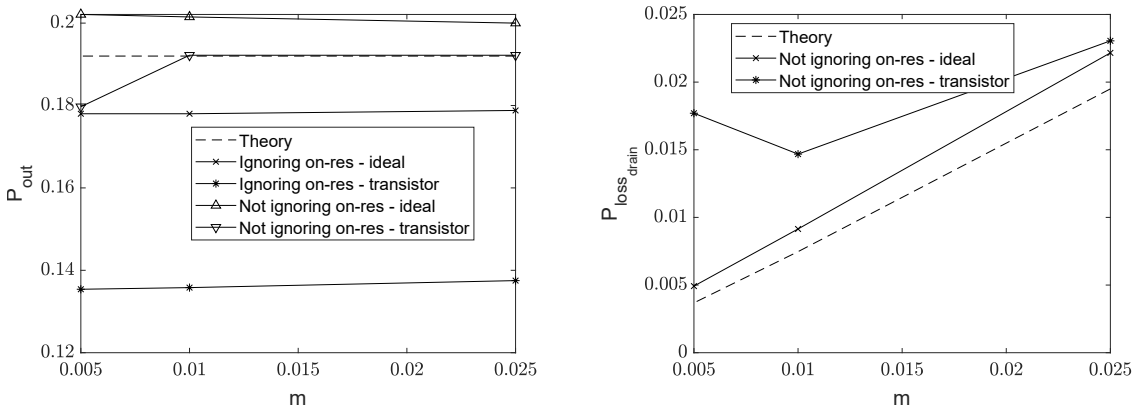


Figure 5.8: Fourth Branch Design Space.

5.2.3.2 Simulation



(a) P_{out} variation with m design variable.

(b) Transistor power loss variation with m design variable.

Figure 5.9: Output power and power losses in the fourth branch design.

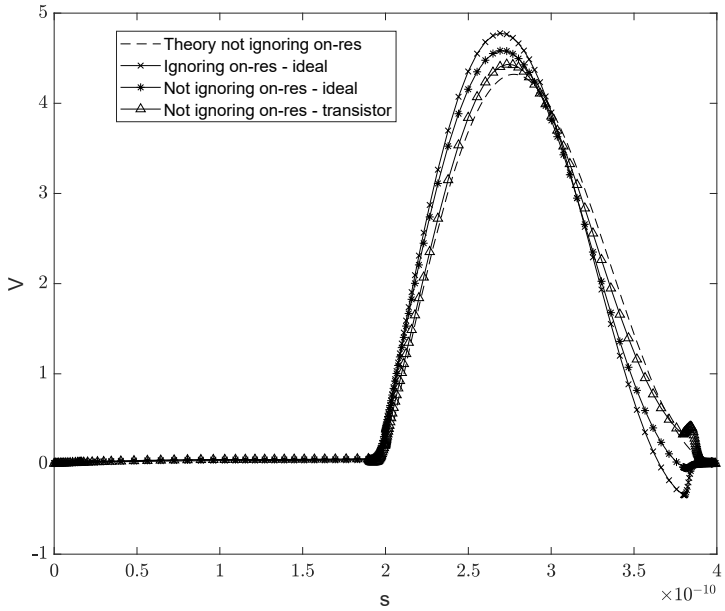
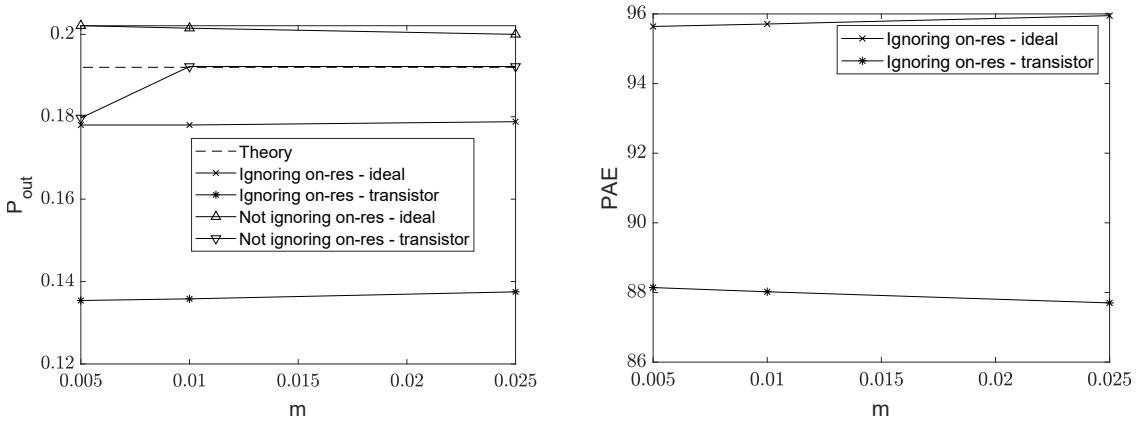


Figure 5.10: Time evolution of the drain voltage in the fourth branch for m=0.01.



(a) PAE of the designs accounting the transistor on-resistance.

(b) PAE of the designs considering the transistor on-resistance ideal.

Figure 5.11: PAE comparison on the fourth branch between the two design kits.

Table 5.10: Fourth branch components value before and after the first optimization.

Parameters	*Before first iteration*	*After first iteration*
Transistor Width	4530 μu	4100 μu
Shunt Capacitor	5.37 pF	2.18 pF
Choke Inductor	0.303 nH	0.303 nH
Tank Inductor	1.915 nH	1.915 nH
Tank Capacitor	2.116 pF	2.116 pF
Tank Additional Reactance	15.79 pF	15.79 pF
Output Resistance	7.5 Ω	7.5 Ω

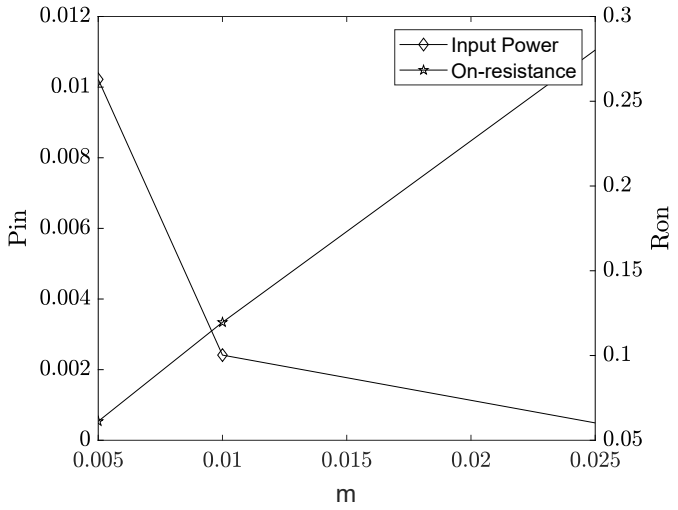


Figure 5.12: Input power and on-resistance variation with m design variable on 4th branch.

5.2.3.3 Tank Analysis

For higher output powers, the total tank resistance is lower. Based on the results from chapter 5, the overall tank efficiency will be lower. This can be corroborated once again by Table 5.11. Note that despite the discrepancies between the AC and PSS simulation, the tendency is correct.

Table 5.11: Fourth branch comparison between tank performance for different analysis.

Parameters	***Theory***	***AC Simulation***	***PSS Simulation***
Inductor Tank $R_{parasite}$ (Ω)	2.4739	2.687	2.647
Transformation Tank $R_{parasite}$ (Ω)	1.0656	1.265	1.265
Transformation Resistance (Ω)	5.0632	5.193	5.191
Total Resistance (Ω)	7.537	7.88	7.846
Tank Efficiency (%)	67.10	65.99	67.82
Transformation Efficiency (%)	78.95	75.65	75.68
Total Efficiency (%)	52.98	49.85	51.33

5.2.3.4 Optimization

In the first approach, the strategy used to account for the overall tank efficiency and the approximated loss in the choke inductor was considered. By the overall tank efficiency a minimum output power of 188 mW. The approximated loss in the choke inductor is 46.52 mW. This amounts to a total approximated power of 234.52 mW. This quantity did not produce the desired optimization results in the sense that the output power is far from the expected. After three iterations, the optimizer restrictions can be observed in Table 5.12

Looking at the three best candidates in Table 5.13, it becomes clear why so many iterations were necessary. First, note the difference between the initial designed output

Table 5.12: Fourth branch optimizer restrictions.

Parameters	*Specification*
Output Power	310 mW < ... > 370 mW
Maximum Voltage	< 2.6V
Power Added Efficiency	max 78%

power and the current output power. Adding to that, the output resistance is remarkably lower. The best PAE point was discarded because of the output power which, unfortunately, is not high enough. Between candidate points, two and three the decision leaned more toward the second candidate because of the maximum voltage restriction. The chosen design point component's value can be consulted in Table 5.14

Table 5.13: Fourth branch optimizer best results.

Design Points	*PAE(%)*	*Max Voltage(V)*	*Output Power(mW)*	*Total Resistance(Ω)*
Best PAE point	79.51	3.00	264	5.5
Candidate Point 2	77.32	2.64	324	3.5
Candidate Point 3	77.95	2.88	325	3.5

Table 5.14: Fourth branch chose design point components description.

Component	*Value*
Common Source Transistor Width (μm)	4580
Common Gate Transistor Width (μm)	4820
Shunt Capacitor (pF)	2.5
Choke Inductor (nH)	0.2
Tank Capacitor (pF)	4.1092
Tank Inductor (nH)	0.986
Additional Tank Reactance (pF)	30
Transformation Inductor (nH)	0.617
Transformation Capacitor (pF)	6.308
Output Resistance (Ω)	50

After replacing the ideal components with their real parts, the output power was fairly close to the desired output power. Because of that, there was no need to further iterations or minor corrections. The final design parameters can be observed in Table 5.15.

Table 5.15: Final design parameters.

Parameters	*Values*
Output power (mW)	96.25
Supply Power (mW)	408.2
Bandwidth (MHz)	455
Total Tank Efficiency (%)	40.6 %
PAE (%)	22.29
Common source input power (mW)	5.252
Common gate input power (μW)	6.207
Total Resistance (Ω)	4.782
Maximum Drain Source voltage of CG	2.372
Maximum Drain Source voltage of CS	1.502

5.3 Overall efficiency calculation

A summary of the 4 branches' characteristics can be observed in Fig. 5.13. From chapter 2.1.4, it is known that the Orthogonal Frequency Division Multiplexing (OFDM) envelope amplitude follows a Rayleigh distribution. Besides that, in the QDA section (3.2.6.1) it was concluded that the best quantized normalized clipping level for 5 quantized bits is around 3.6. To calculate the overall efficiency all that is left to decide is the average power of the OFDM signal. A value can be assigned directly such as the average of the branch's output power or the maximum clipping level can be defined. The latter was defined based on the maximum output power which is 180 mW. This power has a normalized voltage value of 4.24 V. Using equation (5.3), the standard deviation can be calculated.

$$\sigma = \frac{4.24}{3.6} = 1.178\ . \tag{5.3}$$

The Rayleigh distribution can now be defined and can be observed in Fig. 5.14. Since the most significant bit is for defining the polarity, in reality, to calculate the probability using the Rayleigh distribution only 4 bits are relevant. With a maximum clipping voltage equal to 4.24 V and given the quantization levels (16), the step size of the quantizer is 0.283 V. Using this quantizer step, the probability for each of the quantizer levels can be defined. Mathematically, the probability of a quantization level is given by equation (5.4)

$$P_k = \int_{\frac{k}{2}\cdot s_z}^{\frac{k+2}{2}\cdot s_z} \frac{R}{\sigma^2}\cdot e^{-\frac{R^2}{2\cdot\sigma^2}}\ , \tag{5.4}$$

where k represents the quantized level and s_z the quantizer step size. For each of the quantizer levels, one, two or all of the PA's can be working. Considering the digital word $b_k = [a_{k3}\ a_{k2}\ a_{k1}\ a_{k0}]$ which is associated with each of the quantizers levels, the following overall parameters can be defined

$$P_{outk} = a_{k3}\cdot P_{out4th\ Branch} + a_{k2}\cdot P_{out3rd\ Branch} + a_{k1}\cdot P_{out2nd\ Branch} + a_{k0}\cdot P_{out1st\ Branch}\ , \tag{5.5}$$

$$P_{ink} = a_{k3}\cdot P_{in4th\ Branch} + a_{k2}\cdot P_{in3rd\ Branch} + a_{k1}\cdot P_{in2nd\ Branch} + a_{k0}\cdot P_{in1st\ Branch}\ , \tag{5.6}$$

$$P_{DCk} = a_{k3}\cdot P_{DC4th\ Branch} + a_{k2}\cdot P_{DC3rd\ Branch} + a_{k1}\cdot P_{DC2nd\ Branch} + a_{k0}\cdot P_{DC1st\ Branch}\ . \tag{5.7}$$

With these parameters, the PAE associated to each digital word is given by equation (5.8)

$$PAE_k = \frac{P_{outk} - P_{ink}}{P_{DCk}}\ . \tag{5.8}$$

The overall efficiency can be obtained using equation (5.4) and equation (5.8)

$$PAE_{overall} = \sum_{k=0}^{15} PAE_k\cdot P_k = 29.28\%\ . \tag{5.9}$$

The overall PAE value makes sense since the probability of the 4th branch being active is much lower than the probability of the 2nd Branch working, for instance.

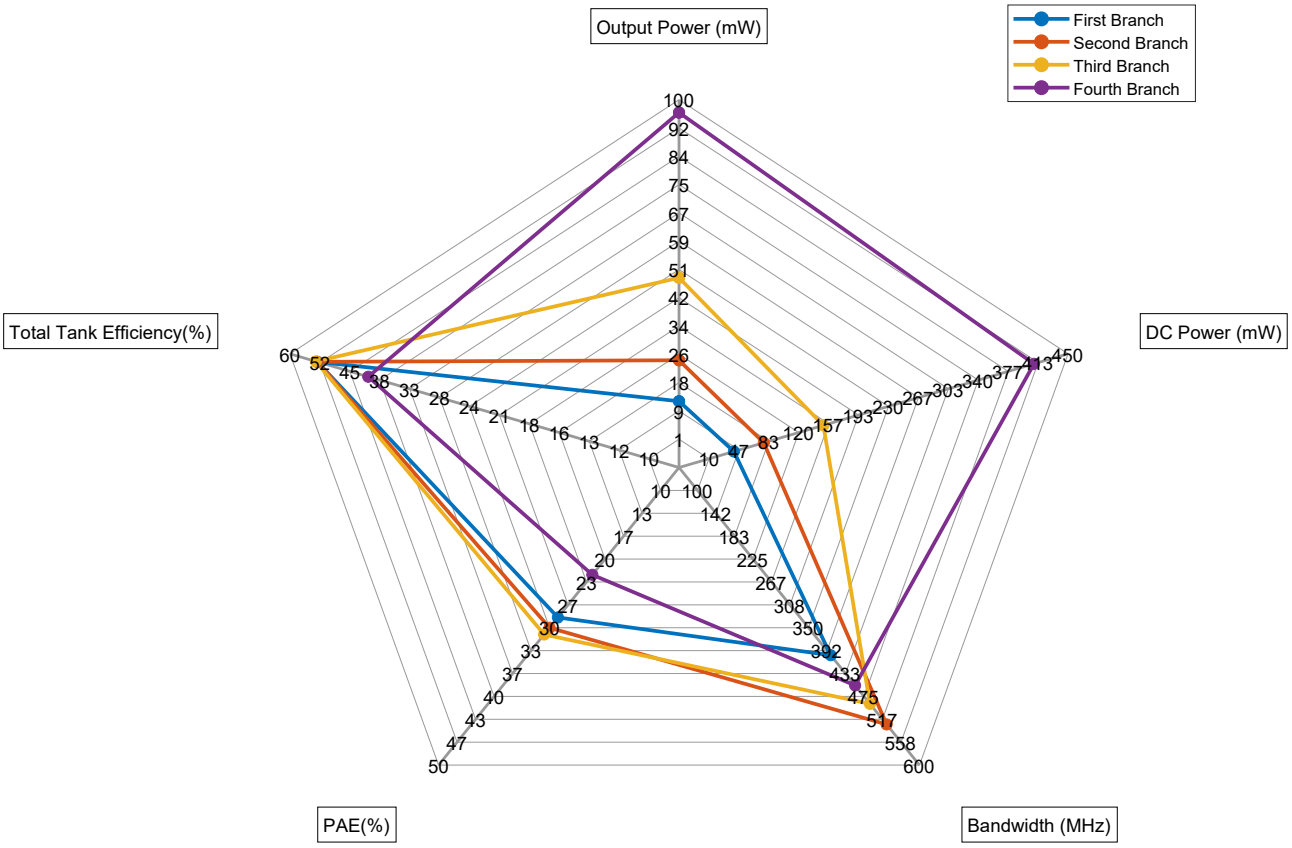


Figure 5.13: Branches Results Summary.

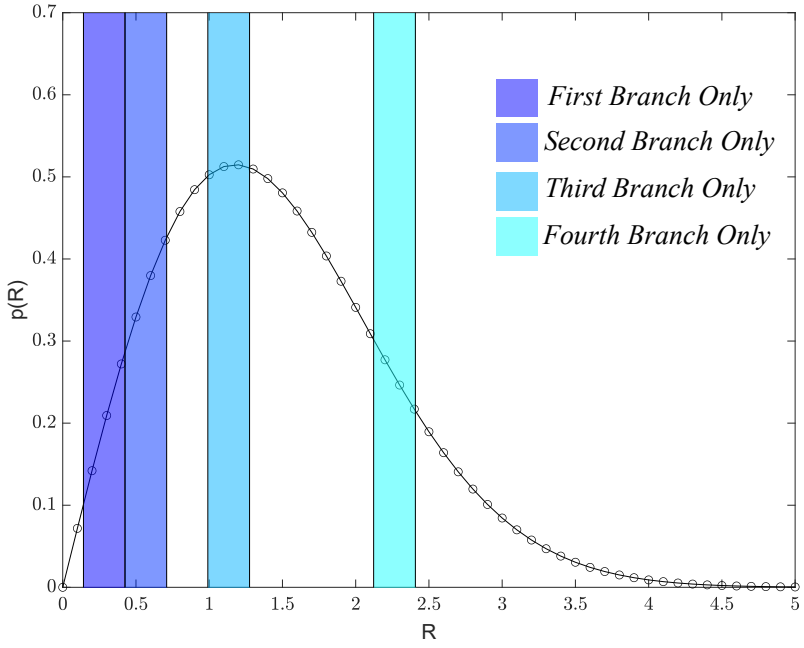


Figure 5.14: Rayleigh Distribution for overall efficiency calculation.

5.4 Power driver on the fourth branch

As proof of concept, a class D inverter will be designed on the fourth branch. It is important to remind the reader that the input power of the fourth branch is not that high and could be easily controlled by a microcontroller. Nevertheless, understanding the design process has added value. The design will not be input power restricted but instead let's design a 3-inverter class D driver. After putting the first inverter, the transistor's widths were swept and the best point resulted in the characteristic described in Table 5.16. Note that, the driver input power might be counter-intuitive to what was said in chapter 5. This indicates that maybe one driver might not do the job. After putting the second inverter,

Table 5.16: Driver first inverter.

Component	*Value*
NMOS transistor width (μm)	192
PMOS transistor width (μm)	692
Driver input power (mW)	1.238
Driver output power (mW)	0.624
PA output power (mW)	91.58

the characteristics are much more favourable as it can be observed in Table 5.17

Table 5.17: Driver second inverter.

Component	*Value*
NMOS transistor width (μm)	88
PMOS transistor width (μm)	317
Driver input power (mW)	0.585
Driver output power (mW)	0.959
PA output power (mW)	95.23

Finally, after the third inverter insertion, there was a drop in the PA output power at which can be observed in Table 5.18. As a trade for that, the driver input power dropped. To correct the PA output power a new design iteration was done. The driver's overall efficiency was 47%

Table 5.18: Driver third inverter.

Component	*Value*
NMOS transistor width (μm)	16
PMOS transistor width (μm)	58
Driver input power (mW)	0.101
Driver output power (mW)	1.084
PA output power (mW)	96.03

5.5 Further optimization

The goal of this section has three main goals. One of the goals is to find ways to improve the PAE. The reader caught a glimpse of how to improve the PAE in the design section. It is directly related to the quality factor. The quality factor chosen was 4 based on the waveform deformation with ideal components. With real components, it was observed that the waveform improved its sinusoidal shape. Another goal is to try to alleviate the voltage stress on the transistors. Since no reliability simulation was applied, there is no accurate way to know if the choice of the maximum voltage stress reduces substantially the transistor lifespan. In order to avoid reliability estimations, the transistors will be replaced by their 3.3V versions. The disadvantage of the latter transistors is that the channel length cannot be lower than 360 nm. This might be a problem since that for the same on-resistance, the transistor width has to be quite higher. Last but not least, to solidly assert the superiority of the developed design kit, the optimizer results and amount of points needed will be compared using the first optimization designs from each design kit as an optimizer starting point.

5.5.1 3.3V Transistor

In the design process, it was assumed that the maximum drain-source voltage would be twice the nominal voltage. With no reliability analysis, it is not certain how much of the transistor life span is being reduced. If the transistors could be replaced by transistors that operate at a higher nominal voltage the problem would be solved. In that sense, the transistors were replaced by their 3.3V version. A first design considered the output power of the 4th branch with a design variable coordinates (q,m) equal to (1.552,0.025). The first problem of this transistor version is that the transistor length is limited to three times the channel length of the original transistor. This has repercussions in the width needed to achieve the same on-resistance as the reader can observe in Table 5.19. With the same design goals, the 3.3 V transistor version fails to achieve the desired output power. The reason is that the parasitic capacitances are far bigger than the required shunt capacitance. This effect can also be seen by comparing the two transistors input powers. For this reason, this type of transistor is not reliable. Even if one used the optimizer and the desired output

power value was achieved, the PAE would be lower which is not a desirable scenario.

Table 5.19: Comparison between 1.2 V and 3.3 V transistor.

Type of Transistor	*Output Power (mW)*	*Input Power*	*DC Power (mW)*	*PAE(%)*
1.2V Transistor	192.2	491.9 μW	216.5	88.54
3.3V Transistor	176.7	27.14 mW	198.9	75.23

5.5.2 Optimizer Comparison

The optimizer results will be compared when using two different starting points: One is the first optimization design point from the developed design kit and the other is the first optimization point from the design kit considering an ideal on-resistance. The goal is to see if there is any advantage of the developed design kit since an optimization process is always inherent. As a first approach, the design variables interval was set the same for both design kits. The number of points evaluated in both situations was practically the same. What is important to compare, is the results that can be observed in Table 5.20. These results were picked based on the output power used for achieving the desired output power with a real component. Despite a slightly better efficiency in the developed design kit, no conclusions can be taken.

Table 5.20: First optimization approach comparison.

Starting Points	*Output Power (mW)*	*Maximum Voltage (V)*	*PAE(%)*
Design kit considering on-resistance	26.92	2.70	77.10
Design kit ideal on-resistance	26.85	2.63	76.50

The problem of this first approach is that the design variables interval was defined so that both starting points could be inside. This can prove an unrealistic situation, or it could mean that, for the design kit with ideal on-resistance to achieve the same results as the developed design kit many iterations are needed. To prove this last point, for each design kit the design variables have the same interval except for the output resistance which will be defined differently depending on the design kit. The results of this approach can be consulted in Table 5.21. The advantage of the developed design kit is now clearer. Combining these results with the results from the first approach, the natural conclusion is that if one uses a design kit considering the on-resistance ideal then more iterations will be needed. The attentive reader can argue that the first approach PAE from the design kit considering the on-resistance ideal is quite close to the second approach PAE from the developed design kit. That is indeed a good question, but I remind the reader that in the first approach the output resistance is much larger than in the second. In other words, the

first approach took around 6 hours with 2554 points evaluated while the second approach took 5 hours with 1972 points evaluated.

Table 5.21: Second optimization approach comparison.

Starting Points	*Output Power (mW)*	*Maximum Voltage (V)*	*PAE(%)*
Design kit considering on-resistance	26.72	2.64	77.45
Design kit ideal on-resistance	26.25	2.60	75.00

The last question is whether the starting point has some relevant impact or it's just the design variables interval. This problem was investigated using only the developed design kit. In Table 5.22 that question can be demystified and the conclusion is that the starting point has little or no relevance.

Table 5.22: Study of the starting point impact.

Starting Points	*Output Power (mW)*	*Maximum Voltage (V)*	*PAE(%)*
Design kit considering on-resistance	26.72	2.64	77.45
Design kit ideal on-resistance	26.71	2.48	77.21

5.5.3 Quality factor reduction

In the design stage, the bandwidth of the fourth branch was slightly better. This happened because the tank quality factor was reduced. Despite this change, the output waveform still resembled a sinusoid. This might indicate that the selection of the quality factor was rather conservative. The choice of the quality factor was based on comparing the output waveform in the design containing ideal components. The real components are frequency independent. This means that the reactance and quality factor change with the frequency. This is beneficial because, for example, as the frequency increases the inductor quality factor increases as well. As a consequence, the impedance for those frequencies increases, leading ever more to the fundamental harmonic isolation. Reducing the quality factor brings the advantage of a higher tank overall efficiency and higher bandwidth. The main goal of this section is to understand how far the quality factor can be reduced and with that improve the PAE. In order to achieve that, the first branch will be used. In the same way, the second branch could be used. The third branch and fourth branch demand a lower output resistance hence a lower tank efficiency.

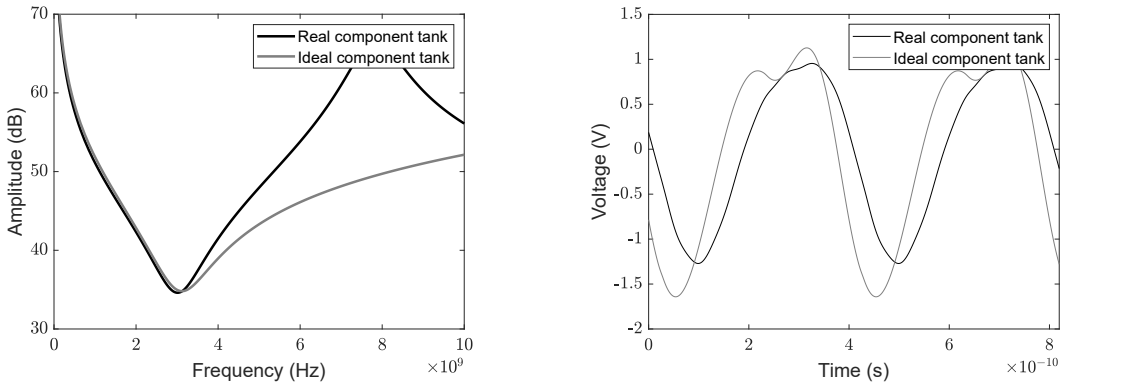
The tank quality factor chosen was **2**. The maximum overall tank efficiency has a value equal to 79.19 % for a total resistance of around 55 Ω. Despite there being no simulation data of the tank efficiency, based on the previous design, the best point is around the maximum tank efficiency. With the overall resistance value known, the next step is to choose the design coordinates (q,m) which based on previous designs knowledge was

chosen to be (1.692,0.01). The selected design point component's values can be observed in Table 5.23.

Table 5.23: Design point component's value of circuit with a quality factor equal to two.

Components	*Value*
Shunt capacitance (pF)	0.487
Choke inductor (nH)	2.907
Transistor width (μm)	410.0
Tank inductor (nH)	7.072
Tank capacitor (pF)	0.573
Transf. inductor (nH)	1.029
Transf. capacitor (pF)	0.467
Output resistance (Ω)	50

The simulation results, after using the already known optimization methodology, are according to the theoretical values. At this point, it is relevant to compare the tank frequency response and the output waveform between the tank with real and ideal components. In Fig. 5.15 (a), the output wave-forms of a real and ideal tank can be observed. Note that in the ideal case the waveform is slightly worse looking. The reason for that can be found in Fig. 5.15 (b). Note that for the same quality factor, the tank with real components presents a higher impedance value at the next harmonic. This happens because the inductors are frequency dependent. For lower frequencies than the working frequency, the reactance and consequently the quality factor remains practically unaltered. For higher frequencies close to the inductor's self-resonant frequency, the quality factor is much larger.



(a) Frequency Response comparison

(b) Output Voltage variation with time comparison

Figure 5.15: Comparison between real components tank and ideal components tank

The next step is to use the optimizer just like in the design stage of the power amplifiers section. The only change is that the quality factor is going to be increased. This can help the optimizer to achieve the best PAE possible without accounting for the losses due to

harmonic content at the output of the circuit. With the optimization completed, there were many possibilities as design point to implement with real components. It was chosen by some candidates and tested in a circuit where the only real component was the choke inductor. The simulation parameters with the best point is shown in Table 5.24. Note that the simulation PAE is different from the optimizer result. The reason lies in the fact that besides the real choke inductor the quality factor used in the optimizer was higher.

Table 5.24: Comparison between all ideal circuit and circuit with real choke inductor.

Parameters	*Optimizer Result*	*Simulation with real choke ind.*
Output power (mW)	17.24	15.06
DC Power (mW)	21.73	24.62
CS input power (μW)	297.6	319.0
CG input power (μW)	0.715	0.051
PAE (%)	77.96	59.88

The natural step now is to replace the tank with real components. The simulation parameters of the final circuit and the comparison with the design considering the quality factor equal to 4 can be observed in Table 5.25.

Table 5.25: Comparison between circuits with different quality factors.

Parameters	*Quality factor = 2*	*Quality factor = 4*
Output power (mW)	12.04	12.08
DC Power (mW)	15.93	40.57
CS input power (μW)	291.2	522.6
CG input power (μW)	0.403	0.847
Total tank efficiency (%)	75.55	52.35
Bandwidth (MHz)	1148	400
PAE (%)	46.15	28.5

It is interesting to compare the output waveform between all these designs. In Fig. 5.16 the output waveform of the circuit with the optimization point only considering the choke inductor with real components and the final circuit with all the real components for a quality factor of 2 is depicted. This result makes sense and supports the explanation given at the beginning of this sub section. In Fig. 5.17 (a) the output waveform of the final circuit with a quality factor of 4 and the output waveform of the final circuit with a quality factor of 2 can be observed. It is noticeable some waveform degradation. To better understand this degradation, the Fig. 5.17 (b) shows the harmonic content of both output voltages

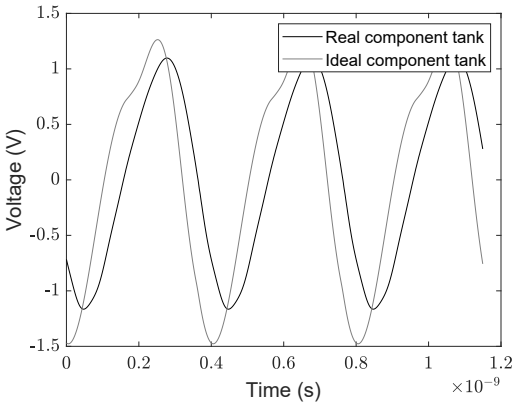
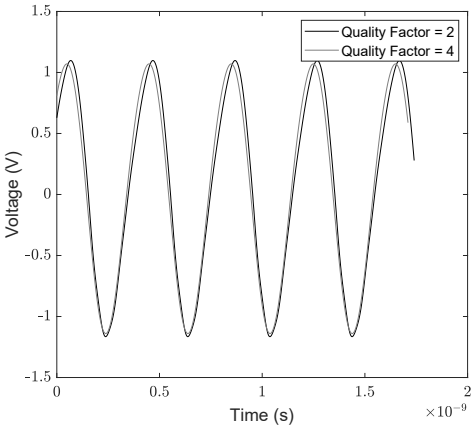
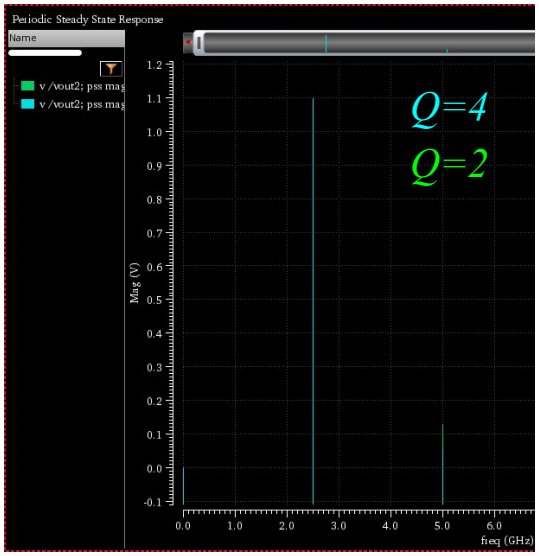


Figure 5.16: Final circuit voltage comparison between ideal and real component tank.

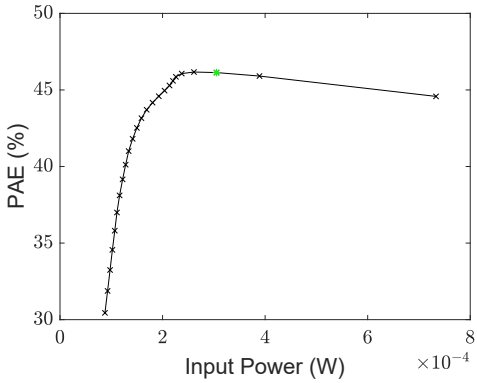


(a) Time Voltage comparison.

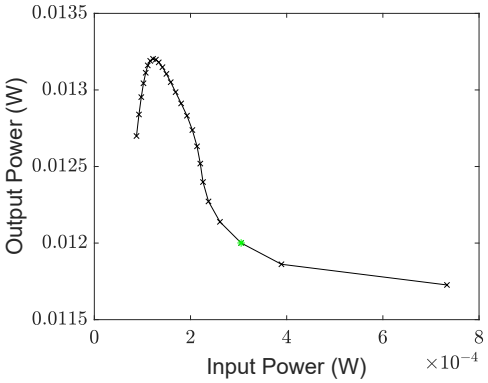


(b) Harmonic comparison.

Figure 5.17: Comparison between two different quality factor circuits.



(a) PAE variation with input power



(b) Output power variation with input power

Figure 5.18: Effect of input power variation

5.6 Discussion of the branches design and results

Starting from the beginning, the transistor on-resistance parametrization was a good step to bridge the design kit and the simulation since the former does not have an explicit relation between the on-resistance and the transistor width. The reader may be thinking if this step was really necessary since the width could be just varied until the transistor on-resistance was desired. By doing the on-resistance parametrization not only the formulas are corroborated but most importantly a first width estimate is obtained meaning that the number of changes in the simulation relative to the transistor width is minimal. Note that, for a lower output on-resistance the number of changes needed was greater due to the asymptotic relation between the transistor width and on-resistance.

The inductor study allowed us to explore the different kinds of integrated inductors and their advantages and disadvantages. In the integrated world, especially the losses in the inductors, nothing should be taken for granted. The inductor parametrizations empower the designer to choose the best tank output resistance. It is funny enough that the best output resistance for the selected quality factor it's approximately a middle term between the best resistance for the impedance transformation which is 50 Ω and the best resistance for the tank which is the lowest possible (ideally 0).

The decision in the design stage boiled down to the selection of a design coordinate (q,m) where the optimal resistance was possible, the additional reactance was a capacitor and the choke inductor was as lowest as possible. The design strategy of choosing a set of m values allowed to know what is the value of m that translates into a higher PAE and allowed, in the optimization process, to compare with the design kit considering the transistor on-resistance 0.

The results speak for themselves as there is a clear advantage of the developed design kit not much because the PAE is far superior but because the output power, after the first optimization, is exactly the desired. The first optimization proved to be effective and confirmed the prediction that the transistor parasite capacitance affects the class E optimal conditions. Furthermore, the error of the transistor on-resistance was clearly visible in this process and because of that easily fixable. One thing common to all the branches, in this first optimization stage, is that for the lowest value of m used the output power fell short. The reason for this is that the transistor parasitic capacitances were bigger than the required shunt capacitance.

After this stage, a cascode solution was implemented to alleviate the voltage stress on the common source transistor. The optimization went as expected and the results manifested the inherent trade-off between the transistor widths and the ohmic losses. Throughout this process, the most difficult task was to correctly define the output power boundaries because of the losses in the choke inductor parasitic resistance. This was definitely worse in the last two branches where more than one iteration was needed.

5.7 Comparison with class E existing solutions

In general, the circuits of the state of art followed the same topology. The exception was in [28] where one transistor was implemented in the class E circuit. This means that the voltage stress, with a supply voltage of 2 V, reached around 5.5 V. This alone represents an advantage to the developed design since there are no power losses due to the common gate transistor. In terms of real components, the quality factor of the inductor based on the short information given seems to be similar. Another reason for the high PAE is the fact that the output resistance is implemented outside the chip.

Relative to the designs that used the same topology as the developed, in [29] the topology is the same as the developed design but an additional optimization iteration is performed to reduce the charging and discharging requirements of the common gate transistor. In [30], the main factor that contributed to a high PAE was the use of bond wires which stated a quality factor of around 35.

Based on Table 5.26 the developed circuit is inside the class E design state of the art. In the section where the quality factor reduction was investigated, with the best optimizer design point and adding the choke inductor, the PAE fell down from 78 to 60 %. This clearly indicates that the real components used have a worst performance than some designs present in the state of the art. To corroborate this idea, note that the output power of the developed class E is substantially lower (10 times).

It is not known for sure if the components used in the other designs have a better quality factor. On one hand, from the supply voltage, this could indicate that for a higher power the optimum resistance is achievable. On the other hand, it is known that the higher the output power, the lower the output resistance is, decreasing the overall tank efficiency. This means that for a lower output resistance, the circuit designed in [31] achieved roughly the same tank efficiency, meaning that the components used in the developed design are worse in terms of quality factor. The reader may be wondering if the PAE obtained is valid since no driver was built alongside it. Based on the driver developed in section 5.4, the PAE might drop 1%. Note that for lower technology nodes, the output power decreased due to the maximum current constraints that come with the transistor length reduction. More interestingly, as the transistor length gets smaller, to achieve the same transistor on-resistance less transistor width is needed. This results in smaller parasitic capacitances potentially reducing the input power. However, note that the PAE for smaller technology nodes dropped.

Table 5.26: Class E state of the art.

Ref.'s	*Freq (GHz)*	*Tech.* (nm)	*Foundry*	*Topology*	*Supply Voltage (V)*	*Power (dBm)*	*PAE (%)*
This work	2.5	130	UMC	Cascode	1.2	10.79	46.1
[28]	1.9	180	NovaTek	C.Source	2	16.30	70
[29]	1.7	130	STM	Cascode	2.5	23.00	67.0
[30]	2.4	180	TSMC	Cascode	3.3	23.00	44.5
[31]	2.4	180	-	Cascode	3.3	21.30	40.0
[32]	2.4	180	UMC	Cascode	3.3	17.72	51.9
[33]	1.8	65	TSMC	Cascode	1.2	14.12	38.4
[34]	2.4	90	-	Cascode	1.2	9.00	30

6

Conclusion and future work

Based on the power-hungry mobile systems, finding ways to efficiently use the energy is a must. In initial mobile systems such as 2G and so on, the envelope fluctuation was not critical, allowing the use of linear amplifiers. The linear amplifiers were explored, and the advantages and disadvantages of each topology were exposed. As a proof of concept, a class A Power Amplifier (PA) was developed. With the increase of the envelope fluctuation due to OFDM implementation, the use of linear amplifiers becomes obsolete because the efficiencies are low due to the required power back-off to not distort the signal. To overcome this problem, non-linear PAs are investigated, namely the class E. This topology of PAs can theoretically reach 100%. However, since our signal has a non-constant envelope, efficiency enhancement techniques such as polar modulation or outphasing need to be employed. A new efficiency enhancement technique called Quantized Digital Amplifier (QDA) was exposed. A brief explanation of each block that constitutes this solution was given. The reader after comparing this new technique with existing solutions can clearly see the enormous potential in setting a new Power Added Efficiency (PAE). With a basic understanding of the QDA the reader can understand that to achieve the highest efficiency, it boils down to get a power combiner as lossless as possible and a very efficient power amplifying stage. The aim of this thesis was then to investigate what are the steps necessary to design a class E PA circuit as efficient as possible.

The first step started with the development of a design kit considering the switching transistor on-resistance. The developed design kit can prove best useful when the used transistor can withstand around 4 times the nominal voltage. In this scenario, no optimization may be required if the methodology of adjusting the on-resistance and the shunt capacitor is used. If the transistor used does not present such characteristics, the optimizer might be almost certain. In this case, using the simplest design kit has the same effect as the developed design kit for relatively high frequencies. Nonetheless, the development of the design kit allowed us to better understand the class E functioning and also helped to understand the effect of the supply voltage. In a nutshell, the class E circuit can be divided into two parts: The output tank and the non-linear part composed of the switching transistor, shunt capacitor, and choke inductor. The developed design

kit gives the designer the optimum non-linear behaviour and the consequential optimum tank impedance. With the addition of real components, the great concern is the inductor. Relative to the non-linear part of the circuit, no optimization was done. The desired output power would simply increase to cover the losses in the choke inductor. With regard to the output tank, a careful analysis was done and it was proven based on the characteristic of the used inductor the maximum tank efficiency was achievable.

The design of 4 power amplifiers had also the purpose to see if there was any convergence between the two design kits. In fact, the output resistance converged and so did the additional tank reactance. This makes sense because of the decrease of the transistor on-resistance. Nevertheless, the shunt capacitor and the choke inductor showed no signs of convergence. This may happen because in the definition of both design kits the variable q was defined and replaced this component values in the equations. The reader may ask if the convergence can be achieved if higher output powers PAs are used (smaller on-resistance). In that sense, simulations using higher output powers were done and the conclusion was the same. The fact that the output resistance converges as the output power increases come in handy to explain where the developed design kit is most useful. In the optimization comparison between both design kits, it was shown that the choice of the output resistance interval is important because it saves iteration time. The developed design kits showed gains in that sense because the output resistance from the initial design was closer to the optimum resistance. This gain fades as both output resistances converge meaning that the developed design kit has only an advantage towards the other design kit when the output power is relatively low. The use of the Rayleigh distribution was useful to bridge the PA design and the type of signal that precedes the amplifying stage block. It can be concluded that the most important branches to define the average PAE were the first two. This is advantageous because as the output power increases, the output resistance is such that the tank efficiency decreases. Besides the higher output power branches not being as relevant, to achieve the same PAE as the first and the second a higher V_{DD} would need to be applied.

A future idea is to use the developed design kit and develop the QDA branches in Gallium Nitride (GaN) technology. This technology compared with Complementary metal–oxide–semiconductor (CMOS) has a much lower on-resistance for the same transistor size. Besides, the breakdown voltage is higher which allows for a higher drain-source voltage maximum [35].

Bibliography

[1] J. M. Lourenço. *The NOVAthesis LaTeX Template User's Manual*. NOVA University Lisbon. 2021. URL: https://github.com/joaomlourenco/novathesis/raw/master/template.pdf (cit. on p. ii).

[2] *Energy efficiency: An overview*. 2020. URL: https://www.gsma.com/futurenetworks/wiki/energy-efficiency-2/ (cit. on p. 1).

[3] *5G technology and networks (speed, use cases, rollout)*. URL: https://www.thalesgroup.com/en/markets/digital-identity-and-security/mobile/inspired/5G (cit. on p. 1).

[4] URL: https://carrier.huawei.com/~/media/CNBG/Downloads/Spotlight/5g/5G-Power-White-Paper-en.pdf (cit. on p. 2).

[5] *5G network energy efficiency - nokia white paper*. URL: https://gsacom.com/paper/5g-network-energy-efficiency-nokia-white-paper/ (cit. on p. 2).

[6] L. F.Clari E.Fadil. *5G and Energy Efficiency - Global5g*. URL: https://global5g.5g-ppp.eu/sites/default/files/BookletA4_EnergyEfficiency.pdf (cit. on p. 2).

[7] P. Chang and G. Miao. "Optimal operation of base stations with deep sleep and discontinuous transmission". In: *IEEE Transactions on Vehicular Technology* 67.11 (2018), pp. 11113–11126. DOI: 10.1109/tvt.2018.2869668 (cit. on p. 2).

[8] R. Dinis and T. Araújo. *Analytical evaluation of nonlinear distortion effects on Multicarrier Signals*. CRC Press, 2017 (cit. on pp. 7, 8).

[9] W. Nottingham. "Optimum conditions for maximum power in class A amplifiers". In: *Proceedings of the IRE* 29.12 (1941), pp. 620–623. DOI: 10.1109/jrproc.1941.233635 (cit. on p. 11).

[10] M. K. Kazimierczuk. *RF Power Amplifiers*. John Wiley and Sons, Ltd., 2015 (cit. on p. 11).

[11] N. Sokal and A. Sokal. "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers". In: *IEEE Journal of Solid-State Circuits* 10.3 (1975), pp. 168–176. DOI: 10.1109/jssc.1975.1050582 (cit. on p. 17).

[12] W.-J. Kim et al. "Digital Predistortion linearizes wireless power amplifiers". In: *IEEE Microwave Magazine* 6.3 (2005), pp. 54–61. DOI: 10.1109/mmw.2005.1511914 (cit. on p. 21).

[13] B. Kim et al. "Push the envelope: Design concepts for envelope-tracking power amplifiers". In: *IEEE Microwave Magazine* 14.3 (2013), pp. 68–81. DOI: 10.1109/mmm.2013.2240851 (cit. on p. 23).

[14] H. Chireix. "High power outphasing modulation". In: *Proceedings of the IRE* 23.11 (1935), pp. 1370–1392. DOI: 10.1109/jrproc.1935.227299 (cit. on p. 25).

[15] P. Viegas et al. "A novel highly-efficient amplification scheme for wireless communications in a CathLab environment". In: *IEEE Access* 9 (2021), pp. 87520–87530. DOI: 10.1109/access.2021.3087966 (cit. on pp. 29, 30).

[16] F. Wang et al. "An improved power-added efficiency 19-dbm hybrid envelope elimination and restoration power amplifier for 802.11g WLAN applications". In: *IEEE Transactions on Microwave Theory and Techniques* 54.12 (2006), pp. 4086–4099. DOI: 10.1109/tmtt.2006.885575 (cit. on p. 30).

[17] R. Ishioka, T. Kimura, and M. Muraguchi. "High-efficiency OFDM power amplifier system using a new polar modulation technique". In: *2016 IEEE Region 10 Conference (TENCON)* (2016). DOI: 10.1109/tencon.2016.7848488 (cit. on p. 30).

[18] M. P. van der Heijden et al. "A 19W high-efficiency wide-band CMOS-gan class-E Chireix RF outphasing power amplifier". In: *2011 IEEE MTT-S International Microwave Symposium* (2011). DOI: 10.1109/mwsym.2011.5972564 (cit. on p. 30).

[19] E. Kaymaksut and P. Reynaert. "Dual-mode CMOS doherty LTE power amplifier with symmetric hybrid transformer". In: *IEEE Journal of Solid-State Circuits* 50.9 (2015), pp. 1974–1987. DOI: 10.1109/jssc.2015.2422819 (cit. on p. 30).

[20] V. Qunaj and P. Reynaert. "26.2 a Doherty-like load-modulated balanced power amplifier achieving 15.5DBM average Pout and 20% average PAE at a data rate of 18Gb/s in 28NM CMOS". In: *2021 IEEE International Solid- State Circuits Conference (ISSCC)* (2021). DOI: 10.1109/isscc42613.2021.9365966 (cit. on p. 30).

[21] M. Acar, A. Annema, and B. Nauta. "Generalized design equations for class-E power amplifiers with finite DC feed inductance". In: *2006 European Microwave Conference* (2006). DOI: 10.1109/eumc.2006.281237 (cit. on p. 31).

[22] I. Casallas et al. "Design methodology of the class-E power amplifier with finite feed inductance—a tutorial approach". In: *Applied Sciences* 10.24 (2020), p. 8765. DOI: 10.3390/app10248765 (cit. on p. 31).

[23] M. Acar, A. J. Annema, and B. Nauta. "Analytical design equations for class-E power amplifiers with finite DC-feed inductance and switch on-resistance". In: *2007 IEEE International Symposium on Circuits and Systems* (2007). DOI: 10.1109/iscas.2007.378758 (cit. on p. 31).

[24] Z. Hua et al. "Class DE power amplifiers". In: *2019 IEEE 9th International Conference on Electronics Information and Emergency Communication (ICEIEC)* (2019). DOI: 10.1109/iceiec.2019.8784492 (cit. on p. 39).

[25] B. Razavi. *RF Microelectronics*. Dorling Kindersley (India), 2014 (cit. on p. 45).

[26] *Mobile Handset Maximum Power*. URL: http://www.silverwing.com.hk/men/news_view_1982_153.html (cit. on p. 59).

[27] A. Mazzanti et al. "Analysis of reliability and power efficiency in Cascode Class-E Pas". In: *IEEE Journal of Solid-State Circuits* 41.5 (2006), pp. 1222–1229. DOI: 10.1109/jssc.2006.872734 (cit. on p. 67).

[28] C.-C. Ho et al. "A fully integrated class-E CMOS amplifier with a class-F driver stage". In: *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2003* (). DOI: 10.1109/rfic.2003.1213928 (cit. on pp. 85, 86).

[29] A. Mazzanti et al. "Analysis of reliability and power efficiency in Cascode Class-E Pas". In: *IEEE Journal of Solid-State Circuits* 41.5 (2006), pp. 1222–1229. DOI: 10.1109/jssc.2006.872734 (cit. on pp. 85, 86).

[30] T. Sowlati and D. Leenaerts. "A 2.4 GHz 0.18 m CMOS self-biased cascode power amplifier with 23 DBM output power". In: *2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315)* (). DOI: 10.1109/isscc.2002.993048 (cit. on pp. 85, 86).

[31] L. Wang and T. Mukherjee. "A 3.4 GHz to 4.3 GHz frequency-reconfigurable class E power amplifier with an integrated CMOS-MEMS LC balun". In: *2010 IEEE Radio Frequency Integrated Circuits Symposium* (2010). DOI: 10.1109/rfic.2010.5477276 (cit. on pp. 85, 86).

[32] A. Melo. *Monolithic RF Class-E power amplifier on CMOS technologies*. 2010-10. URL: https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&cad=rja&uact=8&ved=2ahUKEwir_bnE7K_6AhUMBcAKHRQrC38QFnoECA8QAQ&amp (cit. on p. 86).

[33] J.-C. Du et al. "A current-injection class-E power amplifier". In: *IEEE Microwave and Wireless Components Letters* 30.8 (2020), pp. 775–778. DOI: 10.1109/lmwc.2020.3000994 (cit. on p. 86).

[34] V. Chironi et al. "A digitally modulated class-E polar amplifier in 90 nm CMOS". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 60.4 (2013), pp. 918–925. DOI: 10.1109/tcsi.2012.2215398 (cit. on p. 86).

[35] *Gallium Nitride (GaN) Technology Overview*. URL: https://epc-co.com/epc/ (cit. on p. 88).

A

Class A Design Example

In subsection 2.4.1, the theory behind linear power amplifiers was examined. In order to put some of that theory into practice, a class A linear amplifier will be developed. The design consists of obtaining the desired output power for a given frequency, 1 GHz. Having obtained a good design point the load pull-concept will be explored and conclusions will be taken

A.0.1 Design

The goal of the design is to obtain an output power equal to 10 mW with the highest efficiency possible. The output power of the class A can be given by the following expression

$$P_{out} = \frac{1}{2} \cdot i_D \cdot V_D \ . \tag{A.1}$$

To guarantee that the transistor is always operating in saturation, the drain voltage can never go below the maximum gate voltage minus the threshold voltage. This results in a minimum drain voltage of $2 \cdot (V_{GS} - V_{TH})$. As a consequence, the drain efficiency can be given by

$$\eta = \frac{1}{2} \cdot (1 - \frac{2 \cdot (V_{GS} - V_{TH})}{V_{DD}}) \ . \tag{A.2}$$

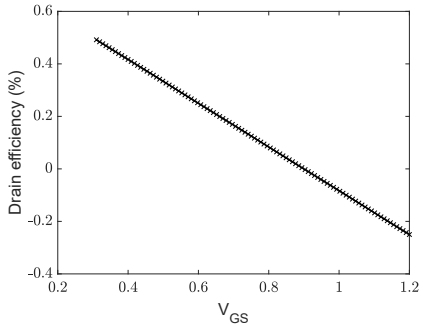
The technology node used will be 130 nm CMOS. The quadratic model will be used as a first approach. The equation (A.1) can then be re-written as

$$P_{out} = \frac{1}{2} \cdot (K_n \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH}) \cdot v_{GS}) \cdot (V_{DD} - 2 \cdot (V_{GS} - V_{TH})) \ . \tag{A.3}$$

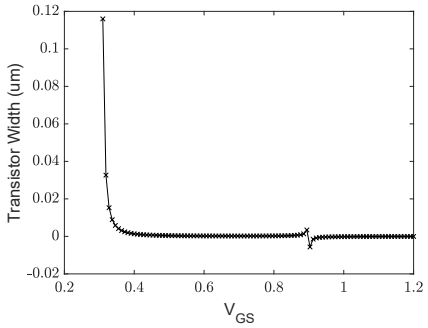
To maximize the efficiency, it was seen that the current must have the maximum excursion possible. This is equivalent to saying that the sinusoid amplitude must have the same amplitude as the DC current. This means that $v_{GS} = V_{GS} - V_{TH}$. Re-writing the output power expression once again

$$P_{out} = \frac{1}{2} \cdot (K_n \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2) \cdot (V_{DD} - 2 \cdot (V_{GS} - V_{TH})) \ . \tag{A.4}$$

The trade-off between efficiency and area is clear. If one wants the best efficiency, the quantity $V_{GS} - V_{TH}$ should be as low as possible. Subsequently, to obtain the same output



(a) Drain Efficiency variation with gate DC voltage.



(b) Transistor width variation with gate DC voltage.

Figure A.1: Class A design strategy.

power, the transistor width has to increase to compensate for that decrease. In Fig. A.1 (a) and Fig. A.1 (b), that trade-off is expressed. The design decision was more on obtaining a good efficiency value. So, the chosen gate DC voltage is 0.4. The transistor channel length was chosen to be three times the minimum length to avoid channel modulation. Relative to the channel width, to obtain the desired output power, this quantity should be 1175 um. The ac output current is around 17.17 mW. Using this value and the output power quantity, the optimal output resistance is around 68 Ω. Relative to the tank, the quality factor is not relevant because there are no concerns regarding a specific bandwidth value. The tank capacitor was assumed to be 1 pF and the working frequency is 1 GHz.

A.0.2 Simulation

The simulation results can be observed in Table A.2. There is a difference in the output power because the ac current is below the expected. To improve these results and obtain the desired output power the transistor width was increased to 1652 um and the output resistance was dropped to 60 Ω. Are these the best results possible in terms of PAE and output power? Is there any advantage in changing the output impedance? These two questions will be analyzed in the next subsection, load-pull simulations.

Table A.1: Class A results.

Parameters	*Theory*	*Simulation*	*Simulation (Optimized)*
Output power (mW)	10	7.25	10.14
AC current (mA)	17.17	15.43	19.15
Minimum drain voltage (V)	0.2	0.2	0.140
Drain Efficiency (%)	41	39.08	40.6

A.0.3 Load-Pull Simulations

This technique, in short, consists in varying the output impedance in order to improve or obtain the desired output power / PAE. The load-pull simulations are quite useful when the transistor model available is not accurate or just complicated to use. Only the output impedance will be swept meaning that the voltage at the gate of the transistor is the same. The design point obtained in the simulation will be used as a reference. It corresponds to a reflection coefficient of $0.0909 + 0 \cdot j$. In Fig. A.2 the PAE smith chart contours can be observed. The marked point corresponds to an output impedance of $65.08 + 47.30 \cdot j$, where the maximum PAE has a value of 45.21 %. This set of contours is not enough because the output power information is not apparent. The output contours can be observed in Fig. A.3. The first interesting observation is that the best PAE point does not correspond to the best output power point. This might be because the PAE design point creates a better ratio between the DC power and the first harmonic by putting the transistor, part of the time, in the triode region. The maximum output power has a value of 10.65 mW and occurs for an output impedance of $48.62 + 30.96 \cdot j$. At this point, the PAE has a value of around 42%. To better see the trade-off between these two quantities, let's overlap the two contours, like in Fig. A.4, and decide the best design point. The selected design point has an impedance equal to $72.53 + 12.10 \cdot j$. What there is left to do is to compare this design point with the original design point whose impedance is equal to 60. This comparison can be consulted in Table A.2. The load-pull point has a better drain efficiency value that the initial point. This justifies the load-pull method and its inherent advantage in accounting for the transistor parasite capacitances. However, note that the minimum drain voltage in the load-pull point is lower which indicates a degradation in the output current and voltage waveforms.

Table A.2: Comparison between load-pull point and design point.

Parameters	*Simulation (Initial Point)*	*Simulation (Load Pull)*
Output power (mW)	10.14	10.13
AC current (mA)	19.15	16.71
Minimum drain voltage (V)	0.140	0.106
Drain Efficiency (%)	40.6	43.18

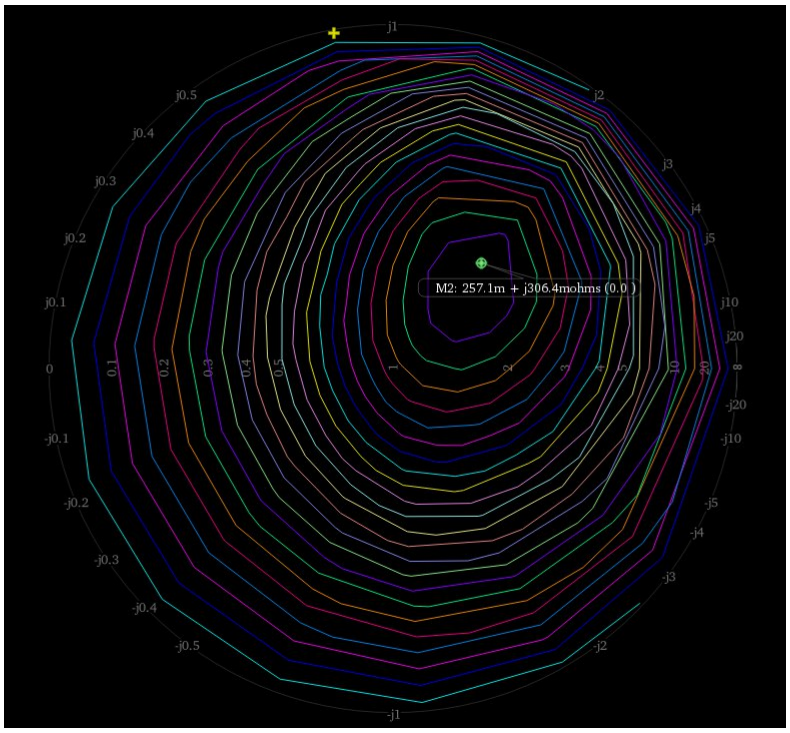


Figure A.2: Load-Pull contours of PAE.

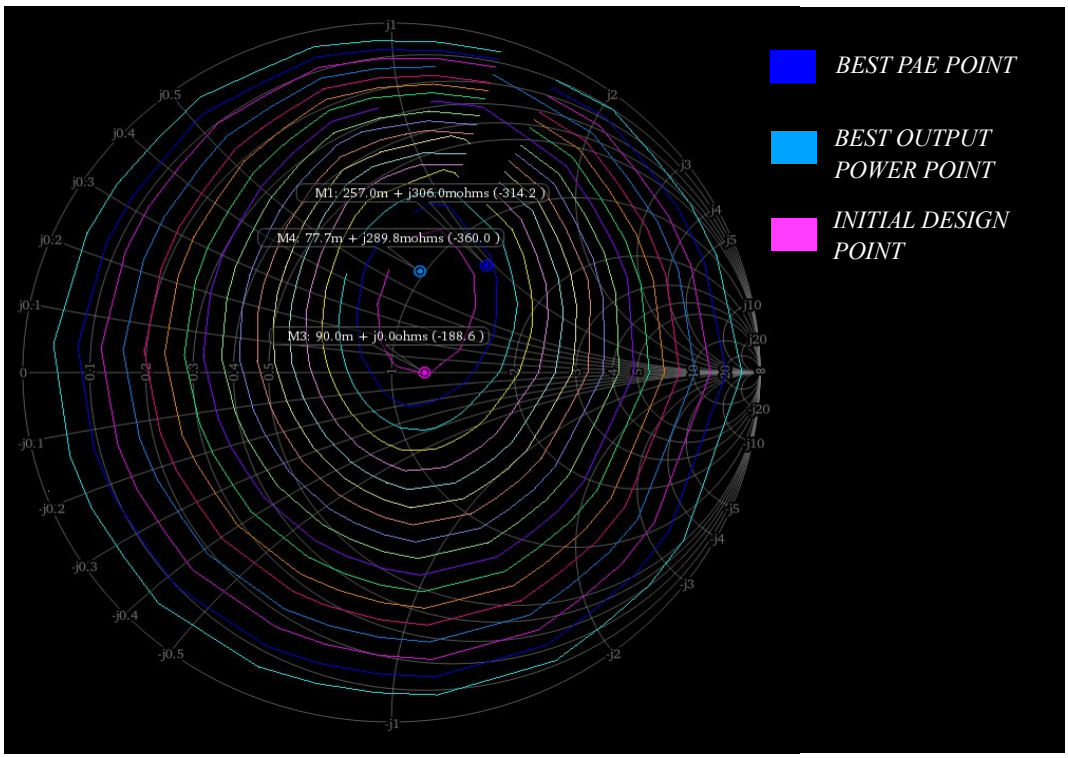


Figure A.3: Load-Pull contours of output power.

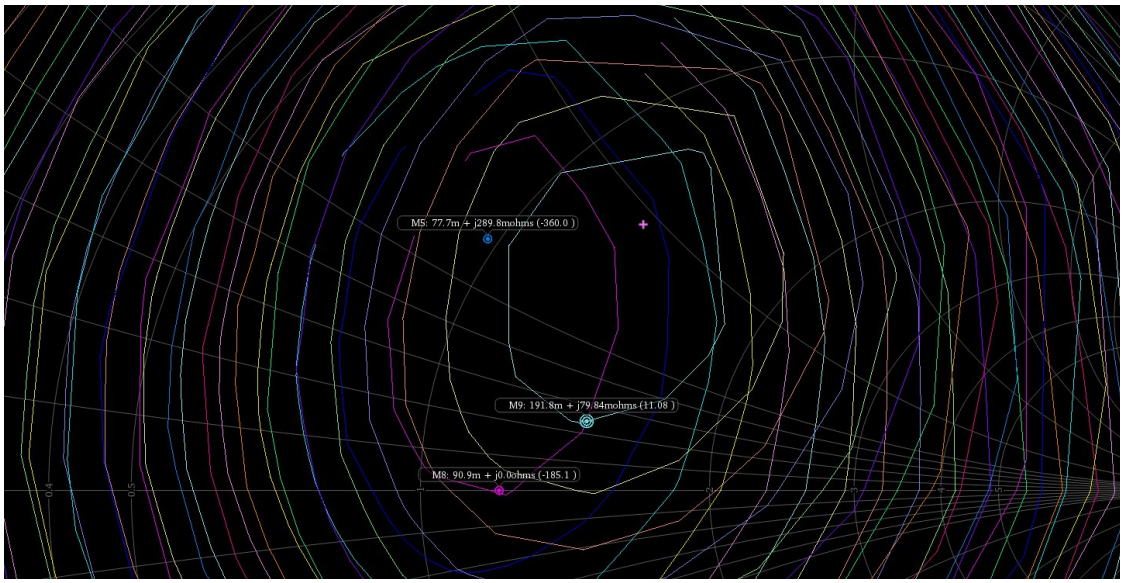


Figure A.4: Tradeoff between the PAE and the Output power.

B

Tutorial on how to corroborate transistor on-resistance

This tutorial has the main goal of guiding the reader on how to obtain the graphics of the transistor on-resistance. The used technology parameters are known, namely, the oxide capacitance per unit area and the mobility constant of the holes and electrons is known. However, it is a good practice to corroborate the parameters. In a nutshell, for each frequency, there will be a design point which contains the value of each component present in the schematic. For every design, the transistor width will be swept. That allows seeing the variation of the transistor on-resistance. The software used are Matlab (Python works as well) and Cadence Virtuoso

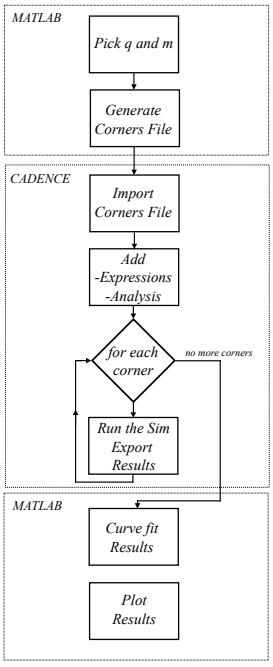


Figure B.1: Flowchart of the tutorial.

B.1 First Step

The first step is for each frequency to choose a design point. This makes sure that for each frequency, despite sweeping the transistor width, we have a condition close to the ideal. The criteria for choosing the design points are totally arbitrary. For each frequency, pick a q and m. For sake of simplicity, the q and m are the same independently of the frequency. With this said the value of q and m are **1.7** and **0.02**, respectively. Also, the output resistance was always set to 50 Ω. In Fig. B.2, the schematic of the class E used, with the respective component values for each frequency, can be observed

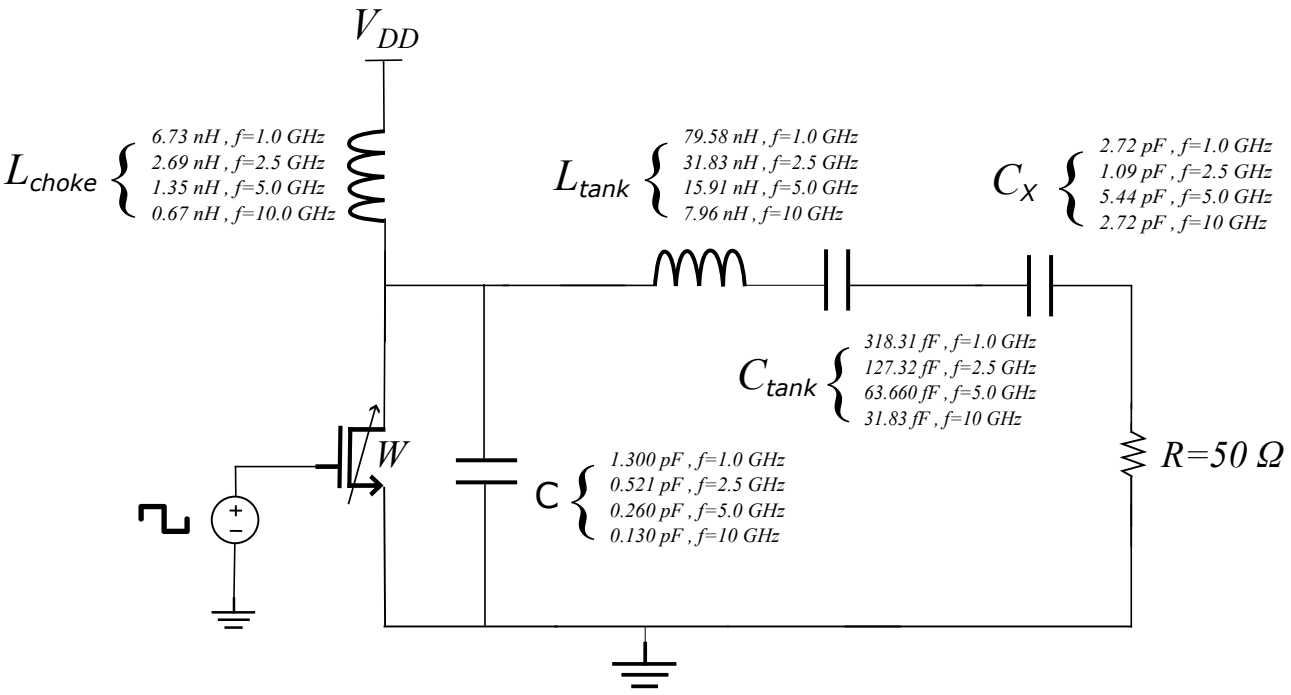


Figure B.2: Class E schematic used in the tutorial.

B.2 Second Step

With the design values, we can move on to the simulator. The simulator used is called Cadence Virtuoso. Inside Virtuoso, the tool used was ADE Explorer. To test the different design points, the functionality corners were used. This is usually used when one wants to change the default fabric transistor parameters such as temperature, and threshold voltage. We can import the design points as corners as long as we put them in the correct format such as a matrix. An example of a valid matrix can be observed in Fig. B.3.

	1	2	3	4	5
1	Corner	C0	C1	C2	C3
2	Enable	t	t	t	t
3	Temperature	27	27	27	27
4	numb	1	1	1	1
5	t_tran	5e-08	5e-08	5e-08	5e-08
6	frequ	1000000000	2500000000	5000000000	10000000000
7	period	1e-09	4e-10	2e-10	1e-10
8	c_shunt	1.3014e-12	5.2055e-13	2.6028e-13	1.3014e-13
9	l_choke	6.735e-09	2.694e-09	1.347e-09	6.735e-10
10	l_tank	7.9577e-08	3.1831e-08	1.5915e-08	7.9577e-09
11	c_tank	3.1831e-13	1.2732e-13	6.3662e-14	3.1831e-14
12	x_tank	2.7196e-12	1.0879e-12	5.4393e-13	2.7196e-13
13	Rout	50	50	50	50
14	t Test::Power_Amplifi...	t	t	t	t

Figure B.3: Corners Matrix Format.

B.3 Third Step

To add the matrix, go to the ADE Explorer main panel and right-click on the corners tab. Then left-click on the Open Corners Setup. This step can be observed in Fig. B.4.

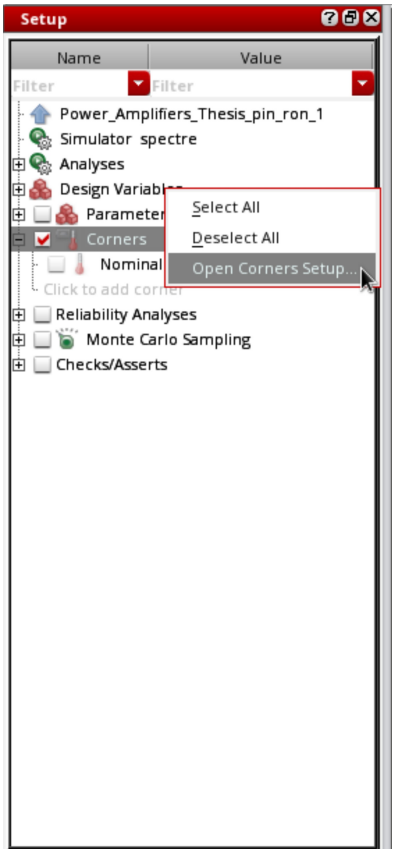


Figure B.4: Third Step - First window.

The previous step will open a new window just like in Fig. B.5. From there, click on the first down arrow counting from the left and click-right on import corners from Comma Separated Values (CSV) file. That will open a window where the reader will choose the CSV file containing the different design points. After the matrix import, the corners setup

should look something like in Fig. B.6.

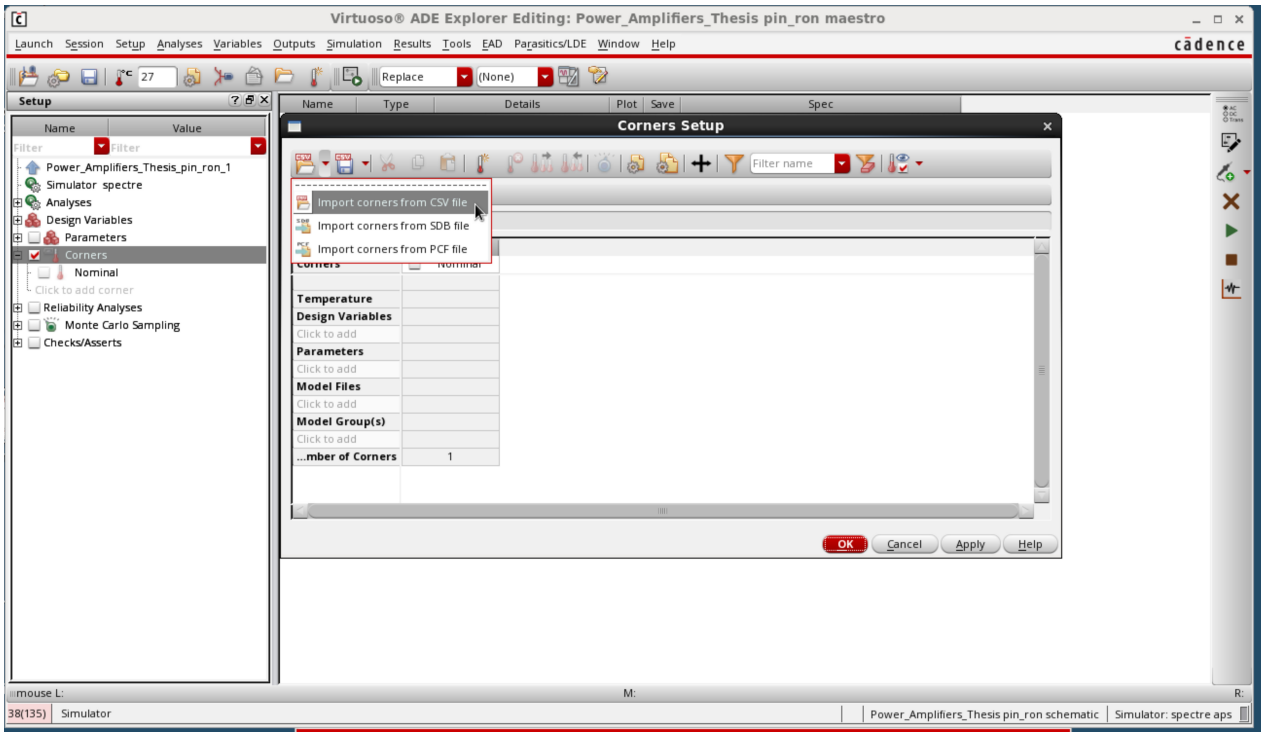


Figure B.5: Third Step - Second window.

B.4 Fourth Step

Once the corners are imported, the definition of the transistor on-resistance must be defined. For that, click on the pen, with the green sum icon which will create a blank expression. This step is illustrated in Fig. B.7. The transistor on-resistance definition might seem complicated but essentially, we are averaging the ratio between the drain voltage and drain current during half of the period when the transistor is ON.

$$r_{on} = average[\ clipX((vtime('tran\ ''/vd1'') \ /\ itime('tran\ ''/M1/D''))$$
$$(5e-08\ -\ (0.75\ \cdot\ VAR(''period''))),\ (5e-08\ -\ (0.5\ \cdot\ VAR(''period'')))\ ] \tag{B.1}$$

B.5 Fifth Step

Once the expressions are good to go, what there is left to do is to define the simulation. All that is necessary is a transient analysis. To define such analysis, double-click on the analysis tab that is located on the left. A new window will pop up. Define the transient analysis like in Fig. B.8.

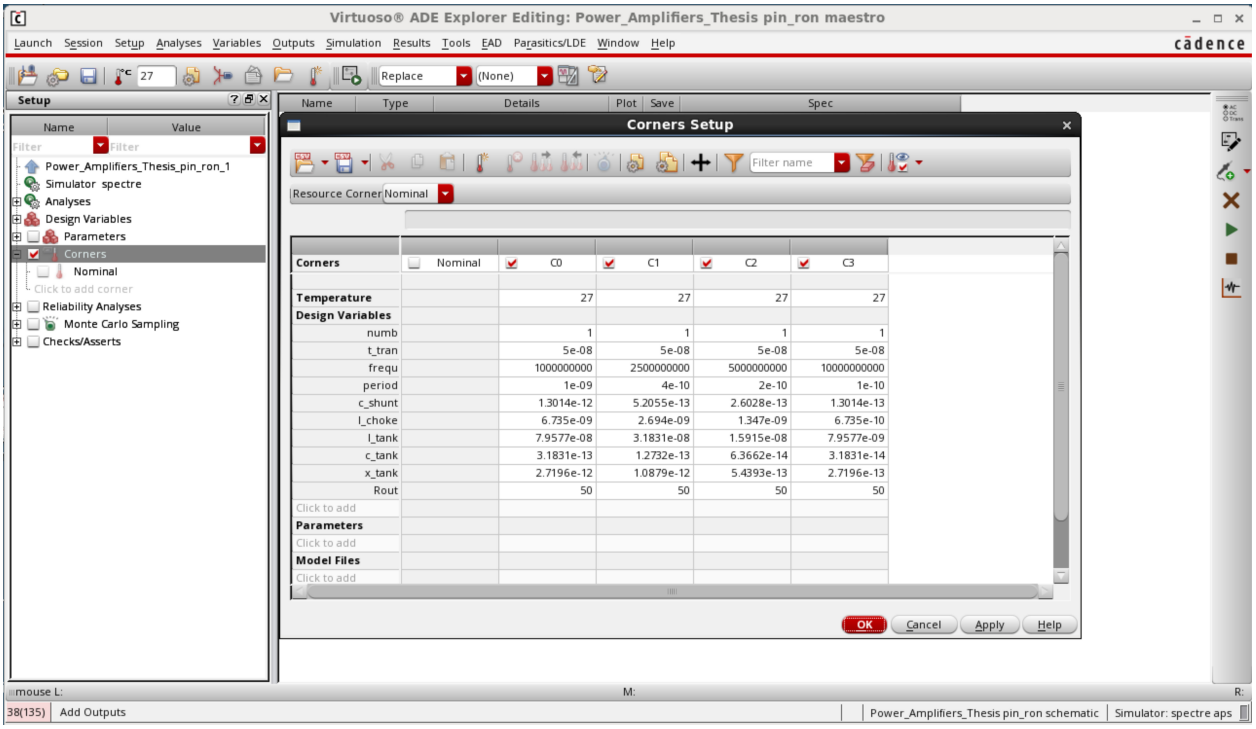


Figure B.6: Third Step - Third window.

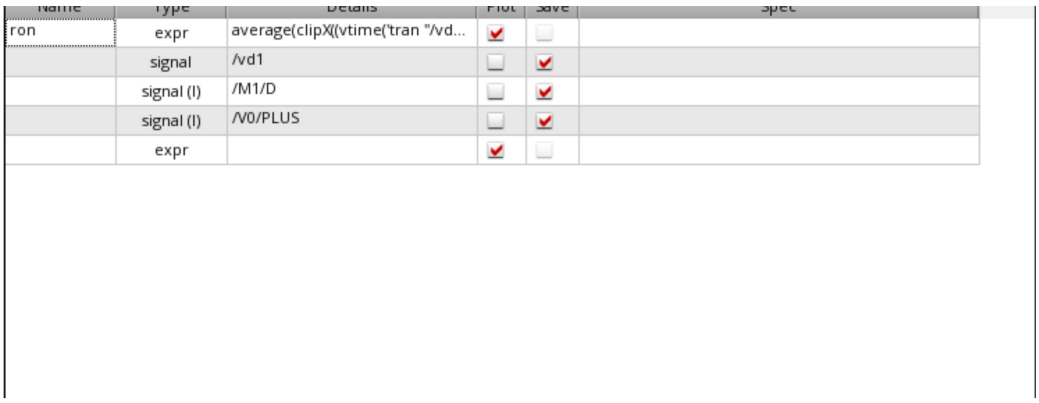


Figure B.7: Fourth Step.

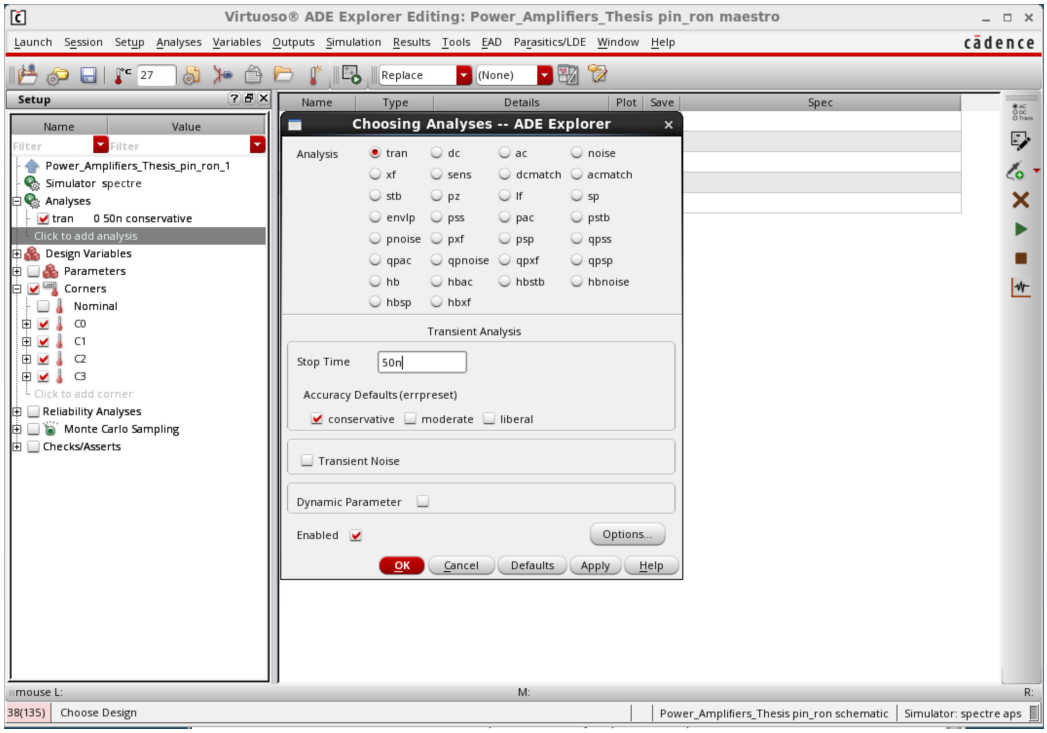


Figure B.8: Fifth Step.

B.6 Sixth Step

Everything is set! Now for each corner (C0, C1, C2, C3) vary the transistor width. Then run the simulation and extract the defined expression.

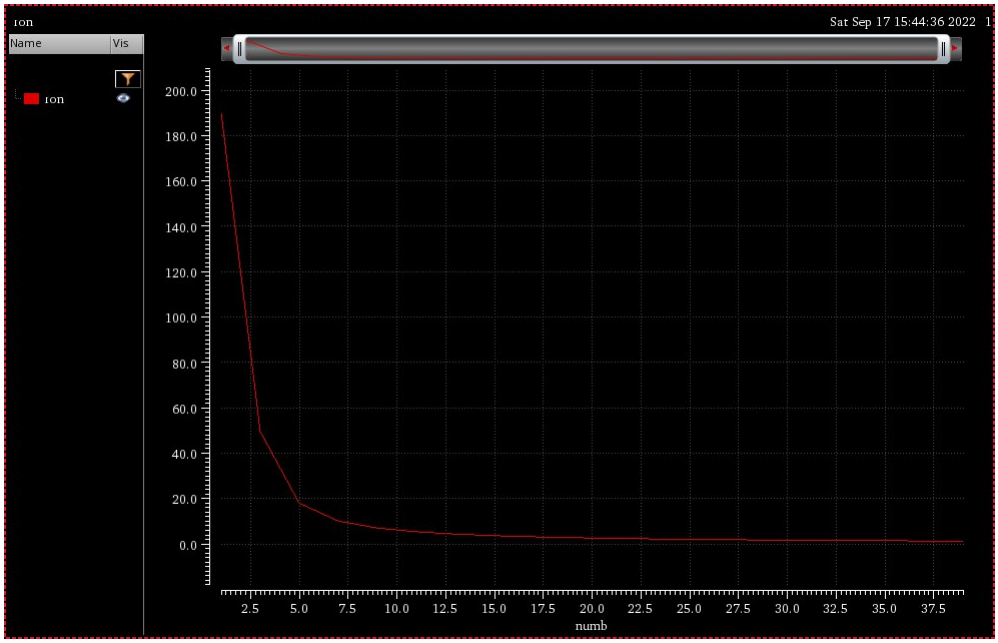


Figure B.9: Sixth Step.

C

Second and Third Branch Design

C.0.1 Second Branch

C.0.1.1 Design

For the second branch, we need 24 mW so the designed output power must be around 46 mW. The design workflow follows the same guidelines as the first branch including the desired total resistance. The design space can be observed in Fig. C.1. The coordinates of (q,m) chosen can be seen in Table C.1

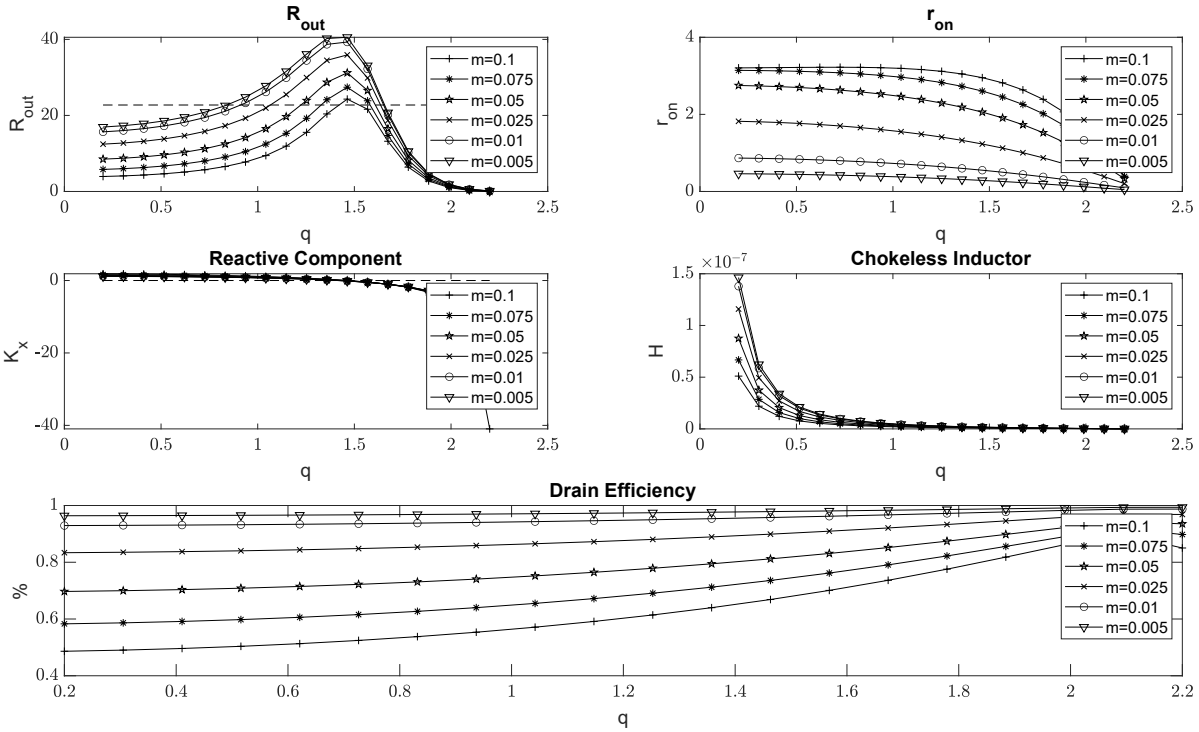
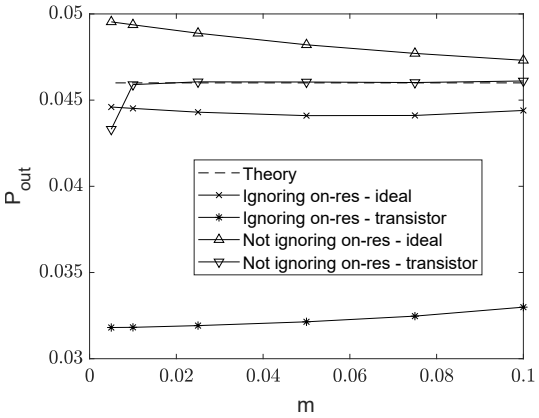


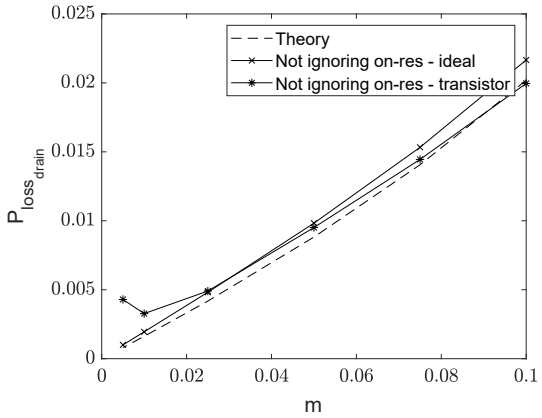
Figure C.1: Second Branch Design Space

Table C.1: Design variables coordinates (q,m) for the second branch.

q	1.5493	1.5831	1.6106	1.6362	1.6514	1.6565
m	0.1	0.075	0.05	0.025	0.01	0.005



(a) P_{out} variation with m design variable



(b) Transistor power loss variation with m design variable

Figure C.2: Output power and power losses in the second branch design.

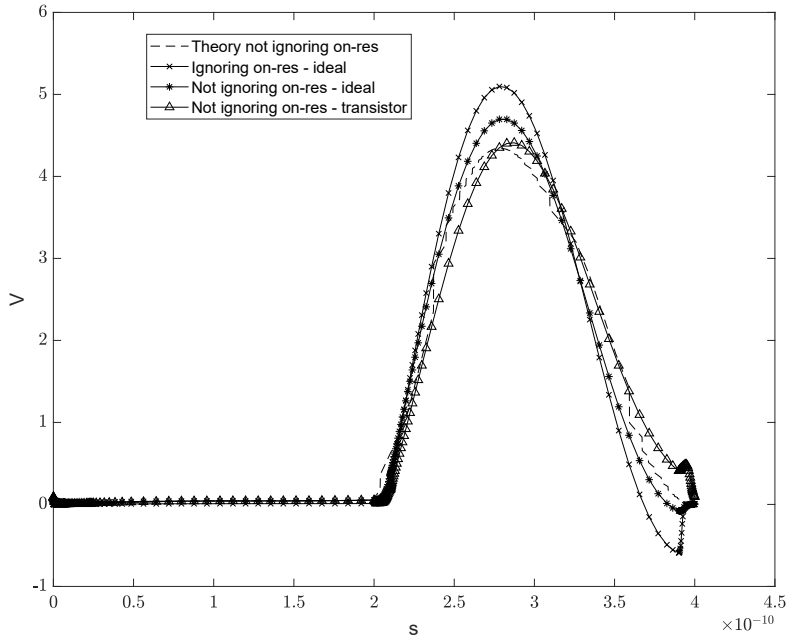
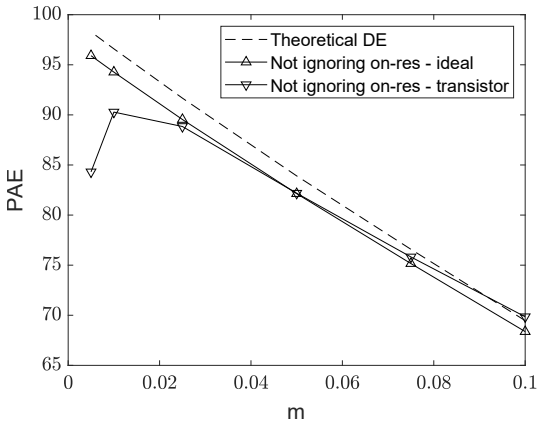
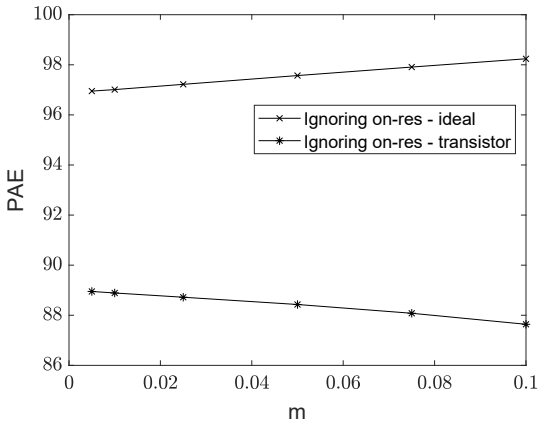


Figure C.3: Time evolution of the drain voltage in the second branch for m=0.01



(a) PAE of the designs accounting the transistor on-resistance.



(b) PAE of the designs considering the transistor on-resistance ideal.

Figure C.4: PAE comparison on the second branch between the two design kits.

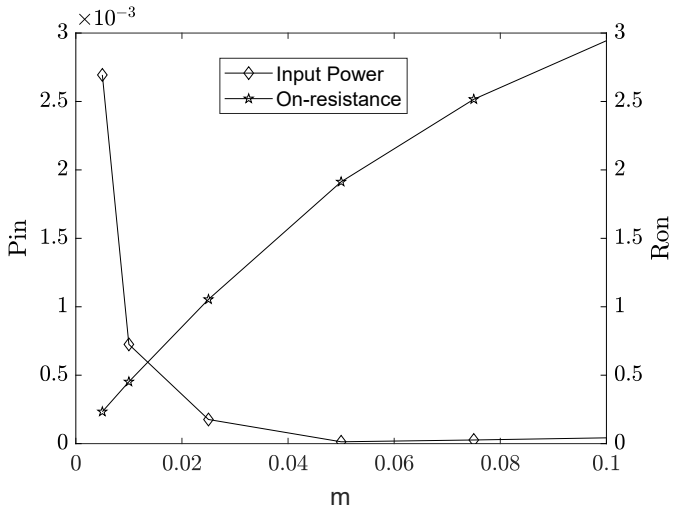


Figure C.5: Input power and on-resistance variation with m design variable in the second branch design.

Table C.2: Components value before and after the first optimization for the second branch.

Parameters	*Before first iteration*	*After first iteration*
Transistor Width	1180 um	1080 um
Shunt Capacitor	1.401 pF	0.600 pF
Choke Inductor	1.061 nH	1.061 nH
Tank Inductor	5.7647 nH	5.7647 nH
Tank Capacitor	0.703 pF	0.703 pF
Tank Additional Reactance	3.154 pF	3.154 pF
Output Resistance	22.76 Ω	22.76 Ω

C.0.1.2 Simulation

C.0.1.3 Optimization

The tank efficiency was omitted because the results are the same as the first branch. Admitting a 60 % tank efficiency, the output power should be higher than 40 mW. The approximated choke inductor power losses are around 12 mW. With this in mind, a range of desired output power was defined. The restrictions regarding the maximum PAE and the maximum drain source voltage of the common gate transistor were kept the same. The optimizer restrictions can be observed in Table C.3

Table C.3: Second branch optimizer Restrictions.

Parameters	*Specification*
Output Power	46 mW < ... > 55 mW
Maximum Voltage	< 2.6
Power Added Efficiency	max 79%

In the second branch, the candidate's selection is a much easier task. The best PAE point is discarded because of the maximum voltage. Relative to the other candidates, both present alluring maximum voltage and total resistance characteristics. The tiebreaker was the output power that it's slightly higher in candidate number 3, despite number 2 having bits more of PAE. The chosen design point has the values of the components described in Table C.5

Table C.4: Optimizer best results for second branch.

Design Points	*PAE(%)*	*Maximum Voltage(V)*	*Output Power(mW)*	*Total Resistance(Ω)*
Best PAE point	78.6	2.702	49.32	23
Candidate Point 2	77.74	2.469	53.19	23
Candidate Point 3	77.7	2.495	53.29	23

After replacing the ideal inductors with real ones, the output power was around 24.37 mW. Replacing the remaining components with real ones, the output power dropped to 22.74 mW. One of the reasons was that the total resistance was higher than necessary. To correct this, the value of the inductor was reduced, reducing its parasite resistance. As a consequence, the quality factor dropped slightly. Then the additional tank reactance was increased to 7.2 pF. The final design parameters are depicted in Table C.6

Table C.5: Second branch chose design point components description.

Component	*Value*
Common Source Transistor Width (um)	810
Common Gate Transistor Width (um)	570
Shunt Capacitor (pF)	1.6
Choke Inductor (nH)	0.8
Tank Capacitor (pF)	0.703
Tank Inductor (nH)	5.765
Additional Tank Reactance (pF)	6
Transformation Inductor (nH)	1.39
Transformation Capacitor (pF)	2.16
Output Resistance (Ω)	50

Table C.6: Second branch final design parameters.

Parameters	*Values*
Output power (mW)	24.03
Supply Power (mW)	77.18
Bandwidth (MHz)	526
Total Tank Efficiency (%)	52.38
PAE (%)	30
Common source input power (uW)	874.7
Common gate input power (uW)	4.134
Total Resistance (Ω)	23.32
Maximum Drain Source voltage of CG	2.09
Maximum Drain Source voltage of CS	1.481

C.0.2 Third Branch

C.0.2.1 Design

For the third branch, the optimum total tank resistance could be the same used in the first and second branch. The reason lies that as the output power increases, to keep the optimum class E conditions, the output resistance has to decrease. This leaves the designer with a new choice to make. The total optimum resistance chosen was around 19 Ω in view of the fact that the tank efficiency does not decrease much from 22.74 Ω to 19 Ω. The designed output power was 92.3 mW. This output resistance decrease can be well observed in Fig C.6. The coordinates of (q,m) chosen can be seen in Table C.7

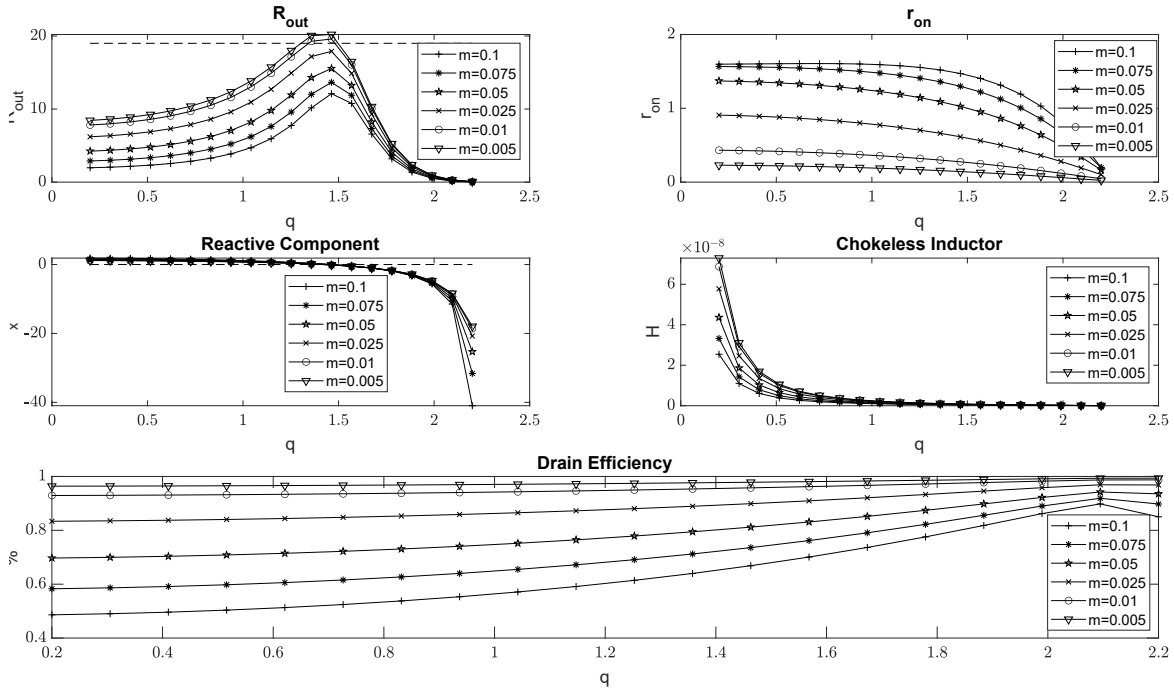
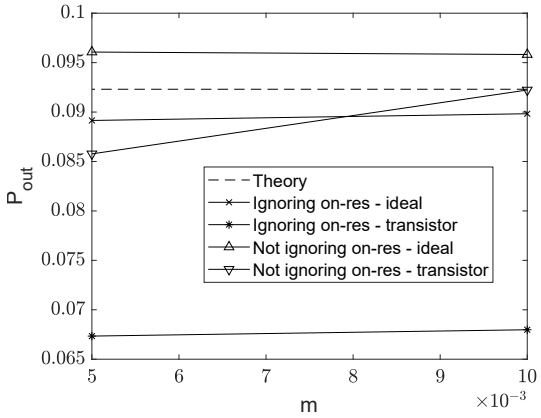


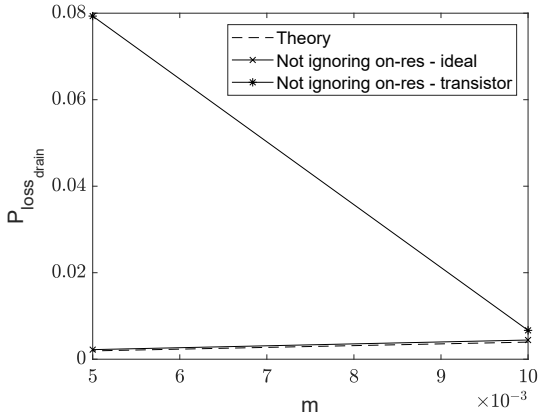
Figure C.6: Third Branch Design Space.

Table C.7: Design variables coordinates (q,m) for the third branch.

q	1.493	1.513
m	0.01	0.005



(a) P_{out} variation with m design variable.



(b) Transistor power loss variation with m design variable.

Figure C.7: Output power and power losses in the third branch design.

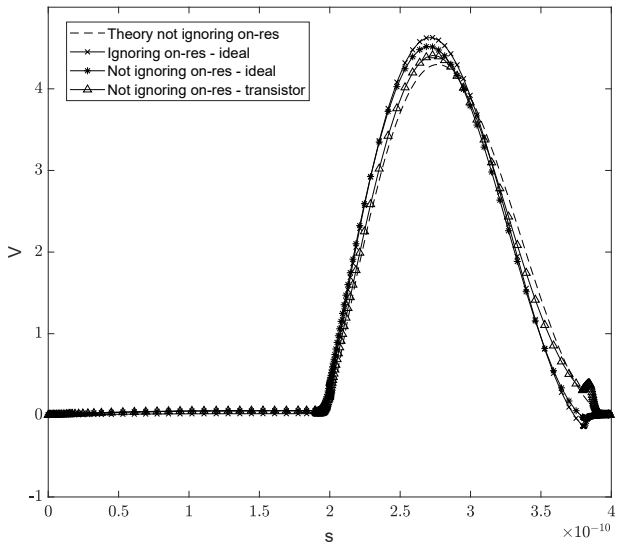
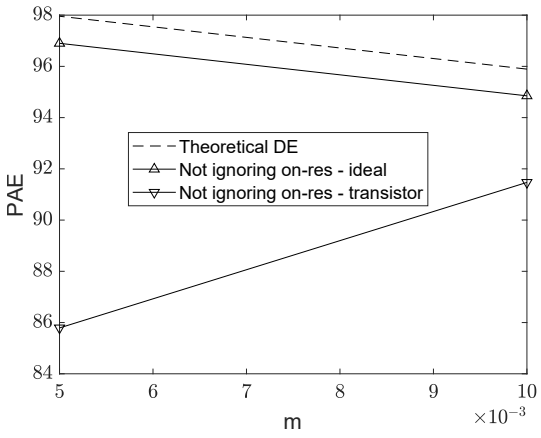
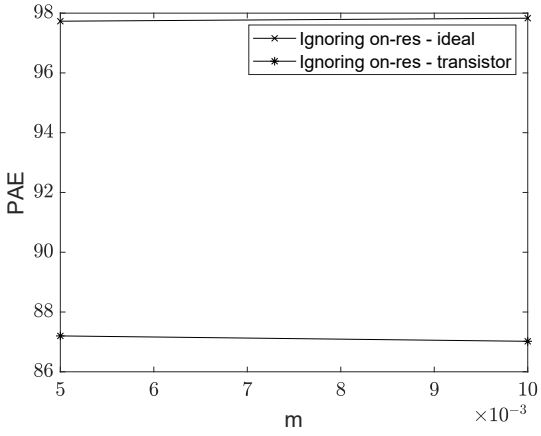


Figure C.8: Time evolution of the drain voltage in the third branch for m=0.01



(a) PAE of the designs accounting the transistor on-resistance.



(b) PAE of the designs considering the transistor on-resistance ideal

Figure C.9: PAE comparison on the third branch between the two design kits.

Table C.8: Third branch components value before and after the first optimization.

Parameters	*Before first iteration*	*After first iteration*
Transistor Width	2010 um	1850 um
Shunt Capacitor	2.38 pF	0.92 pF
Choke Inductor	0.765 nH	0.765 nH
Tank Inductor	4.96 nH	4.96 nH
Tank Capacitor	0.816 pF	0.816 pF
Tank Additional Reactance	14.97 pF	14.97 pF
Output Resistance	19 Ω	19 Ω

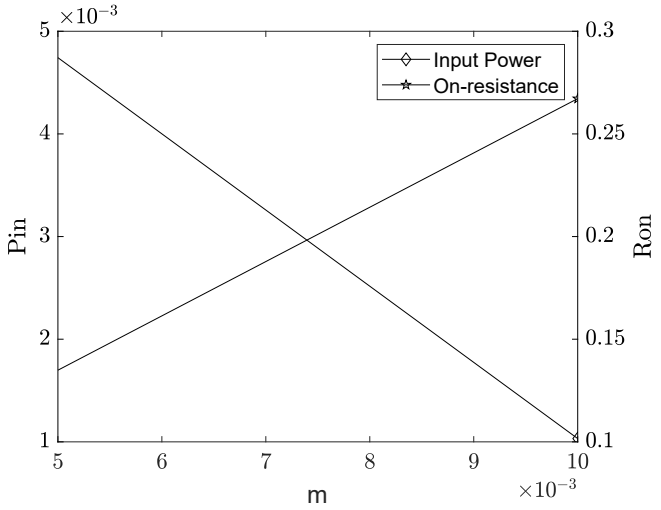


Figure C.10: Input power and on-resistance variation with m design variable in the third branch.

C.0.2.2 Simulation

C.0.2.3 Tank Analysis

Since the optimum tank total resistance changed, it is convenient to study the tank. The methodology used here was the same as the first branch. The results obtained are shown in Table C.9

Table C.9: Comparison between tank performance for different analyses in the third branch.

Parameters	*Theory*	*AC Simulation*	*PSS Simulation*
Inductor Tank $R_{parasite}$	6.823	7.584	7.47
Transformation Tank $R_{parasite}$	1.649	1.796	1.796
Transformation Resistance	12.669	12.37	12.36
Total Resistance	19.49	19.95	20.18
Tank Efficiency	65.01	61.99	66.6
Transformation Efficiency	86.97	85.48	85.67
Total Efficiency	56.55	52.98	57.06

C.0.2.4 Optimization

With the total efficiency value obtained in the PSS analysis, the desired output power should be higher than 84 mW. Adding up the approximated losses in the choke inductor, the total output power rises to 104 mW. In the first optimization iteration, the maximum output power was set to 110 mW. This proved to be not enough because the power losses were in the choke inductor were higher than the approximation. The maximum output

power in the second iteration was set to 125 mW. The rest of the optimization restrictions can be consulted in Table C.10

Table C.10: Optimizer restrictions in the third branch.

Parameters	*Specification*
Output Power	98 mW < ... > 125 mW
Maximum Voltage	< 2.6 V
Power Added Efficiency	max 81%

The three best candidates can be observed in Table C.11. The best PAE point is an appealing choice but the output power is slightly more than necessary. Because of that and the difference between PAE is not that big, the optimization point chosen was candidate point 2. The third candidate point was discarded because of the maximum voltage.

Table C.11: Optimizer Best Results in the third branch.

Design Points	*PAE(%)*	*Maximum Voltage(V)*	*Output Power(mW)*	*Total Resistance(Ω)*
Best PAE point	76.07	2.514	122.7	12
Candidate Point 2	75.82	2.487	120.4	12
Candidate Point 3	75.82	2.764	120.7	13

Table C.12: Third branch chose design point components description.

Component	*Value*
Common Source Transistor Width (um)	1280
Common Gate Transistor Width (um)	2400
Shunt Capacitor (pF)	0.9
Choke Inductor (nH)	0.6
Tank Capacitor (pF)	1.306
Tank Inductor (nH)	3.104
Additional Tank Reactance (pF)	45
Transformation Inductor (nH)	1.09
Transformation Capacitor (pF)	3.23
Output Resistance (Ω)	50

After replacing the ideal components with real ones, the output power was around 45.74 mW. To improve this value, the first step is to replace the tank capacitor and the additional capacitance with its series equivalent. This added about one milliwatt to the output power. The last step to obtain the desired output power was to lower the quality factor by decreasing the tank inductor value. The final design parameters can be observed in Table C.13.

Table C.13: Third Branch final design parameters.

Parameters	*Values*
Output power (mW)	48.09
Supply Power (mW)	150.2
Bandwidth (MHz)	488.5
Total Tank Efficiency (%)	52.74
PAE (%)	30.98
Common source input power (mW)	1.55
Common gate input power (uW)	2.046
Total Resistance (Ω)	13.43
Maximum Drain Source voltage of CG	2.132
Maximum Drain Source voltage of CS	1.505

D

Design kit auxiliary variables and constants

$$c_1 = \frac{V_{DD}\left(-\frac{m\cdot p\cdot q^2\left[\sin(\theta)\cdot\left(a+m\cdot\left(q^2-1\right)\right)+\cos(\theta)\cdot\left(a\cdot m\cdot\left(q^2-1\right)-1\right)\right]}{m^2\cdot\left(q^2-1\right)^2+1}-a\right)}{a-b}\,, \tag{D.1}$$

$$c_2 = \frac{V_{DD}\left(\frac{m\cdot p\cdot q^2\left[\sin(\theta)\cdot\left(b+m\cdot\left(q^2-1\right)\right)+\cos(\theta)\cdot\left(b\cdot m\cdot\left(q^2-1\right)-1\right)\right]}{m^2\cdot\left(q^2-1\right)^2+1}+b\right)}{a-b}\,. \tag{D.2}$$

$$c_3 = -\frac{V_{DD}\left(\cos(2\cdot\pi\cdot q)\left(p\cdot q^2\cdot\cos(\theta)+q^2-1\right)+p\cdot q\cdot\sin(\theta)\cdot\sin(2\cdot\pi\cdot q)\right)}{q^2-1}\,. \tag{D.3}$$

$$c_4 = \frac{V_{DD}\left(p\cdot q\cdot\sin(\theta)\cdot\cos(2\cdot\pi\cdot q)-\sin(2\cdot\pi\cdot q)\left(p\cdot q^2\cdot\cos(\theta)+q^2-1\right)\right)}{q^2-1}\,. \tag{D.4}$$

$$\begin{aligned} a_1 = q^2\cdot V_{DD}\Big(&-ae^{\pi b}m^2\left(q^2-1\right)^2+b\left(e^{\pi a}m^2\left(q^2-1\right)^2-1\right)+\\ &+(a-b)\left(m^2\left(q^2-1\right)^2+1\right)\cos(\pi q)-m\left(q^2-1\right)\left(e^{\pi a}-e^{\pi b}\right)+a\,, \end{aligned} \tag{D.5}$$

$$\begin{aligned} b_1 = q\cdot V_{DD}\Big((a-b)\left(m^2\left(q^2-1\right)^2+1\right)\sin(\pi q)+mq\left(q^2-1\right)\Big(m\left(q^2-1\right)\left(e^{\pi a}-e^{\pi b}\right)+\\ \left(e^{\pi a}+1\right)b-a\left(e^{\pi b}+1\right)\,, \end{aligned} \tag{D.6}$$

$$d_1 = V_{DD}\cdot\left(\left(q^2-1\right)\left(m^2\left(q^2-1\right)^2+1\right)\left((a-b)\cos(\pi q)+a\left(-e^{\pi b}\right)+e^{\pi a}b\right)\right)\,, \tag{D.7}$$

$$\begin{aligned} a_2 = q^2\cdot V_{DD}\Big(&mq\left(q^2-1\right)\Big(a^2\left(\left(e^{\pi b}-1\right)m\left(q^2-1\right)-2b\right)+a\left(2b^2-e^{\pi b}+1\right)-\\ &-\left(e^{\pi a}-1\right)b\left(bm\left(q^2-1\right)-1\right)+ab(a-b)\left(m^2\left(q^2-1\right)^2+1\right)\sin(\pi q)\,, \end{aligned} \tag{D.8}$$

$$b_2 = V_{DD} \cdot \left(q \left(a^2 \left(b \left(m^2 \left(q^2 - 1 \right)^2 - 2q^2 + 1 \right) + \left(e^{\pi b} - 1 \right) m \left(q^2 - 1 \right) q^2 \right) - ab^2 \left(m^2 \left(q^2 - 1 \right)^2 - 2q^2 + 1 \right) + \right. \right.$$
$$+ a \left(e^{\pi b} - 1 \right) m^2 \left(q^3 - q \right)^2 - ab(a-b) \left(m^2 \left(q^2 - 1 \right)^2 + 1 \right) \cos(\pi q) -$$
$$\left. - (e^{\pi a} - 1)\, bmq^2 \left(q^2 - 1 \right) \left(b + m \left(q^2 - 1 \right) \right) \right) , \tag{D.9}$$

$$d_2 = V_{DD} \cdot \left(\left(q^2 - 1 \right) \left(m^2 \left(q^2 - 1 \right)^2 + 1 \right) \left(a^2 \left(e^{\pi b} - 1 \right) q - (e^{\pi a} - 1)\, b^2 q + ab(a-b) \sin(\pi q) \right) \right) . \tag{D.10}$$