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Mestre

CMOS indoor light energy harvesting system for wireless sensing applications

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To Rute and Gonçalo

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Abstract

This research thesis presents a micro-power light energy harvesting system for indoor environments. Light energy is collected by amorphous silicon photovoltaic (a-Si:H PV) cells, processed by a switched-capacitor (SC) voltage doubler circuit with maximum power point tracking (MPPT), and finally stored in a large capacitor. The MPPT Fractional Open Circuit Voltage (V_{OC}) technique is implemented by an asynchronous state machine (ASM) that creates and, dynamically, adjusts the clock frequency of the step-up SC circuit, matching the input impedance of the SC circuit to the maximum power point (MPP) condition of the PV cells. The ASM has a separate local power supply to make it robust against load variations. In order to reduce the area occupied by the SC circuit, while maintaining an acceptable efficiency value, the SC circuit uses MOSFET capacitors with a charge reusing scheme for the bottom plate parasitic capacitors. The circuit occupies an area of 0.31 mm^2 in a 130 nm CMOS technology. The system was designed in order to work under realistic indoor light intensities. Experimental results show that the proposed system, using PV cells with an area of 14 cm^2, is capable of starting-up from a 0 V condition, with an irradiance of only 0.32 W/m^2. After starting-up, the system requires an irradiance of only 0.18 W/m^2 (18 $\mu W/cm^2$) to remain in operation. The ASM circuit can operate correctly using a local power supply voltage of 453 mV, dissipating only 0.085 μW. These values are, to the best of the authors' knowledge, the lowest reported in the literature. The maximum efficiency of the SC converter is 70.3% for an input power of 48 μW, which is comparable with reported values from circuits operating at similar power levels.

Keywords — CMOS integrated circuits, Energy harvesting, Maximum Power Point Tracking (MPPT), Power conditioning, Photovoltaic cells, Wireless sensor networks.

Resumo

Esta tese de investigação apresenta um sistema de colheita de energia luminosa, de micro potência, para ambientes interiores. A energia luminosa é recolhida por células fotovoltaicas de silício amorfo (a-Si:H PV), processada por um circuito duplicador de tensão com condensadores comutados (SC), com seguimento do ponto de máxima potência (MPPT) e, finalmente, armazenada num condensador com um valor grande. A técnica MPPT da tensão de circuito aberto fracional é implementada através de uma máquina de estados assíncrona (ASM) que gera e, dinamicamente, ajusta a frequência de relógio do circuito SC ampliador, conjugando a impedância de entrada do circuito SC com a condição de ponto de máxima potência (MPP) das células PV. A ASM é alimentada por uma fonte de alimentação local separada, para torná-la robusta a variações da carga. De maneira a reduzir a área ocupada pelo circuito SC, mantendo simultaneamente um valor de eficiência aceitável, o circuito SC usa condensadores MOSFET com um esquema de reutilização de carga dos condensadores parasitas da armadura inferior. O circuito ocupa uma área de 0.31 mm^2 numa tecnologia CMOS de 130 nm. O sistema foi projetado de maneira a operar sob intensidades luminosas realistas em interiores. Resultados experimentais mostram que o sistema proposto, usando células PV com uma área de 14 cm^2, é capaz de arrancar, a partir de uma condição de 0 V na saída, com uma irradiância de apenas 0.32 W/m^2. Após o arranque, o sistema precisa de uma irradiância de apenas 0.18 W/m^2 (18 $\mu W/cm^2$) para se manter a funcionar. O circuito da ASM consegue operar corretamente, usando uma tensão de alimentação local de 453 mV, dissipando apenas 0.085 μW. Estes valores são, tanto quanto os autores têm conhecimento, os mais baixos reportados na literatura. A eficiência máxima do conversor SC é de 70.3%, para uma potência de entrada de 48 μW, a qual é comparável com valores reportados de circuitos a operar com níveis de potência semelhantes.

Palavras-chave — Circuitos integrados CMOS, Colheita de energia, Seguimento do ponto de máxima potência (MPPT), Processamento de energia, Células fotovoltaicas, Redes de sensores sem fios.

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ACRONYMS

a-Si:H – Hydrogenated amorphous silicon

AC – Alternating current

ASM – Asynchronous state machine

BEEM – Building Energy and Environment Monitoring

c-Si – Crystalline silicon

CCM – Continuous conduction mode

CMOS – Complementary Metal-Oxide-Semiconductor

CPU – Central processing unit

DC – Direct current

DC-DC – Direct current to direct current

DLC – Double layer capacitor

DUT – Device under test

ESD – Electro static discharge

EWT – Emmiter wrap through

FF – Fill factor

IC – Integrated circuit

I^2C – Inter integrated circuit

IoT – Internet of things

LDO – Low drop out

MEMS – Micro electro mechanical system

MFC – Microbial fuel cell

MOSFET – Metal-Oxide-Semiconductor field effect transistor

MPP – Maximum power point

MPPT – Maximum power point tracking

OTEC – Ocean thermal energy conversion

PCB – Printed circuit board

PEC – Photosynthetic electrochemical cell

PSD – Power spectral density

PV – Photovoltaic

RF – Radio frequency

RFID – Radio frequency identification

SLA – Sealed lead acid

SC – Switched-capacitor

SEPIC – Single-ended primary inductance converter

SOI – Silicon-on-insulator

STC – Standard test conditions

SHM – Structural health monitoring

TEG – Thermoelectric generator

UWB – Ultra wide band

VCR – Voltage conversion ratio

VRC – Voltage reference circuit

WBAN – Wireless body area network

WMSN – Wireless multimedia sensor network

WSN – Wireless sensor network

WWTP – Waste water treatment plant

Chapter 1

INTRODUCTION

1.1 Motivation and context

The capability of electronic circuits to obtain energy from the surrounding environment, for self powering, is an interesting feature that has gained increased attention [1], either for sensor networks [2], [3] or embedded systems [4]. This capability allows for electronic devices to operate without the need to be connected to the power grid, nor the replacement of batteries on a regular basis [1], [3], [5], [6]. This feature is especially important for sensor networks, because the remote sensor nodes can be deployed to any place where a sufficient amount of energy can be obtained from the environment. These networks can be used in a wide range of applications [3] and therefore, the design of low-cost energy harvesting devices and networks is attracting more attention [2]. This philosophy is promising to take over the powering paradigm, in opposition to traditional powering methods, involving batteries or a cord connection to the power grid. Moreover, if there is the intent of deploying a wireless sensor network (WSN) where the extension of the power grid is infeasible, or the replacement of batteries has a large cost, the use of self-powered nodes is the only option. Sensor networks that solely rely on grid connections are limited by having the sensors located close to a power outlet or from the power grid. Thus, if one wants ubiquity and pervasive operation, relying on the power grid is an evident limiting factor.

One step forward, towards unlimited sensor location, could be the use of batteries. This allows for complete freedom in the location of the sensors. However, one last obstacle remains,

which is the batteries themselves, because as their stored energy gets depleted, they need to be replaced. Eventually, this can be a problem if a large number of sensors are deployed and if they reside in places that are difficult to reach. As such, the trivial operation of battery replacement can become expensive and burdensome.

To achieve indefinite operation in inhospitable locations, the sensors must be powered in such a way that they can obtain their power directly from the surrounding environment. This kind of procedure is commonly known as energy harvesting, or energy scavenging. Besides its ubiquitous facet, energy harvesting also reveals to be interesting both in ecological and economical terms. Avoiding the need of batteries, for system main powering purposes, the sensor system will not be responsible for contributing to chemical pollution caused by disposing of batteries, or even their manufacturing, in the first place. In economical terms, not using batteries represents cost reduction both in devices and replacement procedures.

Energy harvesting systems can obtain energy from different sources: light (solar [5] or artificial [7]), electromagnetic emissions [8], mechanical movements (e.g. vibrations) [9], thermal gradients [10], etc. All of these sources share a common limitation: low energy density. This means that the electronic circuits inside the sensor node must operate using extremely low energy levels and must have efficiencies as high as possible. This poses significant design challenges. Furthermore, in many applications, the very limited available energy forces the circuits to remain in a power-down state for most of the time, until enough energy has been harvested and stored. Among all energy sources, light is the one with the highest density by volume unit, for low-power systems [5]. Moreover, photovoltaic (PV) cells are more compact devices than those that harvest energy from other sources and can be compatible with some CMOS processes [11].

In indoor environments, it can be preferable to have a sensor, or network of sensors, self supplied, in order to avoid the use of any cord connection. Using harvested energy, the costs of material like cable duct, the tangling of wires, or any other inconvenient can be avoided, in addition to having the freedom to put the nodes where exactly required. Energy can also be obtained from the light existing indoors, however, using indoor light to power an electronic application, represents an increased challenge. The levels of available light energy inside buildings are much lower than those that can be obtained outside and the available light energy in indoor environments can vary significantly, since the light from the Sun is attenuated and can be mixed with artificial light.

This thesis describes an indoor light energy harvesting system intended to power a sensor node, enabling a network similar to the one described in [12]. Although designed to cope with

indoor light levels, the system is also able to work with higher levels, making it an all-round light energy harvesting system.

A powered sensor circuit can work in an ON-OFF regime, with a low duty-cycle. When the voltage in a storage capacitor becomes larger than a certain value, the sensor circuit can be turned on, drawing current from the storage capacitor, thus reducing its voltage. This will control the maximum output voltage produced by the harvesting system.

The system that will be developed in this thesis should be fully integrated (except for the PV cells and the energy storing large value capacitor), to minimize size and cost.

The harvested energy can be stored, either in a supercapacitor [13], [14], or in a rechargeable battery [15]. The use of any of these devices enables the node to work when there is no energy available from the environment. In order to maximize the harvested power from a PV cell, it is necessary to use a DC-DC converter that can track the MPP of the PV panel. In this thesis, it is proposed to develop a MPPT DC-DC converter based on switched-capacitor (SC) networks instead of inductors [15], to reduce both the cost and volume of the system. The MPPT algorithm will be implemented in the analog domain to save power, putting aside any implementation based on a microcontroller. It is believed that by combining the experiences of specifically designing PV cells for this application, tailored to work in an indoor environment, and also designing optimized electronic circuits for energy conditioning at very low power levels, an innovative solution can be achieved.

Given that some amount of harvested energy is needed to power the control circuits, it is expectable that the efficiency, at this power level, will yield a lower value than that of a larger power application, using the same principles and algorithms. The maximum efficiencies are between 60% to 70% [13], [15]. One thing to keep in mind is that the total harvested energy must be such that it can be made useful for powering the desired application or circuit, and also to self-power the control circuitry that manages the harvester. This demand is formally stated in literature, as the *Energy Neutrality* [4], [16]. Generally speaking, the system will be able to work whenever it has the available energy to do it. If the system has the ability to permanently harvest enough energy from the environment, then it can permanently operate, although occasional interruptions may eventually exist. This means that interruptions will have to be tolerable, or even they can be a strategy of operation. There are a number of strategies that can be adopted, according to the type of system usage [16].

The objective of this thesis is not to develop a wireless node for a specific application, but to show that it is possible to manufacture the harvesting section, such that it can work with the available energy from its surroundings, proving that this concept can be viable. It is expected

that the developed system can be adapted to work with different types of sensors such as temperature, pressure, light, etc. If the purpose of the system is to transmit the light intensity received by the PV cells, then this information will be available from the operating frequency of the DC-DC converter. Such a node could prove its usefulness by monitoring the light conditions inside a room and, using this information, adjust the illumination to an optimal level, optimizing the electrical energy usage. This is why the system must be robust enough to operate in indoor environments, where the available light is substantially less than in outdoor scenarios [16].

Another strong motivation deals with economy and with environmental sustainability. As the overall system is intended to operate without the need of common batteries to get powered, it will pay off in the long term, since there is no need to buy additional powering components. Moreover, the power received from the surrounding environment, is zero-cost.

In addition to the economic benefit, not using batteries also means that it will not be necessary to use any process for recycling drained devices. This environmental aspect is particularly important, even though the most recent generation of batteries is progressively making use of less polluting materials. Yet a more primary consequence of avoiding battery powering, is the fact that batteries do not even need to be manufactured, in the first place.

According to the present trends, and thinking about a broader application, the node supplied by the proposed system could be a part of the Internet of Things (IoT).

1.2 Original contributions

The main contributions of the work carried out in this thesis are concentrated in the development and improvement of CMOS circuits for micro-power DC-DC converters to work with PV cells, including the implementation of MPPT algorithms using low-power controller circuits. These contributions have led to the production of various papers in conferences and journals of the area. The main contributions of this work are summarized next:

- A step-up micro-power converter for solar energy harvesting applications, based on a switched-capacitor voltage doubler architecture with MOSFET capacitors, was developed in [17]. The use of MOSFET capacitors results in an area approximately eight times smaller than when using MiM capacitors for a 0.13 μm CMOS technology. In order to compensate for the loss of efficiency, due to the larger parasitic capacitances, a charge reusing scheme is employed. An extended version of this work is provided in [18], presenting a more complete characterization and results.

- A DC-DC step-up micro-power converter, using a SC voltage tripler architecture, controlled by a MPPT based on the Fractional Open Circuit Voltage method, was developed in [19]. This circuit was designed in a 0.13 μm CMOS technology, in order to work with a a-Si PV cell. The use of this simpler method allowed for having a reduced power dissipation in the MPPT controller circuit. The system has a local power supply voltage, created using a scaled-down SC voltage tripler, controlled by the same MPPT circuit, to make the circuit robust to load and illumination variations. The SC circuits use a combination of PMOS and NMOS transistors to reduce the occupied area. The same charge reusing scheme is used just like before.
- A step-up micro-power converter using a SC voltage tripler, controlled by a MPPT circuit based on the Hill Climbing algorithm was developed in [20]. This circuit was designed in a 0.13 μm CMOS technology in order to work with an a-Si PV cell.
- An analysis of the pertinent issues about designing and developing a DC-DC converter for a low-cost, micro-power indoor light energy harvesting system, using CMOS technology, was published in [21]. From this analysis a possible solution is discussed.
- A voltage limiter circuit for indoor light energy harvesting applications was developed in [22]. This circuit ensures that, even under strong illumination, the generated voltage will not exceed the limit allowed by the technology, avoiding the degradation, or destruction, of the integrated die.
- A start-up circuit for the micro-power indoor light energy harvesting system was developed, manufactured in a 0.13 μm CMOS technology, and experimentally evaluated in [23]. This start-up circuit achieves two goals: firstly, to produce a reset signal, power-on-reset (POR), for the energy harvesting system, and secondly, to temporarily shunt the output of the PV cells to the output node of the system, which is connected to a capacitor. This capacitor is charged to a suitable value, so that a voltage step-up converter starts operating, thus increasing the output voltage to a larger value than the one provided by the PV cells.
- A micro-power light energy harvesting system for indoor environments, aimed to work under realistic indoor light intensities, was designed, manufactured and experimentally evaluated in [24]. In this system, light energy is harvested by a-Si:H PV cells, processed by a SC voltage doubler circuit with MPPT and, finally, stored in a large capacitor. The circuit occupies an area of 0.31 mm^2 in a 130 nm CMOS technology. Experimental results show that the proposed system, using PV cells with an area of 14 cm^2, is capable of starting-up from a 0 V condition, with an irradiance of only 0.32 W/m^2. After

starting-up, the system requires an irradiance of only 0.18 W/m^2 (18 $\mu W/cm^2$) to remain in operation.

- A feasibility study, to check the most suitable PV technology and the levels of available indoor light energy (and their worst case), aiming to enable an indoor WSN, was made in [25]. It could be confirmed that a-Si PV cells are the most adequate for indoors.

1.3 Thesis organization

This thesis is organized as follows: Chapter 2 presents an overview about Energy Harvesting electronic systems, namely regarding energy harvestable sources and a comparison between them. Chapter 3 shows a study about PV cell technologies, an integrated CMOS PV cell that was actually implemented and a light energy availability assessment in indoor environments, in order to check the realistic conditions of the design. Chapter 4 shows the issues related to DC-DC converters, MPPT techniques and energy storing devices. In Chapter 5 it is presented the design of the proposed system. The step-up converter architecture, the design of the ASM that controls the switching and the MPPT technique than is jointly used are described. Chapter 6 presents the physical implementation of the the system, i.e. its layout in integrated circuit, using a CMOS technology. In Chapter 7, it is presented the experimental testbed, its details, and the results that were obtained from the complete manufactured prototype, composed by the integrated system and the PV cells. Finally, Chapter 8 presents the conclusions about this work, discussing the issues and the results that were shown, and future perspectives are also suggested. In Chapter 9, the complete list of literature references is given, which served to aid in the making of all of this work.

Additionally, there are four appendixes. In Appendix A, the light measuring device, used for the light availability study performed in Chapter 3, as well as its accessories, is presented so as to have an overview about it. Appendix B presents the manufacturing, characterization and analysis process of an amorphous silicon PV cell that has been specifically designed and manufactured for this work. The results about a prototype cell are presented, consisting on the parameters that can be used to model the cell for different ambient light intensities. In Appendix C it is presented a short study about how to use the waveform results given by the simulations in Spectre, so that the correct measurements about power can be computed, when dealing with SC circuits. Finally, in Appendix D, it is presented the simulated performance of a MPPT method, the Hill Climbing, firstly thought to be also included in this thesis. This inclusion did not happen but, as promising results about it had been published, it seemed worthy to briefly show the phase generator that was designed and the set of results that was achieved.

Chapter 2

ENERGY HARVESTING ELECTRONIC SYSTEMS

2.1 Introduction

This chapter presents a literature review about the various ambient energy sources that can be harvested and the description of some related systems. As such, Chapter 2 will provide a brief overview about each source and describe some systems that use that same energy source. This will be extended on to the domain of the wireless sensor networks and the aspects related to it, being presented some examples of energy harvesting powered WSN in different environments. A brief description of what is expected from each network and how it succeeds in harvesting the energy that enables it to work, will receive a particular focus.

Since light is the energy source being harvested, in order to power the system described in this research thesis, some more attention will be dedicated to the analysis of this source. Proceeding with this purpose, a more detailed overview about PV technologies will be given in Chapter 3. In addition, a more focused insight covering DC-DC converters, energy storing devices and MPPT techniques, will be given in Chapter 4, so as to complete the literature review opened up in the present chapter.

2.2 Available energy sources

In the surrounding environment, there are a number of possible energy sources that can be conveniently harvested, in order to power electronic applications [5]. Depending on whether a certain energy source is more abundant, that could be the preferred one.

However, another possible configuration that performs ambient energy scavenging relies on the conjunction of multiple energy sources, like in [3], [5], [10] and [26]-[29]. The latter is a highly miniaturized system, designed to have modularity, in the sense that one can add or remove IC layers, which communicate among themselves using the I^2C protocol. This system occupies a volume of only 1 mm^3, entering in the category of smart dust, which are wireless sensor nodes with perpetual energy harvesting. Next, Fig. 2.1 shows the evolution in terms of volume reduction that occurred over the past decades, in conformity with Bell's law, as stated in [29]. This law is somewhat related to the well-known Moore's law [30], although the latter may probably be reaching its limit [31].

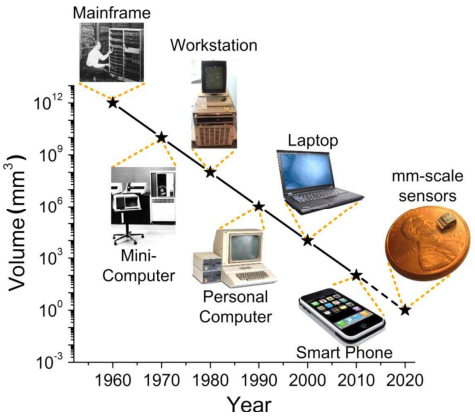


Fig. 2.1 - Continuous down-scaling of micro-size computing systems [29].

The scavenged energy sources more commonly used are presented in this chapter and very briefly described and characterized in the following subsections, as a more detailed overview is outside the scope of this thesis. However, relevant references will be given, in order to aid in getting a broader insight about each source and related systems that are specifically designed to work with it.

2.2.1 Mechanical

Mechanical energy can be harvested from various natural sources, such as wind [32], wave motion [33], vehicle motion, or in general, any kind of vibrations or movement, namely, by resonance. There is an important issue specific to mechanical energy harvesting systems, which is the need to have rectifying circuits. As one is dealing with alternating signals, an AC to DC conversion must be carried out. The rectifiers can be passive or active. The former ones are

based on diode topologies, namely, rectifier bridges, while the latter ones employ some means of switching power conversion, as in [34].

There are several ways of converting mechanical energy into electrical energy, from which one can choose. This conversion can be done by using electromagnetic ([5] and [8]), piezoelectric [9] or electrostatic means [35]. According to [8], the most suitable materials to harvest mechanical energy are those that exploit the electromagnetic and the piezoelectric principles, possessing the highest power density, when compared to the electrostatic ones. Each of these materials has a different electrical behavior, and thus, when using any of them, a different electric interface must be used. Harvesters exploiting vibrations, presently have an efficiency ranging from 25% to 50% [36].

2.2.1.1 Electromagnetic conversion

In order to have the possibility to perform simulations, destinated to check any proof of concept, it is necessary to have a model of the harvester device. In the mechanical context, when dealing with electromagnetic conversion devices, it is usual to have finite element method (FEM) models, so as to have a suitable representation of the harvester. This model can be used in conjunction with electric circuits, in order to enable a simulation. For example, in [8], an electromagnetic energy harvester is studied using this approach. In Fig. 2.2 a), it is given an idea of how the FEM model looks like. Subsequently, this gives origin to a block diagram model at numerical level, which is shown in Fig. 2.2 b), and this one can then be translated to Spectre, for example, allowing for electric simulation. Also, it is to note in Fig. 2.2 b), how the kinematic variables are involved. Electromagnetic transducers generate a voltage offering a low impedance output.

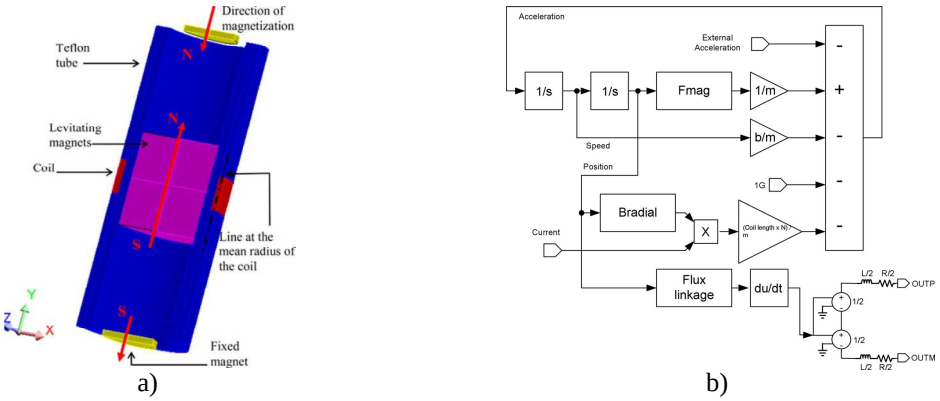


Fig. 2.2 - FEM model of an electromagnetic conversion device [8].

Tipically, electromagnetic conversion is used for larger power levels than the ones aimed by this thesis and, therefore, it will not be addressed further. Moreover, the cost of this type of converters is higher than for other types.

2.2.1.2 Piezoelectric conversion

There is a material, Lead Zirconia Titanate (PZT), widely used for this conversion, which is considered as the silicon counterpart of piezoelectric materials, when dealing with engineering applications, as it can be found in [1], [28] or [37].

A piezoelectric energy harvester is typically a cantilevered beam with one or two piezoceramic layers, which can vibrate in various vibration modes. The induced strain is converted into electrical charge, originating a voltage. The generated voltage is proportional to the force, and thus, to the vibration magnitude applied to the harvester. However, piezoelectric energy transducers are characterized by a high impedance output, unlike conventional voltage sources. This results in the need to use appropriate electric circuits that correctly interface with this type of transducer. The voltage generation mechanism is illustrated in Fig. 2.3.

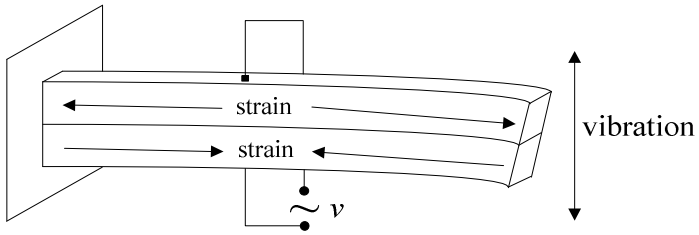


Fig. 2.3 - Voltage generation mechanism in a piezoelectric harvester.

This kind of mechanism is bidirectional, such that by applying a voltage will result in a deformation, meaning that these materials can be used both as sensors or actuators.

The simplified electric model of a unimodal piezoelectric harvester is represented in Fig. 2.4 a).

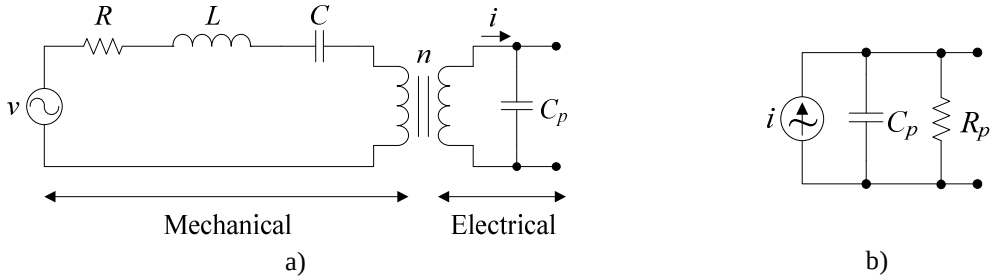


Fig. 2.4 - Simplified model of the piezoelectric harvester [38].

At the left hand side of Fig. 2.4 a), the mechanical part of the model is represented, where *R*, *L* and *C* represent the mechanical parameters loss, mass and stiffness, respectively. The transition from the mechanical to the electrical domain is modeled by a transformer with a ratio of *n*, where the conversion from stiffness to the current *i* is performed, instead of using the generated voltage directly. At the right hand side, i.e. in the electrical domain, C_p represents the

plate capacitance of the piezoelectric material. When at resonance, the whole circuit can be simplified to a current source in parallel with a capacitor and a resistor, in which the latter represents the losses. This model is depicted in Fig. 2.4 b). With this circuit, the MPP condition can be achieved if the load connected at the output is the conjugate of the impedance represented by C_p and R_p, i.e. the load must have an inductive component.

2.2.1.3 Electrostatic conversion

Micro electrical mechanical systems (MEMS) are well suited to collect mechanical energy. Devices using this kind of technology can be built so as to be compatible with CMOS integration, in order to lay out both the harvester and the energy processing system in the same die.

Basically, the harvester can consist of a simple variable plate-distance capacitor. The energy conversion can be achieved in two ways, either by varying the gap between the plates or varying their overlap. A simple way to illustrate this principle is by looking at Fig. 2.5, representing a rest position, from where the moving plate can suffer a translation along any of the axis, as a consequence of vibrations or any other motion.

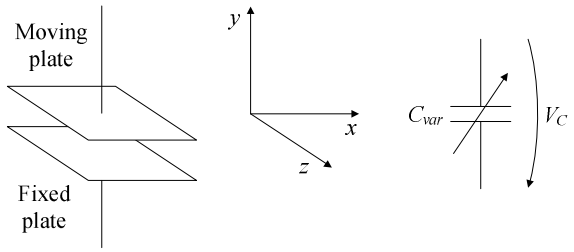


Fig. 2.5 - Symbolic representation of the conversion mechanism using MEMS.

If this translation occurs along the *y* axis, the distance between plates will vary, and the capacitance will vary accordingly, in an inversely proportional way. On the other hand, if the translation occurs along the *x* or the *z* axis, the plate overlap will decrease and so will the resulting capacitance. If the capacitor is pre-charged and then kept open-circuited with a constant charge, the capacitance variation will change the voltage of the capacitor (V_C) and, consequently, the stored energy [39].

The variation of capacitance is given by the parallel plate capacitor equation,

$$C_{var} = \varepsilon_0 \varepsilon_r \frac{A}{d}, \tag{2.1}$$

and relies on modifying either the superposition area of the plates of the capacitor (*A*), the distance between plates (*d*) or even the dielectric constant of the insulation material between plates (ε_r), if a different material is inserted in between. ε_0 is the dielectric constant of vacuum.

By having established the value for the variable capacitance, the voltage that appears at the terminals of the capacitor is

$$V_C = \frac{Q}{C_{var}}, \tag{2.2}$$

and the energy that can be used thanks to this generation process, if the capacitor is discharged over a resistor R during an interval t_{on}, is

$$E(t) = \int_0^{t_{on}} \frac{V_C^2}{R} e^{-\frac{2t}{RC_{var}}} dt. \tag{2.3}$$

MEMS are also compatible with both the piezoelectric and electromagnetic processes.

2.2.2 Thermal gradients

Obtaining energy from temperature sources may be an option in certain contexts, for instance, where there are high temperatures, like furnaces or exhaust pipes. These can be conveniently scavenged as a thermal source, providing a consistent amount of power [1], [5], [10], [37].

Thermoelectric generators (TEG) have the advantageous characteristics of requiring little or none amount of human intervention during their useful lifetime. Moreover, these devices are reliable and quiet, as there are no moving parts.

Current thermoelectric materials can only convert a maximum of 5% to 6% of the useful heat into electricity. However, significant research is being carried out, in order to develop new materials and module constructions which can eventually reach a harvesting efficiency higher than 10% [40].

A thermoelectric element converts thermal energy, in the form of temperature differences, into electrical energy and vice-versa. Devices using Bi_2Te_3 have already proven their usefulness [37] and showed to possess the highest figure of merit [41], defined as

$$Z \cdot T = \frac{\alpha^2 \sigma}{\lambda} \cdot T, \tag{2.4}$$

in which, T is the temperature, α is the Seebeck coefficient, σ is the electrical resistivity and λ is thermal conductivity. Using this material, for temperatures between -50 ºC to 80 ºC, the figure of merit in (2.4) can reach values up to unity.

The drawback behind this kind of source comes from the hostile environment to be scavenged, having to take particular care with the electronic circuits being powered. Thermopiles are among the other types of devices to achieve harvesting from this kind of source, but there are also some novel devices and systems under research [1], [42].

The model of a thermoelectric energy harvester is a simple Thévenin equivalent circuit, like the one shown in Fig. 2.6.

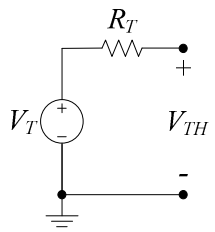


Fig. 2.6 - Electrical equivalent of the thermoelectric generator.

The voltage V_T is an open circuit voltage proportional to the temperature difference between both sides of the TEG, and to the Seebeck coefficient. The latter depends on the material being used and represents a measure of the magnitude of an induced thermoelectric voltage, in response to a temperature difference across that same material. In the model of Fig. 2.6, resistance R_T represents the loss of the model of the TEG and V_{TH} is the output voltage of the harvester. According to the maximum power transfer theorem, the maximum power point can be achieved by matching a load resistance to the source resistance, R_T.

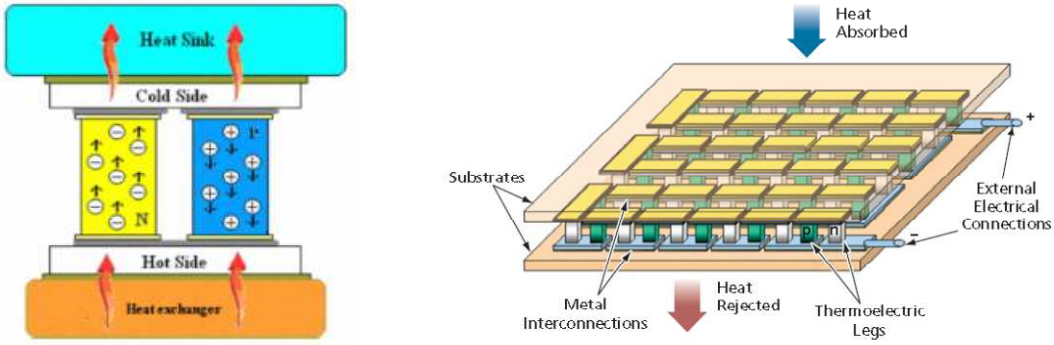
The Seebeck effect is the generation of an electromotive force within two different metals, when their junctions are maintained at different temperatures. A common application of this principle is the use of thermocouples to measure temperature. However, when a thermocouple is used in temperature measurements, the electromotive force being generated is countered by an applied voltage, resulting in no current flowing. The main difference, between using the thermoelectric effect for temperature measurement or for power generation, is the use of semiconductor materials, instead of metals, when the purpose is the latter. This use enables the flow of current in the generator, allowing it to produce power.

The Seebeck coefficient is defined as the obtained voltage variation in response to each degree of temperature gradient. Thus, the thermoelectrically generated voltage in the model of Fig. 2.6 (V_T), is given by (2.5), where S is the Seebeck coefficient (expressed in V/K), which is material-dependent, and ΔT is the temperature difference between the hot and the cold sides of the harvester device.

$$V_T = S \, \Delta T \ . \tag{2.5}$$

Semiconductor materials have a significantly higher Seebeck coefficient, when compared to metals, and so they are more suited to manufacture power generator devices. The Seebeck effect in the n-type material creates a flow of excess electrons from the hot junction to the cold one. In the p-type material, holes migrate toward the cold side creating a net current flow which is in the same direction as the one in the n-type material.

In Fig. 2.7, the schematic structure of a typical semiconductor thermoelectric device is shown.



a) b)

Fig. 2.7 - Typical structure of a semiconductor thermoelectric harvester a) [40] and b) [43].

The device in Fig. 2.7 b) includes multiple n-type and p-type thermoelectric legs sandwiched between two high-thermal-conductivity substrates. The n-type and p-type legs are electrically connected in series by alternating top and bottom metal contact pads. Because, in the depicted situation, heat is flowing from top to bottom, all of the thermoelectric legs are thermally connected in parallel. In the cooling mode, an externally applied electric current forces the heat to flow from top to bottom. In the power-generation mode, heat flowing from the top to the bottom drives an electric current through an external load.

MEMS structures are also used for building TEG and, in [43], a new MEMS fabrication method is presented.

For example, a WSN able to monitor the health of the structure of an aircraft can be established [41]. One of the main advantages of a WSN is to avoid complex wiring, saving material and, consequently, weight and cost. The temperature difference obtained between the aircraft cabin and the aircraft body shell, at high altitudes, can be such to obtain a high potential.

At a bigger scale, thinking about renewable energy sources and environmental issues, [44] proposes using ocean thermal energy conversion (OTEC), by taking advantage of the difference of about 20 ºC existing in sub-zero regions. Since the water is almost at freezing level, and the outside temperature can be at about -20 ºC, this permanent temperature gradient is suitable for thermal energy harvesting. At a smaller scale, this factor could be interesting to deploy a WSN in these geographical zones of the ocean, with the nodes being supplied by this harvestable source.

There are also environments at a much smaller scale, such as wireless body area networks (WBAN), which can also make use of thermal gradients, by using human warmth. This topic will be further explored in Section 2.2.4.

More recently, new technologies have been developed by using an innovative concept of mixing mechanical and thermal energy to harvest energy. This is done by firstly using heat to provoke a deformation in a material, such as a bimetallic. Secondly, that deformation, by electrostatic conversion (see Section 2.2.1.3), is used to produce energy. Such developments can be found in [45] and [46]. According to [46], the energy generation principle is explained next, as represented in Fig. 2.8.

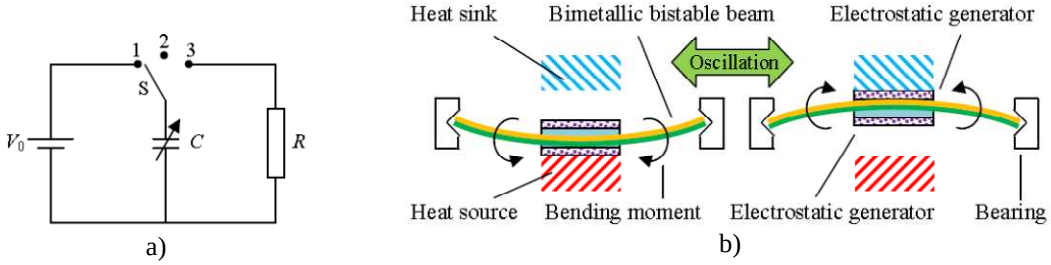


Fig. 2.8 - a) Electrostatic power generation principle under constant charge mode; b) complete harvester in operation: (left) in contact with heat source and (right) in contact with heat sink [46].

Referring to Fig. 2.8 a), with S in position 1, the capacitor *C*, with a maximum capacitance, C_{max}, is charged to V_0. Afterwards, with S in position 2, the capacitive generator is heated up. The dependency of its dielectric permittivity on temperature, leads the capacitance to be reduced to a minimum value, C_{min}. Finally, with S in position 3, a load resistance is connected at the output, dissipating the generated energy. Thereafter, the capacitive generator is cooled down and its capacitance is brought back to C_{max}. After this cooling phase, S returns to position 1. The whole cycle generates a net energy proportional to the difference of capacitance between the beginning and the end of the cycle. If this cycle is periodic, it can be considered that the material is undergoing a vibration with a given frequency. In Fig. 2.8 b), the complete harvester operation is schematically shown.

2.2.3 Radio Frequency electromagnetic energy

In environments mostly located in urban areas, one source that becomes appealing to be harvested is the radio frequency (RF) energy. This energy exists around every place and is generated by sources such as radio and television broadcasting, mobile phone cellular network, Wi-Fi networks and other sources alike.

One important factor that makes this source very appealing to harvest, is the fact that ambient RF energy, as a power source for outdoor sensor nodes, is typically available all the time, either day or night.

As the harvested signals are AC, in order to provide at the end of the chain a stable DC supply, it is necessary to use rectifiers to perform such a conditioning, like it can be found in

[10], [28] and [47]. Harvesters exploiting the RF sources, presently have an efficiency that can go up to 50% [36].

The low magnitude of the voltages resulting from the RF energy harvesting process is at such reduced level, that the design of rectifiers is very challenging, since many half-wave or full-wave diode rectifiers require non-zero turn-on voltages to operate.

Typical rectifier circuits are based on the well-known diode bridge. These can make use on NMOS or PMOS transistors, and can implement half or full-wave rectifiers. According to design parameters and required performance, some trade-offs must be adopted.

In Fig. 2.9, it is shown a way of implementing a MOSFET rectifier circuit using NMOS devices [28]. Voltage v_{in} represents the RF source being harvested.

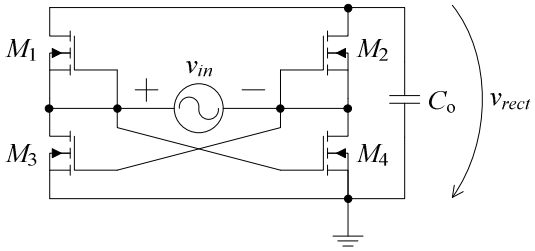


Fig. 2.9 - NMOS full-wave rectifier.

The rectifying process is as follows: when v_{in} is in its positive half cycle, M_1 and M_4 are conducting current, while M_2 and M_3 are in open circuit. During the negative half cycle of v_{in}, the roles of the transistors are exchanged. At the end, the rectified voltage v_{rect}, will ideally be a DC voltage, appearing at the terminals of the filtering capacitor C_o.

With circuits like the one shown, a low voltage drop (v_{ds}) in the transistors implies using wide channels and low frequencies. On the opposite, narrow channels imply a higher voltage drop and the operation at higher frequencies. If, instead of just one transistor, several transistors are connected in parallel, the performance of the rectifier can be improved in terms of working frequency and voltage drop. This technique divides the total current by each one of the transistors in the parallel, thus reducing the voltage drop of each individual device. In addition, frequency can also be improved, because the size of each transistor is smaller, as compared to having just one big transistor. In [28], the implementation of full-wave rectifiers allowed to obtain voltage drops as low as 0.2 V and operating frequencies of 16 MHz, by using a parallel structure of transistors with W = 10 μm and L = 0.28 μm.

In [47], a different type of rectifier is used, by making a field-to-voltage conversion, which is not grounded. This structure is depicted in Fig. 2.10, where v_{in-} and v_{in+} connect to an antenna or similar device.

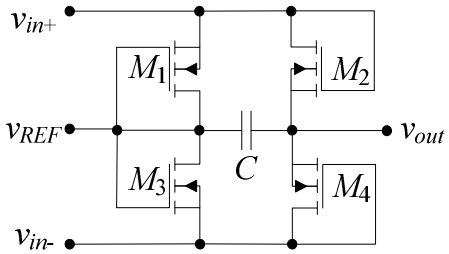


Fig. 2.10 - Full-wave rectifier, acting as a field-to-voltage converter.

The v_{REF} terminal allows for offsetting the output voltage v_{out}. Using this structure, it is possible to stack several of these modules, in which the lower one can have v_{REF} grounded, while its output terminal connects to the v_{REF} terminal of the next structure, and so on. By doing so, the contribution of each rectifier helps to effectively increase the overall output voltage, so as to have, at the output of the upper structure, a suitable value to power an electronic application. A more detailed study of MOSFET rectifiers is done in [48], where the transistors are working in the weak inversion region, having all of the terminals being exploited.

This RF energy source appears typically in a very limited amount, representing a very low power density [1]. In order to assess the real availability of energy that could be made useful by using RF sources, by performing power density measurements, [49] surveys the expected power density levels from GSM 900 and GSM 1800 base stations at a certain distance, and also in a WLAN environment. According to it, for distances ranging from 25 m to 100 m from a GSM base station, power density levels range from 0.1 mW/m^2 to 3.0 mW/m^2. Measurements in a WLAN environment indicated even lower power density values, thus making GSM and WLAN unlikely to produce enough ambient RF energy for wirelessly powering miniature sensors. Also according to [49], a single GSM telephone has proven to deliver enough energy for wirelessly powering small applications at moderate distances.

In general, the levels of power density are very dependent on the frequency of operation and on the distance between the transmitter base station and the receiving harvester.

At a bigger scale, thinking about grid power transfer, [50] presents some results about wireless power transfer, although at reduced distances, as electromagnetic energy has a strong decay over distance and with the frequency being used.

An essential part of this kind of system is the antenna, in order to capture the radio signals. There is a system that agglutinates the functionality of antenna and rectifier, which is called a rectenna. These devices, and antennas in general, have a relatively low conversion efficiency, but this parameter is dependent on the frequency of operation. As such, the key parameters to have into consideration are bandwidth, polarization, directivity and size. In order

to be sensitive to a wider range of frequencies, the antenna must tend to be bigger, in order to capture the lower frequencies. The work in [51] presents an architecture for a RF energy harvesting system, where the system components like the antenna and the ultra wide band (UWB) input matching *LC* network are designed and studied in depth, as well as the optimum rectenna load. Also, a study about the availability of RF ambient energy, coming from digital television broadcasting in a given geographical area and its surroundings, is carried out in [51].

The work developed in [52], besides making use of television broadcasting, also uses the energy radiated by the base transceiver stations of the mobile telephone networks. The collected energy is sufficient to power a sensing application, whose objective is to transmit information about temperature and light. The duty-cycle being used is very small, and the firmware is implemented with particular care about reducing computationally consuming operations.

The applications described in [10] and [28] make use of radio frequency (RF) power as a resource to be harvested in conjunction with other sources. However, in [47], [51] and [52], this is the only source being scanvenged.

Another important set of applications that make use of RF energy harvesting are the radio frequency identification (RFID) tags, widely disseminated in commercially available consumer products. When queried by a reader device, the tag is momentarily powered by a RF signal close to it, and responds by sending a coded identification number. The same type of device can also be used to identify livestock or pets, in which the tag is implanted beneath the skin.

To harvest the electromagnetic energy in RFID systems, an antenna or an inductor coil must be used. However, as with other sources, this RF energy may present itself unpredictable and very dependent on the distance at which the reader is put from the tag. In [53], a system is presented in order to enhance range operation. Due to the dependence on the distance between the reader and the tag, voltage limiter circuits must be used to prevent any damage to the tag being read. Examples of limiter architectures with such a purpose are presented in [54] and [55].

2.2.4 Human generation

The idea behind using applications powered by a human source is very interesting and has captivated the interest of researchers since some years ago [56]. The human body provides multiple sources of energy that can be harvested. According to [57], it has been shown that, ideally, 2.4 W to 4.8 W of power is available in body heat, 0.4 W in exhalation, 0.37 W in blood pressure, 0.76 mW to 2.1 mW in finger motion, 60 W from arm motion, 67 W in heel strike, 69.8 W in ankle motion, 49.5 W in knee motion, 39.2 W from hip motion, 2.1 W in elbow motion, and 2.2 W in shoulder motion.

The necessity of providing energy to wearable computing devices, made the conversion of human motion into useful electrical energy, a topic of extensive study. For instance, in gyms, there is some equipment, like exercising bicycles that have their instrument panel powered by the user who is exercising. However, in such a situation, the user must strive forcefully into the production of the required energy. More broadly, in energy harvesting generated by human motion, the preferable situation is to have the user oblivious of such an action, while providing the necessary energy to power an electronic application. For example, the kinetic energy from human motion is already used to power electronic wrist watches [58]. In the medical domain, electronic medical implants can be powered by using the human heat as a power source.

In fact, the energy generated by human means is coming from a particular environment where there coexist some of the sources already described, namely, the thermal gradients and the mechanical energy sources, but that are not restricted to these. Energy harvesting of electromagnetic radiations is also possible with the human body, as it will be shown ahead.

A very important class of applications, in a human energy harvesting environment, is the implantable bio sensor. There are some requirements for these sensor systems, which are the reduced size, the complete absence of user intervention, once the applications have been deployed into the body, and the possibility of these applications to be hermetically sealed. All of these requirements come from the fact that the applications are to be deployed inside the human organism.

An increased challenge exists, when using the human-originated energy sources, because of the limited power densities that these provide. When compared to sources originated in an industrial or outdoor environment, a single human body provides a reduced amount of power.

With respect to the mechanical generation, the movements of the body occur at a very low frequency, and concerning the thermal gradients, the difference of temperature between the human body and the outside environment is not very high, except perhaps, in extreme cold conditions. Moreover, if the body is immobile, a great deal of potentially available mechanical energy is not available. The best place to put a sensor powered by mechanical means would be in a limb, because this zone is prone to have a greater mechanical activity.

The limit values of the power generated from a linearly-excited motion-driven generator with linear proof-mass motion, mounted on a walking person, when using a conventional MEMS-compatible and inertial micro-generator strapped to the human body are presented in [59]. This is schematically shown in Fig. 2.11. These values are between 1 μW and 4 μW for a device occupying around 0.25 mm^3, rising to between 0.5 mW and 1.5 mW for a generator occupying 8 cm^3.

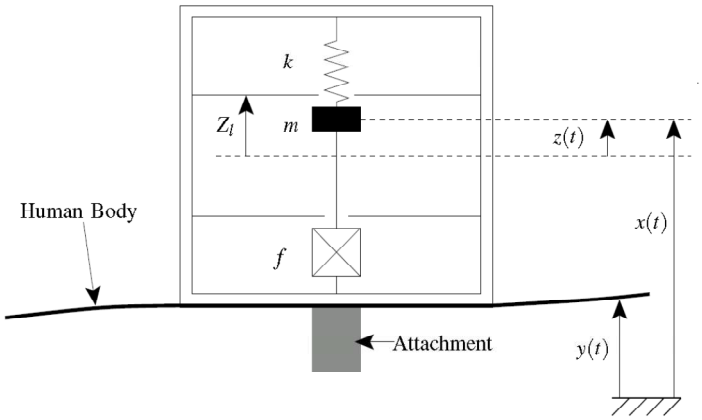


Fig. 2.11 - Inertial generator attached to the human body [59].

In addition, it is presented the upper limit of the power generated from a vibration-driven device in a human worn application, which is

$$P_{max} = 2\frac{Z_l Y_0 \omega^3 m}{\pi}. \tag{2.6}$$

In (2.6), and having into attention Fig. 2.11, Z_l is the amplitude of the inertial mass motion, Y_0 is the amplitude of the driving motion, m is the value of the proof mass and ω is the angular frequency of the driving motion. Also in [59], it is assumed that when a person is running at 12 km/h, Y_0 is 0.25 m and the excitation frequency is around 2 Hz.

The light energy source has some drawbacks when used in the human context. These, are the light availability for implanted devices, or even if the latter are worn under clothing. Although light is a very important source of power, it has been shown that thermoelectric devices, also a reliable solid-state technology, are superior to PV cells in the WBAN domain.

For human implantable devices, the thermoelectric generators are receiving increased attention. In order to maximize the amount of power that can be harvested, it is important to match the output impedance of the harvester with the load being supplied, both at the electrical and at the thermal domain. According to [59], the maximum of electric power that can be extracted from a thermoelectric generator is

$$P_{max} = \frac{(n S \Delta T_{TEG})^2}{4R_T}. \tag{2.7}$$

In this expression, n is the number of P and N elements like those in Fig. 2.7 a) and b), S is the Seebeck coefficient, ΔT_{TEG} is the thermal difference and R_T, the electric resistance of the model of the thermoelectric generator, like the one in Fig. 2.6.

The human body has an almost constant temperature. This temperature is due to the metabolism, which has a power 58.15 W/m^2 over the body surface. A normal adult, with an

average surface area of 1.7 m^2, in thermal comfort and regular metabolism, has a heat loss of approximately 100 W. However, the metabolism can provide a value as low as 46 W/m^2, while sleeping, or as high as 550 W/m^2, when running at 15 km/h. During a common work day, sitting at an office, this value can be 70 W/m^2, corresponding to a power dissipation of 119 W and a burn of about 10.3 MJ during a day [60]. The thermal gradient is established between the body temperature and air around the body. Even if the generated energy is not enough to supply a sensor node on a permanent basis, the usual strategy is to accumulate the harvested energy, so that a transmission is enabled from time to time, powering the transmitter with the energy that has been harvested and stored, in the mean time.

In general, as documented in [59], one has power densities of about 300 $\mu W/cm^3$ and 20 $\mu W/cm^3$, representing the limits for kinetic and thermal devices, respectively, while the user is running. The values of 30 $\mu W/cm^3$ and 10 $\mu W/cm^3$ are the power density limits if the user is walking. The present challenge, which is still under active research, is the means to obtain the correct adaptability for the harvester, in order to match the electric and the thermal impedances, if the body of the user is undergoing a running or a walking regime.

Some specific applications have also been documented, like in [61], where an electromagnetic generator is used both as a harvester and a sensor, in a situation where the respiratory effort mechanical motion is the energy source. The harvested energy has been shown to be enough to continuously power a low-power microcontroller working with a low data rate wireless link, while monitoring the respiratory rate, and depth, of the user, with good accuracy.

A heel impact absorber harvester has also been developed, to store energy by using human locomotion [1], but in [57], a different approach is taken. Instead of heel impact, the human horizontal foot motion is used. This system uses this energy to charge a rechargeable battery. An interesting feature about this application is the introduction of a MPPT Perturb & Observe algorithm (which will be addressed in Section 4.6.3), optimized for low frequency human horizontal foot motion, in order to extract as much power as possible. The information provided by the MPPT controller is delivered to a PI controller, in order to establish the optimal switching rate of both a boost and a buck converter. The power density that can be achieved with this application is 8.5 mW/cm^3.

Another way of harvesting energy from human motion has been used in the Sustainable Dance Club [62], where the energy released by dancing people is used to power the light effects in the dance floor zone. The harvesting is performed by using dance-floor modules, in the form of tiles. A dancing person can, in average, generate a power of about 2 W to 8 W. In order not to be intrusive to the dancer and to his/her dancing experience, the floor tile is only allowed to

displace vertically by a few millimeters, thanks to using a high stiffness spring. Because of the nature of the involved movement, the working frequency is in the range of 1 Hz to 2.5 Hz. To match the harvester as best as possible with the load, it is considered that the combination of a single user plus platform weights about 70 kg to 100 kg. An additional advantage in this system is the fact that the energy is being locally generated, avoiding the losses occurred when energy is being transported by the power grid. The measured efficiency for this system was 48%, including the losses due to the diode rectifier.

The concern about obtaining the intended energy without interfering with the user, so that the harvesting process can be as seamless and unconscious as possible, is also present in [63], where a framework to harvest vibration energy from the human gait is presented. This framework is for calculating the optimal power output for both piezoelectric and electromagnetic vibration harvesters, covering energy harvesting for both walking and running gait of a wide variety of healthy subjects ranging from recreational to elite athletes. The generator is mounted on the lower leg because this is a zone that, because of the foot strike, shows a great acceleration and, simultaneously, allows for conveniently wearing the harvester.

On the other hand, instead of using the sensor in the lower leg, in [64], a miniaturized electromechanical generator, integrated into a human knee prosthesis, is used to power a sensor system inside the prosthesis, enabling it to transmit information about the load on the surfaces of the articulation.

The development of new piezoelectric materials is an active research field. In [65], it is shown the fabrication of piezoelectric rubber films and their applications in heartbeat sensing and human energy harvesting. It was demonstrated that the use of the piezoelectric rubber films can function as both sensing and powering elements, and potentially realize the integration of human physiological monitoring and energy harvesting.

The human body can even be used to harvest energy from electromagnetic radiations. According to a study performed in [66], it has been shown that the properties of the human tissues, which have a high dielectric constant, especially at low frequencies, are very suitable to receive the electromagnetic radiations of low frequency, emitted by the power lines in an indoor environment. Moreover, using an antenna would be very difficult to capture the same radiation because of the low frequency band and the narrow bandwidth. The harvested energy can be delivered to an application by simply making contact with the human body, as schematically shown in Fig. 2.12.

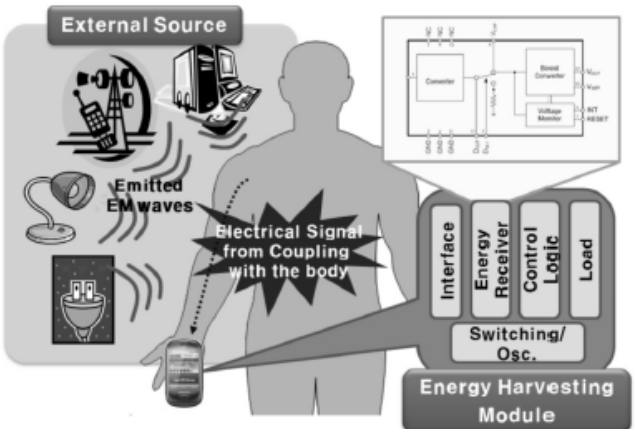


Fig. 2.12 - Energy harvesting from electromagnetic waves using the human body [66].

In [66], measurements were made in order to determine the effective length of the human body. The effective lengths had maximum values (about 5 cm) at about 40 MHz, which is large, considering the poor conductivity of body tissues. With higher and lower frequencies, the length decreases. In addition, measurements also included the estimated voltages received by the human body, which varies from place to place, according to the frequency predominance in the environment.

Another work that also studies the theme of electromagnetic energy harvesting using the human body can be found in [67].

2.2.5 Microbial fuel cells

The microbial fuel cell (MFC) principle is based on the electrochemical reactions that bacteria produce when in activity. The energy generated by these reactions can be harvested, similarly as with the other sources already addressed.

At environments where it is very difficult to reach, in electronic applications that have been deployed, like in underwater monitoring systems, there have been successfully tried several ways to power such applications by using the bacteria that live in the water. In [68], the MFC consists of two electrodes (one anode and one cathode), in which the anode is buried in the sea floor and the cathode is left suspended in the water. On the anode side there is a type of bacteria, the *Shewanella Oneidensis*, which breaks down the lactate in the water and makes it to release electrons and react with water. The basic structure of the setup, and the chemical reactions that occur, are schematically shown in Fig. 2.13, and the reaction just mentioned, appears at the bottom of it.

The electrons produced in the sea floor ($4e^-$), travel to the anode and then, to the cathode, through the load of the MFC. On the other hand, the protons produced by this reaction ($4H^+$), travel to the cathode side, through the water.

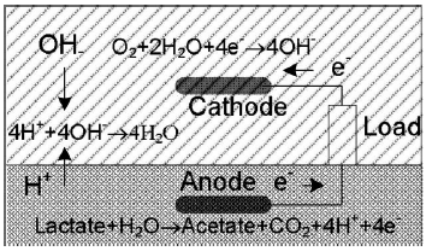


Fig. 2.13 - MFC structure and electrochemical reactions [68].

On the cathode side, the electrons from the anode react with water and with the oxygen in the water, to produce $4OH^-$, as seen by the chemical equation at the top of Fig. 2.13. Ultimately, the reaction of OH^- produced at the cathode, with H^+, coming from the anode, ends up forming water ($4H_2O$). Neither of the electrodes gets corroded, because the chemical reactions just described, do not include any other material than those that were mentioned. Moreover, the net product of the chemical reaction is not some polluting compound. One topic that must be carefully addressed is the surface area of the electrodes, because this factor has a key role in the power density that can be achieved.

Generally, the voltage and the current that can be generated are weak, requiring an adequate power management system to interface the MFC with the load, and having to encompass a storage device. Thus, the load can only work intermittently, in order to correctly meet the demand of power, and for short periods of time. However, an application like the one described, is self-contained, renewable, maintenance-free, and operational (on an intermittent basis), in a water environment.

Another environment, where there is an abundant quantity of bacteria, is in wastewater. This environment is very hostile to humans, so the use of a WSN that requires no human interventions after deployment is unarguably preferable. Another place, with similar problems, is the water tanks of nuclear plants. As such, under the subject of monitoring and control of wastewater treatment plants (WWTP), in [69] it is suggested a system that seeks to have an efficient use of electrical energy in these facilities, as the standards for processed water tend to be increasingly tightened. The architecture of the nodes of a WSN for this purpose, make use of field programmable analog arrays (FPAAs) and low-power networking protocols, and the powering of the nodes, is done by using MFC that harvest energy from the wastewater to which they were deployed. The harvested energy, as usual, is very scarce so, the use of FPAAs represents a very reduced power dissipation, when compared to their digital counterparts, the field programmable gate arrays (FPGAs), and the advantage of having a kind of parallel computing, since there is no central processor.

The electrical model of a MFC is shown in [70]. This model is represented in Fig. 2.14.

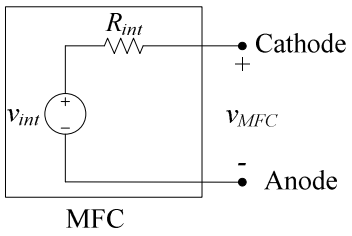


Fig. 2.14 - Electrical model for a MFC.

As it can be seen, the model is a Thévenin equivalent, similar to the model established for the thermal gradient energy source, shown in Fig. 2.6. The internal resistance of the MFC (R_{int}) is the sum of the system ohmic resistance, charge transfer resistance and activation resistance. The internal voltage and resistance can vary non-linearly, as the MFC condition changes. Possible causes for such changes, include instantaneous output power level, accumulated extracted energy, bacteria community and activity shifts and environmental condition changes. The thermodynamic limitations determine that v_{int} will have a maximum value of 0.8 V and a current output in the range of a few mA. In order to extract the maximum power out of the MFC, a load with the same value as R_{int} must be used, meaning that v_{MFC} will drop to half of the value of v_{int}. According to the intended application, this value may not be sufficient, and special measures must be adopted. With the MFC characterized in [70], the values obtained were $v_{int} \approx 0.65$ V and $R_{int} \approx 86\ \Omega$. Thus, when extracting the maximum power, the output voltage will be around 0.33 V.

The work performed in [71] suggests a new type of construction for MFCs, which is called single chamber microbial fuel cell (SCMFC). This type of MFC uses stainless steel attached to the anode and the cathode which showed to help in the constancy of the developed voltage over time. In addition, the pH of the solution inside the MFC became with a lower value (acid). This fact caused the stainless steel plates that were used to help in the process, to suffer some corrosion.

There is another system documented in literature [29], which is relatively recent, that uses a multi-harvest platform, and among the sources that are used, there is a MFC.

2.2.6 Light

Essentially, light is an electromagnetic wave, with the particularity of being visible. There is an interval of frequencies that comprises the visible light. In the lower end of this interval, light tends to be red, and as the frequency moves to higher values, light goes through the known colors, and in the upper end, it gets violet. Thus, light is bounded by infrared and ultraviolet. In Fig. 2.15, the entire electromagnetic spectrum is shown, with emphasis in the visible range.

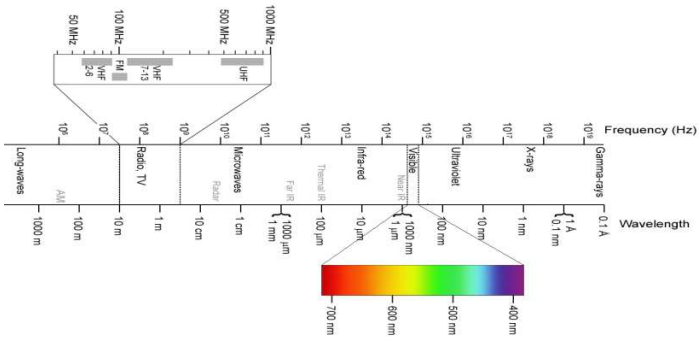


Fig. 2.15 - The electromagnetic spectrum [72].

In this spectrum interval, since the frequency values are already very high, it is more common to use the wavelength, instead of the frequency value, to identify the spectrum zone under consideration.

The spectrum outside the atmosphere, also known as the 5800 K blackbody, has the designation of AM0 (Air Mass 0), meaning “zero atmospheres”. This is the standard used to characterize PV cells to be used in space, for example, to power satellites.

The sunlight, after penetrating the atmosphere, at sea level, perpendicularly to the surface of the Earth, has a spectrum which is referred to as AM1, meaning “one atmosphere”. AM1 is useful for estimating the performance of PV cells in equatorial and tropical regions. The index “1” is related to the angle of solar incidence, which is minimal in this situation.

However, in Europe and in similar latitudes of the North and South hemispheres (where there is a great deal of population and industrial centers), the incidence of the Sun over the surface of the Earth has a different angle than in the Equator. This angle is about 42º from the horizontal line, so sunlight must cross a greater amount of atmosphere. As such, the spectrum is referred to as AM1.5, which means “one and a half atmospheres”, on a clear day. This value is the standard test situation for terrestrial PV panels. However, for higher latitudes, there are more Air Mass indexes, used for higher incidence angles, above 60º. These indexes can go until AM38, in the polar zones, where the incident angle is close to 90º.

In any of the above cases, atmospheric pollution, clouds or fog also have an influence on the amount of irradiated energy that can reach the surface of the Earth, due to the obstruction that they present.

According to AM1.5, after crossing the atmosphere, and at the maximum of its intensity, the light from the Sun can provide about 1 kW/m^2 across the whole wavelength spectrum. The irradiated light energy that the Sun produces is different according to each wavelength. To have an idea of this, the power spectral density of the solar radiation is shown in Fig. 2.16, where the top curve represents the solar spectrum just outside the atmosphere.

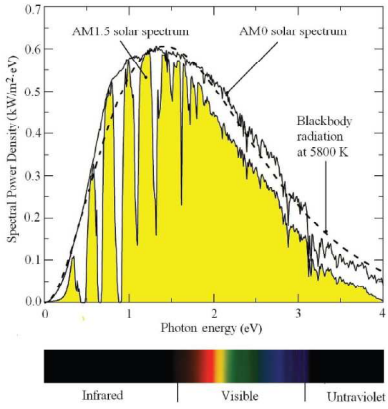


Fig. 2.16 - Power spectral density of solar radiation [73].

The total power density in this zone is 1.366 kW/m^2, which is known as the solar constant. The curve filled with yellow is the standardized solar spectrum on the surface of Earth, for performance evaluation of PV cells (AM1.5), and the standard power density under these conditions is about 1 kW/m^2, as it has already been referred. The dashed curve is the solar radiation spectrum at the position of Earth by modeling the Sun as a blackbody radiator at 5800 K. As shown, the solar spectrum just outside the atmosphere, the AM0 spectrum, matches well with the blackbody radiation spectrum at 5800 K, diluted by the distance from the Sun to Earth. The relation with human vision of color spectrum is shown in the bar beneath. As shown in Fig. 2.16, only about one half of the solar radiation power is in the visible range [73].

Next, in Fig. 2.17, it is shown the average annual amount of insulation hours for the European continent and some countries of the Middle East and the North of Africa.

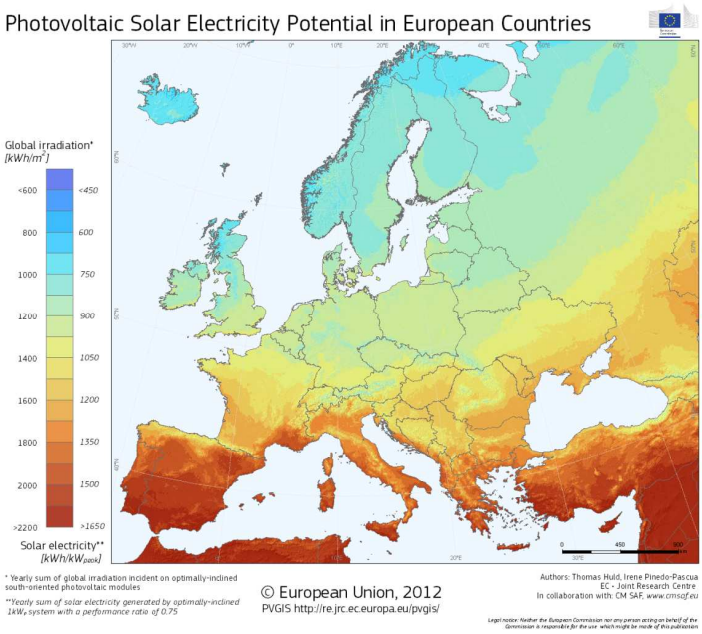


Fig. 2.17 - Photovoltaic solar electricity potential of Europe and some zones of the Middle East and the North of Africa (PVGIS © European Union, 2001-2012) [74], [75].

From this map, it can be seen that Portugal, Italy, Greece and Spain, have the highest potential for solar photovoltaic electricity generation in the European continent, as opposed to the countries of the north, in which the amount of solar radiation is undoubtedly smaller.

The solar energy is the primary source of energy to the planet, and it reaches it in an enormous amount. This is why light has the largest energy density, when compared to the other harvestable sources. According to [73], if one takes into account the total power of solar radiation reaching Earth, it will be about 1.73×10^{17} W, meaning that the total energy of solar radiation reaching Earth, each year, is 5.46×10^{24} J = 5460000 EJ. In the period of 2005 to 2010, the average energy demand in the planet, every year, was about 500 EJ, which means that, less than 0.01% of the total solar energy reaching the planet, would be enough to satisfy all the energetic needs of the world. However, not all solar radiation that irradiates the atmosphere reaches the ground, because about 30% of solar radiation is reflected into space. In addition, about 20% of solar radiation is absorbed by clouds and molecules in the air and also about 75% of the surface of Earth is water. Thus, even if only 10% of total solar radiation was utilizable, only 0.1% of it could power the entire world [73].

In indoor energy harvesting applications, the amount of light energy that is available is, however, much more reduced. The available light energy in indoors can vary significantly, since the light from the Sun is attenuated and can be mixed with artificial light. The literature reports available indoor irradiances ranging from one tenth of the maximum Sun intensity [37] to about 0.833 W/m^2 (100 lux converted to W/m^2 using [76]) in a lightly dimmed room [77], or 10 W/m^2, when the PV cells are placed very close to lamps [7].

The conversion principle indicated in [76], takes into account the nature of the wavelength spectrum in indoor environments. In this kind of environment, there is a predominance of artificial light, provided by light bulbs or light tubes. The latter have such a spectrum, leading to the application of the conversion factor to be

$$E_{rad}\,(\mathrm{W/m^2}) = \frac{E_{rad}\,(\mathrm{lux})}{120}. \tag{2.8}$$

Given the unit of light intensity, the lux (lx), according to some authors, there is a correspondence between the amount of power by unit of area and the amount of incident light, and it is defined under the relation that 1 kW/m^2 = 683 klx, i.e. 1 lx = 1/683 W/m^2, used in [78] and [79], for example. This conversion does not take into account the fact that the light has a specific indoors spectral pattern. According to [78], the level of indoor lighting is still enough to power electronic applications, namely from overhead fluorescent lights, with 34 W of power.

In [80], it is presented how the amount of available light energy is typically distributed along the day, which is depicted in Fig. 2.18, and accounts for the effects of fixed artificial irradiance and variable natural irradiance. It should be noted the difference of scales (10×), between the indoor (left) and the outdoor (right) illuminance values.

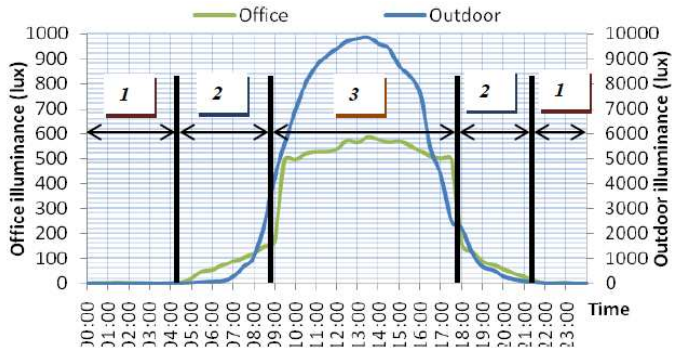


Fig. 2.18 - Office (indoor) and outdoor illuminance levels [80].

The previous graph shows that, in an indoor environment, the most optimistic value is about 5 W/m^2 (600 lux), achieved at about 13h30m. Most of this illuminance is provided by artificial lights. Any energy harvesting function can only be useful in the periods identified by 2 and 3.

In some situations it proves useful to have a history of the typical solar irradiation of the location where the harvester system is to be placed [81], [82]. In [83], a study is made and it is shown that using weather forecasts for predictions in both solar- and wind-powered sensor systems increases each system's ability to satisfy its demands compared with existing strategies. Depending where the system is to be located, the variability of the light source can depend over time. Only in indoor environments, one can consider that there is any constancy, but this condition is not always true.

The key element for light energy harvesting is the PV cell. This solid state device converts light energy directly to electrical energy without using any moving parts. A PV cell is basically a photodiode and it can be manufactured in CMOS technology [84], [85].

When the PV cell is illuminated, its output behaves like a current source in parallel with a diode, the latter acting as a voltage limiter. PV cells are characterized by three main parameters: the maximum power point (MPP), the open circuit voltage (V_{OC}) and the short circuit current (I_{SC}). The PV cell can be modeled by an equivalent electric circuit, shown in Fig. 2.19 a), characterized by the parameters of the equivalent circuit (I_1, R_P and R_S). The parameters of the diode device (D) also play an important role according to the amount of illumination that the PV cell is subjected to. In Fig. 2.19 b), it is shown a typical plot of the power and the current produced by a PV cell, letting know how these functions look like, as a function of the output

voltage v_{out}. The power function of the PV cell is obtained by multiplying the output voltage, v_{out}, by the output current, i_{out}. The MPP of the power function is achieved with an output voltage which is about 71% to 78% of the open circuit voltage of the PV cell [86], varying as the light or the temperature variates. The tracking of the true MPP is an active area of research, corresponding to the MPPT problem, which will be addressed in Chapter 4 - Section 4.6.

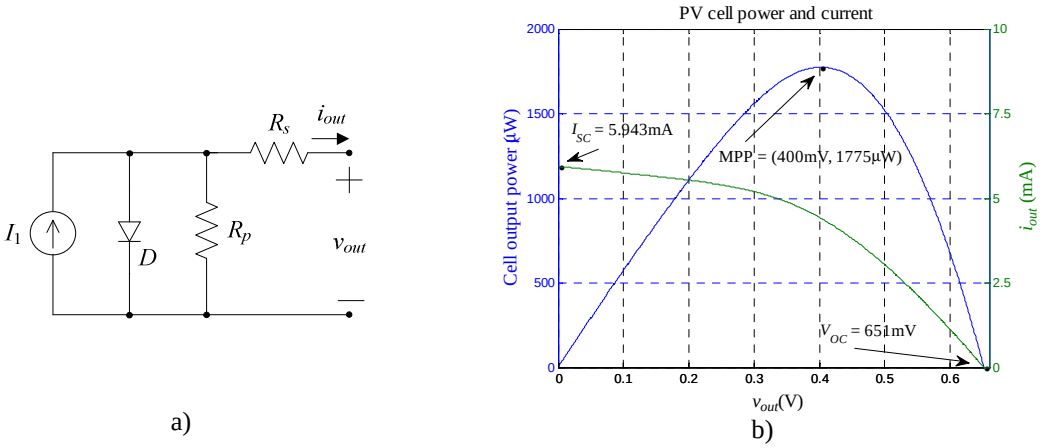


Fig. 2.19 - a) Equivalent electrical circuit of a PV cell, b) Example of typical current and power curves, as a function of the output voltage.

The output current of the PV cell (i_{out}) is related to the remaining elements of the model, according to the following equation:

$$i_{out} = I_1 - I_S\left(e^{q\frac{v_{out}+R_s i_{out}}{nkT}} - 1\right) - \frac{v_{out}+R_s i_{out}}{R_p}. \qquad (2.9)$$

In this equation, I_S is the limit of the current in the diode under high reverse bias. If the diode did not exhibit breakdown, the maximum reverse current that one could get through the diode, with an infinite reverse bias, would be I_S. Another definition for it, is that it is the "dark saturation current", i.e. the diode leakage current density in the absence of light. Also, q is the electron elementary charge ($1.60217657 \times 10^{-19}$ C) and k is the Boltzmann constant ($1.380648813 \times 10^{-23}$ J/K). T is the ambient temperature, expressed in K. The factor n is the emission (or ideality) coefficient, which equals 1 for an ideal diode.

Although it is possible to build a PV cell using CMOS technology, it is not simple to integrate PV cells with other circuits in the same die, in order to obtain a complete System-on-Chip (SoC) [11], [87]. The PV cell causes a positive voltage in the substrate, thus causing a possible latch-up condition in the die. Also, when a series connection of several devices is required, the fact that the diodes are built on the same substrate may be limiting [88]. This limitation has become evident in a PV cell that was manufactured and that appears reported in Chapter 3 - Section 3.5. To cope with these limitations, it is necessary to use more expensive

technologies, such as Silicon-on-Insulator (SOI), which allows for building an almost indefinite number of series connected PV cells, if one wants to obtain a higher voltage value [89].

The efficiency of the most common PV cells is still relatively low, at about 20% [37]. In indoor environments, amorphous silicon PV cells can have efficiencies up to about 7% [78]. However, there are some PV cells that can reach efficiencies as high as about 50%, as claimed in [90], although involving the use of new layout architectures and less common materials, resulting in more expensive systems.

In order to try reducing the production costs, it is possible to use PV cell technologies with lower efficiencies, but that also have lower manufacturing costs, resulting however in a larger area for the PV cell, for the same level of output power. Using amorphous silicon PV cells is an example of such a trade-off, in which costs are lower, but at the expense of a larger area to obtain the same level of power [91]. Next, in Fig. 2.20, the differences of the power densities measured on crystalline silicon (SOLEMS 09/030/012) and amorphous silicon (Schott ASI2Oi05/055) solar panels are illustrated, when different light sources are used to generate the same illuminance level [80].

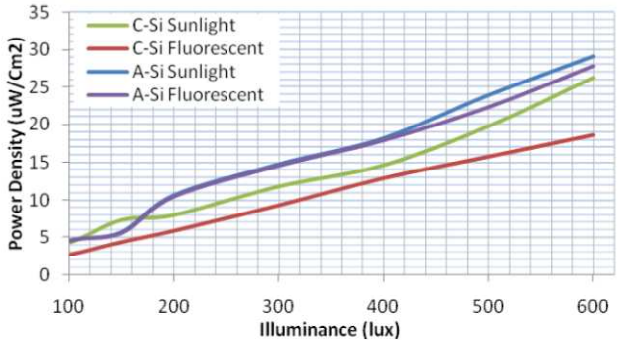


Fig. 2.20 - Power spectral densities of light sources at various illuminances [80].

The previous graph shows that in indoor environments, as opposed to crystalline silicon PV cells, amorphous silicon PV cells do not suffer a strong reduction in their power density, when the source of light changes from sunlight to fluorescent lights. Thus, this evidence is indicating that the amorphous silicon-based PV cells are more suitable for indoor applications.

Nonetheless, if the overall cost is one of the most meaningful factors, this option will also have to be taken into consideration to preserve commercial competitiveness.

There are some other devices that also deal with the harvesting of light energy. These devices are the photosynthetic electrochemical cells (PEC). This kind of cell can generate power both under light and dark conditions, and the principle of the operation of such a device is based on photosynthesis, similarly to plants. This principle is based on a bio-solar process, such that one has production of electrons with light (photosynthesis): $CO_2 + H_2O \rightarrow (CH_2O) + O_2 + e^-$

and with dark (respiration): $(CH_2O) + O_2 \rightarrow CO_2 + H_2O + e^-$ [92]. Photosynthesis and respiration processes are both involved with an electron transfer chain. Similarly to the construction of the electrochemical cell, the PEC is made up of an anode and a cathode, separated by a proton exchange membrane (PEM). The assembly structure of a PEC is shown in Fig. 2.21.

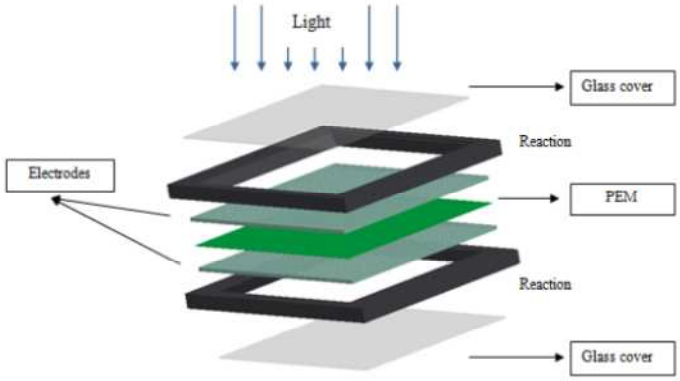


Fig. 2.21 - Schematic assembly of a PEC [92].

The photosynthetic micro-organisms form the anode portion and there is an electron acceptor on the cathode side. A gold electrode is fabricated for the device on top of a proton exchange membrane, which accepts only the positive ions and blocks the electrons. The free electron that is produced is trapped by the electrode. An electric circuit connected to the electrode forms a path and the electron is made to flow through, thereby producing electrical energy. Preparing an external circuit and integrating it with the photosynthetic process enables the flow of electrons in the desired direction, resulting in current.

PECs can be considered to belong to the category of the microbial fuel cells, which were described in Section 2.2.5.

2.3 Comparison of harvestable energy sources

It has been seen that there is a reasonable number of ambient sources that can be harvested. The source that will be harvested is dictated according to the intended application and the energy availability. However, as seen before, a system may even not limit itself to a single source, but for the sake of simplicity, a single source is preferable. Placing all sources side by side, the one that shows the highest power density by volume unity is the light energy, followed by mechanical and thermal energy respectively [5]. It is also important to point out that the operation of converting light energy to electrical energy (using a PV cell) is one of the easiest and cheapest energy conversion operations. Therefore, in most cases, powering the sensor using light energy is always the best option. The only exception is when the sensor is located in a

human (or animal) body. In this case, it would be convenient to use thermal or mechanical energy, for example.

TABLE 2.1, presents some demonstrated capabilities of energy sources and their respective energy densities. This table is adapted from [1], to which some more information has been added, about contexts where the energy can be harvested. The data presented in this table serves to have an idea of how much energy is to expect from a given source and also to have a comparison among the various sources.

TABLE 2.1 - Demonstrated capability of some energy sources, regarding their density and performance, and examples of scenarios where to scavenge such energy sources.

Energy source	Energy density / performance	Short examples of scavenged environments
Ambient radio frequency	< 1 $\mu W/cm^2$	Anywhere, mainly in urban areas
Ambient light	100 mW/cm^2 (directed towards bright sun) 100 $\mu W/cm^2$ (illuminated office)	Anywhere, where natural or artificial light is available
Thermoelectric	60 $\mu W/cm^2$	Furnaces, exhaut pipes, combustion engines, human warmth
Vibrational micro-generators	4 $\mu W/cm^3$ (human motion - Hz) 800 $\mu W/cm^3$ (machines - kHz)	Machines with rotating engines, human movements
Ambient airflow	1 mW/cm^2	Anywhere, where air shows a consistent and abundant flow
Push bottons	50 $\mu J/N$	Human action over buttons of commands
Hand generators	30 W/kg	Human action over specific mechanical generators
Heel strike	7 W potentially available (1 cm deflection at 70 kg per 1 Hz walk)	Using shoe insertion, by human walking motion

2.4 Energy harvesting based sensor networks

2.4.1 Introduction

Wireless sensor networks, whose nodes make use of harvested energy, have interested researchers not only in the adaptation of the nodes to the environments in which those networks can be deployed in, but also in the development of methods and optimization of parameters to extend the operation of the nodes.

Perhaps, the most critical factor concerning these networks is the energy availability, because if that cannot be guaranteed, the whole network can be compromised. However, there are also some other parameters that must be taken into account, in addition to the energy availability. These parameters are the operational lifetime of the node, the sensing reliability, the transmission coverage that the node can provide, and also the cost of the investment, which should be as much affordable as possible.

Typically, the harvesting module inside each node in a sensor network provides some sort of energy storage in order to hold enough energy to power the node during any period in which there is not available energy to be harvested. This kind of storage is normally done by using a device such as a battery or a supercapacitor. The storage device is charged when there is energy being harvested, and discharged, by making use of the stored energy to power the node, in case of need. If the node is provided with processing capabilities, such that it can predict when will begin its next charge cycle, it can execute the convenient or allowable set of operations that optimize the working time, extending it as much as possible, so as to have an effective utility, while consumming energy as moderately as possible. This rationalization can be done by reducing the sampling rate, the transmitted power or the duty-cycle of operations [93].

2.4.2 Energy neutrality

With regard to the management of the energy that is harvested by a node, if this energy is more than the energy being consumed, over a period of time that can be supported by the energy buffers, then the node can operate with a continuous lifetime. This kind of situation is known in literature as the Energy Neutral Operation (ENO) [94]. However, the excess of energy is wasted, instead of being used for increasing the performance of the system. Thus, it can be considered that the node is not operating in a fully efficient fashion. The desired operating regime is when the harvested energy is approximately the same as the consumed energy, while all the harvested energy is put at the service of the performance of the system. Operating in such a way is named in literature as ENO-Max [95]. This type of operation constitutes one of the most important goals of WSNs being powered by energy harvested from the environment, because the system will be conveniently sized to strictly meet the requirements of operation, avoiding waste of resources and increase of costs, due to an eventual system over-sizing.

2.4.3 Examples of WSN powered by harvested energy

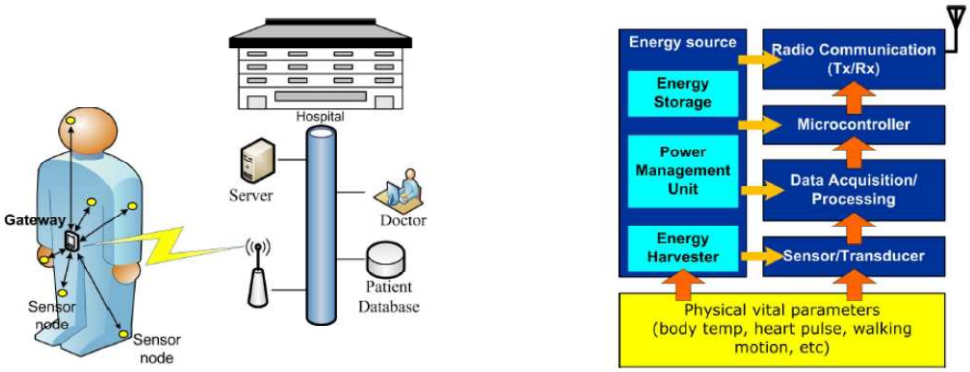
The deployment of WSN can be done to a variety of scenarios. As it could already been seen, almost ever, the use of a given type of energy source is determined according to the type of environment in which the network resides. Next, some examples will be given of such networks.

2.4.3.1 Health condition monitoring

The work reported in [60] concerns about a WBAN in which a number of nodes take place. This network has the purpose of monitoring various vital signs and to collect healthcare data for medical diagnosis purposes, by using different types of physiological sensors onboard of the

sensor nodes. These include devices like the electrocardiogram (ECG) sensor, electromyography (EMG) sensor, electroencephalography (EEG) sensor, blood pressure sensor, tilt sensor, breathing sensor, movement sensor, thermometer, etc. The objective is to gather patient information in a database, in order to have enough data to make a good diagnosis when that becomes urgent by medical staff. There is an additional feature to the nodes, which is the detection of the fall of the patient, by using an accelerometer.

In Fig. 2.22 a) it is shown the schematic structure of this network, as well as how it interfaces with the rest of the healthcare infrastructure. The structure of each node is shown in Fig. 2.22 b).



a) b)

Fig. 2.22 - a) Wireless body area network architecture in medical healthcare system [60], b) Overall structure of a typical wireless sensor node of this WBAN [60].

The nodes in this WBAN are supplied by thermal energy, harvested from the body warmth of the patient. An interesting feature about this network is the fact that the nodes can rotate their role about the gateway function. Instead of being just one of the nodes dedicated to that purpose, each node was given the capability to be a gateway. As this is a very power consuming function, and since transmission is not performed during all the time, different nodes, at each time, serve as a radio interface between the WBAN and the backbone of the healthcare network.

2.4.3.2 Forest surveillance and monitoring

Another scenario in which a WSN proves useful is in forest monitoring, for prevention of forest fires. Under this purpose [96] presents a network whose nodes have their computational capability based on a microcontroller. Each node is equipped with a smoke sensor and an infrared flame detector. Ideally, such a network is intended to replace the traditional forest surveillance, such as ground patrolling, watchtower detecting, aerial patrolling and space satellite detection. Any of these methods is expensive and involves a great deal of human intervention. The deployment of such a network occurs with each node randomly put to the

field, and self organizing together with the other nodes, in order to form a distributed network by protocol. Then, the gathered data can start to flow among nodes, by using the wireless communication interface, and finally it can be transmitted to the monitoring center. Then, the data can be processed and analyzed by the monitoring host computer, to provide visual information for forestry experts or for whichever decisions that should be taken or alarms that should be activated. Each node is put to work by using a low duty-cycle and uses solar energy harvested by a PV cell in order to charge a rechargeable battery.

2.4.3.3 Energy and environment monitoring in buildings

Another area under strong interest from researchers and the general public is domotics and intelligent buildings, namely, Building Energy and Environment Monitoring (BEEM). This kind of monitoring has the objective to use energy more rationally, allowing for an overall reduction of energy consumption and carbon emission, while reducing the present costs associated to this kind of monitoring. Several works have been published in this field, among which, [12] is an example. In this work, a WSN with sixty two nodes is deployed to an office building. Each node contains a microcontroller, for computational purposes, and carries multiple sensors, making it capable of measuring energy consumption, light level, temperature and humidity parameters. Also, each node is able to transmit data using a 2.4 GHz *Zigbee* (IEEE 802.15.4) interface.

In this work, it is claimed to have designed the world's first known indoor light energy harvesting powered BEEM system. The nodes are powered by light energy, harvested in an indoor office environment, using a PV panel with 85 mm × 50 mm. The harvested energy is stored in a supercapacitor, so that the node can continue to operate during the periods when no light is available. This application has succeeded in monitoring the desired parameters continuously for an entire month, requiring no user intervention.

2.4.3.4 WSNs in automotive applications

In an automobile vehicle, the need to keep the quiescent current of the battery as low as possible, in order to extend its durability, has led to the development of applications that use harvested energy as the power source. As such, in [97], an intrusion detection system is powered by harvested energy. This system consists of a wireless network of sensors, whose function is to detect the breaking of glasses caused by burglar assault.

In this application, special care has been taken, regarding the communication among the nodes, which include built-in safety features like plausibility checks, encryption and radio channel monitoring, with special focus being laid on the medium access control (MAC) layer protocol design.

The development of automotive applications has an inherent set of demands that must be addressed. For example, the electronic circuits must be prepared to withstand extreme temperature conditions, as well as humidity. In addition, as the automobile market is global, the regulations about wireless networks and alarm systems must always take the international regulations into account. Another requirement specified by the automotive industry is that with full functionality, a period of more than six weeks can be bridged without recharging the storage device of the sensor node, which can be a rechargeable battery or a supercapacitor. Also, the system has to be connected to the controller area network (CAN) bus of the vehicle.

With the vehicle regularly in use, there are various energy sources that can be harvested: light is accessible through the ceiling and glasses; heat can be harnessed from the exhaut system; or vibrations from the engine or the moving structure, are also available. However, when the car is parked for a long period of time in a dark garage, none of these sources is available. As a consequence, the WSN that implements the intrusion detection system could be disabled. To counter for this eventuality, the nodes are kept sleeping for most of the time and, when in activity, the MAC protocol that is used is very energy efficient.

The limited spatial environment in which the network resides, avoids the need for a routing algorithm, as well as it allows for a small payload to be transported in the messages, keeping the protocol as short as possible. In [97], the network is composed by seven nodes plus a base station, in which the latter is connected to the CAN bus, so that the messages can be processed by an electronic module in the car. Morever, it must be taken into account that, if the car is parked in a parking lot, there is the possibility to exist crosstalk due to networks installed in nearby cars. The protocol that is used accepts longer transmission times, due to a very long preamble. It is possible to let the receivers to stay idle or sleeping for most of the time. A receiver wakes up periodically for just a small interval, to listen to the channel. If the channel is idle, the receiver returns to an energy saving mode.

The sensor nodes are powered by a mechanical energy harvester and, since the glass break sensor in purely passive, it most be polled by a microcontroller, which sleeps in between samples. Only in case of glass break detection, the sensor node immediately tries to contact the base station to report the glass breakage with multiple alarm messages, until the sensor node receives an acknowledgement message from the base station, or the energy storage device is empty. This activity profile allows the WSN to hold for about six weeks without recharging the storage device, while keeping all safety features required by the automotive industry.

2.4.3.5 Structural health monitoring (SHM)

Structural health monitoring (SHM) is useful in many contexts. This is the process of detecting damage in aerospace, civil and mechanical infrastructures [98]. The sensors can be deployed to any structure that needs monitoring, like vehicles, buildings, bridges, monuments, etc.

The detection method can consist of an operation of statistical pattern recognition, requiring four sequential steps: operational evaluation, data acquisition, feature extraction, and statistical modeling for feature classification. The goal of any SHM sensor network is to make the sensor reading as directly correlated with, and as sensitive to, damage as possible, so that the network can adequately observe changes in the system dynamics caused by damage and manage these data for suitable signal processing, feature extraction and classification. Thus, it is very important to make the sensors as independent as possible from all other sources of environmental and operational variability, and independent from each other, while providing maximal data with the minimum number of sensors. Towards these requirements, there are a number of specifications that must be previously established, such as: types of data to be acquired; sensor types, number and locations; bandwidth, sensitivity and dynamic range; data acquisition/telemetry/storage system; power requirements; sampling intervals; processor/memory requirements; and excitation source needs (for active sensing).

Regarding how the hardware is chosen, five issues must be addressed: 1- the length scales on which damage is to be detected, 2 - the time scale on which damage evolves, 3 - the effect of varying and/or adverse operational and environmental conditions on the sensing system, 4 - power availability, and 5 - cost.

The most common measurements made for SHM purposes are acceleration and strain. Acceleration is the most used measurement in SHM, because of the maturity of the technology associated to accelerometers, as well as of the hardware that performs the signal conditioning. However, these devices are mostly used in wired networks, where the voltage of the sensor is transferred to a data acquisition central unit, where it is processed. This kind of procedure is very power consuming, especially because of the number of sensors that may be involved, so accelerometers in MEMS technology can start to be used more often, so as to counter this problem. After acceleration, strain is the most measured physical parameter in SHM. The technology of strain gauges in also mature and the signal is typically measured using a brigde circuit and, also including the signal conditioning, they consume power at a very commensurate level. The most common strain gauge technology is the electric resistive foil gauge, but there has been an increase in the use of fiber optic solutions to strain measurement, although the power requirements are higher than with strain gauges. The two dominant fiber optic

technologies are direct fiber interferometry and fiber Bragg gratings (FBGs). Most commercial systems today take advantage of FBG technology.

Today, two sensor network paradigms exist for SHM, which are having the sensor arrays directly connected to the central processing hardware and the wireless decentralized sensing and processing. Each has advantages and disadvantages. The first has the advantage of being widely commercially available, both in devices and in complete systems. However, it has the disadvantage of being wired, and requiring AC connections due to the power comsumption that it represents. The typical structure associated to this paradigm is represented in Fig. 2.23.

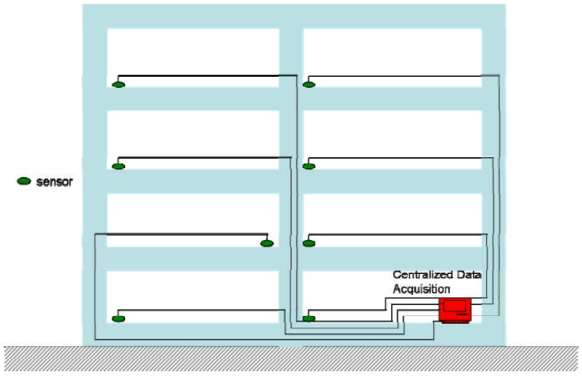


Fig. 2.23 - Conventional wired SHM system with a central monitoring station [98].

The wireless decentralized sensing and processing has been under the strong interest of researchers, regarding many aspects already referred in this text, such as power dissipation and communications, overcoming many limitations of the wired networks. Ad-hoc networking and hopping is usually adopted, with some problems concerning it, like the fact the the nodes closer to the base station are more subjected to data collisions and, as most of the total traffic passes through them, their power source drains out more rapidly. Researchers are also studying the advantages of having mixed wired and wireless networks, in order to explore the advantages of both. The structure of a wireless sensing network is shown in Fig. 2.24.

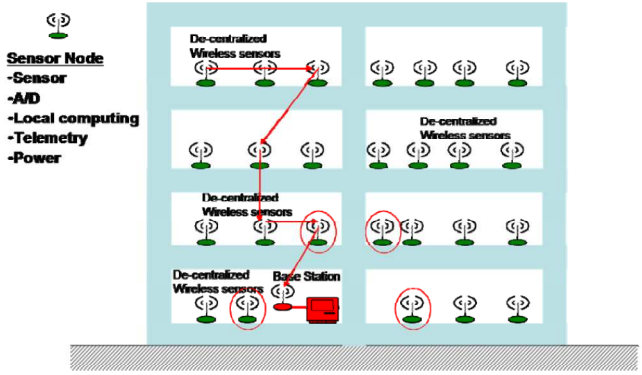


Fig. 2.24 - Decentralized wireless SHM system employing hopping communications protocol [98].

As with every vehicle, aircrafts are prone to have WSN to monitor parameters related to the SHM of body parts made of carbon or glass fiber reinforced plastic [41]. The use of wireless nodes is helpful, because it avoids wiring, thus reducing costs, installation complexity and weight. The latter is critical, regarding the fuel consumption.

2.4.3.6 Wireless networks for localization or study of animals

The subject of animal localization, animal behavior, cattle monitoring, or the improvement of livestock related techniques, have been active research areas for years. In [99], a WSN mostly kinetically powered, has been used for the localization of herds in grazing areas. This network has primary and secondary nodes. Primary nodes are battery powered and serve to collect information transmitted by the secondary nodes, as well as position and time data, to a base station that monitors all the animals. The secondary nodes are attached to the animals and are powered by a mechanical transducer, which generates electrical energy from the motion of the animals. These nodes have the function to broadcast their identification.

The main objective of the work in [99] is to remotely track the movement of animals in herds, such that a herder may know where the herd is, if any animal has left, or where it was lately around. This work was tested with semi-domesticated scandinavian reindeer. Instead of using methods like global positioning system (GPS) tracking, which are expensive and power consuming, in each animal, it is used a kinetic harvester module, which powers a transmitter that can reach up a hundred meters. The nodes are bateryless and require almost no human intervention. Only the primary nodes, which are powered by a battery, get their position by GPS. The secondary nodes use a rectifier, as usual with mechanical energy sources, and a supercapacitor to store the harvested energy. A 20 cm magnet/coil generator has been used as the kinetic-to-electric energy converter. The whole circuit powers a radio transmitter. The node is attached to the animal, by using a collar, as depicted in Fig. 2.25.

Fig. 2.25 - Reindeer wearing a collar containg the sensor node [99].

The nodes mounted on the animals were able to transmit and be detected more than three times per hour, in average, without the need of any battery, proving that the concept is feasible.

There are other situations, in which the study of wildlife has led to the deployment of electronic applications powered by harvested energy. As an example, two of them will be mentioned here, although these have been referred in [93] and [99].

The first one is the *ZebraNet*, which is a network of GPS sensors to track zebra movement and long term animal migration patterns, habitats and group sizes. The nodes in this network are also attached to the neck of the animals with a collar and are powered by solar energy, which is very abundant in the habitat of these animals. The collar has 14 solar modules, a comparator and a boost converter that charges a Li-ion rechargeable battery, so that the node can be powered during night time and bad weather. The battery allows for 72 hours of operation, when completely charged. The peak output power is 400 mW. The node is also composed of a microcontroller which controls the operations of the system, as well as the charging of the battery.

The second one is the *TurtleNet*, whose function is to track turtles. Similarly to the *ZebraNet*, the nodes in this network are also powered by a PV cell that outputs 90 mW at 4.2 V. Moreover, these nodes must be waterproof, because turtles spend much of their time under water. Next, in Fig. 2.26, it is shown the mounting of each of these nodes onto the animals.

a) b)

Fig. 2.26 - Mounting of the sensor nodes in a) *ZebraNet* [93] and b) *TurtleNet* [93].

In [93], there is more information about each of these networks, as well as the indication to the original references that explain all the details.

2.5 Conclusions

In this chapter, an overview about energy harvesting systems was made. By performing a search in some of the available literature, information was collected about the ambient sources that can be harvested, and systems that make use of those sources to power themselves.

According to the type of source that is being harvested, a convenient harvester device must be used and it is an important tool to have a model able to electrically describe how the harvester works. This functionality is particularly important in the design phase, in order to model and simulate the whole system, also encompassing the harvester.

Moreover, for a particular kind of source, there are already certain types of circuits that are strictly required to be used, like the case of rectifiers in RF and in mechanical energy harvesting, for example.

If the deployed systems are able to operate in a self-powered fashion, this brings out a lot of benefits, cost wise. This operation, installation and maintenance philosophy greatly reduces the amount of money needed to keep the system at work. For instance, when looking at installation costs, not needing to connect to the power grid means that wiring and additional equipment is not needed. As a consequence, there is no need for manpower to take care of an elaborated system installation. When looking at the maintenance costs, as the infrastructure is wireless, anything related to cables or similar, and related equipment, does not apply. An expression that can serve to illustrate the intended operation paradigm is "*deploy and forget*" [100]. For systems powered by light, one maintenance factor that should be taken into account is concerned to the hypothetical periodical cleaning of the PV cell, as dust can accumulate over time and deteriorate the harvesting characteristic.

Since the amount of available energy, which can be harvested, is typically very low, and the resulting voltages are also low, these systems must use a voltage elevator, in order to provide a suitable voltage to power an electronic application. In addition to this requirement, there is also the need to provide some means to store the harvested energy so that the load system can be supplied even when there is a shortage of energy from the chosen harvested source. These topics will be addressed in Chapter 4.

The overview that was given in this chapter had the purpose of introducing to the energy harvesting theme. This was done by showing, with some examples of published material, what are the available energy sources, the main parameters and computational infrastructures that must be accounted for, some systems that already exist, and the challenges that one must face when designing a system for such a class of applications. As such, the reader is invited to deepen the search that has been made and presented here, in order to match his search with the real demands to be met, as the material presented in this chapter is only introductory.

Chapter 3

PHOTOVOLTAIC CELL TECHNOLOGIES

3.1 Introduction

The motivation behind the origin of PV cells was to supply remote regions, with electrical energy, where the grid was not available. In 1953, when Darryl Chapin began this work, a method using a photovoltaic effect in Selenium (Se) was already known, in order to produce electrical energy from light [73]. However, the efficiency was very poor (about 0.5 %), making this method impractical. Then, two cientists that had been involved with the early development of the silicon transistor (Gerald Pearson and Calvin Fuller), joined Chapin and, in 1954, developed the first Silicon (Si) technology PV cell, with an efficiency of 5.7 %. This value was found to be satisfactory enough to putting the developed cells to use.

These new cells were made from a p-n junction. The n-side of the junction is very thin and highly doped, allowing light to come to the p-n junction with very little attenuation, but the lateral electric conduction is high enough to collect the current to the front contact through an array of silver fingers. The back side of the silicon is covered with a metal film, typically aluminum. The basic structure of the silicon PV cell has remained almost unchanged until now. The price associated to these newly developed devices was very high, so these were only used for space applications and satellite powering, until about the middle of the decade of 1970.

Then, industry of PV cells was really established, and research increased tremendously. Since then, the price has decreased and the installed power of PV energy has dramatically increased.

PV cells can be associated in series and in parallel, in order to obtain a higher output voltage and output current, respectively, besides obtaining a higher output power. The current-voltage characteristics of the series and parallel association of PV cells is shown next, in Fig. 3.1.

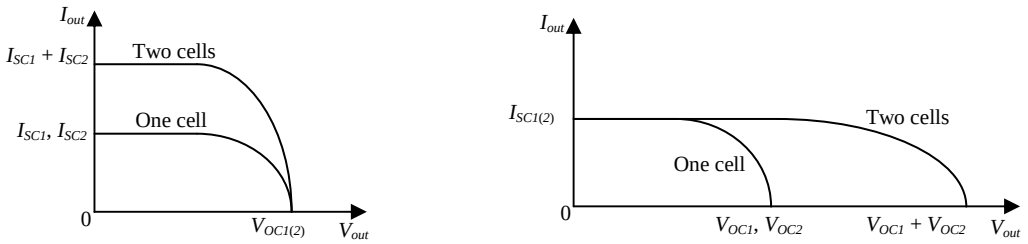


Fig. 3.1 - Connection of two identical PV cells: a) parallel; b) series.

The current-voltage characteristic of a PV cell can vary with the incident light intensity and the temperature. This variance is illustrated next, in Fig. 3.2.

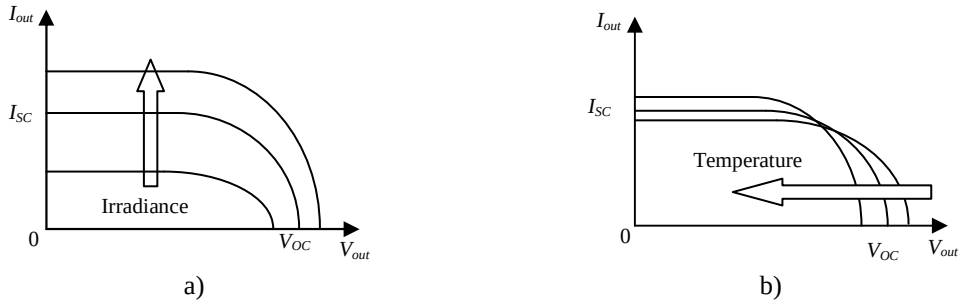


Fig. 3.2 - Influence of irradiance and temperature on the PV cell current: a) increasing irradiance; b) increasing temperature.

3.2 Concepts and parameters regarding PV cells

There are a number of terms that are usual in the context of PV cells. These are briefly explained next.

3.2.1 Standard illumination conditions

The standard conditions that are considered when referring to the efficiency and power output from a PV cell are AM1.5, already defined in Section 2.2.6. Summarizing, these are: irradiance of 1 kW/m^2, 25ºC of ambient temperature and a spectrum of sunlight crossing the atmosphere with an angle of 42º above the horizon.

3.2.2 Fill factor

The current that a PV cell can provide varies between 0 and the short circuit current (I_{SC}). In terms of output voltage of the cell, the extreme values correspond to the open circuit voltage (V_{OC}) and 0, respectively to the current. Graphically, these are related between them according to Fig. 3.3, where these can be found, since a typical current function is shown. In Fig. 2.19 b), such a function had already been shown (see Section 2.2.6).

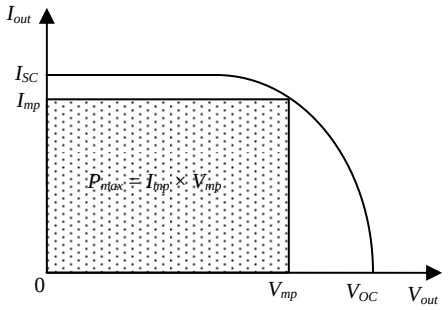


Fig. 3.3 - Maximum power and fill factor.

In general, any rectangle drawn under the current function represents the power that the cell can deliver to a circuit connected at its terminals. In Fig. 3.3, the darkened rectangle represents the maximum power P_{max} that the PV cell can provide, because its area is the biggest that can be achieved. The voltage V_{mp} and current I_{mp}, that allow for this power value, define the MPP of the cell, and are always less than V_{OC} and I_{SC}, respectively.

Thus, the fill factor (*FF*) of a PV cell is defined as the ratio between the maximum power of the PV cell and the product of V_{OC} by I_{SC}, resulting in

$$FF = \frac{P_{max}}{V_{OC}\, I_{SC}} = \frac{V_{mp}\, I_{mp}}{V_{OC}\, I_{SC}}. \tag{3.1}$$

The value of *FF* is, typically, around 0.8 to 0.9.

According to a detailed explanation in [73], the fill factor of semiconductor PV cells, whose electrical model is depicted in Fig. 2.19 a) (see Section 2.2.6), is given by the next equation, where I_S is the saturation current of the diode.

$$FF = \frac{P_{max}}{V_{OC}\, I_{SC}} = 1 - \frac{1 + \ln\ln(I_{SC}/I_S)}{\ln(I_{SC}/I_S)}. \tag{3.2}$$

3.2.3 Efficiency

The efficiency of a PV cell is defined as the ratio of the output electric power versus the input solar radiation power under standard illumination conditions at the maximum power point.

TABLE 3.1, shows the efficiencies of some types of PV cells, which will be addressed later on. The outdoor conditions are those that best meet the standard test conditions indicated in Section 3.2.1.

TABLE 3.1 - Typical environment illuminance level and commercial available solar panel energy conversion efficiencies [80].

		Indoor light	Outdoor light
Illuminance level (lux)		100 - 1000	1000 - 65000
Solar panel energy conversion efficiencies	c-Si	3% - 8%	≈18%
	a-Si	2% - 5%	8% - 13%
	GaAs	2% - 8%	7% - 15%

3.2.4 Peak watt

The "peak watt" (W_p) rating of a solar module is the power (in Watts) produced by the solar module under standard illumination conditions at the MPP. The actual power output of a PV cell, obviously, depends on the actual illumination conditions.

3.3 Generation of electric power in semiconductor PV cells

The basic concept of power generation in semiconductor PV cells is related to the construction of the p-n junction. The base, or substrate, is a piece of p-type silicon, lightly doped with boron, a fraction of a millimeter thick. A highly doped n-type silicon, with a thickness of a fraction of one micrometer is generated by doping with phosphorus of much higher concentration, and laid over the substrate. Because of the built-in potential of the p-n junction, electrons migrate to the n-type region, and generate electric power similar to an electrochemical battery.

When a p-n junction, such like the one described, is irradiated with light, several possibilities may occur. These are indicated in Fig. 3.4.

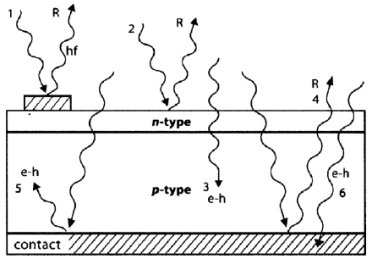


Fig. 3.4 - Behavior of light inciding over a PV cell [101].

The possibilities considered here are: 1 - reflection and absorption at top contact, 2 - reflection at cell surface, 3 - desired absorption, 4 - reflection from rear out of cell, 5 - absorption after reflection, 6 - absorption in rear contact. The desired goal is to have the maximum power at the minimum cost. Thus, to ensure the highest efficiency, cells must be designed to enhance the desired absorption (3) and absorption after reflection (5).

The absorption coefficient indicates how a semiconductor material behaves in absorbing the incoming photons. In Fig. 3.5, the plots of this coefficient are shown, according to the type of semiconductor material being used, as well as to the energy of the photon that hits the cell.

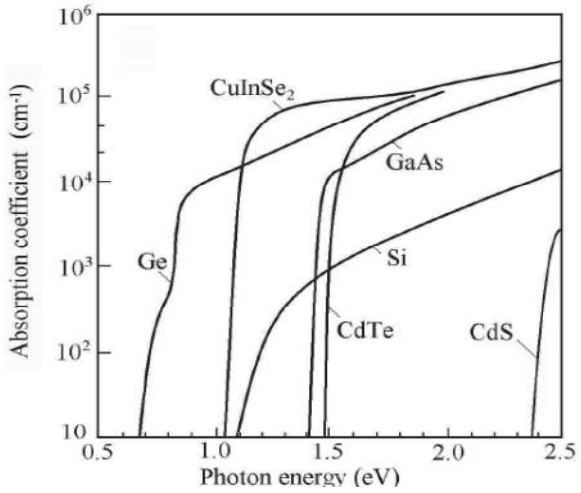


Fig. 3.5 - Absorption coefficient for different semiconductor materials [73].

It can be noted that silicon is not one of the best absorbing materials, as compared to others present in the same graph. This means that, when using silicon, in order to absorb a useful amount of photons, more material must be used, resulting in a thicker layer. Typical values are in the range of 100 μm. On the other hand, materials like GaAs, CdTe or $CuInSe_2$, only require a layer with a few micrometers. The types of PV cells that use any of the materials that were just mentioned will be addressed in Section 3.4.

In order to reduce the loss due to reflection, there are anti-reflection coatings that can be applied at the interface between semiconductor and air [73].

When the desired absorption occurs, a photon, with an amount of energy greater than the energy gap of the semiconductor material, can be absorbed and create an electron-hole pair. Inversely, an electron-hole pair can recombine and emit a photon of energy roughly equal to the energy gap of the semiconductor. This process is schematically described in Fig. 3.6.

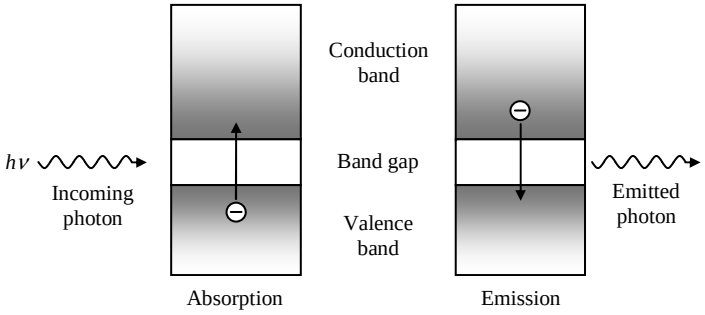


Fig. 3.6 - Interaction of radiation with semiconductors, regarding energy bands.

By observing the left hand side of Fig. 3.7, a photon with energy $h\nu$ generates an electron-hole pair in the p-type region. Because of the built-in electric field (E_x), which points towards the p-type region, the electrons, which are negatively charged, are dragged by this field into the n-type region. V_0 is the built-in potential voltage and q, the charge of the electron.

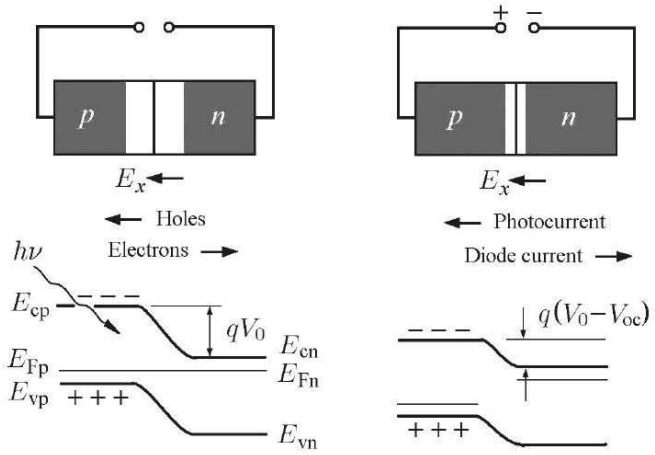


Fig. 3.7 - Separation of holes and electrons in a PV cell [73].

When the two terminals are tied together, an electrical current is established. This is the short-circuit current (I_{SC}) and is determined by the rate of electron-hole pair generation from the radiation. By looking at the right hand side of Fig. 3.7, if the terminals are not connected to each other, the electrons that migrated to the n-type region are accumulated and a voltage across the junction capacitance builds up. The direction of this voltage is the same as the forward bias voltage of the diode, which generates a current to compensate the electron current. At equilibrium, an open-circuit voltage (V_{OC}) is established. This effect is similar to direct biasing the PN junction.

The frequency of the photon is designated as ν. The correspondence between the wavelength λ and the frequency ν is given by

$$\lambda = \frac{c}{\nu}. \tag{3.3}$$

In (3.3), c represents the speed of light in vacuum, which is 299792458 m/s.

The energy of a single photon is given by

$$E_p = h\nu = h\frac{c}{\lambda}. \tag{3.4}$$

The symbol h is the Planck constant, whose value is $6.62606957 \times 10^{-34}$ J·s, or 4.1356674335 eV·s. The latter is more adequate in the present context.

The remaining symbols shown in Fig. 3.7, have the following definition:

TABLE 3.2 - Definition of the symbols present in Fig. 3.7, representing the energy levels.

E_{cp}	Energy level at the bottom of the conduction band in the p-type semiconductor
E_{Fp}	Energy Fermi level in the p-type semiconductor
E_{vp}	Energy level at the top of the valence band in the p-type semiconductor
E_{cn}	Energy level at the bottom of the conduction band in the n-type semiconductor
E_{Fn}	Energy Fermi level in the n-type semiconductor
E_{vn}	Energy level at the top of the valence band in the n-type semiconductor

The Fermi level is equal in both the n-type and the p-type sides, when the junction is short-circuited. However, when the junction is biased or in open circuit while being irradiated, this energy level is different from the n-type to the p-type sides, also as it can be observed in Fig. 3.7.

3.3.1 Efficiency limit according to Shockley and Queisser

There is a theoretical limit to the efficiency, which depends on the type of material being used in the cell. In 1961, William Shockley and Hans Queisser made an extensive analysis of the p-n junction PV cell, and established an upper limit for the efficiency of single-junction PV cells. This is known as the “Shockley - Queisser limit”. In-depth detail on how this limit is derived can be found in [73].

Next, Fig. 3.8 shows how the efficiency is bounded, according to the band gap of the semiconductor material. Some materials are also indicated, in order to have an idea of how much is the energy band gap for each of them.

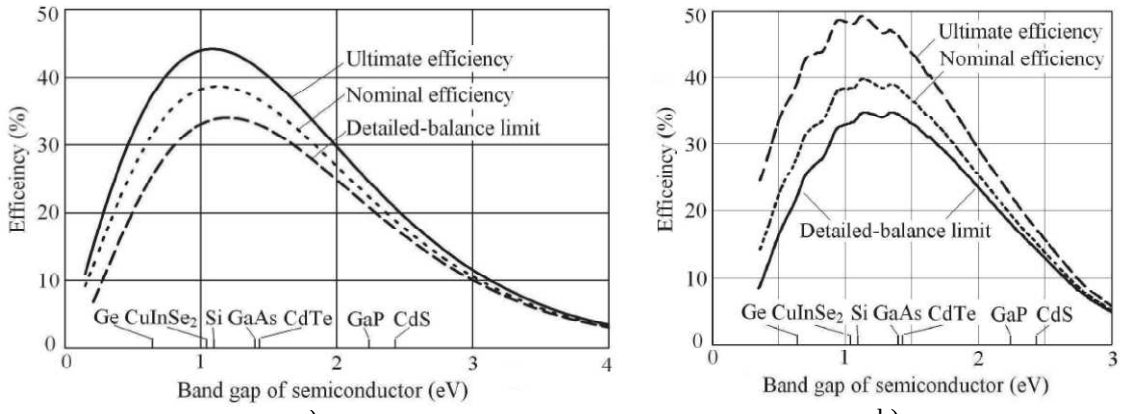


Fig. 3.8 - Efficiency limits of PV cells [73], considering: a) AM0 and b) AM1.5.

Once again, the details about the terms used for each efficiency plot are outside of the scope of this text and should be explored in the references mentioned. The graphs show the functions considering, in part a), a blackbody radiation at 5800 K and, in part b), the radiation used for STC, i.e. AM1.5. As it can be seen, in both situations, silicon (Si) is the material that can achieve the highest efficiency.

3.4 Types of PV cells

The technology of PV cells can be divided into three “generations”. The first generation consists on the use of silicon crystalline structures. This can include the monocrystalline, polycrystalline and emitter wrap through (EWT). This technology has been progressively developed over time, in order to improve its capability and efficiency. Thus, in spite of being the first generation technology, it is not obsolete. The second generation technologies are based on single junction devices, aiming to optimize material usage while trying to keep the efficiencies achieved earlier. This generation comprises materials such as CdTe (Cadmium Telluride), CIGS (Indium incorporated with Gallium - increased band gap) and a-Si (amorphous Silicon). Finally, the third generation encompasses double, triple junction and nanotechnology, which are all showing promising results and efficient cells at a lower cost [73]. As an illustrative summary, representing efficiency versus cost, Fig. 3.9 shows where each one of the three technologies fits.

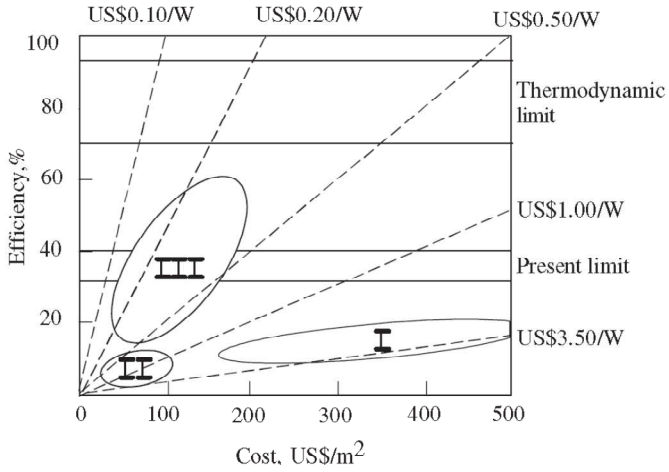


Fig. 3.9 - Efficiency/cost trade-off for the three generations of PV cell technologies (cost in US dollars, in 2003) [102].

3.4.1 First generation PV cells

The crystalline silicon (c-Si) PV cell was the first practical PV cell, invented in 1954. The efficiency of such mass produced PV cells is 14–20%, which is still the highest in single-junction PV cells. It also has a long life and is adequate for mass production. To date, it still accounts for more than 80% of the PV cell market. There are two versions of the c-Si PV cell: monocrystalline and polycrystalline.

3.4.1.1 Monocrystalline PV cells

This is the most common type of cell being used, representing about 80% of the market. Essentially, it uses crystalline silicon p-n junctions. This type of cells is manufactured from a single crystal ingot.

The efficiency of these cells is limited by the amount of energy produced by photons. Working with longer wavelengths does not help in obtaining more energy because, on one hand, energy decreases with longer wavelengths and, on the other hand, there is an increase in thermal dissipation. This causes the cells to heat up, thus decreasing their efficiency because of the energy being lost as heat. Under STC, the maximum recorded efficiency is 24.7%, stated by [101].

After the manufacturing of the silicon ingot, with a diameter of 10 cm to 15 cm, it is then cut in wafers of 0.3 mm thick. There are several silicon PV cell designs. Typically, both sides of the wafer are passivated with an insulator (SiO_2), so as to reduce surface recombination, and small holes are opened through the insulator to place the metal contacts. Then, trivalent dopant is difused to the rear contact areas, in order to form the p^+ zone. At the front side, pentavalent dopant is used in the same way to form the n^+ zone. A textured surface can be used on the front side, to trap the photons that enter the surface. In addition, an antireflective coating can also be used, beneath the textured surface, to maximize the efficiency. The resulting PV cell typically has a short circuit current at about 35 mA/cm^2 and an open circuit voltage of 0.55 V at full illumination [101]. In Fig. 3.10, it is shown how a module based on this type of cell looks like.

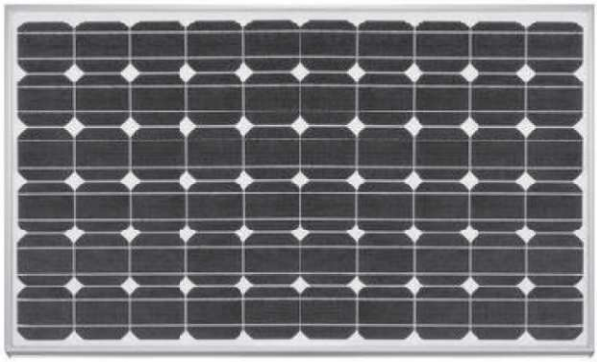


Fig. 3.10 - Monocrystalline PV module [73].

A module is made up of several cells, connected in parallel and in series, so as to produce higher currents and higher voltages, respectively, and consequently, a higher power. The monocrystalline PV cells are cut from a cylindrical single crystal ingot. To save material and space, the solar cells are cut to an octagonal piece, giving them this typical shape. There is always some wasted space because of the cut corners, and wasted material, because of the octagonal cut being performed over the cylindrical ingot.

3.4.1.2 Polycrystalline PV cells

In order to reduce costs and increase production, new crystalization techniques were developed. The costs with the production of polycrystalline cells are lower than with the monocrystalline

ones, although efficiency is inferior to that of the latter, standing at about 15% [101]. However, the main advantage is the reduction of flaws in metal contamination and in the crystal structure.

Polycrystalline cell manufacturing is initiated by melting silicon and solidifying it to orient crystals in a fixed direction, producing a rectangular ingot of multicrystalline silicon to be sliced into blocks and finally into thin wafers. However, this final step can be eliminated by cultivating wafer thin ribbons of polycrystalline silicon. As a result, since the shape of the ingot is rectangular, the PV cells in the PV module will look like as shown in Fig. 3.11, and having no waste of panel space, neither of ingot material. The manufacturing process of the panel modules is similar to the one described for the monocrystalline PV cells.

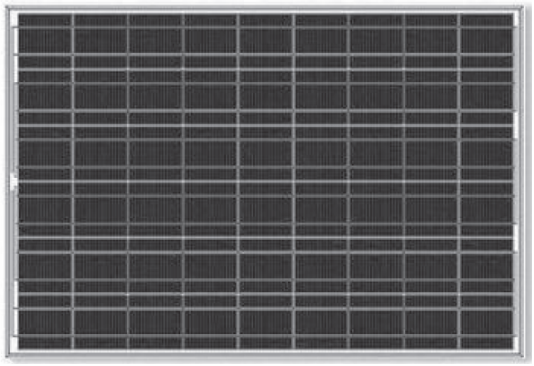


Fig. 3.11 - Polycrystalline PV module [73].

When using silicon modules (mono or polycrystalline), one technique that has emerged, is the use of smaller cells to make up a module, but with the additional placement of large lens over each individual unit. By doing this, the light intensity is magnified by a factor that can reach up to 300 times [101]. This technology is called concentrating PV. Concentration can be achieved by using mirrors, lenses, or the combination of both. This concentration needs some means to track the light, or the use of curved lenses or mirrors, with the cell at the center of the curvature so that the concentrated light can always reach it.

The commercial PV modules, either for mono or polycrystalline situations, given that the cells are fragile and vulnerable to the elements, have to be made more robust. Thus, a framing structure is used, having a piece of glass on the front side of the module, two thin sheets of EVA (ethylene vinyl acetate) film, one at the front and other at the back side of the array of PV cells, and a back plate. All these components are bonded together in a heated press.

3.4.1.3 Emitter wrap through (EWT)

The emmiter wrap through PV cells have achieved an efficiency increase, not because of the type of materials being used, but rather because of the design of the cells.

Small laser drilled holes are used to connect the rear n-type contact with the opposite side emitter. The removal of front contacts allows for the full surface area of the PV cell to absorb solar radiation, because masking by the metal lines is no longer present. Several tests showed that there are manufacturing gains by putting the contacts on the backs of the cell. Using EWT has allowed an increase of 15% to 20% in efficiency [101]. One major disadvantage of this technology is the large area occupied by EWT cells. Also, this technology suffers from high series resistance which limits the fill factor. In Fig. 3.12, there is a schematic representation of such a PV cell.

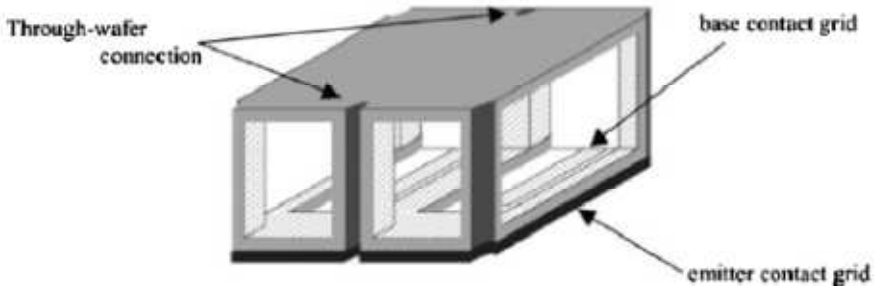


Fig. 3.12 - Schematic representation of an emitter wrap through PV cell [101].

3.4.2 Second generation PV cells

The PV cells included in this generation belong to the thin film technology. This technology aims to reducing the cost of PV cells by reducing material and manufacturing processes, without risking the environment or the lifetime of the cells.

Amorphous silicon (a-Si) thin-film silicon PV cells are much less expensive than the crystalline ones, but the efficiency is only 6% to 10%. In between, are the CIGS (copper indium gallium selenide) and CdTe–CdS thin film PV cells, with a typical efficiency of around 10% and account for about 15% of the market. Because of their very high absorption coefficient, the amount of materials required is small, and the production process is simpler. Thus the unit price per peak watt is lower than for the crystalline silicon PV cells.

The fabrication process is different from the one to achieve crystalline PV cells. Instead of having a layer of p-material with another of n-material on top of it, and glass covering each of the two sides, thin film is based on the deposit of thin layers of materials, on glass, plastic or stainless steel substrates. The thickness of each layer is inferior to 10 μm, while in the crystalline technology, it could have hundreds of microns. This is because amorphous silicon absorbs sunlight very well, so that only a thin layer is required, resulting in less material. Moreover, as the layers are thinner, and laid over stainless steel or plastic, this allows for the creation of flexible products. On the other hand, as less material is laid out, the absorption

potential is also reduced, thus lowering the efficiency of the cell. A factor than can counter this decrease, is the use of materials that can achieve better efficiencies.

There are four types of thin film PV cells that are presently at the market. These are the amorphous silicon cell (multiple junction structure), the thin polycrystalline silicon on a low cost substrate, the copper indium diselenide/cadmium sulphide hetero-junction cell, and the cadmium telluride/cadmium sulphide hetero-junction cell [101].

3.4.2.1 Amorphous silicon

The main difference between this technology and crystalline silicon is the fact that the silicon atoms are randomly located from each other. This random atomic structure causes a band gap of 1.7 eV, which is higher than in crystalline silicon, whose value is 1.1 eV. This larger band gap privileges the absorption of visible wavelengths, when compared to the infrared portion of the spectrum. This technology has several variations, where the substrates can be made of glass, flexible stainless steel or plastic foil, tandem junction, double and triple junctions. In each case, a different performance is achieved.

The maximum efficiencies for amorphous silicon in a laboratory environment are about 12%. However, single junction a-Si PV cells, when exposed to sunlight, degrade due to the Staebler-Wronski effect, which causes changes in the properties of hydrogenated amorphous silicon [101]. Thus, their efficiency progressively drops, until a value of about 4% to 8%. To improve the efficiency and solve the degradation problems, there have been attempted some approaches, such as developing double- and triple-junction a-Si devices. Under STC conditions, the efficiencies of such technologies are around 6% to 7%.

Another technology of construction, whose objective is efficiency improvement, consists to stack junctions, layering two or more junctions on top of each other. At the top of this structure, a very thin layer of a-Si is deposited, in order to convert the shorter wavelengths of the visible spectrum. However, with longer wavelengths, microcrystalline silicon is most effective, in addition to some of the infrared range. This results in higher efficiencies than amorphous silicon cells of about 8% to 9%, depending on the cell structure and layer thicknesses.

Appendix B presents a more in-depth explanation on the procedures and details about the fabrication of an amorphous silicon PV cell that has been used in conjunction with the main system of this research thesis.

3.4.2.2 Cadmium telluride or cadmium sulphide/cadmium telluride

The reason why this kind of technology is used has to do with the use of inexpensive industrial processes, in comparison to crystalline silicon technologies, while offering higher efficiencies than amorphous silicon does [103].

Cadmium telluride (CdTe) has a band gap of 1.45 eV and a high direct absorption coefficient, being recognized as a promising photovoltaic material for thin-film solar cells. Small CdTe cells with efficiencies greater than 15% and CdTe modules with efficiencies greater than 9% have been demonstrated [101].

The toxicity of cadmium (Cd) and the related environmental issues, remain somewhat of a problem for this technology, making necessary a recycling program for decommissioned PV cells. The other potential issue is the availability of telluride in nature, which might cause some raw material constraints that will then affect the cost of the modules.

In Fig. 3.13, a cross section of a typical CdTe PV cell is shown.

Glass superstrate
Front contact (ITO/ZnO)
CdS (cadmium sulphide) n-type layer
CdTe p-type layer
Back contact

Fig. 3.13 - Cross section of a typical CdS/CdTe PV cell.

3.4.2.3 Copper indium diselenide or copper indium gallium diselenide

These are PV devices that contain semiconductor elements from groups I, III and VI of the periodic table. The advantage in the use of these materials is their high optical absorption coefficients and electrical characteristics. In addition, better uniformity is achieved through the usage of selenide, as the number of recombinations is reduced, improving both the quantum and the conversion efficiencies.

CIGS (indium incorporated with gallium - increased band gap) are multi layered thin film composites. The best efficiency of a thin-film PV cell is 20% using CIGS [101]. The use of glass or flexible substrates can be used with this material. The biggest inconvenient with this technology is the shortage of Indium, which is used in the ITO (Indium tin oxide). A strategy to counter this factor is to recycle indium from decommissioned PV cells.

Both CdTe and CIGS modules show degradation in high heat and humidity conditions and need additional barrier coatings to protect them from such degradation. This kind of conditions degrades the junction transport properties and minority carrier transport characteristics of the cell absorber. Fig. 3.14 depicts a typical cross section of a CIGS PV cell.

ZnO transparent oxide
CdS buffer layer [or Indium Sulfide (InS)]
CIGS (absorber)
Mo contact layer
Glass

Fig. 3.14 - Cross section for a copper indium gallium diselenide PV cell.

Some properties of the materials that have been referred are summarized in TABLE 3.3, as adapted from [73].

TABLE 3.3 - Properties of some common PV cell materials.

Material	CuInSe2	Si	GaAs	CdTe
Band gap (eV)	1.04	1.11	1.43	1.49
Absorption edge (μm)	1.19	1.12	0.87	0.83
Absorption coefficient (cm^{-1})	1.0×10^5	1.0×10^3	1.5×10^4	3.0×10^4

3.4.3 Third generation PV cells

This generation of PV cells is based on multi-junctions, where several crystalline layers, with different band gaps, are stacked on top of each other. The objective is to absorb as much solar radiation as possible. In addition, these cells have shown more robustness to outer space radiation [101].

3.4.3.1 Compound semiconductor

These hetero-junctions are tuned to use the full wavelength spectrum. When light hits a wide band gap layer, it produces a high voltage using high energy photons, enabling lower energy photons to transfer to narrow band gap sub-devices, which absorb the transmitted infrared photons. In Fig. 3.15, a structure of a Gallium arsenide (GaAs)/Indium Gallium Phosphide (InGaP) multi-junction PV cell is depicted.

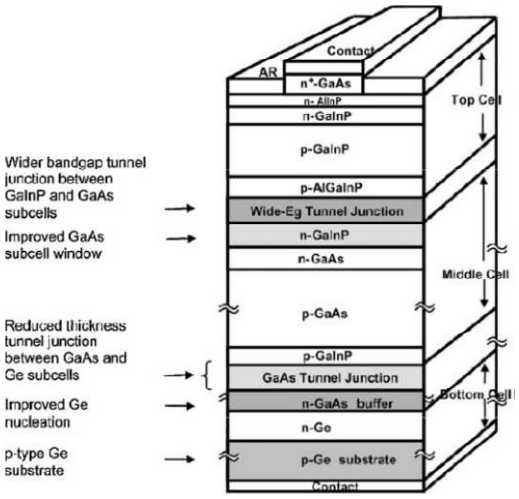


Fig. 3.15 - Epitaxial stack of a multi-junction PV cell [101].

Such devices have reached efficiencies in the order of 40.8%, more exactly from a metamorphic triple-junction PV cell.

3.4.3.2 Dye-sensitized cells

These cells consist of a semiconductor and an electrolytic liquid. The semiconductor and electrolyte work in tandem to split the closely bound electron-hole pairs produced when light hits the cell. The source of the photo-induced charge carriers is a photosensitive dye that gives the PV cells their name "dye-sensitized". In addition, a nanomaterial, most commonly titanium dioxide (TiO_2), is also often used to hold the dye molecules in place, like shown in Fig. 3.16.

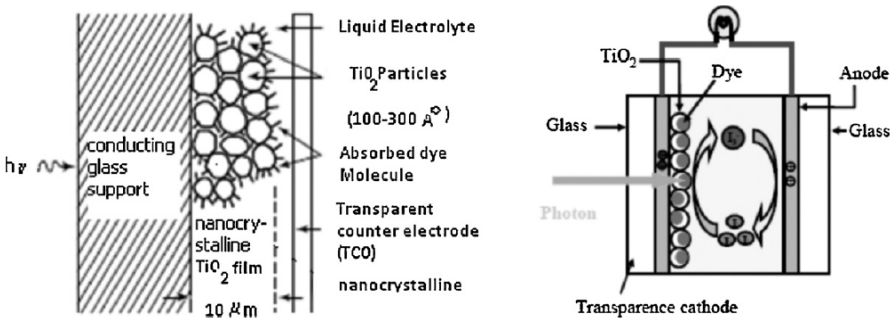


Fig. 3.16 - Cross section of a dye sensitized PV cell [101].

The use of dye sensitized cells for photovoltaic applications tries to emulate chlorophyll action in plants. This technology contains volatile solvents in their electrolytes that can permeate across plastic and present problems for sealing the cells. Cells with these solvents are unattractive for outdoor use due to potential environmental hazards. Researchers have developed PV cells that use solvent-free electrolytes, but the efficiencies of these cells are too low [101]. Heat, ultra-violet light, and the interaction of solvents within the encapsulation of the cell are negative issues with this technology.

3.4.3.3 Organic cells

This type of cells is made from thin films, with about 100 nm of thickness, of organic semiconductors such as polymers and small-molecule compounds like pentacene, polyphenylene vinylene, copper phthalocyanine (a blue or green organic pigment) and carbon fullerenes.

These materials are interesting because of their mechanical flexibility, disposability and low manufacturing cost, because of the use of plastic, as opposed to traditional silicon, and not requiring high temperatures and high vacuum conditions.

Electron (donor-acceptor) pair forms the basis of organic cell operation, where light agitates the donor causing the electron to transfer to the acceptor molecule, hence leaving a hole

for the cycle to continue. The photo-generated charges are then transported and collated at the opposite electrodes to be utilized, before they recombine [101].

Typically, the cell has a glass front, a transparent Indium Tin Oxide (ITO) contact layer, a conducting polymer, a photoactive polymer and the back contact layer (Al, Ag, etc.). Since ITO is expensive, various groups have tried to use carbon nanotube films as the transparent contact layer. A typical cross section of an organic solar cell is shown next in Fig. 3.17.

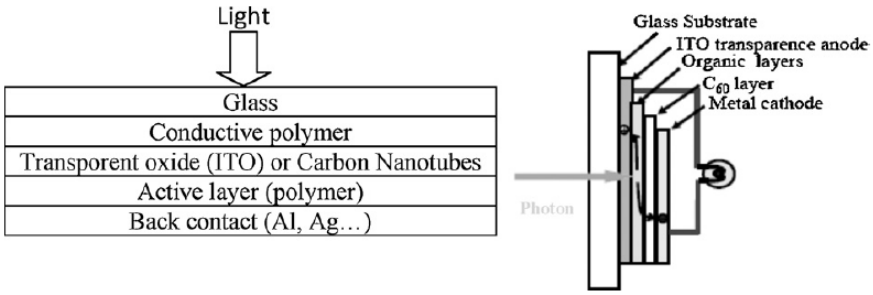


Fig. 3.17 - Structure of an organic PV cell [101].

3.4.3.4 Carbon nano tubes

This kind of technology emerged to mitigate the limitations of the other technologies. Nanoscale components have the ability to control the energy band gap and an enhanced probability of charge recombination. Examples of these nanostructures are the carbon nano tubes.

Carbon nano tubes are made according to a hexagonal carbon lattice, showing excellent mechanical and electrical properties, and can be single-walled or multi-walled, as shown in Fig. 3.18.

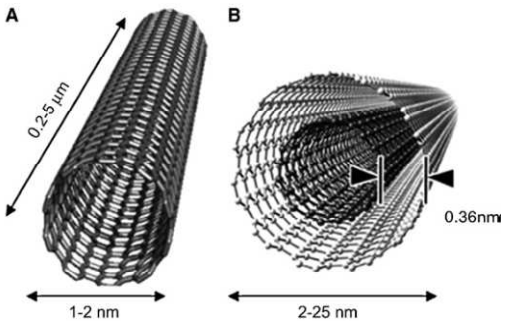


Fig. 3.18 - Single-walled and multi-walled carbon nano tubes [101].

This material is photosensitive just like other materials in photovoltaic technologies. When coated by special p- and n-type semiconductor materials, it forms a p-n junction that generates electrical current. Such a methodology enhances and increases the surface area available to produce electricity [101]. The efficiencies are still in the range from 3% to 4%, but much research is being conducted in this field.

3.4.3.5 Quantum dots

Quantum dots are devices that also fit into the nano technology materials. These, are special semiconductor systems that consist of a combination of periodic groups of materials, molded in a variety of different forms. They are on nanometer scale and have an adjustable band gap of energy levels, performing as a special class of semiconductors [101].

The PV cell with larger and wider band gap absorbs more light, hence producing a bigger output voltage. However, cells with smaller band gap result with larger current but smaller output voltage. The latter includes the band gap in the red end of solar radiation spectrum. Quantum dots are known to be efficient light emitters with various absorption and emission spectra depending on the particle size. Currently, researchers are focusing on increasing the conversion efficiency of these PV cells.

3.4.4 Comparison of the different PV technologies

Up until this point, this chapter has focused on giving an overview about the PV technologies and how these are organized, in terms of devices and materials. This overview is only introductory, focusing on general aspects of each topic.

It is outside of the scope of this thesis, to provide a broader insight about this theme, so the reader is asked to pursue the search for information in the references that have been given along the text. In addition, further information about third generation photovoltaic technologies can be found in [102], [104], [105] and [106], for example.

Having given an overview about the types of PV cells in the previous sections, it is useful to have a comparison between them, in terms of efficiency. Photovoltaic products have grown in commercial availabity in the past few years and the trend is to continue to grow, as a response to trying to find a good alternative for fossil sources of energy. The efficiency of the cell is also a way of quantifying the efficiency of the cost of the investment that is made, although, as it has been seen, the type of material must additionally be taken into account. As such, to have a general idea about the present panorama, the best values for several research cells, in various PV technologies, are shown in Fig. 3.19. In this figure, it can be observed that at the present time, the highest recorded efficiency that appears in the graph is 44.4%, corresponding to a multi-junction cell. It is to note that research PV cells often give better results than commercial ones. This figure serves to have an idea of the progress that PV technologies have had over the years, since about the middle of the decade of 1970, when this industry had a true start.

The technologies shown in Fig. 3.19 include not only those that have been referred, but also some others that have not been addressed in this text.

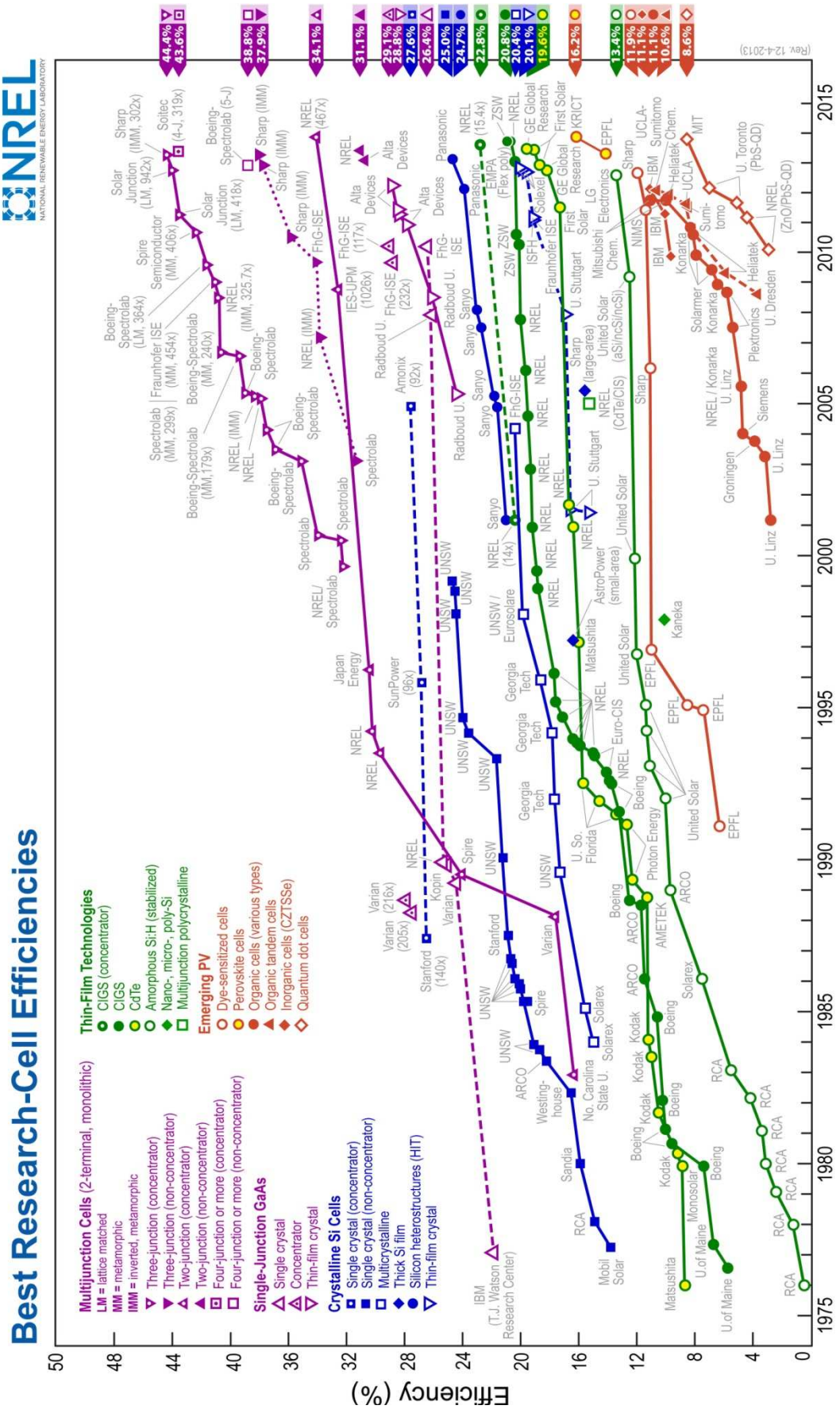


Fig. 3.19 - Timeline of PV cell energy conversion efficiencies (from the U.S. Department of Energy - National Renewable Energy Laboratory).

Since the work presented in this thesis makes use of amorphous silicon PV cells, it is important to notice that the present efficiency for this type of cells is 13.4%. To conclude, it is to stress out that, regardless of the technology being used, the trend is towards an increase in efficiency, which foretells that, in the future, PV technologies have indeed an important role to play when dealing with clean energies, whatever the scale of the applications being used.

3.5 Integrated CMOS PV cell prototype

According to the analysis presented in the previous section, crystalline silicon allows for building one of the most efficient PV cell types. Considering that the energy harvesting system will be built in standard CMOS technology, which uses crystalline silicon, it is natural to try to integrate the PV cell with the system, on the same CMOS die. As shown in [87] or [107] it is possible to build a PV cell in CMOS technology. However, there are some problems associated with this approach that prevent the use of a CMOS PV cell together with other circuits on the same CMOS die. These will be discussed next.

3.5.1 Electrical model of a CMOS PV cell

In order to better understand the possibilities of using an integrated CMOS PV cell, it is necessary to obtain its electrical model. Using the information available in [87], it is possible to build this electrical model, corresponding to the equivalent circuit depicted in Fig. 2.19 a). The model is composed by a current source, a diode model and a series and parallel resistors. The model parameters (I_1, R_P and R_S) are adjusted to match the open circuit voltage and the short circuit current reported in [87], corresponding in the original reference, to measured values at an inciding white light illuminance of 10 klux. Extrapolating the reported PV cell area to 3 mm^2 results in a peak watt around 390 μW and in a short circuit current of 1.62 mA. Using this extrapolation, the values that were obtained for the model were then 1.728 mA, 700 Ω and 20 Ω, respectively. The diode depicted in the model is a diode of the CMOS technology being used, with the width, length and multiplier set to 25 μm, 25 μm and 15000, respectively.

Two of the previous PV cells, in series (each having 3 mm^2), were simulated using two equivalent circuits in series, resulting in the power curves depicted in Fig. 3.20. This graph shows the output power of the PV cells for some levels of light intensity, namely, for 100%, 95%, 90%, 80% and 60% of the maximum illumination (10 klux of white light). This scaling only accounts for the current drawn from the current source of the electric model (I_1), while maintaining the other parameters unchanged. Thus, the power functions for intensities inferior to 100%, were obtained by proportionally scaling the current I_1 of the model. This procedure is

only approximate, since that the other parameters of the model would also need to be adjusted. However, in the absence of more information, this was the adopted procedure.

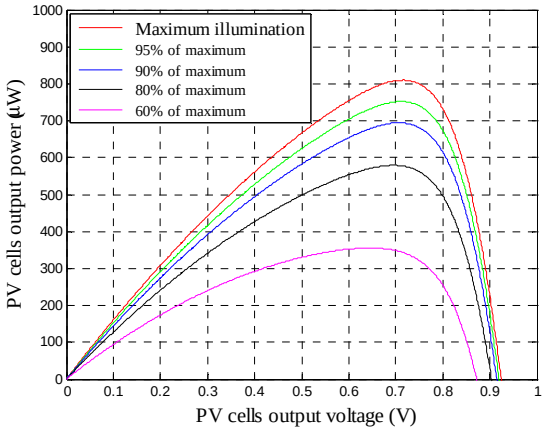


Fig. 3.20 - Power curve of two PV cells equivalent circuits connected in series, for different levels of illumination.

In Appendix B, the characterization of an amorphous silicon PV cell that was specifically manufactured for this work, was performed by taking into account all the changes that the model parameters suffer when there is a change in the level of light inciding over the cell.

The maximum available power at the output will depend on the light intensity to which this cell is subjected. The information about the maximum available power from the PV cells, as well as the voltage at which that maximum power occurs, the short circuit current and the open circuit voltage, is summarized in TABLE 3.4.

TABLE 3.4 - PV cell electrical characteristics for different light intensities.

Light Intensity	Irradiance (klux)	Irradiance (W/m^2)	P_{max} (μW)	v_{max} (mV)	I_{SC} (mA)	V_{OC} (mV)
100%	10	14.64	810.1	718.9	1.680	924.1
95%	9.5	13.91	752.2	710.0	1.596	919.6
90%	9	13.18	694.4	709.9	1.512	914.7
80%	8	11.71	579.3	699.7	1.344	903.6
60%	6	8.78	355.5	648.6	1.008	872.1

Since white light was used in [87], the conversion from lux to W/m^2 is performed using the relation 1 lux = 1/683 W/m^2, as indicated in Section 2.2.6. For a value of 20% of the maximum light intensity (about 2.92 W/m^2), and using the same source of light, the maximum power obtained is only 40.64 μW, at a voltage of 261 mV. Thus, with this level of light intensity, using this series of cells, one would not be able to supply any electronic application, either because of the available output power and the voltage provided at the terminals of the series of cells.

3.5.2 Development and layout of an integrated CMOS PV cell

Since the objective was to use integrated CMOS PV cells, this type of PV cell was actually designed and manufactured in a 0.13 µm CMOS technology. In Fig. 3.21, the layout of the PV cell and the die in which it was included are depicted. In addition, a picture of the actual die after manufacturing, already placed into a PCB using direct bonding (for testing), is also shown.

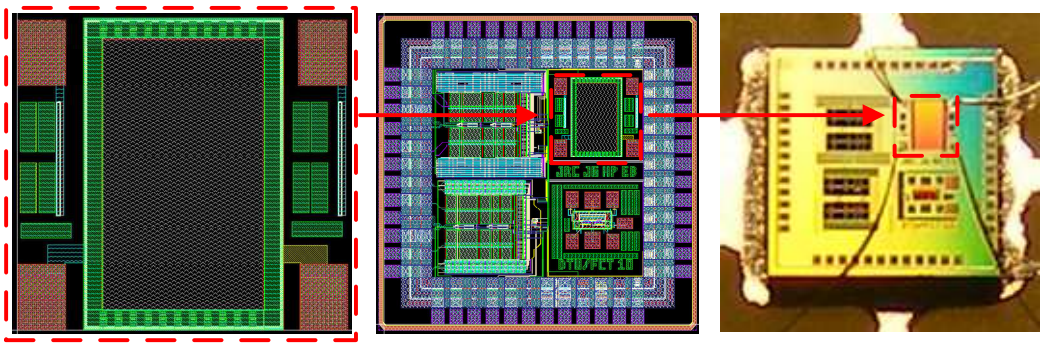


Fig. 3.21 - Layout of the integrated CMOS PV cell (left), integrated die that hosted the CMOS PV cell (middle) and photograph of the die containing the CMOS PV cell (right).

Reference [87] shows a PV cell that was manufactured, experimentally characterized and used to power a ring oscillator. However, the ring oscillator and the PV cell are in fact in two separate CMOS dies. In [107] two separate dies are also used, one for the PV cell and the other for the circuit. The reason why the PV cell cannot be integrated into the same die as the circuit is simple, as referred in Section 3.3: the absorption of photons by silicon is not very efficient. The photons have to travel a certain length before they are completely absorbed. The absorption coefficient of silicon for different wavelengths, together with the percentage of absorbed photons, is shown next in TABLE 3.5. Absorption is taken into account by considering that reflectance is negligible.

TABLE 3.5 - Absorption in Silicon, for various colors.

Color	wavelength (nm)	Energy (eV)	Absorption coefficient (cm^{-1})	Depth (% absorbed), µm		
				10%	50%	90%
Blue	450	2.76	21000	0.05	0.33	1.10
Green	550	2.26	5830	0.18	1.19	3.95
Red	650	1.91	2500	0.42	2.77	9.21

For example, this table reports that the green color, at a depth of 3.95 µm, had 90% of its radiation absorbed. The previous table shows that longer wavelength photons can deposit most of their energy at depths larger than 1 µm. Since the depth of the NWELL in a typical CMOS technology is around 1.5 µm, this means that most of the energy will be deposited in the p^- substrate, located below the NWELL, because it acts as the anode of the PV cell. This has the unintended consequence of producing a positive voltage in the substrate, which can cause latch-up in the CMOS circuit. This also makes impossible to connect two CMOS PV cells in series,

since all the diffusions in CMOS are less than 1 µm in depth. The only option to connect PV cells in series is to use non-standard CMOS technologies such as SOI CMOS [89], because in this case, each PV cell is electrically isolated from its neighbors. However, this technology is much more expensive than standard CMOS technology.

In order to try to integrate a PV cell in the same CMOS die with other circuits, it is necessary to make sure that the positive charge that builds-up in the substrate under the PV cell does not spill over to the rest of the circuit. The only option to do this is by using a guard ring around the PV cell, connected to its cathode. This guard ring is equivalent to connecting a resistor between the anode and the cathode of the PV cell. The value of this resistor depends on the substrate resistivity and on the distance between the guard ring and the p^+ diffusion, which is the anode terminal of the PV cell. This resistor is in parallel with resistor R_p in Fig. 2.19 a), therefore, its value should be as large as possible. Since it is not possible to control the value of the resistivity of the substrate, the only option is to increase the distance between the guard ring and the anode of the PV cell. However, if this distance is large, most of the area taken by the cell will not be producing energy and the PV cell will be very inefficient.

Fig. 3.22 depicts a simplified representation of the structure of the integrated photodiode that was laid out.

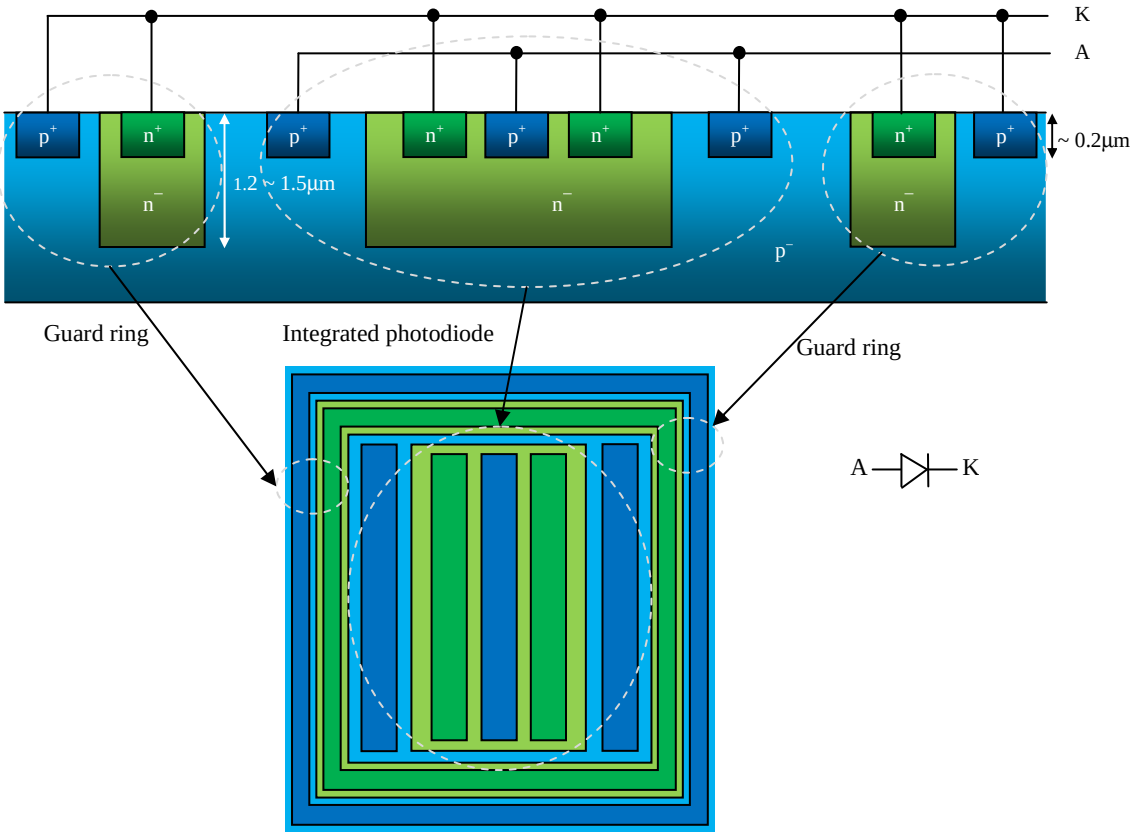


Fig. 3.22 - Simplified structure of the integrated photodiode.

The anode (A) and the cathode (K) terminals correspond to the two lower pads depicted in Fig. 3.21 (left), respectively. When the layout was done, one had to pay particular care to ensure that the area corresponding to the photodiode would not be covered with metals or oxide, as usual in the fabrication process. Otherwise, light would have no way to irradiate the PV structure. On the other hand, all the rest of the surrounding elements were treated as usual when performing a layout, i.e. let them be covered when the die is manufactured.

This type of structure and technology allows for the formation of two junctions, at two different depths. Closer to the surface, in the range of about 0.2 μm, one has a stronger concentration of carriers because of the p^+ and n^+ diffusion implants, and thus a p^+n^+ horizontal junction is formed. However, deeper into the material, the doping concentration decreases, and from about 1.8 μm, the concentration of carriers reaches a minimum value, which holds even for higher depths. This results in p^- material and thus, p^-n^+ vertical junctions are formed.

A guard ring placed around the PV cell, which can be identified in Fig. 3.21 and Fig. 3.22, appears like a frame around the PV structure. When illuminated, the photodiode will be forward biased, meaning that the voltage from A to K will be approximately 0.6 V. Since the cathode is tied to ground (a potential of 0 V), this would mean that the anode (i.e., the substrate) would have its potential increased to 0.6 V.

However, this is not tolerable for the other circuits built on the same substrate, since the latter is supposed to be held at ground potential. For this reason, it was needed to shield the photodiode structure with the guard ring shown around it, so as not to increase the substrate voltage, preventing any latch-up condition. The purpose of this guard ring is to have the same effect of a distributed resistor around the PV cell, so that from its very periphery, until the guard ring, the voltage would gradually decrease along the substrate, from about 0.6 V (the voltage drop across the photodiode junction when illuminated and, consequently, forward biased), to zero (the potential of the substrate), while maintaining the cell in normal operation. In electrical terms, this can be described by the following schematic:

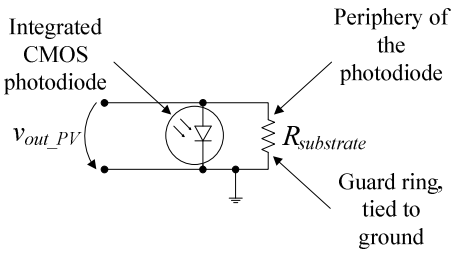


Fig. 3.23 - Equivalent electrical circuit of the purpose required for the guard ring.

In Fig. 3.23, $R_{substrate}$ is the distributed resistor along the substrate, existing all around the PV cell itself, in the stretches that go from its near periphery (A) until the guard ring (K).

Unfortunately, there was not enough information from the foundry. It was expected that the substrate had a very reasonable resistivity, such that the amount of substrate between the periphery of the PV cell and the guard ring would yield a resistance at least in the range of some kΩ. Thus, the PV cell would be able to operate correctly and provide its expected voltage (v_{out_PV}, in Fig. 3.23) to the circuits to be supplied, when exposed to light.

3.5.3 Experimental results of the prototyped integrated PV cell

In contempt of the intended effect, the use of the guard ring caused a short-circuit over the photodiode, because the voltage between the anode and cathode terminals was zero volts, even under maximum illumination conditions.

In addition, the diode was supposed to have a low resistance when forward biased and a very high resistance when reversely biased. However, measuring resistance from A to K and vice-versa, the value obtained, for both situations, was around 120 Ω to 130 Ω. For the reverse biasing case, this value is too low. This test structure was designed with the hope that the substrate resistance would be larger and therefore this guard ring would not be impeditive of the PV cell to produce an output voltage. However, what happened was that the PV cell was effectively shorted due to the guard ring. The distance between the periphery of the photodiode and the guard ring did not provide the necessary amount of resistance so that the PV cell could remain in operation, coexisting with the other circuit structures sharing the substrate. In other words, resistance $R_{substrate}$, in Fig. 3.23, is too small to allow for the photodiode to work. Instead of making a separation between the PV structure and the rest of the die, the guard ring short-circuited the PV structure, causing the major setback of having an unusable PV cell.

Moreover, the two upper terminals, which can be seen in Fig. 3.21 (left), were built with the purpose of experimentally determining the resistance between the guard ring (i.e., the ground terminal) and the piece of substrate connected to the strips of *metal1* seen on the layout, as these are located at different distances from the guard ring. The values of resistance that were measured between those two points were about 100 Ω for the upper left terminal, as well as for the upper right terminal. These values are considered to be very low for the intended purpose and confirm that the resistivity of the substrate is too low to provide the required effect.

A possible solution, to counter for the facts that have been noticed, would be to widen the strip of substrate around the periphery of the PV cell, between it and the guard ring. However, the structure would tend to be inefficient in terms of area, because one would have an amount of die area specifically commited to serve as a separation zone, having no other usefulness. In

addition, since the current prototype shared the integrated circuit with other prototypes, from other designers (see the center of Fig. 3.21), an increase of unused area would be prohibitive.

3.5.4 Conclusions about the integrated PV cell

Unfortunately, as demonstrated by the results that were measured, the experimental cell did not have any acceptable performance and so, the alternative is to use amorphous silicon PV cells, which will be shown in Chapter 7, and more detailed in Appendix B.

By doing a literature research, in [88] there are some problems identified and reported when sharing an integrated PV cell with other circuits in the same substrate. These happened to be the case with the present work. To use such a type of cell, it would have to be placed on a substrate different from the one in which the main system resides. This strategy was the one in both the system and application described in [107] and also in [108]. In these references, it is shown that when stacking a series of PV cells, each individual cell resides in an individual substrate. Because of this, the idea of using an integrated CMOS PV cell, on the same substrate as the circuits to be powered, was dropped.

However, if a SOI technology [89] had been used, there would be no problem in sharing the substrate, because the latter would be an insulator, and thus would provide the necessary electric isolation between the independent structures placed on it, although at a higher cost.

3.6 Indoor light energy availability study

Before starting the design of an indoor environment energy harvesting system, it is necessary to have a better understanding of the available light power, under different situations, in such an environment. In order to assess the amount of available light in an indoor environment, a set of measurements was performed. There are some literature references, some of which have already been mentioned, in which light measurements were also performed. Examples of such are present in [77]-[80]. However, in order to have a hands-on perspective of the light availability in the typical indoor environments that can be found in *campus* facilities, at the geographical location (and sorroundings) in which this whole work was developed, it was decided to perform these measurements. Another important reason is the fact that the measuring device was the same that was used to measure the light intensities that allowed characterizing the a-Si PV cell that was specifically built for this work (see Appendix B). By having the same measuring device, common to these two contexts, there is an improved reliability about the values that are considered and how the PV cell would respond to the light values that were obtained indoors. This measuring device is described in Appendix A, where there are also presented the band-pass

filters that aided in the measurements at several wavelength bands, as well as a brief set of indications to correctly use all of this material.

3.6.1 Light power intensity measurements

Partial measurements were performed, one in each of five wavelength bands. These measurements were then combined into a single light irradiance value. The measurements were performed in four locations inside an office room, as sketched in Fig. 3.24. These locations cover most of the cases that a light energy harvester would find in an indoor environment. These four locations correspond to L_1 and L_2, and in each, at two different heights (h).

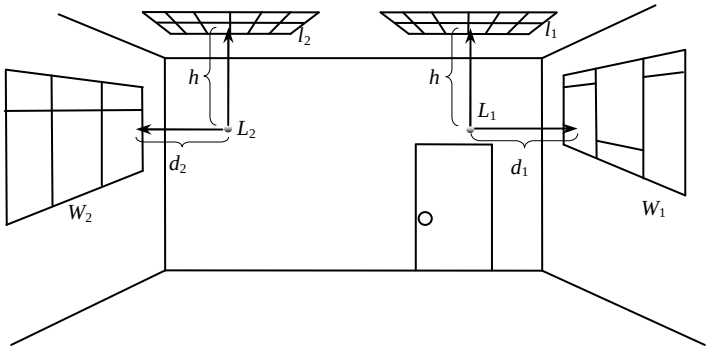


Fig. 3.24 - Schematic picture of the room where the indoor measurements took place.

In this sketch, l_1 and l_2 are the main lamps on the ceiling; h is the distance between the main lamps and the sensor [located either at L_1 (under l_1), or L_2 (under l_2)]; W_1 and W_2 are the windows of the office room; d_1 and d_2 are the horizontal distances between each of the windows and the sensor (located at L_1 or L_2, respectively). The values of the previous dimensions are d_1 = 2.3 m; d_2 = 2.4 m; h = 1 m or 2 m; area of $W_1 = 1 \times 2 = 2$ m^2; area of $W_2 = 1.25 \times 2.6 = 3.25$ m^2.

The room is located at latitude 38º45’25’’N and longitude 9º7’2’’W. Window W_1 is oriented to East and the light entering from it is not as bright as the one that enters through W_2 (oriented to West), because the latter is directly at the façade of the building, while the former is not. Each of the lamps l_1 and l_2 is composed by two fluorescent light tubes, with a power of 36 W each. The light sensor can be oriented upwards to l_1 or l_2 (↑), to W_1 (→) or to W_2 (←). To each position is assigned an index to help identifying it in the subsequent text. A measurement taken outdoors will be identified with index 0. The complete set of positions is enumerated in TABLE 3.6.

In each measurement, the light sensor orientation was slightly adjusted in order to maximize the received light power, as it would occur in a real energy harvesting situation. The measurements were performed during two days (January, the 30th of 2012 and February, the 23rd of 2012), at different times of the day, having sunny weather outside. Since in wintertime,

outdoor light is weaker than in the rest of the year, these measurements can be considered as worst cases.

TABLE 3.6 - Positions where the measurements took place, referring to Fig. 3.24.

Position Index	h	Location	Orientation
0	O U T D O O R		
1	1 m	L_1	↑
2			$\rightarrow W_1$
3			$W_2\leftarrow$
4		L_2	↑
5			$\rightarrow W_1$
6			$W_2\leftarrow$
7	2 m	L_1	↑
8			$\rightarrow W_1$
9			$W_2\leftarrow$
10		L_2	↑
11			$\rightarrow W_1$
12			$W_2\leftarrow$

Outdoor measurements were also performed, in order to have a reference value, which can be compared to the values measured indoor. The indoor measurements, depending on the time of the day, comprehended natural light, natural and artificial light, or only artificial light. The whole set of measured values is listed in TABLE 3.7.

TABLE 3.7 - List of measured values, having sunny weather outside (except at 19h00m).

Position Index	Jan, 30th 2012 10h30m		Jan, 30th 2012 12h30m		Feb, 23rd 2012 16h30m		Feb, 23rd 2012 19h00m	
	P_{total} (μW)	Irradiance (W/m^2)	P_{total} (μW)	Irradiance (W/m^2)	P_{total} (μW)	Irradiance (W/m^2)	P_{total} (μW)	Irradiance (W/m^2)
0	20840	294	24080	340	16640	235	-	-
1	179.86	2.54	172.54	2.43	157.35	2.22	152.37	2.15
2	129.31	1.82	85.28	1.20	75.59	1.07	-	-
3	50.34	0.71	35.10	0.50	17.24	0.24	-	-
4	168.82	2.38	163.88	2.31	159.73	2.25	158.82	2.24
5	20.36	0.29	15.94	0.22	14.23	0.20	-	-
6	162.26	2.29	81.92	1.16	17.20	0.24	-	-
7	72.41	1.02	63.04	0.89	55.31	0.78	54.25	0.77
8	65.31	0.92	18.78	0.26	9.99	0.14	-	-
9	44.00	0.62	23.62	0.33	9.14	0.13	-	-
10	64.31	0.91	56.90	0.80	51.37	0.72	51.60	0.73
11	35.73	0.50	19.50	0.28	12.51	0.18	-	-
12	187.23	2.64	61.31	0.86	18.80	0.27	-	-

This table presents the value of the total power measured by the light sensor and the corresponding calculated irradiance. At 19h00m it was already dark outside so, naturaly, the measurements only account for the artificial light inside the room.

TABLE 3.8 helps to distinguish the more relevant values in TABLE 3.7, summarizing the worst and the best irradiance cases, obtained from the set of measurements that were performed.

TABLE 3.8 - Summary of best and worst irradiance cases from the light power measurements.

Outdoor irradiance (W/m^2)	Indoor irradiance (W/m^2)			
Best case at 12h30m	Natural plus artificial light		Only artificial light	
	Best case	Worst case	Best case	Worst case
340	2.64	0.13	2.24	0.73

It is important to notice that, even though the measurements having been taken in sunny days, the time of the year and the geographical location (winter, in the northern hemisphere), make the overall amount of available light power to be weaker. In wintertime, at latitudes near 38º (which is about the same where the measurements were taken), the actual path across the atmosphere can double, and the spectrum power becomes AM2. In addition, the atmospheric pollution can reduce the irradiance even more. All of these effects, combined among each other, explain the measured value outdoors of 340 W/m^2.

3.6.2 Conclusions

These measurements help to get an *in loco* realistic idea about the amout of light energy that can be used in a typical *campus* office (indoor) environment.

The measurements were performed at different times of the day, allowing that situations including natural light, natural and artificial light, or only artificial light (when dark outside), could be considered.

According to the summarized data in TABLE 3.8, the value of 0.13 W/m^2 is the lowest irradiance value found in this indoor environment, also because the location where it was recorded is not favoured. If the system is designed to be able to work with such a reduced irradiance value, then it will succeed in harvesting light energy the whole time, since under artificial lighting the irradiance value is higher.

If the series of PV cell that was modeled in Section 3.5.1 was to be used in the environment that was assessed, it would have no utility. The lowest level of light that was simulated for this cell is at about the same level of the best case for indoor irradiance reported in TABLE 3.8. Even in this extreme optimistic situation, the series of cells would not have the capacity to power any useful application. To counter this fact, a bigger cell of the same kind could be used, but in this case, the costs of production would seriously increase, making this solution prohibitively expensive.

Chapter 4

VOLTAGE STEP–UP CIRCUITS

4.1 Introduction

Raw electrical energy captured from the ambient sources is generally not suitable for direct usage to power electronic circuits. As such, this energy must be properly conditioned for practical use. The objective is to create a stabilized voltage (or current), which is required to power and bias the sets of load circuits and devices. According to the intended needs, the primary DC voltage must be stepped up (boost operation) or stepped down (buck operation). The classes of circuits that can achieve such a voltage conversion can be divided into those that use inductors and those that do not. Either way, the ultimate objective is to perform the voltage conversion as efficiently as possible. The regulator circuit also plays the role of protecting the energy storage device from overload voltages and, when dealing with a PV based system, of setting the working output voltage of the PV cell, in order to achieve optimal power operation conditions, by using a MPPT algorithm. In the following, the main types of energy conditioning systems will be summarily characterized, as well as energy storing devices and MPPT techniques.

4.2 Types of voltage converters

Whenever there is the need to convert a DC voltage of a certain value, into another one of a different value, higher or lower, there is the need to use a voltage DC-DC converter circuit.

There are various types of voltage converters. Basically, there are two main categories of voltage converters, which are the linear converters and the switched converters.

4.2.1 Linear converters

Linear voltage converters are very simple to implement, but they can only decrease the input voltage, in order to obtain the output voltage, which is kept constant by a controller circuit. This type of converter dissipates the excess of energy that is not intended to be used by the load, making it quite inefficient.

This converter can be implemented either with a series or a shunt topology. As the name implies, the series regulator is connected in series, between the input voltage source and the load, performing a voltage division. The principle of operation of the series voltage converter is shown in Fig. 4.1.

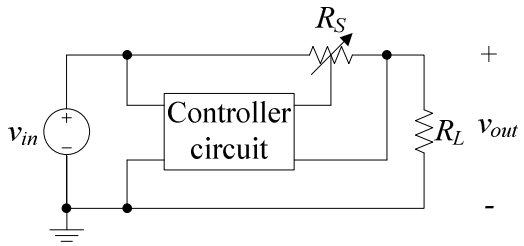


Fig. 4.1 - Conceptual circuit for the linear series converter/regulator.

The converter acts as if it was a variable resistor R_S, providing the output voltage v_{out} through the decrease of the input voltage v_{in}. Should the load R_L show any variations, the converter system adjusts its own resistance (R_S), under the action of a controller circuit, in order to keep a constant output voltage. This controller circuit is powered by v_{in}, and must know the value of v_{out}, in order to adjust R_S according to the needs.

The efficiency of this type of converter is proportional to the ratio between the output and the input voltages (v_{out}/v_{in}). Since this converter can only decrease the input voltage, this means that a higher efficiency is achieved with a smaller difference between v_{in} and v_{out}. Regulators designed to specifically operate under these conditions, by consequence achieving a higher efficiency, are known as low drop-out (LDO).

The shunt converter operates differently from the series converter. This converter acts as a variable resistor placed in parallel with the load, shunting it. This requires the use of a resistor R_{in} to be placed between the input voltage and the parallel arrangement of the converter and the load. This resistor can be the output resistance of the source providing v_{in}, an added resistor, or the combination of both. The principle of operation of the shunt voltage converter is shown in Fig. 4.2.

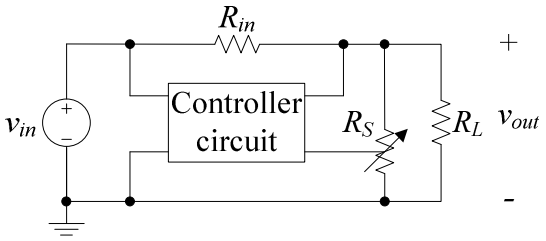


Fig. 4.2 - Conceptual circuit for the linear shunt converter/regulator.

The process that makes v_{out} constant, while the load may be varying, is the controlled adjustment of the equivalent resistance of the converter R_S, in parallel with the load. This control process has the same purpose as the one in the series converter.

The efficiency of a shunt converter can only be maximized if the output power is also maximized. The series converter does not have this limitation. However, the simple implementation of the shunt converter makes it suitable for applications that require a small and almost constant output power, but the problem of on-chip power dissipation persists and becomes more limiting than for the case of linear series voltage converters.

Thus, regarding efficiency issues, it is to stress out that, for a series converter, the power conversion efficiency is proportional to the voltage conversion ratio (VCR) and, for a shunt converter, proportional to the output power.

Either types of converter are very simple, making them very appealing for monolithic integration purposes. However, the converter required for a PV cell must provide an elevated version of the input voltage. As such, linear regulators are definitely not suited for this need, mainly because they can only decrease their input voltage. In addition, their typical low efficiency is also a factor that does not make them suitable, especially because of the very limited available input energy, in an energy harvesting system.

4.2.2 Switched converters

This kind of voltage converter, unlike the linear converters, is theoretically lossless. However, not every type of switched converter is well suited for integration into a silicon die, like the linear converters are.

The operating principle relies on the use of energy storing components and in switches to change the interconnections between the circuit elements in a given topology. Because resistors are not used, the losses can, in theory, be null. The passive components that can be used in these applications are inductors or capacitors. However, one of the most interesting features about switched converters is that, besides decreasing the input voltage, like the linear regulators do, they can increase it, performing a step-up operation.

4.3 Inductor-based converters

The process of using a switched converter to transform a DC voltage value into another DC voltage value relies on transferring energy from the input voltage to a reactive element (an inductor or a capacitor) and then retrieving part of the stored energy to the output, in order to achieve the desired voltage value. However, there is a fundamental difference between using a capacitor or an inductor: the voltage across an inductor can change abruptly and have a large discontinuity. In the case of a capacitor, the voltage cannot have discontinuities. This means that the voltage in a capacitor is always smaller than the input voltage and that the voltage in an inductor can be larger than the input voltage.

It is also important to consider the efficiency of transferring energy to a capacitor or to an inductor. In the operation of a DC-DC converter, these elements are connected to a voltage source through switches, and these switches have ON resistances. This can be represented by the circuits depicted in Fig. 4.3, where the resistor *R* stands for the ON resistance of the switch.

Fig. 4.3 - Equivalent circuits for charging a) a capacitor or b) an inductor.

When the switch *S* closes, the capacitor is charged until it reaches a voltage equal to v_{in} and the inductor is charged until it reaches a current given by v_{in}/R. The voltage in the capacitor and the current in the inductor are given by

$$v_c(t) = v_{in}\left(1 - e^{-\frac{t}{RC}}\right) \tag{4.1}$$

and

$$i_L(t) = \frac{v_{in}}{R}\left(1 - e^{-\frac{R}{L}t}\right), \tag{4.2}$$

respectively.

Using these expressions, it is possible to calculate the current and the voltage and, from those, the instantaneous power in each element of the circuits. Integrating the instantaneous power over time allows for obtaining the energy stored in the reactive elements and the power dissipated by the resistor, for each circuit. The graphs of these energies, as a function of time, are represented next, for the values *R*, *L*, *C* and v_{in} normalized to 1.

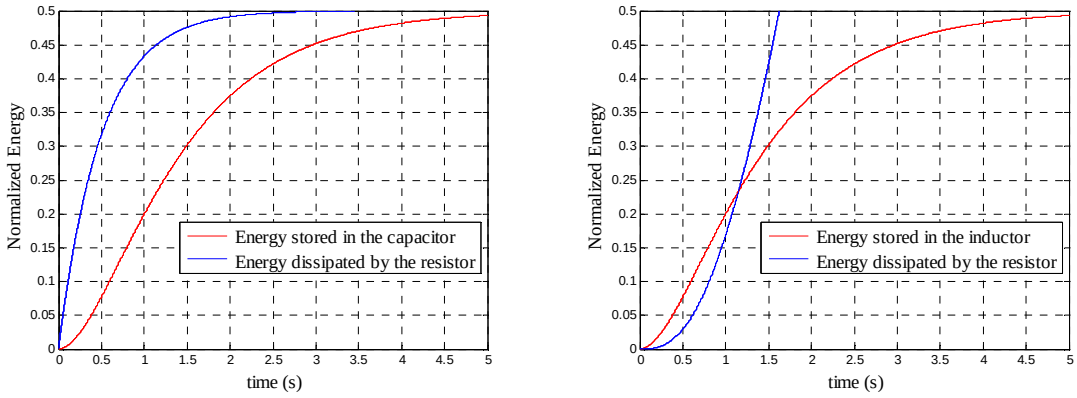


Fig. 4.4 - Instantaneous energy, as a function of time, for a) the capacitor and its series resistor and b) the inductor and its series resistor.

Analyzing Fig. 4.4 a), it is possible to conclude that, as soon as the switch closes, almost all of the energy from the input voltage source is dissipated in the resistor (because the voltage across the capacitor is very small). After the capacitor is completely charged, the energy stored in the capacitor is equal to the energy dissipated in the resistor during the charging process. This means that the maximum possible efficiency of charging a capacitor is 50% and that a voltage converter using capacitors should guarantee that the capacitors are always fully charged in order to maximize its efficiency. In order to obtain an output voltage larger than the input voltage, it is necessary to use more than one capacitor. During a first phase, the capacitors are connected in parallel with the input voltage and, during a second phase, the capacitors are connected in series resulting in an output voltage larger than the input voltage (Parallel-Series topology - Section 4.4.5). To maximize the efficiency, the capacitors should reduce the amount of charge that is charged and discharged. Thus, the maximum efficiency is achieved only when the number of capacitors is close to the required voltage ratio between the output and input voltages [109].

Analyzing Fig. 4.4 b), it is possible to conclude that, just after the switch closing, almost all of the energy from the input voltage source is transferred to the inductor (because the current in the inductor is very small). This means that the efficiency is maximum at this time and it decreases as the inductor is charged to the maximum current. Therefore, in order to maximize the efficiency, a voltage converter using inductors should guarantee that the switches are closed for a time smaller than the time constant of the circuit. Also, a voltage converter circuit can use a single inductor to obtain any required output voltage, without losing efficiency.

4.3.1 Voltage step-up circuits

It is always required to have an output capacitor in switched DC-DC converters, in order to filter the high frequency components. In addition, it also serves as an energy storage element to

supply the load while the converter circuit is in a switching phase such that it is not bringing energy from the input to the output.

4.3.1.1 Boost DC-DC voltage converter

Due to the interesting characteristics of inductors, their conjunction with capacitors may benefit the overall efficiency, in the sense that an inductor can be used to charge a capacitor, instead of using a voltage source. This idea serves as the basis for the circuit shown in Fig. 4.5, the Boost (step-up) DC-DC converter.

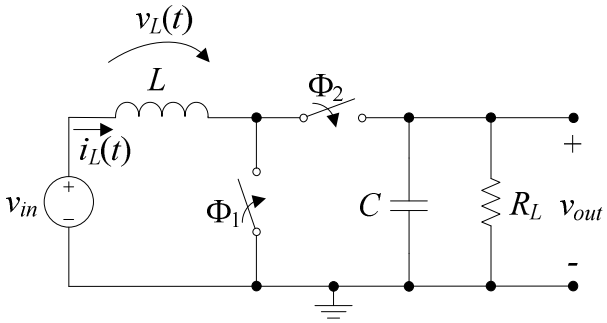


Fig. 4.5 - Boost (step-up) DC-DC voltage converter, using ideal elements.

The principle of operation of this circuit is briefly explained. In continuous conduction mode (CCM), the inductor current $i_L(t)$ has a positive value, different from zero, which occurs according to two clock phases Φ_1 and Φ_2. These two clock phases are non-overlapping, meaning that one phase is the negative logic of the other.

When Φ_1 is active, and its switch is closed (and Φ_2 is not, keeping its switch open), the current i_L increases linearly from its minimum, to a maximum value. During the same time, the output capacitor C discharges through the load R_L.

On the other hand, during the time while Φ_2 is active, and its switch is closed (and Φ_1 is not, keeping its switch open), the inductor L is discharged into C and R_L. This causes i_L to decrease from its maximum value to the minimum value. Moreover, this current is divided, in order to charge C and to supply R_L.

Because the discharge of L is performed in series with the input voltage source v_{in}, the resulting output voltage v_{out} will have a value greater than v_{in}, achieving a voltage elevation.

Let us assume that this circuit is operating in its steady-state, all the electric components contained in it are ideal and have no losses, and the output ripple is negligible (meaning that the output voltage equals its average value and that the ripple in i_L is also negligible). Thus, the energy change in the inductor in a whole period T, is zero. The voltages at the terminals of L,

$v_L(t)$, are v_{in} and $(v_{in} - v_{out})$, for the intervals concerning Φ_1 and Φ_2, respectively, which are denoted by t_1 and t_2, just like depicted in Fig. 4.6.

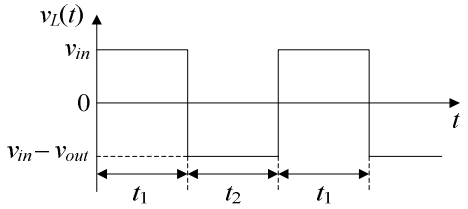


Fig. 4.6 - Ideal voltage $v_L(t)$, as a function of time.

For this reason, across a whole period, its volt-second balance will also be zero, such that

$$\int_0^T v_L(t)\,dt = v_{in}t_1 + (v_{in} - v_{out})t_2 = 0\,. \tag{4.3}$$

By manipulating (4.3), knowing that k is the voltage ratio between the output and the input, and δ is the duty-cycle (given by $t_1 / (t_1 + t_2) = t_1 / T$) one can come to the conclusion that

$$k(\delta) = \frac{v_{out}}{v_{in}} = \frac{t_1 + t_2}{t_2} = \frac{1}{1-\delta}\,. \tag{4.4}$$

This result denotes that the voltage ratio k only depends on the duty-cycle and no other parameter. For instance, to have a voltage doubler, δ must be set to 0.5. In addition, as δ approaches the unit value, the voltage ratio approaches infinity, which will not be physically realizable. Once again, this result is only possible because all the elements in the circuit of Fig. 4.5 are ideal and because of the assumption of a negligible ripple, which can only be true by having L, C and the switching frequency $(1 / T)$ infinitely large. Thus, the explanation that was given only serves to have an idea about the concept involved, although being insufficient for any designing purposes.

Besides the CCM, there is also the discontinuous conduction mode (DCM). This mode of operation considers that the current in the inductor does not flow continuously (both switches in Fig. 4.5 can be open). Although being a possible mode of operation, DCM will not be explained here as it rests outside of the scope of this text. For further information about this subject, [110] can provide a very good detailed insight. In the remaining examples of circuits, it will be considered an operation under a CCM regime and the use of ideal circuit elements.

4.3.1.2 Current-fed bridge DC-DC voltage converter

The Boost converter of Fig. 4.5 is perhaps the most elucidative structure about step-up converters using inductors. However, besides the Boost voltage converter, there are other topologies that also serve as step-up DC-DC converters. The next one being presented is the current-fed bridge, which is shown in Fig. 4.7.

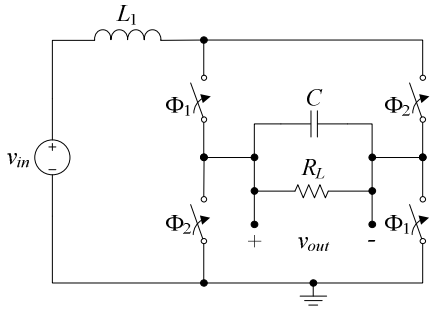


Fig. 4.7 - Current-fed bridge voltage converter.

Under some circumstances, this circuit has the particularity of inverting the polarity of the output voltage, relatively to the input. Without getting into too many details, the mathematical expression of the voltage conversion ratio (VCR) is as follows, making this feature evident.

$$k(\delta) = \frac{v_{out}}{v_{in}} = \frac{1}{2\delta - 1}. \tag{4.5}$$

Thus, if δ is above 0.5 this circuit will be non-inverter, otherwise it will be an inverter. The relation between δ and k is non-linear, and at extreme values of δ (0 and 1), the values of k are -1 and 1, respectively.

4.3.1.3 Inverse Watkins-Johnson DC-DC voltage converter

Another circuit that performs a step-up operation is the inverse Watkins-Johnson DC-DC voltage converter, which is shown in Fig. 4.8.

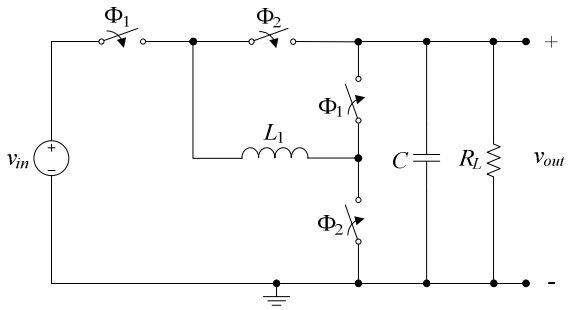


Fig. 4.8 - Inverse Watkins-Johnson DC-DC voltage converter.

The relation between the voltage ratio and the duty-cycle in this circuit is expressed in the following equation.

$$k(\delta) = \frac{v_{out}}{v_{in}} = \frac{\delta}{2\delta - 1}. \tag{4.6}$$

This function also shows that for values of δ below 0.5, the voltage ratio is negative (denoting inversion) and being positive, otherwise. The extreme values that k can assume are 0, at the lower end of δ and 1 at the upper end.

The inverse Watkins-Johnson DC-DC voltage converter can be used under another variant topology, in which, instead of four switches, two switches and two coupled inductors (a transformer) are used. Its behavior is equivalent to the one just described.

As a final remark, about the three step-up topologies that have been addressed, for the same level of output power to be achieved, the one that requires a smaller capacitance (*C*, in each of the topologies shown) to operate, is the Boost converter [110]. Since, in integrated circuits, the area is proportional to the capacitance being used, this is the most suitable converter for integration purposes.

4.3.2 Voltage step-down circuits

It is also possible to use an inductor to reduce the value of the input voltage. The Buck converter is a circuit topology capable of performing this operation and is shown next in Fig. 4.9. Once again, the clock phases are mutually exclusive (non-overlapping).

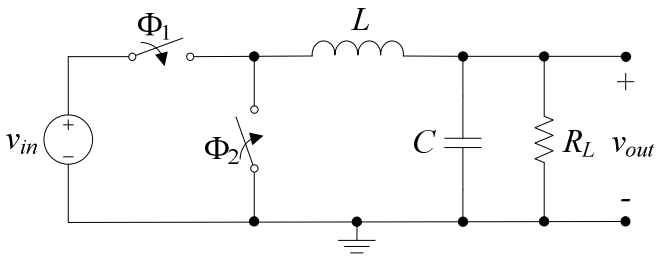


Fig. 4.9 - Buck (step-down) voltage converter.

The difference between this circuit and the step-up converter shown in Fig. 4.5, is that the inductor is now in place of the switch controlled by Φ_2 and vice-versa.

This converter can only reduce the input voltage v_{in}, in order to provide the output voltage v_{out}. The VCR for this circuit is

$$k(\delta) = \frac{v_{out}}{v_{in}} = \delta . \tag{4.7}$$

This means that, in the limit, the output voltage can equal the input voltage, if the switch attached to Φ_1 is closed for the entire time.

There are some other topologies that perform a step-down operation, but as the voltage converter of this research thesis refers to a step-up operation, these will not be further described here, as they do not bring relevant added value. Nevertheless, to general interest and knowledge, some of these voltage converter topologies are the Bridge, the Three-Level Buck, the Buck^2 and the Watkins-Johnson. For further details and explanation about any of these topologies, see [110], for example.

4.3.3 Voltage step-up/down circuits

The next topologies refer to converters that are able to perform stepping-up, as well as stepping-down. The stepping-up feature makes them interesting to be discussed here.

4.3.3.1 Buck-Boost DC-DC voltage converter

The following circuit is the Buck-Boost converter, shown in Fig. 4.10.

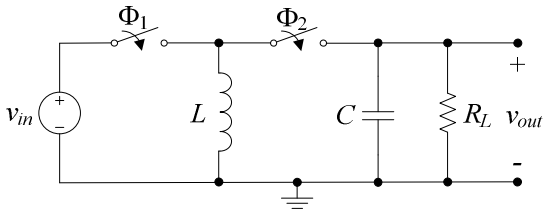


Fig. 4.10 - Buck-Boost voltage converter.

The inductor is part of the input or output loop, thanks to the alternation between Φ_1 and Φ_2, respectively. This circuit is able to step-up or step-down the input voltage, according to the duty-cycle δ that is being used. The VCR is

$$k(\delta) = \frac{v_{out}}{v_{in}} = -\frac{\delta}{1-\delta}. \tag{4.8}$$

From (4.8), it is evident that this topology inverts the polarity of the output voltage, with respect to v_{in}. Moreover, considering only the magnitude of the voltages, if δ does not exceed the value if 0.5, the circuit will work as a step-down converter (buck), while for larger values, it will step v_{in} up (boost).

4.3.3.2 Non-inverting Buck-Boost DC-DC voltage converter

There is another topology with step-up and step-down capabilities, which does not invert the polarity, unlike for the case of the previous one. This is the non-inverting Buck-Boost converter, which is shown in Fig. 4.11.

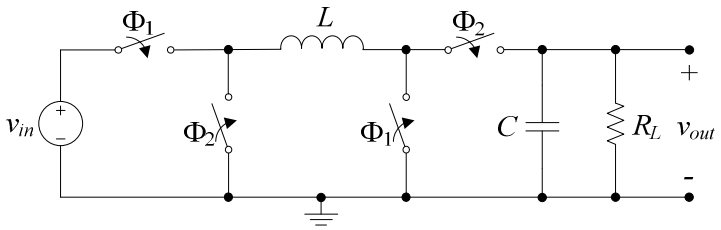


Fig. 4.11 - Non-inverting Buck-Boost voltage converter.

The mathematical expression for the VCR provided by this circuit, is equal to the one of the Buck-Boost converter, but without the negative sign, i.e.

$$k(\delta) = \frac{v_{out}}{v_{in}} = \frac{\delta}{1-\delta}, \tag{4.9}$$

and all the previous considerations that were draw, with regard to the dependence of k with δ, apply here in the same manner.

4.3.3.3 Čuk DC-DC voltage converter

Another topology that has a similar behavior to the Buck-Boost converter is the Čuk converter, which is depicted in Fig. 4.12.

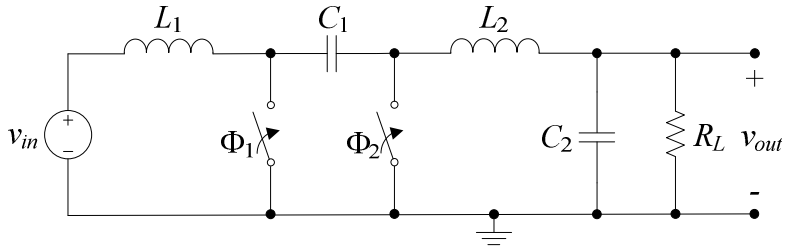


Fig. 4.12 - Čuk voltage converter.

The capacitor C_1 alternates between the input and output, if Φ_2 or Φ_1 is active, respectively. The voltage ratio is exactly like the one in (4.8), but this circuit must have more elements than the one in Fig. 4.10 to achieve the same goal, which is a disadvantage.

4.3.3.4 SEPIC DC-DC voltage converter

Another topology that is worth to mention is the single-ended primary inductance converter (SEPIC), whose circuit can be observed in Fig. 4.13.

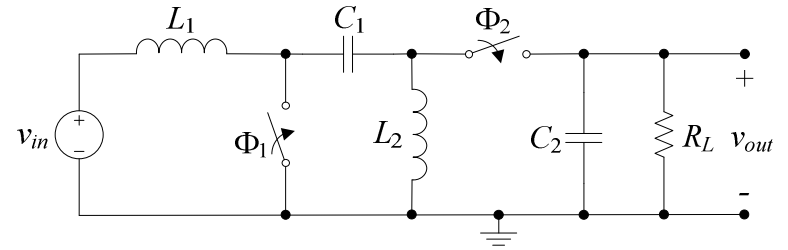


Fig. 4.13 - SEPIC voltage converter.

This circuit is very similar to the Čuk voltage converter, only having L_2 exchanged with the switch controlled by Φ_2. However, this difference in the circuit, makes it not to invert the output voltage, with respect to the input. Thus, the VCR is

$$k(\delta) = \frac{v_{out}}{v_{in}} = \frac{\delta}{1-\delta}. \tag{4.10}$$

4.3.3.5 Zeta DC-DC voltage converter

To complete this set of topologies, which perform a stepping-up operation as well as stepping-down, the Zeta voltage converter is briefly described, and its circuit shown in Fig. 4.14. This converter is also known as Inverse-SEPIC.

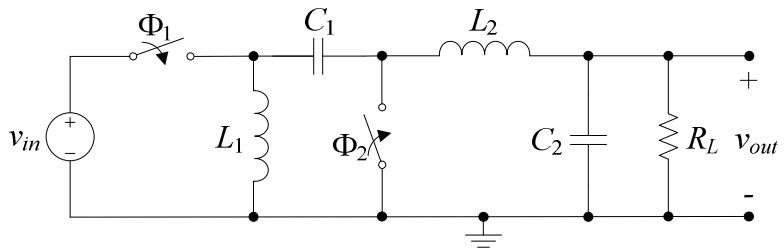


Fig. 4.14 - Zeta voltage converter.

The voltage ratio, as a function of the duty-cycle, is equal to the one of the Non-inverting Buck-Boost converter, shown in (4.9). For an output power greater than 100 mW, it has been shown that the Zeta converter is more suitable for integration, because the total capacitance required by this topology is below the one needed by the other step-up/down topologies [110]. On the other hand, for power levels below 100 mW, the converter that requires the lowest amount of total capacitance is the Non-inverting Buck-Boost.

There are more topologies and variants about the topologies that have been described. However, the discussion about standard topologies using inductors will not be further extended in this text. For a more detailed explanation and supplemental information, see [110] for example. Also, in some of the topologies that have been shown, the switches controlled by the signal Φ_2 could have been replaced by a diode. See, for example, [111].

In [112] a step-up converter is presented, using two boost stages such as the one in Fig. 4.5. However to minimize the use of inductors, one single inductor is shared by both stages according to an implementation of a switch configuration scheme. The overall operation is equivalent to having two inductors, each of them, at each stage, at a time.

The most substantial problem with the voltage converters that use inductors is that the inductance value required by most converters is outside of the range of values that are possible to integrate in CMOS technologies. Therefore, inductor-based voltage converter circuits almost always require a discrete inductor that must be placed outside the integrated system. There are numerous examples of energy conditioning systems based on traditional and more elaborated architectures employing inductors, such as in [42], [81], [112] and [113].

In [114], two approaches that use inductors in a CMOS process, in order to obtain a DC-DC converter completely integrated in CMOS technology are presented. In the first approach,

the inductor is constructed by using bond wires above the integrated circuit. Such an inductor is shown in Fig. 4.15, where one can see it above the silicon die.

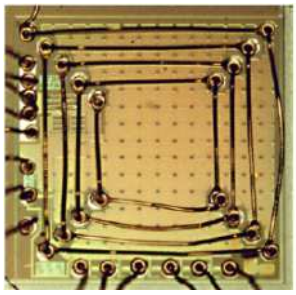
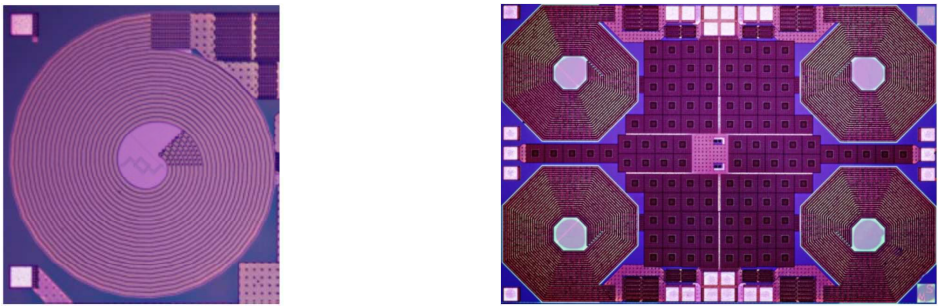


Fig. 4.15 - Prototype of a bond wire inductor, used in a step-up converter [114].

The advantages on using such an inductor are the low series resistance of the wires, the possiblility to have good values of inductance without an increase in the die area, and a low capacitive coupling to the rest of the circuit, as the inductor is above the silicon. However, as the construction is not monolithic, there are intrinsic difficulties in reproducing the device.

Another possible approach is to use an integrated inductor, which may be available in the library of the layout editor software. This type of inductor uses the metals available from the metal stack. However, the resistance of the inductor wire is much higher that the one in the previous case, as well as the capacitive coupling to the rest of the circuit. This device may resemble to the integrated inductor shown in Fig. 4.16 a) and the use of similar devices in an actual monolithic DC-DC converter is depicted in Fig. 4.16 b).



a) b)

Fig. 4.16 - a) Integrated metal track inductor; b) Application of integrated inductors in a layout of a monolithic converter [114].

Given that integrating inductors can be prohibitive in terms of area, other types of solutions exist, so that voltage conversion is achieved without their use. Some of these solutions are based on switched-capacitor (SC) architectures, opening the possibility of fully integrating the voltage converter circuit. A comparative study between inductor- and SC-based conversion technologies is given in [115]. This study concludes that converters based on SC have less losses and that capacitors have a greater energy and power density, when compared to inductors, if small devices are used.

4.4 Switched-capacitors (SC) DC-DC voltage converters

It is possible to have a SC voltage converter circuit entirely built in a CMOS integrated circuit, without the need to have external components. More broadly, SC circuits are used not only for voltage conversion, but also for signal processing, like filtering, programmable gain amplification, and so forth.

As it has been discussed before in Section 4.3, inductor-based converters can achieve high efficiencies. It has also been seen that the operation using capacitors was more prone to have an inferior efficiency.

In general terms, a SC based DC-DC voltage converter consists of two fundamental blocks, as shown in Fig. 4.17.

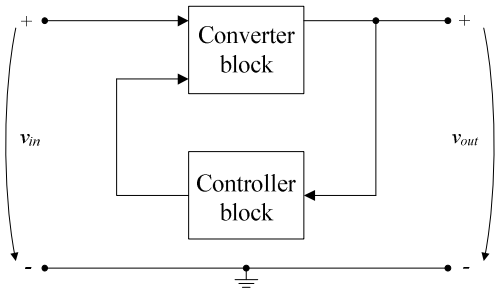


Fig. 4.17 - Main building blocks of a SC DC-DC voltage converter.

The converter block, or power stage, performs the actual voltage conversion, while the controller block dictates how the switches inside the converter block will work to provide for the intended behavior of the converter. The controller block acts over a certain variable of the converter, such as the switching frequency, by monitoring the behavior of the output voltage.

A SC-based converter (as an inductor based converter), is considered as a variable structure system because its structure is repeatedly changed according to the state of the switches. In the converter block, there are two types of capacitors, which are the flying capacitors and the output buffer capacitor. The flying capacitors connect to different nodes in the circuit, transferring charge in accordance to the state of the switches. There can be several states, or phases, to control the action of the switches. However, multi-phase converters are rarely used, and so, having two phases is the most common situation. The use of two phases has already been demonstrated for the inductive converters and it will continue to be used for this discussion about the SC voltage converters. Nevertheless, to have an idea about how a multi-phase voltage converter operates and what it achieves, [116] presents an example.

A parameter that best characterizes a SC voltage converter is its VCR, just like it happened for the case of inductive converters.

The general electric model for the SC-based voltage converter is shown in Fig. 4.18. Should *n* be greater than one, then it will stand for the amount of voltage elevation (VCR), having in this case, a DC-DC voltage step-up converter.

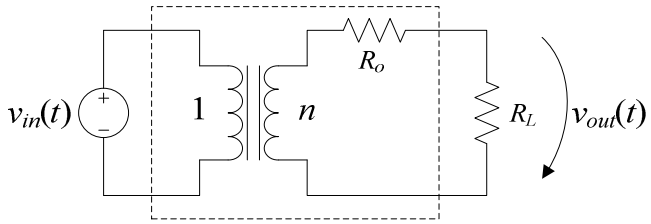


Fig. 4.18 - Electric model of a switched-capacitor DC-DC voltage converter.

The VCR is obtained under no load conditions, and all conversion losses are manifested by a voltage drop associated with non-zero load current through the output resistance R_o. This resistance accounts for capacitor charging and discharging losses and resistive conduction losses. The model in Fig. 4.18 does not take into account some other losses, such as short-circuit currents, parasitic capacitances and gate-drive losses. However, these types of losses can also be incorporated into the model for more completeness.

The output resistance R_o is a frequency dependent variable and has two asymptotic limits: one, where resistive paths dominate the impedance, and another, where charge transfers among idealized capacitors dominate the impedance [117]. These limits are the slow and the fast switching limits, as related to the switching frequency. The slow switching limit (SSL) impedance is calculated assuming that the switches and all other conductive interconnections are ideal, and that the currents flowing between the input and output sources and capacitors are impulsive, modeled as charge transfers. The SSL impedance is inversely proportional to the switching frequency. The fast switching limit (FSL) occurs when the resistances associated with the switches, capacitors and interconnections dominate, and the capacitors act effectively as fixed voltage sources. The details about how the SSL and the FSL are determined and optimized can be found in [117].

There are many different SC converter topologies. In a given topology, the number of flying capacitors can, in most of the cases, tell how much VCR can be achieved, according to the choice about which switches, in a given phase, are to be closed or open. There is a theorem stated in [118], through which it can be predicted which can be the ideal VCR possibilities, given the number of flying capacitors. This theorem is called the “Bounds on Voltage Ratio” and is repeated here, for convenience:

“The realizable conversion ratio of a two-phase switched-capacitor DC-DC converter with a single voltage source V_g is given by a common fraction in the form

$$M_i(k) = \frac{V_o}{V_g} = \frac{P[k]}{Q[k]}, \tag{4.11}$$

where $P[k]$ and $Q[k]$ are integers that satisfy inequalities

$$\begin{aligned} Max[Abs[P[k]], Abs[Q[k]]] &\leq F_k \\ Min[Abs[P[k]], Abs[Q[k]]] &\geq 1 \end{aligned}. \tag{4.12}$$

k is the total number of capacitors, and F_k in k-th Fibonacci number."

At this time, it is worth to remember how the sequence of Fibonacci is. Its general form, $F(n)$, is given by:

$$F(n) = \begin{cases} 0, & \text{if } n = 0 \\ 1, & \text{if } n = 1 \\ F(n-1) + F(n-2), & \text{if } n > 1 \end{cases}. \tag{4.13}$$

Another possible definition is given by:

$$F(n) = \frac{\varphi^n - (1-\varphi)^n}{\sqrt{5}}, \tag{4.14}$$

where φ is known as the golden ratio, defined as $\varphi = (1+\sqrt{5})/2 = 1.6180339887\ldots$. This is the value to how much the ratio, between a number in the Fibonacci sequence, and the number immediately preceeding it, will tend to.

Given this, the Fibonacci sequence results in:

$$F(n) = \{0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, \ldots\}. \tag{4.15}$$

By applying the previous theorem to a given situation, for instance, when having one or two flying capacitors, the results that may be achieved are shown in TABLE 4.1.

TABLE 4.1 - Ideal voltage conversion ratios for switched-capacitor converters with one or two flying capacitors.

Number of flying capacitors	M_i
1	1/2, 1, 2
2	1/3, 1/2, 2/3, 1, 3/2, 2, 3

For example, with two flying capacitors, one will have a total of three capacitors (this includes C_{out}), and the maximum ideal voltage ratio will be the 3rd Fibonacci number, excluding the 0 and the first 1, i.e. 3.

Also in [118], it is stated another theorem that allows for determining how many switches are necessary for a given implementation. This theorem is called "The Number of Switches Required" and just like for the previous theorem, for convenience, this one is also repeated here:

"The number of switches n_s required to realize a maximum attainable voltage ratio $M_{\max}(k)$ with k capacitors is given by

$$n_s\left[M_{\max}(k)\right] = 3k - 2\,. \tag{4.16}$$

For example, when having a voltage doubler using one flying capacitor and an output buffer capacitor ($k = 2$), the number of switches required will equal be $n_s = 4$.

From the various topologies for SC DC-DC voltage converters available from literature, some of them will be shown next and briefly described. Only step-up converters will be shown, because these ones alone are related to the main target of this research thesis. The capacitor C_{out} is the output capacitor that serves as a buffer, or storage, capacitance. It is assumed that this capacitance is much greater than any of the flying capacitors, which have the same value among them. For any explanation that will be given, it is assumed that the circuit is in its steady-state, using only ideal elements, and having no load draining charge from C_{out}.

4.4.1 Voltage step-up converter using the ladder topology

The step-up converter shown in Fig. 4.19 is constructed according to the ladder topology [119]. The ladder topology is based on two rows of capacitors. One set forms a chain from ground, including the input and output voltages. In the case of Fig. 4.19, this set is C_2 and C_4.

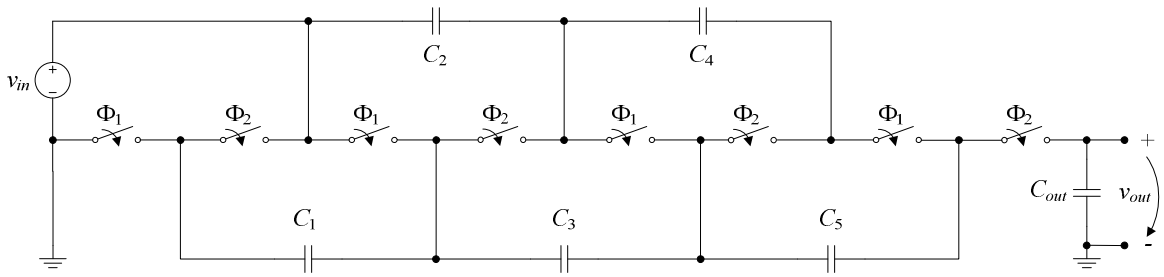


Fig. 4.19 - Switched-capacitor DC-DC voltage step-up converter, using the ladder topology.

These capacitors establish a set of DC potentials at integer multiples of the input voltage. The other set of capacitors, C_1, C_3 and C_5, transfer charge between the DC-referenced capacitors to equalize them. These can be truly designated as flying capacitors. The switches are phased alternately, according to Φ_1 or Φ_2, to connect one set of capacitors to the other, as if they were sliding back and forth. For Fig. 4.19, in the steady-state, every capacitor will be charged to v_{in}, thus when Φ_2 occurs, the path from the input voltage to the output node will make a total of $4\times v_{in}$. Thus, the converter shown in Fig. 4.19 has a VCR of four. Alternatively, the intermediate nodes of the chain of DC-referenced capacitors can be used as outputs, achieving a lower

voltage ratio with respect to v_{in}. Knowing that each capacitor will, in the steady-state, be charged to v_{in}, the resulting VCR can easily by determined by inspection.

All the elements in the structure, except for the output capacitor, are not subjected to a voltage greater than the input voltage value. This fact is particularly important to components that possess a limited voltage capability, which is typical of monolithic integrated circuits.

This structure is very sensitive to stray capacitance, existing between the voltage nodes and the substrate of the chip, affecting the efficiency of the converter. This distributed parasitic capacitance is charged and discharged in each switching period, resulting in the loss of the charge commited to it. If this capacitance did not exist, a high efficiency could be achieved when the system is operating in the steady-state. This condition is valid for every switched-capacitor voltage converter.

For the given topology, in general, having a total of n capacitors (except for the output storage capacitor), the VCR will be:

$$\frac{v_{out}}{v_{in}} = \frac{n+3}{2}. \tag{4.17}$$

This expression is only valid for ladder circuits similar to the one in Fig. 4.19. Such a circuit can be further expanded with similar stages to the right-hand side. Each stage must comprehend one DC-referenced capacitor, one flying capacitor, and two switches controlled accordingly, to complete the structure. In this case, the circuit will operate under the same principles just stated, and (4.17) will apply. Naturally, these stages must be put before C_{out}.

However, considering the following circuit in Fig. 4.20, the only difference between this one and circuit of Fig. 4.19, is the fact that v_{in} now connects to the node between C_2 and C_4.

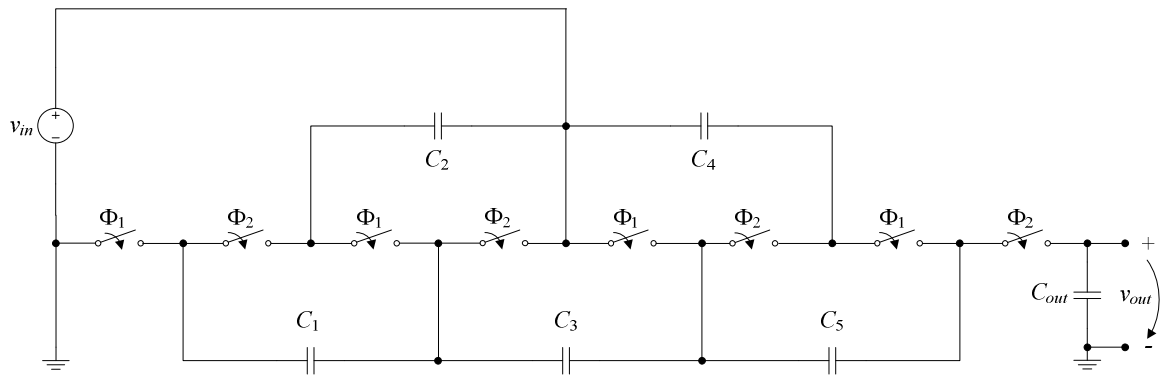


Fig. 4.20 - Ladder step-up converter, with lower VCR.

This has a major impact with respect to the former circuit because now, at the terminals of each capacitor in the circuit, instead of having a voltage with the same value as v_{in}, one has a voltage with a value of $v_{in}/2$. Thus, when Φ_2 occurs, the path from the input voltage to the output node will make a total of $v_{in} + v_{in}/2 + v_{in}/2 = 2 \times v_{in}$. Equivalently, the VCR is now equal to two, which is half of the one of the circuit in Fig. 4.19. In the present situation, the capacitors in the structure can be rated to cope with half of the voltage that they are expected to have in the circuit of Fig. 4.19.

In order to determine the VCR for this circuit, given that to each capacitor corresponds a voltage of $½ \times v_{in}$, the value determined by (4.17) should be multiplied by the same factor that multiplies v_{in} at each individual capacitor. What is being done, when changing the circuit of Fig. 4.19 to the one of Fig. 4.20, is to set an intermediate node voltage in the path of the DC-referenced capacitors, consequently affecting the voltage in the other nodes. This kind of procedure opens the possibility to have fractional voltage conversion ratios. If v_{in} is further displaced to the right-hand side of C_4, instead of the node between C_2 and C_4, each capacitor will develop at its terminals a voltage of $v_{in}/3$, and when Φ_2 occurs, the path from the input voltage to the output node will make a total of $v_{in} + v_{in}/3 = 1.3(3) \times v_{in}$, yielding a VCR of 1.3(3). Under the same line of thought, in the following circuit of Fig. 4.21, each capacitor will also get at its terminals a voltage of $v_{in}/3$, meaning that, in the given situation, the VCR will be equal to 1.6(6).

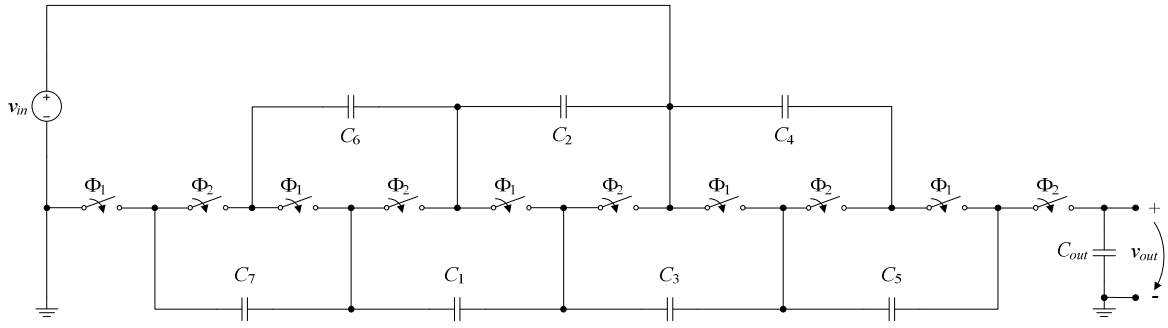


Fig. 4.21 - Ladder step-up converter, with a different VCR, for comparison.

When using the circuit of Fig. 4.21, if the voltage source is connected at different nodes of the upper row of capacitors, from left to right the voltage conversion ratios that can be achieved are 5, 2.5, 1.6(6) (already mentioned), and 1.25, respectively. Thus, it can be concluded that, in each of these four situations, each individual capacitor (except for C_{out}) will achieve at its terminals a voltage value of v_{in}, $v_{in}/2$, $v_{in}/3$ and $v_{in}/4$, respectively.

4.4.2 Voltage step-up converter using the Cockcroft-Walton topology

The converter, shown next in Fig. 4.22, uses the Cockcroft-Walton topology.

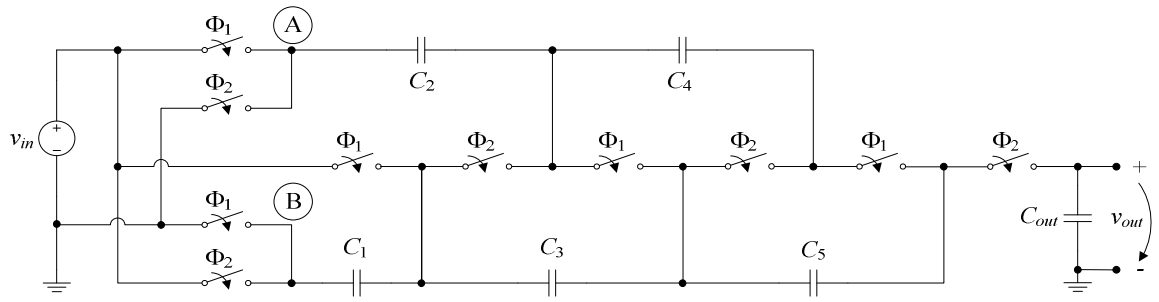


Fig. 4.22 - Switched-capacitor DC-DC voltage step-up converter, using the Cockcroft-Walton topology.

The name of this topology comes after the physicists John D. Cockroft and Ernest T. S. Walton had used it to generate very high voltages for their particle physics experiments [120].

It can be seen that this topology has a similar structure to that of Fig. 4.19. However, in Fig. 4.22, both ladders move relatively to ground. The pairs of extra switches, at the left hand side, cause each ladder to move up and down an amount equal to the input voltage. This causes that the ladder steps are in multiples of twice the input voltage, because they move in opposite directions. This is an important difference relatively to the ladder topology, which achieved steps with only the same magnitude as v_{in}. Thus, in the steady-state, with the exception of C_1, which gets a voltage value equal to v_{in}, every capacitor in the ladders will get at its terminals a voltage with twice the value of v_{in}. Following the path from the input voltage to the output node will make a total of $6\times v_{in}$. Thus, the converter shown in Fig. 4.22 has a VCR of six. It is to note that this topology suffers from the same problem as the ladder topology, with respect to the stray capacitance, when implemented in an integrated circuit. In addition, with the exception of C_1, now all the capacitors in the ladders must be rated to undergo a minimum voltage of $2\times v_{in}$.

Given how this converter works, the VCR can be inferred as being:

$$\frac{v_{out}}{v_{in}} = 2\times N \ , \tag{4.18}$$

with N standing for the number of capacitors in the bottom ladder shown in Fig. 4.22.

4.4.3 Voltage step-up converter using the Dickson charge pump topology

Another very well-known topology, which has been proposed in 1976 by Dickson, is the Dickson charge pump [121]. The basic circuit of this topology is shown in Fig. 4.23.

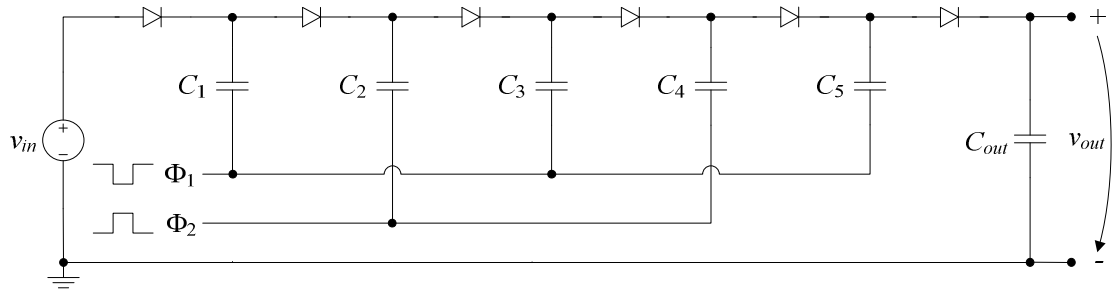


Fig. 4.23 - Dickson charge pump step-up converter basic topology.

One of the first uses that this circuit had was in the process of erasing and writing non-volatile solid-state memories, in order to elevate the voltage to a level sufficient enough to perform those operations. This need led to the first development of on-chip voltage elevators.

A very important characteristic of this circuit is its reduced sensitivity to stray parasitic capacitance. The diodes in this circuit are usually made with MOSFETs connected as diodes, so their threshold voltage must be taken into account for the determination of the output voltage. When reverse biased, each diode is subjected to a voltage of about the same value as v_{in}. However, the capacitors, going from left to right in Fig. 4.23, are subjected to $2\times v_{in}$, $3\times v_{in}$, $4\times v_{in}$, $5\times v_{in}$ and $6\times v_{in}$ (including C_{out}), respectively. It is assumed that the magnitude of the square wave signals (Φ_1 and Φ_2) that switch capacitors C_1 to C_5 has the same value as v_{in}.

In order for this topology to operate efficiently, the voltage drop across the diodes must not have an important expression in the total output voltage. This means that this circuit will become more efficient as the intended output voltage is higher.

Using a very simplistic approach, in which it is considered that the voltage drop across the diodes and the parasitic capacitances along the string of diodes are negligible, there is no load draining charge from C_{out} and the operating frequency is such that the capacitors get fully charged, the VCR of the Dickson charge pump can be expressed by:

$$\frac{v_{out}}{v_{in}} = n+1, \tag{4.19}$$

in which n is the number of capacitors in the charge pump circuit (excluding C_{out}), which are all assumed to have the same value of capacitance. This means that the converter shown in Fig. 4.23 has a conversion ratio of six.

According to [117], another way to implement a Dickson charge pump is by adapting the Cockcroft-Walton topology, like in the circuit shown in Fig. 4.22. This can be achieved by connecting the left plate of each of the capacitors in the top row to the node identified as A, and also by connecting the left plate of each of the capacitors in the bottom row to the node

identified as B. It is to note that such a circuit will not require diodes, having these been replaced by switches, which close or open in the right phase, just like the diodes in the circuit of Fig. 4.23 do, according to the phase signals.

There are improved versions of the Dickson charge pump, in which the effect of the threshold voltage of the diodes is decreased through the use of alternative topologies to implement them, as well as other improvements [122].

4.4.4 Voltage step-up converter using the Fibonacci topology

Another kind of circuit construction, which is shown in Fig. 4.24, is according to the Fibonnacci topology [123], [124].

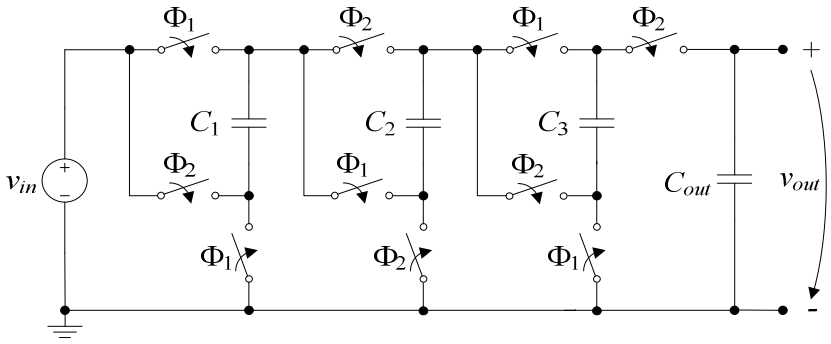


Fig. 4.24 - Switched-capacitor DC-DC voltage step-up converter, using the Fibonacci topology.

This topology has the merit of achieving the highest VCR, for a given number of capacitors, of any of the two-phase topologies.

In Fig. 4.24, it can be seen that the circuit is composed by three cells, each containing one capacitor and three switches. From one cell to its adjacent, the phases are switched in opposition.

This kind of converter has a VCR such that, having a circuit with *n* flying capacitors, this value is:

$$\frac{v_{out}}{v_{in}} = F(n+2)\,. \tag{4.20}$$

This refers to the (*n*+2)-*th* number in the Fibonacci sequence, previously presented in (4.15), considering that the first number is at index 0 (0-*th*). Thus, the converter shown in Fig. 4.24, with three flying capacitors, has a VCR of five, because looking at (4.15), the number at index 5 (considering that the first number is at index 0), is five.

4.4.5 Voltage step-up converter using the Parallel-Series topology

The following topology is the Parallel-Series [124], whose circuit is shown in Fig. 4.25.

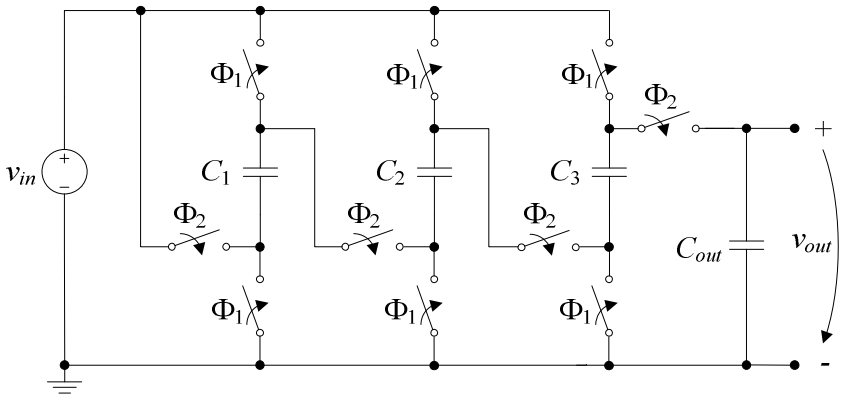


Fig. 4.25 - Switched-capacitor DC-DC voltage step-up converter, according to the Parallel-Series topology.

This is perhaps the most straightforward topology, because one can easily infer about the VCR, just by a direct inspection of the circuit, regarding the number of flying capacitors. Thus, in the case of the converter depicted in Fig. 4.25, its VCR is equal to four.

The name of this topology derives from the form by which the flying capacitors are connected among themselves and with the input voltage source. In the first phase (Φ_1), all of the flying capacitors, along with the input voltage source, are connected together in parallel. This causes that, at the terminals of this parallel connection, there is a voltage determined by the input source v_{in}, which charges all the capacitors. In the second phase (Φ_2), all of the flying capacitors are connected in series with v_{in}. Since every individual capacitor has now, at its terminals, a voltage equal to the value of v_{in}, by establishing the referred configuration, between the ends of the whole series circuit, one will have the input voltage, in addition to a replica of this voltage at the terminals of each capacitor in the series. Thus, the total output voltage is obtained by series discharging the capacitors, achieving a value of $v_{out} = (n + 1) \times v_{in}$, which is held by the output buffer capacitance C_{out}, which is only connected in this phase.

To summarize, if the circuit has n flying capacitors, for the Parallel-Series topology, the VCR will be:

$$\frac{v_{out}}{v_{in}} = n+1 . \tag{4.21}$$

4.4.6 Voltage step-up converter using the Voltage Doubler topology

The topology that follows corresponds to the voltage doubler [124], as shown in Fig. 4.26.

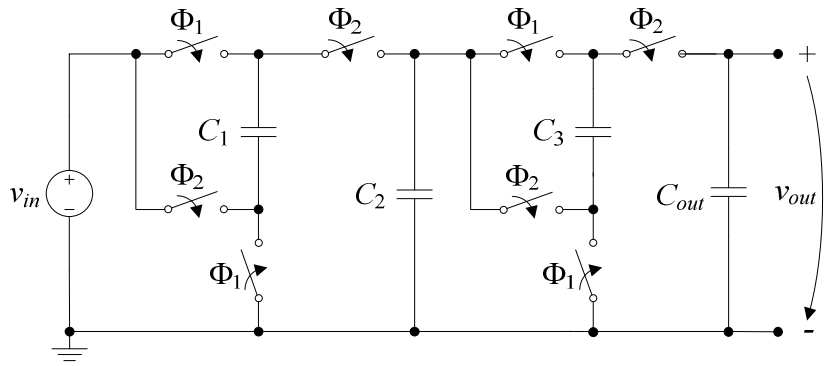


Fig. 4.26 - Switched-capacitor DC-DC voltage step-up converter, using the voltage doubler topology.

This topology consists of cascading similar voltage doubling blocks. Each individual block is of the same kind as the ones used in the Parallel-Series topology. However, between every two of these blocks there is a capacitor, serving as a DC bypass capacitor, which does not get directly switched like the flying capacitor in each individual doubling block. In Fig. 4.26, this capacitor is C_2.

Having a converter with k stages like the ones mentioned, thus concerning to a circuit involving $2k - 1$ capacitors (except for C_{out}), the VCR is

$$\frac{v_{out}}{v_{in}} = 2^k \,. \tag{4.22}$$

This means that from one stage to next, the voltage is consecutively multiplied by two, and the resulting charge is stored in the buffer DC capacitor. Thus, at the output v_{out}, one has a version of v_{in} multiplied by a power of two. In the case of the circuit in Fig. 4.26, since there are two cascaded doubler stages, the converter has a VCR of four.

One interesting thing to note about all of the converters that have been presented is that, if the input voltage source and the output capacitor exchange positions between them, the new value of the obtained conversion ratio, regarding the voltage at the terminals of the output capacitor versus the voltage of the input source at their new positions, is the inverse of the original value. This means that, if this exchange is performed for each of the converters shown above, they will operate as voltage step-down converters with voltage conversion ratios equal to the inverse of the values that were given above.

In [125], it is presented a study about the amount of integrated die area that some of the topologies that have just been presented need to have, according to the number of stages required for a given application. This study concludes that the Dickson, Parallel-Series and Fibonacci topologies are equivalent from an area cost point of view. On the other hand, the voltage doubler topology is inferior from this same point of view.

The topologies that have been shown do not have the concern to match their input impedance with the output impedance of the source providing the input voltage, because it has been assumed that this voltage source is ideal. However, when this is not the case, and especially when the output impedance of the input voltage source is variable, the frequency must be adjusted so that this match is achieved. By having a good match between these two impedances, the converter can extract the maximum power from the input source. In the explanations given for the topologies that were shown, it has only been considered that the frequency was such that the capacitors could fully charge, having no other requirements, such as the one just mentioned.

These converters can reach high efficiencies, but the efficiency value will be greater as the level of involved power, or voltage, is also greater. Especially, when dealing with micro-power harvester systems, the limited available energy makes the converter efficiency issue even more critical. One of the biggest problems, in terms of efficiency, is the bottom plate capacitance associated to every capacitor [42], [117].

Among the various topologies already shown, the Parallel-Series, performs an elevation of the input voltage, according to the number of capacitors involved [117], [124], [125] and, in general, this topology shows a good performance. For this reason, the SC converter used in the present thesis work is based on this type of topology, performing an elevation of two fold the input voltage. To be more precise, the present system implements a dual-branch SC voltage doubler. A voltage doubler whose base is according to the same principle can be found in [126]. This will be further explained in Chapter 5.

To overcome the performance limitations related to the bottom plate parasitic capacitance, [127] proposes some configurations that try to minimize the amount of charge that is lost. Also, in [17] another technique is employed in order to minimize the bottom plate capacitance loss. This same technique is further used in the system in which this entire work is focused on, trying to attain efficiencies as high as possible. In general, when dealing with SC converters performance studies, work can be found in [128] and [129].

4.5 Energy storing devices

Once the energy has been conveniently harvested and conditioned, some means must be used to store that energy, so that it can be used at a later time. The only circumstances that would not require for this class of devices would have to be such in which there was an uninterruptable flow of ambient energy. In real systems, this condition cannot be guaranteed.

For a small system, there are two storing devices available, batteries and supercapacitors, which can be used to perform this task [4]. Depending on the energy usage profile of the system, any of the previous devices can be used in accordance. However, to optimize their utility and lifetime, each must fit into the appropriate energy usage regime [82]. Moreover, if appropriate, the two different types of devices can be used to store energy in the same application, having the purpose to extend the lifetime of each other. Each device requires special attention, as their particular characteristics involve very specific charging strategies [78], [82]. A brief summary of the main issues found in literature for these devices will be presented next.

4.5.1 Batteries

A rechargeable battery is a storage cell that can be charged by reversing the internal chemical reaction. Batteries are used when large energy density is required. However, their lifetime is seriously affected by the number of charging/discharging cycles that they experience. As such, trying to minimize the number of these cycles is an important objective. This aspect is related to the amount of time that a battery can remain in operation, so that the stored charge can hold for as long as possible. An example of a work concerning such an issue is presented in [130].

There are various common types of rechargeable batteries, for instance, Sealed Lead Acid (SLA), Li+/Li–polymer (Lithium-ion / Lithium polymer), NiMH (Nickel Metal Hydride) or NiCad (Nickel Cadmium). Typical operating voltages for these kinds of battery technologies can be approximately 1.2 V for the last two types, 3.7 V for the second type [6] and 6 V for the first type [93]. Actually, conventional Li-ion batteries have a typical operating voltage that ranges from 2.7 V to 4.2 V [35].

The parameters that characterize batteries are weight energy density, power density, charge-discharge efficiency, self-discharge rate and number of deep recharge cycles.

Charge-discharge efficiency is the ratio of energy stored into the battery to the energy delivered by the battery, self-discharge is the loss of battery capacity while it is stored without being used, and deep recharge cycle refers to the cycle of recharging the battery after a complete drain-out.

In TABLE 4.2, a comparison about the various battery technology types, regarding some important parameters, is presented.

The data contained in this table allows for verifying that both Li-ion, and Li-polymer, show the best weight energy density, volume energy density, charge-discharge efficiency and self-discharge rate, besides having no memory effect. Batteries showing this latter effect have a loss of energy capacity due to repeated partial recharges.

TABLE 4.2 - Comparison of recheargable battery technologies [93].

Battery Type	Nominal Voltage (V)	Capacity (mAh)	Weight Energy Density (Wh/kg)	Power Density (W/kg)	Efficiency (%)	Self Discharge (%/month)	Memory Effect?	Charging Method	Recharge Cycles
SLA	6	1300	26	180	70-92	20	No	Trickle	500-800
NiCd	1.2	1100	42	150	70-90	10	Yes	Trickle	1500
NiMH	1.2	2500	100	250-1000	66	20	No	Trickle	1000
Li-ion	3.7	740	165	1800	99.9	<10	No	Pulse	1200
Li-polymer	3.7	930	156	3000	99.8	<10	No	Pulse	500-1000

SLA batteries are the heaviest, most volumous and the ones that possess the least number of recharge cycles. Their nominal voltage is the highest among the types shown, which may be useful in some applications requiring higher supplying voltages. However, by stacking a series of batteries of any of the other types, higher supplying voltages can also be provided.

There are some emerging technologies using materials like $LiCoO_2$ or graphite, that in conjunction with PVDF-Ionic (poly vinylidene fluoride - Ionic) electrolyte, have already given promising results, just like technologies based on other types of materials and electrolytes [37].

If it is intended to use Lithium-ion or Lithium-polymer batteries, their charging process is not trivial, so a specific charging circuit is often used. This circuit is especially designed to guarantee that there is not any overcharging or over discharging that could cause damage to the battery or even set it on fire [78]. Thus, these battery technologies are demanding with respect to this issue. The role of the circuit that controls the charging process is also to guarantee that the battery is provided with a high pulsating charging current. This is why the charging method in TABLE 4.2, for the Li-ion or Li-polymer types, is referred to as pulse charging. In addition to the controlling circuit, an auxiliary battery can be used to provide the charge for the current charging pulses.

The other battery technologies only require that batteries are trickle charged. Trickle charging means that the batteries can be directly connected to an energy source, without requiring any complex circuits controlling the charge by current pulses.

As it can be seen from TABLE 4.2, all technologies have advantages and disadvantages, which must be weighted according to the final application requirements and deployment conditions.

Besides being electric charge buffers, batteries serve as voltage stabilizers, providing a constant voltage at the output of the regulator circuit. Examples of harvesting systems that make use of batteries to store harvested energy can be found, for instance, in [15] and [131].

In order to have an example of how rechargeable batteries may look like, the following picture, extracted from [132], helps to illustrate the actual device.

Fig. 4.27 - An example of a commercially available Li-on rechageable battery [132].

The dimensions of such a devive can be fairly reduced, like 5.8 mm × 31 mm × 52 mm (thickness × width × length), representing the Ultralife UBP053048, one of the devices present in [132].

4.5.2 Supercapacitors

Supercapacitors (or ultracapacitors), are also known as electric double-layer capacitors (DLC). These exhibit particular characteristics that make them different from ordinary capacitors. The DLC consists of activated carbon particles that act as polarizable electrodes. These strongly packed particles are immersed in an electrolytic solution forming a double-layer charge distribution along the contact surface between carbon and electrolyte. The electrical model of a supercapacitor is not simply a high valued capacitor, but instead, a set of several branches with different time constants [133]. Such a model is depicted next in Fig. 4.28.

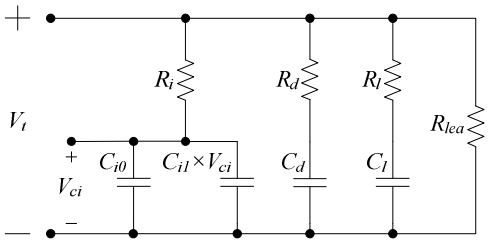


Fig. 4.28 - Equivalent circuit model for a double layer capacitor.

This model is based on the electrochemistry of the interface between two materials in different phases, so that the double layer charge distribution, of differential sections of the interface, is modeled as a series *RC* circuit. The resistive element represents the resistivity of the materials forming the double-layer charge distribution, mainly the resistivity of the carbon particles. The capacitive element represents the capacitance between the two materials, which are carbon and electrolyte. According to [134], in supercapacitors, the electric charge stored at a metal or electrolyte interface is exploited to construct a storage device. The high content of energy stored by supercapacitors comes from activated carbon electrode material, having an extremely high surface area and a short distance of charge separation created by the opposite

charges in the interface between electrode and electrolyte. This is schematically shown in Fig. 4.29.

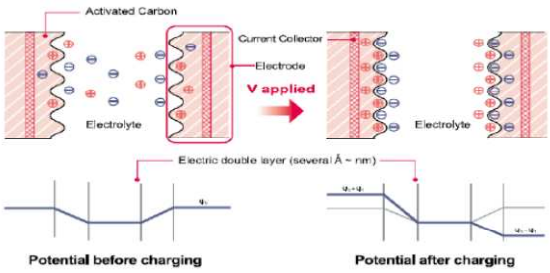


Fig. 4.29 - Working principle of the supercapacitor [134].

Randomly distributed ions in electrolyte move toward the electrode surface of opposite polarity under an electric field when charged. This is a purely physical phenomena rather than a chemical reaction and hence, it is an easily reversible process, which is shown in Fig. 4.30.

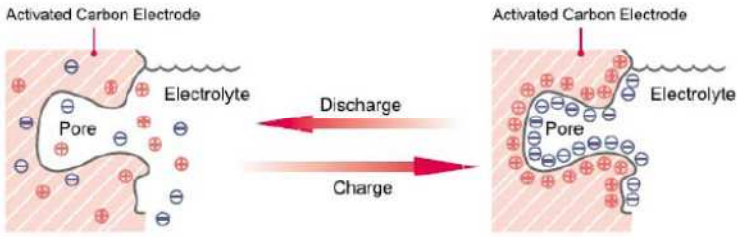


Fig. 4.30 - Charging and discharging mechanism of a supercapacitor [134].

These features result in high power, high cycle life, long shelf life, and in a maintenance-free product.

Although the physical definition could indicate a large number of *RC* time constants describing the microscopic physical structure of the DLC, the electric behavior can be reduced to that of the circuit in Fig. 4.28. These time constants can model how the device behaves, in response to the application of a voltage at its terminals.

The model shown in Fig. 4.28 tries to keep the number of branches to a minimum (for practical reasons), includes an existing non-linear relation between capacitance and terminal voltage in only one of the branches, and also includes the effect of self-discharge. However, in the practical voltage range of the device, the DLC capacitance varies linearly with the capacitor terminal voltage.

Each of the three branches has a distinct time constant differing from the others in more than an order of magnitude. In Fig. 4.28, starting from left, the first branch is called the immediate branch. It contains elements R_i and C_{i0}, as well as the voltage-dependent capacitor (identified as C_{i1}, whose units are in F/V), which depends from V_{ci}. This branch dominates the immediate behavior of the DLC in the time range of seconds, in response to a charging action.

The second is the delayed branch, with parameters R_d and C_d, which dominates the behavior of the device in the range of minutes. The third is the long-term branch, with parameters R_l and C_l. It determines the behavior for times longer than 10 minutes. To reflect the voltage dependence of the capacitance, the first branch is modeled as a voltage-dependent differential capacitor. The differential capacitor consists of a fixed capacitance C_{i0} and a voltage-dependent capacitor $C_{i1} \times V_{ci}$. In the fourth branch, a leakage resistor R_{lea}, in parallel with the terminals of the model, represents the self-discharge property. The total voltage at the terminals of the model is V_t.

For a typical supercapacitor with 470 F, according to the authors of [133], the values for the model parameters are: R_i = 2.5 mΩ, C_{i0} = 270 F, C_{i1} = 190 F/V, R_d = 0.9 Ω, C_d = 100 F, R_l = 5.2 Ω, C_l = 220 F and R_{lea} = 9 kΩ. Further details on such a model can be found in the same reference. Capacitance values of commercially available supercapacitors can be as high as 3000 F [135].

These devices stand a higher number of charge/discharge cycles than batteries can, being suited for applications where this kind of regime is usual. The number of these cycles can be as high as a million, leading to an operational lifetime of ten years, until the capacitance value starts to show some degradation [3]. One very appealing factor about supercapacitors is that they do not require specific charging circuits, being able to stand trickle charging.

Supercapacitors are inexpensive, making them very appealing to use in opposition to batteries, as these are more expensive. Moreover, as seen by TABLE 4.2, there are only a few typical voltage ratings for batteries, depending on the technology being used. With supercapacitors, these ratings are much more diverse, similarly to regular capacitors. This factor is also important, not only because of the end application, but also because it can result in a smaller device, if a lower voltage rating is allowed.

In order to have an idea of how these electronic components may look like, the following picture shows some supercapacitors adequate for using in energy harvesting applications.

Fig. 4.31 - Examples of commercially available supercapacitors (50 F, 10 F and 1 F).

The biggest supercapacitor in this picture has a capacitance of 50 F, although for a maximum voltage rating of 2.3 V. It must be taken into account that, for typical low-power energy harvesting applications, the size of the whole system is intended to be small. As such, although capacitance can reach values as high as 3000 F, for practical small sized applications, due to body size restrictions, the supercapacitors to be used must have lower capacitance values, as well as their voltage rating. The ones in Fig. 4.31 are an example of adequate devices.

An example of a discrete system that makes use of a supercapacitor to store harvested energy from a solar harvester can be found in [14].

Nonetheless, there are some applications that use both a battery and a supercapacitor [6], [82]. These act as a primary and secondary energy buffers, respectively. In addition, the use of batteries helps to get a more stabilized output voltage, thanks to their intrinsic plateau value, as it was already mentioned. This is confirmed in [134].

4.6 Maximum Power Point Tracking (MPPT) techniques

4.6.1 Introduction

There are some limiting factors when building a light energy powered micro sensor system, such as a low energy budget, due to size limitations. This budget must comprehend the energy needed for the controlling circuits to operate, in order to maintain the interaction between the energy processing system and the harvester at an optimum level [82].

To enable the system to maximize, as much as possible, the energy obtained from the PV cells, there is a set of techniques known as Maximum Power Point Tracking (MPPT), which can be used to achieve this goal. If the PV cells operate in a way such that the MPP is always tracked, it will effectively contribute to the performance of the system, since a charging device can be storing energy at the maximum rate that the harvester can possibly provide. If one is even able to use a smaller PV cell, this strategy can ultimately contribute to a reduction of size and cost of the system, while keeping the same performance, when compared to a system where the MPP is not tracked. The use of MPPT techniques, although not mandatory for an energy harvesting application based on PV cells, is highly recommended. This is because it maximizes the chance of seizing the most of the energy that is made available from the environment and that, otherwise, would simply be wasted. This strategy allows for an increase of the harvested energy in about 65% to 90% [4].

According to the models that describe the various types of harvesters, given the ambient energy sources that were previously presented in Chapter 2, every device has a MPP. Although

this section is focused on the subject of tracking of the MPP of PV cells, there are also MPPT applications in literature concerning other sources. For example, regarding TEG, work can be found in [136], on mechanical (piezoelectric) applications, [9] documents some work regarding it, on RF energy harvesting, one has [137] as an example, and on the subject of MPPT when using MFC as energy harvesters, [138] presents a novel approach. However, as the main theme of this research thesis is concerned about light energy, the MPPT of PV cells is the one that will receive the entire attention, being the remaining types of sources outside of the scope of the present discussion.

Some techniques make it possible to manipulate the PV cell position, in order to maximize the light intensity on its surface [139]. This is done by using a mechanism that tries to place the PV panel facing the Sun all the time, by following its position. So, part of the harvested energy is used to put the mechanism to work, which may involve a large amount of energy. In small systems, however, this option is not valid because of both the low power and the low cost budgets and it is preferable not to have any moving parts. The set of MPPT techniques described next, refer to strategies that maximize the amount of electrical power obtained from PV cells under these conditions.

A substantial set of MPPT techniques can be found in the survey made in [86], and some work can be found in [140]-[142] regarding solar panels. Most of the MPPT techniques presented in [86] were developed for large PV arrays that provide hundreds or thousands of Watts. These systems can refer to applications in DC, which [143] is an example, while some others refer to applications in AC, like in [144]. In some cases, the techniques in [86] can be extended to very low power systems, at the scale of μW or mW. The available power being considered for the application in this thesis is at the μW level. This may cause that some of the algorithms in [86] may not be usable. As such, a careful criterion must be taken to choose the appropriate MPPT method, so that the controller can be kept to an acceptable power overhead. As already has been done with other topics concerning this work, as the entire set of issues regarding these techniques is relatively extense, only a brief overview of the main classes of techniques will be given next.

On the other hand, it can also be found in literature some work that, although referring the use of an MPPT technique, in fact the tracking feature is not present. These techniques are supported on setting the working point of the PV cell on its maximum power point, by clamping the voltage at the cell terminals, to a value that is very close to the one determined as being the voltage at which the MPP is reached. Since the voltage is clamped, there is not any chance to track the MPP, if the illumination or temperature conditions change. These techniques are very

simple to implement, but they can only be useful if the environmental conditions are known beforehand and known to have very little changes. For example, in [12], [26], [78], [79], [100] or [145], this technique is used, with the main argument is that in indoor environments the light does not change its pattern enough to demand the use of any tracking technique of the MPP of the PV cell. Although this may be true for some situations and applications, it limits the versatility of the system, forcing it forever to restrict its applicability to indoor environments only. Most of the systems that are tailored to work indoors have the voltage coming from the PV cell clamped to a value that is known beforehand to be in the vicinity of the MPP. Other systems are simply connected directly to the PV panel, usually by means of a diode to prevent reverse current, like in [26], [78], [79] or [100]. Examples of other works according to the principles just outlined can be found in [7], [88] and [146]. This thesis is focused on indoor light energy harvesting, but this principle was not followed and the implemented MPPT method provides an effective tracking of the MPP, enabling the system to operate indoors or outdoors.

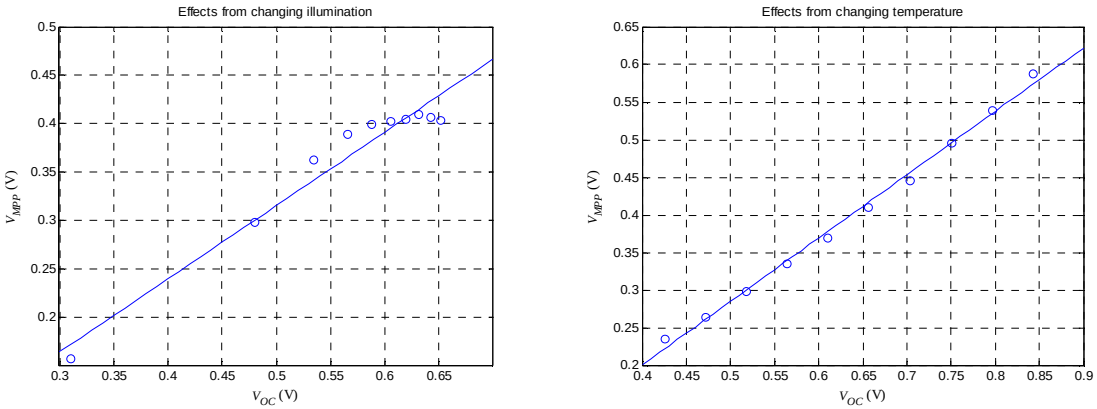
4.6.2 Quasi-MPPT techniques

This type of algorithms cannot reach the true MPP of a PV cell. However, since the power value does not change significantly from the maximum value around its vicinity, this is not a significant problem. The Fractional Open Circuit Voltage (Fractional V_{OC}) method requires the prior determination of the characteristics of the PV cell. The open circuit voltage can be obtained by using a pilot PV cell, smaller than the main cell, exposed in the same way as the latter. The circuitry needed to implement the Fractional V_{OC} method is very simple and dissipates little power, at the cost of producing an approximation of the MPP of the PV cell. This trade-off can be acceptable for a micro-power system.

This method explores the intrinsic property of PV cells, such that the MPP is within the range of 0.71 to 0.78 of the open circuit voltage [86]. This is the value that will be given to the constant k in the following equation:

$$V_{MPP} \cong k \cdot V_{OC} \,. \tag{4.23}$$

The value of k is normally set by using a resistive voltage divider. Work based on this MPPT method can be found in [13] and [140]. In this latter reference, it is shown the procedures to experimentally determine the value of k. The same procedures were followed to determine this coefficient for the PV cell whose curves have been shown in Fig. 2.19 b) as example. This factor must be determined beforehand, by studying the PV cell behavior under several conditions of illumination and temperature. The model of the PV cell was simulated under different conditions and showed the performance depicted in Fig. 4.32.



a) b)

Fig. 4.32 - Fractional open circuit voltage relation between V_{OC} and V_{MPP} under various conditions of a) illumination and b) temperature.

By performing a linear regression (first order approximation) over the points plotted on the obtained graphs, in the same way as in [13], one can determine the slope of these functions. By sweeping a range of temperatures that spanned from –55 ºC to +125 ºC, the ratio was around 0.84. By sweeping illumination from 10% to 100%, the ratio was about 0.76. Assuming that illumination has more importance, as it is more likely to have a bigger variation, a value of 0.77 was selected for *k*, the Fractional V_{OC} coefficient. This value agrees with the ones in [86].

As previously stated, in the case of a micro-power step-up converter, it is possible to tolerate some inaccuracy in the determination of the MPP, in exchange for using a simpler method for determining the MPP of the PV cell that requires less complex circuits and dissipates less power. However, over time, it may be needed to tune the fractional open circuit constant to account for the changes that the PV panel will suffer with aging, for example. The action of the MPPT method over a SC voltage converter will be on the operating frequency. In a capacitor based voltage booster circuit, it is necessary to fully charge the capacitors. This means that the duration of each clock phase must be larger than the *RC* time constant of the circuit. Therefore, a change in the duty-cycle does not change the behavior of the circuit, unlike in the case of an inductor-based converter. Thus, the action of the circuit, in order to control the tracking of the MPP, is by changing the clock frequency alone. More details can be found ahead in Chapter 5.

The class of quasi-MPPT techniques also encompasses some other methods that will not be further explored in this text, but that are worth to be mentioned. As such, in addition to the "Fractional V_{OC}" technique, there is also the "Fractional I_{SC}", which is based on the short circuit current of the PV cell, the "DC link capacitor droop control", the "Load *I* or *V* maximization", the "Array reconfiguration" method, the "Linear current control", the "One-cycle control (OCC) MPPT", the "Best fixed voltage (BFV)" and the "Linear reoriented coordinates method

(LRCM)". The summarized details about any of these methods can be found in [86]. For a truly detailed explanation, the references that can be found in [86] regarding their respective methods, will provide the reader with the necessary depth of detail and information.

4.6.3 True MPPT techniques

These techniques are concerned with obtaining and tracking the actual MPP of the PV cell, independently of light and temperature conditions. This accurate estimation is often based on microcontroller computation [14], requiring the use of an ADC. In general, these MPPT techniques do not need to know the PV cell characteristics in advance, as the converter system adapts itself automatically to the given PV cell. Examples of such techniques include algorithms like the Hill Climbing, used in [14], [15], [131], [147] and [148], and the Ripple Correlation Control (RCC), used in [141]-[143] and [149]. Both of these algorithms can also be implemented using analog circuits, thus reducing the power needed to operate. RCC is possibly the best MPPT method, but requires a multiplication to compute the value of the instantaneous power. Since an analog multiplier is difficult to design and typically dissipates a large amount of power, the RCC method is not suitable for micro-power systems. The Hill Climbing algorithm can have convergence problems if the light intensity changes rapidly. However, according to [150], the Hill Climbing MPPT is one of the less energetic and cost demanding techniques, when compared to the others. This appealing factor was a major motivation to use this MPPT technique in subsequent experiments concerning this thesis work, as it can be found in more detail in Appendix D. The energy consumption is very important, and it has been shown that this algorithm is suited for applications where, specifically, the energy budget is highly restrictive. Basically, this method explores the perturbation in the current provided by the PV cell due to switching. This also perturbs its voltage, and it can be determined in which direction it should go. By looking at the power curve of Fig. 2.19 b), it can be seen that, on the left-hand side of the MPP, incrementing (decrementing) the operating voltage increases (decreases) the power and when operating at the right-hand side of the MPP, the behavior is the opposite. Thus, if there is an increase in power, the next perturbation should be kept in the same direction to reach the MPP and if there is a decrease in power, the perturbation should be reversed. The algorithm is summarized in TABLE 4.3.

TABLE 4.3 - Summary of the Hill Climbing algorithm.

Perturbation	Change in power	Next perturbation
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

The process of determining the “Next perturbation” is repeated periodically until the MPP is reached. The system then oscillates around the MPP. This oscillation can be minimized by reducing the perturbation step size, at the cost of slowing down the MPPT process.

By looking at the right-hand column of TABLE 4.3 (“Next perturbation”), the relation to the “Perturbation” and the “Change in power” variables is according to a logic XNOR function, observable in Appendix D, where further details are given with respect to this MPPT method.

The class of true MPPT techniques includes some other methods that will not be further explained in this text, but that can be mentioned, should the reader wish to explore any of them. So, in addition to the “Hill Climbing” and the “Ripple correlation control (RCC)” techniques, there is also the “Perturb and observe (P&O)”, which is very similar to the Hill Climbing technique, the “Incremental conductance (IncCond)”, the control based on Fuzzy Logic and on Neural Networks, the “Current sweep” method, the “dP/dV or dP/dI feedback control”, the “I_{MPP} & V_{MPP} computation”, the “State-based MPPT” and the “Slide control”. Once again, the summarized details about any of these methods can be found in [86], as well as some references for each of them, for an in-depth explanation with the necessary level of detail and information.

4.6.4 Critical analysis

The choice about which MPPT technique should be used depends on the complexity of the implementation, and which knowledge does the user has in order to implement a solution which is based on analog or digital circuitry. An analog solution mostly requires a printed circuit board (PCB) with the necessary components, or the layout of the needed module, when directly implemented on a silicon die, if the whole system is to be integrated. The latter is the approach taken in this research thesis. On the other hand, a digital solution will include a microcontroller or a DSP, significantly increasing the power dissipation of the MPPT algorithm.

The number of required sensors is also something that affects the decision about which technique to choose. The physical variables that can be sensed are essentially voltage and current, because in some methods, the true amount of power must be computed. However, it is preferable to sense voltage, because current sensors are usually expensive and bulky. There are methods that, instead, make use of irradiance and temperature sensors, such as the “I_{MPP} & V_{MPP} computation”. Particularly, the irradiance sensor is more uncommon. On the other hand, the “Best fixed voltage (BFV)” method does not involve any sensors.

The existence of local maxima in the MPP search can be a serious issue. When a series of PV panels is partially shaded by vegetation or buildings, this is common to happen. Instead of having the typical power curve like that of Fig. 2.19 b), this curve gets deformed as if several of

these curves were superimposed, but displaced from one another, with the individual maxima at distinct levels (see [151], for example). This means that a considerable amount of power can be lost if the system is stuck at a local maximum, instead of the real MPP. The “current sweep” and the “state-based” methods can track the true MPP even in the presence of local maxima.

With respect to costs, the analog implementations are generally less expensive, because these demand only the necessary hardware, unlike in digital implementations, where there is all the overhead associated to the development system and software. When implemented in an integrated circuit, the feature that best quantifies cost is the area occupied by the MPPT system.

Finally, the end application where the PV cell is to serve, can dictate which method to choose. For example, in space applications, where there is no chance of direct intervention to tune the system, the preferred method should be able to continuously track the true MPP, even if more expensive means are needed. Some techniques that could be used towards this objective are the “perturb and observe (P&O)”, “incremental conductance (IncCond)”, “ripple correlation control (RCC)” or the “Hill Climbing”. As another example, in applications where the speed of convergence to track the MPP is important, these could use the “Fuzzy logic control”, “Neural network” or “RCC” techniques. If a low energy budget is available, a simpler technique must be used, such as the “Hill Climbing” or the “Fractional V_{OC}”.

To summarize the MPPT methods addressed in [86], TABLE 4.4, extracted from the same reference, allows for having a comparison among those methods, regarding several important aspects, which may help the designer to choose the most suitable method, according to the needs and to the available resources.

TABLE 4.4 - Major characteristics of MPPT techniques [86].

MPPT Technique	PV Array Dependent?	True MPPT?	Analog or Digital?	Periodic Tuning?	Convergence Speed	Implementation Complexity	Sensed Parameters
Hill-climbing/P&O	No	Yes	Both	No	Varies	Low	Voltage, Current
IncCond	No	Yes	Digital	No	Varies	Medium	Voltage, Current
Fractional V_{OC}	Yes	No	Both	Yes	Medium	Low	Voltage
Fractional I_{SC}	Yes	No	Both	Yes	Medium	Medium	Current
Fuzzy Logic Control	Yes	Yes	Digital	Yes	Fast	High	Varies
Neural Network	Yes	Yes	Digital	Yes	Fast	High	Varies
RCC	No	Yes	Analog	No	Fast	Low	Voltage, Current
Current Sweep	Yes	Yes	Digital	Yes	Slow	High	Voltage, Current
DC Link Capacitor Droop Control	No	No	Both	No	Medium	Low	Voltage
Load I or V Maximization	No	No	Analog	No	Fast	Low	Voltage, Current
dP/dV or dP/dI Feedback Control	No	Yes	Digital	No	Fast	Medium	Voltage, Current
Array Reconfiguration	Yes	No	Digital	Yes	Slow	High	Voltage, Current
Linear Current Control	Yes	No	Digital	Yes	Fast	Medium	Irradiance
I_{MPP} & V_{MPP} Computation	Yes	Yes	Digital	Yes	N/A	Medium	Irradiance, Temperature
State-based MPPT	Yes	Yes	Both	Yes	Fast	High	Voltage, Current
OCC MPPT	Yes	No	Both	Yes	Fast	Medium	Current
BFV	Yes	No	Both	Yes	N/A	Low	None
LRCM	Yes	No	Digital	No	N/A	High	Voltage, Current
Slide Control	No	Yes	Digital	No	Fast	Medium	Voltage, Current

4.7 Conclusions about this chapter

In this chapter, the major focus was on the issue of voltage step-up converters, although the subjects like energy storing devices and MPPT techniques have also been addressed.

Some of the presented topologies can also step the input voltage down, only depending on the duty-cycle of the phase signals. However, the main emphasis rests in the SC voltage step-up converters. Some known topologies have been presented and summarily described. The topology that was chosen to implement the step-up converter in the project of this research thesis is the Parallel-Series converter, using one flying capacitor. Thus, this configuration works as a voltage doubler. The analysis and the design of the actual doubler circuit will be presented in detail in Chapter 5.

The class of devices that can be used to store the energy that has been harvested is a point of concern and thus, this theme has also been addressed. Batteries and supercapacitors, and their technologies, have been presented.

Finally, the issue of MPPT was addressed. This aspect is particularly important in any PV system, so that the maximum power can be extracted from the harvester. There are true and quasi-MPPT methods. The latter are not as accurate as the former, but in general, are simpler to implement and the power overhead needed by the controller is lower. This is especially important in systems with a very low energy budget, which is the case of the present application. As such, the Fractional V_{OC} method has been chosen because of its favorable characteristics. Its operation, under the context of the phase controller of the voltage step-up circuit will be detailed in Chapter 5.

It was shown that, in some systems, these do not use a MPPT method, and instead, the harvested energy is conveyed directly into a supercapacitor. Choosing a supercapacitor is easy to understand, as the circuits that control the charging of batteries are typically more complex.

The energy stored in the supercapacitor may be provided to a circuit that wakes up whenever the voltage level goes above a certain upper threshold. While this circuit is being powered, the voltage at its terminals will progressively drop. Nonetheless, while the provided voltage is still above a lower voltage threshold, the system will remain in the awaken state, being put to sleep only when this limit is reached. Afterwards, the system will go to sleep, while the supercapacitor is being replenished and its charge is not enough to provide a voltage as high as the upper voltage threshold. As an example, consider that a 1 F supercapacitor was charged to 1.3V and then allowed to power a circuit until its voltage decreases to 1.1V. The energy supplied by this discharging capacitor is $E = ½ \times C \times \Delta V_{out}^2$, in this case 0.02 J. This energy

could be used to power a 20 mW transmitter circuit for 1 second, which is enough time, in most cases, to transmit a useful amount of information. In addition, this approach also serves to condition the value of the output voltage.

A similar approach, but acting over the input voltage, is used in [146], for example. The technique being used consists of setting the input voltage of the converter, such that the latter is allowed to bounce inside an interval where the MPP is most likely to be. Although simple to implement, this is not really a MPPT technique, since that under strong light variation, the MPP can move to outside this tolerance window.

Chapter 5

PROPOSED ENERGY HARVESTING SYSTEM

5.1 Introduction

The block diagram, and architecture, of the complete energy harvesting system proposed in this research thesis, is shown next, in Fig. 5.1.

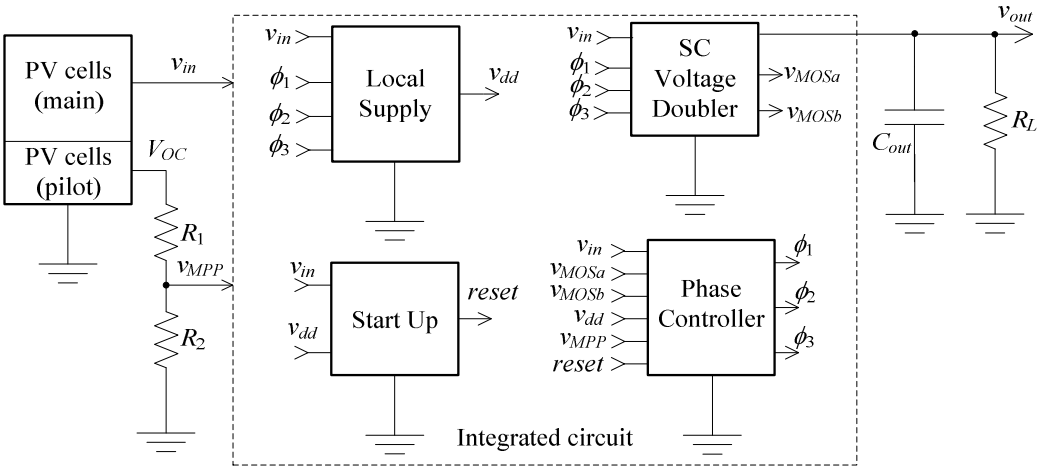


Fig. 5.1 - Architecture of the indoor light energy harvesting system.

Each module in the integrated circuit will be described in this chapter. This description will include the various stages of the design, such as the analysis and the sizing of the devices.

As depicted in Fig. 5.1, the modules that make up the system inside the integrated circuit are: the SC Voltage Doubler, the Local Supply, the Start Up and the Phase Controller blocks. In addition, although not represented in Fig. 5.1, there is also a Voltage Limiter module, acting over the output voltage, preventing it to increase above a certain limit. During the experimental evaluation of the manufactured prototype, this module was powered-down because the generated output voltage was always below the level that would lead it to intervene. As such, in order not to increase the dissipated power, this module was kept OFF and it was not included in Fig. 5.1. However, the details about it will also be presented in this chapter. Each of these modules were laid out using a 130 nm CMOS technology, and integrated into a single silicon die prototype. The CMOS process has one polysilicon layer and eight metal layers.

The Phase Controller module, which generates the phase signals necessary for the SC Voltage Doubler to operate, also implements a MPPT method. Thus, this module is further designated as Phase Controller or MPPT controller. As explained in Chapter 4 - Section 4.6.2, the chosen MPPT method is the Fractional V_{OC}. For prototyping purposes, the voltage divider that determines the value of k of the Fractional V_{OC} MPPT method, as of (4.23), was implemented using an external potentiometer because this allows for more freedom when testing the system and it also allows it to work with different PV cells, if necessary. This voltage divider, as well as the output storage capacitor and the PV cells, were the only devices not included into the integrated circuit. All the rest is fully integrated. In a final system, the only external components that are expected to exist are the small PV panel and a supercapacitor to serve as an energy storing device. This kind of approach is different from others found in literature, as these consist of systems that are not confined to a single integrated circuit. Examples of such systems, consisting of PCB boards, can be found in [7], [13], [14], [27] or [100]. Previously reported indoor light energy harvesting systems are not integrated into a single die, such as [7], [12], [26], [77]-[79], [100] or [145]. In [77], a MPPT method is used to maximize the power provided by the PV cell and to enable the system to operate in environments other than indoors.

Nonetheless, there can also be found examples of fully integrated systems, but whose strategy is different from the one intended for the present work. Examples can be found in [15], [28], [47], [89], [131] or [147].

5.2 SC Voltage Doubler

In order to eliminate the added cost and volume of the system due to an external inductor ([8], [9], [26], [152] and [153]), it was decided to use a SC voltage doubler. The operation of this

circuit is as follows: during phase ϕ_1, the switched-capacitor is charged to the input voltage value (v_{in}) and, during phase ϕ_2, it is connected in series with the input voltage source. This results, ideally, in an output voltage (v_{out}) two times larger than the input voltage. This is exactly the same operation already seen for the Parallel-Series SC voltage step-up converter (see Section 4.4.5), or one SC Doubler module (Section 4.4.6).

A simplified schematic of the step-up converter circuit is depicted in Fig. 5.2, in order to illustrate its concept. This schematic also includes an equivalent switched parasitic capacitor (C_p), representing the load created by the operation of the phase controller circuit that produces the phase signals ϕ_1 and ϕ_2. The PV cell is linearized, and the circuit of Fig. 2.19 a) is replaced by its Thévenin equivalent circuit (v_S and R_S). C_{in} represents the parasitic capacitance of the PV cell (see Appendix B - Section B.2).

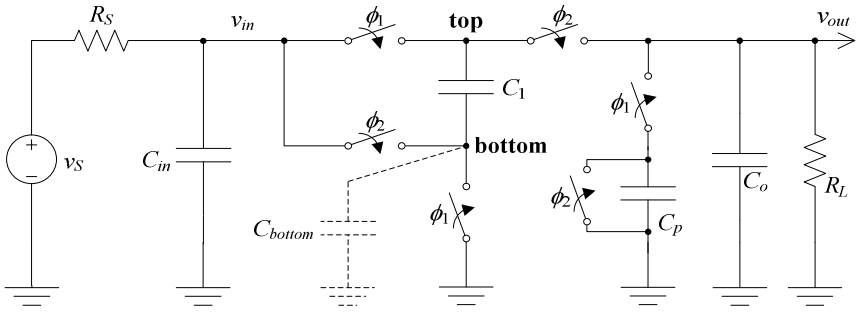


Fig. 5.2 - Simplified schematic of the voltage step-up doubler converter, including the loading caused by the phase controller circuit (modeled as C_p).

At the beginning of phase ϕ_1 (Fig. 5.3), capacitor C_1 is connected between node v_{in} and ground, resulting in a charge redistribution between C_1 and C_{in}, and extra charge flowing through R_s into these two capacitors (i_{in}).

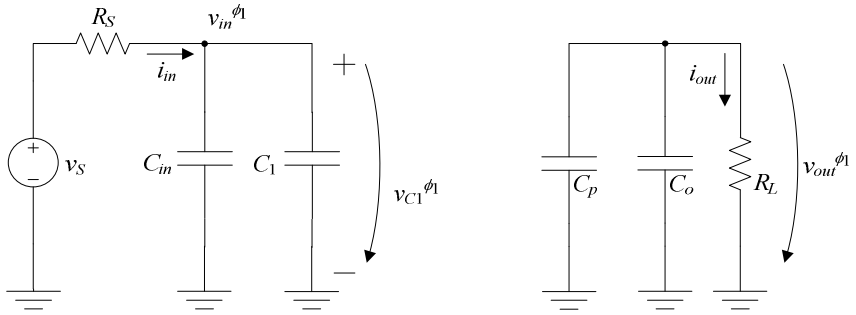


Fig. 5.3 - Circuit during phase ϕ_1.

Voltage v_{in} changes exponentially during phase ϕ_1. Assuming that $T_{CLK} << R_S \times C_{in}$ allows for considering that current i_{in} changes linearly instead of exponentially and, assuming that $T_{CLK} >> R_{ON} \times C_1$ (where R_{ON} is the ON resistance of the switches), allows for considering that the charge redistribution between C_1 and C_{in} is instantaneous. These approximations result in

voltage v_{in} changing instantaneously at the beginning of phase ϕ_1 and then changing linearly during phase ϕ_1. Similarly, assuming that $T_{CLK} << R_L \times C_o$, results in voltage v_{out} also changing linearly during phase ϕ_1. Applying these assumptions to the circuit during phase ϕ_2 (Fig. 5.4), also results in the same variations for the circuit's voltages.

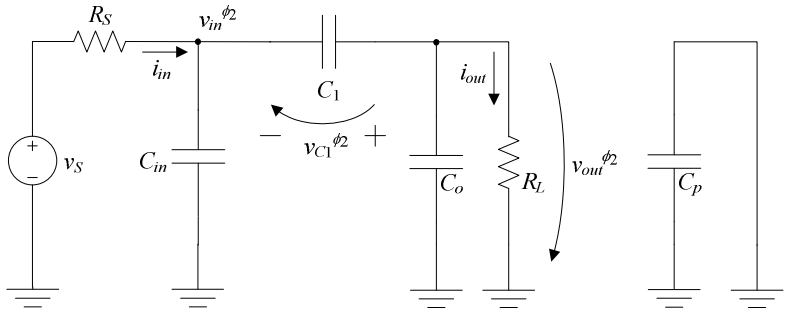


Fig. 5.4 - Circuit during phase ϕ_2.

This means that it is only necessary to calculate the values of the circuit's voltages at the end of each phase, resulting in a discrete-time analysis of the circuit. This is done using conventional switched-capacitor circuit analysis techniques [154] (Chapter 5). The charge in each capacitor is calculated at the end of each clock phase, designating each of these time instants by: $n \times T_{CLK}$ (phase ϕ_1), $(n - ½) \times T_{CLK}$ (phase ϕ_2) and $(n - 1) \times T_{CLK}$ (phase ϕ_1).

When the circuit changes from phase ϕ_1 (Fig. 5.3) to phase ϕ_2 (Fig. 5.4), observing node v_{in}, the charge in the top plates of C_1 and C_{in} at $(n - 1) \times T_{CLK}$, plus the charge coming through R_S during ϕ_1, is equal to the charge in the top plates of C_1 and C_{in} at $(n - ½) \times T_{CLK}$. The charge coming through R_S can be calculated using the average value of the voltage at node v_{in} during phase ϕ_1. A similar analysis can be applied to node v_{out} and then repeated when the circuit changes from phase ϕ_2 to ϕ_1. This results in the set of equations of (5.1):

$$\begin{cases} -C_1 v_{in}[n-1] + C_{in} v_{in}[n-1] + \dfrac{T_{CLK}}{2} \dfrac{v_S - \frac{1}{2}\left(v_{in}[n-1] + v_{in}\left[n-\frac{1}{2}\right]\right)}{R_S} = C_{in} v_{in}\left[n-\frac{1}{2}\right] + C_1\left(v_{in}\left[n-\frac{1}{2}\right] - v_{out}\left[n-\frac{1}{2}\right]\right) \\ C_1 v_{in}[n-1] + C_o v_{out}[n-1] - \dfrac{T_{CLK}}{2} \dfrac{\frac{1}{2}\left(v_{out}[n-1] + v_{out}\left[n-\frac{1}{2}\right]\right)}{R_L} = C_o v_{out}\left[n-\frac{1}{2}\right] - C_1\left(v_{in}\left[n-\frac{1}{2}\right] - v_{out}\left[n-\frac{1}{2}\right]\right) \\ -C_1\left(v_{in}\left[n-\frac{1}{2}\right] - v_{out}\left[n-\frac{1}{2}\right]\right) + C_{in} v_{in}\left[n-\frac{1}{2}\right] + \dfrac{T_{CLK}}{2} \dfrac{v_S - \frac{1}{2}\left(v_{in}\left[n-\frac{1}{2}\right] + v_{in}[n]\right)}{R_S} = C_{in} v_{in}[n] + C_1 v_{in}[n] \\ C_o v_{out}\left[n-\frac{1}{2}\right] - \dfrac{T_{CLK}}{2} \dfrac{\frac{1}{2}\left(v_{out}\left[n-\frac{1}{2}\right] + v_{out}[n]\right)}{R_L} + 0 = C_o v_{out}[n] + C_p v_{out}[n] \end{cases} \quad (5.1)$$

By solving this set of equations, it is possible to obtain the expressions for the sampled input and output voltages, $v_{in}[n]$ and $v_{out}[n]$, respectively. After full simplification, the following expressions are obtained:

$$v_{in}[n] = k_{in}\,(\alpha_{in}\,v_{in}[n-1] + \beta_{in}\,v_{out}[n-1] + \gamma_{in}\,v_S)$$

$$\begin{aligned}
\alpha_{in} &= (4C_oR_L + T_{CLK})(T_{CLK} - 4C_{in}R_S)^2 + 16C_1^2R_S(4(C_{in}+C_o)R_LR_S + (R_L+R_S)T_{CLK}) + \\
&\quad + 4C_1(4C_{in}R_S - T_{CLK})(4(C_{in}-2C_o)R_LR_S - (R_L+2R_S)T_{CLK}) \\
\beta_{in} &= -16C_{in}R_S(2C_1R_S(T_{CLK} - 4C_oR_L)) \\
\gamma_{in} &= 16C_{in}R_ST_{CLK}(4(C_1+C_o)R_L + T_{CLK}) \\
k_{in} &= \frac{1}{(4(C_1+C_{in})R_S + T_{CLK})((4C_oR_L + T_{CLK})(4C_{in}R_S + T_{CLK}) + 4C_1(4(C_{in}+C_o)R_LR_S + (R_L+R_S)T_{CLK}))}
\end{aligned} \tag{5.2}$$

$$v_{out}[n] = k_{out}\,(\alpha_{out}\,v_{in}[n-1] + \beta_{out}\,v_{out}[n-1] + \gamma_{out}\,v_S)$$

$$\begin{aligned}
\alpha_{out} &= 32C_1R_LC_{in}R_S \\
\beta_{out} &= (4C_oR_L - T_{CLK})(4(C_1+C_{in})R_S + T_{CLK}) \\
\gamma_{out} &= 8C_1R_LT_{CLK} \\
k_{out} &= \frac{4C_oR_L - T_{CLK}}{(4(C_o+C_p)R_L + T_{CLK})((4C_oR_L + T_{CLK})(4C_{in}R_S + T_{CLK}) + 4C_1(4(C_{in}+C_o)R_LR_S + (R_L+R_S)T_{CLK}))}
\end{aligned} \tag{5.3}$$

The previous equations describe a second order system. This system has a transient response to the variations of either v_S or R_L. After a certain time, this response ends and the system enters in the steady-state condition. From this instant on, the voltages of the circuit in the previous clock cycle are equal to the ones in the current clock cycle ($V_{IN} = v_{in}[n] = v_{in}[n-1]$ and $V_{OUT} = v_{out}[n] = v_{out}[n-1]$), resulting in the following expressions, after full simplification:

$$V_{IN} = \frac{T_{CLK}\left(4\left(C_o\,C_p + C_1\left(C_o + C_p\right)\right)R_L + \left(C_1 + 4\,C_o + C_p\right)T_{CLK}\right)v_S}{16\,C_1\,C_o\,C_p\,R_L\,R_S + 4\left(C_o\,C_p\,R_L + C_1\left(C_o + C_p\right)R_L + C_1\left(4\,C_o + C_p\right)R_S\right)T_{CLK} + \left(C_1 + 4\,C_o + C_p\right)T_{CLK}^2} \tag{5.4}$$

$$V_{OUT} = \frac{2\,C_1\left(4\,C_o\,R_L - T_{CLK}\right)T_{CLK}\,v_S}{16\,C_1\,C_o\,C_p\,R_L\,R_S + 4\left(C_o\,C_p\,R_L + C_1\left(C_o + C_p\right)R_L + C_1\left(4\,C_o + C_p\right)R_S\right)T_{CLK} + \left(C_1 + 4\,C_o + C_p\right)T_{CLK}^2} \tag{5.5}$$

Voltage V_{IN}, given by equation (5.4), is the steady-state value of the voltage in node v_{in} (it is to note that the steady-state voltage is called V_{IN}, while the instant node voltage is called v_{in}). Voltage v_{in} changes throughout the clock period. Its value, at the end of phase ϕ_1, in the steady-state condition, becomes constant, i.e. the voltage value of v_{in} repeats periodically at each clock cycle. That constant value is given by equation (5.4). The same considerations can be drawn to V_{OUT}, given by (5.5).

The previous expressions show that, for example,

$$\lim_{(C_p,R_S,R_L)\to(0,0,\infty)} V_{IN} = v_S \tag{5.6}$$

and

$$\lim_{(C_p,R_S,R_L)\to(0,0,\infty)} V_{OUT} = 2\times v_S\,, \tag{5.7}$$

as expected from the circuit.

In addition, the ratio between the voltages in (5.4) and (5.5) can also be calculated. This ratio stands for the VCR which, after full simplification, has the following expression:

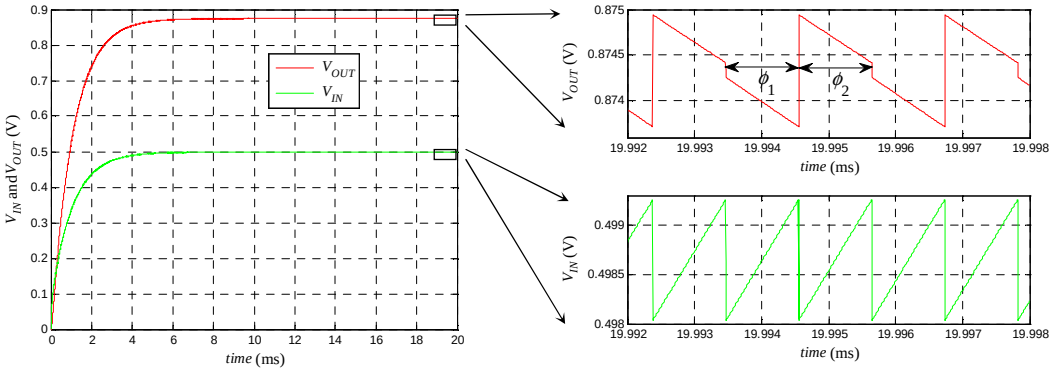
$$\mathrm{VCR} = \frac{V_{OUT}}{V_{IN}} = \frac{2C_1(4C_oR_L - T_{CLK})}{4(C_oC_p + C_1(C_o + C_p))R_L + (C_1 + 4C_o + C_p)T_{CLK}}. \tag{5.8}$$

This expression can also be verified, by calculating its limit under the same conditions as for the cases of (5.6) and (5.7). Thus,

$$\lim_{(C_p, R_S, R_L) \to (0,0,\infty)} \mathrm{VCR} = 2, \tag{5.9}$$

which is the value expected for an ideal voltage doubler circuit.

The circuit of Fig. 5.2 was simulated in Spectre, using ideal circuit elements and different values for C_{in}, C_1, C_o, C_p, R_L and T_{CLK}. The steady-state voltages of the circuit in these simulations were measured, and these values were well within the range of 1% of the values predicted by expressions (5.4) and (5.5). For instance, using for the given parameters the values of v_S = 1 V, R_S = 4 kΩ, R_L = 16 kΩ, C_{in} = 110 nF, C_1 = 1.1 nF, C_p = 20 pF, C_o = 110 nF and $1/T_{CLK} = f_{CLK}$ = 459.1 kHz the resulting voltages were as shown next in Fig. 5.5, in which there are also indicated the intervals concerning to the phase signals ϕ_1 and ϕ_2.



a) b)

Fig. 5.5 - a) Time evolution of voltages V_{IN} and V_{OUT} with f_{CLK} = 459.1 kHz and R_L = 16 kΩ and b) Close-up of voltages V_{IN} and V_{OUT} in the steady-state zone.

The reason why the parameters had the specific values that were used in this simulation will be explained later, in Section 5.3.2.1. Fig. 5.5 a) shows the evolution of voltages V_{IN} and V_{OUT} over time, since the moment the converter starts working, until it settles into the steady-state.

Another simulation has been run, in order to confirm the validity of the expressions shown in (5.4) and (5.5), keeping the parameter values already given, except for the operating frequency and for the load resistor. Their new values are f_{CLK} = 200 kHz and R_L = 110 kΩ. The resulting voltages are shown next in Fig. 5.6.

In Fig. 5.6 a), it can be observed that the transient behavior has a longer duration than that of the previous simulation. This is explained by the fact that, in this situation, the operating frequency is lower, thus the system takes longer to reach the steady-state.

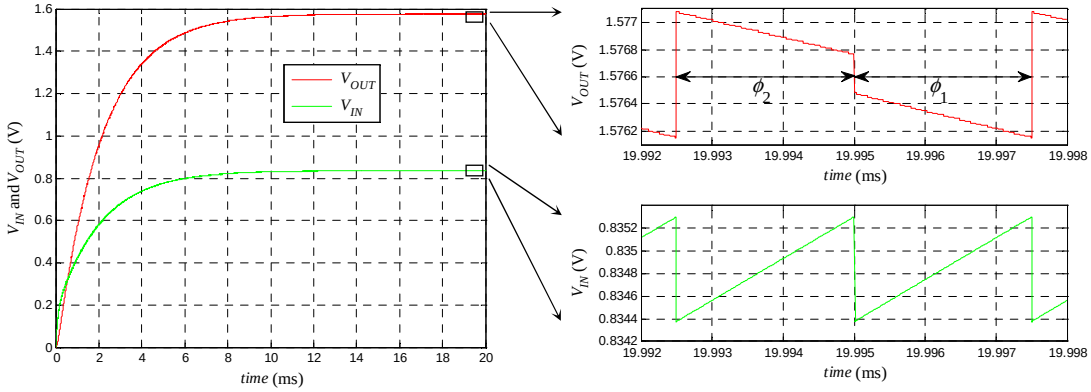


Fig. 5.6 - a) Time evolution of voltages V_{IN} and V_{OUT} with f_{CLK} = 200 kHz and R_L = 110 kΩ and b) Close-up of voltages V_{IN} and V_{OUT} in the steady-state zone.

In both Fig. 5.5 b) and Fig. 5.6 b), the ripple of V_{IN} and V_{OUT} is less than 1.5 mV.

In TABLE 5.1, the values of the theoretical and the simulated values are summarized, as well as the relative error between these two values. This table shows that expressions (5.4) and (5.5) accurately describe the behavior of the circuit. The relative error is given by

$$E_r = \frac{\text{Simulated} - \text{Theoretical}}{\text{Theoretical}} \times 100\% \,. \tag{5.10}$$

TABLE 5.1 - Comparison between theoretical and simulated values of V_{IN} and V_{OUT}.

	R_S = 4 kΩ, v_S = 1 V, C_1 = 1.1 nF, C_p = 20 pF, C_{in} = 110 nF and C_o = 110 nF					
Input and output voltages	Using f_{CLK} = 200 kHz and R_L = 110 kΩ			Using f_{CLK} = 459.1 kHz and R_L = 16 kΩ		
	Theoretical	Simulated	E_r	Theoretical	Simulated	E_r
V_{IN} (V)	0.834973	0.83529	+0.04%	0.499013	0.49926	+0.05%
V_{OUT} (V)	1.57557	1.57613	+0.04%	0.873323	0.87372	+0.05%

The expressions in (5.4) and (5.5) show that voltages V_{IN} and V_{OUT} can be controlled by using the clock frequency. By adjusting this frequency, it is possible to achieve the MPP condition, which occurs when the input impedance of the SC circuit equals the value of R_S, resulting in $V_{IN} = v_S/2$. Equation (5.4) shows that if the clock frequency increases, the input voltage decreases, and vice-versa. This means that when the available input power decreases, corresponding to a decrease of v_S, the clock frequency of the circuit should decrease in order to track the MPP condition, and vice-versa. Other implementations (inductor-based) use a fixed operating frequency and vary the duty-cycle to track the MPP, such as [77], [153] and [155].

However, an oscillator with fixed frequency has constant power dissipation, because the latter depends on frequency and not on the duty-cycle. Moreover, if the clock frequency can decrease when the input power decreases, the power dissipation of the controller circuit also decreases, allowing for the system to operate with lower levels of input power. This principle is also followed by [156], where the level of available light and the charge of the storage capacitor determine the frequency of operation, the available voltage to power the digital circuits, and the bias current of analog circuits, making the system to adapt to the available ambient resources. However, the approach is different from the present work, because the former needs to perform some measurements before proceeding with the changes on the critical parameters, whereas the system underlying this research thesis performs an automatic frequency adjustment.

5.2.1 SC Voltage Doubler with charge reusing

In order to reduce the area occupied by the capacitors, it was decided to use MOS transistor capacitors. This type of capacitor has the largest available capacitance per unit area in the selected CMOS technology. However, this option also results in a large bottom plate parasitic capacitance [117]. In Fig. 5.7, it is shown the structure of such a capacitor, using a NMOS device (M_1), thus with the substrate tied to ground.

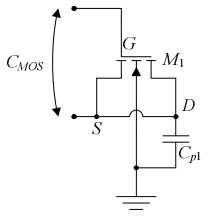


Fig. 5.7 - A MOSFET capacitor, with explicit bottom plate parasitic capacitance.

The drain (D) and the source (S) terminals are shorted together (thus, shorting both ends of the channel) and the desired capacitance (C_{MOS}) develops between this connection and the gate (G) terminal. Summarily, and approaching this device as a planar capacitor, the insulating oxide between the gate and the channel serves as the dielectric, while the channel area ($W \times L$) defines the area of each plate. Since the oxide is very thin (2.2 nm), the capacitance can reach a very high density per unit area. The bottom plate parasitic capacitance is represented by C_{p1} in Fig. 5.7. This capacitance exists between the channel (the bottom plate of the capacitor) and the substrate, corresponding to the stray capacitance, referred in Chapter 4.

Both the MOS capacitance and its bottom plate parasitic capacitance are non-linear and vary with the input voltage. The simulation (in Spectre) of the capacitance behavior, of a capacitor like the one shown in Fig. 5.7, using a 130 nm CMOS technology MOSFET, with dimensions $W = 50\ \mu m$ and $L = 2\ \mu m$, is depicted in Fig. 5.8. The variation of the MOS

capacitance is ploted against the variation of the voltage at the terminals of the MOS capacitor. This figure also shows the various working zones of the channel (accumulation, depletion and inversion) and how the capacitance behaves in each of them. The resulting curve shape is typical for this kind of device. As seen, when MOS capacitors are used, during the voltage elevation process, the MOS capacitor experiences a voltage variation at its terminals, ranging from 0 to v_{in} and from v_{in} to $2 \times v_{in}$, which results in a variation of its capacitance value.

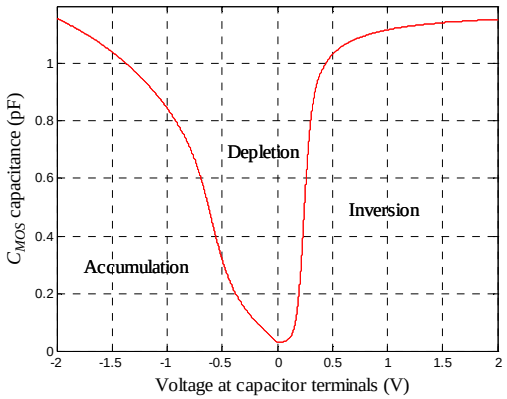


Fig. 5.8 - Typical capacitance variation of a MOSFET capacitor of the 130 nm technology, as a function of the V_{GS} voltage, with W = 50 µm and L = 2 µm.

Fig. 5.9 shows the capacitance variation of the same MOS capacitor as shown in Fig. 5.8, emphasizing the positive voltage in the range of 0 to 0.6 V, which is the voltage difference range most likely to occur in the current SC step-up voltage converter application.

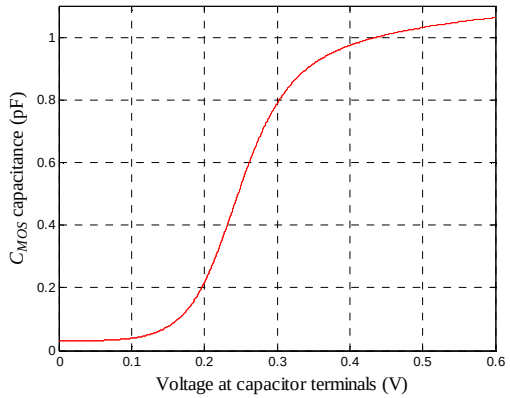


Fig. 5.9 - Capacitance variation for C_{MOS}, when using a MOSFET with W = 50 µm and L = 2 µm.

As it has been said, any real implementation of the circuit in Fig. 5.2 has inherently a parasitic capacitance at the bottom plate node, denoted in this figure as C_{bottom}. This capacitance is charged up to v_{in} during phase ϕ_1 and discharged during phase ϕ_2. This is equivalent to a resistance that dissipates energy, thus lowering the efficiency of the circuit. This problem can be particularly serious when MOS capacitors are used, because of the large parasitic capacitance

value that they introduce. Fig. 5.10 shows the bottom plate capacitance for a MOS transistor like the one whose main capacitance is shown in Fig. 5.9. This capacitance is constituted by (C_{db} + C_{sb}).

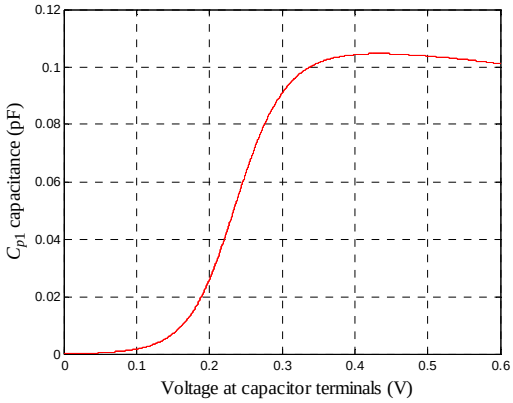


Fig. 5.10 - Variation of the bottom plate capacitance (C_{p1}) when using a MOSFET with W = 50 µm and L = 2 µm.

Fig. 5.11 depicts the ratio between these two capacitances in a MOS capacitor, just like the situation depicted in Fig. 5.7, as a function of the voltage applied to its terminals. This ratio varies with the variation of this voltage and can reach a value as high as 12%.

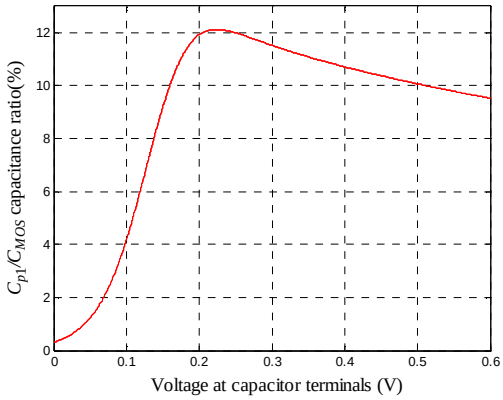


Fig. 5.11 - Ratio between the bottom and the main capacitance of a MOS capacitor like the one in Fig. 5.7, with W = 50 µm and L = 2 µm, using a 130 nm technology.

In order to improve the efficiency, it is necessary to reduce the amount of charge that is lost through the bottom plate parasitic capacitance. In order to address this problem, the approach that was followed consisted on splitting the switched capacitance in two, and then, duplicating the circuit. Naming ϕ_3 the old ϕ_2 phase, a third phase (ϕ_2), is now introduced between ϕ_1 and ϕ_3. During this new phase ϕ_2, the bottom plate nodes of the two half-circuits are connected together. The entire circuit is depicted in Fig. 5.12. In here, $C_{p\{1,2\}}$ is the parasitic capacitance at the bottom plate nodes of each of the MOS capacitors, M_1 and M_2, respectively, which are again made explicit for a better understanding.

When ϕ_1 is active, M_1 and C_{p2} are connected in parallel with the input voltage, and M_2 is placed in series with the input voltage, achieving an ideally voltage doubling at the output, v_{out}. During this phase, C_{p1} is discharged, as both of its plates are grounded.

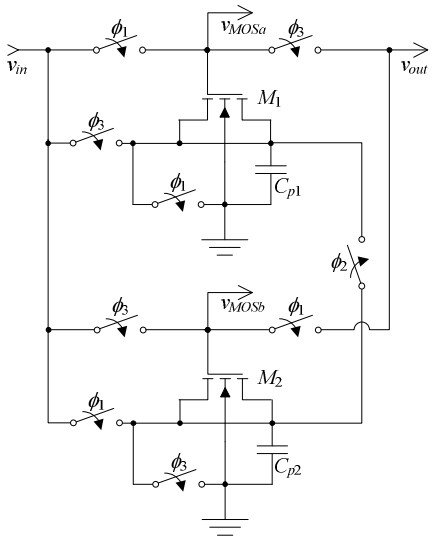


Fig. 5.12 - Schematic of the proposed step-up doubler SC converter, using MOS capacitors with charge reusing.

When ϕ_3 is active, M_2 and C_{p1} change role with M_1 and C_{p2}, leading to the same behavior that took place when ϕ_1 was active.

When ϕ_2 is active, C_{p1} and C_{p2} are connected in parallel, resulting in charge redistribution between these two parasitic capacitances. Because one of these capacitances is charged to v_{in}, while the other is completely discharged, when they are connected together, the charge is equally divided between them and each capacitor will get half of the charge of the capacitor that was firstly charged to v_{in}. Ideally, the voltage across this parallel circuit will be $v_{in}/2$. Now, either in phase ϕ_1 or in phase ϕ_3, the parasitic capacitor to be subsequently connected to v_{in}, will already be pre-charged to half of its final charge value, thus requiring only half of the charge from the input source. This prevents the waste of half of the input charge, inevitably commited to the bottom plate MOSFET capacitances.

In order to confirm the advantage of using the charge reusing technique, capacitor C_1, in the circuit depicted in Fig. 5.2, was replaced by a MOSFET capacitor and the resulting circuit was simulated using Spectre. From these simulations, the efficiency of the circuit, defined as the ratio between the output power and the input power, was calculated. The general expression for the efficiency is given by

$$\eta = \frac{P_{out}}{P_{in}}. \tag{5.11}$$

Next, capacitor C_1 and the associated switches were replaced by the circuit depicted in Fig. 5.12. An extra clock signal (the new ϕ_2) was also added. Once again, the resulting circuit was simulated in Spectre and its efficiency was calculated. In both of these simulations, R_S = 4 kΩ, R_L = 16 kΩ, v_S = 1 V, C_p = 0 and f_{CLK} = 459.1 kHz. The value of C_1 is 1.1 nF for both circuits (in the second circuit, each MOSFET capacitor has half of this value). This value, and the one for f_{CLK}, will be determined and justified later, in Section 5.3.2.1. The efficiency of the circuit, and the output steady-state voltage for each situation, is presented in TABLE 5.2.

TABLE 5.2 - Efficiency comparison of the circuit, with and without the charge reusing technique.

η (simulated without charge reusing)	η (simulated with charge reusing)
63.24% (V_{OUT} = 801 mV)	74.21% (V_{OUT} = 847 mV)

The results presented in TABLE 5.2, show that the efficiency loss due to the bottom plate parasitic capacitance, can be effectively reduced, by using the charge reusing technique.

5.2.1.1 Switch sizing

The switches are implemented by using transmission gates, as shown in Fig. 5.13.

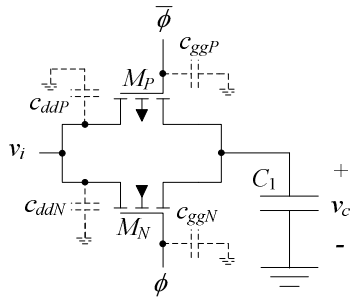


Fig. 5.13 - *RC* circuit using a transmission gate and a capacitor

The issues associated to the switches are their ON resistance (R_{ON}) and the total parasitic capacitance (C_{loss}), which is the total capacitance seen from both gates (c_{ggP} + c_{ggN}), plus the one seen from both drains (c_{ddP} + c_{ddN}), to any other nodes. It is preferable to have both R_{ON} and C_{loss} as low as possible. The problem is that these two parameters are in conflict, since having a low ON resistance means having an increase in the width (W) of the transistors. However, this originates an increase in the total parasitic capacitance. It is to note that the length of the channel in both transistors is the same, but the PMOS has its channel three times wider than the NMOS.

The ON resistance will determine how settled the circuit will be at the end of each half period, each controlled by ϕ_1 or ϕ_3, referring to Fig. 5.12. The law that rules this regime is the well-known capacitor charging equation:

$$v_c(t) = v_i\left(1 - e^{-\frac{t}{R_{ON}C_1}}\right). \tag{5.12}$$

The settling error is given by

$$error = e^{-\frac{T_{CLK}/2}{R_{ON}C_1}}. \tag{5.13}$$

Variables *error*, C_1 and T_{CLK} will determine R_{ON} and, by consequence, the width W of the transmission gates (L is minimum, i.e. 120 nm in the 130 nm CMOS technology). Thus,

$$\ln\left(\frac{1}{error}\right) = \frac{T_{CLK}}{2\,R_{ON}\,C_1} \Leftrightarrow R_{ON} = \frac{1}{2\ln\left(\frac{1}{error}\right) f_{CLK} C_1}. \tag{5.14}$$

There is a coefficient k_R that relates R_{ON} to the width of the switch, knowing that these are inversely proportional to each other:

$$R_{ON} = \frac{k_R}{W} \Leftrightarrow W = \frac{k_R}{R_{ON}}. \tag{5.15}$$

On the other hand, there is also a coefficient k_C that relates the parasitic capacitance of the switch to W, such that

$$C_{loss} = k_C W \Rightarrow C_{loss} = \frac{k_R k_C}{R_{ON}} = 2k_R k_C \ln\left(\frac{1}{error}\right) f_{CLK} C_1. \tag{5.16}$$

The coefficients k_R and k_C were derived by simulation using Spectre, by giving the transmission gate various values for the width of its transistors (1 µm, 5 µm, 10 µm, 20 µm, 30 µm and 40 µm) and performing a linear regression over the dots that were obtained. The obtained functions are shown in Fig. 5.14 and Fig. 5.15, having been obtained k_R = 806.24 Ω·µm and k_C = 7.1 fF/µm, respectively.

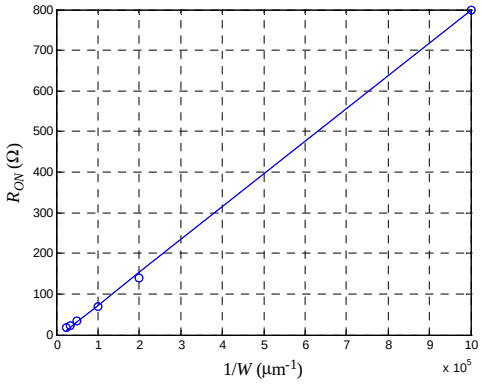


Fig. 5.14 - R_{ON} as function of W^{-1}.

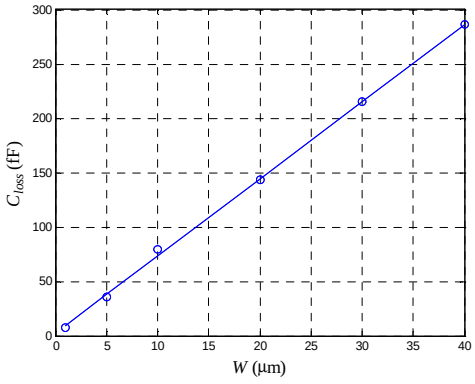


Fig. 5.15 - C_{loss} as function of W.

As understood from Fig. 5.8 to Fig. 5.11, the nature of the MOS capacitors is very non-linear and hard to describe analytically. As such, the adopted strategy relied on an assumption of upgraded (yet reasonable) values for the circuit parameters that determine the size of the switches. The considered values were: C_1 = 3 nF, *error* = 0.1% and f_{CLK} = 2 MHz. This leads to $R_{ON} \approx 12\ \Omega$, meaning that $W = k_R / R_{ON} = 66.8\ \mu m$. As a consequence, the parasitic capacitance associated to the transmission gate is $C_{loss} \approx 474$ fF. These values for R_{ON} and C_{loss} are concentrated into a single switch, as depicted in Fig. 5.13, but the switched-capacitor is placed in series with two switches during each phase. However, the value of C_1 considered in these calculations is the total capacitance, including both branches (each branch has half of the value of C_1). As such, in order to keep the value of the time constant, all the results should be kept as they are, meaning that the values for W, R_{ON} and C_{loss} represent one switch alone.

5.3 Phase Controller

The Phase Controller is the circuit responsible for the generation of the signals controlling the action of the switches in the SC step-up voltage doubler. The phases (ϕ_1, ϕ_2 and ϕ_3) are square wave signals generated by a circuit also implementing the MPPT algorithm. The MPPT technique that has been chosen is the Fractional V_{OC}. This MPPT method has already been addressed in Chapter 4 - Section 4.6.2. Because of its simplicity and low power dissipation, this was the method selected to be included into the phase generator. In order to remind about the main characteristics of this MPPT technique, its main features will be highlighted again.

5.3.1 MPPT regulation using the Fractional Open Circuit Voltage

As it has already been mentioned, the clock phase signals, which control the operation of the SC voltage doubler circuit, should run at a frequency, such that the power transferred from the PV cells can be maximized [82]. Since this power value changes with light intensity and with temperature, the controller circuit that produces these clock signals should use a MPPT method in order to continuously adjust the clock frequency value. One of the main limiting factors when building an indoor light energy powered micro sensor system, is the reduced available energy coming from the PV cells, to power it. Therefore, the controller circuit should use as little power as possible. There are various methods available for the MPPT of a PV cell which are addressed in [86] and have been briefly presented in Chapter 4 - Section 4.6.2. A careful criterion must be taken to choose the appropriate method, in order to keep the controller to an acceptable power overhead, since the current application has a very restricted energy input.

Some of the methods in [86] can track the true MPP of the cell, but these typically require complicated circuits or large computational effort. However, in order to have less complex circuits dissipating less power, some accuracy can be sacrificed in the determination of the MPP, leading to the use of simpler methods. Since that the application described in this thesis has a very low available power, these simpler methods are preferable. As such, the Fractional V_{OC} method was chosen, because it is a very simple and inexpensive (hardware wise) method. This method explores the intrinsic characteristic of PV cells, in which there is a proportionality factor (k) between their open circuit voltage and the voltage at which the MPP occurs (v_{MPP}), as shown in (4.23). This factor must be determined beforehand, by studying the behavior of the PV cell under various conditions of illumination and temperature. This procedure has been exemplified in Section 4.6.2. Pilot PV cells in open circuit (unloaded) are used to measure the open circuit voltage. The optimum voltage of the unloaded PV cell (v_{MPP}) is determined by multiplying the open circuit voltage of the pilot by a factor k, using a resistive divider. The pilot PV cells must have the same temperature and illumination as the PV main cells, in order for the Fractional V_{OC} method to track the MPP voltage as best as possible. The requirement of an auxiliary PV cell is the disadvantage about this method. However, its simplicity allows for building a controller circuit with very low power dissipation, which is an advantage that one believes to be more important than the disadvantage.

The MPPT is achieved by adjusting the loading of the PV cell in order to obtain the desired input voltage (v_{MPP}). Since the equivalent input impedance of the SC voltage doubler circuit is proportional to $1/(f_{CLK} \times C_1)$, when referring to Fig. 5.2, by controlling the clock frequency it is possible to increase or decrease the value of this impedance. When v_{MPP} is larger than the PV cell voltage (v_{in}) this means that the input impedance of the SC doubler circuit is small and therefore it is necessary to decrease the switching frequency to increase this impedance, thus increasing the voltage coming from the PV cell. If v_{MPP} is smaller than the PV cell voltage, it is necessary to increase the switching frequency, so as to decrease the impedance of the SC circuit and therefore decrease the PV cell voltage, i.e. the input voltage of the circuit. This process will result in an average switching frequency value that allows for the SC voltage doubler circuit to have an average input impedance value that originates the MPP voltage at the terminals of the PV cell.

5.3.2 Asynchronous state machine (ASM) circuit

The three clock phases, necessary for the operation of the SC voltage doubler circuit of Fig. 5.12, are generated by an ASM circuit, which automatically and dynamically adjusts the clock frequency, in order to obtain the MPP voltage from the PV cell. The state diagram that

represents the MPPT algorithm, the generation of the three clock phases and the conditions that must be met, in order to go from one state to the next, are shown in Fig. 5.16.

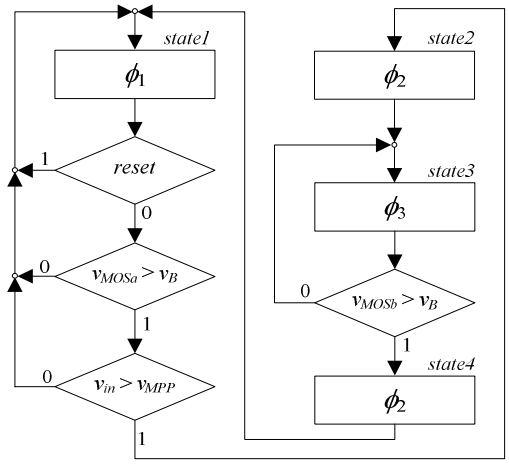


Fig. 5.16 - State diagram of the algorithm performed by the ASM.

The circuit that implements this state diagram, incorporating the Fractional V_{OC} MPPT technique, is depicted next in Fig. 5.17.

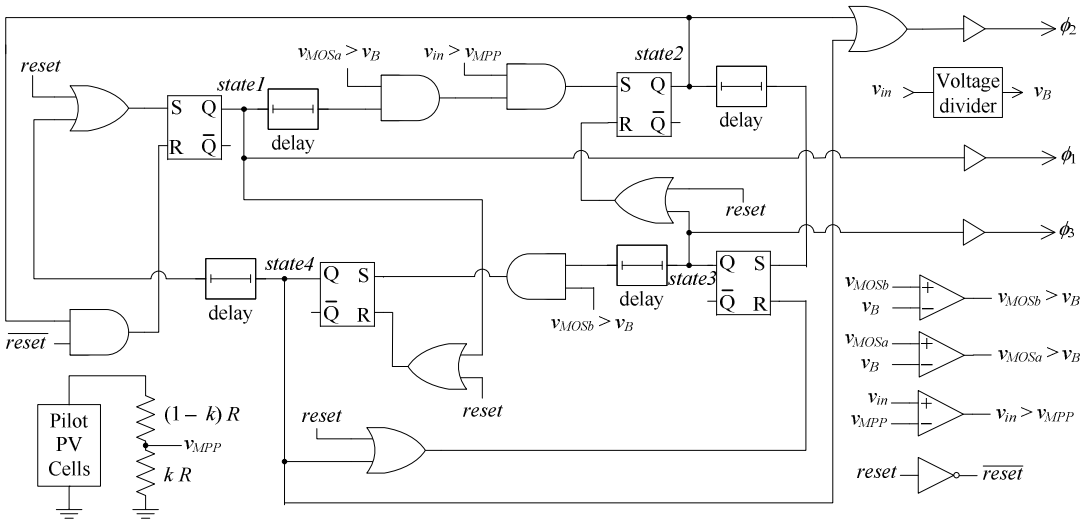


Fig. 5.17 - Phase controller schematic using Fractional V_{OC} MPPT.

This circuit has four states that are determined by the output of four S-R latches. These states correspond to the clock phase signals ϕ_1, ϕ_2, ϕ_3, and again ϕ_2, respectively. In order to change from one state to the next, the *Set* signal of one latch is activated, changing the output of that latch from logic 0 to logic 1. This, in turn, activates the *Reset* signal of the previous latch, causing its output to change from 1 to 0, thus completing the state change. The ASM is continually changing from one state to the next (and then from *state4* to *state1*), in order to create the clock phase signals. This circuit works as a voltage controlled oscillator, where the

maximum frequency is determined by the delay circuits inserted between the output of each latch and the *Set* input of the next latch. Note that the duration of each phase is not the same.

The transitions from *state1* to *state2* and from *state3* to *state4* are delayed by comparators that guarantee that the MOS capacitors, connected to the PV cells, are charged to at least 95% of the input voltage ($v_{MOSa} > v_B$ and $v_{MOSb} > v_B$). The capacitor charging time depends on the series resistance of the input voltage source. Thus, it is necessary to give enough time for the PV cells to completely charge the capacitor when the irradiance is very low. The minimum duration of each state is determined by a delay circuit customized to delay digital signals. In particular, the delaying provided by this circuit is only applied to the rising edge of its input signal, whereas for the falling edge, it is not affected by any delay, just as illustrated in Fig. 5.18.

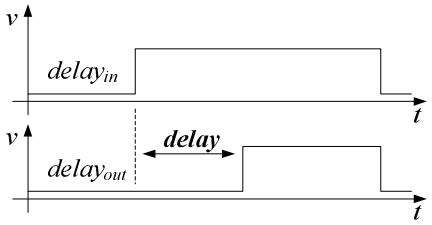


Fig. 5.18 - Time relation between the input and the output signals of the delay circuit.

The schematic of the delay circuit is depicted in Fig. 5.19. This delay circuit is used to establish the minimum duration of the clock phases. Since the delay time depends on the power supply voltage value, the delay circuit was designed in order to guarantee that the minimum delay time is always long enough for the switched capacitor (or its corresponding bottom plate capacitance) to be always completely charged or discharged.

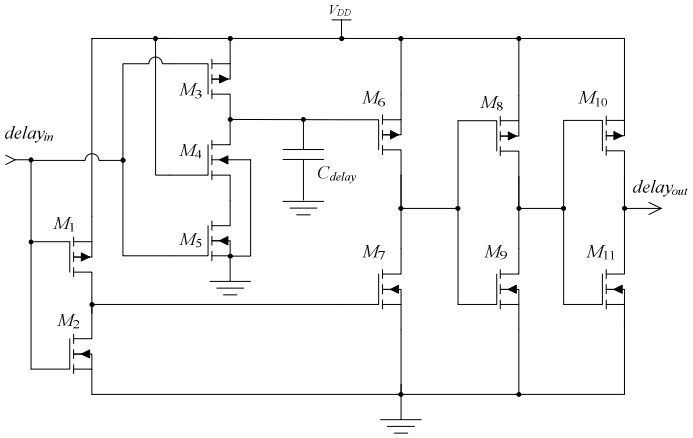


Fig. 5.19 - Schematic of the delay circuit.

The duration of *state1* (phase ϕ_1) is also dependent on the comparison between the main PV cells voltage (v_{in}) and the fractional open circuit voltage obtained from the pilot PV cells (v_{MPP}). When MOS capacitor M_1 is connected to the input PV cells (in the beginning of ϕ_1),

voltage v_{in} drops. The ASM stays in *state1* until the input voltage is charged back to the v_{MPP} value. Therefore, the duration of the oscillation period corresponds to the frequency value that adjusts the input voltage to the MPP voltage value. This approach allows for achieving a very low clock frequency when the light intensity is also very low. In fact, the duration of phase ϕ_1 can be as long as needed by the PV cell, in order to charge the input capacitance to v_{MPP}.

The comparators are similar to the ones described in [20] with the only difference being the addition of a power-down (*pd*) feature that is used in the states where they are not needed by the ASM. This reduces the power dissipation of the phase generator and contributes to the increase of the overall efficiency of the system. The comparator will only be working, thus having power consumption, when *pd* is logic 1. The complete schematic for the comparator is depicted in Fig. 5.20. In this schematic, the substrate connection is omitted, but the bulk of the PMOS devices is connected to V_{DD} and the one in the NMOS devices, is connected to ground.

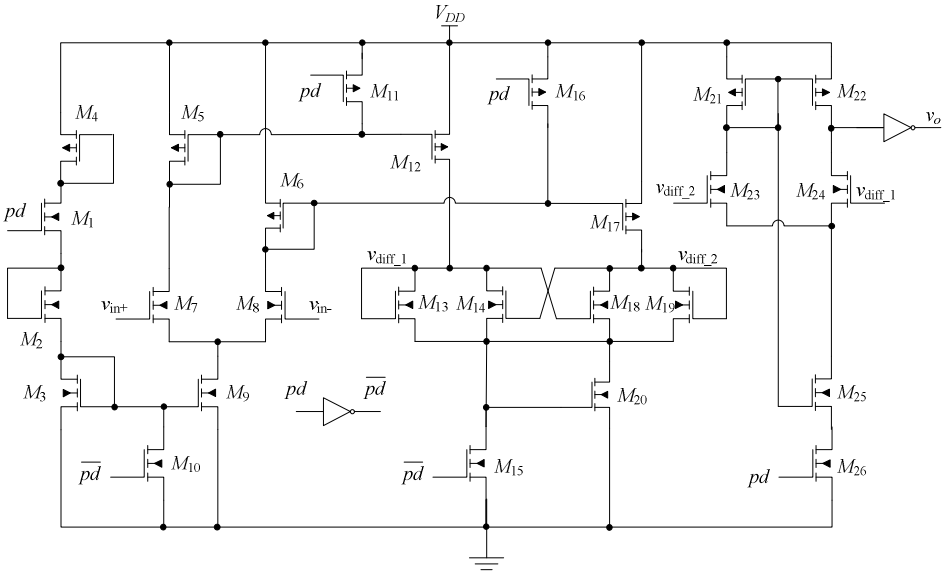


Fig. 5.20 - Schematic of the comparator circuits.

Since the available power is at a premium, the complete phase controller circuit was carefully designed under the perspective of achieving a power dissipation as low as possible. All the gates and circuits that make up the ASM were designed using minimum sizes and the comparators use class AB operation, in order to reduce their bias current. The CMOS gates only dissipate power during the clock transitions, due to the charging to V_{DD} of the parasitic capacitor at the output of each gate, and then discharging it to V_{SS}, and also due to the current that flows directly from V_{DD} to V_{SS} when the PMOS and NMOS devices are simultaneously ON (illustrated in Fig. 5.21).

The two mechanisms can be modeled by a switched parasitic capacitor, of appropriate value, as shown in Fig. 5.21.

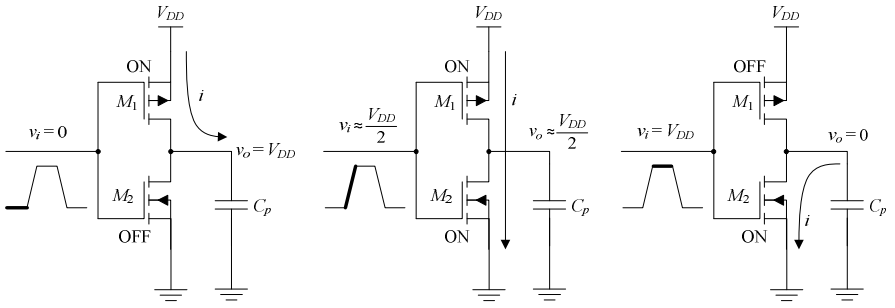


Fig. 5.21 - Current drawn by a logic inverter during a clock transition. During this transition, a current flows from V_{DD} to V_{SS}, when both transistors are ON. This draws a constant charge from V_{DD} in each clock transition, being equivalent to a switched parasitic capacitor, whose value varies with V_{DD}.

This value was determined by simulating the complete phase controller circuit of Fig. 5.17, for different clock frequencies and voltage supply values. The average value of the current drawn by the circuit was measured. As expected, this current increases linearly with the clock frequency and it is not equal to zero when the clock frequency is zero, due to bias currents. The DC value was removed from the average current and the remaining dynamic current was used to calculate the value of $C_p = I_{vdd} / (v_{dd} \times f_{CLK})$. The value of C_p depends on the value of v_{dd} because the shoot through current (Fig. 5.21) depends on the value of v_{dd}. The DC current of the phase controller is modeled by an equivalent resistor in parallel with R_L, and it also depends on v_{dd}. The determined values are C_p = {2.3 pF, 7.5 pF, 23 pF} and R_L = {205.1 kΩ, 135.7 kΩ, 107.5kΩ} for supply voltages v_{dd} = {0.8 V, 1.0 V, 1.2 V}, respectively. The worst case is C_p = 23 pF and this is the value that will be considered in the design of the circuit, for safety.

5.3.2.1 Determination of the optimum circuit parameters

There is a frequency value that enables the switched circuit to achieve the MPP condition. The value of T_{CLK} which allows for achieving this condition is derived assuming that $V_{IN} = v_S/2$. Let us call to V_{IN}, under this condition, V_{INMPP}. Thus,

$$V_{IN_{MPP}} = \frac{v_S}{2}. \tag{5.17}$$

Through solving (5.4) under this assumption, and after full simplification, the value of the clock period is given by the following expression:

$$T_{CLK_{MPP}} = 2\frac{4C_1C_oR_S - C_1C_oR_L - C_1C_pR_L - C_oC_pR_L + C_1C_pR_S + \sqrt{4C_1C_oC_p(C_1+4C_o+C_p)R_SR_L + (C_oC_pR_L + C_1(C_o+C_p)R_L - C_1(4C_o+C_p)R_S)^2}}{C_1+4C_o+C_p}, \tag{5.18}$$

or alternatively, in order to have an expression for the clock frequency,

$$f_{CLK_{MPP}} = \frac{C_1+4C_o+C_p}{2\times\left(4C_1C_oR_S - C_1C_oR_L - C_1C_pR_L - C_oC_pR_L + C_1C_pR_S + \sqrt{4C_1C_oC_p(C_1+4C_o+C_p)R_SR_L + (C_oC_pR_L + C_1(C_o+C_p)R_L - C_1(4C_o+C_p)R_S)^2}\right)}. \tag{5.19}$$

Under these conditions, as a consequence, voltage V_{OUT} is obtained by substituting T_{CLK} in (5.5) by T_{CLKMPP}. Thus, V_{OUTMPP} is given by

$$V_{OUT_{MPP}} = \frac{C_1^2 C_p (R_L - R_S) + 2C_o^2 \left((C_1 + C_p)R_L + 4C_1 R_S\right) + C_1 C_o \left(C_1 R_L + 3C_p R_L + 2C_p R_S\right)}{2C_1 (2C_o + C_p)(C_1 + 4C_o + C_p)R_S} v_S -$$
$$- \frac{C_1 \sqrt{4C_1 C_o C_p (C_1 + 4C_o + C_p)R_S R_L + \left(C_o C_p R_L + C_1 (C_o + C_p)R_L - C_1 (4C_o + C_p)R_S\right)^2}}{2C_1 (2C_o + C_p)(C_1 + 4C_o + C_p)R_S} v_S - \quad (5.20)$$
$$- \frac{2C_o \sqrt{4C_1 C_o C_p (C_1 + 4C_o + C_p)R_S R_L + \left(C_o C_p R_L + C_1 (C_o + C_p)R_L - C_1 (4C_o + C_p)R_S\right)^2}}{2C_1 (2C_o + C_p)(C_1 + 4C_o + C_p)R_S} v_S .$$

Using this expression, the power delivered to the load resistor can be determined. From this, the power efficiency of the system can, finally, be calculated.

Equation (5.20) is somewhat cumbersome, and to have an idea about how it behaves, in Fig. 5.22 its plot is shown, as a function of R_L, using for the remaining parameters the same values that were used for the simulation whose results are depicted in Fig. 5.5.

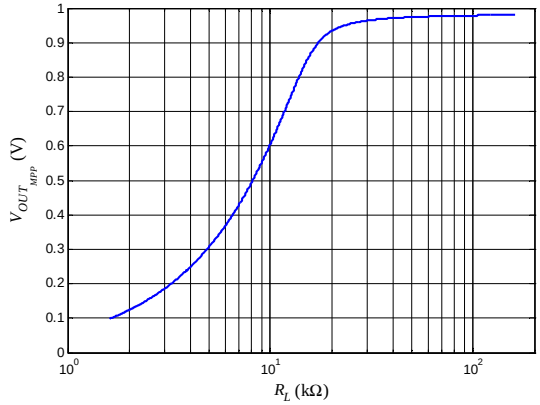


Fig. 5.22 - $V_{OUT_{MPP}}$ as a function of R_L.

Moreover, under this frequency condition, the VCR, which was previously presented in (5.8), is now given by

$$\mathrm{VCR}_{MPP} = \frac{2C_1 \left(C_1 (3C_o + C_p)R_L + C_o (8C_o + 3C_p)R_L - C_1 (4C_o + C_p)R_S - \sqrt{4C_1 C_o C_p (C_1 + 4C_o + C_p)R_S R_L + \left(C_o C_p R_L + C_1 (C_o + C_p)R_L - C_1 (4C_o + C_p)R_S\right)^2}\right)}{(C_1 + 4C_o + C_p)\left(C_o (C_1 + C_p)R_L + 4C_1 C_o R_S + C_1 C_p (R_L + R_S) + \sqrt{4C_1 C_o C_p (C_1 + 4C_o + C_p)R_S R_L + \left(C_o C_p R_L + C_1 (C_o + C_p)R_L - C_1 (4C_o + C_p)R_S\right)^2}\right)}. \quad (5.21)$$

Fig. 5.23 shows a graph of (5.21) as a function of both C_1 and R_L. All the other parameters are set to the values that were used in the simulation that produced the results shown in Fig. 5.5. As it can be seen, with the increase of both variables, VCR_{MPP} asymptotically approaches the value of two, which is the maximum theoretically expected.

In this application, its efficiency (η) is the ratio between the output power and the input power, as given by (5.11). However, the reference criterion for the efficiency is when the circuit is operating at the frequency at which the MPP is achieved.

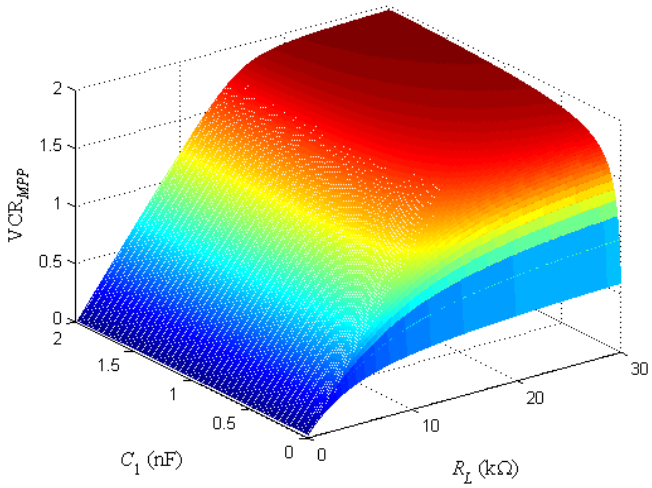


Fig. 5.23 - VCR_{MPP} as a function of both C_1 and R_L.

As such, at this frequency, the output power being delivered to the load, is given by

$$P_{out} = \frac{V_{OUT_{MPP}}^2}{R_L}. \tag{5.22}$$

The expression of P_{out} will not be explicitly shown here, because it is too extense and would not be intuitive. On the other hand, knowing that the input voltage is $V_{INMPP} = v_S/2$, and thus, that the input impedance of the SC voltage converter is given by R_S, the input power is given by

$$P_{in} = \frac{V_{IN_{MPP}}^2}{R_S} = \frac{(v_S/2)^2}{R_S} = \frac{v_S^2}{4\times R_S}. \tag{5.23}$$

Having the two previous equations derived, the expression of the efficiency can also be derived, being shown next in (5.24).

$$\eta = \frac{(a+b)^2(b+c)^2}{d(e+f(b+g))^2}$$

$$\begin{aligned}
a &= -3C_1C_oR_L - 8C_o^2R_L - C_1C_pR_L - 3C_oC_pR_L + 4C_1C_oR_S + C_1C_pR_S \\
b &= \sqrt{4C_1C_oC_p(C_1+4C_o+C_p)R_LR_S + (C_oC_pR_L + C_1(C_o+C_p)R_L - C_1(4C_o+C_p)R_S)^2} \\
c &= -C_oC_pR_L - C_1(C_o+C_p)R_L + C_1(4C_o+C_p)R_S \\
d &= (C_1+4C_o+C_p)^2R_LR_S \\
e &= -C_1(4C_o^2+3C_oC_p+C_p^2)R_L + C_1(4C_o+C_p)^2R_S \\
f &= 4C_o+C_p \\
g &= C_oC_pR_L
\end{aligned} \tag{5.24}$$

The load resistor that maximizes efficiency is $4\times R_S$. This is confirmed by plotting the efficiency function against the ratio R_L / R_S. This plot is depicted next in Fig. 5.24. The

remaining components have the same values as in the simulation whose results are shown in Fig. 5.5.

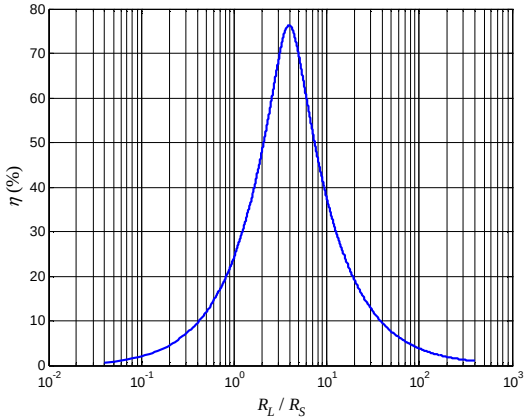


Fig. 5.24 - Efficiency value, as a function of the ratio R_L / R_S.

The plot shown in Fig. 5.24 also allows for understanding that the maximum efficiency, given these conditions, is 76.4%.

The value of the clock frequency producing the MPP condition (f_{CLKMPP}), which has been derived and is shown in (5.19), depends on the value of all the parameters of the circuit, including the value of C_1, the switched-capacitor. The value of f_{CLKMPP} increases if C_1 decreases and vice-versa (for a given load and input power level), as shown next in Fig. 5.25.

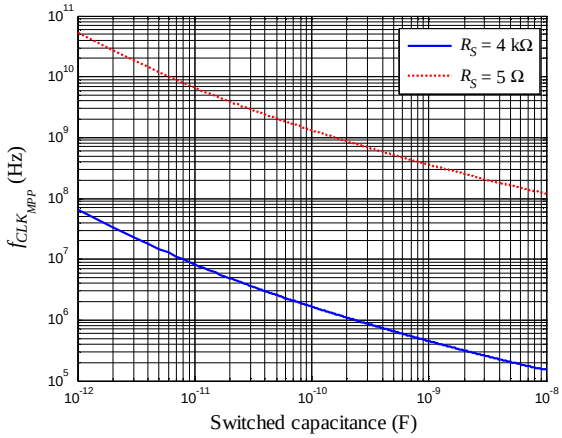


Fig. 5.25 - MPP clock frequency, as a function of the switched capacitance (C_1).

The graphs in Fig. 5.25 were ploted assuming that v_S = 1 V and that R_S = {4 kΩ, 5 Ω}, corresponding to a maximum available power from v_S, of 62.5 µW and 100 mW, respectively. In either case, R_L is equal to 4×R_S. These graphs show that it is possible to achieve the MPP condition with a wide range of values for C_1, each corresponding to a different f_{CLKMPP} value. In order to determine the optimum values for C_1 and f_{CLKMPP}, it is necessary to analyze the efficiency of the system as a function of the value of C_1.

Also seen in Fig. 5.25, if the power level is higher, for the same capacitance value, a higher frequency will be needed, in order to bring in more electric charge from the input node, per unit of time.

Assuming that C_p is equal to the worst case scenario determined in Section 5.3.2, it is possible to calculate the efficiency of the system for different values of C_1 and R_S. This is shown in the graph of Fig. 5.26, corresponding to the plot of the efficiency function shown in (5.24).

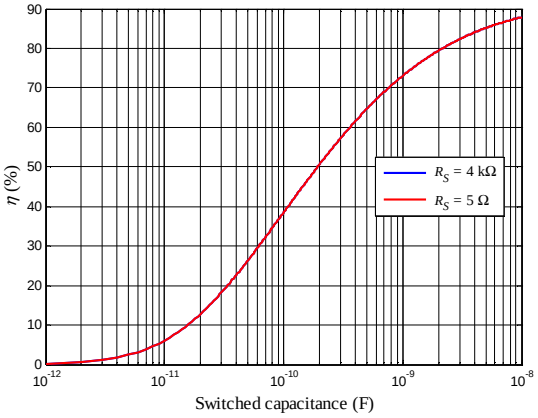


Fig. 5.26 - Efficiency, as a function of the switched capacitance (C_1) value (the traces for the two different values of R_S are overlapped).

The previous graph shows that increasing the value of C_1 also increases the value of the efficiency of the system. This can easily be understood by observing the circuit of Fig. 5.2. In each clock cycle, part of the charge transferred by C_1 to the output node is lost through C_p (note that this behavior occurs in a single clock cycle and therefore does not depend on the value of f_{CLKMPP}). This means that if the ratio C_1/C_p is small, most of the charge will be lost, resulting in a very low efficiency for the system. This is also the reason why the phase generator guarantees that C_1 is charged to at least 95% of v_{in}. Since the value of C_p is set by the controller circuit and this circuit was already designed with the objective of minimizing C_p, the only remaining option to increase the efficiency of the system is by increasing the value of C_1. This also results in a lower value for f_{CLKMPP}, which helps to reduce the dynamic power dissipation of the controller circuit. Due to area and cost limitations, the value of C_1 cannot be very large and, therefore, 1.1 nF was selected as a compromise. This results in f_{CLKMPP} = 459.1 kHz, for a maximum input power of 62.5 µW. The layout area occupied by the main capacitor, with this capacitance, is 0.1697 mm^2 (see Section 6.2.2). If this capacitance was doubled, the area would essentially double, while the theoretical efficiency of the circuit would only increase from 75.4% to 81.2%.

The values presented back in Fig. 5.5, refer to simulations that used the parameter values that have just been explained. This is why, in Fig. 5.5, given that the frequency matches with f_{CLKMPP}, and the switched capacitance is 1.1 nF, V_{IN} is equal to $v_S/2$, i.e. 0.5 V.

Thus, the final capacitors will have 550 pF (1.1 nF / 2), being substantially less (about three times) than the value that was initially referred in Section 5.2.1.1, i.e. 3 nF / 2 = 1.5 nF. The bottom plate capacitance, associated with each of the new capacitance value, will have a maximum value of 66 pF. The operating frequency at which the settling is to be within the error of 0.1% is 459.1 kHz, which is about four times less than 2 MHz, the value considered in advance in Section 5.2.1.1. Although given the conditions that have been determined for the operation at the MPP, it was decided to leave the dimensions of the switches as originally, because the overhead of occupied area, relatively to eventually smaller switches would be negligible in the overall project. Moreover, the decrease of the parasitic capacitance of the switches, when compared to the bottom plate capacitance of the MOS capacitors, would not be significant. In addition, with smaller switches, one would have an increase in their ON resistance, which is unwanted. Thus, each of the sized switches will have a resistance of about 12 Ω and a parasitic capacitance of 474 fF.

5.4 Local Supply

Since this is an energy harvesting system, it must create its own power supply for the controller circuit that generates the clock signals. The main output voltage cannot be used to power the clock generation circuit, because during the start-up of the system, this voltage is 0 V and remains close to 0 V during a long time, due to the large capacitor connected to the output. The solution is to create a local power supply voltage, independent from the output voltage. This allows for the system to start-up even if the large output capacitor is charging from 0V, unlike in [153], where starting-up is only possible when the input or the output voltages are larger than 1 V. Therefore, a smaller SC voltage doubler circuit, controlled by the same phase signals, is used to create a local power supply voltage (v_{dd}) at an internal decoupling capacitor (Local Supply module, in Fig. 5.1). This circuit is a replica of the main SC circuit, but with its capacitors and switches scaled-down to a fraction of the size of the ones in the main SC circuit. As explained before, the total capacitance value for the C_1 capacitor (now, the sum of the capacitance in the branches where M_1 and M_2 are placed, in Fig. 5.12) is limited to 1.1 nF. Thus, it is necessary to determine the fraction of this total capacitance to be assigned to the Local Supply circuit. This can be analytically determined by calculating the value of V_{OUT}, documented in (5.5), for both the main and the scaled-down circuit as a function of the value of C_1. The constraints are to consider that the load of the main circuit is only the optimal R_L, the load of the local power supply is C_p alone and that V_{IN} is $v_S/2$. These functions are plotted in Fig. 5.27, as a function of the ratio between the switched capacitance in each of the SC circuits.

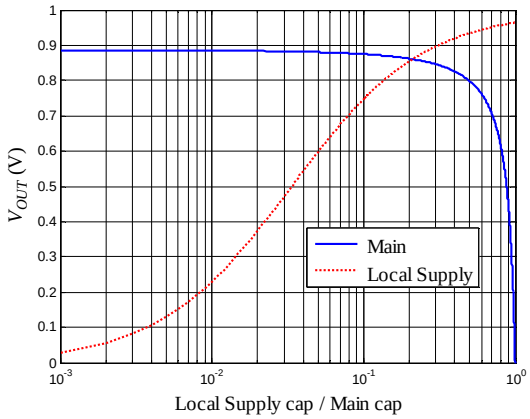


Fig. 5.27 - Output voltages of the main and the Local Supply modules, as a function of the ratio between their respective switched capacitances.

The ratio that best fits for both modules is 0.2. In order to verify this value, some simulations of the circuit, including the clock generator circuit and the Local Supply module were made, confirming that this is, indeed, the best value.

5.5 Start Up

Guaranteeing that an energy harvesting system correctly starts up is a recurrent issue, as it can be found in [157], [158] and [159], for example. Typically, it is necessary to provide a reset signal after the harvested energy source becomes available, in order to guarantee a correct starting-up of the system.

In indoor environments, the available light power can be very low and thus, the more critical is the operation and the starting-up of these systems. The current start-up circuit ensures that, even under very weak environmental illumination, the system can successfully start working. Before starting-up, the local power supply output voltage is 0 V. Therefore, the start-up circuit is used to shunt the input node to the output node of the local power supply voltage. After this voltage is charged to a value sufficient enough for the phase generator circuit to start working, this shunt is removed and the circuit starts its normal operation. The circuit also provides the *reset* signal for the phase generator circuit (MPPT controller), to guarantee that this circuit starts working in *state1* (see Fig. 5.16). The details about this start-up circuit will be given next.

5.5.1 Electrical structure and operating principle

The start-up circuit is show in Fig. 5.28.

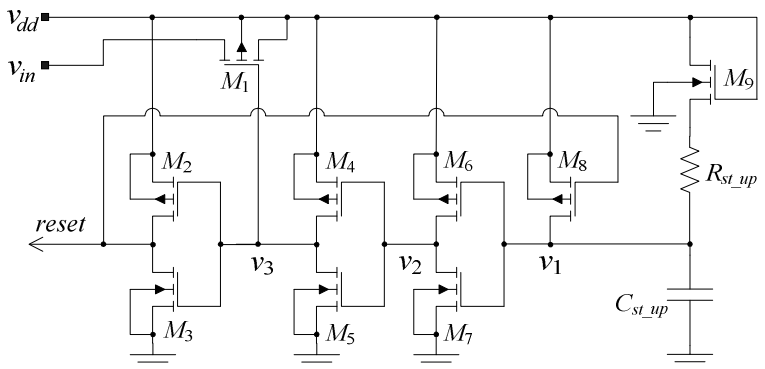


Fig. 5.28 - Schematic of the start-up circuit.

The start-up process is as follows: In the beginning, v_{in} (connected to the PV cells) is the only voltage in the system that is different from 0 V. This node is shorted, by transistor M_1, to the output node of the Local Supply (v_{dd}), which is connected to a capacitor. M_1 is a PMOS device to guarantee that it is ON in this situation. The gate of this transistor is controlled by voltage v_3, which is produced by a chain of two CMOS inverters constituted by M_6–M_7 and M_4–M_5. The input of the first inverter (M_6–M_7) is the voltage of the capacitor C_{st_up} (v_1). This capacitor is charged from v_{dd}, through M_9 and R_{st_up} and, therefore, v_1 is a delayed version of v_{dd}. The *reset* signal is produced by inverter M_2–M_3 from v_3. After the v_{dd} voltage becomes larger than the threshold voltage of the transistors, so that the circuit can properly operate, the values of the voltages in the circuit are: *reset* = v_{dd}, v_3 = 0 V, v_2 = v_{dd} and v_1 = 0 V (increasing).

When voltage v_1 becomes higher than the threshold voltage of the first inverter, voltage v_2 starts to fall, causing voltage v_3 to rise and, ultimately, the *reset* voltage, to fall. This process can take some time and it can produce a slow, or ill-defined, *reset* falling edge. In order to avoid this problem, transistor M_8 is added to the circuit. This transistor adds a positive feedback that speeds-up the previous transition: when the *reset* voltage starts to fall, transistor M_8 turns ON and supplies a large current that quickly charges the capacitor C_{st_up} to v_{dd}.

One of the main problems of indoor light energy harvesting is the low power level, available from the PV cells, which translates into a low input voltage to the system. To guarantee that, during start-up, there is enough voltage for the step-up converter to start working properly, it is necessary to obtain an input voltage as close as possible to the open circuit voltage of the PV cells. This means that the current drawn by the start-up circuit has to be very low. An inverter with an input voltage close to its threshold voltage can have a large leakage current because both of its transistors are ON. This leakage current is minimized by using different threshold voltages for the different inverters (high threshold voltage for M_6–M_7 and M_2–M_3, low threshold voltage for inverter M_4–M_5), by using transistors with long channels and by the quick transition caused by transistor M_8. The threshold voltages of the inverters also

define the minimum value of the v_{dd} voltage required for the system to start-up. The V_{TH} voltage of the transistors is around 250 mV, due to the long channels in the transistors.

The presented start-up circuit has also been used in the energy harvesting system described in [20], whose individual circuits are powered by the series of two PV cells. During normal operation, the input voltage is the maximum power point voltage of the PV cells, which is stepped-up to a desired value to power the circuit. However, during the start-up, the voltage of the PV cells is the only one available for the system to start to work.

5.6 Voltage limiter circuit

5.6.1 Motivation and background

The unpredictable nature of light energy results in a variable amount of available power. Since the PV cells must be sized in order for the energy harvesting system to be able to receive enough energy even when the light intensity is weak, this can result in large power, available from the same PV cells, when the light intensity is strong. The voltage limiter circuit fits in a system such as the one being described in this chapter, to deal with very low levels of light energy, typically found in indoor environments. However, when this system is illuminated by direct sunlight or generally, by high levels of light intensity, the energy harvested by the PV cells is much higher than the value that was expected under the normal indoor illumination conditions. In such a situation, the energy harvesting system must be able to manage the excess of energy being obtained.

The general architecture of a light energy harvesting system is depicted in Fig. 5.29, being constituted by PV cells followed by a voltage step-up converter with MPPT capability. This architecture represents a more general approach of the system shown in Fig. 5.1, meaning that this voltage limiter is able to fit in any system with similar features.

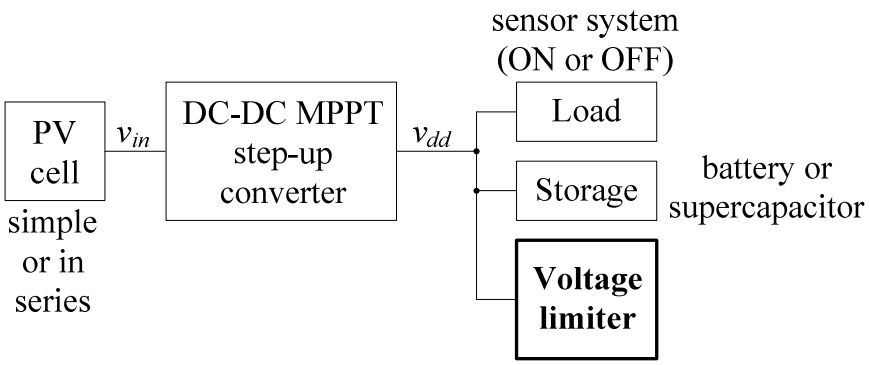


Fig. 5.29 - An energy harvesting architecture that can host the voltage limiter described in this section (all of the modules are referenced to ground).

The output voltage of the converter (v_{dd}) is the one that will be limited by the voltage limiter. The v_{dd} voltage also supplies the inner circuits of the step-up converter. The system can work with one or two PV cells in series and step-up the input voltage (v_{in}) by two or three, depending on the type of PV cells and on the expected light intensities. The power from the PV cell is dependent on its area and on the illumination level, as shown in Fig. 5.30, which shows the simulated power curves of a prototype PV cell that was characterized.

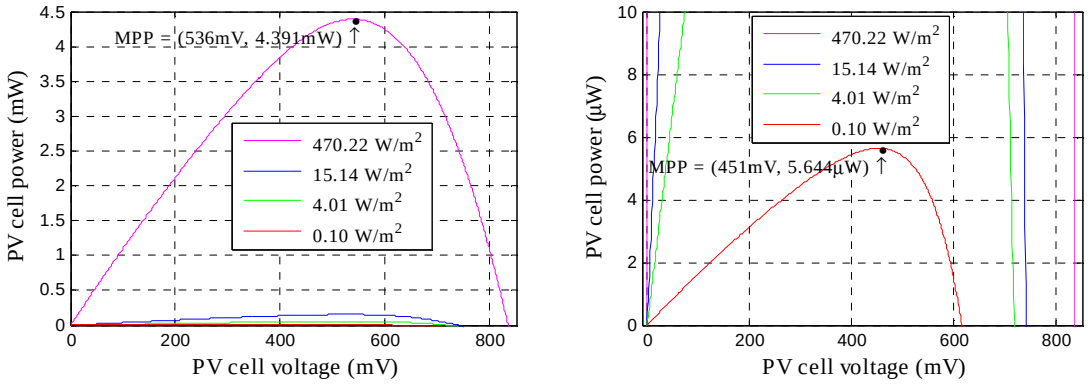


Fig. 5.30 - a) Available power from a prototype PV cell with 1 cm^2, for different irradiance levels; b) Detail showing the power function that corresponds to the lowest irradiance level.

According to a set of indoor light power intensity measurements, whose study is presented in Chapter 3 - Section 3.6.1, the lowest illumination obtained indoors had an ambient irradiance of little more than 0.1 W/m^2, and the typical irradiance using only artificial lighting, was about 0.7 W/m^2. The system must be designed for a worst case scenario (low illumination), meaning that when the light is stronger, the system will produce a large voltage at its output.

The whole system is to be laid out in a 130 nm CMOS technology. This technology allows for a maximum voltage of about 1.4 V. If this value is exceeded, the devices in the die are stressed, reducing their operating lifetime. With a larger voltage, they can even be destroyed.

Since the available power from the PV cells is low, this application typically will work using an ON-OFF regime with a low duty-cycle [16]. While the application is OFF, the harvested energy is stored in a supercapacitor. When the application is ON, it works using this stored energy. In the case of a high light intensity, after the supercapacitor is charged to a desired voltage value, the step-up converter continues to supply a current to the output node (v_{dd}). This results in the output voltage to increase to a value that can be dangerous, being necessary to add a circuit to limit it, by absorbing the excess of current supplied by the step-up converter.

In literature, some work can be found concerning voltage limiters. In [160], the voltage limitation is achieved by opening a switch to a capacitor, whenever its voltage exceeds a certain

limit, on a sample-and-hold basis. There are other systems that also use voltage limiter circuits, like in [54] and [55], where the voltage limitation problem appears under the context of RFID applications. The amount of available power to a RFID tag is dependent upon the distance to the reader device, resulting in a similar problem to the one in a light energy harvesting system. In [54], the voltage limitation is achieved by performing a comparison to a desired limit. In [55], a bandgap reference circuit is used to generate a reference voltage to which the desired voltage is compared to. This approach is similar to the one proposed for this module.

5.6.2 Voltage limiter circuit architecture

The architecture of the voltage limiter is shown in Fig. 5.31.

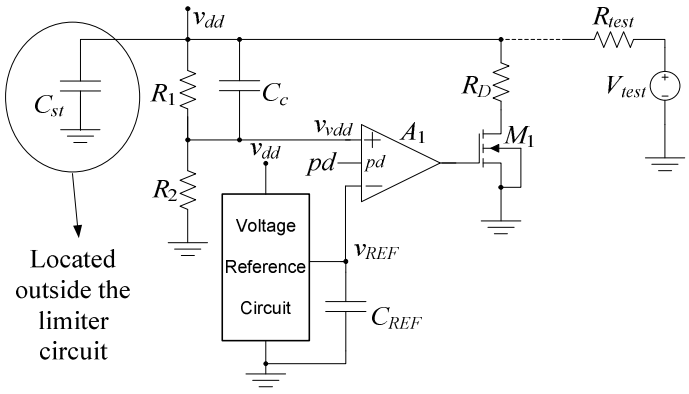


Fig. 5.31 - Architecture of the proposed voltage limiter circuit.

The Thévenin equivalent, at the right hand side of the dashed line, represents the voltage step-up converter. The aim of the proposed circuit is to limit the v_{dd} voltage to be lower than 1.4 V – 5% = 1.33 V. The voltage limiter operates by drawing current through M_1. This current causes a voltage drop across R_{test}, such that v_{dd} remains constant at the required limited value. The value, at which v_{dd} is to be limited, is controlled by a Voltage Reference Circuit (VRC), providing a stabilized and temperature compensated voltage reference.

In normal operation, the voltage divider formed by R_1 and R_2, provides at v_{vdd}, a voltage close to v_{REF}. The amplifier A_1 amplifies the error between v_{vdd} and v_{REF}, providing, at its output, a voltage that directly controls the v_{gs} voltage of M_1, and thus the current drawn from the v_{dd} node, through R_D.

5.6.3 Voltage Reference Circuit

The VRC was adapted from [161], and its schematic is shown in Fig. 5.32 a). The generated reference voltage (v_{REF}), versus the supplying voltage (v_{dd}), and the supply current of the VRC are depicted in Fig. 5.32 b).

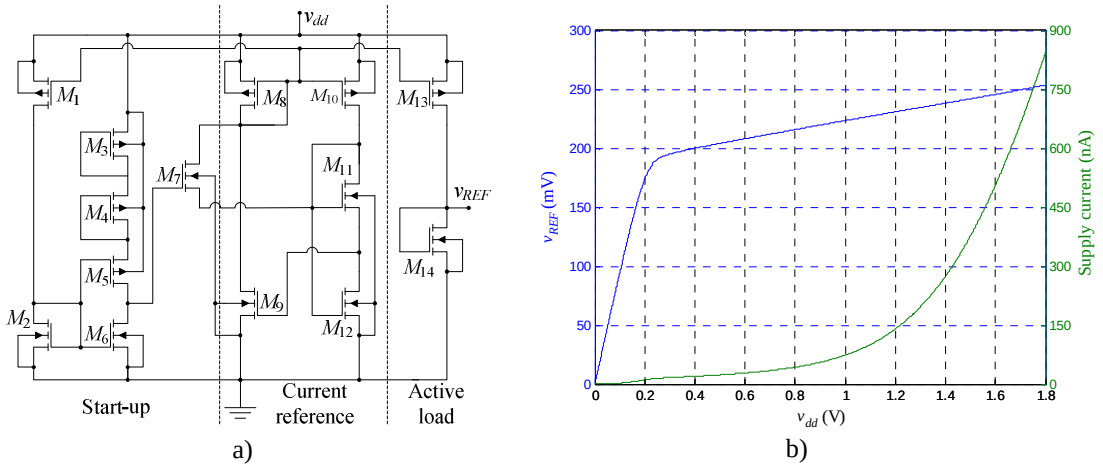


Fig. 5.32 - a) CMOS Voltage Reference Circuit; b) Output reference voltage (v_{REF}), and supply current, as a function of v_{dd}.

M_2 and M_{12} are high voltage transistors (3.3 V), while the others are low voltage ones (1.2 V). The main difference between the original circuit, and the one that was built, is the fact that the one in [161] was built in a 180 nm CMOS technology, whereas the present one uses a 130 nm technology. The transistors were sized based on the sizes presented in [161], making only adjustments due to the different technologies.

In normal operation, considering that v_{dd} = 1.2 V and a temperature of 27 ºC, the nominal output voltage of the VRC is 230.9 mV. The supply current, in this case, is 139.5 nA. These data are shown in Fig. 5.32 b). In Fig. 5.33, the supply current and the reference voltage values, as a function of temperature, for different supplying voltages, are shown.

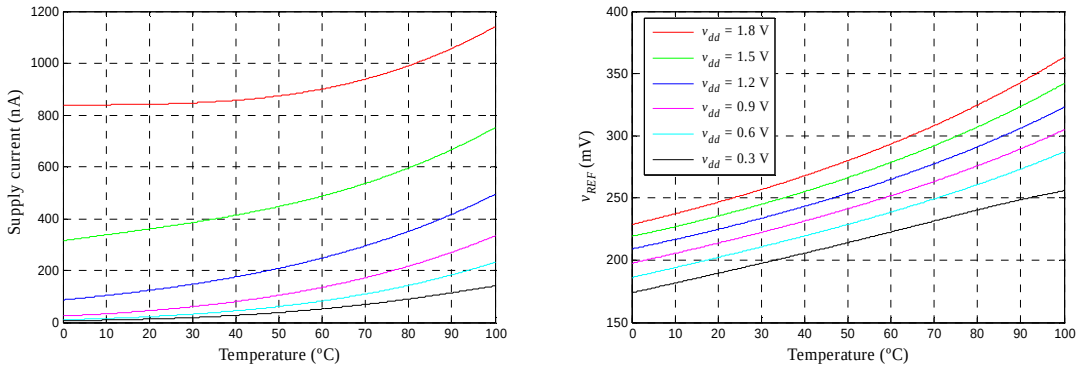


Fig. 5.33 - Temperature dependence of the supply current, and generated voltage reference, for different supplying voltages, for the VRC being used.

5.6.4 Differential voltage amplifier

The topology of the amplifier is shown in Fig. 5.34. This amplifier has a power-down feature (*pd*) to disable it, in order to turn off the voltage limiter circuit. The input stage of this amplifier uses PMOS devices, as the typical values of the input voltage are around 200 mV to 300 mV.

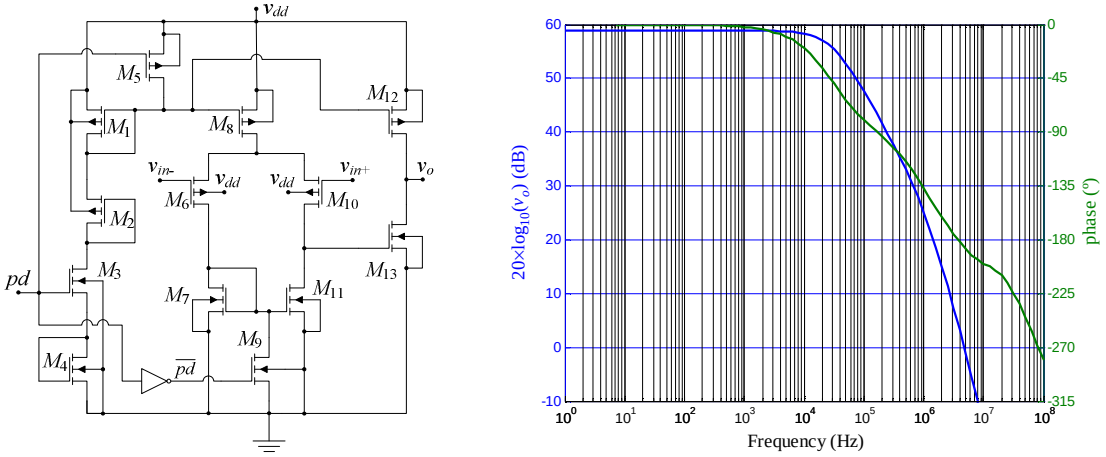


Fig. 5.34 - Differential amplifier circuit: a) schematic, b) frequency response.

5.6.5 Stability analysis

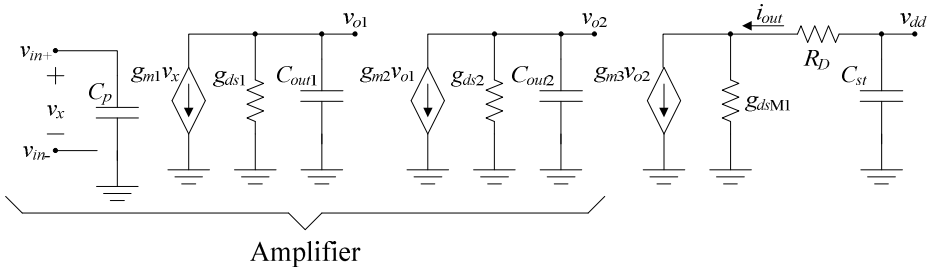
Since this is a closed loop system (Fig. 5.31), it is important to analyze its stability. The feedback network is constituted by R_1, R_2, C_c and C_p (parasitic capacitance at the amplifier input). The feedback factor, β, is given by

$$\beta(s) = \frac{v_{vdd}}{v_{dd}} = \frac{R_2 + sC_cR_1R_2}{R_1 + R_2 + sR_1R_2(C_c + C_p)}. \tag{5.25}$$

The impedance, Z_{22}, of the feedback network from v_{dd} to ground, is

$$Z_{22}(s) = \frac{R_1 + R_2 + sR_1R_2(C_c + C_p)}{(1 + sR_1C_c)(1 + sR_2C_p)}. \tag{5.26}$$

The small-signal model of the amplifier, including the output transistor M_1, is depicted in Fig. 5.35.



$g_{ds1} = g_{ds10} + g_{ds11}$ $\quad C_{out1} = C_{gd10} + C_{db10} + C_{db11} + C_{gs13}$ $\quad (g_{dsM1})^{-1} >> R_D \Rightarrow i_{out} \cong g_{m3}v_{o2}$

$g_{ds2} = g_{ds12} + g_{ds13}$ $\quad C_{out2} = C_{gd12} + C_{db12} + C_{gd13} + C_{db13} + C_{gsM1}$

Fig. 5.35 - Small-signal model of the amplifier and the output M_1 transistor.

As the output variable, i_{out}, is the current drawn from the v_{dd} node, and the input variable is the input differential voltage of the amplifier (v_x), there will be a transconductance function $G_M(s)$ given by

$$G_M(s) = \frac{i_{out}}{v_x} = \frac{g_{m1}g_{m2}g_{m3}}{(g_{ds1} + sC_{out1})(g_{ds2} + sC_{out2})}. \tag{5.27}$$

The impedance seen from v_{dd} to ground, defining $R_o = (g_{dsM1})^{-1} + R_D$, is

$$Z_{out}(s) = Z_{22}(s) // \left(1 \diagup sC_{st} \right) // R_o. \tag{5.28}$$

Let us consider the loop of the system in Fig. 5.31 to be open before the "+" terminal of A_1. Now, by injecting signal in the "–" terminal, and computing the ratio to the signal obtained at the output of the feedback network, the loop gain is

$$G_L(s) = G_M(s)Z_{out}(s)\beta(s). \tag{5.29}$$

This function has four poles and one zero. Their expressions are as follows, considering that C_{st}, connected to the output node, has a value much higher than that of C_c and C_p:

$$\begin{aligned} &f_{p1} = \frac{g_{ds1}}{2\pi C_{out1}}; \quad f_{p2} = \frac{g_{ds2}}{2\pi C_{out2}}; \quad f_{p3} = \frac{1}{2\pi \left(R_o // (R_1 + R_2)\right) C_{st}}; \\ &f_{p4} = \frac{1}{2\pi (R_1 // R_2)(C_c + C_p)}; \quad f_z = \frac{1}{2\pi R_1 C_c}. \end{aligned} \tag{5.30}$$

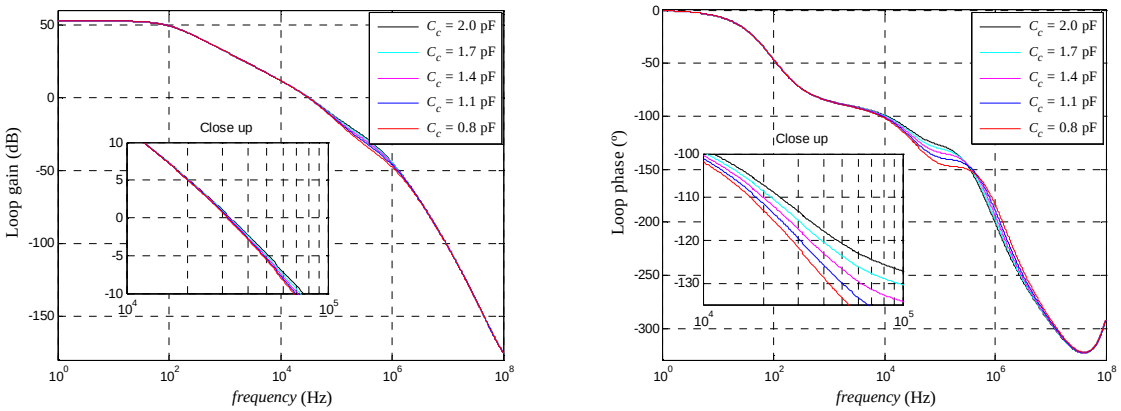
The values of f_{p4} and f_z can be approximately equal, by selecting an appropriate value for C_c, thus canceling out each other, making the system equivalent to having only the other three poles. This is useful in improving the phase margin of the system.

Assuming that R_1+R_2 >> R_o, which is the case, the DC loop gain is given by

$$G_L(0) = \frac{g_{m1}g_{m2}g_{m3}R_2R_o}{g_{ds1}g_{ds2}(R_1 + R_2)}. \tag{5.31}$$

The magnitude and phase of the open loop gain are determined by performing an AC sweep analysis, which is shown next in Fig. 5.36 a) and b), respectively. C_c is swept from 0.8 pF to 2.0 pF, to check what would be the consequence on the phase margin of the system. In these simulations, the value of the storage capacitor, C_{st}, was 1.8 μF.

It can be seen, in the close up inset in Fig. 5.36 a), that regardless of the value of C_c, the zero crossing of the loop gain function occurs at about 32 kHz. As seen by the close up inset in Fig. 5.36 b), at the previous frequency, the spreading of phase values according to the value of C_c, results in a minimum phase margin value of 57º. In order to have an acceptable phase margin value of 60º, the value of C_c was selected to be 1.4 pF. It is important to note that, if the value of C_{st} is increased, the phase margin will also increase.



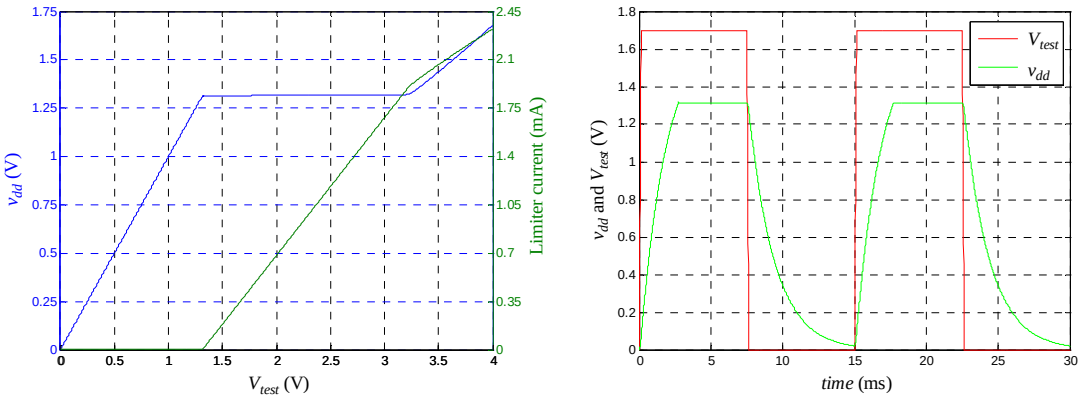
a) b)

Fig. 5.36 - Magnitude and phase functions of the feedback loop circuit of Fig. 5.31.

The value of 1.8 μF, which is a mere commercially available normalized value, is still a relatively small value for a storage capacitor, as it this device can get to units of Farads, or largely more [135]. Thus, this value corresponds to a worst case.

5.6.6 Simulated performance of the voltage limiter

In order to check the behaviour of the voltage limiter circuit, it was simulated in Spectre. In Fig. 5.37 a) and b), there are shown the results of a DC sweep and a transient response, with a period of 15 ms, respectively, so as to demonstrate the correct operation in different ways.



a) b)

Fig. 5.37 - Simulated performance: a) DC sweep response; b) Dynamic transient response.

The function in Fig. 5.37 a) was obtained by running a DC sweep, using V_{test}, on the right hand side of the dashed line in Fig. 5.31. The function in Fig. 5.37 b) was obtained by using a square wave voltage generator in place of V_{test}. As seen in both Fig. 5.37 a) and b), the voltage limiter comes into action whenever the voltage in the v_{dd} node tends to be higher than the limit. The voltage, at which the limitation in v_{dd} is achieved, is about 1.31 V, which is inside the desired limit. In these tests, the supply current of the amplifier was, typically, about 900 nA.

5.7 Conclusions

In this chapter, the design of the proposed energy harvesting system was presented. Moreover, the design of each individual module of the system has been described.

These modules are the SC Voltage Doubler, the Phase Controller, the Local Supply, the Start Up and the Voltage Limiter, as shown by the block diagram of Fig. 5.1. The voltage doubler uses a charge reusing technique in order to reduce the loss because of the bottom plate parasitic capacitance. The phase generator provides the necessary control to the switches in the voltage doubler by using an asynchronous state machine that implements the Fractional V_{OC} MPPT method. The Local Supply is a smaller replica of the main voltage converter, in order to provide a power supply to the inner modules of the system, independent from the main output voltage. The Start Up module is required to start the system up by using the available ambient energy and to provide a power-on-reset signal to initialize the Phase Controller. The Voltage Limiter has the purpose of preventing the output voltage from increasing above a determined level, should the system undergo a much stronger light intensity than the one that served as the basis for system design.

Next, in Chapter 6, the layout of each of these modules will be described, as well as the processes by which the outside world can interact with the integrated prototype, so as to set features or to observe signals.

Chapter 6

LAYOUT OF THE SYSTEM

6.1 Introduction

After the system is defined, and the electrical design of its constituting circuits is concluded, it is necessary to lay out the masks that will define the manufacturing process of the integrated circuit prototype. During the layout process, it is necessary to consider the parasitic effects of the concrete physical implementation of the different circuits, because these can change the performance of the circuits that were previously designed.

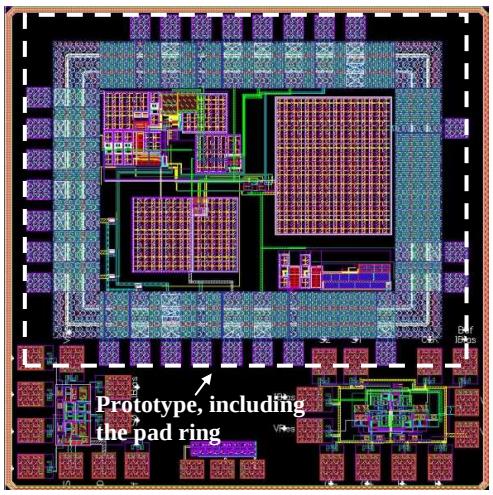


Fig. 6.1 - Entire die layout.

Therefore, the layout process has to take into consideration these non-ideal effects and to include a verification of the exact electrical performance of the circuit by using electrical

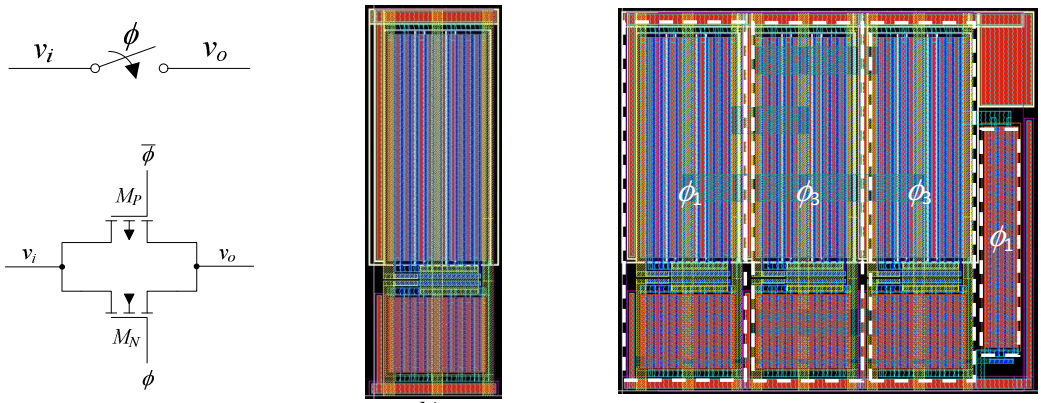
simulations of the circuit extracted from the layout, which includes the parasitic components. This chapter will describe this process. The layout of the entire prototype circuit, in a 130 CMOS technology, located inside the 26-pin pad ring, is shown in Fig. 6.1. The next sections of this chapter will describe the layout process of each constituting block of the prototype integrated circuit.

6.2 SC Voltage Doubler

6.2.1 Switches

When looking at Fig. 5.12, where the SC voltage doubler was presented, it is possible to observe a total of eight switches that perform the switching of the capacitors. Six of these switches are implemented by using a transmission gate. The other two switches, which are the lowest switch in each of the branches, are implemented by using a simple NMOS transistor. The voltage values that are involved in the control of these switches are such that there is no need to use a transmission gate.

The symbol of the switch and the electric circuit of the transmission gate that implements it, are shown in Fig. 6.2 a) and the layout structure of this transmission gate is shown in Fig. 6.2 b). In Fig. 6.2 a), the substrate connection is omitted, but the substrate of the PMOS and NMOS, are connected to v_{dd} and to ground, respectively.



a) b) c)

Fig. 6.2 - Layout of the switches of the SC voltage doubler: a) symbol and electric circuit; b) a single transmission gate and c) the whole set of switches that manages the step-up process in the upper branch of Fig. 5.12.

The upper device of the transmission gate is a PMOS and the lower one is a NMOS. The sizing of the PMOS is $(W/L)_{PMOS}$ = 63 µm / 0.12 µm, using four fingers and a parallel connection of three devices, while for the NMOS, one has $(W/L)_{NMOS}$ = 63 µm / 0.12 µm, using one device with twelve fingers. The need to have three PMOS devices in parallel, is due to their conductivity, which is about three times lower than for a NMOS device with the same size

[162]. This procedure is commonly used throughout the layout of this circuit, when dealing with logic or switching structures. The sizing of these transistors was addressed in Section 5.2.1.1. The upper and lower rails are used to tie the n-well to v_{dd} and the substrate to ground, respectively. The set of four switches that are used in each branch of Fig. 5.12, and are controlled by signals ϕ_1 and ϕ_3, coming the phase (MPPT) controller, are shown in Fig. 6.2 c), for the case of the upper branch. In case of using the lower branch, the phase signals ϕ_1 and ϕ_3 should be swapped.

According to what was mentioned above, in Fig. 6.2 c), it can be observed that there are three transmission gates and one NMOS transistor. This last one, which stands for the switch located in the lowest position in each branch, has its size equal to the NMOS device of the transmission gate. The transmission gate that controls phase ϕ_2, which is responsible for the charge reusing technique, as described in Section 5.2.1, has the same characteristics and structure as the one in Fig. 6.2 b).

6.2.2 MOSFET capacitors

The capacitors used in the voltage converter circuit are implemented using MOSFET devices, as it was mentioned before. The optimum capacitance value was determined in Section 5.3.2.1. Each MOSFET capacitor, of each branch of Fig. 5.12, has a value of 550 pF. Each of these capacitors is built using smaller capacitors connected in parallel. This strategy allows for a more flexible layout procedure.

The capacitors in the two branches were laid out using the common centroid technique [162], [163], [164], in order to reduce the mismatch between them. This technique results in variations in the manufacturing process affecting both capacitors in the same way, thus guaranteeing a good matching between the capacitance values.

Fig. 6.3 a) represents the conceptual principle that served as the basis for the layout of the MOSFET capacitors. It consists of four individual capacitors, each having (W/L) = 50 μm / 2 μm, each of them with four fingers. The capacitors associated to each elemental capacitor are laid out diagonally, in a single structure, as depicted in Fig. 6.3 b).

Thus, this unitary structure contains the two elemental capacitors, one of each branch, named C_1 and C_2. Each of the elemental capacitors, C_1 and C_2, has a capacitance of 2.2 pF. This value was determined by simulating, using Spectre, the circuits of Fig. 6.3 a), biased with 0.6 V.

The connections to this capacitor are placed such that when the capacitors are positioned side by side, vertically or horizontally, each capacitor is connected to its neighbors and a larger capacitor, formed by the parallel connection of all the smaller capacitors, is automatically

obtained. Fig. 6.3 c) shows the whole set, containing both of the capacitors of the switched branches.

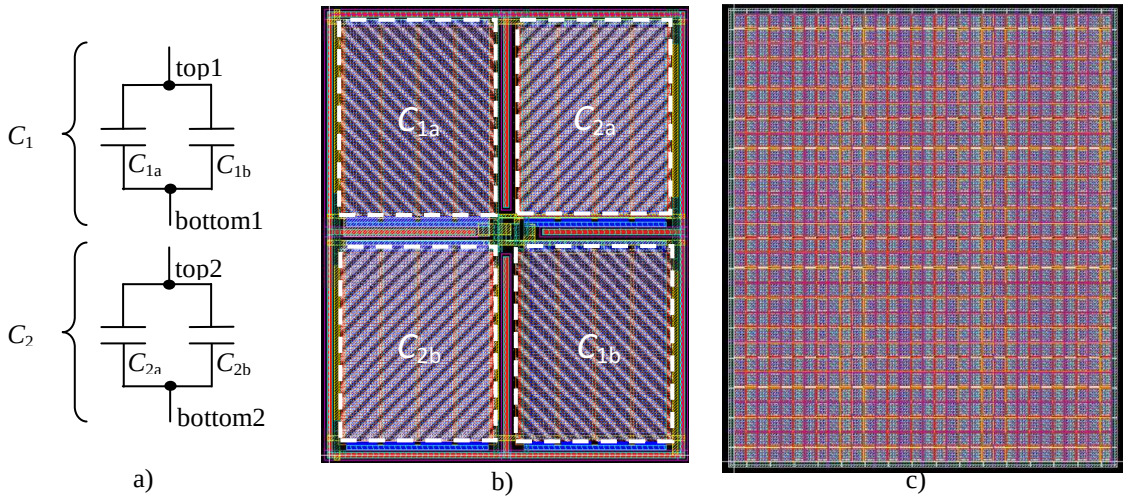


Fig. 6.3 - Layout of the MOSFET capacitors: a) concept; b) single structure; c) complete structure.

Here, as a consequence of the adopted elemental structure, the two capacitors form like a chess pattern interleaved with each other, vertically and horizontally. The top and the bottom plates of each of the capacitors are accessible through four metal rings, each at a different metal layer, all of them, around the complete structure. The purpose is to make any of the plates accessible at any place, all around. Because of the size of the complete MOSFET capacitors, which are the biggest of the modules in this system, it is important to have this spatial flexibility for accessing the terminals of both C_1 and C_2.

In addition to the MOSFET capacitors themselves, the elemental structure of Fig. 6.3 b) has several layers of parallel metal plates placed on top of it, so as to have a structure similar to a MoM capacitor. It was possible to stack three pairs of metal plates, allowing for an additional capacitance to that of the MOS capacitors without an increase in area. Also, the capacitance introduced by the metals is linear, such that the total capacitance is a combination of linear capacitance of the metals and the non-linear capacitance of the MOSFET capacitors.

According to the results of the electrical simulations of the extracted capacitor circuit, including the capacitances from the additional metal layers, the total capacitance of the elemental structure is 2.35 pF, thus increasing by 150 fF, when compared to the case of having only MOSFET capacitance. When compared to the initial estimation, this increase in the original capacitance allowed for saving an area of about 7%, while maintaining the same expected capacitance for the complete structure. The layout area occupied by the structure in Fig. 6.3 c) is 0.1697 mm^2, by using this structure of metal capacitance added to MOSFET capacitors.

When looking at the final structure, there are (16×15) elemental structures, giving a total capacitance of 564 pF. This is 2.5% more than the originally calculated, i.e. 550 pF. This little increase in the total capacitance, as explained in Section 5.3.2.1, benefits the efficiency.

The elemental capacitor layout structure of Fig. 6.3 b) is used in many places in the layout of the system, whenever there is the need to have decoupling capacitors. Since the MOSFET capacitors have a good capacitance density, these have been the ones used in this system, for decoupling purposes. One example of such use is shown next, in Section 6.3.3.

6.3 Phase Controller

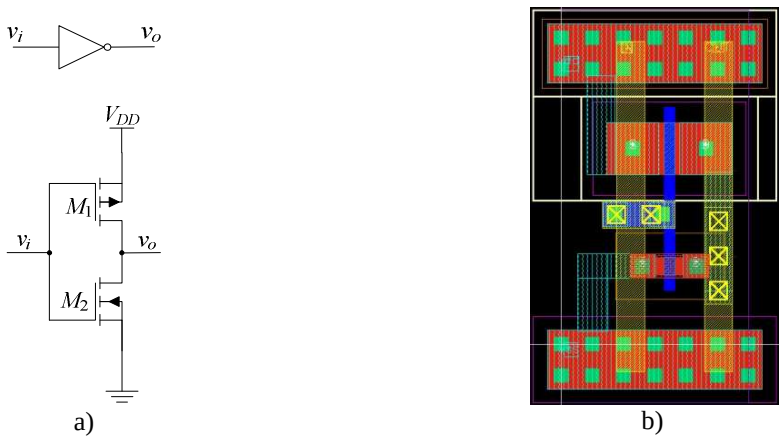
The phase controller is the module that implements the MPPT algorithm and that controls the frequency and the timing of the switches, allowing for the system to operate optimally. This control is done through the operation of the ASM, whose details were presented in Section 5.3.2. More generally, the operation of the phase controller circuit is described in Section 5.3.

The circuit of Fig. 5.17, implementing the phase controller, has a diversity of individual structures. This circuit comprehends logic gates, delay circuits, comparators and a voltage divider and its decoupling capacitor.

6.3.1 Logic gates

The logic gates used in the ASM are of various types. The most basic of them is the logic inverter (NOT). There are also AND gates, OR gates and S-R latches.

The logic inverter uses two MOSFET devices with the minimum length allowed by the technology, in order to obtain the smallest area and power dissipation possible. The sizes of the devices are $(W/L)_{NMOS}$ = 0.2 µm / 0.12 µm and $(W/L)_{PMOS}$ = 0.6 µm / 0.12 µm. The electric circuit and the layout of the inverter are shown next, in Fig. 6.4.



a) b)

Fig. 6.4 - Logic inverter: a) logic symbol and electric circuit; b) layout.

The AND gates were implemented by cascading a NAND gate with a NOT gate. All of the MOSFET devices involved have the same sizes as those just discussed above for the logic inverter, depending whether these are PMOS or NMOS. The electric schematic and the final layout of the AND gate are shown in Fig. 6.5.

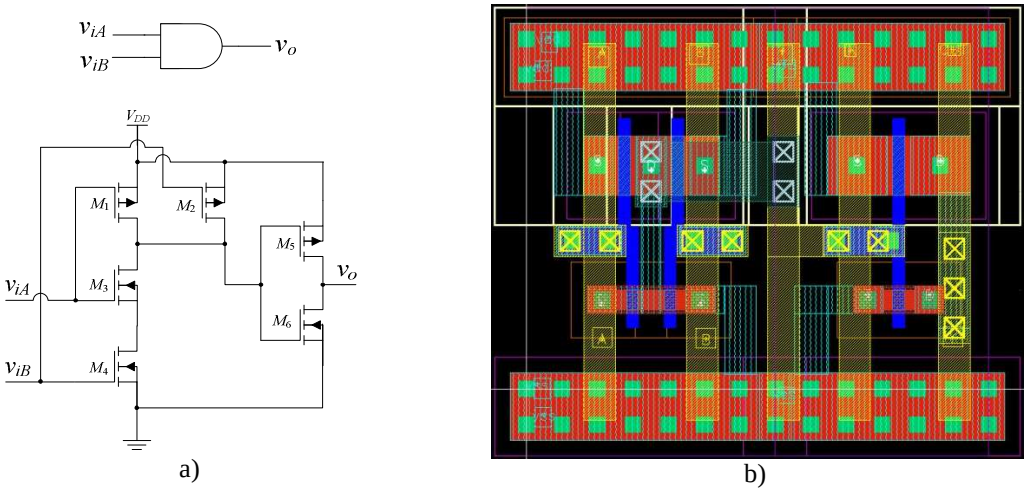


Fig. 6.5 - AND logic gate: a) logic symbol and electric circuit; b) layout.

As for the OR logic gate, just like for the AND gate, this structure uses a NOR gate cascaded with an inverter to obtain its logic function. This is shown next in Fig. 6.6.

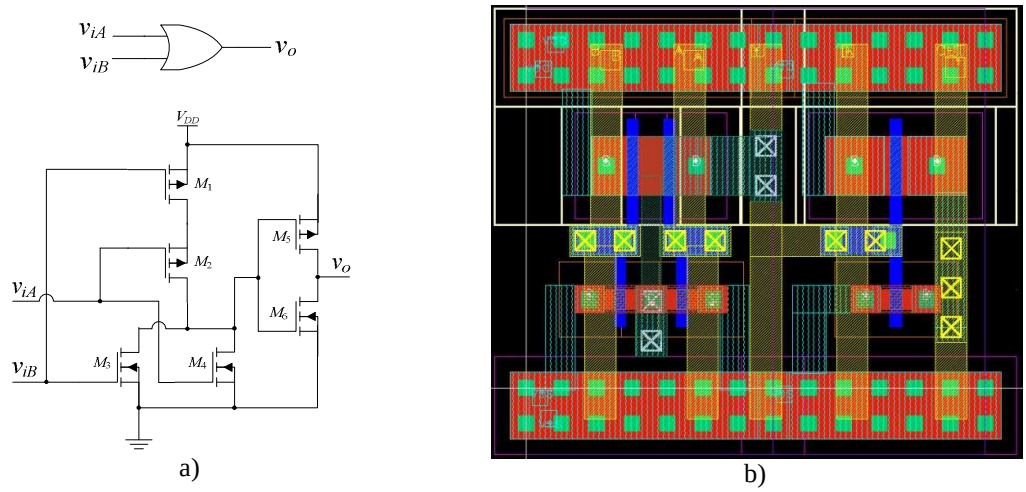


Fig. 6.6 - OR logic gate: a) logic symbol and electric circuit; b) layout.

The last structure in the ASM that is made entirely from logic gates is the S-R latch. This logic structure uses two NOR gates, as shown in Fig. 6.7.

6.3.2 Delay circuits

As already mentioned in Section 5.3.1 and shown in Fig. 5.19, there are four delay circuits that determine the minimum duration of each state in the ASM, as well as they define the duration of phase ϕ_2.

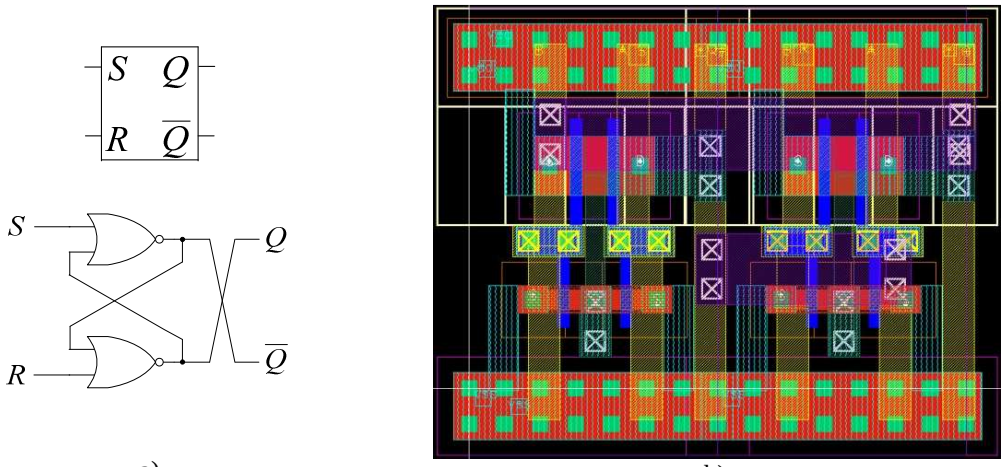


Fig. 6.7 - S-R latch: a) logic symbol and internal logic circuit; b) layout.

There are two amounts of delay that are introduced into the cycle of the ASM. The first one is the minimum duration of *state1* or *state3*, while the second one is the duration of phase ϕ_2. When considering that this delay circuit is being supplied with 1.2 V, the durations of these delays are approximately 12 ns and 18 ns, respectively. These timings are achieved by using a MOSFET capacitor of approximately 100 fF and 160 fF for each case, respectively. By assigning this capacitor (C_{delay}) a given capacitance value, it is possible to control the amount of the desired delay. The values that were presented were adjusted empirically, according to simulations in Spectre, using the "*Typical*" corner, while observing the performance and the behavior of the ASM. The capacitor C_{delay} is a MOSFET capacitor, with one of the two values previously mentioned, which is laid out immediately next to the left-hand side of the layout of the rest of the delay circuit, which is depicted in Fig. 6.8. In this layout, C_{delay} is not included.

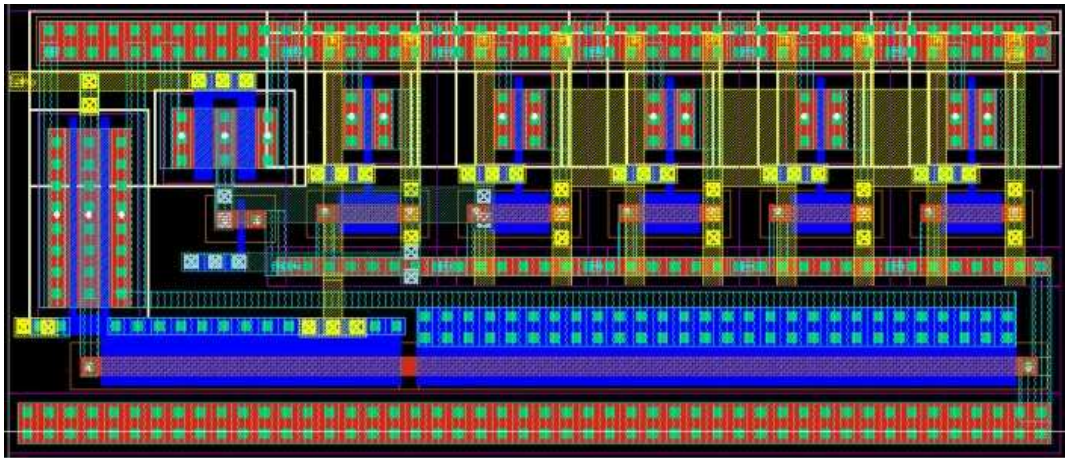


Fig. 6.8 - Layout of the delay circuit, except for the MOSFET capacitor that defines the amount of delay.

The inverters used in the delay circuit have different sizing from those used in the logic gates. The former have longer channels in order to add some more delay.

6.3.3 Voltage divider and its respective decoupling

As it was described in Section 5.3.2, it is necessary to guarantee that the switched MOS capacitors, when connected to the PV cells, are charged to at least 95% of the input voltage value ($v_{MOSa} > v_B$ and $v_{MOSb} > v_B$). This reference percentage is obtained by applying v_{in} to a voltage divider with a ratio of the same value. Moreover, since this voltage is applied to the comparator circuits, and it should be as stable as possible, the output of the voltage divider is conveniently decoupled. The electric circuit and its layout are shown in Fig. 6.9 a) and b), respectively.

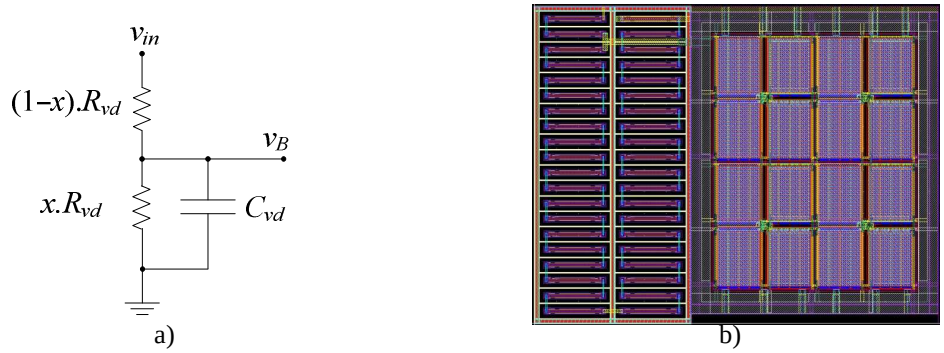


Fig. 6.9 - a) Schematic and b) layout of the voltage divider that provides v_B (95% of v_{in}).

In this circuit, $x = 0.95$. The total amount of resistance of the voltage divider, R_{vd}, is limited to 1 MΩ because increasing this resistor further would not result in a significant power reduction, but would result in an unacceptable large area. The physical resistance is obtained by putting in series forty resistors, each of them, with about 25 kΩ. These can be observed at the left-hand side of Fig. 6.9 b). The decoupling capacitor, located at the right-hand side of Fig. 6.9 b), is made from the same structures as the ones that were used for the MOSFET switched-capacitors. The main difference, in the case of this module, is that the two independent capacitances were connected in parallel, so as to have twice the capacitance of a single capacitor. Thus, the total amount of decoupling capacitance is about 4×2×2.35 pF = 18.8 pF.

The area of this simple structure occupies a large part of the layout of the phase generator, with about 6650 μm^2.

6.3.4 Comparator circuits

The comparators used in the ASM were adapted from [163], but have a power-down feature that allows them to be switched-off, while its use is not needed. The schematic of the comparator circuit was shown in Fig. 5.20.

As this is a differential circuit, special care must be taken while laying it out. The differential sections of the circuit, like those involving M_7–M_8 and M_{23}–M_{24}, were laid out by

using the common centroid technique. By doing so, the matching between the two sides of the differential pair is improved, allowing for the circuit to have a smaller offset voltage. In addition, in the differential sections, dummy elements were used, in order for the boundary of each element to be the same, once again, improving the matching between the two signal paths in the comparator.

The sections of the circuit involving M_3–M_9, M_5–M_{12}, M_6–M_{17}, M_{21}–M_{22}, M_{13}–M_{14} and M_{18}–M_{19} were also laid out employing the common centroid technique, so as to ensure a symmetry, as best as possible, between each of the transistors in these pairs.

The logic inverters that are used to generate the output voltage and to negate the power-down (*pd*) input signal, are exactly the same as those previously explained. When the *pd* signal is HIGH, the amplifier is enabled to work, or disabled, otherwise.

The total area of the layout of this circuit is about 704 μm^2 and it is shown in Fig. 6.10.

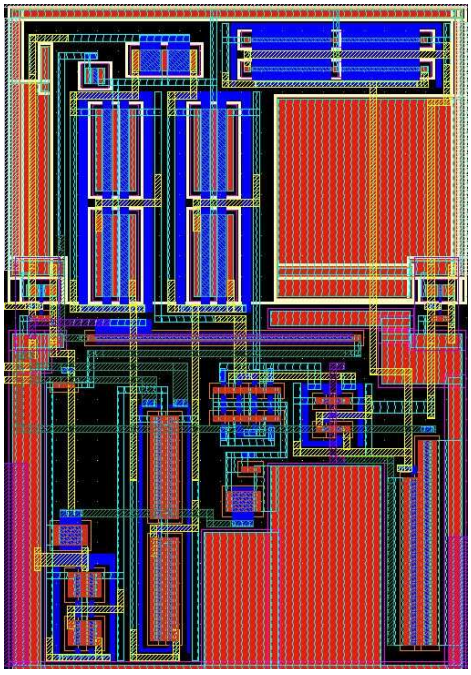


Fig. 6.10 - Layout of the comparator circuit.

Since the current drawn by the comparator can be very high during the comparison time, a local decoupling capacitor is added between the v_{dd} and the ground nodes of this circuit. This capacitance, once again, uses the basic structure of the MOSFET capacitors used for decoupling other structures, with the capacitors connected in parallel. The total decoupling capacitance for each comparator is 2×2×2.35 pF = 9.4 pF. This capacitor is shown in Fig. 6.11: one half located below the comparator circuit and the other half located above it. Fig. 6.11 shows the whole layout of the phase generator. The total layout area of the MPPT phase generator, including interconnections, is 0.0213 mm^2.

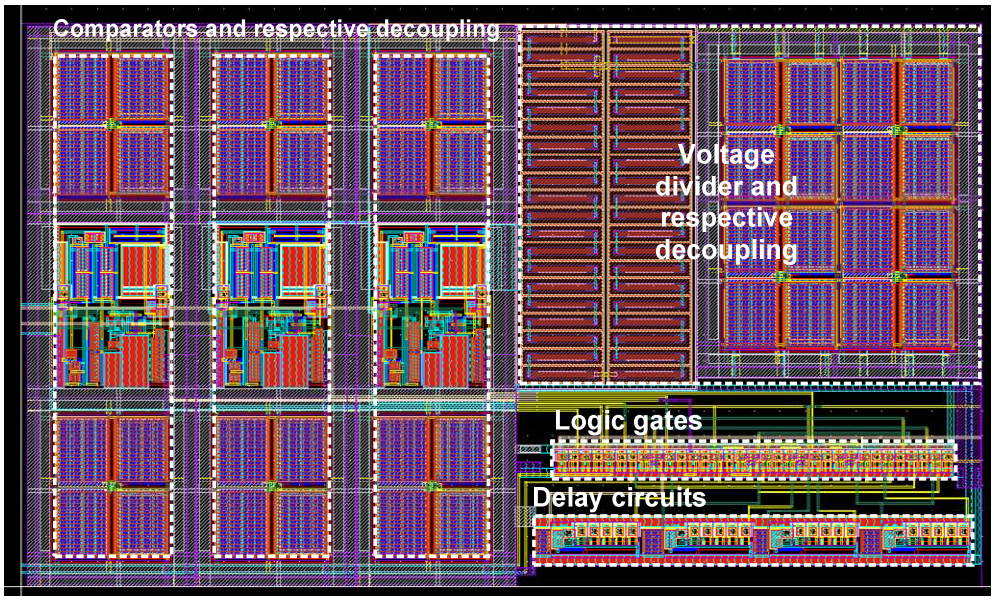


Fig. 6.11 - Complete layout of the MPPT Fractional V_{OC} phase controller circuit.

6.4 Local Supply

The local supply strategy, as explained in Section 5.4, allows for the system to be immune to the load variations. This module is, basically, a smaller replica of the main SC doubler of Fig. 5.12, having the switches and the switched-capacitors, scaled down to 20% of the size of the main circuit, as determined before. The layout of this module can be observed next, in Fig. 6.12.

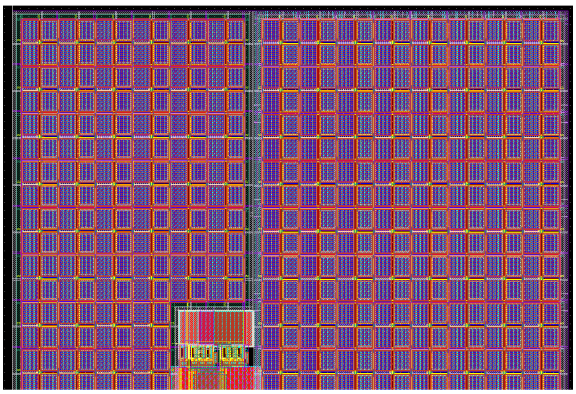


Fig. 6.12 - Layout of the local supply module.

In addition to the local supply SC circuit, it is necessary to use a decoupling capacitor to stabilize the local power supply voltage (v_{dd}). It was decided that the value of this capacitance should be at least 300 pF. Thus, the decoupling capacitance uses sixty four elemental structures like those of Fig. 6.3 b), with the individual capacitors connected in parallel, so as to have twice the value of a single capacitor. As such, the total amount of decoupling capacitance is 64×2×2.35 pF ≈ 301 pF. The total die area occupied by the Local Supply and the associated decoupling capacitance is 0.0839 mm^2.

6.5 Start Up circuit

Next, in Fig. 6.13, the layout appearance of the Start Up circuit is shown.

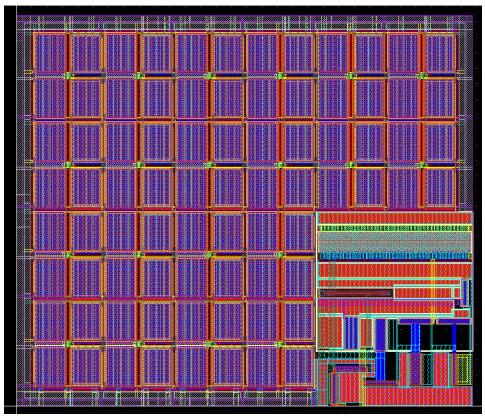


Fig. 6.13 - Layout of the start-up circuit.

The start-up circuit, whose schematic is shown in Fig. 5.28, occupies an area of 0.0189 mm^2. Similarly to the approach that was followed in the Local Supply module, the timing capacitor uses twenty elemental structures like those of Fig. 6.3 b). In this module, just like for several other situations, the two independent capacitances were connected in parallel, to have twice the value of a single capacitor. Thus, the total capacitance of this capacitor is about 20×2×2.35 pF ≈ 94 pF. This capacitor occupies most of the area of this circuit, while the remaining transistors and substrate connections are laid out in the lower right-hand corner of the area occupied by this module.

6.6 Voltage Limiter circuit

The layout of the Voltage Limiter circuit, presented in Section 5.6, is described next.

6.6.1 Voltage Reference Circuit

The layout concerning the VRC, which makes part of the circuit depicted in Fig. 5.31, is shown in Fig. 6.14.

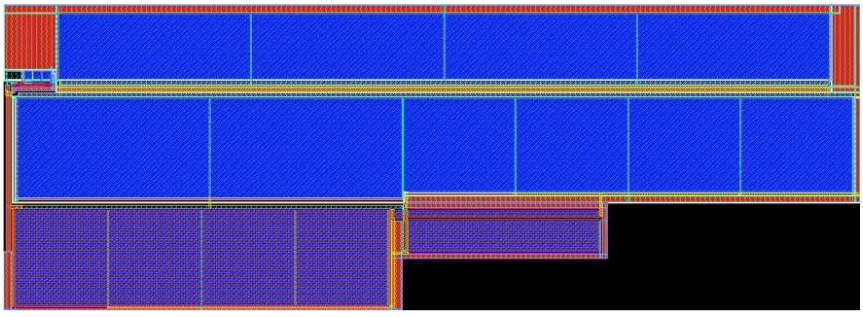


Fig. 6.14 - Layout of the voltage reference circuit.

This layout corresponds to the circuit shown in Fig. 5.32 a). The original circuit was laid out in the 180 nm technology [161] and the present one uses the technology of 130 nm. The original sizing of the transistors is documented in [161]. The layout of the present VRC occupies an area of 15647 μm^2.

6.6.2 Differential voltage amplifier

In Fig. 5.31, one element of the schematic is a differential voltage amplifier, which amplifies an error voltage. In Fig. 6.15, it is shown the layout of this differential amplifier circuit.

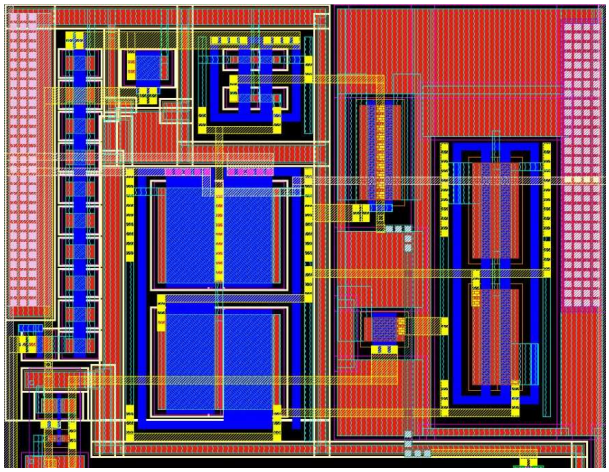


Fig. 6.15 - Layout of the differential amplifier circuit.

This layout corresponds to the circuit shown in Fig. 5.34 a). In this circuit, there are also some differential pairs, as in the comparator circuit of Fig. 5.20, whose layout is shown in Fig. 6.10. Thus, the common centroid layout technique was used once again for this amplifier, just like before, for the comparator. The total occupied area is 500 μm^2.

6.6.3 Complete layout of the Voltage Limiter circuit

The complete layout of the limiter circuit, corresponding to the entire circuit shown in Fig. 5.31, with the identification of the individual modules, can be observed in Fig. 6.16.

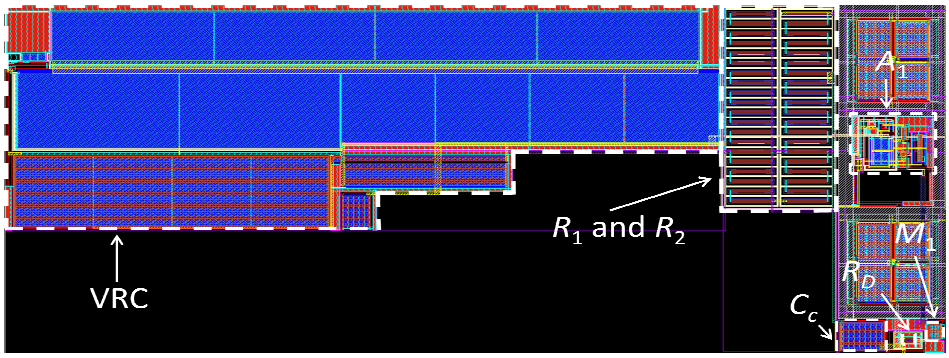


Fig. 6.16 - Layout of the complete voltage limiter circuit.

This layout occupies a total area of 22435 μm^2, in which 4278 μm^2 correspond to the combined layout area of the differential amplifier, its decoupling using MOS capacitors, the compensation capacitor, transistor M_1 and R_D. An area of 15647 μm^2 is assigned to the VRC, and the remaining 2510 μm^2 are occupied by the resistive voltage divider.

6.7 Overall circuit and pin assignment

The total die area occupied by the circuit, accounting for the modules that have been described so far, yet excluding the Voltage Limiter circuit, is summarized next, in TABLE 6.1.

TABLE 6.1 - Partials and total layout areas.

Module	Area (mm^2)
Main MOS capacitors	0.1697
Local Supply and respective decoupling	0.0839
Start-up	0.0189
Switches	0.0019
Fractional V_{OC} phase generator	0.0213
Total	0.2957

+ 5% (interconnections) = 0.31 mm^2

In order to better illustrate the relation of the areas occupied by the various modules, Fig. 6.17 shows the percentage of the total area assigned to each one of them.

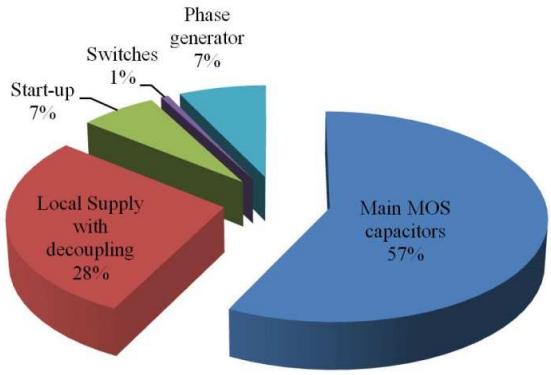


Fig. 6.17 - Relative area occupied by each module.

The voltage limiter was not included in the total value because, in the real situation, as it will be seen in Section 7.2, there was no need to use this module. Moreover, the spatial distribution of the modules was only with prototyping purposes, so the area used for interconnections was also included, and an estimation of 5% of the sum of the area of the individual modules was considered. As such, the total occupied die area is 0.31 mm^2. If the concern was to have a final product, it would make sense to place the modules tight together, so as to have a smaller occupied area. From the total, the area occupied by MOS capacitors, for the

SC step-up circuits and for decoupling the local power supply voltage, is about 0.2536 mm^2. If, instead of MOS capacitors, MiM capacitors had been used, the area would have been about eight times larger [17], i.e. 2.03 mm^2, which is quite significant.

The entire system layout and a die photograph of the prototype integrated circuit are shown next in Fig. 6.18. The silicon die with the prototype circuit was glued to a PCB and its pads connected directly to the latter by using bond wires, as it can also be observed.

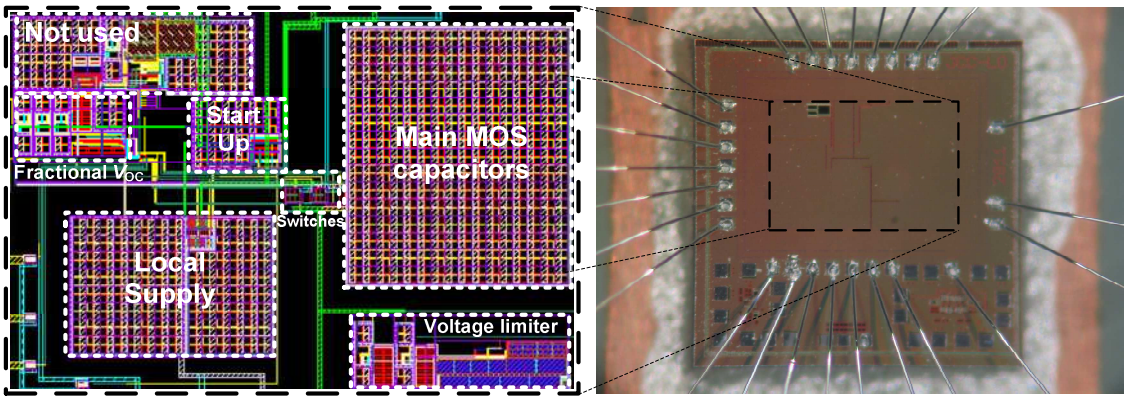


Fig. 6.18 - Layout of the system and die photograph.

A pad ring, which can be clearly identified in Fig. 6.1, is used to interface the prototype to the outside world, as well as to protect it against electro static discharge (ESD). Each input and output has an assigned pin, as well as for auxiliary signals for prototype testing purposes. Also, there are multiple ground pins to keep this node the more accessible as possible by the individual modules. All of these requirements had an influence in the distribution of the modules, forcing them to be located in accordance to the physical pin. Fig. 6.19 shows the pin assignment, as well as the pad ring that surrounds the system.

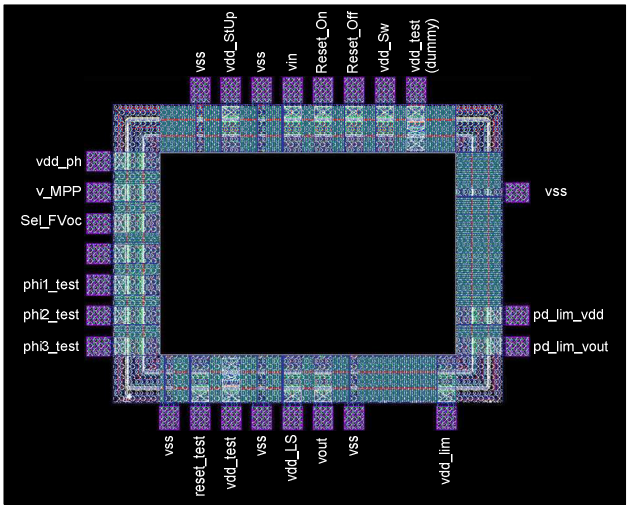


Fig. 6.19 - Pad ring and pin assignment.

The functionality of each pin is explained in TABLE 6.2.

TABLE 6.2 - Designation and functionality of each pin.

Pin designation	Functionality
vss	Ground terminal
vdd_StUp	Supplying terminal of the Start Up module
vdd_ph	Supplying terminal of the Phase Controller module
vdd_Sw	Power tying terminal of the set of switches and the switched MOS capacitors
vdd_LS	Output pin of the Local Supply module
vdd_lim	Supplying terminal of the Voltage Limiter module
vdd_test	Supplying terminal of the buffers that drive the phases and reset signals to the outside, for observation and measurement
vdd_test (dummy)	Auxiliary terminal for vdd_test, to distribute this supplying voltage over the pad ring
vin	Input voltage of the step-up voltage doubler (v_{in})
vout	Output voltage of the step-up voltage doubler (v_{out})
v_MPP	Input for the voltage corresponding to the maximum power point (v_{MPP})
Reset_On	Test pin to hold the *reset* signal HIGH (in case of failure of this module)
Reset_Off	Test pin to hold the *reset* signal LOW (in case of failure of this module)
Sel_FVoc	Input selection to enable the Fractional V_{OC} MPPT phase generator
pd_lim_vdd	Power-down feature for the limiter of the vdd_LS voltage
pd_lim_vout	Power-down feature for the limiter of the vout voltage
phi1_test	Buffered output signal, corresponding to phase signal ϕ_1
phi2_test	Buffered output signal, corresponding to phase signal ϕ_2
phi3_test	Buffered output signal, corresponding to phase signal ϕ_3
reset_test	Buffered output signal, corresponding to the *reset* signal

In order to give a clearer idea of how these pins interconnect to the system modules, the following diagram is shown.

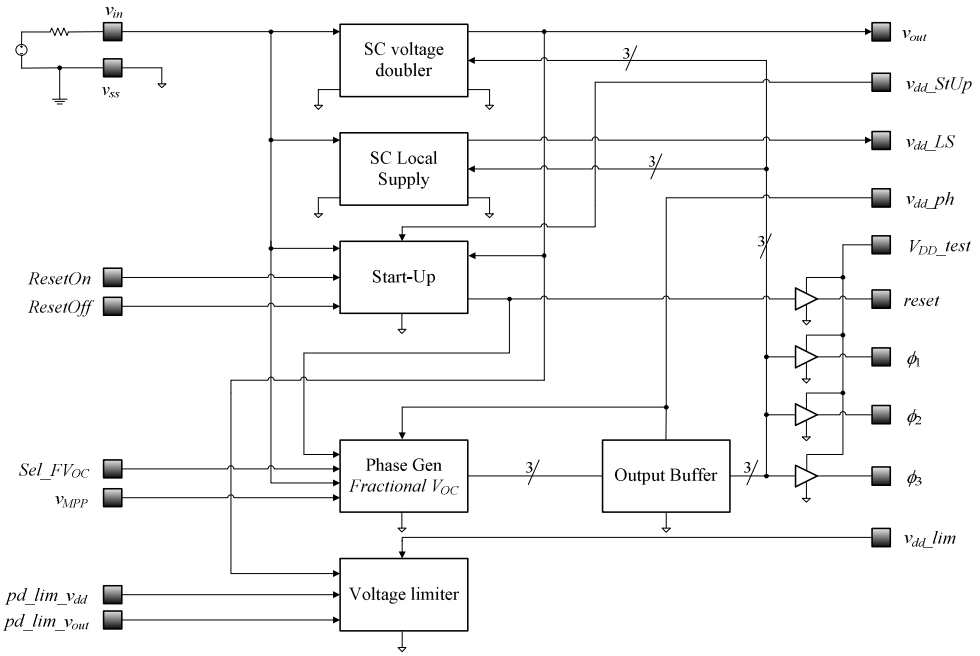


Fig. 6.20 - Pin diagram for interconnection to the prototype PCB.

The input signals *ResetOff* and *ResetOn* only exist for a precaution purpose at a prototyping level, to provide a way to unstuck any situation that does not allow for the system to

start, in case of failure of the Start Up module. These signals are to be kept at logic 1 and 0, respectively, for normal circuit operation.

The *vdd_test* pins are used to power the test buffers that drive the phase signals, as well as the *reset* signal, to the output, in order for these signals to be conveniently observed and measured by an oscilloscope or multimeter, as it will be explained in Section 7.2.2.

The pin *Sel_FV*$_{OC}$ serves to turn ON or OFF the phase generator that implements the *Fractional* V_{OC} MPPT method. If this module is to be disabled, the ASM will be stopped in its initial state (see Fig. 5.16), thus not dissipating any power, because of the absence of dynamic operation. With respect to comparators, these will be disabled, by using their power-down feature. The output phase signals are connected to a set of three buffers. These buffers drive the phase signals to the switches of both the main and the Local Supply SC voltage doublers. The structure of this array of buffers is shown next in Fig. 6.21.

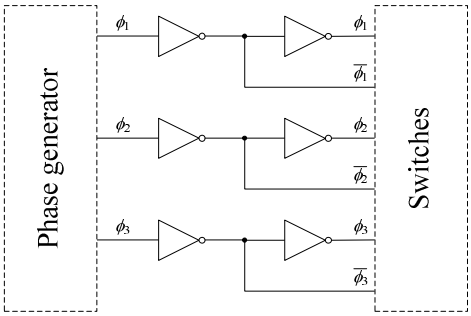


Fig. 6.21 - Array of buffers to drive the switches of both SC voltage doublers.

The main difference between these inverters, and the ones already described, is their size. These have $(W/L)_{PMOS}$ = 3 µm / 0.12 µm and $(W/L)_{NMOS}$ = 1 µm / 0.12 µm. The reason for this sizing stems from the need to conveniently supply or sink the charges for the total parasitic capacitance of the switches of both doubler circuits.

The layout of this structure, which was used as a single module, as of Fig. 6.20, is shown in Fig. 6.22. The total area that it takes is about 100 µm^2.

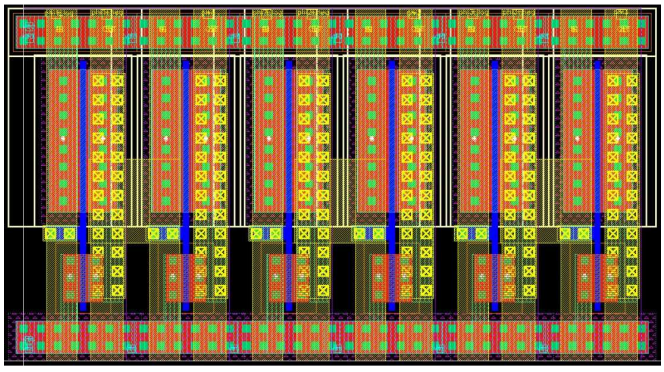


Fig. 6.22 - Layout of the set of output buffers.

The supplying strategy was to power each individual module by distributing the output voltage generated by the Local Supply step-up converter (v_{dd}_LS, which has been formerly designated as v_{dd}). This distribution is achieved at the board level, by connecting v_{dd}_LS to the supplying terminals of the other modules. By having an individual power supply terminal for each module, it allows for a separate analysis of the power being dissipated, if desired. This explains because there are terminals such as: v_{dd}_StUp, v_{dd}_ph and v_{dd}_lim, when in fact, all of these are the already known v_{dd}.

Similarly, there was also the need to have a distributed ground, so to speak. Physically, each module has a ground pin (v_{ss}) close to it, so as not to concentrate the ground terminal in one pin alone.

6.8 Extracted layout simulation

During the layout procedure, it is necessary to comply with the designs rules, which are tested by running the design rule check (DRC) tool and also to perform the layout versus schematic (LVS) verification at the end of the layout of each module. Moreover, if any problem should subsist, and the layout does not fully match the original electric schematic, the designer can be sure that the odds of having a working circuit are practically non-existent.

With the system completely and correctly laid out, having the DRC and LVS tests passed with success, the next step is to check if indeed the circuit, which is now at the physical level, is functional according to what it is expected to do. Having such a structure, which is not ideal anymore, the designer may wonder whether the physical realization of the circuit will still comply with the desired performance. Thus, a test can be performed by running simulations just as before, but now with the non-ideal characteristics that were added when building up the physical structure, and that distinguishes it from the original electrical simulations at the schematic level.

The parasitics associated to the layout of the circuit are obtained using an extraction tool. This software allows for extracting the resistances, the capacitances or the combination of both, which now make part of the actual electrical circuit, as a natural consequence of its physical realization. The extraction of resistances leads to a very large netlist and adding the parasitic resistors would not cause a significant deviation of the behavior of the circuit, so only capacitances were extracted, because the overall system is already considerably large and a simulation of it would be very time consuming.

As a result of the extraction, a new netlist is created, containing not only the devices that already were part of the original modules, but also new parasitic capacitances, that are added

due to the extraction process. These capacitances exist between nodes and from the various nodes to the substrate. In addition to having the parasitic capacitances, the pads used in the padring are also considered, and its netlist is also used, so as to have a match as best as possible to the actual physical system.

With all the necessary conditions gathered, a simulation of the extracted circuit was performed, just to chek if the system was able to start-up and to reach a working steady-state. The input voltage source was set to 1 V and the MPP voltage to 0.5 V. The load being supplied (R_L) has the value of 50 kΩ. A transient simulation was started and taken up until 1 ms. The resulting waveforms for the input voltage (v_{in}), Local Supply output voltage (v_{dd}) and system output voltage (v_{out}), are shown next in Fig. 6.23, as in the actual simulator program.

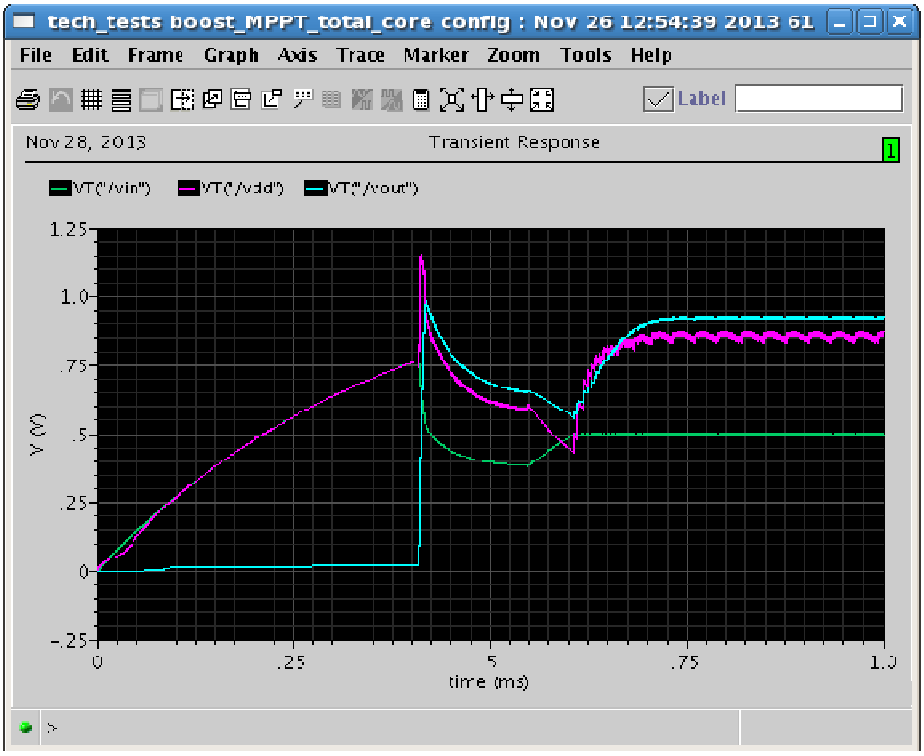


Fig. 6.23 - Transient evolution of voltages v_{in}, v_{dd} and v_{out} during the extracted layout simulation.

It can be seen that the input voltage, in the steady-state, is around 0.5 V, which is the value of the MPP voltage. This shows that the ASM is correctly working, since the MPPT method is achieving the goal of making the input voltage to equal the MPP voltage. This voltage is then increased by the step-up converter. The simulation being shown lasted for more than two days and four hours to complete, under a conservative profile, so as not to lose too much information.

The results shown by the graphs in Fig. 6.23 foresee that the system, after fabrication, will be likely to work as expected.

6.9 Conclusions

The layout of the individual modules that make part of the energy harvesting system was described in this chapter. Each of the modules that make part of the block diagram shown in Fig. 5.1 had their layout shown, as well as the individual constituting structures.

An approximate area value was presented for each module and for the complete structure, including the interconnections between modules. The total area is about 0.31 mm^2.

A padring was used, in order to protect the integrated structures from ESD when the integrated prototype is to be manipulated for PCB assembly and further testing.

The layout of the complete system had its capacitive parasitics extracted, enabling for the simulation of the energy harvesting system at the layout level. This simulation indicated that the system was able to start-up and to track the MPP voltage, thus indicating that the ASM and the MPPT method are working. This fact allows for having a good expectation about how this real physical energy harvesting system will perform. This will be desbribed next, in Chapter 7.

Chapter 7

EXPERIMENTAL EVALUATION OF THE PROTOTYPE

7.1 Experimental prototype

In order to experimentally evaluate the integrated circuit prototype, a printed circuit board (PCB) was designed. This PCB allows to access all the pins of the prototype IC and also connects the prototype to external components and auxiliary voltages. In addition to the functionalities described in TABLE 6.2, there is also the possibility to establish initial conditions to the device under test (DUT), which is illustrated in Fig. 7.1.

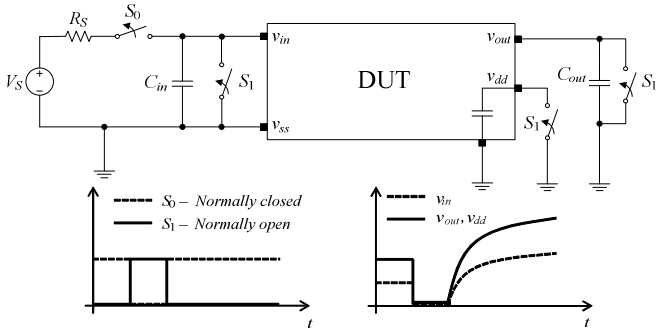


Fig. 7.1 - Establishment of initial conditions to the voltage doubler system.

The switches identified as S_0 and S_1 are implemented in the PCB using commercially available analog switches (74HCT4066D). When the test switches S_0 and S_1 are actuated, the

voltage source (PV cells) is disconnected from the input of the system, and any capacitors present at the input and output pins are discharged, bringing these nodes to a 0 V condition. When the test switches are not actuated, they rest in their default position, allowing for the system to work as expected.

The prototyped integrated circuit was glued to a small PCB, which is designated as “daughter board”. This allows for having more than one daughter board, each with a different sample of the prototype system. These daughter boards can be easily connected or disconnected from the main PCB (the “mother board”), thus allowing to test multiple samples with minimum inconvenience. The layout of this board is shown in Fig. 7.2 a) and the picture of a daughter board with a sample attached to it, is shown in Fig. 7.2 b). The prototyped silicon die is glued to the center of the board and the electrical connections between the board and the die are made using bonding wires. On top of the die and the bond wires there is a transparent plastic for protection.

a) b)

Fig. 7.2 - Daughter board: a) PCB layout and bond connections; b) photograph of a fully assembled unit.

The “mother board”, contains the circuitry to perform the tests and measurements that are required to assess the performance of the prototype, as well as the interconnections to the daughter board, and is shown next in Fig. 7.3. In this figure, it is possible to observe a daughter board at the center of the mother board.

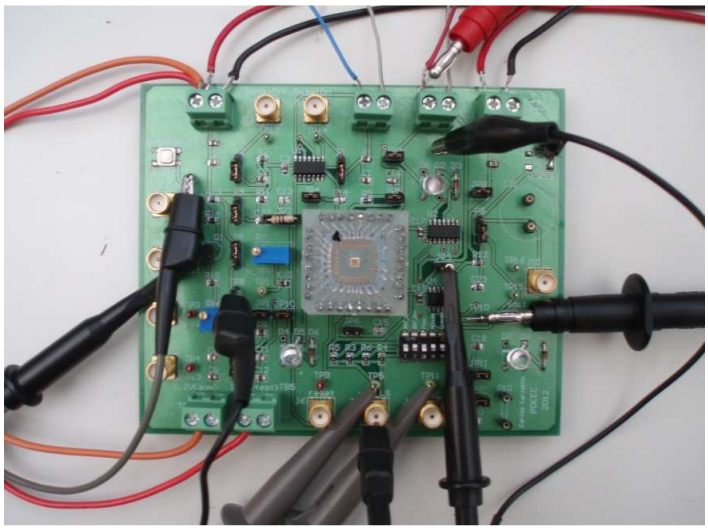


Fig. 7.3 - Complete PCB (mother board), during the tests campaign.

To conclude the presentation of the experimental prototype, Fig. 7.4 shows the whole experimental workbench, in which it can be seen, in addition to the prototype PCB, the laboratorial equipment that was used to obtain the results.

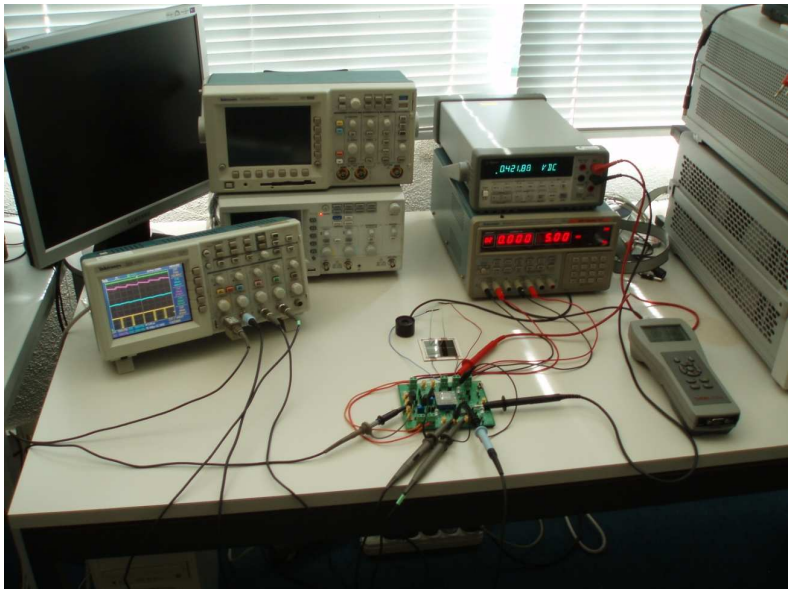


Fig. 7.4 - Experimental apparatus.

7.2 Experimental results

This section presents the tests and the results that were obtained from the laboratorial evaluation of the prototype that has been designed and manufactured.

7.2.1 Experimental evaluation of the Start Up circuit

The experimental setup for the test of the Start Up module is shown in Fig. 7.5.

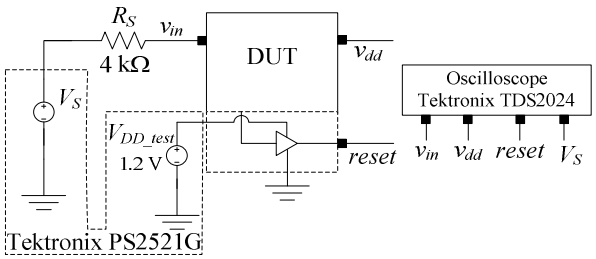


Fig. 7.5 - Experimental testing setup for the Start Up module.

The DUT is the energy harvesting system, which is connected to V_S, through a resistor of 4 kΩ, so as to simulate the PV cells.

Since the transient current and energy used by the circuit during start-up are very small and difficult to measure, these values were estimated by running electrical simulations of the circuit, using Spectre. After start-up, the current drawn by the circuit is negligible.

The available input power depends on the value of V_S, which corresponds to the open circuit voltage of the PV cells. The *reset* signal is buffered so that the capacitance of the oscilloscope probe does not load the inner *reset* node. This buffer is supplied by V_{DD_test}.

The first test replicates a high light intensity situation: V_S abruptly changes from 0 to 2 V. Fig. 7.6 shows the start-up behaviour: firstly, v_{in} and v_{dd} are shorted, and then, after the *reset* signal ceases, both v_{in} and v_{dd} follow their course. The *reset* pulse lasts for 60 µs and the estimated required energy and average supply current of the circuit, during this interval, are 384 pJ and 6 µA, respectively.

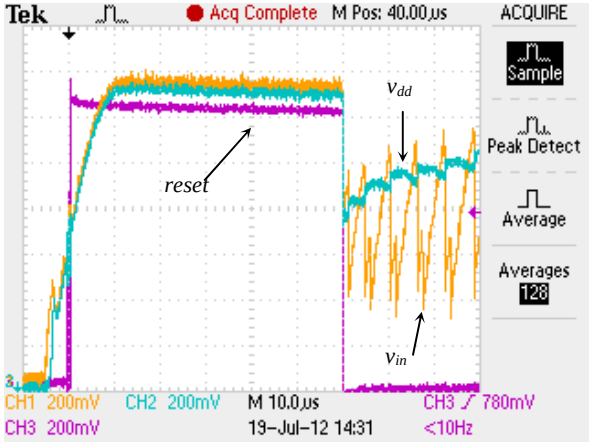


Fig. 7.6 - Starting-up with V_S = 2 V. CH1: v_{in}, CH2: v_{dd}, CH3: *reset*.

The next test corresponds to a low light intensity situation: V_S is now 390 mV. As shown in Fig. 7.7, the circuit successfully starts-up. In this test, V_{DD_test} is reduced to 0.5 V, so that the *reset* buffer can correctly discriminate between logic levels. The *reset* pulse holds for 249 µs and the estimated energy and average supply current during the *reset* pulse are 5.3 pJ and 50 nA, respectively.

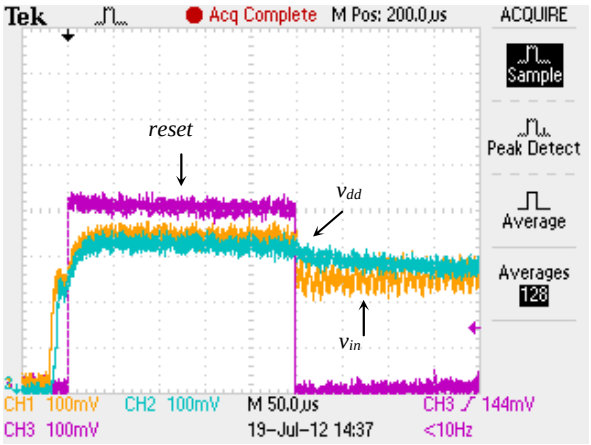


Fig. 7.7 - Starting-up with V_S = 390 mV. CH1: v_{in}, CH2: v_{dd}, CH3: *reset*.

In the last test, the rising of v_{in} is slowed down, by placing a 100 nF capacitor from this node to ground. The waveforms for this situation, including V_S, which is 1.2 V, are depicted in Fig. 7.8. The value of V_{DD_test} is set to 1 V. The *reset* pulse duration is 165 µs. During the start-up pulse interval, the estimated energy and average supply current are 132 pJ and 863 nA, respectively.

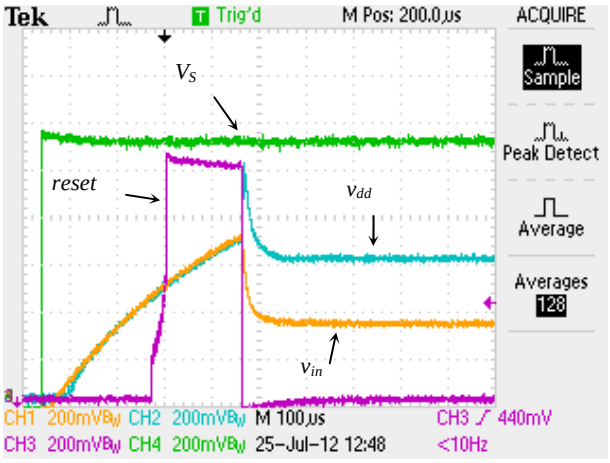


Fig. 7.8 - Starting-up with V_S = 1.2 V. CH1: v_{in}, CH2: v_{dd}, CH3: *reset*, CH4: V_S. v_{in} rising is slowed down,when compared to the previous situations.

In addition to the previous tests, the circuit was also tested using two amorphous silicon PV cells in series, with a total area of 14 cm^2. These cells are described in detail in Appendix B. The circuit was able to start-up the whole system, in a very low illuminated environment, where the measured irradiance was only 0.18 W/m^2.

After this experimental evaluation of the Start Up module, it has been confirmed that the circuit was able to correctly start-up the indoor light energy harvesting system, even for an input as low as 390 mV. In this case, an estimated energy of only 5.3 pJ was used by the circuit.

7.2.2 Experimental evaluation of the DC-DC converter

The previous test showed that the indoor light energy harvesting system is able to successfully start-up. After the system starts up, it is possible to measure the input and output voltages and the input and output currents, for different load values. Using these values it is possible to calculate the efficiency of the DC-DC converter.

The experimental setup used for these measurements is shown next in Fig. 7.9.

Besides the oscilloscope and the voltage source, which were used in the tests of the Start Up circuit, the setup of Fig. 7.9 also includes a precision multimeter.

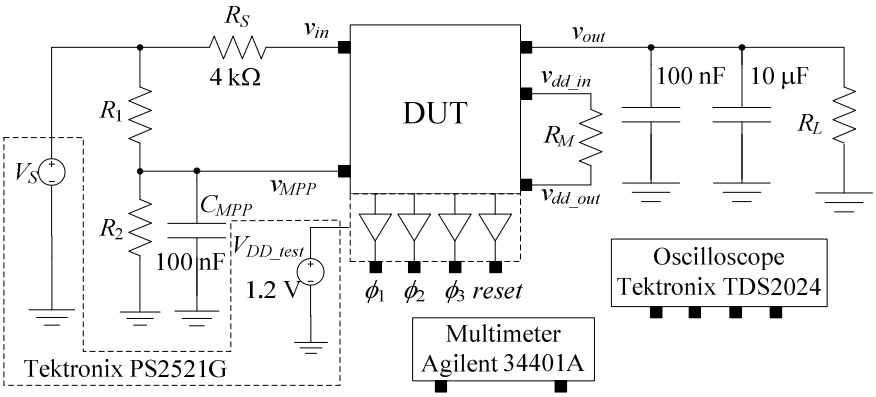


Fig. 7.9 - Experimental setup.

As shown in Fig. 7.1, the PCB allows for the setting of initial conditions for the system (v_{in}, v_{dd} and v_{out}) and provides a power supply voltage (V_{DD_test}) to supply a set of buffers that are used to observe the clock phases of the circuit and the *reset* signal. Just like for the setup in Fig. 7.5, these buffers are used so that oscilloscope probe capacitance does not load the node under observation.

In order to measure the power dissipation of the Phase Controller unit (which includes the implementation of the MPPT method), the local power supply voltage (v_{dd_out}) is connected to the phase controller (v_{dd_in}) through an external resistor (R_M) with a value of 10.4 Ω. By measuring the voltage drop across this resistor, it is possible to indirectly measure the current being delivered from the Local Supply to the Phase Controller.

The test board also includes a potentiometer, symbolized by R_1 and R_2, which creates the v_{MPP} voltage, from the open circuit voltage of the pilot PV cells.

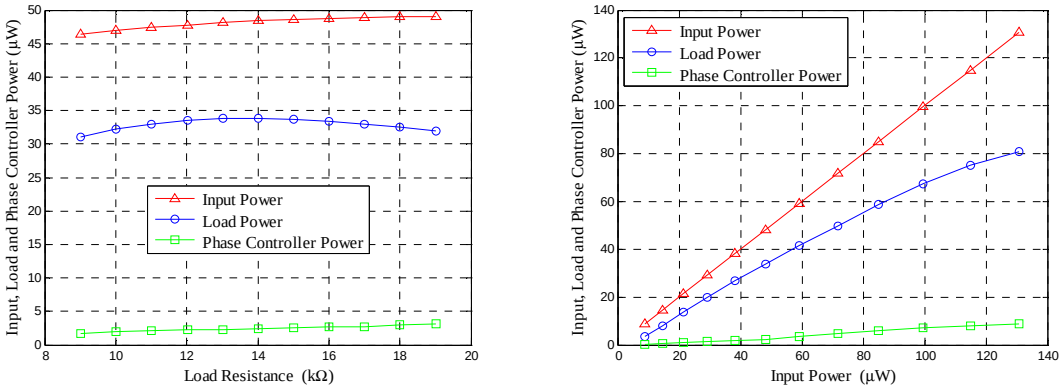
In order to characterize the performance of the circuit independently from the PV cells, these were initially replaced by a voltage source V_S in series with a resistance (R_S) equal to 4 kΩ. The voltage V_S was varied between 0.4 V and 1.5 V, in order to change the maximum available input power from 10 µW to 140 µW, which is the range where the system was designed to work. The voltage source V_S was also connected to the Fractional V_{OC} voltage divider (R_1 and R_2), which was adjusted to a factor of 0.5, in order to create the v_{MPP} voltage. In this case, the input source of the system consists of a Thévenin equivalent, and the MPP voltage is equal to $V_S/2$. In order to confirm that the system has its maximum efficiency for this set of values, different combinations of values for V_S and R_S were also tried. The value of R_S was changed to 500 Ω, 1 kΩ, 2 kΩ, 3 kΩ, 4 kΩ and 6 kΩ and, for each case, the load resistor R_L and the source voltage V_S were varied and the power efficiency was checked. These tests are summarized in TABLE 7.1, where the most relevant cases are shown together with the measured efficiency for each case.

TABLE 7.1 - Summary of the study to determine the value of R_S that yields the best efficiency.

R_S	Range of V_S	Range of R_L	Best efficiency (η)
500 Ω	1.0 V → 1.4 V	2 kΩ → 10 kΩ	38.2 %
1 kΩ	1.0 V → 1.4 V	4 kΩ → 10 kΩ	39.2 %
2 kΩ	1.0 V → 1.4 V	6 kΩ → 10 kΩ	59.3 %
3 kΩ	1.0 V → 1.4 V	10 kΩ → 12 kΩ	63.4 %
4 kΩ	0.4 V → 1.5 V	9 kΩ → 19 kΩ	70.3 %
6 kΩ	1.0 V → 1.2 V	22 kΩ → 26 kΩ	54.5 %

The measurement results presented in TABLE 7.1 confirm that, as expected, the maximum efficiency of the DC-DC converter occurs when R_S is equal to 4 kΩ. It should be noted that the efficiency of the converter does not decrease significantly when R_S is close to the ideal value.

Using the setup of Fig. 7.9, the average values of the voltages and currents of the circuit were measured with the multimeter for different values of input voltage (V_S) and load resistance (R_L). From these measurements, the input power, output power and power dissipated by the phase controller were calculated. These values are shown next in Fig. 7.10, demonstrating that the MPPT phase controller keeps the input power approximately constant, regardless of R_L.

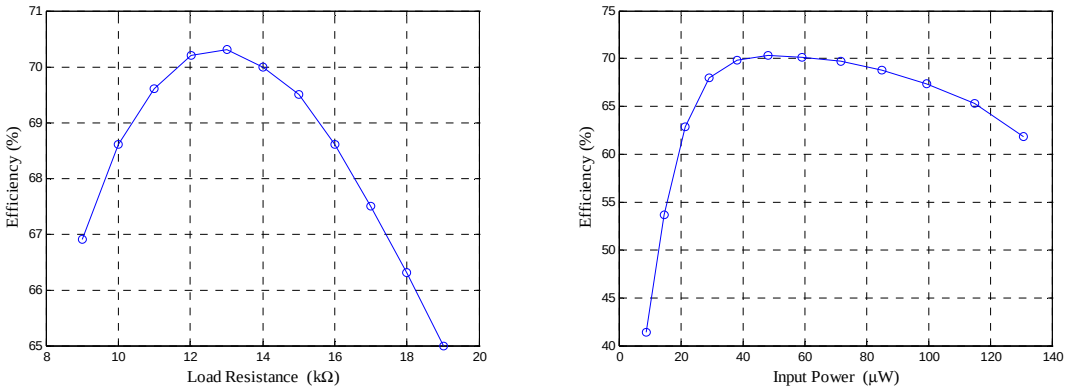


a) b)

Fig. 7.10 - a) Input, output and phase controller power as a function of R_L for V_S = 0.9 V and b) as function of V_S for R_L = 13 kΩ.

The MPPT allows for the input power of the system to closely track the maximum available input power. It is important to note that the circuit operates correctly even for an available input system power of 8.7 µW. In this situation, the local power supply voltage is 453 mV and the phase controller is dissipating only 0.085 µW, as depicted by Fig. 7.10 b), in the lower left-hand corner of the plot.

The previous measurements were used to calculate the efficiency of the circuit, ($\eta = P_{out} / P_{in} \times 100\%$). This is shown next in Fig. 7.11 a) and b).



a) b)

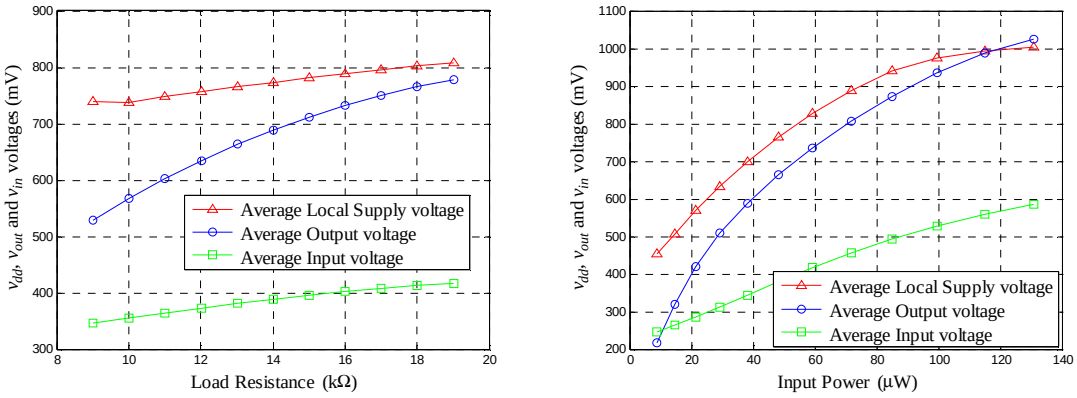
Fig. 7.11 - a) Efficiency, as a function of R_L, for V_S = 0.9V and b) as function of V_S for R_L = 13 kΩ.

The maximum efficiency is 70.3%. It is important to note that this efficiency is achieved for an available input power of only 48.1 μW. The efficiency of the system becomes lower, for lower values of available input power, because the power dissipated by the comparators in the phase controller is constant and does not scale with the clock frequency. This results in reduced efficiency for low available input power levels. The efficiency increases with the available input power because the phase controller power increases less than the power delivered to the load.

As the available input power becomes larger, the local power supply voltage increases, causing the power of the phase controller to grow faster than the available input power. This is due to the dependence of the equivalent parasitic capacitance of the phase controller on the power supply voltage value, thus resulting in a slight decrease of the efficiency.

It should be noted that the maximum efficiency occurs when the load is 13 kΩ, instead of 16 kΩ. This is explained because, when the load resistor is smaller than the optimal value, the power supply voltage is smaller, resulting in a slightly better efficiency. The electrical simulation of the circuit of Fig. 5.12, using for C_1 its post-layout extracted netlist, and the same values for R_L, f_{CLK} and V_S that were recorded for the experimental case, resulted in η = 69.71%, which is very close to the experimentally measured value.

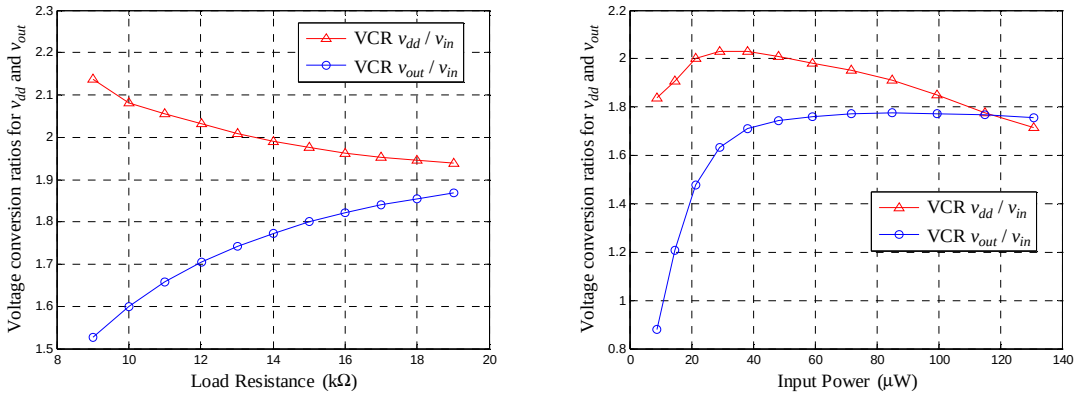
Some more parameters were measured, such as the individual output voltages regarding the main (v_{out}) and the Local Supply (v_{dd}) modules, as well as their respective voltage conversion ratios. The operating frequency is another parameter that was measured and whose results are shown. Next, in Fig. 7.12, the values of the average main and Local Supply output voltages are shown, as well as the input voltage, all of them as a function of the load resistance and the input power, respectively. All of them were measured using the digital multimeter.



a) b)

Fig. 7.12 - a) Local Supply output voltage (v_{dd}), main output voltage (v_{out}) and input voltage (v_{in}) as a function of R_L for V_S = 0.9V and b) as function of V_S for R_L = 13 kΩ.

By looking at Fig. 7.12 a), it is possible to observe that with the increase of the load resistance, as the demand of output current gets less intense, the output voltage generated by the main voltage converter has favorable conditions to increase. Moreover, the input voltage does not remain constant, but slightly increases its value. This also contributes to the increase of both v_{dd} and v_{out}. Through the analysis of Fig. 7.12 b), the sweeping over the input power comes from the sweeping over V_S. Thus, v_{in} also increases and, consequently, both v_{dd} and v_{out}, although the ratio between each of these output voltages and the input voltage is not constant along this interval. The voltage conversion ratios for both the Local Supply and the main voltage converter doubler are shown next in Fig. 7.13.



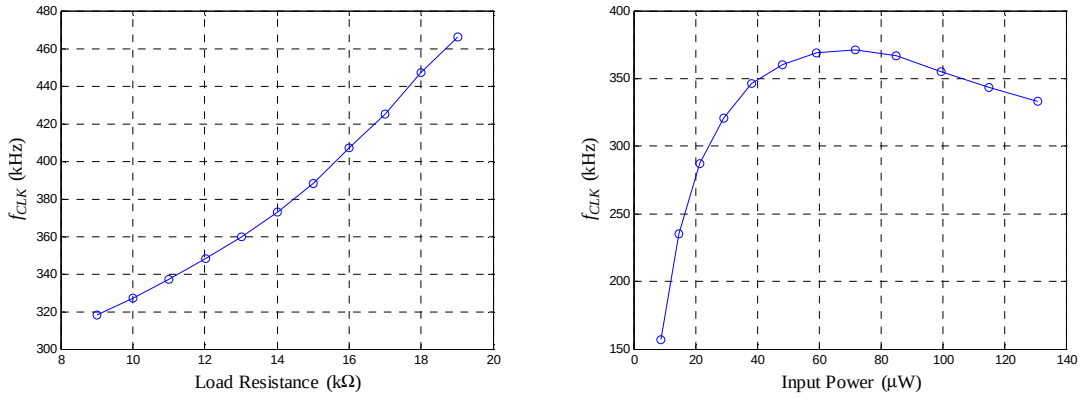
a) b)

Fig. 7.13 - a) Voltage conversion ratios associated to v_{dd} and to v_{out}, as a function of R_L, for V_S = 0.9V and b) as function of V_S, for R_L = 13 kΩ.

As for Fig. 7.13, the maximum VCR value of 2 (see Fig. 5.23) is approached. The output VCR associated to voltage v_{dd} is generally higher than the one associated to v_{out}. This can be explained by the fact that the Phase Controller presents a less demanding load to the Local Supply converter, than the output load resistance (R_L) for the main voltage doubler. As such,

voltage v_{dd} has better conditions to have a higher value than v_{out}. The situations where the VCR exceeds the maximum value of 2, can be explained because this voltage has a large ripple (due to the smaller internal decoupling capacitor) causing the voltmeter to have an error in measuring the average value of v_{dd}. This problem does not affect the measurement of the input and output voltages (v_{in} and v_{out}) because these voltages are decoupled by external larger capacitors and therefore do not have a large ripple value.

In Fig. 7.14 the clock frequency, as a function of the same variables used for the cases already presented, is also shown. In Fig. 7.14 a), it is clear that with the increase of the load resistance, there is also an increase in the operating frequency. The reason is that when R_L increases, it absorbs less power. Since the MPPT is trying to maximize the power obtained from the input, it will increase the clock frequency, resulting in an increase of the power dissipated by the MPPT controller itself. The end result is a decrease in the efficiency of the system. It should be noted that this corresponds to a case where there is more power available to be harvested than the amount of power that the system requires. Therefore, a decrease in efficiency is not important. As explained in Section 5.3.2, an increase in the operating frequency results in the increase of the dynamic power dissipation.



a) b)

Fig. 7.14 - a) Operating frequency (f_{CLK}) as a function of R_L for V_S = 0.9V and b) as function of V_S for R_L = 13 kΩ.

In Fig. 7.14 b), with the increase of the input power, and consequently, the increase of the output power, the operating frequency tends to increase. However, because of the decrease in efficiency from a certain point, the increase in the input power does not translate into an increase at the output, and so the operating frequency decreases given those conditions.

7.2.3 Experimental evaluation of the MPPT controller

The behavior of the MPPT circuit, explained in Section 5.3.2, can be observed in Fig. 7.15. At the rising edge of either ϕ_1 or ϕ_3, a capacitor (M_1 or M_2 of Fig. 5.12) is connected to the input

node, drawing charge from it, and resulting in the decrease of the input voltage. The ASM remains in *state1* until the input voltage is charged to the v_{MPP} value by the PV cells. Only after that, the ASM advances to the next states, in order to complete the cycle.

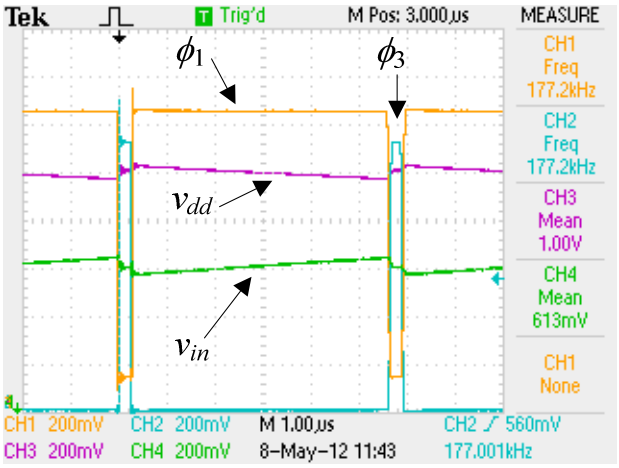


Fig. 7.15 - Behavior of the MPPT circuit. CH1: phase ϕ_1, CH2: phase ϕ_3 CH3: v_{dd} voltage and CH4: v_{in} voltage.

Also, in Fig. 7.15, as it was stated in Section 5.3.2, it is clear that the durations of the phase signals ϕ_1 and ϕ_3 are not the same, since the ASM must wait for the condition $v_{in} > v_{MPP}$ to be met, holding the signal ϕ_1 active (see Fig. 5.16).

In Fig. 7.16 it is shown an enlarged waveform diagram which, in addition to the phase signals shown in Fig. 7.15, allows for seeing the phase signal ϕ_2 between ϕ_1 and ϕ_3, corresponding to the sequence of states shown in Fig. 5.16.

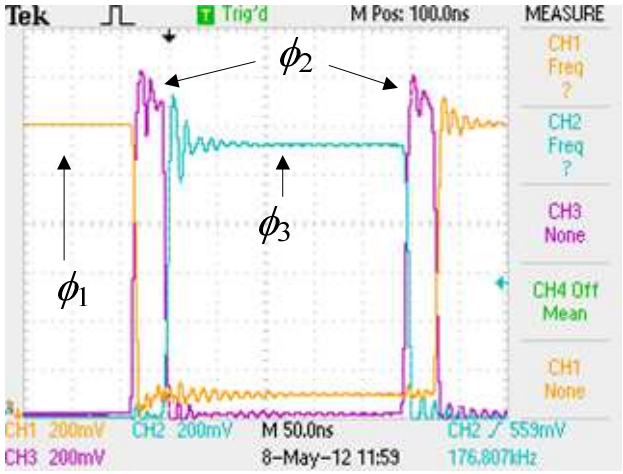


Fig. 7.16 - Detail allowing to see the three phase signals: CH1: phase ϕ_1, CH2: phase ϕ_3, CH3: phase ϕ_2.

In this case, the duration of *state2* (and *state4*) is about 35 ns. As explained before, in Section 5.3.2, this duration is sensitive to the supplying voltage value.

The dynamic response of the MPPT algorithm was tested by using a square wave signal with two levels (0.5 V and 1 V), in place of V_S. This forces the system to adjust the clock frequency in order for the input voltage (v_{in}) to track the v_{MPP} voltage. This behavior is shown next in Fig. 7.17.

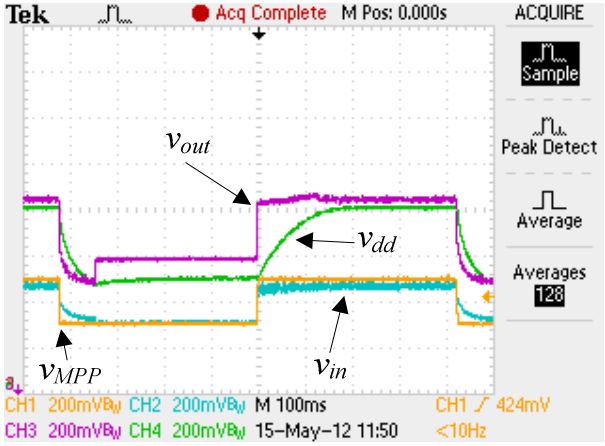


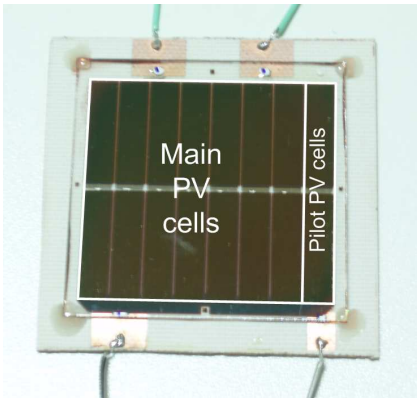
Fig. 7.17 - Input voltage tracking the v_{MPP} voltage. CH1: v_{MPP} voltage, CH2: v_{in} voltage, CH3: v_{out} voltage and CH4: v_{dd} voltage

From this graph, it is possible to conclude that the MPPT method can track the fractional V_{OC} voltage (which corresponds to the maximum available input power) in less than 100 ms.

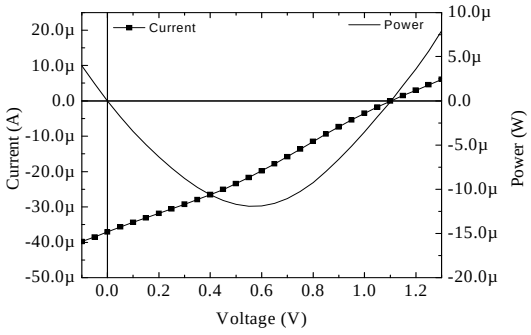
7.2.4 Experimental results using the PV cells

In order to supply power to the circuit, a set of a-Si:H PV cells, with a combined area of 14 cm^2, were manufactured using the procedure described in Appendix B.

These cells were then connected together in order to obtain two cells in series and seven of these sets were connected in parallel. The photograph and the electrical characteristic of these PV cells, for a worst case irradiance of 0.10 W/m^2, are shown next in Fig. 7.18.



a)



b)

Fig. 7.18 - a) Photograph of the a-Si:H PV cells (the areas of the main and pilot PV cells are 14 cm^2 and 2 cm^2, respectively) and b) electrical characteristics (for minimum illumination).

Fig. 7.19 shows another photograph of the set of PV cells, along with a daughter board and 1 F supercapacitor, in order to have an idea of the relative size of each of them.

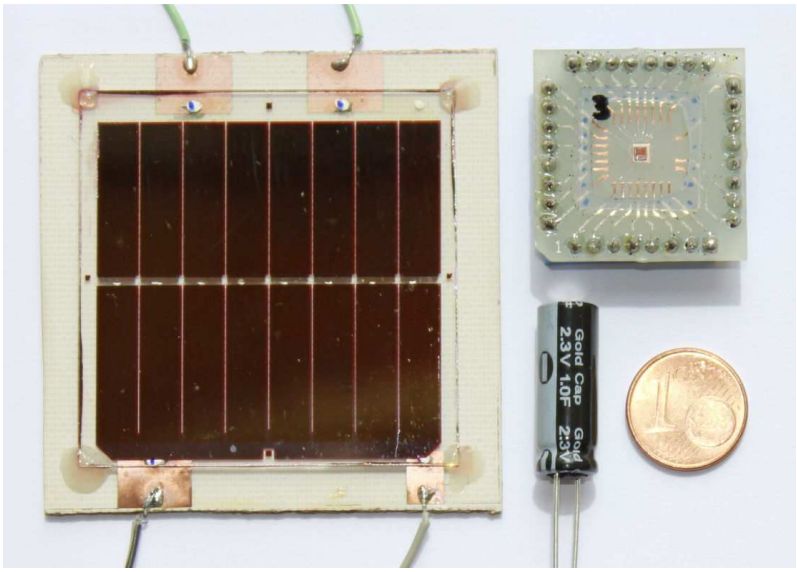
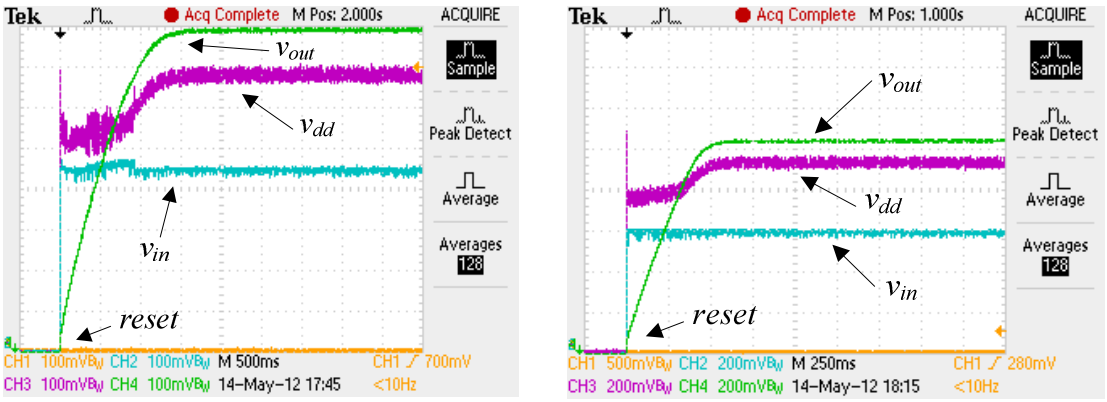


Fig. 7.19 - Photograph of PV cells, daughter board and a 1 F supercapacitor, so as to show their relative size.

Due to a problem during the manufacturing process of the a-Si:H PV cells, which resulted in a high series resistance, these PV cells have worse performance than the prototype evaluated in Appendix B. As a result, the MPP voltage of the PV cells is only about 0.5 of the V_{OC} voltage, instead of about 0.71 to 0.78 [86]. In normal conditions, the value of k would have to be set to an experimentally determined value, which would be done using the procedure described in Section 4.6.2.

The voltage source V_S and the resistor R_S were disconnected from the circuit and the main plus the pilot PV cells were connected to the v_{in} and V_{OC} inputs of the test PCB, respectively.



a) b)

Fig. 7.20 - Voltage waveforms during start up for an irradiance level of a) 0.32 W/m^2 and b) 4.97 W/m^2. CH1: *reset*, CH2: v_{in}, CH3: v_{dd} and CH4: v_{out}.

Fig. 7.20 shows the start-up behavior of the system, with an output 10 μF capacitor, from a 0 V condition for two different light intensities.

Fig. 7.20 a) shows that the system is capable of operating correctly with a power supply voltage of approximately 700 mV, dissipating only 1.43 μW of power, for a very low irradiance condition, which still allowed for the system to start-up (0.32 W/m^2). In this figure, the narrow spike that appears at the left-hand side is the *reset* signal, provided by the Start Up module, which had its results presented back in Section 7.2.1.

The phase controller circuit is able to work with even lower irradiance levels, although in that case, almost all of the harvested energy is being used to supply the energy harvesting controller. Thus, almost no energy is delivered to the output storage capacitor. Nevertheless, this characteristic allows for the system to react more promptly to illumination variations. The lowest recorded irradiance, under which the phase controller had started up and was showing correct activity, was 0.18 W/m^2.

The conclusions about the results that were taken and a broader general conclusion about the whole work carried out in this thesis, as well as possible future developments, are discussed next, in Chapter 8.

Chapter 8

CONCLUSIONS AND FUTURE PERSPECTIVES

8.1 Summary and achievements

This research thesis presented the analysis, design procedures and experimental evaluation of a CMOS energy harvesting system, using a switched-capacitor step-up converter, optimized to work with amorphous silicon photovoltaic (a-Si:H PV) cells with an area of 14 cm^2, under indoor light conditions.

The circuit was manufactured in a 130 nm CMOS technology and occupies an area of 0.31 mm^2. The step-up converter uses switched MOSFET capacitors with a charge reusing scheme, in order to reduce the impact of the parasitic bottom plate parasitic capacitance loss.

The phase generator circuit includes the MPPT Fractional V_{OC} technique, in order to maximize the power obtained from the PV cells. Experimental results showed that the proposed system is capable of starting-up from a 0 V condition, even with an irradiance of only 0.32 W/m^2. After starting-up, the system requires an irradiance of only 0.18 W/m^2 to remain in operation.

The ASM circuit can operate correctly using a local power supply voltage of 453 mV, dissipating 0.085 μW. These values are, to the best of the authors' knowledge, the lowest

reported in the literature. The maximum efficiency of the converter is 70.3% for an input power of 48 μW, which is comparable with reported values from systems operating at similar power levels [8], [9].

A comparison of the presented system with previously reported state-of-the-art publications is presented in TABLE 8.1.

TABLE 8.1 - Comparison with some state-of-the-art publications.

Reference	[8]	[12]	[26]	[153]	This work
PV cell area (cm^2)	N/A	42.5	16.5	N/A	14.0
Min. irradiance (W/m^2)	N/A	2.50 [(a)]	3.17	N/A	0.18
Min. input power (μW)	3300	10625 [(b)]	180	5.0	8.7
Min. voltage supply (V)	5.000	2.500	2.800	1.000	0.453
Min. controller power (μW)	N/A	50	135	2.4	0.085
Efficiency (%)	40.0	75.0	91.8	87.0	70.3
Technology	Discrete	Discrete	Discrete	0.25 μm CMOS	0.13 μm CMOS
Storage device	Supercap	Supercap	Supercap	Battery	Supercap
Converter	Boost	Boost	Boost–Buck	Boost	Boost
Converter based device	Inductor	COTS	Inductor	Inductor	SC

[(a)] – After conversion from lux to W/m^2, as specified in [26] and [76]
[(b)] – Calculated by scaling the value of (Min. irradiance) by (PV cell area)
COTS – Commercial off-the-shelf

Besides the core issue, which was focused on the implementation of a physical prototype, serving as a proof of concept, this research thesis also focused on giving a general overview about energy harvesting systems.

In Chapter 2, the various energy harvestable sources have been presented, along side with examples of existing systems reported in the literature. The purpose was to give the reader an insight about the universe of the energy harvesting area for very low power systems. Although summarized, the coverage intended to be as wide as possible about the topics that a designer will certainly face, when designing a wireless sensor node, from concept to finish. The diversity of scenarios and applications is very wide, and there are many options that can be made in order to build the system up.

The contents in Chapter 3 addressed the theme of PV technologies, since this work is focused on using light energy to get powered. In accordance, this chapter gave an overview about the various types of harvesters that can be currently found. The selected energy source over which the work has been developed is light, mainly in indoor environments. However, the system that has been designed and implemented can also operate in outdoor environments, in which light energy is much more abundant than indoors.

The harvester that has been used, is a PV cell specifically built to be fit into this prototype. The base material of this PV cell is amorphous silicon. This technology has lower manufacturing costs than crystalline silicon or organic cells, just to name a few other technologies, which can be found in Chapter 3. This is an important factor to take into account if this concept is to be brought to the market. Tipically, there is the need to have a bigger area when using amorpous silicon cells, given that their efficiency is lower than for other technologies. However, the area that was employed in this application was the minimum strictly required to meet the needs under the most adverse situation experimentally measured in indoors. The objective was to have the smallest harvester as possible, while ensuring the effectiveness of the system. This is an important factor because area also means cost so, when looking at an affordable solution, this will greatly increase the possibility of having a competitive commercial product. The small size of the harvester, and hence of the whole system, is a positive feature.

Moreover, the area of energy harvesting, by itself, gives an interesting contribution towards the purpose of environmental sustainability, since there is no need to use energy coming from the grid, neither the use of batteries to power the electronic applications. In addition, the energy used to put the applications to work is costless, and just waiting to be harvested. Otherwise, this energy will not be turned into a useful resource, and its potential will simply be wasted.

Also, Chapter 3 documents an approach that was tried in order to use CMOS integrated PV cells in the same die as the circuits that needed to be powered. Unfortunately, one could realize that this solution was not feasible, because when irradiated by light, the substrate would have its voltage increased by the same amount that a diode has when directly biased. The method that was used to repair this occurence was to surround the photodiode with a guard ring. However, this caused the PV structure to be short-circuited, making it impossible to generate a useful voltage. Only by placing the PV cells on one substrate and the other circuits on another substrate, would make it to work.

When designing an energy harvesting system, the source, or sources, to be harvested is the first option to make. Following it, there is the type of harvester to use. Then, according to the requirements of the system to be powered, a convenient power conditioning circuit (step-up or step-down voltage converter) must be used, so as to establish the bridge between the input voltage, coming from the harvester, and the output voltage, supplying the load. Thus, to complete the overview, in Chapter 4, various topologies for step-up converters have been presented, encompassing both the use of inductors and switched-capacitors. The latter was the selected approach, because it is more favorable to having a complete solution integrated into a silicon chip.

8.2 Future perspectives

The whole system that has been designed and developed in this research thesis is only concerned about harvesting energy. As such, a natural upgrade to the system that was built is the inclusion of a sensor and a transmitter circuit. As it is normal in energy harvesting nodes, these have the capability to communicate with other nodes or with communication infrastructures. Thus, the next step could be to supply a low-power, low data rate UWB transmitter [165]. For a start, the information that could be transmitted is the light intensity received by the PV cell. This information is naturally available through the frequency value of the phase generator signals that control the switches in the DC-DC converter. A possibility of usage that such a system could have, is in monitoring the level of the light intensity in an "intelligent house" (domotics). This way, the energy could be more rationally used, reducing monetary costs and natural resources. This kind of concern is gaining more importance and [100] is an example of a research work with this kind of objective in focus.

Regulations allow the unlicensed use of UWB systems as long as the power spectral density (PSD) of the transmitted signals is kept below -41.3 dBm/MHz [166] and contained into certain frequency bands. This makes this type of signals especially appealing for wireless sensors [167]. UWB pulses can be generated using delay lines and digital gates, which can be class B circuits and, therefore, UWB transmitters tend to be very efficient [168]. The transmitted pulse shape depends upon the pulse generating circuit and on the antenna transfer function [169] and, therefore, it is necessary to take this into consideration, during circuit design.

In addition to the previous topic, it has been put to consideration, near the final stage of the prototype testing, to make a re-design of the circuit in order to implement the Hill Climbing MPPT method. Consequently, the phase generator should be worked around accordingly.

Another aspect that can be considered for a re-design is the use of transistors that can undergo a higher voltage. The present project was carried out under the assumption that the output voltage would be at a maximum of about 1.2 V. As such, the concern was focused about this voltage value and on the use of devices for this voltage rating. The technology that was used provides the designer with transistors having ratings of 1.2 V and 3.3 V. Thus, instead of using MOSFETs with a maximum rating of 1.2 V, as it was done, what can be done in the future is to use devices that can undergo 3.3 V. The increase in the amount of harvested energy is very significant. As one knows, the energy is proportional to the square of the voltage at the terminals of the output storage capacitor. Should this voltage increase to 3.3 V, instead of having 1.2 V, this would mean that, for the same capacitance value, the stored energy could be

increased by more than seven fold. Of course, the output supercapacitor would also have to be rated to, at least, 3.3 V.

In Chapter 2, various energy sources have been addressed, as well as different types of harvesters devoted to a corresponding energy source. One interesting thing to do, while pursuing the path that was opened up by the current work, would be to research about different types of phase generators, especially devoted to a particular type of energy source, or energy harvester. Also, as it has been seen in Section 4.6, energy harvesters have a MPP that can be tracked. As such, it would also be very interesting to develop energy harvesting systems with a MPPT capability, which having a starting point based on the present work, would track the MPP of a given harvester, for the corresponding type of energy source. Thus, using the same voltage converter as the one brought forward in this thesis, and exploiting the potential of sources like mechanical, thermal and so forth, is a possibility to consider.

Chapter 9

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Appendix A

LIGHT POWER MEASURING DEVICE

A.1 Device overview

The assessment of the typical level of light in an indoor environment was achieved by performing a set of measurements using a S120B silicon light sensor [170], connected to a measuring device, the Thorlabs PM100 Digital Power Meter Console [171]. This equipment is depicted next, in Fig. A.1.

Fig. A.1 - Thorlabs PM100 digital power meter console and operating elements.

This device allows for separate light power readouts over a set of wavelength widths. In particular, the available wavelengths for the present case were centered at 450 nm, 500 nm, 550 nm, 600 nm and 650 nm. From the point of view of the measuring device, as the light measuring sensor does not respond equally to every wavelength interval, a separate correcting factor must be applied accordingly. This is already taken beforehand by the manufacturer, which has a ROM-based table, built-in to the device, in which the correcting factors are stored. The user must only specify which wavelengths are to be taken into account, by storing the desired list in the device. Afterwards, any of these wavelengths can be chosen, by selecting which wavelength to use, pressing the "λ" key (wavelength correction). By pressing this key repeatedly, the device will cycle around the set of working wavelengths (five, at the most). This key is identified as "wavelength correction" and shown in Fig. A.1 (extracted from [171]).

A.2 Using the band-pass filters

The previously mentioned wavelength values are concerned to a set of optical band-pass filters, which are to be placed in front of the sensor. The sensor is depicted next in Fig. A.2, where a set of mechanical data is provided.

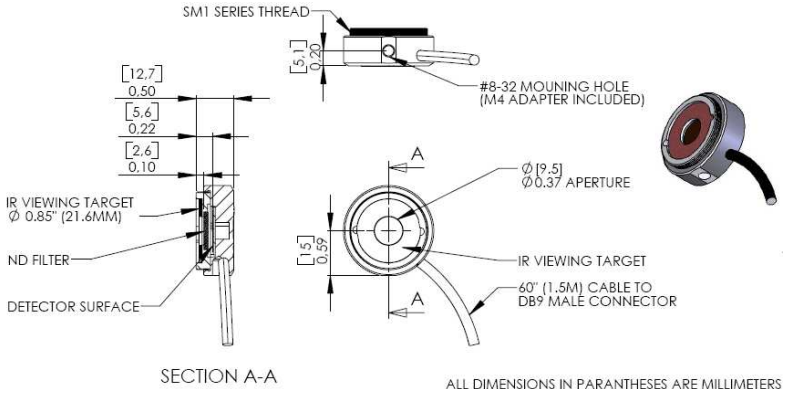


Fig. A.2 - S120B silicon light sensor [170].

Important information to have into consideration is the aperture of the sensor, which has a diameter (d) of 9.5 mm. This means that the area of the sensor that will be shed by light has the value of

$$A = \pi\left(\frac{d}{2}\right)^2 = \pi\left(\frac{0.95}{2}\right)^2 \approx 0.71\text{cm}^2. \qquad \text{(A.1)}$$

When relating this illuminated area with the conventional area of 1 m^2, the resulting measured power must be multiplied by 10000/0.71 = 14108.

What is actually measured, is the amount of light power contained in each of the bandwidths centered at the wavelengths previously mentioned, having a bandwidth, for each

case, of 40 nm. The physical appearence of each band-pass filter is as shown next in Fig. A.3. The one shown here is the one centered at 450 nm [172], but the mechanical features are the same for the other available filters.

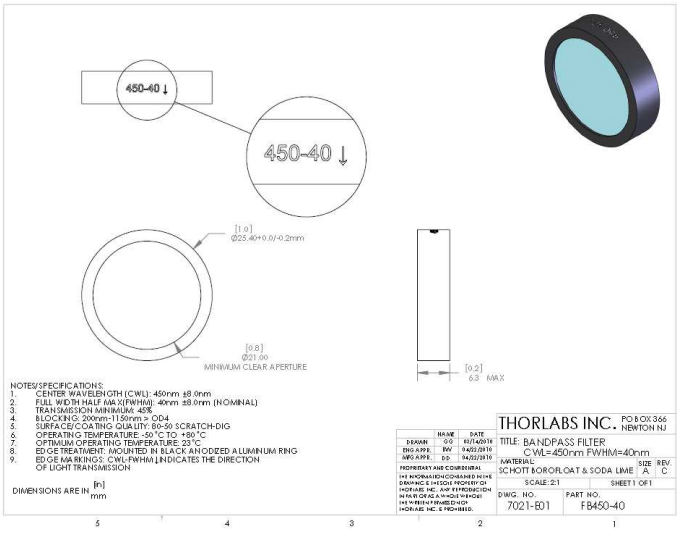


Fig. A.3 - Optical band-pass filter (centered at 450 nm).

The filter must be placed in front of the sensor and the readout will only be reliable if the wavelength correction value (λ) is the same as the one specified for the center wavelength of the filter in use. A detail to have into attention is the direction of how the filter must be placed. There is an arrow on its side (↓), indicating the direction by which light must cross it.

In addition to the wavelength correction factor, which is already accounted for by the manufacturer, as this is only concerned to the sensor, there is another correcting factor regarding the transmission of the band-pass filter in use. The transmission function for each of the available filters is depicted in Fig. A.4.

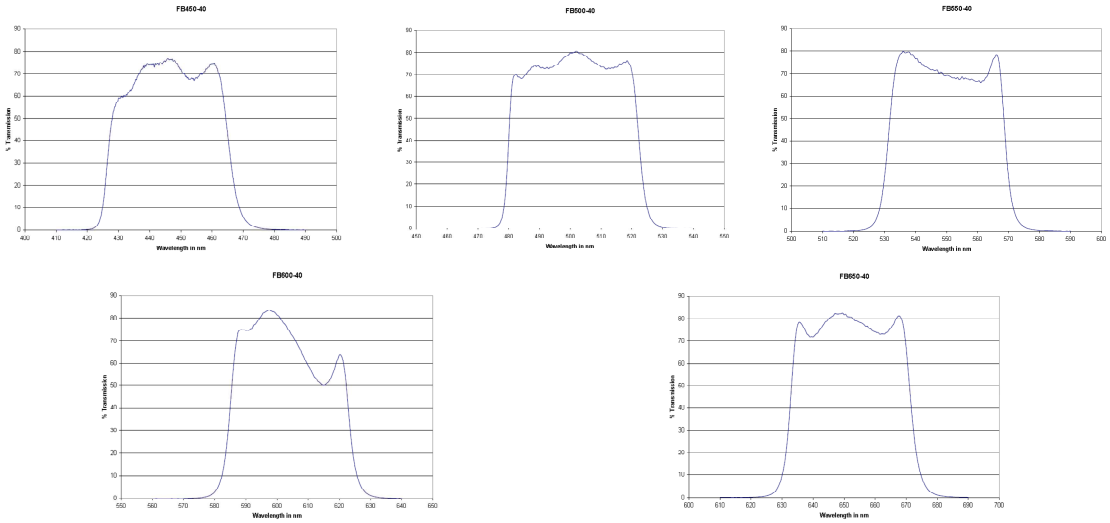


Fig. A.4 - Transmission functions for each of the band-pass filters used.

As it can be seen, none of the filters shows a transmission of 100% in the pass band. As such, it is also possible to correct this feature by setting the attenuation correction in the PM100 with a value that will, at least approximately, cancel out this filter imperfection. It was identified, by observing the graphs in Fig. A.4, that the average band-pass transmission of the whole set of filters is about 80%. The correcting factor that must be inserted into the device will be expressed in dB, and corresponds to the symmetrical of

$$a = 10\log_{10}(T) = 10\log_{10}(0.8) = -0.97 \text{ dB}. \quad \text{(A.2)}$$

Thus, the value to be stored into the device is 0.97 dB. This is done by setting the attenuation correction factor in the PM100.

More detailed information about the PM100, its features and procedures to set parameters in the device, can be found in [171]. However, the procedures described in this appendix can help the user to effectively manipulate the measuring device, as well as the accessories that were presented, in most situations.

Appendix B

DESCRIPTION OF THE MANUFACTURED PV CELL

An amorphous silicon PV cell was selected because this kind of PV cell is cheaper to manufacture than for other PV cell technologies and it is more sensitive in the green visible range of the wavelength spectrum. This wavelength is predominant in the light produced by fluorescent light tubes, which are present in most offices and in many indoor environments. Thus, this type of PV cell has a natural vocation for harvesting indoor lighting energy [21], [80].

B.1 Amorphous silicon PV cell manufacturing procedure

An hydrogenated amorphous silicon (a-Si:H) PV cell with an area of 0.49 cm^2 was deposited in a glass\InO_x\p\i\n\Al structure. The main properties of the constituent layers are presented in TABLE B.1.

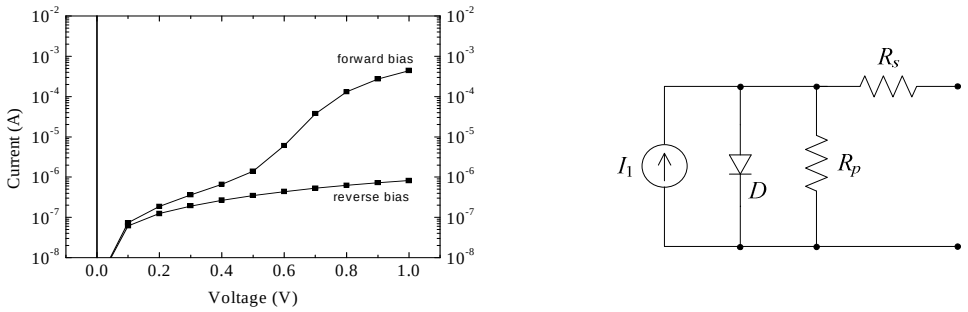
TABLE B.1 - Main properties of the constituent layers.

Layer	Thickness, d [nm]	Optical gap, E_{OP} [eV]	Conductivity, σ $[(\Omega.cm)^{-1}]$	Thermal activation energy of σ, ΔE [eV]
InO_x (TCO)	120	3.55	1.2×10^{3}	-0.010
a-SiC:H p-type	13	1.64	1.2×10^{-4}	0.354
a-Si:H intrinsic	450	1.75	1.4×10^{-9}	0.712
a-Si:H n-type	46	1.71	3.6×10^{-4}	0.304
Al	93	-	5.3×10^{5}	-

InO_x was deposited over soda-lime glass by radio frequency Plasma Enhanced Reactive Thermal Evaporation (rf-PERTE) [173] at room temperature. Then, the semiconductor layers were deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) at 350 ºC using gas mixtures of $B_2H_6 + H_2 + SiH_4 + CH_4$ for the p-type layer, pure silane for the intrinsic layer and $PH_3 + SiH_4$ for the n-type layer [91]. Finally, an aluminum contact was deposited by thermal evaporation.

B.2 Electrical characterization of the PV cell prototype

Fig. B.1 a) shows the $I(V)$ curve of the manufactured PV cell prototype, measured in dark conditions, plotted in a semi-log scale and reduced to the first quadrant (absolute values). The I_{on}/I_{off} ratio for $|V|$=1V is about 630. The equivalent series and parallel resistances of the diode are 645 Ω and 1.21 MΩ, respectively. Fig. B.1 b) depicts the electrical model of the PV cell.



a) b)

Fig. B.1 - a) PV cell $I(V)$ curve, measured in dark conditions (reverse bias corresponds to negative voltage) and b) Electrical model of the PV cell.

Fig. B.2 depicts the $I(V)$ characteristics. These measurements were performed in darkness and under a halogen Philips 13117 lamp illumination, using different intensities, corresponding to irradiations of 0.10 W/m^2, 4.01 W/m^2, 15.14 W/m^2 and 470.22 W/m^2. These irradiances were determined with the same equipment and accessories that were described in Appendix A.

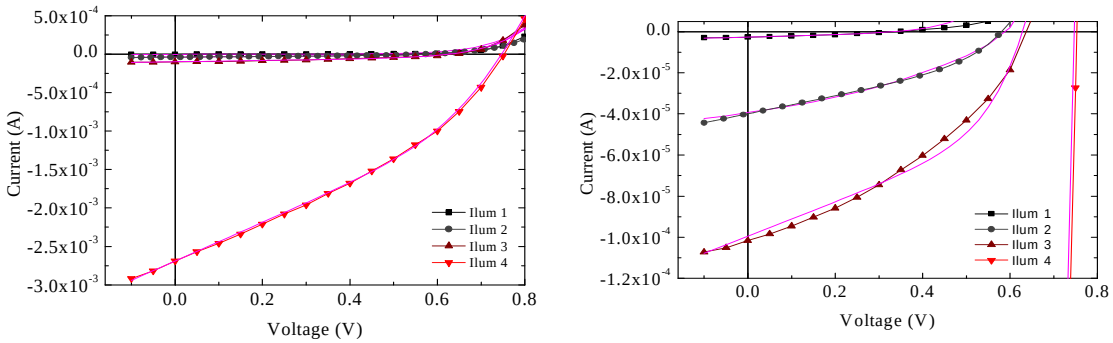


Fig. B.2 - PV cell characteristic curves (measured and SPICE model) under different illumination intensities (left), zoomed for lower illumination intensities (right).

Concerning the PV cell SPICE modelling, it has been optimized for the active zone of the $I(V)$ curve (3rd quadrant) and the values from TABLE B.2 are considered valid only for $0 < V < V_{OC}$. In order to have a more accurate modelling of the cell it is necessary to obtain different SPICE model parameters for different light intensities. In Fig. B.2, the curves resulting from SPICE modelling, whose parameters are described in TABLE B.2, are also plotted.

TABLE B.2 - SPICE modelling parameters of the PV cell and maximum electrical power available for different illumination intensities (PV cell area = 0.49 cm^2).

Irradiance (W/m^2)	SPICE diode parameters				Electrical model components			Max. Power Point	Voltage @MPP
	IS(A)	N	ISR(A)	NR	$R_s(\Omega)$	$R_p(\Omega)$	I_1(A)	MPP (μW)	V(MPP) (V)
0.10 (Ilum 1)	5×10^{-9}	2.83	5×10^{-9}	2.83	40	190000	2.60×10^{-6}	0.28	0.19
4.01 (Ilum 2)	5×10^{-9}	3.00	5×10^{-9}	3.00	40	23000	4.00×10^{-5}	8.44	0.37
15.14 (Ilum 3)	5×10^{-9}	2.80	5×10^{-9}	2.80	58	12000	1.00×10^{-4}	26.05	0.44
470.22 (Ilum 4)	5×10^{-9}	2.46	5×10^{-9}	2.46	58	340	3.15×10^{-3}	687.20	0.46

The manufactured PV cell presents a high series resistance when working as a diode in dark conditions. This fact can be explained by the high resistivity of the amorphous silicon layer, since the series resistance drops to some tens of Ohms when illuminated. On the other hand, the parallel resistance showed a good value in dark, taking into account the area of the device, but fell down to 340 Ω under high intensity illumination.

R_p is usually related with current leakage along the edges of the cell or with point defects in the junctions [174]. However, this would make R_p in dark conditions to be low as well, which does not occur. This fact may be related to non-optimal layer thicknesses or doping levels. When carrier population rises, caused by sample illumination, space charge regions tend to decrease significantly due to the weak rectifying characteristic of the junction and thus, the R_p measured under high illumination intensity decreases drastically.

B.3 Discussion

TABLE B.2 shows that under the lowest illumination condition (corresponding to about the minimum expected irradiance, in a normal office) the PV cell can produce a MPP voltage of only 0.19 V. Thus, it is necessary to use at least two PV cells in series to obtain a MPP voltage of at least 0.4 V, allowing for the step-up doubler circuit to produce an output voltage close to 0.8 V. The question about the number of PV cells to connect in series to power the system is a major design decision point. At low irradiance conditions, both the current and voltage are reduced. However, the voltage tends to decrease logarithmically with the irradiance whereas the current decreases linearly, making sense to maximize the area per cell. On the other hand, for

each additional unit placed in series, the total R_s value of the cell will increase because of the series resistance introduced by each cell, degrading the performance of the whole PV assembly. Also, the area used to connect the cells in series will not be used for energy conversion. Thus, the number of PV cells to place in series must be strictly the minimum necessary to supply the step-up circuit with its required minimum voltage, under the most adverse illumination conditions considered in this work. Also, if more than two PV cells in series are used, then under larger irradiance conditions, the input voltage of the system might be too large and could cause voltage stress in the circuit, potentially reducing its operating lifetime or even destroying it. Therefore it was decided to use just two PV cells in series to power the system.

Based also on TABLE B.2, if the PV cells are to supply at least 10 μW of power, this means that the required minimum area for the cell is 17.5 cm^2, 0.59 cm^2, 0.19 cm^2 or 0.007 cm^2, depending on the illumination level. Assuming the worst case illumination for the system, the area of the PV cell should be 17.5 cm^2. It was decided, for simplicity, to use an area of $4 \times 4 =$ 16 cm^2. This area was used to implement the main PV cells and the pilot PV cells with 14 cm^2 and 2 cm^2, respectively. This means that the available power from the main PV cells will be 8 μW under the expected worst case light irradiance. When comparing to other PV cell areas referred in literature for similar purposes [77], the area here proposed is much smaller.

The capacitance of such a PV cell can be estimated, assuming it to be a parallel plate capacitor. Every elemental section of the PV cell, which is depicted in Fig. 7.18 a), has an area of 1 cm^2. For the main PV cell, one has a series of two of these elements, and then, a parallel of seven of these series. The pilot cell has only one series. The capacitance of each element is given by

$$C = \varepsilon_{Si}\varepsilon_0 \frac{A}{d}. \tag{B.1}$$

where $\varepsilon_{Si} = 11.9$, $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, $A = 1$ cm^2 and $d = 13 + 450 + 46 = 509$ nm. Thus, each element has a capacitance of 20.7 nF. A series of two of these elements has a capacitance of 10.35 nF, allowing the parallel structure to achive a total of 72.45 nF.

This value is a mere approximation, since the junctions also contribute to the total capacitance, and that contribution is related with the biasing being used. However, this capacitance is much smaller than the one determined by the metals and the semiconductor. The latter, having a low conductance, in the order of $\sigma \approx 10^{-10}$ $(\Omega \cdot cm)^{-1}$, behaves just like an insulator, especially for relatively low frequencies, where the impedance due to the reactive component of the capacitor greatly surpasses the ohmic resistance.

Appendix C

COMPUTATION OF POWER IN A CIRCUIT WITH A SWITCHED–CAPACITOR

Let us consider the following circuit:

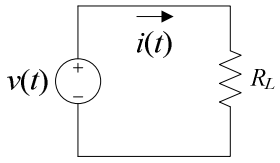


Fig. C.1 - Simple circuit for the computation of power.

The instantaneous power in the resistor R_L is given by

$$p(t) = v(t) \cdot i(t) \tag{C.1}$$

and the average power is given by

$$\overline{P} = \frac{1}{T} \int_0^T p(t)\, dt = \frac{1}{T} \int_0^T v(t) \cdot i(t)\, dt\,. \tag{C.2}$$

This average power corresponds to the accumulated sum of instantaneous power during an amount of time, divided by that same amount of time.

The instantaneous current, as a function of the elements in the circuit, is given by

$$i(t) = \frac{v(t)}{R_L}\,. \tag{C.3}$$

Correspondingly, the instantaneous power is given by

$$p(t) = \frac{v^2(t)}{R_L} = R_L i^2(t)\,. \tag{C.4}$$

As such, by performing the required substitutions, one gets

$$\overline{P} = \frac{1}{T}\int_0^T \frac{v^2(t)}{R_L}\,dt = \frac{1}{T}\frac{1}{R_L}\int_0^T v^2(t)\,dt = \frac{1}{T}\int_0^T R_L i^2(t)\,dt = R_L\,\frac{1}{T}\int_0^T i^2(t)\,dt\,. \tag{C.5}$$

The definition of the root mean square (*rms*) value for the current is

$$i_{rms} = \sqrt{\frac{1}{T}\int_0^T i^2(t)\,dt}\,. \tag{C.6}$$

Similarly, for the voltage case, its *rms* value is

$$v_{rms} = \sqrt{\frac{1}{T}\int_0^T v^2(t)\,dt}\,. \tag{C.7}$$

Thus, this means that the average power can also be expressed by

$$\overline{P} = R_L i_{rms}^2\,, \tag{C.8}$$

or by

$$\overline{P} = \frac{v_{rms}^2}{R_L}\,. \tag{C.9}$$

It is interesting to note that

$$\overline{P} = v_{rms} \cdot i_{rms}\,, \tag{C.10}$$

however, the average power is not equal to the product of the average voltage by the average current, as it can be noted by

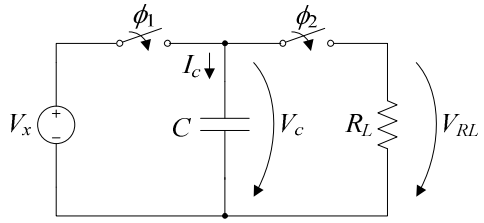
$$\overline{P} \neq \frac{1}{T}\int_0^T v(t)\,dt \times \frac{1}{T}\int_0^T i(t)\,dt \Leftrightarrow \overline{P} \neq \frac{1}{T^2}\int_0^T v(t)\cdot i(t)\,dt\,. \tag{C.11}$$

For the particular case where the voltage is constant, such as $v(t) = V_{DD}$, one can determine the average power, which is given by

$$\overline{P} = \frac{1}{T}\int_0^T p(t)\,dt = \frac{1}{T}\int_0^T V_{DD}\cdot i(t)\,dt = \frac{V_{DD}}{T}\int_0^T i(t)\,dt = V_{DD}\cdot \bar{i}\ . \qquad \text{(C.12)}$$

These derivations depend on the fact that voltage and current are proportional between themselves through R_L, which is resistive. For reactive loads, one will have a different situation.

To prove these conclusions, consider the following circuit, which has been simulated in Spectre:



$$Q = C\cdot V_x \Leftrightarrow I_c = C\frac{V_x}{T}$$

Fig. C.2 - Switched-capacitor circuit simulated in Spectre.

The values considered in the simulation are indicated in TABLE C.1.

TABLE C.1 - Values of the components of the circuit of Fig. C.2.

f	V_x	C	R_L
10 MHz	1 V	10 pF	100 Ω

Theoretically, the average power provided by the voltage source is given by

$$\overline{P}_x = V_x\cdot I_c = V_x\,C\frac{V_x}{T} = 1\times 10\times 10^{-12}\,\frac{1}{0.1\times 10^{-6}} = 100\ \mu\text{W}\ . \qquad \text{(C.13)}$$

The average power in the capacitor is given by

$$\overline{P_c} = V_c\cdot \bar{I}_c = V_c\times 0 = 1\times 0 = 0\ . \qquad \text{(C.14)}$$

Finally, the average power in the load resistance is given by

$$\overline{P}_{RL} = \frac{1}{T}\int_0^T \frac{V_{RL}^2}{R_L}dt = \frac{1}{T\times R_L}\int_0^T V_{RL}^2\,dt = \frac{1}{T\times R_L}\int_0^T \left(e^{-\frac{t}{R_LC}}\right)^2 dt = \frac{1}{T\times R_L}\int_0^T \left(e^{-\frac{2t}{R_LC}}\right)dt =$$
$$= \frac{1}{T\times R_L}\left[-\frac{R_LC}{2}e^{-\frac{2t}{R_LC}}\right]_0^T = -\frac{C}{2T}\left(e^{-\frac{2T}{R_LC}}-1\right) = \frac{C}{2T}\left(1-e^{-\frac{2T}{R_LC}}\right) = 50\,\mu\text{W} \qquad \text{(C.15)}$$

The data extracted from simulation are presented next in TABLE C.2, in which the computation of the power on the three circuit elements (switches are excluded) is performed by three different methods, by using the auxiliary tools provided by the results browser of the simulator. Only one of them is correct.

TABLE C.2 - Results for the power computation, according to three different methods.

Method	P_x	P_c	P_{RL}
average($i(t) \times v(t)$)	99.82 μW	696.4 nW	49.2 μW
rms($i(t) \times v(t)$)	3.906 mW	2.13 mW	494.4 μW
rms($i(t)$) × rms($v(t)$)	3.906 mW	2.807 mW	49.2 μW

According to the various possible computatiom methods which are presented, the one that shows coherence with the values obtained theoretically is the one in the first line. Thus, given the computation objectives, this is the one that should be used.

Appendix D

EVALUATION OF THE HILL CLIMBING MPPT METHOD

D.1 Introduction

In order to show how the Hill Climbing MPPT method performs, there are some simulation results, that were taken about a system similar to the one described in this thesis, but that was designed earlier. Instead of a doubler step-up converter, a tripler circuit was used. This appendix makes a summarized overview of what this system is about and the results that were achived.

The circuit of the SC step-up tripler converter is shown in Fig. D.1.

The Start Up module is like the one described in Section 5.5 and the Local Supply has a very similar approach to the one that is shown and that has already been described in Section 5.4. However, for instance, the values of the switched-capacitors are naturally different from the ones presented in Chapter 5, given that the optimization procedure was not yet developed at this time. The ratio that was used to scale the Local Supply module was also different from the one already known. The circuit operates as follows:

The principle of operation of this circuit is the same as the SC voltage tripler [109]. During phase ϕ_1, the MOS capacitors of the upper half-circuit (step-up A), M_{1A} and M_{2A}, are

charged to the input voltage value (v_{in}) and after, during phase ϕ_3, they are connected in series with the input voltage source.

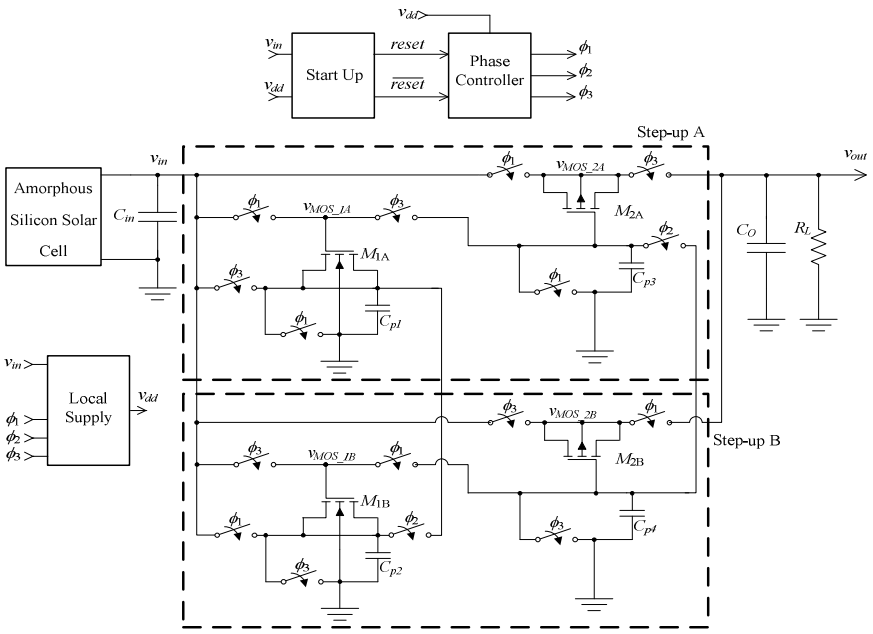


Fig. D.1 - Step-up SC voltage tripler circuit.

If there were no losses, this would result in an output voltage (v_{out}) three times larger than the input voltage value. The clock frequency and the capacitance values are dependent on the amount of power that must be transferred to the load. According to a preliminary theoretical analysis (which will not be presented), the MOS capacitances that would yield the best efficiency were determined to have 4.2 nF. As such, the dimensions of the transistors were set to achieve this MOS capacitance value. With this value, the corresponding operating frequency of the system was determined to be about 1.5 MHz. The theoretical efficiency of this circuit (assuming that there were no parasitic losses) would only depend on the values of the input and output voltages [109]. Just like before, in order to reduce the area of the circuit, MOS capacitors are used instead of MiM capacitors. Since, during phase ϕ_3, the drain/source voltage increases, the threshold voltage of a NMOS transistor also increases due to the body effect, resulting in a decrease of the capacitance of the transistor (MOS capacitor). This reduction can be significant for transistor M_{2A}. Therefore, this device is a PMOS instead of an NMOS transistor.

The other issue of using MOS capacitors is the large parasitic capacitance associated to the bottom plate nodes (drain/source nodes). In order to reduce the amount of charge lost in these parasitic capacitances, the circuit is split into two halves. The top half (A) is composed by M_{1A} and M_{2A} and the bottom half (B) is composed by M_{1B} and M_{2B}. The bottom half works in the same way as the top half, with phase ϕ_1 interchanged with phase ϕ_3. The charge reusing technique was already adopted here so, during an intermediate phase (ϕ_2), the bottom nodes of

both MOS capacitors of the upper and lower half-circuits are connected together, thus transferring half of the charge in one parasitic capacitance to the other, before the bottom plate nodes are shorted to ground. This reduces by half the amount of charge that is lost in the parasitic capacitance nodes, just as explained in Chapter 5 - Section 5.2.1.

The clock phases are generated by the phase controller circuit that will be described next. The output voltage of the circuit depends on the value of the load resistance (R_L). During start-up the output voltage will be 0 V because the large output capacitor (C_o) will be discharged. This means that the output voltage cannot be used to power the phase generator; therefore a smaller SC voltage step-up circuit, controlled by the same clock, is used to create a local power supply voltage (v_{dd}). This circuit is a replica of the step-up circuits (A + B), scaled to 3% of their area, as this ratio yielded the best results, according to simulations that were performed in Spectre. This local power is decoupled internally with MOS capacitors.

D.2 MPPT regulation using the Hill Climbing method

The amount of power transferred from the PV cell to the circuit depends on the impedance presented by the step-up converter to the PV cell (Z_{in}). An increase in Z_{in} leads to an increase in the PV cell output voltage and a decrease in the output PV cell output current. The impedance should be adjusted in order to maximize the power coming from the PV cell. This means that, if the PV voltage is lower than the MPP voltage, then the PV voltage should increase. Otherwise, it should decrease. Since there is only a small amount of power available for the system, it is difficult to use hardware to compute the power by performing a multiplication between voltage and current. Therefore a different approach should be followed. The power delivered to the load depends on the output voltage and on the load resistance value. Assuming that the load resistance value is constant (or only has slight variations), the variation of the power can be determined by measuring the variation of the output voltage. This means that the MPP can be found by maximizing the output voltage. In reality, this method maximizes the power delivered to the load and not the power coming from the PV cell [15]. However, this is preferable because the final objective should always be to maximize the efficiency of the system composed by the PV cell and the step-up converter and not simply to extract the maximum power from the cell at the expense of delivering less power to the load.

The Hill Climbing MPPT circuit works by comparing the variation of the output voltage between two consecutive clock cycles. However, since the output voltage is typically connected to a large capacitor, the amount of voltage variation would be extremely small and very difficult to detect. In order to solve this problem, the local power supply voltage (v_{dd}) is monitored instead. Note, that if the load resistor decreases, this results in a decrease of the output voltage

which, in turn, leads to a decrease in the voltage of the PV cell, finally resulting in a decrease in v_{dd} that the MPPT circuit can detect.

The MPPT circuit is based on the one used in [15] and it can be observed in Fig. D.2.

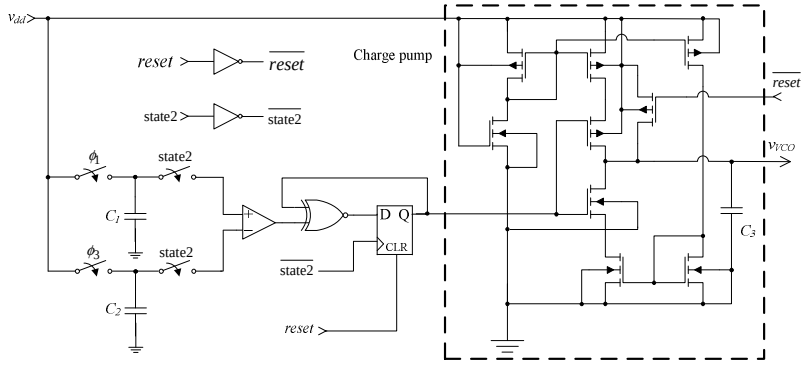


Fig. D.2 - MPPT Control Module circuit.

This circuit compares the value of v_{dd} at the end of phase ϕ_1 (v_{dd_new}) with the value of v_{dd} at the end of phase ϕ_3 (v_{dd_old}). If $v_{dd\_new} > v_{dd\_old}$ the charge pump remains in the same state, increasing (or decreasing) the v_{VCO} voltage. This will increase or decrease the clock frequency, which in turn will decrease (or increase) Z_{in}. If $v_{dd\_new} < v_{dd\_old}$ the circuit will toggle the way it was changing Z_{in} (if it was decreasing, it should now increase and *vice-versa*). The comparator circuit is as the one described in [163] (Figure 27.8, p. 914).

D.3 Phase generation and control

The three clock phases necessary for the operation of the SC step-up circuit are generated by an Asynchronous State Machine (ASM). This circuit is depicted in Fig. D.3.

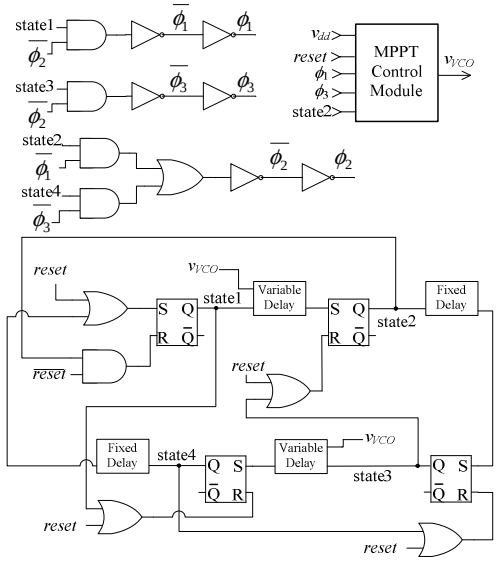


Fig. D.3 - Schematic of the phase generator.

The operation of this circuit is similar to the one described in [19], but with the improvement of explicitly preventing the phase signals from overlapping, as seen by the logic sub-circuits that provide the phase signals. This circuit has four states that are determined by the output of four latches. These states correspond to the clock phases ϕ_1, ϕ_2, ϕ_3, and again ϕ_2, respectively. In order to change from one state to the next, the *Set* signal of the latch is activated, thus changing the output of the latch from 0 to 1. This, in turn, activates the *Reset* signal of the previous latch, causing its output to change from 1 to 0 completing the state change. A start-up circuit (described in [17]) generates a *reset* signal that guarantees that the first state is state1 and that the capacitor at the v_{VCO} voltage is pre-charged to speed-up the MPPT algorithm. The frequency of operation is defined by the delay circuits inserted between the output of each latch and the *Set* input of the subsequent latch. The variable delay circuit is shown in Fig. D.4. The amount of delay of the variable delay circuits is controlled by the voltage v_{VCO} created in the MPP Control Module, depicted in Fig. D.2.

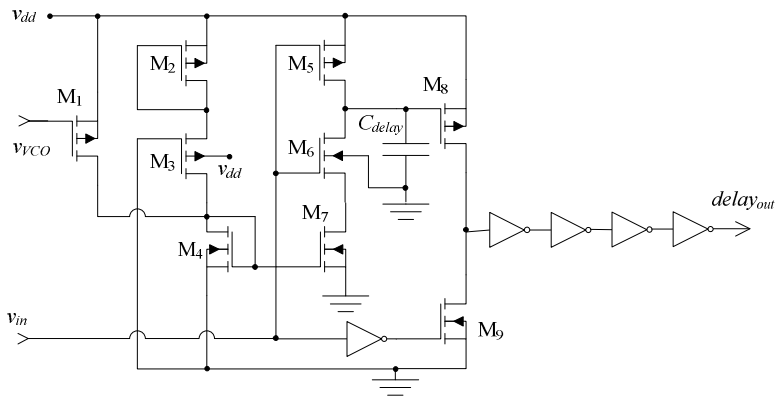


Fig. D.4 - Variable delay circuit.

The variable delay circuit only delays the rising edge of the input clock. When this input clock is *low*, transistor M_5 charges C_{delay} instantly to v_{dd}, turning off M_8 and turning on M_9. This will result in a low level to appear at the output of the circuit, after the four inverters. When the clock changes to *high*, transistor M_6 is turned on, allowing the drain current from M_7 to gradually discharge C_{delay}. After a certain time, the voltage in C_{delay} will be low enough to turn M_8 on and this will result in a HIGH level to appear at the output of the circuit. During this time, transistor M_9 is turned off to guarantee that there is no current from v_{dd} through transistors M_8 and M_9. This is necessary to limit the power dissipation of the delay circuit. The input voltage v_{VCO} controls the drain current of the PMOS transistor M_1. This current is added to the drain current of M_2 and mirrored through M_4 and M_7 [175]. Thus, an increase in the v_{VCO} voltage results in a decrease in the mirrored current and, ultimately, in an increase in the delay value.

D.4 Simulation results

The step-up converter was designed to work with a single amorphous PV cell, the same as in [19], with an area of about 1 cm^2, supplying a maximum power of 1775 µW and an MPP voltage of 403 mV, in a standard 0.13 µm CMOS technology with V_{TN} = 0.38 V and V_{TP} = – 0.33 V.

In order to verify the MPPT behavior of the circuit, the value of the current I_1 in the PV cell model, shown in Fig. 2.19 a), was changed from its maximum value (100%) to a lower value (17.5% or 19%, according to the test) to simulate the change of illumination conditions. The value of the output capacitor of the circuit (C_o) was only 10 nF due to simulation time restrictions. This results in a larger ripple in the output voltage. The behavior of the circuit, when the illumination changes from 100% to 17.5%, is shown in Fig. D.5.

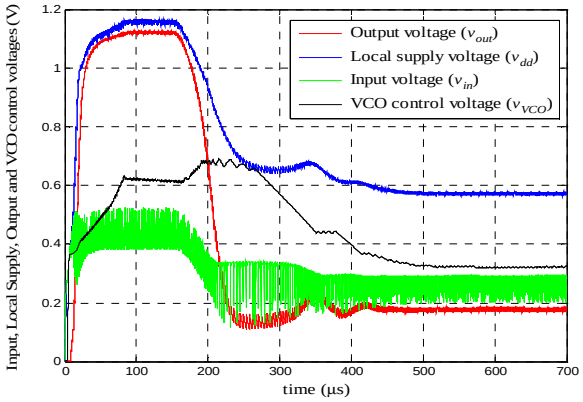


Fig. D.5 - Evolution of v_{in}, v_{dd}, v_{out} and v_{VCO}, during start-up and transient operation (illumination of 100% and 17.5%, changing at 150 µs).

This simulation shows that, under low illumination, the MPPT circuit is still capable of operating with a PV voltage as low as 0.28 V, resulting in a local power supply voltage of only 0.57 V. This corresponds to the lowest illumination for which the circuit was capable of operating. The circuit is capable of starting-up with 19% of maximum illumination and a load resistance of 1 kΩ, as shown in Fig. D.6.

Also, the circuit is capable of withstanding a change in the output resistor from 1 kΩ to 100 Ω, under maximum illumination, as shown in Fig. D.7. In these tested situations, the changes of illumination, or resistance, took 1 µs to be completed.

The average relevant parameters of the converter circuit, for the different illuminations, were calculated from the previous simulations, using the time interval where the system behavior was stable (steady-state). These results are summarized and presented in TABLE D.1.

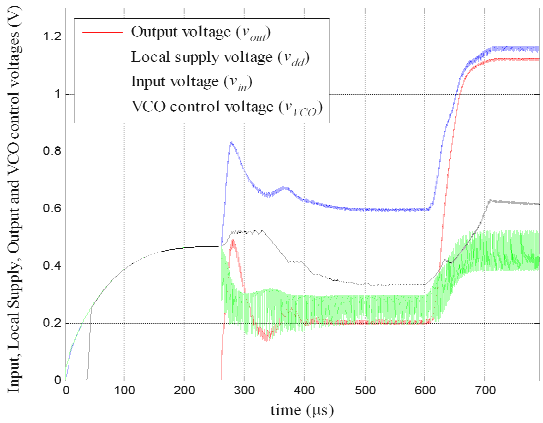


Fig. D.6 - Evolution of v_{in}, v_{dd}, v_{out} and v_{VCO}, during start-up and transient operation (illumination of 19% and 100%, changing at 600 µs).

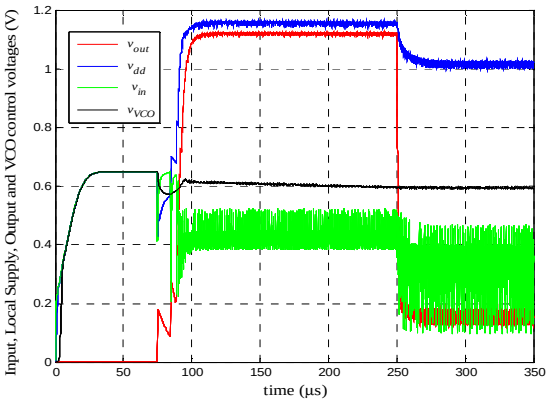


Fig. D.7 - Evolution of v_{in}, v_{dd}, v_{out} and v_{VCO}, during start-up and transient operation (Ilumination of 100% and load resistance changing at 250 µs from 1 kΩ to 100 Ω).

TABLE D.1 - Steady-state performance of the step-up circuit.

Light Intensity (max. PV power)	**R_L = 1 kΩ**						
	P_{out} (µW)	**P_{in} (µW)**	**v_{out} (V)**	**v_{in} (V)**	**v_{dd} (V)**	**f_{CLK} (MHz)**	**η (%)**
100% (1775 µW)	1266	1712	1.13	0.43	1.16	1.756	73.9
19% (167 µW)	42.2	148	0.21	0.28	0.88	0.423	28.6
17.5% (141 µW)	31.6	126	0.18	0.28	0.57	0.380	25.0

Next, in Fig. D.8, one can observe the efficiency and power values of the circuit for different values of the load resistance, obtained through electrical simulations in Spectre.

This graph shows that when the load resistance is 750 Ω, the maximum efficiency of the circuit is 74.13%, for a power delivered to the load of 1269 µW and a solar cell power of 1712 µW. In this situation, v_{in} converged to 401 mV.

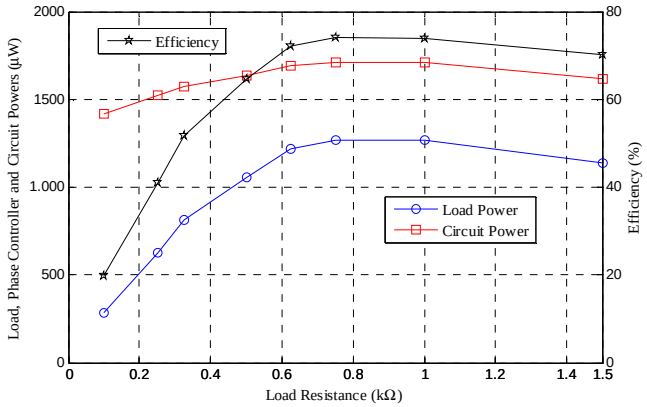


Fig. D.8 - Efficiency, circuit (input) power and load (output) power, as a function of the load resistance.

D.5 Conclusions

A step-up micro-power converter for solar energy harvesting applications was presented. The circuit uses a SC voltage tripler architecture, controlled by an MPPT circuit implementing a Hill Climbing algorithm. This circuit was designed in a 0.13 µm CMOS technology in order to work with a a-Si PV cell. The circuit uses a local power supply voltage, created using a scaled-down SC voltage tripler (controlled by the same MPPT circuit) to make the circuit more robust to load and illumination variations. The SC circuits use a combination of PMOS and NMOS transistors, instead of MiM capacitors, to reduce the occupied area. A charge reuse scheme is used to compensate for the loss of charge due to the large parasitic capacitances associated to the bottom plate nodes of the MOS capacitors. Simulation results showed that the circuit can deliver a power of 1266 µW to the load using 1712 µW of power from the PV cell, corresponding to an efficiency as high as 73.91%, with a 1 kΩ load. The simulations also show that the circuit is capable of starting-up with only 19% of the maximum illumination level.