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Analysis and Implementation of a Multi-Ratio Switched Capacitor DC-DC Converter for a Supercapacitor Power Supply

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To Raquel and my family

Acknowledgements

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Abstract

An energy harvesting system requires an energy storing device to store the energy retrieved from the surrounding environment. This can either be a rechargeable battery or a supercapcitor. Due to the limited lifetime of rechargeable batteries, they need to be periodically replaced. Therefore, a supercapacitor, which has ideally a limitless number of charge/discharge cycles can be used to store the energy; however, a voltage regulator is required to obtain a constant output voltage as the supercapacitor discharges. This can be implemented by a Switched-Capacitor DC-DC converter which allows a complete integration in CMOS technology, although it requires several topologies in order to obtain a high efficiency. This thesis presents the complete analysis of four different topologies in order to determine expressions that allow to design and determine the optimum input voltage ranges for each topology. To better understand the parasitic effects, the implementation of the capacitors and the non-ideal effect of the switches, in 130 nm technology, were carefully studied. With these two analysis a multi-ratio SC DC-DC converter was designed with an output power of 2 mW, maximum efficiency of 77%, and a maximum output ripple, in the steady state, of 23 mV; for an input voltage swing of 2.3 V to 0.85 V. This proposed converter has four operation states that perform the conversion ratios of $1/2$, $2/3$, $1/1$ and $3/2$ and its clock frequency is automatically adjusted to produce a stable output voltage of 1 V. These features are implemented through two distinct controller circuits that use asynchronous time machines (ASM) to dynamically adjust the clock frequency and to select the active state of the converter. All the theoretical expressions as well as the behaviour of the whole system was verified using electrical simulations.

Keywords: DC-DC power converters, Switched capacitor circuits, Supercapacitor, Performance analyses, Design optimization, Efficiency, CMOS, Fully integrated converter.

RESUMO

Um sistema de recolha de energia necessita de um dispositivo de armazenamento de energia, para armazenar a energia recolhida do ambiente, em que este está inserido. Esta energia pode ser armazenada quer numa bateria recarregável, quer num supercondensador. Devido ao tempo de vida limitado das baterias recarregáveis, estas têm de ser substituídas periodicamente. Um supercondensador é caracterizado por ter numero quase ilimitado de cargas e descargas, permitindo assim, um tempo de vida útil muito superior ao das baterias. Contudo, é necessário a utilização de um regulador de tensão de modo a obter-se uma tensão de saída constante à medida que a tensão no condensador vai decrescendo. Para este fim, pode ser utilizado um conversor DC-DC baseado em condensadores comutados (SC), que permite uma total integração em circuitos integrados. No entanto, este precisa de múltiplas topologias de modo a obter eficiências altas. Esta tese apresenta uma analise completa de quatro diferentes topologias de circuitos DC-DC SC, de modo a obter equações matemáticas que permitem descrever o seu funcionamento, e determinar a gama ótima de tensão entrada para cada topologia. Para uma melhor compreensão dos efeitos devido às capacidades parasitas e efeitos não lineares provenientes dos condensadores flutuantes e dos interruptores, estes,foram cuidadosamente estudados na tecnologia CMOS de 130 nm. Estas duas análises, em conjunto, permitiram a implementação de um conversor multi-rácio SC DC-DC com uma potência de saída de 2 mW, eficiência máxima de 76% e um ripple máximo (em regime permanente) na tensão de saída de 23 mV. Este conversor proposto tem quatro estados que produzem idealmente os rácios de conversão de $1/2$, $2/3$, $1/1$ e $3/2$. A sua frequência interna é automaticamente ajustada, de modo a que a tensão de saída permaneça constante em torno de 1 V. Estas duas funcionalidades são implementadas por dois controladores distintos, que fazem uso de máquinas de estados assíncronas (ASM), uma que ajusta dinamicamente a frequência do relógio, e outra que seleciona o estado atual do conversor. Todas as expressões teóricas bem como o comportamento de todo o sistema, foram verificados e validados através de simulações eléctricas.

Palavras-chave: DC-DC conversores de potência, Circuitos de condensadores comutados, Supercondensador, analise de desempenho, modelo de optimização, Eficiência, CMOS.

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Acronyms

ASM Asynchronous state machine.

CMOS Complementary metal-oxide-semiconductor.

DC-DC Direct current to direct current.

IoT Internet of Things.

LDO Low-dropout.

MIM Metal-Insulator-Metal.

SC Switched Capacitor.

VCO Voltage-controlled oscillator.

CHAPTER 1

INTRODUCTION

1.1 Motivation and Background

In order to achieve infinite operation, electronic systems must obtain their energy directly from the surrounding environment [1]. This kind of procedure is commonly known as energy harvesting. Depending on the environment where the system is located, there are different energy sources that can be harvested [2]. In the case of systems with small size, the available energy is necessarily reduced, typically only providing a fraction of the necessary power needed for the continuous operation of the system. Therefore, such a system has to be powered down while it harvests enough energy in order to work during a short time and then, this cycle is repeated. This type of operation is useful for wireless sensor nodes, where the node only needs to report data periodically. This operation requires an energy storing device, which can be either a rechargeable battery or a supercapacitor. A rechargeable battery has the advantage of having a larger energy storing capacity, but its lifetime is seriously reduced by the number of charge/discharge cycles (typically the maximum number is around 1000 cycles). A supercapacitor has the advantage of having limitless charge/discharge cycles and being less expensive than a battery, although it stores much less energy for the same volume [3]. Depending on the mode of operation of the energy harvesting system, a battery, a supercapacitor or both, can be used as the energy storing device. In the case of a low power remote sensor that uses a power-down power-up cycle, it makes more sense to use a supercapacitor as the energy storage, since batteries need to be replaced periodically. If a large number of sensors are deployed and if they are in places that are difficult to access, this replacement can become expensive and difficult. Furthermore, the present trends like Internet of Things (IoT) could benefit from having systems with lower maintenance.

The energy stored in a capacitor is given by $E_c = 1/2 \cdot C \cdot V_c^2$, this means that as the capacitor supplies energy to the circuit its output voltage drops. As an example a 1 F

supercapacitor charged to its maximum voltage (usually 2.3 V) can store 2.645 J, if this capacitor supplies energy for a circuit with a supply current of 10 mA during 10 s, its output voltage would drop $\Delta V_c = (I \cdot \Delta t)/C = 100$ mV. Since the power supply voltage of the circuit should be constant, it is necessary to have a voltage regulator between the supercapacitor and the circuit. A voltage regulator is necessary to be able to both down-convert and up-convert the input voltage in order to achieve high efficiency that maximize the supercapacitor energy retrieved. This prevents the use of a linear voltage converter, because it can only step-down the voltage and its efficiency is reduced when the input voltage is much larger than the output voltage.

The voltage regulator can be implemented using either an inductor based or a capacitor based DC-DC converter. The first option requires an inductor which is not feasible to implement in a CMOS integrated circuit. The second option can be fully integrated in a CMOS integrated circuit; however, SC based DC-DC converters have maximum efficiency for a specific input output voltage ratio. This means that in order to maintain a high efficiency, the SC voltage converter circuit has to change its topology as the input supercapacitor voltages decreases [4]. Therefore a careful analysis of each converter topology should be carried out to determine its efficiency as a function of the input voltage and the different parasitic capacitance of the circuit. This analysis will determine the voltages values that will result in a change in the voltage conversion factor.

For this multi-ratio SC DC-DC converter to work it needs an adjacent system. This is depicted in Fig. 1.1. Apart from the converter, the system is composed by four other circuits: Start up, Drivers, Phase and State controllers. The Start up circuit is responsible for the power up of the system. Its task is to pull the output node to 1 V through the input power supply (Supercapacitor) in order to provide a power supply voltage for the converter to start working. The drivers are used to feed the clock signals to the switches

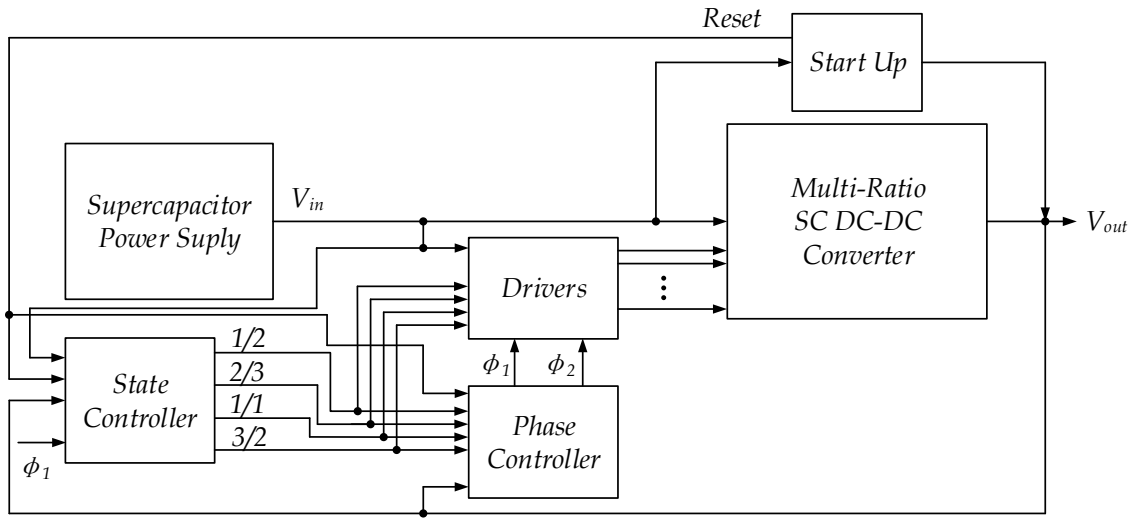


Figure 1.1: Diagram of the proposed system

of the converter and determine the topology, as well as the charge and discharge of the flying capacitors in each clock phase. These clock phases are generated through the phase controller which detects if the output voltage is above/below 1 V and produces two non-overlapping complementary clock signals which frequency is adjusted to maintain a stable output voltage of 1 V. The state controller defines whose topology must be activated for a given voltage level of the supercapacitor and supplies this information to both the drivers and the phase controller so they can carry out their task.

1.2 Thesis Organization

This thesis is organized in 6 chapters, including this introductory one. In Chapter 2 a theoretical analysis of four SC DC-DC converter topologies: the step-down 1/2 and 2/3; the 1/1 and the step-up 3/2 converters is presented. Two distinct analyses for each converter: the first shows the effect on the output voltage due to the flying capacitors, parasitic capacitances, output power and the operation frequency were carried out. The second, studies the efficiency and the corresponding impact on it due to the parasitic capacitances of the flying capacitors and of the switches.

In chapter 3 the choice of the technology used to implement the flying capacitors was studied. The issues of the 130-nm CMOS technology regarding the switches implementation - resistance, area, parasitic capacitances and power consumption. Lastly, it is determined a theoretical expression to size each switch for each converter topology and through that determine the parasitic capacitance and power consumption.

The following chapter, chapter 4, the proposed multi-ratio SC DC-DC converter and the overall system are shown. The converter and each adjacent circuit of the system is detailed analysed and explained.

The simulation results of the whole system are depicted and discussed in chapter 5. Finally, chapter 6 presents the conclusions and the future work of this thesis.

1.3 Contributions

The main contribution of this thesis is the study, design, and validation through electrical simulation (using spectre) of a Power Management Unit (PMU) composed by a multi-ratio SC DC-DC, a clock and phase generator and a start-up circuit.

The SC DC-DC converter can be configured into 4 different topologies in order to maximize the conversion efficiency when the input voltage changes from 2.3 V to 0.85 V and the output voltage is constant at 1 V. The clock and phase generator automatically adjusts the clock frequency (using negative feedback) in order to maintain the output voltage constant. A state machine associated to this circuit selects the topology that maximizes the efficiency of the DC DC converter using the input voltage value. The start-up circuit guaranties that when a charged supercapacitor is connected to the input, the system starts to operate in the correct state.

The development of this system allowed the author a better understand of the behaviour and working principle of SC DC-DC converters, as well as the limitations and characteristics of the 130-nm CMOS technology. During the development a significant number of limitations that were not expected at the beginning were encountered. These were overcome and lead to a better understand of the non-ideal effects presented in this field of work. Moreover, the design of an entire system showed other arising problems such as the overlap of the clocks, kickback noise, parasitic capacitances, and feed-forward problems.

Chapter 2 and the beginning of chapter 3 originated a paper [5] that has been orally presented in the field of Electronics and Telecommunication, at the 5^{th} Doctoral Conference on Computing Electrical and Industrial Systems (DoCEIS).

CHAPTER 2

ANALYSIS OF THE SC DC-DC CONVERTER TOPOLOGIES

As previously explained in chapter 1, a SC based DC-DC converter achieves maximum efficiency for a specific input/output voltage ratio. This means that as the supercapacitor discharges and its input voltage drops while the output voltage remains constant, it is necessary to use different topologies for the SC converter circuit in order to maintain high efficiency. There is a compromise between the number of different topologies and the

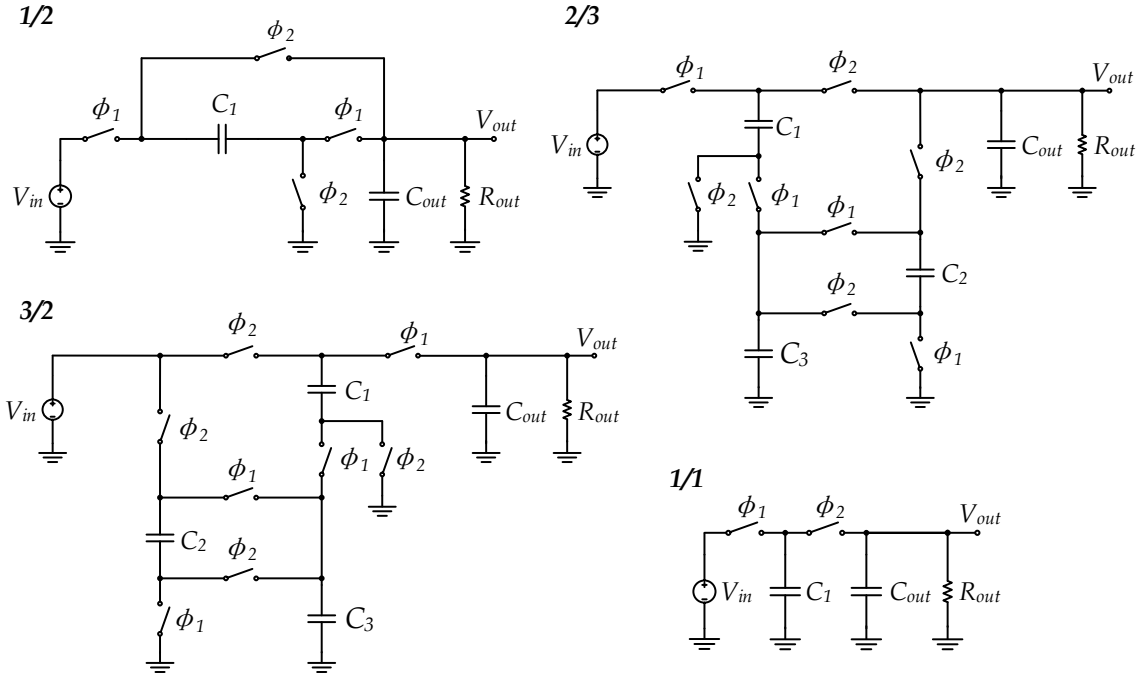


Figure 2.1: Simplified schematic of the selected topologies for the SC DC-DC converters

complexity of the circuit. In this case, the input voltage can vary from 2.3 V to 0 V and the output voltage should be held constant around 1 V. Assuming that a supercapacitor with 1 F is used, the available energy, for the maximum voltage, will be 2.645 J. When the capacitor voltage is equal to 1 V the energy remaining in the capacitor is still 0.5 J and when it is equal to 0.7 V the remaining energy is only 0.245 J. This means that there is a small pay-off in trying to up-convert input voltages smaller than 0.7 V, which would require a circuit with a voltage conversion factor larger than 2. After analysing the efficiency of several voltage conversion circuits for the different input voltages, it was decided to use only 4 SC DC-DC voltage converter circuits. These are depicted in Fig. 2.1 and correspond to the voltage conversion factors of $1/2$, $2/3$, $1/1$ and $3/2$ [4]. Each of these converters is responsible for a given range of the input voltage (where its efficiency is maximized) and its clock frequency is adjusted in order to obtain an output voltage of 1 V, independently of the input voltage and of the load. These 4 topologies can be combined into a single circuit with 3 capacitors that can be configured to any of the 4 topology using switches [4]. In order to determine what are the input voltage ranges that maximize the efficiency for the different topologies it is necessary to analyse the behaviour of each converter to determine its operating parameters (efficiency and output voltage) as function of the different design parameters (capacitance values, clock frequency, etc.) and the different non-ideal effects (e.g. parasitic capacitance, switch ON resistance).

2.1 Analysis of the SC DC-DC 1/2 Step Down Converter

2.1.1 Analyses of the Output Voltage

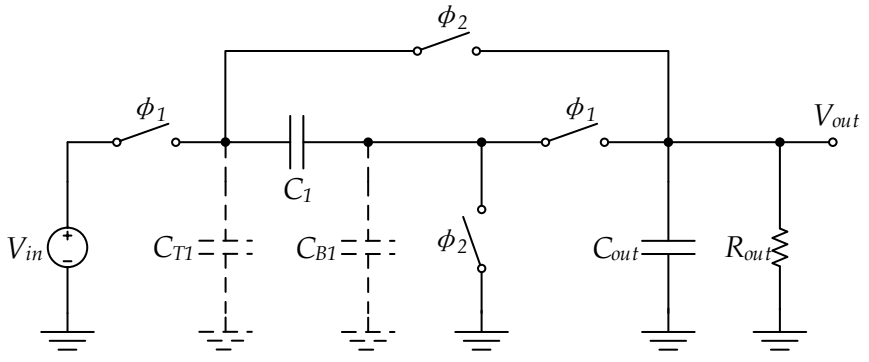
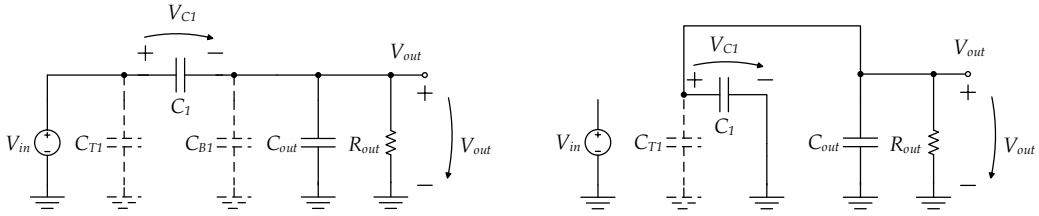


Figure 2.2: Simplified schematic of the $1/2$ converter

Figure 2.2 shows the topology chosen to down-convert the input voltage (V_{in}) into two times smaller, $V_{out} = V_{in}/2$ [4]. The operation of this circuit is divided in two different phases: phase one (ϕ_1) in which the capacitors C_1 and C_{out} are connected in series with the

input voltage V_{in}; and phase two (ϕ_2) where the capacitors C_1 and C_{out} are now connected in parallel resulting in, ideally, an output voltage (V_{out}) of half the input voltage.



(a) Phase 1: ϕ_1 (b) Phase 2: ϕ_2

Figure 2.3: Simplified schematic of the 1/2 SC converter in the two phases

Figures 2.3(a) and 2.3(b) show the schematics of the resulting circuit in each clock phase (ϕ_1 and ϕ_2). The two capacitors C_{T1} and C_{B1} represent the top and the bottom plate parasitic capacitances of the flying capacitor C_1, respectively. At the beginning of phase ϕ_1 there is charge conservation between C_1 and C_{out}. Notice that there is also a load resistor (R_{out}) in parallel with C_{out}. Therefore, some of the charge is going to flow through R_{out}. During the phase ϕ_1 the voltage on the node V_{out} decreases exponentially between $V_{out_{min}}$ and $V_{out_{max}}$. Assuming that $C_{out} \times R_{out} \gg T_{CLK}$ allow considering that $V_{out_{min}} = V_{out_{max}}$ and so the amount of charge flowing through R_{out} can be easily determined by (2.1) [6]. Notice that phase ϕ_1 last only $T_{CLK}/2$. The same procedure can be applied to phase ϕ_2.

$$\Delta Q_{R_{out}} = \overline{I_{out}} \cdot \frac{T_{CLK}}{2} = \frac{v_{out} \cdot T_{CLK}}{2 \cdot R_{out}} \tag{2.1}$$

The conventional switched-capacitor circuit analysis techniques [7](Chapter 5) determines the charge in each capacitor at the end of each clock phase: $(n-1) \times T_{CLK}$ (phase ϕ_1), $(n-1/2) \times T_{CLK}$ (phase ϕ_2) and $n \times T_{CLK}$ (phase ϕ_1). When the circuit changes from ϕ_1 to ϕ_2, there is charge conservation in the node that connects the top plate of C_1, C_{T1} and C_{out}. Therefore, in phase ϕ_2 at $(n-1/2) \times T_{CLK}$ the charge from the top plates of C_1, C_{T1} and C_{out} is equal to the charge from the top plate of C_1, C_{T1} and C_{out} at ϕ_1 at $(n-1) \times T_{CLK}$ plus the charge lost from R_{out} during ϕ_1, $\Delta Q_{R_{out}}$. In the transition from phase ϕ_2 to ϕ_1 the node that connects the bottom plate of C_1 the top plate of C_{B1} and C_{out} has charge conservation. Thus, the sum of the charges of C_1, C_{B1}, C_{out} at ϕ_1 at $n \times T_{CLK}$ is equal to the sum of C_1 and C_{out} from ϕ_2 at $(n-1/2) \times T_{CLK}$ and the charge lost in R_{out} during ϕ_2. The resulting system of the equations described can be seen in (2.2) and (2.3).

$$Q_{C_1}^{\phi_1} + Q_{C_{T1}}^{\phi_1} + Q_{C_{out}}^{\phi_1} = Q_{C_1}^{\phi_2} + Q_{C_{T1}}^{\phi_2} + Q_{C_{out}}^{\phi_2} + \Delta Q_{R_{out}} \quad , \quad \phi_1 \rightarrow \phi_2 \tag{2.2}$$

$$-Q_{C_1}^{\phi_2} + Q_{C_{out}}^{\phi_2} = -Q_{C_1}^{\phi_1} + Q_{C_{B1}}^{\phi_1} + Q_{C_{out}}^{\phi_1} + \Delta Q_{R_{out}} \quad , \quad \phi_2 \rightarrow \phi_1 \tag{2.3}$$

Replacing $Q = V \cdot C$ in (2.2) and (2.3) results in the set of equations shown below.

$$\begin{aligned} &(V_{in} - V_{out}[n-1])\, C_1 + V_{out}[n-1]\, C_{out} + V_{in}\, C_{T1} = V_{out}\left[n - \frac{1}{2}\right] \left(C_1 + C_{T1} + C_{out} + \frac{T}{2\, R_{out}}\right) \\ &V_{out}\left[n - \frac{1}{2}\right] (-C_1 + C_{out}) = (V_{out}[n] - V_{in})\, C_1 + V_{out}[n] \left(C_{B1} + C_{out} + \frac{T}{2\, R_{out}}\right) \end{aligned} \tag{2.4}$$

Solving in order to $V_{out}[n]$ results in

$$V_{out}[n] = \frac{2\,R_{out}\left(V_{in}\left(2\,C_{out}\,R_{out}\left(2\,C_1 + C_{T1}\right) + C_1\,T\right) + 2\,R_{out}\left(C_1 - C_{out}\right)^2 V_{out}[n-1]\right)}{\left(2\,R_{out}\left(C_1 + C_{B1} + C_{out}\right) + T\right)\left(2\,R_{out}(C_1 + C_{out} + C_{T1}) + T\right)} \tag{2.5}$$

Considering only the steady state condition ($V_{out}[n] = V_{out}[n-1] = V_{out}$)

$$V_{out} = \frac{2\,R_{out}\,V_{in}\left(2\,C_{out}\,R_{out}\left(2\,C_1 + C_{T1}\right) + C_1\,T\right)}{4\,R_{out}^2(C_1\left(C_{B1} + 4\,C_{out} + C_{T1}\right) + C_{B1}\left(C_{out} + C_{T1}\right) + C_{out}\,C_{T1}) + 2R_{out}\,T\left(2\,C_1 + C_{B1} + 2\,C_{out} + C_{T1}\right) + T^2} \tag{2.6}$$

Since $C_{out} \gg C_1$, the approximation $C_{out} \to \infty$ can be applied in (2.6). In this case C_{out} only affects the ripple of V_{out}. The resulting equation is

$$V_{out} = \frac{R_{out}\,V_{in}\left(2\,C_1 + C_{T1}\right)}{R_{out}\left(4\,C_1 + C_{B1} + C_{T1}\right) + T} \tag{2.7}$$

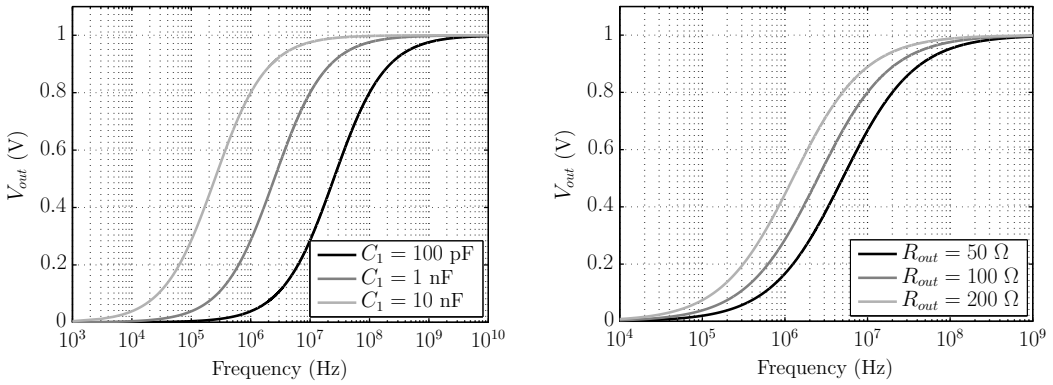
or as a function of the clock frequency ($F = 1/T$)

$$V_{out} = \frac{F\,R_{out}\,V_{in}\left(2\,C_1 + C_{T1}\right)}{F\,R_{out}\left(4\,C_1 + C_{B1} + C_{T1}\right) + 1} \tag{2.8}$$

Finally, for simplicity it is possible to look at the equation considering an ideal capacitor ($C_{T1} = C_{B1} = 0$) in order of T_{CLK} or F_{CLK}.

$$V_{out} = \frac{2\,C_1\,R_{out}\,V_{in}}{4\,C_1\,R_{out} + T} \tag{2.9}$$

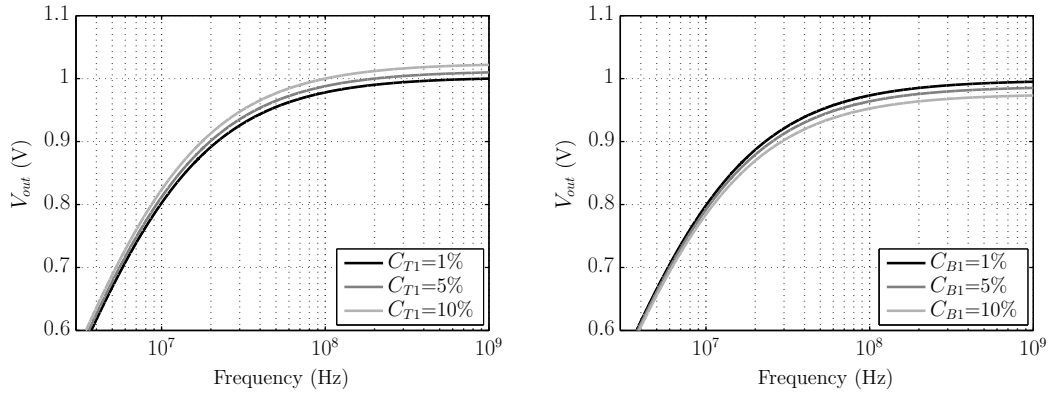
$$V_{out} = \frac{2\,C_1\,F\,R_{out}\,V_{in}}{1 + 4\,C_1\,F\,R_{out}} \tag{2.10}$$



(a) C_1 effect with $R_{out} = 100\ \Omega$ (b) R_{out} effect with $C_1 = 1$ nF

Figure 2.4: V_{out} as function of the clock frequency for $V_{in} = 2$ V

Figure 2.4(a) shows the plot of (2.10) where it can be seen the impact that C_1 has on V_{out} for a given value of frequency. It is possible to see that C_1 restricts the minimum value of the working frequency in order to have V_{out} equal to 1 V. Figure 2.4(b) shows V_{out} for three different values of R_{out}. These values represent three different power output values ($R_{out} = 50\ \Omega \to P_{out} = 20$ mW, $R_{out} = 100\ \Omega \to P_{out} = 10$ mW, and $R_{out} = 200\ \Omega \to$



(a) C_{T1} effect with $C_{B1} = 0$ (b) C_{B1} effect with $C_{T1} = 0$

Figure 2.5: V_{out} as function of the clock frequency for $V_{in} = 2$ V, $C_1 = 1$ nF and $R_{out} = 100\,\Omega$

$P_{out} = 5$ mW). Once again, an increase in R_{out} results in an increase of the minimum working frequency in order to maintain the output voltage constant.

Figures 2.5(a) and 2.5(b) show the plot of (2.8) as function of the clock frequency for different values of C_{T1} and C_{B1}. As C_{T1} increases V_{out} increases its value. This effect is easily explain because C_{T1} charges to V_{in} in ϕ_1 and in ϕ_2 discharges this extra voltage to V_{out}. The effect of C_{B1} is the opposite. C_{B1} charges to V_{out} in ϕ_2, and in ϕ_1 discharge to zero. If both parasitic capacitances were equal, V_{out} would remain unchanged. Nevertheless, this extra charge and discharge will increase the current drain from V_{in} and V_{out}. Even though that V_{out} remains the same, these capacitance will lead do lower efficiencies.

By solving (2.8) in order to the frequency (2.11) it is possible to determine the required frequency for the converter to produce an output voltage of 1 V (for example) for a given V_{in}, C_1 and R_{out}.

$$F_{CLK_{1/2}} = \frac{V_{out}}{R_{out}\left(2\,C_1\left(V_{in} - 2\,V_{out}\right) + C_{T1}\left(V_{in} - V_{out}\right) - C_{B1}\,V_{out}\right)} \tag{2.11}$$

considering an ideal capacitor (2.11) results in

$$F_{CLK_{1/2}} = \frac{V_{out}}{2\,R_{out}\,C_1\left(V_{in} - 2\,V_{out}\right)} \tag{2.12}$$

Figure 2.6 shows the plot of (2.12) for different values of the output resistance with $C_1 = 1$ nF and $V_{out} = 1$ V. For $V_{out} = 1$ V the optimum point of conversion would be at $V_{in} = 2$ V. However, since R_{out} determines the current drain from the output node, in the optimum point of conversion, the frequency would have to be infinite in order for the current to be larger than zero. This is why the asymptote at $V_{in} = 2$ V appears in the graph. As V_{in} increases, the converter produces an output voltage higher than 1 V. Therefore, in order to adjust the value of V_{out} to 1 V, the amount of charge transferred to R_{out} must decrease, thus the clock frequency must decrease. With V_{out} fixed at 1 V, an increase in R_{out} reduces the drained current - Ohms Law. Hence the amount of charge lost per time period is lower and so the frequency can be decreased.

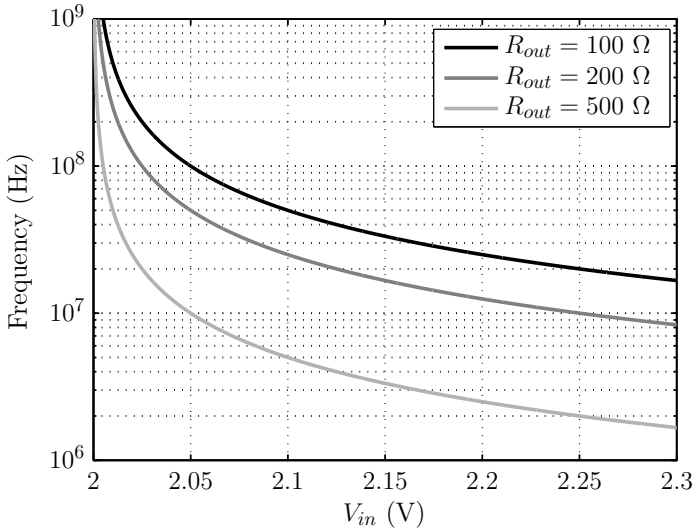
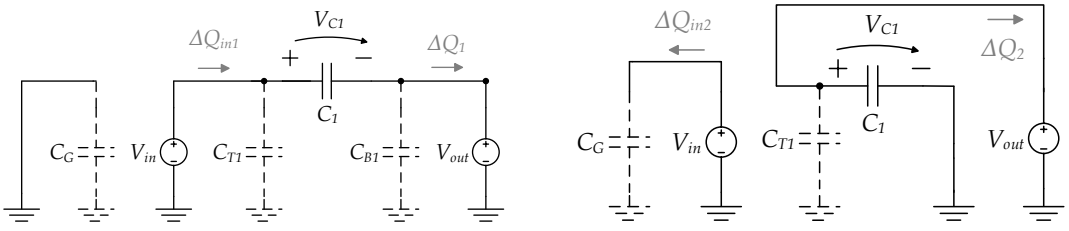


Figure 2.6: F_{CLK} as function of V_{in} for $V_{out} = 1$ V and $C_1 = 1$ nF

2.1.2 Analysis of the Efficiency

Assuming that the clock frequency is adjusted to have the desired output voltage (e.g. V_{out}=1 V) and that output decoupling capacitor C_{out} is large enough, it is reasonable to assume that the output voltage value is constant. In this case, the schematics of the 1/2 converter circuit with an ideal output voltage supply connected to V_{out} during phase ϕ_1 and ϕ_2 are shown in figure 2.7(a) and 2.7(b) respectively. In these, C_G represents the gate capacitance of all the CMOS switches in the circuit. In each clock cycle, the switches drain a charge (ΔQ_{in2}) from V_{in} through the clock buffers. Using conventional switched-capacitor circuit analysis techniques [5](Chapter 5) it is possible to determine the charge in each capacitor at the end of each clock phase. The resulting equations are shown in (2.13) and



(a) Phase 1: ϕ_1 (b) Phase 2: ϕ_2

Figure 2.7: Simplified schematic of the 1/2 SC DC-DC converter in each phase, with an ideal output voltage source

these allow to determine ΔQ_{in1}, ΔQ_{in2}, ΔQ_1, and ΔQ_2.

$$\begin{cases} (V_{in} - V_{out})\ C_1 + V_{in}\, C_{T1} = V_{out}\ (C_1 + C_{T1}) + \Delta Q_2 \\ 0 = V_{in}\, C_G + \Delta Q_{in2} \\ -V_{out}\, C_1 = (V_{out} - V_{in})\ C_1 + V_{out}\, C_{B1} + \Delta Q_1 \\ V_{out}\ (C_1 + C_{T1}) = (V_{in} - V_{out})\ C_1 + V_{in}\, C_{T1} + \Delta Q_{in1} \end{cases} \tag{2.13}$$

where $\Delta Q_{1,2}$ is the charge absorbed by the output power supply in each phase. Solving the previous equations in order to ΔQ_{in1}, ΔQ_{in2}, ΔQ_1, and ΔQ_2; results in

$$\begin{cases} \Delta Q_{in1} = -C_1\, V_{in} - C_{T1}\, V_{in} + 2\, C_1\, V_{out} + C_{T1}\, V_{out} \\ \Delta Q_{in2} = -C_G\, V_{in} \\ \Delta Q_1 = C_1\, V_{in} - 2\, C_1\, V_{out} - C_{B1}\, V_{out} \\ \Delta Q_2 = C_1\, V_{in} + C_{T1}\, V_{in} - 2\, C_1\, V_{out} - C_{T1}\, V_{out} \end{cases} \tag{2.14}$$

The input (P_{in}) and output (P_{out}) power are calculated using ΔQ_{in1}, ΔQ_{in2}, ΔQ_1, ΔQ_2 and the values of V_{in} and V_{out}. These are given by

$$\begin{cases} P_{in} = I_{in}\, V_{in} = V_{in}\ (\Delta Q_{in1} + \Delta Q_{in2})\ F_{CLK} \\ P_{out} = I_{out}\, V_{out} = V_{out}\, (\Delta Q_1 + \Delta Q_2)\, F_{CLK} \end{cases} \tag{2.15}$$

$$\begin{cases} P_{in} = V_{in}\, (V_{out}\, (2\, C_1 + C_{T1}) - V_{in}\, (C_1 + C_G + C_{T1}))\, F_{CLK} \\ P_{out} = -V_{out}\, (-2\, C_1\, V_{in} + 4\, C_1\, V_{out} + C_{B1}\, V_{out} - C_{T1}\, V_{in} + C_{T1}\, V_{out})\, F_{CLK} \end{cases} \tag{2.16}$$

The efficiency (η) is defined as the ratio between P_{out} and P_{in}, it is given by

$$\eta_{1/2} = \frac{|P_{out}|}{|P_{in}|} = \frac{V_{out}\, ((2\, C_1 + C_{T1})\, V_{in} - (4\, C_1 + C_{B1} + C_{T1})\, V_{out})}{V_{in}\, ((C_1 + C_G + C_{T1})\, V_{in} - (2\, C_1 + C_{T1})\, V_{out})} \tag{2.17}$$

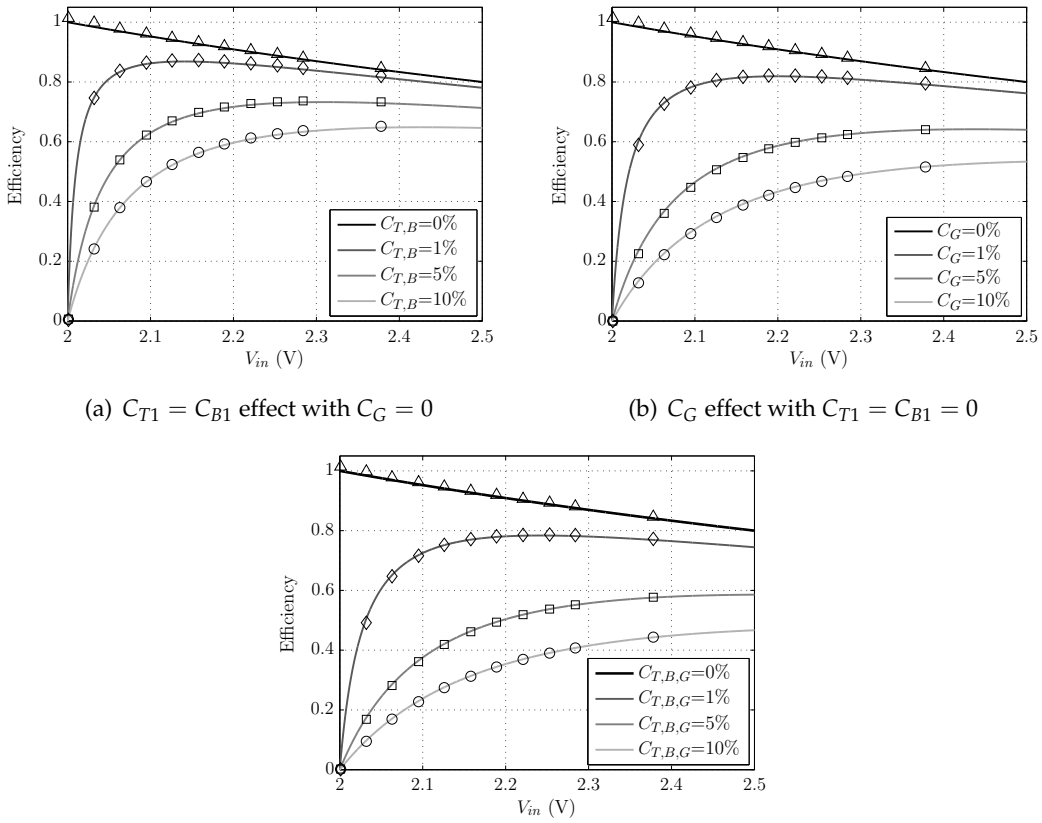
this equation can be solved for $V_{out} = 1$ V resulting in

$$\eta_{1/2} = \frac{-V_{in}\, (2\, C_1 + C_{T1}) + 4\, C_1 + C_{B1} + C_{T1}}{V_{in}\, (-V_{in}\, (C_1 + C_G + C_{T1}) + 2\, C_1 + C_{T1})} \tag{2.18}$$

Notice that $\eta_{1/2}$ does not depend on the clock frequency, but only on the ratio between C_1 and the parasitic capacitances C_{T1}, C_{B1} and C_G; for a given value of V_{in}. The 1/2 converter circuit was simulated in Spectre with ideal switches and capacitors for different input voltages between 2 to 2.5 V and with V_{out} fixed at 1 V. From these transient simulations its efficiency was calculated and compared to the efficiency calculated using (2.18) for different parasitic capacitance values.

First, the effect of both top and bottom plate parasitic capacitances ($C_{T1} = C_{B1}$) of C_1 was analysed assuming that the switch parasitic capacitances $C_G = 0$. Therefore, (2.18) was plotted for different values of C_{T1} and C_{B1} (0%, 1 %, 5 % and 10% of C_1) Fig. 2.8(a). For

$C_{B1} = C_{T1} = 0$ the efficiency decreases almost in a straight line as the value of V_{in} increases. However, as C_{T1} and C_{B1} increases the efficiency decreases and the maximum achievable efficiency shifts to higher values of V_{in}. Figure 2.8(b) shows the plot of the efficiency with the effect of C_G ($C_{T1} = C_{B1} = 0$). This effect is similar to the top and bottom parasitic capacitance, even though the relation between the increase of C_G and the corresponding decrease in η is more considerable. Lastly, Fig. 2.8(c) shows the plot for $C_{BT1} = C_{B1} = C_G$. The behaviour is similar to the previous plots, although the decrease in η is more marked. The simulation results (markers) prove that (2.18) accurately describes the behaviour of the converter efficiency and validates the theoretical analysis.



(a) $C_{T1} = C_{B1}$ effect with $C_G = 0$

(b) C_G effect with $C_{T1} = C_{B1} = 0$

(c) $C_{T1} = C_{B1} = C_G$ effect

Figure 2.8: Efficiency of the 1/2 converter circuit as function of V_{in} with $C_1 = 1$ nF, $V_{out} = 1$ V for different values of C_{T1}, C_{B1} and C_G

2.2 Analysis of the SC DC-DC 2/3 Step Down Converter

2.2.1 Analyses of the Output Voltage

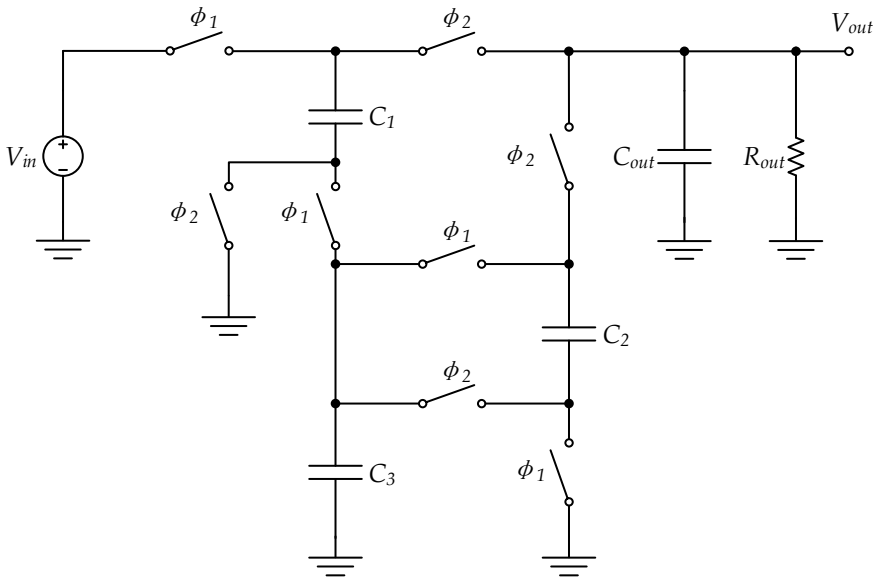
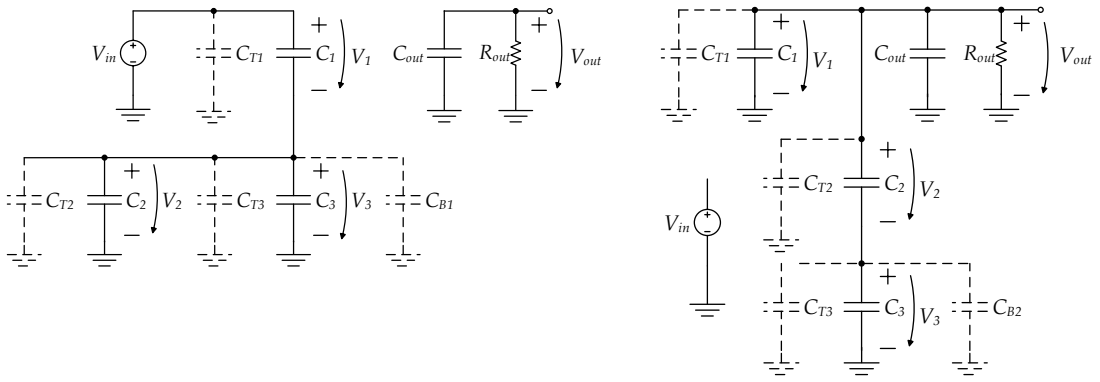


Figure 2.9: Simplified schematic of the 2/3 SC converter

Figure 2.9 shows the topology chosen to down-convert the input voltage (V_{in}) into two thirds smaller, $V_{out} = 2/3\, V_{in}$ [4]. The operation of this circuit is divided in two different phases: phase one (ϕ_1) in which the capacitor C_1 charges to the input voltage V_{in} in series with the parallel of C_2 and C_3; and phase two (ϕ_2) where the capacitor C_1 and the series of C_2 and C_3 are discharge.



(a) Phase 1: ϕ_1 (b) Phase 2: ϕ_2

Figure 2.10: Simplified schematic of the 2/3 SC DC-DC converter in the two phases

Figures 2.10(a) and 2.10(b) shows the schematics of the resulting circuit in each clock phase (ϕ_1 and ϕ_2). There are a total of five parasitic capacitances (C_{T1}, C_{B1}, C_{T2}, C_{B2}, and C_{T3}) associated to the three flying capacitors (C_1, C_2 and C_3). From ϕ_1 to ϕ_2 there is charge

conservation in two nodes: the one that connects the top plate of C_1, C_{T1}, C_2, C_{T2}, and C_{out}; and again the load resistor (R_{out}) in parallel with C_{out}; the second node connects the bottom plate of C_2 and the top plate of C_3, C_{B2} and C_{T3}. From ϕ_2 to ϕ_1 there is again charge conservation in two nodes: the one that connects the bottom plate of C_1 and the top plates of C_2, C_3, C_{T2}, C_{T3} and C_{B2}; the other connects the top plate of C_{out} with R_{out}. The same conditions in order to maintain valid (2.1) are kept in this converter.

Applying the same analyses as in the previous section, the equations that describe the conservation of charge can be seen in (2.19).

$$\begin{cases} Q_{C_1}^{\phi_1} + Q_{C_{T1}}^{\phi_1} + Q_{C_2}^{\phi_1} + Q_{C_{T2}}^{\phi_1} + Q_{C_{out}}^{\phi_1} = Q_{C_1}^{\phi_2} + Q_{C_{T1}}^{\phi_2} + Q_{C_2}^{\phi_2} + Q_{C_{T2}}^{\phi_2} + Q_{C_{out}}^{\phi_2} + \Delta Q_{R_{out}} \\ -Q_{C_2}^{\phi_1} + Q_{C_3}^{\phi_1} + Q_{C_{T3}}^{\phi_1} = -Q_{C_2}^{\phi_2} + Q_{C_{B2}}^{\phi_2} + Q_{C_3}^{\phi_2} + Q_{C_{T3}}^{\phi_2} \\ -Q_{C_1}^{\phi_2} + Q_{C_2}^{\phi_2} + Q_{C_{T2}}^{\phi_2} + Q_{C_3}^{\phi_2} + Q_{C_{T3}}^{\phi_2} = -Q_{C_1}^{\phi_1} + Q_{C_{B1}}^{\phi_1} + Q_{C_2}^{\phi_1} + Q_{C_{T2}}^{\phi_1} + Q_{C_3}^{\phi_1} + Q_{C_{T3}}^{\phi_1} \\ Q_{C_{out}}^{\phi_2} = Q_{C_{out}}^{\phi_1} + \Delta Q_{R_{out}} \end{cases} \tag{2.19}$$

Replacing $Q = V \cdot C$ in (2.19) results in the set of equations shown below.

$$\begin{cases} (V_{in} - V_2)\, C_1 + V_2\, (C_2 + C_{T2}) + V_{in}\, C_{T1} + V_{out}[n-1]\, C_{out} = \\ \qquad = \left(V_{out}\left[n - \frac{1}{2}\right] - V_3\right) C_2 + V_{out}\left[n - \frac{1}{2}\right]\left(C_1 + C_{out} + C_{T1} + C_{T2} + \frac{T}{2\,R_{out}}\right) \\ V_2(C_3 + C_{T3}) - V_2\, C_2 = \\ \qquad = \left(V_3 - V_{out}\left[n - \frac{1}{2}\right]\right) C_2 + V_3\,(C_3 + C_{B2} + C_{T3}) \\ -V_{out}\left[n - \frac{1}{2}\right] C_1 + \left(V_{out}\left[n - \frac{1}{2}\right] - V_3\right) C_2 + V_3\,(C_3 + C_{T3}) + V_{out}\left[n - \frac{1}{2}\right]\,(C_{T1} + C_{T2}) = \\ \qquad = (V_2 - V_{in})\, C_1 + V_2\,(C_2 + C_3 + C_{B1} + C_{T2} + C_{T3}) \\ V_{out}\left[n - \frac{1}{2}\right] C_{out} = V_{out}[n]\left(C_{out} + \frac{T}{2\,R_{out}}\right) \end{cases} \tag{2.20}$$

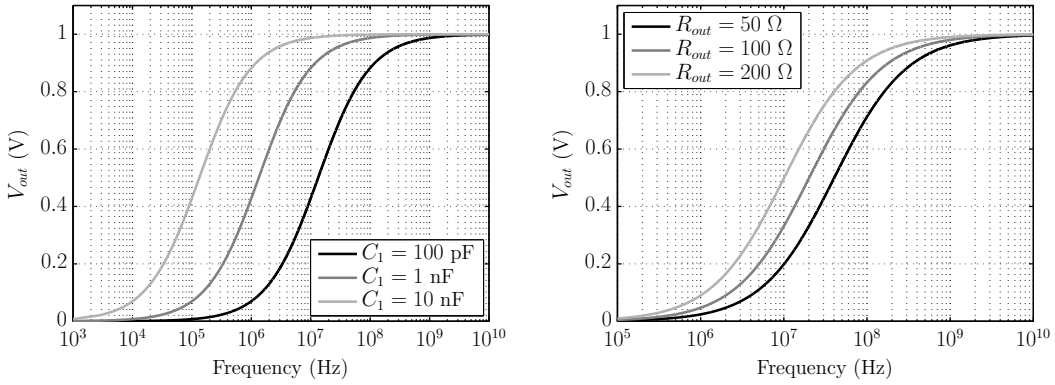
As in the preview section, (2.20) is solved in order to V_{out}, then considering only the steady state ($V_{out}[n] = V_{out}[n-1] = V_{out}$) and, finally, considering the approximation $C_{out} \to \infty$. Due to the large size of the resulting equation, only the equations without the effect of parasitics capacitances ($C_{T1} = C_{B1} = C_{T2} = C_{B2} = C_{T3} = 0$) and considering $C_1 = C_2 = C_3$ in order of T_{CLK} or F_{CLK} are showed (2.21) and (2.22).

$$V_{out} = \frac{2\,C_1\,R_{out}\,V_{in}}{3\,C_1\,R_{out} + 2\,T} \tag{2.21}$$

$$V_{out} = \frac{2\,C_1\,F\,R_{out}\,V_{in}}{3\,C_1\,F\,R_{out} + 2} \tag{2.22}$$

Figure 2.11(a) shows the plot of (2.22) where it can be seen the impact that C_1 has on V_{out} for a given value of frequency. As in the previous converter, the value of C_1 restricts the minimum value of the working frequency in order to have V_{out} equal to 1 V. Figure 2.11(b)

shows V_{out} for three different values of R_{out}. These values represent three different power output values ($R_{out} = 50\ \Omega \rightarrow P_{out} = 20$ mW, $R_{out} = 100\ \Omega \rightarrow P_{out} = 10$ mW, and $R_{out} = 200\ \Omega \rightarrow P_{out} = 5$ mW). Once again, an increase in R_{out} results in a increase of the minimum working frequency in order to maintain the output voltage constant.



(a) C_1 effect with $R_{out} = 100\ \Omega$ (b) R_{out} effect with $C_1 = 0.33$ nF

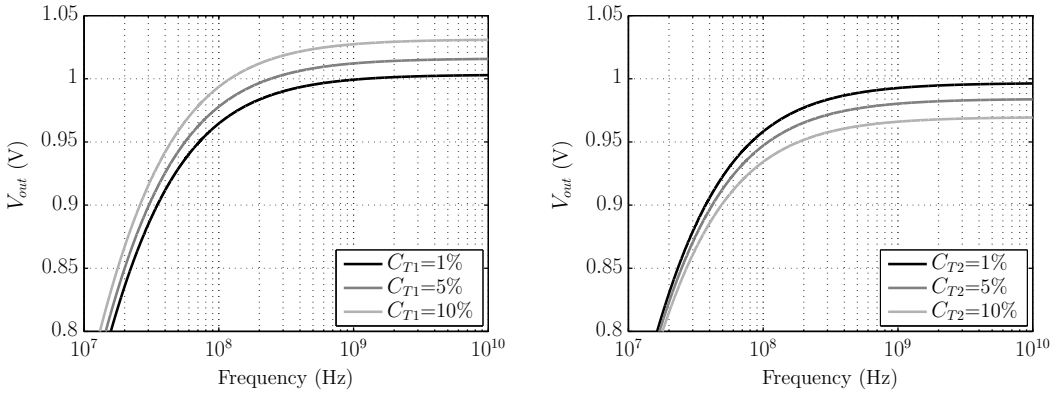
Figure 2.11: V_{out} as function of the clock frequency for $V_{in} = 1.5$ V

Figures 2.12 show the plot of V_{out} as function of the clock frequency for $V_{in} = 2$ V, $C_1 = C_2 = C_3 = 0.33$ nF and $R_{out} = 100\ \Omega$ for different values of C_{T1}, C_{B1}, C_{T2}, C_{B2} and C_{T3}. Figures 2.12(c) and 2.12(d) show that C_{T3} and C_{B1} have no effect in V_{out}. The first, C_{T3}, charges in parallel with C_3 and so does not affect V_{out}; the second, C_{B1}, charges to V_2 in ϕ_1 and in ϕ_2 discharges to ground. Figure 2.12(a) shows that as C_{T1} increases V_{out} increases its value. This is because C_{T1} charges to V_{in} in ϕ_1 which is at a higher potential than V_{out} in ϕ_2. Figures 2.12(b) and 2.12(e) show that as C_{T2} or C_{B2} increase V_{out} decreases. The first, C_{T2}, charges to V_2 in ϕ_1 which is at a lower potential than V_{out} in ϕ_2, and so drain charge from V_{out}; the second, C_{B2} drains charge from V_3 in ϕ_2 and discharges to ground in ϕ_2 and thefores affects the V_{out} value. Finally, Fig. 2.12(f), shows the effect if all parasitic capacitances were equal. This results in a decrease in V_{out}, although the decrease is very small, almost negligible.

From (2.22) it is possible to calculate the value of F_{CLK} as a function of V_{in}, V_{out}, C_1, and R_{out}. This results in expression (2.23).

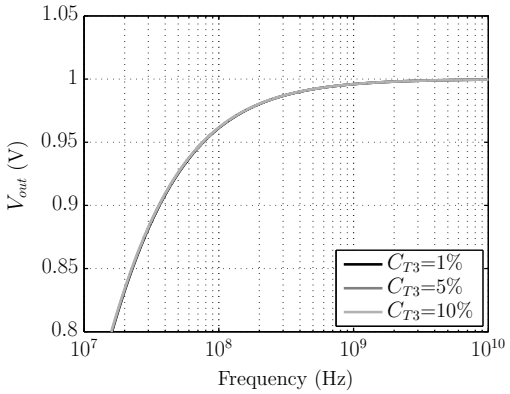
$$F_{CLK_{2/3}} = \frac{2\,V_{out}}{2\,C_1\,R_{out}\,V_{in} - 3\,C_1\,R_{out}\,V_{out}} \tag{2.23}$$

Figure 2.13 shows the plot of (2.23) for different values of the output resistance with $C_1 = C_2 = C_3 = 0.33$ nF and an output voltage of 1 V. With $V_{out} = 1$ V this plot shows that the optimum point of conversion would be at $V_{in} = 1.5$ V. The plot shows the asymptote in $V_{in} = 1.5$ V and as V_{in} increases, the clock frequency decreases in order to produce $V_{out} = 1$ V. Lastly, increasing the value of R_{out} results in a decrease in the range of frequency values.

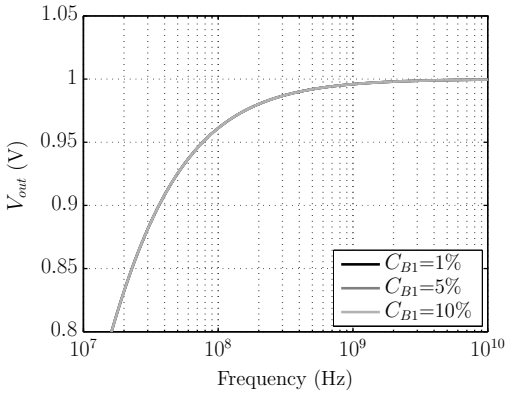


(a) C_{T1} effect with $C_{T2,3} = C_{B1,2} = 0$

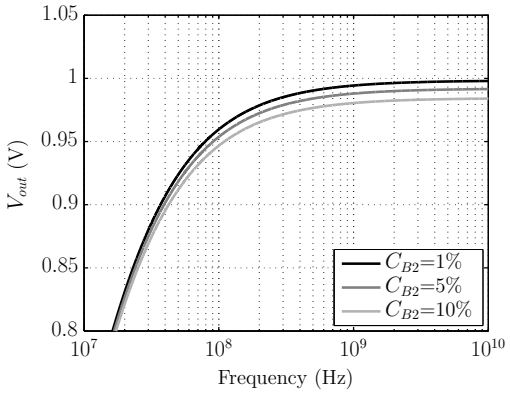
(b) C_{T2} effect with $C_{T1,3} = C_{B1,2} = 0$



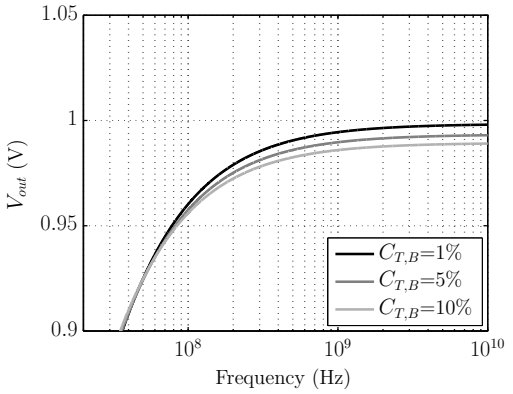
(c) C_{T3} effect with $C_{T1,2} = C_{B1,2} = 0$



(d) C_{B1} effect with $C_{T1,2,3} = C_{B2} = 0$



(e) C_{B2} effect with $C_{T1,2,3} = C_{B1} = 0$



(f) $C_{T1,2,3} = C_{B1,2}$ effect

Figure 2.12: V_{out} as function of the clock frequency for $V_{in} = 1.5$ V, $C_1 = C_2 = C_3 = 0.33$ nF and $R_{out} = 100\ \Omega$

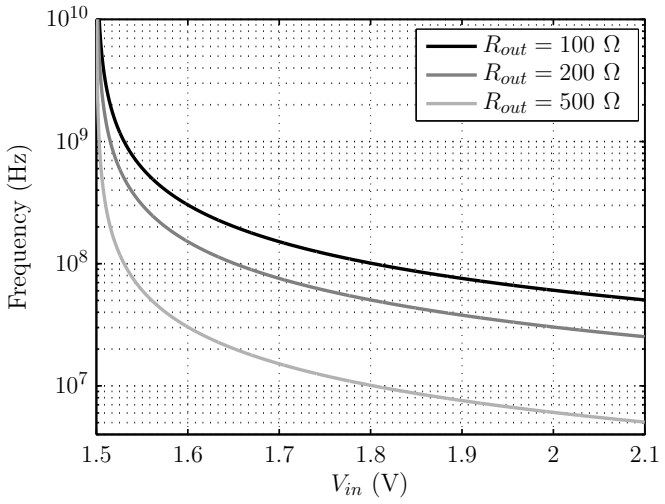
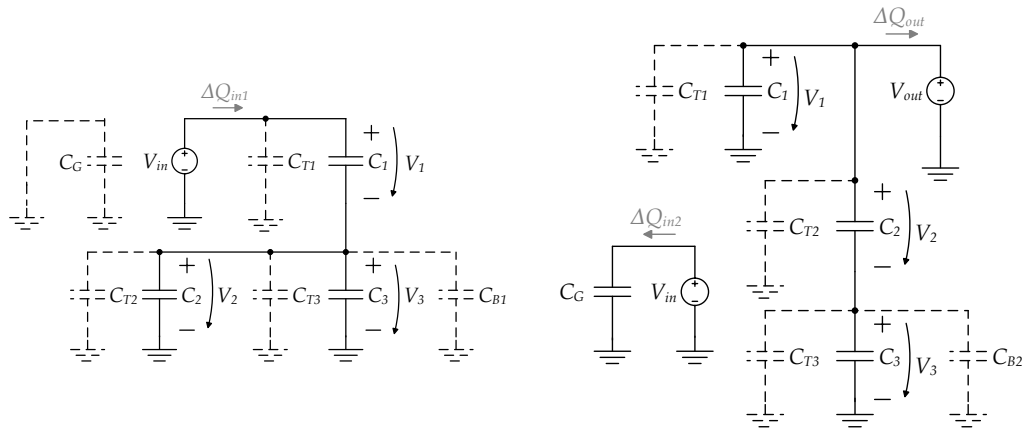


Figure 2.13: $F_{CLK_{2/3}}$ as function of V_{in} for $V_{out} = 1$ V and $C_1 = C_2 = C_3 = 0.33$ nF

2.2.2 Analysis of the Efficiency

The efficiency analyses, performed on the 1/2 converter, can be replicated for this converter as well. The schematics of the 2/3 converter circuit during phase ϕ_1 and ϕ_2 are shown in figure 2.14(a) and 2.14(b) respectively. Using conventional switched-capacitor circuit analysis techniques [7](Chapter 5) it is possible to determine the charge in each capacitor at the end of each clock phase. The resulting equations are shown in (2.24) and these allow to determine ΔQ_{in1}, ΔQ_{in2}, and ΔQ_{out}. Where ΔQ_{out} is the charge absorbed by the output power supply in ϕ_2.



(a) Phase 1: ϕ_1

(b) Phase 2: ϕ_2

Figure 2.14: Simplified schematic of the 2/3 SC DC-DC converter in each phase, with an ideal output voltage source

$$\begin{cases} (V_{in} - V_2)\, C_1 + V_2\, (C_2 + C_{T2}) + V_{in}\, C_{T1} = \\ \qquad\qquad = V_{out}\, (C_1 + C_{T1} + C_{T2}) + (V_{out} - V_3)\, C_2 + \Delta Q_{out} \\ 0 = V_{in}\, C_G + \Delta Q_{in2} \\ V_2\, (C_3 + C_{T3}) - V_2\, C_2 = (V_3 - V_{out}) C_2 + V_3\, (C_3 + C_{B2} + C_{T3}) \\ -V_{out}\, C_1 + (V_{out} - V_3)\, C_2 + V_3\, (C_3 + C_{T3}) + V_{out}\, C_{T2} = \\ \qquad\qquad = (V_2 - V_{in})\, C_1 + V_2\, (C_2 + C_3 + C_{B1} + C_{T2} + C_{T3}) \\ V_{out}\, (C_1 + C_{T1}) = (V_{in} - V_2)\, C_1 + V_{in} C_{T1} + \Delta Q_{in1} \end{cases} \tag{2.24}$$

Solving the previous equations in order to ΔQ_{in1}, ΔQ_{in2}, and ΔQ_{out}; then P_{in} and P_{out} can be determined by replacing the resulting equations in 2.25.

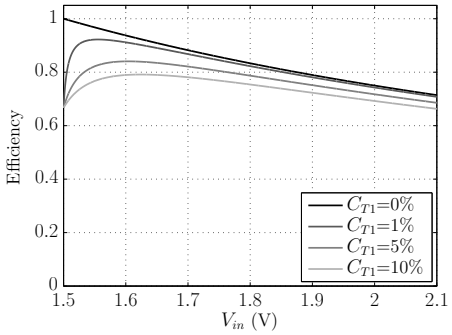
$$\begin{aligned} P_{in} &= I_{in}\, V_{in} = V_{in}\, (\Delta Q_{in1} + \Delta Q_{in2})\, F_{CLK} \\ P_{out} &= I_{out}\, V_{out} = V_{out}\, \Delta Q_{out}\, F_{CLK} \end{aligned} \tag{2.25}$$

The efficiency (η) with V_{out}=1 can be determined by

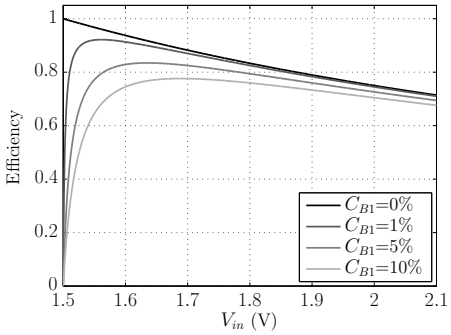
$$\eta_{2/3} = \frac{|P_{out}|}{|P_{in}|} \tag{2.26}$$

Due to the size of the resulting equation, only its plot is shown. Notice that $\eta_{2/3}$ does not depend on the clock frequency, but only on the ratio between C_1, C_2 and C_3 and the corresponding parasitic capacitances C_{T1}, C_{B1}, C_{T2}, C_{B2}, C_{T3} and C_G; for a given value of V_{in}. The 2/3 converter circuit was simulated in Spectre with ideal switches and capacitors for different input voltages between 1.5 to 2.1 V and with V_{out} fixed at 1 V. From these transient simulations its efficiency was calculated and compared to the efficiency calculated using (2.26) for different parasitic capacitance values.

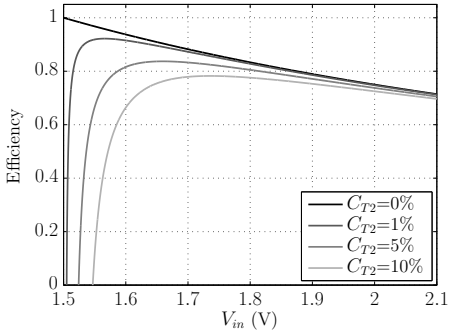
The previous analyses showed that the parasitic capacitances have small influence in the output voltage. However, in terms of efficiency figures 2.15 show that these have a strong impact in the efficiency. Figures 2.15(a), 2.15(b), 2.15(c) and 2.15(d) affect the efficiency almost in the same way - an increase in the capacitances result in a decrease in the efficiency. Figure 2.15(e) shows that C_{T3} has no impact. This is because this parasitic capacitance charge and discharge in parallel with C_3 and so no charge is lost. Figure 2.15(f) shows the effect of C_G where the decrease in the efficiency is more pronounced than one caused if all parasitic capacitances of the flying capacitors were equal (Fig. 2.15(g)). Lastly, figure 2.15(h) shows the plot for $C_{T,B} = C_G$. The behaviour is the same as in the previous plots, although the decrease in η is more noticeable. The simulation results (markers) prove that (2.26) accurately describes the behaviour of the converter efficiency and validates the theoretical analysis.



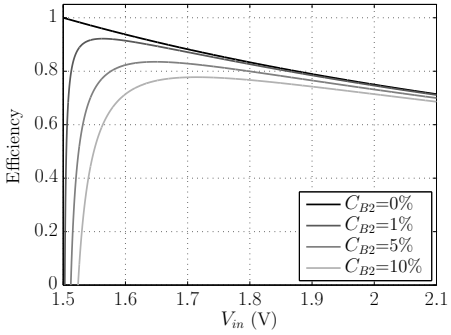
(a) C_{T1} effect with $C_{T2,3} = C_{B1,2} = C_G = 0$



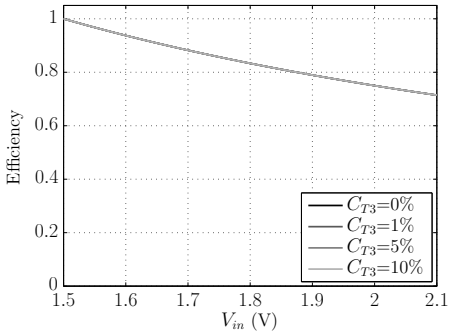
(b) C_{B1} effect with $C_{T1,2,3} = C_{B2} = C_G = 0$



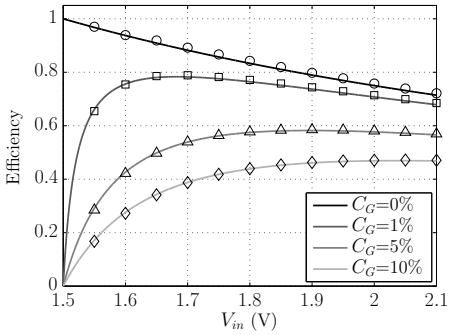
(c) C_{T2} effect with $C_{T1,3} = C_{B1,2} = C_G = 0$



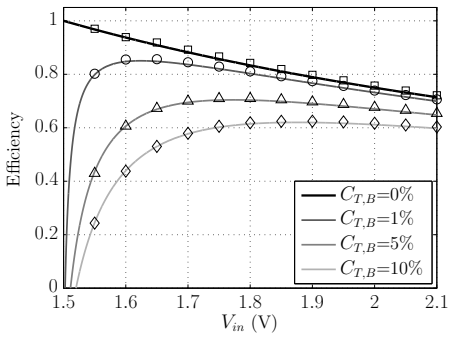
(d) C_{B2} effect with $C_{T1,2,3} = C_{B1} = C_G = 0$



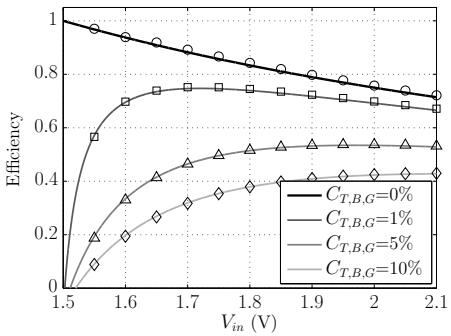
(e) C_{T3} effect with $C_{T1,2} = C_{B1,2} = C_G = 0$



(f) C_G effect with $C_{T1,2,3} = C_{B1,2} = 0$



(g) $C_{T,B}$ effect with $C_G = 0$



(h) $C_{T,B,G}$ effect

Figure 2.15: η as function of the clock frequency for $V_{in} = 1.5$ V and $C_1 = C_2 = C_3 = 0.33$ nF

2.3 Analysis of the SC DC-DC 1/1 Converter

2.3.1 Analyses of the Output Voltage

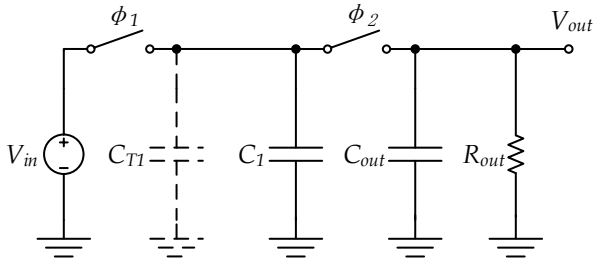
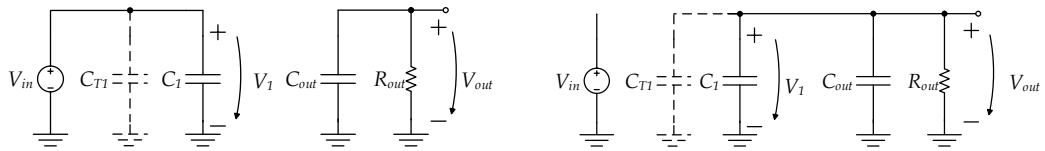


Figure 2.16: Simplified schematic of the 1/1 SC DC-DC converter

Unlike the two previous converters, this converter, show in figure 2.16, does not step-down or step-up the input voltage. Its function is simpler - transfer the input voltage (V_{in}) into to the output voltage, $V_{out} = V_{in}$ [4]. In phase one (ϕ_1) the capacitor C_1 charges to the input voltage (V_{in}) and in phase two (ϕ_2) the capacitor C_1 discharge to V_{out}.



(a) Phase 1: ϕ_1 (b) Phase 2: ϕ_2

Figure 2.17: Simplified schematic of the 1/1 SC DC-DC converter in the two phases

Figures 2.17(a) and 2.17(b) shows the schematics of the resulting circuit in each clock phase (ϕ_1 and ϕ_2). There is only one parasitic capacitance to have into account - C_{T1}. From ϕ_1 to ϕ_2 there is charge conservation in the node that connects C_1, C_{T1}, and C_{out} top plates and the load resistor (R_{out}). From ϕ_2 to ϕ_1 there is charge conservation in the node that connects C_{out} top plate and R_{out}. As in the previous converters, the assumptions that validate the use of (2.1) are kept. Applying the same analyse as in the previous sections, the resulting system of charge equations can be seen in (2.27).

$$\begin{cases} Q_{C_1}^{\phi_1} + Q_{C_{T1}}^{\phi_1} + Q_{C_{out}}^{\phi_1} = Q_{C_1}^{\phi_2} + Q_{C_{T1}}^{\phi_2} + Q_{C_{out}}^{\phi_2} + \Delta Q_{R_{out}} \\ Q_{C_{out}}^{\phi_2} = Q_{C_{out}}^{\phi_1} + \Delta Q_{R_{out}} \end{cases} \tag{2.27}$$

Replacing $Q = V \cdot C$ in (2.27) results in the set of equations shown below.

$$\begin{cases} V_{in}\,(C_1 + C_{T1}) + V_{out}[n-1]\,C_{out} = V_{out}\left[n - \dfrac{1}{2}\right]\left(C_1 + C_{T1} + C_{out} + \dfrac{T}{2\,R_{out}}\right) \\ V_{out}\left[n - \dfrac{1}{2}\right]\,C_{out} = V_{out}[n]\left(C_{out} + \dfrac{T}{2\,R_{out}}\right) \end{cases} \tag{2.28}$$

As in the previous sections, solving (2.28) in order to V_{out}, then considering only the steady state ($V_{out}[n] = V_{out}[n-1] = V_{out}$) and, finally, considering the approximation $C_{out} \to \infty$; results in

$$V_{out} = \frac{R_{out}\,V_{in}\,(C_1 + C_{T1})}{C_1\,R_{out} + C_{T1}\,R_{out} + T} \tag{2.29}$$

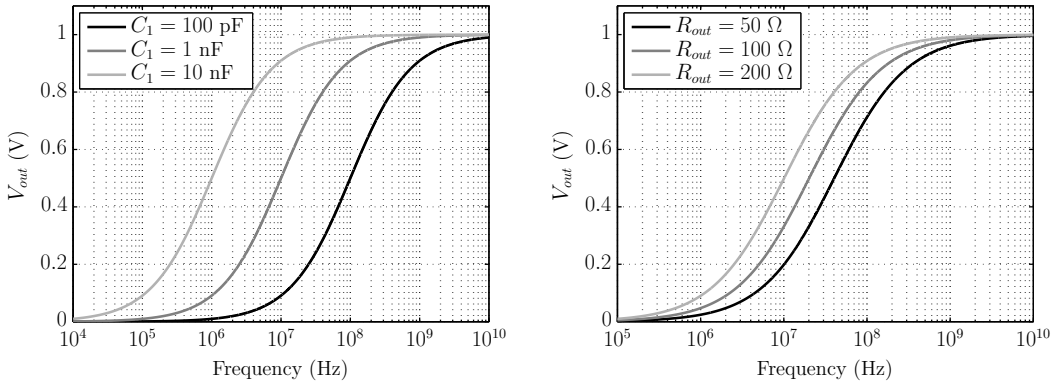
or as a function of the clock frequency ($F = 1/T$)

$$V_{out} = \frac{F\,R_{out}\,V_{in}\,(C_1 + C_{T1})}{F\,R_{out}(C_1 + C_{T1}) + 1} \tag{2.30}$$

For simplicity it is possible to calculate V_{out} considering the ideal capacitor ($C_{T1} = 0$) in order of T or F.

$$V_{out} = \frac{C1\,R_{out}\,V_{in}}{C_1\,R_{out} + T} \tag{2.31}$$

$$V_{out} = \frac{C_1\,F\,R_{out}\,V_{in}}{C_1\,F\,R_{out} + 1} \tag{2.32}$$



(a) C_1 effect with $R_{out} = 100\,\Omega$ (b) R_{out} effect with $C_1 = 1$ nF

Figure 2.18: V_{out} as function of the clock frequency for $V_{in} = 1$ V

Figure 2.18(a) shows the plot of (2.32) where it can be seen the impact that C_1 has on V_{out} for a given value of frequency. As in the previous converter, the value of C_1 restricts the minimum value of the working frequency in order to have V_{out} equal to 1 V. Figure 2.18(b) shows V_{out} for three different values of R_{out}. These values represent three different power output values ($R_{out} = 50\ \Omega \to P_{out} = 20$ mW, $R_{out} = 100\ \Omega \to P_{out} = 10$ mW, and $R_{out} = 200\ \Omega \to P_{out} = 5$ mW). Once again, an increase in R_{out} results in an increase on the minimum working frequency in order to maintain the output voltage constant..

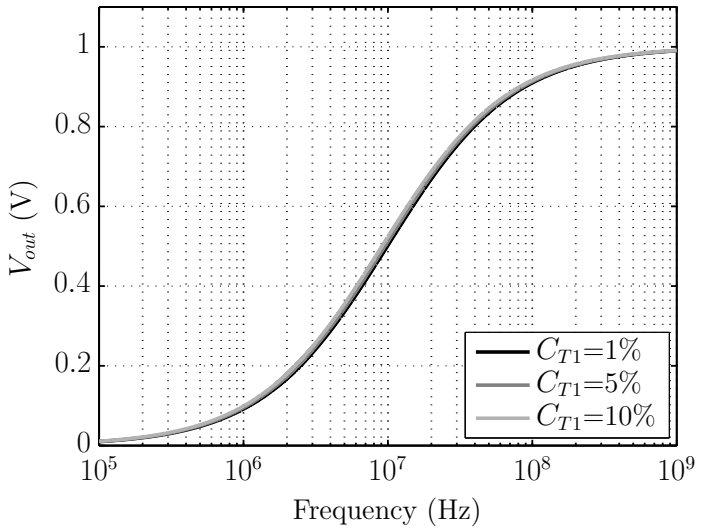


Figure 2.19: V_{out} as function of the clock frequency for $V_{in} = 1$ V, $C_1 = 1$ nF and $R_{out} = 100\ \Omega$

Figures 2.19 shows the plot of V_{out} as function of the clock frequency for $V_{in} = 1$ V, $C_1 = 1$ nF and $R_{out} = 100\ \Omega$ for different values of C_{T1}. The plot shows that C_{T1} has no effect in V_{out}, because this capacitance is parallel with C_1.

Solving (2.30) in order to the frequency results in

$$F_{CLK_{1/1}} = \frac{V_{out}}{R_{out}\,(C_1 + C_{T1})\,(V_{in} - V_{out})} \tag{2.33}$$

and considering an ideal capacitor results in

$$F_{CLK_{1/1}} = \frac{V_{out}}{C_1\,R_{out}\,(V_{in} - V_{out})} \tag{2.34}$$

Figure 2.20 shows the plot of (2.34) for different values of the output resistance with $C_1 = 1$ nF and $V_{out} = 1$ V. As expected, the asymptote is located in $V_{in} = 1V$ and decreases rapidly from this value. Again, increasing R_{out} results in a decrease in the range of frequency values.

2.3.2 Analysis of the Efficiency

The schematics of the 1/1 converter circuit during phase ϕ_1 and ϕ_2 are shown in figure 2.21(a) and 2.21(b) respectively. Using conventional switched-capacitor circuit analysis techniques [7](Chapter 5) it is possible to determine the charge in each capacitor at the end of each clock phase. The resulting equations are shown in (2.35) and these allow to determine ΔQ_{in1}, ΔQ_{in2}, and ΔQ_{out}. Where ΔQ_{out} is the charge absorbed by the output power supply in ϕ_2.

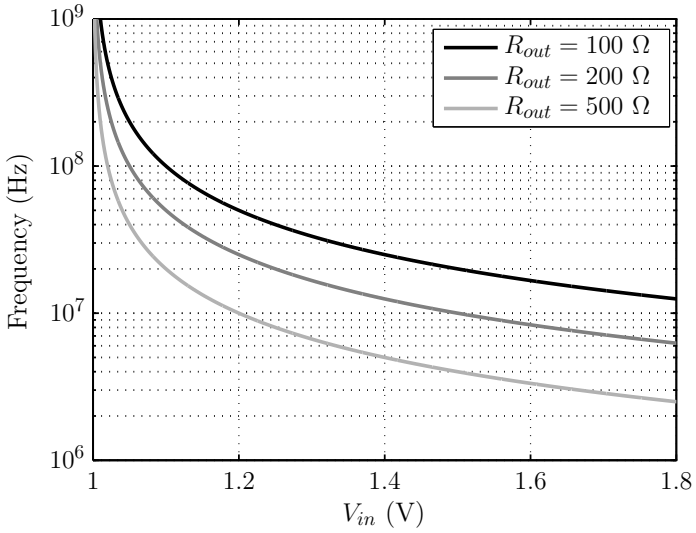
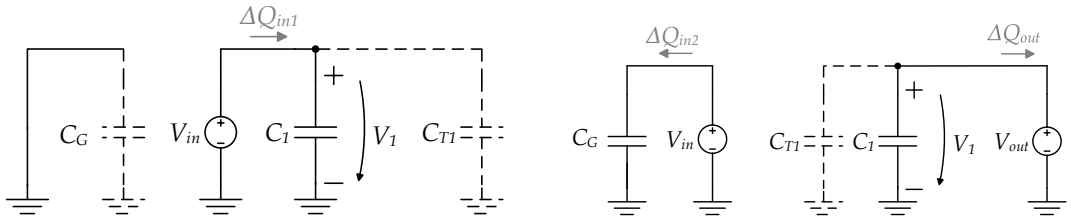


Figure 2.20: $F_{CLK_{1/1}}$ as function of V_{in} for $V_{out} = 1$ V and $C_1 = 1$ nF



(a) Phase 1: ϕ_1 (b) Phase 2: ϕ_2

Figure 2.21: Simplified schematic of the 1/1 SC DC-DC converter in each phase, with an ideal output voltage source

$$\begin{cases} V_{in}\,(C_1 + C_{T1}) = V_{out}\,(C_1 + C_{T1}) + \Delta Q_{out} \\ 0 = C_G\,V_{in} + \Delta Q_{in2} \\ V_{out}\,(C_1 + C_{T1}) = V_{in}\,(C_1 + C_{T1}) + \Delta Q_{in1} \end{cases} \tag{2.35}$$

Solving the previous equations in order to ΔQ_{in1}, ΔQ_{in2} and ΔQ_{out}; results in

$$\begin{cases} \Delta Q_{in1} = -(C_1 + C_{T1})\,(V_{in} - V_{out}) \\ \Delta Q_{in2} = -C_G\,V_{in} \\ \Delta Q_{out} = (C_1 + C_{T1})\,(V_{in} - V_{out}) \end{cases} \tag{2.36}$$

The input (P_{in}) and output (P_{out}) power are calculated using ΔQ_{in1}, ΔQ_{in2}, ΔQ_{out}, V_{in} and V_{out}. These are given by

$$\begin{cases} P_{in} = I_{in}\,V_{in} = V_{in}\ (\Delta Q_{in1} + \Delta Q_{in2})\ F_{CLK} \\ P_{out} = I_{out}\,V_{out} = V_{out}\,\Delta Q_{out}\,F_{CLK} \end{cases} \tag{2.37}$$

$$\begin{cases} P_{in} = \dfrac{V_{in}\left(V_{out}\left(C_1 + C_{T1}\right) - V_{in}\left(C_1 + C_G + C_{T1}\right)\right)}{T} \\ P_{out} = \dfrac{V_{out}\left(C_1 + C_{T1}\right)\left(V_{in} - V_{out}\right)}{T} \end{cases} \tag{2.38}$$

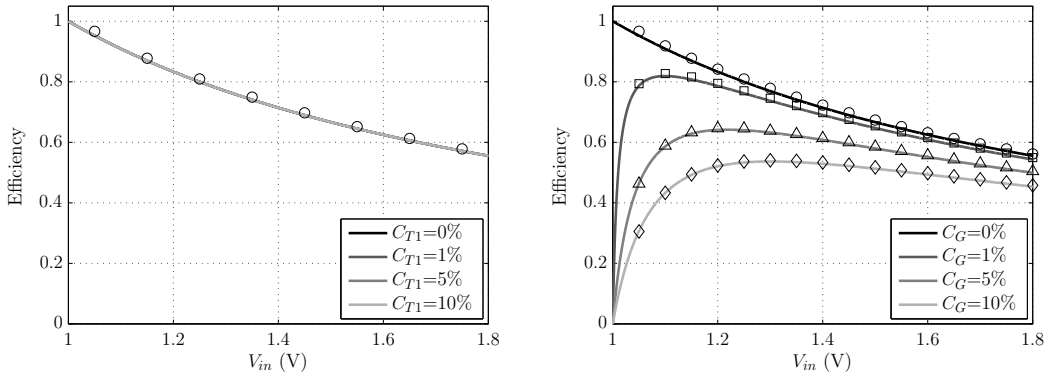
The efficiency (η) defined by the ratio between P_{out} and P_{in} is given by

$$\eta_{1/1} = \frac{|P_{out}|}{|P_{in}|} = \frac{V_{out}\left(C_1 + C_{T1}\right)\left(V_{in} - V_{out}\right)}{V_{in}\left(V_{in}\left(C_1 + C_G + C_{T1}\right) - V_{out}\left(C_1 + C_{T1}\right)\right)} \tag{2.39}$$

solving for $V_{out} = 1$ V results in

$$\eta_{1/1} = \frac{\left(V_{in} - 1\right)\left(C_1 + C_{T1}\right)}{V_{in}^2\left(C_1 + C_G + C_{T1}\right) - V_{in}\left(C_1 + C_{T1}\right)} \tag{2.40}$$

Again $\eta_{1/1}$ does not depend on the clock frequency, but only on the ratio between C_1, C_{T1}, and C_G for a given value of V_{in}. The 1/1 converter circuit was simulated in Spectre with ideal switches and capacitors for different input voltages between 1.1 to 1.8 V and with V_{out} fixed at 1 V. From these transient simulations its efficiency was calculated and compared to the efficiency calculated using (2.40) for different parasitic capacitance values.



(a) C_{T1} effect $C_G = 0$ (b) C_G effect $C_{T1} = 0$

Figure 2.22: η as function of the clock frequency for $V_{out} = 1$ V and $C_1 = 1$ nF

Figures 2.22 show the plots of (2.40) with $V_{out} = 1$ and $C_1 = 1$ nF for different values of C_{T1} and C_G. Figure 2.22(a) shows the effect of C_{T1} with $C_G = 0$ where it can be seen that this does not effect the efficiency. Again, this is due to the charge and discharge of the capacitance in parallel with C_1, resulting in a increase of the C_1 value. Figure 2.22(b) shows the effect of C_G. Increasing its value results in a strong decrease of the maximum achievable efficiency. The simulation results (markers) prove that (2.40) accurately describes the behaviour of the converter efficiency and validates the theoretical analysis.

2.4 Analysis of the SC DC-DC 3/2 Step up Converter

2.4.1 Analyses of the Output Voltage

Figure 2.23 shows the topology of the circuit chosen to up convert the input voltage (V_{in}), ideally, into three and half times greater, $V_{out} = 3/2\, V_{in}$ [4]. Notice that this topology is almost equal to the 2/3 converter shown in Fig. 2.9. The difference being that the input and output voltage are exchanged. The operation of the circuit is divided in two different phases: phase one (ϕ_1), where the capacitors C_1 and the parallel of C_2 and C_3 are now connected in series with C_{out} and R_{out}; and phase two (ϕ_2), in which the capacitors C_1 and the series of C_2 and C_3 are connected in parallel with the input voltage V_{in}.

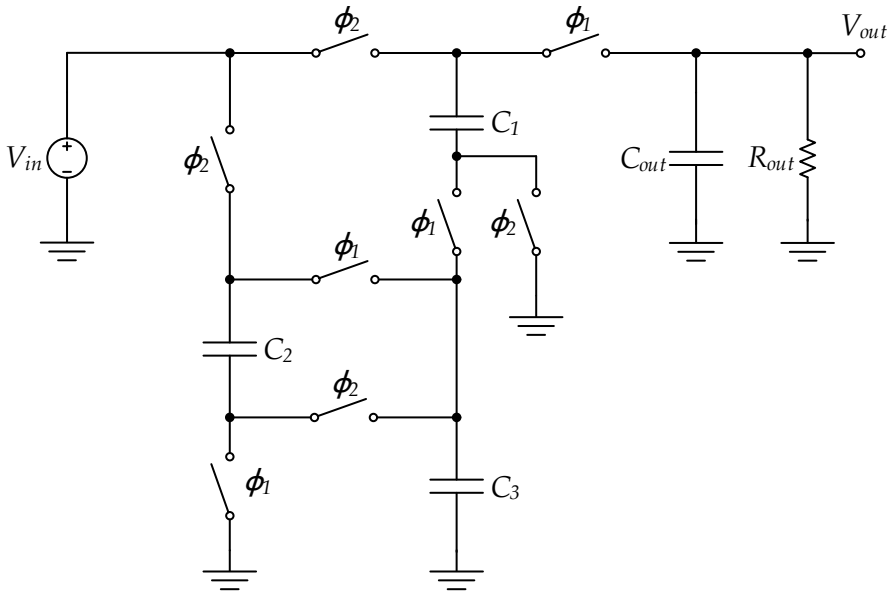
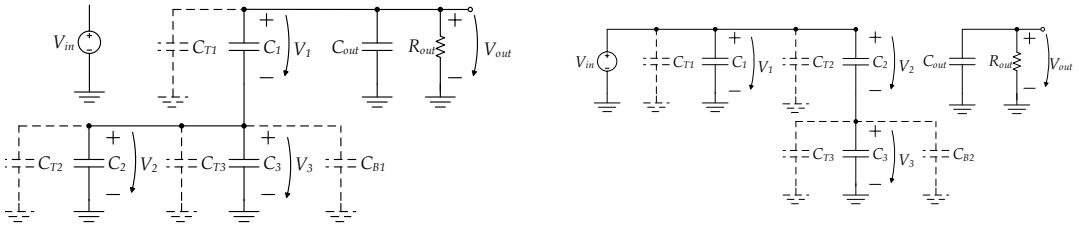


Figure 2.23: Simplified schematic of the 3/2 SC DC-DC converter

Figures 2.24(a) and 2.24(b) shows the schematics of the resulting circuit in each clock phase (ϕ_1 and ϕ_2). There are five parasitic capacitances (C_{T1}, C_{B1}, C_{T2}, C_{B2} and C_{T3}) from the three flying capacitors (C_1, C_2 and C_3). At the beginning of phase ϕ_1, figure 2.3(a), there is charge conservation in two nodes - the one that connects the bottom plate of C_2 with



(a) Phase 1: ϕ_1 (b) Phase 2: ϕ_2

Figure 2.24: Simplified schematic of the 1/2 SC converter in the two phases

the top plates of C_3, C_{B2} and C_{T3}; and the one that connects C_{out} top plate with R_{out}. In ϕ_2, there is also charge conservation in two nodes - the node that connects the top plates of C_1, C_{T1} and C_{out} with R_{out}; and the one that connects C_1 bottom plate with the top plates of C_2, C_3, C_{B1}, C_{T2} and C_{T3}. As in the previous converters, the assumptions that validate the use of (2.1) are kept. Using the conventional switched-capacitor circuit analysis techniques [7] (Chapter 5) the resulting system of charge equations can be seen in (2.41).

$$\begin{cases} -Q_{C_2}^{\phi_1} + Q_{C_3}^{\phi_1} + Q_{C_{T3}}^{\phi_1} = -Q_{C_2}^{\phi_2} + Q_{C_{B2}}^{\phi_2} + Q_{C_3}^{\phi_2} + Q_{C_{T3}}^{\phi_2} \\ Q_{C_{out}}^{\phi_1} = Q_{C_{out}}^{\phi_2} + \Delta Q_{R_{out}} \\ -Q_{C_1}^{\phi_2} + Q_{C_2}^{\phi_2} + Q_{C_{T2}}^{\phi_2} + Q_{C_3}^{\phi_2} + Q_{C_{T3}}^{\phi_2} = \\ \qquad\qquad = -Q_{C_1}^{\phi_1} + Q_{C_{B1}}^{\phi_1} + Q_{C_2}^{\phi_1} + Q_{C_{T2}}^{\phi_1} + Q_{C_3}^{\phi_1} + Q_{C_{T3}}^{\phi_1} \\ Q_{C_1}^{\phi_2} + Q_{C_{T1}}^{\phi_2} + Q_{C_{out}}^{\phi_2} = Q_{C_1}^{\phi_1} + Q_{C_{T1}}^{\phi_1} + Q_{C_{out}}^{\phi_1} + \Delta Q_{R_{out}} \end{cases} \tag{2.41}$$

Replacing $Q = V \cdot C$ in (2.41) results in the set of equations shown below.

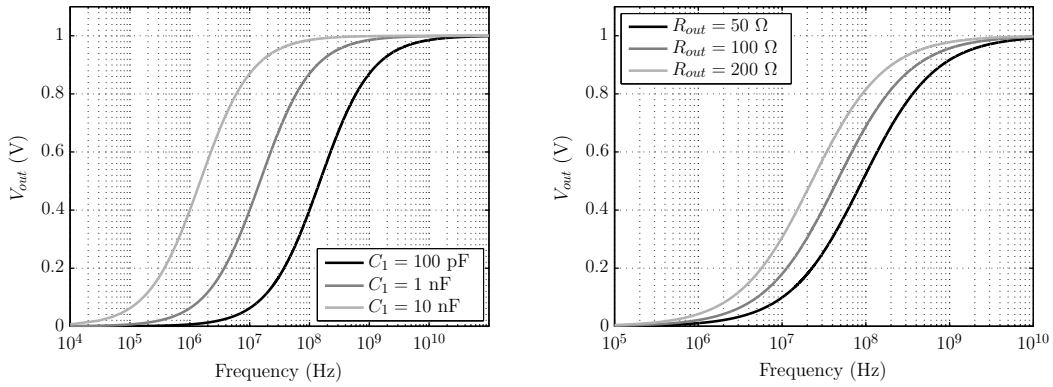
$$\begin{cases} -V_2\,C_2 + V_2\,(C_3 + C_{T3}) = (V_3 - V_{in})\,C_2 + V_3\,(C_3 + C_{B2} + C_{T3}) \\ V_{out}[n-1]\,C_{out} = V_{out}\left[n - \frac{1}{2}\right]\left(C_{out} + \frac{T}{2\,R_{out}}\right) \\ (-V_{in})\,C_1 + (V_{in} - V_3)\,C_2 + V_3\,(C_3 + C_{T3}) + V_{in}\,C_{T2} = \\ \qquad\qquad = (V_2 - V_{out}[n])\,C_1 + V_2\,(C_2 + C_3 + C_{B1} + C_{T2} + C_{T3}) \\ V_{in}\,(C_1 + C_{T1}) + V_{out}\left[n - \frac{1}{2}\right]\,C_{out} = (V_{out}[n] - V_2)\,C_1 + V_{out}[n]\left(C_{out} + C_{T1} + \frac{T}{2\,R_{out}}\right) \end{cases} \tag{2.42}$$

As in the previous sections, (2.42) are solved in order to V_{out}, then considering only the steady state ($V_{out}[n] = V_{out}[n-1] = V_{out}$) and, finally, considering the approximation $C_{out} \to \infty$. Due to the large size of the resulting equation, only the equations without the effect of parasitics capacitances ($C_{T1} = C_{B1} = C_{T2} = C_{B2} = C_{T3} = 0$) and considering $C_1 = C_2 = C_3$ in order of T_{CLK} or F_{CLK} are showed.

$$V_{out} = \frac{3\,C_1\,R_{out}\,T\,V_{in}}{2\,C_1\,R_{out}\,T + 3} \tag{2.43}$$

$$V_{out} = \frac{3\,C_1\,R_{out}\,V_{in}}{2\,C_1\,R_{out} + 3\,F} \tag{2.44}$$

Figure 2.25(a) shows the plot of (2.44) where it can be seen the impact that C_1 has on V_{out} for a given value of frequency. As in the previous converter, the value of C_1 restricts the minimum value of the working frequency in order to have V_{out} equal to 1 V. Figure 2.25(b) shows V_{out} for three different values of R_{out}. These values represent three different power output values ($R_{out} = 50\ \Omega \to P_{out} = 20$ mW, $R_{out} = 100\ \Omega \to P_{out} = 10$ mW, and $R_{out} = 200\ \Omega \to P_{out} = 5$ mW). Once again, an increase in R_{out} results in a increase of the minimum working frequency in order to maintain the output voltage constant..



(a) C_1 effect with $R_{out} = 100\ \Omega$ (b) R_{out} effect with $C_1 = 0.33$ nF

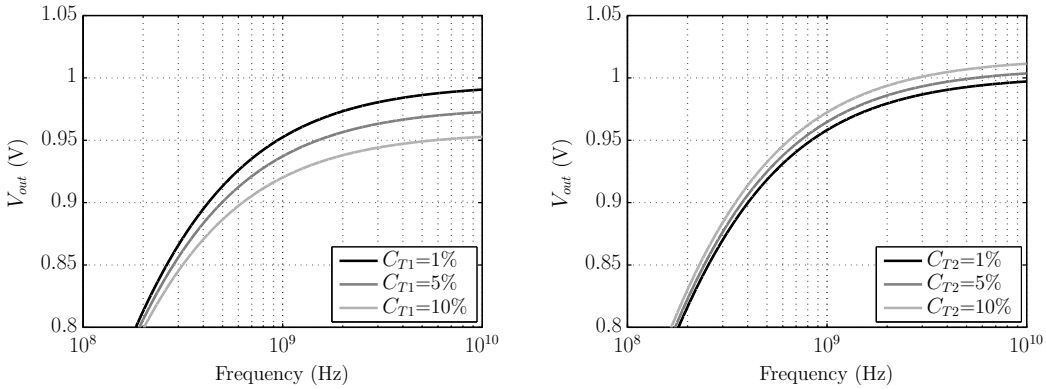
Figure 2.25: V_{out} as function of the clock frequency for $V_{in} = 0.67$ V

Figures 2.26 show the plot of V_{out} as function of the clock frequency for $V_{in} = 0.67$ V, $C_1 = C_2 = C_3 = 0.33$ nF and $R_{out} = 100\ \Omega$ for different values of C_{T1}, C_{B1}, C_{T2}, C_{B2} and C_{T3}. Figures 2.26(c) and 2.26(e) show that C_{T3} and C_{B2} have no effect in V_{out}. The first capacitor charges to V_2 in ϕ_1 and discharges to V_3 in ϕ_2 and therefore, it has the same behaviour of C_3; the second, C_{B2}, charges to V_3 in ϕ_2 and discharges to ground in ϕ_1 without affecting V_{out}. Figure 2.26(b) shows that as C_{T2} increases V_{out} increases its value. This is because C_{T2} charges to V_{in} in ϕ_2 and add this charge to V_2 in phase ϕ_1. Figures 2.26(a) and 2.12(d) show that as C_{T1} or C_{B1} increase V_{out} decreases. The first is because the V_{in} node is at a lower potential than the V_{out} node and therefore, C_{T1} drain charge from V_{out} in ϕ_1; the second capacitor is due to this capacitance charge to V_2 in ϕ_1 and in ϕ_2 discharge do ground. Finally, Figure 2.26(f) shows the effect if all parasitic capacitances were equal. This results in a decrease in V_{out}.

By solving (2.44) in order to the frequency, it is possible to calculate the required value of the frequency for the converter to produce an output voltage of 1 V for a given V_{in}, C_1 and R_{out}. The resulting equation can be seen in (2.45).

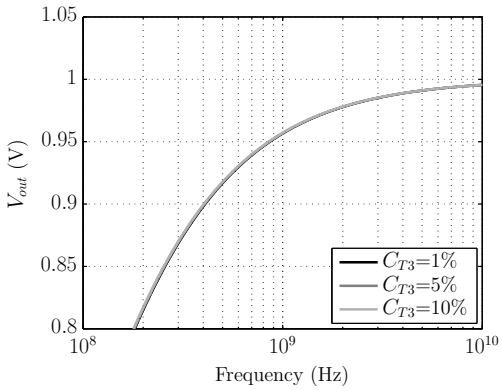
$$F_{CLK_{3/2}} = \frac{3\,V_{out}}{3\,C_1\,R_{out}\,V_{in} - 2\,C_1\,R_{out}\,V_{out}} \tag{2.45}$$

Figure 2.27 shows the plot of (2.45) for different values of the output resistance with $C_1 = C_2 = C_3 = 0.33$ nF and an output voltage of 1 V. For $V_{out} = 1$ V the optimum input voltage would be at $V_{in} = 0.67$ V. The plot shows the asymptote in $V_{in} = 0.67$ V and as V_{in} increases, the clock frequency decreases in order to produce the same V_{out} of 1 V. Lastly, increasing the value of R_{out} results in a decrease in the range of frequency values.

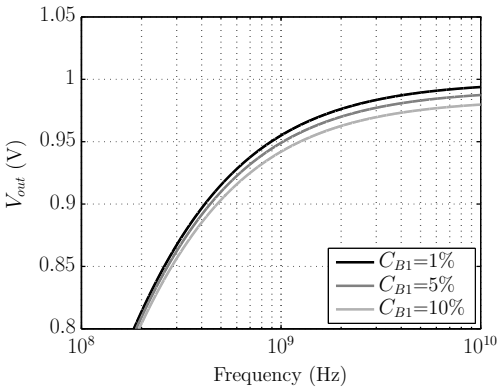


(a) C_{T1} effect with $C_{T2,3} = C_{B1,2} = 0$

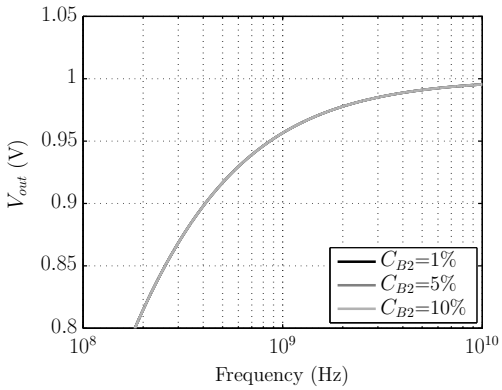
(b) C_{T2} effect with $C_{T1,3} = C_{B1,2} = 0$



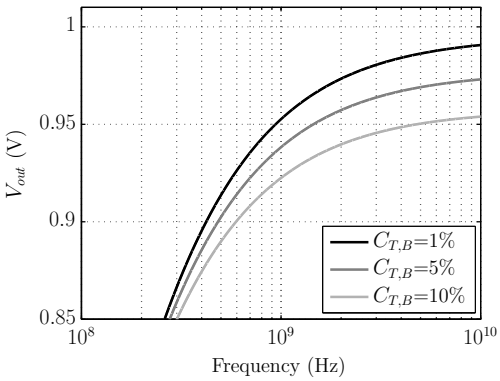
(c) C_{T3} effect with $C_{T1,2} = C_{B1,2} = 0$



(d) C_{B1} effect with $C_{T1,2,3} = C_{B2} = 0$



(e) C_{B2} effect with $C_{T1,2,3} = C_{B1} = 0$



(f) $C_{T1,2,3} = C_{B1,2}$

Figure 2.26: V_{out} as function of the clock frequency for $V_{in} = 0.67$ V, $C_1 = C_2 = C_3 = 0.33$ nF and $R_{out} = 100\ \Omega$

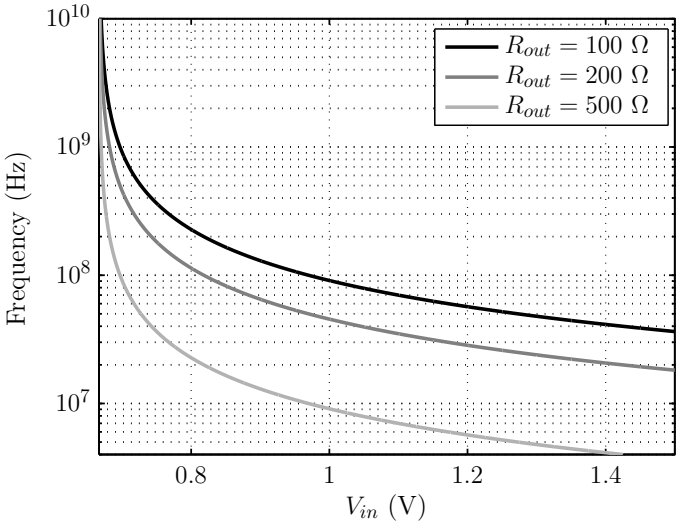
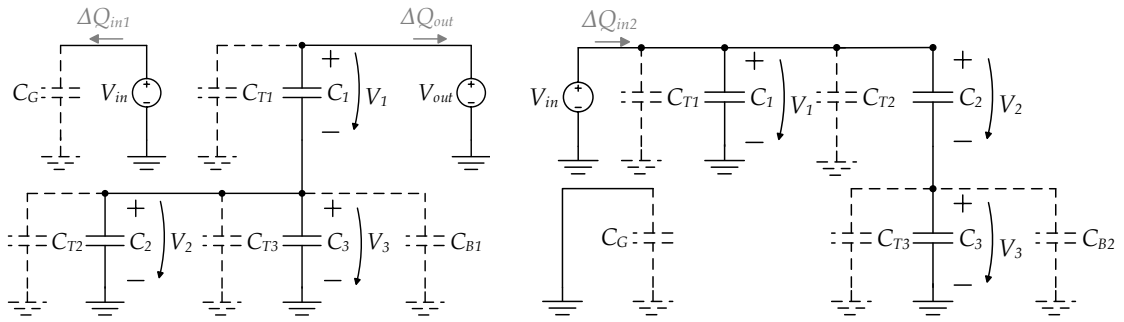


Figure 2.27: $F_{CLK_{3/2}}$ as function of V_{in} for $V_{out} = 1$ V and $C_1 = C_2 = C_3 = 0.33$ nF

2.4.2 Analysis of the Efficiency

As in the previous efficiency analysis, it is assumed that the clock frequency is adjusted in order to have the desired output voltage (e.g. V_{out}=1 V) and that output decoupling capacitor C_{out} is large enough so that the output voltage value is constant. In this case, figures 2.28(a) and 2.28(b) show the schematics of the 3/2 converter circuit during phase ϕ_1 and ϕ_2, respectively. In each clock cycle, the switches drain a charge (ΔQ_{in1}) from V_{in} through the clock buffers. Using conventional switched-capacitor circuit analysis techniques [7](Chapter 5) it is possible to determine the charge in each capacitor at the end of each clock phase. The resulting equations are shown in (2.46) and these allow to determine ΔQ_{in1}, ΔQ_{in2} and ΔQ_{out}. Where ΔQ_{out} is the charge absorbed by the output power supply.



(a) Phase 1: ϕ_1 (b) Phase 2: ϕ_2

Figure 2.28: Simplified schematic of the 3/2 SC DC-DC converter in each phase, with an ideal output voltage source

$$\begin{cases} (V_{out} - V_2)\, C_1 + V_2\, (C_2 + C_{T2}) + V_{out}\, C_{T1} = \\ \qquad\qquad = V_{in}\, (C_1 + C_{T1} + C_{T2}) + (V_{in} - V_3)\, C_2 + \Delta Q_{in1} \\ V_2\, (-C_2 + C_3 + C_{T3}) = (V_3 - V_{in})\, C_2 + V_3\, (C_3 + C_{B2} + C_{T3}) \\ V_{in}\, (C_1 + C_{T1}) = C_1\, (V_{out} - V_2) + C_{T1}\, V_{out} + \Delta Q_{out} \\ V_{in}\, (-C_1 + C_{T2}) + (V_{in} - V_3)\, C_2 + V_3\, (C_3 + C_{T3}) = \\ \qquad\qquad = (V_2 - V_{out})\, C_1 + V_2\, (C_2 + C_3 + C_{B1} + C_{T2} + C_{T3}) \\ 0 = C_G\, V_{in} + \Delta Q_{in2} \end{cases} \tag{2.46}$$

Solving the previous equations in order to ΔQ_{in1}, ΔQ_{in2}, and ΔQ_{out}; then P_{in} and P_{out} can be determined by replacing the resulting equations in 2.47.

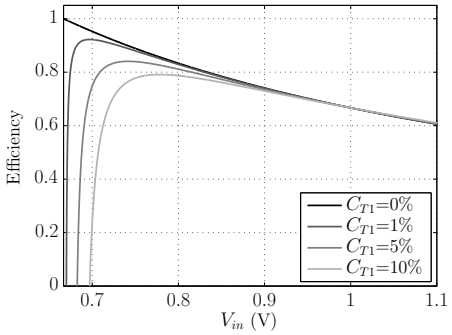
$$\begin{aligned} P_{in} &= I_{in}\, V_{in} = V_{in}\ (\Delta Q_{in1} + \Delta Q_{in2})\ F_{CLK} \\ P_{out} &= I_{out}\, V_{out} = V_{out}\, (\Delta Q_{out})\, F_{CLK} \end{aligned} \tag{2.47}$$

The efficiency (η) with V_{out}=1 can be determined by

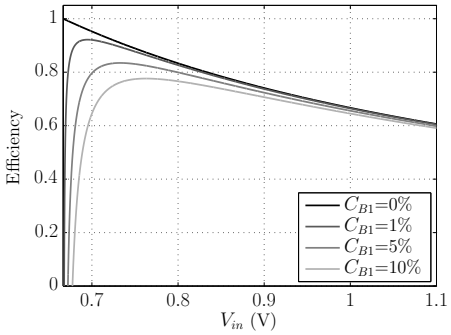
$$\eta_{3/2} = \frac{|P_{out}|}{|P_{in}|} \tag{2.48}$$

Again, due to the large size of the resulting equation only its plot is shown.

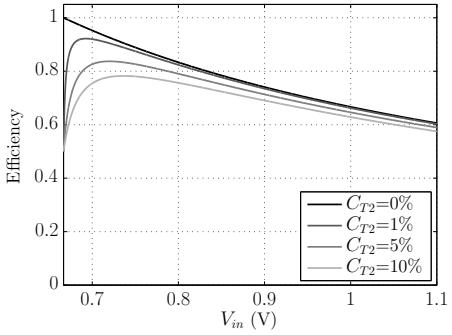
Figures 2.29 show the parasitic capacitances effect on the efficiency for a given value of V_{in}. Figures 2.29(a), 2.29(b), 2.29(c) and 2.29(d) show the effect of C_{T1}, C_{B1}, C_{T2}, and C_{B2}, respectively. These affect the efficiency almost in the same way - an increase in the capacitances result in a decrease on the efficiency and also limit the maximum working input voltage. This shift of the maximum efficiency peak is more noticeable in C_{T1} effect. Similar to the 2/3 converter figure 2.29(e) show that C_{T3} has no impact. The reason is the same - C_{T3} charge and discharge in parallel with C_3. Figure 2.29(f) shows the effect of C_G where the decrease in the efficiency is almost equal to the decrease caused if all parasitic capacitances of the flying capacitors were equal (Fig. 2.29(g)). Lastly, figure 2.29(h) shows the plot for $C_{T,B} = C_G$. The behaviour is the same as in the previous plots, although, as would be expected, the decrease in η is more noticeable. The simulation results (markers) prove that (2.48) accurately describes the behaviour of the efficiency of the converter and validates the theoretical analysis.



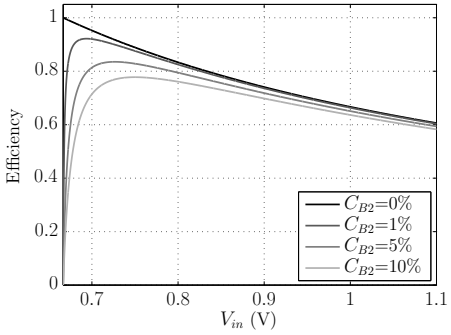
(a) C_{T1} effect with $C_{T2,3} = C_{B1,2} = C_G = 0$



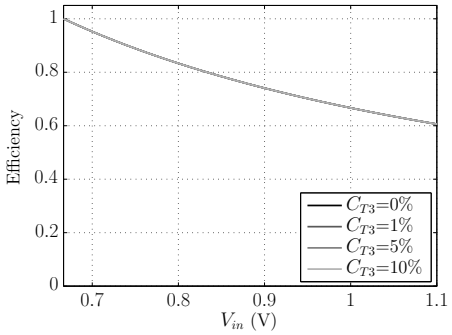
(b) C_{B1} effect with $C_{T1,2,3} = C_{B2} = C_G = 0$



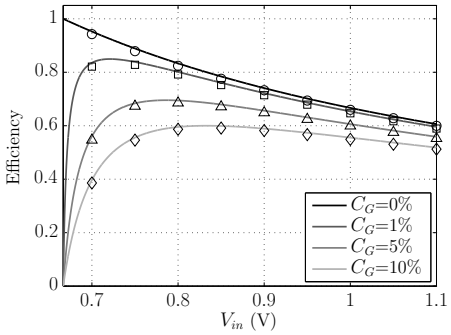
(c) C_{T2} effect with $C_{T1,3} = C_{B1,2} = C_G = 0$



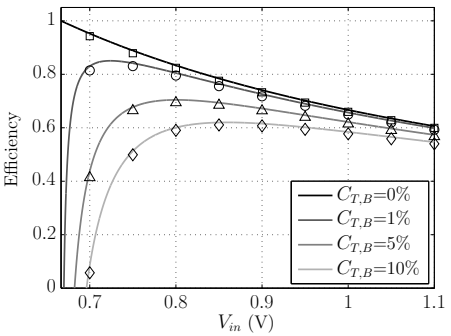
(d) C_{B2} effect with $C_{T1,2,3} = C_{B1} = C_G = 0$



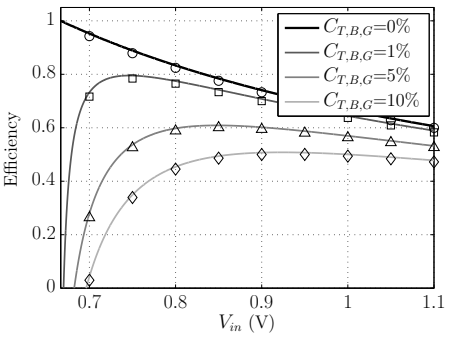
(e) C_{T3} effect with $C_{T1,2} = C_{B1,2} = C_G = 0$



(f) C_G effect with $C_{T1,2,3} = C_{B1,2} = 0$



(g) $C_{T,B}$ effect with $C_G = 0$



(h) $C_{T,B,G}$ effect

Figure 2.29: η as function of the clock frequency for $V_{out} = 1$ V and $C_1 = C_2 = C_3 = 0.33$ nF

CHAPTER 3

IMPLEMENTATION IN CMOS

3.1 Capacitor

In the previous chapter the impact of the parasitic capacitances of the flying capacitors in the converters circuits has been studied. The results showed that these have a strong impact in the output voltage as well as in the efficiency of the converters. Therefore, the structure chosen to implement the flying capacitors must be carefully understood. In this section the operation and vantages/disadvantages of two structures used to implement a capacitor in integrated circuits, *MOS* capacitors and MIM capacitors, are analysed .

3.1.1 MOS Capacitor Overview

A possible structure to build a capacitor in CMOS integrated circuit is to use a MOS transistor. This section will focus in the PMOS transistor, figure 3.1. In this configuration the transistor has two terminals - one terminal is the gate and the other is the source, drain and bulk all shorted together. In this configuration, $V_{DS} = 0$ and $V_{SG} = -V_{GS}$ is the voltage on the capacitor [8](Chapter 1).

The *PMOS* device has three operating regions - accumulation, depletion (weak inversion) and strong inversion. The *accumulation region* occurs when $V_{SG} < 0$ where n-type carriers from the n-well substrate are attracted (or accumulated) under the gate oxide. This results in a capacitor given by the sum of C_{GD}, C_{GS}, and C_{GB}. There is a significant resistance in series with C_{GB}. The resistance comes from the physical distance between the substrate connection and the area under the gate oxide. The resistivity of the source and drain regions in series with C_{GS} and C_{GD} tends to be small enough to be neglected in most circuit designs [9](Chapter 5).

When $0 < V_{SG} < |V_{thp}|$ the transistor enters in the *depletion region*. In this, the transistor is OFF and the small-signal capacitance is mainly provided by the overlap capacitances

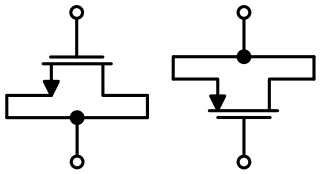


Figure 3.1: Simplified schematic of a NMOS and PMOS capacitor

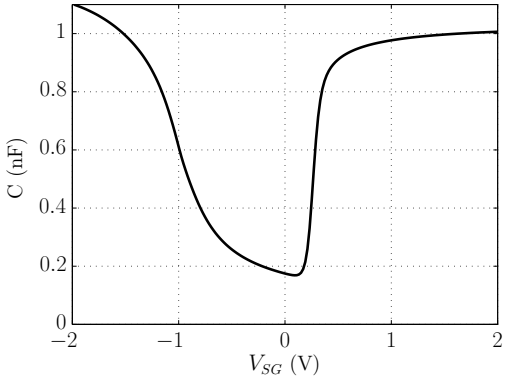


Figure 3.2: Simulation results derived by Spectre PMOS transistor with $-2 < V_{SG} < 2$

C_{GS} and C_{GD}. As V_{SG} increases a capacitance between the gate and the induced channel under the oxide appears.

If V_{SG} is sufficiently large ($\gg |V_{thp}|$), the device enters the *strong inversion* region and the small-signal capacitance is given by the sum of C_{GS}, C_{GD} and C_{GB} (which is usually neglected for being much smaller).

Figure 3.2 shows the three operating regions for a $-2 < V_{SG} < 2$. Due to the large parasitic resistance of the substrate connections around the gate oxide in the accumulation region it is preferable to operate in strong inversion. The PMOS body terminal is typically a n-type well in the p-type substrate, isolated from ground by a reversed biased pn-junction. Therefore, there is a junction capacitance between the body and ground, C_{BB}, which can be quite large and its value varies with changes in the body voltage. Simulation results from Spectre for a 130-nm CMOS technology using BSIM3v3.4 models showed $C_{BB} = 179.35$ pF, $C_{js} = 1.95$ pF and $C_{js} = 2.05$ pF for a PMOS capacitor with 1 nF of nominal capacitance value for $V_{SG} = 1$ V. This means a total parasitic capacitance (C_P) of 183.35 pF which represents 18.35% of the nominal value.

3.1.2 Metal-Insulator-Metal Capacitor

The MIM capacitor are formed by a thin insulator film between two plane metals (Fig. 3.3). The value of the simplified capacitance, neglecting fringe fields around the edges of the capacitor [1], is given by (3.1).

$$C = \frac{\varepsilon_{ox} A}{t_{ox}} \tag{3.1}$$

Where t_{ox} is the spacing between plates, ε_{ox} is the permittivity of the insulator between the plates and A is the area of the plates. These metal planes are asymmetric - the bottom plate is larger than the top plate. Thus, this results in a bottom parasitic capacitance larger

[1] These are relatively small if the capacitor area is large

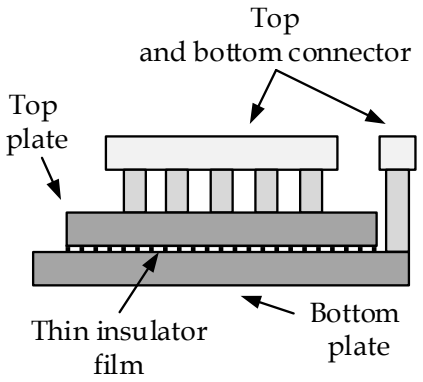


Figure 3.3: Simplified cross-section of a planner MIM capacitor

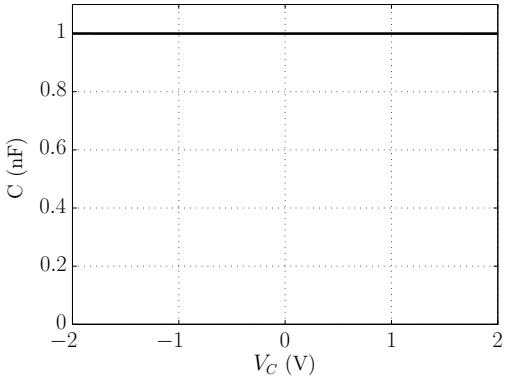


Figure 3.4: Simulation results for a 1 nF MIM capacitor with $-2 < V_C < 2$

than the top parasitic capacitance ($C_B > C_T$). In order to minimize the parasitic influence of the capacitances, the bottom plate of the capacitor can be connected to the node with constant potential with respect to ground [8](Chapter 1).

Simulation results obtained from spectre in a 130-nm technology, for a 1 nF MIM capacitor with a voltage across the terminals of 1 V, showed a bottom a top parasitic capacitances of 5.85 pF and 1.54 pF, respectively. This means a $C_T = 0.15\%$ and $C_B = 0.59\%$ of the nominal value of the capacitor. Figure 3.4 shows that the nominal value of the capacitance remains constant as the voltage across its terminals (V_C) varies.

3.1.3 Conclusions

The *MOS* capacitor is a relatively well-modelled by the standard circuits simulator, which makes it easy to analyse. It has a high capacitance-per-unit-area due to the very thin oxide layer. And lastly, it requires no special modification to CMOS integrated-circuit fabrication processes [8](Chapter 1). Nevertheless, its capacitance is highly non-linear and sensitive to voltage variations across the terminals. They also have a large bottom parasitic capacitances (18.34%), which may cause efficiency problems.

The MIM capacitor presents a high linear capacitance, reduced bottom/top plate parasitic capacitances and higher breakdown voltages. Although it has a lower capacitive density when compare with the *MOS* capacitor and requires extra masks in fabrication phase, which increases the cost[2] [10].

With this in mind, the chosen structure to implement the flying capacitors of the converters was the MIM capacitors. The main reasons relies on the low parasitic bottom/top capacitances and on the constant value of the nominal capacitance independently on the voltage across the terminals.

[2]Nowadays the cost of fabrication is less expensive

3.2 Switches

Apart from the flying capacitors, the other main issue affecting the efficiency of the converters is the influence of the parasitic capacitance due to the switches. In the previous chapter, it was showed that these could drastically decrease the converters efficiency. These parasitic capacitances are highly non linear which makes it difficult to modulate their effect. Through the next sections an analysis based on the work in [6] is presented, in order to have a reasonable approach of the value of these parasitic capacitances for a given W/L of the transistors in 130-nm technology.

3.2.1 Basic NMOS and PMOS Switch

An analog switch, in its most basic form, can be implemented by a single NMOS or PMOS transistor. These should have a low and linear ON resistance (R_{ON}) even for a large signal swing. R_{ON} refers to the resistance of the channel between the drain and source of the transistor, which, in the linear region, is given by [11]

$$R_{ON} = \frac{1}{g_{DS}} = \frac{L}{\mu\, C_{ox}\, W\, (v_{GS} - V_T - v_{DS})} \tag{3.2}$$

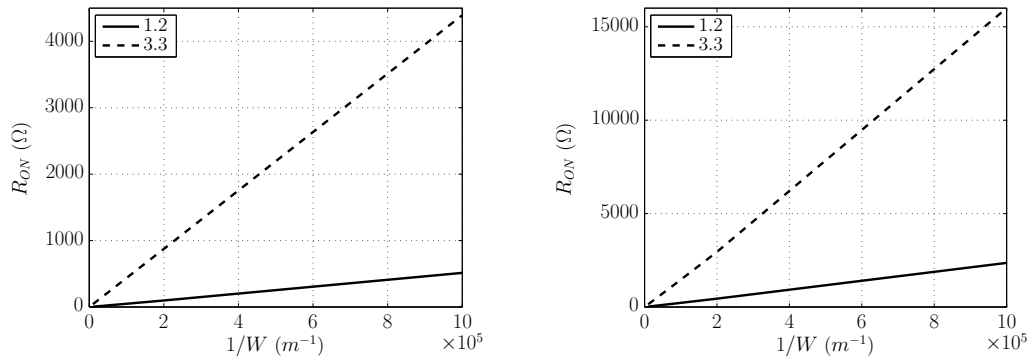
where g_{DS} refers to the drain-to-source conductance, μ the mobility in the channel, C_{ox} the oxide capacitance per unit are, W and L the width and length of the transistor, respectively, v_{GS} the gate-to-source voltage, V_T the threshold voltage and v_{DS} the drain-to-source voltage. Assuming that V_T is constant, v_{DS} is small and can be ignored (which is reasonable for small values of R_{ON}) and that the mobility is constant along the channel, then, R_{ON} depends on the geometry, W/L and on the effective gate-to-source voltage, $v_{eff} = v_{GS} - V_T$ [11].

Keeping L to its minimum, and applying a constant voltage of 1 V to the gate it is possible to calculate R_{ON} as a coefficient (k_R) divided by W [6]

$$R_{ON} = \frac{k_R}{W} \tag{3.3}$$

This coefficient, using the same procedure as in [6], was derived by simulation, using Spectre and standard 1.2 V and 3.3 V 130-nm CMOS technology and BSIM3v3.4 models. In these simulations, the W of the transistors was swept from 1 μm to 100 μm and a linear regression was performed over the obtained values of R_{ON}. Figures 3.5(a) and 3.5(b) show the values and the linear regression obtained for the NMOS and PMOS transistors, respectively. Table 3.1 show the values of k_R from the simulation.

For example, an 1.2 V transistor with an area of 12 μm^2 have a R_{ON} of 5.13 and 24.0 Ω for a NMOS and PMOS transistors ($L_{min} = 0.12$ μm), respectively. For the same area, using 3.3 V transistors, results in R_{ON} values of 124.7 and 397.5 Ω for NMOS ($L_{min} = 0.34$ μm) and PMOS ($L_{min} = 0.3$ μm) , respectively. This clearly shows the difficulty to attain low values of R_{ON} using 3.3 V transistors. If area was not a problem, it would be possible to increase W in order to obtain de desire R_{ON}. Although, as it is shown next, higher W will



(a) R_{ON} NMOS (b) R_{ON} PMOS

Figure 3.5: R_{ON} as function of W^{-1} for standard 1.2 V and 3.3 V 130-nm CMOS technology and BSIM3v3.4 models

Table 3.1: k_R values derived by electrical simulation using spectre

Device	k_R ($\mu\,\Omega\,\mathrm{m}$)
1.2 V NMOS	512.48
1.2 V PMOS	2400.0
3.3 V NMOS	4400.0
3.3 V PMOS	15900.0

lead to higher gate capacitances, which in turn, leads to an increase in the required power by the clock circuit.

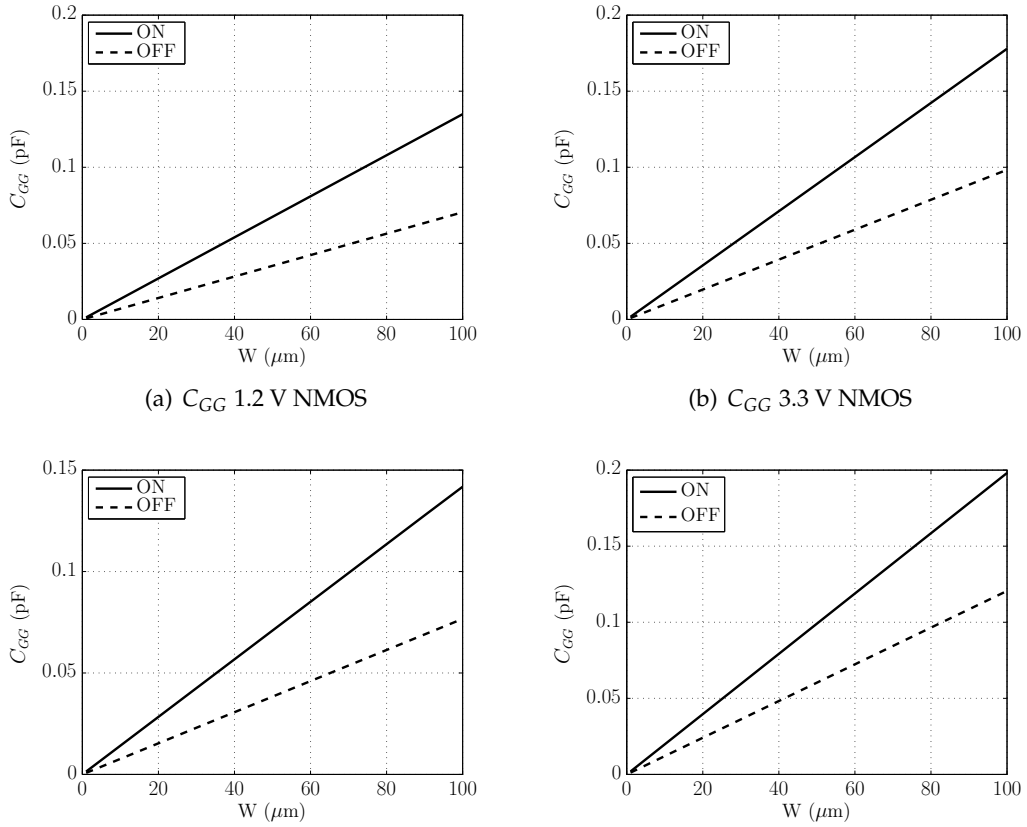
The second main issue with the MOS switch is the parasitic capacitance seen from the gate. It is mainly composed by the existing capacitance between the gate and the channel region (C_{GC}), the capacitance between the bulk and the channel (C_{BC}), the capacitances gate-to-source (C_{GS}) and the capacitance gate-to-drain (G_{GD}). For a simpler approach, the capacitance studied is the total gate capacitance (C_{GG}) which is defined by the sum off all the capacitances mention above. The value off C_{GG} is also proportional to the size of the transistor, this relation can be seen in the following equation [6]

$$C_{GG} = k_C\, W \tag{3.4}$$

where k_C relates C_{GG} to W. Combining (3.3) and (3.4) results in

$$R_{ON} = \frac{k_R\, k_C}{C_{GG}} \tag{3.5}$$

This shows that C_{GG} and R_{ON} are inversely proportional, as one increase the other decrease. Thus, there is a trade-off point where lowering R_{ON} brings no advantages, as C_{GG} increases the power required by the clock circuit.



(a) C_{GG} 1.2 V NMOS

(b) C_{GG} 3.3 V NMOS

(c) C_{GG} 1.2 V PMOS

(d) C_{GG} 3.3 V PMOS

Figure 3.6: C_{GG} as function of W for standard 1.2 V and 3.3 V 130 nm CMOS technology and BSIM3v3.4 models

The same analysis made to determine k_R was carried out to determine k_C. Figures 3.6 show that the value of C_{GG} changes from the ON state to the OFF state, where is approximately half of the ON value. This relation is verified in all the devices, figures 3.6(a), 3.6(b), 3.6(c) and 3.6(d), in the 3.3 V devices the relation is slightly greater, $\approx$55% for NMOS and $\approx$60% for PMOS. This is due to the increase of the gate-to-source and gate-to-drain capacitances caused by the increase of the gate-to-channel capacitance (ON state). On the OFF state these are reduced to the overlapped values [11]. Table 3.2 summarize the resulting values of k_C determined by performing a linear regression over the values obtained from simulation.

For example, for R_{ON} of 5 Ω, an 1.2 V transistor has a C_{GG} of 138 fF (NMOS) and 682 fF (PMOS), when ON with $L_{min} = 0.12$ μm, respectively. For the same R_{ON}, using 3.3 V transistors, results in C_{GG} values of 1.6 pF and 6.3 pF for NMOS ($L_{min} = 0.34$ μm) and PMOS ($L_{min} = 0.3$ μm), respectively. Although the k_C values are not so different between the 1.2 V and 3.3 V transistors, the increase in W for the same R_{ON} makes the 3.3 V transistors achieve much higher values of C_{GG} than the 1.2 V transistors.

Table 3.2: k_C values derived by electrical simulation using spectre

Device		k_C $(fF/\mu\text{m})$
1.2 V NMOS	ON	1.35
	OFF	0.70
1.2 V PMOS	ON	1.42
	OFF	0.77
3.3 V NMOS	ON	1.78
	OFF	0.98
3.3 V PMOS	ON	1.98
	OFF	1.2

3.2.2 Switch Sizing

The switches of the converter are implemented using NMOS and PMOS transistors, as shown in figure 3.7.

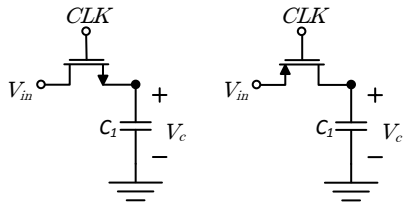


Figure 3.7: RC circuit using an NMOS and PMOS transistor and a capacitor

The ON resistance will determine the settling behaviour of the circuit, thus determining the voltage at the end of the clock phase. By using the capacitor charging equation, the settling error is given by [6]

$$error = e^{-\frac{T_{CLK}}{2\,R_{ON}\,C_1}} \tag{3.6}$$

solving the previous equation in order to R_{ON} and replacing $T_{CLK} = 1/F_{CLK}$ results in

$$R_{ON} = \frac{1}{2\,F_{CLK}\,C_1\,\ln\left[\frac{1}{error}\right]} \tag{3.7}$$

by fixing the variables *error*, C_1 and F_{CLK} the value of R_{ON} can be calculated. Combining (3.3) and (3.7) results in

$$W = 2\,k_R\,F_{CLK}\,C_1\,\ln\left[\frac{1}{error}\right] \tag{3.8}$$

this way, the size, W, of the transistors can be determined (L is kept to its minimum L_{min}). Finally, using (3.4) the value of C_{GG} can also be determined.

$$C_{GG} = 2\,k_C\,k_R\,F_{CLK}\,C_1\,\ln\left[\frac{1}{error}\right] \tag{3.9}$$

the three previous equation can be adapted to other technologies by simply adjusting the coefficients k_R and k_C.

3.2.3 Conclusions

The study presented in Sec. 3.2.1 showed that it is necessary to have large transistors in order to obtain small values of R_{ON}. These large transistors, apart from area problems, have high values of parasitic gate capacitance which leads to an increase in the power dissipated by the clock. Moreover, using 3.3 V transistors for such low values of R_{ON} results in abnormal values of W and C_{GG} which are impractical.

The last sub-section presented a way to sizing the transistors for a desire value of R_{ON}, F_{CLK} and determine the corresponding C_{GG} value.

3.3 Gate Oxide Breakdown

The supercapacitor can storage voltages up to 2.3 V. This means that the switches, in this case the 130-nm CMOS transistors, must be able to handle voltages of this magnitude because depending on the voltage across its terminals, a destructive breakdown of the transistor can occur. In this work there is no problem regarding *Junction Breakdown* - breakdown of the junction p-n that leads to a large reversed current flowing through this; as for the 130-nm technology the value of voltage breakdown is around $|10|$ V or higher (chapter 4)[12]. The main problem is the *Gate Oxide Breakdown* which occurs when the voltage across the oxide is above the limits causing a catastrophic failure (chapter 4)[12]. It is important to emphasize that oxide breakdown refers to the voltage between the gate-to-channel when the transistor is ON, and between the gate-substrate when the transistor is OFF. In 130-nm technologies, for gate oxides below the 3 nm (Ultrathin) the breakdown is different - *soft breakdown*. In this, the voltage of the gate does not collapse abruptly after the breakdown, the most significantly effect is an increase in the noise of the gate (Chapter 6)[13].

The models of the 130-nm 1.2 V transistors used (BSIM3v3.4) have a oxide thickness (t_{ox}) of 2.7 nm. According to [14, 15] these transistors, with this t_{ox}, can handled voltages until 2 V without compromising their lifetime.

3.4 Analysis of the Switches Impact on the SC DC-DC Converters

The size of the MOS switch will affect and determine the overall performance of the SC DC-DC converters. Therefore, a study on how the clock frequency, input/output voltage and output power affects the ON-resistance, gate capacitance and the size of the switches was carried out. This study aims to understand the limits of the output power due to the limitation of the technology used, i.e. understand the impacts of using large switches.

3.4.1 1/2 Converter

As mention in Sec. 3.2.1 the two main variables of a CMOS switch are its ON resistance (R_{ON}) and the parasitic gate capacitance (C_{GG}). Combining (3.7) and (2.11), which are repeated where for convenience, a relation between the input voltage and the value of R_{ON} can be obtained.

$$R_{ON} = \frac{1}{2\,F_{CLK}\,C_1\,\ln\left[\dfrac{1}{error}\right]} \tag{3.7 revisited}$$

$$F_{CLK_{1/2}} = \frac{V_{out}}{R_{out}\left(2\,C_1\left(V_{in} - 2\,V_{out}\right) + C_{T1}\left(V_{in} - V_{out}\right) - C_{B1}\,V_{out}\right)} \tag{2.11 revisited}$$

The new R_{ON} can be seen in (3.10).

$$R_{ON_{1/2}} = \frac{\left(2\,C_1 + C_{T1}\right)R_{out}\,V_{in} - \left(4\,C_1 + C_{B1} + C_{T1}\right)R_{out}\,V_{out}}{2\,C_1\,V_{out}\,\ln\left[\dfrac{1}{error}\right]} \tag{3.10}$$

Considering the ideal capacitor ($C_{T1} = C_{B1} = 0$), $R_{ON_{1/2}}$ does not depend on the value of the flying capacitance, as the follow equation shows

$$R_{ON_{1/2}} = \frac{R_{out}\left(V_{in} - 2\,V_{out}\right)}{V_{out}\,\ln\left[\dfrac{1}{error}\right]} \tag{3.11}$$

Since V_{out} is fixed at 1 V, V_{in} is fixed according to the maximum frequency/efficiency and the *error* is fixed at 1%, $R_{ON_{1/2}}$ only depends on R_{out}. Considering that the output power, P_{out} is given by $P_{out} = V_{out}^2/R_{out}$, then $R_{ON_{1/2}}$ can be written as function of P_{out}. The resulting equation is given by

$$R_{ON_{1/2}} = \frac{V_{out}\left(V_{in} - 2\,V_{out}\right)}{P_{out}\,\ln\left[\dfrac{1}{error}\right]} \tag{3.12}$$

the equation shows that $R_{ON_{1/2}}$ is inversely proportional to P_{out}. The width, W of the switches can also be determined using (3.3).

$$W_{1/2} = \frac{k_R\,P_{out}\,\ln\left[\dfrac{1}{error}\right]}{V_{out}\left(V_{in} - 2\,V_{out}\right)} \tag{3.13}$$

Finally, C_{GG} can be determined using (3.4)

$$C_{GG_{1/2}} = \frac{k_R\, k_C\, P_{out}\, \ln\left[\dfrac{1}{error}\right]}{V_{out}\,(V_{in} - 2\,V_{out})} \tag{3.14}$$

The clock power can be analysed in terms of the power required by an inverter to charge and discharge the gate capacitance of the switch (3.15).

$$P_{CLK} = C_{GG}\, F_{CLK}\, V_{CLK}^2 \tag{3.15}$$

where V_{CLK} is the voltage swing of the inverter. Considering only one switch, (3.15) can be written using (2.11) in place of F_{CLK} and (3.14) in place of C_{GG}. The new equation, considering an ideal capacitor ($C_{T1} = C_{B1} = 0$), is given by

$$P_{CLK_{1/2}} = -\frac{k_R\, k_C\, V_{CLK}^2\, P_{out}^2\, \ln\left[\dfrac{1}{error}\right]}{V_{out}^2\,(V_{in} - 2V_{out})\,(4\,C_1\,V_{out} - 2\,C_1\,V_{in})} \tag{3.16}$$

note that $P_{CLK_{1/2}} \propto P_{out}^2$. The influence of V_{CLK} on the power dissipation needs to be carefully analysed. Increasing it will increase the V_{eff} of the transistors, thus the value of R_{ON} will decrease for the same area. Therefore, W can be reduced leading to smaller values of C_{GG}. Since $k_{R,C}$ where determined for a V_{GS} of 1 V (-1 V for PMOS), this value will be used for both NMOS and PMOS switches ($|V_{CLK}| = 1$ V).

3.4.2 2/3 Converter

The same analysis carried in the previous section is repeated here with the equations of the 2/3 converter. In this, it is assumed that the flying capacitors have all the same value $C_1 = C_2 = C_3$. Combining (3.7) and (2.23), which is repeated here for convenience and considering an ideal capacitor for simplicity, the relation between the input voltage and the value of R_{ON} is given by (3.17).

$$F_{CLK_{2/3}} = \frac{2\,V_{out}}{2\,C_1\,R_{out}\,V_{in} - 3\,C_1\,R_{out}\,V_{out}} \tag{2.23 revisited}$$

$$R_{ON_{2/3}} = \frac{R_{out}\,(2\,V_{in} - 3\,V_{out})}{4\,V_{out}\,\ln\left[\dfrac{1}{error}\right]} \tag{3.17}$$

The relationship between P_{out} and R_{ON}, W and C_{GG} are given by

$$R_{ON_{2/3}} = \frac{V_{out}\,(2\,V_{in} - 3\,V_{out})}{4\,P_{out}\,\ln\left[\dfrac{1}{error}\right]} \tag{3.18}$$

$$W_{2/3} = \frac{4\,k_R\,P_{out}\,\ln\left[\dfrac{1}{error}\right]}{V_{out}\,(2\,V_{in} - 3\,V_{out})} \tag{3.19}$$

$$C_{GG_{2/3}} = \frac{4\,k_R\,k_C\,P_{out}\,\ln\left[\dfrac{1}{error}\right]}{V_{out}\,(2\,V_{in} - 3\,V_{out})} \tag{3.20}$$

Replacing (2.23) and (3.20) in (3.15), gives the power required by the clock per switch (3.21)

$$P_{CLK_{2/3}} = \frac{8\,k_R\,k_C\,V_{CLK}^2\,P_{out}^2\,\ln\left[\dfrac{1}{error}\right]}{C_1\,V_{out}^2\,(2\,V_{in} - 3\,V_{out})^2} \tag{3.21}$$

3.4.3 1/1 Converter

The 1/1 converters is the simplest converter with only two switches. Combining (3.7) and (2.34), which is repeated here for convenience, the relation between the input voltage and the value of R_{ON} is shown in (3.22).

$$F_{CLK_{1/1}} = \frac{V_{out}}{(C_1 + C_{T1})\,R_{out}\,(V_{in} - V_{out})} \tag{2.34 revisited}$$

$$R_{ON_{1/1}} = \frac{(C_1 + C_{T1})\,R_{out}\,(V_{in} - V_{out})}{2\,C_1\,V_{out}\,\ln\left[\dfrac{1}{error}\right]} \tag{3.22}$$

As before, considering an ideal capacitor ($C_{T1} = 0$) $R_{ON_{1/1}}$ does not depend on the value of the flying capacitance (3.23).

$$R_{ON_{1/1}} = \frac{R_{out}\,(V_{in} - V_{out})}{2\,V_{out}\,\ln\left[\dfrac{1}{error}\right]} \tag{3.23}$$

The relationship between P_{out} and R_{ON}, W and C_{GG} are given by

$$R_{ON_{1/1}} = \frac{V_{out}\,(V_{in} - V_{out})}{2\,P_{out}\,\ln\left[\dfrac{1}{error}\right]} \tag{3.24}$$

$$W_{1/1} = \frac{2\,k_R\,P_{out}\,\ln\left[\dfrac{1}{error}\right]}{V_{out}\,(V_{in} - V_{out})} \tag{3.25}$$

$$C_{GG_{1/1}} = \frac{2\,k_R\,k_C\,P_{out}\,\ln\left[\dfrac{1}{error}\right]}{V_{out}\,(V_{in} - V_{out})} \tag{3.26}$$

Replacing (2.34) and (3.26) in (3.15), the power required by the clock per switch is given by

$$P_{CLK_{1/1}} = \frac{2\,k_R\,k_C\,V_{CLK}^2\,P_{out}^2\,\ln\left[\dfrac{1}{error}\right]}{C_1\,V_{out}^2\,(V_{in} - V_{out})^2} \tag{3.27}$$

3.4.4 3/2 Converter

Finally, the analysis is repeated for the last converter - 3/2 converter. Where again the flying capacitors have equal values, $C_1 = C_2 = C_3$. Combining (3.7) and (2.45), which is repeated here for convenience and considering the ideal capacitor for simplicity, the relation between the input voltage and the value of R_{ON} is given by (3.28)

$$F_{CLK_{3/2}} = \frac{3\,V_{out}}{C_1\,R_{out}\,(3\,V_{in} - 2\,V_{out})} \tag{2.45 revisited}$$

$$R_{ON_{3/2}} = \frac{R_{out}\,(3\,V_{in} - 2\,V_{out})}{6\,V_{out}\,\ln\left[\dfrac{1}{error}\right]} \tag{3.28}$$

The relationship between P_{out} and R_{ON}, W and C_{GG} is given by

$$R_{ON_{3/2}} = \frac{V_{out}\,(3\,V_{in} - 2\,V_{out})}{6\,P_{out}\,\ln\left[\dfrac{1}{error}\right]} \tag{3.29}$$

$$W_{3/2} = \frac{6\,k_R\,P_{out}\,\ln\left[\dfrac{1}{error}\right]}{3\,V_{in}\,V_{out} - 2\,V_{out}^2} \tag{3.30}$$

$$C_{GG_{3/2}} = \frac{6\,k_R\,k_C\,P_{out}\,\ln\left[\dfrac{1}{error}\right]}{3\,V_{in}\,V_{out} - 2\,V_{out}^2} \tag{3.31}$$

Replacing (2.45) and (3.31) in (3.15), the power required by the clock per switch is given by

$$P_{CLK_{2/3}} = \frac{18\, k_R\, k_C\, V_{CLK}^2\, P_{out}^2\, \ln\left[\dfrac{1}{error}\right]}{C_1\, V_{out}^2\, (3\, V_{in} - 2\, V_{out})^2} \tag{3.32}$$

3.4.5 Conclusions

To help understand the impact of the power dissipation due to the the charge and discharge of the gate parasitic capacitances from the switches, the 1/2 converter was analysed in detail. Notice that the same analysis can be replicated for the other three converters.

The equations of the switch $R_{ON_{1/2}}$ (3.12) showed an inversely proportional relation to the output power. Moreover, there is also a linear relation with the input voltage. These are the two main variables that will define the value of the switch ON resistance.

Figure 3.8 shows the plot (3.12) for a P_{out} sweep between 1 mW to 20 mW, four different values of V_{in}, $V_{out} = 1$ V and a *error* of 1%. As expected the plot shows that R_{ON} decreases as P_{out} increases, and vice-versa. Moreover, as V_{in} decreases the value of R_{ON} decreases as well. This means that the minimum value of V_{in} determines the minimum required value for R_{ON}. This minimum value of V_{in} is the voltage limit until which the converter operates. In order to guarantee that the switches work on the voltage limit means they will be oversized when V_{in} is above the limit.

Figure 3.9 shows the plots of (3.13) for an 1.2 V NMOS and PMOS transistors[3], a P_{out} sweep between 1 mW to 20 mW, four different values of V_{in}, $V_{out} = 1$, and a *error* of 1%. As seen in Sec. 3.2.1 W is inversely proportional to R_{ON}. Therefore, the plots shows that $P_{out} \propto W$; as P_{out} increases so does W increases. The plots show that using PMOS switches results in a substantial larger W comparing with NMOS switches for the same values of P_{out}. Thus, in order to reduced the area it is preferable to use NMOS rather PMOS switches.

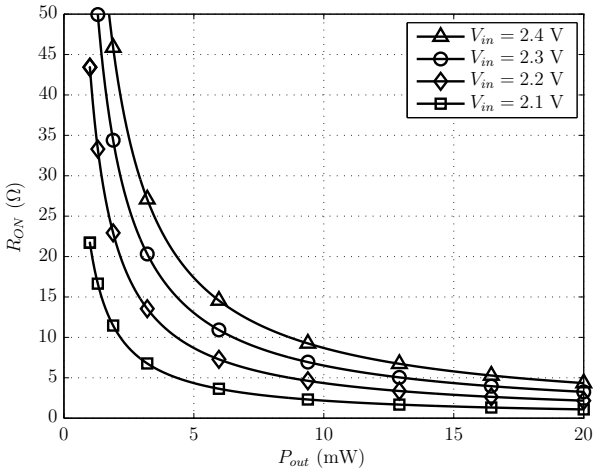
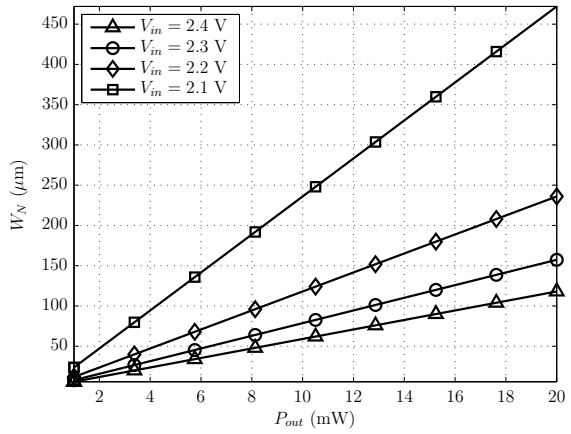
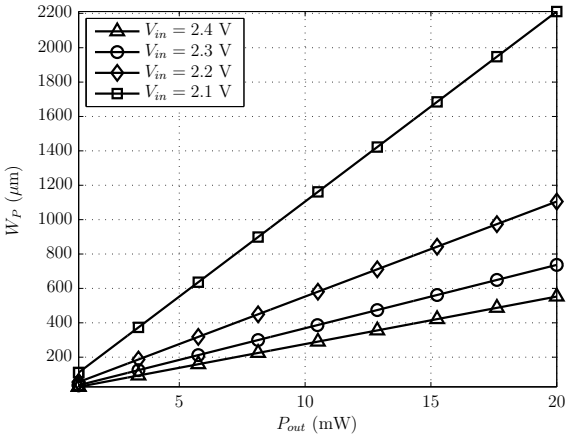


Figure 3.8: $R_{ON_{1/2}}$ as function of P_{out} for $V_{out} = 1$ V and $error = 1\%$

[3]The values of k_R and k_C are the ones derived by simulation in Sec. 3.2.1



(a) W NMOS

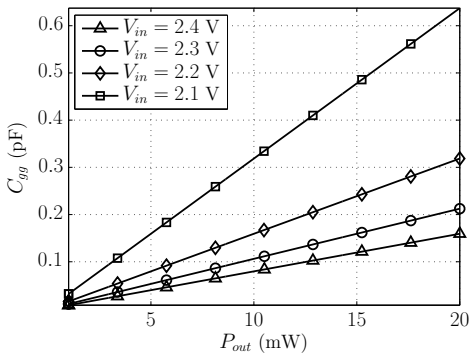


(b) W PMOS

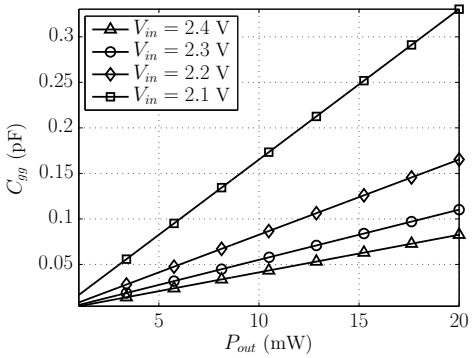
Figure 3.9: W of a 1.2 V NMOS and PMOS switch as function of P_{out} for $V_{out} = 1$ V and $error = 1\%$

Figure 3.10 shows the plot of (3.14) for an 1.2 V NMOS and PMOS transistors[3], a P_{out} sweep between 1 mW to 20 mW, four different values of V_{in}, $V_{out} = 1$, and a *error* of 1%. Since C_{GG} changes its value between the ON and OFF states there are two plots for each switch state. As seen in the equations $C_{GG} \propto P_{out}$, therefore the plots show that increasing P_{out} leads to an increase in C_{GG}, and vice-versa. There is an increase in the W of PMOS switches when comparing with NMOS switches for the same P_{out}. These plots shows the consequences of this difference - the values of C_{GG} are higher on the PMOS, approximately 5 times, than the NMOS switches. The difference between the switch ON and OFF state is almost to two times of the ON value in the OFF state. It is important to notice the magnitude of the values of C_{GG} for powers above the 5 mW, especially on the PMOS transistors which reach 3 pF at 20 mW. These values are abnormally high and will require high power to charge and discharge - transition between ON and OFF state.

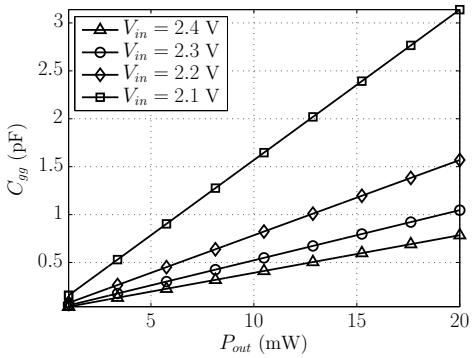
The previous plots refer only to one switch. In the 1/2 converter, there are two active switches in ϕ_1 and other two in ϕ_2. This means that the values presented in the plot of



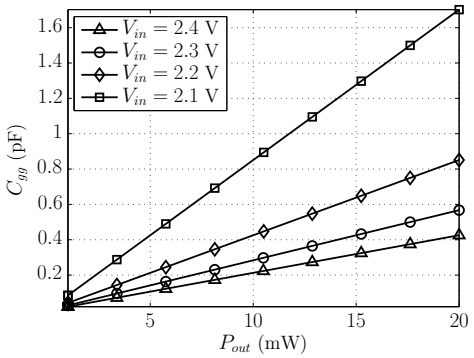
(a) $C_{GG_{1/2}}$ ON state NMOS



(b) $C_{GG_{1/2}}$ OFF state NMOS



(c) $C_{GG_{1/2}}$ ON state PMOS



(d) $C_{GG_{1/2}}$ OFF state PMOS

Figure 3.10: C_{GG} of a 1.2 V NMOS and PMOS switch as function of P_{out} for $V_{out} = 1$ V and $error = 1\%$.

$R_{ON_{1/2}}$ must be divided by two. Moreover, this means that there will be four $C_{GG_{1/2}}$ to charge and discharge by the clock. Since the range of operation of this converter is 2.3 V to 2 V, this means that the switches must be implemented by PMOS transistors as there is no available clock source higher than V_{in}.

With this in mind, it is possible to determine (approximately) the power dissipated by the clock, P_{CLK}, for the 1/2 converter with four PMOS switches assuming that these are feed through CMOS inverters with a voltage swing of V_{in} to (V_{in}-1 V)[4]. Equation (3.33) shows the total power delivered by the clock as the sum of each power from each switch.

$$P_{CLK_{1/2}} = 4 \cdot P_{CLK_{1/2,PMOS}} \tag{3.33}$$

Figure 3.11 shows the plot of (3.33) for an 1.2 V NMOS and PMOS transistors, a P_{out} sweep between 1 mW to 20 mW, three different values of V_{in}, $V_{out} = 1$ and a *error* of 1%. As P_{out} increases the P_{CLK} of all the switches increase quadratically. Moreover, has the limit voltage of operation decreases P_{CLK} increases as expected.

To better understand the impact of the power delivered by the clock to the switches, figure 3.12 shows the plot of (2.18) with C_G replaced by the four parasitic gate capacitances

[4]In order to maintain valid the coefficients k_R and k_C derived for a V_{gs} of 1 V

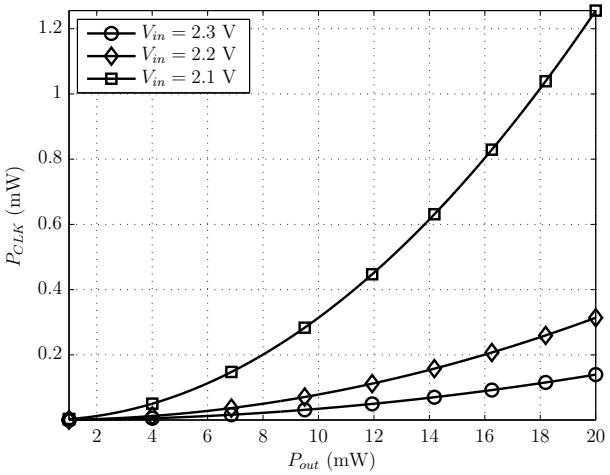


Figure 3.11: $P_{CLK_{1/2}}$ as function of P_{out} for $V_{out} = 1$ V and $error = 1\%$

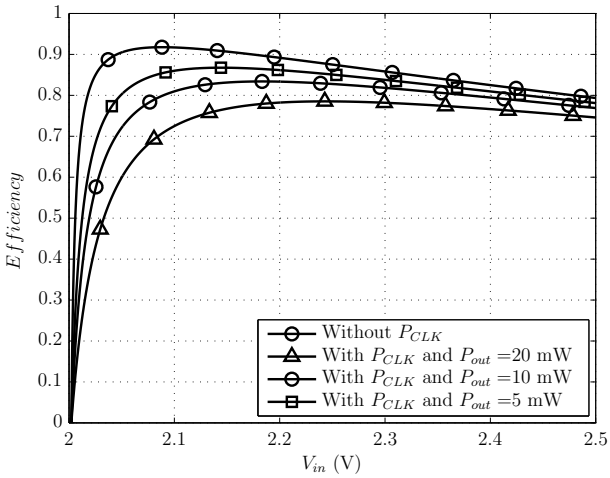


Figure 3.12: η as function of V_{in} for $V_{out} = 1$ V and $error = 1$ % with the parasitic capacitance effect from the switches

of the PMOS switches and C_{T1} and C_{B1} replaced by the parasitic capacitances of the MIM capacitor, 0.15% and 0.59% of C_1 value, respectively. The plot shows that for a C_G of zero, the efficiency has a maximum value of around 90%. When accounting the value of P_{CLK} in function of P_{out} the plots shows, as expected, a decrease in the efficiency. Moreover, for $P_{out} = 20$ mW the maximum efficiency is reduced, approximately, by 10%. For lower values of P_{out} this effect is reduced.

The aim of this study was to better understand how the switches affects the operation of the SC DC-DC converters. The output power and the limit voltage of operation must be carefully chosen, due to these have a high impact on the overall efficiency of the converters. Remembering, that this results are approximations to have an overall idea and starting point when sizing the switches. Simulations are needed to have more accurate results.

CHAPTER 4

PROPOSED CIRCUIT AND SYSTEM

As previously discussed in chapter 1 the main goal of this work is to have a SC DC-DC converter that achieves maximum efficiency throughout the input voltage range by configuring its topology to match one of the the four SC DC-DC converter topologies presented in chapter 2. This approach uses the same capacitor for all the circuits thus saving area. For this one converter to work, it needs two main controllers to select the state (1/2, 2/3, 1/1 or 3/2) and to generate the clock signals to each switch accordingly to the active state. This section presents the design of the converter and its implementation. Discusses the issues that must be solved in order to achieve a correct operation. The overall system description and operation principle of each block are also presented.

4.1 Proposed Circuit

Figure 4.1 shows the simplified schematic of the proposed SC DC-DC converter. There are a total of 15 switches (A_1, A_2, etc.) which simultaneous control the state (1/2, 2/3, 1/1 and 3/2) and the phase (ϕ_1 and ϕ_2) of the active converter. The capacitors $C_{1,2,3}$ represent the flying capacitors. Table 4.1 shows the active switches per state and phase.

In each state the active switches (Table 4.1) define a path for each phase that performs the same operation of the converters described and studied in section 2. The main difference is that there are three flying capacitors (C_1, C_1 and C_3). Because states 2/3 and 3/2 need this numbers of capacitors to perform the voltage conversion. In states 1/2 and 1/1, where only one capacitor is needed, the capacitors are connected in parallel ($C_{fly} = C_1 + C_1 + C_3$) and the switches are divided into three (e.g. $A = A_1 + A_2 + A_3$) in both phases to perform the conversion.

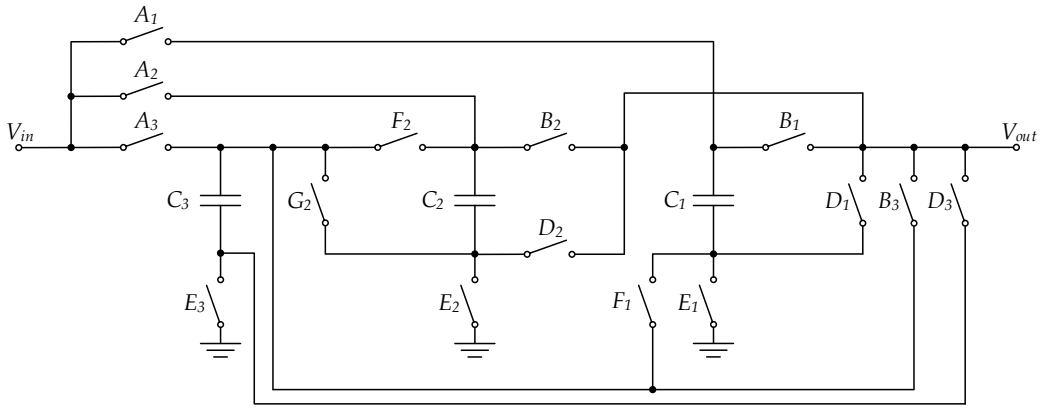


Figure 4.1: Simplified schematic of the proposed SC DC-DC converter

Table 4.1: Active switches on each state

Phase	1/2	2/3	1/1	3/2
	$A_1\ A_2\ A_3$	A_1	$A_1\ A_2\ A_3$	$A_1\ A_2$
ϕ_1	$D_1\ D_2\ D_3$	$E_2\ E_3$	$E_1\ E_2\ E_3$	$E_1\ E_3$
		$F_1\ F_2$		G_2
	$B_1\ B_2\ B_3$	$B_1\ B_2$	$B_1\ B_2\ B_3$	B_1
ϕ_2	$E_1\ E_2\ E_3$	$E_1\ E_3$	$E_1\ E_2\ E_3$	$E_2\ E_3$
		G_2		$F_1\ F_2$

4.1.1 Design Constraints

The proposed converter is designed using a 130-nm CMOS technology and MIM capacitors, including parasitics ($C_T = 0.15\%$ and $C_B = 0.59\%$, see section 3.1.3), are used to implement the flying capacitors. Limiting the total area for the capacitors to 1 mm^2 results in a maximum capacitance value of 1 nF. Therefore, the 1/2 and 1/1 converters will have a capacitor of 1 nF composed by three 0.33 nF capacitors in parallel, and the 2/3 and 3/2 converters will have three 0.33 nF capacitors.

As mention in section 3.3 the 1.2 V transistors only support voltages until 2 V before they suffer from gate oxide breakdown. When the super-capacitor is fully charged (2.3 V), the switches A will have to withstand 2.3 V which is out of the safe operation region. The 3.3 V transistors have large parasitic gate capacitances and it is difficult to attain low values of R_{ON}. Therefore, to overcome this problem without recurring to 3.3 V transistors the choice of transistors (NMOS or PMOS) and ways to avoid voltage breakdown were carefully analysed.

The A switches must be PMOS transistors since there is no available voltage above V_{in}. Moreover, to work in the safe operation region, the switch voltages (V_G), were controlled

to always be below 2 V. For example, when ON, the V_G of the A switch have 1 V instead of 0 V ($V_{SG} = V_{DG} = 2.3 - 1 = 1.3$ V); when OFF, V_G has the same voltage as V_{in} ($V_{SG} = V_{DG} = V_{DB} = 2.3 - 2.3 = 0$ V)[1]. This way the voltage gate-to-channel and gate-to-substrate is always smaller than the maximum allowable voltage.

The B switches also deal with the maximum voltage of V_{in}. And, when ON, they handle voltages of around 1 V. Therefore, they are implemented again by PMOS transistors with a clock swing from V_{in} to 0 V. The problems regarding the gate oxide breakdown only arise in the $1/2$ and $2/3$ states. However, as the clock signal decreases from V_{in} to zero the node voltage (the one with V_{in}) decreases, with the same pace, from V_{in} to around 1 V and so neither V_{SG} or V_{DG} have a voltage above 1.3 V.

The D switches are only used in the $1/2$ state. These connect the flying capacitor in parallel with the output capacitor. Therefore, they always handled voltages of half the input voltage. In the worst case, they will have V_D and V_S of around 1.15 V and so they work within the safe operation region. They are implemented trough PMOS transistors since their drain voltage is always around 1 V.

The E switches are responsible for connecting the flying capacitors to ground. Thus, they can easily be implemented by NMOS transistors. The maximum voltage occurs in the $1/2$ converter and in the worst case is 1.15 V. Therefore, they are always in the safe operation region.

The F_1 and G_2 switches are used in the $2/3$ and $3/2$ converters. They are implemented by NMOS switches since their drain voltages are below 1 V. However, they are connected to voltages close to 1 V, which means that these switches must either be implemented using a transmission gate or use a up-converted clock signal. In the $1/2$, these switches are OFF ($V_G = 0$) and $V_S = V_{in}$ which is, in the worst case, outside the safe operation region. To overcome this problem, a technique using stacking of transistors was used [16] in order to reduced the voltage across them. This technique can be applied because $V_D = 0$ when $V_S = V_{in}$ and so using two transistors, with equal sizes, performs a resistive ladder to ground. The transistor connecting to V_{in} has a gate voltage of 1 V ($V_{GS} = 1 - V_{in} = -1.3$ V) which remains OFF and has a maximum voltage across the gate within the safe operating region. The second transistor has a $V_{GS} = 1.15$ V that is also within the safe operation region. With this protection the switches were implemented by NMOS transistors with complementary circuits to up-convert the clock signal, which be explain later in this section.

Lastly, the F_2 switch is implemented by an NMOS transistor with a up-convert clock signal for the same reasons of the F_1 and G_2 switches. This switch is activated in $2/3$ and $3/2$ states, and in the $1/2$ state is connect to V_{in} in both terminals ($V_G = V_S = V_{in}$). Again, when $V_{in} = 2.3$ V to avoid the gate destruction, V_G is set at 1 V. This results in a $V_{GS} = V_{GD} = 1.15$ V and so the switch remains OFF and within the safe operating region.

[1]In the OFF state, V_{DG} may not have the same value has V_{SG} since the voltage of the node can vary. Therefore, it is necessary to have into account what is the voltage of V_{DG} when the switch is OFF and if it is under the limits of breakdown.

Switches A, B and D where implemented by 1.2 V PMOS transistors and E, F and G by 1.2 V NMOS transistors.

4.1.2 Efficiency Analysis and Operation Limits

The proposed circuit performs the operation of four different converters. As shown in chapter 2 the impact of the parasitic capacitance of the flying capacitors and switches is different from one converter to another. Moreover, the efficiency, frequency and output voltage is also distinct and depends strongly in the design of the switches. In the proposed circuit, the number of active switches in each state is not the same as in the studied converters in chapter 2. To understand how this will impact the efficiency, in each state, the analysis made in chapter 2 and section 3.4 is now repeated for the proposed converter.

4.1.2.1 1/2 State

Table 4.2 shows the ON switches in each phase for the 1/2 state. In ϕ_1 the A and D switches are ON. This means that there are two R_{ON} in series with the flying capacitor. The $R_{ON_{1/2}}$ (3.12) from the 1/2 converter (section 3.4.2), only considers one R_{ON}, therefore it must be divided by two. Furthermore, since A is divided into three switches with one third of the size and the flying capacitor is also one third of its nominal value, the $R_{ON_{1/2}}$ equation remains valid. Although, since W is three times smaller ($L = L_{min}$) the R_{ON} of each individual switch (A_1, A_2 and A_3) is three times higher. The same conclusions are valid to ϕ_2 with B and E switches. The resulting R_{ON} for each switch is given by

$$R_{ON_{A_{1,2,3}}} = R_{ON_{B_{1,2,3}}} = R_{ON_{D_{1,2,3}}} = R_{ON_{E_{1,2,3}}} = 3\,\frac{R_{ON_{1/2}}}{2} \tag{4.1}$$

Table 4.2: Active switches on the 1/2 state in each phase

ϕ_1	ϕ_2
A_1 A_2 A_3	B_1 B_2 B_3
D_1 D_2 D_3	E_1 E_2 E_3

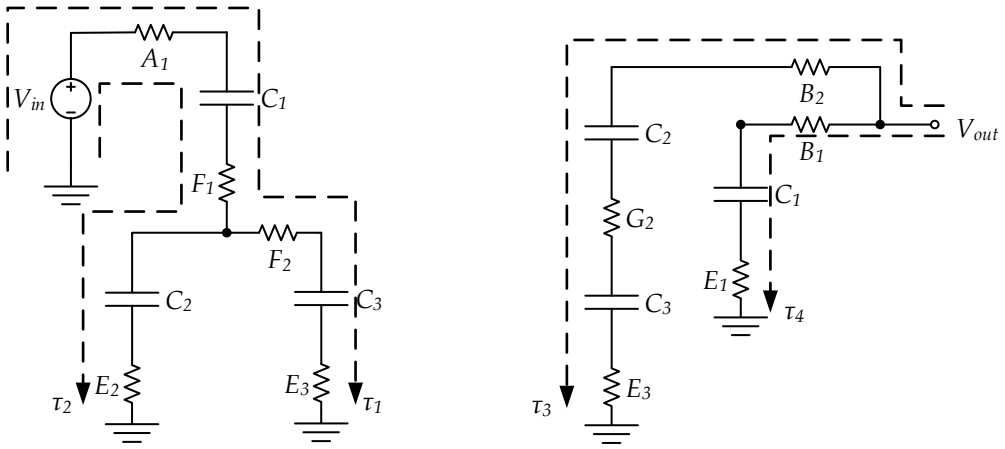
4.1.2.2 2/3 State

In the 2/3 state the three capacitors are not all in parallel and so the R_{ON} analysis is not as simple as the 1/2 state. To calculate each R_{ON} of the switches would imply a third order differential equation which solution is quite complex. Therefore, to make it easier, a method using the time constants of each branch to determine the R_{ON} value was used. When a switch share two different time constant the slowest one is chosen. This way, even though some switches may be oversized, the design will be according to the specifications. Table 4.3 shows the ON switches in each phase.

Figure 4.2 shows the 2/3 state with the R_{ON} from the active switches. There are two time constants in each phase, performing a total of four time constants. These are given by

Table 4.3: Active switches on the 2/3 state

ϕ_1	ϕ_2
A_1	B_1 B_2
E_2 E_3	E_1 E_3
F_1 F_2	G_2



(a) Phase 1 (b) Phase 2

Figure 4.2: Simplified schematic of the 2/3 SC converter in the two phases

$$\phi_1 : \begin{cases} \tau_1 = 4\,R_{ON}\,(C_1//C_3) = 2\,R_{ON}\,C_1 \\ \tau_2 = 3\,R_{ON}\,(C_1//C_2) = \frac{3}{2}\,R_{ON}\,C_1 \end{cases}$$
$$\phi_2 : \begin{cases} \tau_3 = 3\,R_{ON}\,(C_1//C_3) = \frac{3}{2}\,R_{ON}\,C_1 \\ \tau_4 = 2\,R_{ON}\,C_1 \end{cases} \tag{4.2}$$

In ϕ_1 the slowest time constant is τ_1 and in ϕ_2 the slowest is τ_4. Thus, relating each switch with its time constant and (3.18) from section 3.4.2; the R_{ON} of each switch is

$$\begin{aligned} R_{ON_{A_1}} &= \frac{R_{ON_{2/3}}}{2} & R_{ON_{E_1}} &= \frac{R_{ON_{2/3}}}{2} & R_{ON_{F_1}} &= \frac{R_{ON_{2/3}}}{4} \\ R_{ON_{B_1}} &= \frac{R_{ON_{2/3}}}{2} & R_{ON_{E_2}} &= \frac{2}{3}\,R_{ON_{2/3}} & R_{ON_{F_2}} &= \frac{R_{ON_{2/3}}}{2} \\ R_{ON_{B_2}} &= \frac{2}{3}\,R_{ON_{2/3}} & R_{ON_{E_3}} &= \frac{R_{ON_{2/3}}}{2} & R_{ON_{G_2}} &= \frac{2}{6}\,R_{ON_{2/3}} \end{aligned} \tag{4.3}$$

Notice that the switches F_1 and G_2 have two transistors for voltage protection reasons. And so, their R_{ON} must be divided by two.

4.1.2.3 1/1 State

Table 4.4 shows the active switches on the 1/1 state in each phase. In ϕ_1 both A and E are ON. Therefore, their R_{ON} has to be $R_{ON_{1/1}}$ (section 3.4.3 Eq. (3.24)) divided by two. In ϕ_2 B

and E are ON, thus $R_{ON_{1/1}}$ must also be divided by two. Lastly, the switches are divided into three individual switches as well as the flying capacitor, thus the value of their R_{ON} must be multiplied by three. The R_{ON} of each individual switch is given by

$$R_{ON_{A_{1,2,3}}} = R_{ON_{B_{1,2,3}}} = R_{ON_{E_{1,2,3}}} = 3\,\frac{R_{ON_{1/1}}}{2} \tag{4.4}$$

Table 4.4: Active switches on the 1/1 state

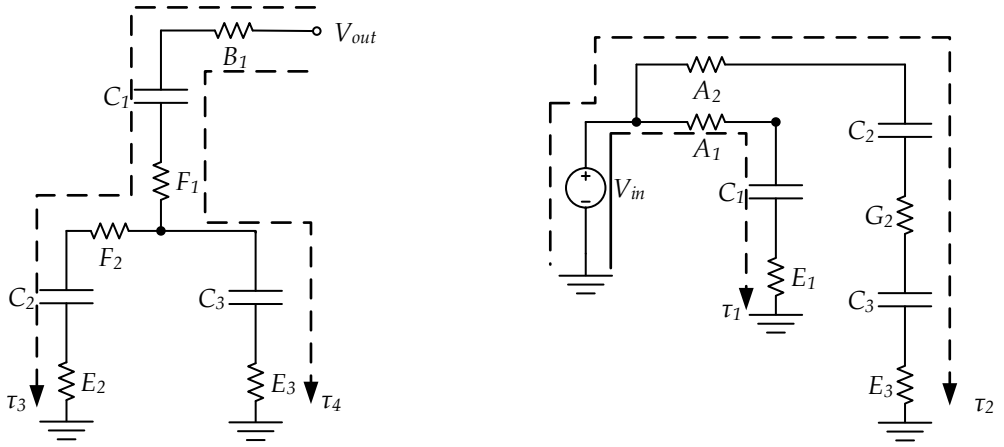
ϕ_1	ϕ_2
$A_1\ A_2\ A_3$	$B_1\ B_2\ B_3$
$E_1\ E_2\ E_3$	$E_1\ E_2\ E_3$

4.1.2.4 3/2 State

Lastly, on the 3/2 state, the active switches in each phase are shown in table 4.5. As in the 2/3 state, this analyses refers to a single switch in series with a capacitor of 333.33 pF. Thus, the total $R_{ON_{3/2}}$ (section 3.4.4 Eq. (3.29)) must be divided by the number of switches. The method using the slowest time constant of the circuit in each phase is applied again in this state.

Table 4.5: Active switches on the 3/2 state

ϕ_1	ϕ_2
$A_1\ A_2$	B_1
$E_1\ E_3$	$E_2\ E_3$
G_2	$F_1\ F_2$



(a) Phase 1 (b) Phase 2

Figure 4.3: Simplified schematic of the converter in the 3/2 state for the two phases

Figure 4.3 shows the 3/2 state with the R_{ON} from the active switches. The time constants of each phase are given by

$$\phi_1 : \begin{cases} \tau_3 = 4\,R_{ON}\,(C_1//C_2) = 2\,R_{ON}\,C_1 \\ \tau_4 = 3\,R_{ON}\,(C_1//C_3) = \frac{3}{2}\,R_{ON}\,C_1 \end{cases}$$
$$\phi_2 : \begin{cases} \tau_1 = 2\,R_{ON}\,C_1 \\ \tau_2 = 3\,R_{ON}\,(C_2//C_3) = \frac{3}{2}\,R_{ON}\,C_1 \end{cases} \tag{4.5}$$

The slowest time constants are τ_3 (ϕ_1) and τ_1 (ϕ_2). Therefore, the R_{ON} of each switch are given by

$$\begin{array}{lll} R_{ON_{A_1}} = \dfrac{R_{ON_{3/2}}}{2} & R_{ON_{E_1}} = \dfrac{R_{ON_{3/2}}}{2} & R_{ON_{F_1}} = \dfrac{R_{ON_{3/2}}}{4} \\ R_{ON_{A_2}} = \dfrac{2}{3}\,R_{ON_{3/2}} & R_{ON_{E_2}} = \dfrac{R_{ON_{3/2}}}{2} & R_{ON_{F_2}} = \dfrac{R_{ON_{3/2}}}{2} \\ R_{ON_{B_1}} = \dfrac{R_{ON_{3/2}}}{2} & R_{ON_{E_3}} = \dfrac{2}{3}\,R_{ON_{3/2}} & R_{ON_{G_2}} = \dfrac{2}{6}\,R_{ON_{3/2}} \end{array} \tag{4.6}$$

Again, notice that the switches F_1 and G_2 have two transistors for voltage protection reasons. And so their R_{ON} must be divided by two.

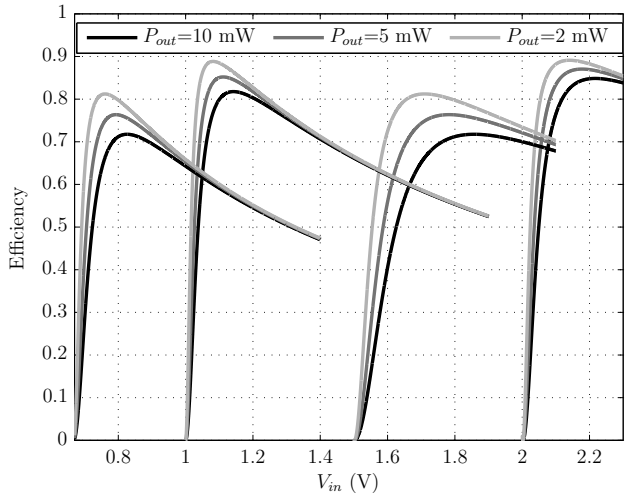
4.1.2.5 Overall Efficiency

In the previous sub-sections the choice of the transistors which implement the switches and the required R_{ON} value for a given frequency, flying capacitor, and technology (k_R, k_C) was carried out. In section 3.4 the relation between R_{ON}, W, and C_{GG} for each separated converter was analysed and showed that R_{ON} is inversely proportional to C_{GG} times a coefficient (3.5). Thus, each switch C_{GG} can be determined replacing (3.5) in (4.1), (4.3), (4.4), and (4.6). The effect of all parasitic gate capacitances is the sum of each individual C_{GG} which depends on V_{in}, V_{out}, F_{CLK}, P_{out} and *error*. Replacing the new equation in all the efficiency equations of the converters (2.18), (2.26) , (2.40), and (2.48) results η as function of V_{in}, V_{out}, *error*, P_{out} and F_{CLK}. This now takes into account the effect of the frequency in the parasitic capacitances of the switches. Replacing 2.11, 2.23[2], 2.33, and 2.45[2] in this new expression results in η in function of V_{in}, V_{out}, the parasitic capacitances of the flying capacitors, *error*, and P_{out}. This final equation describes the efficiency with the frequency adjusting to the value necessary to maintain a certain V_{out} (in this case of 1 V) and the extra power dissipated by the switches clock drivers due to this adjustment. Due to the large size of this equations they will not be shown and only relevant plots will be depicted.

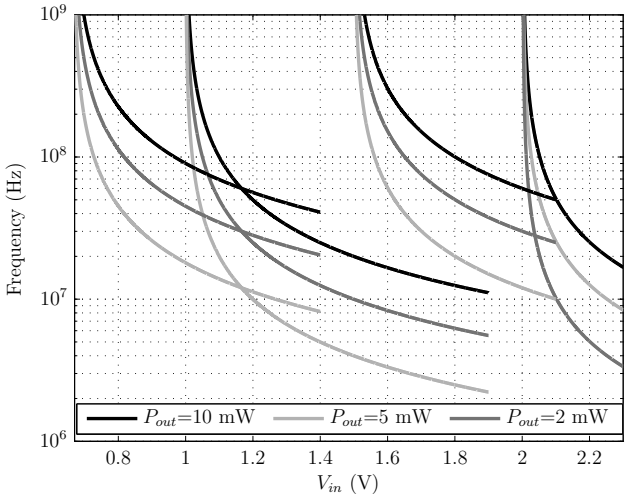
Figure 4.4(a) shows the plot of η as function of V_{in} for the four converters (1/2, 2/3, 1/1 and 3/2), with three different values of P_{out} (10, 5, and 2 mW), $V_{out} = 1$ V, settling error of 1%, $C_1 = 1$ nF (for the 1/1 and 1/2), $C_1 = C_2 = C_3 = 0.33$ nF (for the 2/3 and 3/2), and all the parasitic capacitances of the flying capacitors ($C_B = 0.59\%\ C_1$ and $C_T = 0.15\%\ C_1$),

[2]Considering parasitics capacitances from the flying capacitors.

accordingly to the nominal value of the flying capacitor. The plot shows the maximum achievable efficiency and the corresponding value of V_{in}. As P_{out} increases η decreases. This is consistent with the conclusions made until now - an increase in P_{out} results in an increase of P_{CLK} resulting in a decrease of η (section 3.4). Through this it is possible to determine the range of operation for each converter. Figure 4.4(b) shows the plot of the frequency 2.11, 2.23[3], 2.33, and 2.45[3] as function of V_{in} in the same conditions as the plot of the efficiency above. It is important to analyse simultaneously both of the plots to



(a) Efficiency as a function of V_{in}



(b) Frequency as a function of V_{in}

Figure 4.4: Plot of the proposed circuit efficiency and frequency regions as function of V_{in} with $V_{out} = 1$ V, settling error of 1%, $C_1 = 1$ nF (for the 1/1 and 1/2), $C_1 = C_2 = C_3 = 0.33$ nF (for the 2/3 and 3/2), and $C_B = 0.59\%\ C_1$ and $C_T = 0.15\%\ C_1$, accordingly to the nominal value of the flying capacitor

[3]Considering parasitics capacitances from the flying capacitors.

understand the frequencies regions of the converters.

Initially, the converter was to be design with a output power of 10 mW. However, this showed to be impractical. Establishing the limits of operation (V_{in}) of the four states is the first step towards the design of the proposed converter. By Analysing figure 4.4(a) the chosen limits were 2.08, 1.7, 1.05, and 0.75 V which correspond to the transition points where the η of the next state is higher than the previous state (except for the 3/2 state). These values result in maximum frequency values of 65, 150, 200, and 370 MHz. These frequency values are too high for the overall system because they result in a very large power dissipation for the clock drivers. Thus, new limits were chosen by limiting also the maximum frequency to 150 MHz. The new limits were 2.08, 1.7, 1.066, and 0.87 V which correspond to 65, 150, 150, and 150 MHz. Table 4.6 shows the values of R_{ON}, W, and $C_{GG,ON}$ using the equations described in section 4.1.2 and 3.2, for $P_{out} = 10$ mW, the chosen transition limits, and $error = 1\%$. The R_{ON} values are around 2 to 1 Ω, resulting in large transistors area ($\gg W$) and thus large gate parasitic capacitances ($\gg C_{GG}$). The switches with the smallest R_{ON} must be chosen to size the switches since they are shared by all the states - these are depicted in bold. There are C_{GG} values up to 3.2 pF. These, in simulations results, showed power consumptions of the clock drivers up to 5-6 mW. Remembering, that the output power is 10 mW and it must provide power for some of these clock circuits, along with the power drained from V_{in} to the rest of the clock circuits. P_{out} also has to provide power for the rest of the system, this will lead to values of efficiency under 50%. Moreover, notice that the power values do not take into account the shoot-through current

Table 4.6: Proposed converter R_{ON}, W, and $C_{GG,ON}$ of the switches in each state for $P_{out} =$ 10 mW, transition limits of 2.08, 1.7, 1.066, and 0.87 V (V_{in}), and $error = 1\%$

S	R_{ON} (Ω)				W (μm)				C_{GG} ON (pF)			
	1/2	2/3	1/1	3/2	1/2	2/3	1/1	3/2	1/2	2/3	1/1	3/2
A_1	2.6	1.1	**1.1**	1.1	921.0	2210.5	**2232.8**	2174.2	1.3	3.1	**3.2**	3.1
A_2	2.6	0	**1.1**	1.5	921.0	0	**2232.8**	1630.7	1.3	0	**3.2**	2.3
A_3	2.6	0	**1.1**	0	921.0	0	**2232.8**	0	1.3	0	**3.2**	0
B_1	2.6	1.1	**1.1**	1.1	921.0	2210.5	**2232.8**	2174.2	1.3	3.1	**3.2**	3.1
B_2	2.6	1.4	**1.1**	0	921.0	1657.9	**2232.8**	0	1.3	2.4	**3.2**	0
B_3	2.6	0	**1.1**	0	921.0	0	**2232.8**	0	1.3	0	**3.2**	0
D_1	**2.6**	0	0	0	**921.0**	0	0	0	**1.3**	0	0	0
D_2	**2.6**	0	0	0	**921.0**	0	0	0	**1.3**	0	0	0
D_3	**2.6**	0	0	0	**921.0**	0	0	0	**1.3**	0	0	0
E_1	2.6	1.1	**1.1**	1.1	196.7	472.0	**476.8**	464.3	0.3	0.6	**0.6**	0.6
E_2	2.6	1.4	**1.1**	1.1	196.7	354.0	**476.8**	464.3	0.3	0.5	**0.6**	0.6
E_3	2.6	1.1	**1.1**	1.5	196.7	472.0	**476.8**	348.2	0.3	0.6	**0.6**	0.5
F_1	0	**0.5**	0	0.6	0	**944.0**	0	928.6	0	**1.3**	0	1.3
F_2	0	**1.1**	0	1.1	0	**472.0**	0	464.3	0	**0.6**	0	0.6
G_2	0	**0.7**	0	0.7	0	**708.0**	0	696.4	0	**1.0**	0	0.9

of the inverters, as well as the power for the remaining system, which at frequencies of 100/150 MHz has a considerable value.

With this in mind and remembering that the power driven by the clock drivers decrease quadratically with P_{out} (section 3.4.5), a 2 mW output power was chosen and the choice of the limits was again carried out. There are some restraints that were not explained until now. Due to the clock swing voltage ($V_{in} \rightarrow 1$ V) of the A switches in the 2/3 state, for safety reasons (section 4.1.1), the V_{eff} of the switches drops bellow 1 V. Meaning that the projected R_{ON} will be in fact higher, thus leading to lower efficiencies. The same problem is presented in the 3/2 state when $V_{in} < 1$ V and affects both A and B switches. This could easy be solved placing a NMOS transistor in parallel, although it would bring problems of gate oxide breakdown when operating in the 1/2 and 2/3 sate. This mean that the theoretical curves of η (Fig. 4.4(a)) start to fail. Therefore, the transition limits between states were chose from figure 4.4(a) as a starting point and then adjusted through simulation derived by spectre. The chosen values were 2.05, 1.7, 1.05 [4], and 0.85 V. This corresponds to maximum frequency values of 20, 33, 45, and 50 MHz. Table 4.7 shows the values of R_{ON}, W, and $C_{GG,ON}$ using the equations described in section 4.1.2 and 3.2, for for $P_{out} = 2$ mW, the chosen transition limits, and $error = 1\%$. The R_{ON} values are now around 3 to 8 Ω, resulting in transistors almost ten time smaller than the previous case ($P_{out} = 10$ mW). The average value of the parasitic capacitances is approximately

Table 4.7: Proposed converter R_{ON}, W, and $C_{GG,ON}$ of the switches in each state for $P_{out} = 2$ mW, transition limits of 2.05, 1.7, 1.05[4], and 0.85 V (V_{in}), and $error = 1\%$

S	R_{ON} (Ω)				W (μm)				C_{GG} ON (pF)			
	1/2	2/3	1/1	3/2	1/2	2/3	1/1	3/2	1/2	2/3	1/1	3/2
A_1	8.1	5.4	8.1	**5.0**	294.7	442.1	294.7	**482.3**	0.4	0.6	0.4	**0.7**
A_2	8.1	0	8.1	**6.6**	294.7	0	294.7	**361.7**	0.4	0	0.4	**0.5**
A_3	**8.1**	0	**8.1**	0	**294.7**	0	**294.7**	0	**0.4**	0	**0.4**	0
B_1	8.1	5.4	8.1	**5.0**	294.7	442.1	294.7	**482.3**	0.4	0.6	0.4	**0.7**
B_2	8.1	**7.2**	8.1	0	294.7	**331.6**	294.7	0	0.4	**0.5**	0.4	0
B_3	**8.1**	0	**8.1**	0	**294.7**	0	**294.7**	0	**0.4**	0	**0.4**	0
D_1	**8.1**	0	0	0	**294.7**	0	0	0	**0.4**	0	0	0
D_2	**8.1**	0	0	0	**294.7**	0	0	0	**0.4**	0	0	0
D_3	**8.1**	0	0	0	**294.7**	0	0	0	**0.4**	0	0	0
E_1	8.1	5.4	8.1	**5.0**	62.9	94.4	62.9	**103.0**	0.1	0.1	0.1	**0.1**
E_2	8.1	7.2	8.1	**5.0**	62.9	70.8	62.9	**103.0**	0.08	0.1	0.1	**0.1**
E_3	8.1	**5.4**	8.1	6.6	62.9	**94.4**	62.9	77.2	0.08	**0.1**	0.1	0.1
F_1	0	2.7	0	**2.5**	0	188.8	0	**206.0**	0	0.3	0	**0.3**
F_2	0	5.4	0	**5.0**	0	94.4	0	**103.0**	0	0.1	0	**0.1**
G_2	0	3.6	0	**3.3**	0	141.6	0	**154.5**	0	0.1	0	**0.2**

[4]Simulation results showed that it is preferable to size the transistors as if the limit were 1.1 V and increase frequency to 45 MHz in order to work at 1.05 V than increase the size of the switches

500 fF. The switch with the smallest R_{ON} determine the sizing of the transistors (W, with $L = L_{min} = 120$ nm), which are depicted in bold.

Figure 4.5 shows the plot of the theoretical efficiency (solid lines) and the simulation results derived from spectre (markers) for for $P_{out} = 2$ mW, $V_{out} = 1$ V, $error = 1\%$, and with the sizing of the transistors (W) done through the bold numbers in table 4.7. As expected the simulation results show efficiencies bellow the theoretical plot. Moreover, in states 2/3 and 3/2 it is clear the effect of $V_{eff} < 1$. Table 4.8 summarizes the transition voltages and the corresponding frequency and efficiency for the simulation results. Remembering, that these results only count with the proposed circuit and the drivers of the switches (which will be explain later in section 4.2.3). The final results with the overall system will be shown in the next chapter.

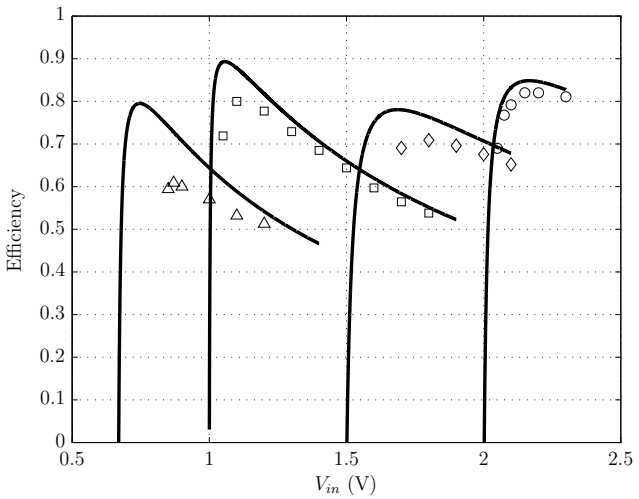


Figure 4.5: η in function of V_{in} for $P_{out} = 2$ mW, $V_{out} = 1$ V and $error = 1\%$. Simulation results derived by spectre are displayed in markers

Table 4.8: Operation region and the corresponding efficiency and frequency of the proposed converter for $P_{out} = 2$ mW, this results were taken by simulation derived by spectre

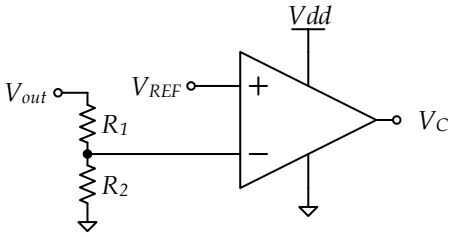
		1/2	2/3	1/1	3/2
V_{in} (V)	Begin	2.3	2.05	1.7	1.05
	Opt.	2.15	1.8	1.1	0.87
	End	2.05	1.7	1.05	0.85
Freq. (MHz)	Begin	4	11	3	16
	Opt.	7	21	20	35
	End	20	33	45	50
η (%)	Begin	81.8	66.4	56.4	55.1
	Opt.	82.0	70.9	80.0	60.9
	End	69.0	69.1	71.9	59.4

4.2 The Overall System

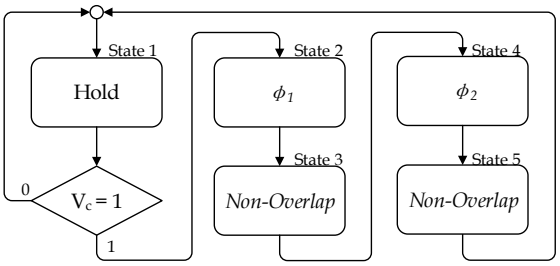
4.2.1 Clock and Phase Generator

The generation of the two clock signals which define the phases ϕ_1 and ϕ_2 needed for the proposed converter is carried out by the clock and phase generator circuit. This is composed by an Asynchronous state machine (ASM) based on the phase controller implemented in [6] and a comparator that provides a control signal (V_c) which produces a logic 1 if V_{out} decreases below 1 V or logic 0 if $V_{out} > 1$ V. This way, the frequency at which phases ϕ_1 and ϕ_2 occur depends on the value of the output voltage - Voltage-controlled oscillator (VCO). Figure 4.6(a) shows the circuit that performs this comparison where V_{REF} is a voltage signal of 500 mV produced by a Bandgap circuit that will be later explained. A resistive ladder $R_1 = R_2 = 1$ MΩ is used to down converter V_{out} from 1 V to 500 mV.

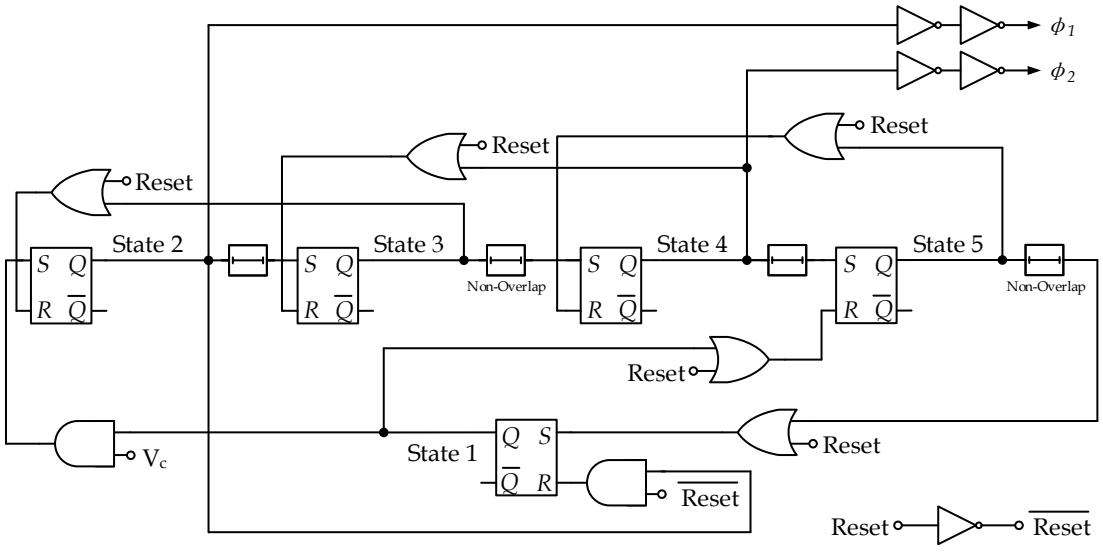
The ASM operation mode can be seen in figure 4.6(b) in form of a state diagram. It initiates in state 1 - *holding state*. As the name imply, this state does not do anything until the output voltage becomes smaller than 1 V. At that time, the ASM changes to state 2



(a) Schematic of the circuit responsible for the comparison



(b) State diagram of the clock generator



(c) Simplified schematics

Figure 4.6: Clock phase ($\phi_{1,2}$) generator

through the AND gate. This state produces a 1 V pulse (ϕ_1) whose width depends on the following delay circuit. At the rising edge of the delayed ϕ_1, the ASM shifts to state 3. In this state there is a 1 ns delay to avoid overlap between the clock phases. In the rising edge of this 1 ns delayed signal, the ASM shifts to state 4 where it produces ϕ_2 and performs the same operation as in state 2. State 5 is equal to state 3 and with the same objective. This will produce one period of two square waves in phase opposition, ϕ_1 and ϕ_2, where their duration can be controlled according to the delay of each pulse. Moreover, this delay will define the maximum frequency that the phase clock signals can achieve in a given state of the converter operation. The schematics of the circuit that implements this state diagram is depicted in 4.6(c).

The states are implemented by S-R latches. These are activated by the *Set* signal which changes the output Q from 0 to 1. This in turn, activates the *Reset* signal of the previous latch, causing its output to change from 1 to zero thus completing the state. V_c is the output of a comparator that indicates if V_{out} is above/below of 1 V.

Figure 4.7 shows the two clock signals generated by the generator. It is possible to see the time space between the falling edge of ϕ_2 and the rising edge of the ϕ_1 where both are at 0 V - non-overlap. This plot was taken from the system simulation at the 1/2 state in which the frequency of both is approximately at 23 MHz.

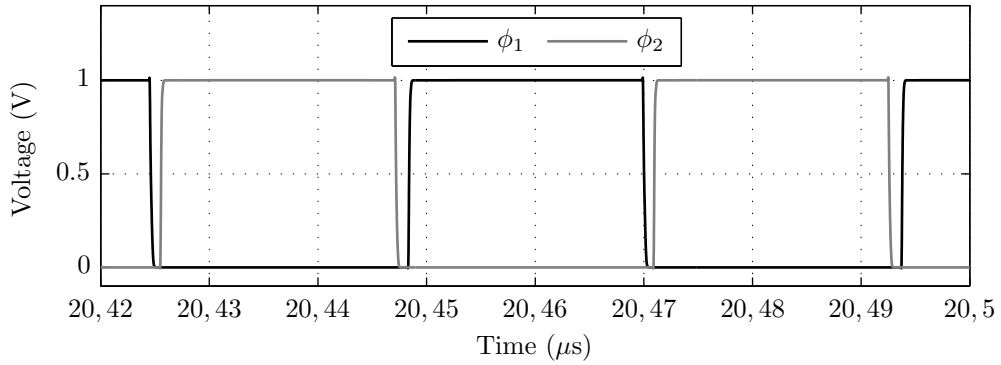
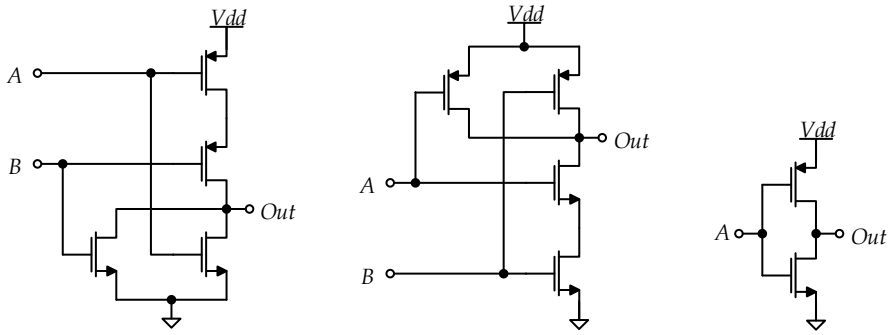


Figure 4.7: Simulation results of the clock generator circuit (Fig. 4.6(c)) at the 1/2 state

4.2.1.1 Logic Gates

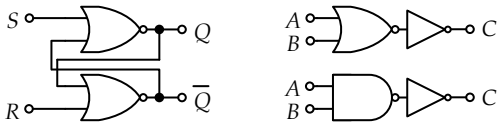
Logic operations are used in the clock generator to perform its task and change from one state to another. As shown in 4.6(c) *S-R* latches, *AND*, *OR* and *NOT* gates are used. These are implemented by using combinations of *NOR*, *NAND* and *NOT* gates. Figures 4.8 show the simplified schematic of these gates. All the logic gates are sized with the minimum length (L) and W (for the NMOS) allowed by the technology, in order to reduced the area and power dissipation. Thus, all the *NOR* (Fig. 4.8(a)), *NAND* (Fig. 4.8(b)) and *NOT* gates (Fig. 4.8(c)) are sized with $(W/L)_{\text{NMOS}}$ of 0.16/0.12 μm and $(W/L)_{\text{PMOS}}$ of 0.75/0.12 μm unless otherwise stated. Only the last output inverter of ϕ_1 and ϕ_2 are sized with 2 times de minimum size.



(a) NOR gate (b) NAND gate (c) NOT gate

Figure 4.8: Simplified schematic of the logic gates used in the generator circuit. The PMOS and NMOS with undefined bulk have their bulk connected do V_{DD} and ground, respectively

Figures 4.9(a) and 4.9(b) show the logic gates implemented by means of *NOR*, *NAND* and *NOT* gates, described in the previous paragraph with the corresponding sizing.



(a) Schematic of the S-R latch (b) Top: OR gate, Bottom: AND gate

Figure 4.9: Logic gates used in the generator circuit

4.2.1.2 Delay Circuit

The maximum frequency of operation depends on the active converter state (1/2, 2/3, 1/1, and 3/2). This is controlled by the delay circuit used in states 2 an 4. There are be four different times delays which are implemented by the circuit depicted in figure 4.10 [6]. Where the delay time is basically defined by an *RC* constant between M_4 (act as a resistor) and the MOS capacitor M_8, M_{11}, M_{14} and M_{17}. According to the actual state, the transmission gates controls which capacitor is connected to node. These capacitors have different values for each state, thus defines distinct delay values. Table 4.9 shows the transistor size.

Figure 4.11 shows a simulation result of the time delay for the 1/2 state. The delay is approximately 22 ns, notice that the delay provided by this circuit is only applied to the rising edge of its input signal.

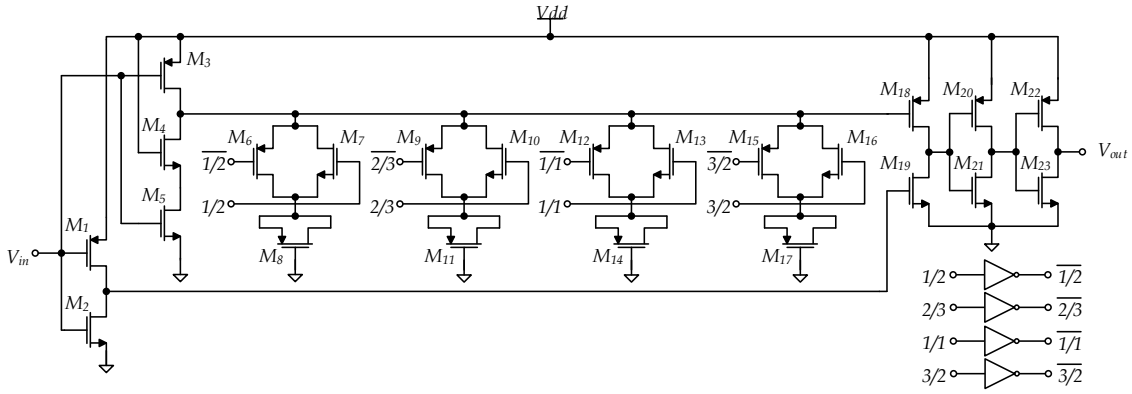


Figure 4.10: Schematic of the 1 ns delay circuit, PMOS and NMOS with undefined bulk have their bulk connected do V_{DD} and ground, respectively

Table 4.9: Transistor sizes in the delay circuits

Transistor	Size (μm)
M_1, M_3, M_6, M_9, M_{12}, M_{15}, M_{18}, M_{20}, M_{22}	0.75/0.12
M_2, M_5, M_7, M_{10}, M_{13}, M_{16}, M_{19}, M_{21}, M_{23}	0.16/0.12
M_4	0.16/50
M_8	10.9/10.9
M_{11}	4/4
M_{14}	2/2
M_{17}	0.7/0.7

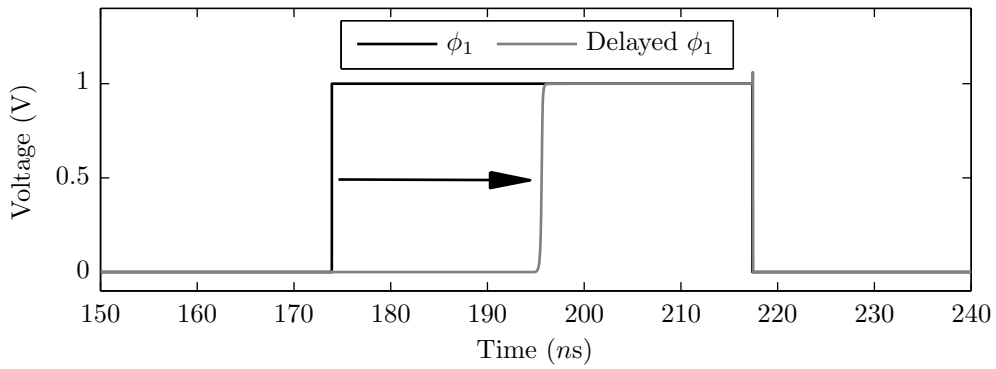


Figure 4.11: Simulation results of the delay circuit for the 1/2 state with a time delay of, approximately, 22 ns

The delay circuit used to avoid the overlap between the clock signals is shown in Fig. 4.12. A safety margin of 1 ns between the two clock signals was chosen. Its operation is equal to the previous delay circuit, but with only one MOS capacitor since it has always the same delay independently of the converter state. The transistors M_4 and M_6 are sized with (W/L) of 8/0.12 and with 0.75/0.12 μm. All the others transistor sizes are equal to the ones in the previous delay circuit.

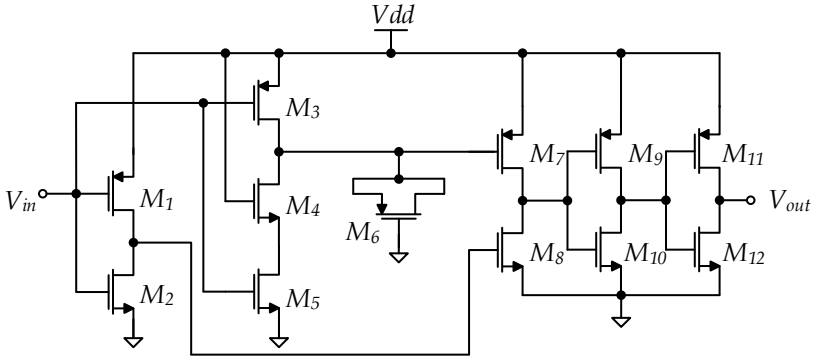


Figure 4.12: Schematic of the delay circuit. PMOS and NMOS with undefined bulk have their bulk connected do V_{DD} and ground, respectively

4.2.1.3 Comparator

The comparator used to generate the control signal V_c (Fig. 4.6(a)) is depicted in figure 4.13. It is equal to the one described in [6]. This has enable (*en*) feature that is not used in this work once there is no extra clock signal. Thus *en* is always connected to V_{DD}.

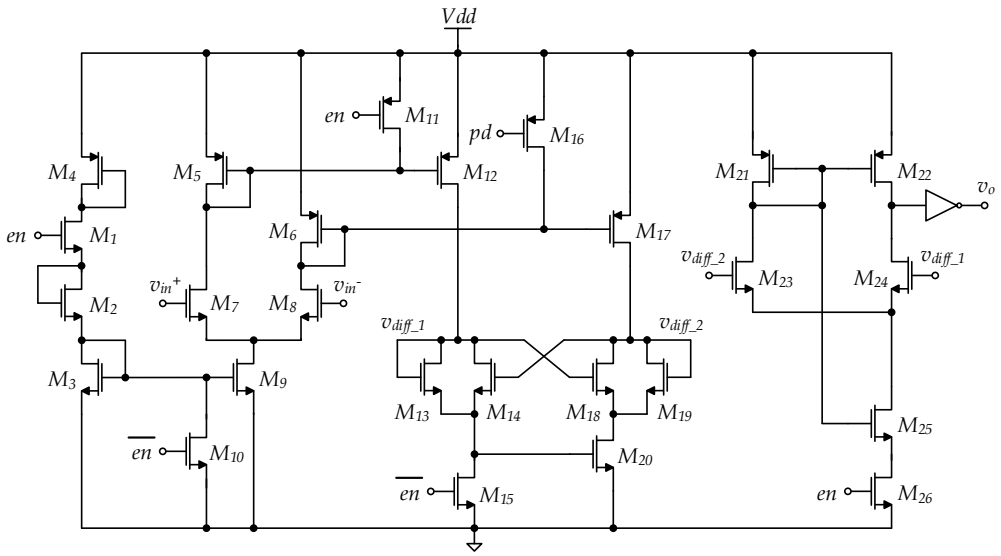


Figure 4.13: Schematic of the comparator circuit. PMOS and NMOS with undefined bulk have their bulk connected tdo V_{DD} and ground, respectively

4.2.2 Converter State Controller

The active converter state (1/2, 2/3, 1/1, or 3/2) is defined by the state controller converter. The state is determined by the voltage of the supercapacitor and by the operation voltage limits of each state converter, which were previously defined in section 4.1.2.5. Figure 4.14 shows a simplified block diagram of the controller. Resistive ladders are used to scale-down V_{in} and V_{REF} (which is generated by a Bandgap circuit) to perform the comparison between V_{in} and the transition voltage limits of the proposed circuit. A voltage level selector, which is basically a set of transmission gates controlled by an logic circuit, controls the voltage limit which is at the input of the comparator, according with the current state. The comparator compares the two voltages from both resistive ladders, and acts on the state machine to change state or remain in the current state.

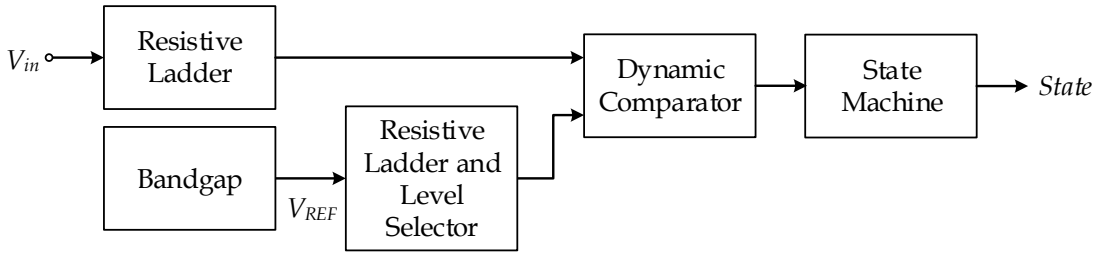


Figure 4.14: State diagram of the converter state controller

4.2.2.1 Resistive Ladder and Voltage Level Selector

Figure 4.15(d) shows the resistive ladder used to produce the different voltage levels that determine the transitions between the different converters. There are three transition voltages between the four states of the converter. These transition voltage levels are defined using a resistive ladder (R_1, R_2 ..., R_6). To avoid problems of multiple transitions around the voltage limits, extra voltages transitions are added to create *hysteresis*. In the 1/2 state, there is only one limit since there is no upper state. This limit is represented by V_{12B} (where "B" means bottom) in the resistive ladder. The 2/3 and the 1/1 states have a top (V_{23T} and V_{11T}) and a bottom limit (V_{23B} and V_{11B}), since these can change to an upper or inferior state. Lastly, the 3/2 state only has a top limit (V_{32T}) as there is no state after. The difference between the voltages $V_{1/2B}$ and $V_{2/3T}$, and so on, establish the hysteresis voltage.

The output voltage of the Bandgap circuit is 500 mV (V_{REF}). Thus, the voltage limits (2.05, 1.7, and 1.05) where divide by 4.5 to be within the 500 mV range. The hysteresis factor chosen was 10 mV, since higher values, when multiplied with 4.5, would increase too much the upper voltage transitions. Table 4.10 present all the voltage transitions values divided by the 4.5 factor.

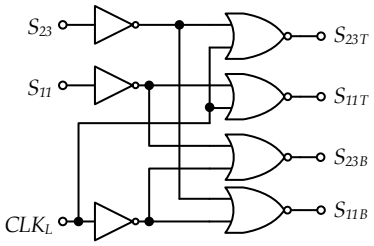
Transmission gates 4.15(c) are used to perform the selection of the voltages in the resistive ladder to the input of the comparator, V_{LV}. The ones without hysteresis, with

Table 4.10: Voltage levels of the restive ladder divided by a factor of 4.5

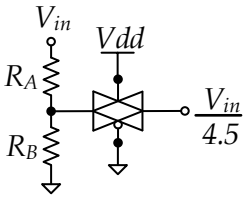
States \ V_{LV} (mV)	Top	Bot.
1/2	-	456
2/3	466	378
1/1	388	233
3/2	243	-

only one limit (1/2 and 3/2), are controlled by the output voltage of the state machine. The other two states (2/3 and 1/1) have a small logic circuit 4.15(a) that controls which transmission gate is activated depending on the active state and the value of the clock signal CLK_L, which will be later explained. The size of all the transmission gates is, in μm, NMOS 0.16/0.12 and PMOS 0.75/0.12.

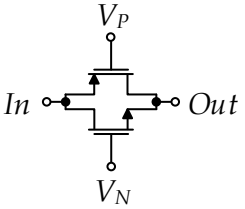
Lastly, the input voltage must also be divided by the 4.5 factor for the comparison to work. This is done through another restive ladder 4.15(b) with two resistors R_A and R_B. The two resistive ladders most have an impedance seen from the input of the comparator



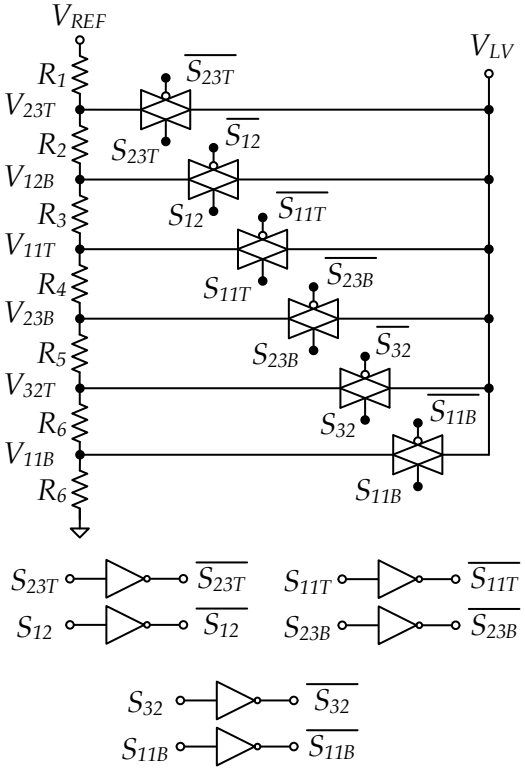
(a) Logic selector



(b) V_{in} resistive ladder



(c) CMOS transmission gate



(d) Resistive ladder of the limits selector

Figure 4.15: Simplified schematics of the V_{in} and V_{LV} resistive ladders. PMOS and NMOS with undefined bulk have their bulk connected do V_{DD} and ground, respectively

as close as possible. This helps to mitigate the errors on the comparison due to the kickback noise. Moreover, as the total value of the resistors decreases the effect of the kickback noise is again reduced. However, this brings problems of static power consumption. With this trade-off into account, the total budget chosen for the V_{REF} resistive ladder was of 500 KΩ. The impedance seen from the comparator changes accordingly to the voltage limit. To match as close as possible the resistive ladder impedance of V_{in} the budget was defined by the mean square of the impedance seen from each voltage limits of the V_{REF} ladder (V_{23T}, V_{12B},...,V_{11B}). Also, a dummy transmission gate was added with the same size as the ones of the V_{REF} ladder. The resistors values for both resistive ladders are

$$\begin{aligned} &R_1 = 34\ K\Omega \quad R_2 = 10\ K\Omega \quad R_3 = 68\ K\Omega \quad R_4 = 10\ K\Omega \quad R_5 = 135\ K\Omega \\ &R_6 = 10\ K\Omega \quad R_7 = 233\ K\Omega \quad R_A = 375\ K\Omega \quad R_B = 107\ K\Omega \end{aligned} \tag{4.7}$$

4.2.2.2 Conventional Dynamic Comparator

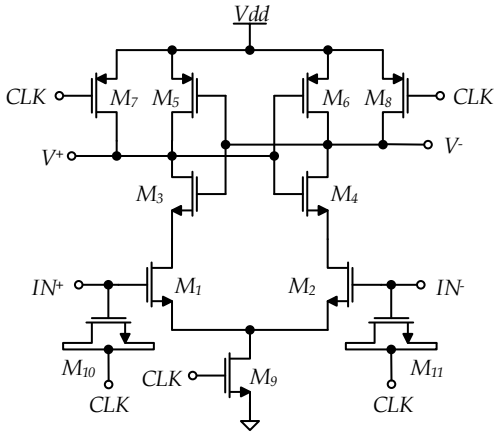


Figure 4.16: Simplified schematic of the conventional dynamic comparator. PMOS and NMOS with undefined bulk have their bulk connected do V_{DD} and ground, respectively

The simplified schematics of the *Conventional Dynamic Comparator* [17, 18, 19] is shown in figure 4.16. It is known by its high input impedance, rail-to-rail output swing and no static power consumption [17]. The comparison is divided in two phases: *Reset phase* and *Comparison phase*. In the *Reset phase*, $CLK = 0$ and so M_9 is OFF and $M_{7,8}$ are ON, thus the output nodes V^+ and V^- are charged to V_{DD}. This provides the start condition for the next phase of the comparison. Note that in this configuration $M_{5,6}$ are OFF and $M_{3,4}$ are ON; In the *Comparison phase* $CLK = V_{DD}$ which turns OFF $M_{7,8}$ and turns ON M_9. With this, V^+ and V^- start to discharge (from its previous value of V_{DD}) due to the current flowing through the transistors $M_{3,4}$ and $M_{1,2}$. Both discharges at different rates depending on the voltage of inputs in the differential pair (IN^+ and IN^-). Assuming that $V_{IN^-} < V_{IN^+}$, V^+ discharges faster than V^- because the current flowing through the transistor M_1 is larger

than the one flowing through M_2. When the V^+ discharges to $V_{DD} - |V_{thp}|$ before V^-, the corresponding PMOS transistor M_6 will turn ON initiating the latch regeneration caused by the back-to-back inverters ($M_{3,5}$ and $M_{4,6}$). By that, V^- pulls to V_{DD} and V^+ discharges to ground. If $V_{IN^-} > V_{IN^+}$, the circuit works vice versa.

Transistors $M_{10,11}$ are used to reduced the kickback noise. This kickback noise comes from the leaking current caused by the parasitic capacitance between the drain and gate (C_{DG}) due to the large current flowing through $M_{1,2}$ when $CLK = 1$ V. Thus, $M_{10,11}$, which are sized with half the size of $M_{1,2}$, act like a capacitor that injects a current that helps to cancel this leaking current. Simulation results showed a significantly reduction of the kickback noise by implying this technique. Table 4.11 shows the transistor sizes.

Table 4.11: Transistor dimensions used in the implemented conventional dynamic comparator

Transistor	Size (μm)
M_1, M_2, M_3, M_4, M_9	1/0.12
M_5, M_6, M_7, M_8	4.7/0.12
M_{10}, M_{11}	0.5/0.12

When $CLK = 0$ the comparator outputs V^+ and V^- are charged to V_{DD} and does not depend either if $V^- > V^+$ or counter wise. This could cause errors of comparison to the state machine that receives a logic 1 that is not a result of a comparison. Therefore a S-R latch (Fig. 4.9(a)) is connected at the outputs of the comparator to prevent these errors (Fig. 4.17). The $V_{in}/4.5$ is connected to the IN^+ and the V_{LVL} to the IN^- of the comparator. This way, the final output of the comparator (V_C), only is logic 1 when the divided V_{in} voltage is below the V_{LVL}.

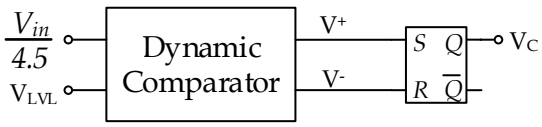


Figure 4.17: Comparator followed by a S-R latch

4.2.2.3 Bandgap

Both the comparator seen in section 4.2.1.3 and the dynamic comparator (seen in section 4.2.2.2) need a stable reference voltage to perform a comparison. This is done through the implementation of a *Bandgap* circuit. Figure 4.18 show the schematics of a *Bandgap* circuit which was developed in [20]. The working principle of this circuit is beyond the aim of this work and a detail analysis can be seen in [20]. The resistance R_{ladder} refers to

the resistive ladder that sets the voltage transitions (Fig. 4.15(d)). A MOS capacitor (M_{10}) of 500 fF is used to decrease the ripple of V_{REF}.

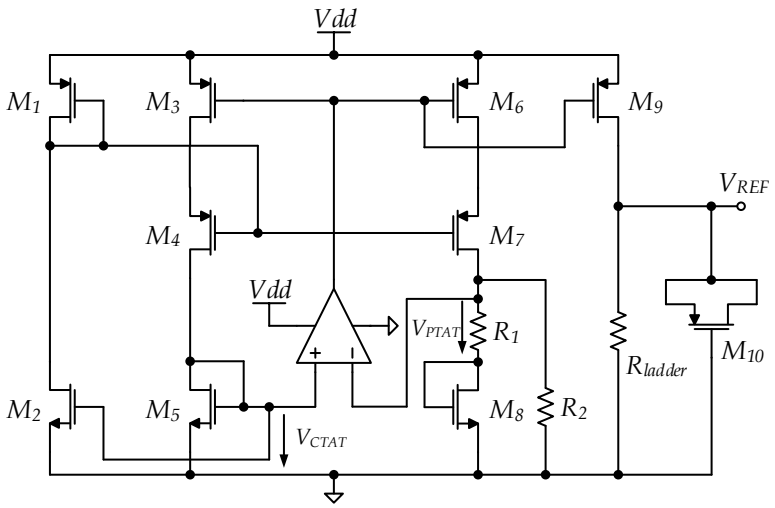


Figure 4.18: Schematic of the Bandgap circuit. PMOS and NMOS with undefined bulk have their bulk connected tdo V_{DD} and ground, respectively

Figure 4.19 shows the schematics of the *Operational Transconductance Amplifier* used in the Bandgap circuit.

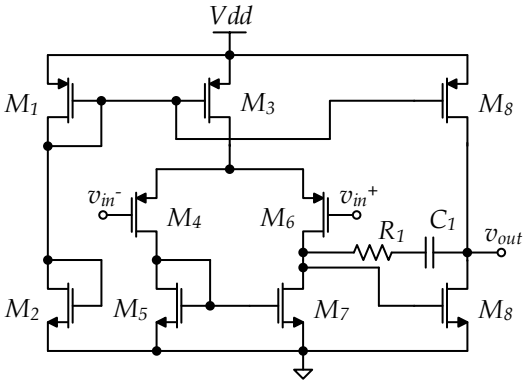


Figure 4.19: Schematic of the OPAMP circuit. PMOS and NMOS with undefined bulk have their bulk connected tdo V_{DD} and ground, respectively

4.2.2.4 State Machine

Before entering in the details of the state machine, it is important to explain why there are three different clock signals (CLK_L, CLK_C, and CLK_S). The controller needs to periodically check if it is time to change or not from the current state. This is triggered through the rising edge of ϕ_1 from the clock generator (section 4.2.1). It is not necessary to check in every rising edge of ϕ_1 if it is necessary to change state since the input voltage of the supercapacitor changes slowly. With this in mind, a new clock signal (CLK_S) was created,

which corresponds to ϕ_1 divided by 8 (dividing it further would not result in a significant power reduction). This way, the state controller will initiate its operation after 8 rising edges of ϕ_1. Moreover, notice that when the converter gets closer to the transition voltages, the rising edge of ϕ_1 will occur more often and so the state controller will also check more often if it is time to change than when V_{in} is far from the voltage transitions. This greatly reduces the power consumption of the controller and the associated circuits such as the comparator.

In order to allow the voltage in the resistive divider enough time to settle (V_{LV}) as well as for have enough time for the response from the comparator (V_C), two extra clocks were created - CLK_C and CLK_L. The first, CLK_C, is CLK_S divided by two and is used as the clock signal of the comparator. The second, CLK_L, is CLK_C divided by two, and it is used to control V_{LV} of the resistive ladder. Figure 4.20 shows simulation results derived by spectre of the three clock signals (the circuits used for generate these signals will be explained later). When CLK_L is at logic 1, V_{LV} is, according to the current state, at the down voltage level. When CLK_C rises to logic 1 the comparator is activated and performs the comparison. Finally, only when the CLK_S is at logic 1 at the same time as the previous signals, the state machine "sees" if it must hold on the current state or rather change to the down state. The same procedure is repeated for the upper limits when CLK_L is at logic 0.

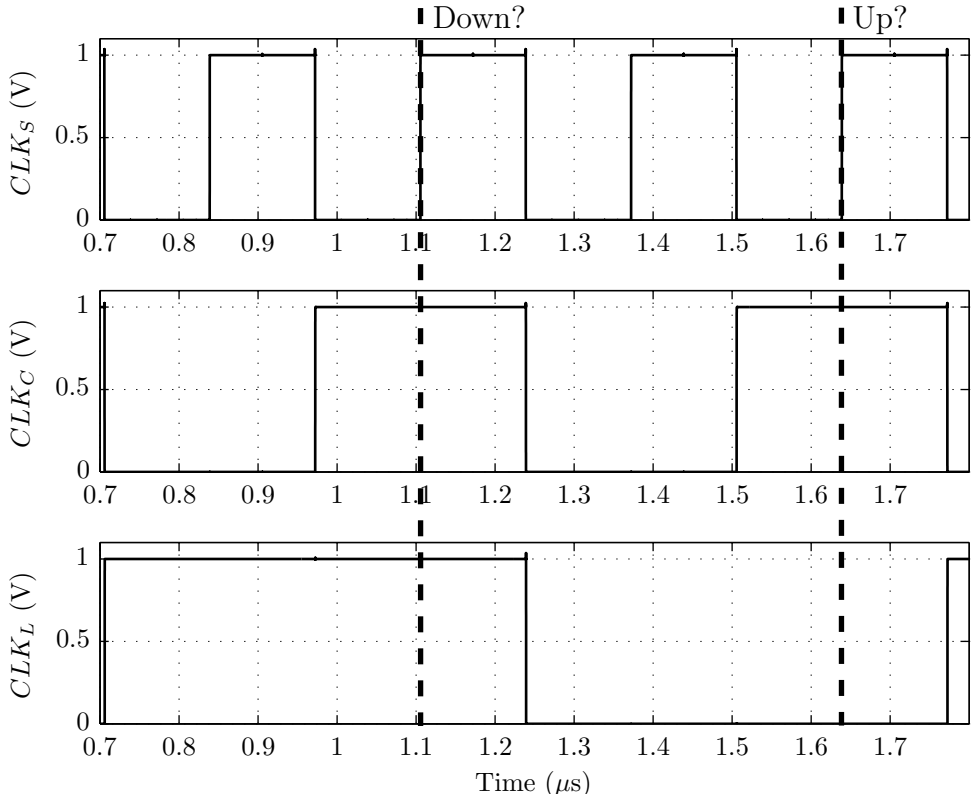
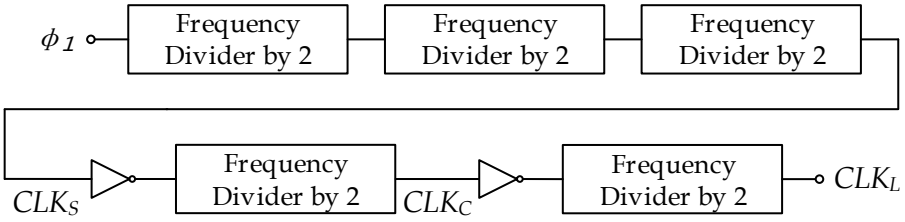
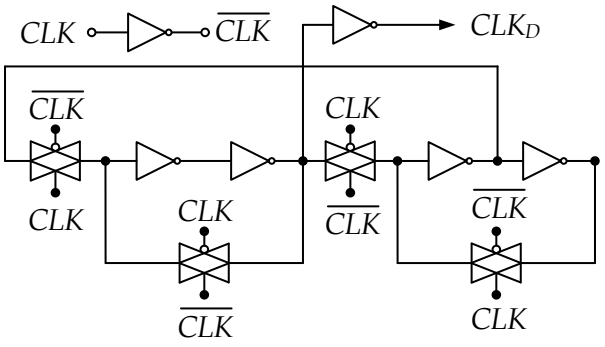


Figure 4.20: Simulation results derived by spectre of the three clock signals $CLK_{S,C,L}$



(a) Generation of $CLK_{S,C,L}$



(b) Frequency divider by two

Figure 4.21: Simplified schematics the divider by two circuit and the generation of the three clock signals $CLK_{S,C,L}$

Figure 4.21(a) shows how the three clock signals are generated through ϕ_1. The frequency dividers by two are implemented through the circuit depicted in figure 4.21(b). Their operation is quite simple: assuming that CLK_D starts at a logic 1 and $CLK = 0$ V then, when CLK changes to logic 1 CLK_D is forced to logic 0 by the signal drained between the two inverters from the second block. When CLK returns to zero CLK_D holds the logic 0. Finally, CLK_D is forced to 1 when CLK goes back to 1. This way CLK_D is a logic 1 for two pulses of CLK and a logic 0 for other two pulses of CLK - the frequency is divided by two. The transmission gates (Fig. 4.15(c)) are implemented with NMOS 0.16/0.12 and PMOS 0.75/0.12, in μm.

The state machine is the core of the state controller. It is responsible for defining the current state as well as decide if it has to change based on the receiving information of the circuits above described. Figure 4.22 shows a simplified state diagram of the state machine. It initiates in state 1/1 to perform the start-up of the circuit. Assuming a start position from state 1/2, it holds in this until $V_{in} < V_{LV}$, which in this state is 456 mV (2.05 V). When V_{in} is below this bottom limit, the state machine changes to the 2/3 state where the top and bottom limit changes to 466 mV (hysteresis) and 378 mV (1.7 V), respectively. From this point the machine can return to the 1/2 state (Up) or change to the next state (Down), 1/1 state, when V_{in} is above the top limit or below the bottom limit. The same procedure is repeated for the 1/1 state with the corresponding top and bottom limits of 388 mV (Hysteresis) and 233 mV (1.05 V), respectively. Lastly, in the 3/2 state there is no further state, thus it can only return to the previous state when V_{in} increases above the

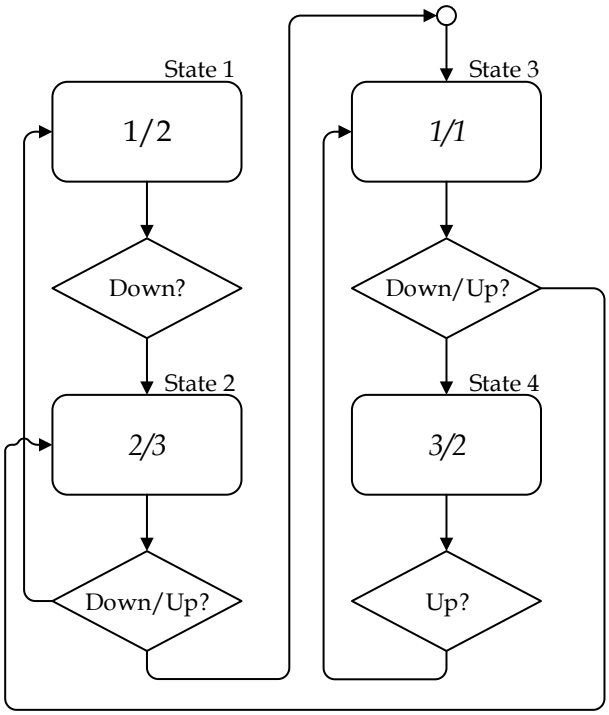


Figure 4.22: State diagram of the state machine from the state controller

243 mV (1.05 plus hysteresis). This way, the converter will change states when either the supercacitor discharges or charges.

Figure 4.23 shows the simplified schematics that implements the previous state diagram. The states are implemented by S-R latches such as the states of clock generator. The logic circuits Down, Down/UP, and UP are responsible for the decision of the transition of state. Table 4.12 shows the truth table of their logic operation. These receive four input signals - CLK_L, CLK_C, CLK_S, and V_C. When all clock signals are at the logic 1, means the state machine will analyse if it must go down or hold according with the value of V_C. If it is 0, then $V_{in} > V_{LV}$ and the state machine hold until the next verification. If it is 1, then the logic output down is activated which enable the set of the next S-R latch from the next state. When comparing the top limit ($CKL_L = 0$ and $CKL_{C,S} = 1$) and V_C is 0 means that $V_{in} > V_{LV}$. Thus, the up output of the logic circuit is activated which enable the set of S-R latch of the previous state and the reset of the current S-R latch. The output of all other possible input combinations produce a logic 0. The circuits that implement these logic circuits are depicted in figures 4.24.

Table 4.12: Truth table of the up/down logic

CLK_L	CLK_C	CLK_S	V_C	Up	Down
1	1	1	1	0	1
0	1	1	0	1	0

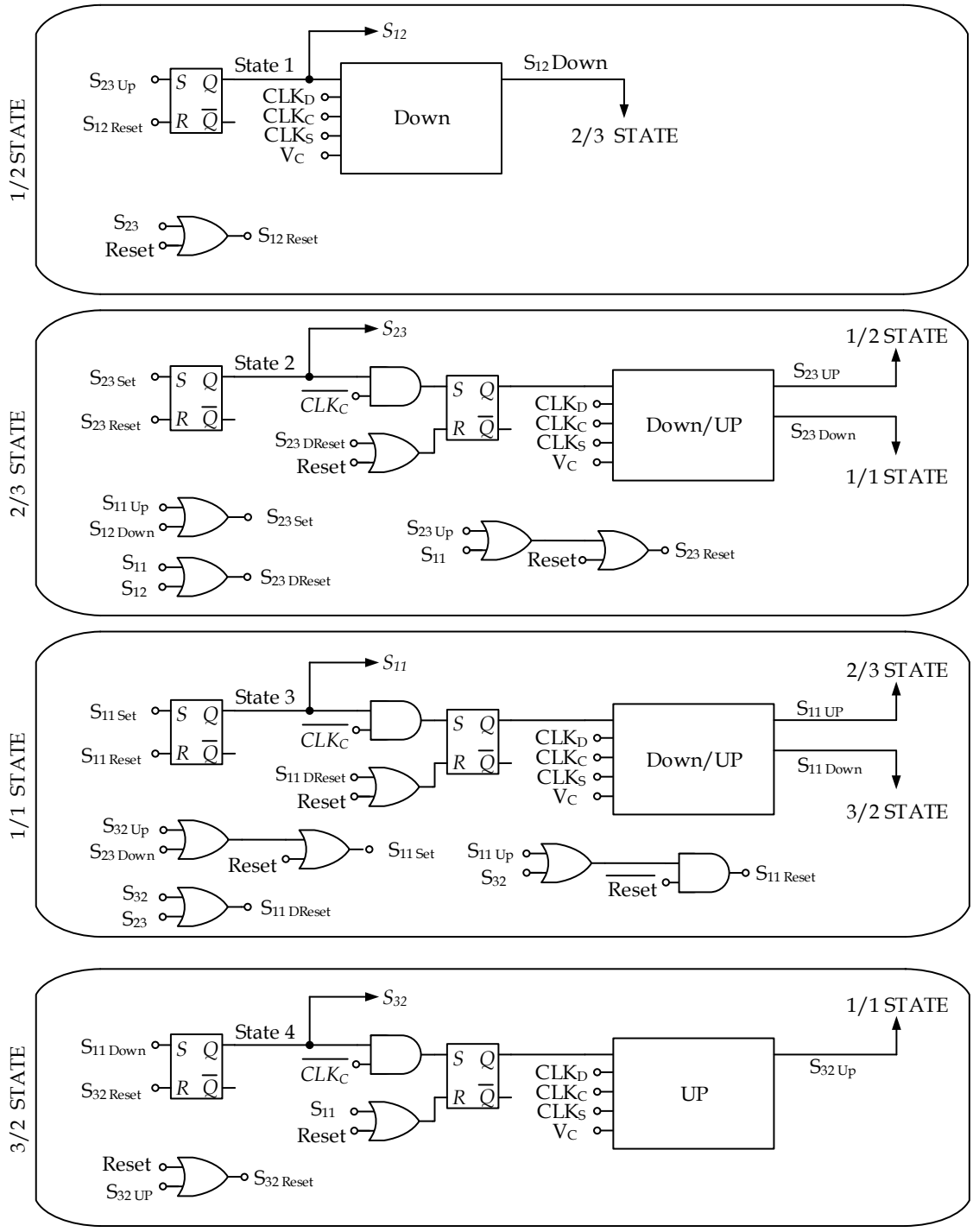
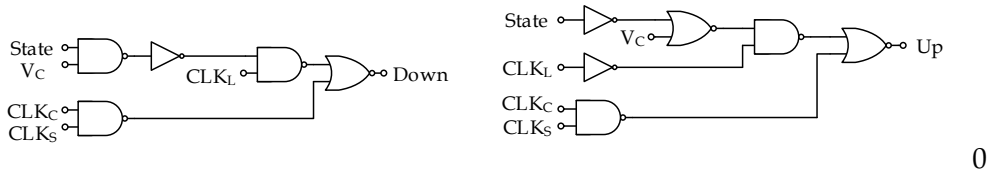


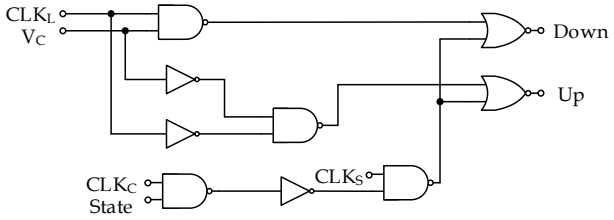
Figure 4.23: Simplified schematics of the state controller

When there is a transition and a new state is activated it is necessary to ensure that the comparison used to activate this transition is not used again in the new state, thus avoiding it to automatically skip the new state. To this end, an *AND* gate is used to compare the new state with $\overline{CLK_C}$ - is activated when $CLK_C = 0$. By that time, it means that the comparison is finished and a new one can take place. An extra state is then required to provide a



(a) Simplified schematic of the logic circuit Down

(b) Simplified schematic of the logic circuit Up



(c) Simplified schematic of the logic circuit Down/Up

Figure 4.24: state controller Up and Down circuits implemented by logic gates

constant logic 1 to the logic circuits *Down/Up* since with the *AND* gate the signal will change with CLK_C. This is employed in all states except for the 1/2 were there is no comparison done after [5]

The *Reset* of the machine must be performed at the start of the controller circuit. This will put a logic 0 in all states except in the 1/2 state which is the starting state. When a *Down* transition occurs the reset signal of the current state is turned OFF by the transition logic circuit down output and the extra-state, if exists, is turned OFF by the next state. This guarantees that the new state is set to the logic 1 before the transition logic circuit output becomes zero. The same operation method is repeated for the *Up* case.

4.2.2.5 Simulation Results

Figure 4.25 shows a simulation result of the whole system with an ideal voltage source that varies from 2.3 to 800 mV and then returns back to 2.3 V. It is possible to see V_{LV} changing the limits as it changes from one state to another. The comparison error is, in the worst case, approx. 3 mV which corresponds to a 13.5 mV (3×4.5) when looking at V_{in}. Figure 4.26 shows a close up from the transition between the 2/3 and the 1/1 state. The decision making only occurs when the clock signals and the ouptut of the comparator (V_C) have the logic values presented in table 4.12. The Bandgap output (V_{REF}) is also showed in this plot and it yields constant at approx. 500 mV during the whole controller operation.

[5] There is in fact an *Up* comparison before the 1/2 state, however since the transition logic circuit only uses the *Down* condition there is no problem in skipping the state.

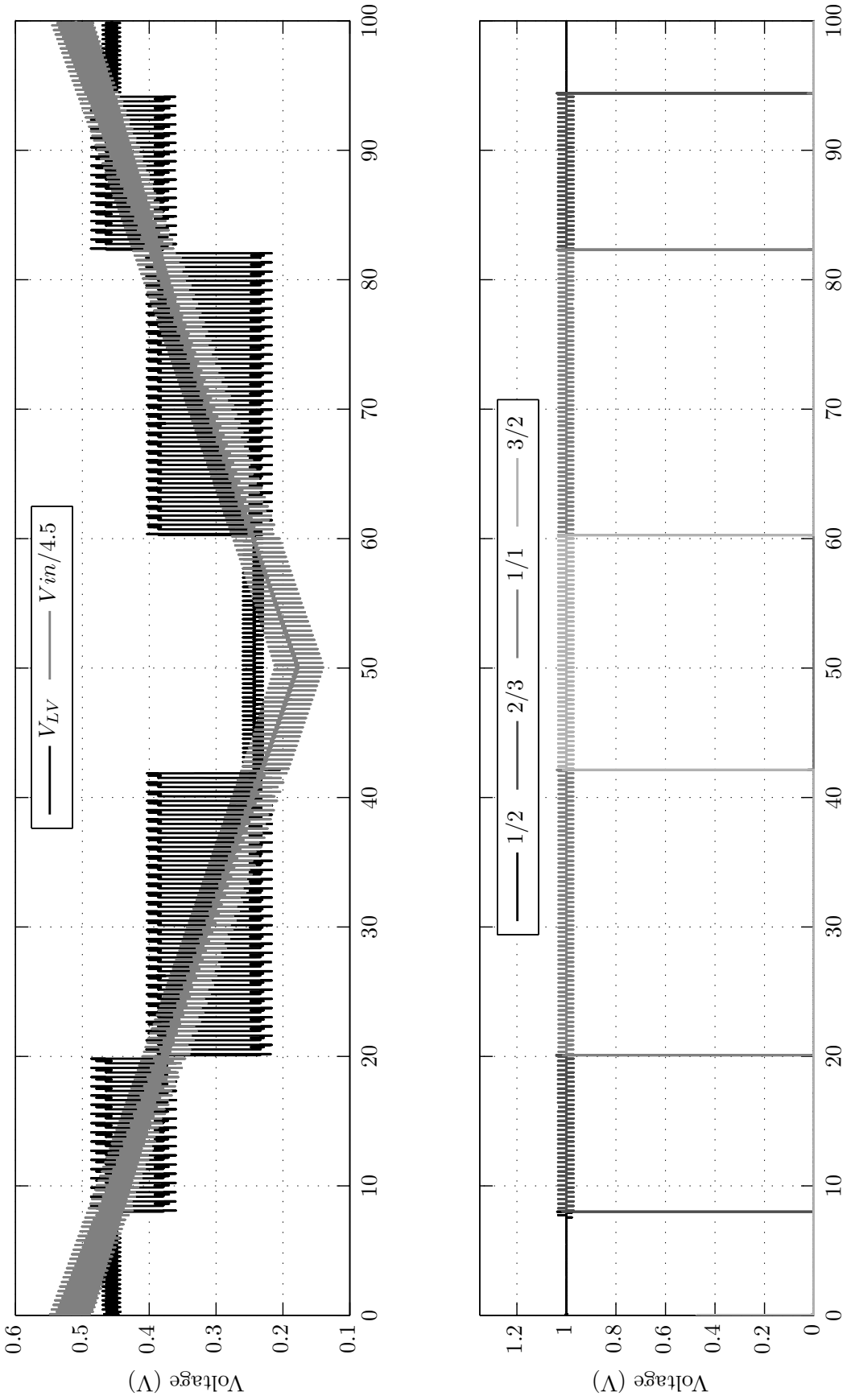


Figure 4.25: Simulation results derived by spectre of the converter state controller

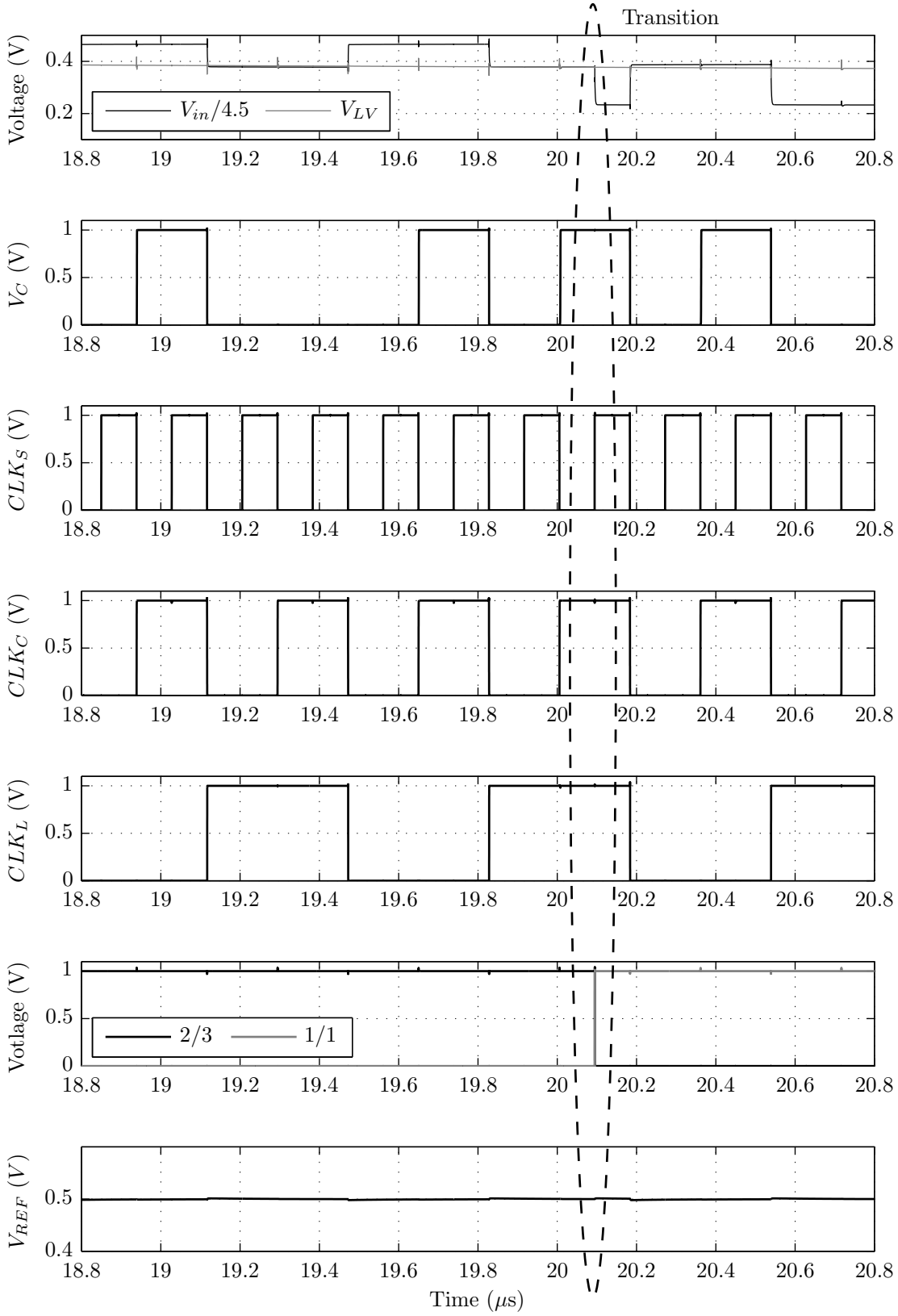


Figure 4.26: Close up of the converter state controller simulation results derived by spectre

4.2.3 Switch Drivers

This section presents the different clock buffers used to drive all the proposed converter switches. As V_{in} varies the drivers must adapt to the current state in order to work in safe operation mode - avoid voltage breakdown in the switches. To solve this problem, different driver circuits were used, especially in the A, B, F, and G switches.

4.2.3.1 A Driver

Table 4.13 shows the required output voltage swing on each state for the A_1, A_2, and A_3 switches. The clock signal in states 1/2 and 2/3 cannot go bellow 1 V in order to work in the safe operating region. States 1/1 and 3/2 have maximum voltage swings under 1.7 V. Thereby, the clock voltage can go from V_{in} to zero.

Table 4.13: A driver output swing voltage on each state

Switch \ State	1/2	2/3	1/1	3/2
A_1	$V_{in} \rightarrow 1$	$V_{in} \rightarrow 1$	$V_{in} \rightarrow 0$	$V_{out} \rightarrow 0$
A_2	$V_{in} \rightarrow 1$	OFF	$V_{in} \rightarrow 0$	$V_{out} \rightarrow 0$
A_3	$V_{in} \rightarrow 1$	OFF	$V_{in} \rightarrow 0$	OFF

A CMOS level shifter is commonly used to generate a voltage swing from high V_{DD}. In its conventional form, it produces a clock signal of V_{High} to 0 through a cross-coupled PMOS transistors and two NMOS transistors driven by complementary input signals [21]. When working with voltages higher than 2 V_{DD} the output node have difficulty to discharge and the LS cannot correctly operate [21]. Moreover, for voltages over 2 V the problem of gate oxide breakdown arises. To overcome this 3.3 V transistors can be used. However, simulation results showed this would lead to large power consumptions. Another solution using the stacking of MOS transistors in order to work in the safe operation region is proposed in [16]. Notwithstanding, in this case, the output voltage swing is limited between V_{High} and approximately V_{DD}, which is not suitable for the propose of this work as it would not work for the 1/1 and 3/2 states.

With this in mind, clock-bootstrapping circuits were used to boost the clock signal and then used to control an inverter that produces the output swing of the driver (Fig. 4.28).

Figure 4.27 shows the clock boosting circuit used to double the voltage of the clock signal [22]. The output capacitance, C_L, refers to the parasitic gate capacitance, C_{GG} of the MOS transistor. The circuit operates in two distinct phases. When $CLK = 0$ V, the MOS capacitor M_{10} is charged to V_{DD} by transistors M_1 and M_9. While the output node is discharged to zero by the transistors M_3 and M_4. When $CLK = 1$ V, the capacitor (M_{10}) is connected in series with C_L and V_{CB}. This way, if $V_{CB} = V_{DD}$ then V_{CB} plus V_{DD}, from the

capacitor, gives the $2\,V_{DD}$ output voltage.

$$V_{Boost} = \frac{(V_{DD} + V_{CB})\,C_{fly}}{C_{fly} + C_L} \tag{4.8}$$

Equation (4.8) describes the explained behaviour, where C_{fly} is the MOS capacitor M_{10}. This shows that it is impossible to achieve $2\,V_{DD}$ due to the C_L capacitor. However, for larger values o C_{fly} or low values of C_L the voltage becomes closer to the $2\,V_{DD}$. All the transistors, except M_{10}, were sized with the same sizes has the ones on [22].

Figure 4.28 shows the overall driver circuit that produces the clock signal for switches A_1, A_2 and A_3. This is composed by an inverter with two NMOS paths: M_2 to produce the

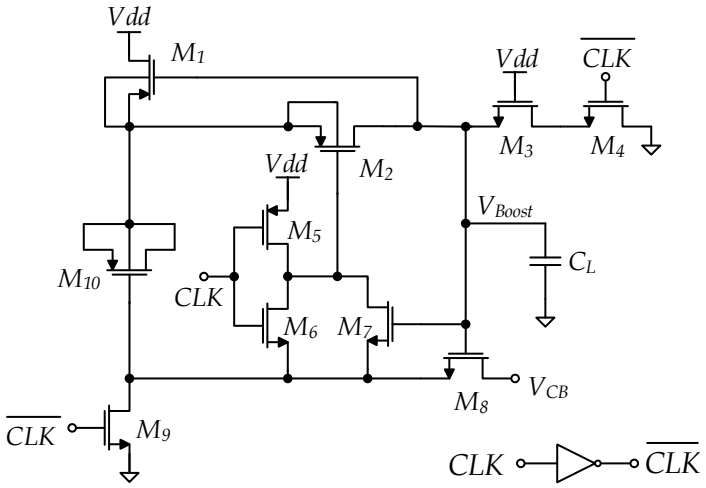


Figure 4.27: Simplified schematic of the clock boosting circuit. PMOS and NMOS with undefined bulk have their bulk connected do V_{DD} and ground, respectively

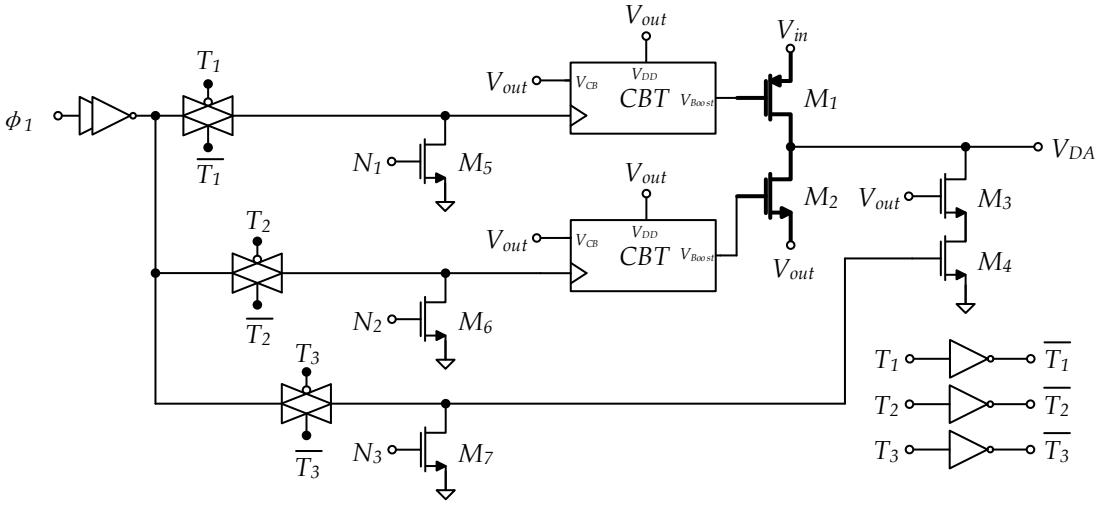
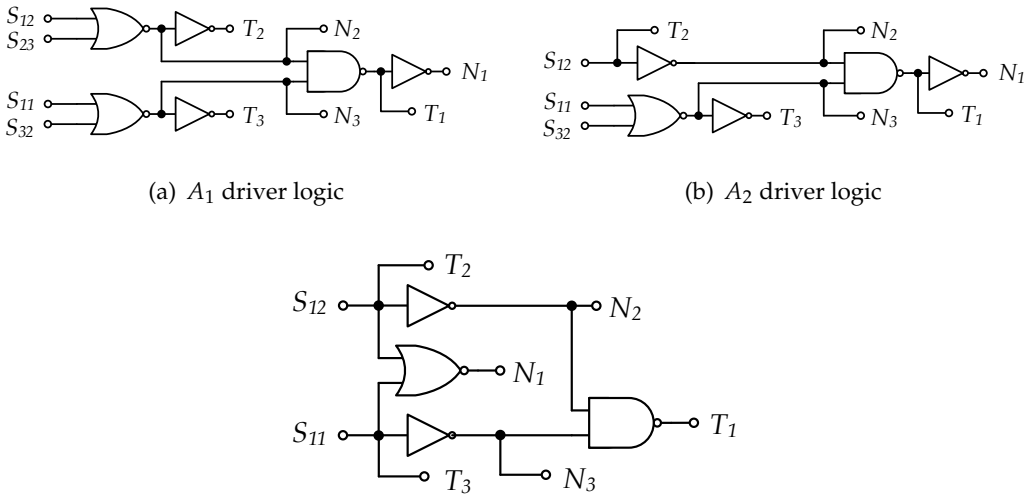


Figure 4.28: Simplified schematic of the A driver. Transistor $M_{1,2}$ (in bold line) are 3.3 V and all the remaining transistors (normal line) are 1.2 V transistors. PMOS and NMOS with undefined bulk have their bulk connected do V_{in} and ground, respectively

$V_{in} \rightarrow 1$ ($V_{out} = 1$ V) and the $M_{3,4}$ to produce $V_{in} \rightarrow 0$. Using 3.3 V transistor in $M_{1,2}$ brings two advantages: there is no problems regarding gate oxide breakdown and, since these have higher V_{th} ($\approx 500mV$), M_1 is turned OFF with the 2 V from the CBT (in the worst case $V_{in} = 2.3$ V). Moreover, the shoot-through current of the inverter is reduced. With the same purpose, $M_{3,4}$ are implemented by 1.2 V and controlled with a clock signal of 1 V. Where transistor M_3 is used guarantee that M_4 does not suffer oxide breakdown when $V_{DA} > 2.3$. All the A drivers (A_1, A_2 and A_3) work with ϕ_1 (see Table 4.1). Transmission gates and NMOS transistors ($M_{5,6,7}$) are used to control the main inverter (M_1/M_2). Moreover, this also allow the drivers to turn OFF or apply ϕ_1 to each individual switch. This is controlled by logic gates that differ from a switch to another. To ensure that ϕ_1 is capable of handling the total input capacitance of the driver two inverters with 3 and 6 times the minimum size are used, $(W/L)_{\text{NMOS}}$ of 0.48/0.12 and $(W/L)_{\text{PMOS}}$ of 2.3/0.12 in μm and $(W/L)_{\text{NMOS}}$ of 0.96/0.12 and $(W/L)_{\text{PMOS}}$ of 4.5/0.12 in μm, respectively. The transmission gates are sized with 4 times the minimum size, $(W/L)_{\text{NMOS}}$ of 0.64/0.12 and $(W/L)_{\text{PMOS}}$ of 3/0.12 in μm. Figures 4.29 show the simplified schematics of the logic circuits that control the driver (Fig. 4.28) for each switch. Lastly, Table 4.14 shows the transistors size of each driver.



(a) A_1 driver logic

(b) A_2 driver logic

(c) A_3 driver logic

Figure 4.29: Simplified schematic of the logic circuits used to control the A_1, A_2, and A_3 drivers

Table 4.14: Transistor sizes used in the implemented drivers of A_1, A_2, and A_3

Driver	Transistor	Size (μm)
A_1	M_1	200/0.3
	M_2	110/0.34
	M_3, M_4	26/0.12
	M_5, M_6, M_7	0.16/0.12
	CBT M_{10}	60/60
A_2	M_1	146/0.3
	M_2	77/0.34
	M_3, M_4	20/0.12
	M_5, M_6, M_7	0.16/0.12
	CBT M_{10}	60/60
A_3	M_1	140/0.3
	M_2	62/0.34
	M_3, M_4	16/0.12
	M_5, M_6, M_7	0.16/0.12
	CBT M_{10}	60/60

4.2.3.2 *B* Driver

Table 4.15 shows the required output swing voltage on each state for the switches B_1, B_2 and B_3. All the B switches are implemented by a PMOS switch that connects the V_{out} node to the flying capacitors. This means that the voltage through the drain and source is always 1 V. Thereby, a voltage swing $V_{in} \rightarrow 0$ stays in the safe operation region for any value of V_{in}.

Table 4.15: B driver output swing voltage on each state

Switch \ State	1/2	2/3	1/1	3/2
B_1	$V_{in} \rightarrow 0$	$V_{in} \rightarrow 0$	$V_{in} \rightarrow 0$	$V_{out} \rightarrow 0$
B_2	$V_{in} \rightarrow 0$	$V_{in} \rightarrow 0$	$V_{in} \rightarrow 0$	OFF
B_3	$V_{in} \rightarrow 0$	OFF	$V_{in} \rightarrow 0$	OFF

The circuit used to implement the drivers B_1, B_2, and B_3 is depicted in figure 4.30. The same operation method used on the A drivers is replicated here. The *CBT* circuit (Fig. 4.27) is used to turn OFF the PMOS transistor M_1 and 3.3 V transistors are used to prevent gate oxide breakdown and to increase V_{th} in order to reduced the shoot-through current. The switches B_1, B_2, and B_3 only work with ϕ_2. Therefore, one transmission gate and one

NMOS (M_3) transistor is used to control the driver. When the transmission gate is ON, the driver produces a complementary clock signal of ϕ_2 from V_{in} to zero (Note that the B switches are PMOS transistors, thereby to be activated with ϕ_2 they need a complementary clock signal). When the transmission gate is OFF and M_3 is ON, the inverter produces V_{in} that turns of the switch. Figure 4.30 shows the three different logic circuits for each B switch. Table 4.16 shows the sizes used for the inverter transistors. Again, Two inverters are used to drive ϕ_2 with 3 and 6 times the minimum size. The transmission gates are sized with 4 times de minimum size.

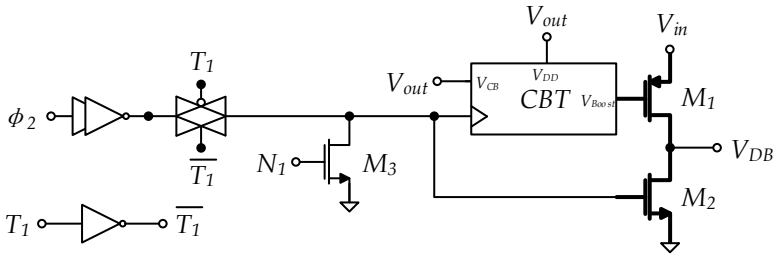


Figure 4.30: Simplified schematic of the B driver where transistors $M_{1,2}$ (in bold line) are 3.3 V transistors. PMOS and NMOS with undefined bulk have their bulk connected do V_{in} and ground, respectively

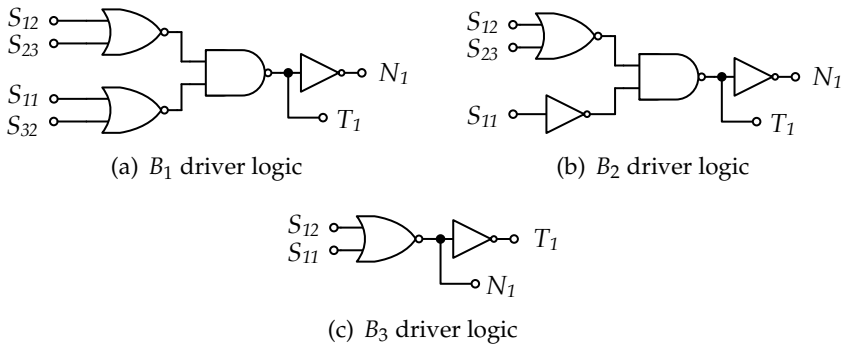


Figure 4.31: Simplified schematic of the logic circuits used to control the B_1, B_2, and B_3 drivers

In the 3/2 state V_{in} is going to be under 1 V. This means that the A_1, A_2, and B_1 drivers will have a voltage swing under 1 V. Therefore, R_{ON} will increase due to the decrease in the V_{eff}. To avoid this, a voltage power supply selector circuit, Fig. 4.32, is used to change the supply of this drivers from V_{in} to V_{out} in this state.

The M_1, M_2, M_3, and M_4 transistors implement a level shifter. When $S_{32} = 0$ V, M_2 turns ON and pull its node to ground which turns OFF M_6 with V_{in}. M_5 is turned ON and so $V_{H32} = V_{in}$. When $S_{32} = 1$ V, M_5 turns OFF ($V_{in} \approx 1$ V) and M_4 turns on, which pull its node to ground and turns ON M_6 - $V_{H32} = V_{out}$. Table 4.17 shows the transistors dimensions used to implement this circuit.

Table 4.16: Transistor dimensions used in the implemented drivers of B_1, B_2, and B_3

Driver	Transistor	Size (μm)
B_1	M_1	200/0.3
	M_2	56/0.34
	M_3	0.16/0.34
	CBT M_{10}	30/30
B_2	M_1	144/0.3
	M_2	40/0.34
	M_3	0.16/0.34
	CBT M_{10}	30/30
B_3	M_1	116/0.3
	M_2	32/0.34
	M_3	0.16/0.34
	CBT M_{10}	30/30

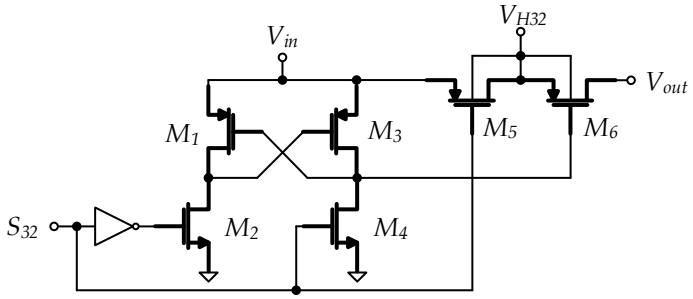


Figure 4.32: Simplified schematic of the voltage power supply selector circuit with 3.3 V transistors (in bold lines). PMOS and NMOS with undefined bulk have their bulk connected do V_{in} and ground, respectively

Table 4.17: Transistor dimensions used in the implemented the power voltage supply selector

Transistor	Size (μm)
M_1, M_3	0.73/0.34
M_2, M_4	0.6/0.3
M_5, M_6	300/0.3

4.2.3.3 *D* Drivers

The *D* switches are only activated in the 1/2 state. They handle voltages of $V_{in}/2$ when ON and 1 V when OFF. Being implemented by a PMOS switch means they only need a clock signal with 1 V of peak-to-peak voltage to turn OFF. Table 4.18 shows the required

Table 4.18: D drivers output voltage swings on each state

Switch \ State	1/2	2/3	1/1	3/2
D_1	$V_{out} \rightarrow 0$	OFF	OFF	OFF
D_2	$V_{out} \rightarrow 0$	OFF	OFF	OFF
D_3	$V_{out} \rightarrow 0$	OFF	OFF	OFF

output swing voltage on each state for the switches $D_{1,2,3}$.

Figure 4.33 shows the circuit that implements the D drivers. The two input inverters are sized with 2 and 3 times the minimum size, respectively; and the transmission gate is sized with 3 times the minimum size. The D switches are only activated in the 1/2 state and so all the three drivers are equal. Moreover, their logic circuit is composed by a single inverter which is more simpler than the previous drivers. The sizing of the transistors is presented in Table 4.19.

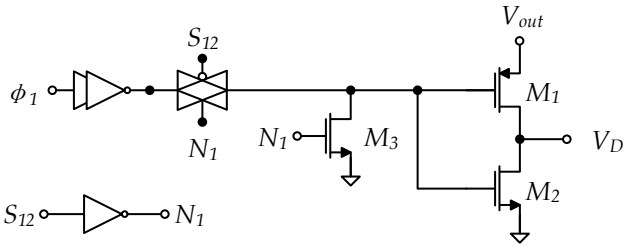


Figure 4.33: Simplified schematic of the D driver. PMOS and NMOS with undefined bulk have their bulk connected do V_{in} and ground, respectively

Table 4.19: Transistor dimensions used in the implemented drivers of D_1, D_2, and D_3

Driver	Transistor	Size (μm)
$D_{1,2,3}$	M_1	9/0.12
	M_2	2/0.12
	M_3	0.16/0.12

4.2.3.4 E Drivers

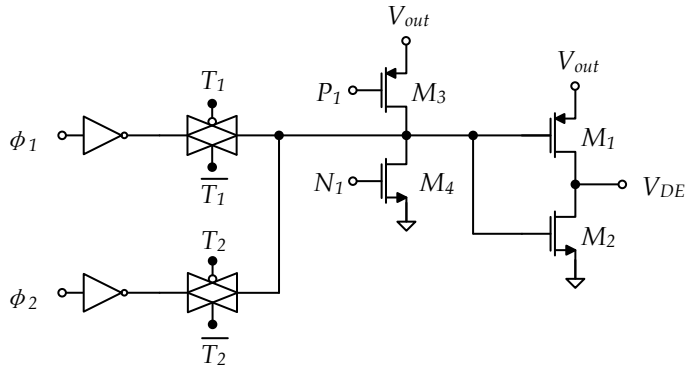
The E switches are responsible for connecting the flying capacitors to ground. Therefore, they are implemented using NMOS switches and need at least a 1 V to turn on. Table 4.20 shows the needed output swing voltage on each state for the switches E_1, E_2 and E_3.

The E_1 and E_2 drivers have to produce clock signals in phase with ϕ_1 or ϕ_2 depending on the current state. Figure 4.34(a) shows the simplified schematic of these two drivers and figures 4.34 shows the logic gates to produce the clock signal according with the active

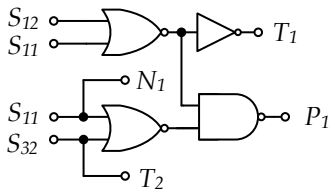
Table 4.20: E drivers output voltage swings on each state

Switch \ State	1/2	2/3	1/1	3/2
E_1	$V_{out} \rightarrow 0$	$V_{out} \rightarrow 0$	ON	$V_{out} \rightarrow 0$
E_2	$V_{out} \rightarrow 0$	$V_{out} \rightarrow 0$	ON	$V_{out} \rightarrow 0$
E_3	$V_{out} \rightarrow 0$	ON	ON	ON

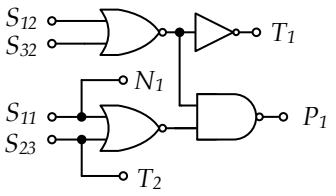
state (see Table 4.1). The input inverters and transmission gates are sized with 3 times the minimum size.



(a) E_1 and E_2 driver circuit



(b) E_1 driver logic



(c) E_2 driver logic

Figure 4.34: Simplified schematics of the E_1 and E_2 drivers and logic circuits. PMOS and NMOS with undefined bulk have their bulk connected do V_{in} and ground, respectively

The E_3 driver, is always ON, except for the 1/2 state. Its circuit is presented in Fig. 4.35 with the associated logic circuit.

Since the gate capacitance of these switches is, approximately, the same the inverters were equaly sized for all the drivers. Table 4.21 shows the size of transistors of all the three drivers.

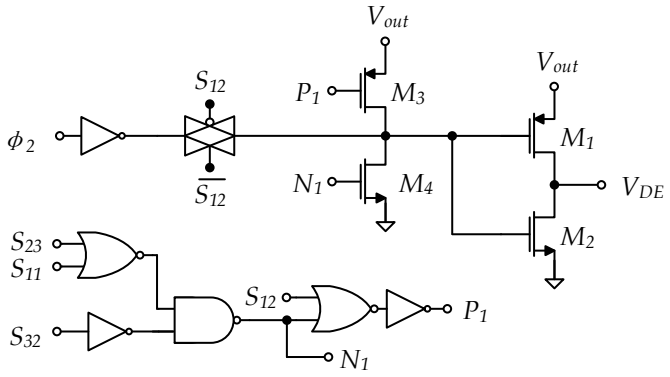


Figure 4.35: Simplified schematic of the E_3 driver. PMOS and NMOS with undefined bulk have their bulk connected do V_{in} and ground, respectively

Table 4.21: Transistor dimensions used in the implemented drivers of E_1, E_2, and E_3

Driver	Transistor	Size (μm)
$E_{1,2,3}$	M_1	4.7/0.12
	M_2	1/0.12
	M_3	0.75/0.12
	M_4	0.16/0.12

4.2.3.5 F and G Drivers

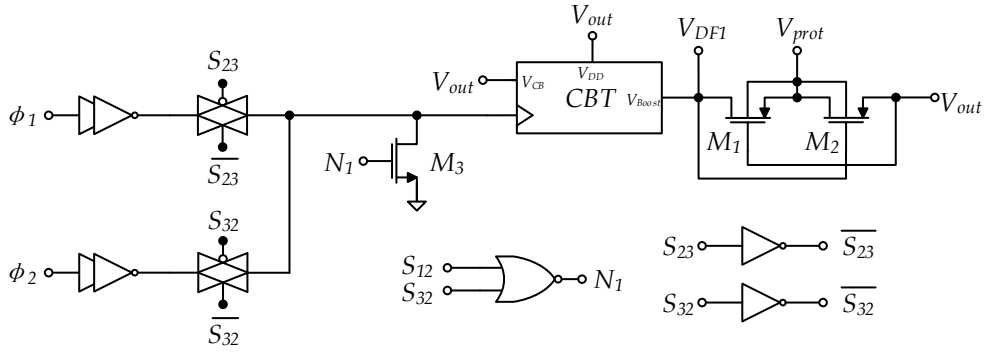
The drivers of switch F_1, F_2 and G_2 only operate in the 2/3 and 3/2 states. However, some concerns regarding the gate oxide voltage breakdown during the 1/2 state must be taken into consideration. These were explained in section 4.1.1 and Table 4.22 summarizes the required voltages on each state.

Figures 4.36 shows the circuits used to implement the $F1$ and G_2 drivers. A Clock boosting circuit is used to increase V_G in order to reduce R_{ON} of the transistors and enable the use of only a NMOS switch (without recurring to transmission gate). Moreover, the

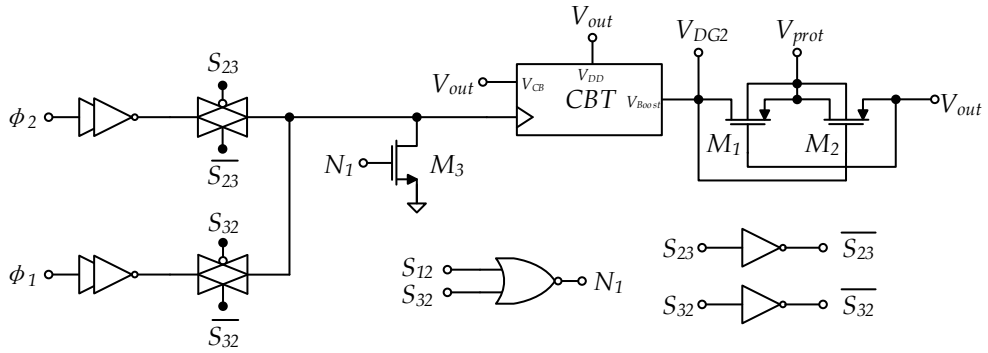
Table 4.22: F and G drivers output voltage swings on each state

Switch	State			
	1/2	2/3	1/1	3/2
F_1	OFF	$2\ V \rightarrow 0$	OFF	$2\ V \rightarrow 0$
$F_{1,Prot}$	V_{out}	$2\ V \rightarrow 1$	V_{out}	$2\ V \rightarrow 1$
F_2	V_{out}	$2\ V \rightarrow 0$	OFF	$2\ V \rightarrow 0$
G_2	OFF	$2\ V \rightarrow 0$	OFF	$2\ V \rightarrow 0$
$G_{2,prot}$	V_{out}	$2\ V \rightarrow 1$	V_{out}	$2\ V \rightarrow 1$

drivers F_1 and G_2 feed two extra switches that make use of the stacking MOS technique [16] to protect the transistors. This is performed by the V_{prot} signal that has an output of 1 V (V_{out}) when $V_{DF1} = 0$ V by turning ON M_2 and turning OFF M_1; and when $V_{DF1} = 2$ V has an output of 2 V by turning ON M_1 and turning OFF M_2. In sum, V_{DF1} will have a $2 \rightarrow 0$ V swing and V_{prot} a swing of $2 \rightarrow 1$ V. The same operation is presented in the G_2 driver.



(a) F_1 driver



(b) G_2 driver

Figure 4.36: Simplified schematic of F_1 and G_2 drivers. PMOS and NMOS with undefined bulk have their bulk connected do V_{in} and ground, respectively

To work in the safe operation region, the F_2 driver needs an output voltage of 1 V in the 1/2 state. This is implemented by the circuit depicted in figure 4.37. In the 1/2 state the CBT circuit is set to produce an output of 1 V through the M_1 transistor. In the the states 2/3 and 3/2 it works normally with a voltage swing between 2 and 0 V. The 1/2 to 2/3 transition showed in simulation a peak voltage of 2 V. Therefore, two delay circuits (section 4.2.1.2) of 10 ns are used to delay the change from 1 V to the clock signal 2-0 V.

The two input inverters of all the three drivers are sized with 3 and 6 times the minimum size, respectively; and the transmission gate sized with 3 times the minimum size. Table 4.23 shows the size of the transistors in all three drivers.

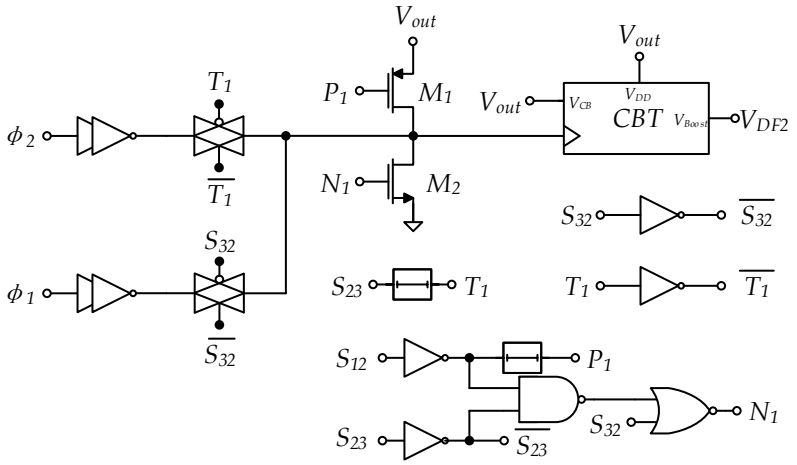


Figure 4.37: Simplified schematic of the F_2 driver. PMOS and NMOS with undefined bulk have their bulk connected do V_{in} and ground, respectively

Table 4.23: Transistor dimensions used in the implemented drivers of F_1, F_2, and G_3

Driver	Transistor	Size (μm)
F_1	M_1, M_2	16/0.12
	M_3	0.16/0.12
	CBT M_{10}	30/30
F_2	M_1	0.75/0.12
	M_2	0.16/0.12
	CBT M_{10}	30/30
G_2	M_1, M_2	16/0.12
	M_3	0.16/0.12
	CBT M_{10}	30/30

4.2.3.6 Start-Up Circuit

Figure 4.38 shows the schematic of the start-up circuit, responsible for the power-up of the system, based on [6]. The supercapacitor is charged by a external source, therefore, at the beginning, V_{in} will start to rise from 0 V. This will create a *Reset* signal through the level shifter implemented by M_1, M_2, M_3 and M_4. R_1 and R_2 guarantees that the transistor M_4 is turned ON so that M_5 will also be turned ON. This will directly connect the V_{out} node to V_{in} starting the charging process. They will be connected until v_3 reaches the M_2 threshold voltage. v_3 is generated by a resistive voltage divider (R_3 and R_4) that is feed by a delayed version of V_{out} performed by the chain of inverters (M_9-M_{10} and M_7-M_8), R_d, and C_d. This means that R_3 and R_4 define the start-up voltage in which M_5 is turned OFF and $Reset = 0$ V. An extra level shift implemented by M_{13}, M_{14}, M_{15}, and M_{16} is used to ensure that M_{12} is turned off for high values of V_{in}. Table 4.24 shows the transistors,

resistors and capacitors sizes of the start-up circuit in order start working when $V_{in} = 1.2$ V. At that time, M_5 is turned OFF and V_{out}, which is also 1.2 V, starts to decay to 1 V.

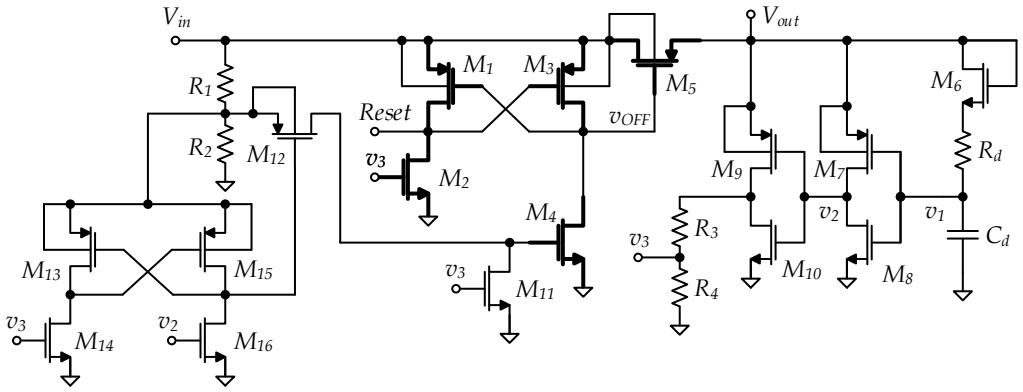


Figure 4.38: Simplified schematic of the start-up circuit. Transistors in bold lines are 3.3 V and normal lines refer to 1.2 V transistors. Also PMOS and NMOS with undefined bulk have their bulk connected do V_{in} and ground, respectively

Table 4.24: Transistor, resistors and capacitors in the start-up circuit

Transistor	Size (μm)
M_1, M_3	9.2/0.3
M_2, M_4	39/0.34
M_5	100/0.3
M_6, M_8, M_{10}, M_{11}, M_{14}, M_{16}	0.16/0.12
M_7, M_9, M_{12}, M_{13}, M_{15}	0.75/0.12
Resistors	Size (KΩ)
R_1, R_2, R_d	500
R_3	530
R_4	470
Capacitors	Size (pF)
C_d	1

CHAPTER 5

ELECTRICAL SIMULATIONS

In this section electrical simulation results of the whole system are presented and discussed. It shows four simulations of distinct behaviours of the circuit.

- The first simulation shows the behaviour of the system as the input capacitor discharges from 2.3 V to 0.85 V and then the charging back to 2.3 V. This was carried out with $C_{in} = 100$ nF;
- The second simulation shows the discharge of the input capacitor from the 2.3 V to 0.69 V and then charged back to 2.3 V. In this case the V_{out} decreases below 1 V showing the ability of the system to recover to 1 V once the input voltage is high enough. This was again carried out with $C_{in} = 100$ nF;
- In this simulation C_{in} is increased to 400 nF and simulated for an input voltage swing from 2.3 to 0.85 V;
- Finally, the last simulation shows the start up of the system with $C_{in} = 1$ F and $P_{out} = 2$ μW from a 0 V voltage value for both input and output.

All these simulation were carried out with $C_{out} = 100$ nF and, with the exception of the last simulation, $P_{out} = 2$ mW.

5.1 Simulation Results and Conclusions

Figure 5.2 shows the simulation results of the system with $P_{out} = 2$ mW and $C_{in} = C_{out} = 100$ nF. The system starts with the input capacitor charged with 2.3 V which corresponds to the 1/2 state. V_{out} remains approximately constant through the charge/discharge of the flying capacitors as V_{in} decreases. When V_{in} reaches the transition voltages - 2.05, 1.69, and 1.04 V; the system changes to the next state. The error between the measure transition

voltage is, in the worst case, ≈ 10 mV. At $t = 76$ μs, C_{in} is charged by an external current supply in order to see the system going backwards. The upper transition voltage levels were 1.1, 1.87 and 2.17. These values are higher than the ideal values due to the hysteresis in the resistive ladder of the state controller (section 4.2.2.1).

To observe the ability of the system to recover when the output voltage decreases below 1 V, the previous simulation was repeated with a longer delay before the charge of C_{in} through the external current supply. This way, as the plot shows, when $V_{in} < 0.85$ V the system is unable to maintain $V_{out} = 1$ V and this voltage begins to drop. When V_{in} starts to increases, the output voltage start increasing to 1 V and, as the plot shows, the system managed to successfully return to $V_{out} = 1$ V as well as returning to its normal behaviour.

Figure 5.4 shows the discharge of the supercapacitor from 2.3 V to 0.77 V with $P_{out} = 2$ mW, $C_{in} = 400$ nF and $C_{out} = 100$ nF. There is an increase in the working time of the converter as it would be expected. Moreover, this time approximately four times longer than the previous simulation with a $C_{in} = 100$ nF. This shows an approximately linear relation between the system working time and the value of the input capacitor

In all plots, the slope of V_{in} changes from state to state. Whereas, the smallest slope is in the $1/2$ state and the largest in the $3/2$ state. This is an indication of which which states drain more current from C_{in}.

In section 4.1.2.5 the efficiency was calculated considering the steady state of the converter. The efficiency can also be determined by the ratio between the energy drained

Table 5.1: Simulation results summary and efficiency for the discharge of C_{in} with 100 nF and 400 nF, $C_{out} = 100$ nF, and $P_{out} = 2$ mW

State	Work Time (μs)			Voltage range (V)		$E_{C_{in}}$ (nJ)	$E_{R_{out}}$ (nJ)	η (%)
	t_1	t_2	Δt	$V_{in,t1}$	$V_{in,t2}$			
				$C_{in} = 100$ n F				
1/2	0	21.71	21.71	2.3	2.05	54.375	40.49	74.46
2/3	21.71	43.34	22.17	2.05	1.69	67.32	43.28	65.95
1/1	43.34	71.85	28.51	1.69	1.04	88.725	57.21	64.01
3/2	71.85	76.72	4.87	1.04	0.85	17.955	9.74	54.25
				$C_{in} = 400$ nF				
1/2	0	78.22	78.22	2.3	2.07	201.02	153.70	76.46
2/3	78.22	165.13	86.91	2.07	1.7	278.98	173.9	62.33
1/1	165.13	281.2	116.07	1.7	1.05	357.5	232.9	65.14
3/2	281.2	301.3	20.1	1.05	0.85	76.9	40.02	52.92

by R_{out} with the one supplied by C_{in} (5.1). Table 5.1 shows the new values of efficiency calculated using (5.1) for the first and third simulation during the discharge of C_{in}. As expected, the 1/2 is the state with higher η and the 3/2 the one with the lowest.

$$\eta_{energy} = \frac{\Delta E_{R_{out}}}{\Delta E_{C_{in}}} = \frac{\int_{t1}^{t2} \left(\frac{V_{out}}{R_{out}} \right) dt}{0.5\, V_{in,t1}^2\, C_{in} - 0.5\, V_{in,t2}^2\, C_{in}} \tag{5.1}$$

Figure 5.1 and table 5.2 show the simulation results of the efficiency for $P_{out} = 2$ mW and $V_{out} = 1$ V; with V_{in} connected to an ideal voltage supply. This enables to determine the efficiency in the steady state condition for a specific input voltage. The plot shows that η decreased approximately 3-5% when compared with the plot in figure 4.5 that only

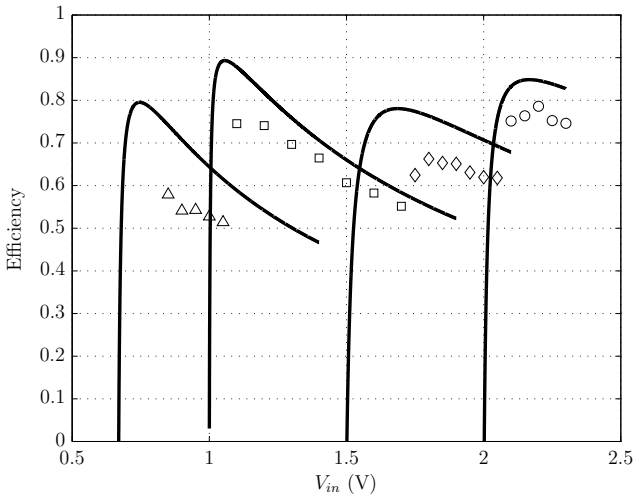


Figure 5.1: η of the whole system as a function of V_{in} for $P_{out} = 2$ mW and $V_{out} = 1$ V. Simulation results derived by spectre are displayed in markers

Table 5.2: Simulation results of the efficiency (η) in the steady state condition for the four states with $P_{out} = 2$ mW and $V_{out} = 1$ V

State	V_{in} (V)	P_{in} (mW)	η (%)
1/2	2.3	2.68	74.6
	2.1	2.66	75.1
2/3	2.05	3.24	61.8
	1.75	3.20	62.5
1/1	1.7	3.62	55.2
	1.1	2.68	74.5
3/2	1.05	3.89	51.4
	0.85	3.45	57.9

accounts with the drivers effect. Notice that the values from η_{energy} are close to the average values, in each state, of η measured for the steady state.

Table 5.3 shows the maximum values of ΔV_{out} measured considering only the steady state. In these simulations the value of V_{in} was swept from 2.3 to 0.85 V using an ideal voltage power supply. The results show that the ripple is different from one state to another and, in the worst case, ΔV_{out} as a maximum ripple of approx. 23.4 mV on the $1/1$ state.

Table 5.3: Maximum ΔV_{out} values for each state of the converter with a V_{in} sweep from 2.3 to 0.85 V with $C_{out} = 100$ nF

State	$\max\{\Delta V_{out}\}$ (mV)
$1/2$	11.19
$2/3$	10.07
$1/1$	23.42
$3/2$	13.44

Figure 5.5 shows the starting-up of the system. The system starts the operation when $V_{in} = V_{out} = 1.2$ V and so the *Reset* signal is pulled to 0 V and the v_{OFF} signal turns off the connection between the input and output node. In this simulation the external current supply keeps charging the supercapacitor and the converter performs its task to produce a stable $V_{out} = 1$ V. Notice that in the start of the circuit the output load must be turned off ($R_{out} \approx 500\ K\Omega$).

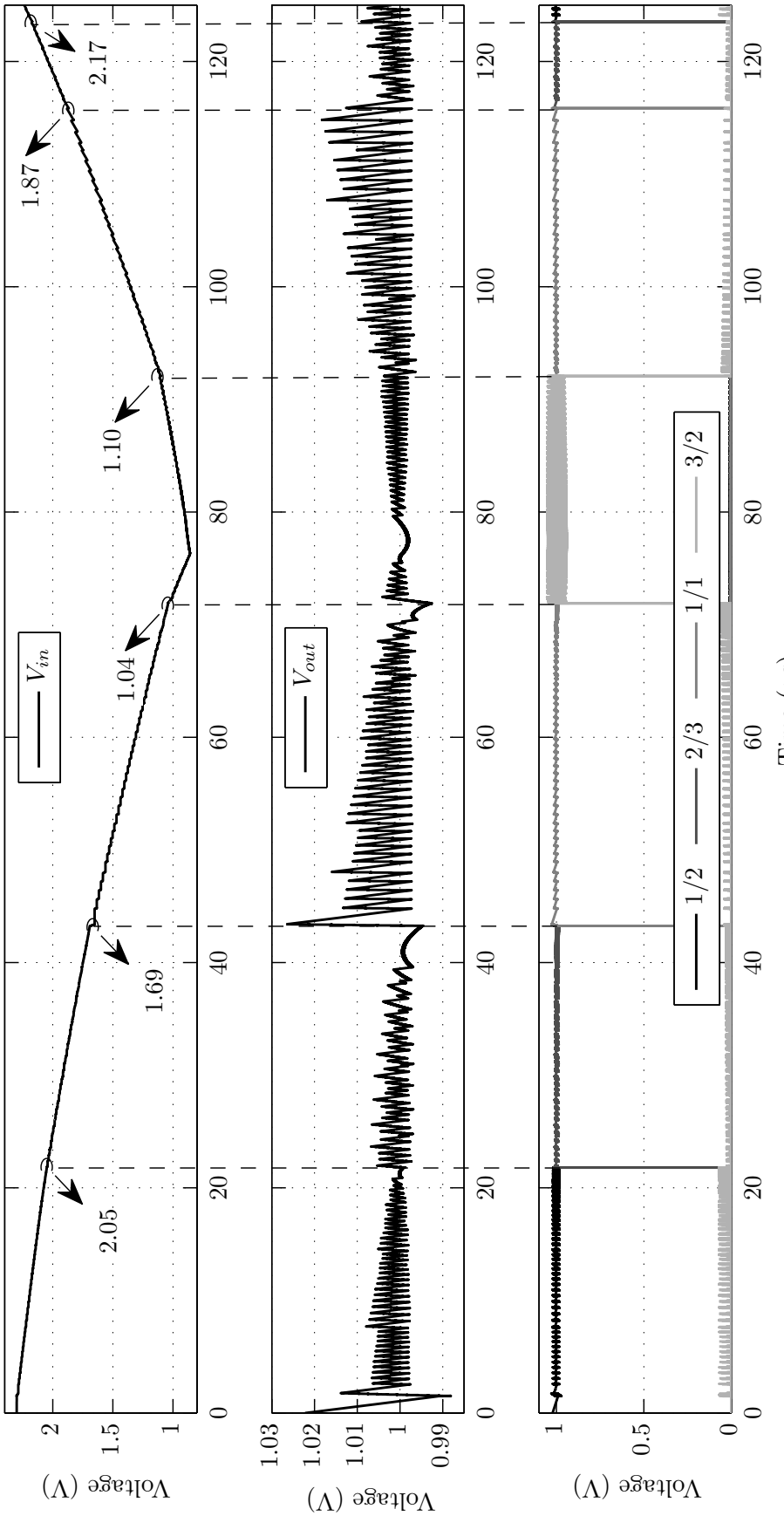


Figure 5.2: Simulation results of the whole system with $P_{out} = 2$ mW and $C_{in} = C_{out} = 100$ nF for a V_{in} swing between 2.3 and 0.85 V and back to 2.3 V

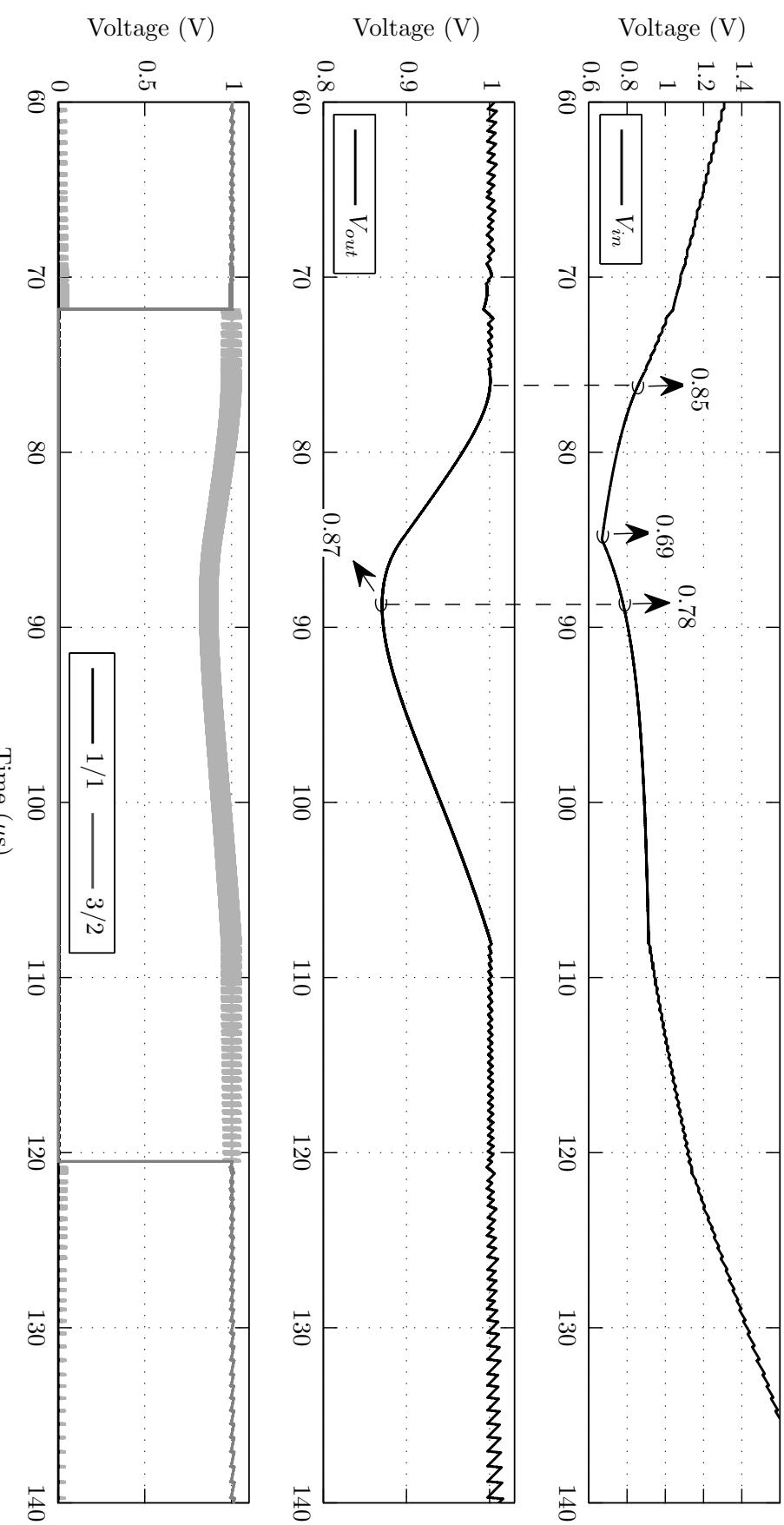


Figure 5.3: Close up on the simulation of the whole system with $P_{out} = 2$ mW and $C_{in} = C_{out} = 100$ nF for a V_{in} swing between 2.3 and 0.69 V and back to 2.3 V

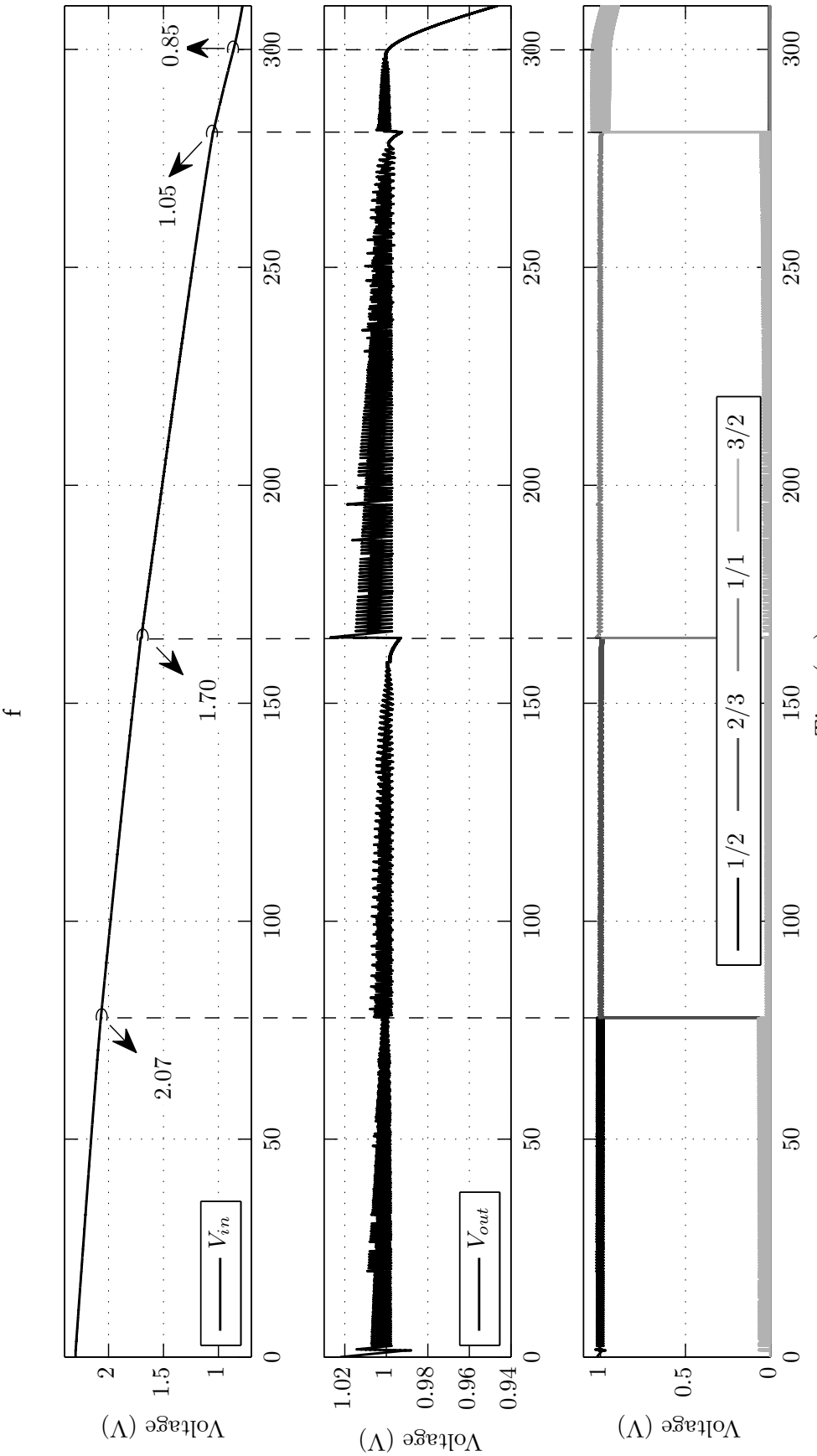


Figure 5.4: Simulation results of the whole system with $P_{out} = 2$ mW, $C_{in} = 400$ nF, and $C_{out} = 100$ nF for a V_{in} swing between 2.3 and 0.77 V

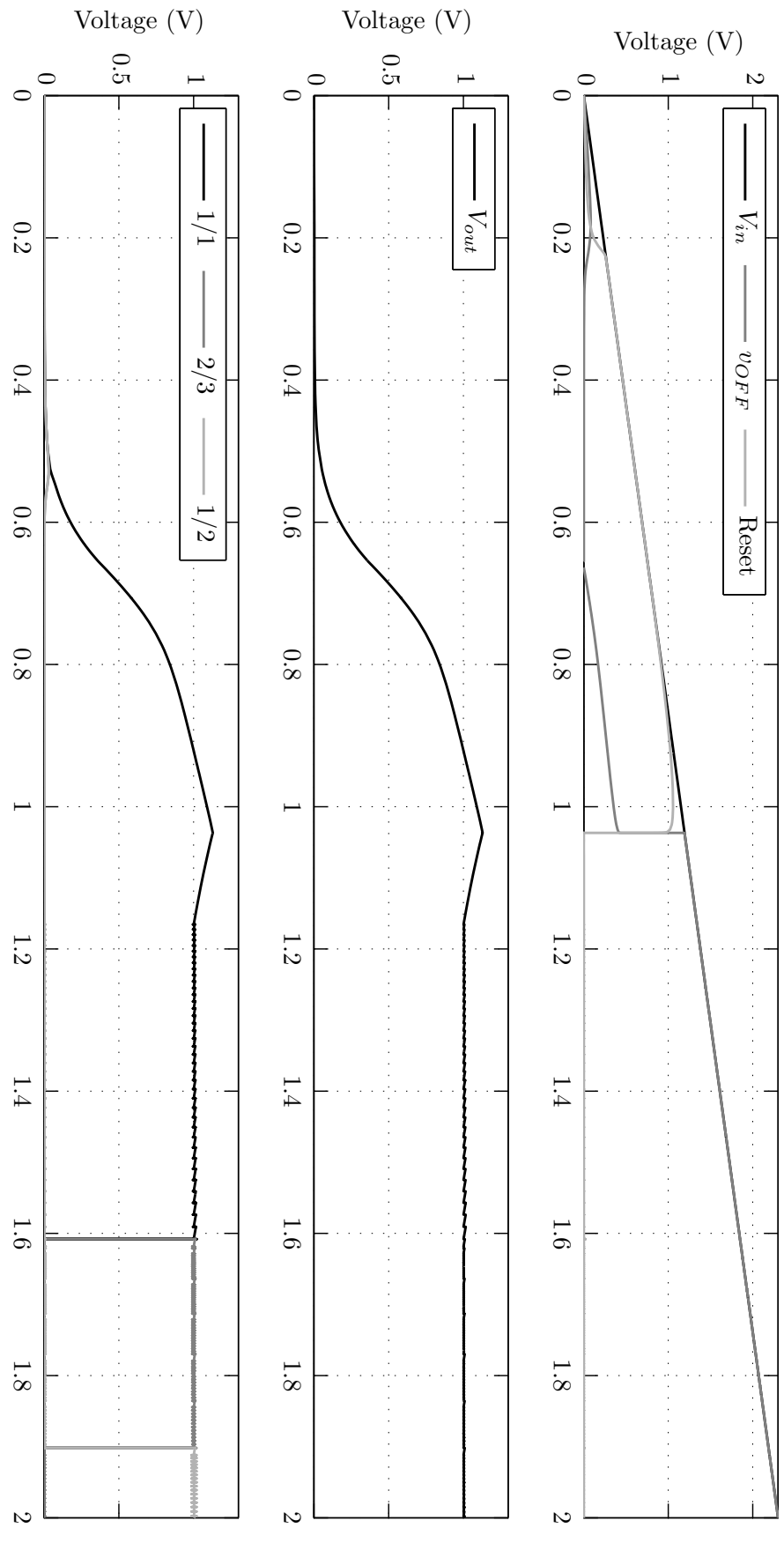


Figure 5.5: Simulation results of starting-up of the system through an external current supply with $P_{out} = 2\ \mu W$, $C_{in} = 1$ F, and $C_{out} = 100$ nF

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

The objective of the work presented in this thesis was to develop a multi-ratio SC DC-DC converter, in 130-nm technology, that is able to convert a variable input voltage provided by a supercapacitor, into a stable 1 V output voltage. To perform its task the converter needs auxiliary circuits, such as a phase and state generator, switch drivers and a start-up circuit. These form a system that is able to produce a stable 1 V output voltage within a input voltage swing of 2.3 V to 0.85 V with an output power of 2 mW and a maximum output ripple of 23 mV.

In chapter 2 four different topologies of SC DC-DC converters were analysed. In these it was seen that the parasitic capacitances from the flying capacitors and from the switches have a strong impact in the efficiency and output voltage. With the resulting equations of the efficiency regarding the parasitic effects, it is possible to choose in which regions of the input voltage the converter can or must work to achieve the best performance. Another important equation studied in this chapter is the frequency as function of the output voltage, flying capacitors and parasitics, output power, and input voltage. By setting the value of the flying capacitors and the output power (setting R_{out}) it is possible to calculate at which frequency the converter must work to produce a desire output voltage.

The capacitors and switches implemented in 130-nm technology were studied in chapter 3. Two structures to implement a capacitor in IC were presented. It was shown that the use of a MOS device as a capacitor has a large bottom plate parasitic capacitance. Thereby, due to their lower parasitic capacitances and higher breakdown voltages the MIM capacitors were chosen.

The study of a switch implemented through a MOS device was also carried out in this chapter. To better understand the switching parameters, R_{ON}, C_{GG}, and W/L of the

transistors, equations that relate these parameters with the 130-nm technology (k_R and k_C) were determined. This showed that 3.3 V transistors need a much larger area, when compared with 1.2 V transistors, to implement the same R_{ON}, which brings problems regarding the power consumption of these switches. However, 1.2 V transistor can not support voltages above 2 V without suffering from gate oxide breakdown. With this trade-off between the 3.3 and 1.2 V transistors in mind and the resulting switch parameters, the choice of the switches was carefully studied in chapter 4. Lastly, a case study for the 1/2 state was presented in which the impact that the output power has in the switch parameters and in their power consumption is shown. A quadratically relation between the power drained by the switches and the output power was observed. Moreover, the input voltage until which the converter works also affects this relation. With this, the efficiency equation determined in section 2.1.2 was recalculated to account the power drained by the switches. As expected, the efficiency values were decreased.

The proposed multi-ratio SC DC-DC converter and the overall system are shown and studied in chapter 4. This converter is composed by three flying capacitors (C_1, C_2 and C_3), fifteen MOS switches (A_1,A_2,..., F_2, and G_2), and an output capacitor C_{out}. The goal was to perform the tasks of the four converters presented in chapter 2, in one single converter. This was achieved through a different combination of active switches that performs the same operation as the separate converters. Therefore, the converter is divided into four states (1/2, 1/1, 2/3 and 3/2) with two phase clocks ϕ_1 and ϕ_2. The input swing voltage can go to 2.3 V which is out of the 1.2 V transistors safe operation region. To this end the stacking of transistors and a controlled V_G in some switches were employed. This was carefully studied and tested through simulation to ensure that there was no gate oxide breakdown in all the switches.

The efficiency equation was adapted to the new number of switches as well as the new power drained by the clock circuits. Through this and the frequency equations, it was possible to decide the regions of V_{in} that each state operates and the corresponding efficiency as well as the operation frequency regions. This allowed to size the converter and calculate the switch parameters that were later used to size the drivers and the overall system. The converter was to be designed with a 10 mW output power. However, it was not possible to achieve such power values and so the specification was changed to 2 mW. In sum, the proposed converter has an output power of 2 mW, with $C_1 = C_2 = C_3 = 333$ pF (which was set by an area specification), $C_{out} = 100$ nF (set to be 10 times higher than the total of the flying capacitors). Simulation results, considering the overall system, showed efficiency values below the theoretical ones, specially in the 2/3 and 3/2. In this last case, its mainly due to $V_{eff} < 1$ V of the switches that arouse from the safe operation restrictions as well as the integration of the four converters in one single converter. Other effects such as the shoot-through current and overlap of the inverter drivers, the power consumption of the remaining system, which is presented in all states, contribute to this reduction.

Also in this fourth chapter, the overall system is presented. Starting with the generation of the two phase clocks ϕ_1 and ϕ_2 through an ASM with a non-overlap technique and a power down feature. These clock signals change their frequency automatically, through controlled delay circuits, according to the active state of the converter. The ASM is controlled by a comparator that indicates if the output voltage is below the reference voltage and, if it is, starts the generation of the clocks and when above returns to the power down mode. Simulation results showed that the overlap between the clock signals is a key aspect in the converter efficiency. Thus it was added a time delay (1 ns) between the two phases to ensure that there are no active switches from different phases activated in the clock transitions.

The four states of the system was also implemented through an ASM controller. In this a Bandgap circuit was used to produce a reference voltage of 500 mV to enable the generation of the voltage transistors through a resistive ladder. Hysteresis was added to the upper voltage transitions (when the converter is changing backwards) to avoid multiple transition errors. A dynamic comparator with a kick-back noise reduction technique was used to compare the voltage levels with the input voltage from the supercapacitor. Finally, the ASM receives the information from the comparator and decides which state must be activated. To decrease the power consumption and avoid errors in the decision making three extra clocks were generated through frequency divider circuits. This slows down the frequency in which these circuits work and avoid problems regarding settling error. Simulation results derived by spectre showed an overall good performance of this state controller with an offset error inferior to 3 mV.

The final part of chapter 4 showed the implementation of the drivers that feed the converter switches. These were design to achieve the lowest possible power dissipation and at the same time set the needed voltage values for the switches to work in the safe operation region. The use of MOS level shifters was analysed and shown to be unable to deal with the output voltage specifications as well as high power consumption values. Thereby, the implementation relied on clock-bootstrapping circuits followed by an inverter. Transmission gates were used to decide either or not to pass the phase signals to each driver. They are controlled by logic gates according to the active state. This way, feed-forward techniques using the two phase clock signals to generate the new clock signals for each driver were avoided.

The fifth chapter, chapter 5, electrical simulations of the whole system are presented. These showed a stable output voltage of 1 V for a input voltage swing between 2.3 V to 0.85 V. where the efficiency were calculated from the supplied/drained energy during time. The maximum achievable efficiency was 76% in the 1/2 state and the remaining states reached 66%, 65% and 53% in the 2/3, 1/1 and 3/2 sates, respectively. The maximum output ripple, (ΔV_{out}), was approximately 23 mV.

6.2 Future Work

The start-up circuit needs to be further investigated and optimized so that it can achieve a better efficiency in the starting up of the system. Charge reusing techniques to reduce the power losses from the flying capacitors [6] could be used to achieve better efficiencies. Also, there are other techniques that were not tested in this work and could result in an improvement on the overall performance of the proposed converter. For example, reducing the output ripple as well as the C_{out} value by splitting the proposed converter in smaller modules connected in parallel [23]. Other techniques using the inactive flying capacitors to act as an output capacitor [24] can also be used for this aim.

It is also possible to eliminate the output ripple by using a Low-dropout (LDO) regulator which provides a regulated voltage source for noise-sensitive blocks [25, 26, 27]. Hence, the output voltage, for example, could be decreased to 950 mV by meanings of a *LDO* and thus eliminate the output ripple.

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