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Design of a Power Output Stage for a Class D Audio Power Amplifier based on an 1.5-bit $\Sigma\Delta$M

Dissertação apresentada para obtenção do Grau de Mestre em Engenharia Electrotécnica e de Computadores, pela Universidade Nova de Lisboa, Faculdade de Ciências e Tecnologia.

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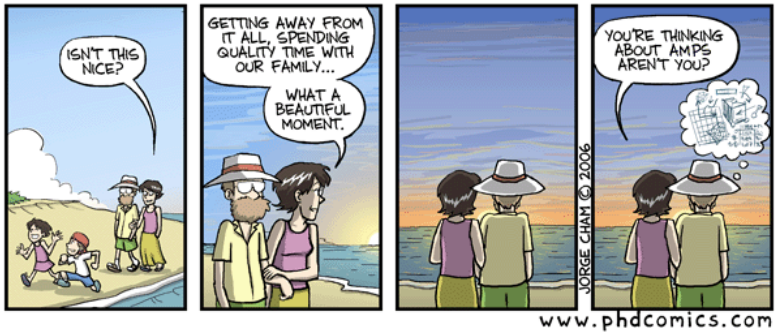
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- yes.

To Mia, who fills my half-empty cup.

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Resumo

Existe uma crescente preocupação com a eficiência energética dos dispositivos eletrónicos à medida que estes se tornam mais autónomos e portáteis. Os amplificadores áudio, parte integrante destes dispositivos, são um dos maiores responsáveis pela sua elevada dissipação de energia. Nos amplificadores áudio Classe D o andar de potência comporta-se como um interreptor, o que resulta numa eficiência energética teórica de 100%. Tal acontece devido ao facto de quando os transístores MOSFET conduzem, existe uma pequena queda de tensão do dreno para a fonte, o que faz com que a sua dissipação de energia seja quase nula, potencializando a sua eficiência energética para os 100%.

A presente dissertação tem como objectivo estudar, desenhar e implementar um andar de potência para um amplificador áudio Classe D, baseado num modelador sigma-delta de 5ª ordem optimizado, capaz de esquemas de quantização de 1-bit e 1.5-bit e de ter o andar de potência dentro da malha de realimentação. O andar de potência proposto é capaz de gerar uma queda de tensão de 28 V pico-a-pico numa carga de 8-Ohm, e as simulações eléctricas mostram que o mesmo é capaz de atingir uma relação sínal ruído-e-distorção (SNDR) de 94.52 dB e uma ditorção harmónica total (THD) de -96.65 dB com uma eficiência energética de 88.46%, quando o esquema de quantização é de 1.5-bit. Simulações com 1-bit de quantizacao são também realizadas e é possível atingir uma SNDR de 77.99 dB e uma THD de -81.42 dB com 78.54% de eficiência.

Os resultados experimentais dos amplificadores prototipados motram que quando se utiliza 1.5-bit de quantização existe um decréscimo na performance, tendo uma SNDR de 47.52 dB, THD de -48.08 dB e uma eficiência energética de 85.8%. A distorção inserida é devido à distorção do andar de potência e ao *mismatch* na malha de realimentação de 1.5-bit.

Palavras-chave: Class D audio amplifier, power amplifiers, power efficiency, output stage, gate drivers, continuous-time sigma-delta modulation.

Abstract

There is an ongoing tendency to increase the energy efficiency of every electronic device as global sustainability becomes a major concern. Audio amplifiers, which are found in every-day electronic systems, play a big role regarding their power consumption. In Class D amplifiers the output stage devices operate as switches, resulting in a theoretical power efficiency of 100% due to the fact that when the power output MOSFETs are conducting there is a small drain-to-source voltage drop causing their dissipated power to be close to zero.

The objective of this thesis is to study, design and implement a power output stage for a Class D audio power amplifier based on an optimized continuous-time 5^{th} order sigma delta modulator, capable of 1-bit and 1.5-bit quantization scheme, with the output stage inside the feedback path. The proposed power output stage generates a floating differential output voltage up to 28 V peak-to-peak on an 8-Ohm load and achieve 94.52 dB signal-to-noise-and-distortion-ratio (SNDR) and a -96.65 dB total-harmonic-distortion (THD) with a power efficiency of 88.46% when 1.5-bit quantization scheme is in use. The 1-bit quantization scheme allows a SNDR of 79.57 dB, THD of -81.42 dB and a power efficiency of 78.54%.

The measured performance of the implemented prototypes show that the 1.5-bit Class D audio amplifier achieves a SNDR of 47.52 dB and a THD of -48.08 dB with a power efficiency of 85.8%. The performance decrease appears due to the distortion in the power output stage and due to the 1.5-bit feedback mismatch.

Keywords: Class D audio amplifier, power amplifiers, power efficiency, output stage, gate drivers, continuous-time sigma-delta modulation.

Acronyms

$\Delta\Sigma$M *Sigma-Delta Modulator*

BoM *Bill of Materials*

BW *Bandwidth*

CMOS *Complementary Metal-Oxide Semiconductor*

CMRR *Common-mode rejection ratio*

CT *Continuous-time*

DAC *Digital-to-Analog converter*

EMI *Electromagnetic interference*

FFT *Fast Fourier Transform*

IC *Integrated Circuit*

KCL *Kirchoff's Current Law*

LC *Inductor-capacitor*

MOSFET *Metal-Oxide Semiconductor Field-Effect Transistor*

opamps *Operational amplifier*

OSR *Oversampling ratio*

PA *Power amplifier*

PDM *Pulse-density modulation*

PWM *Pulsed Wave Modulation*

RC *Resistor-capacitor*

SMD *Surface-mount device*

SNDR *Signal to Noise-plus-Distortion Ratio*

THD *Total Harmonic Distortion*

TTL *Transistor-transistor logic*

VCM *Common-mode voltage*

VDVS *Voltage depended voltage source*

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Chapter 1

Introduction

1.1 Motivation and Background

The acquisition, modulation and reproduction of audio signals were among the first electronics applications. They started in 1906 with the first audio amplifier which came in form of triode vacuum tubes, designed by Lee De Forest, which was vital to the first Amplitude Modulation (AM) radio [DF07]. Transistors soon replaced this technology due to their low power dissipation, low size, higher energy-efficiency and their low price.

In a conventional transistorized amplifier, the output stage drains a constant continuous current in order to polarize the output transistors, even in idle operation, since they need to be in the triode region to achieve great linearity. The most typical audio amplifier topologies, which includes Class A, B and AB, share this characteristic. Although having a great linearity and audio characteristics can be a huge benefit, Class AB amplifiers can only achieve a maximum theoretical efficiency of 78.5% at full power, which is a severe drawback, taking into consideration that audio amplifiers play a big role regarding power consuming in electronic systems [SS04].

In Class D amplifiers the output stage devices operate as switches, using Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) in the cut-off and triode region, thus not requiring a constant biasing current as the previous topologies. This results in a small drain-to-source voltage drop when the output MOSFETs are conducting, causing the dissipated power by the amplifier to be close to zero. This will require less power from the power supply and smaller heat sinks for the amplifier, thus achieving a theoretical

power efficiency of 100% [DD96].

The sound quality of Class D amplifiers is often compromised by the modulation technique applied to the analog input signal, regardless the output stage design. This modulation, which converts the analog signal into digital, can be accomplished in a different number of ways, provided the input signal can be reconstructed from its digital representation with a low-pass filter. Common techniques include, for instance, Pulse-Width Modulation (PWM) and Pulse-Density Modulation (PDM), which can be achieved with the use of Sigma-Delta Modulators ($\Delta\Sigma$M). In order to achieve an audio performance comparable to other classes, the modulation complexity has to increase.

The Class D amplifier output stage will also introduce non-linearities in the system, degrading the audio quality of the output signal. These depend mainly on the output stage configuration, which can be half-bridge or full-bridge (H-bridge), and the quality of the output switching [Ber03b]. These non-linearities can nonetheless be reduced by including the output stage in the feedback loop of the $\Delta\Sigma$M, in order to correct the output stage errors. The output stage should amplify the digital signal received from the modulator with low power dissipation and high fidelity.

The field of application of Class D audio amplifiers can be broadly divided into two areas, low power and high power output. The low power output are aimed to be included in portable applications such as mobile phones and laptops, that are very battery dependable, and the power output is generally around a few milliwatts. The high power output application include power-amplifiers (PA) systems and home theatres. Class D audio amplifiers generally come as a single Integrated Circuit (IC) chip, with or without a separate output stage. Due to their complexity the ICs are not fully disclosed and they are not very instructive to those planning to design a discrete Class D amplifier [Sel12].

The objective of this thesis is to design a discrete Class D audio power amplifier based on an optimized continuous-time (CT) 5^{th} order $\Delta\Sigma$M, with 1-bit and with 1.5-bit quantization schemes. Another goal of this thesis is explore design options concerning the implementation of the $\Delta\Sigma$M and the discrete power output stage. As a motivational factor, this will allow to implement different versions, topologies and bypass real-life problems. An implementation histogram of this thesis can be reviewed in the appendix section.

1.2 Thesis Organization

The presented thesis is organized in 6 chapters, including this introductory one. The chapter 2 introduces the conceptual description of a Class D audio amplifier, the most common used modulation techniques and describes the power output stages topologies, major causes of distortion, power losses and how to include the output stage inside the feedback path when 1.5-bit quantization scheme is used.

The following chapter, chapter 3, presents the proposed power output stage design. The used architecture for the high side gate driver allows the power output stage to be scaled to any power supply voltage level. This chapter also presents a theoretical analysis which describes the relative power consumption of the high side gate driver relatively to the power delivered to the load.

In the forth chapter, chapter 4, electrical simulations are performed taking into consideration the power output stage described in chapter 3, which is used with a 5^{th} order $\Delta\Sigma$M with 1-bit and 1.5-bit quantization scheme, at a switching frequency of 1.60 MHz. The electrical audio performance and power efficiency of the system is also analysed in this chapter, taking into account the non-linearity effects presented in chapter 2.

The two Class D audio amplifier prototypes, with 1-bit and with 1.5-bit quantization schemes are measured in chapter 5, which presents and summarizes their experimental results. The sixteenth and last chapter draws some conclusions and presents a comparison between the electrical and measured results. Some further possible research suggestions are also presented.

The appendix section reviews the prototyping histogram that was developed during the writing of this thesis. Among with some testing circuits, all $\Delta\Sigma$Ms prototypes are presented, along as some different modules of the Class D power output stage and a 5-V small power output stage prototyped for debug and testing purposes.

1.3 Contributions

The main contribution of this thesis is to study, design and implement a simple and power efficient fully-differential Class D audio power amplifier with discrete components. The

development of this thesis allowed the author to develop soldering and PCB manufacturing skills, mainly through CNC machining. Besides technical skills, this thesis also provided the contact with real life problems that are hidden from the electrical simulation world. Nonetheless, the most important contribution was the opportunity to be part of a project that went through every stage - design, electrical simulation and experimental validation.

The power output stage presented in Chapter 3 with an optimized 1.5-bit 3^{rd} order CT $\Delta\Sigma$M originated a paper [LMP13] that has been orally presented and awarded ***Best Paper Award*** in the field of Electronics and Telecommunications, presented at the 4^{th} Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS).

Chapter 2

Class D Audio Amplifiers

2.1 Conceptual Description

The Class D audio amplifier in open-loop configuration can be conceptually described using the block diagram presented in Fig. 2.1.

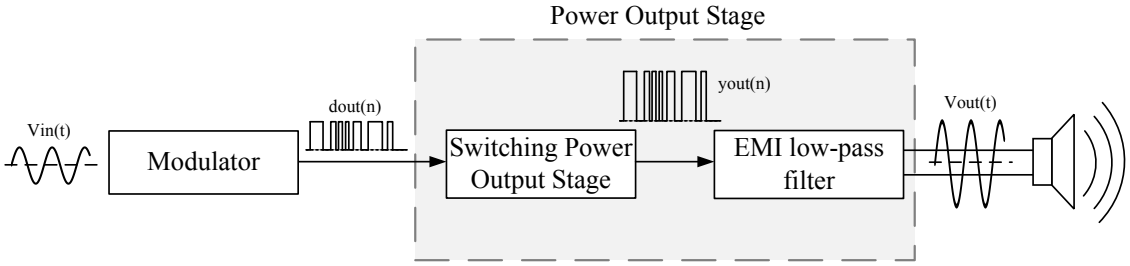


Figure 2.1: Conceptual Class D audio power amplifier

The first stage, the signal modulator, encodes the analog input audio signal into a binarized format, $d_{out}(n)$. This can be achieved using different modulation techniques, typically PWM or PDM. The two-level (1-bit) signal is then amplified by the switching power output stage and then filtered by an Electromagnetic Interference (EMI) low-pass filter which has a cutoff frequency inside the audio band, demodulating the digitized signal into an analog signal, $v_{out}(t)$, which can drive the loudspeaker at a higher volume. The applied low-pass filter will not only minimize the EMI but also avoid driving the loudspeaker with too much high frequency energy content.

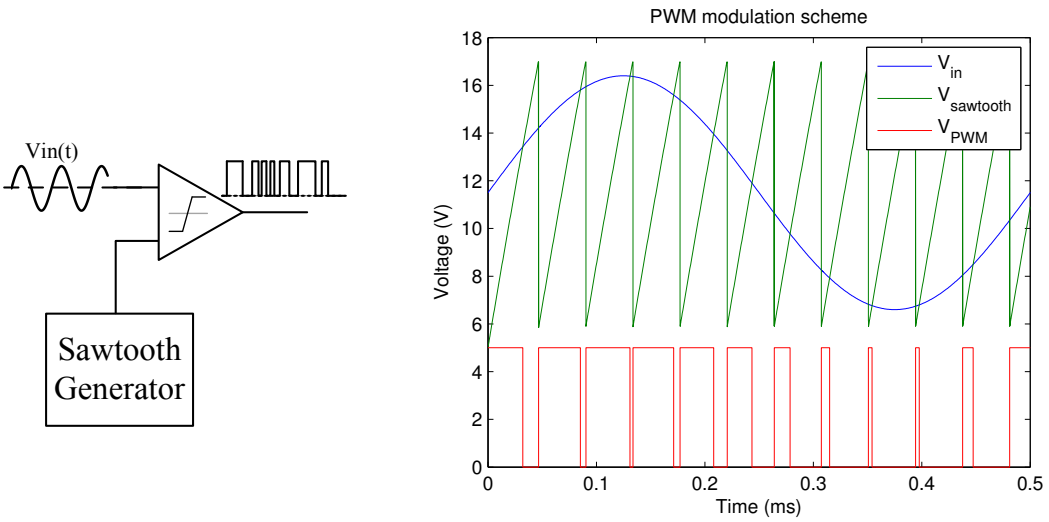
Each stage will be reviewed throughout the presented chapter.

2.2 Signal Modulation Techniques

Any signal modulator that encodes the audio signal into a stream of pulses can be used in a Class D audio amplifier, as these are amplified by the power output stage. Generally, the pulse widths are correlated with the signal amplitude and the spectrum includes the desired audio signal plus some high frequency content, which results from the modulation.

2.2.1 Pulse Width Modulation

The most popular and common modulation technique used in Class D audio amplifiers is PWM, mainly due to its conceptual simplicity [BBH04]. The audio information is encoded in the duty-cycle of a 2-level signal, which increases with a positive input, and decreases with a negative input. The digital signal is amplified by the output stage, which will deliver more power to the load with an higher duty-cycle and less power to the load with a lower duty-cycle. Fig. 2.2 shows an example for the PWM modulation with an exaggerated slow sawtooth input wave.



(a) PWM generator schematic (b) PWM modulation waveforms

Figure 2.2: PWM modulation example

The PWM compares the input signal with a triangular waveform that runs at a constant slope and carrier frequency, creating a stream of pulses with a frequency several times higher than the desired audio band. Although the concept is fairly simple, the PWM

technique has some disadvantages. It requires a highly linear sawtooth wave generator as any variation in the frequency or amplitude of the sawtooth wave will introduce distortion. Depending on the carrier frequency some multiples of the modulation frequency can even fall inside the AM radio band, creating EMI distortion and increasing the THD. It can even easily collapse the speed-limited output stage at full power, when using a close to zero duty-cycle, creating pulses in the order of nano-seconds.

2.2.2 Pulse Density Modulation

In PDM, unlike PWM, the input signal amplitude is not encoded into pulses with a defined frequency and variable duty-cycle. Instead, it is modulated in the relative density of the pulses, hiding the modulation frequency. PDM can be achieved by using ΔΣMs, which is an architecture of choice when concerning audio analog-to-digital converters (DAC) and therefore the design of these types of circuits is very well understood.

The output of the ΔΣM, which is typically a low resolution digital signal, has to be fed back and subtracted to the input signal. This can be easily achieved by adding the complementary output signal to the corresponding input signal, instead of subtracting it. The resulting error gets modulated and the successive approximations allows the ΔΣM to generate the digital representation of the input signal. Fig. 2.3 shows an example for this architecture, where a fully-differential 1^{st} order CT 1-bit ΔΣM is addressed and an example for the respective input and output waveforms are presented in Fig. 2.4.

Although having higher complexity than the PWM, PDM technique presents some advantages over PWM. The digital output stream rate is set by the clock applied to the sample-and-hold (S&H) block, usually implemented with a flip-flop D (FF-D) with complementary outputs. The clock signal can be a simple square wave implemented by a crystal oscillator and the signal applied to the FF-D comes from a comparator, which is simply comparing the V_{op} minus the V_{om} voltages with zero. The inherent feedback path allows a fully differential output stage to be directly inserted in the feedback loop and as the output signal is not depended on the duty-cycle the clock frequency does not appear in the spectrum. Nonetheless, it is conceptually harder to understand and requires a higher switching frequency in order to achieve the same theoretical performance as PWM.

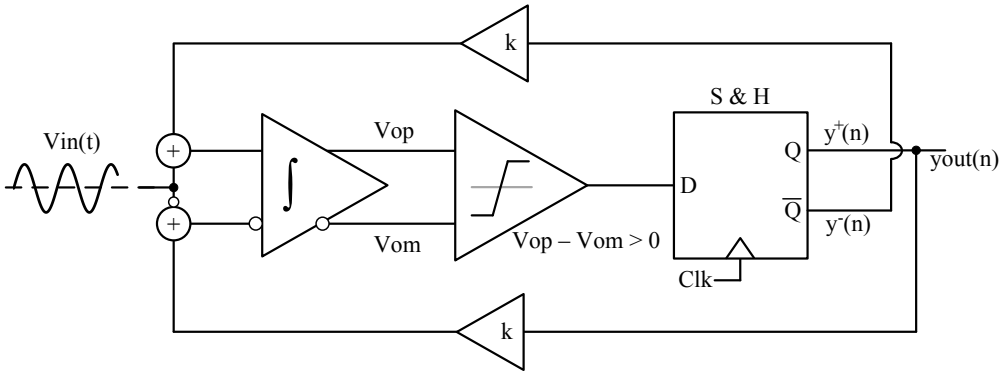


Figure 2.3: Fully differential CT 1^{st} order 1-bit $\Delta\Sigma$M

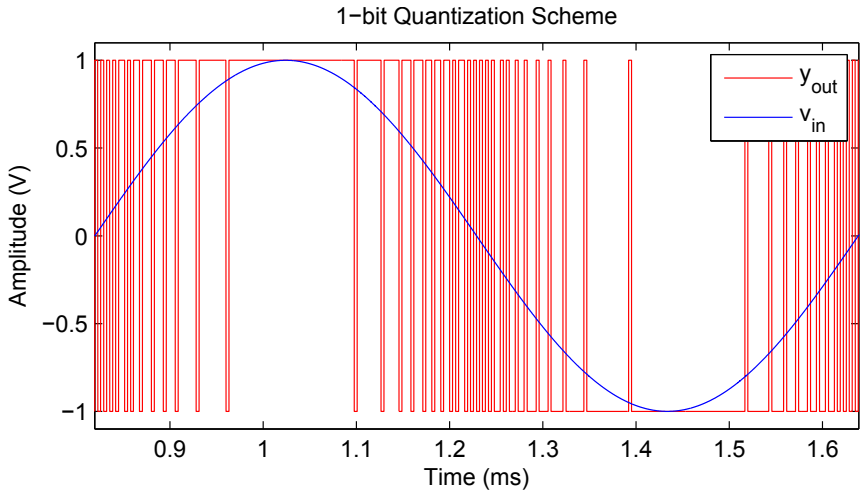


Figure 2.4: Example for a sinusoidal input and PDM output wave with 1-bit quantization scheme

2.2.2.1 1.5-bit Quantization Scheme

Although the $\Delta\Sigma$M also allows the use of n-bits, the most advantageous multibit quantization scheme regarding the Class D audio amplifiers is 1.5-bit quantization scheme, which means that the output stream would be +1, -1 or 0 (zero), where in the 0-state no current is delivered or sank from the output. This quantization scheme, which generates a 3-level digital signal and comes with an increased complexity, has a few advantages over the 1-bit quantization scheme. Nonetheless, the use of an 1.5-bit quantization scheme challenges the fully differential nature of the $\Delta\Sigma$M, as the feedback also has to be 1.5-bit [LLC08].

Adding a new quantization level will increase the modulator stability and greatly reduce the number of transitions and optimize the dissipated power, by only delivering energy to the load when necessary. This will allow to increase the sampling frequency of

the modulator without compromising its efficiency. In addition, increasing the modulator frequency will actually increase the resolution of the signal, improving its performance.

Keep in mind that the fully differential CT 1^{st} order 1.5-bit $\Delta\Sigma$M depicted in Fig. 2.5 generates four digital signals, y_1^+, y_1^-, y_2^+ and y_2^-. As the output stream, defined by y_{out} = y_1^+ - y_2^+ is 1.5-bit, the feedback also has to be 1.5-bit. This can be achieved by adding the complementary signals to the output with half the weight.

The threshold value, V_t, will define the range where there should be a 0-state. When the signal V_{op} - V_{om} is between V_t and -V_t the output is zero, so no energy is delivered or sank. When this signal is higher than V_t the $\Delta\Sigma$M will produce the logic level +1 and when is lower it will produce the logic level -1. The Table 2.1 presents the quantization and codification scheme and the Fig. 2.6 shows a practical example of the codification. An example for the output waveforms of the $\Delta\Sigma$M depicted in Fig. 2.5 is also presented in Fig. 2.7.

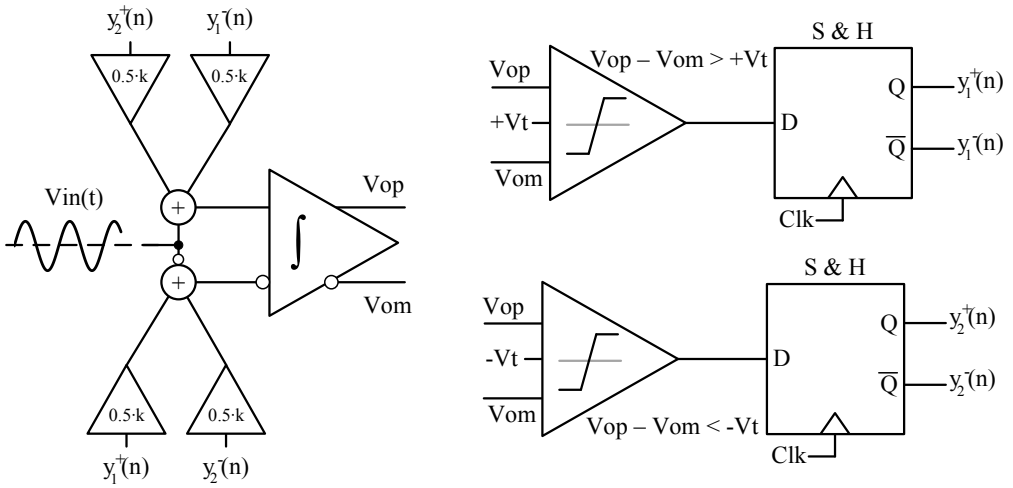
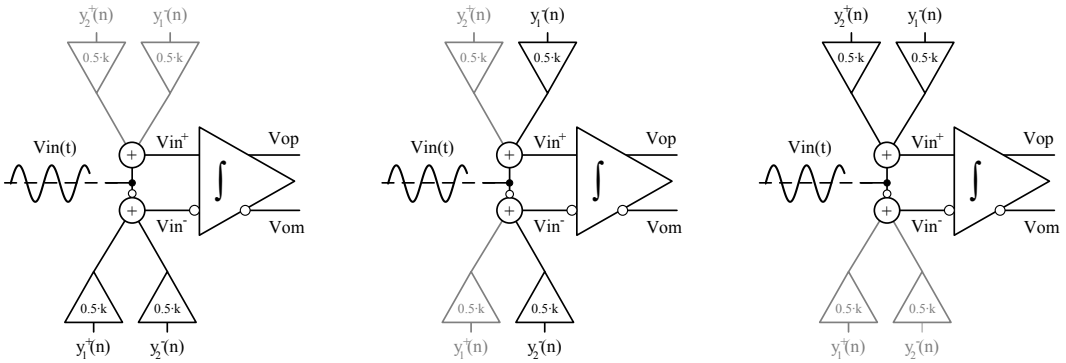


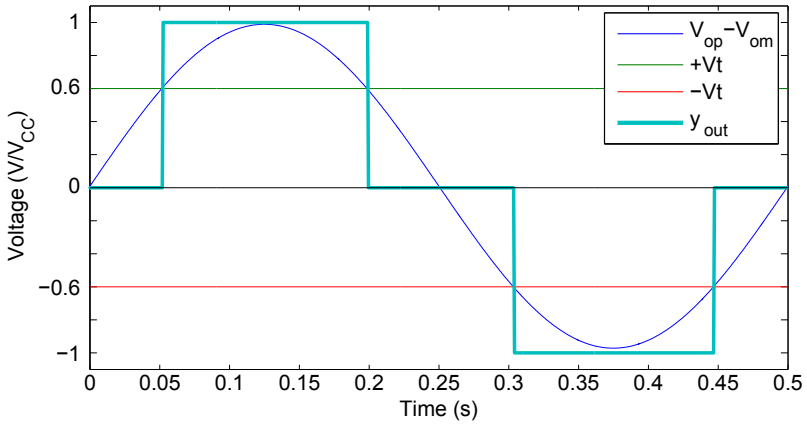
Figure 2.5: Fully differential CT 1^{st} order 1.5-bit $\Delta\Sigma$M

Bit	Condition	Y_1^+	Y_2^-	Y_2^+	Y_1^-	$Y_{out} = Y_1^+ - Y_2^+$
+1	$V_{op} - V_{om} > +V_t$	1	1	0	0	1
0	$+ Vt > V_{op} - V_{om} > -V_t$	0	1	0	1	0
-1	$-Vt > V_{op} - V_{om}$	0	0	1	1	-1

Table 2.1: 1.5-bit quantization scheme and its codification



(a) +1 bit (b) 0 bit (c) -1 bit



(d) 1.5-bit quantization scheme; V_{op} - V_{om} wave (blue), $+V_t$ (green), $-V_t$ (red), Y_{out} (cyan)

Figure 2.6: +1, 0 and -1 states and the amount of feedback that is injected into the modulator

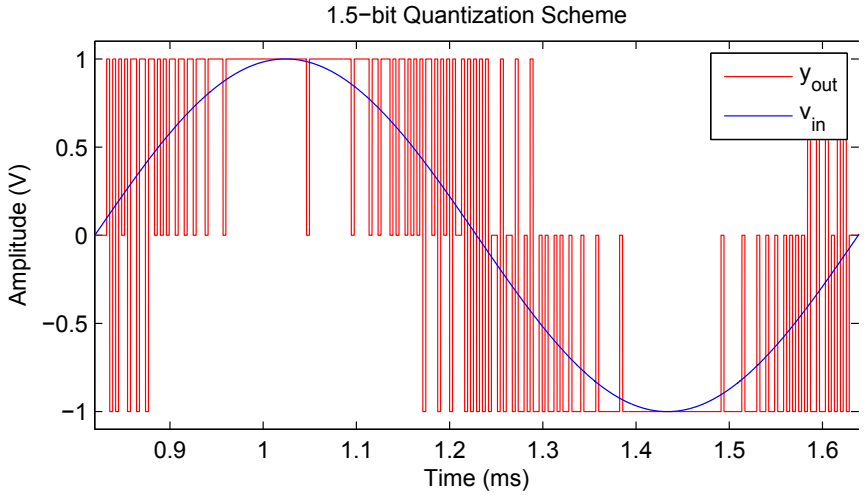


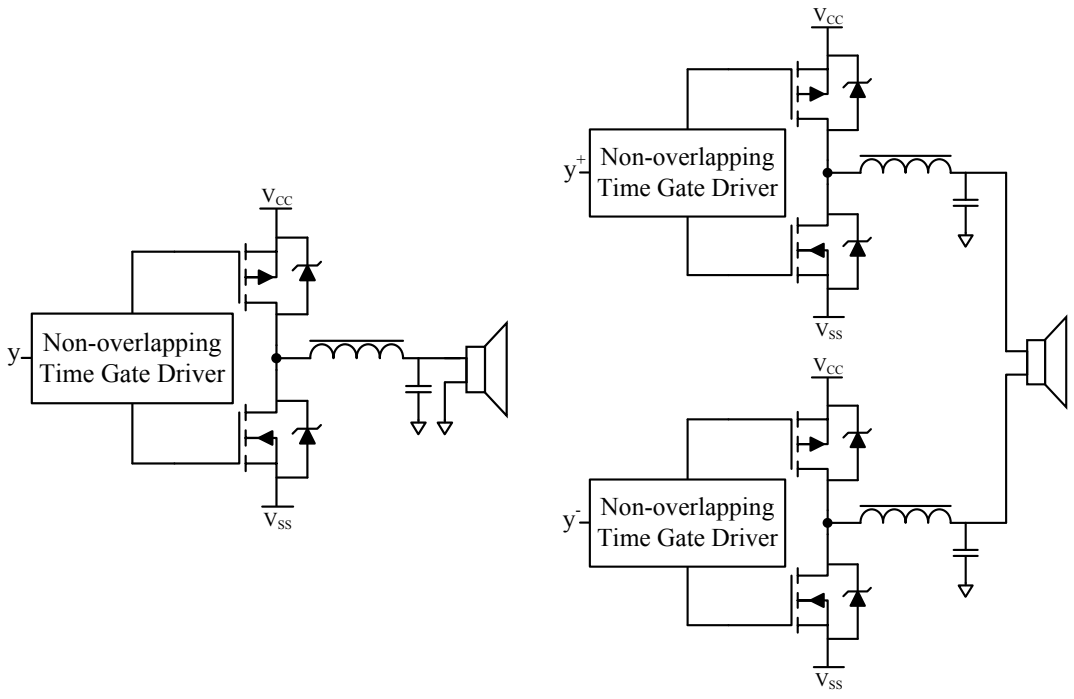
Figure 2.7: Example for a sinusoidal input and PDM output waveforms with 1.5-bit quantization scheme

2.3 Power Output Stages

Class D audio amplifiers take advantage of their switching nature to maximize their power efficiency. Theoretically, the power output stage will either deliver full or zero power to the load, almost only dissipating energy in the transitions. This is done using two low-ohmic switches, implemented by power MOSFETs, which alternatively connect the output node to the positive or negative supply rail, producing a train of voltage pulses. As the power MOSFETs have zero current when they are not conducting and a small V_{ds} voltage drop when conducting, this results in a near zero $V_{ds} \times I_{ds}$ product which translates in low power dissipation during conduction.

2.3.1 Output Stages Topologies

The Class D audio amplifier output stage can be implemented using either an half-bridge or full-bridge (H-bridge) configurations, as represented in Fig. 2.8, where the power output MOSFETs are in a PMOS-NMOS totem-pole arrangement. The non-overlapping time gate driver circuit is used to synchronize the switching and to drive power output MOSFETs.



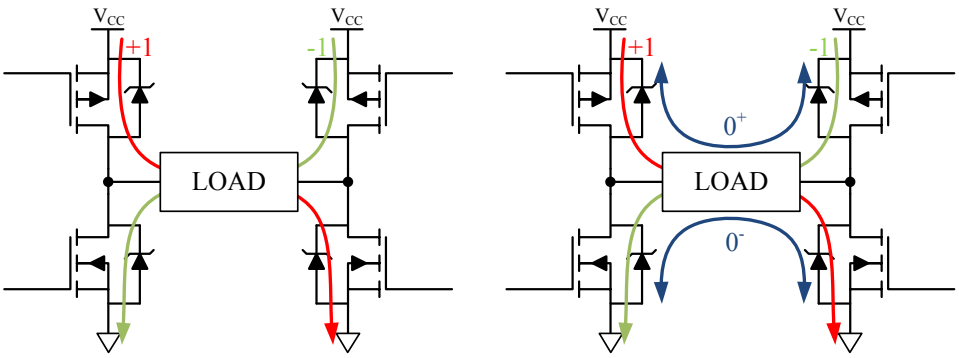
(a) Half-bridge configuration (b) H-bridge configuration

Figure 2.8: Class D output stage topologies

An half-bridge is consisted by two power MOSFETs and an output EMI low-pass filter, usually implemented using a passive inductor-capacitor (LC) low-pass filter, while a H-bridge is consisted by two half-bridges. Although having increased complexity and requiring two times the necessary devices than in an half-bridge configuration, the H-bridge configuration is generally implemented with a single power supply (V_{DD}) with ground used as the negative power supply (V_{SS}), contrary to the half-bridge which generally requires two power supplies (V_{DD} and -V_{DD} as V_{SS}). The half-bridge can also be implemented with a single power supply, but it will require a DC blocking capacitor in order to remove the $V_{DD}/2$ offset across the loudspeaker.

The use of a H-bridge enables the use of a differential nature, where it is possible to deliver twice the power supply voltage to the load with zero offset (which theoretically means deliver four times the maximum output power), cancel out even order harmonic distortion and enable the use of an 1.5-bit quantization scheme. This is done due to the fact that the load is considered floating. The use of 1.5-bit quantization scheme will also decrease the switching activity which consequently also decreases the EMI and the dissipated power.

The Fig. 2.9 shows the used quantization scheme for the 1-bit and 1.5-bit when a H-bridge is used. Both the 0^+ and 0^- in the 1.5-bit quantization scheme represents the logic level zero, where no voltage drop is applied to the load.



(a) 1-bit quantization scheme (b) 1.5-bit quantization scheme

Figure 2.9: H-Bridge with 1-bit and 1.5-bit quantization scheme

2.3.2 Major Causes of Distortion

Ideally, a Class D power output stage should have no distortion, generate zero noise in the audible band and have 100 % power efficiency. In practical, there are several causes of non-linearity and distortion in a Class D power output stage. Nonetheless, as some of them can be easily pinpointed, they can also be reduced with careful design. Fig. 2.10 illustrates some of the major causes which can be identified as:

- Non-linearities in the modulator
- Timing errors added by the switching output stage
- Unwanted characteristics in the switching devices, such as finite $R_{ds}(on)$ and switching speed
- Parasitic components that cause ringing on transient edges
- Power supply voltage fluctuations due to their finite output impedance
- Non-linearity in the output EMI low-pass filter

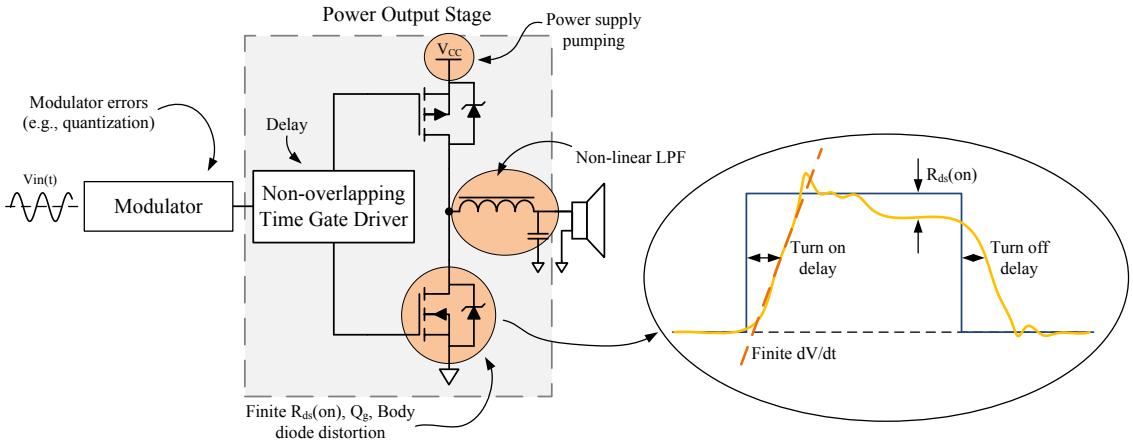


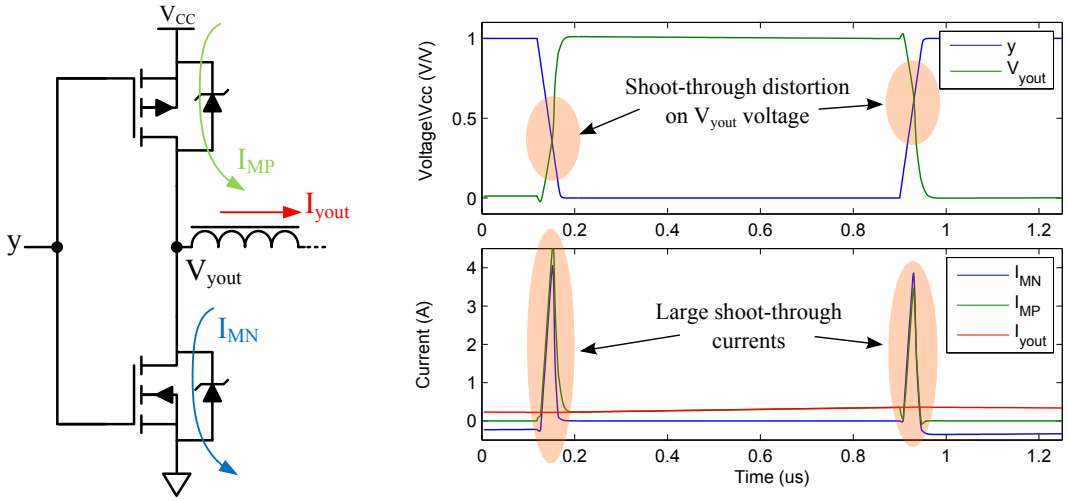
Figure 2.10: Class D audio power amplifier and its major causes of distortion

2.3.2.1 Shoot-Through current

In Fig. 2.10 the non-overlapping time gate driver circuit is used to synchronize the PMOS and the NMOS switching, in order to prevent them to be simultaneous on. By limiting

the cross-talk between them, as this would create a short-circuit path between the power supply and ground, will optimize the power dissipation. The short-circuit effect is called shoot-through current and can cause large current spikes which will degrade the output signal and eventually permanently destroy the power output MOSFETs. Fig. 2.11 shows an example for the transitory waves where the same control signal is considered, and Fig. 2.12 shows the same transitory waves while using synchronized switching.

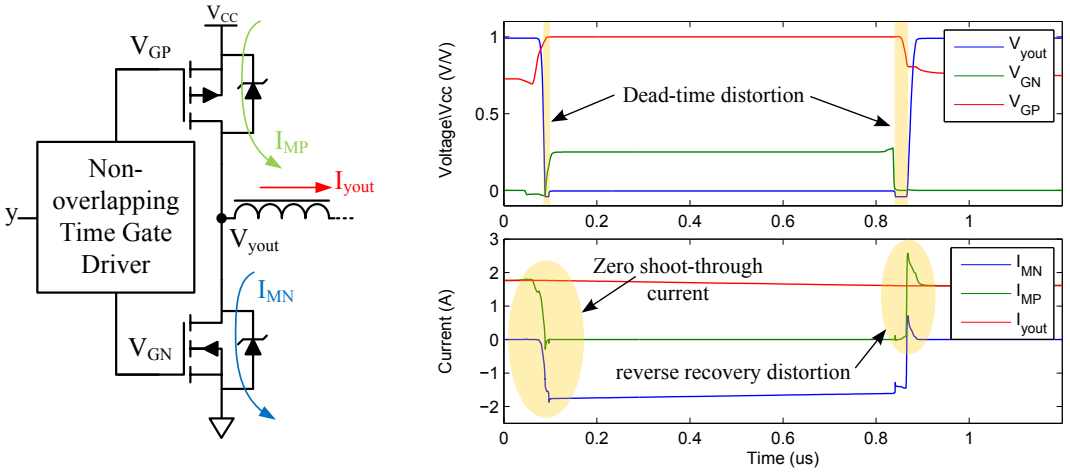
By synchronizing the control signals (V_{GP} and V_{GN}), the shoot-trough current can be cancelled, maximizing the power efficiency in the transitions. This will nonetheless cause dead-time distortion, as there is a period where both transistors are turned off. The effect called reverse recovery which appears in Fig. 2.12(b) will be discussed in subsection 2.3.2.4.



(a) Half-bridge with no non-overlapping gate drive

(b) Transitions waveforms; top: V_{yout} node voltage, y node voltage; bottom: I_{MP} current, I_{yout} current and I_{MN} current

Figure 2.11: Transition waveforms with the same control signal



(a) Half-bridge with non-overlapping time gate drive

(b) Transitions waveforms; top: V_{yout} node voltage, V_{GP} node voltage and V_{GNP} node voltage; bottom: I_{yout} current, I_{MP} current and I_{MN} current; the reverse recovery phenomenon is presented in chapter 2.3.2.4

Figure 2.12: Transition waveforms using synchronized switching

2.3.2.2 Dead-Time distortion

By introducing synchronized switching in the power output stage there will be a transitory period where both M_P and M_N will be in the cut-off region, meaning that the output node, V_{yout}, will be floating. This transitory is called dead-time and although the power consumption will significantly decrease, dead-time is one of the most dominant sources of distortion in Class D audio amplifiers, and thus should be minimized [Ber03a].

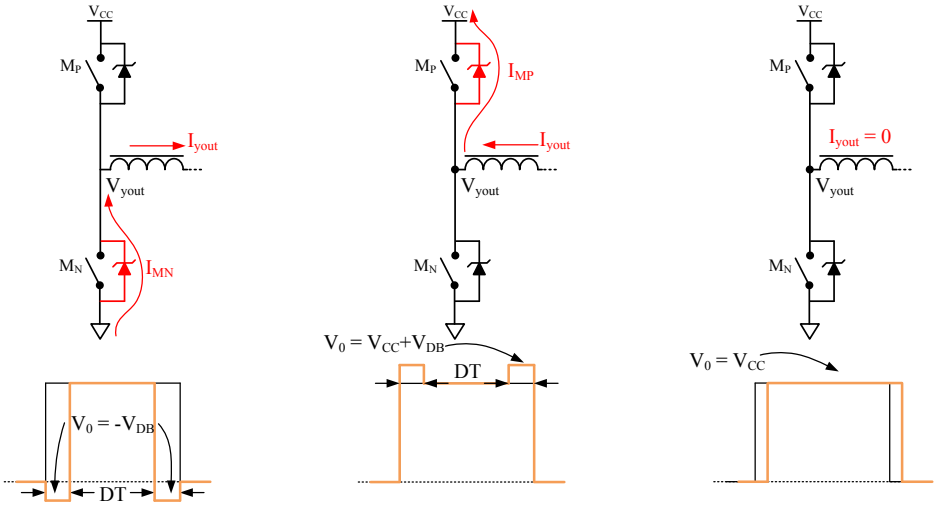
Since output EMI low-pass filter, implemented as a passive LC low-pass filter, is connected to the V_{yout} node, the filter's inductor will force a continuous output current during the dead-time that will have to flow through either one of the back-gate diodes, as the transistors are turned off [Ber03b]. Fig. 2.13 shows an example for the dead-time distortion, where the dead-time distortion in the output node can be recognized by the small rectangular distortions on the output signal, which are caused by the forward bias voltage of the back-gate diodes.

Considering that the output current, I_{yout}, is flowing towards the load (refer to Fig. 2.13(a) where $I_{yout} > 0$) and that V_{yout} has ground voltage level, then when transistor M_N switches off prior to the low to high transition the M_N's back-gate diode will be

forwardly biased and produce a V_{yout} voltage equal to ground minus its biasing voltage during the dead-time period. When V_{yout} is V_{CC} and M_P turns off (during the V_{yout} transition from high to low) the V_{yout} node will be immediately pushed-down due to the M_N's back-gate diode that gets forwardly biased due to the I_{yout} current.

The opposite will occur if we consider that I_{yout} is flowing from the load (Fig. 2.13(b)), but this time its the M_P's back-gate diode that gets forwardly biased. If the I_{yout} is zero (Fig. 2.13(c)) then V_{yout} will simply present a time delay. Hence, the following set of equations can be drawn and remain valid for both the half-bridge and the H-bridge configurations during the dead-time period:

$$V_{yout} = \begin{cases} -V_{BackGateDiode} & if\, I_{yout} > 0 \\ V_{CC} + V_{BackGateDiode} & if\, I_{yout} < 0 \\ V_{CC} & if\, I_{yout} = 0 \end{cases} \tag{2.1}$$



(a) $I_{yout} > 0$ (during dead-time) (b) $I_{yout} < 0$ (during dead-time) (c) $I_{yout} = 0$ (during dead-time)

Figure 2.13: Dead-time distortion on V_{yout} node due to the back-gate diode forwardly biased; V_{yout} node voltage (orange)

2.3.2.3 Power Supply Distortion

An ideal power supply has zero internal resistance and has the capability to deliver and sink infinite current. Since the Class D amplifier has a switching nature, the current drained from the power supply also has the same switching nature. This will cause distortion due to the finite characteristics of a power supply, making the voltage level float around its nominal value.

This will create two types of distortion, a low frequency effect called power supply pumping and an high frequency effect that is caused due to the R_{ds}(on) of the output power MOSFET and the internal resistance of the power supply.

Power supply pumping distortion

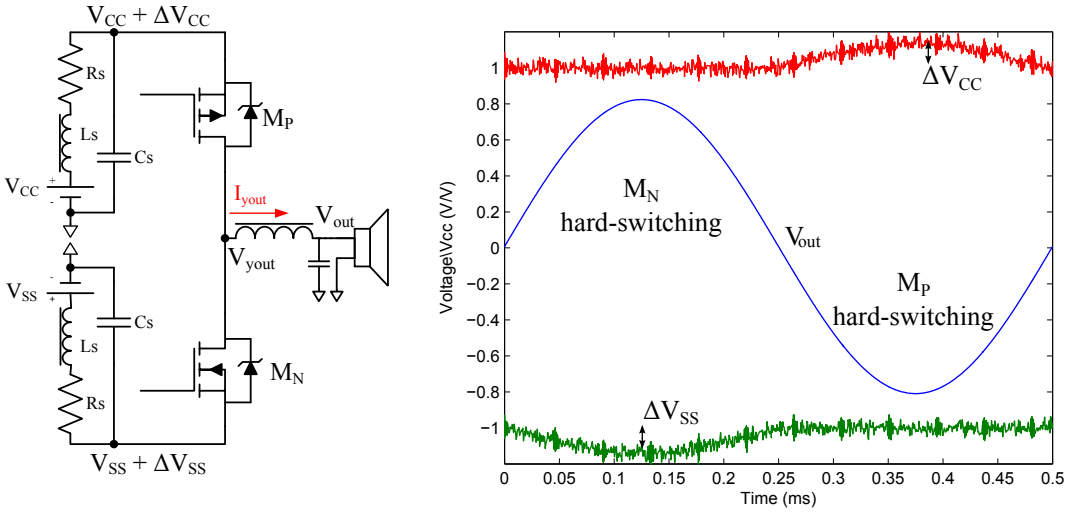
Power supply pumping distortion occurs when the energy store inside the inductor from the EMI low-pass filter is fed back to the power supply. As the power supply has no way to absorb the energy that is being returned, its voltage level can be pumped beyond its nominal value and sometimes can even achieve the maximum absolute rating of the output MOSFETs, permanently destroying them. This type of distortion is a known characteristic of the half-bridge topology.

Fig. 2.14 shows an example where power supply pumping occurs in an half-bridge output stage. As the I_{yout} current is defined by the inductor from the low-pass filter, when M_L tries to hard switch the direction of the current this current is fed back to the power supply through its back-gate diode. Due to its internal resistance the nominal value of the V_{SS} power supply is pumped up. The opposite will occur during the V_{yout} node voltage's negative arcade.

The H-bridge topology does not suffer from this type of distortion because the output current that flows from one inductor will also flow from the other, creating a local current loop that minimally disturbs the power supplies. This will occur as long as the same power supply is used for both half-bridges. This effect can be reduced by using an 1.5-bit quantization scheme which will present less power supply distortion than the 1-bit quantization scheme due to the fact that only one half-bridge is switching at a time. Fig. 2.15 shows an example for the 1.5-bit quantization scheme, where the power supply

is minimally disturbed when the V_{yout} voltage is crossing zero and hard-switching occurs, inject current into the power supply.

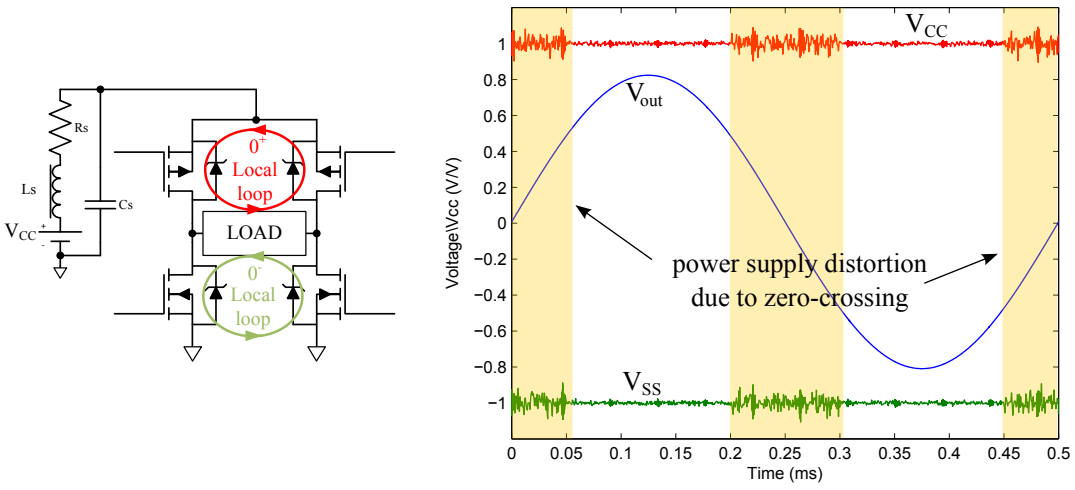
These problems can be bypassed by carefully selecting a wide variety of capacitors to efficiently decouple the power supply.



(a) Half-bridge with non-ideal power supplies

(b) Power supply pumping distortion with low-frequency input; V_{yout} as blue, V_{CC} as red and V_{SS} as green

Figure 2.14: Power supply pumping distortion example in half-bridge configuration



(a) Half-bridge with non-ideal power supplies

(b) Power supply pumping distortion with low-frequency input; V_{yout} as blue, V_{CC} as green and V_{SS} as red

Figure 2.15: Power supply pumping distortion example in H-bridge configuration with 1.5-bit quantization scheme

Finite MOSFET R_{ds}(on) distortion and internal power supply resistance

Due to the finite R_{ds}(on) resistance from the output MOSFETs and the current flowing from the power supply, the V_{ds} voltage drop will not remain constant, introducing distortion. The Fig. 2.16 shows an example where as the output current that flows from the power output MOSFETs increases, the V_{ds} voltage drop will also increase. This will affect the voltage level applied to the load and, if the output stage is inserted in the feedback loop of the modulator, the amount of feedback that is fed back into the modulator. This will nonetheless allow the modulator to correct this type of distortion.

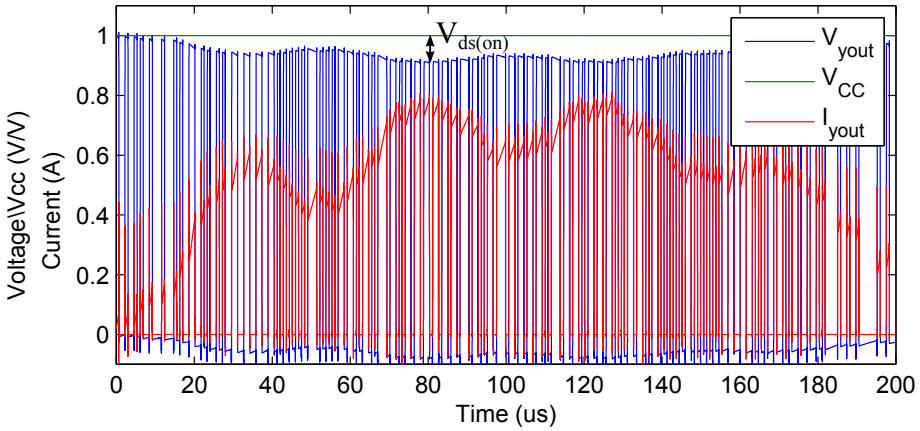


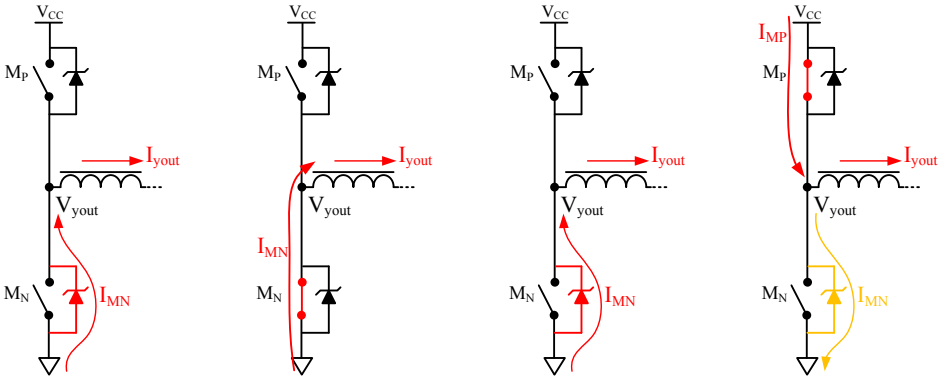
Figure 2.16: R_{ds}(on) distortion; V_{yout} as blue, V_{CC} as green and I_{yout} as red

2.3.2.4 EMI from reverse recovery

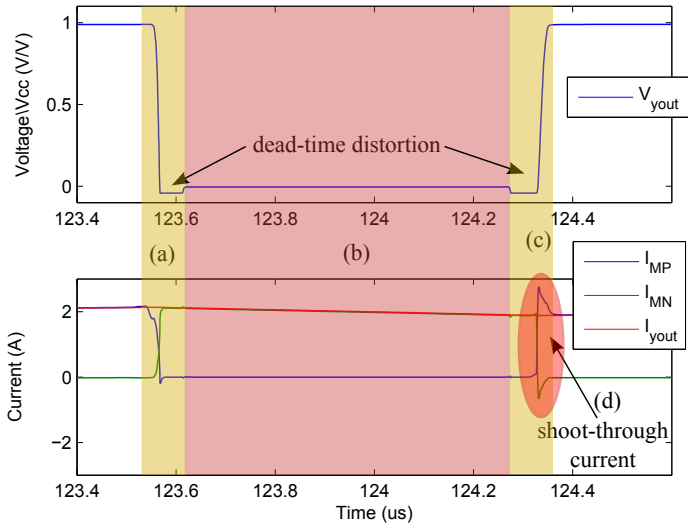
One of the major sources of EMI is associated with the back-gate diodes from the output MOSFETs where hard-switching (the output current counteracts the intended transition) is applied [Ber09, Ber03b]. This known phenomenon, called reverse recovery, can sometimes compromise the power output transistors and the power efficiency.

Consider the example from Fig. 2.17 where the I_{yout} current is conducting towards the load and that M_P is turned on. When the dead-time kicks in, M_P is turned off and the I_{yout} current starts flowing from the M_N's back-gate diode (a), thus pushing down the V_{yout} node to the negative supply rail almost immediately. After the dead-time the transistor M_N is turned on which bypasses its back-gate diode and the system behaves normally (b). At the end of the pulse the output stage enters again in dead-time. The M_N transistor is turned off forcing the I_{yout} current to be conducted through its back-gate

diode, creating dead-time distortion, until M_P is turned on (c). As V_{yout} node gets pulled up the voltage on the M_N's back-gate diode is reversed, and due to its minority charge stored in the diode there will be a fast and high short-circuit current between the power supplies, similar to the shoot-through current, that will last as long as the stored charge is not flushed out (d). The same will occur during the V_{yout} high to low transition when $I_{yout} < 0$.



(a) During dead-time (b) NMOS turned on (c) During dead-time (d) Reverse recovery



(e) Transitory waveforms

Figure 2.17: Reverse recovery phenomenon

2.3.3 Output Stage Protection techniques

Most of the Class D audio amplifiers implemented in IC technology have integrated protection circuits, that will turn the device off before they achieve hazardous operating points,

such as high output currents or temperatures [Sel12, Ber03c].

Some of the protection circuits are:

1. Overheating detection
2. Excessive current flow in the output transistors detection (indicating short-circuits, either from shoot-through current or malpractice)
3. Undervoltage detection; if the supply voltage falls too low then there may not be enough gate drive voltage to turn the output MOSFETs fully on which will dissipate excessive power.
4. Output transistor turn-on timing.

These type of protection circuits will add complexity to the system, increasing its costs and area.

2.3.4 Non-overlapping Time Gate Driver

The non-overlapping time gate driver is consisted by a dead-time generator circuitry, the high side gate driver and the low side gate driver, as depicted in Fig. 2.18. The dead-time generator circuitry synchronizes the high and low MOSFETs transitions, in order to prevent shoot-through current. The high side gate driver can be considered a level shifter, as typically the dead-time generator circuitry works with a Transistor-Transistor Logic (TTL) (5 V high logic level) or Complementary Metal-Oxide-Semiconductor (CMOS) logic (3.3 V high logic level) and it is necessary to level shift the logic signal to the V_{CC} voltage level, which can be several times the logic value.

Depending on the output stage topology and the power output MOSFETs totem-pole arrangement, both the high side and low side gate driver require different implementation topologies.

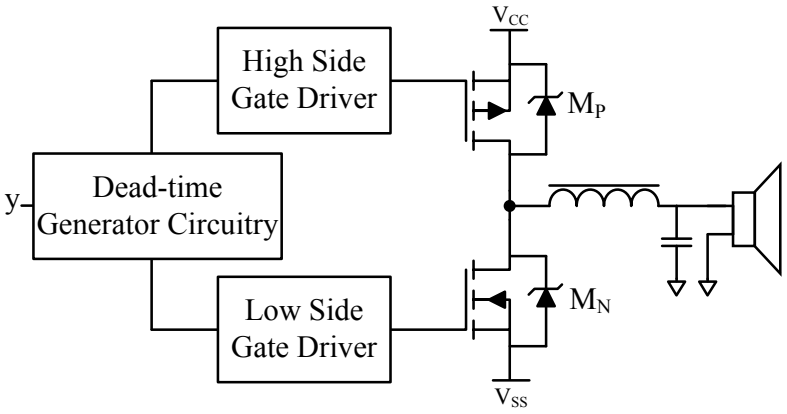


Figure 2.18: Switching control unit

2.3.4.1 Power output MOSFETs

In IC technology the output transistors are typically implemented using two identical NMOS transistors in a totem-pole arrangement. They are preferred because of their $R_{ON}\times$ Area product and low R_{DS} value, but require additional components and complexity in order to drive the high side NMOS transistor transitions. An illustrative example is presented in Fig. 2.19.

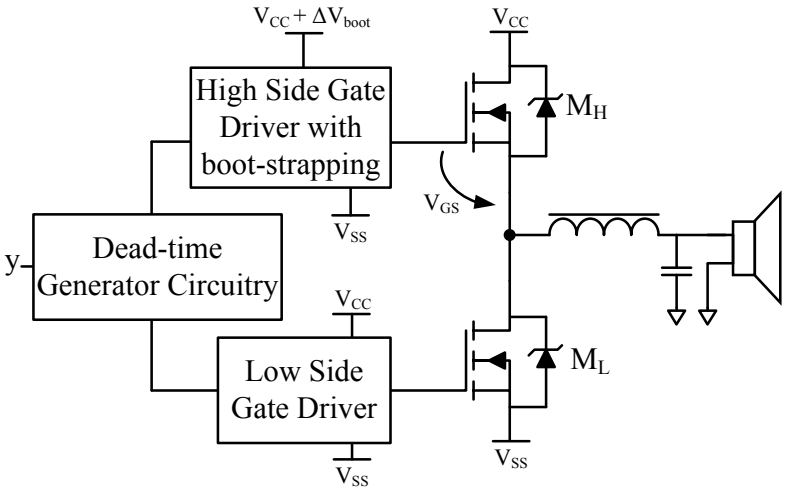


Figure 2.19: Simplified Class D output stage with an external bootstrap capacitor in a NMOS-NMOS totem-pole arrangement

Since a voltage level higher than the power supply is necessary in order to turn M_H on ($V_{gs} = V_g$ - $Y_{out} > V_{th}$), an additional bootstrap capacitor, C_{Boot}, serves as a floating power supply for the high side gate driver. This technique is known as boot strapping

technique [NKRA06].

The use of a PMOS-NMOS totem-pole arrangement serves the same purpose without the need for additional complexity, which simplifies the design. This can be an advantage, specially in discrete technology, where a simpler design can simplify the circuit design and still achieve a similar performance [YH08, MGM04].

2.3.4.2 Dead-time Generator

The dead-time generator, typically implemented as a non-overlapping circuit, serves to synchronize the power output transistors. There are two main variants: one where a fixed non-overlapping time circuit is used and the second, more complex, where an adaptive non-overlapping time circuit is used.

The fixed non-overlapping circuitry (utilized in e.g. [FWNS09] and depicted in 2.20) utilizes a constant dead-time, which can lead to a temperature and process dependency.

By monitoring the state of the output node, the high side, and the low side gate driver, it is possible to use a feedback in the non-overlapping time circuitry, achieving an adaptive non-overlapping time circuitry. This is done by using an handshake carousel, which can lead to increased complexity [Ber03b, Ber03a]. Fig. 2.21 illustrates an example of this architecture.

The Fig. 2.22 shows an example of the waveforms after the dead-time generation.

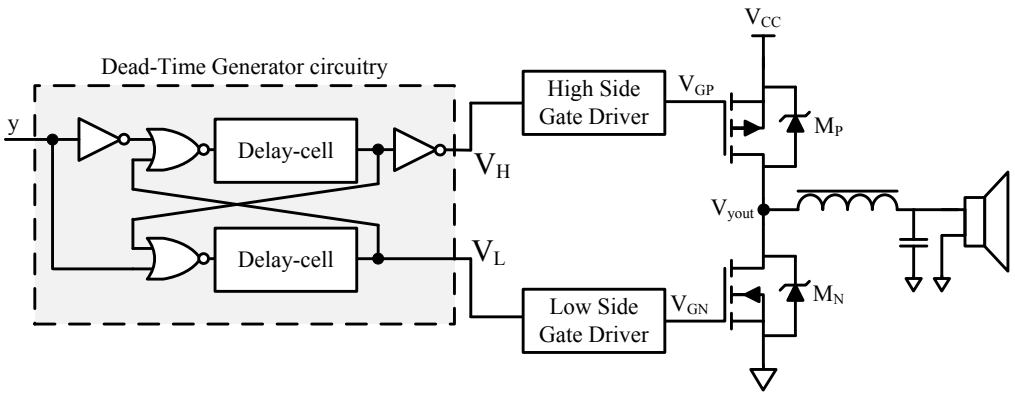


Figure 2.20: Non-overlapping time circuitry examples

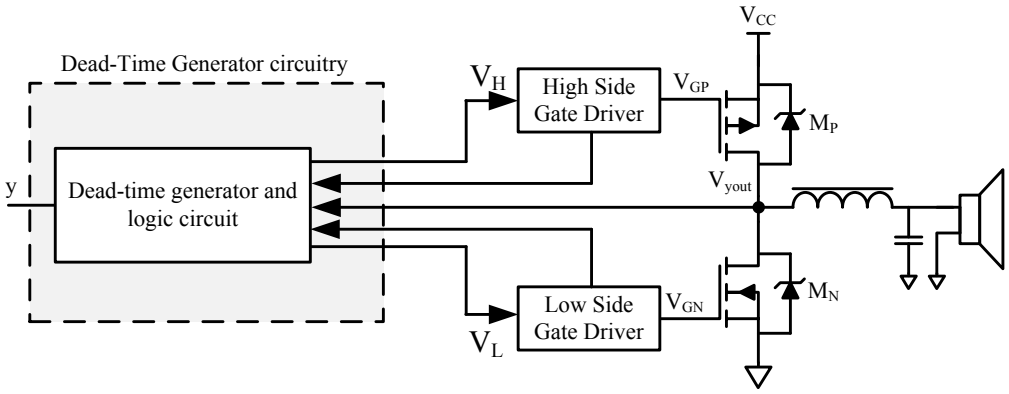


Figure 2.21: Adaptative non-overlapping time

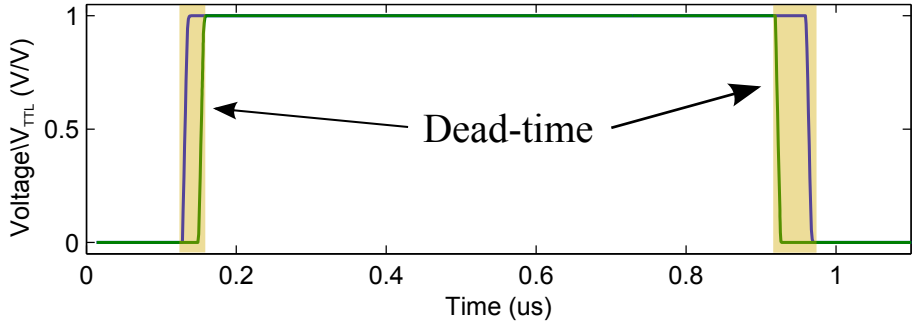


Figure 2.22: Transition waveforms example; V_H as blue and V_L as green

2.3.5 Output EMI Low-pass Filter Design

Since the loudspeaker and the human ear have a limited bandwidth, the quantization noise that comes from the digital signal is somewhat filtered when it arrives at the loudspeaker. Nonetheless, applying a high frequency energy to a loudspeaker can be potentially hazardous mainly due to the EMI. Even commercial systems often have strict regulation standards for the EMI (e.g. CISPR 22 or FCC Part 15 Class B) which they have to comply.

This required the need to implement a low-pass filter in order to remove the high frequency content of the signal. Although they could be easily implemented using active components (and achieve higher orders at lower cost), these would dissipate too much energy which would degrade the power efficiency.

2.3.5.1 Unity gain 2^{nd} order low-pass filter design

When regarding the audio band, it is necessary a flat magnitude response in order to avoid distortion, and this can be achieved with a Butterworth filter. The standard unity gain 2^{nd} order filter can be easily implemented using a simple inductor-capacitor (LC) structure, providing a -40 dB/dec slope attenuation and -3 dB at the cutoff frequency, with just two components and the load.

The standard unity gain 2^{nd} order filter transfer function can be written as:

$$H(s) = \frac{\omega_n^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{2.2}$$

The ω_n is the undamped natural frequency (rad/s) and Q is the filter's quality factor, which has to be $Q = 1/\sqrt{2} \simeq 0.707$ in order to have a critically damped response. Using an higher Q value will require extra current from the power supply at the cutoff frequency due to the undamped characteristic, and a lower Q will degrade the performance of the low-pass filter by creating a premature attenuation in the audio band (over damped response). Fig. 2.23 shows the bode plot with $1/\sqrt{2}$ quality factor and a normalized cut-off frequency.

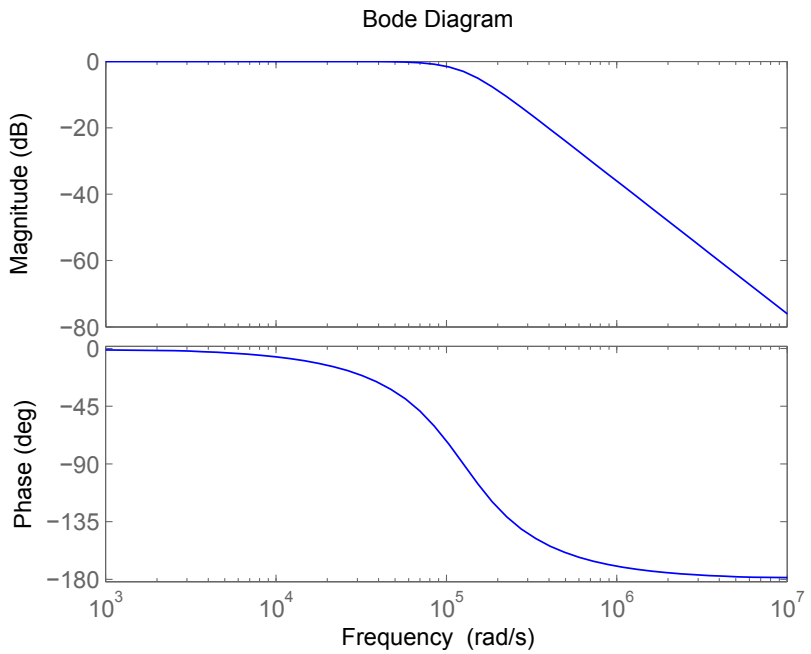


Figure 2.23: Bode diagram plot with $Q = 1/\sqrt{2}$ and a normalized cutoff frequency

2.3.5.2 Unity gain 2^{nd} order low-pass filter design applied to the half-bridge topology

Considering an half-bridge topology, the low-pass filter can be implemented using the LC structure depicted in Fig. 2.24, where the loudspeaker is simply represented as a resistive load, R_L.

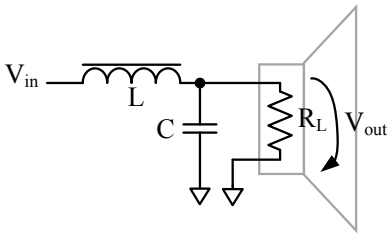


Figure 2.24: Unity gain 2^{nd} order LC low-pass filter structure for half-bridge topology

The circuit transfer function can be written as:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{1}{LC}}{s^2 + \frac{1}{R_L C}s + \frac{1}{LC}} \tag{2.3}$$

Rearranging Eq. 2.2 and Eq. 2.3, the following relationships can be drawn:

$$\omega_n = \frac{1}{\sqrt{LC}} \tag{2.4}$$

$$\frac{\omega_n}{Q} = \frac{1}{R_L C} \tag{2.5}$$

Assuming a constant and known R_L, Q and ω_n, the value for the inductor, L, and capacitor, C, can be derived as:

$$C = \frac{Q}{R_L \omega_n} \tag{2.6}$$

$$L = \frac{R_L}{Q \omega_n} \tag{2.7}$$

2.3.5.3 Unity gain 2^{nd} order low-pass filter design applied to the H-bridge topology

Doubling a single-ended filter it is possible to achieve a differential low-pass filter, as represented in Fig. 2.25.

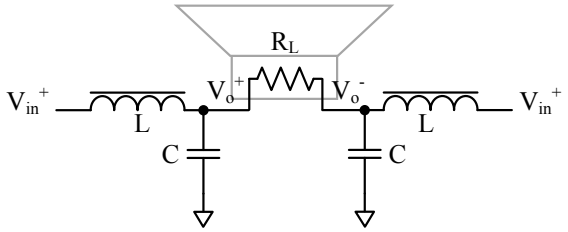


Figure 2.25: Unity gain 2^{nd} order LC low-pass filter structure for H-bridge topology

It is possible to derivate the circuit transfer function (App. A), which is given by:

$$H(s) = \frac{v_o^+(s) - v_o^-(s)}{v_{in}^+(s) - v_{in}^-(s)} = \frac{\frac{1}{LC}}{s^2 + s\frac{2}{R_L C} + \frac{1}{LC}} \tag{2.8}$$

Hence, it is possible to conclude the following relationships:

$$\omega_n = \frac{1}{\sqrt{LC}} \tag{2.9}$$

$$\frac{\omega_n}{Q} = \frac{2}{R_L C} \tag{2.10}$$

Which means that assuming a known R_L, Q and ω_n the inductor and capacitor can be computed as:

$$\begin{cases} C = 2\frac{Q}{R_L \omega_n} \\ L = \frac{1}{2}\frac{R_L}{Q\omega_n} \end{cases} \tag{2.11}$$

with additional capacitor C_E

By adding an additional coupling capacitor in parallel with the load, some high frequency content that is able to bypass the low-pass filter is bypassed by the C_E capacitor. This will force the v_o^+ node to follow the v_o^- node, and vice-versa, forcing the high frequency content to flow around the filter instead of being dissipated in the loudspeaker.

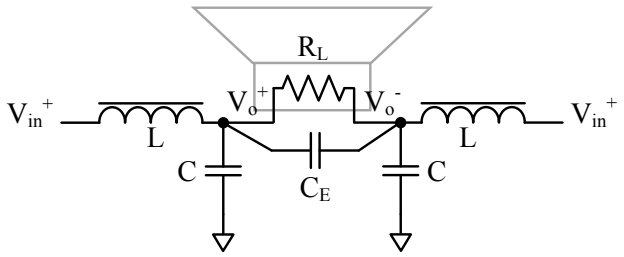


Figure 2.26: Output EMI filter with an additional external capacitor

The transfer function is

$$H(s) = \frac{v_o^+(s) - v_o^-(s)}{v^+(s) - v^-(s)} = \frac{\frac{1}{L(C+2C_E)}}{s^2 + s\frac{2}{R_L(C+2C_E)} + \frac{1}{L(C+2C_E)}} \tag{2.12}$$

Assuming that the same electrical charge (Q) as if in an half-bridge is desired then

$$Q = V_{out} \cdot C \Leftrightarrow Q = 2V_{out} \cdot C_E$$

hence, assuming $C = 2C_E$ and $C^* = C + 2C_E$, then following relationships arise:

$$\begin{cases} L = \frac{1}{2}\frac{R_L}{Q\omega_n} \\ C = \frac{Q}{R_L\omega_n} \\ C_E = \frac{Q}{2 \cdot R_L\omega_n} \end{cases} \tag{2.13}$$

2.3.6 Power Output Stage Losses

An ideal output stage would be able to deliver full power to the load without dissipating energy, translating into 100% power efficiency. Nonetheless, in a real system, there are power losses that cannot be avoided.

The power efficiency of a full Class D audio amplifier power output stage can be described as

$$Efficiency = \frac{P_{Load}}{P_{gate\ drivers} + P_{output\ transistors} + P_{EMI\ filter} + P_{Load}} \cdot 100\ (\%) \tag{2.14}$$

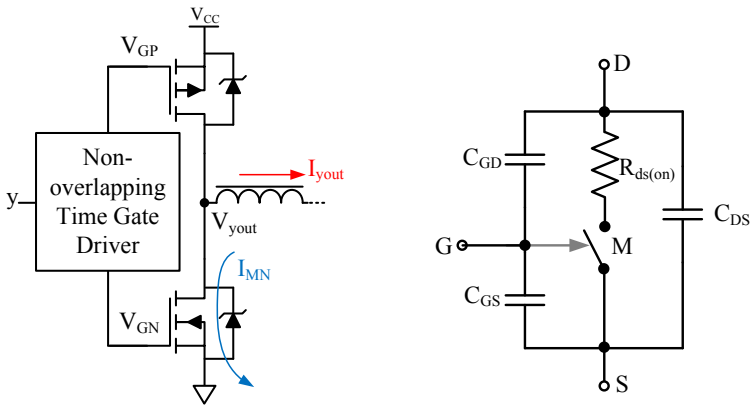
where the power dissipated by the gate drivers depends on their implementation and the

power dissipated by the EMI low-pass filter can be minimized by correctly selecting the filter's components. Although considered here, the EMI low-pass filter can be disregarded when designing power output stages in IC technology, where the EMI low-pass filter is externally added to the power output stage. This means that the key factor in order to meet the power efficiency specification is in diminishing the power losses in the power output MOSFETs.

2.3.6.1 Power Output Transistors Losses

Considering the half-bridge output stage to be analysed and the MOSFET switching model depicted in Fig. 2.27(a) and Fig. 2.27(b), respectively, theses losses can be categorized and simplified has conduction losses, switching losses and capacitive losses [vd99, SMVR11, EH94, MU07]. The back-gate recovery diode losses are neglected in this analysis.

The Fig. 2.28 shows the switching waveforms of the above half-bridge, during the output NMOS transistor turn-on and turn-off, which can be used to calculate the switching and conduction losses. This analyses can also be extrapolated for the PMOS transistor.



(a) Half-bridge ouput stage

(b) Switch model equivalent of a MOSFET transistors

Figure 2.27: Half-bridge output stage and MOSFET switch model equivalent

During the NMOS turn-on the I_{Load} current starts flowing through the NMOS transistor, creating a switching loss, which lasts t_{rise} seconds (which is a transitor's fabrication parameter). At the end of the turn-on there is a V_{DS}(on) voltage drop due to its finite R_{ds}(on), which creates a constant conduction loss during the time the transistor is turned

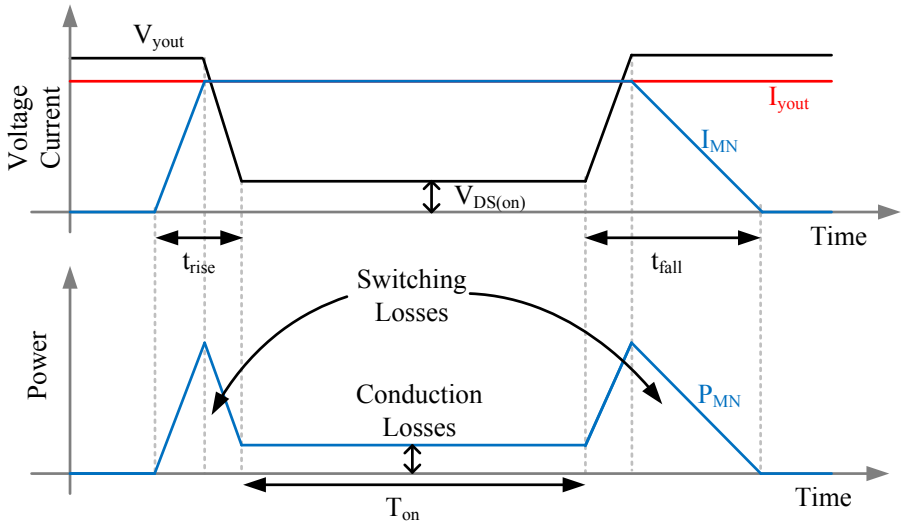


Figure 2.28: Switching waveforms of a power output NMOS transistor

on. The turn-off procedure will also dissipate a similar switching loss, but this time lasts as long as t_{fall} seconds. By this time the I_{Load} current will start flowing from the PMOS transistor which will suffer similar losses.

The conduction losses appears due to the non-zero on-resistance of the power output NMOS transistor, $R_{ds}(on)$, and the current, $I_{DS} = I_{Load}$, that flows through it. It is also dependable on the time that the transistor is turned on, and can be given as

$$P_{cond} = R_{ds}(on) \cdot I_{DS}^2 \cdot \frac{T_{on}}{T_{period}} \ (W) \tag{2.15}$$

where the T_{on}/T_{period} is the amount of time the NMOS transistor is turned one in one period.

The switching losses, which happens at the switching frequency, f_{switch}, can be written, using the triangular area during the t_{rise} and t_{fall}, in Fig. 2.28, as

$$P_{sw} = 1/2 \cdot V_{CC} \cdot I_{DS} \cdot (t_{rise} + t_{fall}) \cdot f_{switch} \ (W) \tag{2.16}$$

which means that there is a large amount of instantaneous power being dissipated during the turn-on and turn-off intervals. This result also shows that the dissipated power by the power output transistor varies linearly with the switching frequency and the switching time, defined as $t_{rise} + t_{fall}$.

Due to the internal parasitic capacitances of the MOSFET, namely C_{GS}, C_{GD} and C_{DS} (refer to Fig. 2.27(b)), there is energy stored inside the device that will latter translate into capacitive loss. This energy is dissipated in the circuit also at the rate of the switching frequency. Considering the Miller effect, the C_{GD} parasitic capacitance contributes to the total input and output capacitance with $2 \cdot C_{GD}$ [JSS07]. As it is necessary to drive the gate of the power output transistor, which has a parasitic C_{in} capacitance and is driven by its V_{GS} voltage, the capacitive losses can be written as follows

$$P_{cap} = 2 \cdot C_{in} \cdot V_{GS}^2 \cdot f_{switch} = 2 \cdot Q_g \cdot V_{GS} \cdot f_{switch} \ (W) \tag{2.17}$$

where the multiplicative factor 2 is added as it is necessary to turn on and turn off the NMOS transistor.

Given the previous equations, the power dissipated by a single power output transistor can be computed as

$$\begin{aligned} P_T = &\ P_{cond} + P_{sw} + P_{cap} = \\ = &\ f_{sw} \cdot \left(R_{ds}(on) \cdot I_{DS}^2 \cdot T_{on} + 1/2 \cdot V_{CC} \cdot I_{DS} \cdot (t_{rise} + t_{fall}) + 2 \cdot Q_g \cdot V_{GS} \right) \end{aligned} \tag{2.18}$$

2.3.7 Including the power output stage in the feedback path

Most of the major causes of distortion of the output stage, described in subsection 2.3.2, can be reduced by inserting the output stage in the feedback path.

Due to the ΔΣM architecture, it requires the feedback voltage to have the same common-mode voltage as the loop filter of the modulator. This forces the output stage to level-shift its voltage through a voltage divider, which can increase the dissipated power.

The process of including the power output stage in the feedback path is not trivial as if done poorly can lead to a huge number of mismatches and increase the distortion.

Since the 1-bit quantization scheme has a fully differential nature, the output stage can be inserted directly without the need for external circuitry in the ΔΣM.

An example using a fully differential 1^{st} order ΔΣM with a H-bridge output stage inserted in the feedback path is showed in Fig. 2.29. Nonetheless, as the power output

stage has an inevitably delay, this will create instability problems since a delay in the feedback path will decrease the phase margin of the ΔΣM.

Although the H-bridge can also work under a 1.5-bit quantization scheme, there will be an asymmetry regarding the logic level 0, as it can produce this logic level by either short-circuiting the load at V_{SS} or at V_{CC}. Even though the effect on the output is the same, the amount of feedback that is injected into the modulator is not, as this will introduce a dynamic mismatch into the system that can have unwanted effects. In order to achieve a good linearity and symmetry so as to reduce the even order harmonic distortion and noise floor, the logic level +1, 0 and -1 should all fall onto the same line, but, due to the distortion inserted by the output stage, 0^+ and 0^- are different. Fig. 2.30 shows an example for this case, where if an 1-bit quantization scheme is completely linear, as two points can always describe a line, 1.5-bit quantization scheme can not.

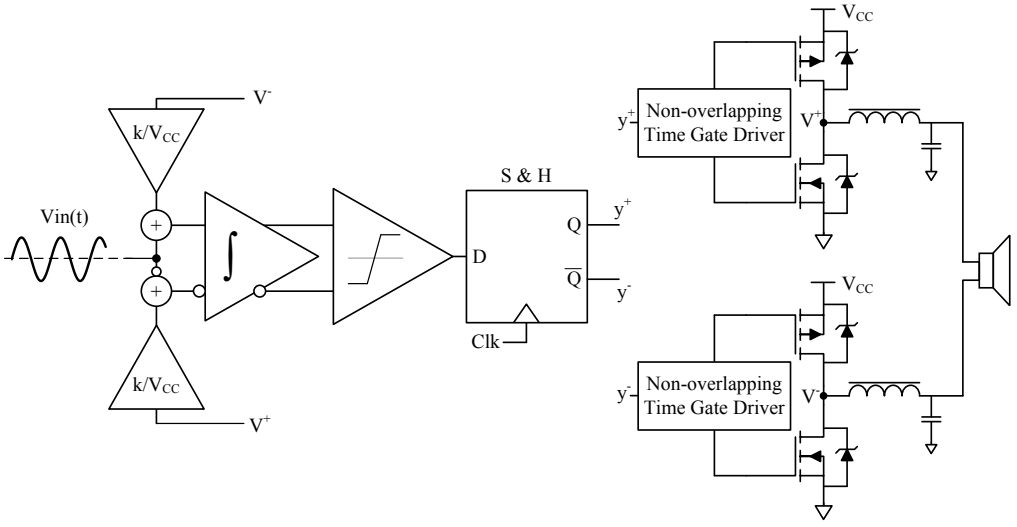
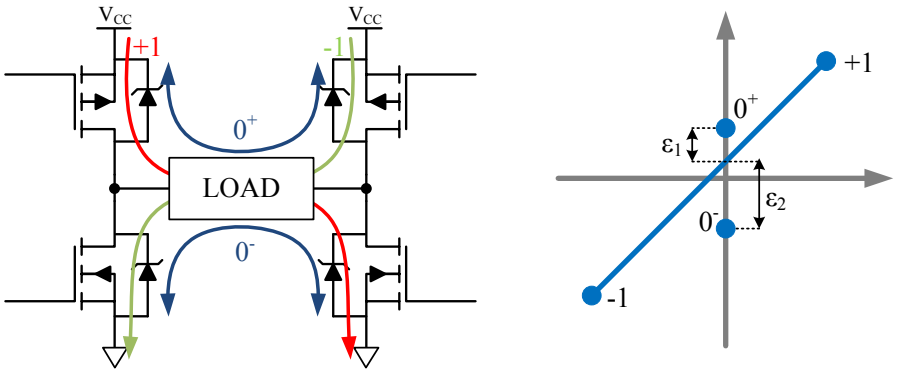


Figure 2.29: Fully differential 1^{st} order ΔΣM with a H-bridge output stage inside the feedback path using 1-bit quantization scheme



(a) 1.5-bit quantization scheme in the power output stage

(b) Non-linearity in the dynamic element mismatching

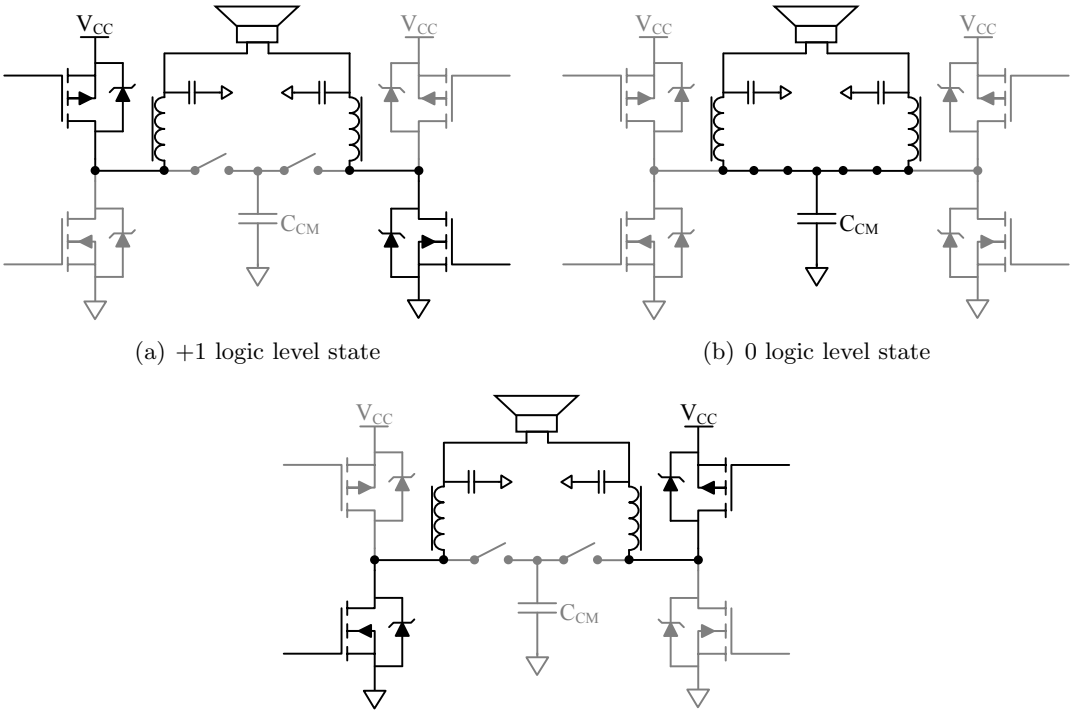
Figure 2.30: Dynamic element mismatch

In order to bypass this asymmetry, dynamic element matching can be used [Gal10]. This can be achieved by using successively 0^+ and 0^- when the output is the logic level 0, so that the average of the pulses will provide the common-mode voltage of the output stage and the error introduced by the dynamic mismatching is reduced [CTY+12]. Nonetheless, this implementation requires a low and matched dead-time and delay of both half-bridges, otherwise it will create jitter noise. The additional circuitry can be inserted in the modulator stage. Using dynamic element matching will nevertheless degrade the power efficiency as more transitions are required, forcing the system to have a switching behaviour of the 1-bit quantization scheme.

Another possibility is to use four additional switches at V_{CC} that will short-circuit the output EMI filter and the loudspeaker during the 0-state, while the output MOSFETs are all turned-off [NLJY13]. This technique, called charge sharing, require additional gate drivers to short-circuit the load, which is impractical when using high V_{CC} voltages. Fig. 2.31 shows an example of a H-bridge power output stage using this type of architecture.

2.4 Summary

The conceptual description and the most common signal modulation techniques and power output stage architectures of a Class D audio amplifier are introduced in this chapter. Concerning the signal modulation technique, the PDM presents several advantages over the



(a) +1 logic level state

(b) 0 logic level state

(c) -1 logic level state

Figure 2.31: Three-level switching H-bridge with charge sharing

PWM, mainly since it can be implemented using a $\Delta\Sigma$M, which is an architecture of choice when concerning audio ADCs. As it has an inherited feedback, the power output stage can be inserted in this feedback path and have its distortion corrected by the modulator. The quantization scheme, which can be 1-bit or 1.5-bit, is also addressed.

The power output stage topologies are introduced and the major causes of distortion are presented, such as dead-time, power supply and reverse recovery distortion. The theoretical output EMI low-pass filter and a theoretical analysis of the power output transistor losses, which come mainly from the switching, are described.

A subsection describing how to include the power output stage in the feedback path is also addressed, due to the feedback mismatch when the 1.5-bit quantization scheme is used. Dynamic element matching and charge sharing are presented in order to bypass this mismatch.

Chapter 3

Output Stage Design

3.1 Introduction

The starting point when designing a Class D audio amplifier is to establish the output stage topology and the modulation technique. As the work objective is to design a simple, discrete, and yet power efficient output stage, several design options are explored prior to define the audio performance goals.

This chapter describes the proposed power output stage.

Modulation technique and system architecture

In order to achieve the best overall performance, a H-bridge output stage topology, which its advantages are described in subsection 2.3.1, is adopted. By inserting the output stage in the feedback path most of the distortion caused by the output stage will be corrected.

The PDM is implemented using an optimized CT fully-differential $\Delta\Sigma$M for Class D audio amplifiers which can use either 1-bit or 1.5-bit quantization scheme and has distributed and local resonator feedback [dMP10a]. The ability to optimize the $\Delta\Sigma$M with the output stage in the feedback loop, allows the system to converge even with severe time constrains in the output stage [dMNPG12]. Fig. 3.1 shows an illustrative example of the SNDR versus the sampling frequency for an optimized CT $\Delta\Sigma$M, concerning 1-bit and 1.5-bit quantization schemes.

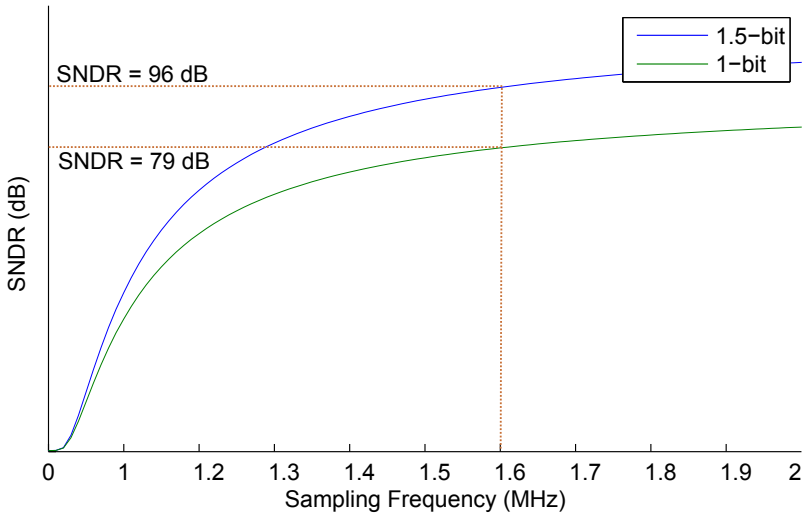


Figure 3.1: Illustrative example of the SNDR vs sampling frequency for an optimized CT ΔΣM with 0 dBV input signal concerning 1-bit and 1.5-bit quantization schemes

It is possible to see that using the same sampling frequency it is possible to achieve a better SNDR using 1.5-bit quantization scheme rather than 1-bit. This is due to the fact that the use of 1.5-bit improves the linearity of the feedback which results in a more stable loop, increasing the stopband ripple in the modulator and therefore improving the maximum achievable SNDR [dMP10b].

Both quantizations schemes will be used in order to study the output stage performance.

Output stage topology

The ΔΣM and the dead-time generator circuitry generates two TTL digital control signals, y^+ and y^-, which are amplified by the non-overlapping time gate driver and the output power MOSFETs. The use of a PMOS-NMOS totem-pole arrangement also simplifies the high side gate driver design without compromising the power efficiency. Fig. 3.2 shows the chosen architecture for the output stage.

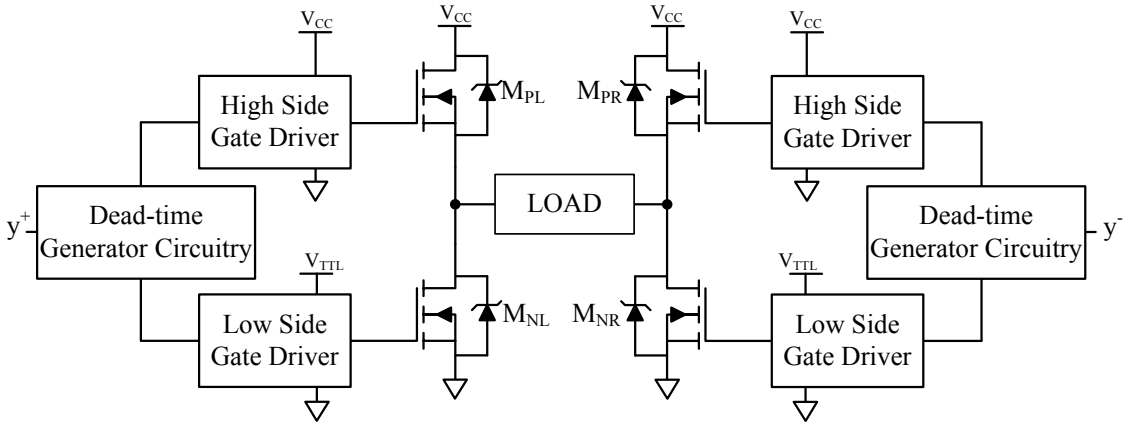


Figure 3.2: Class D audio amplifier output stage in H-bridge configuration

3.2 Non-overlapping Time Gate Driver

3.2.1 Low Side Gate Driver

Since the source of the power output NMOS transistor is connected to ground, the low side gate driver can be simply implemented as a PMOS-NMOS inverter with a TTL power supply. Controlling the inverter switching with timed pulses, just like the dead-time procedure, can significantly decrease the power consumption of the low side gate driver by preventing shoot-through current in the gate driver. This can be implemented using a non-overlapping time circuit. The Fig. 3.3 shows the low side gate driver with the non-overlapping time circuit and the Fig. 3.4 depicts the switching currents and voltages in the gate driver, where the drain current of M_P (I_P) and M_N (I_N) only flows through the gate of M_{NL} (I_G).

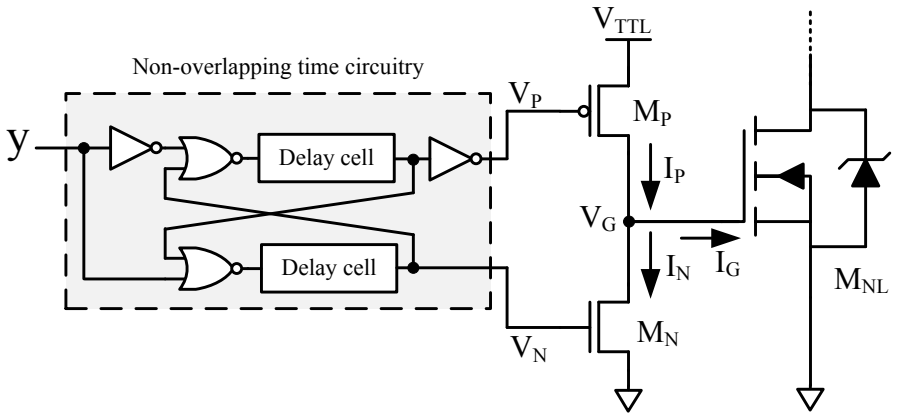


Figure 3.3: Low side gate driver and power NMOS transistor

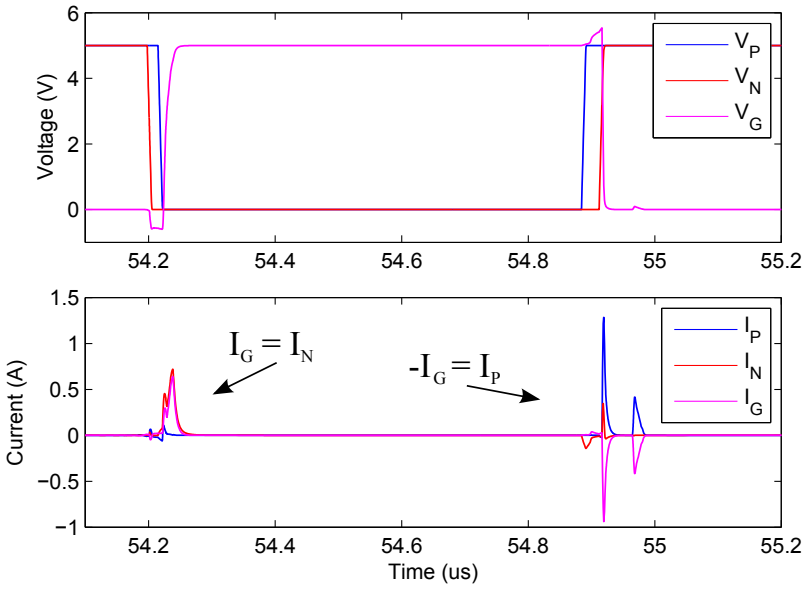


Figure 3.4: Example with simulated voltage levels and current flow in the low side gate driver during the M_{NL} switching

3.2.2 High Side Gate Driver

As the logic circuitry generates a TTL digital signal that will drive the high side gate driver, the gate driver needs to level shift this signal to V_{CC} with enough power efficiency and speed so that it doesn't compromise the output stage performance.

3.2.2.1 Starting Point

The starting point for the high side gate driver design is the PMOS gate driver described in [YH08] and depicted in the box of Fig. 3.5.

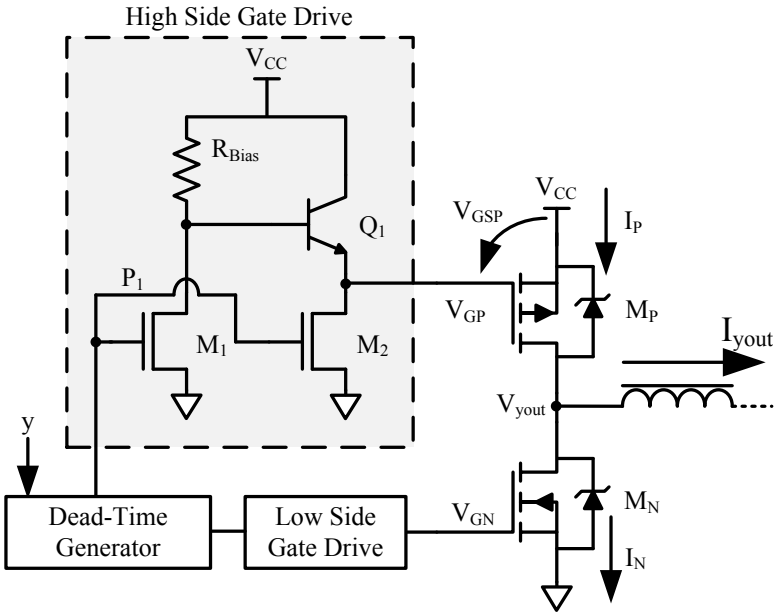


Figure 3.5: Output stage with the PMOS gate driver (in box [YH08])

Circuit Operation

The circuit operation is as follows: when P_1 is high the transistors M_1 and M_2 are on, forcing the base-to-emitter voltage drop of transistor Q_1 to be zero, turning it off. M_2 will also push-down the gate voltage of transistor M_P to zero, turning it on. When P_1 is low, the transistor Q_1 will turn on due to the current defined by the resistor R_{Bias}, which will pull-up the gate voltage of M_P.

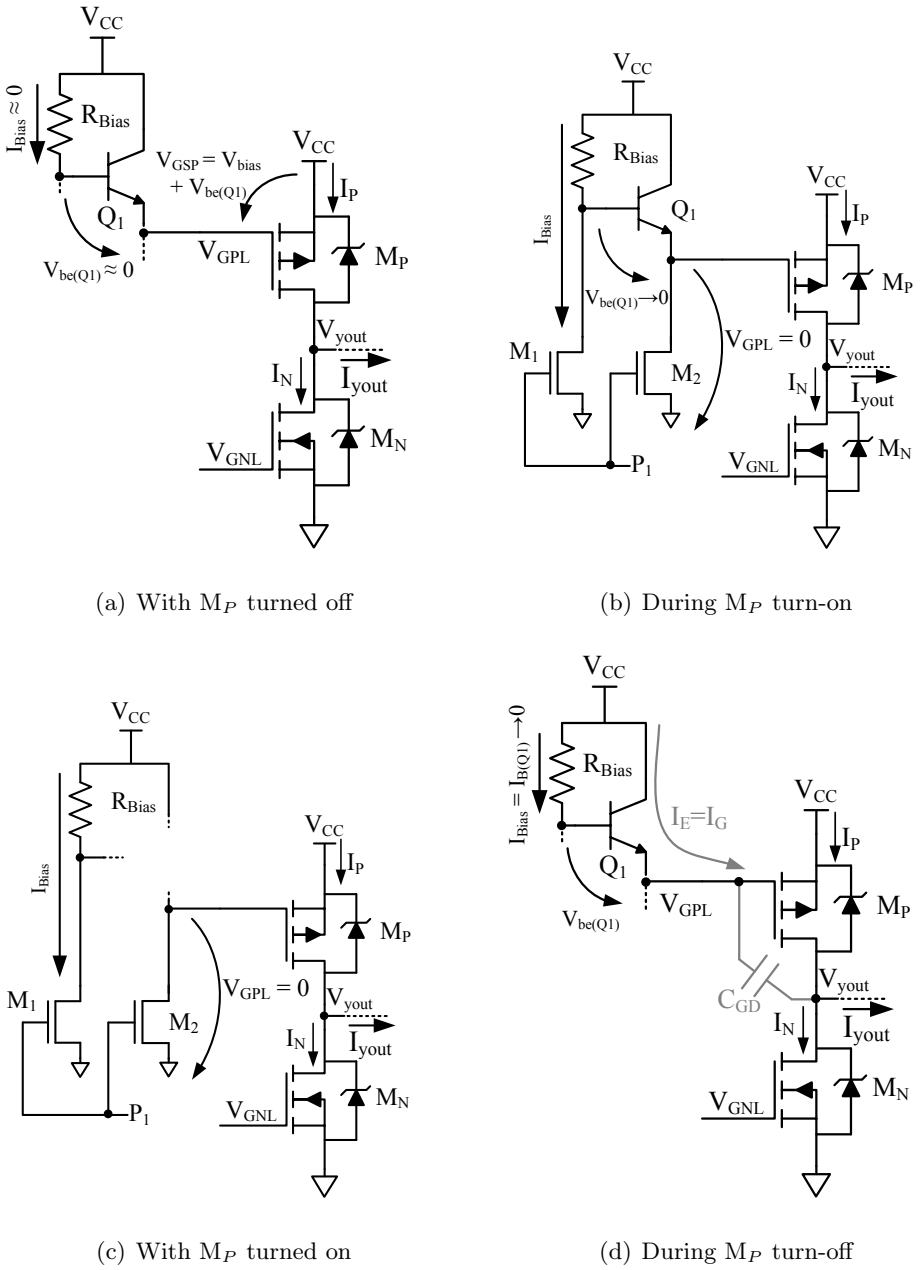
This means that the M_P turn-off speed is dependent on R_{Bias} which imposes a severe trade-off: when M_P is on, a DC current $V_{CC}/(R_{Bias} + R_{DS}(M_1))$ will flow through R_{Bias}

and M_1, creating an undesired power dissipation. Increasing R_{Bias} in order to reduce this current will slow down the M_P turn-off speed as this resistor bias Q_1. This classifies the gate drive as Class A when the M_P is on, as it is necessary to have a constant DC current. By inspecting the high side gate driver it is also possible to see that the M_P gate-to-source voltage, V_{GSP}, is equal to $V_{RBias} + V_{BE}(Q_1)$. This will eventually cause shoot-through current, as M_P can not be fully turned off due to the fact that V_{GSP} is not exactly zero. Nonetheless, as the solely responsible for the M_P turn-on is M_2, the turn-on speed is rather fast due to its low R_{ds}(on) value.

The Fig. 3.6 shows the starting point high side gate driver circuit during the M_P turn on and turn off states. The Fig. 3.7(a) and Fig. 3.7(b) also shows the transitory waveforms of the gate driver, with $I_{yout} > 0$ and $I_{yout} < 0$, respectively.

When the output current is positive and M_N is conducting (refer to Fig. 3.6(a)), the output stage behaves normally until M_N turns off due to the dead-time. M_N's backgate diode gets positively forwarded and conducts the I_{yout} current until the end of the dead-time, forcing the V_{yout} node to have $-V_{BackGateDiode}$ voltage level. As M_P turns on, at the end of the dead-time, reverse recovery occurs due to the stored charge in the M_N's backgate diode and a small shoot through current occurs. The PMOS transistor is turned-on by short-circuiting the V_{be} voltage drop of Q_1 and forcing the V_{GPL} voltage to be zero. At this time the high side gate driver will consume the I_{Bias} current (Fig. 3.6(b) and Fig. 3.6(c)).

During the V_{yout} transition from high to low, the R_{Bias} resistor will bias Q_1 in order to pull up the V_{GPL} voltage, and the output stage enters in dead-time. Nonetheless, the I_{Bias} resistor will tend to zero as the V_{GPL} tends to V_{CC} (refer to Fig. 3.6(d)) and this current will stop being consumed as the M_P is turned off. The V_{yout} node gets the $-V_{BackGateDiode}$ voltage level again as the I_{yout} current flows through M_N's backgate diode. Even though there is a huge parasitic capacitance C_{GDP} in the power output PMOS transistor, which will pull down the M_P gate voltage during the transition from high to low, Q_1 is capable to keep up by supplying the required current. This can be also seen due to the fact that the V_{GP} voltage halts during the V_{yout} from high to low transition. The transition waveforms for this case are depicted in Fig. 3.7(a).



(a) With M_P turned off

(b) During M_P turn-on

(c) With M_P turned on

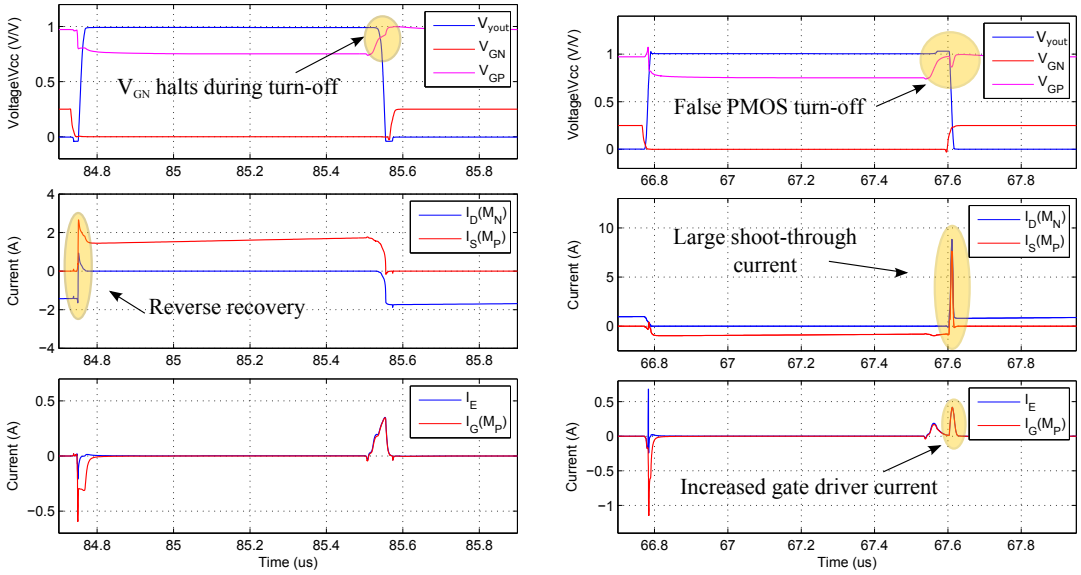
(d) During M_P turn-off

Figure 3.6: Starting point high side gate driver during M_P turn on and turn off

When $I_{yout} < 0$, in Fig. 3.7(b), the dead-time distortion occurs due to the M_P back-gate diode. When M_N turns off in order to shift the V_{yout} node from low to high, the M_P back-gate diode gets positively biased and starts conducting, forcing the V_{yout} node to V_{CC} plus $V_{BackGateDiode}$. Due to the C_{GDP} capacitance the V_{GPL} node also gets pulled beyond V_{CC} during dead-time, which is then pushed down by M_2, turning M_P on. When the gate driver wants to turns off M_P, Q_1 starts conducting and pulling up the V_{GPL} node

to $V_{RBias}+V_{BE}(Q_1)$, which is near the V_{th} voltage of the output PMOS. As M_N turns on, it will start pushing down the V_{yout} node with an increased slope, which will activate the PMOS due to the C_{GDP} capacitance, as the V_{GPL} voltage is close to V_{th} (which means that it is falsely turned-off). The reverse recovery also occurs, which will increase even more the shoot through current. This will force Q_1 to keep up with the V_{GPL} decrease by supplying an undesired current at a rate of $C_{GDP} \cdot \frac{d(V_{GP}-V_{yout})}{dt}$, which he may be unable to deliver.

This phenomenon will compromise the high side gate driver performance and power efficiency.



(a) $I_{yout} > 0$ (b) $I_{yout} < 0$

Figure 3.7: Transitory waves during the dead-time distortion with negative and positive I_{yout} current

3.2.2.2 Proposed Gate Driver

The proposed gate driver is depicted in the box of Fig. 3.8. By increasing its complexity it is possible to bypass the problems encountered in the starting point gate driver.

Circuit Operation

In order to achieve lower power dissipation one zener diode was inserted in each branch of the circuit. The zener voltage of these diodes should be V_{CC} - 5 V so that the V_{GS} voltage

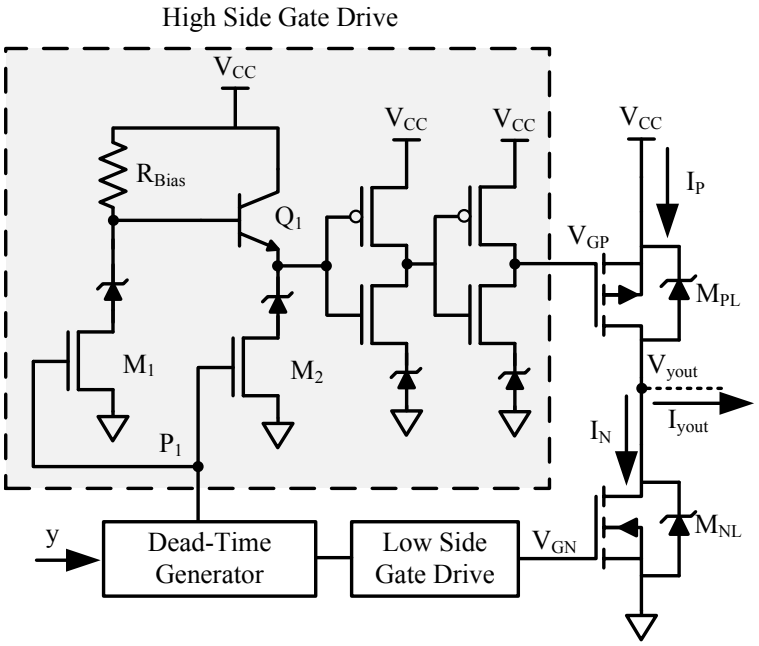


Figure 3.8: Proposed high side gate driver (in box)

drop of the output PMOS transistor, the R_{Bias} voltage drop and the CMOS inverters only swings 5 V from V_{CC}. Two CMOS inverters were also placed at the gate of the power output PMOS for two main reasons: to force the V_{GP} voltage to be exactly V_{CC} when the M_P is off and to have a fast PMOS turn on and a slow PMOS turn off.

As the output stage delivers power to the load only when the high side power MOSFET is on, this will extend the positive pulse, thus optimizing the power efficiency. Since the output stage is inserted inside the feedback path of the modulator, the excessive power delivered to the load is being continuously corrected. This design will also simplify the power supply scaling, as only the zener diode needs to be scaled for the gate driver to work the same way, since the current that bias Q_1 is constant (providing that the same V_{Rbias} voltage drop is applied).

Nonetheless, the same DC current as in the starting point gate driver appears during the PMOS turn on state. This means that a careful analysis on how the R_{Bias} branch influences the power efficiency of the high side gate driver can be done, which differs with the used quantization scheme and if the dynamic element matching technique is applied. Assuming an 1-bit quantization scheme, each half-bridge will consume this DC current at a time, as they have complementary signals. By using an 1.5-bit quantization scheme

the high side gate driver power consumption can be lowered, as in order to perform the 0-state both the PMOS transistors can be turned off (0^- state). Despite all, this approach will perform poorly when dynamic element matching is used, as it will have the same performance as if an 1-bit quantization scheme was used. This is due the fact that when the output stage is performing the 0-state, it can either have both PMOS turned off or both PMOS turned on, which is the same as having one PMOS turned on and one turned off for the same time period, just like in an 1-bit quantization scheme.

Considering 1.5-bit quantization scheme and just one half-bridge in a periodic sinusoidal input, the theoretical DC power dissipation in this branch depends on how much time the PMOS transistor of that half-bridge is turned on, and can be written as:

$$P_{branch} = PMOS_{on} \cdot (P_{Rbias} + P_{Zener} + P_{M1}) \; [W] \tag{3.1}$$

where the $PMOS_{on}$ constant represents the amount of time that the PMOS of that half-bridge is turned on in one sinusoidal period.

Assuming a low M_1's R_{ds}(on), the equation can be simplified to

$$P_{branch} \approx PMOS_{on} \cdot \left(\frac{5^2}{R_{Bias}} + \frac{V_{CC} - 5}{R_{Bias}} \right) \; [W] \tag{3.2}$$

Fig. 3.9 (top) shows the plot of Eq. 3.2 for different loudspeakers impedances and R_{Bias} values. Fig. 3.9 (bottom) also shows the PMOS turn-on and PMOS turn-off delay with different R_{Bias} values. It is possible to see that the turn-off delay is constant with R_{Bias} as it only depends on M_2 transistor while the turn-on delay is proportional to R_{Bias} increase.

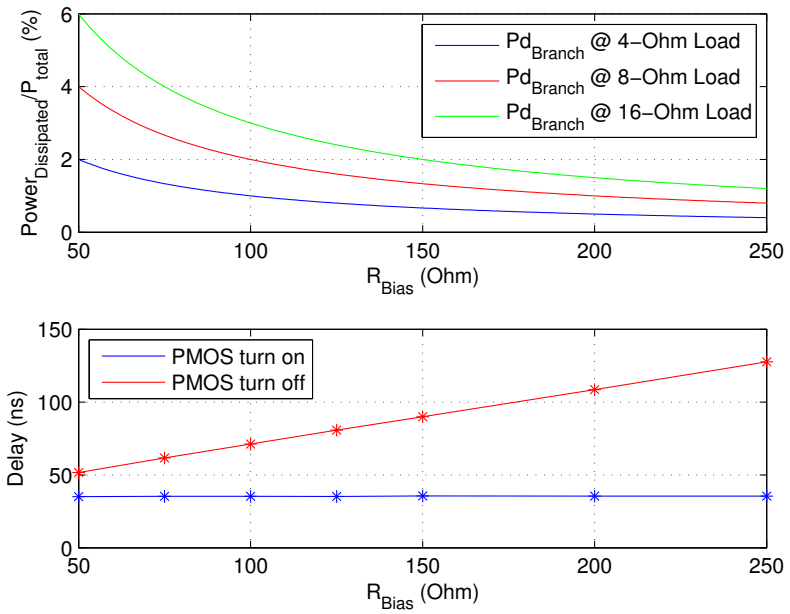
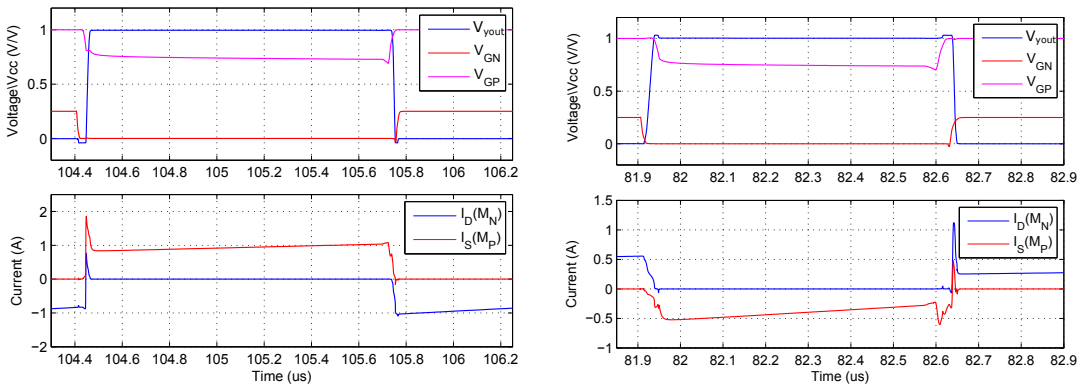


Figure 3.9: Relative power dissipated by the R_{Bias} branch with different loudspeakers impedances and the average delay for different R_{Bias} values (simulated results from schematic presented in chapter 5.1 while using 1.5-bit quantization scheme without dynamic element matching)

Fig. 3.10(a) and Fig. 3.10(b) shows the transitory waves. In comparison with the starting point it is possible to see that the V_{GP} is well-defined by the CMOS inverters at the gate of M_P and that there is only a small shoot-though current when the reverse recovery occurs, which is an expected phenomenon.



(a) $I_{yout} > 0$ (b) $I_{yout} < 0$

Figure 3.10: Transitory waves during the dead-time distortion with negative and positive I_{yout} current

3.2.3 Dead-Time Generator

The dead-time generator allows the synchronization of the high side and low side MOSFETs switching in order to prevent shoot-through current.

The Fig. 3.11 shows the fixed dead-time generator circuitry which is implemented using a non-overlapping time circuit where the delay cells are implemented using a passive resistor-capacitor (RC) low-pass filter [LLC08]. Although due to its fixed delay characteristic the dead-time circuit is very dependable on process and temperature variations, which can create an increased dead-time or even an unexpected shoot-through current, it can be fine-tuned by using a trimmer taking into consideration the high and low gate driver delay.

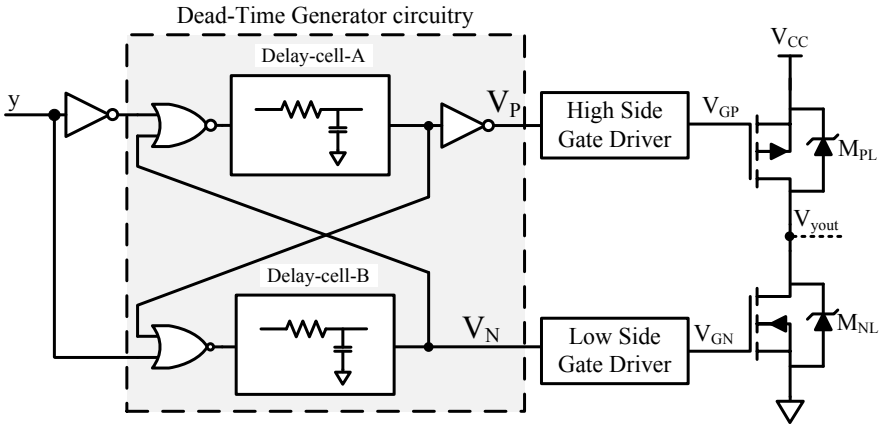


Figure 3.11: Fixed Dead-time generator circuity

The delay-cells will define the amount of delay between the V_P and V_H transitions. Fig. 3.12 shows the transitory waves with equal delay cells (top) and with delay-cell-A 100x the delay-cell-B (bottom). The region where they have opposite signs (e.g. V_N is low and V_H is high) will create the desired dead-time.

This approach can lead to close to zero dead-time distortion, but it is dependable on the high side and low side gate driver speed. Since, for instance, R_{Bias} resistor is responsible for the PMOS turn off speed, every time the R_{Bias} changes a delay cell reconfiguration in order to create the necessary dead-time is required.

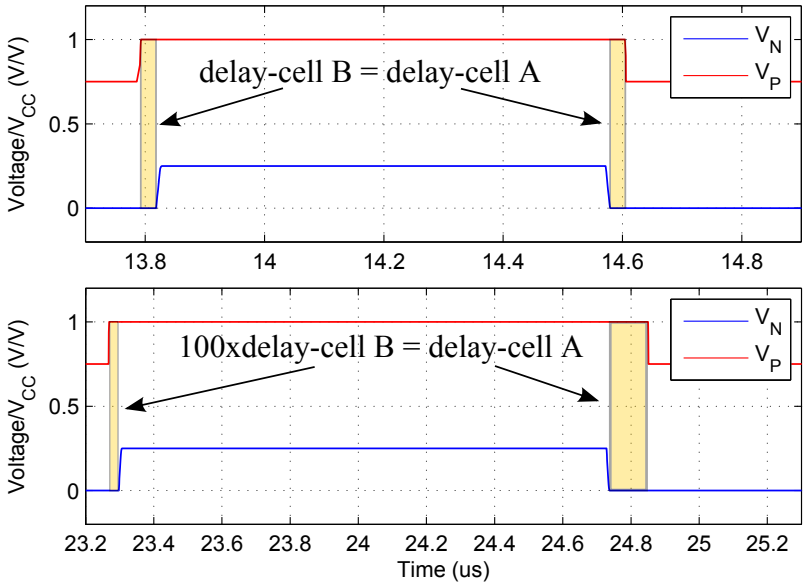


Figure 3.12: Transitory waves for the dead-time generator circuit with equal delay cells (top) and with delay-cell-A 100x the delay-cell-B (bottom).

3.3 Output EMI low-pass filter

In order to reduce the EMI and preserve the signal in the audio band frequency, a passive LC low-pass filter, introduced in Chapter 2.3.5, can be applied. The H-bridge topology requires a fully differential filter, which can be implemented using two variants: with or without an external capacitor in parallel with the loudspeaker. By introducing this external capacitor the remaining high frequency energy is forced to circle inside the LC low-pass filter rather than dissipating on the loudspeaker. The values summary for the two different implementations are presented at the end of this section.

3.3.1 Theoretical transfer function

By using a cutoff frequency of 24 kHz and a critically damped response ($Q = 1/\sqrt{2}$) a distortion free response inside the audio band can be achieved. The filter's transfer function presented in Eq. 2.2 with the previous constrains applied can be written as:

$$H(s) = \frac{(2\pi \cdot 24 \times 10^3)^2}{s^2 + \frac{2\pi \cdot 24 \times 10^3}{1/\sqrt{(2)}} s + (2\pi \cdot 24 \times 10^3)^2} = \frac{2.274 \times 10^{10}}{s^2 + 2.133 \times 10^5 \cdot s + 2.274 \times 10^{10}} \quad (3.3)$$

Fig. 3.13 shows the frequency response of the theoretical filter where it is possible to see that it has a -3 dB attenuation at the cutoff frequency and a critically damped response.

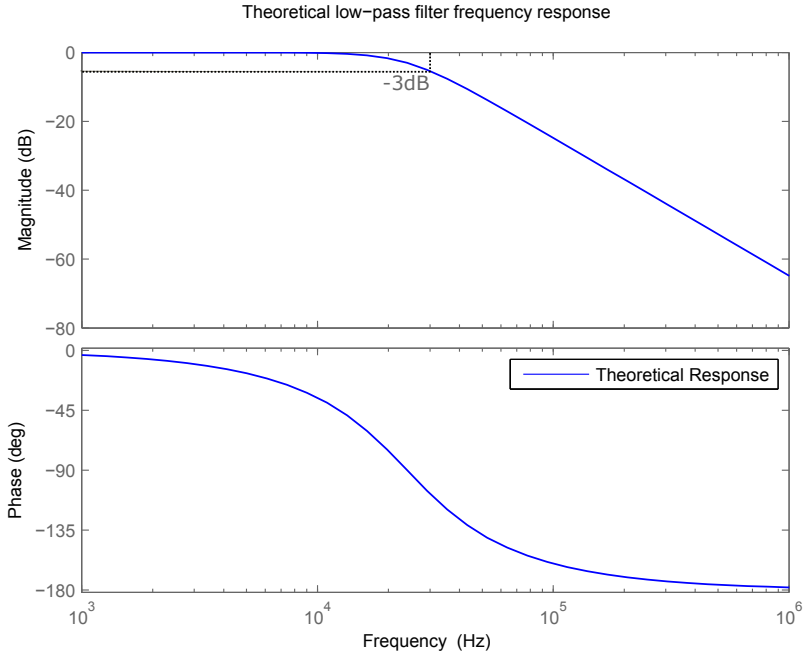


Figure 3.13: Theoretical low-pass filter frequency response with 24 kHz cutoff frequency and critically damped response

3.3.2 Components value determination

3.3.2.1 Traditional fully differential LC low-pass filter design

From Eq. 2.11 it is possible to write the equation that determines the filters inductor and capacitor value in function of the loudspeaker impedance, which is presented in Eq. 3.4.

$$\begin{cases} C = 2\frac{Q}{R_L\omega_n} \\ L = \frac{1}{2}\frac{R_L}{Q\omega_n} \end{cases} = \begin{cases} C = \frac{9.3783}{R_L}\ (nF) \\ L = R_L \cdot 4.6891\ (nH) \end{cases} \tag{3.4}$$

Using this type of filter doesn't allow any degree of freedom.

3.3.2.2 Fully differential LC low-pass filter design with additional C_E capacitor

By adding a capacitor in parallel with the loudspeaker its frequency response will alter, decreasing the loudspeaker impedance ($Z_L = C_E//R_{Load}$) with the frequency increase.

Assuming the relationship between the parallel and the grounded capacitor described in Eq. 2.13, the Fig. 3.14 shows the frequency response of Z_L impedance with different loudspeaker impedances. It is possible to see that Z_L impedance only starts to decay after the 20 kHz bandwidth. Eq. 3.5 presents the filter components values in function of the loudspeaker impedance.

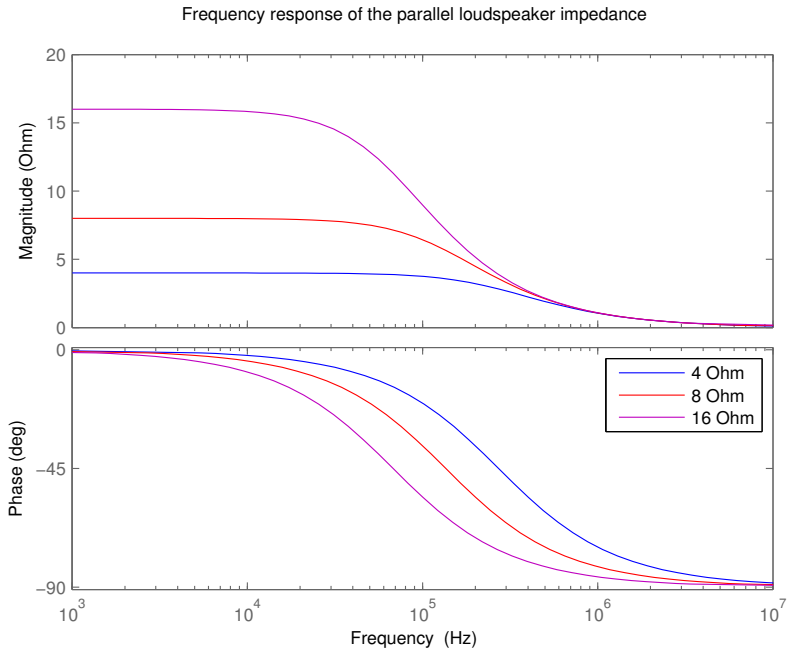


Figure 3.14: Frequency response of the parallel loudspeaker impedance with different loudspeaker impedances

$$\begin{cases} C = \frac{Q}{R_L \omega_n} \\ C_E = \frac{1}{2} \cdot \frac{Q}{R_L \omega_n} \\ L = \frac{1}{2} \frac{R_L}{Q \omega_n} \end{cases} = \begin{cases} C = \frac{4.6891}{R_L} \ (nF) \\ C_E = \frac{2.3446}{R_L} \ (nF) \\ L = R_L \cdot 4.6891 \ (nH) \end{cases} \tag{3.5}$$

3.3.3 Filter components values summary

The Table 3.1 presents the inductor and capacitors values for the low-pass filter.

	Loudspeaker (Ω)	L (μH)	C (μF)	C_E (μF)
Traditional	4	18.757	2.340	-
	8	37.513	1.172	-
	16	75.026	0.5861	-
With external C_E	4	18.757	1.172	0.5861
	8	37.513	0.5861	0.2931
	16	75.026	0.2930	0.1465

Table 3.1: LC low-pass filter values with different loudspeaker impedances

3.4 Summary

This chapter presents the proposed output stage design for the Class D audio power amplifier. The use of a H-bridge power output stage topology allows the system to reduce the offset, even order harmonics and to use 1.5-bit quantization scheme, which will decrease the number of transitions, thus optimizing the power efficiency. Nonetheless, the power output stage is not restricted to the 1.5-bit quantization scheme, but the use of the 1-bit quantization scheme will decrease the power efficiency.

The proposed H-bridge is based on a PMOS-NMOS totem pole which will simplify the design of the high side gate driver. The use of a non-overlapping time in the low side gate driver will lower its dissipated power and the problems of the high side gate driver starting point are bypassed by the proposed high side gate driver. A theoretical analysis of how the power consumption of the high side gate driver affects the power efficiency is also presented.

The introduced dead-time generator allows to set a fix dead-time which can be easily modified by changing the resistor value of the RC low-pass filter of the delay cell.

The components values for the output EMI low-pass filter are also determined, assuming the typical loudspeaker impedances of 4, 8 and 16-Ohm.

Chapter 4

Class D Audio Amplifier Electrical Simulations

Keeping in mind that the maximum output power of a Class D audio amplifier is directly proportional to the power supply voltage level and the loudspeaker impedance, by designing the system to have 20 V power supply and an 8-Ohm load, it can theoretically deliver up to 50 W to the load. This can define the first constrain of the power output stage, which is the loudspeaker impedance and ratings, the power supply voltage level and the maximum drained current. The use of a 20 V power supply and an 8-Ohm load sets the maximum constant drained current from the power supply, assuming ideal transistors, to be 2.5 A. By using a 4-Ohm load instead, the system would be able to deliver twice the power but will also drain twice the current from the power supply, requiring components with higher absolute maximum rating values, thus increasing the project costs.

Regardless of the power supply voltage level, the energy delivered to the load also depends on the modulator. By using an optimized fully-differential CT $\Delta\Sigma$M with the output stage in the feedback path, the system can achieve high SNDR and low THD, but, in order to do this, the optimization results in a maximum output voltage level, at full power, around 70% of the power supply voltage level [dMNPG12]. This means that assuming a 20 V power supply and an 8-Ohm load, the maximum peak-to-peak voltage would be

$$V_{pp} = 2 \cdot 20 \cdot 0.7 = 28V \tag{4.1}$$

with a RMS voltage given by

$$V_{RMS} = \frac{V_{pp}}{2\sqrt{2}} \approx 9.9V \tag{4.2}$$

and a maximum power delivered to the load of approximately

$$P_{Load} = \frac{V_{RMS}^2}{R_{Load}} = 12.25W \tag{4.3}$$

The proposed Class D audio amplifier will be simulated using two fully-differentials CT 5^{th} order $\Delta\Sigma$M with 1.60 MHz switching frequency and 20 kHz bandwidth (BW) (which gives an Oversampling Ration (OSR) of 40), one using 1.5-bit quantization scheme with and without dynamic element matching and another with 1-bit quantization scheme, all of them with the proposed output stage inside the feedback path. The architectures for the various $\Delta\Sigma$Ms are presented in Fig. 4.1. All $\Delta\Sigma$Ms were optimized [dMNPG12] taking into account an average 100-ns power output stage delay.

The first part of this chapter will discuss how to determine the Class D $\Delta\Sigma$M and the power output stage electrical components. The second part will define the base FFT of the Class D audio amplifier, by simulating just the $\Delta\Sigma$M with an ideal 100-ns delay power output stage. By introducing the real power output stage inside the feedback loop it will be possible to study the distortion inserted by it and its performance.

All simulations were performed using an high performance SPICE simulator[1].

4.1 Electrical Components Selection

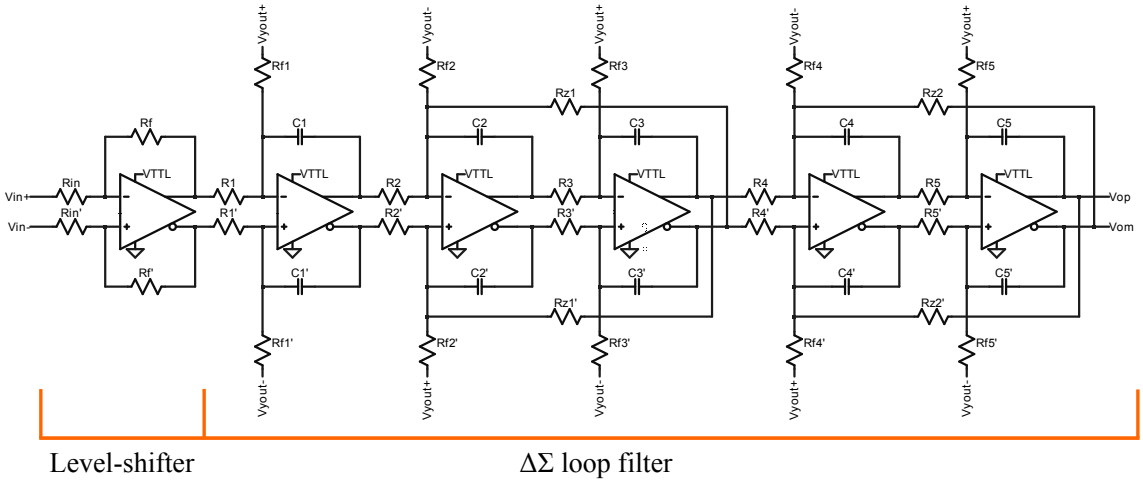
By using surface-mount-technology (SMD) components it is possible to simplify the layout design of the PCB, the soldering process, to reduce board area and the component costs. This will also allow to decrease most of the parasitics in the board due to the reduction of the lengths of the paths in the PCB. The $\Delta\Sigma$Ms were optimized considering a 2 % tolerance for the resistors, so 1 % tolerance resistors, which falls inside the safe-guard

[1]LTspice from Linear Technologies; all non-included models were inserted using SPICE3 models

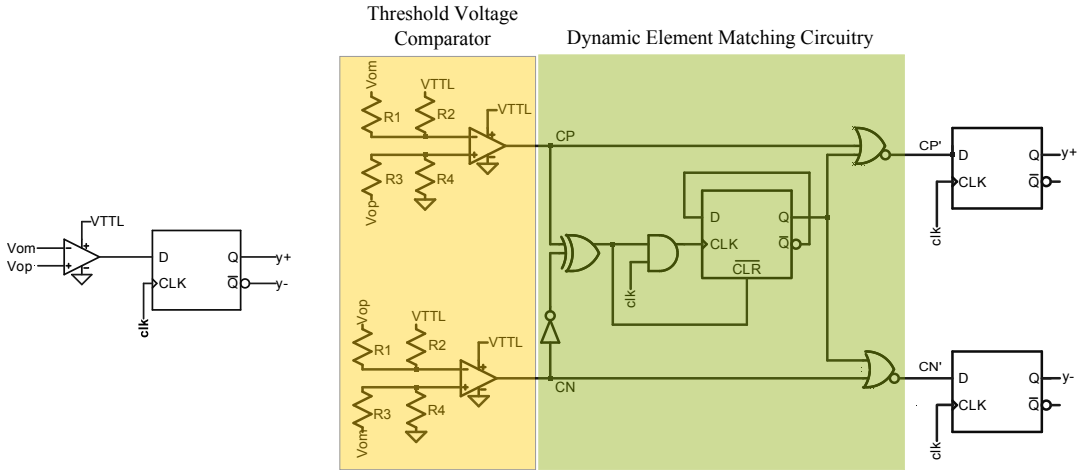
band, are used.

4.1.1 ΔΣ Modulators

The fully-differential CT 5^{th} order ΔΣM architecture for the Class D audio amplifier is depicted in Fig. 4.1 and is an extended and mirrored version of the single-ended 3^{rd} order ΔΣM optimized for Class D audio amplifiers presented in [dMP10b].



(a) Selected CT 5^{th} order ΔΣM architecture for Class D audio amplifiers



(b) 1-bit quantization

(c) 1.5-bit quantization with dynamic element matching

Figure 4.1: Selected ΔΣMs architectures for the Class D audio amplifier with 1-bit and 1.5-bit quantization schemes with dynamic element matching

The first stage of the modulator consists in a level-shifter that can be easily converted into a single-ended-to-differential conversion circuit, just by short-circuiting one of the Operational Amplifiers (opamps) inputs to ground. This will allow to level shift the

ground referenced input signal to the circuit's common-mode voltage, so that the $\Delta\Sigma$M loop filter circuit works properly. This poses no problem due to the high common-mode-rejection-ratio (CMRR) of the selected opamps. The loop filter stage, implemented using fully differential opamps, uses local and distributed feedback. Depending on the desired quantization scheme, additional circuitry may be required.

For an 1-bit quantization scheme the fully-differential signal from the integration stage, V_{op} minus V_{om}, is compared with zero and the resulting digital output is directly held by the FF-D.

Regarding the 1.5-bit quantization scheme, additional circuitry is required to correctly perform the quantization. A threshold comparator is used to compare the V_{op} minus V_{om} signal with a threshold value. If dynamic element matching is desired, this additional circuitry can be inserted before the FF-D.

The signal held by the FF-D is then amplified by the output stage.

4.1.1.1 Threshold voltage comparator

To achieve 1.5-bit quantization scheme, a threshold voltage comparator is required. This can be done by using a voltage divider between the V_{op} minus V_{om} voltage and the power supply voltage; this circuit is presented in Fig. 4.2.

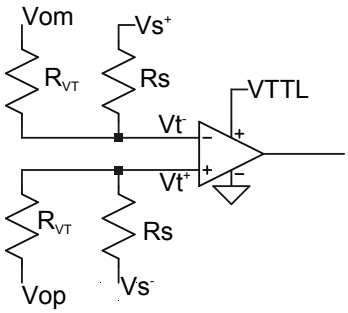


Figure 4.2: Threshold voltage comparator

The equations that describes the comparator behaviour can be written as

$$\begin{aligned} V_T^+ &= \frac{R_S}{R_{VT}+R_S} \cdot (V_{op} - V_S^-) - V_S^- \\ V_T^- &= \frac{R_S}{R_{VT}+R_S} \cdot (V_{om} - V_S^+) - V_S^+ \end{aligned} \tag{4.4}$$

where assuming $\Delta V_T = V_T^+ - V_T^-$ comes that

$$\begin{aligned} \Delta V_T = & \frac{R_S}{R_{VT}+R_S} \cdot (V_{op} - V_{om}) + \left(\frac{R_S}{R_{VT}+R_S} - 1\right) \cdot (V_S^+ - V_S^-) \\ \Delta V_T = & \frac{R_S}{R_{VT}+R_S} \cdot \Delta V_o - \frac{R_{VT}}{R_{VT}+R_S} \cdot \Delta V_S \\ \Delta V_T = & \frac{R_S}{R_{VT}+R_S} \cdot \left(\Delta V_o - \frac{R_{VT}}{R_S}\Delta V_S\right) \end{aligned} \tag{4.5}$$

As the goal comparison equation is $\Delta V_o - \Delta V_{TH} > 0$, then the previous equation can be rewritten, considering $\Delta V_S = V_{TTL} - 0\ V = 5\ V$ and a scale factor, as

$$\begin{aligned} \Delta V_o - \Delta V_{TH} = & \frac{R_S}{R_{VT}+R_S} \cdot \left(\Delta V_o - \frac{R_{VT}}{R_S}\Delta V_S\right) \\ \Delta V_{TH} = & \frac{R_{VT}}{R_S} \cdot 5\ V \\ \Delta V_{TH} = & \frac{R_{VT}}{5\ k\Omega} \cdot 5\ V \\ \Delta V_{TH} = & R_{VT}\ (mV) \end{aligned} \tag{4.6}$$

which means that there is a direct conversion between the ΔV_T voltage threshold and the R_{VT} resistor.

4.1.1.2 Dynamic Element Matching Logic

If the dynamic element matching logic was placed after the FF-D it could produce nanosecond spikes due to the fact that both inputs of the last two NOR logic gates don't share the same delay. This problem is bypassed by placing the dynamic element matching logic before the FF-D, as represented in Fig. 4.3.

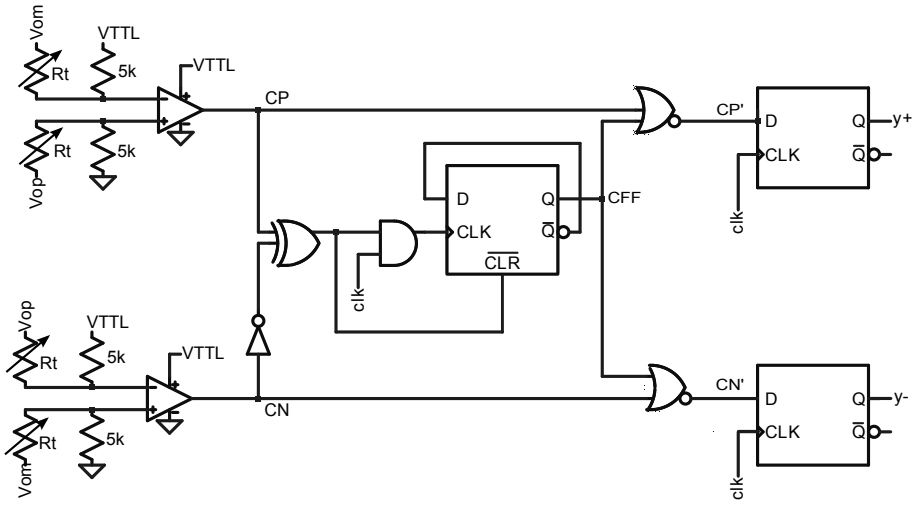


Figure 4.3: Dynamic element matching logic

The dynamic element matching can be described with the following simplified diagram presented in Fig. 4.4.

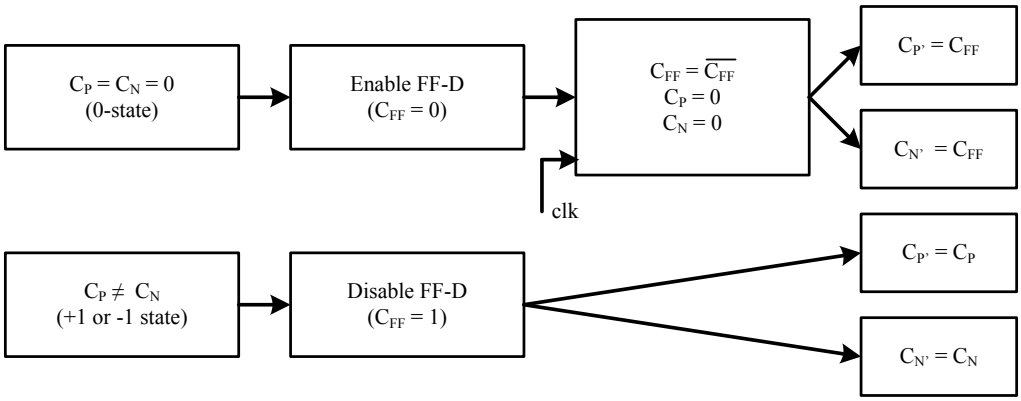


Figure 4.4: Simplified dynamic element matching diagram

Fig. 4.5 shows an example of the dynamic element matching logic output waveforms, where there is a train of 0-states.

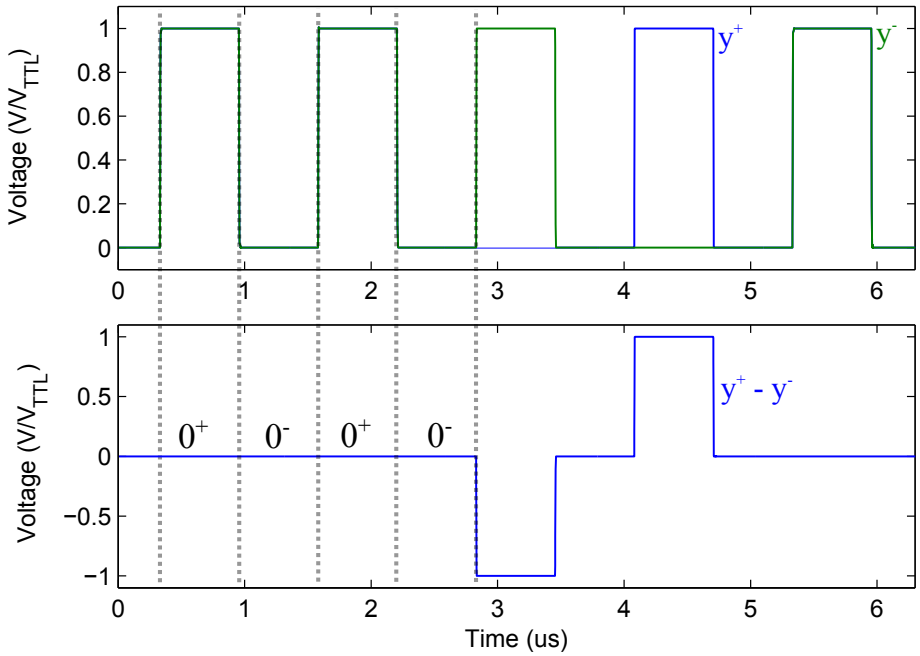


Figure 4.5: Dynamic element matching logic example waveforms

4.1.1.3 Fully-differential opamps

In order for the ΔΣM, depicted in Fig. 4.1, to operate correctly, the fully-differential opamps that are part of the loop filter stage must at least verify the constrains presented in Table 4.1 [dMP10b], so that they don't affect the performance of the modulator signif-

icantly.

Parameter	Value
Positive Power supply (V)	5
Negative Power supply (V)	0
$V_{common-mode}$ (V)	2.5
Slew-rate (V/μs)	10
Open-loop gain (dB)	72
Bandwidth (MHz)	50

Table 4.1: Required fully-differential opamp characteristics

The $\Delta\Sigma$Ms are initially simulated using ideal fully-differential opamps implemented using voltage-dependent-voltage-sources (VDVS), which are depicted in Fig. 4.6 [Bak11]. Assuming high open-loop gain and infinite BW it is possible to define the maximum performance that the system is capable of achieving, allowing to determine the distortion inserted by the selected fully-differential opamp.

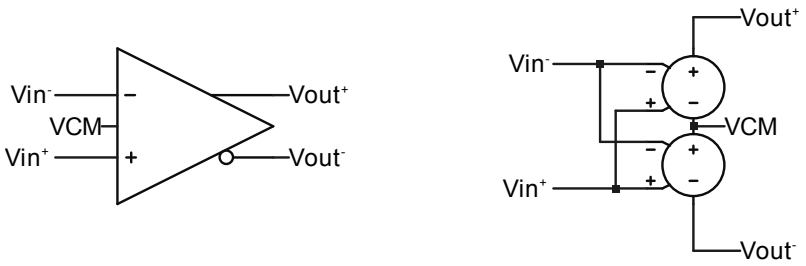


Figure 4.6: Ideal fully-differential opamp using VDVS

The comparator does not have any special requirements, other than having a response time lower than 10ns; nonetheless, a dual-comparator package is preferred due to layout simplicity. The FF-D and the dynamic element matching logic are also only required to be have a fast response time and to be TTL compatible, which means that any of the most common IC logic families will work.

Table 4.2[2] summarizes some commonly found parts that can be used.

[2]Slew-rate (SR), open-loop gain (A_{VOL}).

Part	Manufactor part	Manufactor	SR (V/μs)	A_{VOL} (dB)	BW (MHz)	Response time (ns)	Package	Price (1k) (€)
Fully-diff. opamp	LTC6362	Linear Technology	45	95	34	-	MSO-8	1.870
	THS4531	Texas Instruments	200	115	36	-	MSO-8	1.450
	LT1994	Linear Technology	65	95	70	-	MSO-8	2.050
Comparator	LT1720	Linear Technology	-	-	-	4.5	SO-8	3.210
	MAX962ESA+.	Maxim Integ. Prod.	-	-	-	4.5	SO-8	5.740
FF-D	CD74AC175M	Texas Instruments	-	-	-	7.0	SO-16	0.500
NOR	74HC02D	NXP	-	-	-	7.0	SO-14	0.104
NOT	74HC04D	NXP	-	-	-	6.0	SO-14	0.123
XOR	74AHC1G86W5-7	Diodes Inc.	-	-	-	4.9	SOT-25	0.071
AND	74AHC1G08W5-7	Diodes Inc.	-	-	-	4.6	SOT-25	0.088

Table 4.2: Various commonly-found parts for the $\Delta\Sigma$M

Although the LTC6362 presents a lower BW than the one specified in the table 4.1, it has a lower price and power dissipation than the LT1994, which fulfils every requirement. Both opamps are from the Linear Technologies which can ship a limited number of samples with no cost for prototyping purposes. The THS4531 does not offer a SPICE model compatible with the SPICE simulator and thus is only presented as an alternative.

4.1.2 Power Output Stage

Due to the fact that the power output MOSFETs are in a PMOS-NMOS totem-pole arrangement, the high side and low side power transistors should have fairly equal characteristics. This means that they both should be capable of handling the absolute maximum ratings of the system, have low R_{ds}(on) and a low gate capacitance, in order to require a small heatsink and to be easily driven.

Correctly choosing the output stage electrical components is a key component regarding a good power efficiency.

4.1.2.1 Power Output MOSFETs

Assuming a maximum continuous drain current of 2.5 A from a 20 V power supply voltage, there is a wide range of options in the market for complementary power output MOSFETs. However, the components should at least be able to sustain twice the system ratings, due to inevitable switching voltages overshoots. In order to simplify the PCB layout, a dual N-Channel and P-Channel MOSFET transistor in a single package is preferred.

The peak voltage is also one of the main constrains when choosing the transistors. From equation 4.1 it is possible to see that since the output stage is in H-bridge configuration each power output transistor should be able to handle the V_{pp} voltage. Based on this, the power output transistors should be able to handle at least a V_{DS} voltage of 30 V. Ensuring that the output transistors also have a typical threshold voltage V_{th} lower than 2 V will ensure a safe turn on from the gate drivers.

The Table 4.3 shows some commonly-found power output transistors that meet the requirements. They all have the same SO-8 package type and pinout.

Component	Manufactor	Channel	Cont. I_{DS} (A)	V_{DS} breakdown (V)	Cont. I_{SM} (body-diode) (A)	typ. V_{th} (V)	R_{DS}(on) @ 4.5-V V_{GS} (mΩ)	Q_G (nC)	t_{rise} (ns)	t_{fall} (ns)	Max. $P_{Dissipation}$ (W)	Price (1k) (€)
IRF7309	Inter.	N	4.0	30	1.8	1.0	80.0	25.0	21.0	7.7	1.4	0.311
	Rect.	P	-3.5	-30	-1.8	-1.0	160.0	25.0	17.0	18.0		
IRF7389	Inter.	N	7.3	30	2.5	1.0	32.0	22.0	8.9	17.0	2.5	0.303
	Rect.	P	-5.3	-30	-2.5	-1.0	76.0	23.0	13.0	32.0		
IRF7319	Inter.	N	6.5	30	2.5	1.0	32.0	22.0	8.9	17.0	2.0	0.311
	Rect.	P	-4.9	-30	-2.5	-1.0	76.0	23.0	13.0	32.0		
IRF9389	Inter.	N	6.8	30	2.0	1.8	33.0	6.8	4.8	3.9	2.0	0.093
	Rect.	P	-4.6	-30	-2.0	-1.8	82.0	8.1	14.0	15.0		

Table 4.3: Various commonly-found dual N and P channel MOSFETs

The Fig. 4.7 shows a power dissipation comparison between the previously presented power MOSFETs, assuming the power dissipation equations described in chapter 2.3.6.

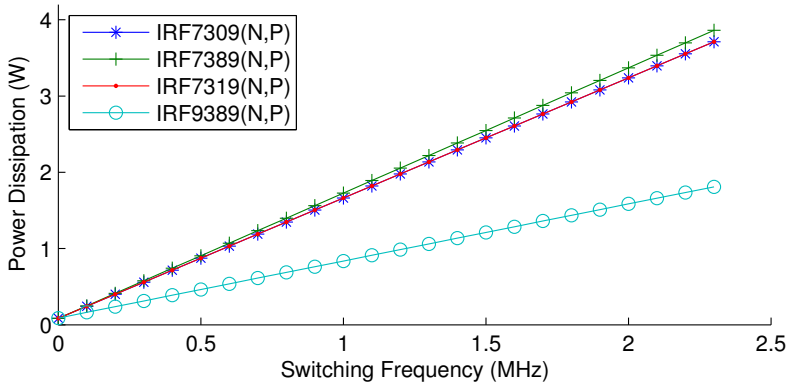


Figure 4.7: Power output MOSFET transistor comparison chart

Even though the IRF9389 MOSFET clearly stands out, no electrical model was found. As only the IRF7309 MOSFET had a SPICE3 model available it ended up being he one chosen to simulate the full system.

4.1.2.2 Low Side Gate Driver

The low side gate driver uses a simple dead-time circuit and a PMOS-NMOS inverter in order to drive the power output NMOS MOSFET. Several inverters in parallel are placed at the gate of the PMOS-NMOS inverter in order to sink and source enough current to successfully drive their gate. The same is used for the delay-cell, which is implemented using a passive RC low-pass filter.

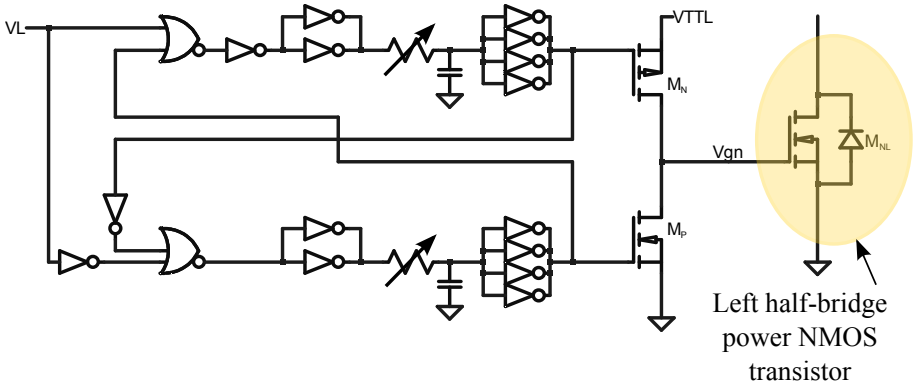


Figure 4.8: Low side gate driver schematic

Any logic transistor can be used in order to implement the PMOS-NMOS inverter, as long as they have low on-resistance and provide fast switching. As a safe-guard measure, their maximum V_{DS} voltage should be at least three times the V_{TLL} voltage and have a minimum of 0.5 A I_{DS} current.

4.1.2.3 High Side Gate Driver

In order to implement the high side gate driver it is necessary to take some constrains into consideration. The R_{Bias} resistor and the zener diode should be able to sustain their dissipated power, which is set by the I_{Bias} current. In order to reduce costs the same transistors type used in the low side gate driver can be used for the two CMOS inverters connected to the gate of the power PMOS MOSFET. Nonetheless, the NPN transistor that pulls-up the gate of the first inverter should be able to drain enough current to drive the inverters gate and be able to provide fast switching rates.

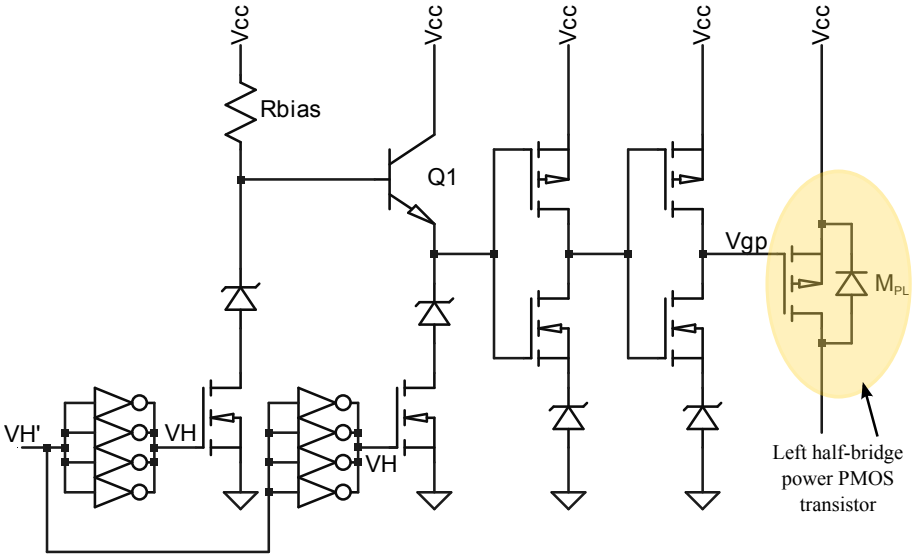


Figure 4.9: High side gate driver schematic

The selected value for the R_{Bias} resistor is 125 Ω, which, from the Fig. 3.9, present a good compromise between the dissipated power in this branch and the PMOS turn-on speed. The theoretical current that flows from this resistor is 40 mA which, if a static current would be applied, would dissipate 200 mW in the resistor and 600 mW in the zener diode.

As a design option, two 500 mW rated zener diodes in parallel were used, and the R_{Bias} resistor was implemented using one 1/2 W 100 Ω resistor in series with an 100 Ω 1/4 W trimmer, thus also allowing some adjusting capabilities to the circuit.

4.1.2.4 Dead-Time Generator Circuit

The dead-time generator circuit, depicted in Fig. 4.10, uses a predefined dead-time which can be set by a trimmer in the low-pass RC filter. A set of inverters are placed before the RC low-pass filter in order to correctly drive the filter. The same is done to drive the two NMOS transistors of the high side gate driver.

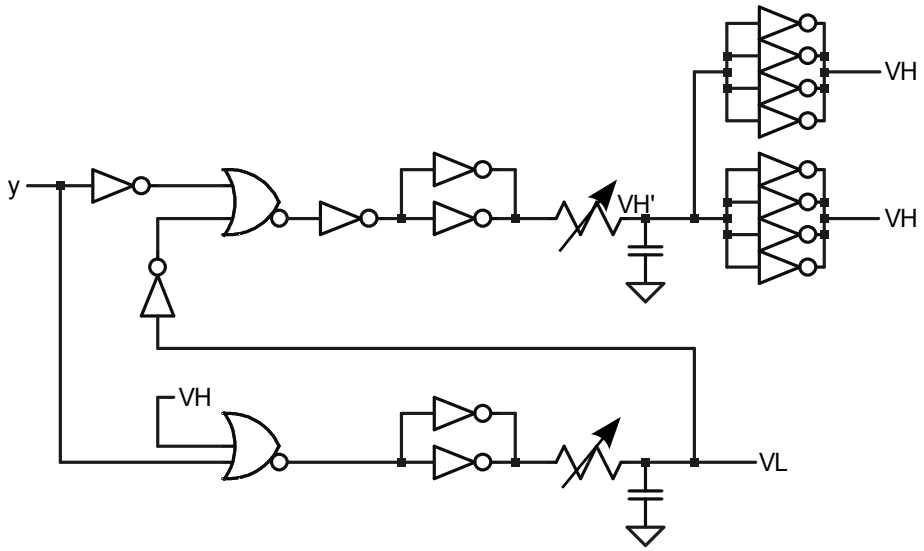


Figure 4.10: Dead-time generator circuitry

The time constant for the RC low-pass filter is defined by τ = RC, where, using a fixed capacitor value of 100 pF, the time constant can be computed as

$$\begin{aligned} \tau &= RC \\ \tau &= R\ (\Omega) \cdot 100p\ (F) \\ \tau &= R\ \cdot 0.1\ (ns) \end{aligned} \tag{4.7}$$

which means that, e.g., using R = 100 Ω will create a 10.0 ns dead-time.

4.1.2.5 EMI Output Low-pass Filter

The Table 3.1 introduced in chapter 3.3 presents the theoretical filter's values summary. As there are only standardized values in the market, some mismatches can occur. The inductor should have a low Equivalent Series Resistance (ESR) in order to have a near-zero power dissipation and to be able to sustain the maximum continuous current. The capacitor is only required to be able to sustain at least twice the maximum peak voltage.

The used values for the traditional filter and the filter with the external capacitor using an 8-Ohm load are presented in Table 4.4 and Table 4.5, respectively. The selected inductor's ESR is 50 mΩ and is capable of sustaining an maximum of 3 A of DC current.

Component	Manufactor part	Manufactor	Theo. Value	Part Value	E_R (%)	Price (1k) (€)
Inductor (μH)	PE-54040NL	Pulse	37.513	38	1.29	1.100
Capacitor (μF)	ECQ-E1125JF	Panasonic	1.172	1.2	2.39	0.329
Cutoff Freq. (kHz)	-	-	24.00	23.57	1.79	-
Quality Factor	-	-	$\sqrt{2}/2$	0.7108	0.52	-

Table 4.4: Traditional filter selected components

Component	Manufactor part	Manufactor	Theo. Value	Part Value	E_R (%)	Price (1k) (€)
Inductor (μH)	PE-54040NL	Pulse	37.513	38	1.29	1.100
Capacitor (μF)	DME1P56K-F	Cornell Dubilier	0.5861	0.56	4.45	0.332
Capacitor C_E (μF)	BFC247936304	Vishay	0.2931	0.3	2.35	0.581
Cutoff Freq. (kHz)	-	-	24	23.97	0.12	-
Quality Factor	-	-	$\sqrt{2}/2$	0.687	2.83	-

Table 4.5: With external C_E capacitor filter's selected components

4.2 Electrical Simulations

This section discusses the electrical simulation results of the Class D audio power amplifier, using either 1-bit or 1.5-bit quantization scheme with and without dynamic element matching.

The Fig. 4.11 exemplifies the electrical simulation workflow, where the goal is to step-by-step introduce non-linearities into the system and analyse their effect. This is done for both quantization schemes.

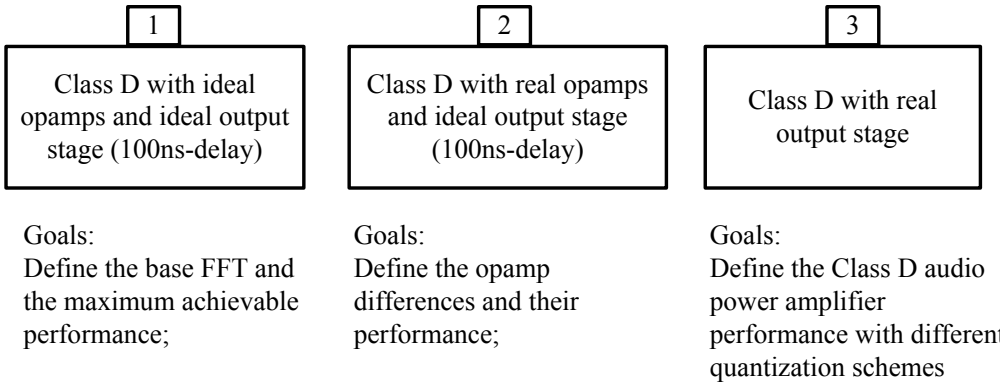


Figure 4.11: Electrical simulations workflow

The electrical simulation definitions are as follows:

- The ideal opamps were implemented using VDVS blocks, depicted in Fig. 4.6, with an open-loop gain of 180 dB and infinite BW; two real differential opamps are tested as integrators, LT6362 and LT1994, where the first one has a lower BW than the latter but presents a lower price and power dissipation.

- The ideal output stage is implemented as a VDVS block with a static 100-ns propagation delay;

- Every Fast-Fourier-Transform (FFT) is computed using a Blackman-Harris window with 2^{24} points and the $V_{out} = V^{+}_{out}$ - V^{+}_{out} output wave. The simulation length is 80 ms using an 1 Vrms differential sinusoidal input at 2 kHz frequency which provides 160 periods;

- The power output stage performance is analysed using an average of 15 periods with an 1 Vrms differential sinusoidal input at 2 kHz frequency.

The $\Delta\Sigma$M coefficients for both quantization schemes are presented in Table 4.6 and the Fig. 4.12 depicts the used Class D $\Delta\Sigma$M with a generic quantization scheme and ideal output stage. The chosen electrical component and the complete schematic are presented in subsection 5.1.

Coefficient	1-bit ΔΣM-5 @ 1.60 MHz	1.5-bit ΔΣM-5 @ 1.60 MHz
R_1 (kΩ)	51.67	13.86
R_2 (kΩ)	3.46	3.79
R_3 (kΩ)	6.21	4.22
R_4 (kΩ)	1.76	1.43
R_5 (kΩ)	1.36	1.70
Rf_1 (kΩ)	110.92	34.22
Rf_2 (kΩ)	110.92	18.82
Rf_3 (kΩ)	51.43	16.51
Rf_4 (kΩ)	18.25	6.99
Rf_5 (kΩ)	8.790	6.27
Rz_1 (kΩ)	11.30	17.91
Rz_2 (kΩ)	175.70	122.38
R_T (Ω)	-	263.30
C_I (nF)	1.00	1.00

Table 4.6: ΔΣM coefficients

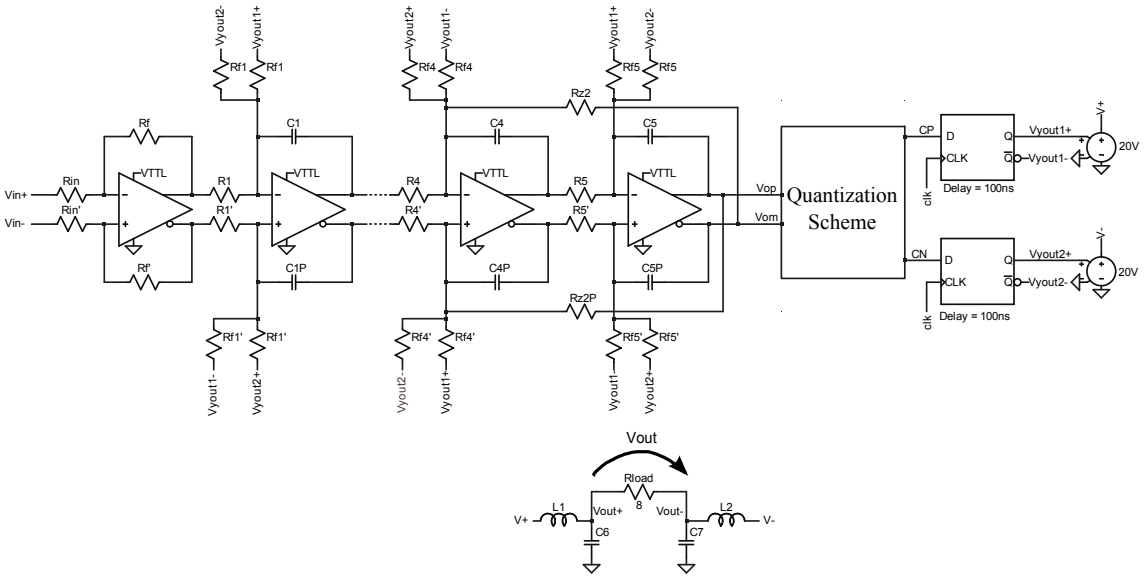


Figure 4.12: Class D ΔΣM with ideal output schematic

4.2.1 1.5-bit 5^{th} Order $\Delta\Sigma$ Modulator @ 1.60 MHz

The 1.5-bit 5^{th} order $\Delta\Sigma$M will be simulated using an ideal 100-ns delay power output stage and the proposed output stage. For the latter, the system will also be simulated with and without dynamic element matching in order to attempt the correction of the feedback mismatch presented in chapter 2.3.7. Two different opamps will also be simulated with the real output stage.

4.2.1.1 Ideal 100-ns delay power output stage

The output waveforms of the simulated $\Delta\Sigma$M with the ideal power output stage inside the feedback loop are depicted in Fig. 4.13.

It is possible to see, from the output waveform, that only one half-bridge is switching at each half sinusoidal period, which will lower the number of transitions and optimize the power efficiency. The Fig. 4.14 shows the FFT of the output wave $V_{out} = V^{+}_{out}$ - V^{-}_{out} using the ideal, LTC6362 and LT1994 opamps.

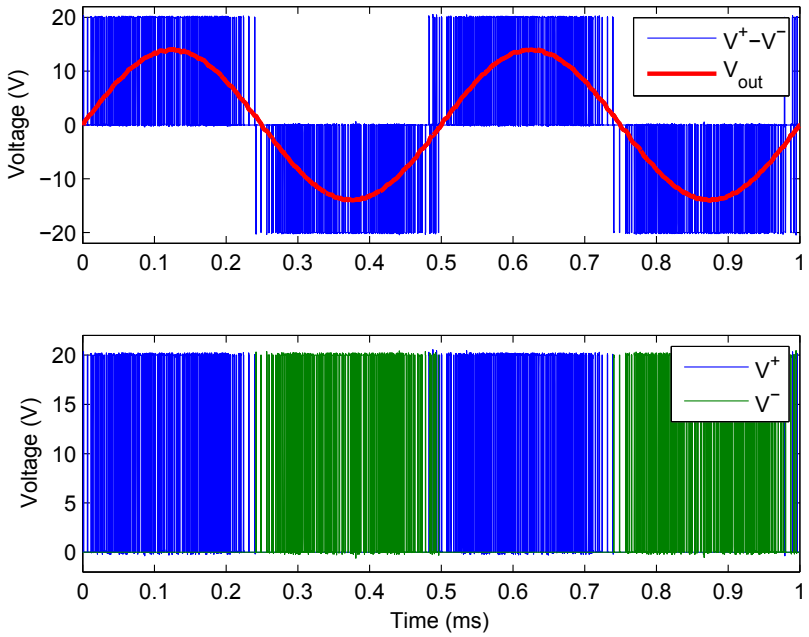


Figure 4.13: Output waveforms of the Class D audio power amplifier with an ideal 1.5-bit $\Delta\Sigma$M; top: bitstream (V^{+} - V^{-}) and V_{out}; bottom: V^{+} and V^{-}

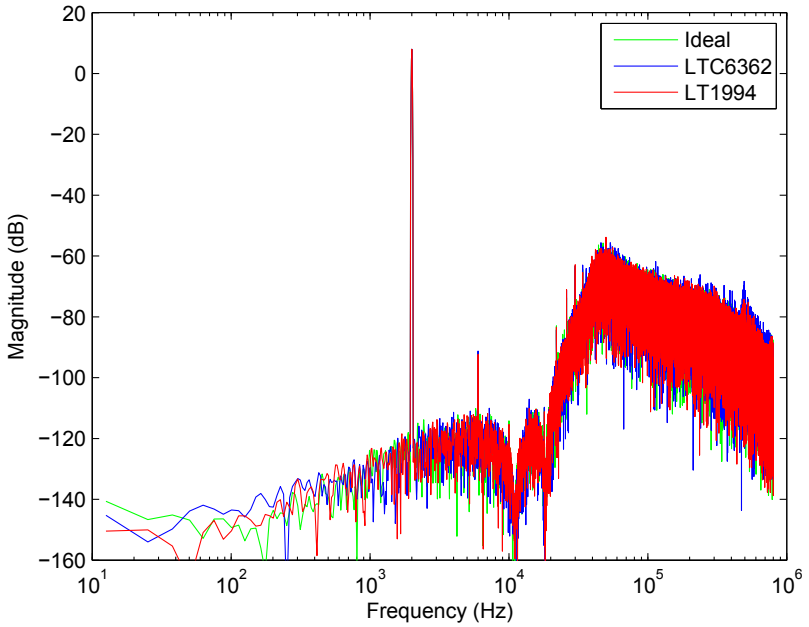


Figure 4.14: FFT of the Class D audio amplifier with ideal (blue), LTC6362 (red) and LT1994 (green) as differential opamps, using 1.5-bit quantization scheme and ideal output stage

Simulations show that the ΔΣM with ideal opamps is capable of achieving a SNDR of 96.23 dB with a THD of -98.87 dB. By using real opamps the SNDR and the THD remains virtually the same, as the LTC6362 decreases the SNDR by 0.29% and the LT1994 increases by 0.49%. These differences can be from the numerical approximations in the simulation process.

It is possible to conclude that the performance of the ΔΣM is not affected by the selected opamps when an ideal 100-ns power output is considered.

OpAmp	SNDR (dB)	THD (dB)	F_0 (dB)	HD_2 (dB)	HD_3 (dB)	HD_4 (dB)	HD_5 (dB)	V_{pp} (V)
Ideal	96.23	-98.88	7.968	-121.94	-99.22	-119.97	-121.72	27.88
LTC6362	95.95	-98.62	7.975	-119.35	-99.11	-118.95	-125.36	27.94
LT1994	96.73	-99.99	7.975	-120.03	-100.35	-124.37	-122.98	27.94

Table 4.7: AC performance summary of the 1.5-bit Class D audio power amplifier with 100-ns delay with ideal output stage

4.2.1.2 Real power output stage without dynamic element matching

When the real power output stage is included in the feedback path, a feedback mismatch occurs, as described in subsection 2.3.7. This will cause distortion in the Class D amplifier as the common mode rejection of the opamps is finite. But, as it is a fully-differential architecture, the modulator will correct most of the mismatch. The Fig. 4.15 depicts the loop filter of the ΔΣM, where the virtual ground points of the opamps are highlighted as V_{ICM}^{X}. By monitoring these points in the circuit it is possible to see if the opamps and the feedback are working correctly. The Fig. 4.16 shows the output waveforms of the power output stage, where it is possible to observe the power output stage distortion in the form of dead-time and power supply distortion.

The 0-state is performed with the 0^{-}-state of the power output stage, as described in chapter 2.3.7. This is done in order to optimize the power efficiency, as both PMOS power output transistors are turned-off during this state (refer to chapter 3.2.2.2). By monitoring the virtual grounds of the loop filter, which are depicted in Fig. 4.17, it is possible to see that their DC voltage is lower than the V_{CM} of the circuit, which is 2.5 V for a 5 V power supply. This is due to the 0^{-}-state of the power output stage that is being fed back, which pushes-down the DC integration point. This will create a feedback mismatch, as the 0-state that is being fed back is not correct, since during this state the power output stage is not delivering power to the load but is pushing down the DC virtual ground of modulator, where it should remain the same (no energy delivered to the load should mean no current being fed back). This increases the system's noise floor and total harmonic distortion, which can be seen by the FFT presented in Fig. 4.18. Due to the fact that the V_{ICM}^{X} nodes when the LT1994 is used float around the same value, harmonic distortion is minimized. This can be seen in the Table 4.8, which presents the performance summary of the Class D audio power amplifier, where the even harmonic distortion is smaller when the LT1994 is used.

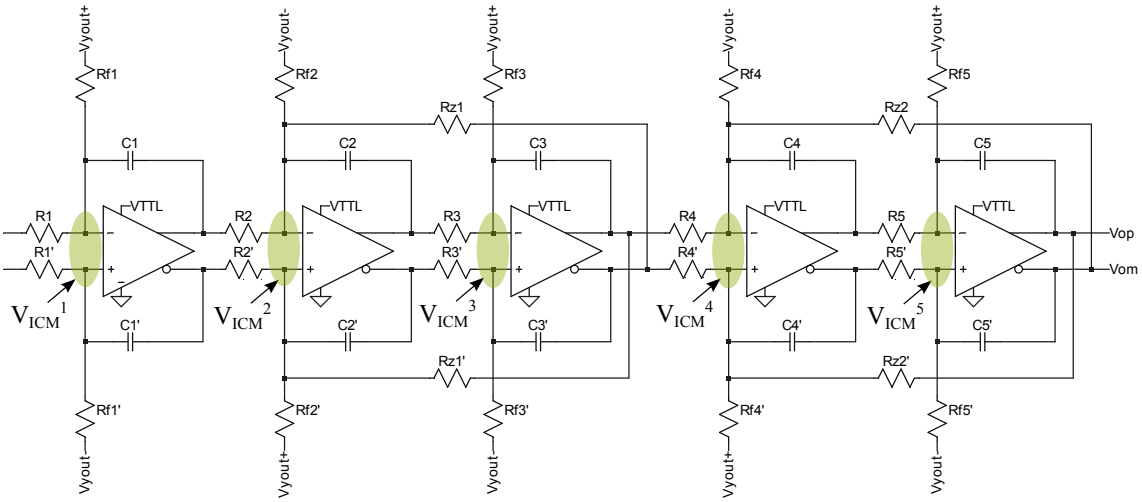


Figure 4.15: Loop filter of the Class D ΔΣM-5

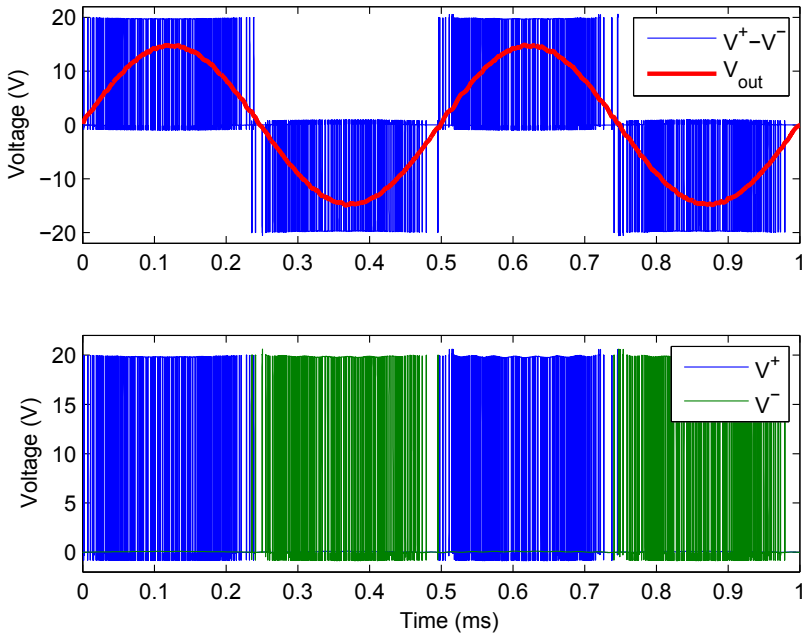


Figure 4.16: Output waveforms of the Class D audio power amplifier with 1.5-bit quantization scheme and without dynamic element matching; top: bitstream (V^+ - V^-) and V_{out}; bottom: V^+ and V^-

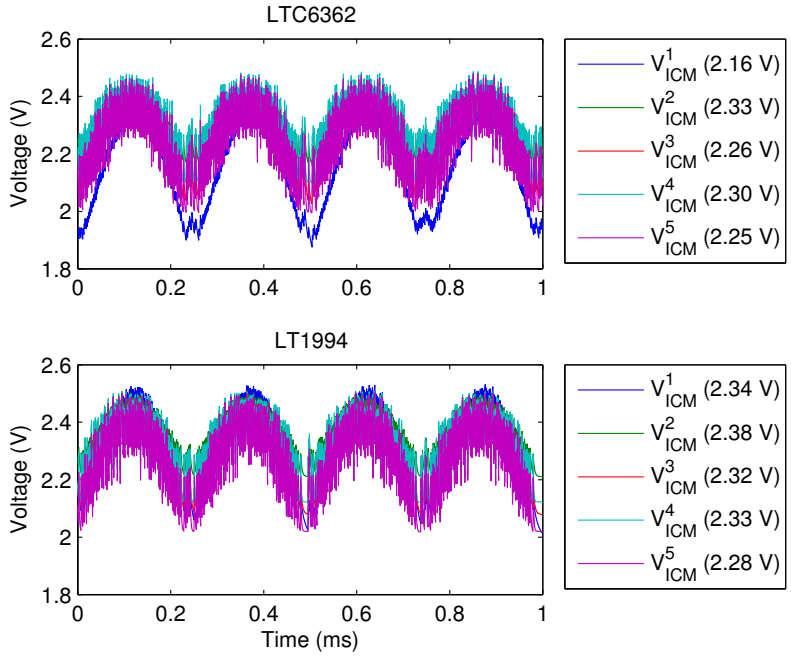


Figure 4.17: Loop filter's virtual ground AC and DC voltages

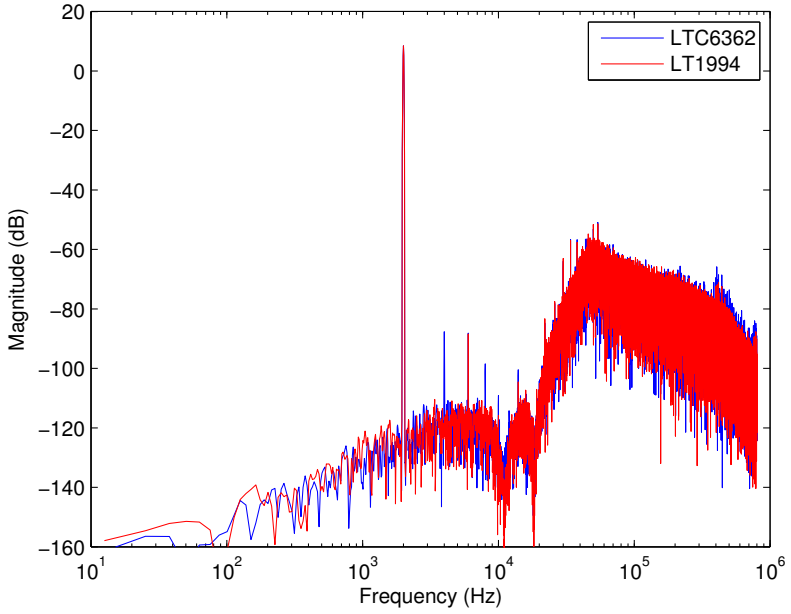


Figure 4.18: FFT of full Class D audio power amplifier without dynamic element matching, with LTC6362 and LT1994 as differential opamps

OpAmp	SNDR (dB)	THD (dB)	F_0 (dB)	HD_2 (dB)	HD_3 (dB)	HD_4 (dB)	HD_5 (dB)	V_{pp} (V)
LTC6362	91.90	-92.88	8.450	-95.99	-96.66	-106.56	-117.92	29.50
LT1994	94.52	-96.65	8.450	-118.59	-97.01	-121.16	-120.44	29.50

Table 4.8: Performance summary of the 1.5-bit Class D audio power amplifier with real output stage and without dynamic element matching

Power output stage electrical analysis

Fig. 4.19 shows the gate voltages and currents of the power output MOSFETs from the left half-bridge of the power output stage, considering a positive output I_{yout} current. The dead-time distortion can be recognized by the small rectangular waves on the V^+ wave during the high to low and low to high transitions. Due to the fact that the output current in this transition is positive, there is reverse recovery of the NMOS back-gate diode as the V^+ node shifts from low to high, creating a small shoot-through current. From the high to low transition no shoot-through current occurs.

Considering one sinusoidal period, the Fig. 4.20 shows the instant switching frequency, dead-time and the output stage delay of the left half-bridge. The V_{out} and the V^+ node voltages are also shown. Due to the 1.5-bit quantization scheme, the average switching frequency is roughly 2/3 of the sampling frequency (1.1 MHz versus 1.6 MHz). The average delay of the half-bridge is around 115 ns and the dead-time is around 18 ns.

Fig. 4.21 shows the graph of the instant power delivered to the load (P_{Load}), the power dissipated by the MOSFETs power supply source ($P_{MOSFETS}$) and the left half-bridge gate driver's power supply sources ($P_{High\ Side}$ and $P_{Low\ Side}$). The power supply source connected to the power output MOSFETs continues to dissipate and absorb power through the hole sinusoidal period due to the fact that it is also connected to the right half-bridge. In the highlighted close-up (Fig. 4.22), there is only power being dissipated from the left half-bridge's gate drivers power supply sources when the transitions occur, except for the high side gate driver, that continues to dissipate power through the R_{Bias} resistor during the time the PMOS transistor is turned on. In the close-up, it is also possible to see the

power dissipated though the reverse recovery phenomenon in the $P_{MOSFETS}$ power supply source.

Due to the fact that the output stage uses 1.5-bit quantization scheme with no dynamic element matching and performs the 0^- state, hard-switching (forcing the power output transistors to counteract the I_{yout} current) rarely occurs, which means that the power supply is minimally disturbed by rarely absorbing the energy flowing in the EMI output low-pass filter.

The Table 4.9 summarizes the power consumption of each branch of the power output stage, the power delivered to the load and their percentage relatively to the total power consumption in the power output stage. The performance regarding how much the PMOS is turned on during a single period ($PMOS_{on}/T_s$), which is proportional to the high side gate driver power dissipation, the number of half-bridge transitions per period, the average sampling frequency, dead-time and delay is also shown. A pie-chart for a graphical visualisation of the consumed power is also presented in Fig. 4.23.

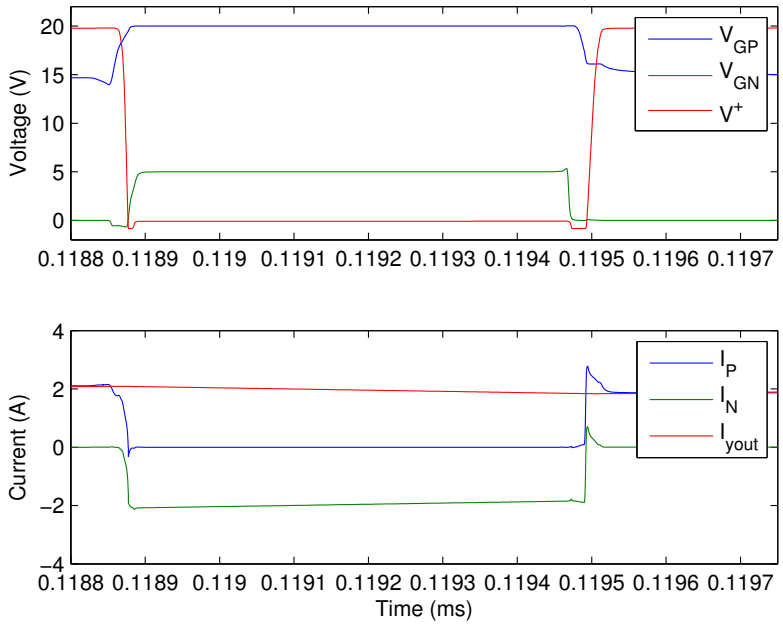


Figure 4.19: Left half-bridge power output stage transitory waveforms; top: V_{GN}, V_{GP} and V^+ waveforms; bottom: $I_{yout} = I_P$ - I_N;

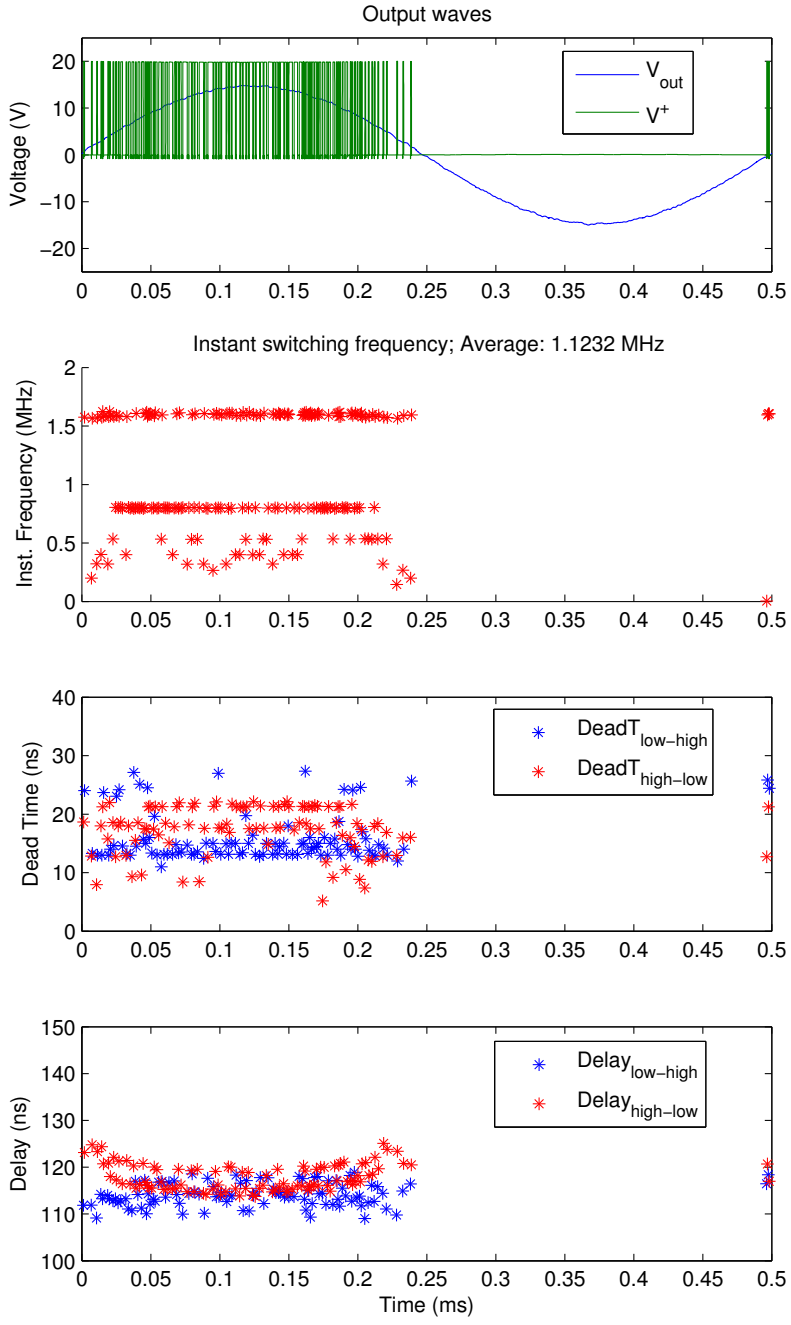


Figure 4.20: Left half-bridge power output stage waveforms; top: V_{yout} and V^+; middle: instant switching frequency; bottom: low to high transition dead-time and delay

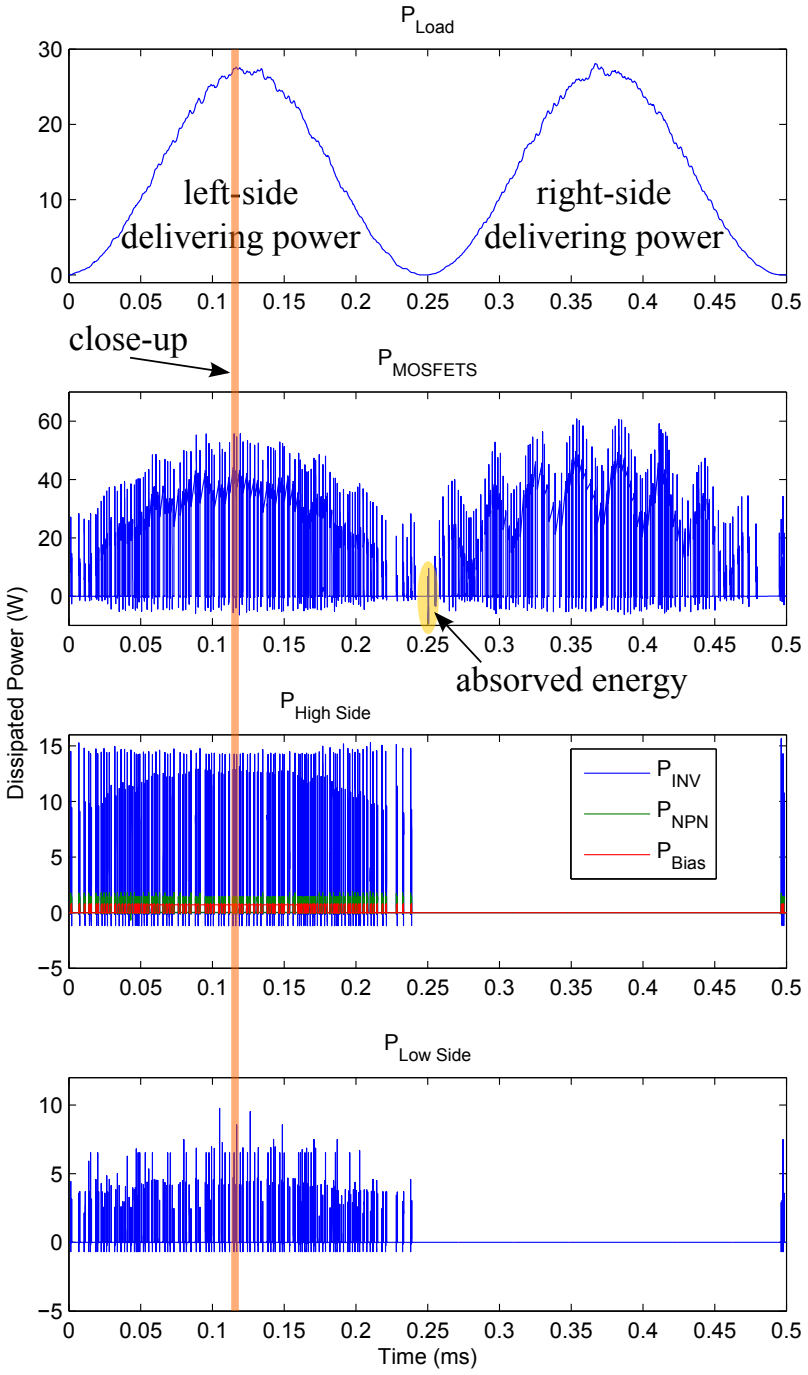


Figure 4.21: Power delivered to the load, power dissipated by the power output MOSFETS power supply source and the power dissipated by the left half-bridge's gate drivers power supply sources; close-up in Fig. 4.22

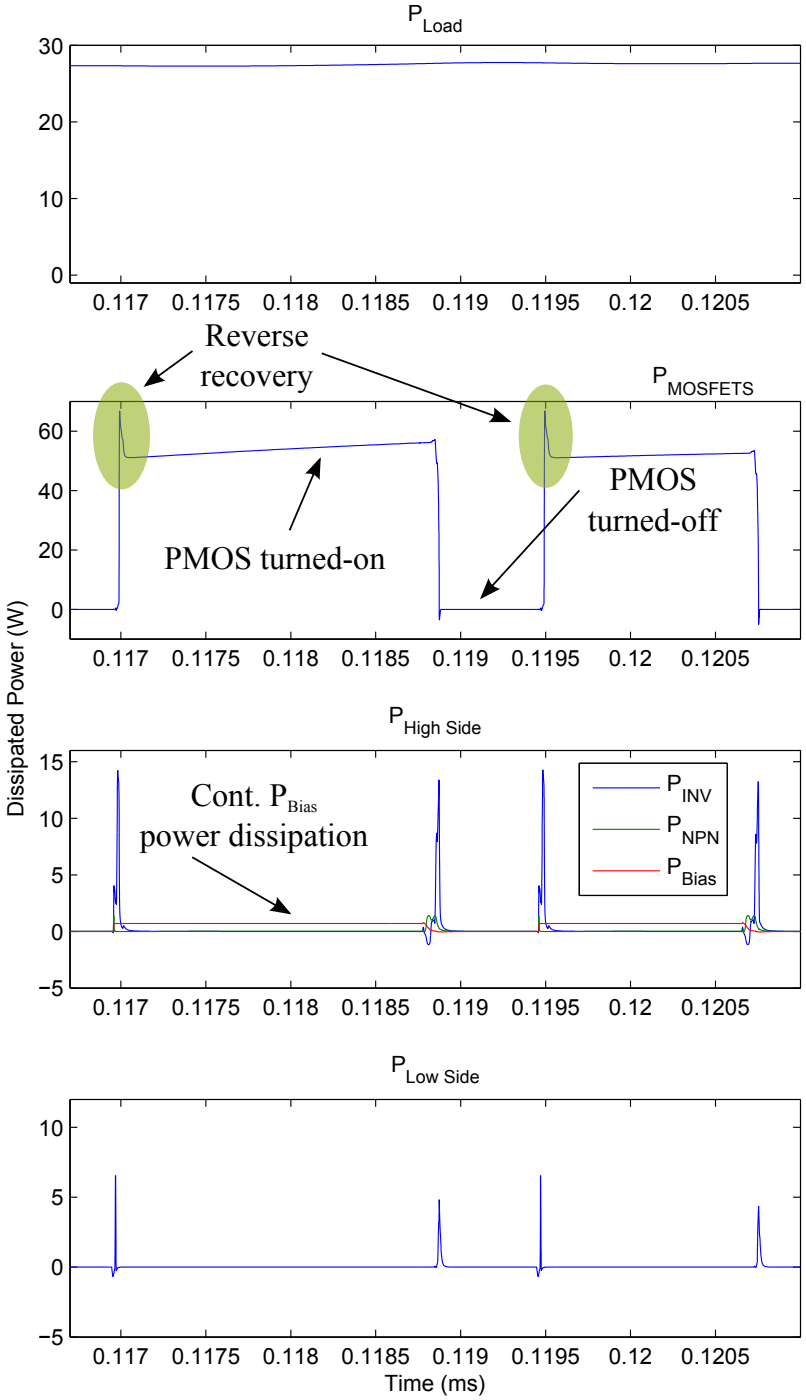
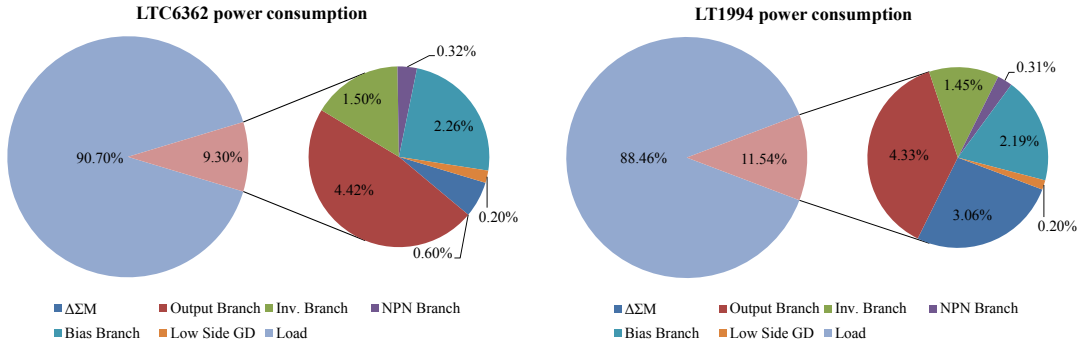


Figure 4.22: Close-up of the power delivered to the load, power dissipated by the power output MOSFETS power supply source and the power dissipated by the left half-bridge's gate drivers power supply sources during two transitions

OpAmp	LTC6362			LT1994		
half-bridge	Left	Right	(%)	Left	Right	(%)
$PMOS_{on}/T_s$ (%)	24.05	23.94	-	23.96	24.14	-
Nr. Trans./T_s	207	207	-	205	205	-
Avg. Samp. Freq. (MHz)	1.11	1.11	-	1.10	1.11	-
Avg. dead-time (low-high) (ns)	14.69	14.82	-	14.92	14.94	-
Avg. dead-time (high-low) (ns)	18.47	18.49	-	18.46	18.32	-
Avg. delay (low-high) (ns)	114.30	114.41	-	114.41	114.49	-
Avg. delay (high-low) (ns)	117.99	118.01	-	117.86	118.05	-
$P_{\Delta\Sigma M}$ (mW)	89.776		0.60	470.890		3.06
$P_{Low\ side\ GD}$ (mW)	15.301	15.292	0.20	15.068	15.104	0.20
P_{Bias} Branch (mW)	169.110	169.110	2.26	168.380	168.370	2.19
P_{NPN} Branch (mW)	24.214	24.203	0.32	23.956	24.027	0.31
P_{INV} Branch (mW)	112.392	112.310	1.50	110.954	111.380	1.45
P_{Output} Branch (mW)	663.230		4.42	666.000		4.33
$P_{Dissipated}$ (W)	1.394		9.30	1.774		11.54
P_{Load} (W)	13.597		90.70	13.596		88.46
P_{Total} (W)	14.992		100.00	15.370		100.00
Power efficiency (%)	90.70			88.46		

Table 4.9: 1.5-bit without dynamic element matching Class D power output stage electrical analysis summary



(a) LTC6362 power comsuption

(b) LT1994 power comsuption

Figure 4.23: Pie-charts of the power consumption analysis for the 1.5-bit Class D audio amplifier without dynamic element matching

4.2.1.3 Real power output stage with dynamic element matching

By introducing the dynamic element matching, the 0-state that is being fed back to the modulator will be the 0^+ and 0^- average, which will eventually lead up to the correct 0-state. This will make the DC voltage of the loop filter's virtual grounds, depicted in Fig. 4.26, to be around the common-mode voltage of the ΔΣM, which will decrease the even order harmonic distortion and the noise floor. The output stage waveforms are presented in Fig. 4.24, where a close-up of the bitstream and the V_{yout} waveform is depicted in Fig. 4.25. As the delay of the half-bridges is dependent if there is a positive or negative dead-time distortion, there will be a mismatch when the output stage if performing successively the 0^+ and the 0^- state, creating small pulses that are being fed back to the modulator. As these small pulses are also being applied to the load and the power output stage is inside the feedback loop, the modulator will eventually correct this error.

The FFT of the Class D audio power amplifier using dynamic element matching is depicted in Fig. 4.27 and the Table 4.10 summarizes the Class D audio power amplifier performance.

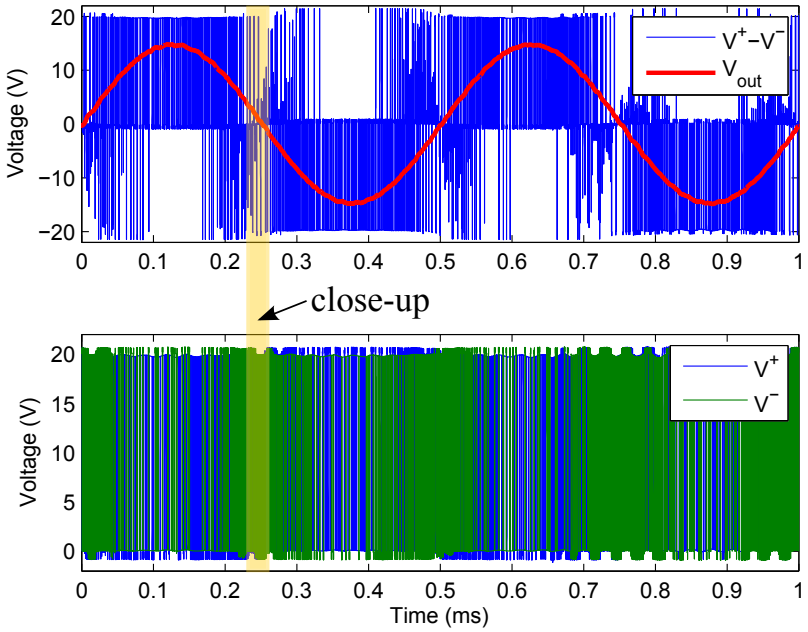


Figure 4.24: Output waveforms of the Class D audio power amplifier with 1.5-bit quantization scheme with dynamic element matching; top: bitstream (V^+ - V^-) and V_{out}; bottom: V^+ and V^-

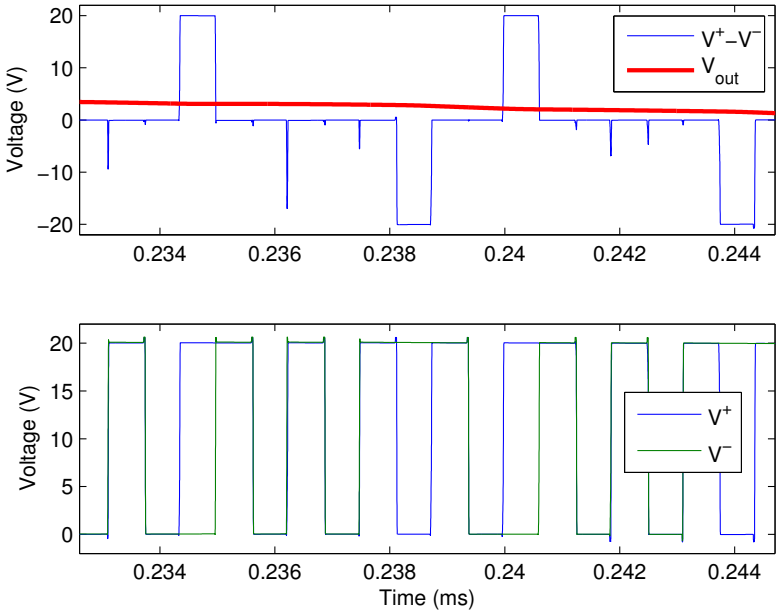


Figure 4.25: Close-up of the output waveforms of the Class D audio power amplifier with 1.5-bit quantization scheme with dynamic element matching; top: bitstream (V^+ - V^-) and V*out*; bottom: V^+ and V^-

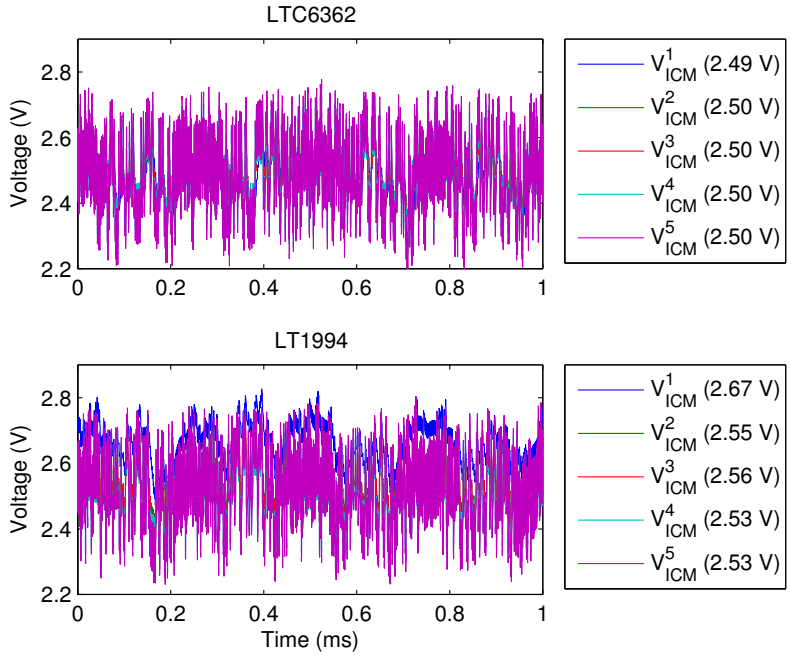


Figure 4.26: Loop filter's virtual ground AC and DC voltages

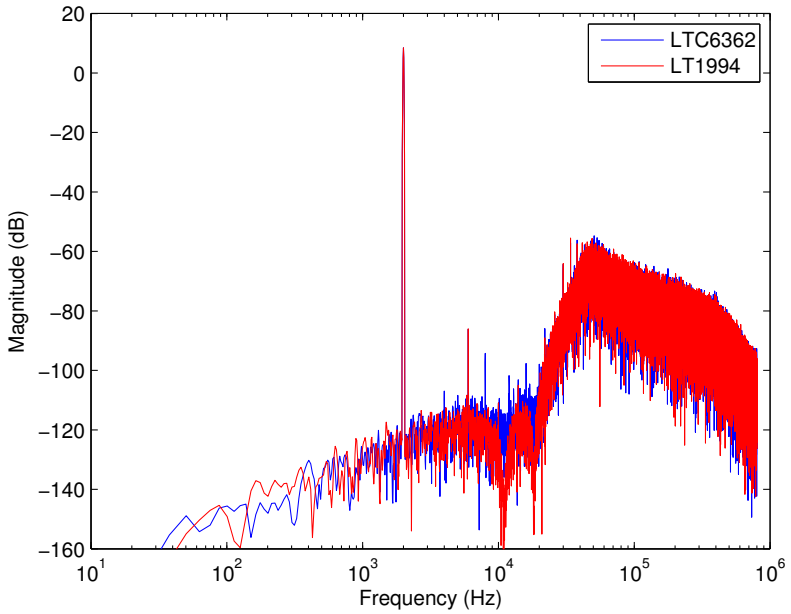


Figure 4.27: FFT of full Class D audio power amplifier using dynamic element matching, with LTC6362 and LT1994 as differential opamps

OpAmp	SNDR (dB)	THD (dB)	F_0 (dB)	HD_2 (dB)	HD_3 (dB)	HD_4 (dB)	HD_5 (dB)	V_{pp} (V)
LTC6362	91.13	-93.16	8.443	-113.83	-94.53	-102.29	-118.11	29.46
LT1994	93.08	-94.37	8.443	-121.60	-94.53	-123.21	-119.00	29.46

Table 4.10: Performance summary of the 1.5-bit Class D audio power amplifier with real output stage and with dynamic element matching

Power output stage electrical analysis

The Fig. 4.28 shows the transitory waveforms of the left half-bridge power output MOSFETs, with $I_{yout} > 0$.

The Fig. 4.29 depicts the switching waveforms of the left side half-bridge, the instant switching frequency, dead-time and delay for one sinusoidal 2 kHz period input. By using dynamic element matching, both half-bridges are always switching in order to correctly perform the 0-state. Therefore the output stage is forced to do hard-switching, which inevitably will pump energy back into the power supply, even though there is a local loop. The dead-time distortion will even increase the high-to-low delay and decrease the low-to-high delay. This depends on the I_{yout} current; if, e.g., the I_{yout} current is negative, (case highlighted in Fig. 4.29), this will create a positive dead-time distortion on the left half-bridge (small rectangular pulses plus V_{CC} on the V^+ voltage) which are inserted by the PMOS back-gate diode, that will immediately pull-up this node from the low to high transition at the start of the dead-time, and will only allow the high to low transition at the end of the dead-time and after the fully discharge of the PMOS back-gate diode.

The instant power delivered to load (P_{Load}), the power dissipated by the power output MOSFETs power supply source ($P_{MOSFETS}$) and the left half-bridge's gate drivers power source dissipation ($P_{High\ Side}$ and $P_{Low\ Side}$) are depicted in Fig. 4.30. It is possible to see that the left half-bridge continues to switch in order to perform the 0-state, which will create the visual distortion in the $P_{MOSFETS}$ graph. This is due to when performing the 0^+ state there will be energy being fed back into the power supply, as the I_{yout} current, that goes through the inductor, has to be continue. An example is displayed in the highlighted

close-up of Fig. 4.30 (Fig. 4.31).

The output bitstream is displayed alongside with the $P_{MOSFETS}$ graph. Considering that, during the +1 state, where the left half-bridge has its high side gate driver activated and is delivering energy to the load, from there it shifts to the 0^+ state, which will force the power output stage to fed back the current that flows through the inductor into the power supply source, creating power supply distortion due to the right half-bridge hard-switching. The Table 4.32 summarizes the power output stage performance when 1.5-bit quantization scheme with dynamic element matching is used and a pie chart representation of the consumed power is also presented in Fig. 4.32.

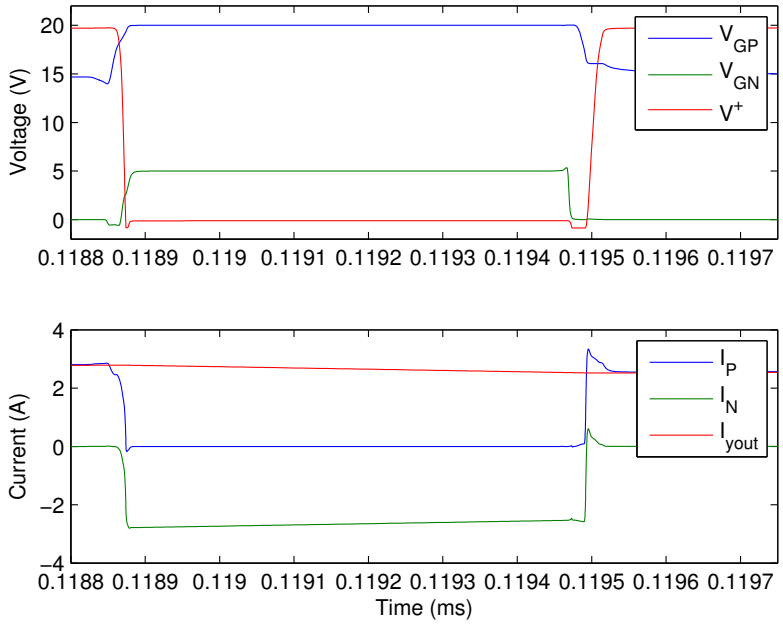


Figure 4.28: Power output stage transitory waves from one half-bridge; top: V_{GN}, V_{GP} and V^+ waveforms; bottom: I_P, I_N and I_{yout} currents

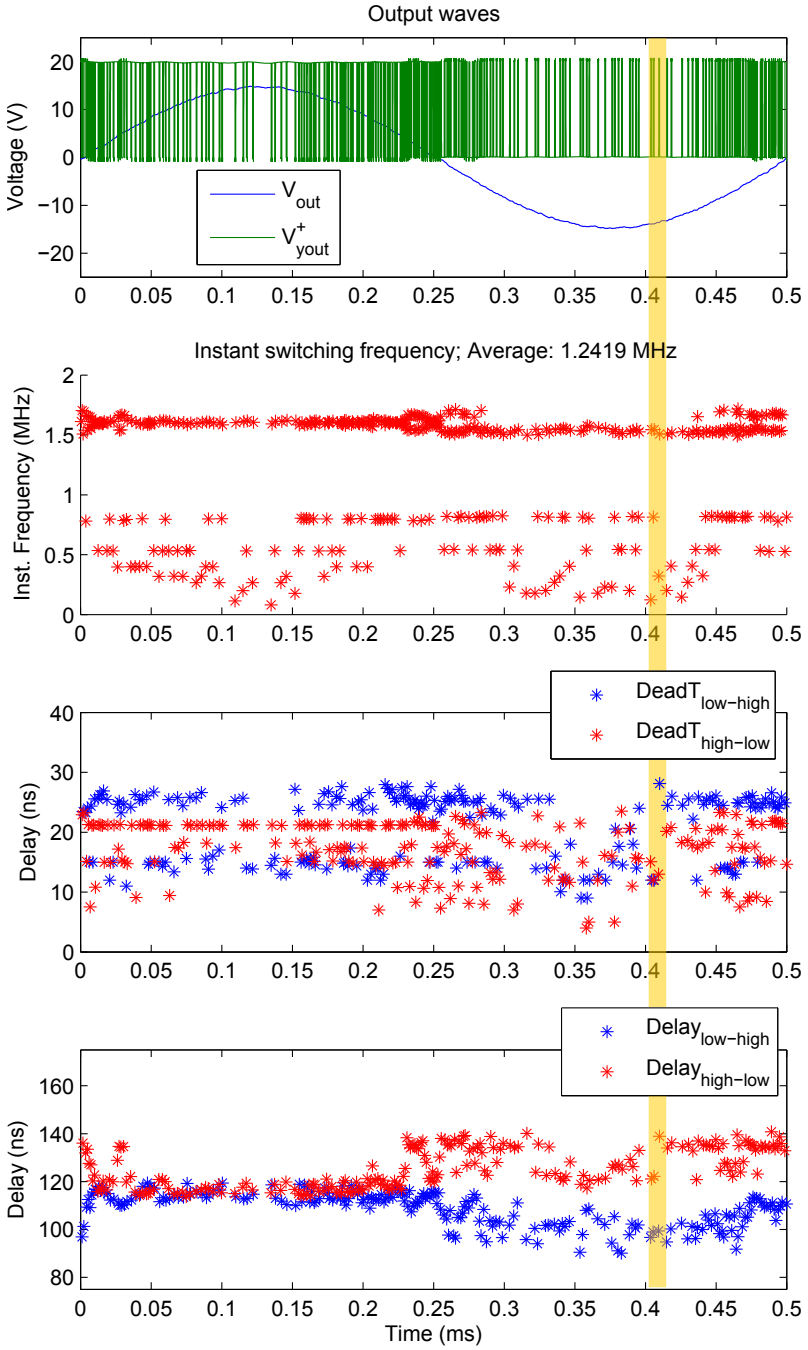


Figure 4.29: Left half-bridge output waveforms, instant switching frequency, dead-time and delay

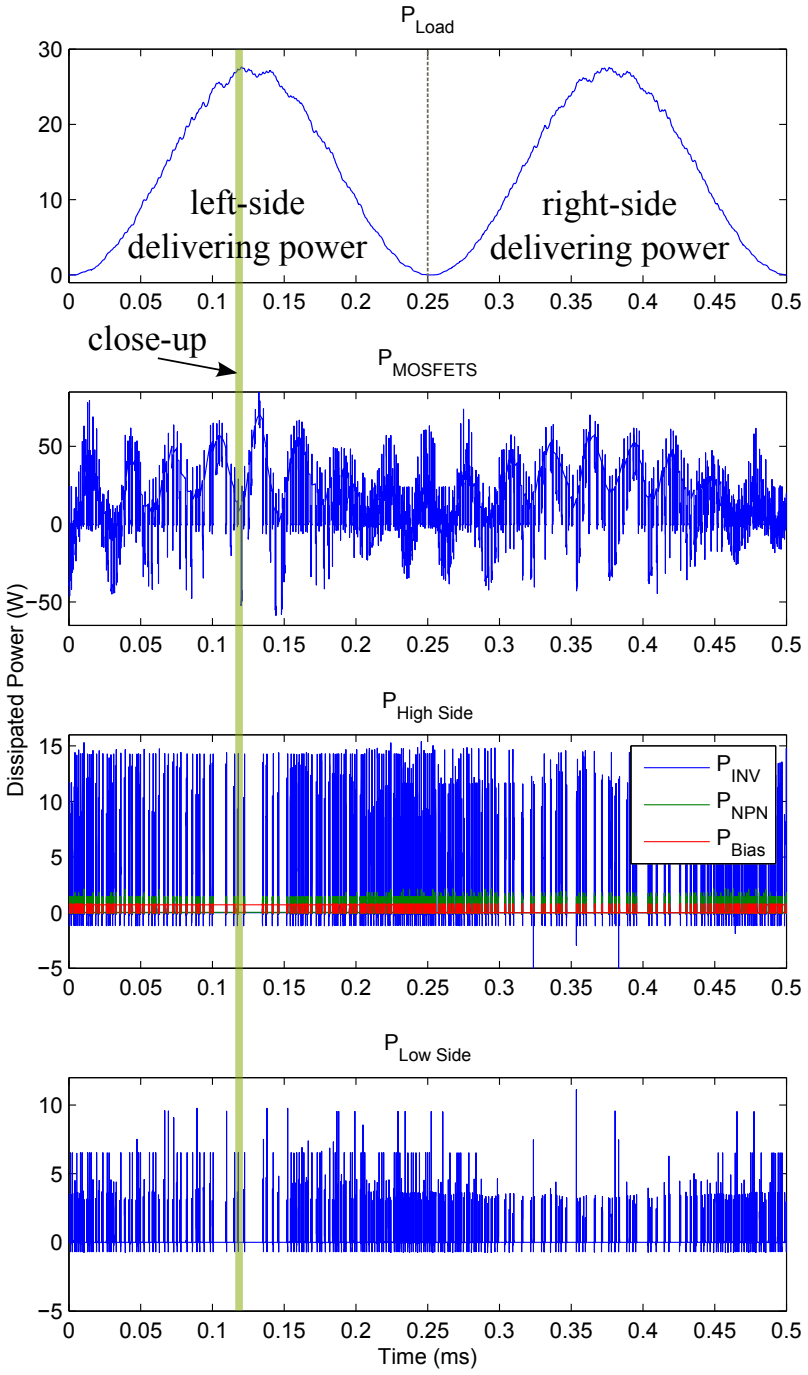


Figure 4.30: Power delivered to the load, power dissipated by the power output MOSFETS power supply source and the power dissipated by the left half-bridge's gate drivers power supply sources; close-up in Fig. 4.22

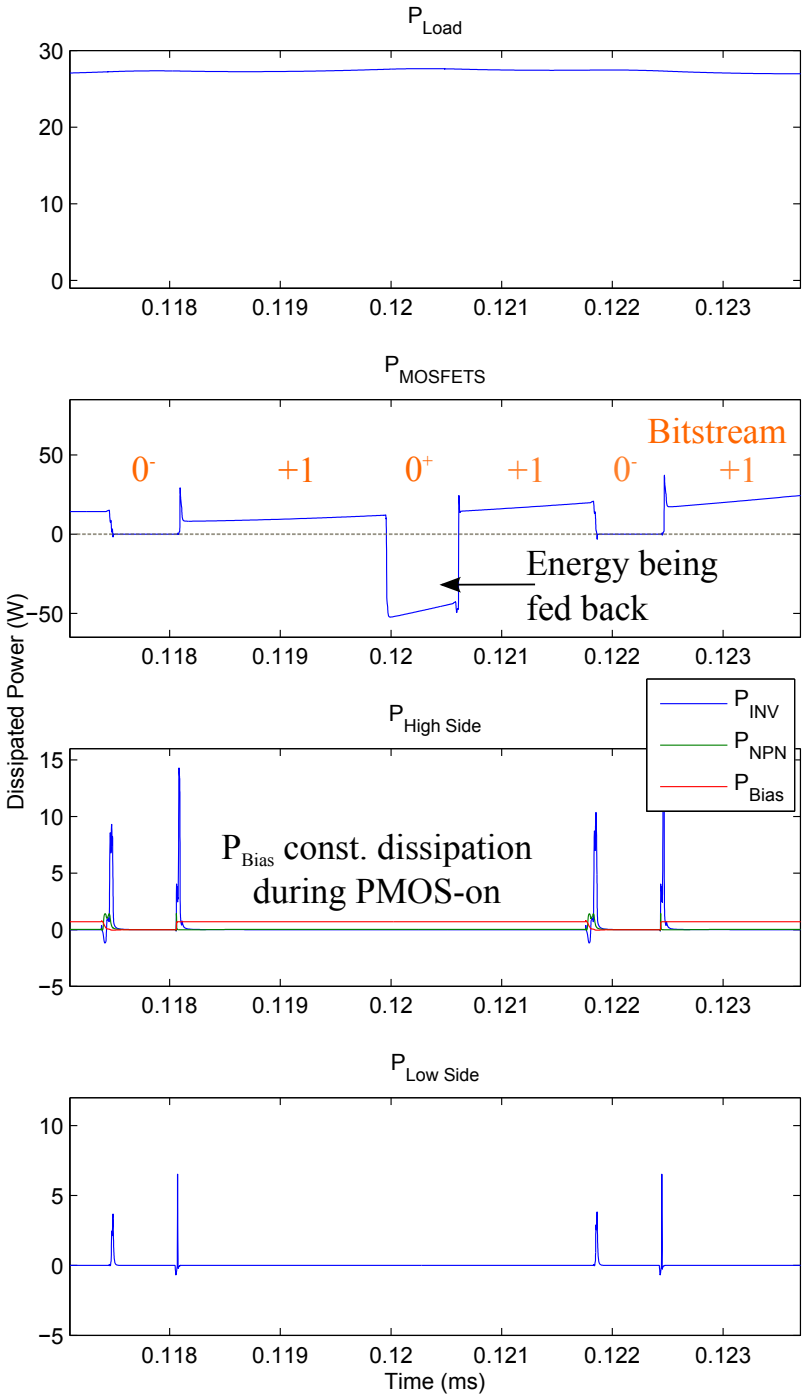
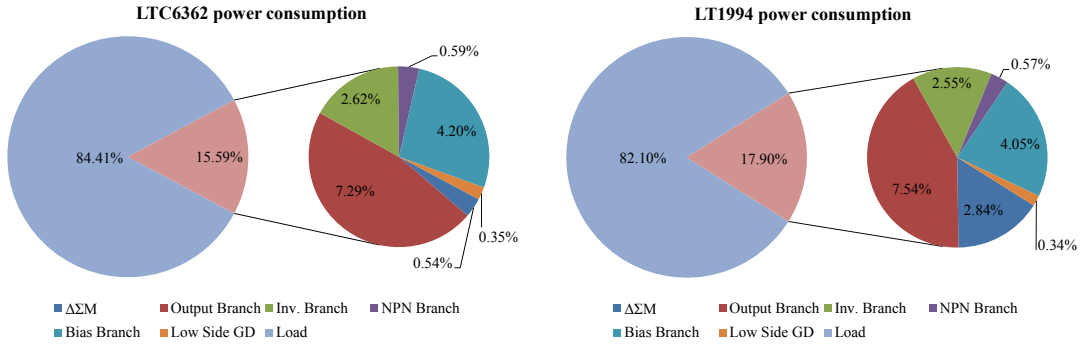


Figure 4.31: Close-up of the tower delivered to the load, power dissipated by the power output MOSFETS power supply source and the power dissipated by the left half-bridge's gate drivers power supply sources with $I_{yout} > 0$

OpAmp	LTC6362			LT1994		
half-bridge	Left	Right	(%)	Left	Right	(%)
$PMOS_{on}/T_s$ (%)	48.23	47.98	-	47.62	47.70	-
Nr. Trans./T_s	407	402	-	408	408	-
Avg. Samp. Freq. (MHz)	1.26	1.26	-	1.25	1.26	-
Avg. dead-time (low-high) (ns)	20.87	20.79	-	20.81	20.80	-
Avg. dead-time (high-low) (ns)	18.10	18.11	-	18.05	17.97	-
Avg. delay (low-high) (ns)	108.98	109.17	-	109.10	109.13	-
Avg. delay (high-low) (ns)	124.81	124.86	-	124.72	124.72	-
$P_{\Sigma\Delta M}$ (mW)	87.596		0.54	468.790		2.84
$P_{Low\ side\ GD}$ (mW)	28.432	28.094	0.35	28.354	28.211	0.34
P_{Bias} Branch (mW)	337.390	337.640	4.20	334.970	335.050	2.19
P_{NPN} Branch (mW)	47.561	47.043	0.59	47.507	47.331	0.57
P_{INV} Branch (mW)	211.871	209.135	2.62	211.692	210.681	2.55
P_{Output} Branch (W)	1.1725		7.29	1.2461		7.54
$P_{Dissipated}$ (W)	2.507		15.59	2.958		17.90
P_{Load} (W)	13.574		84.81	13.573		82.10
P_{Total} (W)	16.082		100.00	16.532		100.00
Power efficiency (%)	84.41			82.10		

Table 4.11: 1.5-bit with dynamic element matching Class D power output stage electrical analysis summary



(a) LTC6362 power comsuption (b) LT1994 power comsuption

Figure 4.32: Pie-charts of the power consumption analysis for the 1.5-bit Class D audio amplifier with dynamic element matching

4.2.2 1-bit 5^{th} Order $\Delta\Sigma$ Modulator @ 1.60 MHz

The 1-bit Class D audio power amplifier will be briefly analysed in order to serve as term of comparison for the 1.5-bit quantization scheme. Since the $\Delta\Sigma$M with 1-bit quantization scheme requires a higher close-loop gain than the 1.5-bit quantization scheme, this will result in a low output swing of the modulator and therefore lesser power delivered to the load. In this case, since the system no longer has the 0-state, the problems associated with the feedback mismatch that appeared in the 1.5-bit quantization scheme are eliminated.

4.2.2.1 Ideal 100-ns delay power output stage

The Fig. 4.33 shows the FFT of the output wave V_{out} using an ideal 100-ns delay output stage and the Table 4.12 summarizes its performance.

OpAmp	SNDR (dB)	THD (dB)	F_0 (dB)	HD_2 (dB)	HD_3 (dB)	HD_4 (dB)	HD_5 (dB)	V_{pp} (V)
Ideal	79.65	-85.02	6.710	-105.95	-87.62	-111.25	-114.06	24.14
LTC6362	79.36	-85.59	6.716	-107.88	-90.72	-120.16	-119.926	24.16
LT1994	79.29	-87.07	6.710	-108.39	-90.50	-111.67	-119.93	24.14

Table 4.12: Performance summary of the 1-bit Class D audio power amplifier with 100-ns ideal output stage

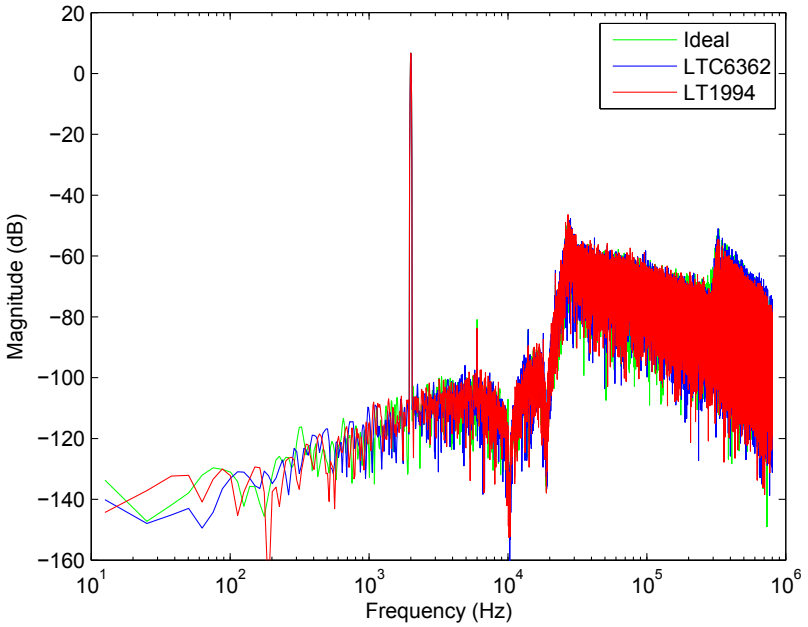


Figure 4.33: FFT of the Class D audio power amplifier using 1-bit quantization scheme and the ideal, LTC6362 and LT1994 as differential opamps with an ideal 100-ns delay output stage

4.2.2.2 Real power output stage

The output waveforms are depicted in Fig. 4.34, where it is possible to see the 1-bit nature of the bitstream due to the V^+ and V^- node voltage which have opposite signs of each other. The Fig. 4.35 shows the virtual ground nodes of the loop filter, where, since the feedback common mode voltage is constant, these DC voltages do not differ from the common-mode voltage of the $\Delta\Sigma$M. Fig. 4.36 depicts the FFT of the Class D power output stage with the real output stage inside the feedback loop and with 1-bit quantization scheme, using the LTC6362 and the LT1994 opamps. The Table 4.13 summarizes their performance.

OpAmp	SNDR (dB)	THD (dB)	F_0 (dB)	HD_2 (dB)	HD_3 (dB)	HD_4 (dB)	HD_5 (dB)	V_{pp} (V)
LTC6362	79.70	-84.63	6.981	-111.16	-87.86	-112.98	-111.27	24.92
LT1994	79.57	-84.48	6.974	-108.42	-88.33	-107.54	-111.91	24.88

Table 4.13: AC performance summary of the 1-bit Class D audio power amplifier with the real power output stage inside the feedback loop

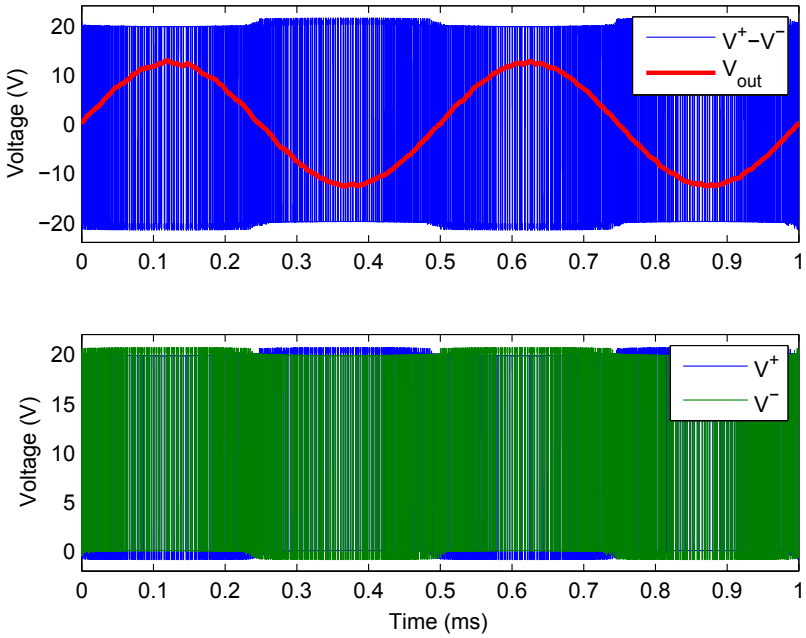


Figure 4.34: Output waveforms of the Class D audio power amplifier with 1-bit quantization scheme; top: bitstream (V^+ - V^-) and V_{out}; bottom: V^+ and V^-

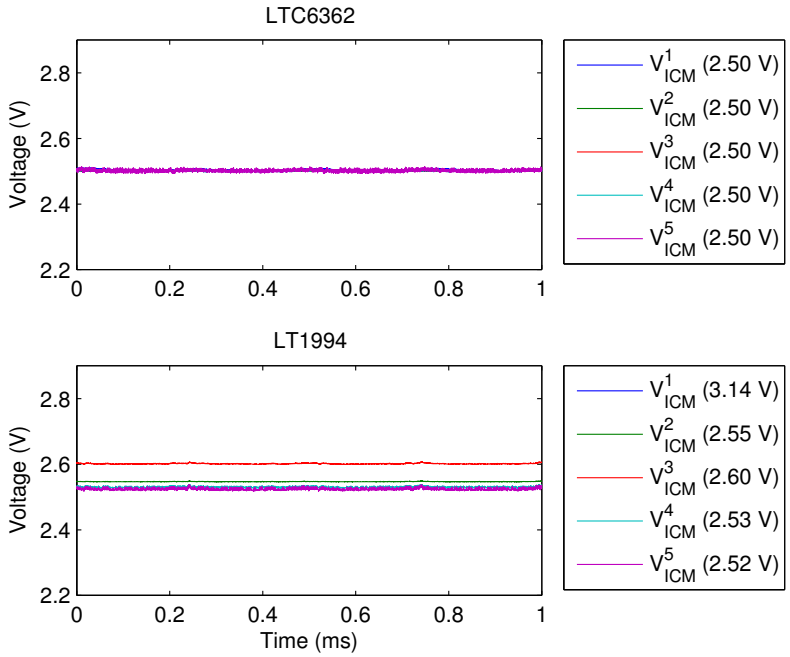


Figure 4.35: Loop filter's virtual ground AC and DC voltages

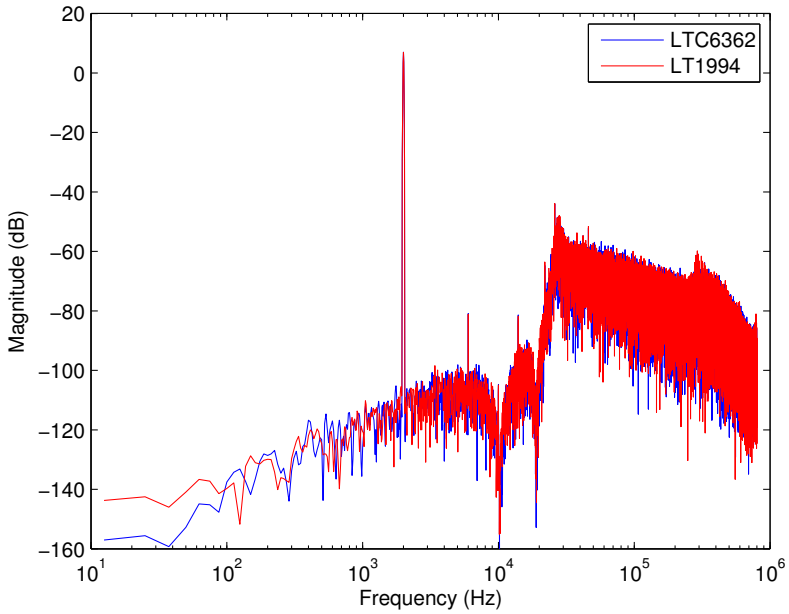


Figure 4.36: FFT of full Class D audio power amplifier using 1-bit quantization scheme with LTC6362 and LT1994 as differential opamps

Power output stage electrical analysis

The output waveforms, instant switching frequency, the instant dead-time and the instant delay are depicted in Fig. 4.37. Fig. 4.38 shows the instant power delivered to the load, the power dissipated by the MOSFETs power supply source and the left half-bridge's gate drivers power supply sources dissipation. A pie-chart of the dissipated power is also shown in Fig. 4.39.

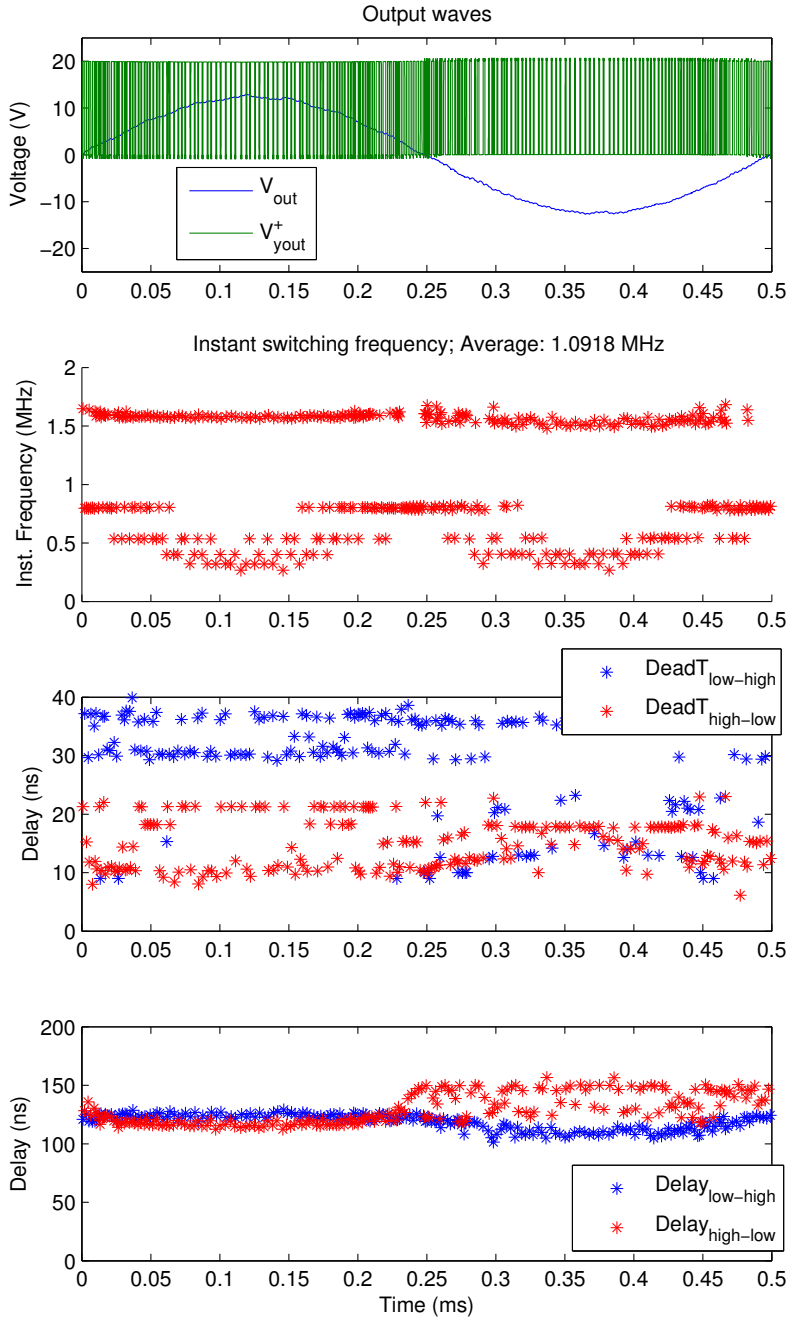


Figure 4.37: Left half-bridge output waveforms, instant switching frequency, dead-time and delay

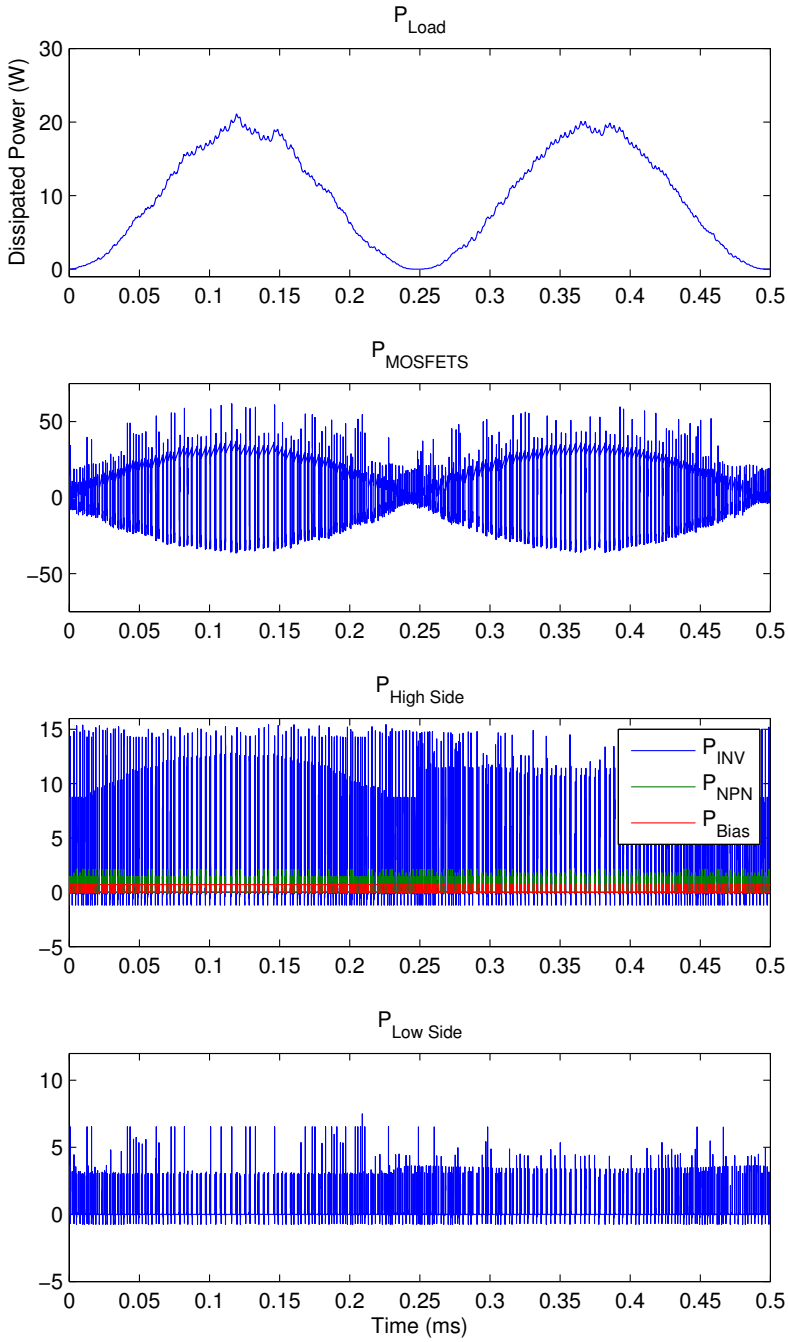
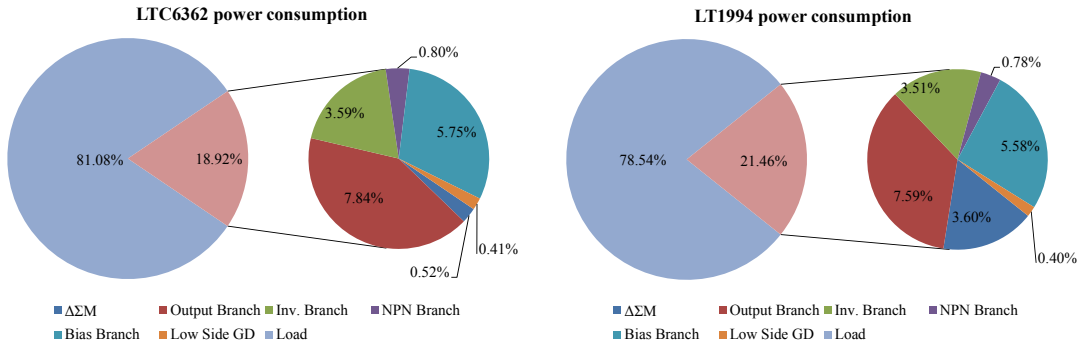


Figure 4.38: Power delivered to the load, power dissipated by the power output MOSFETS power supply source and the power dissipated by the left half-bridge's gate drivers power supply sources

OpAmp	LTC6362			LT1994		
half-bridge	Left	Right	(%)	Left	Right	(%)
$PMOS_{on}/T_s$ (%)	51.73	51.38	-	51.62	51.42	-
Nr. Trans./T_s	409	409	-	410	410	-
Avg. Samp. Freq. (MHz)	1.09	1.09	-	1.09	1.09	-
Avg. dead-time (low-high) (ns)	29.63	29.37	-	29.44	29.50	-
Avg. dead-time (high-low) (ns)	15.15	15.03	-	15.01	15.06	-
Avg. delay (low-high) (ns)	119.30	129.36	-	118.03	119.36	-
Avg. delay (high-low) (ns)	119.34	129.23	-	129.32	127.92	-
$P_{\Sigma\Delta M}$ (mW)	62.409		0.52	443.850		3.60
$P_{Low\ side\ GD}$ (mW)	24.557	24.503	0.41	24.686	26.694	0.40
P_{Bias} Branch (mW)	343.910	343.900	5.75	343.850	343.860	5.58
P_{NPN} Branch (mW)	48.115	48.119	0.80	48.315	48.317	0.78
P_{INV} Branch (mW)	241.946	214.971	3.59	216.273	216.160	3.51
P_{Output} Branch (W)	0.937		7.84	0.935		7.59
$P_{Dissipated}$ (W)	2.263		18.92	2.645		21.46
P_{Load} (W)	9.696		81.08	9.683		78.54
P_{Total} (W)	11.959		100.00	12.328		100.00
Power efficiency (%)	81.08			78.54		

Table 4.14: 1-bit quantization scheme Class D power output stage electrical analysis summary



(a) LTC6362 power comsuption (b) LT1994 power comsuption

Figure 4.39: Pie-chart power consumption analysis for the 1-bit Class D audio amplifier

4.2.3 Summary

The Table 4.15 presents the summary of the Class D audio power amplifier using either 1-bit and 1.5-bit quantization scheme, with and without dynamic element matching. The results from the ideal opamps with the ideal 100-ns delay power output stage are also shown for comparison (which are presented as the ideal case).

Concerning the 1.5-bit quantization scheme, the highest power efficiency is achieved by using the LTC6362 (which has a low power dissipation) without dynamic element matching. Nonetheless, as the LTC6362 has poorer characteristics than the LT1994, it presents a lower SNDR with higher THD and even order harmonics, due to the fact that the virtual grounds of the loop filter are being constantly pushed down. When dynamic element matching is used the number of transitions per sinusoidal period (Nr. Sw/T_s) almost double, increasing the power dissipation in the gate drivers and the power output transistors, which translates in a lower power efficiency. As the DC virtual grounds voltage of the loop filter now remains virtually constant, when in comparison with the system without the dynamic element matching, the even order harmonic distortion are reduced, specially when the LTC6362 is used. Nonetheless, the noise floor remains practically the same as there is no noise in the simulation.

From this preliminary data, taking into account the power efficiency, the maximum SNDR, the minimum THD and the harmonic distortion, the dynamic element matching can be disregarded if the LT1994 differential opamp is used. Another main reason in order to eliminate the dynamic element matching is that the power efficiency decreases

significantly (approx. 6 %) regarding the best performance.

The Class D audio amplifier with the 1-bit quantization scheme has a similar performance in comparison to the ideal 100 ns delay power output stage. The average switching per period is also similar to the 1.5-bit quantization with dynamic element matching, as expected.

Parameter	1.5-bit QS					1-bit QS		
	Ideal	without DEM		with DEM				
		LTC6362	LT1994	LTC6362	LT1994	Ideal	LTC6362	LT1994
V_{pp} (V)	13.94	14.75	14.75	14.73	14.73	12.07	12.46	12.44
Nr. Sw/T_s	-	207	205	407	402	-	409	410
SNDR (dB)	96.23	91.90	94.52	91.13	93.08	79.65	79.70	79.57
THD (dB)	-98.88	-92.88	-96.65	-93.16	-94.37	-85.02	-84.63	-84.48
HD_2 (dB)	-121.94	-95.99	-118.59	-113.83	-121.60	-105.95	-111.16	-108.42
HD_3 (dB)	-99.22	-96.66	-97.01	-94.53	-94.53	-87.62	-87.86	-88.33
HD_4 (dB)	-119.97	-106.56	-121.16	-102.29	-123.21	-111.25	-112.98	-107.54
HD_5 (dB)	-121.72	-117.92	-120.44	-118.11	-119.00	-114.06	-111.27	-111.91
$P_{\Sigma\Delta M}$ (mW)	-	89.776	470.890	87.596	468.790	-	62.409	443.850
$P_{LS\ GD}$ (mW)	-	30.593	30.172	56.526	56.565	-	49.060	49.380
$P_{HS\ GD}$ (W)	-	0.611	0.607	1.190	1.187	-	1.213	1.216
$P_{Out.\ Bra.}$ (W)	-	0.663	0.666	1.172	1.246	-	0.937	0.935
$P_{Dissipated}$ (W)	-	1.394	1.774	2.507	2.958	-	2.263	2.645
P_{Load} (W)	-	13.597	13.596	13.574	13.573	-	9.696	9.683
P_{Total} (W)	-	14.992	15.370	16.082	16.532	-	11.959	12.328
Eff. (%)	-	90.69	88.46	84.41	82.10	-	81.08	78.54

Table 4.15: Electrical simulations performance summary

Chapter 5

Class D Audio Amplifier Prototype

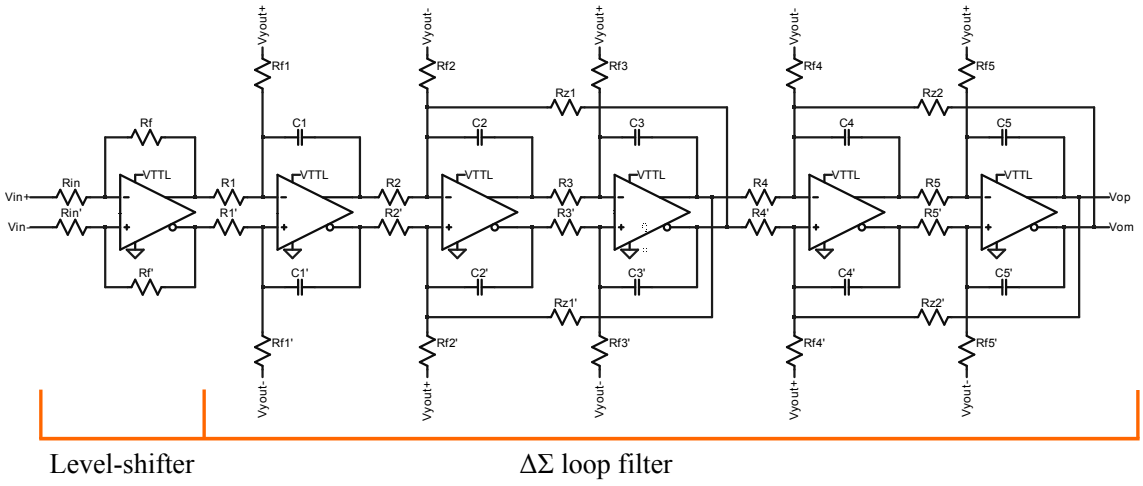
This chapter presents the experimental results measured using several Class D audio amplifier prototypes. From the electrical simulation results presented in subsection 4.2, concerning the 1.5-bit quantization scheme, the use of the dynamic element matching technique can be disregarded as it has a lower power efficiency and it presents no improvements in the SNDR nor the THD of the Class D audio amplifier.

Two $\Delta\Sigma$M versions were implemented, one with 1-bit and the other with 1.5-bit quantization schemes, and both of these versions uses the LT1994 opamp. Although the LT1994 opamp presents a higher power dissipation than the LTC6362 opamp, during the experimental prototyping and testing the LTC6362 opamps often kept failing and malfunctioning without any warning. Due to this reason, the LT1994 opamp proved to be more robust and it was selected instead of the LTC6362 opamp. The manufacturer, Linear Technologies, was inquired about the problem with the LTC6362 opamp, but at the moment of the writing of this thesis the reason for the low reliability of the LTC6362 opamp is still unknown.

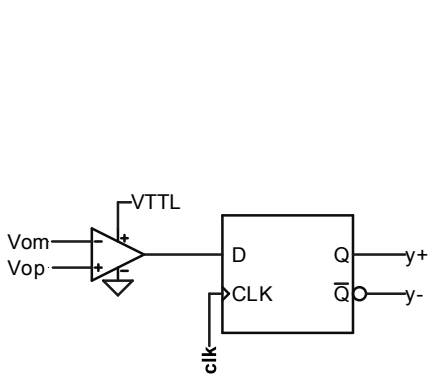
The complete schematic, PCB layout and the bill of materials (BoM) in order to build the prototype are also presented in this chapter.

5.1 Class D Audio Amplifier Complete Schematic

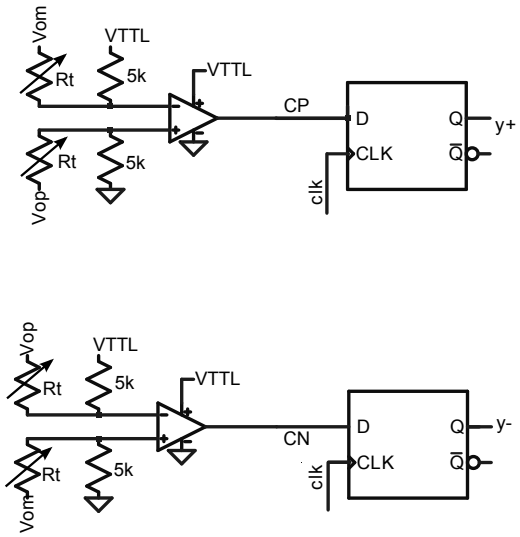
The complete schematic of the Class D audio power amplifier is presented in Fig. 5.1 and in Fig. 5.2. The first figure depicts the schematic of the CT 5^{th} order $\Delta\Sigma$M with the two different quantizations schemes and the second figure the schematic of the proposed power output stage.



(a) CT 5^{th} order $\Delta\Sigma$M



(b) 1-bit quantization scheme



(c) 1.5-bit quantization scheme

Figure 5.1: Schematics the $\Delta\Sigma$Ms with 1-bit and 1.5-bit quantization schemes

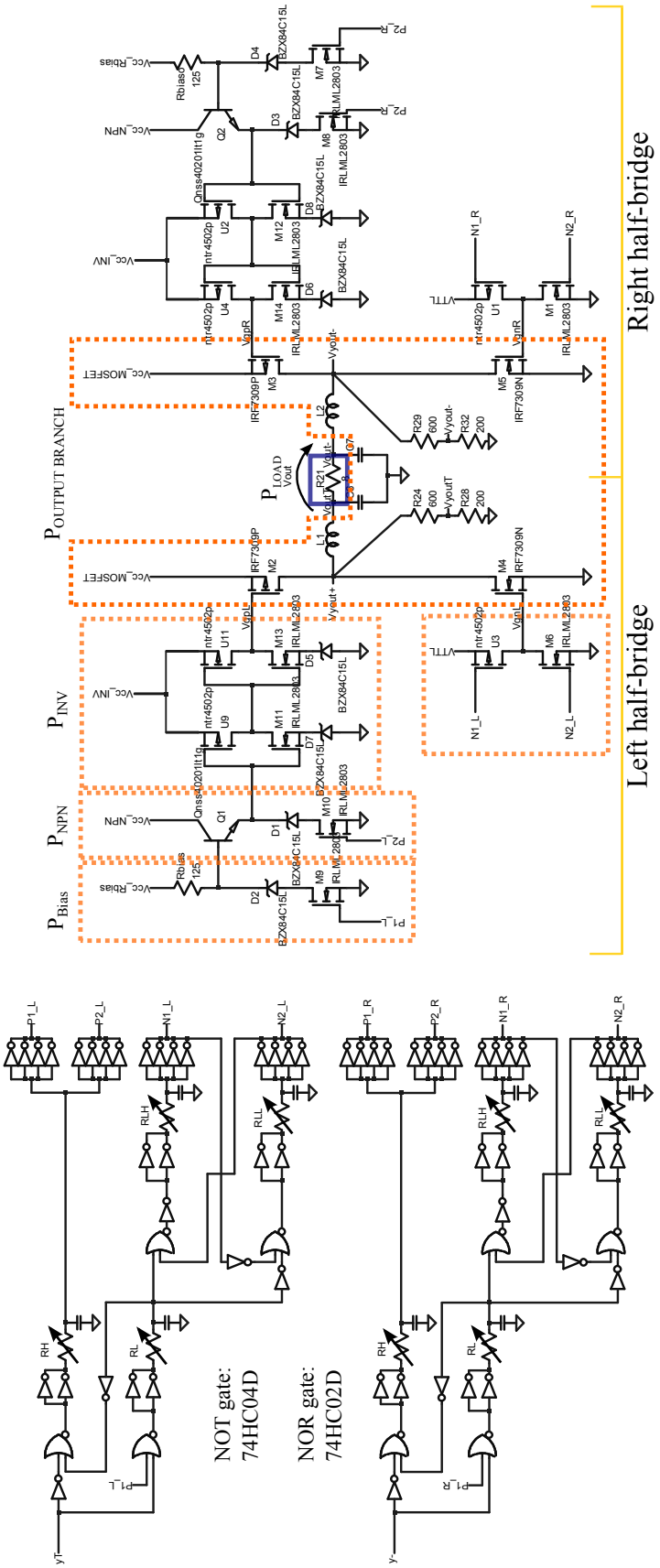


Figure 5.2: Complete power output stage schematic with 20 V power supply

5.2 Class D Audio Amplifier PCB Layout

Although the Class D ΔΣM has different optimization values when using either 1.5-bit or 1-bit quantization schemes, in order to cut down production costs the ΔΣM PCB layout should be designed so that it can support both quantization schemes. This can be accomplished by either soldering or bypassing certain components.

The layout of the ΔΣM prototype PCB allows the implementation of any CT fully-differential ΔΣM up to 7^{th} order either as standalone or as Class D audio amplifier ΔΣM, with the use of 1.5-bit or 1-bit quantization schemes. The use of the MSO-8 package with a standard pinout for the fully-differential opamps allows to test different opamps from different manufacturers (Linear Technologies, Texas Instrumentals, etc).

Since the Class D power output stage is independent of the used quantization scheme, it does not require any additional tweaking in order to work with the desired quantization scheme.

5.2.1 ΔΣM PCB Layout

The ΔΣM PCB which uses 1.5-bit quantization scheme is presented in Fig. 5.3(a) (top layer) and Fig. 5.3(b) (bottom layer). The input is made by a 3-pin header which allows the first fully-differential opamp to act either as a voltage level-shifter or a single-ended-to-differential converter, depending on how the input pins are connected. This approach will allow to easily switch the input between a fully-differential input or a simple audio source, such as a portable MP3 player.

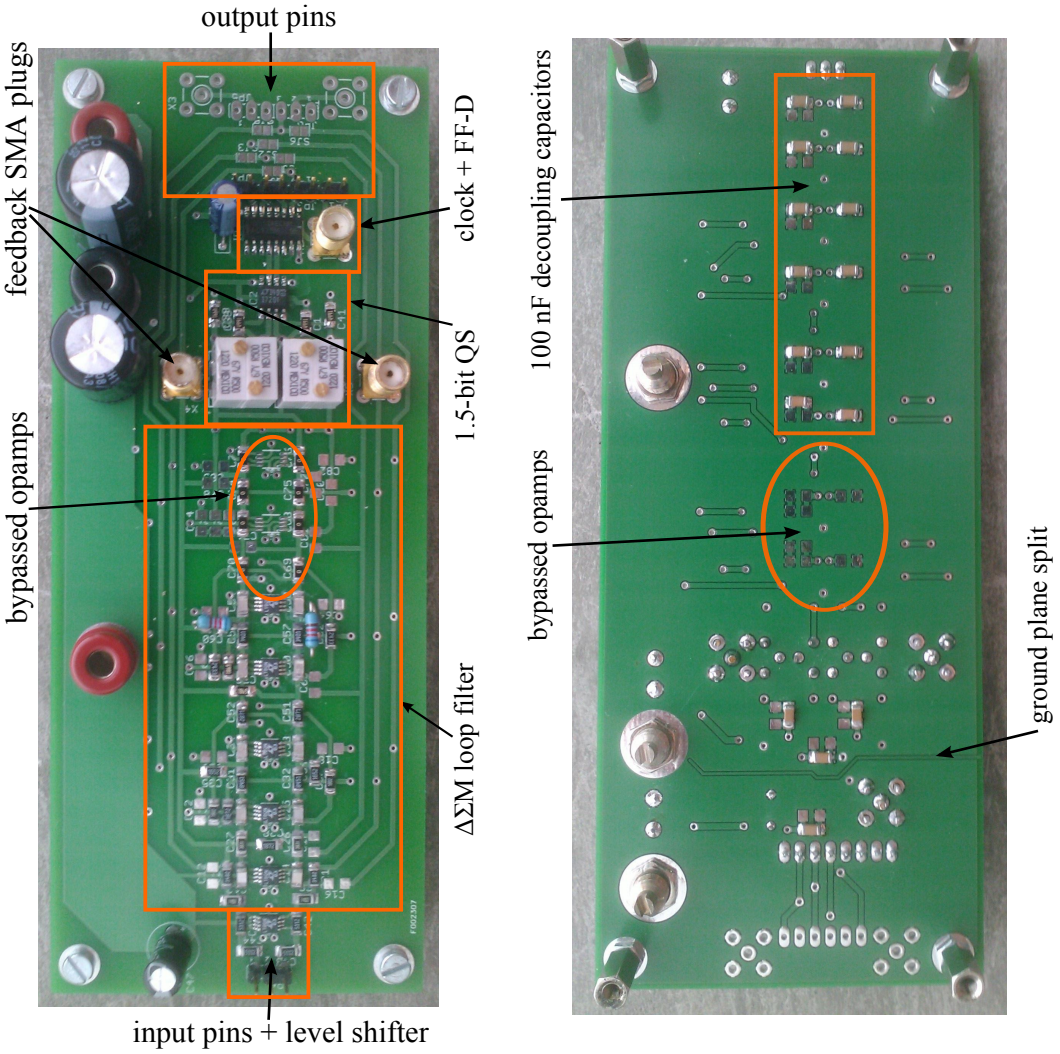
The feedback from the power output stage is made through 50 Ω cables, which connects the ΔΣM and the power output stage through SMA plugs. These can provide good signal isolation, as they have a tubular conducting shield connected to the ground plane, at only one end of the cable, in order to prevent ground-loops.

The quantization scheme is defined by either soldering the threshold voltage comparator (described in chapter 4.1.1.1), which will make the system behave as an 1.5-bit quantization scheme, or just by short-circuiting the output of the integrator stage (V_{op} and V_{om} nodes) to the input of the comparator, which will define the system as 1-bit. This

is done in Fig. 5.4(a) (top layer) and Fig. 5.4(b) (bottom layer) which presents the ΔΣM PCB for the 1-bit quantization scheme, where the threshold comparator was bypassed in order to behave as a simple comparator.

The input buffer, the loop filter and the comparator have a separate power supply from the FF-D, to prevent switching noise from the digital section of the circuit to reach the analog section. The ground plane is partially spilt in order to enhance this isolation. Both power supplies are decoupled by using 100 μF and 10 μF electrolytic capacitors on the PCB's power supply connector and 100 nF decoupling ceramic capacitors as close as possible to power supply pin of each chip, except for the differential opamps which also have another 100 nF decoupling capacitor at the V_{OCM} pin. The FF-D is driven by an external clock signal connected through a SMA plug.

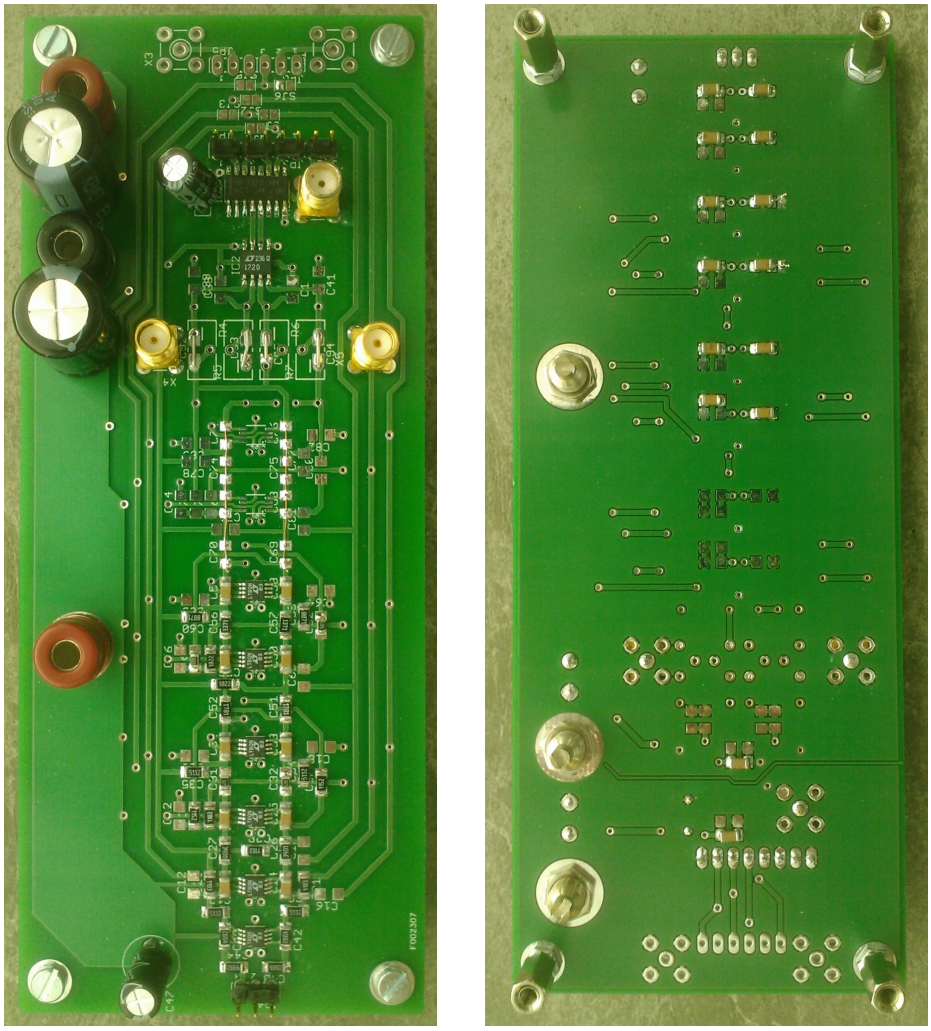
The last row of pin headers and jumpers have the purpose to set the ΔΣM as a standalone device or to set it as a ΔΣM for a Class D audio amplifier, where the signal is send to the power output stage through SMA connectors.



(a) Top layer

(b) Bottom layer (ground plane)

Figure 5.3: Class D 5^{th} order ΔΣM PCB with 1.5-bit quantization scheme



(a) Top layer (b) Bottom layer (ground plane)

Figure 5.4: Class D 5^{th} order $\Delta\Sigma$M PCB with 1-bit quantization scheme

5.2.2 Power output stage PCB layout

The power output stage PCB, depicted in Fig. 5.5(a) (top layer) and Fig. 5.5(b) (bottom layer), has the complete H-bridge in a single board, which will minimize stray inductances due to long paths, preventing ringing transients during the switching operation.

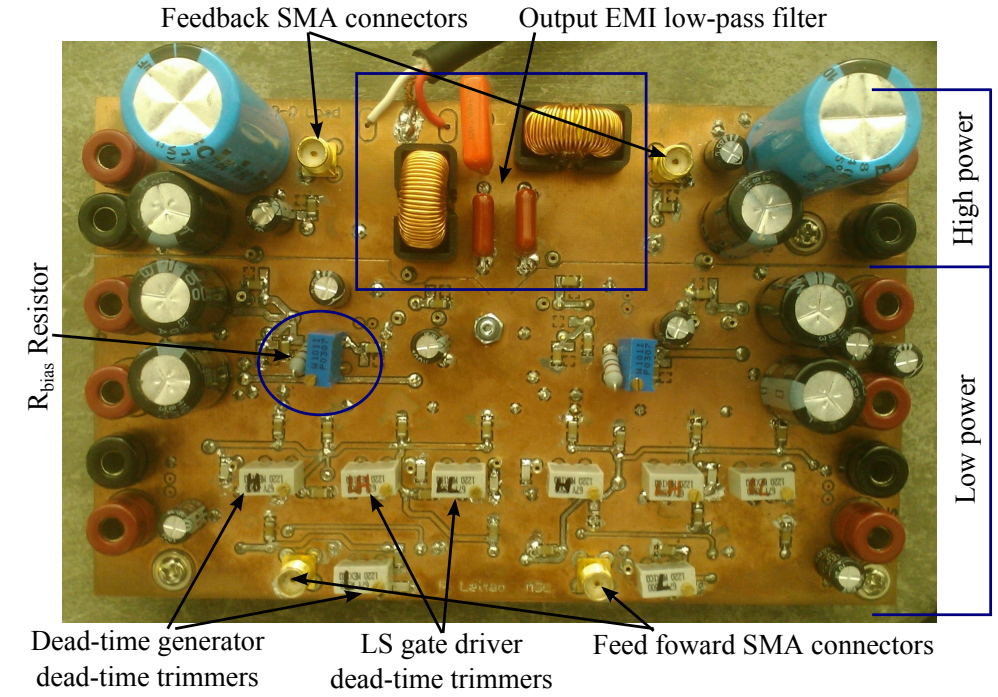
The half-bridges are divided in a low power section, where the dead-time generator circuitry and the gate drivers are located, and a high power section, where the power output MOSFETs and the EMI low-pass filter are located. In order to prevent ground loops, the ground plane is partially split. Each dead-time generator circuitry, gate driver and power MOSFETS has separate power supplies plugs that are also decoupled. Nonetheless, the

power MOSFETS of each half-bridge have to share the same power supply.

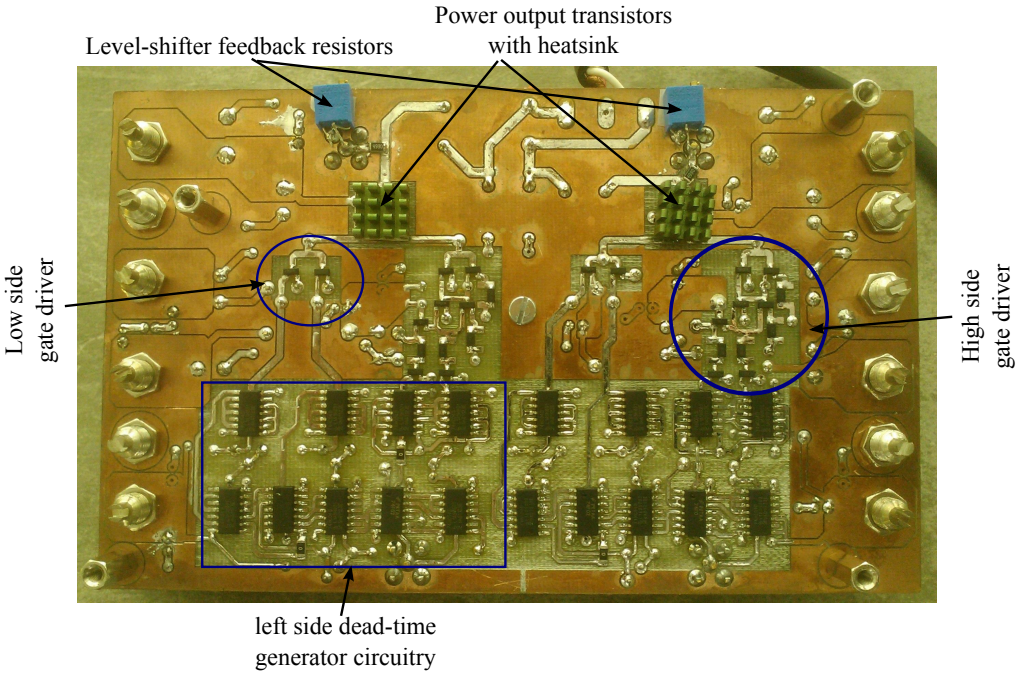
The dead-time generator circuitry allows the user to manually set the necessary dead-time in the low side gate driver and in the half-brigde, through the use of eight trimmers.

As a precaution, due to the high currents that flow through the power output stage PCB, the layout option of placing the ground plane on the top layer was made. This way, the paths that have high currents and voltages, such as in the high power section of the PCB, are unreachable to the user.

In order to insert the power output stage inside the feedback loop, it is necessary to convert the 20 V output signal to the modulator's V_{CC}, which is 5 V. This can be done through a voltage divider using two resistors.



(a) Top layer (ground plane)



(b) Bottom layer

Figure 5.5: Power output stage PCB

5.2.3 Bill of Materials

The Table 5.1 and the Table 5.2 shows the bill of materials of the Class D ΔΣM and the proposed power output stage, for 1k units. The price is shown for 1k orders and it is taken from the Portuguese Farnell distributor[1].

Number #	Manufactor part	Manufactor	Quantity	Price (1k) (€)	Comment
1	LT1994	Linear Technologies	6	2.050	Opamp: 5 for loop filter + 1 for level shifting
2	LT1720	Linear Technologies	1	3.210	Comparator
3	CD74AC175M	Texas Instruments	1	0.500	FF-D
4	SMD 1206 Res.	-	34	0.002	1206 SMD resistors (1% tol.)
5	Trimmers	Vishay Sfernice	4	0.530	500-Ω 22 turns trimmer
6	1nF SMD Cap.	-	10	0.029	1206 SMD capacitor (5% tol.)
7	100nF SMD Cap.	-	21	0.017	1206 SMD capacitor (10% tol.)
8	10uF Elect. Cap.	Multicomp	2	0.014	10uF Elect. Cap. 50 V ratings
9	100uF Elect. Cap.	Multicomp	2	0.028	100uF Elect. Cap. 50 V ratings
10	5-1814832-1	TE Connectivity	5	1.430	SMA PCB female connector
11	-	-	1	5.000	(Avg.) Standard PCB board
		Total 1 unit (€)		31.079	

Table 5.1: Class D ΔΣM bill of materials for 1k complete units

[1]Portuguese Farnell distributor website: http://pt.farnell.com/

Number #	Manufactor part	Manufactor	Quantity	Price (1k) (€)	Comment
1	IRF7389	International Rectifier	2	0.600	Power output MOSFETs
2	PE-5404NL	Pulse	2	1.430	24 kHz inductor filter
3	1.2 uF Cap	Panasonic	2	0.640	24 kHz film capacitor filter
4	NSS40201LT1G	On-semi.	2	0.440	HS gate driver NPN trans.
5	BZX84C15LT1G	On-semi.	8	0.038	HS gate driver 15V zener diode
6	IRLML2803	International Rectifier	10	0.134	HS and LS gate driver NMOS
7	NTR4502PT1G	On-semi.	6	0.098	HD and LS gate driver PMOS
8	Trimmers	Vishay Sfernice	12	0.530	500-Ω 22 turns trimmer (RC delay cell + R_{bias} + $R_{Feedback}$)
9	1nF SMD Cap.	-	8	0.029	1206 SMD capacitor (RC delay cell) (5% tol.)
10	74HC02D	NXP	4	0.104	NOR gate for dead-time
11	74HC04D	NXP	14	0.123	NOT gate for dead-time
12	100nF SMD Cap.	-	30	0.017	1206 SMD capacitor (10% tol.)
13	10uF Elect. Cap.	Multicomp	8	0.014	10uF Elect. Cap. 50 V ratings
14	100uF Elect.	Multicomp	6	0.028	100uF Elect. Cap. 50 V ratings
15	1000uF Elect. Cap.	Multicomp	2	0.420	1000uF Elect. Cap. 50 V ratings
16	5-1814832-1	TE Connectivity	4	1.430	SMA PCB female connector
17	-	-	1	5.000	(Avg.) Standard PCB board
Total 1 unit (€)				29.532	

Table 5.2: Class D proposed power output stage bill of materials for 1k complete units

5.3 Experimental Results

This subsection presents the experimental results of both ΔΣMs, with 1-bit and with 1.5-bit quantization scheme. Two sets of results are used for comparison, the ΔΣM without the power output stage inside the feedback path (just as standalone) and with the power output stage inside the feedback path (Class D audio amplifier). The waveforms are exported using a Digital Storage Oscilloscope IDS-8000 series from the ISO-TECH. The performance of the standalone ΔΣM is measured with a Digital Analyser and the Class D audio amplifier performance is measured with an Audio Precision ATS-2.

The exported waveforms from the oscilloscope are presented with a 2 kHz input signal to maintain consistency with the electrical simulations chapter and the performance of the amplifier is measured with an 1 kHz input signal, as standard.

5.3.1 Experimental testing workbench

Two experimental workbenches were used. The first, depicted in Fig. 5.6, was used to serve as preliminary testing and to export the waveforms from the oscilloscope. The use of several power sources also allowed to calculate the detailed power efficiency of the full system.

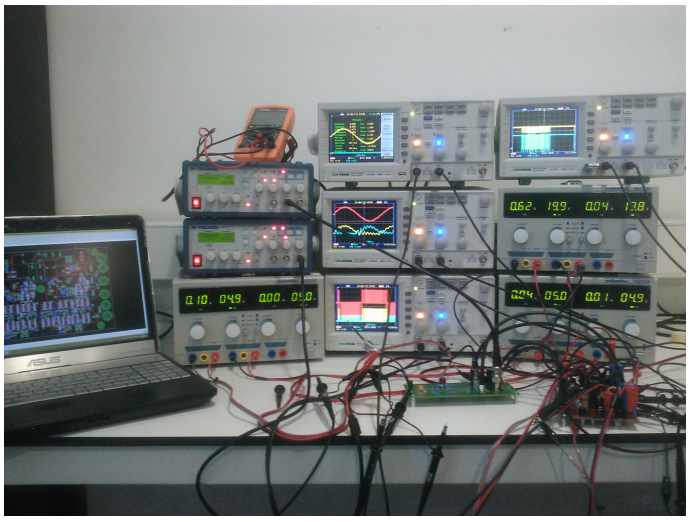


Figure 5.6: Preliminary testing workbench setup

The experimental workbench in Fig. 5.7 allowed to test the performance of the circuits with the Audio Precision and the digital analyser. An high-end digital clock generator is

also used.

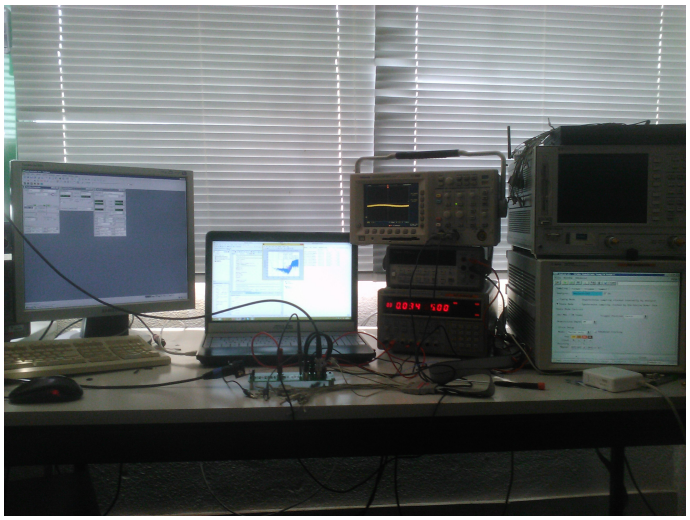


Figure 5.7: High end testing workbench setup

5.3.2 1.5-bit 5^{th} order $\Delta\Sigma$ Modulator @ 1.60 MHz

The Fig. 5.8 depicts a single-ended input, V_{in}, as yellow, with 2.80 V peak-to-peak, and the V^+ node voltage, with the power output stage inside the feedback path. By monitoring this node and the bitstream presented in the Fig. 5.9, it is possible to see that the $\Delta\Sigma$M is working correctly, as this output waveforms are identical to the simulated ones, presented in Fig. 4.13. The output voltage, V_{out}, depicted in the Fig. 5.10, has 29.4 V peak-to-peak which translates into 13.5 W power to the load. Due to the 1.5-bit quantization scheme, only one half-bridge will be delivering power to the load at each half sinusoidal period, which is why the V^+_{out}, as yellow, and V^-_{out}, as blue, waveforms have the presented behaviour (refer to Fig. 5.10).

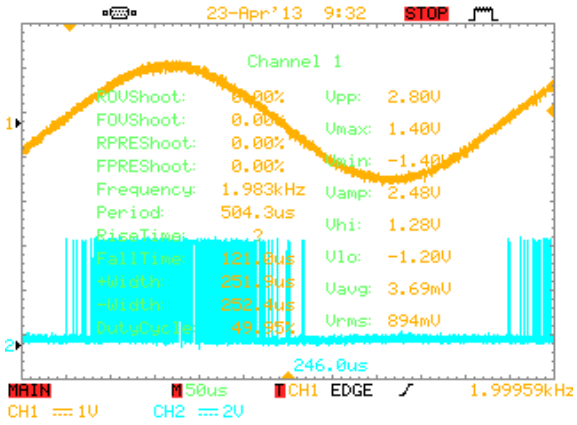


Figure 5.8: Single-ended input, V_{in}, with 2.8 Vpp as yellow and V^+ node, as blue

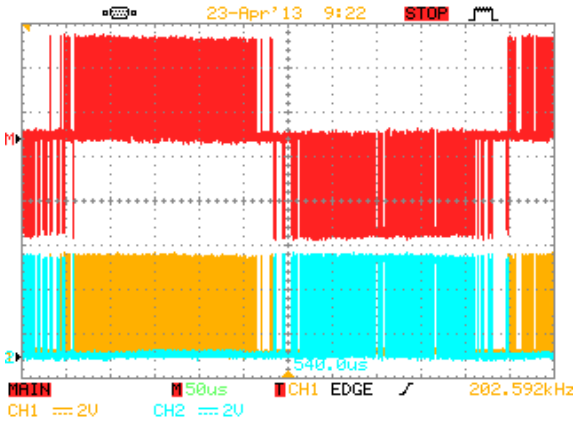


Figure 5.9: V^+ node as blue, V^- node as yellow and the bitstream as red

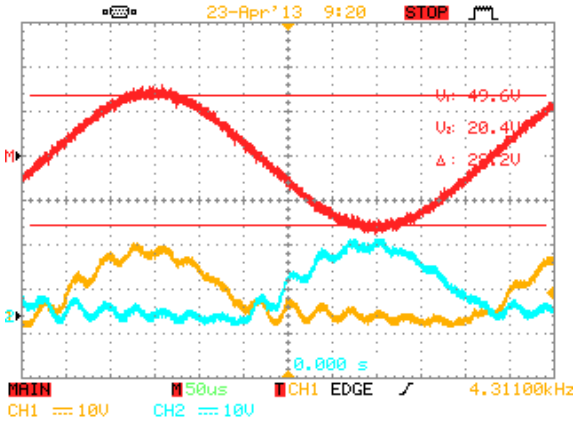


Figure 5.10: V_{out} voltage (red) with 29.4 V peak-to-peak; V^+_{out} as yellow and V^-_{out} as blue

The Fig. 5.11 shows the FFT of the standalone ΔΣM without the power output stage inside the feedback path with an input voltage of 0 dBV. It is possible to see that there is a displacement of the zeros of the loop filter, which will degrade the performance of

the ΔΣM. This is mainly due to the fact that there is a mismatch in the feedback, as the 0-state of the modulator is being performed as the 0^{-}-state in order to optimize the power efficiency of the power output stage. By inserting the power output stage inside the feedback path the FFT of the V_{out} signal can be measured in the Audio Precision, which is presented in Fig. 5.12 with a sinusoidal input of 0 dBV (full power), -6 dBV (half power) and -12 dBV (quarter power). Fig. 5.13 shows a comparison of the SNDR versus the input voltage between the standalone ΔΣM and the Class D audio amplifier and the Fig. 5.14 shows the THD+N versus the input frequency of the Class D audio amplifier considering 1/4 and 1/8 of the full power.

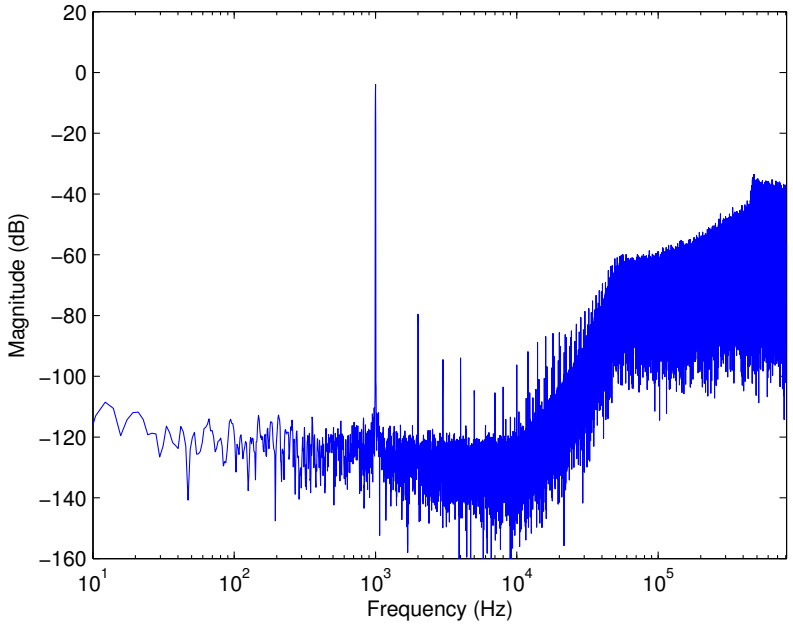


Figure 5.11: FFT of the standalone 1.5-bit ΔΣM with an input of 0 dBV

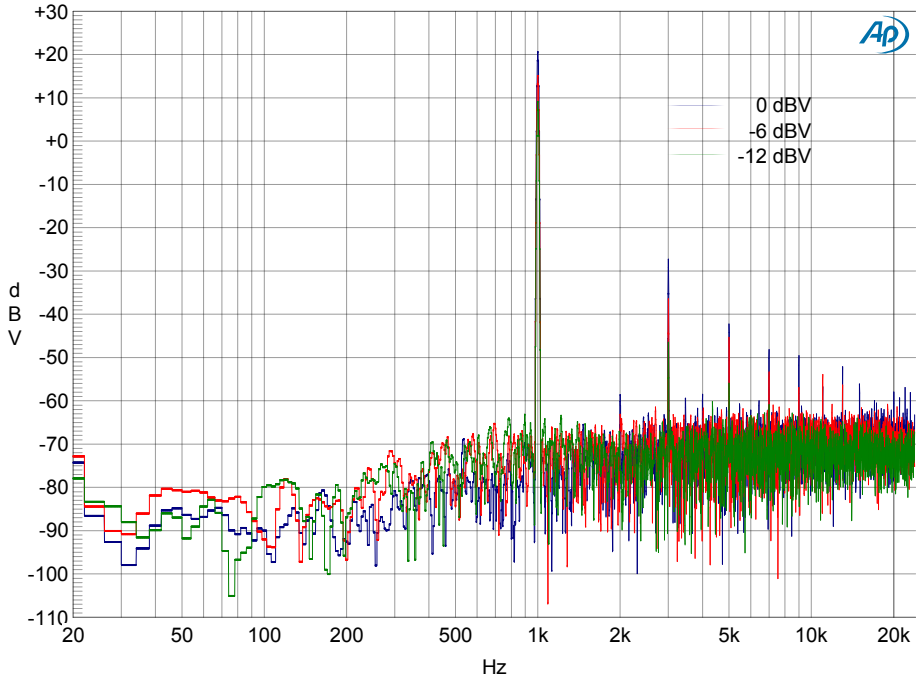


Figure 5.12: Audio Precision exported FFT with an input of 0 dBV (full power), -6 dBV (half power) and -12 dBV (quarter power) input (8192 points) of the 1.5-bit Class D audio amplifier

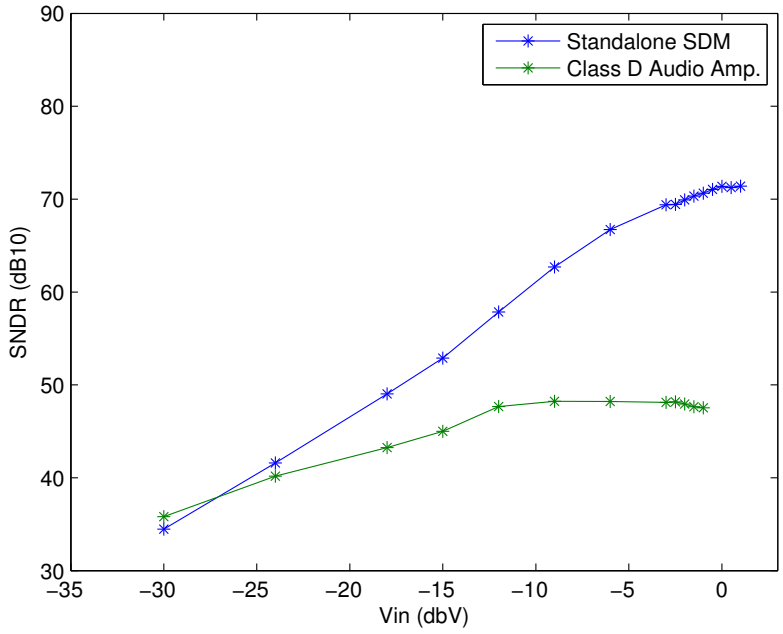


Figure 5.13: SNDR versus the input voltage (dBV) of the standalone 1.5-bit $\Delta\Sigma$M and the Class D audio power amplifier

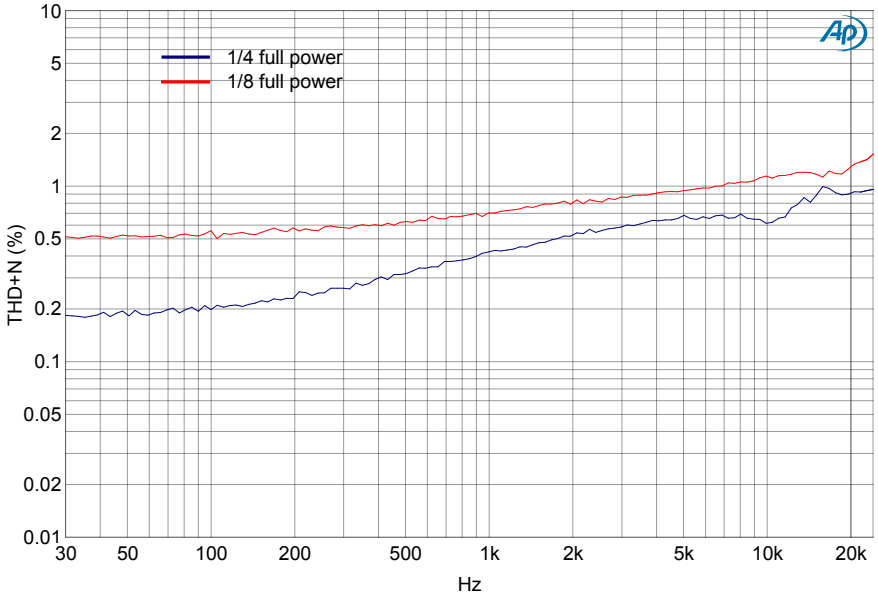


Figure 5.14: THD+N versus the input frequency of the 1.5-bit Class D audio amplifier

5.3.3 1-bit 5^{th} order $\Delta\Sigma$ Modulator @ 1.60 MHz

The Fig. 5.15 depicts a 2.8 V peak-to-peak single-ended input, as yellow, and a single-ended 1-bit digital representation of this signal, as blue. These waveforms are consisted with the ones from the electrical simulation which are presented in Fig. 4.34. The fully-differential bitstream of the input signal is presented in Fig. 5.16 and the Fig. 5.17 depicts the output voltage of the Class D audio amplifier, which is 24.8 V peak-to-peak and is delivering 9.61 W to the 8-Ohm load. Due to the 1-bit nature of the Class D audio amplifier, the depicted voltage nodes V_{out}^{+} and V_{out}^{-} will behave as two 180º out of phase representations of the input signal. The Fig. 5.18 depicts the FFT of the standalone 1-bit $\Delta\Sigma$M with an input voltage of 0 dBV, where it is possible to see the correct placement of the loop filter's zeros. (see Fig. 4.36 for the corresponding electrical simulation). The FFT of the Class D audio amplifier can be computed with the Audio Precision and is presented in Fig. 5.19, with an input voltage of 0 dBV, -6 dBV and -12 dBV. It is possible to see that the Class D audio amplifier lacks the even order harmonics, as expected in a H-bridge topology, but nonetheless its noise floor is increased, in comparison with the electrical simulation.

A SNDR versus the input voltage comparison between the standalone $\Delta\Sigma$M and the 1-bit Class D audio amplifier is presented in Fig. 5.20 and the Audio Precision graph of the THD+N versus the input frequency for 1/4 and 1/8 of the full power is also depicted in Fig. 5.21.

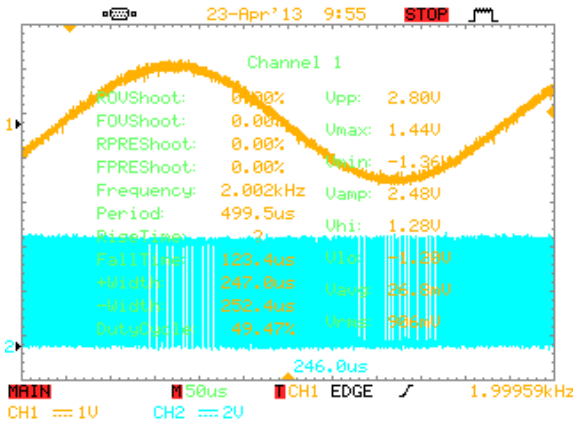


Figure 5.15: Single-ended input, V_{in}, with 2.8 V peak-to-peak as yellow and V^{+} node, as blue

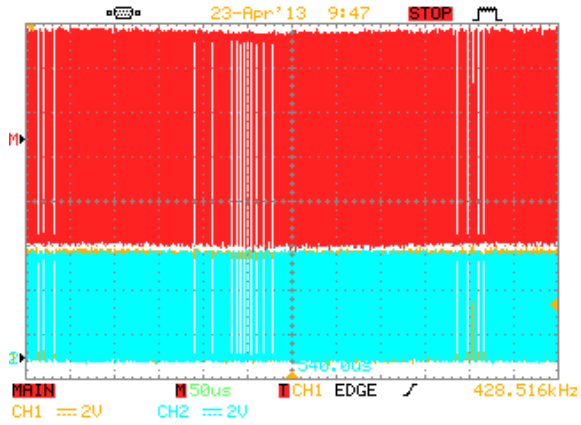


Figure 5.16: V^+ node as blue, V^- node as yellow and the bitstream as red

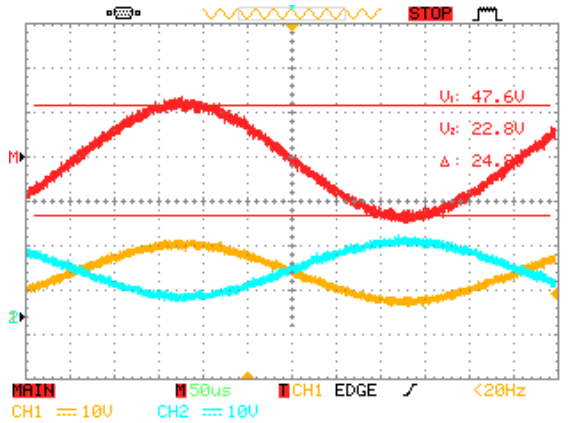


Figure 5.17: V_{out} voltage (red) with 24.8 V peak-to-peak; V^+_{out} as yellow and V^-_{out} as blue

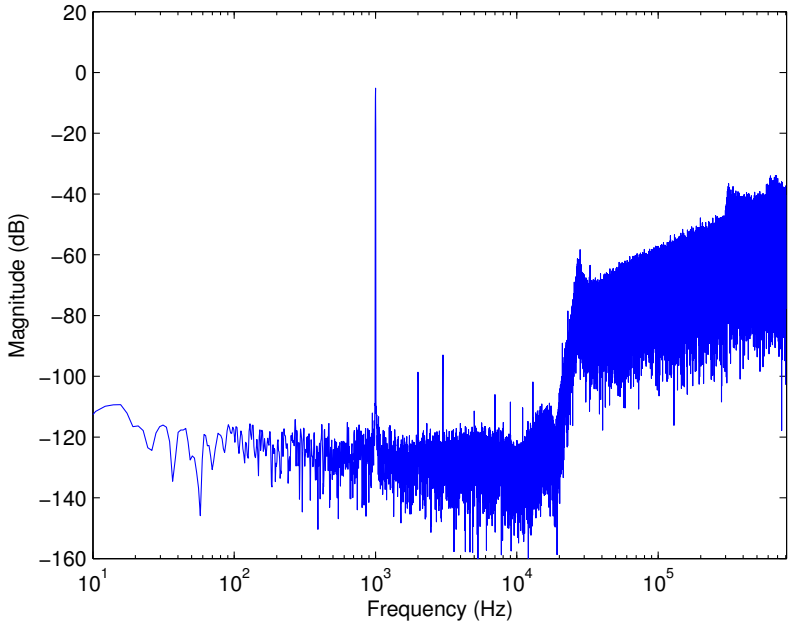


Figure 5.18: FFT of the standalone 1-bit $\Delta\Sigma$M with an input of 0 dBV

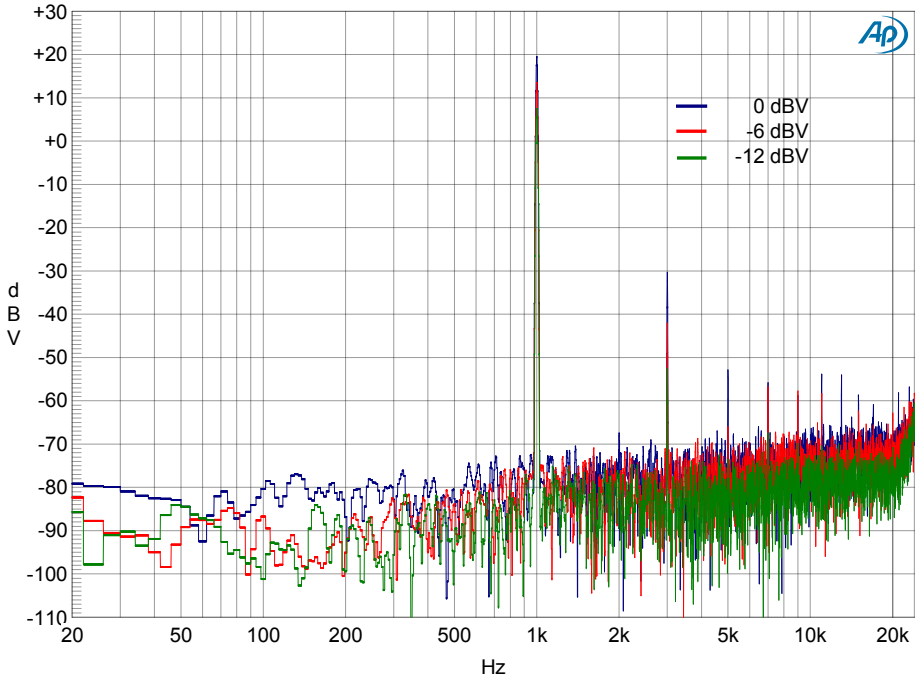


Figure 5.19: Audio Precision exported FFT with an input of 0 dBV (full power), -6 dBV (half power) and -12 dBV (quarter power) input (8192 points) of the 1-bit Class D audio amplifier

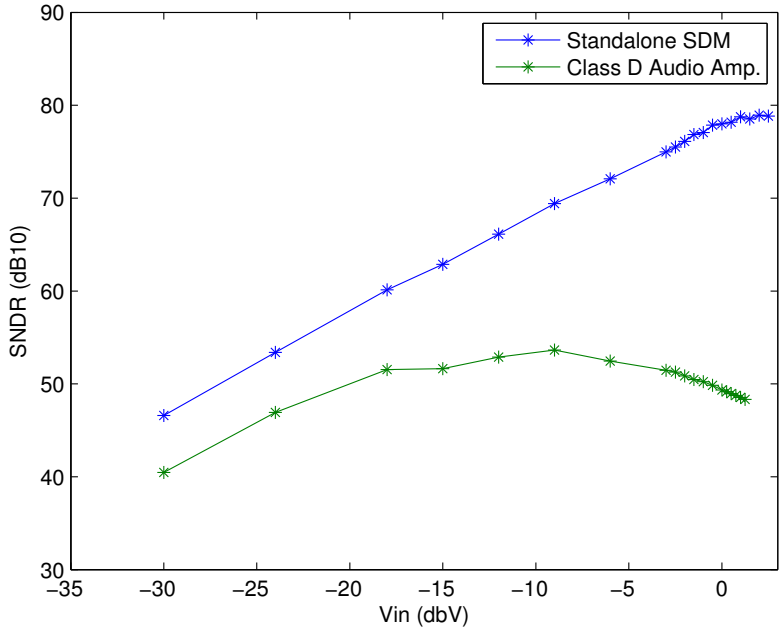


Figure 5.20: SNDR versus the input voltage (dBV) of the standalone 1-bit $\Delta\Sigma$M and the Class D audio power amplifier

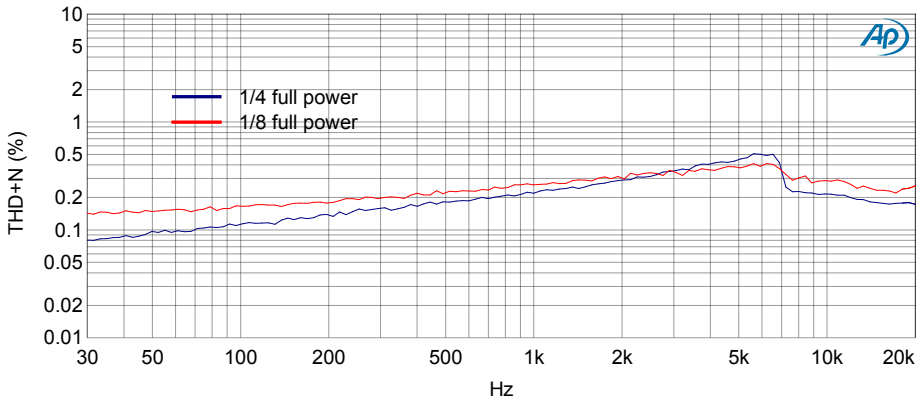


Figure 5.21: THD+N versus the input frequency of the 1-bit Class D audio amplifier

5.4 Summary

The Table 5.3[2] summarizes the experimental results of Class D Audio amplifier with 1-bit and 1.5-bit quantization scheme.

Parameter	1.5-bit QS			1-bit QS		
	Simulated	w/o OS	w/ OS	Simulated	w/o OS	w/ OS
V_{pp} (V)	29.50	-	29.2	24.88	-	24.8
SNDR (dB)	94.52	71.37	47.52	79.57	77.99	49.34
THD (dB)	-96.65	-72.78	-48.08	-84.48	-81.42	-49.65
HD_2 (dB)	-118.59	-75.60	-75.77	-108.42	-93.31	-86.31
HD_3 (dB)	-97.01	-90.61	-48.39	-88.33	-87.83	-49.77
HD_4 (dB)	-121.16	-90.07	-79.56	-107.54	-114.66	-90.36
HD_5 (dB)	-120.44	-100.49	-62.43	-111.91	-105.80	-73.00
$P_{\Sigma\Delta M}$ (mW)	470.89	465	465	443.85	470	470
$P_{LS\ GD}$ (mW)	30.17	-	50	49.38	-	100
$P_{HS\ GD}$ (W)	0.60	-	0.80	1.21	-	1.60
$P_{dead\ time}$ (mW)	n/a	-	200	n/a	-	200
$P_{Out.\ Bra.}$ (W)	0.66	-	0.68	0.94	-	0.99
$P_{Dissipated}$ (W)	1.77	-	2.20	2.65	-	3.36
P_{Load} (W)	13.59	-	13.32	9.68	-	9.61
P_{Total} (W)	15.37	-	15.52	12.33	-	12.97
Eff. (%)	88.46	-	85.8	78.54	-	74.1

Table 5.3: Experimental performance summary

Concerning the 1.5-bit quantization scheme and the ΔΣM as a standalone device, there is approximately -20 dB of difference in the SNDR between the electrical simulation and the experimental result. This can be explained due to the fact that the simulated result had no mismatches in the feedback, while the prototyped standalone ΔΣM performed the 0-state as 0^-. This mismatch in the feedback will increase the noise floor and create harmonic distortion because the modulator will try to correct errors that do not exist. By introducing the power output stage inside the feedback path these mismatches will amplify, and the

[2]Quantization scheme (QS); without power output stage (w/o OS); with power output stage (w/ OS)

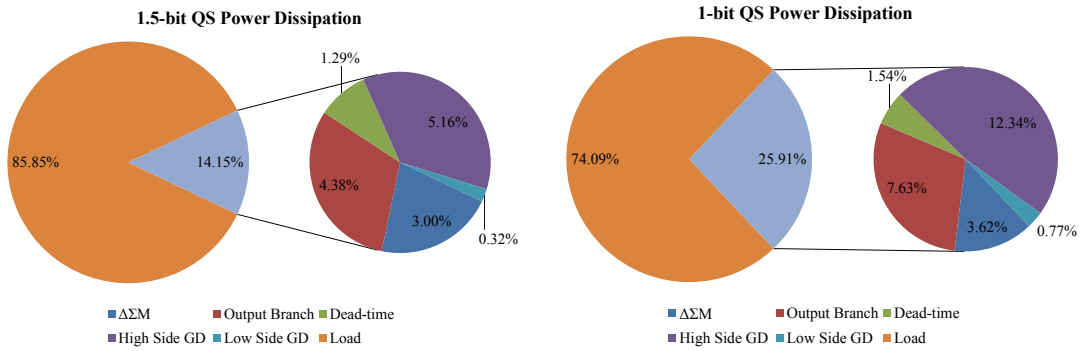
noise floor will increase (THD increase), degrading the Class D audio amplifier performance by almost 20 dB in the SNDR. Although this situation was electrically simulated, due to the simplified spice models and zero noise in the simulations, these problems do not occur.

When the ΔΣM is used as a standalone device with 1-bit quantization scheme it can achieve the electrically simulated performance, differing by only 1.6 dB in the SNDR, because the feedback is being performed correctly and has no mismatches. Inserting the power output stage inside the feedback path will decrease significantly the performance of the Class D audio amplifier, due to mainly the excessive switching noise of the power output stage that cannot be corrected by the modulator.

The THD+N versus the input frequency for both quantization schemes are correlated with the FFT measured by the Audio Precision (e.g., Fig. 5.19 and Fig. 5.21 for the 1-bit quantization scheme), as the noise floor of the FFT starts to increase with the increase of the input frequency. The same thing occurs for the THD+N graph.

The experimental power efficiency for 1.5-bit quantization scheme Class D audio amplifier is of 85.8%, presenting a 3% relative error from the simulated result, which does not take into account the power dissipation made by the dead-time circuitry. For the 1-bit quantization scheme, the experimental power efficiency is of 74.1%, which has a relative error of 5.6% from the simulated result.

A pie-chart of the experimental power consumption of the prototyped 1-bit and 1.5-bit Class D audio power amplifiers are presented in Fig. 5.22.



(a) 1.5-bit QS power comsuption

(b) 1-bit QS power comsuption

Figure 5.22: Pie-chart experimental power consumption analysis 1-bit and 1.5-bit Class D audio amplifier

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The objective of the work presented in this thesis was to develop a Class D audio power amplifier with a simple power output stage while using an optimized CT 5^{th} order $\Delta\Sigma$M at 1.60 MHz switching frequency. From this objective two prototypes were developed, one using 1-bit and another using 1.5-bit quantization scheme. Both shared the proposed power output stage, which is capable of driving an 8-Ohm load with a 20 V power supply. In order to implement the prototypes several activities and studies were performed, which are summarized in the following paragraphs.

In the second chapter, the Class D audio amplifiers are introduced and the major causes of distortion of the power output stage are described. By placing the power output stage inside the modulator's feedback path most of this distortion in attenuated, but a problem rises when the 1.5-bit quantization scheme is used, which is the mismatch in the feedback. Dynamic element matching and charge sharing are described in order to correct this problem, but due to the high voltage supply only the dynamic element matching, which has the disadvantage of doubling the average number of switching of the power output stage, is considered.

In the third chapter, the proposed power output stage is presented, which has the capability of being scaled to any given power supply voltage level. A theoretical analysis describes the relative power consumption of the proposed high side gate driver in relation to the power delivered to the load, which sets the performance constrains.

In the forth chapter, which describes the electrical simulations, a sizing for the power output stage and the schematic for the CT 5^{th} order $\Delta\Sigma$M with 1-bit and 1.5-bit with and without dynamic element matching is provided. The electrical components are selected, such as the fully-differential opamps, where the LTC6362 and LT1994 opamps stands-out. The first opamp, which has a poorer performance, also has a lower power dissipation than the LT1994 opamp. The electrical simulations, summarized in Table 4.15, show that when the power output stage is inserted in the modulator's feedback path, the highest power efficiency is of 90.69% with a SNDR of 91.90 dB when the LTC6362 opamps is used, assuming an 1.5-bit quantization scheme without dynamic element matching. Introducing the dynamic element matching, no significant increase occurs regarding the SNDR and THD performance of the Class D audio amplifier, except for a decrease in the power efficiency of approx. 6% regarding the best power efficiency measure. Using the LT1994 opamp the power efficiency decreases to 88.46% but the SNDR increases to 94.52 dB, also with 1.5-bit without dynamic element matching. The 1-bit Class D audio amplifier maximum power efficiency is of 81.08% and the electrical simulation achieves the theoretical SNDR value of 79.70 dB. Regarding the 1.5-bit electrical simulation results, the dynamic element matching technique can be disregarded.

The fifth chapter presents the experimental results of the two prototyped Class D audio power amplifiers, with 1-bit and with 1.5-bit quantization scheme, whose measured performance is summarized in Table 5.3. Both prototypes were measured using the $\Delta\Sigma$M modulator as a standalone device (no power output stage inside the feedback path), which enable to see the maximum available performance with a digital analyser, and with the power output stage inside the feedback path, whose experimental results were measured using the Audio Precision. During this stage, although the LTC6362 opamp provided a better power efficiency, during the prototyping they started failing and malfunctioning without any apparent reason. Thus, in order to have a more reliable opamp, the LT1994 opamps were used for the prototyping.

Regarding the 1.5-bit quantization scheme, the $\Delta\Sigma$M as a standalone device has approximately -20 dB of difference from the simulated performance. This can be explained by the fact that the feedback is not being performed correctly; during the 0-state, the

feedback is providing 0^--state to the modulator, forcing the modulator to correct errors that do not exist. By introducing the power output stage inside the feedback path, the SNDR decreases to 47.52 dB. Nonetheless, the power efficiency is of 85.8%, which presents a relative error of 3% from the electrical simulation.

The prototyped 1-bit $\Delta\Sigma$M as a standalone device achieved a SNDR of 77.99 dB, -1.58 dB from the simulated result. This can be explained by the fact that the feedback is being performed correctly. Even tough the $\Delta\Sigma$M as a standalone device achieved the simulated performance, when including the power output stage inside the feedback path the SNDR performance decreases to 49.34 dB. The experimental power efficiency is of 74.1%, minus 5.6% of the simulated power efficiency.

The fact that introducing the power output stage inside the feedback path of the modulator will decrease the expected SNDR, specially in the 1-bit quantization scheme, where the simulated performance is achieved while using the $\Delta\Sigma$M as a standalone device, can be due to fact that the switching noise of the power output stage is too much for the modulator to handle. As this is an high frequency feedback, every ringing transient from the power output stage is being fed back, which will eventually decrease its performance (note that the feedback of the standalone $\Delta\Sigma$M is made directly from the FF-D, which have near zero ringing transients).

6.2 Future Work

Given the light of the work developed throughout this thesis, a new investigation topic emerged from the obtained results and, more specially, from the encountered problems. The proposed future work for this thesis concerns the 1.5-bit feedback problem.

As the power output stage is inserted inside the feedback, the signal that is being fed back is an amplified high-frequency representation of the desired output signal, and every ringing transient is begin fed back into the modulator along with the desired low-frequency output signal.

The proposed, as future work, feedback architecture for the Class D audio power amplifier is presented in Fig. 6.1.

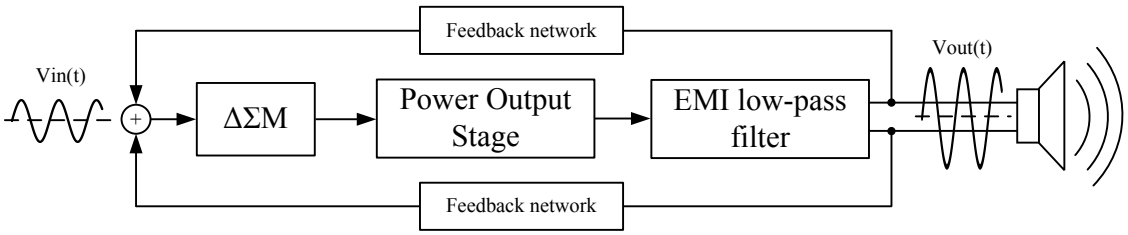


Figure 6.1: Future work proposed 1.5-bit feedback architecture

Considering the ΔΣM as a closed block, it is possible to achieve an 1.5-bit quantization scheme without any mismatch in the ΔΣM feedback. With the ΔΣM working correctly, the power output stage is only used to amplify the digital signal. Taking advantage of the low-frequency output signal, a low-frequency feedback can be perform which will both correct the ΔΣM and the power output stage errors.

Appendix

Appendix A

H-Bridge Output EMI Low-pass Filter Deduction

Fig. A.1 presents the H-bridge output EMI low-pass filter schematic.

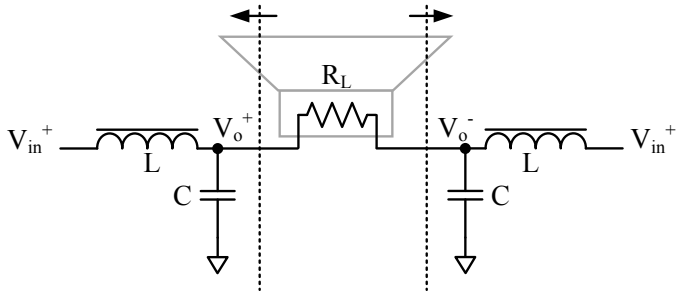


Figure A.1: H-bridge output EMI low-pass filter

Considering a balanced filter, it is possible to calculate the Thévenin equivalent, presented in Fig. A.2, as

$$V_{th^+} = \frac{1}{1 + s^2 \cdot L \cdot C} \cdot V_{in}^+ \tag{A.1}$$

$$V_{th^-} = \frac{1}{1 + s^2 \cdot L \cdot C} \cdot V_{in}^- \tag{A.2}$$

where the equivalent impedance is given by

$$Z_{th} = sL || \frac{1}{sC} = \frac{sL}{s^2 LC + 1} \tag{A.3}$$

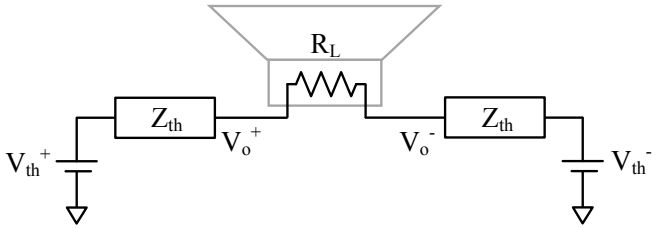


Figure A.2: H-bridge output EMI low-pass filter Thévenin equivalent circuit

Applying the Kirchoff's Current Law (KCL) to the Thévenin equivalent it is possible to draw the equation that describes the circuit, which is given by

$$\frac{V_o^+ - V_o^-}{R_L} = \frac{V_{th}^+ - V_o^+}{Z_{th}} = \frac{V_o^- - V_{th}^+}{Z_{th}} \tag{A.4}$$

Rearranging Eq. A.1, A.2 A.3 and A.4, the H-bridge filter's transfer function can be described as

$$H(s) = \frac{v_o^+(s) - v_o^-(s)}{v_{in}^+(s) - v_{in}^-(s)} = \frac{\frac{1}{LC}}{s^2 + s\frac{2}{R_L C} + \frac{1}{LC}} \tag{A.5}$$

By adding an external C_E capacitor, the load can be described as $R_L' = \frac{1}{sC_E} || R_L$ and the filter's transfer function, using the Eq. A.5, is

$$H(s) = \frac{v_o^+(s) - v_o^-(s)}{v^+(s) - v^-(s)} = \frac{\frac{1}{L(C+2C_E)}}{s^2 + s\frac{2}{R_L(C+2C_E)} + \frac{1}{L(C+2C_E)}} \tag{A.6}$$

Appendix B

Prototype Histogram

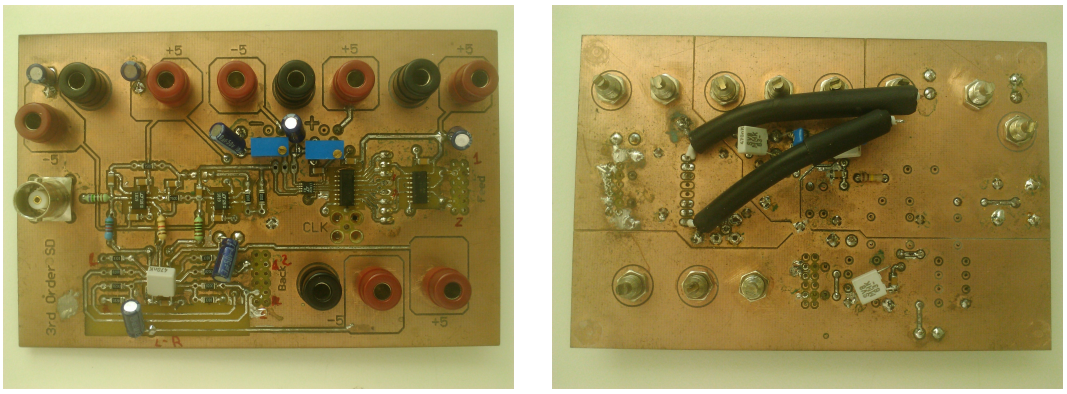
This appendix is a histogram of the implemented prototypes during the course of this thesis. It is divided into two subsections: the first presents the ΔΣM prototypes histogram and the second subsection the power output stage histogram.

B.1 ΔΣM prototypes histogram

The first prototyped ΔΣM is a single-ended 1.5-bit ΔΣM-3 at 1.28 MHz switching frequency which uses the LT1819 opamp in the loop filter and is presented in Fig. B.1. The goal was to prove the concept and to prove that the designed ΔΣM actually work. Nonetheless, due to its type of architecture, the noise floor was excessively high and it could not achieve the theoretical performance. This created the need to design a fully-differential version of the ΔΣM, depicted in Fig. B.2, which uses the LTC6362 opamp in the loop-filter. However, due to a design error, the feedback is not performed correctly. It shares the same problem as the designed Class D audio amplifier in this thesis, as it performs the 0-state as 0^--state. A corrected version is presented in Fig. B.3, which proved to achieve the theoretical performance. Proven the design, an 1-bit ΔΣM-3 using the LTC6362 was also prototyped, depicted in Fig. B.4, which also achieves the theoretical performance. Proven the ΔΣM design, either for 1-bit and 1.5-bit quantization scheme, the first Class D ΔΣM was prototyped, which uses the LTC6362 opamps in the loop filter and has the dynamic element matching implemented (not populated), presented in Fig. B.5. During the preliminary tests, the use of the dynamic element matching proved

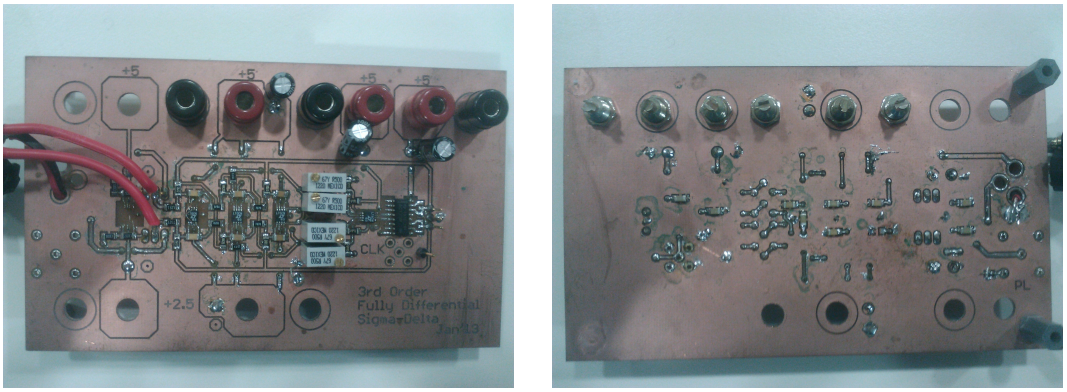
to increase the delay which would make the ΔΣM to saturate prematurely.

The Fig. B.6 presents the generic up to 7^{th} order ΔΣM, which has the capability to work as a standalone ΔΣM or as a Class D ΔΣM, with the power output stage inside the feedback loop. This prototype is discussed in subsection 5.2.1.



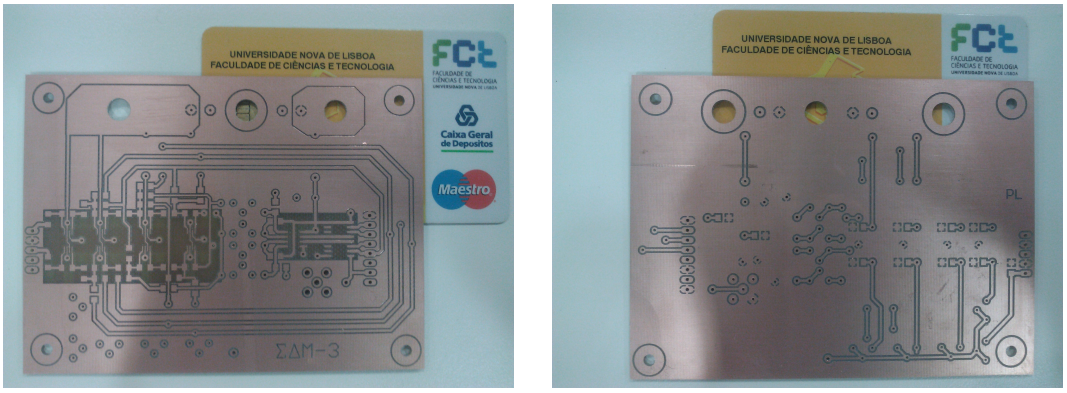
(a) Top layer (b) Bottom layer (ground plane)

Figure B.1: CT single-ended 1.5-bit ΔΣM-3



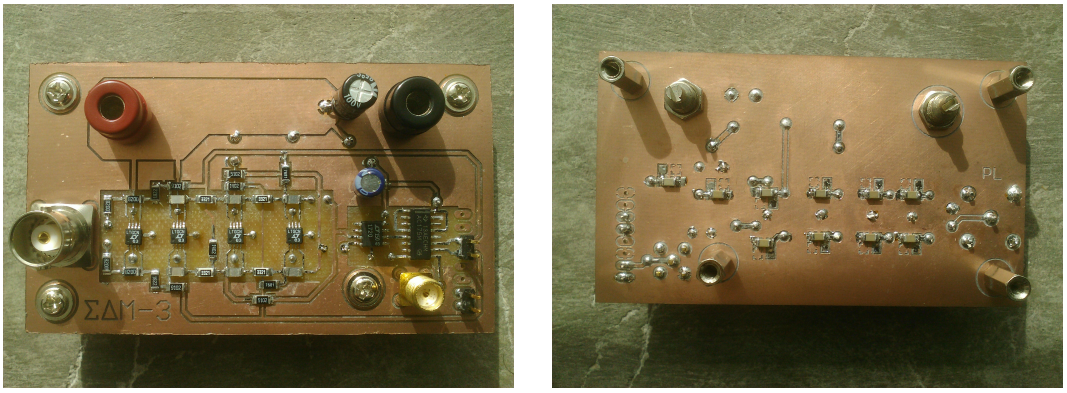
(a) Top layer (b) Bottom layer (ground plane)

Figure B.2: CT fully-differential 1.5-bit ΔΣM-3 @ 1.28 MHz with severe feedback mismatch prototype



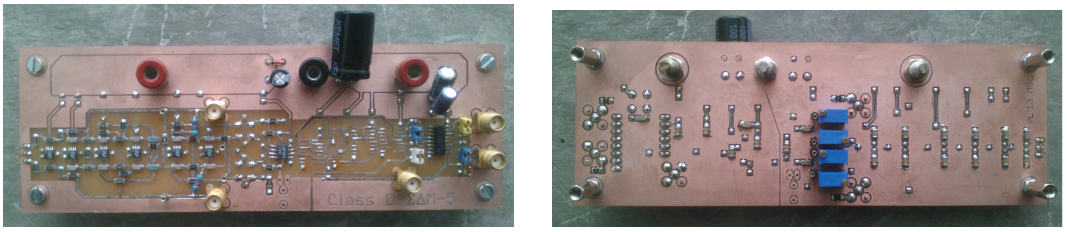
(a) Top layer (b) Bottom layer (ground plane)

Figure B.3: Unpopulated CT fully-differential 1.5-bit ΔΣM-3 @ 1.28 MHz prototype



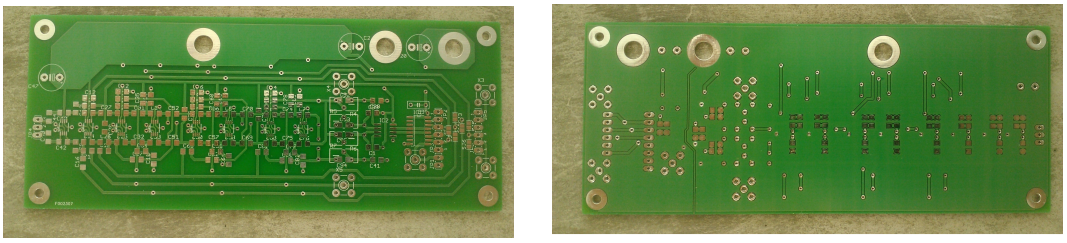
(a) Top layer (b) Bottom layer (ground plane)

Figure B.4: CT fully-differential 1-bit ΔΣM-3 @ 1.0 MHz prototype



(a) Top layer (b) Bottom layer (ground plane)

Figure B.5: Class D CT fully-differential 1.5-bit ΔΣM-5 with unpopulated dynamic element matching prototype



(a) Top layer

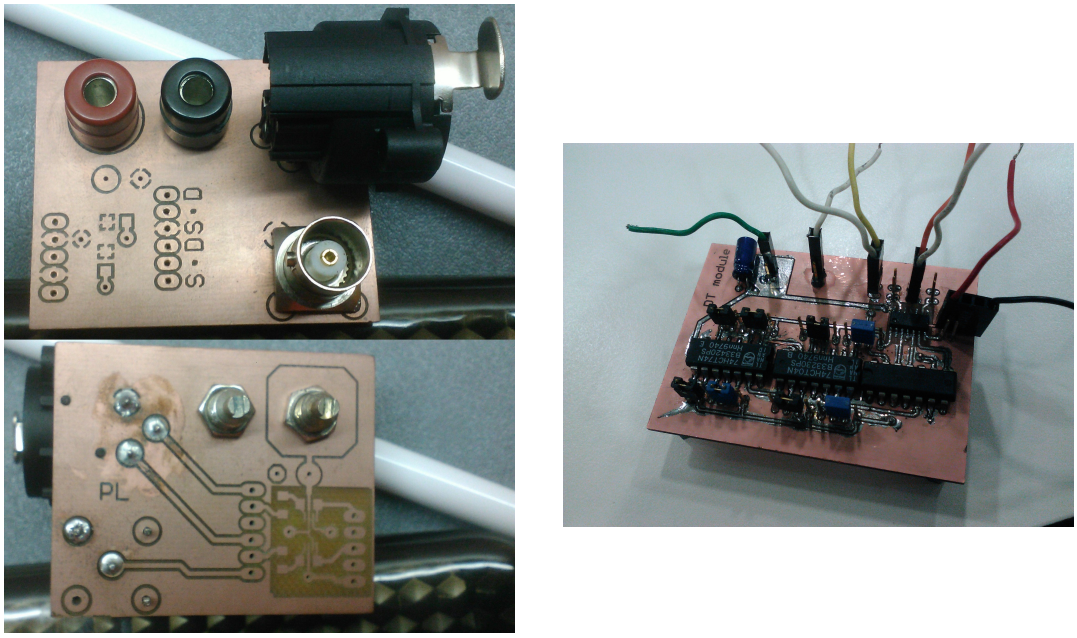
(b) Bottom layer (ground plane)

Figure B.6: Generic CT fully-differential ΔΣM prototype board capable of 1-bit and 1.5-bit quantization scheme and up to 7^{th} order

B.2 Power output stage prototypes histogram

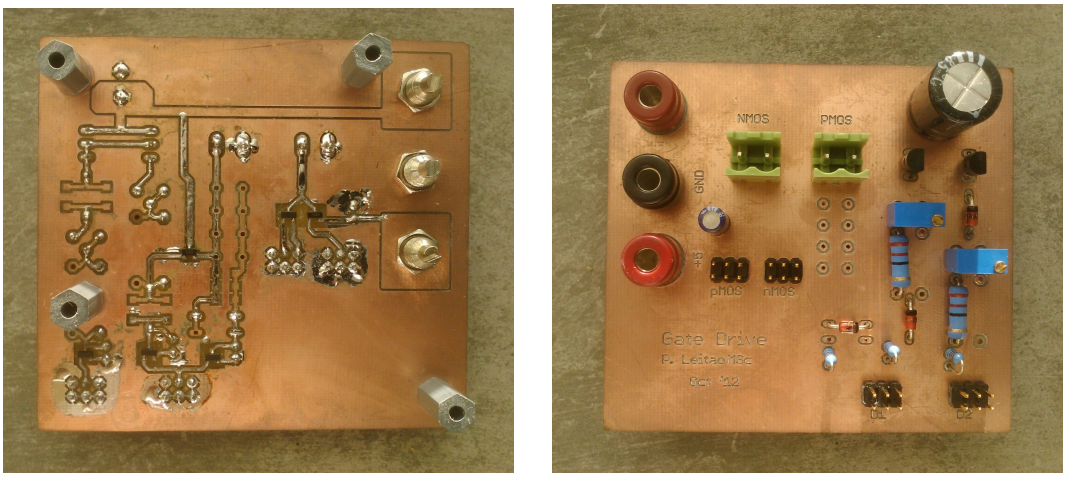
In order to check design flaws, an half-bridge of the proposed power output stage was prototyped. The Fig. B.7(a) shows a XLR or SMA to pin converter, with an embedded level-shifter and the Fig. B.7(b) shows a dead-time module (which can be easily incremented) where the delay-cells are implemented using 74x04 inverters. Two prototyped high-side and low-side gate drivers versions are depicted in Fig. B.8 and Fig. B.9. The first version replaces the R_{Bias} resistor with a current mirror in an attempt to reduce the power dissipation. Nonetheless, it increased the delay and the complexity without any significant advantage in the dissipated power in comparison to the latter version, which uses the R_{Bias} resistor and uses a non-overlapping time circuitry in the low-side gate driver. Fig. B.10 presents the prototyped power MOSFET transistor with limiting resistors in the source of the PMOS and NMOS.

A simple 5-V power output stage was later prototyped for debugging purposes. As it is only 5-V, it uses two low side gate drivers as H-bridges. The prototyped 20-V power output stage is depicted in Fig. B.12 and is discussed in subsection 5.2.2.



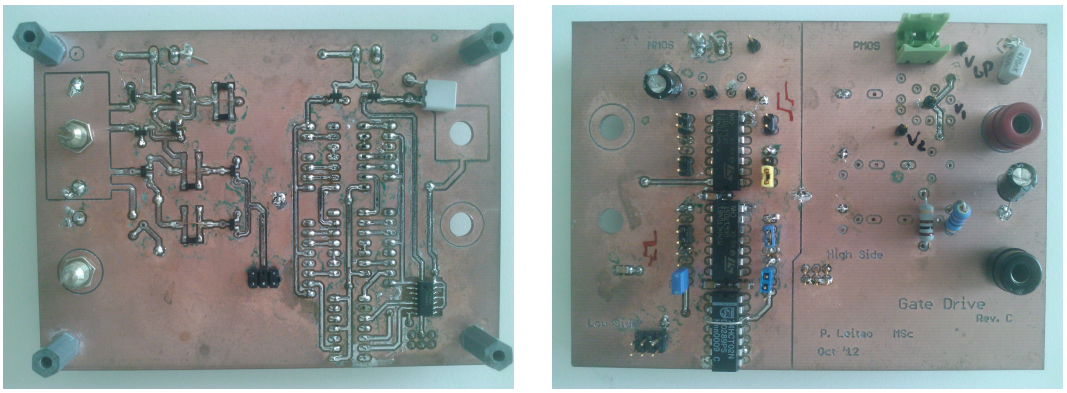
(a) SMA and XLR input and level-shifter (top) (b) Dead-time module (top)

Figure B.7: (a) SMA and XLR input and level-shifter to pin converter and (b) simple dead-time module with jumpers to define the required dead-time



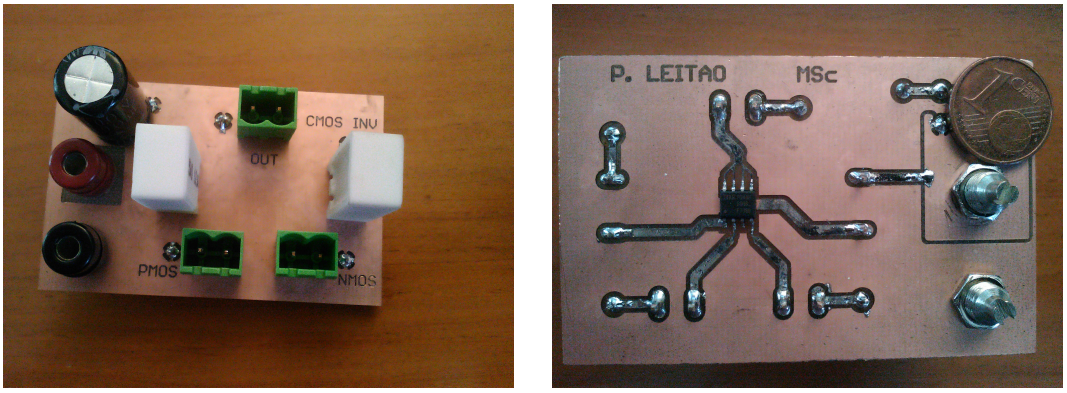
(a) Top layer (ground plane) (b) Bottom layer

Figure B.8: First prototype high-side and low-side gate driver; the R_{Bias} is replaced using a current mirror in an attempt to reduce the dissipated power



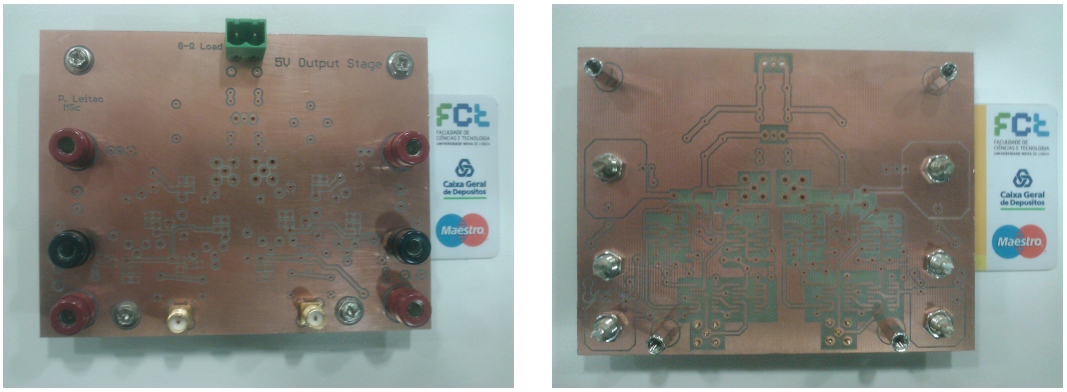
(a) Top layer (ground plane) (b) Bottom layer

Figure B.9: Second prototype high-side and low-side gate driver; the R_{Bias} is used to improve speed and the low-side gate driver has an embedded non-overlapping time circuit



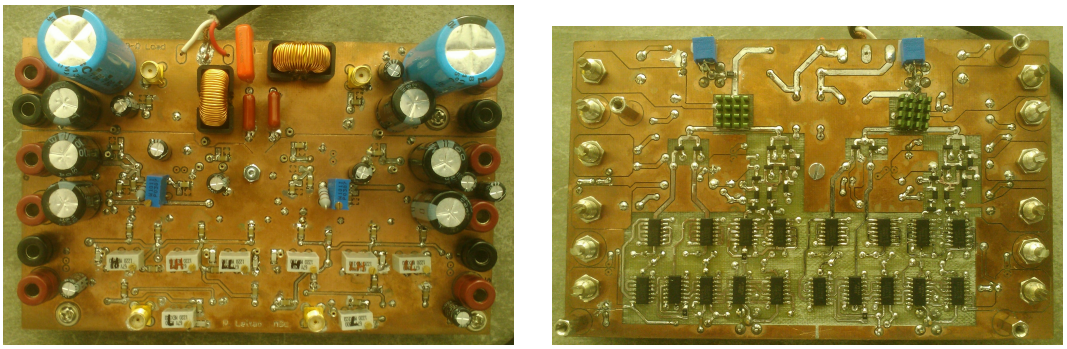
(a) Top layer (ground plane) (b) Bottom layer

Figure B.10: Prototyped power output MOSFET transistor PCB board, with a limiting resistor in the source of the PMOS and NMOS



(a) Top layer (ground plane) (b) Bottom layer

Figure B.11: Prototyped unpopulated 5-V power output stage



(a) Top layer (ground plane) (b) Bottom layer

Figure B.12: Proposed 20-V power output stage

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