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Design of a Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) Modulator for Class D Audio Power Amplifiers

Por

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À minha família, em especial, aos meus pais
João Luís e Maria Isilberta.

Agradecimentos

Ao terminar esta tese resta-me registar os momentos mais marcantes e agradecer a todas as individualidades que de várias formas contribuíram para a conclusão da mesma. Os momentos mais marcantes, em termos de decisões, foram quando deixei na ilha do Pico família e amigos para vir para Lisboa há 11 anos e, há 6 anos, ter interrompido o meu antigo e motivante trabalho para ingressar na faculdade.

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Sumário

A crescente procura por equipamentos portáteis com recursos de áudio é uma realidade. Estes equipamentos precisam de amplificadores de potência de áudio para produzir som através de pequenos alto-falantes ou auscultadores. Como estes equipamentos dependem de baterias para a sua própria alimentação, o uso de amplificadores de áudio extremamente eficientes é de relevante importância, tal como reduzir o calor gerado pelo amplificador de potência, de modo que dissipadores de calor volumosos possam ser eliminados, permitindo uma redução de tamanho aos equipamentos.

Amplificadores lineares, como os de Classe AB, embora exibam uma alta linearidade, possuem baixo rendimento, especialmente para níveis reduzidos de potência. Amplificadores de Classe D podem atingir um alto rendimento, já que os transístores de saída são utilizados como interruptores e, portanto, a dissipação de potência é idealmente zero. Um dos principais desafios no projecto de amplificadores de Classe D é a concepção do modulador, que codifica o sinal analógico de entrada em uma sequência de pulsos usados para produzir o sinal de potência da saída. O espectro da sequência de pulsos contém o sinal de áudio pretendido, bem como, as componentes indesejáveis (mas inevitáveis) de alta frequência.

Este trabalho apresenta um modulador Sigma-Delta de terceira ordem com 1,5-bit com realimentação distribuída e deslocação de zeros para amplificadores de áudio de Classe D. A fim de melhorar a relação sinal-ruído (SNDR), sem aumentar significativamente a sobre amostragem (OSR) ou a ordem do modulador (não superior a

3), o modulador usa deslocação de zeros e 1,5-bit de quantização.

Palavras Chave: Amplificador de Class D, Modulação Sigma-Delta , Áudio .

Abstract

An increasing demand for portable media devices with audio capabilities is the reality today. These devices need audio power amplifiers to produce sound trough speakers or earphones. Since these devices rely on batteries for their energy needs, the use of extremely efficient audio amplifiers is of paramount importance. It is also important to reduce the heat generated by the power amplifier itself, so that the bulky heat sink can be eliminated, thus allowing for small size portable devices.

Linear amplifiers, such as class AB, have high linearity, but have low efficiency especially for lower power levels. Class D amplifiers can achieve high efficiencies because the power devices are used as switches and therefore their power dissipation is, ideally, zero. One of the main challenges in the design of class D amplifiers is designing the modulator circuit that encodes the input analogue signal into a switching sequence used to produce the output power signal. The spectrum of the switching sequence contains the desired audio signal plus undesired (but unavoidable) high-frequency content.

This work presents a 3^{rd} order 1.5-bit $\Sigma\Delta$ modulator with distributed feedback and local resonator feedback for Class D audio amplifiers. In order to improve the signal-to-noise-and-distortion ratio (SNDR), without increasing significantly the oversampling ratio (OSR) or the order of the modulator (not greater then 3), the modulator uses transmission zeros and 1.5-bit quantization.

Keywords: Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$), Class D amplifier, Audio.

Contents

List Of Acronyms

A/D, ADC Analog-to-Digital Converter

CT Continuous Time

DR Dynamic Range

DT Discrete Time

GBW Gain-Bandwidth Product

NTF Noise Transfer Function

OSR Over-Sampling Ratio

PCB Printed Circuit Board

PSNR Peak SNR

PSRR Power Supply Rejection Ratio

PWM Pulse-Width Modulation

SDM Sigma-Delta Modulation

SNDR Signal-to-Noise and Distortion Ration

SNR Signal-to-Noise Ratio

STF Signal Transfer Function

THD Total Harmonic Distortion

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Chapter 1

Introduction

1.1 Motivation

Due to the major concerns of global sustainability, there is a growing need for energy saving. The energy efficiency of audio amplifiers can be an important contribution to this end. Furthermore, the increasing demand for portable media devices with audio capabilities is a reality. These devices need audio power amplifiers to produce sound trough small speakers or earphones. Since these devices rely on batteries for their energy needs, the use of extremely efficient audio amplifiers is of paramount importance. It is also important to reduce the heat generated by the power amplifier itself, so that the bulky heat sink can be eliminated, thus allowing for small size portable devices.

Linear amplifiers, such as class AB, have high linearity, but have low efficiency especially for lower power levels. Class D amplifiers can achieve high efficiencies because the power devices are used as switches and therefore their power dissipation is, ideally, zero [1] [2]. The efficiency advantage of the Class D amplifiers is unquestionable and, through this trait, this Class of amplifier has earned much interest.

1.2 Audio Amplifiers

1.2.1 Introduction

The most important characteristics of an amplifier are efficiency, linearity, output power, and signal gain. Typically, there is a trade-off between these characteristics. Understanding these trade-offs is an essential step in the designing process of an audio amplifier.

Power Efficiency

The power efficiency is defined as

$$\eta = \frac{P_{load}}{P_{source}} \cdot 100\% \tag{1.1}$$

where P_{load} is the average power delivered to the load and P_{source} is the average power supplied by the source. The average power is given by

$$P_{avg} = \frac{1}{T} \int_0^T p(t)dt$$

and where T is the period of the signal.

Linearity

An amplifier is linear if it preserves the details of the signal waveform, such that,

$$V_{out}(t) = G \cdot V_{in}(t)$$

where, V_{out} and V_{in} are the output and input signals respectively, and G is a constant representing the gain of the amplifier.

1.2.2 Class A

Class A amplifiers have the best linearity characteristic of all (for a theoretical point of view) but also has the lowest efficiency that ideally can not be larger than 50%. This is due to the fact that the output transistors are always ON (see Figure 1.1). To achieve high linearity and gain, the amplifier base and drain DC voltage should by chosen correctly so that the amplifier operates in the linear region, meaning that the bias current should be equal to the maximum load current. The device, since it is turn on (conducting), is constantly carrying current, which represents a continuous loss of power in the amplifier and consequently, a degradation of efficiency.

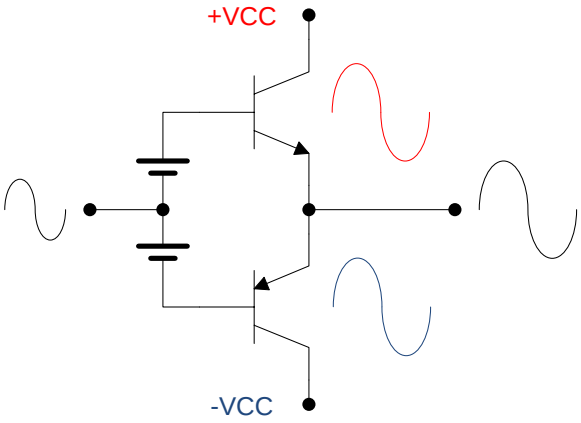


Figure 1.1: Class A Amplifier.

1.2.3 Class B

Class B (depicted in Figure 1.2) is characterized by biasing the output transistors on the edge of the cut-off region resulting in a bias current of zero. This increases the efficiency of the circuit, ideally, to 78.5%. The transistors only drive current when they are excited by the input signal.

Essentially, this Class of amplifier implements two devices in the output stage in a "push-pull" configuration, with each amplifying half of the waveform and operating in strict time alternation. This configuration provides much greater efficiency than Class A. The drawback of Class B amplifiers is that the zero-crossing point of the

wave-form can create distortion because one device must change from the ON region to the cut-off region while the other device changes form the cut-off region to the ON region. Any asymmetry in this transition leads to part of the signal to be cut.

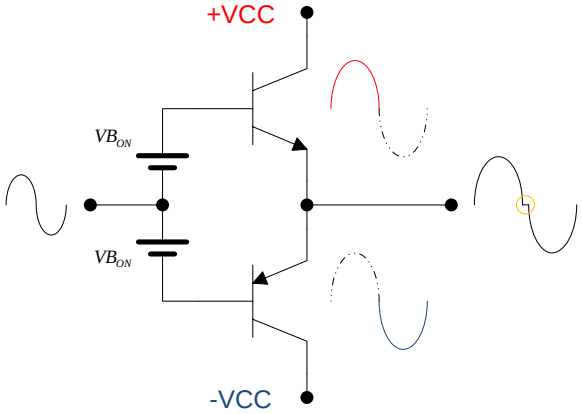


Figure 1.2: Class B Amplifier.

1.2.4 Class AB

The Class AB is an intermediate class between class A and B where, the output stage devices are biased with a DC current larger then 0, thus minimizing the crossover distortion. In this case, there is a current in the output transistors (bias current) which is smaller, when compared to the bias current of Class A, so that the efficiency is close to Class B.

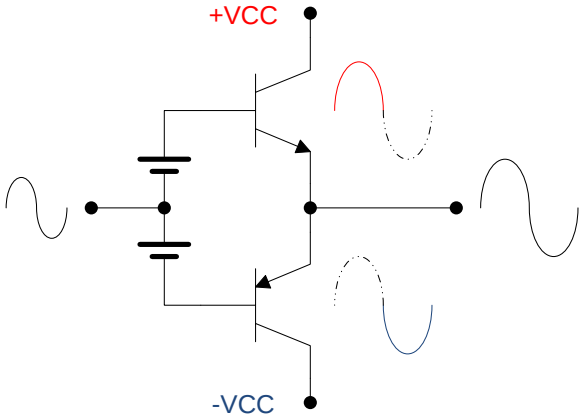


Figure 1.3: Class AB Amplifier.

Figure 1.3 shows the Class AB amplifier with two bias voltages to avoid crossover distortion. This Class is frequently used in audio amplifiers.

1.2.5 Class D

Class D amplifiers differ fundamentally from the more familiar classes of A, B, and AB. In this Class of amplifier the output devices do not operate in the linear mode. Instead the output transistors are operated as switches. When a transistor is off, the current through it is zero. When it is on, the voltage across it is very small, ideally zero. In each case, the power dissipated ($P = V \times I$) as the heat in the transistor is very low. This increases the efficiency, therefore requiring less power from the power supply and smaller heat sinks for the amplifier. The main drawback of this class of amplifier is the distortion and noise introduced into the signal by the switching operation of the power stage. A broad overview of class D amplifiers will be studied in Chapter 2.

1.3 Thesis Objectives and Contributions

The main objective of this thesis is to research and design of a Continuous-time (CT) Sigma-Delta ($\Sigma\Delta$) modulator for Class D audio power amplifiers. This work gives an important contribution of personal knowledge acquired and to the scientific community as a result of the published papers.

1.4 Thesis Structure

After a brief introduction, the remainder of the dissertation is organized as follows. Chapter 2 gives a general overview of the Class D amplifiers. Sigma-Delta modulation and several architecture options for the modulator will be studied in Chapter 3. The Chapter 4 proposes a combination of two architectures studied in Chapter

3 in order to improve the SNDR value, and also, explains the steps necessary to design the circuit implementation of the proposed $\Sigma\Delta$ modulator, and shows the electrical simulations results of the modulator circuits. Finally, Chapter 5 concludes the thesis and discusses future work.

Chapter 2

Class D Amplifiers

2.1 Introduction

Typically, a Class D amplifier (Figure 2.1) consists of two stages. The first stage is a signal processing stage that converts the input audio signal into a two-level (1-bit) signal. This two-level signal represents a Pulse-Width Modulation (PWM) signal or a Pulse-Density Modulation (PDM) signal. The second stage of the amplifier is a power output stage, in which the two-level signal drives the output power MOSFETs (half-bridge or full-bridge).

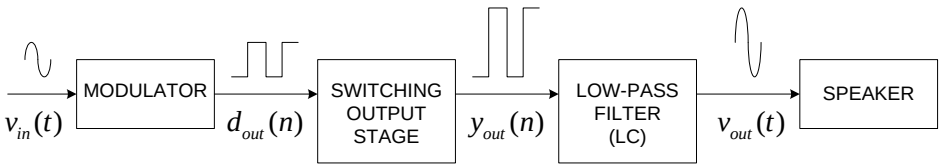


Figure 2.1: Class D open-loop-amplifier block diagram.

The Class D amplifier dissipates much less power than the traditional Class A/AB. The output stage devices switches between the positive and negative power supplies so as to produce a train of voltage pulses. This waveform reduces the power dissipation of the amplifier, because the output transistors have zero current when not switching, and have low V_{DS} when they are conducting current, thus resulting in a

smaller power dissipation ($V_{DS} \times I_{DS}$) in the amplifier. Due to the binary switching of the output devices of the amplifier, the output signal of the amplifier contains high frequency components. These components must be filtered in order to reduce the electromagnetic energy radiated by the amplifier, typically, a LC filter is used for this function.

2.1.1 Important Factors in Audio Class D Design

The strongest motivation to use Class D for audio applications is the low power dissipation, but there are important challenges in the design of this type of amplifiers. These include:

- Sound quality
- Modulation techniques
- Electromagnetic interference (EMI)
- LC filter design
- Total system cost
- System specifications

2.2 Sound Quality

To achieve a good sound quality in Class D audio amplifiers, some issues must be taken into account.

The sound quality of an audio amplifier is fundamentally determined by its performance in term of distortion (e.g. THD) and noise (e.g. PSRR). One of the problems with open-loop Class D amplifier is the propensity of the output stage to introduce non-linearities and noise into the signal [3]. The non-linearity and noise will, as a result, lead to poor THD and PSRR performance in an open-loop Class D amplifier.

The Power-supply noise couples almost directly to the speaker with very small rejection. This occurs because the output stage transistors connect the power supplies to the low-pass filter through a very low resistance. The filter rejects high-frequency noise, but is designed to allow all audio frequencies, including the low frequencies from the Power-supply (noise). However, there are good solutions to these problems. Using singe-loop feedback with high loop gain (as is done in many linear amplifiers) or double-loop feedback contributes a lot for a better performance [4]. Feedback from the LC filter input will significantly improve PSRR and attenuate all non-LC-filter distortion mechanisms. LC filter nonlinearities can be attenuated by including the speaker in the feedback loop. On the other hand, the use of a loop feedback complicates the amplifier design.

2.3 Modulation Technique

The first step in designing a switching amplifier is the choice of the modulation technique.

One of the main challenges in the design of class D amplifiers is designing the modulator circuit that encodes the input analogue signal into a switching sequence used to produce the output power signal. The spectrum of the switching sequence contains the desired audio signal plus undesired (but unavoidable) high-frequency content. The three most common architectures used to implement the modulator are: pulse-width modulation (PWM) [3] with a triangle-wave (or saw-tooth) oscillator, self-oscillating modulation [5] and Sigma-Delta Modulation [6] [7] (SDM).

2.3.1 Pulse Width Modulation (PWM)

Pulse-width modulation is the most common modulation technique, as shown in Figure 2.2. Conceptually, PWM compares the input audio signal to a triangular or ramping waveform with a fixed carrier frequency. This creates a stream of pulses at

the carrier frequency within each period of the carrier, the duty-cycle ratio of the PWM pulse is proportional to the amplitude of the input signal . This sampling process is called natural sampling. One challenge in this case is to generate a linear carrier to minimize harmonic distortion, this can be particulary hard for large carrier frequencies.

This modulation technique is attractive because the concept is simple and it allows high SNR on audio-band; however, PWM has several problems: The PWM process inherently adds distortion in many implementations [8], also, harmonics of the PWM carrier frequency produce electromagnetic interference (EMI).

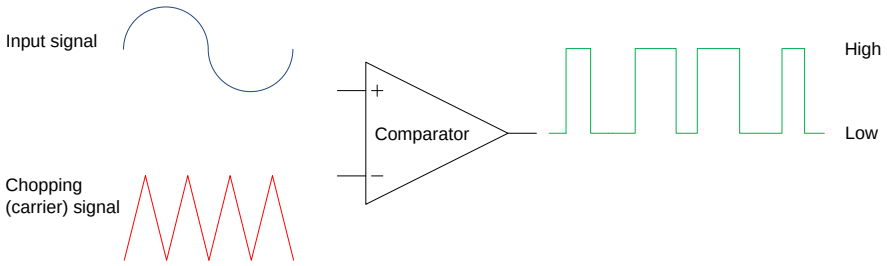


Figure 2.2: Analog PWM generator.

2.3.2 Pulse Density Modulation (PDM)

A PDM signal can be generated using a ($\Sigma\Delta$) modulator. The modulator uses a low resolution quantizer (typically 1-bit) to produce a digital signal from the input signal. The filter in the modulator has a high-pass transfer function that removes the quantization noise from the lower frequencies and transfers it to the higher frequencies. The high frequency quantization noise can be eliminated by a low pass filter. Sigma-Delta modulators are very well known and are the chosen architecture for A/D converter of audio signals and therefore the design of these type of circuits is very well understood [7]. A broad overview of $\Sigma\Delta$ Modulation will be presented in Chapter 3.

2.3.3 Self-Oscillating Modulation

Self-oscillating amplifiers use the feedback loop to create their own clock signal, instead of using an externally provided clock [5]. The properties of the loop determine the variable switching frequency of the modulator. An outstanding audio quality is possible thanks to the feedback; nevertheless, the loop is self-oscillating, so it's difficult to synchronize with any other switching circuits, or to connect to digital audio sources without first converting the digital to analog. Figure 2.3 depicts the principle of an self-oscillating amplifier.

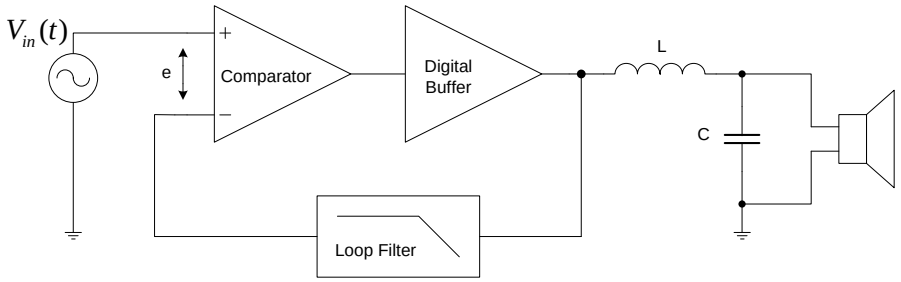


Figure 2.3: Principle scheme of an basic Self-Oscillating amplifier.

The basic building block consists of a comparator, a loop filter and a digital buffer. The comparator is not clocked, so the loop is fully analog. The loop filter is constructed so the loop is unstable. A limit cycle oscillation exists in the loop, resulting in a square wave output with a determined frequency. When this unstable system is forced by an external signal (V_{in}) with a frequency lower than this self-oscillation frequency, the limit cycle acts as dither and linearizes the system as long as the error signal (e) at the inputs of the comparator is smaller than the limit cycle amplitude at the comparator input. The output is a square wave containing the limit cycle frequency and the forced signal. The transfer function of the linearized system is dependent on the limit cycle amplitude [9].

2.4 Output Power Stage

The output stage of the Class D amplifiers are usually implemented using two topologies: half-bridge or full-bridge configurations. Each topology has advantages and disadvantages.

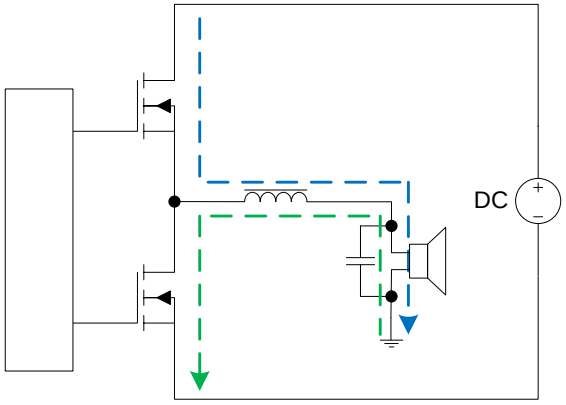


Figure 2.4: Half-bridge output stage with LC low-pass filter.

In brief, a half-bridge (depicted in Figure 2.4) is potentially simpler and requires a simpler low pass filter, however the current drawn from the power supplies is signal dependent and therefore a signal replica can appear in the power supply voltages which can cause distortion. In order to reduce this effect it is necessary to filter the signal from the power supply using large capacitors.

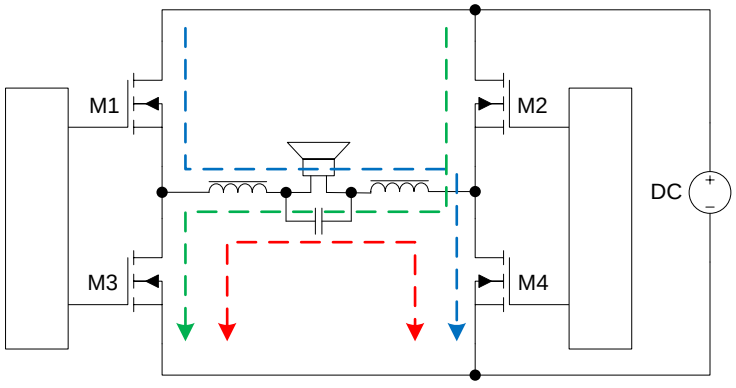


Figure 2.5: Full-bridge output stage with LC low-pass filter.

The full-bridge is shown in Figure 2.5). This topology requires two half-bridge amplifiers and a more complicated output filter. The full-bridge draws a constant

current from the power supply and therefore does not introduce the signal in the power supply, which improves the circuit performance and simplifies the design of the power supply circuit. Another advantage of the full-bridge configuration is the absence of the offset, which means that zero DC current flows at the output and consequently improving the global power dissipation. Also, this configuration allows 1.5-bit quantization and the corresponding three-level quantization can be described as:

1. $[-1] \rightarrow$ green path (M2 to M3)

2. $[\ \ 0] \rightarrow$ red path (M3 to M4 or M4 to M3)

3. $[+1] \rightarrow$ blue path (M1 to M4)

2.5 EMI Considerations

The high-frequency components of the switching signal in a Class D amplifier outputs requires serious consideration. If not properly understood and managed, these components can generate large amounts of electromagnetic interference (EMI) and disrupt operation of other electrical equipment nearby.

The EMI can have two sources of origin: signals that are radiated into space and those that are conducted via speaker and power-supply wires. A useful principle is to minimize the area of loops that carry high-frequency currents, since the strength of associated EMI is related to loop area and the proximity of loops to other circuits [10]. The amount of power radiated from these loops is dependent of the loop area when compared to the wavelength of the signals, therefore it is also important to reduce the maximum frequency of the signals in the amplifier. This means that it is very important to use a switching frequency as low as possible, corresponding to using a low OSR in the $\Sigma\Delta$ modulator.

2.6 LC Filter

The essential idea of the output filter of a Class D audio amplifier is to prevent the radiation of the high frequency components of the switching output signal. Since the energy of the unwanted signals is located at high frequencies this means using a low-pass filter. The inductance of a loudspeaker coil alone will, in general, be low enough to allow some of the switching-frequency energy to pass through it to ground, causing significant losses [11]. A correctly designed output filter limits supply current, protects the loudspeaker from switching waveforms and reduces EMI.

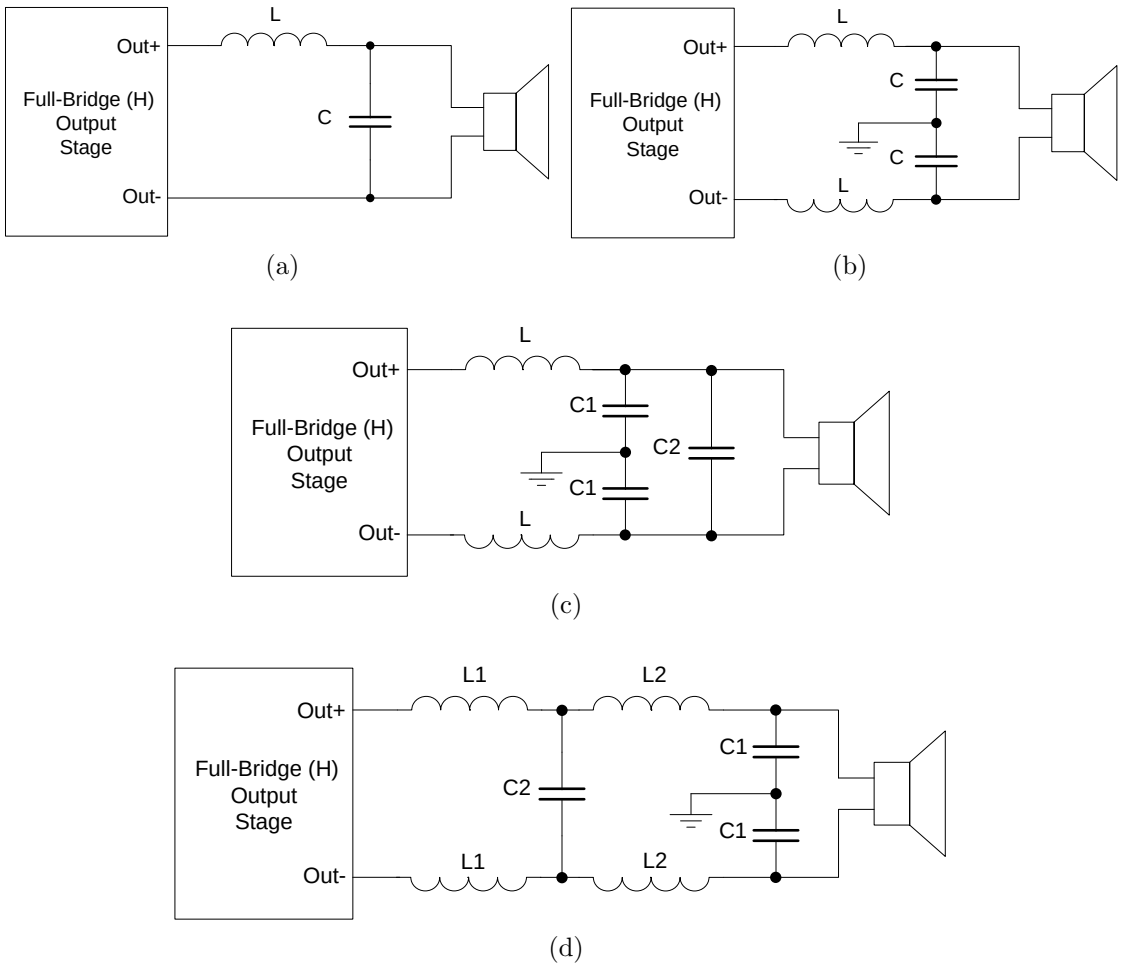


Figure 2.6: Filter arrangements for the full-bridge output stage. (a) is the simplest but allows a common-mode signal on the speaker cabling. (b) and (c) are the most usual versions. (d) is a four-pole filter.

The use of an output full-bridge requires a somewhat more complex output filter. If the simple two-pole filter of Figure 2.6a is used, the switching frequency is kept out of the loudspeaker, but the wiring to it will carry a large common-mode signal from the amplifier. A balanced filter is therefore commonly used, in either the Figure 2.6b or Figure 2.6c versions. Figure 2.6d illustrates a four-pole output filter.

2.6.1 Design

The design of the the low-pass filter for the Class D amplifier is based on a single-ended approach (Figure 2.7).

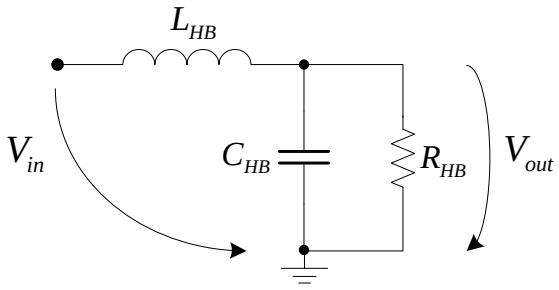


Figure 2.7: LC low-pass filter for single-ended.

The transfer function of the filter can be derived using a voltage divider equation in which the load impedance is a parallel combination of R_{HB} and C_{HB}.

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{R_{HB}}{s \cdot R_{HB} \cdot C_{HB}+1}}{\frac{R_{HB}}{s \cdot R_{HB} \cdot C_{HB}+1} + s \cdot L_{HB}} = \frac{\frac{1}{L_{HB} \cdot C_{HB}}}{s^2 + s \cdot \frac{1}{R_{HB} \cdot C_{HB}} + \frac{1}{L_{HB} \cdot C_{HB}}} \tag{2.1}$$

A Butterworth approximation low pass filter for providing flat response in the pass band can be chosen, which is critical for the audio system to improve its dynamic performance. Equaling Equation 2.1 to the characteristic equation of a second-order Butterworth filter in a standard form is obtained.

$$H(s) = \frac{\frac{1}{L_{HB} \cdot C_{HB}}}{s^2 + s \cdot \frac{1}{R_{HB} \cdot C_{HB}} + \frac{1}{L_{HB} \cdot C_{HB}}} = \frac{1}{s^2 + s \cdot \sqrt{2} + 1} \tag{2.2}$$

Analyzing the Equation 2.2 an equation for C_{HB} can be written as:

$$C_{HB} = \frac{1}{2 \cdot \sqrt{2} \cdot \omega_c \cdot R_{HB}} \tag{2.3}$$

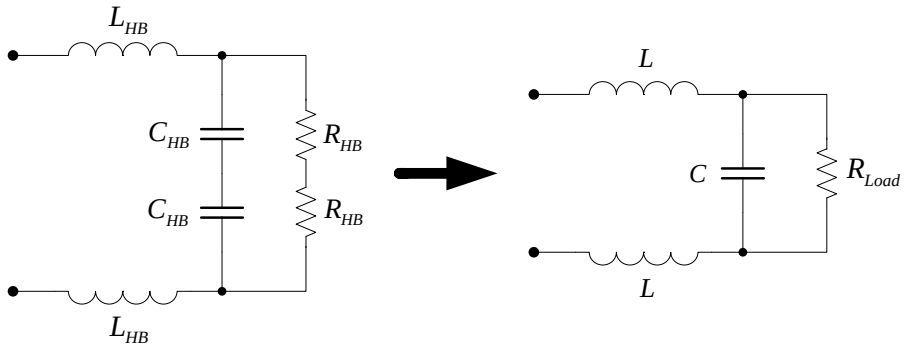


Figure 2.8: Combination of two half-bridge in to a full-bridge topology.

Due to the combination of two half-bridge in to a full-bridge topology (depicted in Figure 2.8) some relations can be done: $C = \frac{C_{HB}}{2}$ and $R_{Load} = R_{HB} \cdot 2$.
Replacing in Equation 2.3 the C_{HB} for $C \cdot 2$ and R_{HB} for $\frac{R_{Load}}{2}$ the Equation for the capacitor is given by:

$$C = \frac{1}{2 \cdot \sqrt{2} \cdot \omega_c \cdot R_{Load}} \tag{2.4}$$

The value of the inductance remain the same, after the combination of two half-bridge in to a full-bridge, and the expression for the L_{HB} is given by:

$$L_{HB} = \frac{1}{C_{HB}} = \frac{\sqrt{2} \cdot R_{HB}}{\omega_c} \rightarrow L = L_{HB} \tag{2.5}$$

Typically, a 4 or 8 Ω resistor is assumed for the calculus of the filter components; however, it is necessary to have in mind that, in reality, we have different speakers with different types of frequency response. Due to this, is necessary to compensated the filter variations with a proper network feedback design.
The output inductor should withstand the whole output current without saturation, as well as keep the energy for the off cycle. An ideal inductor (in terms of linearity)

is an air-cone; nerveless, the size and number of turns required for the output stage of Class D amplifiers makes it impractical, so a core has to be used in order to reduce turn number and also provided a confined magnetic circuit. Powder cores or ferrite cores can be used [12]. In Ferrite cores, it is necessary a "gap" where the energy is stored.

2.7 Total system cost

In the design of the Class D amplifiers it is necessary to have in mind the estimative of the total system cost for the success of the product in terms of market share and viability.

One way (and the most significant) to reduce the total system cost is the use of the half-bridge topology for power stages in order to take advantage of the minor complexity and reduced of material costs. Since a half-bridge is normally half of a common full-bridge output, the quantity of power MOSFET's and output filter components is reduced by a factor of 2. However, the use of a half-bridge instead of a full-bridge topology requires a DC-blocking capacitor at the output, hence highly susceptible to noise on the power supply rail, and does not allow the use of 1.5-bit quantization.

Another situation to have in mind is the choice of the tolerance of the resistors (R) and capacitors (C) . The use of components mismatch with R=1% and C=5% instead of R=5% and C=20%, increases the cost of those components (R and C) in about 40%; however, the results will be better in terms of performance. This analysis was based on prices from the online store *RS*® [1].

[1] http://pt.rs-online.com/web/

2.8 System Specifications

The sensitivity of the human ear is biased toward the lower end of the audible frequency spectrum, around 3 kHz. Being 50 Hz, the bottom end of the spectrum, and being 17 kHz, the top end at those limits, the sensitivity of the ear is reduced by approximately 50 dB from the sensitivity at 3 kHz [13]. Taking advantage of these features of the ear and considering that most people will not be able to hear sounds above 16 kHz, the bandwidth of an audio amplifier, in reality, does not need to be higher than 18 kHz.

A low switching frequency is important because it allows to use power transistors with lower transition frequency (fT), thus lowering the cost. The behavior of the transistor is similar to an ideal switch, when the switching frequency is lower. The choice of f_S have also to have in mind the limits of the frequency switching of the IC drivers existing in the market[2], in order to possibility the implementation of the output stage with IC drivers and to not increase significantly the oversampling ratio (OSR).

[2]ZL1505 - An integrated high-speed MOSFET driver from *Intersil*® (http://www.intersil.com)

Chapter 3

Sigma-Delta Modulation

3.1 Introduction

Sigma-Delta ($\Sigma\Delta$) modulators are the most suitable A/D converters for low-frequency, high-resolution applications, in view of their inherent linearity, reduced anti-aliasing filtering requirements and robust analog implementation. Moreover, by trading speed for accuracy, $\Sigma\Delta$ modulators allow high performance to be achieved with low sensitivity to analog component imperfections and without need for component trimming [14].

One of the advantages of Sigma-Delta Modulation (SDM) is that most of the high-frequency energy in Sigma-Delta is distributed over a wide range of frequencies (not concentrated in tones at multiples of a carrier frequency, as in PWM) providing SDM with a potential EMI advantage over PWM.

Sigma-Delta Modulation can be implemented using Continuous-time (CT) or discrete-time (DT) integrators. Compared to their discrete-time counterparts, CT-SDM's provide the added benefit of inherent anti-alias filtering and sampling error suppression [15]. Also, the gain-bandwidth product (GBW) and slew rate requirements of the used amplifiers in CT are much lower compared to their DT. However, their principal disadvantage is their sensitivity to clock jitter [16]. Several architectures

options for a modulator in order to improve the signal-to-noise-and-distortion ratio (SNDR) value, without increasing the oversampling ratio (OSR) or the order of the modulator, can be implemented [17].

3.2 $\Sigma\Delta$ ADC Basic Concepts

This chapter is intended to give an basic introduction and overview of analog-to-digital conversion (ADC), first in general and thereafter for the $\Sigma\Delta$ modulation, in this case, the CT-$\Sigma\Delta$ modulator.

3.2.1 Sampling and Quantization

The process of the conversion of analog signals to the digital domain can be separated in two operations [18]: the uniform sampling in time and the quantization in amplitude. Assuming that the signal information of the continuous input signal $x(t)$ is contained in the signal band ($\mid f_{sig} \mid \leq f_B$ where f_B is the signal bandwidth), the sampling in time is a completely reversible process. The original signal (continuous input signal) can be reconstructed without aliasing by simply low-pass filtering the sampled signal, as long as the Nyquist Theorem is fulfilled ($f_S \leq 2 \cdot f_B = f_N$).
In the process of quantization in amplitude, a continuous range of analog values is encoded into a set of discrete levels and the process of quantization is non-reversible. The quantization process involved in A/D conversion is an inherently non-linear operation and introduces errors to the conversion [19]; thus, the primary objective in A/D converter design is to limit this error.
The Figure 3.1 shows the transfer function of an ADC or quantizer, and as previously mentioned, is nonlinear. Considering that the input signal is random, that it changes rapidly and that the number of quantization steps is large, then the quantization error or noise (e_n) can be considered white noise. The quantization steps can be defined as $\Delta = \frac{FS}{2^B - 1}$ where FS is the full-scale output range and B the number of

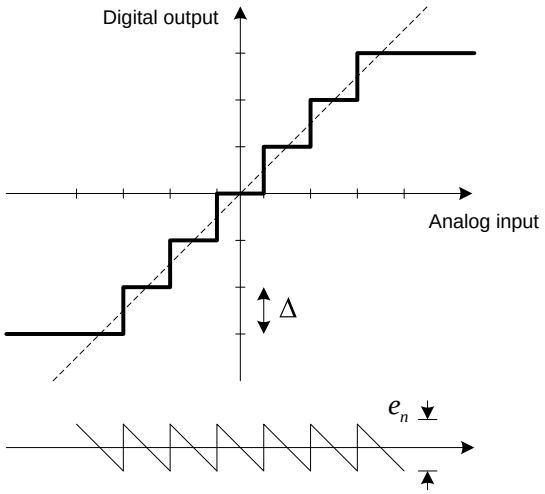


Figure 3.1: Quantization error (e_n) when the quantization interval is defined by the midpoint.

bits. Thus, the quantization noise power can be expressed as:

$$e_{rms}^2 = \frac{1}{\Delta}\int_{\frac{\Delta}{2}}^{-\frac{\Delta}{2}} e^2 \, de = \frac{\Delta^2}{12} \tag{3.1}$$

The noise power spectral density (PSD) of the quantization is given by:

$$S_e(f) = \frac{e_{rms}^2}{f_S} = \frac{\Delta^2}{12} \cdot \frac{1}{f_S} \tag{3.2}$$

Oversampling

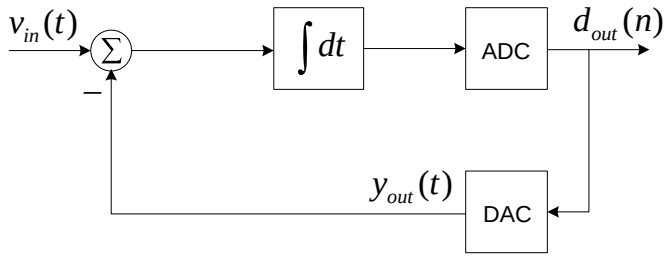
If an ideal low pass filter is used the SNR improves 3 dB each time the over-sampling ratio is doubled (where $OSR = \frac{f_S}{2 \cdot f_B}$). A generic equation for the SNR is given by [6]:

$$SNR = 6.02 \cdot B + 1.76 + 10 \cdot log(OSR) \ (dB) \tag{3.3}$$

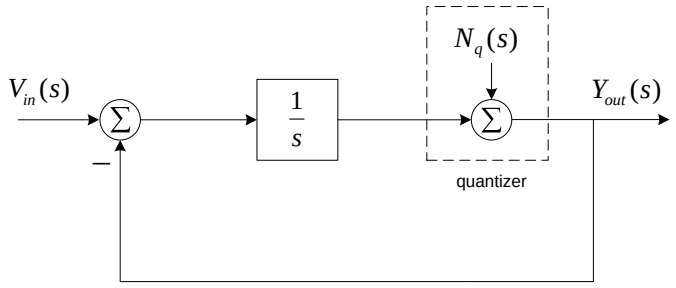
It is important to understand that this is an approximated expression due to the fact that in reality the quantization noise is correlated to the input signal and therefore the PSD of the quantization noise is not uniform.

3.2.2 First order CT-ΣΔ Modulator

The analysis of the sampling and noise theory, mentioned before, can now be used to show how a ΣΔ modulator shapes quantization noise. The Block Diagram of the 1st order ΣΔ modulator principle is illustrated in Figure 3.2a.



(a) ΣΔ modulator principle.



(b) Linearized mathematical model.

Figure 3.2: Block Diagram of the 1st order ΣΔ modulator

The comparator of the circuit is represented in the sum node at the right of the integrator and it's here that sampling occurs and quantization noise is added. Constantly, the output value is subtracted from its input signal and the result of this operation is fed to the quantizer via an integrator. The feedback forces the average value of the quantized output to track the average input. Any differences between them accumulates in the integrator and the feedback loop will correct itself.

The main characteristic of a ΣΔ modulator is the different transfer behavior for the quantization error signal, the noise transfer function (NTF) and the input signal the signal transfer function (STF). Analyzing the mathematical model from Figure 3.2b, the modulator output may be expressed by 2 ways:

1. Letting $N_q(s) = 0$ for the moment, and solving for $\frac{Y_{out}(s)}{V_{in}(s)}$ is possible to obtain the STF:

$$Y_{out}(s) = [V_{in}(s) - Y_{out}(s)] \cdot \frac{1}{s}$$

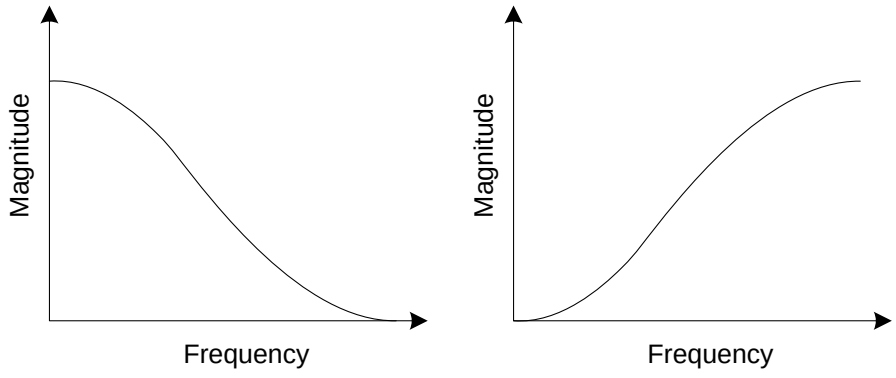
$$STF = \frac{Y_{out}(s)}{V_{in}(s)} = \frac{\frac{1}{s}}{1 + \frac{1}{s}} = \frac{1}{s+1} \tag{3.4}$$

2. By letting the signal $V_{in}(s) = 0$ and solving for the $\frac{Y_{out}(s)}{N_q(s)}$ the NTF is obtained:

$$Y_{out}(s) = -Y_{out}(s) \cdot \frac{1}{s} + N_q(s)$$

$$NTF = \frac{Y_{out}(s)}{N_q(s)} = \frac{1}{1 + \frac{1}{s}} = \frac{s}{s+1} \tag{3.5}$$

Analyzing the Equations 3.4 and 3.5 above, they shows that indeed the oversampled modulator acts as a low-pass filter for the input signal (showed in Figure 3.3a) and a high-pass filter for noise. In Figure 3.3b is shown the noise shaping of the oversampled 1st order ΣΔ modulator.



(a) STF (b) NTF

Figure 3.3: NTF and STF of the 1st order ΣΔ modulator

3.3 Study of 3rd Order CT-ΣΔ Modulators

The first step in the design of the modulator is choosing the order modulator, the clock frequency value, and the bandwidth. ΣΔ modulators of orders higher than 2 are possible to design but they cannot simply be made by adding further stages because the resulting system would, most likely, be unstable. In view of this problem, the design procedure for finding the optimal 3rd ΣΔ modulator coefficients was based on the described in [20]. Briefly, this methodology describes an empirical method based on ordinary filter design that can be used to design high-order modulators.
Taking advantage of the features of the human ear described in Chapter 2 Section 2.8 and considering that most people will not be able to hear sounds above 16 kHz, the bandwidth of an audio amplifier, in reality, does not need to be higher than 18 kHz. Therefore the modulator will be designed to have a signal bandwidth of 18 kHz and a peak SNDR value with at least 80 dB (the SNDR is defined for a bandwidth of 18 kHz).
As previously stated, it very important to use a low sampling frequency value in order to reduce the EMI of the amplifier and also to avoid non-ideal effects in the output devices during switching. A ideal 3rd ΣΔ modulator (assuming that it could be stable) with an OSR value of 32 could theoretically produce an SNDR value of around 95 dB. Therefore a sampling frequency value of 1.2 MHz is selected, resulting in a OSR value of about 33.3.
However, due to the inherent instability of the modulator it is necessary to use a transfer function that limits the noise shaping resulting in a lower SNDR value. Therefore, several architecture options for the modulator will be studied in order to improve the SNDR value.

3.3.1 1-bit with Distributed Feedback

The block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback, implemented using CT integrators, is shown in Figure 3.4. The signal transfer function (STF) of this structure is given by Equation 3.6 and will be essentially a 3rd order Butterworth low pass filter. The cut-off frequency of this filter function is selected in order to limit the maximum gain of the NTF and eliminate the instability of the modulator.

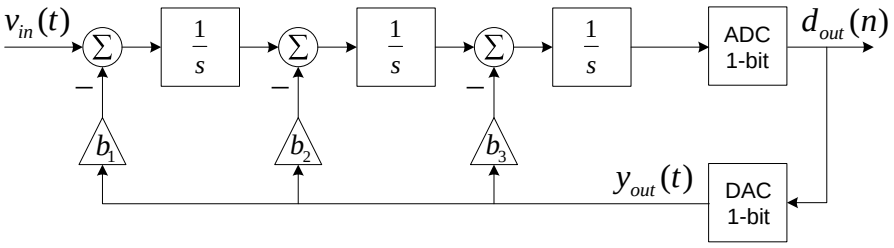


Figure 3.4: Block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback.

The noise transfer function (NTF) given by Equation 3.7 was designed to be a 3rd order Butterworth high-pass filter with a cut-off frequency of 99.6 kHz. The values of the coefficients b_1, b_2 and b_3 were calculated in order to implement the selected Butterworth transfer function. The modulator was simulated using $SIMULINK$®. Each simulation calculated 2^{19} points of the output signal and a fast Fourier transformation using a Blackman-Harris window was applied in order ro complete the output spectrum.

$$STF = \frac{1}{s^3 + s^2 \cdot b_3 + s \cdot b_2 + b_1} \tag{3.6}$$

$$NTF = \frac{s^3}{s^3 + s^2 \cdot b_3 + s \cdot b_2 + b_1} \tag{3.7}$$

Figure 3.5 shows the output spectrum of the traditional 3rd order 1-bit ΣΔ modu-

lator, obtained by simulation, in this case a maximum SNDR value of 64.2 dB was obtained. The frequency of the sine wave input signal is 1 kHz.

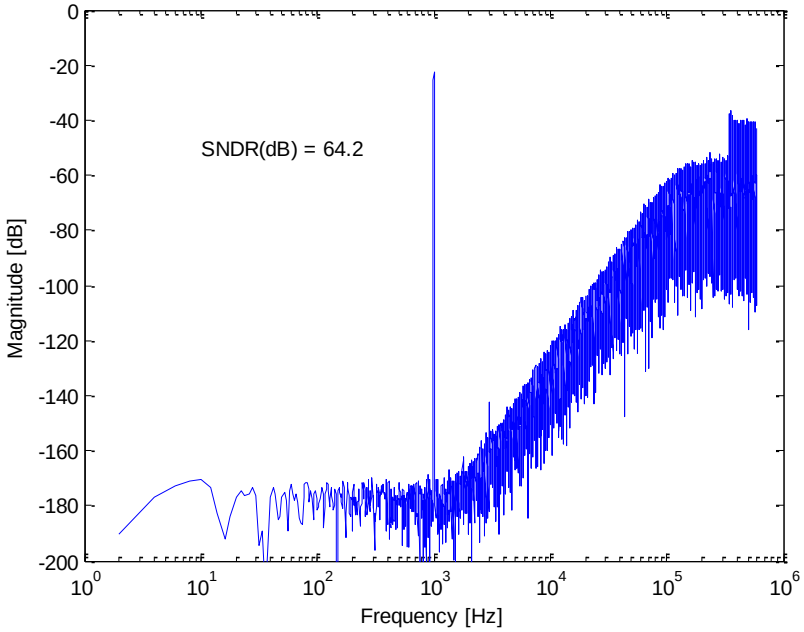


Figure 3.5: Output spectrum of the 3rd order 1-bit $\Sigma\Delta$ modulator with distributed feedback (2^{19} points FFT using a Blackman-Harris window).

The low SNDR results from the low cut-off frequency of the filter which in term can not be increased because the modulator would became instable.

3.3.2 1-bit with Distributed Feedback and Local Resonator Feedback

One technique to improve the SNDR is to optimally distribute the zeros of NTF inside the signal bandwidth, unlike the traditional design described above where NTF zeros are all placed at DC. The architecture shown in Figure 3.6 allows distributing the zeros of NTF inside the signal bandwidth and can be designed using a Chebyshev type II high-pass filter, in this case the stopband edge frequency of the filter is 18 kHz. The coefficients b_1, b_2 and b_3 determine the position of the poles and α the position of the zeros of the NTF (Equation 3.9). Note that the zeros do

not appear in the STF (Equation 3.8).

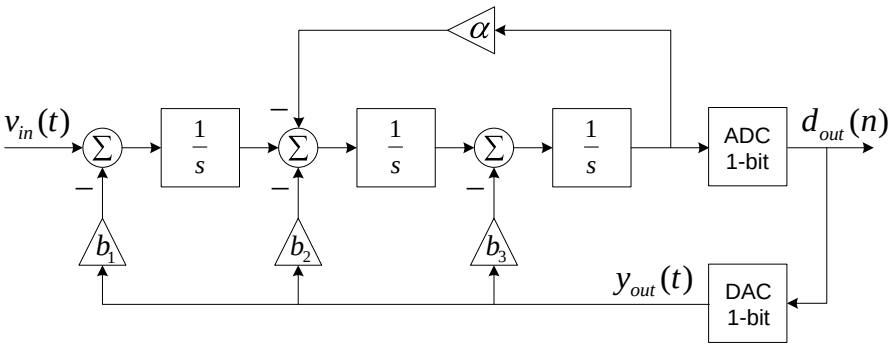


Figure 3.6: Block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback.

$$STF = \frac{1}{s^3 + s^2 \cdot b_3 + s \cdot (\alpha + b_2) + b_1} \tag{3.8}$$

$$NTF = \frac{s \cdot (s^2 + \alpha)}{s^3 + s^2 \cdot b_3 + s \cdot (\alpha + b_2) + b_1} \tag{3.9}$$

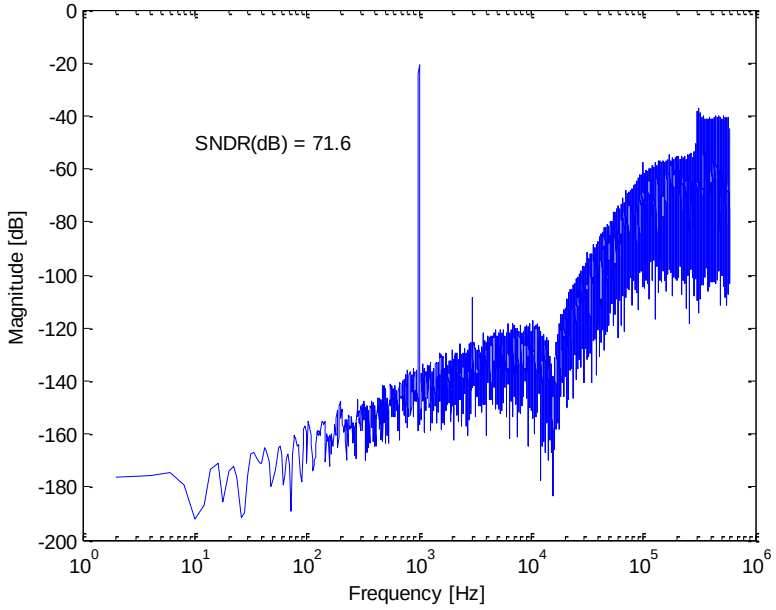


Figure 3.7: Output spectrum of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback (2^{19} points FFT using a Blackman-Harris window).

The Figure 3.7 shows the output spectrum of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback, obtained by simulation, in this case a maximum SNDR value of 71.6 dB was obtained. As expected, the shift of the zeros from DC to the signal bandwidth improved the maximum SNDR value.

3.3.3 1.5-bit with Distributed Feedback

Another option to improve the SNDR is use a 1.5-bit quantizer (corresponding to three-level quantization) instead of 1-bit quantizer. The increase of the resolution of the quantizer improves the linearity of the feedback in the modulator. Since this results in a more stable loop, it is possible to use a larger cut-off frequency in the modulator and therefore improve the maximum SNDR value. In this case a cut-off frequency of 133.2 kHz was selected. The use of three levels also reduces unnecessary switching of the full-bridge output stage so that the switching loss is minimized.

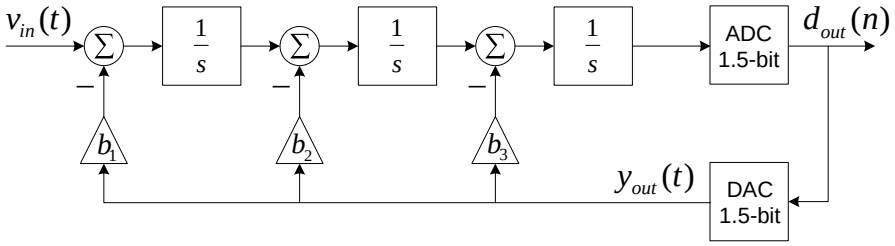


Figure 3.8: Block diagram of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback.

Figure 3.9 shows the simulated output spectrum of the 3rd order 1-bit ΣΔ modulator with a 1.5-bit quantizer, in this case a maximum SNDR value of 76.9 dB was obtained. As expected the increase in the resolution of the quantizer improved the maximum SNDR value of the modulator.

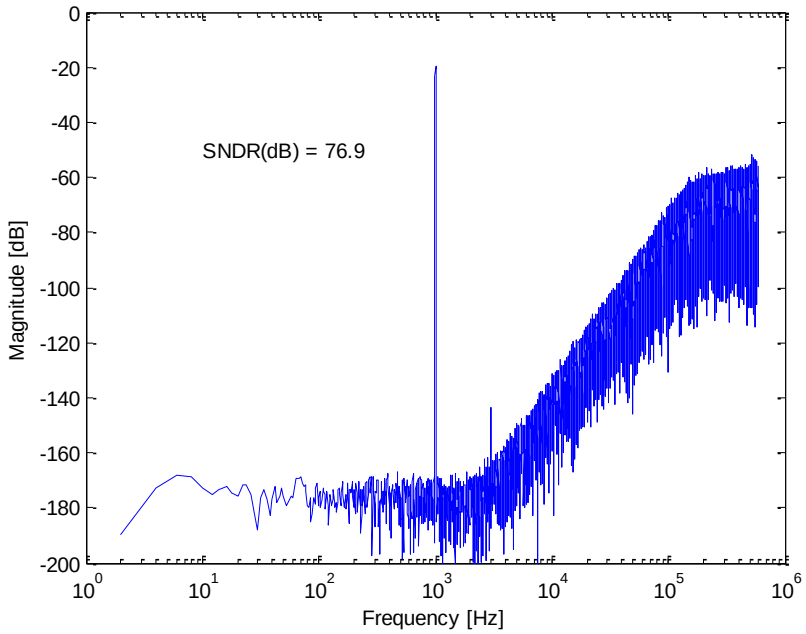


Figure 3.9: Output spectrum of the 3$^{\text{rd}}$ order 1.5-bit ΣΔ modulator with distributed feedback (2^{19} points FFT using a Blackman-Harris window).

Chapter 4

Proposed Architecture

4.1 Introduction

In order to obtain a maximum SNDR value with at least 80 dB, the topologies described in Chapter 3 Section 3.3 (3^{rd} order 1-bit $\Sigma\Delta$ with distributed feedback and local resonator feedback and the 3^{rd} order 1.5-bit $\Sigma\Delta$ with distributed feedback) were combined into the same modulator (Figure 4.1). The loop filter in the modulator was designed to have a stopband edge frequency of 18 kHz and a stop band attenuation of 58.5 dB, with a sampling frequency (f_S) of 1.2 MHz.

The choice of f_S was based in Chapter 2 Section 2.8 were the limits of the frequency switching of the IC drivers existing in the market and also a low switching frequency is important for a better performance in terms off efficiency. Furthermore, the stopband edge frequency of 18 kHz is based in Chapter 2 Section 2.8, were the features of the ear and considering that most people will not be able to hear above 16 kHz, the bandwidth of an audio amplifier, in reality, does not need to be higher than 18 kHz.

4.2 Theoretical Analysis

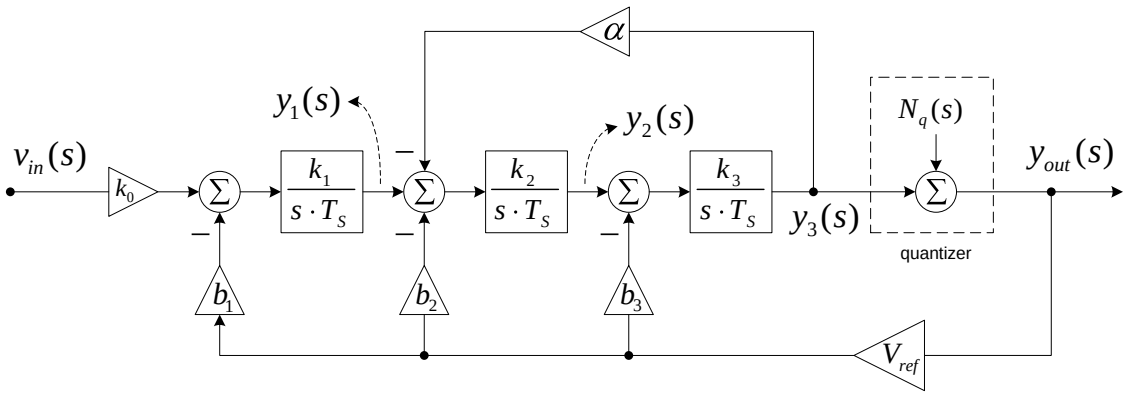


Figure 4.1: Block diagram of the 3rd order 1.5-bit ΣΔ modulator (mathematical model) with distributed feedback and local resonator feedback.

Analyzing the Block diagram of the Figure 4.1 same equations can be writen in order to obtain the signal transfer function (STF) and the noise transfer function (NTF) of the proposed architecture.

Letting $N_q(s) = 0$ for the moment the equations for the outputs are:

$$
\begin{aligned}
y_1(s) &= [v_{in}(s) \cdot k_0 - b_1 \cdot V_{ref} \cdot y_{out}(s)] \cdot \frac{k_1}{s \cdot T_S} \\
y_2(s) &= [y_1(s) - y_3(s) \cdot \alpha - b_2 \cdot V_{ref} \cdot y_{out}(s)] \cdot \frac{k_2}{s \cdot T_S} \\
y_3(s) &= [y_2 - b_3 \cdot V_{ref} \cdot y_{out}(s)] \cdot \frac{k_3}{s \cdot T_S} \\
y_{out}(s) &= y_3(s)
\end{aligned}
$$

Solving the the system of Equations for $\frac{y_{out}(s)}{v_{in}(s)}$ and for simplification assuming $k_1 = k_2 = k_3 = T_S$ the STF is obtained as:

$$
STF = \frac{y_{out}(s)}{v_{in}(s)} = \frac{k_0}{s^3 + s^2 \cdot b_3 \cdot V_{ref} + s \cdot b_2 \cdot V_{ref} + b_1 \cdot V_{ref}} \tag{4.1}
$$

By letting the signal $V_{in}(s) = 0$ the equations for the outputs are defined as:

$$
\begin{aligned}
y_1(s) &= [0 - b_1 \cdot V_{ref} \cdot y_{out}(s)] \cdot \frac{k_1}{s \cdot T_S} \\
y_2(s) &= [y_1(s) - y_3(s) \cdot \alpha - b_2 \cdot V_{ref} \cdot y_{out}(s)] \cdot \frac{k_2}{s \cdot T_S} \\
y_3(s) &= [y_2 - b_3 \cdot V_{ref} \cdot y_{out}(s)] \cdot \frac{k_3}{s \cdot T_S} \\
y_{out}(s) &= N_q(s) + y_3(s)
\end{aligned}
$$

Assuming for simplification $k_1 = k_2 = k_3 = T_S$ and solving for the $\frac{y_{out}(s)}{N_q(s)}$ the NTF is obtained as:

$$NTF = \frac{y_{out}(s)}{N_q(s)} = \frac{s(s^2 + \alpha)}{s^3 + s^2 \cdot b_3 \cdot V_{ref} + s \cdot b_2 \cdot V_{ref} + b_1 \cdot V_{ref}} \tag{4.2}$$

The NTF of the filter (Equation 4.2) allows distributing the zeros of NTF inside the signal bandwidth and can be designed using a Chebyshev type II filter. In order to implement the filter transfer function it was used the tool $SIMULINK®$ for several simulations . The $MATLAB®$ code synthesizing a CT Chebyshev type II filter is:

$$[A, B] = CHEBY2(order, R, Wn, 'high', 's')$$

where $order = 3$ defines the NTF order of the filter, with the stopband ripple $R =$ 58.5 dB and stopband edge frequency $Wn = 18 \cdot 10^3 \cdot 2\pi$ [rad/s] and the "'high','s'" designs a CT high-pass filter. The Equation 4.3 gives the transfer function of the high-pass filter obtained with the previous $MATLAB®$ code.

$$NTF = \frac{s(s^2 + 9.574 \cdot 10^9)}{s^3 + s^2 \cdot 1.334 \cdot 10^6 + s \cdot 8.999 \cdot 10^{11} + 3.034 \cdot 10^{17}} \tag{4.3}$$

Comparing the NTF of Equation 4.2 with the NTF of Equation 4.3 it is possible to obtain all the coefficients for the simulation of the proposed architecture in

SIMULINK®. Note that is necessary to adjust the stopband ripple to obtain a maximum SNDR value and also a stable loop filter.

The Table 4.1 gives the coefficients values of the simulated architecture.

Table 4.1: Coefficients of the proposed architecture.

Coefficients					
k_0	$k_1 = k_2 = k_3$	b_1	b_2	b_3	α
0.0621	1	0.1756	0.6249	1.1120	0.0066

Figure 4.2 shows the output spectrum of the modulator, obtained by simulation, in this case a maximum SNDR value of 80.2 dB was obtained. The combination of all the previous techniques, studied in Chapter 3 Section 3.3, allowed to obtain a maximum SNDR value with at least 80 dB using a 3rd order $\Sigma\Delta$ modulator with an OSR value of approximately 32.

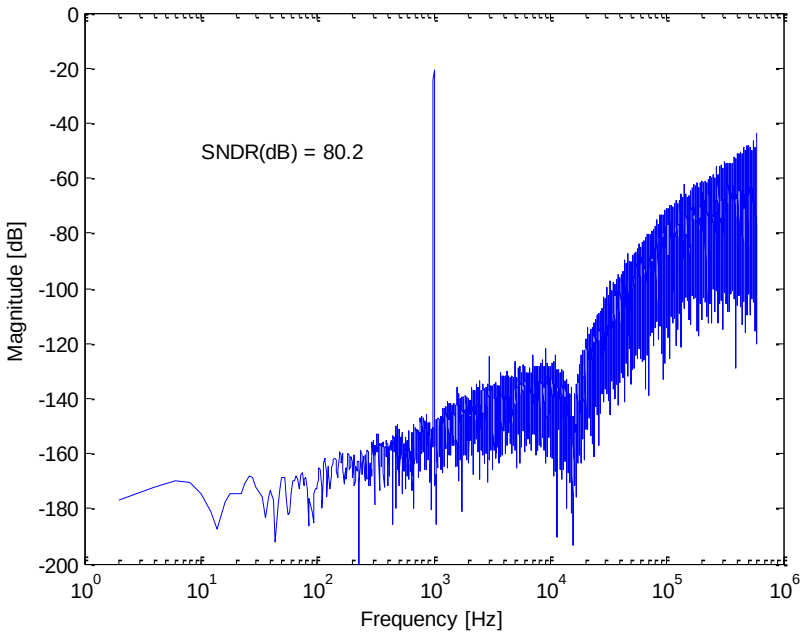


Figure 4.2: Output spectrum of the 3rd order 1.5-bit $\Sigma\Delta$ modulator with distributed feedback and local resonator feedback (2^{19} points FFT using a Blackman-Harris window).

4.3 Circuit Design

It is necessary to design an electrical circuit that has the same behavior as the architecture that was developed in the previous section.

Figure 4.3 shows a simple method to convert the mathematical model into the electrical model. Note that the T_S ($\frac{1}{F_S}$) is the period of the sampling frequency (F_S = 1.2 MHz).

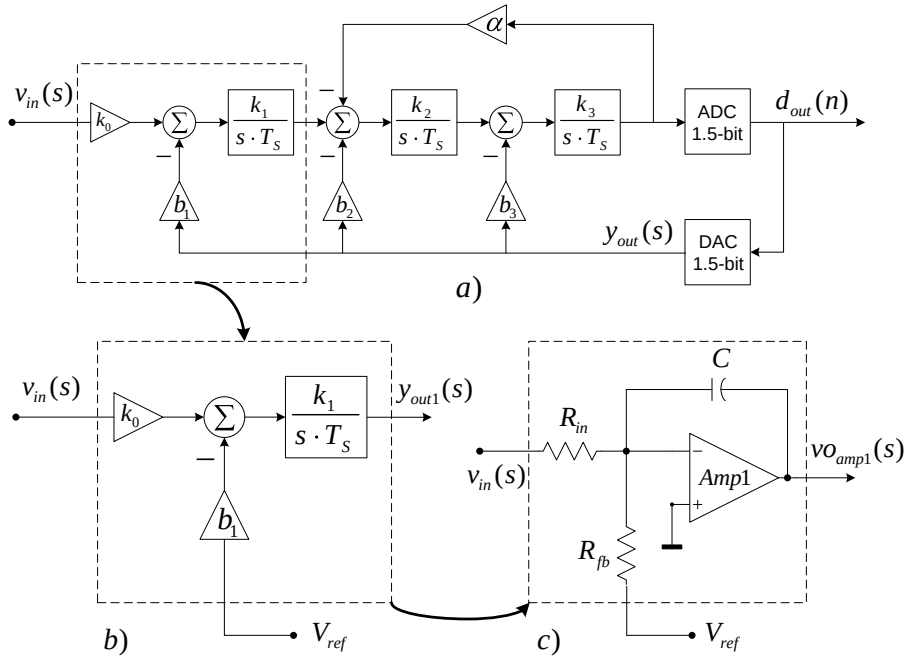


Figure 4.3: Conversion of the mathematical model into the electrical model.

Analyzing the Figure 4.3.b) an equation for $y_{out1}(s)$ can be written as:

$$y_{out1}(s) = \frac{k_0 \cdot k_1}{s \cdot T_S} \cdot v_{in}(s) - \frac{b_1 \cdot k_1}{s \cdot T_S} \cdot v_{ref}(s) \tag{4.4}$$

The equation for the output ($vo_{amp1}(s)$) of the integrator (depicted in Figure 4.3.c)) is given by:

$$vo_{amp1}(s) = -\frac{1}{s \cdot R_{in} \cdot C} \cdot v_{in}(s) - \frac{1}{s \cdot R_{fb} \cdot C} \cdot v_{ref}(s) \tag{4.5}$$

Equaling Equation 4.4 to Equation 4.5 ($y_{out1}(s) = vo_{amp1}(s)$) is possible to obtain

an expression for R_{in} and R_{fb}. Note that the operational amplifier is considered ideal in this approach.

$$R_{in} = \frac{T_S}{k_0 \cdot k_1 \cdot C}, \qquad R_{fb} = \frac{T_S}{b_1 \cdot k_1 \cdot C} \tag{4.6}$$

The same idea can be applied to the other integrators blocks of the modulator resulting in the modulator circuit shown in Figure 4.4. The values of the components can be obtained using the approach previously described, assuming that all the capacitors have a 1nF value.

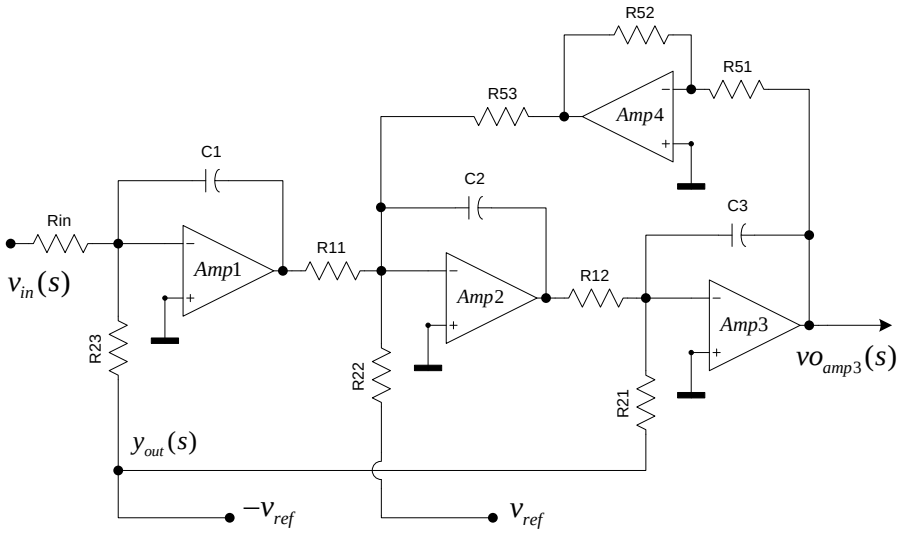


Figure 4.4: Schematic design of the modulator.

Table 4.2 gives all passive component values for the modulator.

Table 4.2: Selected passive component values.

Components		
Id.	Value	Units
$C_1 = C_2 = C_3$	1	nF
R_{in}	13.3	kΩ
$R_{11} = R_{12}$	825	Ω
R_{23}	4.75	kΩ
R_{22}	1.33	kΩ
R_{21}	750	Ω
$R_{51} = R_{52}$	10	kΩ
R_{53}	124	kΩ

In order to confirm the correct design of the modulator, the STF (Figure 4.5) and NTF (Figure 4.6) of the modulator are obtained by performing two AC simulations of the circuit of Figure 4.4, after replacing the quantizer by a wire.

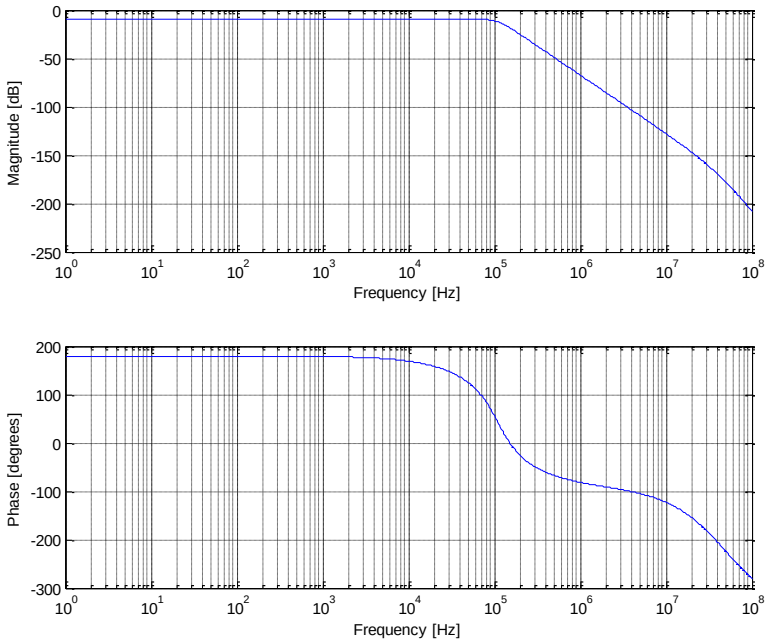


Figure 4.5: Bode diagram of the STF of the modulator.

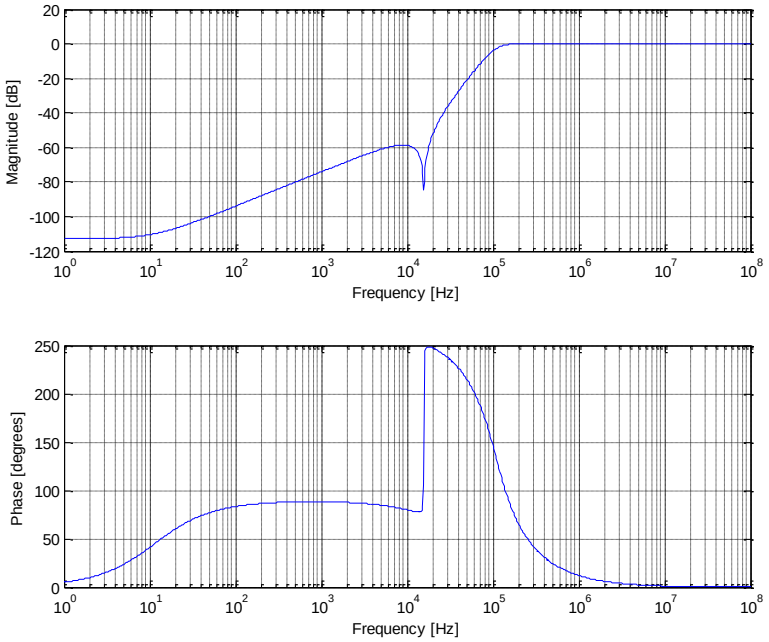


Figure 4.6: Bode diagram of the NTF of the modulator.

4.3.1 ADC Design

The 1.5-bit quantizer (three levels) is realized by two comparators and is showed in Figure 4.7. The output of the comparators is encoded to 1.5-bit representation using the circuit shown in Figure 4.10. The threshold voltage for comparison is determined by several simulations of the propose architecture in order to obtain the max point of the SNDR as function of the threshold voltage. Figure 4.8 shows the measured SNDR as function of threshold voltage (V_t), from this simulation results the value of 0.36V was selected for V_t.

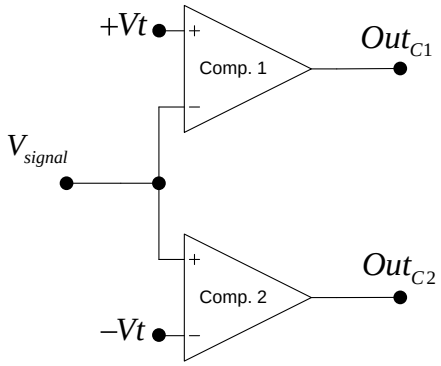


Figure 4.7: Schematic design of 1.5-bit quantizer.

Table 4.3: ADC codification.

V_{Signal}	State	Out_{C1}	Out_{C2}
$V_{Signal} > V_t$	+1	0	1
$-V_t < V_{Signal} < V_t$	0	1	1
$V_{Signal} < V_t$	-1	1	0

Since the threshold voltage of the comparators has a random error, a Monte Carlo analysis, where the V_t voltage of the comparators was randomly changed from the selected nominal value with a 3σ value of 10 mV, was performed for 500 cases. The histogram of the SNDR values obtained in this analysis is shown in Figure 4.9, this histogram shows that the SNDR in the worst case only degrades about 0.8 dB with the variation of the offset of the comparators.

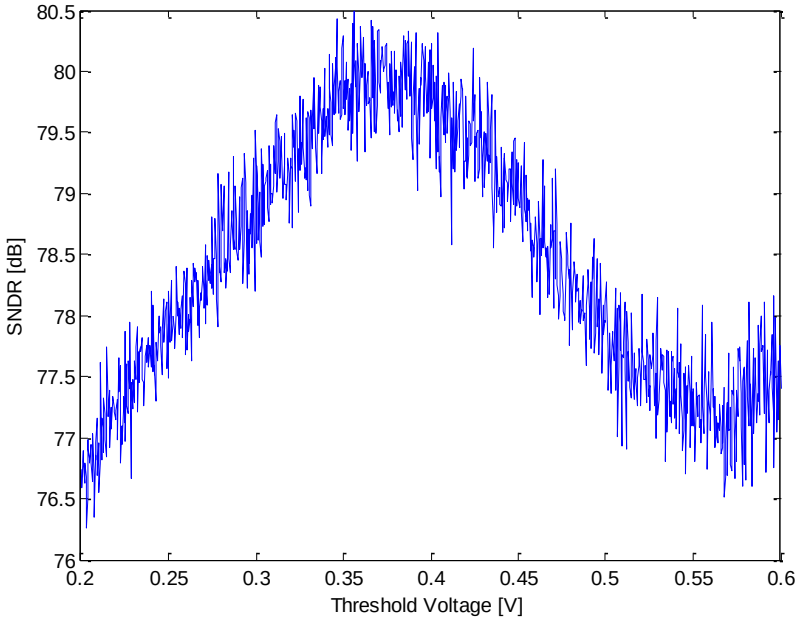


Figure 4.8: Measured SNDR as function of threshold voltage (V_t). Data obtained by running 1000 simulations with a Vt step of 0.4 mV.

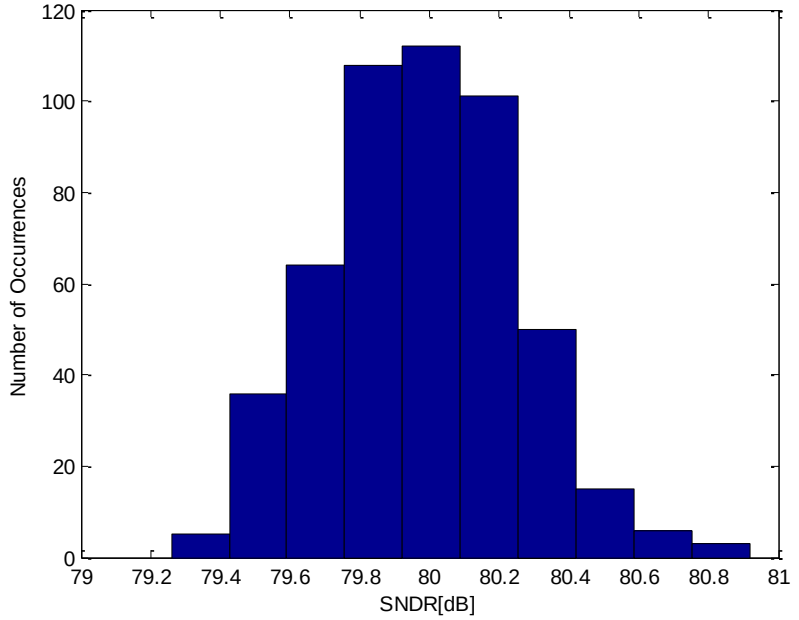


Figure 4.9: Histogram of the behavioral simulated SNDR of the proposed $\Sigma\Delta$ modulator ($3\sigma_{vt} = 10$ mV) . Data obtained by running 500 Monte-Carlo simulations of the proposed architecture.

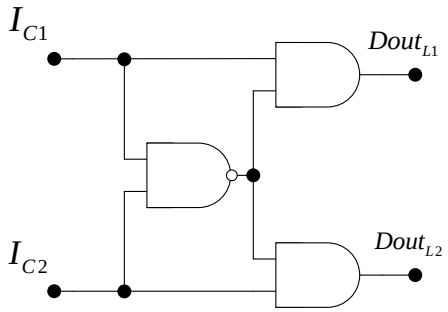


Figure 4.10: Encoding logic for 1.5-bit quantizer.

Table 4.4: Logic codification of the 1.5-bit quantizer.

I_{C1}	I_{C1}	State	$Dout_{L1}$	$Dout_{L2}$
0	0	x	0	0
0	1	+1	0	1
1	0	-1	1	0
1	1	0	0	0

4.3.2 Important Parameters in Operational Amplifiers

In the previous analysis it was assumed that the operational amplifiers were ideal, when real amplifiers are used the non-ideal effects can change the behavior of the modulator. In order to understand what is the required performance of the different parameters of the amplifiers, such as: gain-bandwidth product (GBW), slew rate and DC gain, the modulator circuit was simulated using a first order electrical model for the amplifiers. This model includes DC gain, a single pole and the slew rate effect. In these simulations the amplifier parameters were set to different values in order to determine the minimum required values for the different parameters.

To investigate the SNDR degradation due to the variation of the parameters of the operational amplifiers, different electrical simulations with variations in the DC gain, the GBW, and the slew rate were performed. In these simulations a first order model for the amplifier with a DC gain = 72 dB, a GBW = 50 MHz, and a slew rate = 10 V/μs was used. The output of the circuits was analyzed using a 2^{16} points FFT with a Blackman-Harris window, these results are shown in Figures (4.11, 4.12, and 4.13).

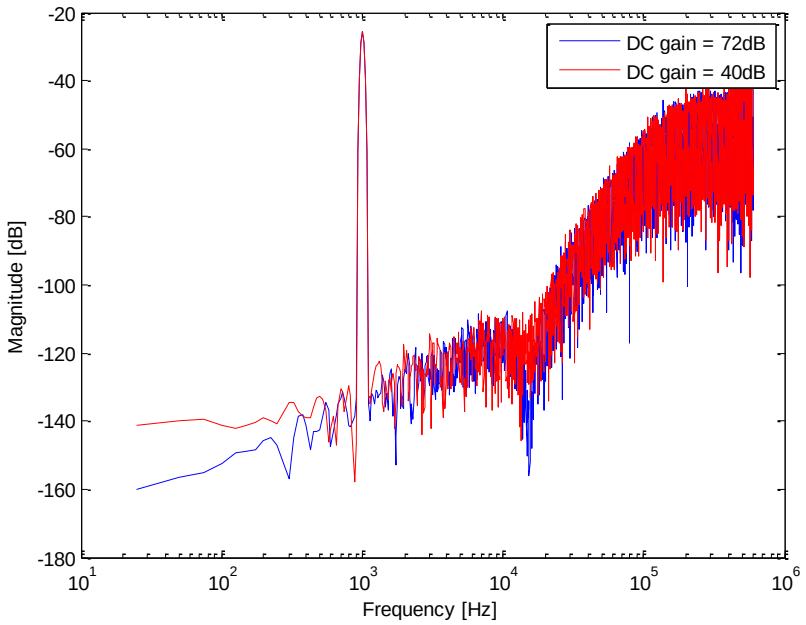


Figure 4.11: Influence of the DC gain in the output spectrum of the modulator (results obtained with electrical simulations with first order model amplifier with a GBW = 50 MHz, and a slew rate = 10 V/μs).

Observing Figure 4.11 it is clear that a reduction of the DC gain of the first amplifier causes a reduction of noise shaping at low frequencies. The reduction of the gain in the second and third operational amplifier decreases notch attenuation due to zeros in the NTF.

As it can be observed in Figure 4.12, the decrease of the GBW of the amplifiers decreases the frequency of the zeroes, resulting in added noise in the upper part of the signal band, therefore degrading the SNDR.

From Figure 4.13 it is possible to conclude that a low slew rate in the amplifier results in added distortion and a degradation of the notch produced by the zeroes.

These simulations show that if the amplifiers have a DC gain of 72 dB, a GBW of 50 MHz and a slew rate of 10 μV they do not affect the performance of the modulator significantly.

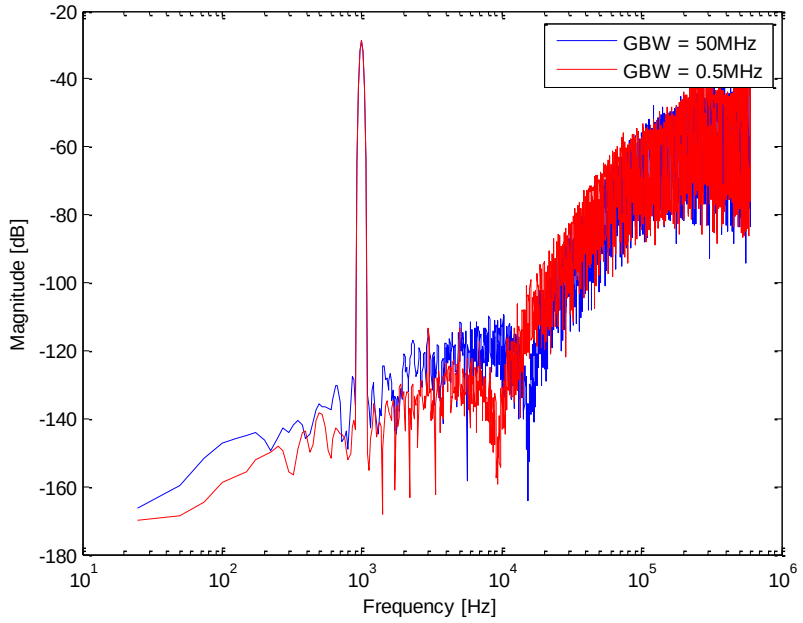


Figure 4.12: Influence of the GBW in the output spectrum of the modulator (results obtained with electrical simulations with first order model amplifier with a DC gain = 72 dB, and a slew rate = 10 V/μs).

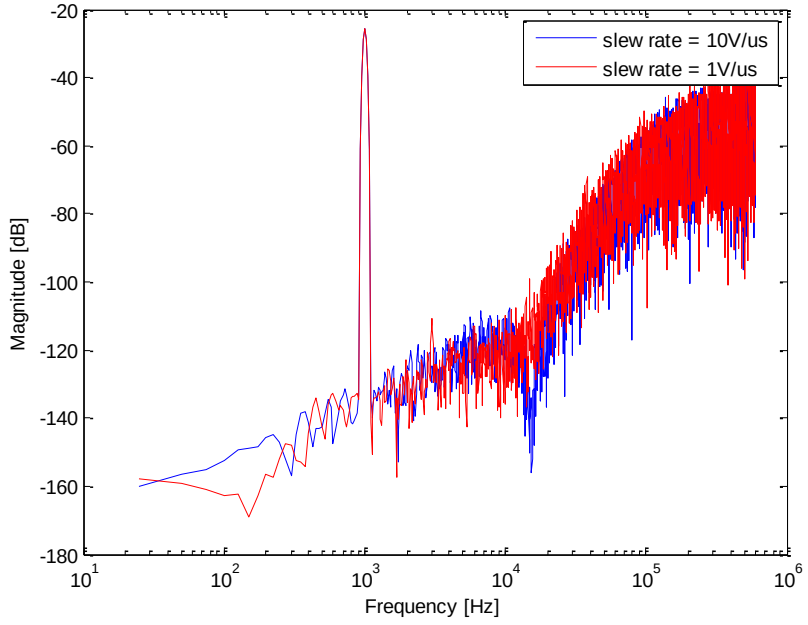
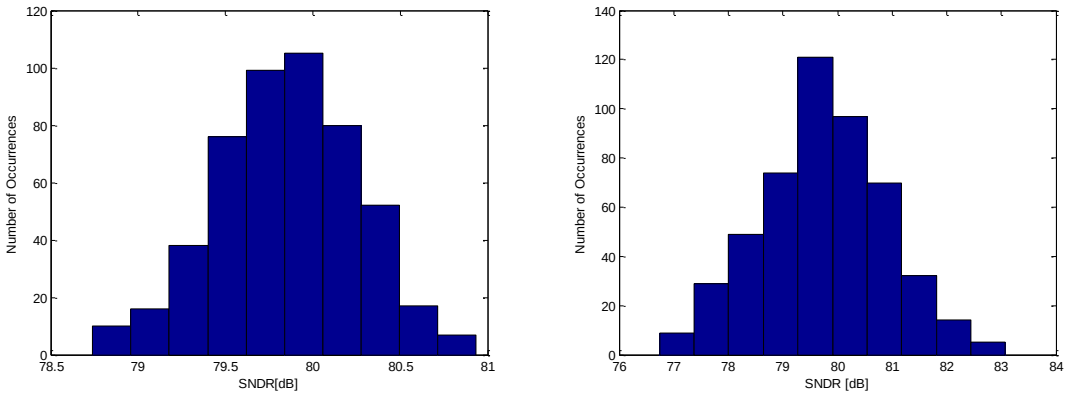


Figure 4.13: Influence of the slew rate in the output spectrum of the modulator (results obtained with electrical simulations with first order model amplifier with a DC gain = 72 dB, and a GBW = 50 MHz).

4.4 Monte Carlo Analysis of the Circuit

In order to verify the stability of the design, a 500 cases Monte Carlo analysis where the value of the components were randomly selected around the nominal values with a gaussian distribution with $3\sigma = 5\%$ and $3\sigma = 20\%$ for the capacitors and with $3\sigma = 1\%$ and $3\sigma = 5\%$ for the resistors.

Figure 4.14 shows the histograms of the SNDR values obtained in this analysis, and shows that the SNDR in worst case degrades about 1.4 dB (Figure 4.14a) due to components mismatch of $3\sigma_{\frac{\Delta R}{R}} = 1\%$ and $3\sigma_{\frac{\Delta C}{C}} = 5\%$ and in the order case degrades about 3 dB (Figure 4.14b) due to components mismatch of $3\sigma_{\frac{\Delta R}{R}} = 5\%$ and $3\sigma_{\frac{\Delta C}{C}} = 20\%$.



(a) $3\sigma_{\frac{\Delta R}{R}} = 1\%$ and $3\sigma_{\frac{\Delta C}{C}} = 5\%$ (b) $3\sigma_{\frac{\Delta R}{R}} = 5\%$ and $3\sigma_{\frac{\Delta C}{C}} = 20\%$

Figure 4.14: Histogram of the behavioral simulated SNDR of the proposed $\Sigma\Delta$ modulator with component values mismatch. Data obtained by running 500 Monte-Carlo simulations of the proposed architecture.

The output swing of the three integrators in the modulator was verified using behavioral simulations. The histogram of each output voltage is depicted in Figure 4.15, these histograms show that the output voltages are smaller than $\pm$ 1.5V, therefore the operational amplifiers should not approach saturation during the operation of the circuit.

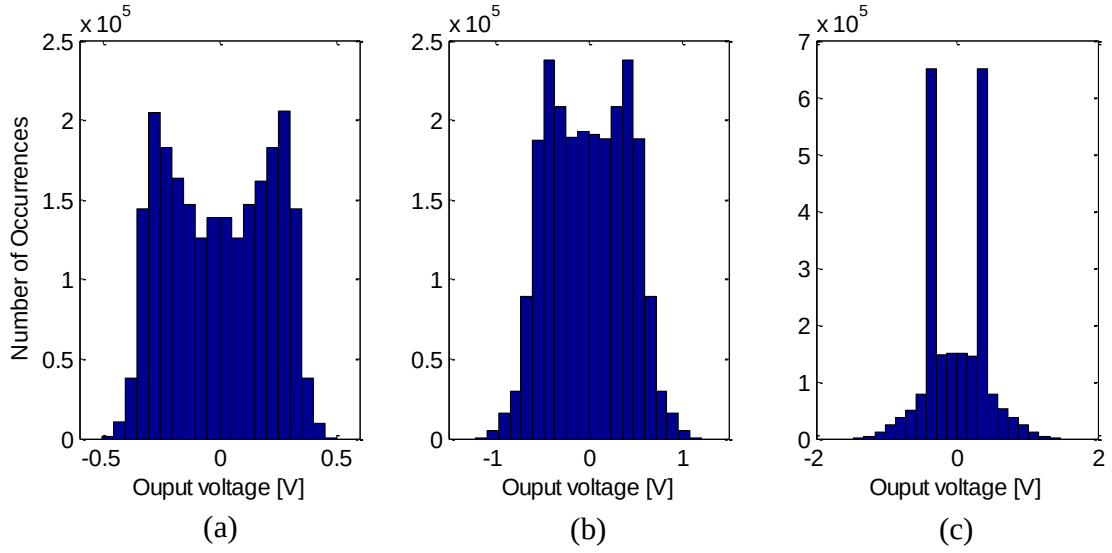


Figure 4.15: Histogram of the behavioral simulated output voltage of the (a) first integrator, (b) second integrator, and (c) third integrator for the proposed ΣΔ modulator.

4.5 Simulation Results

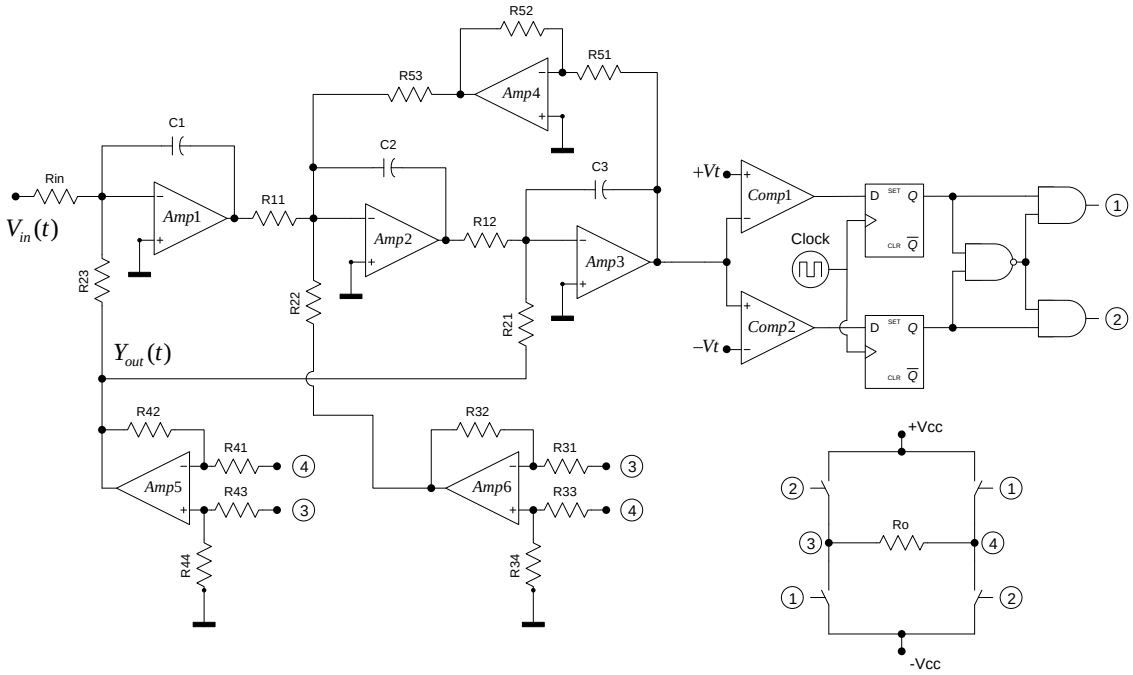


Figure 4.16: Class D audio amplifier implementation.

Figure 4.16 shows the circuit implementation of the proposed architecture. This

circuit was simulated using an electrical simulator and the output spectrum was calculated, this is shown in Figure 4.17 and in this case a maximum SNDR value of 80.1 dB was obtained. The electrical simulations used a first order model amplifier with a DC gain = 72 dB, a GBW = 50 MHz, and a slew rate = 10 V/μs.

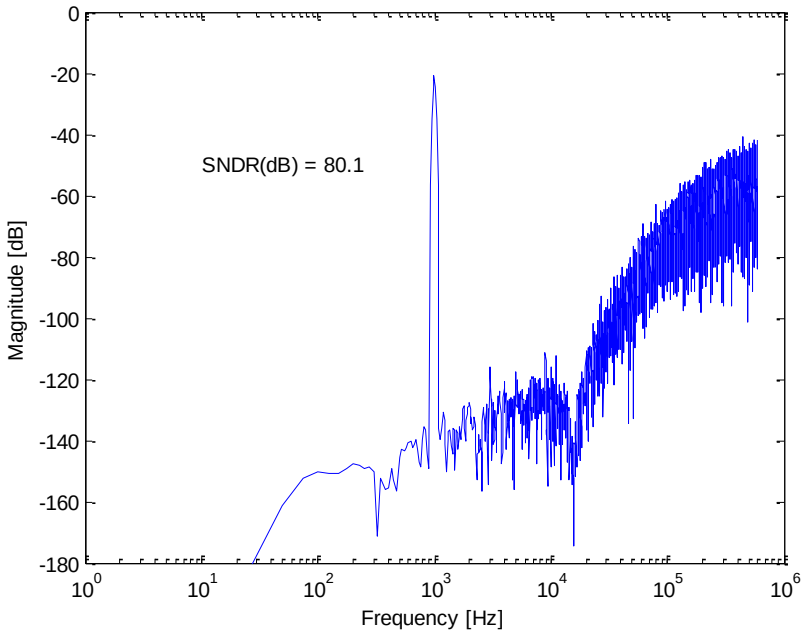


Figure 4.17: Output spectrum of the proposed architecture obtained with electrical simulations with first order model amplifier with a DC gain = 72 dB, a GBW = 50 MHz, and a slew rate = 10 V/μs (2^{16} points FFT using a Blackman-Harris window).

The simulations shows good results, either in tool $MATLAB®/SIMULINK®$ (80.2 dB) or in the electrical simulator (80.1 dB) and are virtually identical. However, it is necessary to have in account that the simulations in the tool $SIMULINK®$ were performed with noise and in the electrical simulator did not introduce any noise in the circuit.

In order to obtain the evolution of the SNDR of the modulator as a function of the input signal amplitude, several simulations were performed for input signal with different amplitude values and the SNDR value was calculated for each case. The measured SNDR as function of input level is shown in Figure 4.18 and this curve shows that the $\Sigma\Delta$ modulator has a dynamic range (DR) of about 77.5 dB and a

peak SNDR value of about 81.9 dB.

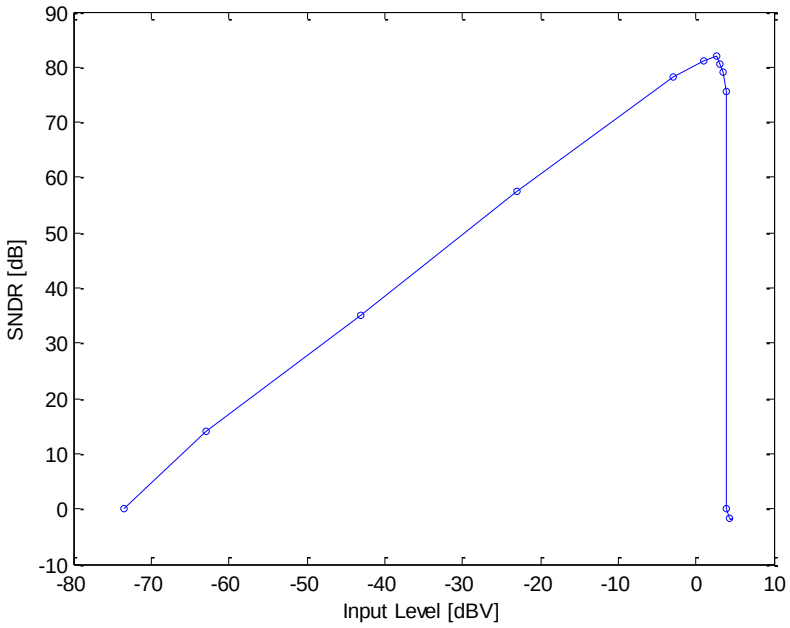


Figure 4.18: Measured SNDR as function of Input Level.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

A key motivation to use Class D amplifiers in many applications is the high efficiency. One of the main challenges in the design of class D amplifiers is designing the modulator circuit that encodes the input analogue signal into a switching sequence used to produce the output power signal. The new advancements in Class D modulation techniques have permitted Class D amplifiers to prosper in applications where linear amplifiers have dominated.

In the design of the modulator, and depending of the application, the choice of the order, the bandwidth, the clock frequency, and the components mismatch, are very important to limit the system cost and also for the performance of the amplifier.

The 3^{rd} order 1.5-bit $\Sigma\Delta$ modulator with distributed feedback and local resonator feedback for Class D audio amplifiers, proposed in this work, allows to improve the signal-to-noise-and-distortion ratio (SNDR), without increasing significantly the oversampling ratio (OSR) or the order of the modulator (not greater then 3), to achieve this, the modulator uses transmission zeros and 1.5-bit quantization. The electrical simulation results indicate that this proposed architecture can achieve a least 80 dB of a maximum SNDR value with a dynamic range (DR) of about 77.5

dB.

Table 5.1: Comparison of similar architectures.

Ref.	Architecture	BW[kHz]	SNR[dB]	DR[dB]	f_S[MHz]
[21]	3rd CT-ΣΔ 4-bit	24	92.5	93.5	3
[22]	3rd CT-ΣΔ 12-bit	25	66	81	2.4
[23]	3rd CT-ΣΔ 12-bit	25	73	80	2.4
[24]	3rd CT/DT-ΣΔ 4-bit	20	99	106	5.1
[25]	3rd CT-ΣΔ 4-bit	20	77	95	12
This work	3rd CT-ΣΔ 1.5-bit	18	80.1[1]	77.5	1.2

Analyzing the Table 5.1, this work has the lower sampling frequency, as desired, with a considerable SNDR.

5.2 Future Work

The implementation of the proposed architecture in PCB is the obvious future work. This implementation is important to confirm the good results obtained in the tool $MATLAB®/SIMULINK®$ as well in the electrical simulator. As future work, is also important, the study of new feedback topologies from the output stage and the speaker in order to improve the power supply rejection ratio (PSRR) and the total harmonic distortion (THD).

[1] SNDR - electrical simulator

Appendix A

SIMULINK Circuit

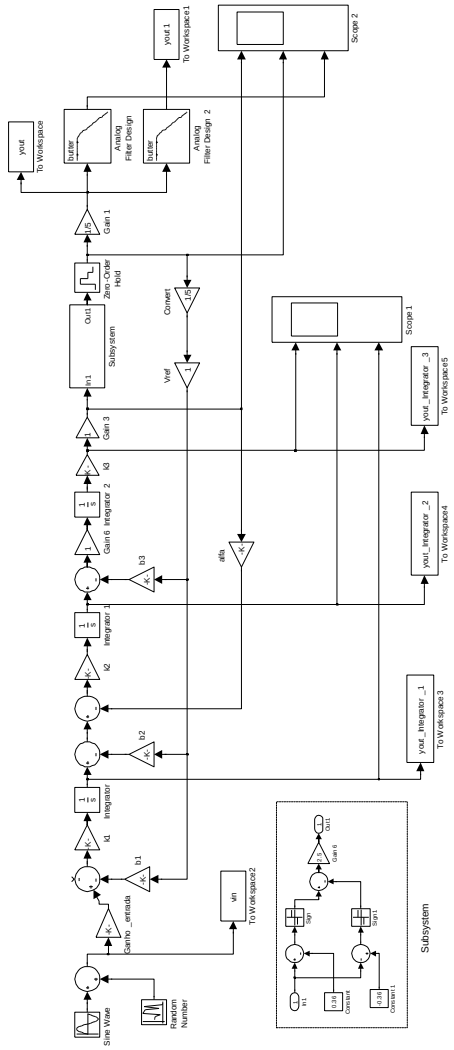


Figure A.1: Simulink circuit of the proposed architecture.

Appendix B

MATLAB Code

```
clear all;

%-------------------------------------------------------------------------
R_1_perc=[1.00  1.02  1.05  1.07  1.10  1.13  1.15  1.18  1.21  1.24  1.27...
          1.30  1.33  1.37  1.40  1.43  1.47  1.50  1.54  1.58  1.62  1.65...
          1.69  1.74  1.78  1.82  1.87  1.91  1.96  2.00  2.05  2.10  2.15...
          2.21  2.26  2.32  2.37  2.43  2.49  2.55  2.61  2.67  2.74  2.80...
          2.87  2.94  3.01  3.09  3.16  3.24  3.32  3.40  3.48  3.57  3.65...
          3.74  3.83  3.92  4.02  4.12  4.22  4.32  4.42  4.53  4.64  4.75...
          4.87  4.99  5.11  5.23  5.36  5.49  5.62  5.76  5.90  6.04  6.19...
          6.34  6.49  6.65  6.81  6.98  7.15  7.32  7.50  7.68  7.87  8.06...
          8.25  8.45  8.66  8.87  9.09  9.31  9.53  9.76];

R_5_perc=[1.0 1.1 1.2 1.3 1.5 1.6 1.8 2.0 2.2 2.4 2.7 3.0 3.3...
          3.6 3.9 4.3 4.7 5.1 5.6 6.2 6.8 7.5 8.2 9.1];

%-------------------------------------------------------------------------
Vin=1*sqrt(2);
Vref=1;
N=3;
Fs=1.2e6;
B=18e3;
osr=Fs/(2*B);

Vin_freq=2*pi*1000;

[b,a]=CHEBY2(N,58.5,(2*pi)*B*0.999,'high','s');


k=b(1);
b=b/k;

p=roots(a);
z=roots(b);

alfa=b(3);


Hs=tf(b,a)
figure(1)
subplot(2,2,1)
pzmap(Hs)
subplot(2,2,2)
impulse(Hs)

g=abs(freqs(b,a,[0 Fs/osr Fs/4 Fs/2]));

np=2^19;
i=1:np;
fi=0+i*2*pi*Fs/(np*2);
h=freqs(b,a,fi);
subplot(2,1,2)
semilogx(fi,20*log10(abs(h)))

text(10^-3,35,'Ganho da NTF a 0, osr, pi/4 e pi/2')
text(10^-3,15,num2str(g))

fi=0+i*1*pi*Fs/(np*osr);
```

```
h=freqs(b,a,fi);
noisedBV=10*log10(Vref^2/12*(1/((2*osr*np))*sum(h.*conj(h))));

text(1,-75,['Vnt=' num2str(noisedBV)])

%-------------------------------------------------------------------------
k1=Fs;
k2=Fs;
k3=Fs;

alfa=alfa/(k2*k3);

b1=(a(4))/(Vref*k1*k2*k3);
b2=((a(3))-alfa)/(Vref*k2*k3);
b3=a(2)/(Vref*k3);

Ganho_entrada=b1*(Vref/(2*Vin))*1;
k0=Ganho_entrada;

if 1==1
C1=1*10^(-9);
C2=1*10^(-9);
C3=1*10^(-9);

[R1,R2]=solve(['1/(' num2str(C1) '*R1)=' num2str(k1*k0)],...
   ['1/(' num2str(C1) '*R2)=' num2str(b1*k1)]);

[R3,R4,R5]=solve(['1/(' num2str(C2) '*R3)=' num2str(k2)],...
   ['1/(' num2str(C2) '*R4)=' num2str(b2*k2)],...
   ['1/(' num2str(C1) '*R5)=' num2str(alfa*k2)]);

[R6,R7]=solve(['1/(' num2str(C3) '*R6)=' num2str(k3)],...
   ['1/(' num2str(C3) '*R7)=' num2str(b3*k3)]);

end
%-------------------------------------------------------------------------


TR=0.05;
TC=0.20;

n_sim=1;


vect_sim=ones(1,n_sim);
for iaux = 1:n_sim;

if false %-----------------------------------------------------------
if true
R1=13.3e3;
R2=4.75e3;
R3=825;
R4=1.33e3;
R5=124e3;
R6=825;
R7=750;

end
```

```
b1=1/(C1*(1+randn/3*TC)*R2*(1+randn/3*TR)*k1);
b2=1/(C1*(1+randn/3*TC)*R4*(1+randn/3*TR)*k2);
b3=1/(C1*(1+randn/3*TC)*R7*(1+randn/3*TR)*k3);
alfa=1/(C1*(1+randn/3*TC)*R5*(1+randn/3*TR)*k2);

Ganho_entrada=b1*(Vref/(2*Vin));

end %-------------------------------------------------------------


open_system('SD_3_zero_move_1ponto5_Bit.mdl');
set_param('SD_3_zero_move_1ponto5_Bit/Sine Wave','Amplitude',num2str(double(Vin)))
set_param('SD_3_zero_move_1ponto5_Bit/Sine Wave','Frequency',num2str(double(Vin_freq)))

set_param('SD_3_zero_move_1ponto5_Bit/Ganho_entrada','Gain',num2str(double↙
(Ganho_entrada)));

set_param('SD_3_zero_move_1ponto5_Bit/k1','Gain',num2str(double(k1)))
set_param('SD_3_zero_move_1ponto5_Bit/k2','Gain',num2str(double(k2)))
set_param('SD_3_zero_move_1ponto5_Bit/k3','Gain',num2str(double(k3)))

set_param('SD_3_zero_move_1ponto5_Bit/b1','Gain',num2str(double(b1)))
set_param('SD_3_zero_move_1ponto5_Bit/b2','Gain',num2str(double(b2)))
set_param('SD_3_zero_move_1ponto5_Bit/b3','Gain',num2str(double(b3)))
set_param('SD_3_zero_move_1ponto5_Bit/alfa','Gain',num2str(double(alfa)))
set_param('SD_3_zero_move_1ponto5_Bit/Zero-Order Hold','sample time',num2str(double↙
(1/Fs)))

set_param('SD_3_zero_move_1ponto5_Bit/Vref','Gain',num2str(double(Vref)))
%-------------------------------------------------------------------------

n_sim=1;

vect_sim22=ones(1,n_sim);
vect_sim2=ones(1,n_sim);


for iaux2= 1:n_sim

%valor=0.2+iaux2/2500;
%vect_sim22(iaux2)=valor;
valor=0.36;

%valor= 0.36 + (randn/3)* 0.01; %10mV
set_param('SD_3_zero_move_1ponto5_Bit/Subsystem/Constant','value',num2str(double↙
(valor)))

%valor= 0.36 + (randn/3)* 0.01; %10mV
set_param('SD_3_zero_move_1ponto5_Bit/Subsystem/Constant1','value',num2str(double(-↙
valor)))

sim('SD_3_zero_move_1ponto5_Bit')

%-------------------------------------------------------------------------
np=max(size(yout.signals.values));
yf=fft(yout.signals.values.*blackmanharris(np));
yp=yf.*conj(yf)/np^2;
f=(1:np)*Fs/np;
[value,index]=max(yp(1:np/osr));
```

```
Ps=sum(yp(index-4:index+4));
PN=sum(yp(1:np/(2*osr)))-Ps;

SNRteorica=10*log10(Vin^2/2)-noisedBV;
SNRsim=10*log10(Ps/PN)

vect_sim(iaux)=SNRsim;
vect_sim2(iaux2)=SNRsim;
end

end

%------------------------------------------------------------------------
figure(2)
semilogx(f(1:end/2),10*log10(yp(1:end/2)),'b')

text(10,-50,['SNDR(dB) = ' num2str(SNRsim,3)])

XLABEL('Frequency [Hz]')
YLABEL('Magnitude [dB]')

AXIS([1 10^6 -200 0]);
```

Appendix C

Cadence Virtuoso Spectre Circuits

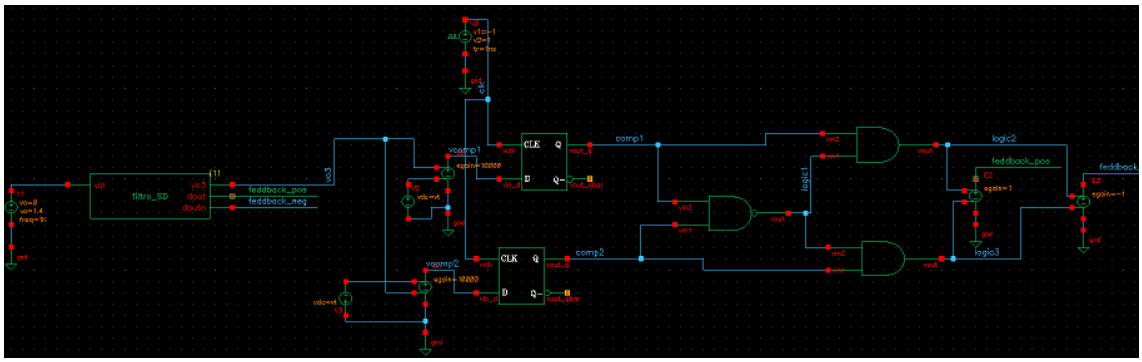


Figure C.1: Proposed architecture.

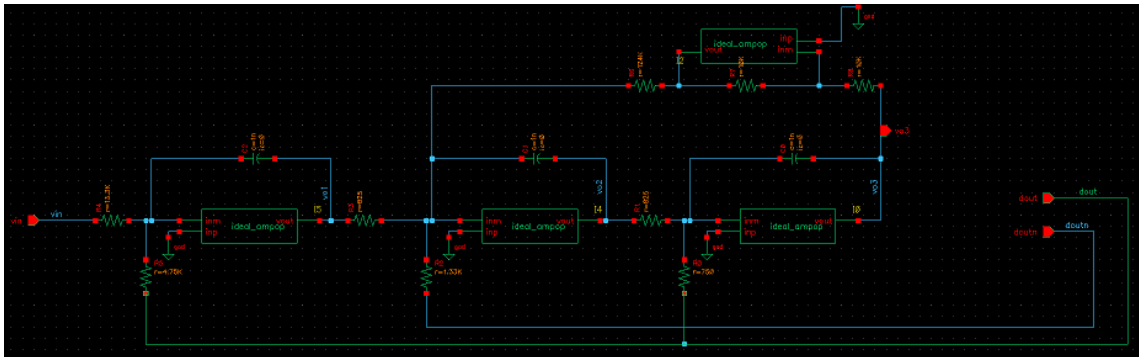


Figure C.2: Filter of the proposed architecture.

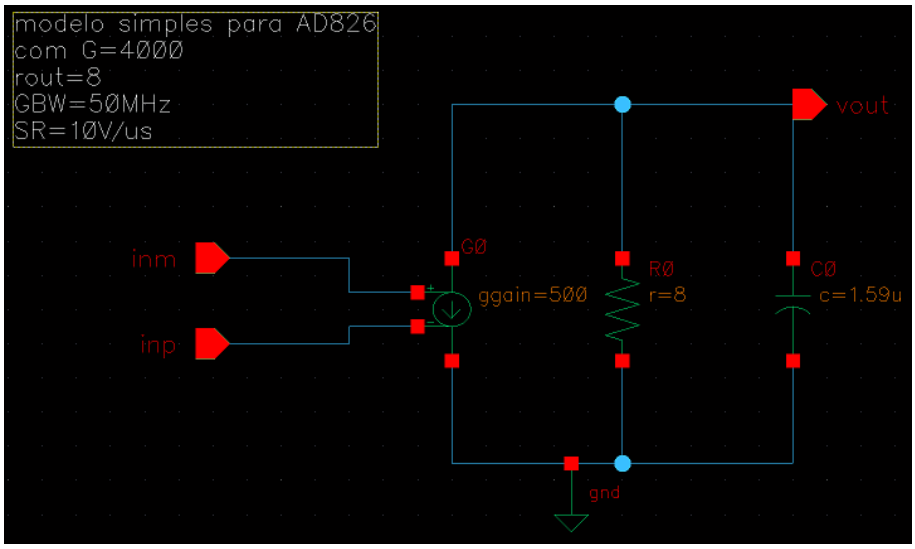


Figure C.3: Operational amplifier.

Appendix D

Published Papers

D.1 MIXDES'10

A 3rd Order 1.5-bit Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) Modulator Optimized for Class D Audio Power Amplifier

MIXDES 2010, 17th International Conference

A 3rd Order 1.5-bit Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) Modulator Optimized for Class D Audio Power Amplifier

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***Abstract*—This paper presents a 3rd order 1.5-bit $\Sigma\Delta$ modulator with distributed feedback and local resonator feedback for a Class D audio amplifier. In order to improve the signal-to-noise-and-distortion ratio (SNDR), without increasing the oversampling ratio (OSR) or the order of the modulator, the modulator uses transmission zeros and 1.5-bit quantization. High level simulations of the modulator show that it has a maximum SNDR value of 82.4 dB and a dynamic range (DR) of 76 dB, for a signal bandwidth of 18 kHz and a sampling frequency of 1.2 MHz. The use of a full-bridge output stage allows 1.5-bit quantization.**

***Index Terms*—Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$), Class D amplifier, Audio.**

I. Introduction

Due to the major concerns of global sustainability, there is a growing need for energy saving. The energy efficiency of audio amplifiers can be an important contribution to this end.

The traditional Class AB continuous-time power amplifiers have a maximum theoretical efficiency of 78.5% [1] while Class D amplifiers can approach 100% in theory. The efficiency advantage of the Class D amplifiers is irrefutable and, through this trait, switching-amplifier topologies have earned much of their market share. The basic idea of a Class D amplifier is that the devices of the output stage work as switches, therefore, under ideal conditions, the power dissipation of the output devices is zero (because when the device is ON its current is large but its voltage is zero). In order for a Class D amplifier to work it is necessary to transform the input analog signal into a digital signal that controls the switching of the output devices.

Sigma-Delta ($\Sigma\Delta$) modulators are the most suitable A/D converters for low-frequency, high-resolution applications, in view of their inherent linearity, reduced anti-aliasing filtering requirements and robust analog implementation. Moreover, by trading speed for accuracy, $\Sigma\Delta$ modulators allow high performance to be achieved with low sensitivity to analog component imperfections and without requiring component trimming [2].

This paper describes a 3rd order 1.5-bit continuous-time (CT) $\Sigma\Delta$ modulator with distributed feedback and local resonator feedback intended for use in a Class D full-bridge audio power amplifier, in order to obtain a large SNDR value while using a moderately low switching frequency. The use of local resonator feedback in the modulator, allows to implement a Chebyshev type II filter, which results in a large SNDR value even for a low oversampling ratio (OSR) value. The use of 1.5-bit in the quantizer can eliminate some the inherent drawbacks of a binary switching scheme. With this technique, the output stage provides current to load only when needed, and the switching activity of output stage is greatly reduced, especially when input signal has a small amplitude value. These features increase the power efficiency of the amplifier [3].

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II. Class D Amplifiers

Typically, a Class D amplifier (Figure 1) consists of two stages. The first stage is a signal processing stage that converts the input audio signal into a two-level (1-bit) signal. This two-level signal represents a Pulse-Width Modulation (PWM) signal or a Pulse-Density Modulation (PDM) signal. The second stage of the amplifier is a power output stage, in which the two-level signal drives the output power MOSFETs (half-bridge or full-bridge).

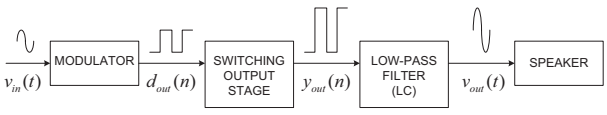

Fig. 1. Class D open-loop-amplifier block diagram.

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low V_{DS} when they are conducting current, thus resulting in a smaller power dissipation $(V_{DS} \times I_{DS})$ in the amplifier. Due to the binary switching of the output devices of the amplifier, therefore the output signal of the amplifier contains high frequency components. These components must be filtered in order to reduce the electromagnetic energy radiated by the amplifier, typically, a LC filter is used for this function.

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- Modulation techniques
- EMI
- LC filter design
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The obvious shortcoming of this circuit is the variability of the switching frequency in function of the power supply voltage. A minor modification is to use the switching waveform itself as the hysteresis feedback. Amplifiers constructed along these lines typically produce fairly respectable performance, accounting for the popularity of this arrangement. This still leaves two rather serious drawbacks. The most important problem is the lack of control over the output filter. The other is that the minimum pulse width produced is only half that of the idle pulse width [4].

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The output stage of the Class D amplifiers are usually implemented using two topologies: half-bridge or full-bridge (depicted in Figure 2) configurations. Each topology has advantages and disadvantages. In brief, a half-bridge is potentially simpler and requires a simpler low pass filter, however the current drawn from the power supplies is signal dependent and therefore a signal replica can appear in the power supply voltages which can cause distortion. In order to reduce this effect it is necessary to filter the signal from the power supply using large decoupling capacitors. The full-bridge topology requires two half-bridge amplifiers and a more complicated output filter. The full-bridge draws a constant current from the power supply and therefore does not introduce the signal in the power supply, which improves the circuit performance and simplifies the design of the power supply circuit [5].

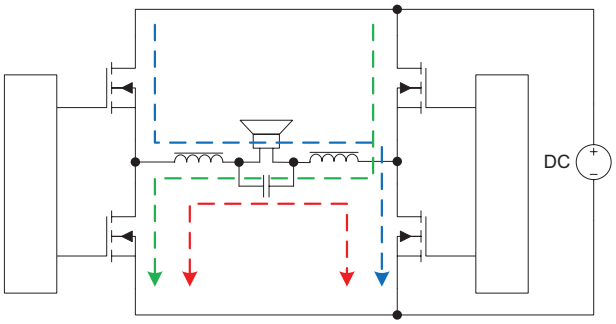

Fig. 2. Differential switching output stage with LC low-pass filter.

D. EMI Considerations

The high-frequency components of the switching signal in a Class D amplifier outputs requires serious consideration. If not properly understood and managed, these components can generate large amounts of electromagnetic interference (EMI) and disrupt operation of other equipment.

The EMI can have two sources of origin: signals that are radiated into space and those that are conducted via speaker and power-supply wires. A useful principle is to minimize the area of loops that carry high-frequency currents, since the strength of associated EMI is related to loop area and the proximity of loops to other circuits [6]. The amount of power radiated from these loops is dependent of the loop area when compared to the wavelength of the signals, therefore it is also important to reduce the maximum frequency of the signals in the amplifier. This means that it is very important to use a switching frequency as low as possible, corresponding to using a low OSR in the $\Sigma\Delta$ modulator.

III. 3RD ORDER CONTINUOUS-TIME (CT) ΣΔ MODULATOR

The first step in the design of the modulator is choosing the order modulator and the clock frequency value.(ΣΔ) modulators of orders higher than 2 are possible to design but they cannot simply be made by adding further stages because the resulting system would, most likely, be unstable. In view of this problem, the design procedure for finding the optimal 3rd ΣΔ modulator coefficients was based on the described in [7]. Briefly, this methodology describes an empirical method based on ordinary filter design that can be used to design high-order loops.

The sensitivity of the human ear is biased toward the lower end of the audible frequency spectrum, around 3 kHz. Being 50 Hz, the bottom end of the spectrum, and being 17 kHz, the top end, the sensitivity of the ear is down by approximately 50 dB on that at 3 kHz [8]. Taking advantage of these features of the ear and considering that most people will not be able to hear above 16 kHz, the bandwidth of an audio amplifier, in reality, does not need to be higher than 18 kHz. Therefore the modulator will be designed to have a signal bandwidth of 18 kHz and a peak SNDR value larger than 80 dB (the SNDR is defined for a bandwidth of 18 kHz).

As previously stated, it very important to use a low sampling frequency value in order to reduce the EMI of the amplifier and also to avoid non-ideal effects in the output devices during the switching. A ideal 3rd ΣΔ modulator (assuming that will be stable) with an OSR value of 32 could theoretically produce an SNDR value of around 95 dB. Therefore a sampling frequency value of 1.2 MHz is selected, resulting in a OSR about 33.3.

However, due to the inherent instability of the modulator it is necessary to use a transfer function that limits the noise shaping resulting in a lower SNDR value. Therefore, several architecture options for the modulator in order to improve the SNDR value, will be studied.

A. 1-bit with Distributed Feedback

The block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback, implemented using CT integrators, is shown in Figure 3. The signal transfer function (STF) of this structure is given by Equation 1 and will be essentially a 3rd order Butterworth low pass filter. The cut-off frequency of this filter function is selected in order to limit the maximum gain of the NTF and eliminate the instability of the modulator.

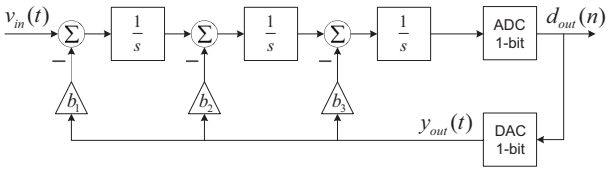

Fig. 3. Block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback.

The noise transfer function (NTF) given by Equation 2 was designed to be a 3rd order Butterworth high-pass filter with a cut-off frequency of 99.6 kHz. The values of the coefficients b_1, b_2 and b_3 were calculated in order to implement the selected Butterworth transfer function. The modulator was simulated using $SIMULINK^{®}$. Each simulation was calculated using 2^{19} points and a fast Fourier transformation using a Blackman-Harris window was applied.

$$STF = \frac{1}{s^3 + s^2 \cdot b_3 + s \cdot b_2 + b_1} \tag{1}$$

$$NTF = \frac{s^3}{s^3 + s^2 \cdot b_3 + s \cdot b_2 + b_1} \tag{2}$$

Figure 4 shows the output spectrum of the traditional 3rd order 1-bit ΣΔ modulator, obtained by simulation, in this case a maximum SNDR value of 64.2 dB was obtained. The frequency of the sine wave input signal is 1 kHz.

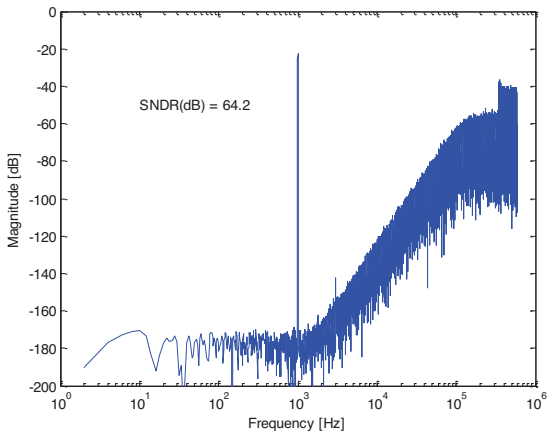

Fig. 4. Output spectrum of the 3rd order 1-bit ΣΔ modulator with distributed feedback (2^{19} points FFT using a Blackman-Harris window).

B. 1-bit with Distributed Feedback and Local Resonator Feedback

One technique to improve the SNDR is to optimally distribute the zeros of NTF inside the signal bandwidth, unlike the traditional design described above where NTF zeros are all placed at DC. The architecture shown in Figure 5 allows distributing the zeros of NTF inside the signal bandwidth and can be designed using a Chebyshev type II filter, in this case the stopband edge frequency of the filter is 18 kHz. The coefficients b_1, b_2 and b_3 fix the position of the poles and α the position of the zeros of the NTF (Equation 4). Note that the zeros do not appear in the STF (Equation 3).

$$STF = \frac{1}{s^3 + s^2 \cdot b_3 + s \cdot (\alpha + b_2) + b_1} \tag{3}$$

$$NTF = \frac{s \cdot (s^2 + \alpha)}{s^3 + s^2 \cdot b_3 + s \cdot (\alpha + b_2) + b_1} \tag{4}$$

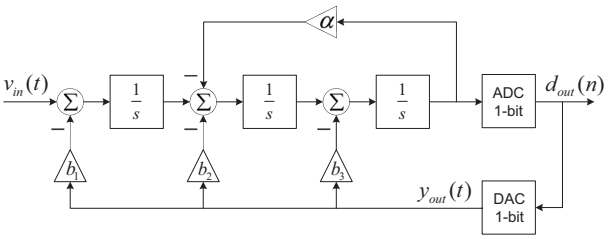

Fig. 5. Block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback.

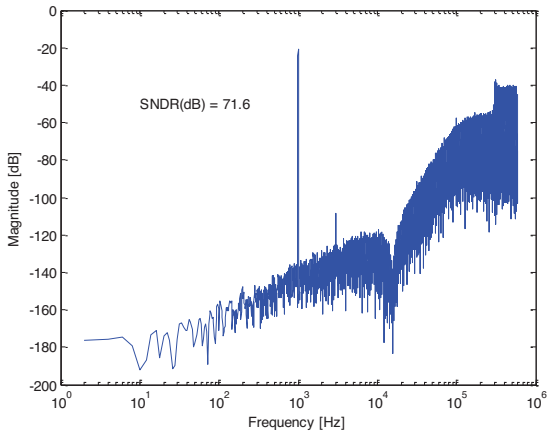

Fig. 6. Output spectrum of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback (2^{19} points FFT using a Blackman-Harris window).

The Figure 6 shows the output spectrum of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback, obtained by simulation, in this case a maximum SNDR value of 71.6 dB was obtained. As expected, the shift of the zeros from DC to the signal bandwidth improved the maximum SNDR value.

C. 1.5-bit with Distributed Feedback

Another option to improve the SNDR is use a 1.5-bit quantizer (corresponding to three-level quantization) instead of 1-bit quantizer. The increase of the resolution of the quantizer improves the linearity of the feedback in the modulator. Since this results in a more stable loop, it is possible to use a larger cut-off frequency in the modulator and therefore improve the maximum SNDR value. In this case a cut-off frequency of 133.2 kHz was used. The use of three levels also reduces unnecessary switching of the full-bridge output stage so that the switching loss is minimized.

Figure 8 shows the simulated output spectrum of the 3rd order 1-bit ΣΔ modulator with a 1.5-bit quantizer, in this case a maximum SNDR value of 77.3 dB was obtained. As expected the increase in the resolution of the quantizer improved the maximum SNDR value of the modulator.

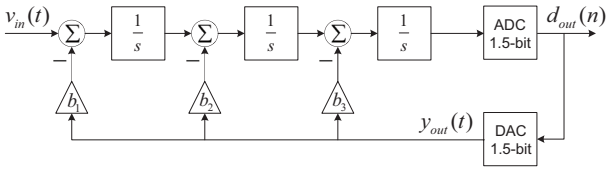

Fig. 7. Block diagram of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback.

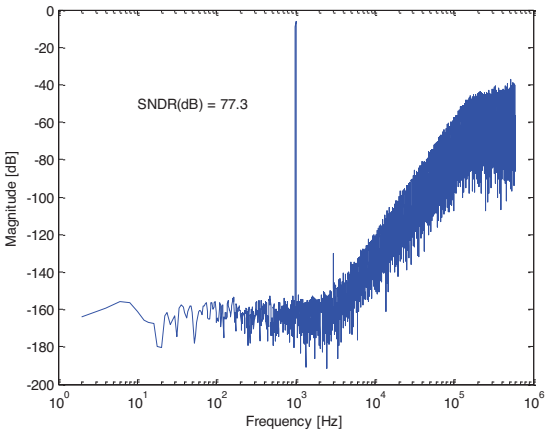

Fig. 8. Output spectrum of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback (2^{19} points FFT using a Blackman-Harris window).

IV. Proposed ΣΔ Modulator

In order to obtain a maximum SNDR value larger than 80 dB, the topologies described above (3rd order 1-bit ΣΔ with distributed feedback and local resonator feedback and the 3rd order 1.5-bit ΣΔ with distributed feedback) were combined into one modulator (Figure 9). The loop filter in the modulator was designed to have a stopband edge frequency of 18 kHz.

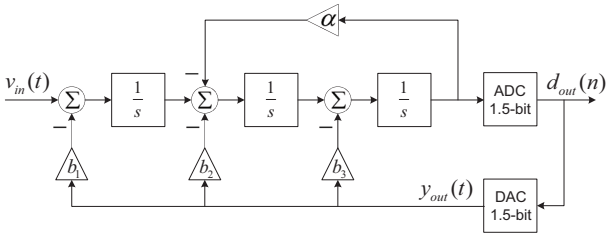

Fig. 9. Block diagram of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback.

Figure 10 shows the output spectrum of the modulator, obtained by simulation, in this case a maximum SNDR value of 82.4 dB was obtained. The combination of all the previous techniques allowed to obtain a maximum SNDR value larger than 82.4 dB using a 3rd order ΣΔ modulator with an OSR value of approximately 32.

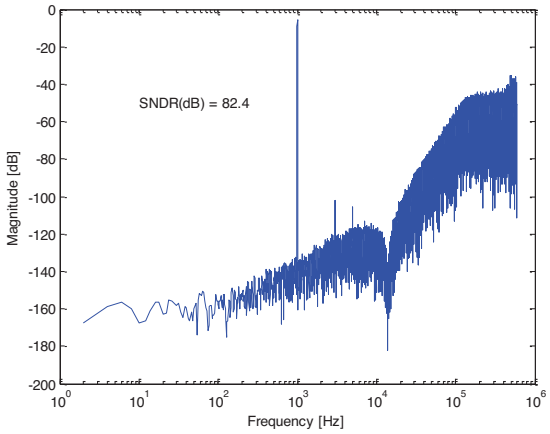

Fig. 10. Output spectrum of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback (2^{19} points FFT using a Blackman-Harris window).

In order to obtain the evolution of the SNDR of the modulator as a function of the input signal amplitude, several simulations were performed for input signal with different amplitude values and the SNDR value was calculated for each case. The measured SNDR as function of input level is shown in Figure 11 and this curve shows that the ΣΔ modulator has a dynamic range (DR) of about 76 dB.

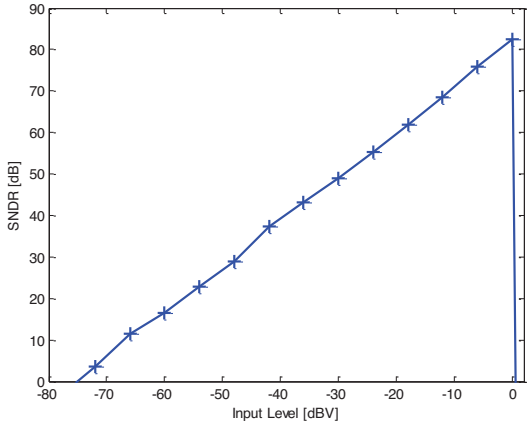

Fig. 11. Measured SNDR as function of Input Level.

V. Conclusion

This paper presents a 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback for a Class D audio amplifier. In order to improve the SNDR, without increasing the OSR or the order of the modulator (not greater then 3), the modulator uses transmission zeros and 1.5-bit quantization. High level simulations of the modulator show that it has a maximum SNDR value of 82.4 dB and a dynamic range of 76 dB, for a signal bandwidth of 18 kHz and a sampling frequency of 1.2 MHz. The increase of the resolution of the quantizer (1.5-bit quantizer instead of 1-bit quantizer) improves the linearity of the feedback in the modulator. Since this results in a more stable loop, it is possible to increase the stopband ripple in the modulator and therefore improve the maximum SNDR value.

Acknowledgment

This work was supported by the Portuguese Foundation for Science and Technology (FCT/MCTES) (CTS multiannual funding) through the PIDDAC Program funds.

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International Journal of Microelectronics and Computer Science

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João de Melo, *Student Member, IEEE,* and Nuno Paulino, *Member, IEEE*

***Abstract*—This paper presents a 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback for a Class D audio amplifier. In order to improve the signal-to-noise-and-distortion ratio (SNDR), without increasing the oversampling ratio (OSR) or the order of the modulator, the modulator uses transmission zeros and 1.5-bit quantization. High level simulations of the modulator architecture show that it has a maximum SNDR value of 81 dB, for a signal bandwidth of 18 kHz and a sampling frequency of 1.2 MHz. An electrical circuit is designed to implement the proposed architecture and the electrical simulations show that it has a maximum SNDR value of 76.1 dB. The influence of the constituting blocks of the circuit in the performance of the modulator is investigated using electrical simulations.**

***Index Terms*—Continuous-Time (CT) Sigma-Delta (ΣΔ), Class D amplifier, Audio.**

I. Introduction

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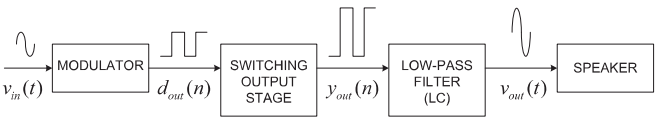

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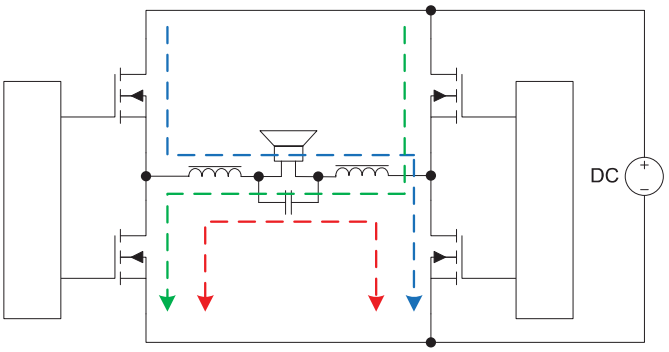

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D. EMI Considerations

The high-frequency components of the switching signal in a Class D amplifier outputs requires serious consideration. If not properly understood and managed, these components can generate large amounts of electromagnetic interference (EMI) and disrupt operation of other equipment.

The EMI can have two sources of origin: signals that are radiated into space and those that are conducted via speaker and power-supply wires. A useful principle is to minimize the area of loops that carry high-frequency currents, since the strength of associated EMI is related to loop area and the proximity of loops to other circuits [6]. The amount of power radiated from these loops is dependent of the loop area when compared to the wavelength of the signals, therefore it is also

important to reduce the maximum frequency of the signals in the amplifier. This means that it is very important to use a switching frequency as low as possible, corresponding to using a low OSR in the ΣΔ modulator.

III. 3RD Order Continuous-Time (CT) ΣΔ Modulator

The first step in the design of the modulator is choosing the order modulator and the clock frequency value.(ΣΔ) modulators of orders higher than 2 are possible to design but they cannot simply be made by adding further stages because the resulting system would, most likely, be unstable. In view of this problem, the design procedure for finding the optimal 3rd ΣΔ modulator coefficients was based on the described in [4]. Briefly, this methodology describes an empirical method based on ordinary filter design that can be used to design high-order loops.

The sensitivity of the human ear is biased toward the lower end of the audible frequency spectrum, around 3 kHz. Being 50 Hz, the bottom end of the spectrum, and being 17 kHz, the top end, the sensitivity of the ear is down by approximately 50 dB on that at 3 kHz [7]. Taking advantage of these features of the ear and considering that most people will not be able to hear above 16 kHz, the bandwidth of an audio amplifier, in reality, does not need to be higher than 18 kHz. Therefore the modulator will be designed to have a signal bandwidth of 18 kHz and a peak SNDR value larger than 80 dB (the SNDR is defined for a bandwidth of 18 kHz).

As previously stated, it very important to use a low sampling frequency value in order to reduce the EMI of the amplifier and also to avoid non-ideal effects in the output devices during the switching. A ideal 3rd ΣΔ modulator (assuming that will be stable) with an OSR value of 32 could theoretically produce an SNDR value of around 95 dB. Therefore a sampling frequency value of 1.2 MHz is selected, resulting in a OSR about 33.3.

However, due to the inherent instability of the modulator it is necessary to use a transfer function that limits the noise shaping resulting in a lower SNDR value. Therefore, several architecture options for the modulator in order to improve the SNDR value, will be studied.

A. 1-bit with Distributed Feedback

The block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback, implemented using CT integrators, is shown in Figure 3. The signal transfer function (STF) of this structure is given by Equation 1 and will be essentially a 3rd order Butterworth low pass filter. The cut-off frequency of this filter function is selected in order to limit the maximum gain of the NTF and eliminate the instability of the modulator.

The noise transfer function (NTF) given by Equation 2 was designed to be a 3rd order Butterworth high-pass filter with a cut-off frequency of 99.6 kHz. The values of the coefficients b_1, b_2 and b_3 were calculated in order to implement the selected Butterworth transfer function. The modulator was simulated using $SIMULINK^{®}$. Each simulation was calculated using 2^{19} points and a fast Fourier transformation using a Blackman-Harris window was applied.

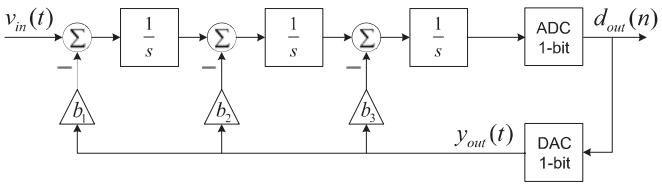

Fig. 3. Block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback.

$$STF = \frac{1}{s^3 + s^2 \cdot b_3 + s \cdot b_2 + b_1} \tag{1}$$

$$NTF = \frac{s^3}{s^3 + s^2 \cdot b_3 + s \cdot b_2 + b_1} \tag{2}$$

Figure 4 shows the output spectrum of the traditional 3rd order 1-bit ΣΔ modulator, obtained by simulation, in this case a maximum SNDR value of 64.2 dB was obtained. The frequency of the sine wave input signal is 1 kHz.

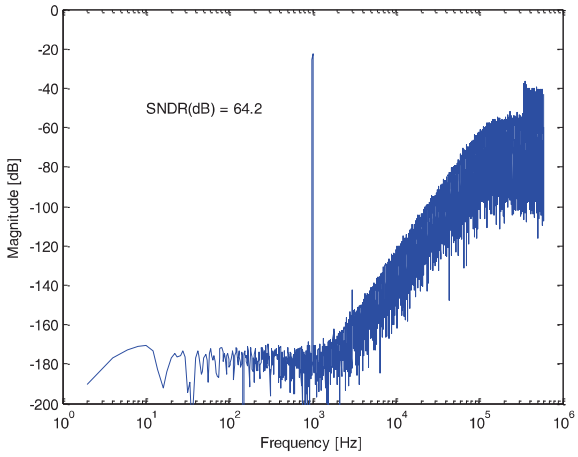

Fig. 4. Output spectrum of the 3rd order 1-bit ΣΔ modulator with distributed feedback (2^{19} points FFT using a Blackman-Harris window).

B. 1-bit with Distributed Feedback and Local Resonator Feedback

One technique to improve the SNDR is to optimally distribute the zeros of NTF inside the signal bandwidth, unlike the traditional design described above where NTF zeros are all placed at DC. The architecture shown in Figure 5 allows distributing the zeros of NTF inside the signal bandwidth and can be designed using a Chebyshev type II filter, in this case the stopband edge frequency of the filter is 18 kHz. The coefficients b_1, b_2 and b_3 fix the position of the poles and α the position of the zeros of the NTF (Equation 4). Note that the zeros do not appear in the STF (Equation 3).

$$STF = \frac{1}{s^3 + s^2 \cdot b_3 + s \cdot (\alpha + b_2) + b_1} \tag{3}$$

$$NTF = \frac{s \cdot (s^2 + \alpha)}{s^3 + s^2 \cdot b_3 + s \cdot (\alpha + b_2) + b_1} \tag{4}$$

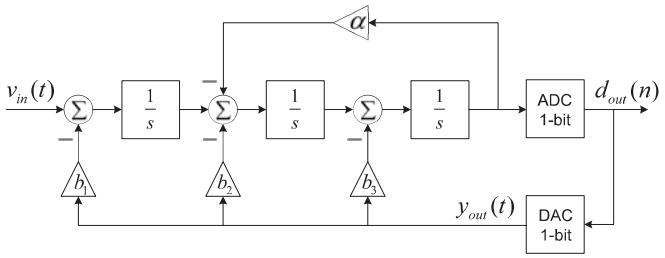

Fig. 5. Block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback.

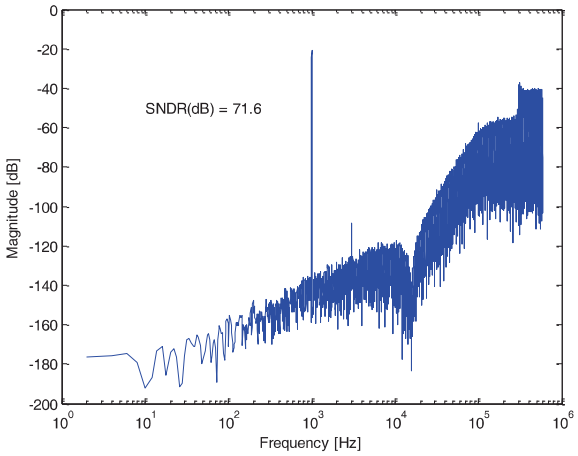

Fig. 6. Output spectrum of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback (2^{19} points FFT using a Blackman-Harris window).

The Figure 6 shows the output spectrum of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback, obtained by simulation, in this case a maximum SNDR value of 71.6 dB was obtained. As expected, the shift of the zeros from DC to the signal bandwidth improved the maximum SNDR value.

C. 1.5-bit with Distributed Feedback

Another option to improve the SNDR is use a 1.5-bit quantizer (corresponding to three-level quantization) instead of 1-bit quantizer. The increase of the resolution of the quantizer improves the linearity of the feedback in the modulator. Since this results in a more stable loop, it is possible to use a larger cut-off frequency in the modulator and therefore improve the maximum SNDR value. In this case a cut-off frequency of 133.2 kHz was used. The use of three levels also reduces unnecessary switching of the full-bridge output stage so that the switching loss is minimized.

Figure 8 shows the simulated output spectrum of the 3rd order 1-bit ΣΔ modulator with a 1.5-bit quantizer, in this case a maximum SNDR value of 76.9 dB was obtained. As expected the increase in the resolution of the quantizer improved the maximum SNDR value of the modulator.

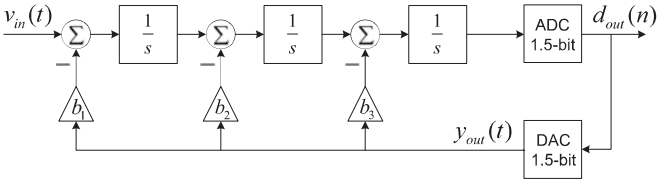

Fig. 7. Block diagram of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback.

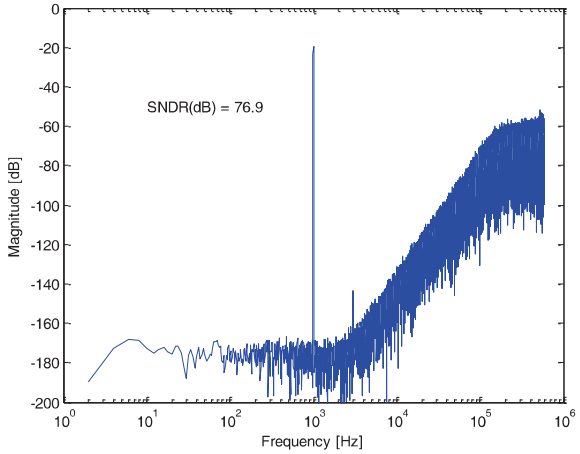

Fig. 8. Output spectrum of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback (2^{19} points FFT using a Blackman-Harris window).

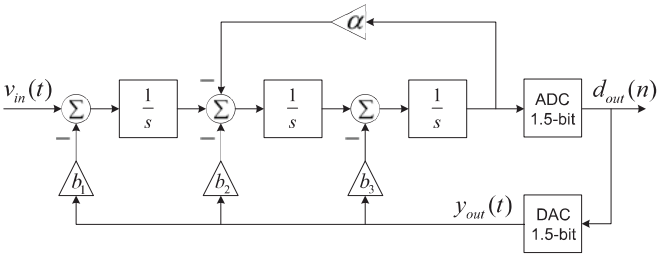

Fig. 9. Block diagram of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback.

IV. Proposed Architecture for the ΣΔ Modulator

In order to obtain a maximum SNDR value larger than 80 dB, the topologies described above (3rd order 1-bit ΣΔ with distributed feedback and local resonator feedback and the 3rd order 1.5-bit ΣΔ with distributed feedback) were combined into one modulator (Figure 9). The loop filter in the modulator was designed to have a stopband edge frequency of 18 kHz.

Figure 10 shows the output spectrum of the modulator, obtained by simulation, in this case a maximum SNDR value of 81 dB was obtained. The combination of all the previous techniques allowed to obtain a maximum SNDR value larger than 81 dB using a 3rd order ΣΔ modulator with an OSR value of approximately 32.

V. Circuit Design

It is necessary to design an electrical circuit that has the same behavior as the architecture that was developed

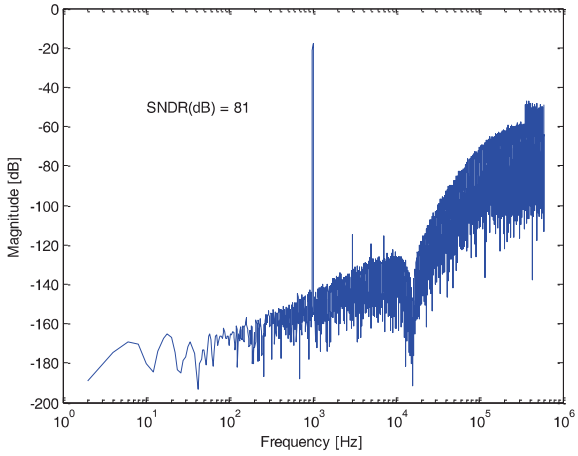

Fig. 10. Output spectrum of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback (2^{19} points FFT using a Blackman-Harris window).

in the previous section. During this design, as it will be explained next, it was realized that due to the variations of the components of the filter (capacitors, resistors, and operational amplifiers), the modulator circuit could become unstable. In order to increase the yield of the design it was necessary to reduce the gain of the NTF in order to make the modulator more stable.

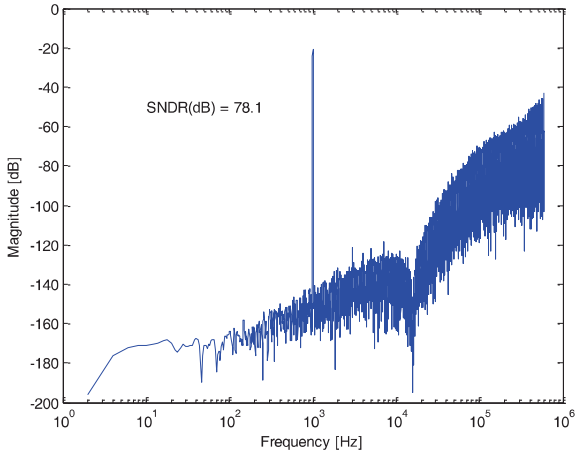

Fig. 11. The new output spectrum of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback (2^{19} points FFT using a Blackman-Harris window).

The modulator with the new NTF was simulated and the new output spectrum of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback is shown in Figure 11, in this case the maximum SNDR value is 78.1 dB, as expected, the added stability of the modulator resulted in a lower value for the SNDR. However, with increased stability margin due to reduced gain of the NTF, the harmonics are attenuated.

The Table I gives the coefficients values of the simulated architecture.

TABLE I
COEFFICIENTS OF THE PROPOSED ARCHITECTURE.

Coefficients					
k_0	$k_1 = k_2 = k_3$	b_1	b_2	b_3	α
0.0415	1	0.1173	0.4772	0.9701	0.0066

The Figure 12 shows a simple method to convert the mathematical model into the electrical model. Note that the T_S ($\frac{1}{F_S}$) is the period of the sampling frequency (F_S = 1.2 MHz).

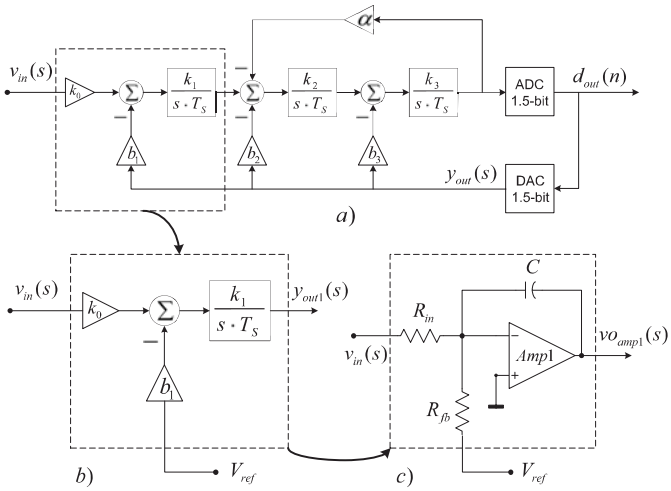

Fig. 12. Conversion of the mathematical model into the electrical model.

Analyzing the Figure 12.b) an equation for the $y_{out1}(s)$ can be written as:

$$y_{out1}(s) = \frac{k_0 \cdot k_1}{s \cdot T_S} \cdot v_{in}(s) - \frac{b_1 \cdot k_1}{s \cdot T_S} \cdot v_{ref}(s) \quad (5)$$

The equation for the output ($vo_{amp1}(s)$) of the integrator (depicted in Figure 12.c)) is given by:

$$vo_{amp1}(s) = \frac{1}{s \cdot R_{in} \cdot C} \cdot v_{in}(s) - \frac{1}{s \cdot R_{fb} \cdot C} \cdot v_{ref}(s) \quad (6)$$

Equaling Equation 5 to Equation 6 ($y_{out1}(s) = vo_{amp1}(s)$) is possible to obtain an expression for R_{in} and R_{fb}. Note that the operational amplifier is considered ideal in this approach.

$$R_{in} = \frac{T_S}{k_0 \cdot k_1 \cdot C} \quad (7)$$

$$R_{fb} = \frac{T_S}{b_1 \cdot k_1 \cdot C} \quad (8)$$

The same idea can be applied to the other integrators blocks of the modulator resulting in the modulator circuit shown in Figure 13. The values of the components can be obtained using the approach previously described, assuming that all the capacitors have a 1nF value.

Table II gives all passive component values for the modulator.

In order to confirm the correct design of the modulator, the STF (Figure 14) and NTF (Figure 15) of the modulator are

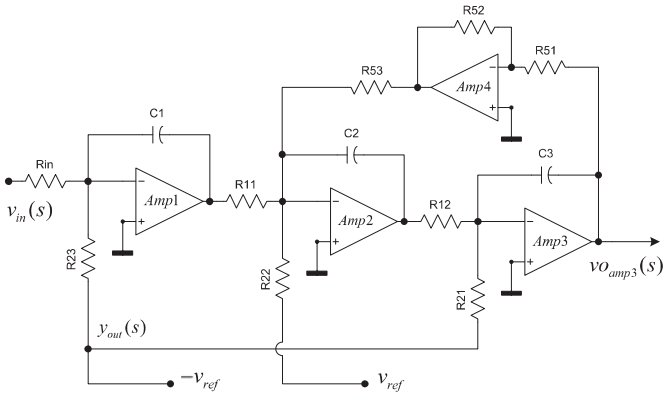

Fig. 13. Schematic design of the modulator.

TABLE II
SELECTED PASSIVE COMPONENT VALUES.

Components		
Id.	Value	Units
$C_1 = C_1 = C_1$	1	nF
R_{in}	20.5	kΩ
$R_{11} = R_{12}$	825	Ω
R_{21}	7.15	kΩ
R_{22}	1.74	kΩ
R_{23}	845	Ω
$R_{51} = R_{52}$	10	kΩ
R_{53}	127	kΩ

obtained by performing two AC simulations of the circuit of Figure 13.

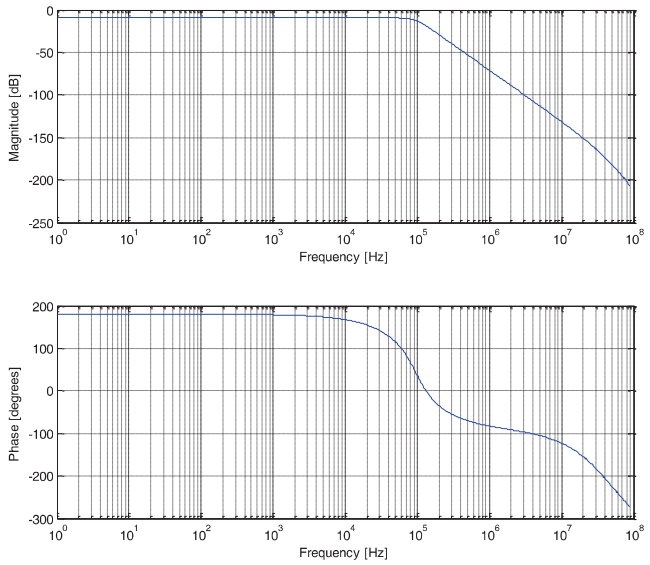

Fig. 14. Bode diagram of the STF of the modulator.

A. ADC Design

The 1.5-bit quantizer (three levels) is realized by two comparators and is showed in Figure 16. The output of the comparators is encoded to 1.5-bit representation using the

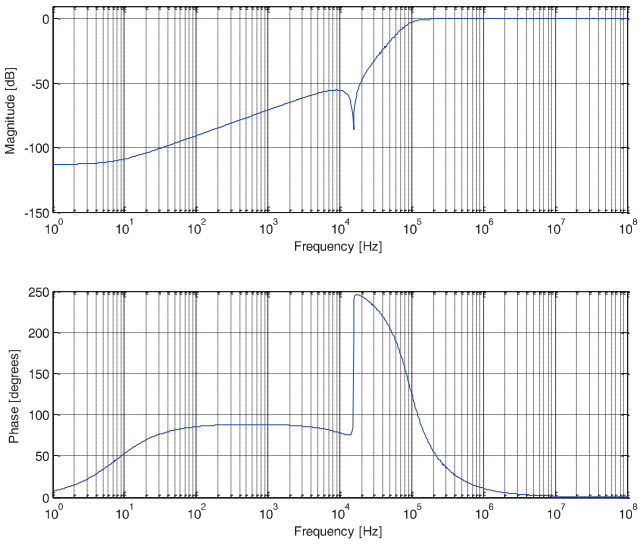

Fig. 15. Bode diagram of the NTF of the modulator.

circuit shown in Figure 19. The threshold voltage for comparison is determined by several simulations of the propose architecture in order to obtain the max point of the SNDR as function of the threshold voltage. The Figure 17 shows the measured SNDR as function of threshold voltage (V_t) and the selected value was 0.33V.

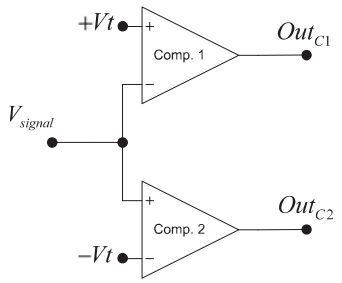

Fig. 16. Schematic design of 1.5-bit quantizer.

TABLE III
ADC CODIFICATION.

V_{Signal}	State	Out_{C1}	Out_{C2}
$V_{Signal} > V_t$	+1	0	1
$-V_t < V_{Signal} < V_t$	0	1	1
$V_{Signal} < V_t$	-1	1	0

Since the threshold voltage of the comparators has a random error, a Monte Carlo simulation where the V_t voltage of the comparators was randomly changed with a 3σ value of 10 mV was performed for 500 cases. The histogram of the SNDR values obtained in this analysis is shown in Figure 18, this histogram shows that the SNDR in worst case only degrades about 0.7 dB with the variation of the offset of the comparators.

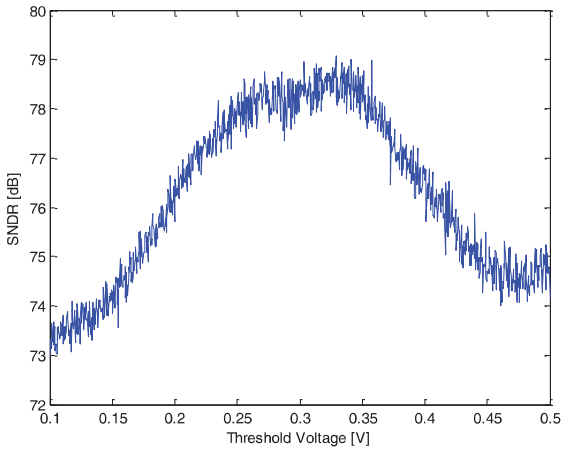

Fig. 17. Measured SNDR as function of threshold voltage (V_t). Data obtained by running 1000 simulations with a Vt step of 0.4 mV.

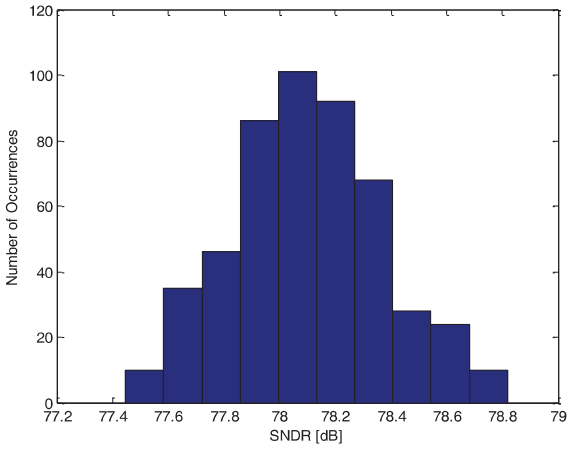

Fig. 18. Histogram of the behavioral simulated SNDR of the proposed ΣΔ modulator ($3\sigma_{vt}$ = 10 mV) . Data obtained by running 500 Monte-Carlo simulations of the proposed architecture.

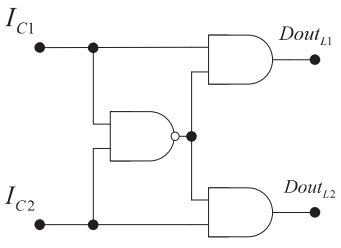

Fig. 19. Encoding logic for 1.5-bit quantizer.

TABLE IV
LOGIC CODIFICATION OF THE 1.5-BIT QUANTIZER.

I_{C1}	I_{C1}	State	$Dout_{L1}$	$Dout_{L2}$
0	0	x	0	0
0	1	+1	0	1
1	0	-1	1	0
1	1	0	0	0

B. Important Parameters in Operational Amplifiers

In the previous analysis it was assumed that the operational amplifiers were ideal, when real amplifiers are used the non-ideal effects can change the behavior of the modulator. In order to understand what is the required performance of the different parameters of the amplifiers, such as: gain-bandwidth product (GBW), slew rate and DC gain, the modulator circuit was simulated using a first order electrical model for the amplifiers. This model includes DC gain, a single pole and the slew rate effect. In these simulations the amplifier parameters were set to different values in order to determine the minimum required values for the different parameters.

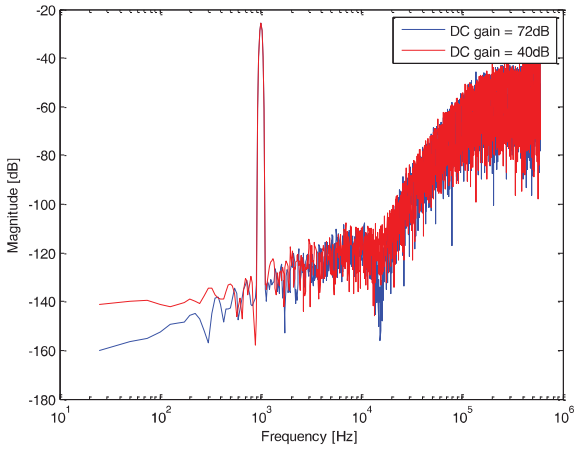

Fig. 20. Influence of the DC gain in the output spectrum of the modulator (results obtained with electrical simulations with first order model amplifier with a GBW = 50 MHz, and a slew rate = 10 V/μs).

To investigate SNDR degradation due to variation of the parameters of the operational amplifiers, different electrical simulations with variations in the DC gain, the GBW, and the slew rate were performed. In these simulations a first order model for the amplifier with a DC gain = 72 dB, a GBW = 50 MHz, and a slew rate = 10 V/μs was used. The output of the circuits was analyzed using a 2^{16} points FFT with a Blackman-Harris window, these results are shown in Figures (20, 21, and 22).

Observing Figure 20 it is clear that a reduction of the DC gain of the first amplifier causes a reduction of noise shaping at low frequencies. The reduction of the gain in the second and third operational amplifier decreases notch attenuation due to zeros in the NTF.

As it can be observed in Figure 21, the decrease of the GBW of the amplifiers decreases the frequency of the zeroes, resulting in added noise in the upper part of the signal band, therefore degrading the SNDR.

From Figure 22 it is possible to conclude that a low slew rate in the amplifier results in added distortion and a degradation of the notch produced by the zeroes.

These simulations show that if the amplifiers have a DC gain of 72 dB, a GBW of 50 MHz and a slew rate of 10 μV they do not affect the performance of the modulator significantly.

C. Simulation Results

In order to verify the stability of the design, a 500 cases Monte Carlo analysis where the value of the components were

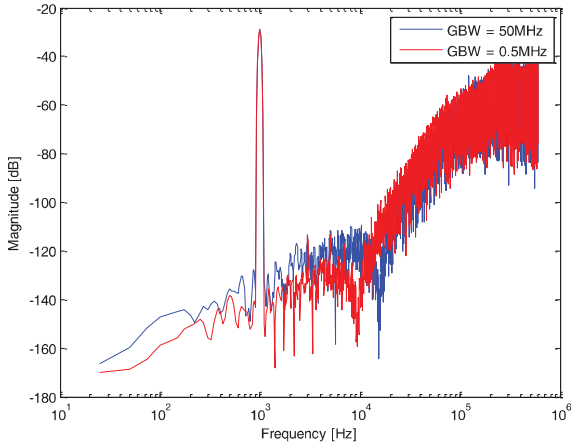

Fig. 21. Influence of the GBW in the output spectrum of the modulator (results obtained with electrical simulations with first order model amplifier with a DC gain = 72 dB, and a slew rate = 10 V/μs).

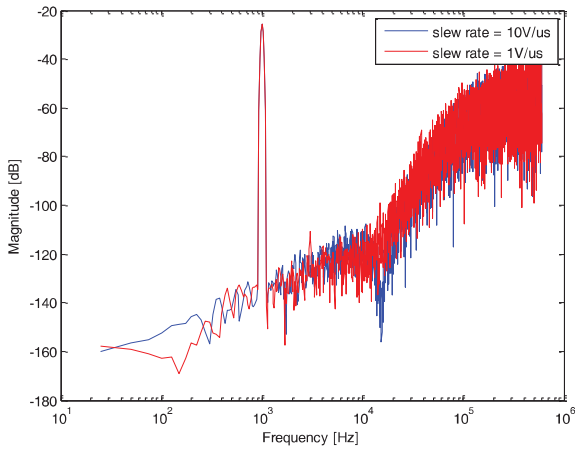

Fig. 22. Influence of the slew rate in the output spectrum of the modulator (results obtained with electrical simulations with first order model amplifier with a DC gain = 72 dB, and a GBW = 50 MHz).

randomly selected around the nominal values with a normal distribution with $3\sigma = 5\%$ for the capacitors and with $3\sigma = 1\%$ for the resistors. Figure 23 shows the histogram of the SNDR values obtained in this analysis, and shows that the SNDR in worst case degrades about 1.5 dB due to components mismatch.

The output swing of the three integrators in the modulator was verified using behavioral simulations. The histogram of each output voltage is depicted in Figure 25, these histograms show that the output voltages are smaller than $\pm$ 1.2V, therefore the operational amplifiers should not approach saturation during the operation of the circuit.

Figure 24 shows the circuit implementation of the proposed architecture. This circuit was simulated using an electrical simulator and the output spectrum was calculated, this is shown in Figure 26. The electrical simulations used a first order model amplifier with a DC gain = 72 dB, a GBW = 50 MHz, and a slew rate = 10 V/μs.

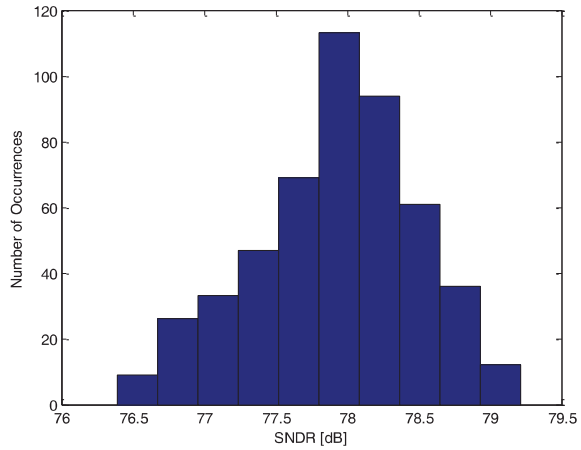

Fig. 23. Histogram of the behavioral simulated SNDR of the proposed $\Sigma\Delta$ modulator with component values mismatch of $3\sigma\frac{\Delta R}{R} = 1\%$ and $3\sigma\frac{\Delta C}{C} = 5\%$. Data obtained by running 500 Monte-Carlo simulations of the proposed architecture.

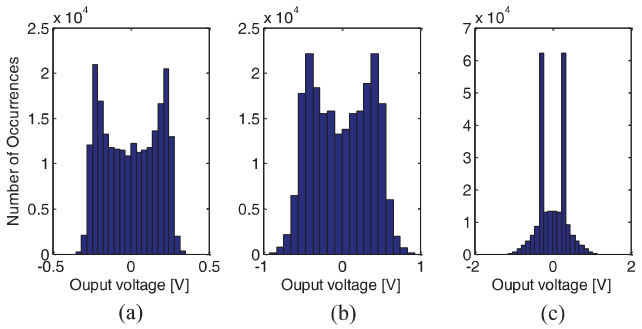

Fig. 25. Histogram of the behavioral simulated output voltage of the (a) first integrator, (b) second integrator, and (c) third integrator for the proposed $\Sigma\Delta$ modulator.

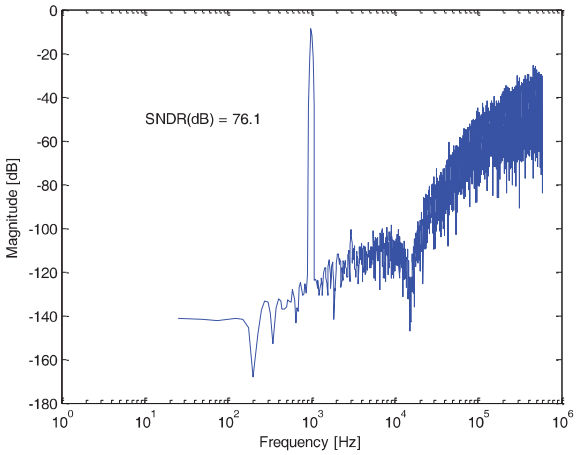

Fig. 26. Output spectrum of the proposed architecture obtained with electrical simulations with first order model amplifier with a DC gain = 72 dB, a GBW = 50 MHz, and a slew rate = 10 V/μs (2^{16} points FFT using a Blackman-Harris window).

VI. Conclusion

This paper presents a 3rd order 1.5-bit $\Sigma\Delta$ modulator with distributed feedback and local resonator feedback for

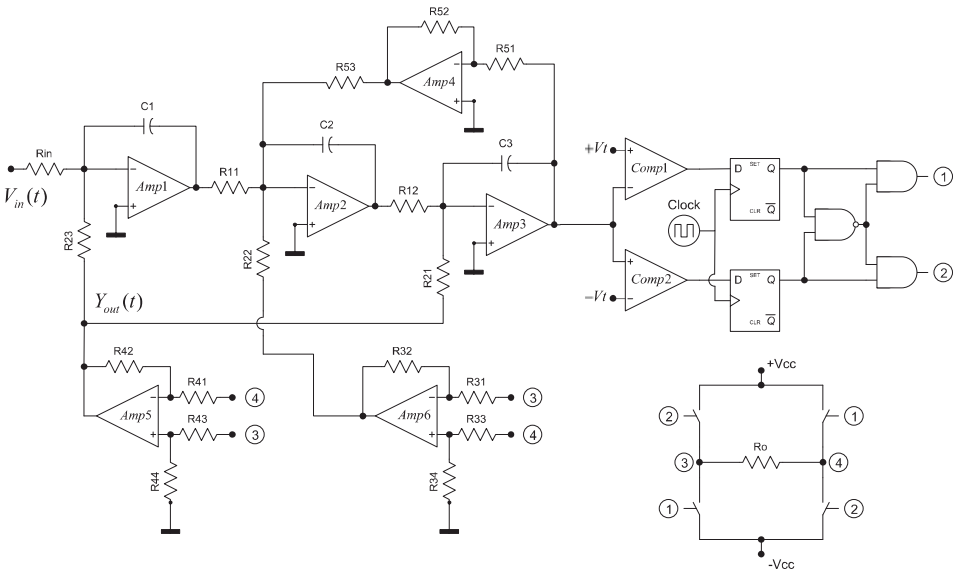

Fig. 24. Class D audio amplifier implementation.

a Class D audio amplifier. In order to improve the SNDR, without increasing the OSR or the order of the modulator (not greater then 3), the modulator uses transmission zeros and 1.5-bit quantization. High level simulations of the modulator show that it has a maximum SNDR value of 81 dB for a signal bandwidth of 18 kHz and a sampling frequency of 1.2 MHz. The increase of the resolution of the quantizer (1.5-bit quantizer instead of 1-bit quantizer) improves the linearity of the feedback in the modulator. Since this results in a more stable loop, it is possible to increase the stopband ripple in the modulator and therefore improve the maximum SNDR value. An electrical circuit was designed to implement the proposed architecture and the electrical simulations showed that it has a maximum SNDR value of 76.1 dB. The influence of the constituting blocks of the circuit in the performance of the modulator was investigated using electrical simulations.

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