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Atomic Layer Deposition of Al_2O_3 Dielectrics for Low-Temperature TFT Process

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Atomic Layer Deposition of Al_2O_3 Dielectrics for Low-Temperature TFT Process

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"O que dá o verdadeiro sentido ao encontro é a busca, e é preciso andar muito para se alcançar o que está perto."

José Saramago

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Abstract

Thin-film-transistor (TFT) technology has been prominent in the modern era, being devices particularly suitable for large-area applications such as displays and flexible electronics. When thinking about applications demanding low cost and/or mechanical flexibility, there is a need for a process that can deliver quality films in substrates which require a low thermal budget. In this work, Atomic Layer Deposition (ALD) is studied as a process for low-temperature depositions of Al_2O_3 dielectric layers to be used in a well-established oxide TFT process.

The first part of this work focused on establishing and optimizing a 150 ºC ALD process for Al_2O_3, through adjustment of precursor exposure and purge times, which was done by studying both the optical and electrical properties of the dielectrics and comparing these to ones grown at 200 ºC. Optical results showed good quality film growth, uniform film thickness throughout 3” substrates, and a constant growth-per-cycle for a given process. The optimized 150 ºC Al_2O_3 layers had a dielectric constant of 8.4±0.6 and a breakdown field of 4.0±2.1 MV/cm, which are comparable to state-of-the-art Al_2O_3 films fabricated at 200 °C or higher temperatures.

The second part of this work was the implementation of the 50 nm thick optimized ALD dielectric as a gate insulator in top-gate and bottom-gate oxide TFTs based on indium-gallium-zinc oxide (IGZO) semiconductor. The bottom-gate transistors show hysteresis in the transfer curves, unlike the top-gate transistors, associated to charge trapping at the Al_2O_3/IGZO interface arising from the damage of the IGZO sputtering process. The bottom-gate and top-gate transistors have average saturation mobility of 6.3 cm^2/Vs and 1.3 cm^2/Vs, respectively, and a SS of approximately 0.1 V/dec and 0.2 V/dec. While future engineering of the dielectric/semiconductor stack can further improve device performance and stability, the results obtained already demonstrate that 150 °C Al_2O_3 layers by ALD are very good candidates for flexible oxide TFTs on temperature-sensitive substrates.

Keywords: ALD, Al_2O_3, low temperature, IGZO, TFT

Resumo

A tecnologia de transístores de filme fino (TFT) é cada vez mais importante na atualidade, devido à aplicabilidade destes dispositivos em tecnologias de grande área como mostradores e eletrónica flexível. A necessidade de baixo custo e flexibilidade mecânica nestas áreas incita a procura de um processo capaz de produzir filmes de alta qualidade acomodados a substratos que requerem baixas temperaturas. Neste trabalho, a técnica de deposição de camadas atómicas (ALD) é estudada para deposições de camadas dielétricas de Al_2O_3 a baixa temperatura, para uso em tecnologia TFT de óxidos.

A primeira parte deste trabalho focou-se na otimização de um processo de ALD para Al_2O_3 a 150ºC, através de ajustes nos tempos de exposição e purga do precursor e do elemento reativo. Para tal, estudaram-se as propriedades elétricas e óticas do dielétrico e compararam-se com as propriedades de Al_2O_3 depositado a 200 ºC. As propriedades óticas demostraram crescimento de boa qualidade dos filmes, espessura uniforme ao longo de substratos de 3" e um crescimento por ciclo constante para cada processo. As camadas depositadas a 150 ºC apresentaram uma constante dielétrica de 8.4±0.6 e um campo elétrico de rutura de 4.0±2.1 MV/cm, que são equiparáveis ao estado da arte de filmes de Al_2O_3 fabricados a temperaturas iguais ou superiores a 200 °C.

A segunda parte centrou-se na implementação da camada de 50 nm do processo otimizado como dielétrico da porta em TFTs *top-gate* e *bottom-gate* de óxido de índio-gálio-zinco (IGZO). Os transístores *bottom-gate* apresentam histerese nas curvas de transferência, ao contrário dos *top-gate*, que se deve à acumulação de cargas na interface Al_2O_3/IGZO proveniente dos danos da pulverização catódica de IGZO. Os transístores *bottom-gate* e *top-gate* apresentam, respetivamente, mobilidades de 6.3 cm^2/Vs e 1.3 cm^2/Vs e SS de 0.1 V/dec e 0.2 V/dec. Embora seja possível melhorar o desempenho dos dispositivos, os resultados obtidos demonstram que as camadas de Al_2O_3 a 150 ºC são já boas candidatas para processos de TFTs de óxidos flexíveis em substratos sensíveis à temperatura.

Palavras-chave: ALD, Al_2O_3, baixa temperatura, IGZO, TFT

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List of abbreviations

ALD	atomic layer deposition
CENIMAT	Centro de Investigação de Materiais
CVD	chemical vapor deposition
FCT-UNL	Faculdade de Ciência e Tecnologia da Universidade Nova de Lisboa
FTIR	Fourier-transformed infrared spectroscopy
GPC	growth per cycle
IGZO	indium-gallium-zinc oxide
MIM	metal-insulator-metal
MOSFET	metal-oxide-semiconductor field-effect-transistor
TMA	trimethylaluminum
TFT	thin-film-transistor
XPS	x-ray photoelectron spectroscopy

List of symbols

C_{ox} oxide capacitance density

d_{ox} oxide thickness

ε_0 permittivity in vacuum, 8.854×10^{-12} F ·m^{-1}

g_m transconductance

I_D drain current

I_G gate current

J current density

κ relative permittivity or dielectric constant

L channel length

n refractive index

SS subthreshold swing

V_D drain voltage

V_G gate voltage

V_{ON} turn-on voltage

W channel width

μ_{FE} field-effect mobility

μ_{sat} saturation mobility

Motivation and Objectives

TFT technology has been widely used nowadays alongside other transistor technologies, as its available substrates can have large areas or mechanical flexibility, properties that allow this technology to be used in many fields, including displays and flexible electronics [1], [2]. This variety of substrates comes, however, with some limitations regarding process temperatures, as some of them may not be suitable for some of the high temperatures inherent to available thin film deposition processes, without compromising its properties and the quality of the films. This is the case with some polymer substrates, whose glass transition temperature is around 150 ºC, and, as such, the processes used to fabricate TFTs on them should restrain themselves from exceeding this temperature [3].

Atomic Layer Deposition (ALD) is a process that can deliver uniform, conformal thin films with good properties at low temperatures [4]. ALD has already been used to produce the electrodes, the semiconductor and dielectric layers in TFT technology, [5] and ALD-grown dielectrics have been reported in flexible oxide TFTs [6].

The objective of this work is the implementation of atomic layer deposition to produce an aluminum oxide dielectric layer at low temperature, not exceeding 150 °C, for application in an oxide TFT process available at CENIMAT.

This is the first reported work at FCT-UNL using thermal ALD for deposition of Al_2O_3. Initially, this work was meant as a collaboration between CENIMAT and FlexEnable Ltd, in Cambridge, UK, also focusing on the low-temperature deposition of aluminum oxide dielectrics, to be used in the TFT process developed by the company, using organic semiconductors. However, due to the restrictions imposed by the Covid-19 pandemic, the course of this work shifted from implementing the dielectrics in FlexEnable's organic TFT process, to implementation of these dielectrics into CENIMAT's oxide semiconductor TFT process.

In the first part of this study, 50 nm Al_2O_3 ALD-grown layers at 150 ºC were deposited on 3" Si wafers and into MIM structures to determine optical and electrical properties, respectively. Process optimization is conducted by altering the precursor and reactant exposure and purge times, to find the layers with the overall best properties, using the dielectric constant as the primary indicator of the best process.

The optimized process is then used for dielectric deposition in indium-gallium-zinc oxide (IGZO) semiconductor TFTs and these devices are submitted to electrical characterization.

1 Introduction

1.1 Atomic Layer Deposition

Atomic Layer Deposition (ALD) is a variant of Chemical Vapor Deposition (CVD), in which a simultaneous flow of multiple gases enables thin film growth over a hot surface. In an ideal CVD, there is no reaction between reactant gases in the gas phase, as they should only react with the surface as they are heated moving towards it. A reaction between gas phases could lead to the formation of unwanted particles that can end up embedded in the film.

While ALD follows the same principle of CVD, unlike CVD, the gas reactants in this process are introduced in the reaction chamber alternately, to avoid contamination, reacting only with the surface. This leads to a self-limited deposition of monolayers that are subsequently stacked to form a layer with the desired thickness according to the number of ALD cycles and the average layer growth during each ALD cycle – the growth per cycle (GPC). It is considered a very effective technique in thin-film technology as its monolayers have high uniformity and conformality over large substrates with varying surface roughness, its thickness is easily controlled, and can grow films with relatively high purity and density at temperatures as low as room temperature [4], [7]. The principle of ALD can be traced back to the 1960s, in the Soviet Union, with the term "molecular layering", although the origin of ALD is attributed to Tuomo Suntola, from Finland, for what was known at the time as "atomic layer epitaxy" [8-9].

1.1.1 ALD Process Description

In ALD, thin films are built up in cycles in which the surface is exposed to gaseous species in alternating, separated doses. In each cycle, a sub-monolayer of material is deposited. As shown in Figure 1.1, a typical cycle consists of four steps: (1) a precursor dosing step, where a precursor is typically an inorganic coordination compound, i.e., a metal center surrounded by chemical functional groups called ligands; (2) a purge/pump step; (3) a co-reactant step, typically involving a small molecule; and (4) a purge/pump step.

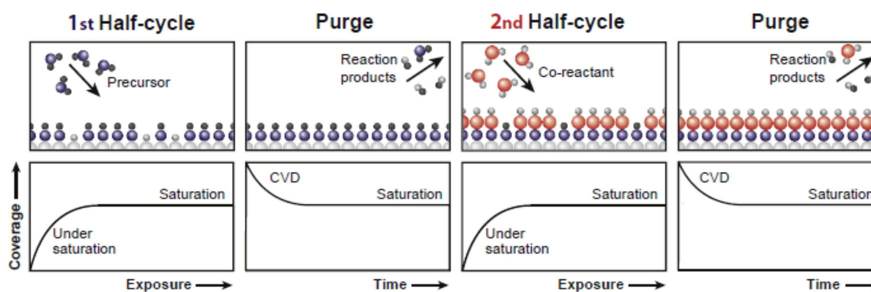


Figure 1.1. Schematic of an ALD cycle. The half-cycles both consist of a self-limiting reaction, where the process stops once all available surface sites are occupied. Between each half-cycle, a purge step removes undesirable reaction products. The cycles are then repeated until the desired thickness is obtained [10].

The precursor, and in many cases the co-reactant, bring elements to the surface that lead to film growth. The precursor is responsible for the deposition of the metallic center, while the reactant for the deposition of typically a non-metal such as O, N, S.

The precursor and co-reactant must both react with the surface in a self-limiting way, which means the precursor molecules and co-reactant species react with surface sites and/or surface chemical groups while these are present or accessible, thus the surface reactions eventually saturate and stop. As such, the precursor molecules and co-reactants react neither with themselves nor with the surface groups that they create. In the purge and/or pump steps, gaseous reaction products generated during the surface reactions, as well as any excess precursor or co-reactant molecules, are removed from the ALD reactor, which is very important to avoid reactions between the gas-phases of precursor and co-reactant molecules, as it could lead to an undesired CVD component [10].

The conditions which are necessary to obtain self-limiting growth differ for each ALD process and lead to a characteristic growth per cycle (GPC), which is the amount of material that is deposited in an ALD cycle. Furthermore, each process is deemed to have a specific temperature window in which ALD behavior is obtained. An idealized temperature window is shown in Figure 1.2, where the GPC is plotted as a function of temperature.

For ideal ALD growth, the temperature window represents a temperature range that shows a non-dependency of the temperature on the growth per cycle. Outside the window, the ALD behavior can be lost at low temperatures due to condensation and low reactivity, and also at high temperatures due to decomposition and desorption. At low temperatures, reactions may not take place and precursors can condense on the surface preventing effective purging. At higher temperatures, precursors can decompose and originate a sub-product that can affect growth, and desorption of the film or the precursor can occur, reducing growth [4], [7], [10].

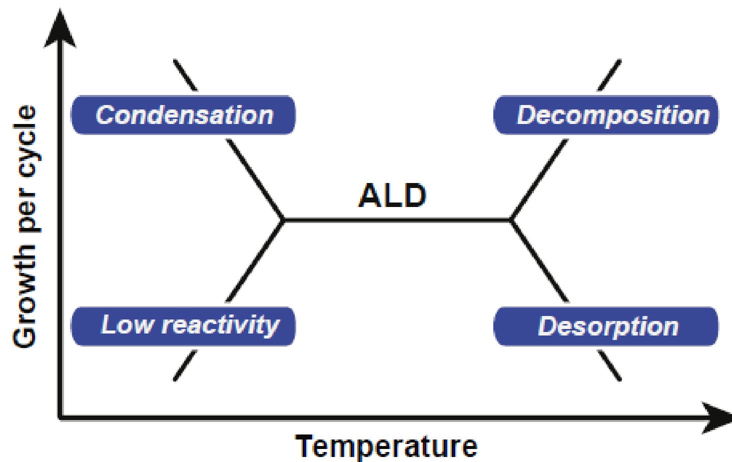


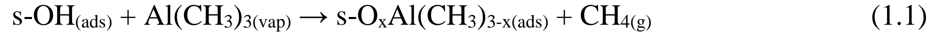
Figure 1.2. Growth per cycle dependency on the process temperature. Undesirable phenomena for the ALD process outside the temperature window, where the GPC is temperature non-dependant, are represented [10].

ALD can be either thermal or plasma/radical enhanced, where the radicals or other energetic species in the plasma help to induce reactions that are not possible using just thermal energy. Plasma sources can be used to generate hydrogen radicals that reduce the metal or semiconductor precursors. Plasma enhanced ALD makes it easier to deposit single-element films of metals and semiconductors [4].

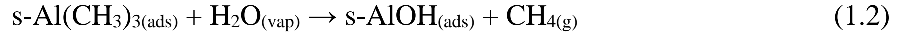
1.1.2 Aluminum Oxide Thermal ALD

Aluminum oxide (Al_2O_3) is one of the most used materials in ALD, as it has applications over various fields as an insulator/dielectric, such as solar cells, optical coatings, and coatings for nanoparticles [7]. TFTs using Al_2O_3 as its gate dielectric have also been reported, including TFTs using indium-gallium-zinc oxide (IGZO) as semiconductor, on flexible substrates [6].

Al_2O_3 can be grown by either thermal ALD or plasma-based ALD, using water or oxygen and ozone, respectively, as their oxygen donors. Many precursors have been studied as the Al-source, including trimethylaluminum (TMA), with the chemical formula for its molecule as $Al(CH_3)_3$, which is the most commonly reported precursor, having simple chemistry for both thermal and plasma-enhanced ALD processes. In this work we study thermal ALD, using TMA as precursor and H_2O as co-reactant. Each cycle for ALD can be divided into two half-cycles, for TMA condensation and H_2O hydrolysis. These half-cycles are represented in equations (1.1) and (1.2), and equation (1.3) represents the simplified full cycle reaction in stoichiometric proportions.



$$s\text{-}OH_{(ads)} + Al(CH_3)_{3(vap)} \rightarrow s\text{-}O_xAl(CH_3)_{3-x(ads)} + CH_{4(g)} \quad (1.1)$$



$$s\text{-}Al(CH_3)_{3(ads)} + H_2O_{(vap)} \rightarrow s\text{-}AlOH_{(ads)} + CH_{4(g)} \quad (1.2)$$

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6\,CH_4 \quad (1.3)$$

In the TMA half-cycle (1.1), the surface hydroxyl group (s-OH) donates a proton to a methyl (CH_3) group on the TMA, resulting in the formation of a surface O–Al bond and release of methane (CH_4) as a reaction product, to be purged immediately after. TMA usually bonds via one methyl group but can bond via two, which is more unlikely. In the H_2O half-cycle, hydrolysis of the methyl ligands occurs, resulting in the formation of surface O–Al bonds as well as methane, like in the first half-cycle [4], [7], [10]. Although ideally, a full monolayer of aluminum oxide is formed after each ALD cycle, it is less than one. This phenomenon is due to a steric effect regarding the TMA molecule, as its large size makes it harder to fully position enough aluminum atoms on the surface to yield a full monolayer of aluminum oxide. However, the reported sizes of ALD grown Al_2O_3 monolayers are larger than theoretical sizes that should be observed, closer to a full monolayer. As such, it is thought that each monolayer can contain smaller molecules, other than TMA, which are chemisorbed into the monolayer [7].

Al_2O_3 has been reported to be grown at temperatures as high as 500 ºC, although at around 300 ºC, TMA begins to decompose, so deposition GPC may not follow the standard ALD temperature window, as there is a decrease in density of surface OH groups [7].

1.1.3 Low-Temperature Thermal ALD

Low-temperature processes below 200 ºC, are important for low thermal budgets, not only to prevent interdiffusion of materials but also to prevent damage in thermally fragile substrates such as polymeric flexible substrates or biological samples. Currently, both thermal ALD and radical enhanced ALD have been reported at room temperature [7].

Depositions of Al_2O_3 by thermal ALD for temperatures as low as 33 ºC have been reported since 2004, along with an extensive study of these films' properties. Electrical properties reported in the article are relatively constant with temperature decrease, showing a low leakage current density, dielectric constant κ around 7.7, and a breakdown voltage of 4.3 MV/cm for 177 ºC and 3.7 MV/cm at 33 ºC. Although here, GPC does not see a major decrease with temperature, properties such as the refractive index, n, along with density do show a significant decrease, which can translate in a higher impurity content between monolayers [10-11]. This can be mainly attributed to the lower thermal energy available for H_2O reactivity, as the species have more difficulty in removing CH_3 groups. Plasma enhanced ALD does not have this problem as it uses oxygen as a co-reactant, and, as such, is more suitable for low-temperature depositions [4], [10].

To overcome these problems, the purge times after H_2O exposure are increased to ensure a higher removal of CH_3 groups preventing Al–O bonding. It was found, however, that CH_3 groups persist in lower temperature deposition processes after saturation of H_2O half-cycle, which means that the ALD process at these temperatures is limited by the reactivity of H_2O towards these groups [12].

1.1.4 ALD in TFT Technology

Thin Film Transistor (TFT) technology was first introduced in 1962, as an alternative to the standard MOSFET. [13] Like MOSFET, TFTs are field-effect devices, whose current flows through a semiconductor between a source and drain electrodes. A dielectric layer is in contact with the semiconductor and a third electrode, the gate, contacts with this layer and is responsible for the current modulation in the device, by injecting carriers into the dielectric/semiconductor interface. Figure 1.3 shows some of the conventional structures used for TFTs [1].

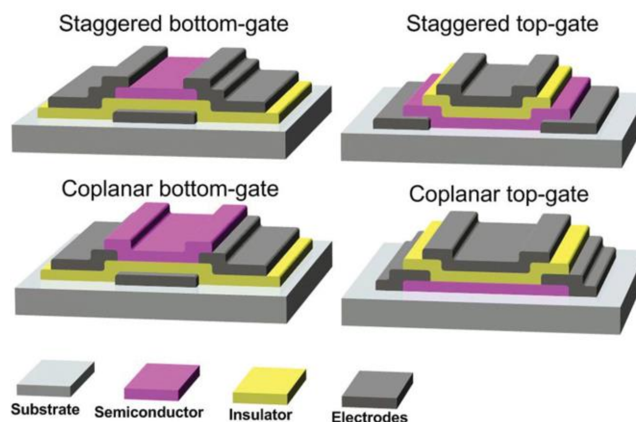


Figure 1.3. Schematic representing different structures for TFTs [1].

Unlike classical MOSFET, which uses the Si wafer as both their substrate and semiconductor for carrier mobility, TFTs can be fabricated in a variety of substrates, such as glass and polymers, since its semiconductor is deposited as a thin film, along with the dielectric and electrode layers. Different semiconductors have been reported in TFTs, including amorphous Si, organic semiconductors, and oxide semiconductors. Oxide semiconductors have shown great promise for multiple applications, as they can attain high carrier mobilities, low subthreshold swing (*SS*), and low leakage currents while being produced at relatively low temperatures. [1]

ALD has already been reported for the production of not just the gate dielectric, but also the semiconductor, as well as the gate, source, and drain electrodes [5], [14]. Several works detail Al_2O_3 grown by ALD as a gate dielectric in oxide TFTs, including IGZO semiconductor TFTs in flexible substrates. These TFTs have shown mobilities of up to 15.5 cm^2V/s, high On/Off ratios (around 10^7, all the way up to 10^9), and *SS* as low as 0.2 V/dec [5-6], [15-16].

This work has the main goal of implementing an Al_2O_3 layer grown by a 150 ºC thermal ALD process for use in oxide TFT technology as a gate dielectric, and for that, it was divided into two phases. The first phase consists in an optimization of the 150 ºC, by studying the properties of the deposited 50 nm Al_2O_3 layers, as well as ones deposited at 200 ºC, and comparing them with one another, as well as other works. To study the electrical properties, a metal-insulator-metal (MIM) structure using Al for metal contacts and Al_2O_3 was produced. In the second phase, we take the optimized 150 ºC process as well as the standard 200 ºC process and use them for gate dielectric deposition for both top-gate and bottom-gate TFTs based in indium-gallium-zinc oxide (IGZO) semiconductor, which is already an optimized process at FCT-UNL.

2 Materials and Methods

2.1 Al_2O_3 Depositions and MIM Structure Production and Characterization

Corning Glass with 2.5 cm by 2.5 cm was used as a substrate for both MIM structures and TFTs, and the cleaning process is the same for both. The glass is placed in a tray with acetone, in an ultrasonic bath, for 10 minutes and is then moved into a tray filled with isopropanol, also put in an ultrasonic bath for 10 minutes. Finally, the glass is cleaned with water, dried with a nitrogen gun, and placed on a hot plate at 150 ºC for about 20 minutes. Firstly, 100 nm of aluminum was deposited by e-beam evaporation for the bottom contacts of the MIM structure, using a mechanical mask available at CENIMAT (Annex 1). Before submitting the samples to ALD, a Kapton strip is put over a part of the metal contacts to protect them from alumina deposition. For thermal ALD, a Beneq TFS-200 reactor was used. The original recipe from the manufacturer for 50 nm layers, at 200 ºC, can be found in Annex 2. For the depositions at 150 ºC, a process optimization was done to replicate or enhance the dielectric layer's properties compared to the 200 ºC ones. This optimization process would see a variation in all these times as depicted in Table 2.1. The first process was based on [11] and processes 2-5 would see a slight variation in the times, to understand its effects. Processes 6-9 would have a considerably large purge time for both precursor and reactant to ensure complete removal of excess non-reactive precursor and reactant and had variations in both exposure times.

Table 2.1. Summary of process times for the standard 200 ºC and the different 150 ºC ALD processes for deposition of 50 nm Al_2O_3.

Process	**TMA Exposure (s)**	**TMA Purge (s)**	**H_2O Exposure (s)**	**H_2O Purge (s)**	**Process Time for 475 Cycles (min)**
200 ºC	0.15	0.65	0.15	1	15
P1	0.15	0.65	0.3	2	25
P2	0.15	0.65	0.3	5	48
P3	0.15	0.65	0.6	5	51
P4	0.3	1	0.3	5	52
P5	0.3	2	0.3	5	60
P6	0.3	5	0.3	8	108
P7	0.3	5	0.15	8	106
P8	0.15	5	0.3	8	106
P9	0.15	5	0.15	8	105

After ALD deposition, 100 nm thick Al top contacts were deposited by e-beam evaporation. The MIM structures' area was then measured using an Olympus BX51 optical microscope and would then undergo electrical characterization using a Keysight B1500A semiconductor parameter analyzer and a Cascade Microtech EPS 150 manual probe station. Alongside the substrates for MIM structures, a 3" p-type Si wafer was also put in the reaction chamber, in each process. These wafers were then used for optical characterization of the dielectric, via FTIR, using a Thermo Nicolet 6700 and via ellipsometry, using a Horiba-Jobin Yvon Spectroscopic Ellipsometer. The optimal process would be chosen as a result of the structure that presented the overall best properties upon its characterization, with a focus on a high dielectric constant, and would then be used as the dielectric in the IGZO TFT.

2.2 IGZO TFT Production and Characterization

60 nm of molybdenum were deposited for gate and source/drain electrodes in both top-gate and bottom-gate transistors via sputtering in an AJA ATC 1800. Patterning was done by spin-coating AZ ECI 3007 positive photoresist, exposing it in a Suss MA6 UV mask aligner, and then developing it using an AZ 726 MIF developer. Molybdenum was then dry-etched using SF_6 gas in a Trion Phantom 3 reactive ion etcher. After each etching, the remaining photoresist is removed using acetone.

The top-gate TFTs undergo an optimized deposition of 30 nm IGZO (with In:Ga:Zn in a 2:1:1 atomic ratio) semiconductor, using an AJA ATC 1300-F. Patterning was done similarly to the previous step, using instead positive photoresist AZ ECI 3012. IGZO was wet etched using HCl dissolved in H_2O with a 1:20 ratio, and after photoresist removal, was thermally annealed at 180ºC. After IGZO annealing is complete for the top-gate TFTs, both top-gate and bottom-gate would undergo ALD for deposition of a 50 nm Al_2O_3 layer for either the optimized 150 ºC process or the standard 200ºC process. The dielectric was then patterned similarly to the semiconductor and was wet etched using H_3PO_4, at 80 ºC. The bottom-gate transistors would then undergo IGZO deposition and patterning as the top-gate transistors did, and finally, the top Mo contacts were deposited for all the TFTs (source/drain and gate electrodes for bottom- and top-gate transistors, respectively), which would undergo a final thermal annealing at 180ºC. The produced TFTs were submitted to electrical characterization using an Agilent 4155C semiconductor parameter analyzer and a Cascade Microtech M150 manual probe station. To capture images of the TFTs, a Zeiss Axioscope 5 optical microscope was used.

The IGZO/Al_2O_3 interface was studied by x-ray photoelectron spectroscopy (XPS), using a Kratos Axis Supra. For this study, both interfaces reminiscent of the top-gate and bottom-gate TFTs were deposited on top of Si wafer substrates, that is, Al_2O_3 stacked on top of IGZO to resemble the top-gate TFTs and IGZO stacked on top of Al_2O_3 to resemble the bottom-gate TFTs. While the bottom layers' thickness was the same as the one used in the TFTs (50 nm for Al_2O_3 and 30 nm for IGZO), the top layers' thickness was fixed at 5 nm.

3 Results and Discussion

3.1 Optical Characterization

3.1.1 FTIR

FTIR data was obtained from a Thermo Nicolet 6700 by single-bounce attenuated total reflectance (ATR) sampling, with a range from 4500 cm^{-1} to 500 cm^{-1}. Data recorded for < 700 cm^{-1} was ultimately disregarded, as it contained artifacts from the equipment. Figure 3.1 shows the spectra obtained for the Al_2O_3 layers grown at 200 ºC and at 150 ºC using low purge time processes, P1 to P5, as well as the Si wafer substrate, without any ALD exposure. The most noticeable peak is located at around ~900 cm^{-1} and is directly correlated with Al_2O_3 deposition, which has been previously reported [17-18]. This is corroborated by the absence of this peak on the Si wafer spectrum. The peak located at 1105 cm^{-1} can be attributed to Si – O bond due to native oxide present in the Si wafer. The region from ~3500 cm^{-1} to ~4000 cm^{-1}, which is mainly associated with the presence of OH groups, is smooth in most spectra. The bonds observed at 2917 cm^{-1} and 2850 cm^{-1} are the C – H asymmetric and symmetric stretching bonds, characteristic of CH_3 from Al – CH, which is a resulting product of the trimethylaluminum $Al(CH_3)_3$ precursor exposure step [19].

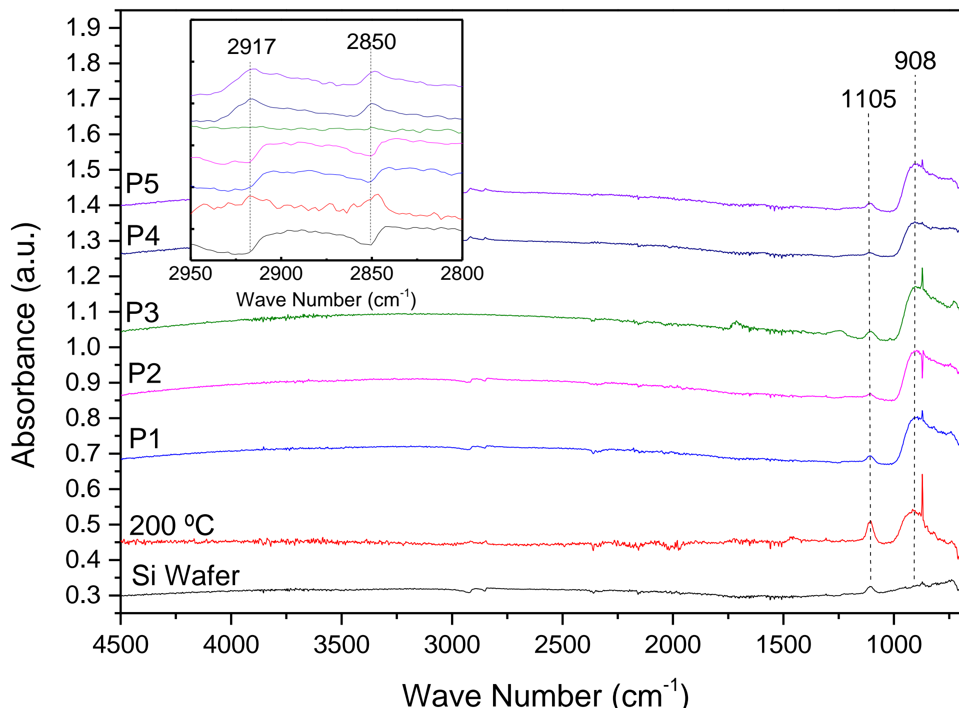


Figure 3.1. FTIR Data for 50 nm standard 200 ºC and 150 ºC ALD-grown Al_2O_3 layers from processes P1 – P5 and the Si wafer substrate without Al_2O_3. Inset shows the region between 2950 cm^{-1} and 2800 cm^{-1} as well as observed peaks.

When lowering the temperature of the ALD process, it is known that precursors have less reactivity, and so a larger exposure time is used to help overcome this. We notice the absence of the aforementioned C – H peaks in process P3, which uses the larger exposure time for H_2O from all of the samples, which indicates H_2O successfully reacted with more of the CH_3.

Figure 3.2 shows spectral data for the large TMA and H_2O purge time processes P6 – P9. All spectra show, overall, a higher intensity on the CH stretching bonds. The peak at 740 cm^{-1}, which is more pronounced on the 150 ºC P9 and the 200 ºC is characteristic of a C – H rocking bond, whose origin is also related to TMA's Al – CH. These processes have the same exposure times for both precursors and the lowest exposure time for H_2O, which can explain the higher intensities on these last peaks.

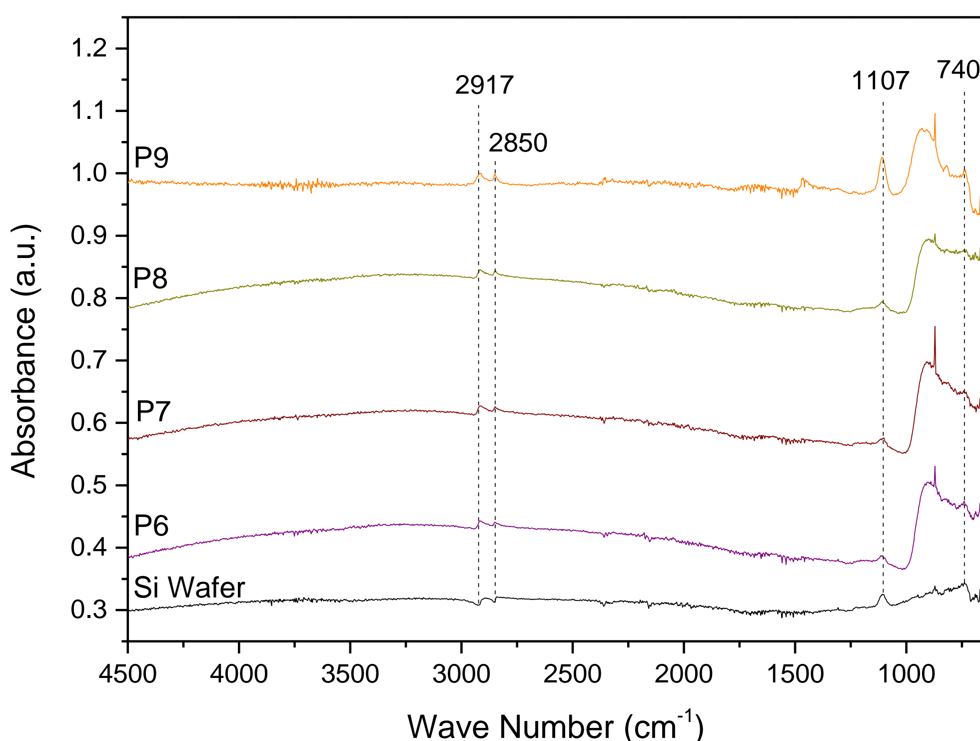


Figure 3.2. FTIR spectra for 150 ºC Al_2O_3 ALD processes P6 – P9, with large purge times and Si wafer substrate, without any alumina.

3.1.2 Ellipsometry

Ellipsometry data was collected from a range of 0.59 eV – 6.5 eV for a 200 ºC ALD-grown 50 nm and a 100 nm layer, as well as for a 50 nm layer grown with all 150 ºC processes, considering the Tauc-Lorentz model. For each 3" substrate, a total of five points were measured to find out layer thickness uniformity over the wafer area: one point is located on the center and the remaining four on opposite edges. The results obtained from ellipsometry analysis are summarized in Table 3.1.

Table 3.1. Summarized data of ellipsometry data for all ALD-grown Al_2O_3 layers.

Temperature	Layer	Thickness (nm)	GPC (Å)	*n* at 635 nm	*n* at 400 nm
150 ºC	**P1**	52.8 ± 0.1	1.11	1.617	1.639
	P2	55.3 ± 0.1	1.16	1.617	1.639
	P3	58.9 ± 0.1	1.24	1.621	1.642
	P4	53.8 ± 0.1	1.13	1.614	1.635
	P5	52.1 ± 0.5	1.10	1.620	1.644
	P6	51.9 ± 0.2	1.09	1.626	1.648
	P7	50.1 ± 0.3	1.06	1.618	1.648
	P8	47.6 ± 0.2	1.00	1.625	1.647
	P9	45.9 ± 0.2	0.97	1.629	1.651
200 ºC	**50 nm**	53.0 ± 0.1	1.12	1.639	1.658
	100 nm	103.1 ± 0.2	1.09	1.640	1.658

Figure 3.3 shows the refractive index, *n,* for all 200 ºC grown layers and 150 ºC grown layers over the wavelength range of 400 nm – 800 nm. The 200 ºC layers have a higher refractive index *n* than the 150 ºC ones, which is associated with a decrease in film density, as well as a higher impurity content for the lower temperature [11].

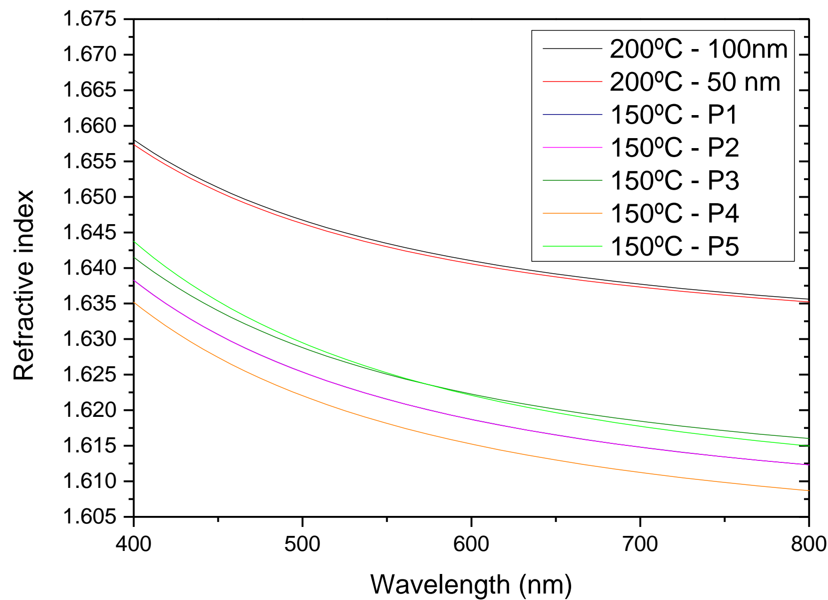


Figure 3.3. Refractive index for 50 nm and 100 nm Al_2O_3 layers that were grown at 200 ºC and 50 nm Al_2O_3 layers grown with 150 ºC low purge time processes.

Processes P1 and P2 appear to overlap in the plot which means the increase in purge time for H_2O did not result in any significant effect. Processes P3 and P5 have a slightly higher, similar *n*, while process P4 has the lowest *n* of the data, which can be related to a higher exposure time

to TMA, as the layer is exposed to more CH species provided by TMA. This overexposure is compensated with a larger purge time following TMA exposure in process P5. The higher *n* on P3 could be due to a decrease in CH impurity content, due to a higher H_2O exposure time.

Figure 3.4 shows a comparison between the 200 ºC layers and the high purge times processes P6 to P9. It is noticeable that these processes have a higher *n* when compared to the other 150 ºC processes, which means that the higher purge times removed impurities between each ALD cycle and overall contributed to higher densities, closer to the 200 ºC layers. The 150 ºC process with higher *n* was P9, which goes on par with FTIR results, by being the process that originates the layer that most resembles the layers from the 200 ºC process.

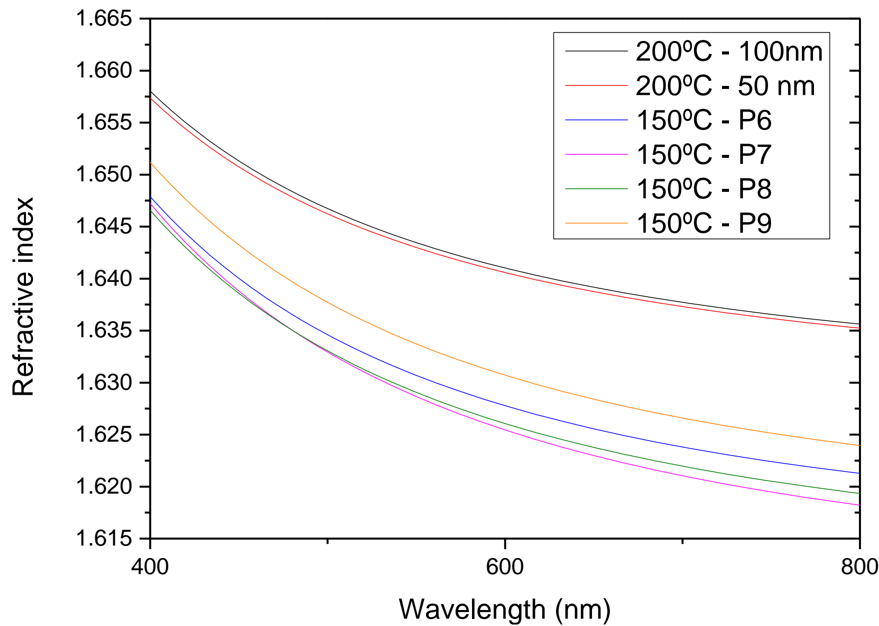


Figure 3.4. Refractive index for 50 nm and 100 nm Al_2O_3 layers that were grown at 200 ºC and 50 nm Al_2O_3 layers grown at 150 ºC with high purge time processes.

Comparing change in layer thickness throughout all substrates, we realize this change is always in the Å range and that the maximum error observed constitutes a change in less than 1% of thickness size, which demonstrates ALD as a technique for precise and uniform film growth. GPC is constant between all depositions, located around a 1 to 1.2 Å growth per cycle. Overall, the high purge time processes P6 to P9 have a lower GPC, as these purge times remove most of the unwanted species from the surface of the samples. Process P3 stands out as the process with higher GPC which can be justified by the higher exposure to H_2O. Overall, this set of refractive index is comparable with other works. [11], [20]

3.2 Electrical Characterization of MIM Structures

After the production of MIM structures, these were seen in an Olympus BX51 optical microscope to measure the sides and determine the area of these structures. Figure 3.5 shows a sample with 6 MIM structures which were numbered from 1 to 6 in increasing area size. Figure 3.6 shows an image of one MIM structure from an Olympus BX51 optical microscope used to measure the areas presented in Table 3.2. Average side and area dimensions of the different MIM structures. The results presented in the table are the average values for both the side and area of the different MIM structures, over four different samples.

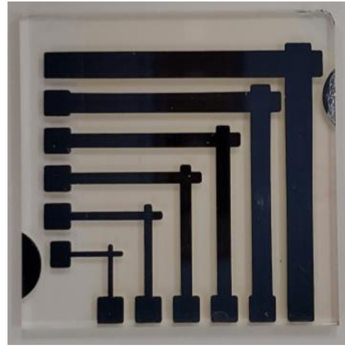


Figure 3.5. Alumina MIM structures produced over a 2.5 cm by 2.5 cm Corning glass substrate. Structures were numbered from 1 through 6, from the left to the right, by an increase in area size.

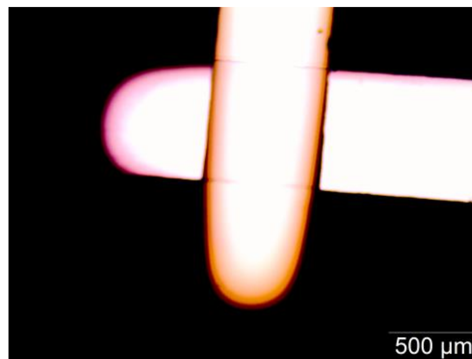


Figure 3.6. Optic microscope image of a number 2 MIM structure, with a horizontal bottom contact and a vertical top contact.

Table 3.2. Average side and area dimensions of the different MIM structures.

Device	S1	S2	S3	S4	S5	S6
Side (mm)	0.4	0.7	0.9	1.1	1.6	2.1
Area (mm^2)	0.17	0.44	0.85	1.20	2.58	4.42

To study the electrical properties of the produced devices, current-voltage (C–V) curves were used to find the oxide capacitance density C_{ox} as well as the dielectric constant κ, the main parameter used to choose the overall best process to use for dielectric production in oxide TFT process. I–V curves were used to find the breakdown field of the devices as well as leakage current. To find out how C_{ox} is affected with frequency, final C–f curves were performed on the best process.

3.2.1 C–V Curves

Figure 3.7 shows the capacitance-voltage characteristics, at a 100 kHz frequency, for MIM structures with a 100 nm dielectric grown at 200 ºC, which are similar to other C–V curves from all the optimization processes. Numbered curves S1 through S6 are associated with the structures in each glass substrate, S1 being the structure with the smallest area and S6 with the largest. Considering these MIM structures as parallel plate capacitors, it is expectable to see an increase in capacitance with area increase. However, when looking at the oxide capacitance density, there should be no correlation with area size.

Capacitance density curves were created from C–V curves by dividing the corresponding area of each MIM structure. Figure 3.8 shows capacitance density for the same set of samples and, as we can see, C_{ox} is independent of the area, within the error of 7 nF/cm^2. This correlation was verified for all sets of data, and no systematic trend was found.

Considering each MIM as a parallel plate capacitor, we determine κ, as shown in (3.1), considering d_{ox} as the dielectric layer thickness.

$$\kappa = C_{ox}\frac{d_{ox}}{\varepsilon_0} \tag{3.1}$$

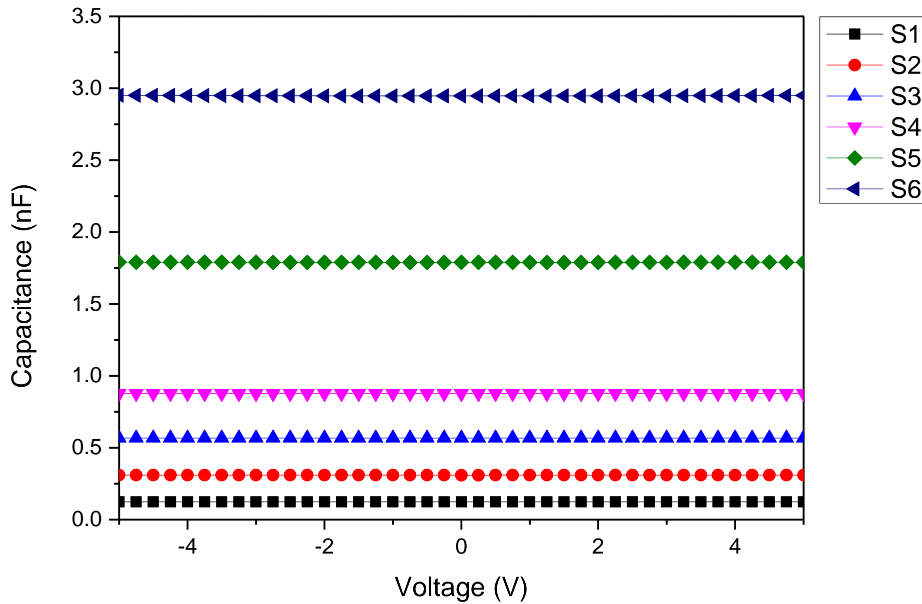


Figure 3.7. *C-V* curves for 6 MIM structures named S1 to S6, in the same substrate.

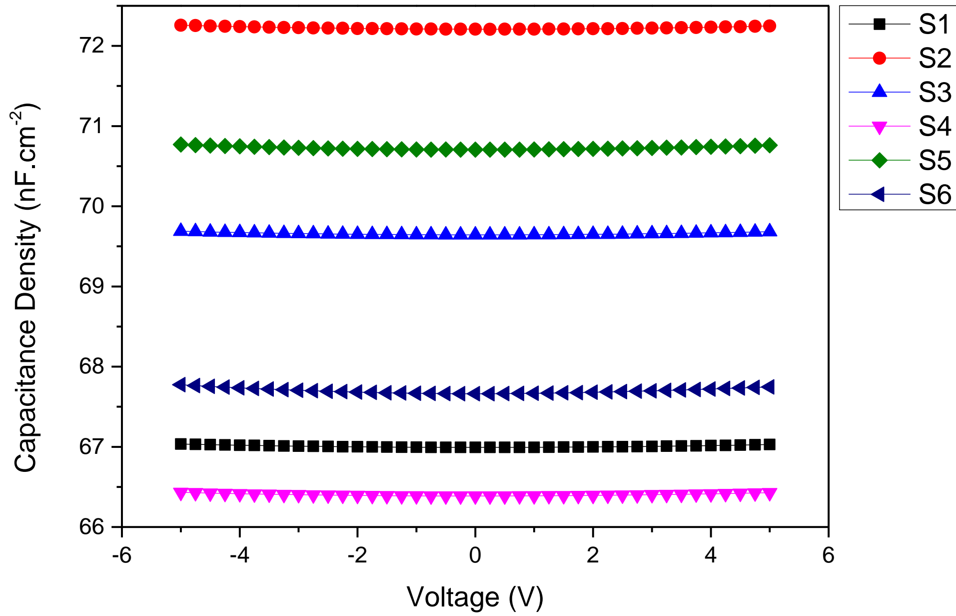


Figure 3.8. Capacitance density for 6 MIM structures named S1 to S6, in the same substrate.

Figure 3.9 compares C_{ox} between 50 nm and 100 nm layers both grown with the 200 ºC process and Figure 3.10 compares κ between these same layers. 50 nm have about double C_{ox} when compared to 100 nm, which is to be expected as the thickness is halved. κ is about the same for both sets of MIMs, which means there's not a visible correlation of κ with film thickness, within the error of 0.7 nF/cm^2. Overall these κ values for 200 ºC are on a par with the values found in other works for ALD amorphous Al_2O_3 grown at similar temperatures. [11], [21] The C_{ox} and κ values for the Al_2O_3 grown by the different 150 ºC processes can be found in Table 3.3.

Regarding the dielectric constant, the long purge time processes, P6-P9, show an improvement, when compared to the short time purge times, P1-P5. This is expected, as it has been already shown that longer purge times successfully remove more methyl groups from the surface, allowing more Al-O bonding. The effect of purge times can also be observed between processes P1 – P5 processes. Processes P2 and P5 have the same exposure times as P1 and P4, respectively, but they increase purge time for H_2O in the first case and TMA in the second one. This directly translates to an increase in κ from P1 to P2 and from P4 to P5. Processes P6 to P9 all have dielectric constants as high as the 200 ºC process, and comparable to other works, which would mean that any one of these processes could be considered. [11], [21]

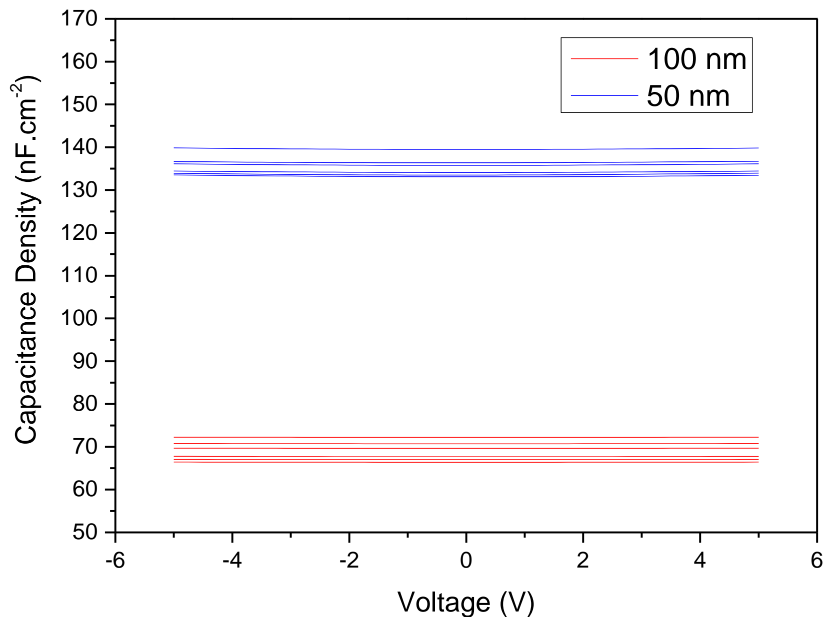


Figure 3.9. Capacitance density for 50 nm and 100 nm Al_2O_3 grown at 200 ºC.

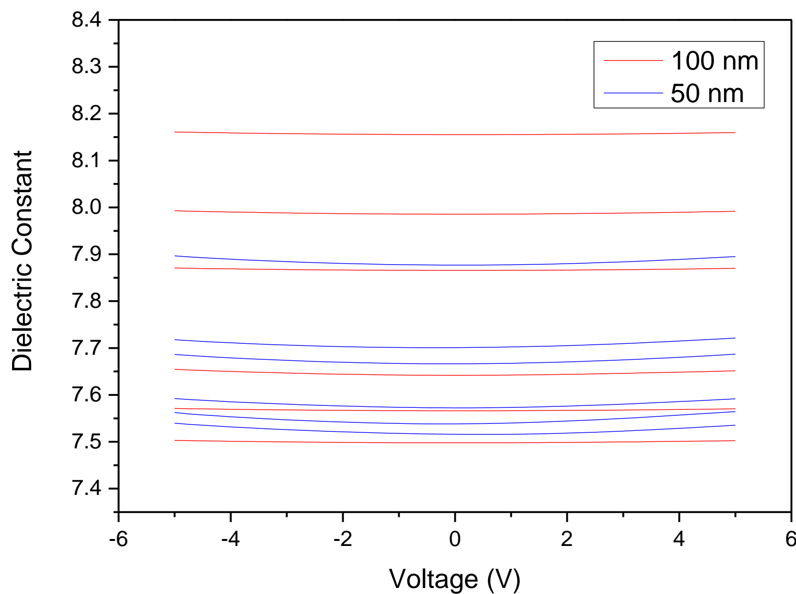


Figure 3.10. Dielectric constant for 50 nm and 100 nm Al_2O_3 grown at 200 ºC.

3.2.2 I–V Curves

After C–V, the current-voltage characteristics were determined for all dielectric layers. From standard I–V curves, as seen in Figure 3.11, a plot of current density was created as a function of electric field to easily determine leakage current density as well as the breakdown field. Figure 3.12 shows typically observed curves for the 150 ºC processes, showcasing 12 samples, across 2 substrates, for P3, in this instant. For this process in specific, most MIMs did

not hit breakdown while submitted to a maximum electric field of 8 MV/cm. The samples that did hit breakdown, were the larger area ones, for both substrates.

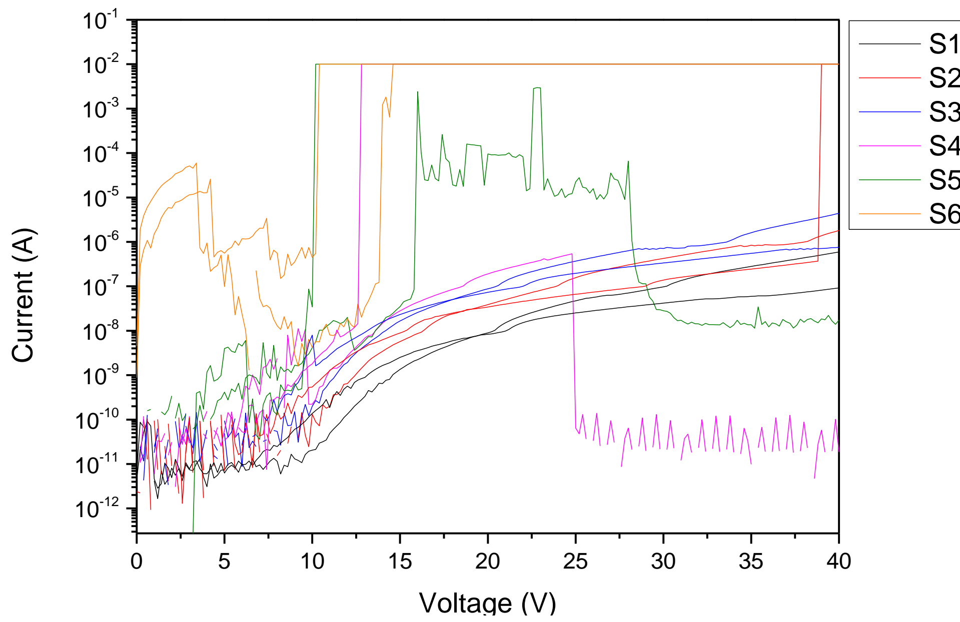


Figure 3.11. Current-Voltage curve for process P3 across 2 substrates, with 6 samples each.

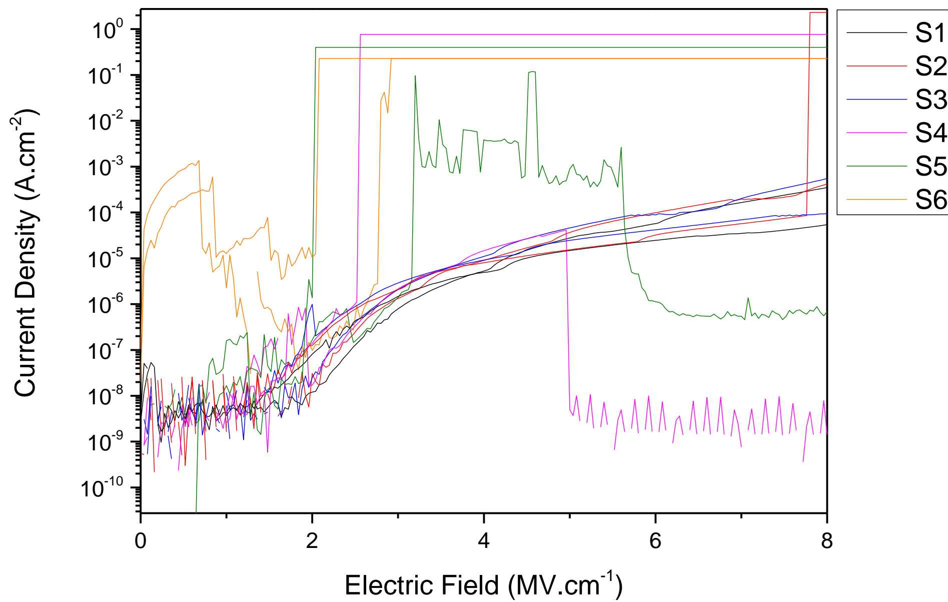


Figure 3.12. Current density as a function of electric field for process P3 across 2 substrates, with 6 samples each.

Overall, there is a slight tendency on larger area samples presenting a lower breakdown field. With larger areas, the presence of punctual defects is more likely and could lead to breakdown more rapidly. The average breakdown fields, as well as the leakage current densities are summarized in Table 3.3 for all dielectric layers.

Table 3.3. Electrical properties of Al_2O_3 layers for all ALD processes.

Temperature	**Layer**	**Breakdown Field (MV/cm)**	**Leakage Current Density at 1 MV/cm (A/cm^2)**	C_{ox} **(nF/cm^2)**	κ
	P1	7.8 ± 0.2	~ 1×10^{-7}	103 ± 21	5.8 ± 1.2
	P2	2.7 ± 0.9	~ 1×10^{-8}	130 ± 12	7.3 ± 0.7
	P3	5.4 ± 2.5	~ 5×10^{-9}	108 ± 7	6.1 ± 0.4
	P4	7.3 ± 0.9	~ 6×10^{-9}	116 ± 9	6.6 ± 0.6
150 ºC	**P5**	3.7 ± 1.6	~ 8×10^{-9}	136 ± 6	7.7 ± 0.3
	P6	4.1 ± 1.6	~ 1×10^{-8}	141 ± 7	7.9 ± 0.4
	P7	2.9 ± 1.2	~ 1×10^{-8}	151 ± 5	8.6 ± 0.3
	P8	3.8 ± 2.0	~ 1×10^{-8}	152 ± 6	8.6 ± 0.4
	P9	4.1 ± 2.2	~ 1×10^{-8}	149 ± 10	8.4 ± 0.6
200 ºC	**50 nm**	> 4	~ 2×10^{-8}	137 ± 3	7.7 ± 0.2
	100 nm	> 4	~ 2×10^{-8}	71 ± 3	7.8 ± 0.3

Breakdown fields for both 200 ºC layers were not registered, as the electric fields applied to these samples were only as high as 4 MV/cm. It is important to note that the 150 ºC samples were all submitted to a maximum bias of 40V, which translates into an electric field of 8 MV/cm. As some contacts did not reach breakdown upon reaching this point, to determine average breakdown field data it was considered that they reached breakdown at 8 MV/cm, which means that breakdown field values can be higher for some processes. Looking at the breakdown fields from processes P6 to P9, they are around 4 MV/cm, which is a similar value to other works [11]. Regarding leakage current density, most processes have values around 10 nA/cm^2 at 1 MV/cm which are comparable to the 200 ºC processes as well as other works. [11], [21]

Considering the electrical and optical properties of all the studied layers, the process chosen to implement into the second phase of this work was process P9. Although electrical results from processes P6 to P9 are very similar, the P9 layer has shown a higher n, as well as FTIR peaks similar to the 200 ºC, making it the most suitable process. While this process is the one with less precursor overall exposure time, making it more cost-effective, it does have a long process time, which in practical terms would not be very well suited for large batch productions and would thus require further optimization for that end.

A Capacitance-frequency analysis for all MIM structures produced with the optimized P9 process, Figure 3.13, shows that C_{ox} is relatively constant at values up to 100 kHz.

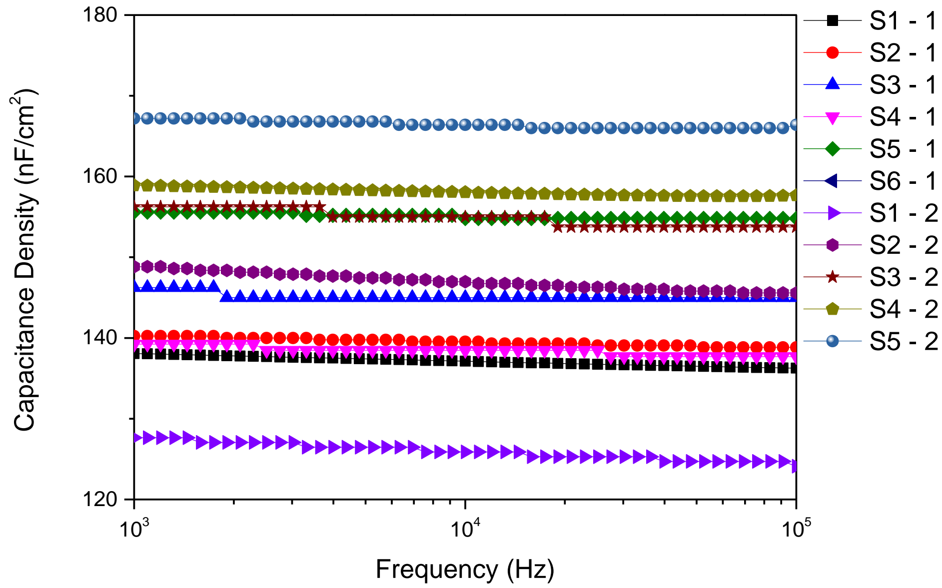


Figure 3.13. Frequency variation of capacitance density of Al_2O_3 films produced by process P9 in samples numbered 1 and 2.

3.3 Electrical Characterization of Oxide TFTs

Figure 3.14 showcases a top view of the structure design for top-gate TFTs produced. The right image allows visualization of the gate contact in white, the source and drain contacts, as well as the deposited IGZO layer in the intersection of these contacts. Al_2O_3 is not seen, as it is deposited all over the substrate, except for some parts of the metal pads to allow access to the bottom metal contacts. These images were used to determine channel width *W* and length *L* for all devices. In Figure 3.15, a schematic of the cross-section of the TFTs, shows the layer deposition in the top-gate staggered and bottom-gate staggered structures that were produced.

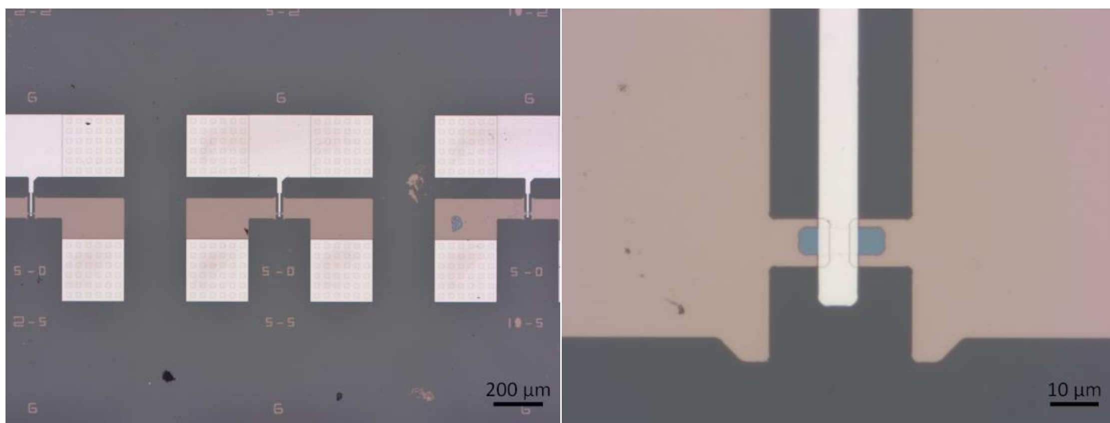


Figure 3.14. Optical microscope images of top-gate TFTs. The left image shows a set of TFTs and the right image shows the device channel for a 5 µm by 5 µm TFT.

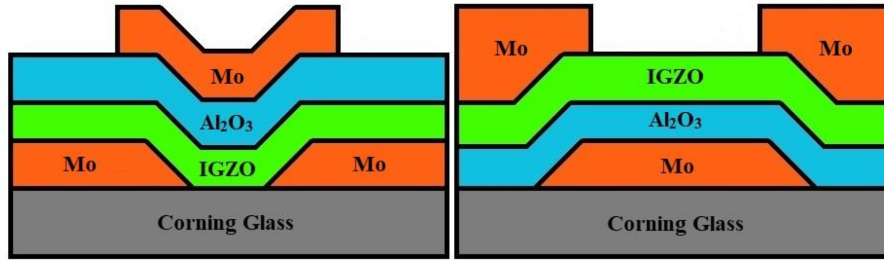


Figure 3.15. Schematic of the cross-section of the produced staggered top-gate (left) and bottom-gate (right) TFTs.

3.3.1 Transfer curves for TFT stabilization, in linear region and in saturation

Before proper characterization of the TFTs, a set of transfer curves is performed to normalize measurements between TFTs, to try to achieve device stabilization and comparable results among all the devices characterized. Figure 3.16 and Figure 3.17 show a set of 3 sweeps for W/L=20/20 (µm/µm) top-gate and bottom-gate devices, respectively.

It is important to mention that for 200 ºC devices, the maximum range of the V_G sweep was increased, from the 150 ºC sweep, to ensure that the maximum value for both mobilities was successfully extracted, which may not have happened for some of the bottom-gate 150 ºC TFTs. As such, a larger voltage shift for the 200 ºC devices should be related to the increased sweep and not directly with the fabrication process temperature.

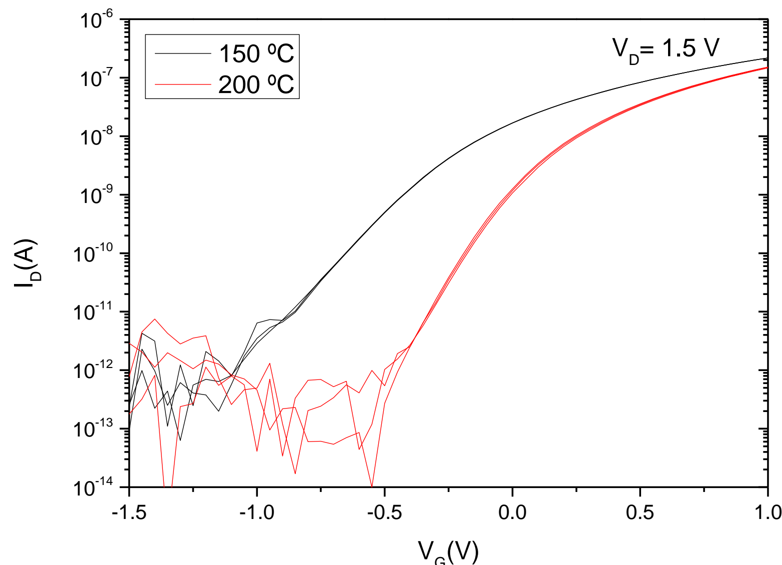


Figure 3.16. Transfer curves for device stabilization for 20 x 20 µm top-gate TFTs for both temperature processes.

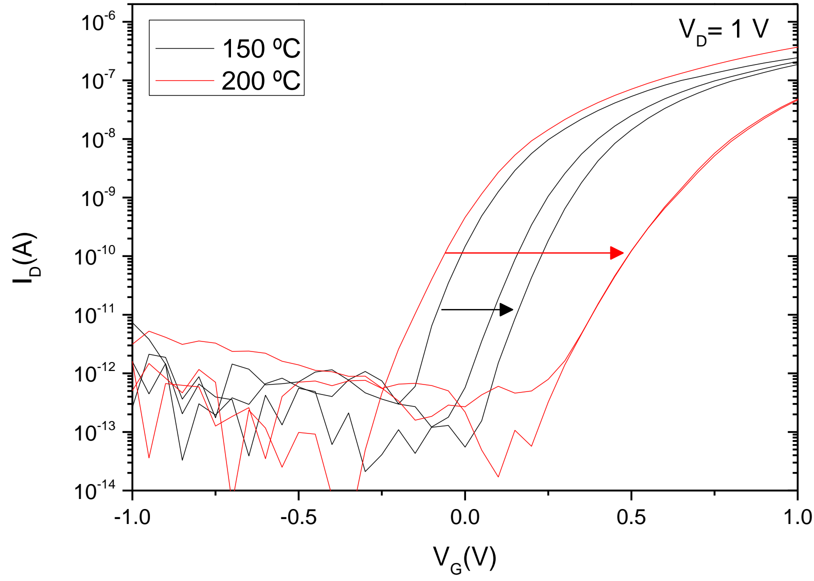


Figure 3.17. Transfer curves for device stabilization for 20 x 20 µm bottom-gate TFTs for both temperature processes. Arrows show the shift direction of the curves.

The top-gate TFTs show no voltage shift with the increasing number of sweeps, while the bottom-gate TFTs show a large shift, of up to 1 V. This phenomenon is caused by charge trapping in the dielectric/semiconductor interface and it translates into hysteresis in the transfer curves. Since top-gate TFTs, as seen in Figure 3.18, do not present a significant hysteresis in the transfer curves as the bottom-gate do, the ion bombardment from the sputtering process to the dielectric is the most likely cause for the hysteresis seen in bottom-gate TFTs, Figure 3.19. This kind of damage from sputtering in Al_2O_3 layers has already been reported by other authors. [15], [22] From these curves the turn-on voltage, V_{ON}, as well as the ON/OFF ratio were directly extracted. The subthreshold swing, *SS*, was also based on these curves, by determination of the subthreshold slope from (3.2).

$$SS = \left[\left(\frac{d \log I_D}{dV_G}\right)_{max}\right]^{-1} \tag{3.2}$$

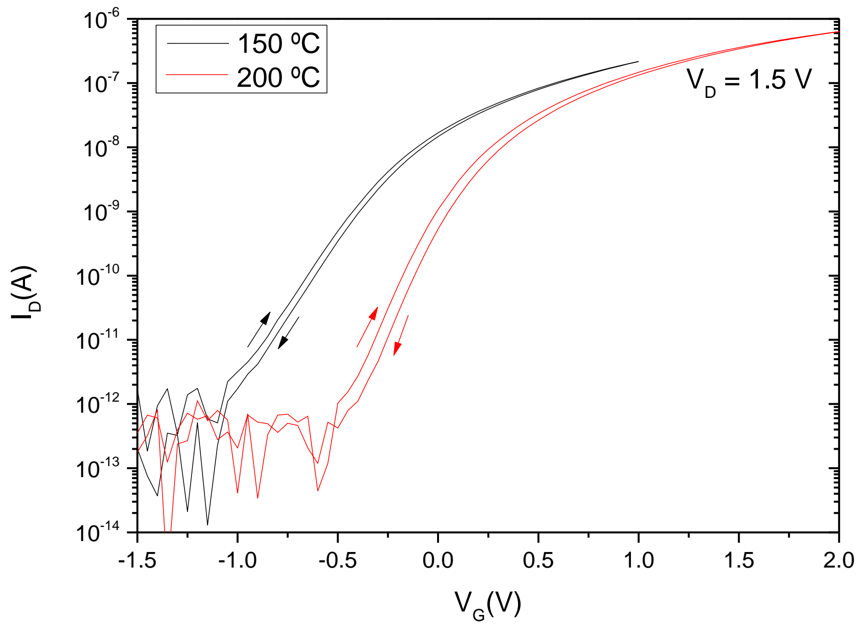


Figure 3.18. Transfer curves in saturation with a double sweep for top-gate TFTs.

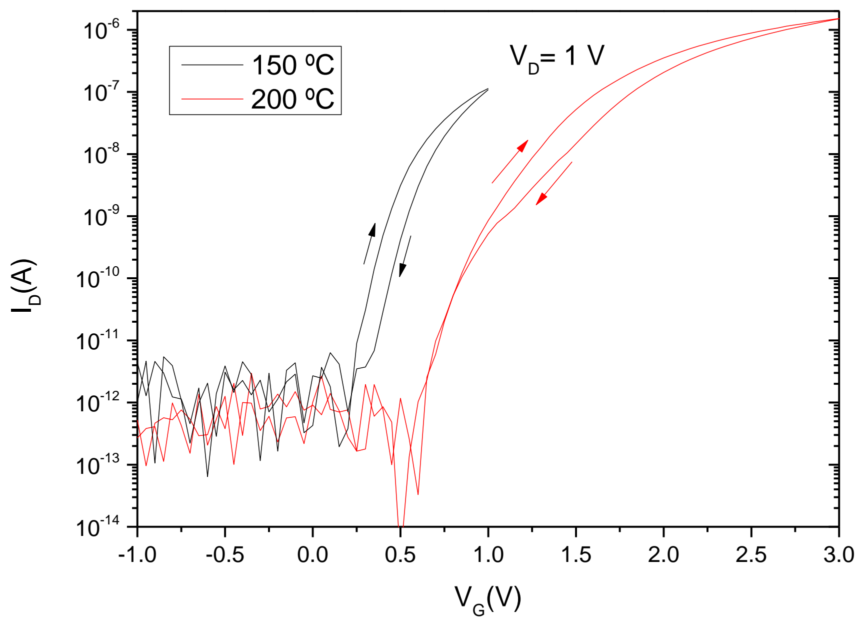


Figure 3.19. Transfer curves in saturation with a double sweep for bottom-gate TFTs.

3.3.2 Field-effect mobility and Transfer mobility determination methods

Field-effect mobility μ_{FE} was determined from the transfer curves in the linear region, considering the equation for I_D in this region, (3.3). The field-effect mobility is dependent on the derivative of I_D, the transconductance parameter g_m, as well as the W/L ratio, the oxide capacitance C_{ox}, which was previously determined, and the drain voltage V_D, as seen in equation (3.4).

$$I_{D,lin} = \frac{\mu_{FE} C_{ox}}{2} \frac{W}{L} \left[2(V_G - V_T)V_D - V_D^2 \right] \quad (3.3)$$

$$\mu_{FE} = \frac{g_m}{\frac{W}{L} V_D C_{ox}} \quad (3.4)$$

Saturation mobility is determined similarly, taking the equation for I_D in the saturation regime, (3.5), which, after derivation and term arrangement, leads to the equation (3.6).

$$I_{D,sat} = \frac{\mu_{sat} C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 \quad (3.5)$$

$$\mu_{SAT} = \frac{2 \left[\frac{d\sqrt{I_D}}{dV_G} \right]^2}{\frac{W}{L} C_{ox}} \quad (3.6)$$

The desired values for mobility are the points in which the derivative is at its highest and so a plot of both mobilities for both TFT structures was done. A μ_{FE} plot is shown in Figure 3.20 for 9 bottom-gate devices using the 150 ºC process, 3 for each size. Similarly, a μ_{sat} plot is shown in Figure 3.21 for 9 top-gate devices with a 200 ºC dielectric.

The values for both these properties are presented in Table 3.4 for all device sizes and in Table 3.5 as an average of all considered devices in the next subsection, together with the discussion.

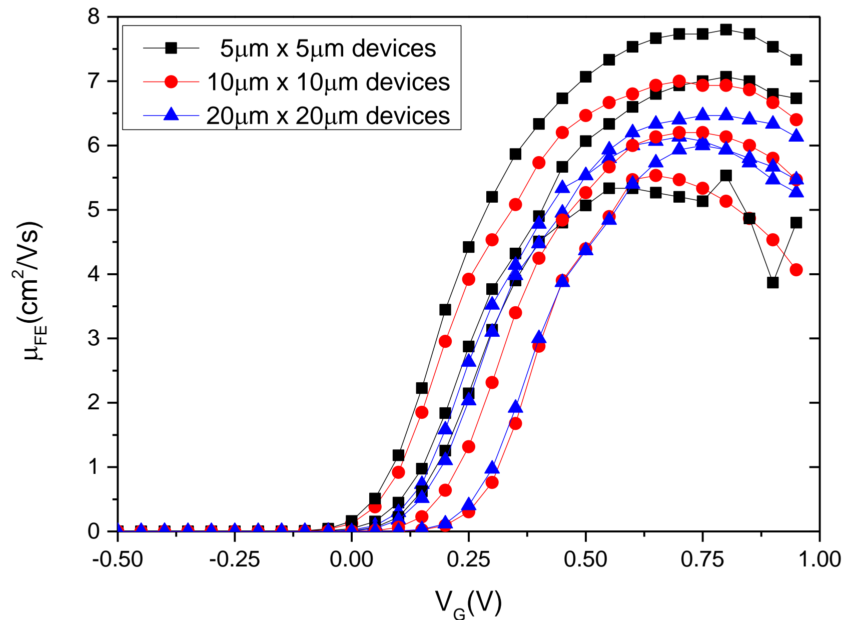


Figure 3.20. Field-effect mobility for 9 150 ºC bottom-gate TFTs sorted by their W and L sizes.

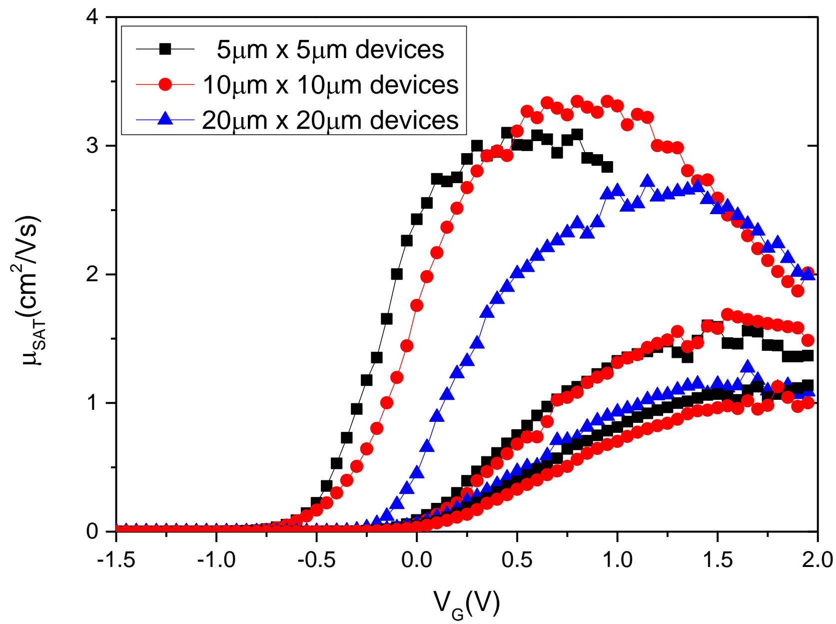


Figure 3.21. Saturation mobility for 9 200 ºC top-gate TFTs sorted by their W and L sizes.

3.3.3 Output characteristics

Output curves for different-sized devices are shown for top-gate TFTs and bottom-gate TFTs, with the 150ºC dielectric, in Figure 3.22 and Figure 3.23, respectively. Regarding top-gate TFTs, the observed curves are relatively standard, showcasing currents in the range of 100 nA in the saturation region for a V_G of 1V. When looking at the curves for the bottom-gate transistors, there is a slight oversaturation hump of the current upon reaching the saturation region, which can be explained by the aforementioned charge trapping caused by the IGZO sputtering. [15]

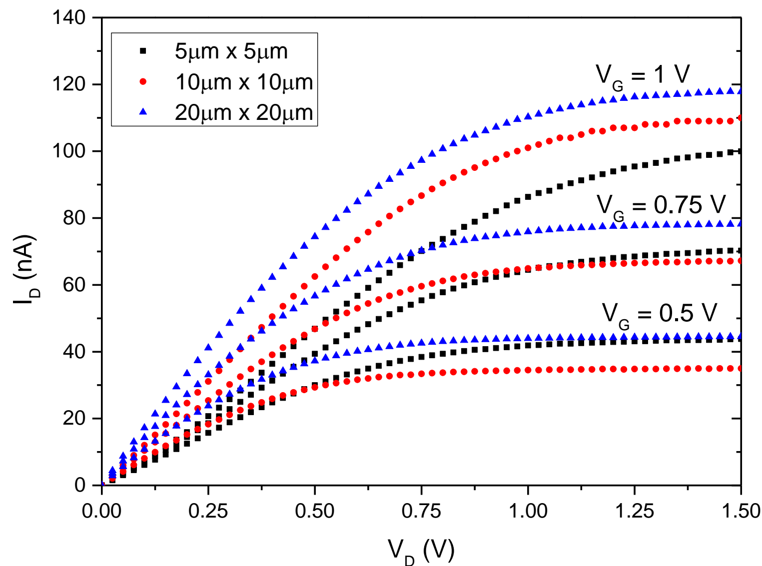


Figure 3.22. Output characteristics for 150 ºC top-gate TFTs for V_G = 0.6 V, 0.8 V and 1 V.

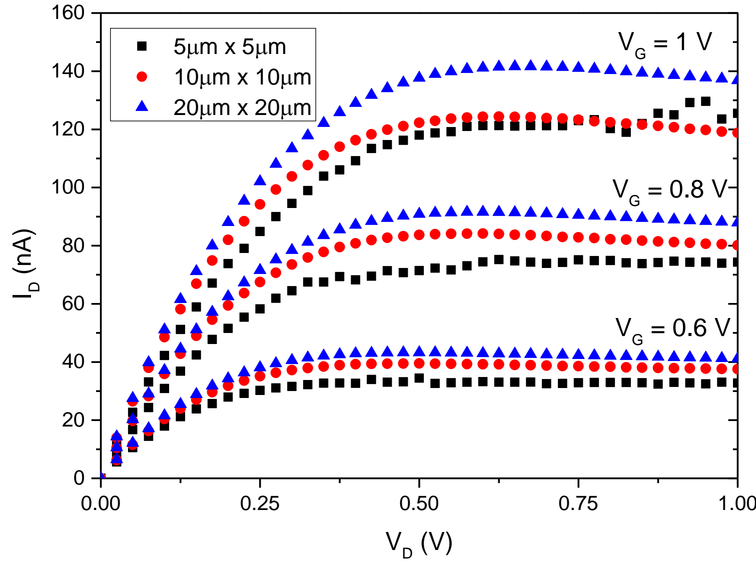


Figure 3.23. Output characteristics for 150 ºC bottom-gate TFTs for V_G = 0.5 V, 0.75 V and 1 V.

Considering the results shown in Table 3.4, it is noticeable that top-gate transistors all have a negative V_{ON}, which is around -1 V in 150 ºC TFTs and -0.6 V for the 200 ºC ones. The bottom-gate TFTs all have a V_{ON} around 0 V, which is ideal, despite the voltage shifts observed for the stabilization curves. As the negative value of V_{ON} is only observed for the top-gate transistors, it could be related to the effects of the Al_2O_3 deposition process on the IGZO/Al_2O_3 interface. Some works report that indium oxide films, when exposed to low-pressure processes, such as sputtering or ALD, are susceptible to change of oxygen content, as the interstitial oxygen concentration is dependent on its partial pressure and thus it may result in dissociation of oxygen [23–25]. As a result, there is a formation of In nanoparticles as well as adsorption of negatively charged OH^- at the surface, which could induce the V_{ON} observed. This alteration of surface conductivity and morphology could also explain lower values in mobility for the top-gate TFTs.

The top-gate transistors both have an average μ_{FE} and μ_{sat} around 1 cm^2/Vs, with the 200 ºC showing slightly better properties, for both parameters. For the 150 ºC TFTs these values slightly increase with increasing TFT size, which could indicate possible irregularities from the TFT production process. Bottom-gate TFTs have larger μ_{FE} and μ_{sat} than the top-gate transistors for both process temperatures. Comparing between the two temperatures, for the larger sized transistors, the 200 ºC TFTs attain a μ_{FE} up to 8 cm^2/Vs, slightly larger than the one observed for 150 ºC at around 6 cm^2/Vs, which is still a relevant value. It is important to mention that the smaller sizes for the 200 ºC TFTs have a substantial decrease in mobility with size decrease, which could also be related to irregularities during production. μ_{sat} values are, on the other hand, very similar between the two process temperatures, which is a good indicator that there was no substantial loss in quality, with temperature decrease. All these mobilities are relatively on par with some of the values reported for oxide TFTs, including ones that use Al_2O_3 as a gate dielectric. [1], [5], [6]

Table 3.4. μ_{FE}, μ_{sat}, and V_{ON} properties for all different devices, sorted by their size.

TFT structure	Device size (μm)	Temperature (ºC)	V_{ON} (V)	μ_{FE} (cm²/Vs)	μ_{SAT} (cm²/Vs)
Top Gate	5μm	150	-1.2 ± 0.2	0.4 ± 0.1	0.6 ± 0.3
		200	-0.7 ± 0.3	1.1 ± 0.6	1.0 ± 0.6
	10 μm	150	-0.9 ± 0.3	0.8 ± 0.1	1.1 ± 0.2
		200	-0.6 ± 0.1	1.4 ± 0.7	1.3 ± 0.7
	20 μm	150	-1.0 ± 0.2	1.2 ± 0.2	1.4 ± 0.3
		200	-0.6 ± 0.1	1.4 ± 0.6	1.2 ± 0.6
Bottom Gate	5μm	150	-0.01 ± 0.04	6.7 ± 0.8	7.2 ± 0.7
		200	-0.04 ± 0.23	0.2 ± 0.2	0.06 ± 0.02
	10 μm	150	0.06 ± 0.06	6.0 ± 0.5	6.1 ± 0.5
		200	0.36 ± 0.76	2.9 ± 0.9	1.7 ± 1.1
	20 μm	150	0.04 ± 0.13	6.0 ± 0.5	5.9 ± 0.4
		200	0.01 ± 0.21	8.1 ± 2.3	6.2 ± 1.8

Table 3.5 shows the average results for bottom-gate and top-gate transistors for V_{ON}, the ON/OFF ratio and *SS*. Regarding the ON/OFF ratio, the values do not differ much between TFT process temperatures and structures, although bottom-gate TFTs do have a slight edge. As for *SS*, for top-gate TFTs, we have 0.2V/dec and 0.1 V/dec for bottom-gate TFTs. Even though the ON/OFF ratio may not be as high as others reported, *SS* is relatively on par with other oxide TFTs. [1], [6]

Table 3.5. Average Top-gate and bottom-gate TFT properties for 200 ºC and 150 ºC Al_2O_3 processes.

TFT structure	Temperature (ºC)	V_{ON} (V)	ON / OFF ratio	*SS* (V/dec)
Top-Gate	150	-1.0 ± 0.25	≈ 10^5	0.23 ± 0.06
	200	-0.6 ± 0.17	≈ $10^5 – 10^6$	0.21 ± 0.03
Bottom-Gate	150	0.03 ± 0.09	≈ $10^5 – 10^6$	0.09 ± 0.01
	200	0.05 ± 0.48	≈ $10^5 – 10^6$	0.10 ± 0.01

Overall, comparing the results between the two structures produced for TFTs, there is a somewhat relevant difference between most parameters, as previously shown. However, when looking at devices with the same structure, produced at different temperatures, this difference between properties is not as significant. Even though devices produced at 200 ºC yield slightly better properties, 150 ºC TFTs still show relevant properties. This indicates that the decrease in temperature from 200 ºC to 150 ºC did not compromise the devices' characteristics and performance, which ultimately means that low-temperature ALD can provide a quality film with good dielectric properties.

3.3.4 Bias stress stability

A set of bias stress voltage curves was done at a later stage for two 150 ºC W/L=20/20 (µm/µm) devices, a top-gate and a bottom-gate TFT, to test these devices' electrical stability. Both devices were submitted to 60 minutes of stress using a gate voltage of 1 V and were allowed up to 100 minutes of recovery. Figure 3.24 shows the bias stress stability for the top-gate transistor. The voltage shift after 60 minutes of stress is minimal, which, along with the low hysteresis observed in the transfer curves, endorses the stability of the top-gate devices.

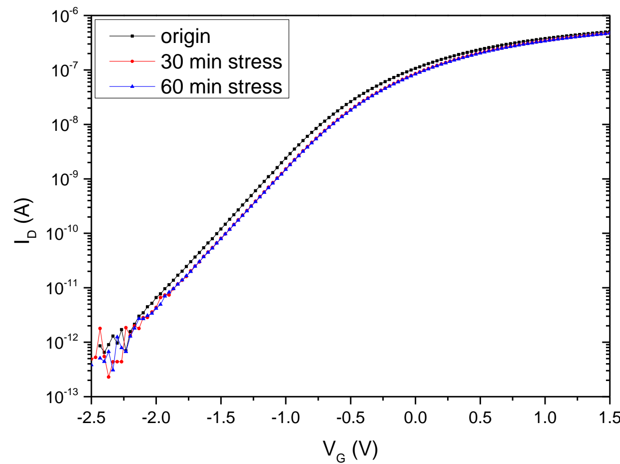


Figure 3.24. Bias stress stability of a 150 ºC top-gate TFT with an applied voltage of 1 V to the gate for 60 minutes.

When looking at the bottom-gate TFTs' results, showcased in Figure 3.25, there is a considerable positive bias shift of about 0.5 V after 60 minutes of stress, with 100 minutes being insufficient for the device's complete recovery. This shift is also coherent with the previously observed results from the bottom-gate devices, as it should be mostly related with the charge trapping at the interface that resulted from the IGZO sputtering

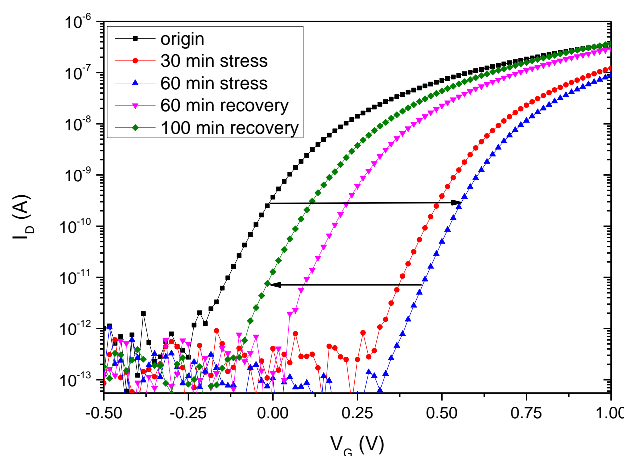


Figure 3.25. Bias stress stability of a 150 ºC top-gate TFT with an applied voltage of 1 V to the gate for 60 minutes, featuring a 100-minute recovery.

3.3.5 XPS analysis of the IGZO / Al_2O_3 interface

Along with the bias stress analysis, an XPS analysis was also done at a later stage to further study the IGZO/Al_2O_3 interface present in both the top-gate and bottom-gate TFTs. Figure 3.26 shows 3 spectra regarding In 3d emission. The samples to which correspond the top spectra and the middle spectra resemble the 150 ºC and 200 ºC top-gate TFTs, as they have Al_2O_3 from 150 ºC and 200 ºC processes respectively, deposited on top of IGZO. The bottom spectrum corresponds to a sample that resembles the bottom-gate TFT, as it has IGZO stacked on top of Al_2O_3. When comparing the three spectra, we notice a peak asymmetry in the top-gate stacks, not present in the bottom-gate stack. The fitting of the results was done using the sample that showed no peak asymmetry.

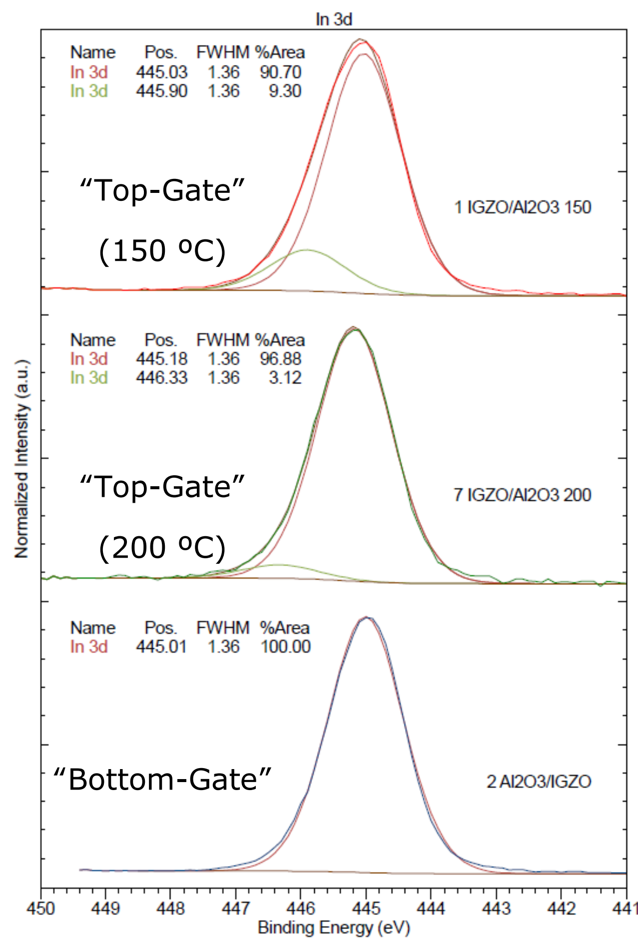


Figure 3.26. XPS analysis of three IGZO/Al_2O_3 interfaces in In 3d emission. The top two spectra correspond to samples in which Al_2O_3 grown at 150 ºC and 200 ºC is stacked on top of IGZO, while IGZO is stacked on top of Al_2O_3 for the last sample.

When comparing the top-gate 150 ºC and 200 ºC samples, the asymmetric peak has a lower intensity in the 200 ºC sample, as well as a larger shift toward a higher binding energy. As the binding energy increases, there's a decrease in the kinetic energy of the photoemission electron, represented by the peak intensity, which has previously been observed [26]. This energy loss is

related with the carrier concentration in the interface as these carriers interfere with the free electrons, resulting in a broader and less intense photoemission.

These results can be linked with the conductivity on the interface, as the bottom-gate stack has no peak asymmetry, which would mean a higher conductivity and would explain the higher mobility values registered for bottom-gate TFTs. The top-gate stacks, which show this asymmetry would be, therefore, less conductive, which would explain the lower mobility values when compared to the bottom-gate. As the 200ºC stack has a lower intensity asymmetric peak than the 150 ºC stack, the conductivity would be lower in the 200 ºC devices, which matches the slightly lower values of mobility of the 200 ºC top-gate TFTs when compared to the 150 ºC top-gate TFTs.

This sub-peak asymmetry can also be related to precursor waste on the interface and to the negative values of V_{ON} in the top-gate TFTs. As it was previously mentioned, the 150 ºC depositions can have more remnants of precursor, when compared to the 200 ºC depositions due to a lower reactivity of the water molecules at lower temperatures, and this presence is visible in the FTIR analysis (Figure 3.2) in the C–H groups, which are related to the methyl groups present in the TMA. The presence of precursor remnants in the sample can be linked with the higher intensity of the asymmetric peaks. The incomplete conversion of the precursor could lead to doping of the semiconductor, which could in turn explain the values observed for V_{ON}, more negative in the 150 ºC top-gate devices (Figure 3.18).

4 Conclusions and Future Perspectives

Atomic Layer Deposition is a staple in deposition techniques as its alternating gas pulses guarantee a self-limited thin film growth throughout a substrate. As a result, ALD-grown films have very good uniformity and conformality, as well as very precise thickness, over a wide range of temperatures. ALD can be performed at temperatures as low as room temperature, which makes this technique very suitable for depositions in substrates with a limited thermal budget. This fact along with its ability to deposit oxides with *high-κ* makes this process a very suitable candidate for flexible thin-film technology.

In this work, optimization of a thermal ALD process for deposition of Al_2O_3 at a low temperature of 150 ºC is reported, with the primary goal of implementation of the dielectrics in an oxide TFT process, for low-temperature applications. This is the first reported use of atomic layer deposition at FCT-UNL. The initial focus was the study of optical and electrical properties of Al_2O_3 layers to find an optimal 150 ºC process, which, on a second phase, was used to grow the gate dielectrics in bottom-gate and top-gate IGZO TFTs.

The 150 ºC optimized layers show good optical and electrical properties, which are comparable to other low temperature grown Al_2O_3 layers. These include a refractive index of 1.63 at 635 nm, a breakdown field around 4.1 MV/cm, leakage current density at around 10 nA/cm^2, and a dielectric constant around 8.4.

Both bottom-gate and top-gate TFTs were produced, for 150 ºC and 200 ºC processes. Overall bottom-gate TFTs present better properties than the top-gate TFTs, with μ_{FE} around 6 cm^2/Vs, a *SS* at around 0.1 V/dec, and V_{ON} close to 0 V. These devices, however, show a high hysteresis due to trapped charges at the interface, as a result of the sputtering process. Top-gate TFTs show almost no hysteresis, although they present μ_{FE} and μ_{sat} at 1 cm^2/Vs, a *SS* around 0.2 V/dec, and a negative V_{ON} due to arising negative charges from the ALD process.

Regarding the same structured TFTs for the 150 ºC and 200 ºC processes, 150 ºC dielectrics can show results just as good as 200 ºC dielectrics, with a slight decrease in some properties. This means that the optimized Al_2O_3 ALD 150 ºC process is a suitable candidate for use in low-temperature thin-film electronics.

A later study regarding bias stress voltage for the electrical stability of the devices was performed on the 150 ºC transistors and it corroborated some comments regarding previous results: top-gate transistors have almost no voltage shift, whereas bottom-gate transistors have large voltage shifts, as a result of the damage from the sputtering process, with a 100 minute recovery proven insufficient for full recovery of the device.

A later XPS study on the dielectric/semiconductor interface showed a peak asymmetry and decrease in intensity in the interface stack reminiscent of the top-gate TFTs. This can be related, on the one hand, with a decrease in conductivity of the top-gate TFTs, which would explain their lower mobility values. On the other hand, this asymmetry can be linked to the presence of more

precursor remnants on the low temperature dispositions, as it could lead to doping of the semiconductor, and thus to the more negative values of V_{ON}.

A future improvement of this process would firstly focus on overall process time reduction. While it keeps precursor consumption to a minimum, the cost-effectiveness of the optimized process is hindered by the large process time coming from the large purge steps required for 150 ºC ALD. An immediate way to improve the process time would be to gradually reduce the purge times after precursor TMA exposure and then the purge times after co-reactant H_2O exposure, which is the most critical for quality films at this temperature, to try and find a compromise between process time and the quality of the dielectric films.

A study of the dielectric layer for thicknesses other than 50 nm to implement in TFTs could also be conducted with the main goal of reducing the process time, by trying a different number of cycles for ALD deposition and also finding a compromise between decreased oxide thickness and its properties.

Finally, as the focus was on working with a limited thermal budget for temperature-sensitive substrates, it would be interesting to implement one of these materials as a substrate for the TFT process, to ascertain the electrical properties of the TFTs on these substrates, as well as to analyze the reliability of the device stack under mechanical stress.

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Annexes

Annex 1 Shadow Mask for MIM structures

E-beam evaporation for the Aluminum contacts on the MIM structure was mad using a shadow mask represented in Figure A.1. This mask allowed for simultaneous deposition of metal contacts for a total of 4 samples. In order to obtain the right pattern for the MIM structures, the bottom 2 samples would switch places with the top 2 between depositions.

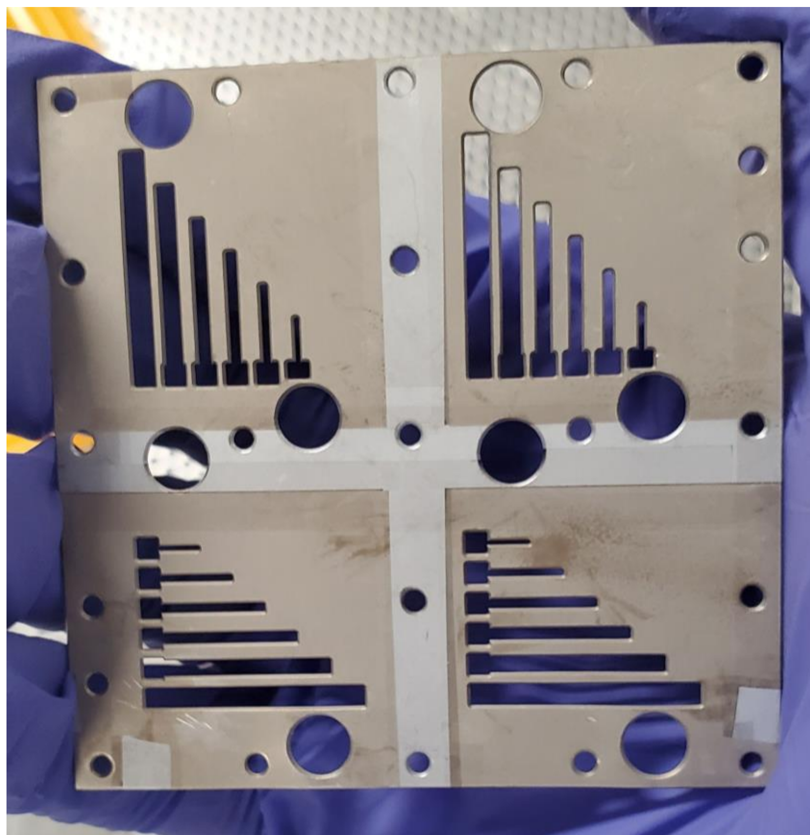

Figure A.1. Shadow mask used for the MIM metal contacts e-beam evaporation.

Annex 2 TFS-200 Recipe for Aluminum Oxide ALD

The following recipe is the standard recipe provided by Beneq for 50 nm of Al_2O_3 ALD at 200 ºC. Deposition parameters were changed by altering values in this recipe, namely the temperature at line 46, the number of cycles at line 57 and the exposure and purge times for precursor at lines 59, 60, and for co-reactant at lines 62 and 63. For 100 nm deposition, the number of cycles is doubled.

	Al2O3 50nm
1	*Recipe Al203 50 nm
2	*Recipe for 50 nm Al2O3
3	*Precursors TMA and Water by own vapor pressures
4	*Mim, 2008 1 July
5	*Based on flow chart N503256
6	*TMA at liquid source 2
7	*Water at liquid source 4
8	*Source needle valves (NV-PL4 open 1 turn, NV-PL1 open 1 turn)
9	*Reactor temperature 200
10	
11	*Program start
12	SPROG
13	
14	*Close Glove box valve
15	CLOSE DV-GB1
16	
17	*Open the N2 main valve and chamber flow valve and make sure filing valve is closed
18	OPEN DV-SN1,DV-NV2
19	CLOSE DV-NV1
20	
21	*Open main vacuum valve
22	OPEN DV-VP1
23	
24	*Set flows
25	FLOW MFC-NOVS=250
26	FLOW MFC-NOPS=600
27	
28	*Close pulse valves
29	CLOSE DV-PL1,DV-BL1
30	CLOSE DV-PL2,DV-BL2
31	CLOSE DV-PL3,DV-BL3
32	CLOSE DV-PL4,DV-BL4
33	CLOSE DV-PH1,DV-BH1,DV-BHA1
34	CLOSE DV-PH2,DV-BH2,DV-BHA2
35	
36	*Close process gas valves

```
37  CLOSE DV-PN1
38  CLOSE DV-PG1
39  CLOSE DV-PG7,DV-PG8
40  CLOSE DV-PG1C
41
42  *Check the vacuum level
43                      WUNTIL PT-P1<10 10s
44
45  *Set temperatures
46                      TEMP TE-R1S=200
47
48  *Wait until temperature is ok
49                      WUNTIL TE-R1>TE-R1S 5h
50
51  *Are temperatures ok to start process ?
52  WRITE M5
53  WUSER YES
54
55  *Pulsing TMA and Water 950 cycles, appr. 100 nm
56
57  REPEAT 475
58
59                      Pulse DV-PL2 150ms
60                      Purge 650ms
61
62                      Pulse DV-PL4 150ms
63                      Purge 1s
64
65  REND
66
67  *Set temperatures
68                      TEMP TE-R1S=10
69
70  *Close pulse valves
71  CLOSE DV-PL1,DV-BL1
72  CLOSE DV-PL2,DV-BL2
73  CLOSE DV-PL3,DV-BL3
74  CLOSE DV-PL4,DV-BL4
75  CLOSE DV-PH1,DV-BH1,DV-BHA1
76  CLOSE DV-PH2,DV-BH2,DV-BHA2
77
78  *Close process gas valves
79  CLOSE DV-PN1
80  CLOSE DV-PG1
81  CLOSE DV-PG7,DV-PG8
82  CLOSE DV-PG1C
```

```
83
84  *Close precursor hand valves
85  WRITE M7
86  WUSER YES
87
88  *Confirm that all precursor hand valves are closed
89  WRITE M22
90  WUSER YES
91
92  *Start TMA line purge
93  WRITE M39
94  WUSER YES
95
96  PULSE DV-PL2 2min
97  PULSE DV-BL2 2min
98
99  *End program
100 EPROG
```