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Wideband CMOS Receiver

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Wideband CMOS Receiver

To my family and friends.

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Abstract

In this thesis a wideband radio frequency (RF) receiver, with integrated filtering that can be precisely controlled by the local oscillator (LO) frequency to attenuate out-of-band interferers, is presented. Two key blocks of the receiver are studied: low-noise amplifier (LNA) and mixer. The LNA consists in a widely tunable narrowband balun-LNA with integrated high-Q bandpass filters (BPF), which allows the attenuation of undesired interferers that can corrupt the desired signal. The mixer is a passive current-driven circuit that also performs filtering, due to its impedance transformation properties. For the LNA, developed in 130 nm, simulation results show a voltage gain higher than 23.8 dB, a noise figure (NF) lower than 3.3 dB, an $IIP_2 > 22$ dBm and an $IIP_3 > -4$ dBm, for a working band between 0.3 GHz and 1 GHz with a power consumption of 3.6 mW. Regarding the receiver analog front-end (AFE) it was obtained a NF lower than 10 dB, for intermediate frequencies (IF) of interest, and an IIP_3 of 0.23 dBm.

To convert the IF signal at the mixer's output to the digital domain a current-mode sigma-delta ($\Sigma\Delta$) modulator is employed. Since the $\Sigma\Delta$ was implemented using CMOS 65 nm technology, the studied receiver was redesigned in this technology to allow the full integration of the receiver. Operating at full scale, the $\Sigma\Delta$ modulator shows a $SNDR = 36.9$ dB and an $ENOB = 6.2$ bits.

Keywords: High-Q BPF, N-path filter, widely tunable LNA, SAW-less receiver, current-mode $\Sigma\Delta$ modulator, RF receiver.

Resumo

Neste trabalho foi desenvolvido um recetor de rádio frequência (RF) de banda larga, com filtros integrados que podem ser sintonizados através da frequência do oscilador, para atenuar interferentes indesejados. Foram estudados dois blocos cruciais do recetor: *low-noise amplifier* (LNA) e misturador. O LNA consiste num balun-LNA de banda estreita com filtros integrados, que permite a atenuação de sinais interferentes que podem corromper o sinal desejado. O misturador consiste num circuito passivo que funciona em modo de corrente e que, devido às suas propriedades de transformação de impedâncias, também atua como filtro. Relativamente ao LNA, desenvolvido em CMOS 130 nm, foi obtido um ganho de tensão maior do que 23.8 dB, uma *noise figure* (NF) menor do que 3.3 dB, um $IIP_2 > 22$ dBm e um $IIP_3 > -4$ dBm, para uma banda de funcionamento entre 0.3 GHz e 1 GHz e um consumo de potência de 3.6 mW. Relativamente ao *analog front-end* (AFE) do recetor foi obtida uma NF menor do que 10 dB, para as frequências intermédias (IF) de interesse, e um IIP_3 igual a 0.23 dBm.

Para converter o sinal à saída do misturador para o domínio digital foi utilizado um modulador $\Sigma\Delta$ que funciona em modo de corrente. Como o $\Sigma\Delta$ foi desenvolvido em CMOS 65 nm foi necessário redesenhar o recetor nesta tecnologia para ser possível obter um recetor completamente integrado no mesmo chip. À saída do $\Sigma\Delta$ foi obtido um $SNDR = 36.9$ dB e um $ENOB = 6.2$ bits, a operar em *full-scale*.

Palavras-chave: Filtros passa-banda com elevado Q, filtros *N-path*, LNA sintonizável, recetor *SAW-less*, modulador SD de modo de corrente, recetor de RF.

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Acronyms

ADC Analog-to-Digital Converter

AFE Analog Front-end

BOM Bill of Materials

BPF Bandpass Filter

CB Current-Buffer

CG Common-Gate

CS Common-Source

DFT Discrete Fourier Transform

FFT Fast Fourier Transform

GSM Global System for Mobile Communications

HPF Highpass Filter

IC Integrated Circuit

IF Intermediate Frequency

IM Intermodulation

IP_2 Second-order Intercept Point

IP_3 Third-order Intercept Point

KCL Kirchhoff's Current Law

KVL Kirchhoff's Voltage Law

LNA Low-Noise Amplifier

LO Local Oscillator

LPF Low-pass Filter

NF Noise Figure

P_{1dB} 1 dB Compression Point

PSD Power Spectral Density

QAM Quadrature Amplitude Modulation

RF Radio Frequency

$\Sigma\Delta$ Sigma-delta

SNDR Signal-to-noise and Distortion Ratio

SNR Signal-to-noise Ratio

SoC System on Chip

TIA Transimpedance Amplifier

1

Introduction

1.1 Background and Motivation

With the evolution of wireless communications, the use of wireless devices had an huge increase in the last years. These kind of communications avoids the need of a physical connection between the multiple devices, reducing the overall system costs and area occupation, which is an huge advantage comparing with traditional (wired) systems. Due to these systems' popularity there is a large interest in create compact, functional and low power devices with low cost. Contrary to other technologies, the CMOS (Complementary Metal–Oxide–Semiconductor) technology allows the development of low cost and low power circuits that can operate at high frequencies. It also enables the circuit full integration in the same die (System on Chip (SoC)), avoiding the need to match the various Radio Frequency (RF) circuits' inputs and outputs, to allow the maximum power transfer between them, and the parasitic effects due to off-chip electrical connections at high frequencies [1, 2].

One of the most interesting RF receivers topologies is the low-IF (Intermediate Frequency), since it allows the receiver full integration and avoids problems related with flicker noise, intermodulation, among others [3]. This kind of receiver has three key blocks: Low-Noise Amplifier (LNA), Local Oscillator (LO) and mixer. The LNA has the purpose of amplify the RF receiver's input signal introducing almost no noise, since this block noise contributions have an huge influence in the overall receiver Noise Figure (NF). There are two main types of LNAs: narrowband and wideband. Narrowband LNAs are low noise but are limited to one specific frequency, occupy a large area, due to the use of reactive components to perform the impedance matching, and require a technology with RF options, to have inductors with high Q factor. On the other hand,

wideband LNAs support multiple frequencies but have, typically, a large NF and need to guarantee the proper impedance matching over the entire working band. These kind of LNAs can also be achieved by using multiple narrowband LNAs, with very low NF, but that occupy a large area and have high power consumption. More recently, wideband LNAs that employ noise and distortion canceling techniques [4, 5] have been proposed, which can have NFs below 3 dB and occupy a small area.

The mixers are divided in two main groups: actives and passives. Active mixers can provide gain, reducing the overall receiver NF, but have an high power consumption and occupy a large die area. Passive mixers do not provide gain but are very small and low power. Recently, current-driven passive mixers have become very popular due to their high linearity, low noise and interesting impedance transformation properties [1]. These kind of mixers require a Transimpedance Amplifier (TIA) at the output, to convert the Intermediate Frequency (IF) signal to a voltage signal that can be processed by a typical Analog-to-Digital Converter (ADC). However, a new sort of ADCs has been emerging [6], that allows to convert a current signal directly to the digital domain, avoiding the use of a TIA that occupies die area and add more noise to the receiver.

In order to minimize interferers that can corrupt the desired receiver's input signal, mainly by saturating the LNA, new filtering techniques [7–10], based in current-driven mixers, have been recently employed. Since these filters are passive, they can be easily integrated in the receiver, avoiding the use of external filters that occupy a large area and have an high cost.

The main goal of this work is to design a complete wideband RF receiver Analog Front-end (AFE) (except the LO) that employs the previously mentioned filtering techniques to attenuate interferers that can affect negatively the overall circuit performance. Also, to avoid the use of a TIA at the output of the current-driven mixer, a current-mode Sigma-delta ($\Sigma\Delta$) modulator [6] is used to directly convert the IF signal to the digital domain. The receiver blocks were employed in CMOS 130 nm and CMOS 65 nm.

1.2 Thesis Organization

This thesis is organized in six chapters, including this introduction, as follows:

Chapter 2 – Receiver Architectures and RF Blocks
This chapter introduces some basic concepts and definitions that are usually employed in a RF receiver. It also reviews the key receiver architectures, including the low-IF, which is used in this work, and presents an overview of the studied receiver blocks (LNA, mixer, filters and ADC).

Chapter 3 – Wideband Cascode Balun-LNA
The circuit studied in this chapter consists in a wideband cascoded balun-LNA, which performs conversion from single-ended to differential. This circuit employs noise and

distortion canceling techniques that allows to reduce its noise contributions. Also, to increase the voltage gain and reduce the NF, the traditional load resistors are replaced by active devices. The main purpose of the cascode stages is to allow the integration of a filter, studied in chapter 4, in the LNA nodes. First, all the theoretical expressions (input impedance, load impedance, voltage gain and noise factor) of the LNA are derived and then the circuit is simulated using both CMOS 130 nm and CMOS 65 nm technologies. Finally, both technologies are compared.

Chapter 4 – High-Q Bandpass Filter

In this chapter a high-Q Bandpass Filter (BPF), based in a current-driven passive mixer, is reviewed. This filter performs impedance transformation that allows to shift a baseband impedance to the input node, transforming a low-Q Low-pass Filter (LPF) in a high-Q BPF. The circuit is intended to be used at the LNA nodes, to attenuate interferers that are located outside of the input signals band. This filter is developed in two versions, single-ended and differential, that will be employed according to the LNA nodes characteristics. First, the filter theoretical expressions are analyzed in order to understand its behavior and then the circuits are simulated in order to validate the obtained equations. Finally, some considerations about its functioning are made.

Chapter 5 – Complete Receiver

In this chapter the full RF receiver is presented. The LNA with integrated filtering is simulated and compared with the LNA of chapter 3, to understand the advantages and disadvantages of this technique. This analysis is made for CMOS 130 nm and CMOS 65 nm. The current-driven passive mixer, that also has filtering properties, is studied and then integrated in the full receiver, developed in 130 nm, with an ideal TIA block connected to the mixer's output. To avoid the use of a TIA, a new receiver architecture is presented, employed in 65 nm. This receiver has a current-mode $\Sigma\Delta$ modulator connected to the mixer's output, to perform the conversion of the IF signal directly to the digital domain. The interface between the mixer and the $\Sigma\Delta$ is made through a Current-Buffer (CB) that allows to amplify/attenuate the IF signal so that the $\Sigma\Delta$ can operate at maximum performance. All the circuits are validated through simulation.

Chapter 6 – Conclusions and Future Work

Finally, this chapter discusses the obtain results and presents further research suggestions.

1.3 Main Contributions

A current-mode receiver architecture, integrated in a single chip, is employed to overcome the problem created by interferers that can be located near the circuit's operating

frequency. To achieve the desired interferers attenuation, it was designed a widely tunable narrowband balun-LNA with integrated filtering that consists in the LNA and the high-Q BPF of chapters 3 and 4, respectively, avoiding the use of external filters that increase the overall circuit cost and area. To convert the desired signal to the digital domain a current-mode $\Sigma\Delta$ modulator is used. The main advantages of this receiver are the interferers attenuation, the reduced number of AFE blocks and its easy integration in the same chip.

This work has originated a paper titled "A Widely Tunable Narrowband Balun-LNA with Integrated Filtering" [11], presented at 2014 Mixed Design of Integrated Circuits & Systems (MIXDES).

2

Receiver Architectures and RF Blocks

The main purpose of this chapter is to introduce basic concepts related with RF electronics and to do an overview of receiver architectures and the RF front-end key blocks.

First, the basic concepts are introduced and the advantages and disadvantages of the different receiver architectures are described. Then, the basic aspects of LNAs, filters, mixers and ADCs are reviewed in order to understand their importance and how they can be integrated in a receiver AFE.

2.1 Basic Concepts

2.1.1 Impedance Matching

Lumped circuit analysis assumes that the physical dimensions of the network are much smaller than the electromagnetic wavelength and therefore the voltage and current do not vary significantly over the physical dimension of the elements. However, at high frequencies the network dimensions tends to be of the same order or even bigger than the wavelength (which is inverse to the frequency), and the voltage and current no longer remain spatially uniform over the network length so the transmission lines need to be treated as distributed parameter networks. A transmission line can be represented by an equivalent lumped circuit, as shown in Figure 2.1, where R, L, G, and C are frequency-dependent parameters defined per unit length [12, 13]. The resistance R is related with the finite conductivity of the conductors, the inductance L represents the self-inductance of the wire and the mutual inductance between the two conductors, the capacitance C is due to the proximity of the two conductors and the conductance G is the electric loss in the material between the conductors.

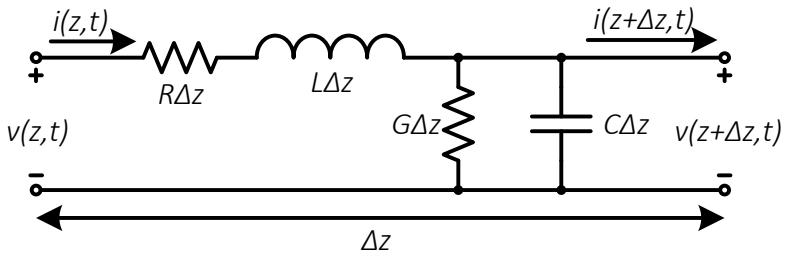


Figure 2.1: Transmission line equivalent circuit representation (adopted from [13])

Applying the Kirchhoff's Voltage Law (KVL) to the circuit of Figure 2.1, and using cosine-based phasor notation for simplicity (considering steady-state sinusoidal regime), is possible to conclude that

$$V\left(z\right) = \left(R + j\omega L\right) I\left(z\right) \Delta z + V\left(z + \Delta z\right) \tag{2.1}$$

and Kirchhoff's Current Law (KCL) leads to

$$I\left(z\right) = \left(G + j\omega C\right) V\left(z + \Delta z\right) \Delta z + I\left(z + \Delta z\right). \tag{2.2}$$

Dividing the equations (2.1) and (2.2) by Δz and taking the limit as $\Delta z \to 0$ results in the following differential equations:

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2.3}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{2.4}$$

Deriving the both terms of (2.3) and (2.4), the wave equations for $V(z)$ and $I(z)$ are given as follows:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{2.5}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0, \tag{2.6}$$

where

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.7}$$

is the complex propagation constant, which is frequency dependent. The solutions to these equations are two exponential functions for the voltage and for the current that are general solutions for transmission lines aligned along the z-axis, as shown in Figure 2.1, at a specific point z [13]:

$$V(z) = V_o^+ e^{-\gamma z} + V_o^- e^{\gamma z} \tag{2.8}$$

$$I(z) = I_o^+ e^{-\gamma z} + I_o^- e^{\gamma z}, \tag{2.9}$$

where V_o^+ and I_o^+ are, respectively, the voltage and current amplitudes of the incident waves and V_o^- and I_o^- are the voltage and current amplitudes of the reflected waves. The term $e^{-\gamma z}$ represents the wave propagation in the $+z$ direction and the $e^{\gamma z}$ in the $-z$ direction. Deriving (2.3) and applying to (2.8), the current on the line is given by

$$I(z) = \frac{\gamma}{R + j\omega L}\left(V_o^+ e^{-\gamma z} - V_o^- e^{\gamma z}\right). \tag{2.10}$$

Comparing the previous equation with (2.9) shows that the transmission line characteristic impedance Z_0 can be defined as

$$Z_0 = \frac{V_o^+}{I_o^+} = -\frac{V_o^-}{I_o^-} = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}. \tag{2.11}$$

Assuming an arbitrary load impedance Z_L located at $z = 0$, as shown in Figure 2.2, and that an incident waveform is generated from a source at $z < 0$, from (2.8) and (2.10) is possible to define Z_L as

$$Z_L = \frac{V(0)}{I(0)} = \frac{V_o^+ + V_o^-}{V_o^+ - V_o^-} Z_0. \tag{2.12}$$

Solving the previous equation in order to V_o^-/V_o^+ shows that the voltage reflection coefficient Γ, which is the amplitude of the reflected voltage wave normalized to the amplitude of the incident voltage wave, is given by

$$\Gamma = \frac{V_o^-}{V_o^+} = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{2.13}$$

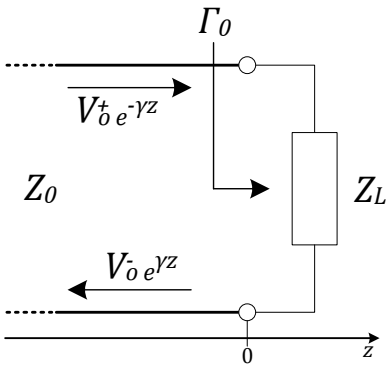


Figure 2.2: Transmission line terminated in an arbitrary load impedance Z_L

Since the time-average power that flows along a transmission line is given by [13]

$$P_{avg} = \frac{1}{2}\frac{|V_o^+|^2}{Z_0}\left(1 - |\Gamma|^2\right), \tag{2.14}$$

to achieve the maximum power transfer to the load there should not exist reflected wave in order to $\Gamma = 0$, so the load impedance must be matched to the characteristic impedance of the transmission line ($Z_L = Z_0$), as stated in 2.13. RF antennas usually have a characteristic impedance of 50 Ω so the first block of a receiver AFE (commonly a LNA) implemented in an Integrated Circuit (IC) must have its input impedance matched to 50 Ω. This match can be achieved using the transistors transcondutance, as it will be shown further later, or using reactive elements that are problematic due to area consumption and bandwidth limitation. The internal blocks do not need to be matched because the distance between the blocks is so tiny that the electromagnetic wavelength is bigger than the circuit dimensions.

2.1.2 Scattering Parameters

Due to the difficulties measuring voltage and current in a RF circuit, since these measurements usually involve the magnitude and phase of traveling or standing waves, the circuit measurements are made using the average power instead of the traditional open-circuit or short-circuit measurements [12]. The scattering parameters (S-parameters) are parameters that can be obtained through those power measurements in order to describe the network. Considering a two-port network, as shown in Figure 2.3, with the the input and output incident waves V_1^+ and V_2^+, and the corresponding reflected waves V_1^- and V_2^-, the input and output reflected waves voltage is given by [1]

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \tag{2.15}$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+, \tag{2.16}$$

where S_{mn} are the different S-parameters.

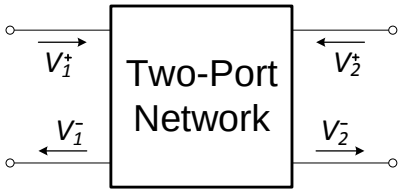


Figure 2.3: Incident and reflected waves in a two-port network

- S_{11} is the input reflection coefficient and represents the accuracy of the input matching. This parameter is the ratio of the reflected and incident waves at the input port when there is no incident wave at the output port:

$$S_{11} = \frac{V_1^-}{V_1^+}_{|V_2^+=0}$$

If the input of the network is completely adapted there is no reflect wave at the input (V_1^-) and consequently $S_{11} = 0$. Usually a $S_{11} < -10$ dB means that the input of the circuit is correctly matched.

- S_{12} is known as reverse voltage gain and characterizes the "reverse isolation" of the circuit. This parameter is the ratio of the reflected wave at the input port to the incident wave into the output port when the input port is matched:

$$S_{12} = \frac{V_1^-}{V_2^+}_{|V_1^+=0}$$

- S_{21} is the forward voltage gain of the network and represents the voltage gain of the circuit, as expected. This parameter is the ratio between the reflected wave at the output port and the incident wave at the input port, when the incident wave at the output is zero:

$$S_{21} = \frac{V_2^-}{V_1^+}_{|V_2^+=0}$$

- S_{22} is the output reflection coefficient and represents the accuracy of the output matching. This parameter is the ratio of the reflected and incident waves at the output port when there is no incident wave at the input port:

$$S_{22} = \frac{V_2^-}{V_2^+}_{|V_1^+=0}$$

Those values depend of the working frequency of the circuit and are usually represented in units of dB.

2.1.3 Gain

Nowadays the signals at the input of receivers are very weak, commonly in the microvolt (μV) range, so they need to be amplified in order to allow their processing by the receiver circuit. This factor makes the gain a very important measure of the performance of an amplifier or a mixer because it expresses the capability of the circuit to increase the amplitude of an input signal, ideally introducing no distortion [14]. Usually there are three different types of gain considered in electronics: voltage gain, current gain and power gain. For example, the voltage gain is defined as

$$A_v = \frac{v_{out}}{v_{in}}. \tag{2.17}$$

If $A_v > 1$ the input signal is amplified and if $A_v < 1$ the input signal is attenuated. For simplicity, the gain is often expressed in dB. It is important to note that voltage and current gains are expressed as $A_{v,i}|_{dB} = 20\log|A_{v,i}|$ and power gain is expressed as $A_p|_{dB} = 10\log|A_p|$.

2.1.4 Noise

Noise is a random process, i.e. its instant value cannot be predicted at any time, that is present in all electronic circuits due to external interference or physical phenomena related with the nature of materials. Since the noise presence is inevitable and it degrades the circuit behavior,it is important to analyze its impact, through statistical models, and create methods that allow the minimization of its effect in the circuit [2]. In this section the two main noise sources present in CMOS transistors, thermal and flicker noise, are described. Finally NF will be presented, which is the most common measure of the noise generated by a circuit.

2.1.4.1 Thermal Noise

The thermal noise in circuits is due to thermal excitation of charge carriers in a conductor. It occurs in all resistors (including semiconductors) working above absolute zero temperature and introduces fluctuations in the voltage measured across the device. This kind of noise has a white (flat) spectrum that is proportional to absolute temperature [15]. In a resistor the thermal noise can be modeled as a voltage source with a Power Spectral Density (PSD) of $\overline{V_n^2}$ in series with a noiseless resistor (Thevenin equivalent), or as a current source with a PSD of $\overline{I_n^2}$ in parallel with the same resistor (Norton equivalent) [1], as shown in Figure 2.4. The average thermal noise power generated in a resistor is given by

$$\overline{V_n^2} = 4kTR\Delta f, \tag{2.18}$$

where k is the Boltzmann constant, T is the material temperature in Kelvin and Δf is the system bandwidth. Usually it is assumed $\Delta f = 1$, for notation simplicity, which means that the noise power is expressed per unit bandwidth.

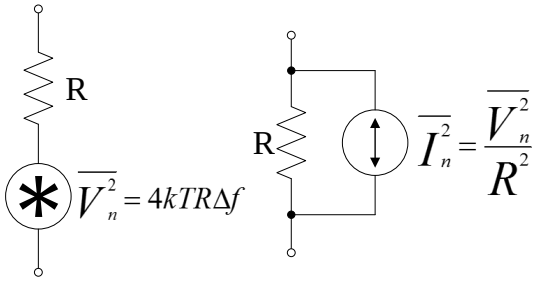


Figure 2.4: Thevenin and Norton models of resistor thermal noise

The MOS transistors also exhibit thermal noise that is almost completely generated in the channel due to carrier motion, and for long-channel devices operating in saturation it can be modeled by a current source connected between the drain and source terminals [2], as shown in Figure 2.5. In this case, the average thermal noise current generated by a

MOS transistor is given by

$$\overline{I_n^2} = 4kT\gamma g_m, \tag{2.19}$$

where γ is the *excess noise factor* and has the value of 2/3 for long-channel transistors and higher values for short-channel devices [16], and g_m is the transconductance.

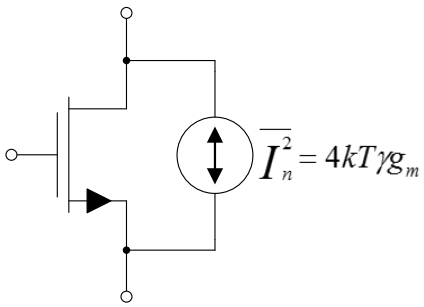


Figure 2.5: Thermal channel noise of a MOS transistor model

For the particular case of a MOS transistor operating in deep triode region, where $V_{DS} \approx 0$, it acts like a voltage-controlled resistor with V_{GS} used as control terminal, and with an on resistance given by $R_{on} \approx r_{ds} = 1/g_{ds}$. Then, as with the resistors, the generated thermal noise current is given by

$$\overline{I_n^2} = 4kTg_{d0}, \tag{2.20}$$

where g_{d0} is the transistor output conductance (g_{ds}) for $V_{DS} = 0$. It is important to note that in this operating region $\gamma = 1$, so it is omitted in (2.20).

Another source of thermal noise in MOS transistors is related with the gate resistance. Despite being more negligible than the noise due to channel carrier motion, this effect is becoming more important for the new technologies, as the gate length is scaled down [1].

2.1.4.2 Flicker Noise

Flicker noise is present in all active devices, although only occurs when a DC current is flowing, and has origin in a phenomenon at the interface between the gate oxide (SiO_2) and the silicon substrate (Si). As charge carriers move at the SiO_2 – Si interface, some are randomly trapped and released introducing "flicker" noise in the drain current [2]. Beyond this phenomenon, other mechanisms are believed to generate flicker noise [17]. Unlike thermal noise in MOS transistors, this noise is more easily modeled as a voltage source in series with the gate and exhibits the following PSD:

$$\overline{V_{nf}^2} \approx \frac{K_f}{C_{ox}WLf}, \tag{2.21}$$

where K_f is a process dependent constant that is bias independent, C_{ox} is the gate oxide

capacitance, W is the transistor channel width and L is the transistor channel length. It is important to note that K_f is lower for p-channel devices, so PMOS exhibit less flicker noise than NMOS. Also, the flicker noise is inverse to transistor dimensions and to decrease the noise the device area must be increased. Since this noise is well modeled as having a $1/f$ spectral density, as shown in Figure 2.6, it is also known as 1/f noise.

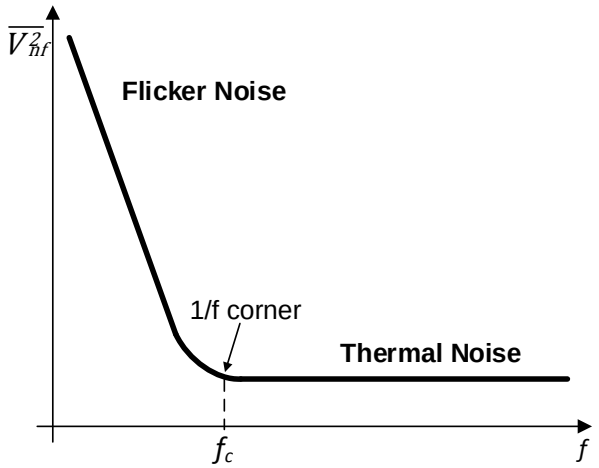


Figure 2.6: Power spectrum of flicker and thermal noise

The 1/f noise corner frequency, f_c in Figure 2.6, can be obtained by converting the flicker noise voltage (2.21) to current and equating the result to the thermal noise current expressed in (2.19) [1], resulting in

$$f_c = \frac{K_f}{WLc_{ox}} \frac{g_m}{4KT\gamma}. \tag{2.22}$$

For today's MOS technologies the corner frequency is relatively constant and falls in the range of tens or hundreds of megahertz [1].

2.1.4.3 Noise Figure

The Noise Factor (F) or Noise Figure (NF) (when expressed in dB) is the most common measure of the noise generated by a circuit and is defined as the ratio of the total available noise power at the output of the circuit to the available noise power at output, due to noise from the input termination, as shown in (2.23).

$$F = \frac{N_o}{N_i G_A}, \tag{2.23}$$

where N_i and N_o are, respectively, the available power noise at the input and output of the circuit, and G_A is the available power gain of the circuit. By definition, N_i is the noise power resulting from a matched resistor at T_o = 290 K [13].

Assuming that the circuit is a two-port network, as shown in Figure 2.7, with both input and output ports adapted, if a power signal S_i is applied at the input then the

signal is totally transferred to the network output (according to maximum power transfer theorem), and therefore the power gain of the circuit is expressed by

$$G_A = \frac{S_o}{S_i}. \tag{2.24}$$

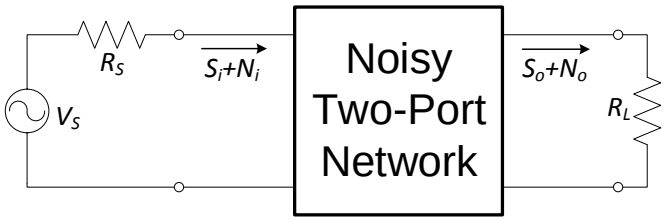


Figure 2.7: Noisy two-port network

Replacing (2.24) in (2.23) is possible to conclude that

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{SNR_i}{SNR_o} \tag{2.25}$$

or, in decibels,

$$NF = 10 \log \frac{SNR_i}{SNR_o}. \tag{2.26}$$

The previous equation shows that NF is a measure of the degradation in the Signal-to-noise Ratio (SNR) between the input and output of the circuit, so if no noise is introduced by the network, $F = 1$ or $NF = 0$ dB.

For a circuit with *m* cascaded stages the total NF is given by

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{G_{A1}} + \ldots + \frac{NF_m - 1}{G_{A1} \ldots G_{A(m-1)}}, \tag{2.27}$$

where NF_x and G_{Ax} are the NF and the available power gain of the stage *x*, respectively. This equation[1] shows that the first stages in a cascade circuit are the most critical, since the noise contribution of the stages decreases as the total power gain preceding that stage increases [1].

2.1.5 Nonlinearities Effects

Although analog circuits can be approximated by a linear model for small-signal operation, modeled as a Taylor series in terms of the input signal voltage, as expressed in (2.28), there are no ideal linear components due to some non-linear characteristics related with noise, gain compression, etc., presented in real devices like transistors. These non-linearities may lead to signal distortion, losses, interference with other radio channels, among others [13]. Linearity is one important measurement of performance of a system

[1] Known as Friis' equation [18].

and describes the impact of the non-linearities over an output signal.

$$v_o = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \dots \tag{2.28}$$

If a sine-wave, $v_i(t) = V_o \cos(\omega t)$, is applied to the input of a device, the system response can be well described as the following third-order polynomial:

$$v_o = a_0 + a_1 V_o \cos(\omega t) + a_2 V_o^2 \cos^2(\omega t) + a_3 V_o^3 \cos^3(\omega t) \tag{2.29}$$

or

$$\begin{aligned} v_o = & \overbrace{\left(a_0 + \frac{1}{2} a_2 V_o^2\right)}^{\text{DC}} + \overbrace{\left(a_1 V_o + \frac{3}{4} a_3 V_o^3\right) \cos(\omega t)}^{\text{Fundamental Harmonic}} + \overbrace{\frac{1}{2} a_2 V_o^2 \cos(2\omega t)}^{2^{nd}\text{ Harmonic}} \\ & + \underbrace{\frac{1}{4} a_3 V_o^3 \cos(3\omega t)}_{3^{rd}\text{ Harmonic}} . \end{aligned} \tag{2.30}$$

From previous equation is possible to conclude that a nonlinear system produces as much harmonics as the order of its nonlinearities. The even order coefficients compromise the DC component and the odd order coefficients affect the fundamental harmonic (ω) amplitude.

In this section, the 1 dB Compression Point ($\mathrm{P_{1dB}}$) and the second and third-order intermodulation products will be presented since these parameters are very important to analyze the system performance related with linearity, and they usually appear in the system specifications.

2.1.5.1 Gain Compression

The 1 dB Compression Point ($\mathrm{P_{1dB}}$) quantifies the operating range of a circuit and is defined as the input signal level that causes the gain to decrease 1 dB compared with the ideal linear characteristic, as shown in Figure 2.8. Since the voltage gain of the signal at the fundamental harmonic frequency ω_0 is, as stated in (2.30), given by

$$A_v = \left(\frac{v_o}{v_i}\right)_{\omega_0} = a_1 + \frac{3}{4} a_3 V_o^2 \tag{2.31}$$

and typically a_3 as the opposite sign of a_1 [13], the gain of the circuit tends to be lower than the expected for large values of V_o, which causes this gain compression and consequently degrades de output signal. For an ideal linear circuit the gain would be equal to a_1.

Is important to note that the $\mathrm{P_{1dB}}$ can be referred to the input (IP_{1dB}) or to the output (OP_{1dB}). Typically it is given as the larger option, so for an amplifier is usually specified as OP_{1dB} and for a mixer as IP_{1dB}.

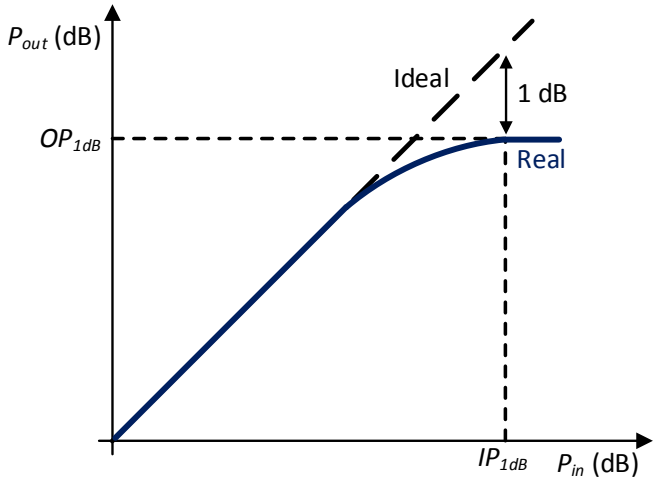


Figure 2.8: Definition of P_{1dB}

2.1.5.2 Intermodulation Distortion

The previous nonlinearity considers only one signal at the input of the system. which creates undesired frequency components at multiples of ω_0 that usually lie outside the passband of the circuit and do not interfere with the desired signal. If two signals are applied to the circuit, there are other nonlinear effects that do not manifest themselves in the previous situation, and can corrupt the desired signal since they produce harmonics that are not multiples of the fundamental harmonic frequency. This phenomenon is called Intermodulation (IM). For instance, assume that a signal $v_i(t) = V_{o1}\cos(\omega_1 t) + V_{o2}\cos(\omega_2 t)$ is applied to a system modeled by (2.28). Considering only the second and third terms of the Taylor series, the IM products at the output are given by

$$\begin{aligned} IM2 = a_2 &\left[\frac{1}{2}V_o^2(1+\cos(2\omega_1 t)) + \frac{1}{2}V_o^2(1+\cos(2\omega_2 t))\right] \\ &+ a_2\left[V_o^2\cos(\omega_1 t - \omega_2 t) + V_o^2\cos(\omega_1 t + \omega_2 t)\right] \end{aligned} \tag{2.32}$$

$$\begin{aligned} IM3 = a_3 V_o^3 &\left[\frac{1}{4}\cos(3\omega_1 t) + \frac{1}{4}\cos(3\omega_2 t) + \frac{3}{4}\cos(\omega_1 t) + \frac{3}{4}\cos(\omega_2 t)\right] \\ &+ a_3 V_o^3\left[\frac{3}{2}\cos(\omega_2 t) + \frac{3}{4}\cos(2\omega_1 t - \omega_2 t) + \frac{3}{4}\cos(2\omega_1 t + \omega_2 t)\right] \\ &+ a_3 V_o^3\left[\frac{3}{2}\cos(\omega_1 t) + \frac{3}{4}\cos(2\omega_2 t - \omega_1 t) + \frac{3}{4}\cos(2\omega_2 t + \omega_1 t)\right]. \end{aligned} \tag{2.33}$$

These interacting signals will produce intermodulation products that originate harmonics at the sum and difference of both input signals frequencies and their multiples, as shown in Figure 2.9.

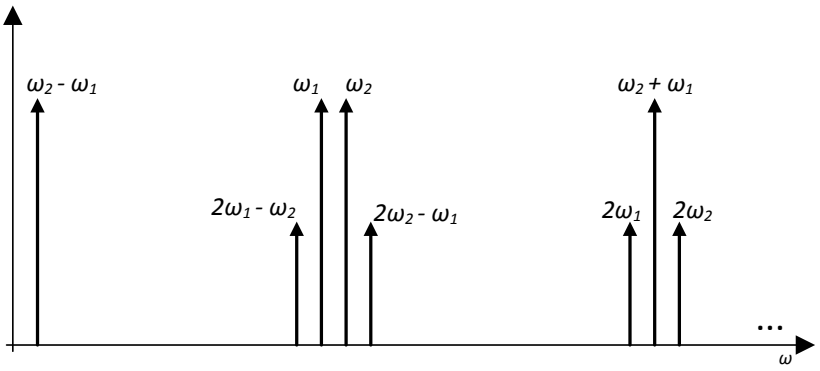


Figure 2.9: Output spectrum of IM2 and IM3

If the both input signals frequencies, ω_1 and ω_2, are close, the second order intermodulation products can be easily filtered from the output since they are far from the input frequencies. However, the third order intermodulation products are very near of the input signals, as shown in Figure 2.9, and corrupt the desired signals because it is very difficult to filter them with a bandpass filter. From this analysis is possible to conclude that the IM3 is more problematic than IM2 and requires special attention.

To understand in which point the curves of power output of fundamental frequency and of the third-order intermodulation product would intercept if they were linear, i.e. they do not suffer compression at high input power, the Third-order Intercept Point (IP_3) was defined. As shown in Figure 2.10, the IP_3 can be input-referred (IIP_3) or output-referred (OIP_3) and the chosen result is typically the largest value as in the $\mathrm{P}_{1\mathrm{dB}}$.

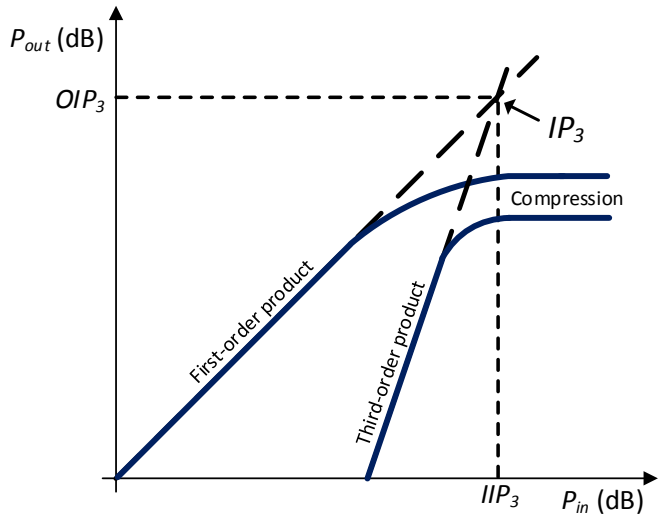


Figure 2.10: Definition of $IP3$

From Figure 2.10 is possible to note that the output power of the first-order product is proportional to the input power and, since the voltage associated with the third-order products increases as V_o^3, as shown in (2.33), the output power of the third-order product

has a slope of 3, so they always intercept each other assuming that both are ideal (do not suffer compression). A practical rule that is usually employed is that the IP_3 is 10–15 dB greater than P_{1dB} [13].

For the second-order intermodulation product exists a similar analysis that is known as Second-order Intercept Point (IP_2).

2.2 Receiver Architectures

In a wireless system the receiver AFE is one of the most critical components since, due to the communication medium (air), the received signals are usually very weak and noisy. A wireless receiver needs to have the capability to filter the incoming signal in order to eliminate undesired interferes that can corrupt it, and detect the information present in the signal of interest. Since the signals are propagated at high frequencies, because it is possible to store more information using higher bandwidth and the antennas size is smaller, the receiver needs to convert those signals to lower frequencies. In summary, a receiver needs to filter and amplify the received signal, introducing almost no noise, and then down-convert that signal so that it can be demodulated and processed by a digital system. The main blocks of a wireless receiver are the LNA, the LO and the mixer. Receivers can be divided into three main groups: heterodyne, homodyne and low-IF, that will be presented in this section.

2.2.1 Heterodyne Receiver

The super-heterodyne receiver, also known as IF receiver, is one of the most used receiver topologies in wireless communication systems, and was proposed by Armstrong in 1917 [3]. As shown in Figure 2.11, the down-conversion is done in two steps. First, the input signal is converted to a fixed IF, after being amplified by a LNA and filtered (by an image rejection BPF), and then that signal is filtered by a channel select BPF and down-converted to baseband.Finally, it is filtered again by a LPF. The down-conversions are made by a multiplication (mixing) of the RF with the signal produced by the LO. At the end the signal is converted to the digital domain by an ADC [1].

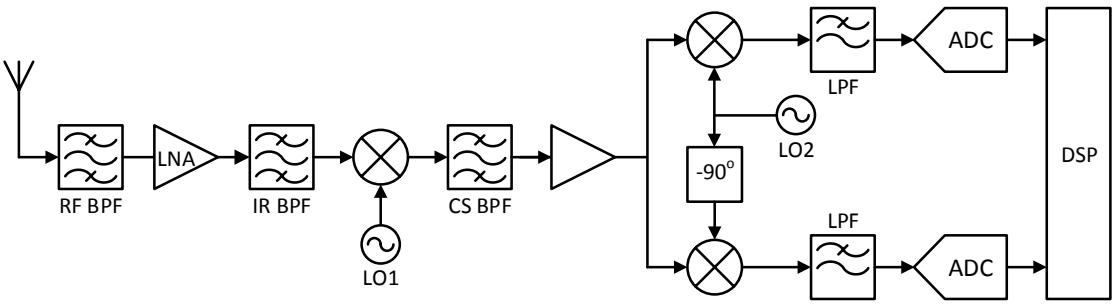


Figure 2.11: Super-Heterdoyne receiver architecture (adopted from [3])

The main purpose of the image rejection filter (IR BPF) is to eliminate the image that can be produced in the down-conversion, since two input frequencies can produce the same IF, as shown in Figure 2.12. The channel select filter (CS BPF) filters the interferers that are down-converted together with the signal and can corrupt it at the next down-conversion. The choice of the IF needs to take into account that with high IF the image rejection filter is easier to design and with low IF the suppression of interferers is easier [3]. Due to the required high Q of the filters, they need to be implemented with discrete components which is not a good solution for modern applications where a low-area and low-cost design is required. The main advantage of this kind of receiver is that is possible to handle modern modulation schemes that require IQ (in-phase and quadrature) signals to fully recover the information.

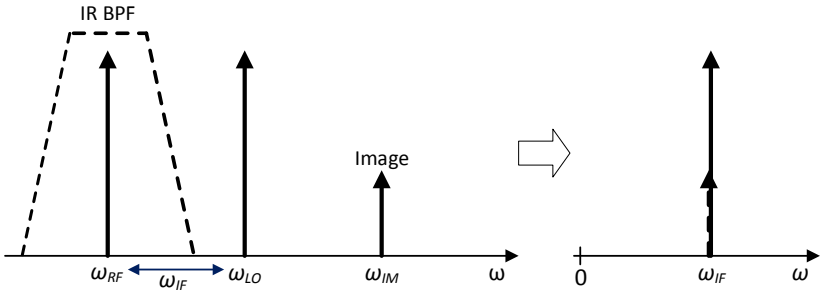


Figure 2.12: Image rejection in super-heterdoyne receiver (adopted from [3])

Assuming that the receiver input signal is a sinusoid given by $v_{RF}(t) = V_{RF}\cos(\omega_{RF}t)$ and the LO is another sinusoid given by $v_{LO}(t) = V_{LO}\cos(\omega_{LO}t)$, the signal at the output of the first mixer is given by

$$v_{IF}(t) = v_{RF}(t) \cdot v_{IF}(t) = \frac{1}{2}V_{RF}V_{LO}\left[\cos(\omega_{RF}t - \omega_{LO}t) + \cos(\omega_{RF}t + \omega_{LO}t)\right] \tag{2.34}$$

with $\omega_{IF} = \omega_{RF} - \omega_{LO}$.
Although the RF BPF eliminates the unwanted signals that may be present in the spectrum and are far from ω_{IF}, a major problem can occur if exists a signal with frequency $\omega_{IM} = 2\omega_{LO} - \omega_{RF}$ at the RF input of the mixer, called image signal. After the mixing, this signal originates two signals at frequencies $\omega_1 = \omega_{LO} - \omega_{RF}$ and $\omega_2 = 3\omega_{LO} - \omega_{RF}$, as stated in (2.34). If no IR BPF is used, the frequency ω_1 overlaps and degrades the signal of interest, since $|\omega_1| = |\omega_{IF}|$. As shown in Figure 2.12, this filter needs to have an high Q, mostly if ω_{IF} is low.

2.2.2 Homodyne Receiver

The homodyne receiver, also known as direct-conversion receiver or zero-IF receiver, translates the input signal to the baseband in a single down-conversion, using a LO with the same frequency as the RF signal. This avoids the use of an external image rejection

filter, and only a LPF is required after the mixer to do the proper channel selection, as shown in Figure 2.13.

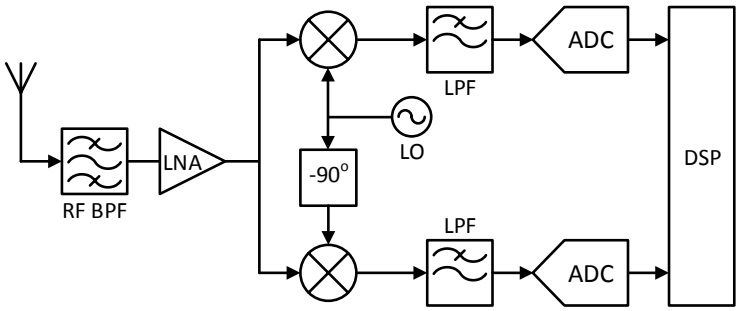


Figure 2.13: Homodyne receiver architecture (adopted from [3])

The BPF before the LNA is often used to suppress the interferers outside the receiver band, so the Q requirements are not very demanding. The main advantages of this kind of receiver are the low-power, low-area and low-cost realization [3]. Despite these advantages, homodyne receivers have several disadvantages, comparing with heterodyne receivers, that prevent this architecture from being applied in more demanding applications [1, 3]:

LO leakage As shown in Figure 2.14, due to device capacitances between the LO and RF ports of the mixer and capacitances or resistances between the LNA ports, the receiver will couple signal to the antenna that will be emitted and can interfere with other receivers using the same wireless standard. This effect can be minimized with the use of differential LO and mixer outputs to cancel common mode components.

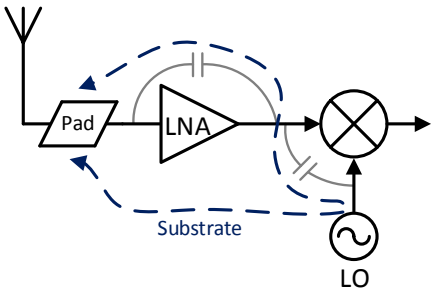


Figure 2.14: Homodyne receiver LO leakage (adopted from [1])

DC offsets Due to the LO leakage, studied above, that appears at the LNA and mixer inputs, a DC component is generated at the output of the mixer (this process is known as LO "self-mixing") that can saturate the baseband circuits, preventing signal detection. This topology of receiver needs DC offset removal in order to avoid this kind of problems.

Channel selection The LPF must suppress the out-of-channel interferers in order to be possible to convert the desired baseband signal to the digital domain. This filter should have high linearity and low-noise which makes it difficult to implement.

Flicker noise This type of noise can corrupt the baseband signals, as explained in section 2.1.4.2, since its frequency is close to DC in these type of receivers.

Even-order distortion If two interferers exist near the channel of interest, after the mixing one of the interferers components is shifted near to the baseband and appears at the output together with the down-converted signal, as shown in Figure 2.15, which leads to signal distortion. Thus, these kind of receivers must have a very high IP_2. One solution to avoid this problem is use differential LNAs and mixers, in order to eliminate even-order harmonics.

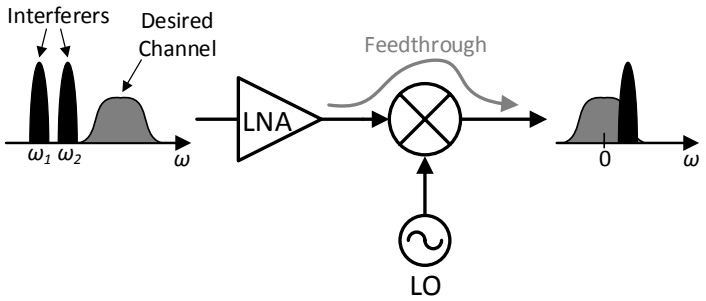


Figure 2.15: Effect of even-order distortion (adopted from [1])

I/Q mismatch Errors in the 90º phase shift circuit and mismatches between the I and Q mixers result in imbalances in the gain and phase of the baseband I and Q outputs, that can corrupt the down-converted signal constellation (e.g. in Quadrature Amplitude Modulation (QAM)). Since modern wireless applications have different information in I and Q signals, this aspect is very critical in direct-conversion receivers because it is very difficult to implement high frequency blocks with very accurate quadrature relationship.

This kind of receiver requires very linear blocks and very precise quadrature oscillators, in order to avoid the problems described above, that are very difficult to achieve for high frequencies.

2.2.3 Low-IF Receiver

Although the heterodyne receiver has high performance and flexibility, it requires the use of external components, which does not allow the receiver full integration. On the other hand, the homodyne receiver can be totally integrated but has some problems related with flicker noise, intermodulation, etc. The low-IF receiver combines the advantages of both types of receivers, and uses a mixed approach, which consists in select a low intermediate frequency, avoiding the direct conversion problems previously indicated. To overcome the image problem related with the non-direct conversion, without the need of an image rejection filter, it is used a technique to cancel the image signal that consists in a quadrature architecture that suppresses the image by generating a negative replica. There are two main image rejection architectures, the Hartley and the Weaver [1, 3], as shown in Figure 2.16.

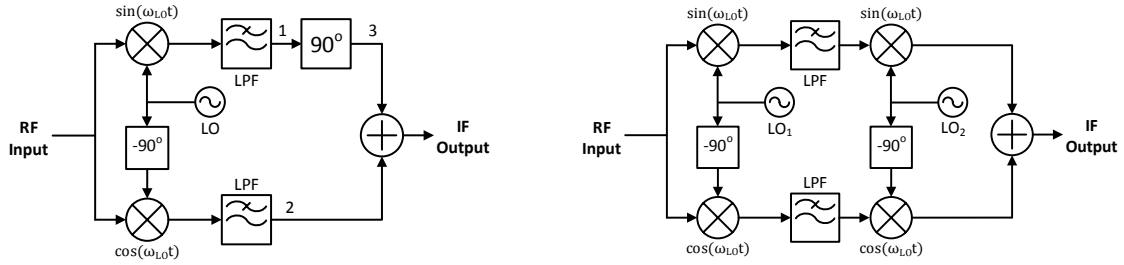


Figure 2.16: Image rejection architectures: (a) Hartley (b) Weaver (adopted from [3])

The Hartley architecture [19] mixes the RF signal with the quadrature outputs of the LO and, after the LPF, one of the resulting signals is shifted 90º and subtracted to the other signal, as shown in Figure 2.16a. For instance, consider that the signal $x(t) = V_{RF}\cos(\omega_{RF}t) + V_{Im}\cos(\omega_{Im}t)$ is placed at the input of the receiver, where V_{RF} and V_{Im} are, respectively, the amplitude of RF and image signals. After down-conversion and filtering,

$$x_1(t) = -\frac{V_{RF}}{2}\sin[(\omega_{RF} - \omega_{LO})t] + \frac{V_{Im}}{2}\sin[(\omega_{LO} - \omega_{Im})t] \tag{2.35}$$

$$x_2(t) = \frac{V_{RF}}{2}\cos[(\omega_{LO} - \omega_{RF})t] + \frac{V_{Im}}{2}\cos[(\omega_{LO} - \omega_{Im})t]. \tag{2.36}$$

Since a shift of 90º is equivalent to a change from $\sin$ to $(-\cos)$,

$$x_3(t) = \frac{V_{RF}}{2}\cos[(\omega_{RF} - \omega_{LO})t] - \frac{V_{Im}}{2}\cos[(\omega_{LO} - \omega_{Im})t]. \tag{2.37}$$

Due to 90º the phase shift, this receiver produces the same polarities for the desired signal and opposite polarities for image, in the two paths. Summing both signals, $x_2(t)$ and $x_3(t)$, results in

$$x_{IF}(t) = V_{RF}\cos[(\omega_{RF} - \omega_{LO})t] \tag{2.38}$$

Thus, the image component is canceled and the desired signal is doubled in amplitude. The main problem of this architecture is the receiver sensitivity to the local oscillator quadrature errors and the incomplete image cancellation due to the mismatches in the two signal paths.

The Weaver architecture, as shown in Figure 2.16b, is similar to the Hartley architecture, but the 90º phase shift is performed by a second mixing operation in both signal paths. This kind of approach has the same problems of the Hartley architecture and it suffers from an image problem in the second down-conversion, if the signal is not converted to the baseband.

2.3 Low-noise Amplifiers

This section discusses some LNA topologies and typical requirements for this kind of amplifiers. The LNA is typically the first stage of a RF receiver so its input impedance should match the antenna characteristic impedance in order to maximize the power transfer, as discussed in section 2.1.1. The LNA should introduce a minimum noise in the system while providing enough gain for the required SNR. As expressed in (2.27), in a cascade circuit the NF of the first stage (LNA) is dominant and should be very low, and the gain should be very large to reduce the noise contribution of the next stages. Regarding the circuit linearity, in a cascaded circuit it is limited by the stage with the worst IP_3, and the gain of the preceding stages affects negatively the IP_3 of the subsequent stages, as expressed in (2.39), so there is a trade-off between noise and linearity, since a low NF demands a high gain as explained before [1].

$$\frac{1}{IP_{3,tot}} = \frac{1}{IP_{3,LNA}} + \frac{G_{A,LNA}}{IP_{3,mixer}} + \dots \tag{2.39}$$

Regarding the LNA linearity, in most applications it does not limit the linearity of the receiver since it is not affected by the gain of any stage, so usually the LNAs are designed and optimized with little concern about this aspect.

Concerning the bandwidth, LNAs can be narrowband or wideband. In this section some LNA topologies will be presented and their behavior with respect to input matching, gain, and noise figure will be analyzed.

2.3.1 Narrowband LNAs

This kind of LNA works for a fixed input frequency so the input matching is easier to achieve than in wideband LNAs, because the LNA only needs to be matched to the antenna for that frequency, and the matching can be performed with reactive components.

2.3.1.1 Common-Source LNA with Inductive Degeneration

The Common-Source (CS) LNA with inductive degeneration [20], represented in Figure 2.17, is one of the most used topologies of narrowband LNAs because it allows easy input matching, high gain and low noise figure.

The input impedance of this LNA is given by

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s. \tag{2.40}$$

By choosing $L_s + L_g$ to resonate with C_{gs} is possible to eliminate the imaginary terms of the input impedance, so the impedance will look real near the desired operating frequency. Adjusting the inductance L_s is possible to match the antenna impedance for that frequency. Since the inductors are ideally noiseless, they contribute with almost no noise to the LNA so it has a low noise figure. The main disadvantage of this circuit is the large

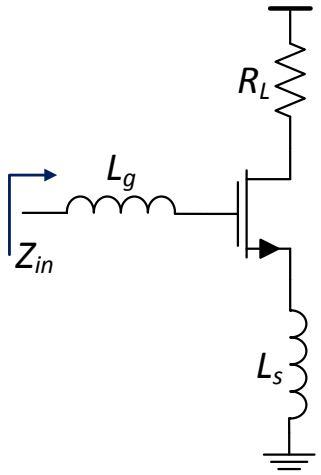


Figure 2.17: CS LNA with inductive degeneration

die area and the special RF options needed to design inductors with an high Q factor, which increase the production cost.

2.3.2 Wideband LNAs

This kind of LNA operates in a large spectrum so it needs to have an high bandwidth and the input impedance should match the antenna impedance for the all LNA working band, so it can not be achieved using reactive components.

2.3.2.1 Common-Source with Resistive Input Matching

The resistive input matching is the easiest way to obtain a stable input impedance over the LNA working band because, as shown in Figure 2.18, the input resistor is in parallel with the transistor gate, which has infinite input impedance.

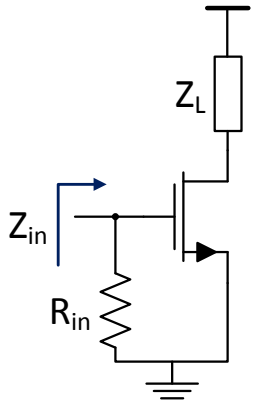


Figure 2.18: CS LNA with resistive input matching

The main drawback of this configuration is that the resistor introduces a significant amount of noise to the amplifier. Assuming that the LNA has an available power gain G_A and

a noise power at output P_n, and the source has an impedance R_S (from antenna) that is matched to R_{in}, from (2.18) and (2.23) is possible to obtain the resulting noise factor:

$$F = \frac{4kTR_sG_A + 4kTR_{in}G_A + P_n}{4kTR_sG_A} = 2 + \frac{P_n}{4kTR_{in}G_A} \tag{2.41}$$

that is at least 2, resulting in a noise figure greater than 3 dB.

2.3.2.2 Common-Gate

The Common-Gate (CG) [1, 21] is one of the most used topologies to implement wideband LNAs because it has an intrinsic wideband response. As shown in Figure 2.19, its input impedance is approximately $1/g_m$, neglecting channel-length modulation and body effect. Thus, the dimensions of the transistor and the bias current are chosen in order to obtain $g_m = 1/R_S = 20$ mS for a 50 Ω antenna.

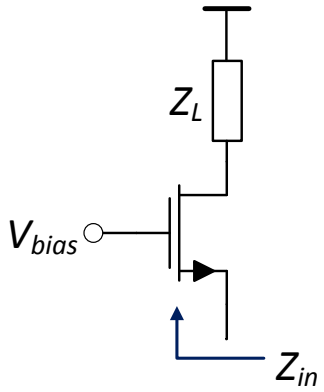


Figure 2.19: CG LNA

Considering only the transistor thermal noise, and assuming that it is a long channel device, the minimum noise factor of this topology can be easily calculated through (2.23), where $N_i = \overline{I_s^2}$ and $N_o = (\overline{I_s^2} + \overline{I_d^2})G_A$.

$$F = \frac{(\overline{I_s^2} + \overline{I_d^2})G_A}{\overline{I_s^2}G_A} = 1 + \frac{\overline{I_d^2}}{\overline{I_s^2}} \tag{2.42}$$

The average thermal noise at the input of the LNA due to the input impedance (transistor source) is $\overline{I_s^2} = 4kT/R_S = 4kTg_m$, and the average thermal noise generated at the gate of a MOS device working at the active region, $\overline{I_d^2}$, is given by (2.19), so

$$F = 1 + \frac{4kT\gamma g_m}{4kTg_m} = 1 + \gamma. \tag{2.43}$$

As shown before, for a long channel device operating in the active region $\gamma = 2/3$, so the minimum noise factor of a CG amplifier is about $5/3$, which corresponds to a noise figure of 2.2 dB that is lower than the previous topology. The main disadvantage of this LNA is the fact that the gain is given by $G_A = g_mZ_L$. Since g_m is fixed due to the

impedance matching, to increase the gain is necessary to increase Z_L, and consequently the noise figure increases, limiting the achievable gain. Usually this kind of LNA has a noise figure above 3 dB. However, there are some noise cancellation techniques, such as will be analyzed in the next chapter, that can be used to reduce the LNA noise figure.

2.3.3 Discussion

In this section it was shown that there are two major LNA architectures, narrowband and wideband. Table 2.1 presents the main characteristics of both.

Table 2.1: Comparison between Narrowband and Wideband LNAs

Narrowband	**Wideband**
Low NF	High NF
High gain	Low power
Large area due to the inductors	Low area
High chip cost (special RF options)	Low cost (Standard CMOS)

The LNA architectures presented in this section are single-ended, so they only have one output. In order to transform the input signal into a differential signal at the output, a balun structure can be used instead, as will be studied in the next chapter. The main drawback of this structures is the extra loss and additional noise that are introduced, since more components are required.

2.4 Mixers

The mixer is key block of a RF front-end since it is responsible for the frequency translation of a RF signal to an IF or to baseband, in a process called down-conversion. Ideally, the output signal is a multiplication of the RF input signal by another RF signal provided by a LO, as shown in Figure 2.20. The resulting signal consists in two frequency components, equal to both the difference and sum of the input frequencies [3].

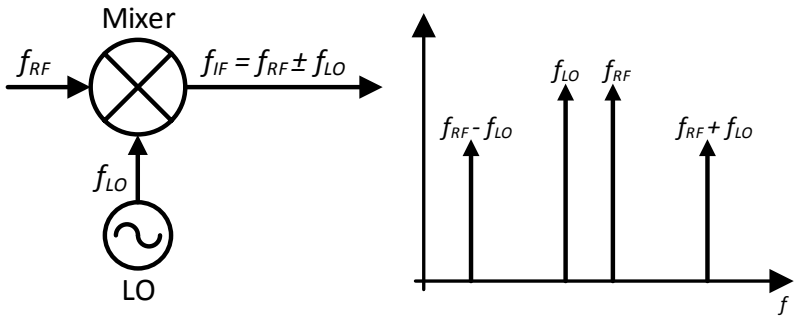


Figure 2.20: Down-conversion mixer

Considering that the RF input signal has the form $v_{RF}(t) = \cos(2\pi f_{RF} t)$ and the LO

has the form $v_{LO}(t) = \cos(2\pi f_{LO}t)$, the output of the mixer is [13]

$$v_{IF}(t) = \frac{K}{2}\left[\cos(2\pi(f_{RF} - f_{LO})t) + \cos(2\pi(f_{RF} + f_{LO})t)\right], \tag{2.44}$$

where *K* is related to the voltage conversion loss of the mixer. For a down-conversion mixer the desired frequency component is $f_{IF} = f_{RF} - f_{LO}$, called *lower sideband* (LSB), that can be easily selected by a LPF.

In this section the most important characteristics of mixers are reviewed: noise figure, intermodulation points, gain, etc., and different types of mixers (active and passive) are revisited [1, 3, 13].

2.4.1 Performance Parameters

Noise Since the mixer performs frequency translations, the noise at both sideband frequencies are also converted with the same efficiency, which means that the effects of both LNA and LO noise will appear at the mixer output. That's why it is important to design those components to have a low NF, as explained before. Also, the input noise of the mixer is divided by the LNA gain so the NF of the mixer is very dependent of the LNA characteristics. Another important aspect is the flicker noise. If the output frequency (IF) is below the 1/f noise corner frequency (Figure 2.6), its effect will be very pronounced at the mixer output, so the IF selection must be done carefully.

Conversion gain The voltage conversion gain of a mixer is given by the ratio between the *rms* voltage of the IF signal and the *rms* voltage of the RF signal.

$$\text{Voltage Gain (dB)} = 20\log\left(\frac{V_{IF}}{V_{RF}}\right). \tag{2.45}$$

The conversion gain allows to distinguish between two different mixer types: passive mixers, that have conversion loss (gain lower than one), and active mixers, that have conversion gain.

Linearity Mixers perform a nonlinear operation, so the transistors behavior are nonlinear and the LO port of the mixer should also be very nonlinear due to gain and noise constraints. Due to these characteristics, there are undesirable spurious terms at the output of the mixer that can affect the desired signal. In order to measure a mixer linearity is used the IM (section 2.1.5.2). In an heterodyne receiver the third-order IM is the most important because if the two input frequencies are close, the third-order IM components will be close to that frequencies, making them very difficult to remove. In an homodyne receiver the second-order IM is more important since the IM due to the two input signals can be close to DC and corrupt the output signal band. Larger order IM products are usually ignored because they are far from the band of interest and have lower amplitudes.

It is important to note that the IP_3 of a mixer is scaled down by the LNA gain, as stated in (2.39), so there is a trade-off between the mixer NF and its linearity.

2.4.2 Passive Mixers

This type of mixer do not operate as amplifying device and consequently its conversion gain is lower than one. The easiest way to implement a mixer is by using a switch based in a MOS transistor, as shown in Figure 2.21. Although this mixer consists in an active device, it acts like a switch (operating at triode region) and consequently has no DC consumption, high bandwidth, high linearity and very low flicker noise, which make it very attractive for use in microwave circuits.

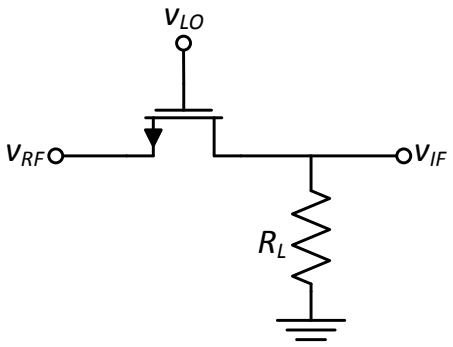


Figure 2.21: Mixer using a MOS switch

The RF signal is placed at the source of the transistor and the LO signal, usually a rail-to-rail square wave[2], is fed trough the transistor gate. When the LO signal is at high level the signal at the input is transferred to the output, since the switch is on, resulting in a frequency translation of the input signal to a frequency given by the difference of the RF and LO signals. This circuit is commonly called a *return-to-zero* mixer since the output is zero when the switch turns off. If the resistor R_L is replaced with a capacitor, the mixer operates as a sample-and-hold circuit, because the output does not fall to zero when the switch is off, resulting in an higher conversion gain. That configuration is called *non-return-to-zero* mixer.

In modern RF design, the mixers are realized as a single-balanced (have a single-ended input), as shown in Figure 2.22, or as double-balanced (have a differential input), instead of the single-ended topology of Figure 2.21. With this techniques is possible to obtain a conversion gain twice than the *return-to-zero* mixer, because the output signal is differential. The double-balanced mixer also eliminates the LO-IF feed-through, which translates the LO frequency to the output and can affect the mixer performance.

Current-Driven Passive Mixers

If the LNA as an high output impedance, it can be seen as a current source. Thus, the input of the passive mixer is driven by a current source instead of a voltage source, and exhibit different properties (gain, noise, input impedance, etc.). Since a mixer is a *time-variant* circuit, the input impedance of a current-driven mixer is very different from a

[2]This guarantees that when the LO signal is high the transistor operates in the deep triode region.

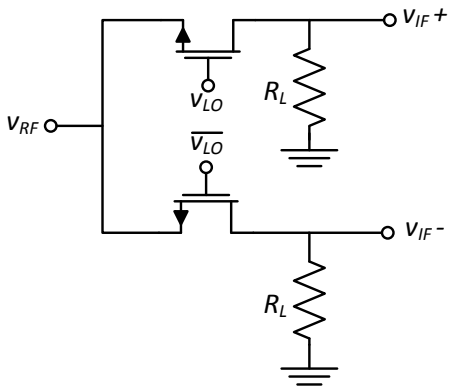
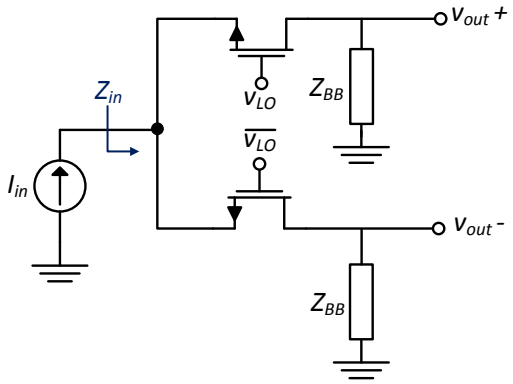


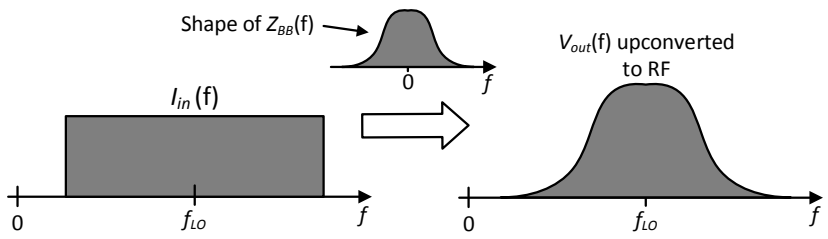
Figure 2.22: Single-balanced passive mixer using a MOS switch

voltage-driven mixer.

Considering the circuit of Figure 2.23a, from [22] is possible to conclude that the switches mix the baseband waveforms with the LO, translating its spectrum to RF, as shown in Figure 2.23b. Due to this effect, the input impedance around f_{LO} is a frequency-translated version of $Z_{BB}(f)$, i.e., if Z_{BB} is a low-pass impedance (e.g. a capacitor), then $Z_{in}(f)$ has a band-pass behavior. As will be analyzed in this work, this property can be very helpful to filter undesired components of the RF signal. Another advantage of this kind of mixer is that a device in series with a current source does not change the current that passes through it, so its noise and non-linearity contributions are very reduced.



(a)



(b)

Figure 2.23: (a) Current-driven passive mixer, (b) input spectrum

As will be demonstrated later the passive mixers do not need to use a 50% LO duty-cycle, and the use of another duty-cycles (p. ex. 25%) can be very beneficial in terms of gain, noise figure, harmonic rejection, among others [23].

2.4.3 Active Mixers

Unlike passive mixers, this topologies provide conversion gain greater than one that helps to reduce the effect of noise generated by subsequent stages, as demonstrated in section 2.1.4.3. Due to this property, these mixers are very used in RF systems. The mixing operation is very similar to the passive mixers but instead of being used a MOS switch, a differential pair is used, as shown in Figure 2.24, that operates in the saturation region, and consequently provides current gain and high output impedance. In this structure, known as *single-balanced active mixer*, the current source is controlled by the RF signal and the differential pair is controlled by the LO signal. It converts the v_{RF} to a current that flows to one branch of the differential pair (where it is amplified) according to the value of v_{LO}, and it is converted again to voltage by the resistors R_D, generating the output differential voltage v_{IF}. Since it is single-balanced, this mixer only operates with a single-ended RF input.

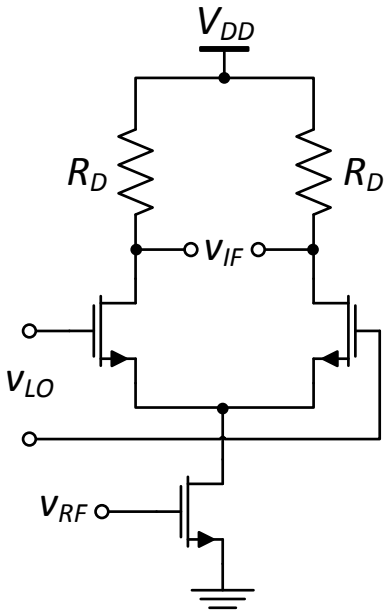


Figure 2.24: Single-balanced active mixer (adopted from [3])

Another very popular implementation is the Gilbert cell [24], also called *double-balanced active mixer*, as shown in Figure 2.25, which as higher gain, lower NF, good linearity, higher spurious rejection, higher port-to-port isolation and is less sensitive to even order distortion, comparing with the single-balanced implementation. Due to its complexity and number of active devices, the main drawbacks of this topology are the power consumption and the increased area. Since it is double-balanced, this mixer needs a differential RF signal at the input to operate properly.

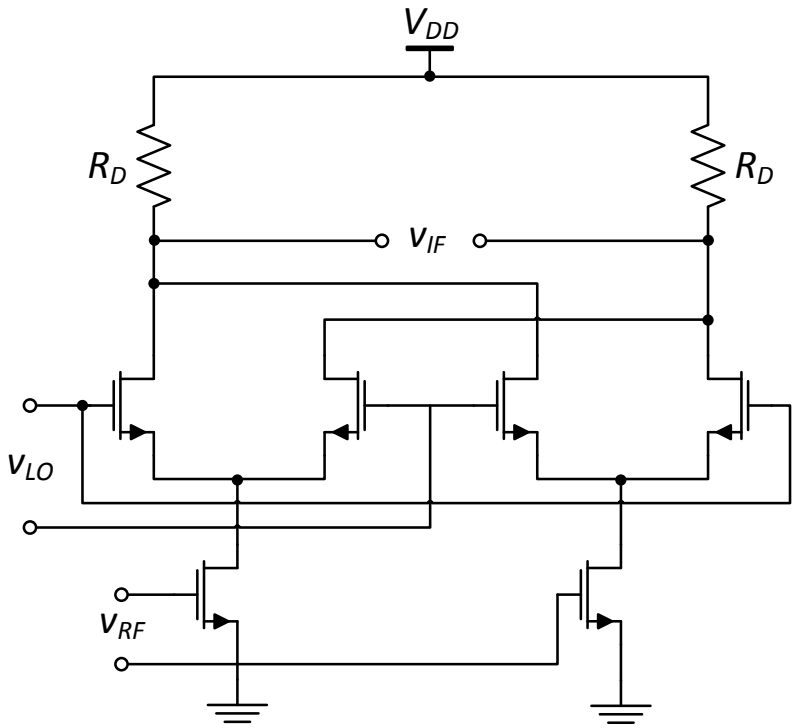


Figure 2.25: Double-balanced active mixer (adopted from [3])

2.4.4 Discussion

In this section two main mixer architectures were presented: *passive* and *active*. The passive mixers do not offer conversion gain but are very low power, have low noise and high linearity. Also, a passive mixer can be current-driven instead of voltage-driven, which have some advantages like baseband impedance transformation and low noise and nonlinearity contributions. The active mixers have as main advantage the conversion gain greater than one that helps to reduce the noise contribution of the subsequent stages of the receiver, but have more power consumption, noise (since they have DC current they produce flicker noise), occupy more area due its complexity and have lower linearity.

Regarding the mixer inputs and outputs, the two main configurations are the *single-balanced* and the *double-balanced*. Both have differential outputs, which doubles the mixer gain relatively to a single-ended topology (Figure 2.21). The single-balanced implementation needs a single-ended signal at the input while the double-balanced needs a differential signal at the input, which sometimes requires the use of a balun, but has advantages in terms of gain, noise, linearity, port-to-port feed-through (especially LO-IF), among others. The disadvantages of double-balanced mixers comparing with single-balanced mixers are the power consumption and increased area, due to the larger number of active elements.

2.5 RF Filters

With the growth of wireless communications the demanding of high-performance RF (or microwave) filters is becoming huge due to the limitations of the frequency spectrum and the consequently increase of communication standards. The frequencies that are used to transmit the information are closer to each other, which means that there are more interferers near the band of interest that need to be filtered in order to prevent the leakage of out-of-band inter-modulation products and harmonics to the receiver [25]. Due to this proximity, the filters must have an high Q factor, to suppress the nearest interferers, and low losses in the interesting band, in order to not attenuate the desired signals.

A key filter in a RF receiver AFE is the SAW filter, shown in Figure 2.26, that attenuates the out-of-band blockers at the input of the receiver and consequently prevents the LNA saturation. The major problem of this filter is that it is very expensive and bulky, and have insertion loss since is usually based in resonators [7]. In a passive filter based in resonators the insertion loss is inversely proportional to its bandwidth and resonator Q factor, and is proportional to the number of resonators [25]. Also, high-Q resonators are physically large. Active filters can be used to avoid this problem, since they have gain that compensates for the losses related with the resonators, but they suffer from harmonic distortion, increased NF and non-linearities [26]. In order to save in area and cost, filters based on resonators can be implemented in CMOS technologies and integrated in the receiver chip. However, unlike the off-chip filters, on-chip filters have low-Q factor, limited tuning range and the integrated coils take large chip area. There are some techniques to increase the Q factor but they degrade the filter noise and linearity [9].

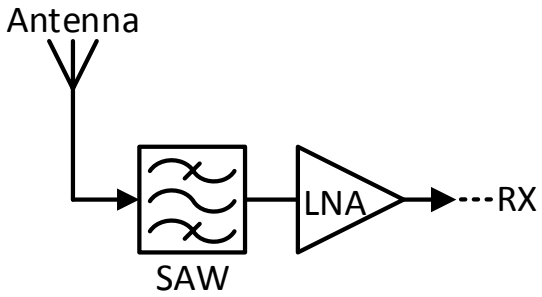


Figure 2.26: Receiver AFE input

To overcome the problems of resonator based filters, an old technique, called N-path filtering [27], has been widely used in modern receivers, including this work. This solution is based in current-driven passive mixers, referred in section 2.4.2, and allows the realization of a passive filter without inductors that can be precisely controlled by the LO frequency, resulting in a very programmable filter that occupies low area. Also, these filters have high linearity, an acceptable NF and an high-Q factor (e.g. Q = 98 for 6.1 MHz bandwidth around 600 MHz) [7–10], as will be demonstrated later in this work. Due to its simplicity, this kind of filters can be easily integrated in the receiver chip, avoiding the

use of off-chip SAW filters.

Bandpass Filter Quality Factor

The quality factor (usually referred as Q factor) is a key parameter to measure the performance of a BPF. The expression of the Q factor is given by

$$Q = \frac{\omega_0}{BW}, \tag{2.46}$$

where ω_0 is the filter center frequency and BW is the filter bandwidth, which is given by $BW = \omega_2 - \omega_1$. Frequencies ω_1 and ω_2 are the frequencies at which the magnitude response of the filter drops 3 dB relatively to its maximum value (at ω_0), as shown in Figure 2.27.

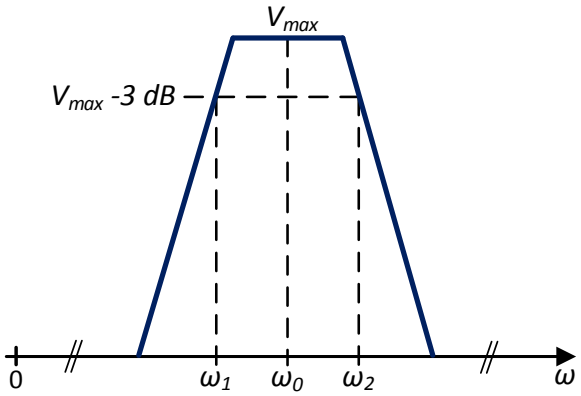


Figure 2.27: BPF frequency response and Q factor

Thus, the Q factor is a parameter that measures the filter sharpness (or selectivity) and as higher the Q factor is, the better is the filter. This means that an high-Q BPF can block undesired signals that are closer to the band of interest, comparing with a low-Q BPF.

2.6 Analog-to-Digital Converters

Although the incoming signals of a RF receiver are in the analog domain, since the physical world is analog, with the evolution of the technology those signals began to be processed in the digital domain because digital systems are more simple, cheap and flexible. To make this possible is necessary to employ an ADC, as shown in Figure 2.28, that converts an analog signal to the digital domain. Due to the performance requirements needed to digitize a RF signal, the ADC can not be moved towards the antenna because a converter that fulfill these requirements is impractical in actual CMOS technology. This is why the AFE has a very important role in wireless communications, because it converts the RF signal to an analog signal that can be handled by the ADC.

B_{out} is the digital output word generated by the ADC with respect to the analog input signal V_{in} and the analog reference signal V_{ref}. It is important to note that the ADCs can

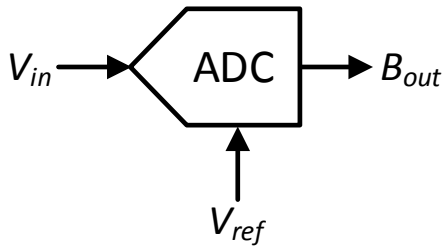


Figure 2.28: ADC block diagram

be voltage or current-driven, as will be verified in this work.

There are two main ADC types: *Nyquist-rate* and *oversampling*. The *Nyquist-rate* ADCs generate output values that has a one-to-one correspondence whit a single input value and usually operate at 1.5 to 10 times the Nyquist rate. The *oversampling* ADCs operate much faster than the input signal Nyquist rate and filter the quantization noise that is not in the desired signal's bandwidth, in order to increase the output SNR [15]. This type of ADCs are very popular for high-resolution medium-to-low-speed applications because they allow to relax the requirements of the analog circuitry and consequently reduce the circuit area and power consumption. Also, this type of ADCs allow the extraction of extra bits of resolution than the Nyquist-rate converters, due to signal oversampling. The devices that perform this kind of conversions are usually called $\Sigma\Delta$ modulators [15].

This project do not consist in the design of an $\Sigma\Delta$ modulator so only a very short summary of this kind of converters is presented.

3

Wideband Cascode Balun-LNA

A balun (which performs conversion from single-ended to differential) wideband LNA, based in [4, 5], has been proposed. This topology is a good solution to integrate in a RF receiver because it can be directly coupled to a differential mixer without a separate balun or impedance matching networks, while performing noise and distortion cancellation through the CS stage. Since the output is differential it reduces harmonic distortion, improving the linearity, and rejects power supply and substrate noise. The cascode devices are used to allow the integration of a passive filter in the LNA nodes, as will be demonstrated, but also contributes to decrease the effective input capacitance, which helps to improve the impedance matching over the working band, and to increase the voltage gain. In order to improve the LNA voltage gain and NF some existing techniques were employed [28]. This design was implemented in two different technologies, CMOS 130 nm and CMOS 65 nm, that will be detailed and compared in the following sections.

This chapter is structured as follows: a theoretical analysis of the LNA is made and the main equations for its characterization are derived and validated through simulation, for both technologies.

3.1 Theoretical Analysis

The proposed LNA is represented in Figure 3.1. From basic circuit analysis it is known that the CG and CS configurations have approximately the same voltage gain, in module, but with opposite phase. Thus, the signal at the output of the CG stage (M_1) is equal to the input signal amplified, whereas the CS (M_2) has the opposite phase, and the LNA output signal is equal to the sum of the signals of these two stages since $v_{out} = v_{out+} - v_{out-}$. On the other hand, the thermal noise produced by the CG stage (and modeled by $\overline{i_n}$)

generates a noise voltage $\overline{v_{n,in}}$ at the input of the CS stage, since it flows into R_S. It also generates a noise voltage $\overline{v_{n,out+}}$, with opposite phase, at the CG output. Since the CS inverts the voltage phase, both noise voltages at the output of the CG and the CS have the same signal, and are canceled at the output of the LNA. To a full noise cancellation it is critical that the gain of both stages is matched.

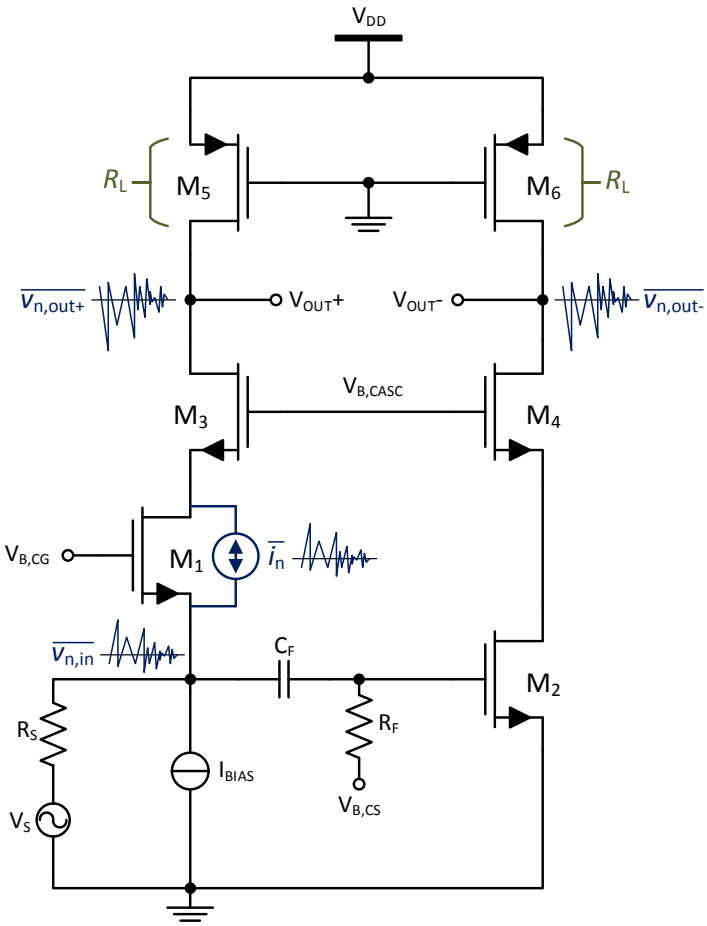


Figure 3.1: Wideband cascoded balun LNA with CG noise cancellation

In order to improve the LNA behavior, the traditional load resistors were replaced by PMOS transistors (M_5 and M_6) that operate in the triode region [28]. Thus, the impedance seen at the LNA output nodes is approximately given by $R_L = r_{ds} = 1/g_{ds}$, where g_{ds} is the transistor output conductance. By employing this technique is possible to increase the incremental load resistance with the same DC voltage drop, comparing with traditional resistors, and consequently increase the voltage gain and reduce the circuit's NF.

The following circuit equations are derived neglecting the transistors capacitive effects, the CG transistor body effect and the short-channel effects (due to the use of the minimum L allowed by the technology in the transistors), for simplicity.

3.1.1 Input Impedance

Assuming that the biasing current-source I_{bias} has a very high output impedance, the LNA input impedance is given by the parallel of the CG and CS stages,

$$Z_{in} \cong Z_{in,CG} \parallel Z_{in,CS}. \tag{3.1}$$

Since the CS input is the transistor gate, which have a very high impedance, Z_{in} can be expressed by [15]

$$Z_{in} \cong Z_{in,CG} \cong \frac{1}{g_{m,CG}} \left(1 + \frac{R_{casc}}{r_{ds,CG}}\right), \tag{3.2}$$

where $g_{m,CG}$ and $r_{ds,CG}$ are, respectively, the transconductance and the output resistance of the CG transistor. The R_{casc} is the impedance seen from the cascode transistor (M_3) input (source) and is very similar to (3.2):

$$R_{casc} \cong \frac{1}{g_{m,Casc}} \left(1 + \frac{R_L}{r_{ds,Casc}}\right), \tag{3.3}$$

where $g_{m,Casc}$ and $r_{ds,Casc}$ are, respectively, the transconductance and the output resistance of the cascode transistor. For simplicity, considering that $r_{ds,Casc} \gg R_L$ and $r_{ds,CG} \gg R_{casc}$, then

$$Z_{in} \approx \frac{1}{g_{m,CG}}. \tag{3.4}$$

3.1.2 Voltage Gain

Given that the LNA output is differential and the input signal of both stages is the same, the voltage gain is given by [15]

$$A_v = A_{v,CG} - A_{v,CS} \cong g_{m,CG} \cdot R_{out} + g_{m,CS} \cdot R_{out} \tag{3.5}$$

because the voltage gain of the CS has the opposite signal of the CG. R_{out} is the LNA output impedance seen at one node and is expressed by $R_{out} = r_{CG} \parallel R_L$ in the CG stage and $R_{out} = r_{CS} \parallel R_L$ in the CS stage, where r_{CG} and r_{CS} are the impedances seen from the output of the cascode devices of the CG and CS stages, respectively, and are given by $r_{Cx} \cong r_{ds,Cx} \cdot r_{ds,Casc} \cdot g_{m,Casc}$. Therefore, considering that r_{CG} and r_{CS} are very high comparing with R_L, then $R_{out} \approx R_L$ and consequently

$$A_v \approx g_{m,CG} \cdot R_L + g_{m,CS} \cdot R_L. \tag{3.6}$$

Since both stages need to have the same gain to allow the full cancellation of the CG noise,

$$A_v \approx 2 \cdot g_{m,CG} \cdot R_L \tag{3.7}$$

It is important to note that the cascode devices increase the output impedance of the transconductors (input transistor plus cascode) but do not affect the voltage gain of the LNA because these impedances (r_{CG} and r_{CS}) are much higher than the resistance of the PMOS devices (R_L), as explained before. Thus, from (3.5) is easy to understand that increasing the resistance R_L still improving the voltage gain comparatively with a LNA without the cascodes, because r_{CG} and r_{CS} have almost no influence in R_{out}, since they are in parallel with R_L.

3.1.3 Noise Factor

The noise factor (or Noise Figure (NF) when expressed in dB) referred in 2.1.4.3, is one of the most important measurements of a LNA, because this circuit is intended to have low noise contributions since they have an huge impact in the receiver's total NF. Since the cascode devices don't force current into the LNA, their noise contributions are very reduced (it was verified by simulation that these transistors have a noise contribution between 3% and 5% of the total LNA's circuit) and consequently M_3 and M_4 were ignored in this analysis, i.e. the analysis was made considering the basic CG and CS topologies. Also, only the transistors' thermal noise was considered, since flicker noise is negligible at high frequencies.

3.1.3.1 Common-Gate Stage

The CG stage small signal noise model is presented in Figure 3.2. There are three main noise sources that will be considered in this analysis: due to the source resistor (R_S), due to the CG transistor (M_1) and due to the load resistor (R_L). All of these sources will be analyzed separately, ignoring the other noise sources, and added together in order to obtain the stage's noise factor. For simplicity, it was considered that $g_{m_1} \gg g_{ds_1}$ and $r_{ds_1} \gg R_L$ in all calculations.

Thermal noise due to R_S

Considering only the noise source from R_S, in Figure 3.2, the output noise power is given by

$$\overline{V^2_{nR_S,out_{CG}}} = \overline{V^2_{nR_S}} A^2_{v,CG}. \tag{3.8}$$

In a CG stage, $A_{v,CG} \approx \frac{g_m R_L}{1+g_m R_S}$ [14] and from (2.18) it is known that $\overline{V^2_{nR_S}} = 4kTR_S$, which leads to

$$\overline{V^2_{nR_S,out_{CG}}} \approx \frac{4kTR_S \left(g_{m_1} R_L\right)^2}{(1+g_{m_1} R_S)^2}. \tag{3.9}$$

Thermal noise due to M_1

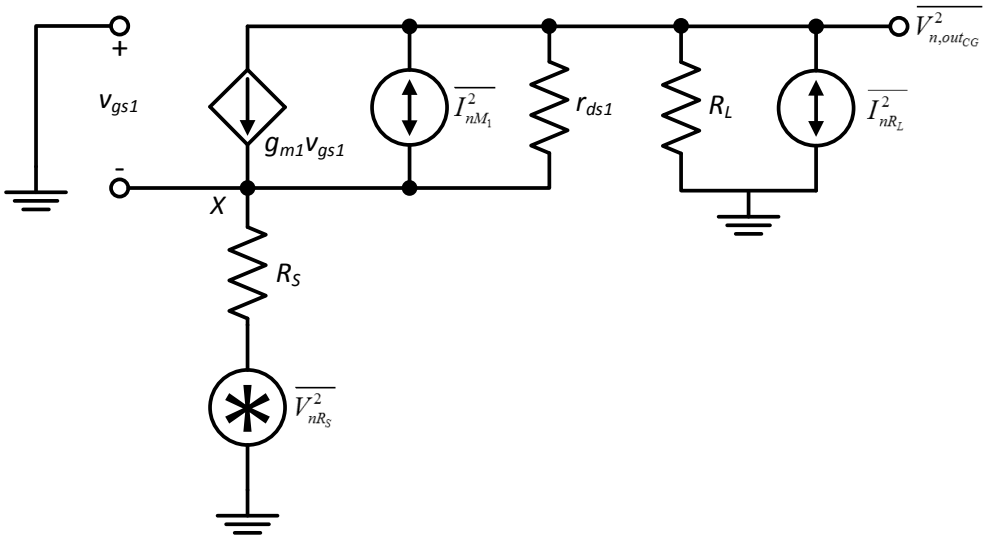


Figure 3.2: Small signal noise model of the CG stage

Considering only the noise source from M_1, in Figure 3.2, and applying the KCL at node X, is possible to obtain

$$i = \frac{I_{nM_1} - g_{ds_1} \cdot V_{nM_1,out_{CG}}}{1 + R_S(g_{m_1} + g_{ds_1})}, \tag{3.10}$$

which results in the following output noise voltage:

$$V_{nM_1,out_{CG}} = i \cdot R_L \approx I_{nM_1} \frac{R_L}{1 + g_{m_1} R_S}. \tag{3.11}$$

From (2.19) it is known that $\overline{I^2_{nM_1}} = 4kT\gamma g_{m_1}$, leading to

$$\overline{V^2_{nM_1,out_{CG}}} \approx 4kT\gamma g_{m_1} \left(\frac{R_L}{1 + g_{m_1} R_S} \right)^2. \tag{3.12}$$

Thermal noise due to R_L

Finally, and considering only the noise source from R_L, in Figure 3.2, and taking into account that $v_{gs_1} = 0$ V (since R_S is ignored),

$$V_{nR_L,out_{CG}} = I_{nR_L}(r_{ds_1} \parallel R_L) \approx I_{nR_L} R_L. \tag{3.13}$$

The noise voltage at the CG input due to R_L is equal to

$$V_{nR_L,in} = \frac{V_{nR_L,out_{CG}}}{A_{v,CG}} \approx \frac{I_{nR_L} R_L}{A_{v,CG}}. \tag{3.14}$$

However, this result does not take into account the effect of R_S. Considering the Thevenin's equivalent of the CG input, shown in Figure 3.3, the voltage at the transistor's input is

given by (3.15) [4].

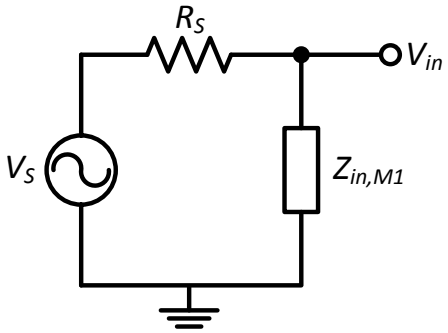


Figure 3.3: CG Thevenin's equivalent circuit

$$V_{in} = \frac{Z_{in,M_1}}{Z_{in,M_1} + R_S} V_S \approx \frac{1}{1 + g_{m_1} R_S} V_S, \tag{3.15}$$

with $Z_{in,M_1} \approx 1/g_{m_1}$ as stated in (3.4). Substituting V_S by (3.14) leads to

$$V_{in} \approx \frac{1}{1 + g_{m_1} R_S} \cdot \frac{I_{nR_L} R_L}{A_{v,CG}}. \tag{3.16}$$

Considering that $\overline{V^2_{nR_L,out_{CG}}} = \overline{V^2_{in}} A^2_{v,CG}$ and $\overline{I^2_{nR_L}} = 4kT/R_L$ (from (2.18)), is possible to obtain the following output power noise, considering R_S,

$$\overline{V^2_{nR_L,out_{CG}}} \approx \frac{4kTR_L}{(1 + g_{m_1} R_S)^2}. \tag{3.17}$$

Noise Factor

As stated in (2.23), the CG stage noise factor is given by

$$F = \frac{\overline{V^2_{n,out_{CG}}}}{\overline{V^2_{nR_S}} \cdot A^2_{v,CG}}, \tag{3.18}$$

where

$$\overline{V^2_{n,out_{CG}}} = \overline{V^2_{nR_S,out_{CG}}} + \overline{V^2_{nM_1,out_{CG}}} + \overline{V^2_{nR_L,out_{CG}}}. \tag{3.19}$$

The noise factor is

$$F \approx 1 + \frac{\gamma}{g_{m_1} R_S} + \frac{1}{g^2_{m_1} R_S R_L} \tag{3.20}$$

3.1.3.2 Common-Source Stage

The CS stage small signal noise model is presented in Figure 3.4. As with the CG stage, there are three main noise sources: due to the source resistor (R_S), due to the CS transistor (M_2) and due to the load resistor (R_L). For simplicity, it was considered that $r_{ds_2} \gg R_L$ in all calculations.

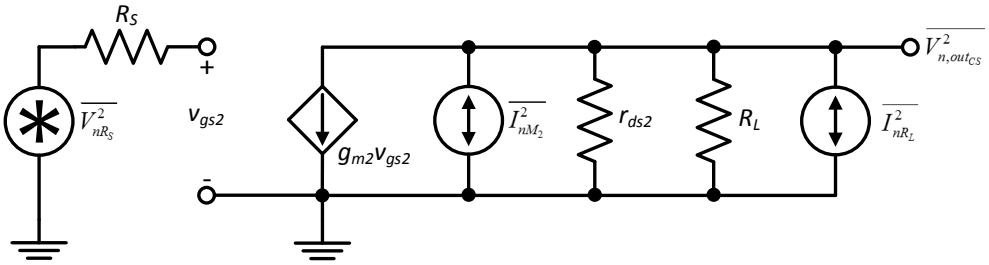


Figure 3.4: Small signal noise model of the CS stage

Thermal noise due to R_S

Considering only the noise source from R_S, in Figure 3.4, the output noise power can be written as

$$\overline{V^2_{nR_S,out_{CS}}} = \overline{V^2_{nR_S}} A^2_{v,CS}. \tag{3.21}$$

In a CS stage, $A_{v,CS} \approx -g_m R_L$ [14] and from (2.18) it is known that $\overline{V^2_{nR_S}} = 4kTR_S$, resulting in

$$\overline{V^2_{nR_S,out_{CS}}} \approx 4kTR_S \cdot g^2_{m_2} \cdot R^2_L. \tag{3.22}$$

Thermal noise due to M_2

Considering only the noise source from M_2, in Figure 3.4, and knowing that in this configuration $v_{gs_2} = 0$ V,

$$V_{nM_2,out_{CS}} = I_{nM_2}(r_{ds_2} \parallel R_L) \approx I_{nM_2} R_L. \tag{3.23}$$

From (2.19) it is known that $\overline{I^2_{nM_2}} = 4kT\gamma g_{m_2}$, and consequently

$$\overline{V^2_{nM_2,out_{CS}}} \approx 4kT\gamma g_{m_2} R^2_L. \tag{3.24}$$

Thermal noise due to R_L

Finally, considering only the noise source from R_L, in Figure 3.2, and given that $v_{gs_2} = 0$ V, the output noise voltage is given by

$$V_{nR_L,out_{CS}} = I_{nR_L}(r_{ds_2} \parallel R_L) \approx I_{nR_L} R_L. \tag{3.25}$$

From (2.18) it is known that $\overline{I^2_{nR_L}} = 4kT/R_L$, which leads to

$$\overline{V^2_{nR_L,out_{CS}}} \approx 4kTR_L. \tag{3.26}$$

Noise Factor

As shown in (2.23), the CS stage noise factor is given by

$$F = \frac{\overline{V_{n,out_{CS}}^2}}{\overline{V_{nR_S}^2} \cdot A_{v,CS}^2}, \tag{3.27}$$

with

$$\overline{V_{n,out_{CS}}^2} = \overline{V_{nR_S,out_{CS}}^2} + \overline{V_{nM_2,out_{CS}}^2} + \overline{V_{nR_L,out_{CS}}^2}, \tag{3.28}$$

resulting in the following CS noise factor

$$F \approx 1 + \frac{\gamma}{g_{m_2} R_S} + \frac{1}{g_{m_2}^2 R_S R_L}. \tag{3.29}$$

3.1.3.3 Complete LNA

Comparing (3.20) and (3.29) is possible to conclude that the noise factors of CG and CS stages are identical. Since the noise generated by the CG stage appears at the CS input, is necessary to obtain the noise power generated by the CG that manifests at the output of the CS, i.e. is necessary to divide the noise generated by the CG stage by the CG gain and multiply it by the CS gain, as shown in the following equations. Initially, the noise generated by R_S is neglected and added in the final equation, as with the thermal noise analysis of R_L in the CG stage. For simplicity, is assumed that $g_{m_1} = g_{m_2}$, as explained in section 3.1.2.

$$\overline{V_{nM_1,out_{CS}}^2} = \overline{V_{nM_1,out_{CG}}^2} \frac{A_{v_{CS}}^2}{A_{v_{CG}}^2} \approx 4kT\gamma g_m R_L^2 \tag{3.30}$$

$$\overline{V_{nR_L,out_{CS}}^2} = \overline{V_{nR_L,out_{CG}}^2} \frac{A_{v_{CS}}^2}{A_{v_{CG}}^2} \approx 4kTR_L \tag{3.31}$$

Obviously, the noise generated by the CS also appears at the CG output, so is necessary to perform an identical operation for these noise contributions.

$$\overline{V_{nM_2,out_{CG}}^2} = \overline{V_{nM_2,out_{CS}}^2} \frac{A_{v_{CG}}^2}{A_{v_{CS}}^2} \approx \frac{4kT\gamma g_m R_L^2}{(1 + g_m R_S)^2} \tag{3.32}$$

$$\overline{V_{nR_L,out_{CG}}^2} = \overline{V_{nR_L,out_{CS}}^2} \frac{A_{v_{CG}}^2}{A_{v_{CS}}^2} \approx \frac{4kTR_L}{(1 + g_m R_S)^2} \tag{3.33}$$

The total noise at the LNA output is given by the sum of all the noise contributions of both stages, $\overline{V_{n,out_{LNA}}^2} = \overline{V_{n,out_{CG}}^2} + \overline{V_{n,out_{CS}}^2}$,with

$$\overline{V_{n,out_{CG}}^2} = \overline{V_{nM_1,out_{CG}}^2} + 2\overline{V_{nR_L,out_{CG}}^2} + \overline{V_{nM_2,out_{CG}}^2} \tag{3.34}$$

$$\overline{V_{n,out_{CS}}^2} = -\overline{V_{nM_1,out_{CS}}^2} + 2\overline{V_{nR_L,out_{CS}}^2} + \overline{V_{nM_2,out_{CS}}^2} \tag{3.35}$$

Since the CS inverts the signals at its input, the thermal noise generated by the CG transistor (M_1) appears at the CS output with opposite signal, as shown in (3.35), and is canceled as desired. Thus, the LNA's thermal noise depends only of M_2 and R_L. Applying the same logic as in (3.15), the LNA noise factor is given by

$$F = \frac{(1+g_m R_S)^2(\overline{V_{nR_S}^2}A_{v_{LNA}}^2 + \overline{V_{n,out_{LNA}}^2})}{(1+g_m R_S)^2\overline{V_{nR_S}^2}A_{v_{LNA}}^2} = 1 + \frac{\overline{V_{n,out_{CG}}^2} + \overline{V_{n,out_{CS}}^2}}{\overline{V_{nR_S}^2}A_{v_{LNA}}^2}, \tag{3.36}$$

with $A_{v_{LNA}} \approx 2 \cdot g_{m,CG} \cdot R_L$, as stated in (3.7), and $\overline{V_{nR_S}^2} = 4kTR_S$. Solving the previous equation, and assuming that in the CG stage $g_m R_S \ll 1$ for simplicity,

$$F \approx 1 + \frac{\gamma}{2g_m R_S} + \frac{1}{g_m^2 R_S R_L}. \tag{3.37}$$

As stated before, the previous equation shows that by increasing the load resistance R_L is possible to decrease the circuit NF.

3.1.4 Load Transistors Resistance

As explained before, PMOS devices (M_5 and M_6) were used to replace the traditional load resistors. These transistors work in the triode region and behave like a voltage controlled-resistor with V_{GS} used as control terminal. At this region, the current that passes through a PMOS transistor is given by [15]

$$I_D = \mu_P C_{ox}\frac{W}{L}\left[(|V_{GS}| - |V_{tp}|)\,|V_{DS}| - \frac{V_{DS}^2}{2}\right], \tag{3.38}$$

which leads to

$$R_L = r_{ds} = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1} = \frac{1}{\mu_P C_{ox}\frac{W}{L}\left(|V_{GS}| - |V_{tp}| - |V_{DS}|\right)}. \tag{3.39}$$

From the previous equation is possible to conclude that if $|V_{DS}|$ (also referred as V_{R_L} in this work) is increased, the resistance R_L also increases, and the voltage gain becomes higher, as demonstrated before. Another option is to decrease $V_{DSsat} = V_{GS} - V_{tp}$. However, too keep the transistor operating at the triode region is necessary to guarantee that $0 < |V_{DS}| < |V_{DSsat}|$ and if V_{DSsat} is reduced, this condition is more complicated to accomplish. For this work it was chosen $V_G = 0$ V, which leads to $|V_{GS}| = V_{DD}$ (because the source of the transistors is connected to V_{DD}) and guarantees that $|V_{DSsat}| > |V_{DS}|$, as desired. By changing the transistors width (*W*) is possible to change V_{R_L} to the intended value, and consequently change R_L.

As stated in (2.18) and (2.19), the thermal noise generated by a MOS transistor is

given by $\overline{I_{n,MOS}^2} = 4kT\gamma g_m$ and the thermal noise generated by a resistor is given by $\overline{I_{n,res}^2} = 4kT/R$. Considering that for a transistor operating in triode region $\gamma = 1$,

$$\frac{\overline{I_{n,MOS}^2}}{\overline{I_{n,res}^2}} = \frac{4kTg_m}{4kT/R} = g_m \cdot R. \tag{3.40}$$

For example, to obtain a resistance of $400\ \Omega$, in a PMOS device is necessary a $g_m \approx 1.6$ mS (for CMOS 130 nm technology) and a resistor of $R = 400\ \Omega$. Thus, from (3.40) is possible to conclude that $\overline{I_n^2, MOS} \approx 0.64 \cdot \overline{I_n^2, res}$, which means that a transistor operating at triode generates less thermal noise than a resistor. Also, since the voltage gain of the LNA is higher, the associated NF is lower, as stated in (2.23). Due to the high circuit operating frequencies, the flicker noise is negligible. This analysis proves that using PMOS transistors as active loads, instead of resistors, increases the overall LNA performance, increasing the voltage gain and reducing the NF.

This increase of the load resistance, compared with traditional resistors, also contributes to the increase of the LNA output impedance, since $R_{out} = r_{CG} \parallel R_L$. Since the mixer of the AFE is current-driven, as will be shown later, the LNA's output impedance needs to be high in order to approximate an ideal current source and guarantee the mixer proper functioning.

As disadvantages, the bandwidth of the LNA is lower due to the transistors capacitances that reduces the frequency of the pole of the output node (dominant pole), and the linearity suffers a penalty mainly due to the improvement of the voltage gain and the intrinsic nonliniarities of MOS transistors [28].

3.2 Circuit Implementation using CMOS 130 nm

Given that the typical impedance of an antenna is 50 Ω, the LNA was designed to have the same input impedance, to allow the maximum power transfer, as referred in section 2.1.1. The circuit's supply voltage is $V_{DD} = 1.2$ V. The biasing current was chosen to be 1.5 mA and $V_{R_L} = 600$ mV, in order to have high load resistance values while ensuring the sufficient DC voltage to keep all the transistors in the active region. The cascodes were designed to have a reasonable input impedance to allow the integration of the BPF that will be studied in the next chapter. In order to be possible to achieve the desired frequencies, all the transistors have the minimum channel length (L) allowed by the CMOS 130 nm technology, which is 120 nm. The capacitor $C_F = 5$ pF and the resistor $R_F = 20$ kΩ are intended to isolate the CG and CS stages at DC, allowing both stages to have a DC operating point independent of each other. They act as a Highpass Filter (HPF) with a bandwidth of approximately 1.6 MHz.

From (3.4) is possible to fix the transconductance of M_1, and consequently of M_2 (since the voltage gain of both stages needs to be equal to achieve the CG full noise cancellation), in 20 mS. Different $g_m - R_L$ relations was studied in [4, 5] but they consume more power and this LNA is intended to have low current consumption. The DC voltage $V_{B,CG}$ was

chosen in order to keep the desired operation of the transistor and give some room to implement a bias current source with a simple current-mirror. The DC voltage $V_{B,CS}$ is used to adjust the DC current of M_2 to the desired value of 1.5 mA. Finally, $V_{B,Casc}$ was chosen to be equal to V_{DD} in order to allow all transistors to operate in the active region and ensure a low g_m (and consequently an high input impedance) of the cascode devices.

With respect to the cascode transistors, they were projected to have an input impedance of about 300 Ω. This impedance value was chosen considering the filter that will be employed at the cascodes input, and will be detailed in the next chapter. Since this impedance is given by (3.3), to achieve $R_{casc} \approx 300\ \Omega$ is necessary to have $g_{m,Casc} \approx 3.3$ mS. Notice that if R_{casc} is very large, $g_{m,Casc}$ needs to be very small and, since $g_m = 2I_D/V_{DSsat}$ and I_D is fixed, V_{DSsat} becomes very large. In order to keep all the transistors in the active region $V_{DS} > V_{DSsat}$, so if the input impedance of the cascodes is very large, the transistors V_{DS} needs also to be very large and is more difficult to keep all the transistors in the active region, because the supply voltage is limited to 1.2 V.

Simulation Results

To verify the LNA parameters equations that were previously analyzed, some simulations were made taking into account the circuit constraints that were referred before. Table 3.1 shows the transistors dimensions, used in the simulation, and their DC operating points (operating region, DC current, V_{DSsat} and g_m).

Table 3.1: LNA parameters (CMOS 130 nm)

Transistor	W (μm)	L (μm)	Region	I_D (mA)	V_{DSsat} (V)	g_m (mS)
M_1	75.2	0.12	active	1.50	109.6	20.1
M_2	230.4	0.12	active	1.52	77.8	27.3
M_3	5.6	0.12	active	1.50	298.1	3.8
M_4	5.6	0.12	active	1.52	301.2	3.7
M_5	7.2	0.12	triode	1.50	-736.7	1.9
M_6	7.2	0.12	triode	1.52	-737.5	1.9

The chosen bias voltages are $V_{B,CG} = 535$ mV and $V_{B,CS} = 383$ mV. Relatively to M_1 and M_2 dimensions, the difference of sizes is explained by the body effect that were ignored in the theoretical analysis and affects the CG transistor, increasing its gain. To compensate this problem is necessary to increase the CS transistor g_m in order to obtain the same voltage gain at both stages. To increase g_m, V_{DSsat} should be decreased (because g_m is inverse to this voltage, as referred previously), which leads to a larger transistor. With respect to transistors M_3 and M_4, the high V_{DSsat} is due to the lower g_m that is needed to achieve a node input impedance of about 300 Ω, as desired. Regarding the load resistance R_L (transistors M_5 and M_6), it was obtained a value of approximately 724 Ω for the desired voltage drop of $V_{R_L} = 600$ mV. As expected, these transistors operate at the triode region. If traditional resistors were used, $R_L = 600\text{mV}/1.5\text{mA} = 400\ \Omega$, resulting in a lower voltage gain and output impedance, and an higher NF.

As shown in Figure 3.5, the LNA input impedance is about $74\,\Omega$ for lower frequencies and starts to decrease at higher frequencies, achieving the value of $60\,\Omega$ at 1 GHz, which is different from the target (equation (3.4)). This difference is mainly due to the fact that the output impedance of the CG transistor ($r_{ds,CG}$) is not much larger than the input impedance of the cascodes (R_{casc}), as assumed in (3.4). This leads to an increase of the LNA input impedance, as stated in (3.2). The decrease of the LNA input impedance for higher frequencies is related with the parasitic capacitances of the transistors, that were neglected in the section 3.1.1. However, despite this deviation from the desired value, it was obtained $S_{11} < -10$ dB for frequencies below 3.6 GHz, as shown in Figure 3.6, which means that the input of the LNA is matched for these frequencies.

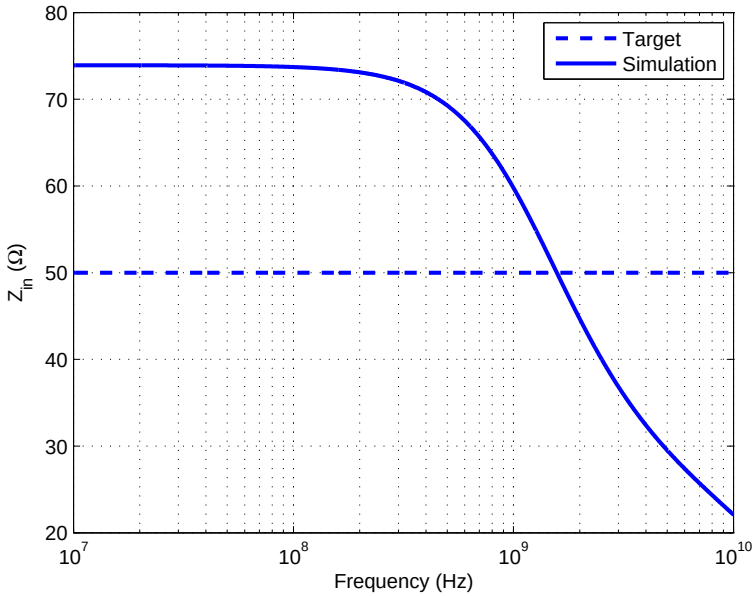


Figure 3.5: LNA input impedance

The LNA voltage gain, illustrated in Figure 3.7, is approximately 27.4 dB for lower frequencies. The LNA has a bandwidth of 2.36 GHz and for this design was considered a working band between 300 MHz (due to NF as will be explained) and 1 GHz, which is suitable for the desired applications. The low bandwidth (comparing with other similar designs [4, 28]) is related with the load PMOS devices, as explained before, and with the cascode devices that also contributes with parasitic capacitances to the output node, decreasing the dominant pole frequency. The difference between the theoretical and simulated voltage gain is explained by the output impedance. At (3.6) it was assumed that $R_{cx} >> R_L$, which was not verified during the simulations and has as consequence the reduction of the voltage gain, because both resistances are in parallel. Also, the cascode parasitic capacitances have a negative influence in the circuit's voltage gain, due to the reduction of the cascodes' output impedance (r_{Cx}), and were not considered in the theoretical analysis.

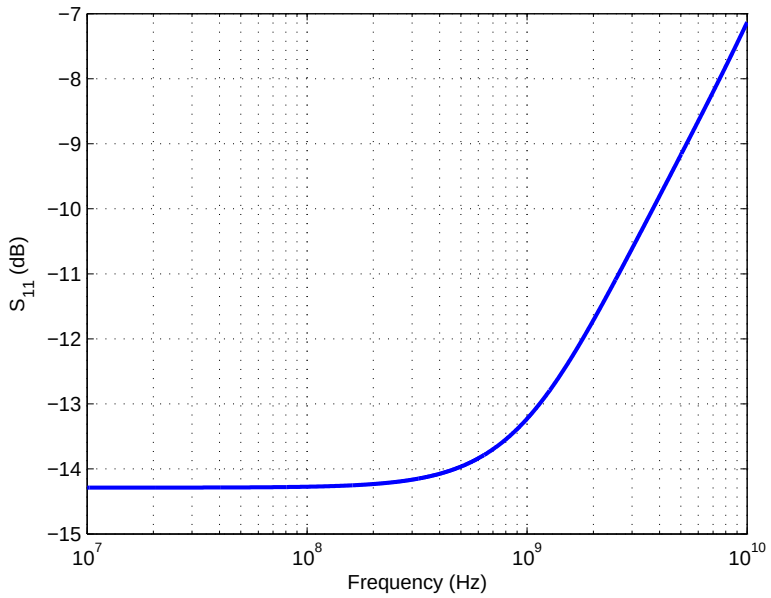


Figure 3.6: LNA S_{11} parameter

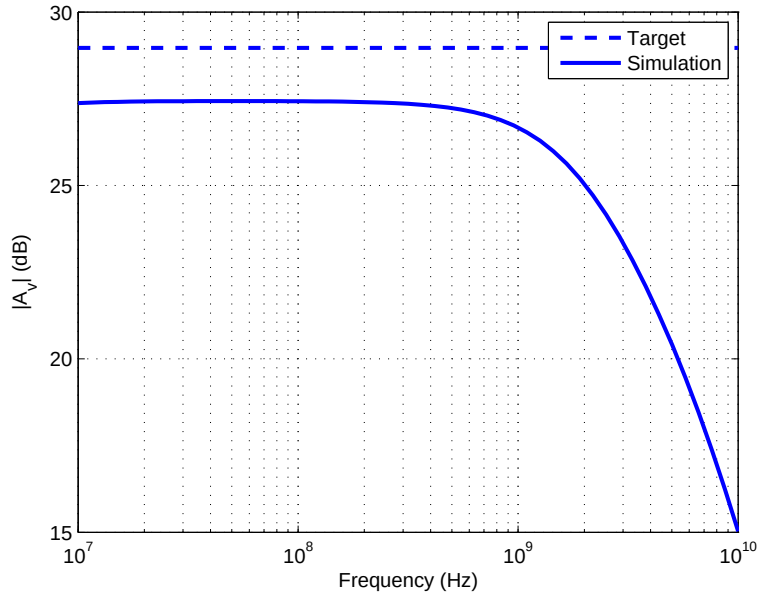


Figure 3.7: LNA voltage gain

Regarding the NF, shown in Figure 3.8, it is below 1.84 dB for the working band (300 MHz - 1 GHz), which is a very acceptable value for this kind of LNA. Below 300 MHz the NF is higher due to the effect of the flicker noise (explained in section 2.1.4.2) and the filter composed by C_F and R_F. For higher frequencies it starts to increase, mainly as consequence of the reduction of the voltage gain. For the theoretical expression (equation 3.37)) the noise excess factor (γ) was considered equal to one, due to the short channel effects of the transistors. The target (1.96 dB) and the obtained NF at the LNA working

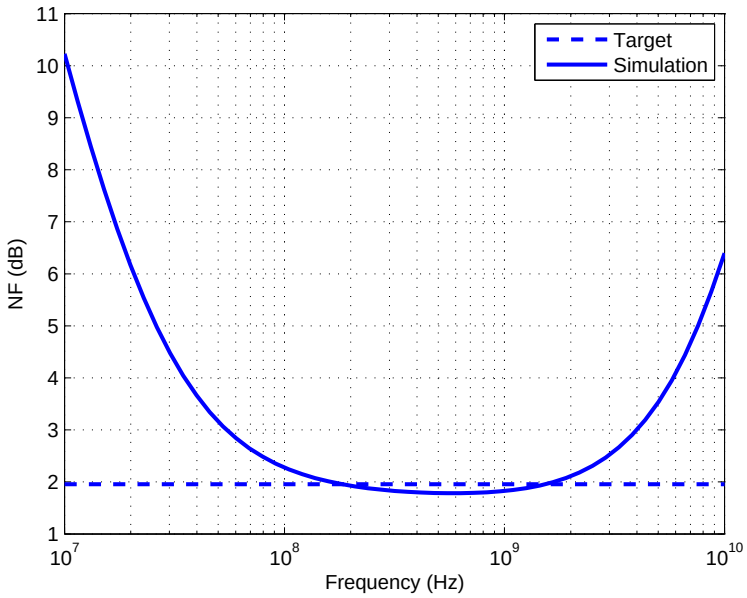


Figure 3.8: LNA noise figure

band are quite similar, which proves that the flicker noise is negligible at high frequencies, since it was not considered in the theoretical expression, and that all the approximations made in the theoretical analysis are valid. The higher NF obtained in the theoretical analysis, comparing with the simulation results, is explained by the use of PMOS devices as load resistors in the simulated circuit, that decreases the LNA noise contributions as mentioned before.

Concerning linearity, the LNA presents $IIP_2 = -2.3$ dBm (Figure 3.9) and $IIP_3 = -9.7$ dBm (Figure 3.10). To perform this simulation, two pure sinusoids were placed at the input of the LNA, spaced 20 MHz, $f_1 = 600$ MHz and $f_2 = 620$ MHz. As expected, due to the high voltage gain, IIP_2 and IIP_3 are below 0 dB. Also, the nonlinearities of the active loads, referred in section 3.1.4, contribute to the degradation of the LNA's linearity.

3.3 Circuit Implementation using CMOS 65 nm

This circuit was dimensioned considering the same aspects as the 130 nm circuit. The only difference is the input impedance of the cascode devices that was chosen to be approximately 100 Ω, which makes the circuit easier to dimension due to g_m constraints explained in the previous section. Also, it was chosen $V_{B,CG} = 560$ mV, $V_{B,CS} = 347$ mV and $V_{B,Casc} = 980$ mV. Obviously these values depend of the circuit characteristics and since the used technologies are different the bias voltages need to be different. To allow a direct comparison between the circuits of both technologies, the transistors length was decided to be 120 nm, as well as in the previous section.

Table 3.2 shows the transistors dimensions for the LNA developed in 65 nm and their DC operating points.

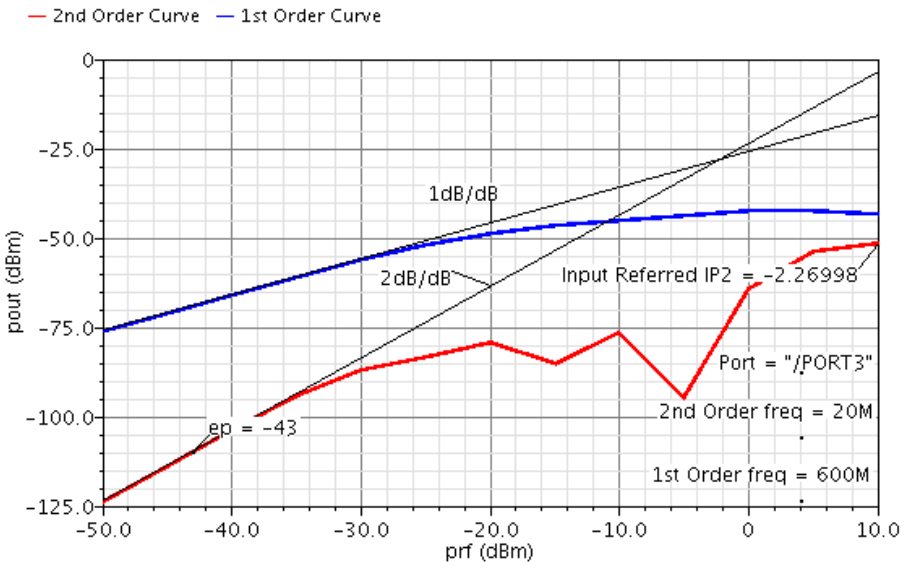


Figure 3.9: LNA IIP_2

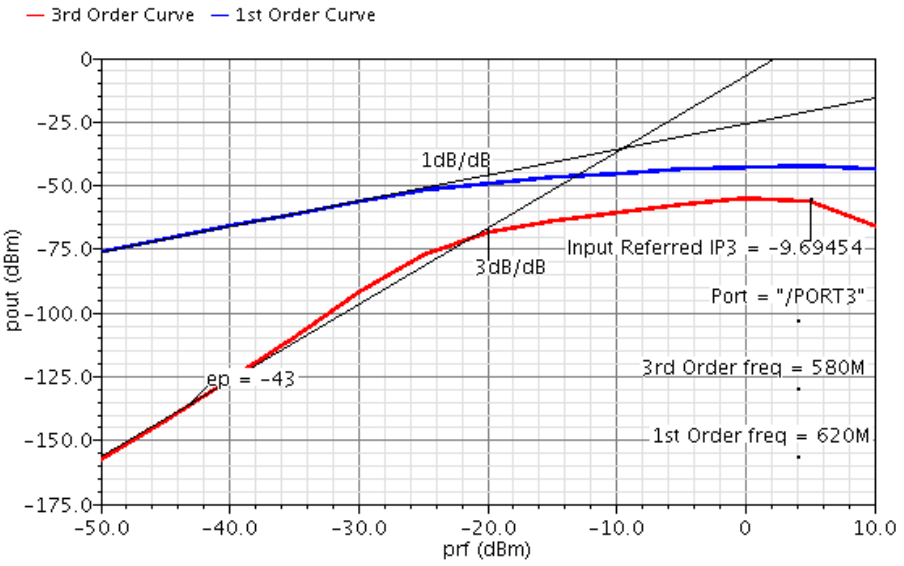


Figure 3.10: LNA IIP_3

Table 3.2: LNA parameters (CMOS 65 nm)

Transistor	W (μm)	L (μm)	Region	I_D (mA)	V_{DSsat} (V)	g_m (mS)
M_1	86	0.12	active	1.50	73.1	19.8
M_2	120	0.12	active	1.51	61.0	22.1
M_3	20	0.12	active	1.50	145.6	9.9
M_4	20	0.12	active	1.51	146.02	9.9
M_5	5.85	0.12	triode	1.50	-785.2	1.7
M_6	5.85	0.12	triode	1.51	-785.3	1.7

The analysis that was made in the previous section still valid to this circuit, since the LNA response and characteristics are the same. The obtained simulation results are referred in Table 3.3.

Table 3.3: LNA simulation results (CMOS 65 nm)

Freq. [GHz]	Volt. Gain [dB]	NF [dB]	S_{11} [dB]	IIP2 [dBm]	IIP3 [dBm]	Power [mW]	V_{DD} [V]	Tech. [nm]
0.3 - 1	$>$ 28.8	$<$ 4	$<$ -19	$>$ 145.3m	$>$ -14.4	$\approx$ 3.6	1.2	65

It was obtained a load resistance $R_L \approx 770\,\Omega$ and a bandwidth of approximately 4.5 GHz. The bandwidth increase, comparing with the 130 nm circuit, is related with the transistors switching frequency that is much higher for CMOS 65 nm technology due to the smaller parasitic effects and allowed channel lengths.

3.4 Discussion

The equations derived in section 3.1 are intended to help to dimension the circuit, but do not have into account the body effect of the CG transistor, the short-channel effects and the parasitic capacitances of the transistors, that have a some influence in the circuit functioning. For the specific case of the parasitic capacitances, that have an huge influence in the LNA bandwidth, they can be reduced by decreasing the transistors size, if a faster circuit is needed. For example, the largest capacitance of a MOSFET, C_{gs}, is approximately given by [15]

$$C_{gs} \cong \frac{2}{3} W L C_{ox}, \tag{3.41}$$

where C_{ox} is the gate capacitance per unit area. On the other end, to avoid short channel effects is necessary to increase the transistor's channel length, which reduce the maximum operating frequency since $f \propto 1/L^2$.

However, despite the differences between the theoretical and simulation results, due to the approximations that were made, the performance of the LNA is within the expected. A table with the LNA key parameters, for the circuits using both 130 nm and 65 nm CMOS technologies, is presented below.

Table 3.4: LNA simulation results

Tech. [nm]	Freq. [GHz]	Volt. Gain [dB]	NF [dB]	S_{11} [dB]	IIP_2 [dBm]	IIP_3 [dBm]	Power [mW]	V_{DD} [V]
130	0.3 - 1	$>$ 26.6	$<$ 1.84	$<$ -13.2	$>$ -2.3	$>$ -9.7	$\approx$ 3.6	1.2
65	0.3 - 1	$>$ 28.8	$<$ 4	$<$ -19	$>$ 145.3m	$>$ -14.4	$\approx$ 3.6	1.2

Since the 65 nm circuit's resistance R_L is higher, the voltage gain is higher, as verified. The obtained NF for the 65 nm is more than the double comparing with the 130 nm circuit. This discrepancy is related with the technology properties and the BSIM models that were used in the Cadence simulations, which are different for the two used technologies and need to be studied to understand this effect. Both circuits are matched to the antenna's impedance, as expected. Due to the higher gain, the IIP_3 of the 65 nm circuit is poorer than of the 130 nm circuit, as explained in 2.1.5.2. The low IIP_3 of this kind of LNA is related with the nonlinearities of the load devices and the circuit's high gain. Thus, is possible to conclude that both circuits can accomplish the desired function but the 130 nm circuit is much better in terms of NF and IIP_3, although its voltage gain and IIP_2 are slightly lower.

4

High-Q Bandpass Filter

In order to attenuate out-of-band interferers that can corrupt the signals at the receiver's AFE, specially by saturating the LNA, an integrated high-Q Bandpass Filter (BPF), based in [7–10], is employed in this work. As referred in section 2.5, this filter is based in a passive current-driven mixer (introduced in section 2.4.2), which has very interesting properties related with impedance transformation. For example, if the filter's baseband impedance is a low-Q LPF (e.g. a capacitor), the impedance at its input will be an high-Q BPF, as shown in Figure 4.1, centered in the LO frequency, ω_{LO}.

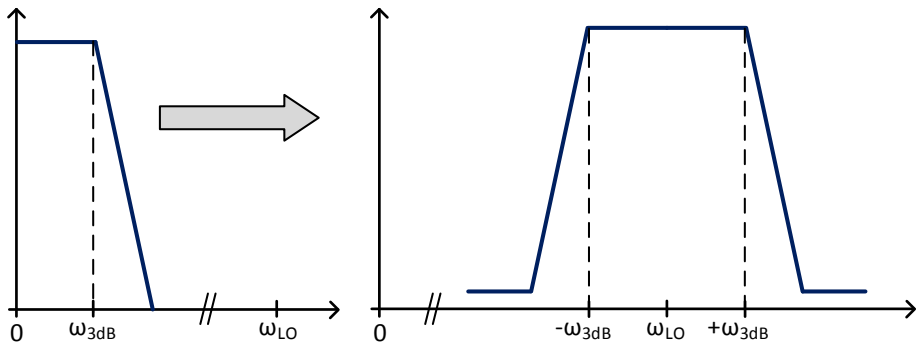


Figure 4.1: LPF to BPF transformation

Due to this characteristic, the resulting filter exhibits high impedance for the desired signal frequencies (near ω_{LO}) and offers a low impedance path to interferers that are located outside of the filter's cutoff frequency [29]. This behavior makes this kind of circuit ideal for wideband receivers were is desirable to have high-Q BPFs than can be precisely tuned

according to the input signal's frequency.

This chapter is structured as follows: a theoretical analysis of the filter is made and the main equations for its characterization are derived and validated by simulation.

4.1 Theoretical Analysis

The basic structure of the proposed High-Q BPF is shown in Figure 4.2a. This filter is driven by a LO that produces rail-to-rail non-overlapped square waves with a frequency equal to ω_{LO} and a duty cycle of $1/M$, as shown in Figure 4.2b, where M is the number of phases of the filter. The pulse width of each phase is equal to T_{LO}/M, where T_{LO} is the period of the clocks. This means that only one of the *M* switches is ON at a specific clock phase, i.e. the current that flows to one of the baseband impedances is equal to the RF current, if the corresponding switch is ON, or zero, if it is OFF. Usually, the impedance Z_{BB} is a capacitor (C_{BB}), as explained before. However, if higher bandwidth is required, a parallel *RC* should be used to have a lower droop in the filter response across the desired band [7].

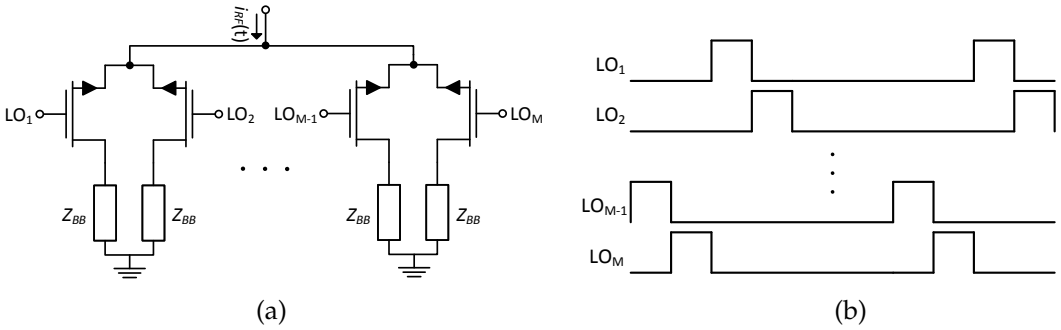


Figure 4.2: (a) Single-ended N-phase High-Q BPF. (b) LO waveforms for a N-phase filter

Assuming that all the switches are ideal, with an ON resistance equal to R_{SW}, the input impedance of the filter described in Figure 4.2 is given by [8]

$$\begin{aligned} Z_{in}(\omega) = R_{SW} &+ \frac{1}{M} Z_{BB}(\omega) + \frac{M}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) \times [Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})] \\ &+ \frac{M}{4\pi^2} \sin^2\left(\frac{2\pi}{M}\right) \times [Z_{BB}(\omega - 2\omega_{LO}) + Z_{BB}(\omega + 2\omega_{LO})] \\ &+ \frac{M}{9\pi^2} \sin^2\left(\frac{3\pi}{M}\right) \times [Z_{BB}(\omega - 3\omega_{LO}) + Z_{BB}(\omega + 3\omega_{LO})] + \dots \end{aligned} \tag{4.1}$$

From the previous equation is possible to conclude that the input impedance is a translation of Z_{BB} to the integer harmonics of the LO, with a scaling factor that is inverse to *M*, as shown in Figure 4.3.

To simplify the filter analysis, and since the desired signals are located near ω_{LO}, the

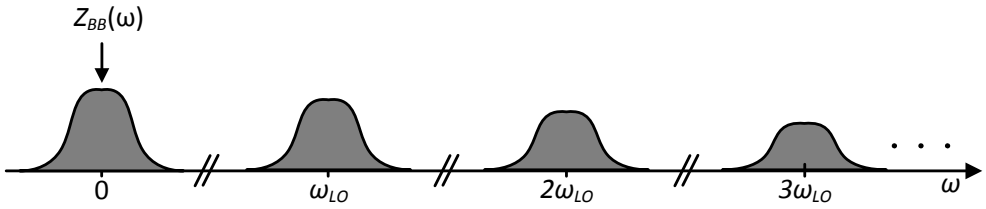


Figure 4.3: Single-ended M-phase high-Q BPF input impedance spectrum

DC and high order terms can be ignored, leading to

$$Z_{in}(\omega) \cong R_{SW} + \frac{M}{\pi^2}\sin^2\left(\frac{\pi}{M}\right) \times \left[Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})\right]. \tag{4.2}$$

Given this approximation, the filter's input impedance is approximately equal to the baseband impedance Z_{BB} shifted to the LO frequency, in series with the switch resistance R_{SW}, resulting in a tunable BPF that is precisely controlled by the LO frequency, as desired. This allows the implementation of this type of filters in wideband receivers, where the frequency of interest can vary significantly. As explained before, (4.2) shows that the low-Q baseband impedance is transferred to a high-Q RF impedance. This means that if Z_{BB} exhibits a very high impedance at DC (e.g. the impedance of a capacitor is infinite at DC) the filter's impedance will be ideally infinite at ω_{LO} and for frequencies far from the frequency of interest the filter's impedance will be equal to R_{SW}, because Z_{BB} diminishes.

Regarding the number of phases, a higher M increases the filter in-band impedance, decreases the folding components gain and moves the closest folding frequency component to $(M-1)\omega_{LO}$, avoiding the folding of interferers situated in some harmonics of ω_{LO} on top of the desired signal [8]. This means that to avoid image related problems $M \geq 4$, otherwise the closest folding frequency will be located at ω_{LO}. The main disadvantages of using an high M are the increase of the number of necessary switches, that results in a larger Bill of Materials (BOM) and consequently increases the filter noise contributions, and the complexity of the LO.

Since the switches are implemented with MOSFETs, operating in deep triode region ($V_{DS} \approx 0$), the channel region behaves like a voltage controlled resistor R_{SW} that, for a NMOS device, is given by [15]

$$R_{SW} \approx r_{ds} = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1}_{|V_{DS}=0} = \frac{1}{\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)} \tag{4.3}$$

For a constant transistor length (L), by increasing the transistor width (W) is possible to decrease the resistance R_{SW} and consequently the impedance $Z_{in}(\omega)$ also decreases for frequencies distant from ω_{LO} (at ω_{LO} the effect of R_{SW} is neglected because the filter's impedance is very high), as expressed in (4.2). Since the filter's out-of-band impedance is equal to R_{SW}, this resistance should be very low in order to obtain the maximum interferers attenuation. However, from (2.20) is possible to conclude that if R_{SW} is decreased

the thermal noise current generated by the filter increases, leading to an higher filter's noise contribution. The main advantage of operating at the deep triode region is that due to this region properties the resulting filter is very linear.

4.1.1 Single-ended Version

A 4-phase single-ended high-Q BPF, identical to the presented in Figure 4.2, is proposed to be employed at the input of the LNA studied in chapter 3. This circuit was designed to filter the input signal, attenuating undesired signals located outside of the interest band, and to contribute to the LNA input impedance matching.

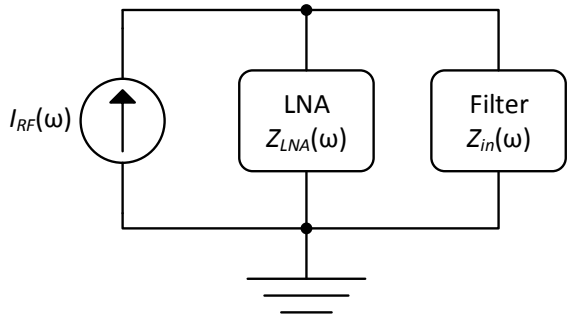


Figure 4.4: Equivalent circuit of LNA input connected to the proposed high-Q BPF

Consider that the LNA has an equivalent input impedance $Z_{LNA}(\omega)$ and is in parallel with the proposed filter, as shown in Figure 4.4. If a current $I_{RF}(\omega)$ is flowing into the circuit (Norton equivalent) the ratio between the RF voltage and the RF current is given as

$$\frac{V_{RF}(\omega)}{I_{RF}(\omega)} = Z_{LNA}(\omega) \parallel Z_{in}(\omega). \tag{4.4}$$

Substituting $Z_{in}(\omega)$ by (4.2), and for a number of phases M,

$$\frac{V_{RF}(\omega)}{I_{RF}(\omega)} \cong Z_{LNA}(\omega) \parallel \left(R_{SW} + \frac{M}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) \times [Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})] \right). \tag{4.5}$$

This means that for frequencies near ω_{LO} the equivalent node impedance is approximately equal to $Z_{LNA}(\omega)$, because the filter impedance is very high (ideally is infinite) as explained before, and the filter will not have much impact on the desired RF signal. For frequencies far from w_{LO} the node impedance is $Z_{LNA}(\omega) \parallel R_{SW}$, which is approximately equal to R_{SW} considering that $R_{SW} \ll Z_{LNA}(\omega)$. This small impedance attenuates undesired out-of-band interferers.

Considering a particular case where $Z_{LNA}(\omega)$ is a resistor R_{LNA} and the filter's base-band impedances are capacitors C_{BB}, (4.5) can be written as [8]

$$\frac{V_{RF}(\omega)}{I_{RF}(\omega)} \cong \frac{R_{LNA}}{R_{LNA}+R_{SW}} \times \left[R_{SW} + \frac{\frac{M^2}{\pi^2}\sin^2\left(\frac{\pi}{M}\right) R_{LNA}}{1+jM(R_{LNA}+R_{SW})C_{BB}(\omega-\omega_{LO})} \right]. \quad (4.6)$$

Analyzing (4.6) is possible to verify that the resulting filter consists in a BPF with the equivalent LPF bandwidth given by

$$\omega_{3dB} \cong \frac{1}{M(R_{LNA}+R_{SW})C_{BB}}. \quad (4.7)$$

Considering that the filter is symmetric, as shown in Figure 4.1, its bandwidth is equal to $2 \cdot \omega_{3dB}$ and the Q factor is $Q = \omega_{LO}/(2 \cdot \omega_{3dB})$, as referred in section 2.5. By increasing M is possible to decrease the bandwidth and increase the filter sharpness (Q) by M times. The bandwidth also depends of the LNA input impedance and the filter's switches resistance.

For the specific case of $M = 4$, that corresponds to the filter used in this work, and considering that $R_{LNA} \gg R_{SW}$, the transfer function at ω_{LO} is

$$\frac{V_{RF}(\omega_{LO})}{I_{RF}(\omega_{LO})} \cong \frac{R_{LNA}\left(R_{SW}+\frac{8}{\pi^2}R_{LNA}\right)}{R_{LNA}+R_{SW}} \approx \frac{8}{\pi^2}R_{LNA}. \quad (4.8)$$

This means that, comparing with the LNA circuit without the BPF, the circuit gain drops by $8/\pi^2 = -1.82$ dB at ω_{LO}. This reduction of the gain is due to the higher harmonics effect [7], referred in (4.4), that were ignored during the filter analysis and makes the impedance seen from the filter finite, contrarily to the expected. If M takes a larger value, the circuit input impedance is higher, as stated in (4.6), which means that for higher M the effect of high order harmonics is less noticeable. For frequencies far from ω_{LO} the transfer function is equal to $R_{LNA} \parallel R_{SW}$, as shown before, which means that the maximum out-of-band attenuation depends of R_{SW}. To achieve the filter maximum performance R_{SW} should be close to zero and R_{LNA} should be much larger than R_{SW}, to achieve the maximum gain at ω_{LO}, as stated in (4.8).

4.1.2 Differential Version

For the differential nodes of the LNA, a differential version of the high-Q BPF, shown in Figure 4.5, should be employed. This filter has the same functioning as the single-ended version but, since is differential, presents the double of the input impedance. Also, since the number of necessary switches is doubled, the filter noise contributions increases substantially.

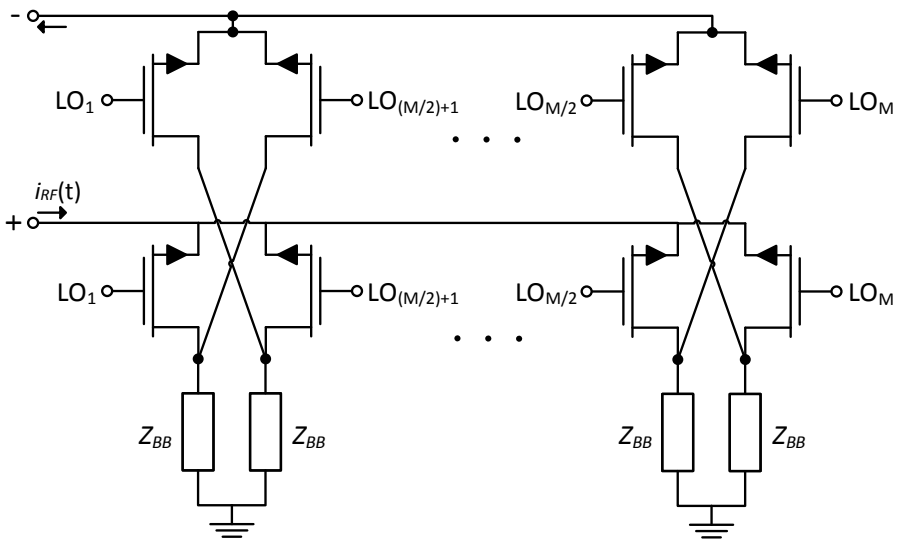


Figure 4.5: Differential N-phase High-Q BPF

The input impedance of the differential filter is given by [8]

$$\begin{aligned} Z_{in}(\omega) = 2R_{SW} &+ \frac{2M}{\pi^2}\sin^2\left(\frac{\pi}{M}\right) \times [Z_{BB}(\omega-\omega_{LO}) + Z_{BB}(\omega+\omega_{LO})] \\ &+ \frac{2M}{9\pi^2}\sin^2\left(\frac{3\pi}{M}\right) \times [Z_{BB}(\omega-3\omega_{LO}) + Z_{BB}(\omega+3\omega_{LO})] \\ &+ \frac{2M}{25\pi^2}\sin^2\left(\frac{5\pi}{M}\right) \times [Z_{BB}(\omega-5\omega_{LO}) + Z_{BB}(\omega+5\omega_{LO})] + \dots \end{aligned} \tag{4.9}$$

which means that the differential filter cancels all the even harmonics (including DC), so the impedance around these harmonics is approximately zero (assuming $R_{SW} \approx 0$). The input impedance spectrum is shown in Figure 4.6.

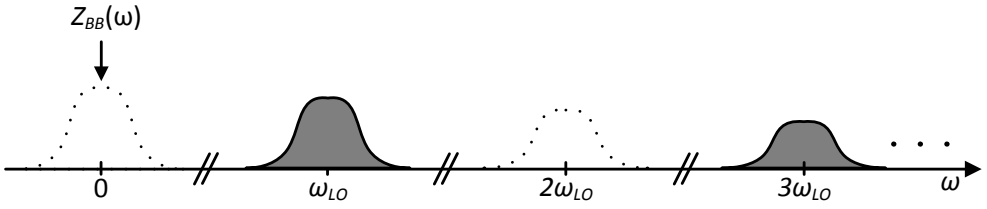


Figure 4.6: Differential M-phase high-Q BPF input impedance spectrum

An interesting property of this filter is the fact that the baseband impedances $Z_{BB}(\omega)$ of two phases separated by 180º can be replaced by a floating impedance of size $2Z_{BB}(\omega)$, as shown in Figure 4.7. This is very useful, specially if the baseband impedances are capacitors (C_{BB}) because two capacitors can be replaced by a capacitor of size $C_{BB}/2$, which results in a reduction of the capacitors area by four times [8].

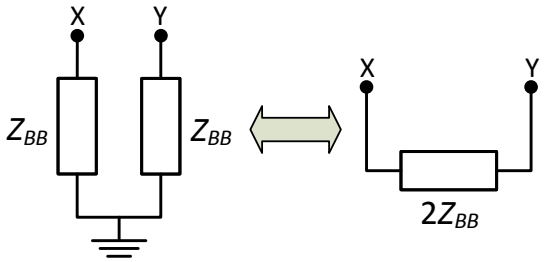


Figure 4.7: Differential N-phase High-Q BPF with floating impedances

4.2 Circuit Implementation

To verify if the filter has the expected response, a setup circuit with the following parameters was employed: $R_{LNA} = 100\,\Omega$, $R_{SW} = 10\,\Omega$, $C_{BB} = 50$ pF, $M = 4$ and $f_{LO} = 600$ MHz. The simulation was made through PSS (with the LOs fundamental tones and no output harmonics) and PAC analysis, with a DC current source (with PAC magnitude equals to one) connected to the filter's input. The LOs produce the waveforms[1] shown in Fig. 4.2b, with 1.2 Vpp, an offset of 600 mV and rise and fall times of 10 ps. The employed technology is CMOS 130 nm. Figure 4.8 shows the obtained results of the single-ended version of the filter, as well as the expected response, derived in section 4.1.

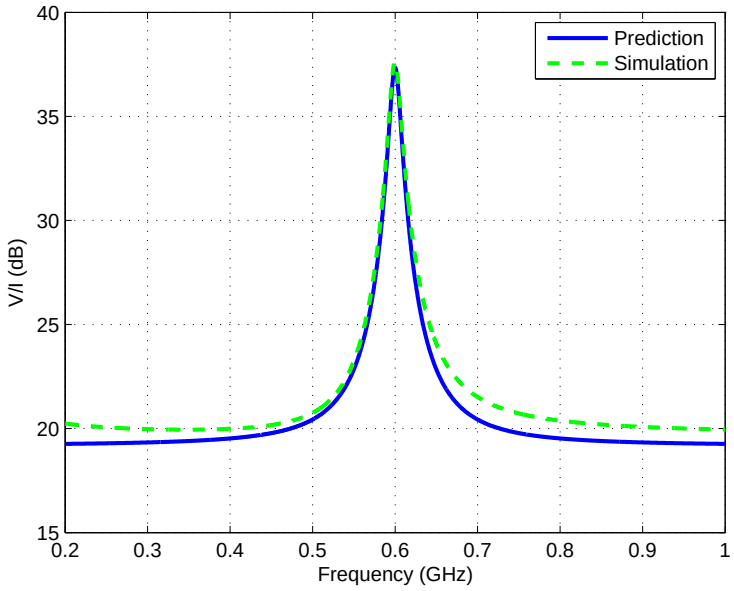


Figure 4.8: Prediction of (4.6) *vs.* simulation results for single-ended BPF

As shown in Table 4.1, the obtained results are within the expected. The differences of the simulated and expected results are mainly due to the approximations that were made in (4.6). If an higher number of phases (M) is used, the simulated and expected results become more identical because, as referred before, for higher M the effect of the

[1] All of the LO waveforms used in this work are equal to this one, except for the f_{LO} parameter.

other harmonics (including DC) is less noticeable.

Table 4.1: Single-ended high-Q BPF results

	Bandwidth [MHz]	Q	Z_{in} @ f_{LO} [Ω]	Z_{in} [Ω][a]
Prediction	14.5	41.4	82.8	9.1
Simulation	16.1	37.3	75.9	10

[a] out-of-band

From this simulation is possible to conclude that the filter exhibits high Q factor values that are very difficult to achieve using traditional external filters, as stated in section 2.5.

In order to understand the behavior of the studied topologies a simulation was made with the previous setup, but with $f_{LO} = 300$ MHz (Figures 4.9 and 4.10). As expected, the single-ended filter input impedance is similar to the presented in Figure 4.8 and the differential filter input impedance is approximately the double of the single-ended version, as referred in (4.9). Also, the bandwidth of the differential filter is the double of the single-ended for the same input circuit, which means that the differential filter has a lower Q factor.

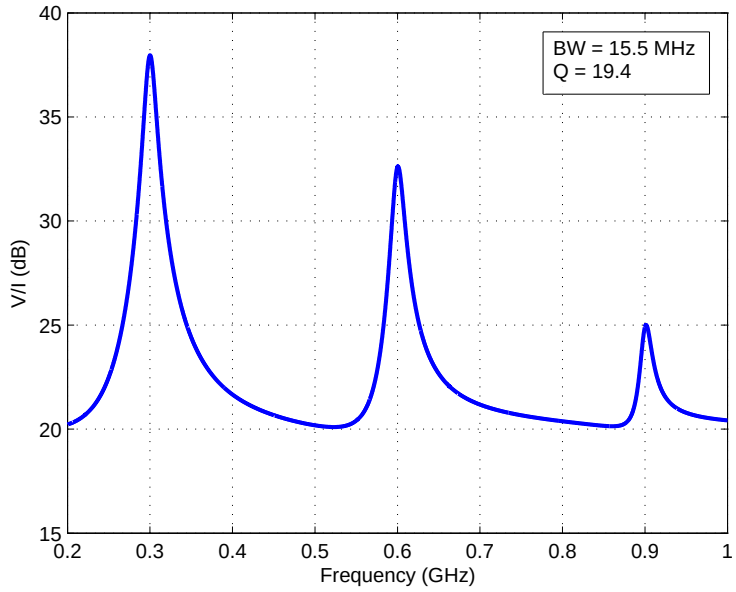


Figure 4.9: Single-ended BPF response with $f_{LO} = 300$ MHz

As shown in Figure 4.10, the differential filter cancels the even order harmonics, as referred in section 4.1.2, leading to a lower degradation of the signal at the desired frequency component (f_{LO}), that occurs due to the high order harmonics effects.

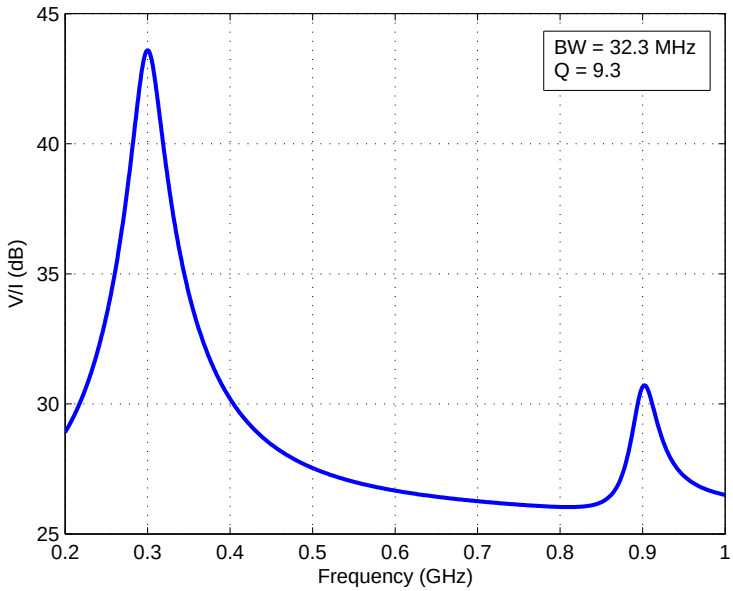


Figure 4.10: Differential BPF response with $f_{LO} = 300$ MHz

4.3 Discussion

The presented high-Q BPF is a very good solution to employ in an integrated RF receiver due to its circuit's simplicity and reduced number of active devices. This circuit performs the conversion from a low-Q LPF to an high-Q BPF that is precisely controlled by the LO waveform, with a minimum penalty in the overall circuit voltage gain. This allows to filter the undesired interferers located at out-of-band frequencies, avoiding the use of external filters that requires an external chip that occupies more area and is more expensive. Since it is passive, this filter has almost no power consumption and flicker noise, leading to very low noise contributions to the receiver.

For single-ended nodes of the receiver, a single-ended version of the filter should be used, and for differential nodes there is the need to employ a differential filter. The main advantages of the differential filter are the full cancellation of the even order harmonics and the double input impedance, comparing with the single-ended version. However, since this circuit has more active devices for the same number of phases, its complexity and noise contributions are higher and the Q factor is lower, for the same circuit characteristics.

Regarding the number of phases, increasing M increases the filter in-band impedance, decreases the folding components gain, moves the closes folding frequency component to $(M-1)\omega_{LO}$ and increases the number of filter's active devices (increasing the filter noise contributions) and the LO complexity. In this work is used $M = 4$, which is the best compromise between the circuit overall performance and complexity.

5

Complete Receiver

As mentioned before, a RF receiver performs the conversion of a RF input signal to a signal, with lower frequency, that can be handled by an ADC and thereafter be processed by a digital circuit. This work consists in the receiver indicated in Figure 5.1. A low-IF receiver was chosen for this work due to its simplicity and the possibility to allow its full integration in the same chip, as explained in section 2.2.3. The studied circuit only represents one branch of the receiver. To avoid image related problems two identical branches, which operate in quadrature, are required.

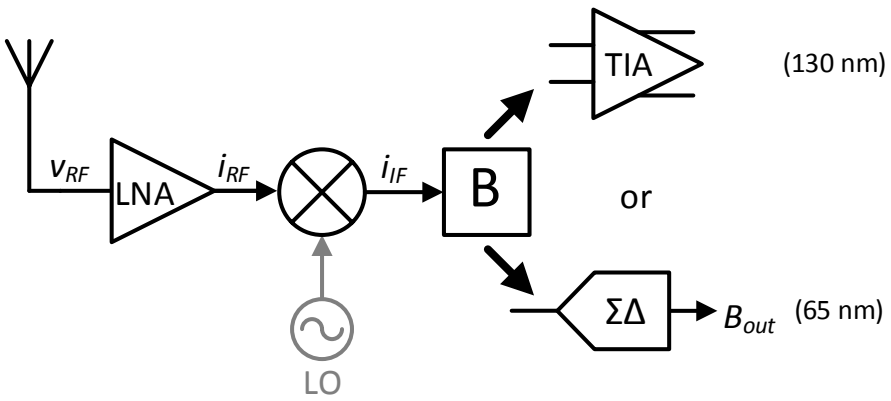


Figure 5.1: Complete receiver

The receiver consists in a LNA, with integrated filtering, that amplifies the input signal, a current-driven mixer that converts the RF signal to a baseband signal, a end block (B) and a LO that was not studied in this work. The end block can be either a TIA (studied in section 5.3), that converts the current IF signal to a voltage signal, or a $\Sigma\Delta$ modulator (studied in section 5.5), that directly converts the current IF signal to the digital domain,

as shown in Figure 5.1. The receiver that uses the TIA was developed in CMOS 130 nm technology and produces a baseband voltage that is proportional to the RF signal that enters in the LNA. The 65 nm receiver has the same characteristics of the 130 nm circuit but instead of a TIA it uses a current-mode $\Sigma\Delta$. Also, it uses a current buffer to perform the interface between the mixer's output and the $\Sigma\Delta$ input, as will be explained in section 5.4.

This chapter is structured as follows: first, the block composed by the LNA studied in Chapter 3 and the high-Q BPF studied in chapter 4 is analyzed and validated through simulation and both technologies are compared. Then, the mixer and the TIA are reviewed and the complete receiver, composed by those three blocks, is studied. Finally, the current-buffer that performs the interface between the mixer and the $\Sigma\Delta$ is reviewed and the complete receiver using the $\Sigma\Delta$ modulator is analyzed.

5.1 Balun-LNA with Integrated Filtering

One of the biggest concerns in modern RF receivers is the attenuation of undesired interferers that can corrupt the RF signal and saturate the LNA. To overcome this problem, two high-Q BPF were integrated in the studied LNA circuit, as shown in Figure 5.2.

The input filter consists in a single-ended high-Q BPF (studied in section 4.1.1), that also contributes to impedance matching. The filter at the input of the cascode stages is a differential high-Q BPF (studied in section 4.1.2). Both filters have four phases ($M = 4$).

As explained before, this block was developed in 130 nm and 65 nm CMOS technologies. In the next sections both circuits will be presented, analyzed and compared.

5.1.1 LNA With Integrated Filtering using CMOS 130 nm

For this specific circuit both filters were designed in order to the complete block have a bandwidth of approximately 6 MHz. The filters' component values are described in Table 5.1.

Table 5.1: Filters' component values (CMOS 130 nm)

Filter	W (μm)	L (μm)	R_{SW} (Ω)	C_{BB} (pF)
Single-ended	16	0.12	28.6	200
Differential	8	0.12	74	55

W and L are the switches dimensions, R_{SW} is the switches ON resistance and C_{BB} is the baseband capacitances value. The filters' behavior is very influenced by the transistors dimensions, as explained in chapter 4. For example, if the switches resistance is large, the filter noise contributions will be small but the filter's effect is less noticeable (less amplification at ω_{LO} and less attenuation of undesired signals), comparing with a lower value of R_{SW}. The chosen L is 120 nm, which is the minimum size allowed by the technology. Since the transistors operate as switches (triode region), the short channel effects are

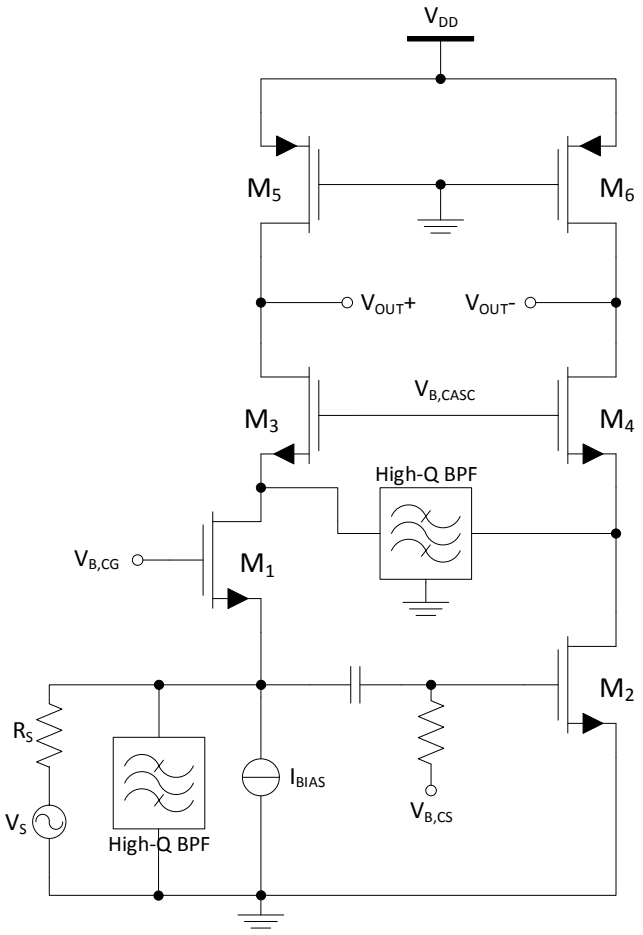


Figure 5.2: Cascode balun-LNA with integrated filters

negligible and this size allows the devices to operate at the maximum speed, because the maximum operating frequency is inverse to L^2.

5.1.1.1 LNA Response Analysis

By integrating the both filters in the LNA nodes is expected a frequency response similar to the shown in Figure 4.8. Figure 5.3 shows the LNA voltage gain for three different LO frequencies: 300 MHz, 600 MHz and 900 MHz. Due to the filters' properties, explained before, at frequencies near f_{LO} the input signal flows almost completely through the LNA transistors, since the filters' input impedance is very large. For frequencies far from f_{LO} the filters' impedance is much lower than the impedance of the LNA nodes, and consequently the signal flows almost completely through the filters, resulting in less amplification of the undesired interferers.

From this simulation is possible to conclude that the LNA behaves like a BPF with an high Q factor, since it has a low bandwidth and is centered in a high frequency. The obtained bandwidths and Q factors are presented in Table 5.2.

As desired, the bandwidth is approximately 6 MHz for the entire LNA working band.

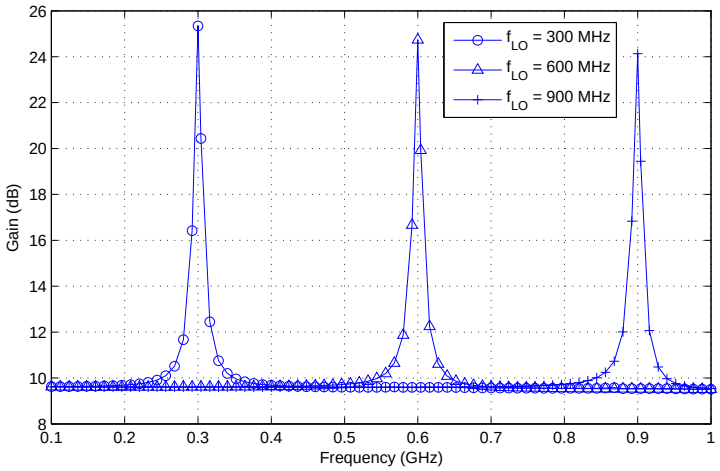


Figure 5.3: LNA voltage gain, for multiple values of f_{LO}, with both filters (CMOS 130nm)

Table 5.2: Filtered LNA bandwidths and Q factors (CMOS 130 nm)

f_{LO} (MHz)	300	600	900
Bandwidth (MHz)	5.7	6.1	6.6
Q	52.6	98.4	136.4

The variation of this value along the frequency is mainly due to the parasitic capacitances that are frequency dependent and affect the circuit bandwidth. Regarding the Q factor, it grows almost linearly with the frequency and presents high values, as expected. Since out-of-band signals are corrupted by the filters, the NF at those frequencies is very high, as shown in Figure 5.4.

The S_{11} parameter has the same shape of NF because for out-of-band frequencies the filters' impedance is very low (approximately R_{SW}), and since the filters are in parallel with the LNA nodes, the equivalent input impedance is very low, resulting in a poor input matching and consequently an high S_{11}.

By using this technique is possible to employ a narrowband widely tunable balun-LNA, which means that the resulting circuit is a narrowband balun-LNA (with a bandwidth of about 6 MHz) that can be tuned to operate over the entire working band of the LNA of chapter 3 (0.3 – 1 GHz), by programming the LO waveform, according to the RF input signal frequency.

5.1.1.2 LNA Frequency Sweep

In order to understand the effect of the filters in the LNA response, it was made a frequency sweep, for the entire LNA working band, to analyze the different parameters – voltage gain, NF, S_{11}, IIP_2 and IIP_3. This frequency sweep was performed in three different configurations: using only the input filter, using only the cascode filter and using both filters.

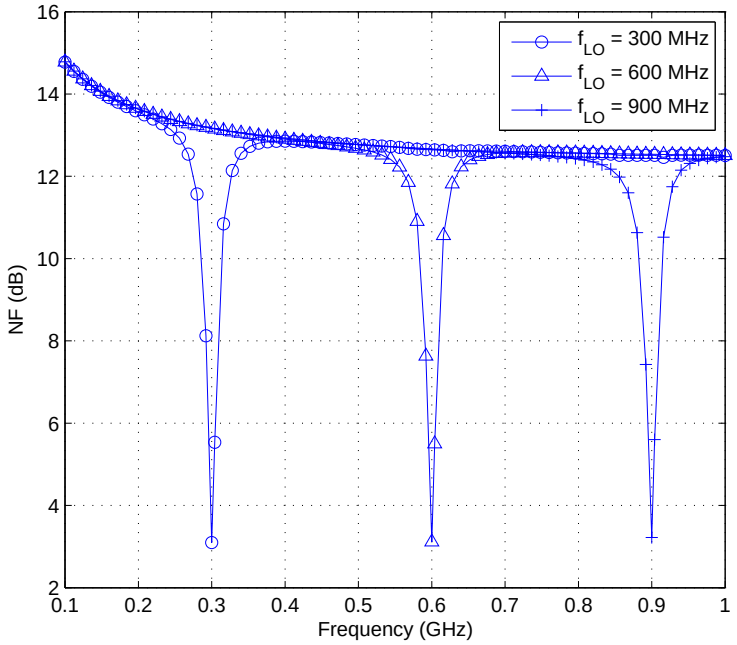


Figure 5.4: LNA noise figure, for multiple values of f_{LO}, with both filters

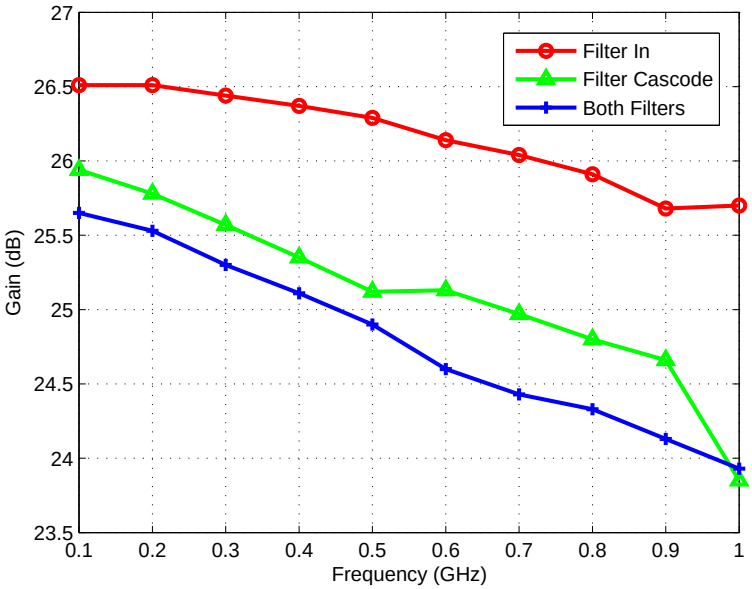


Figure 5.5: LNA voltage gain at f_{LO}

Comparing the voltage gain at f_{LO} (Figure 5.5) with the voltage gain of the LNA only (referred in Table 3.4) is possible to conclude that when both filters are used the gain drop is about 3 dB in the worst case. This reduction of gain is related with the filter properties described in section 4.1.1, i.e., due to the harmonics effect the filters' impedance is not infinite at f_{LO}, as desired, and consequently the signal of interest does not flow completely

through the LNA. Also, (4.8) despises R_{SW} that obviously has an influence in the circuit voltage gain at this frequency. As expected, the voltage gain decreases with the increase of the number of filters. A solution to overcome this problem is to increase the number of phases of the filters, as explained before.

Table 5.3: LNA out-of-band voltage gain

	Filter Input	Filter Cascode	Both Filters
Voltage gain [dB]	21.5	14.7	9.6

The out-of-band voltage gain (Table 5.3) is approximately 10 dB when both filters are used, for the entire LNA working band, which means that the undesired signals suffer an attenuation of approximately 14 dB, comparing with the signals at the desired frequencies. One interesting property is the fact that by increasing the number of the filters the out-of-band gain suffers a huge reduction while the gain at f_{LO} is only slightly reduced. This means that if is desired an higher interferers attenuation more filters can be integrated in the receiver's circuit, with a minor penalty in the voltage gain at the desired frequencies.

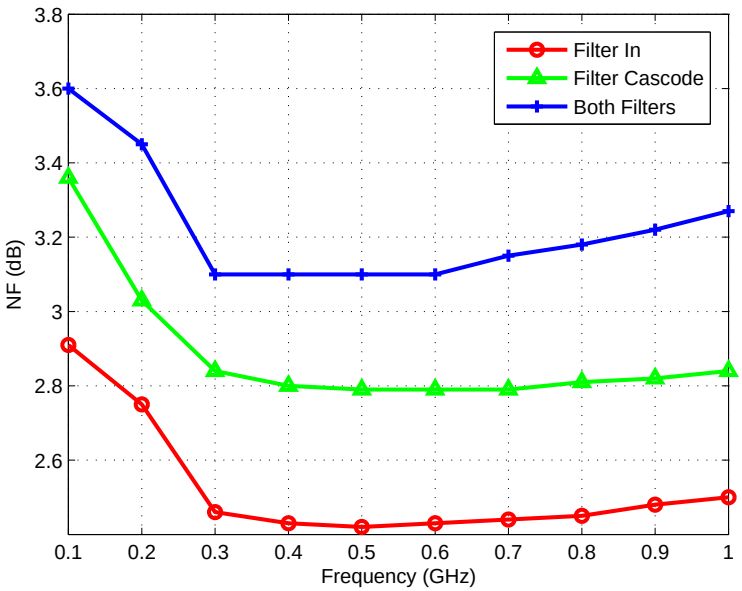


Figure 5.6: LNA NF at f_{LO}

Regarding the NF (Figure 5.6), it is approximately 1.5 dB higher than the LNA only (Table 3.4), when both filters are used, and has the same shape of Figure 3.8, due to the reasons that were explained before. As stated in section 4.1, by increasing the number of filters the NF also increases, due to the filters noise contributions. Also, the differential filter contributes with more noise than the single-ended filter due to the higher number of devices. The lower voltage gain (relatively to the LNA only) also increases the NF, as stated in 2.23.

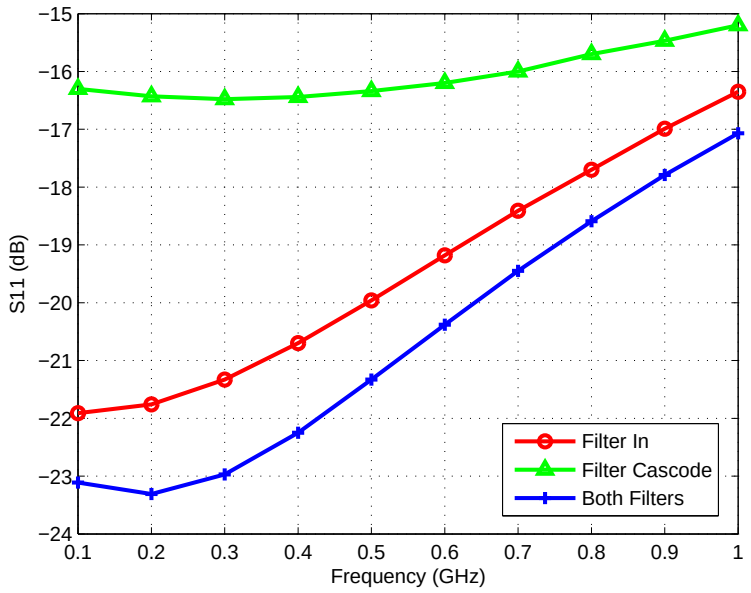


Figure 5.7: LNA S_{11} at f_{LO}

Concerning the input impedance matching, Figure 5.7 shows that the LNA is matched to the antenna's impedance for the entire working band, in the three configurations. When both filters are used is possible to obtain $S_{11} < -17$ dB (that is 4 dB lower than the LNA only). As shown in Figure 5.7, the input filter improves significantly the impedance matching, as referred before, because it is in parallel with the LNA input. Thus, this filter's component values are limited to certain values because its impedance has an huge impact in the LNA input impedance.

Since the most filtering effect is achieved when both filters are used, the IIP_2 and IIP_3 analysis were performed for the LNA with both filter integrated. In order to understand the influence of the filters in the even-order distortion and intermodulation problems, two pure sinusoids were placed at the input of the LNA, one at f_{LO} and another at f_{LO} + 20 MHz. It is important to note that the LNA bandwidth is approximately 6 MHz.

As shown in Figure 5.8, it were obtained $IIP_2 > +22$ dBm and $IIP_3 > -4$ dBm, significantly better comparing with the values of the LNA only (Table 3.4). These values are very acceptable for a wide number of applications like Global System for Mobile Communications (GSM) and DVB-H [30]. The decrease of these parameters' values with the frequency is mainly due to the LNA non-linearities that are most evident for higher frequencies and to the increase of the bandwidth, as stated in Table 5.2, that reduces the filter sharpness and allow closer interferers to corrupt the desired signal.

5.1.2 LNA With Integrated Filtering using CMOS 65 nm

Since the technology used in the circuit of this subsection is different from the previous one, the component values need to be dimensioned again in order to achieve the desired

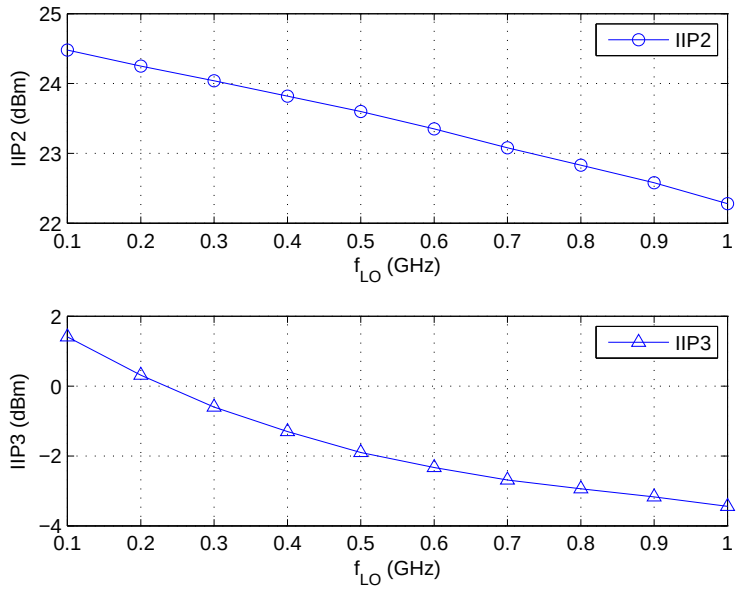


Figure 5.8: LNA IIP_2 and IIP_3

performance and characteristics. However, the analysis that was made in the previous subsection is valid for this one, since the circuit is the same.

Regarding the bandwidth, it was desired a value of approximately 4.5 MHz for the LNA with integrated filtering, which leads to the filters' components values presented in Table 5.4.

Table 5.4: Filters component values (CMOS 65 nm)

Filter	W (μm)	L (μm)	R_{SW} (Ω)	C_{BB} (pF)
Single-ended	10	0.06	32.7	400
Differential	5	0.06	83.4	95

The chosen length (L) is 60 nm, which is the minimum size allowed by the technology. In order to verify the circuit's behavior, it was made a simulation identical to the presented in Figure 5.3. The results are shown in Figure 5.9.

As expected, the circuit has the same behavior as the one analyzed in the previous subsection. As referred in section 3.4, the voltage gain of the 65 nm circuit is higher than the 130 nm circuit. Also, interferers suffer a lower attenuation, about 12 dB (comparing with 14 dB), because the switches impedances (R_{SW}) of this circuit are higher, and from (4.6) it is known that the out-of-band impedance of the studied high-Q BPF is given by $R_{LNA} \parallel R_{SW}$. Table 5.5 presents the obtained bandwidth and Q factor.

The variation of the bandwidth is related with the parasitic effects explained before. Since this circuit has a bandwidth lower than the 130 nm version, the resulting Q factor is higher, which means that the CMOS 65 nm narrowband balun-LNA is more selective and can attenuate blockers that are located closer to f_{LO}. Obviously, this property

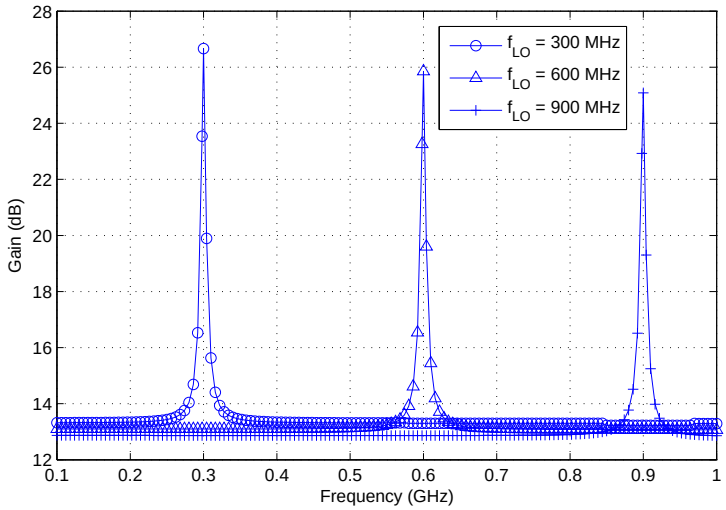


Figure 5.9: LNA voltage gain, for multiple values of f_{LO}, with both filters (CMOS 65 nm)

Table 5.5: Filtered LNA bandwidth and Q factor (CMOS 65 nm)

f_{LO} (MHz)	300	600	900
Bandwidth (MHz)	3.8	4.5	4.7
Q	79	133.3	191.5

depends entirely of the filters component values and the LNA nodes impedances, and are unrelated with the used technology. In order to obtain the LNA response parameters, simulations identical to the presented in section 5.1.1.2 were made. The results are shown in Table 5.6.

Table 5.6: Narrowband balun-LNA simulation results (CMOS 65 nm)

Freq. [GHz]	V. Gain [dB]	Atten.[a] [dB]	NF [dB]	S_{11} [dB]	IIP2 [dBm]	IIP3 [dBm]	Power [mW]	V_{DD} [V]
0.3 - 1	> 24.8 [b]	> 12	< 6.3 [b]	$<$ -17 [b]	> 20.2	$>$ -1.3	≈ 3.6	1.2

[a] Out-of-band attenuation
[b] At f_{LO}

Comparing this values with the obtained for the LNA only (Table 3.3) is possible to verify that the voltage gain suffers a drop of about 4 dB in the worst case, the circuit's NF increases approximately 2 dB and IIP_2 and IIP_3 parameters are much better, due to the introduced filtering. This difference in the circuit parameters is mainly due to the filters' characteristics. As with the 130 nm circuit, the filters can be dimensioned according to the system requirements.

5.1.3 LNAs Comparison

Table 5.7 shows a comparison of the LNAs with both filters integrated, for CMOS 130 nm and CMOS 65 nm technologies.

Table 5.7: Filtered LNAs comparison

Tech. [nm]	V. Gain[a] [dB]	Atten.[b] [dB]	NF[a] [dB]	S_{11}[a] [dB]	IIP2 [dBm]	IIP3 [dBm]
130	> 23.8	> 14	< 3.3	$<$ -17	> 22	$>$ -4
65	> 24.8	> 12	< 6.3	$<$ -17	> 20.2	$>$ -1.3

[a] At f_{LO}
[b] Out-of-band attenuation

The operating frequency (0.3 – 1 GHz), $V_{DD} = 1.2$ V and power consumption (3.6 mW) are the same for both circuits. Analyzing Table 5.7 is possible to conclude that both LNAs are identical. The 65 nm LNA has better voltage gain and a larger working band (this property was not studied in this work since both circuits were design to operate at the same frequencies), as explained in section 3.3. However, the NF of the 65 nm is practically the double of the 130 nm, due to the reasons explained in section 3.4 that need to be analyzed in a future work. Thus, and although both circuits can achieve the desired function, the 130 nm circuit proved to be the best solution to employ in an integrated RF receiver, only because of the obtained NF. By using this technique is possible to attenuate out-of-band interferers at least 14 dB (comparing with the signals at f_{LO}), avoiding the use of external filters, with a minimum penalty in NF (about 1.5 dB in the worst case) and in voltage gain (about 3 dB in the worst case), comparing with the LNA of chapter 3. The IIP_2 and IIP_3 simulations demonstrate that the interferers suffer a considerable attenuation, avoiding distortion and intermodulation problems that have an huge impact in modern RF receivers, specially in the LNA stage. The higher IIP_3 of the 65 nm circuit is due to the lower bandwidth, which allows to attenuate interferers that are closer to the desired signal, comparing with the 130 nm circuit.

It was verified that exists a trade-off between the filters' performance (f_{LO} and out-of-band impedances) and the NF of the overall circuit. Therefore, the filters' dimensions should be chosen according to the circuit specifications. The only purpose of the chosen values for both circuits is to verify if they have the desired behavior.

5.2 Passive Mixer and Transimpedance Amplifier

The mixer that was employed in this receiver has the same properties of the filter studied in chapter 4, and is shown in Figure 5.10. Due to the mixer operate in current mode, its noise contributions are reduced and is very linear, as referred in section 2.4.2. Also, the use of the TIA at the mixer's output guarantees that the variation of the V_{DS} of the switches is reduced, which improves the circuit's linearity.

Since the best LNA performance was achieved with the 130 nm circuit, the mixer was developed in that technology and the transistors have a channel length of 120 nm, due to the reasons explained before.

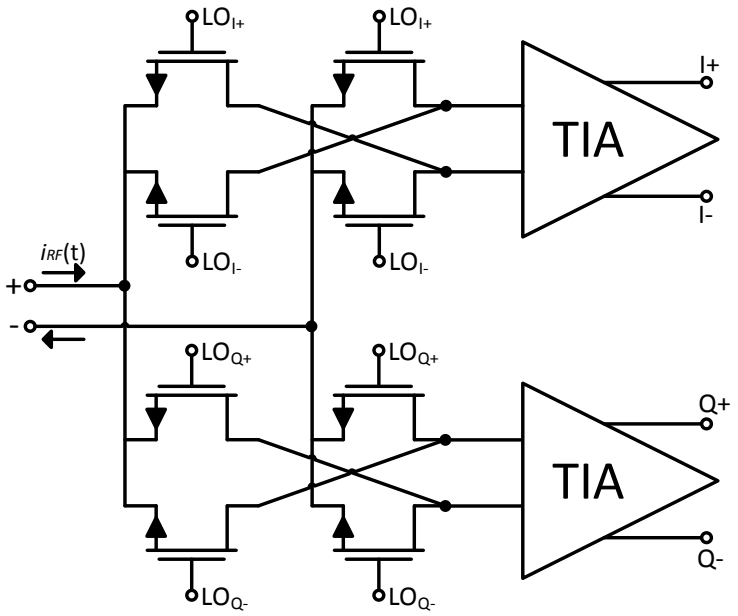


Figure 5.10: Mixer and TIA schematic

The mixer's outputs are connected to an ideal TIA with an input impedance of 100 kΩ, a transimpedance gain $A_{vi} = 10$ kΩ and a bandwidth of approximately 8 MHz. The mixer has quadrature outputs in order to handle modern modulation schemes, has four phases and needs to be driven by the same signal that clocks the two high-Q BPFs that are integrated in the LNA, since it has the same behavior. Regarding the input, the simulations that were made in this section consider that the mixer is driven by a load equal to the studied LNA's output impedance, $R_L \approx 700\ Omega$. Since this node is differential, the total equivalent resistance is approximately 1.4 kΩ. The mixer input impedance is shown in Figure 5.11.

Due to the configuration represented in Figure 5.10 the mixer's input presents a lower impedance for frequencies near f_{LO} and an higher impedance for frequencies far from the desired. This means that the mixer behaves like a notch filter, i.e. allows the desired signals (near f_{LO}) to flow to the circuit and be shifted to the IF, since it presents a low impedance at these frequencies, and attenuates the signals located at undesired frequencies (far from f_{LO}) due to the large input impedance. The mixer was projected to exhibit a bandwidth identical to the LNA studied in section 5.1.1 and taking into account the TIA's bandwidth that was previously referred. Dimensions of $W = 34.4\,\mu$m, which leads to $R_{SW} \approx 61\Omega$, were obtained for a mixer's bandwidth of 5.7 MHz, with $f_{LO} = 600$ MHz.

By applying a differential current RF signal with $I_{in} = 10\ \mu$A and $f_{RF} = 601$ MHz at the mixer's input, fed by a LO with $f_{LO} = 600$ MHz, the signal at the output of the TIA can be seen in Figure 5.12.

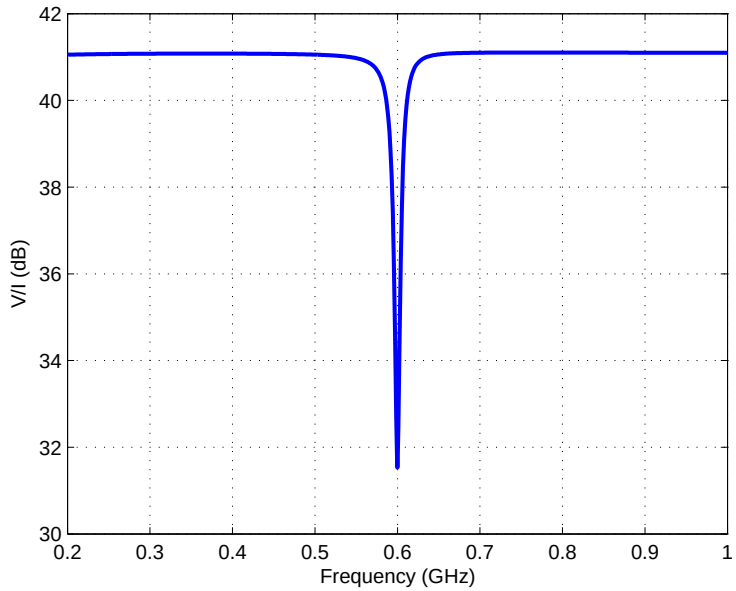


Figure 5.11: Mixer input impedance with $f_{LO} = 600$ MHz

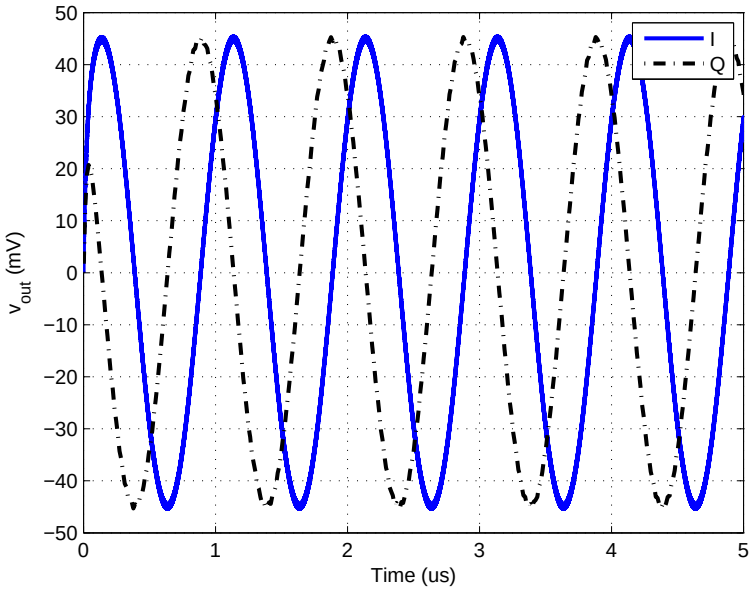


Figure 5.12: TIA output signal

As expected, the I and Q signals are identical, with a difference of 90º in phase. The output signal has a value of $v_{out} = 45.4$ mV, with a frequency equal to $f_{RF} - f_{LO} = 1$ MHz. This IF value was chosen taking into account that a low-IF is desired in order to relax the ADC requirements. The mixer's conversion gain (CG_{mixer}) is given by

$$CG_{mixer} = 20\log\left(\frac{v_{out}}{i_{in} \cdot A_{vi}}\right) = 20\log\left(\frac{45.4m}{10\mu \times 10k}\right) = -6.86\,\text{dB} \tag{5.1}$$

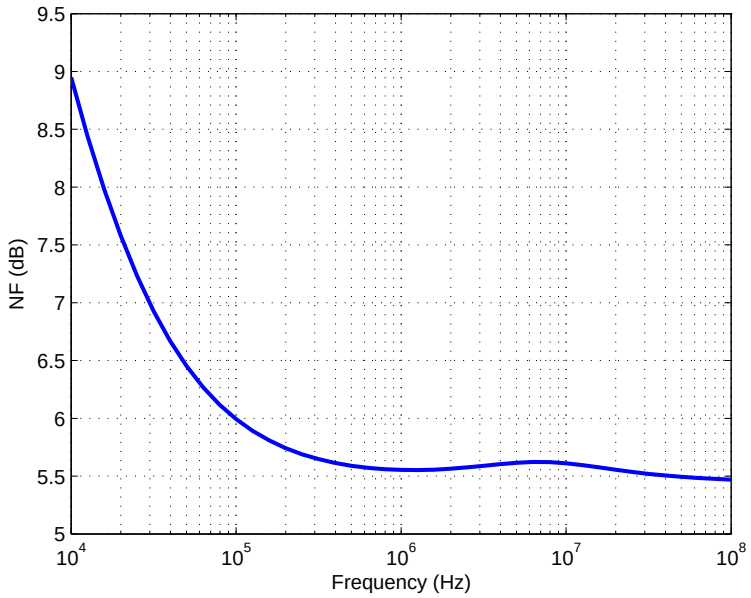


Figure 5.13: Mixer NF with $f_{LO} = 1$ GHz

Regarding the NF, it is lower than 6 dB for frequencies above 100 kHz and for all the interesting IF values (hundreds of kHz to few MHz), as shown in Figure 5.13. For this simulation it was considered $f_{LO} = 1$ GHz, which is the maximum operating frequency of the receiver and, as with the LNA (Figure 5.6), is the working frequency where the circuit has more noise contributions, i.e. for the other f_{LO} values between 0.3 GHz and 1 GHz, the mixer's NF is lower than the presented in this simulation. These noise contributions are mainly due to the thermal noise of the mixer's switches. Since the mixer is passive, the flicker noise is negligible (decoupling capacitors were placed between the LNA and the mixer to guarantee that there is no DC current flowing in this path). In order to reduce the NF, the transistors' size can be reduced to increase R_{SW} and consequently decrease the transistors' current thermal noise, as expressed in (2.20). However, reducing R_{SW} increases the circuit bandwidth (and reduces the Q factor) and decreases the mixer's interferers attenuation as stated in (4.8), since R_{SW} becomes closer to the LNA's output resistance. It also reduces the CG_{mixer}, because the mixer's input impedance grows and consequently the RF signal flows less to the mixer's path, being attenuated. As with the LNA, the mixer should be projected according to the system requirements.

For the IIP_3 simulation, shown in Figure 5.14, was obtained a value of 17.45 dBm, which means that the mixer can handle large interferers without corrupting the desired signal and is very linear, as expected in a current-driven passive mixer. For this simulation two pure sine waves were placed at the mixer's input, spaced 20 MHz, $f_1 = 1001$ MHz and $f_2 = 1021$ MHz, with a LO frequency of $f_{LO} = 1$ GHz. As with the LNA (Figure 5.8), the lower IIP_3 value was obtained for this frequency, for the same reasons.

A summary of the mixer's parameters is presented in Table 5.8.

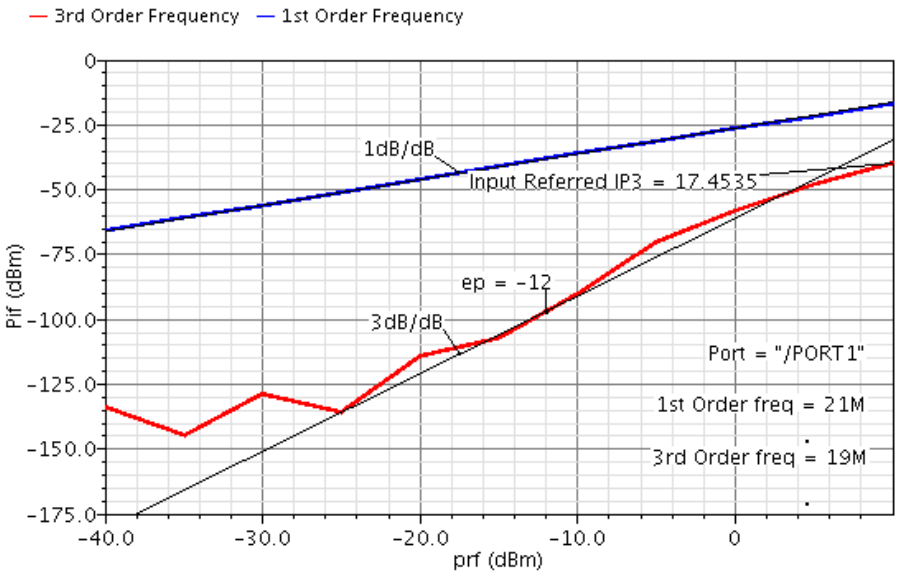


Figure 5.14: Mixer IIP_3 with $f_{LO} = 1$ GHz

Table 5.8: Mixer parameters

CG_{mixer} [dB]	NF [dB]	IIP_3 [dBm]	Tech. [nm]
-6.86	< 6	> 17.45	130

5.3 Complete receiver with Transimpedance Amplifier

To validate if the developed receiver has the desired behavior, the blocks that were analyzed in the previous sections were combined, resulting in the circuit of Figure 5.15. It is important to note that this analysis was made only for the circuit at 130 nm, since the best results were achieved using this technology. The 65 nm receiver will be referred in the next sections.

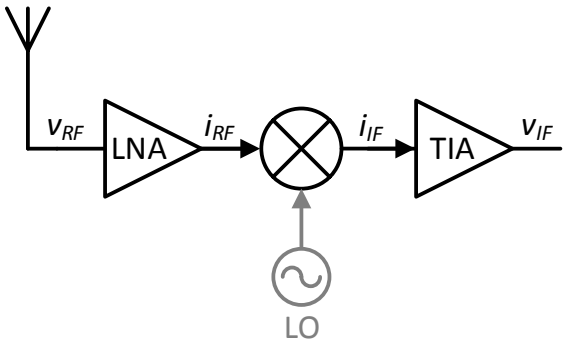


Figure 5.15: RF receiver with TIA

By placing a pure sinusoid with $f_{RF} = 601$ MHz and $v_{RF} = 1$ mV at the input of the receiver, with $f_{LO} = 600$ MHz, the obtained simulation result for the receiver's output

signal is shown in Figure 5.16. As expected, this signal is the same pure sine wave translated to 1 MHz (as shown section 5.2) and with an amplitude of $v_{out} \approx 142$ mV, which means that the mixer's output current is approximately $14.2\ \mu$A.

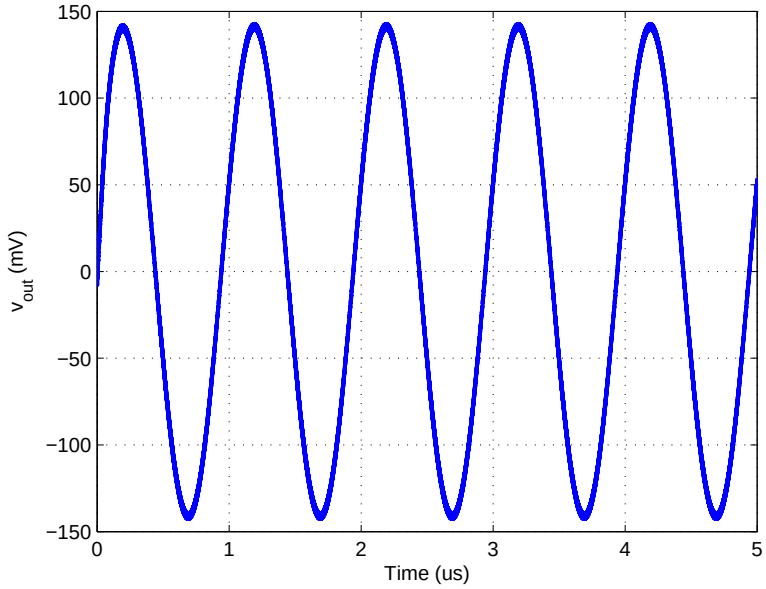


Figure 5.16: Receiver output signal with one sine wave at the input

As with the mixer (section 5.2), the receiver highest NF is verified when $f_{LO} = 1$ GHz. The obtained simulations results can be seen in Figure 5.17.

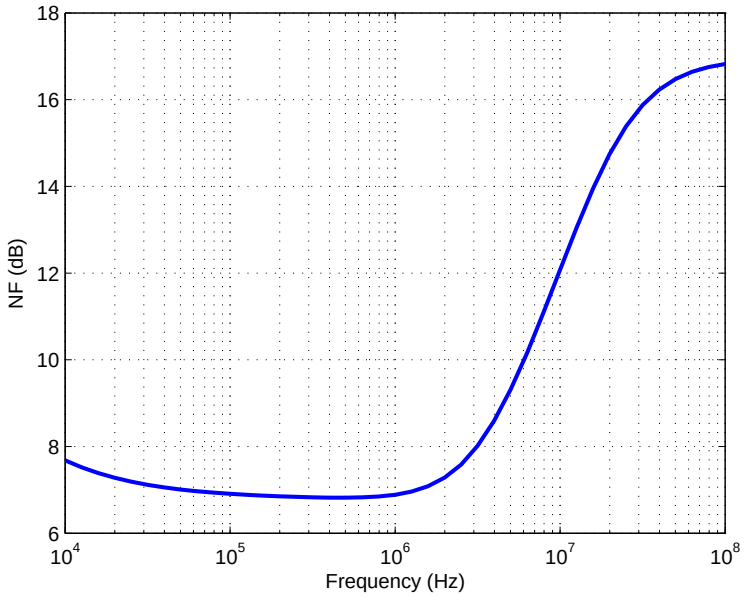
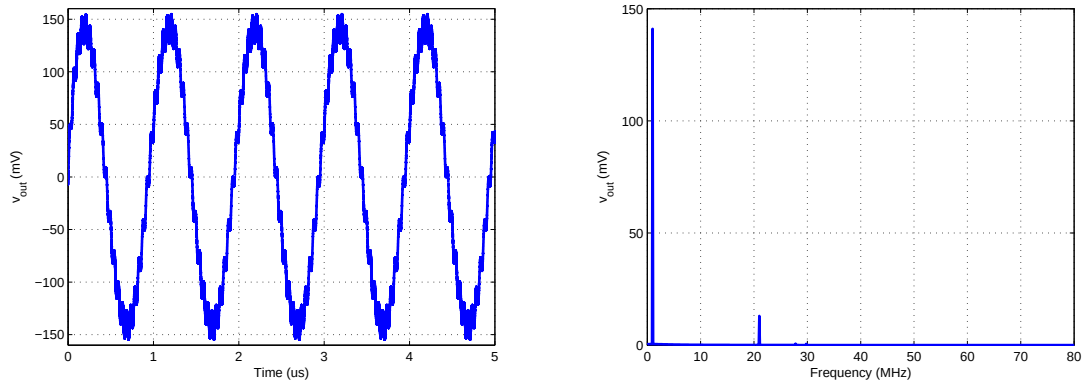


Figure 5.17: Receiver NF with $f_{LO} = 1$ GHz

For the desired IF values (hundred of kHz to few MHz) was obtained a $NF < 10$ dB

and for the IF used in this work (1 MHz) the receiver's NF is approximately 6.9 dB. The large growth of the NF at high frequencies is mostly related with the LNA's noise contributions that, as shown in Figure 5.4, are very large for frequencies far from f_{LO}. For lower frequencies the LNA noise contributions are reduced due to the BPF effect of the integrated filters' baseband capacitors. Such as the mixer, the receiver's NF has an huge peak at f_{LO}, but this frequency is very far from the desired IF and consequently this effect is insignificant.

To test the interferers attenuation two pure sinusoids were placed at the receiver's input, both with the same amplitude $v_{RF} = 1$ mV, one at $f_{RF_1} = 601$ MHz and another at $f_{RF_2} = 621$ MHz (acting as an out-of-band interferer). The time domain response (Figure 5.18a) shows that the output signal is a sine wave at 1 MHz, as expected, but with a little amount of noise that was introduced by the second sinusoid (f_{RF_2}).



(a) (b)

Figure 5.18: Receiver output signal with two sine waves (a) time domain (b) DFT

By analyzing the signal Discrete Fourier Transform (DFT) (Figure 5.18b) is possible to conclude that exist two frequency components. The desired, at 1 MHz, and an undesired component at 21 MHz. This second component is the f_{RF_2} translated to the baseband. However, this component is very attenuated (is more than ten times smaller than the desired signal) and has a minor effect in the output signal. This proves that the receiver can handle larger interferers without affecting to much the desired signal, since they are attenuated more than 20 dB comparing with the signal at f_{LO}.

Regarding the receiver's IIP_3, it was obtained a value of 0.23 dBm, as shown in Figure 5.19. For this simulation two pure sine waves were placed at the receiver's input, spaced 20 MHz, $f_1 = 602$ MHz and $f_2 = 622$ MHz, with $f_{LO} = 600$ MHz. Contrary to the IIP_3 simulation of the previous section, the chosen IF is 2 MHz and the f_{LO} is not 1 GHz, which is the frequency where the IIP_3 has the worst value, theoretically. This discrepancy is due to simulator constraints that does not allow to use the previous values. However, this analysis still valid and allows to understand the receiver's behavior.

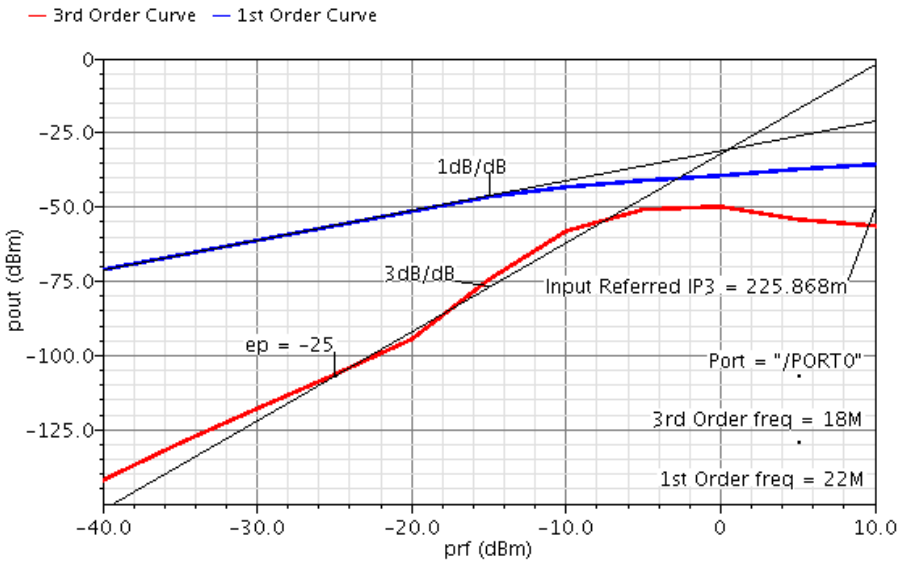


Figure 5.19: Receiver IIP_3

5.4 Current-buffer

In order to avoid the use of a TIA, to convert the IF current signal to a voltage signal before the digital part of the receiver, a current-driven $\Sigma\Delta$ modulator [6] was used in this work, which allows to directly convert the signal at the mixer's output to the digital domain. The Current-Buffer (CB) studied in this section is intended to perform the interface between the receiver's AFE and the $\Sigma\Delta$ modulator, as shown in Figure 5.20. This circuit is essential to guarantee the receiver proper functioning, since both blocks (mixer and $\Sigma\Delta$) have different impedances, which causes the second circuit to load the first one an consequently interfere with its operation. Also, this CB can provide current gain (or attenuation) to allow the tuning of both circuits and ensure that the $\Sigma\Delta$ operates at full-scale when the RF signal at the AFE's input is maximum.

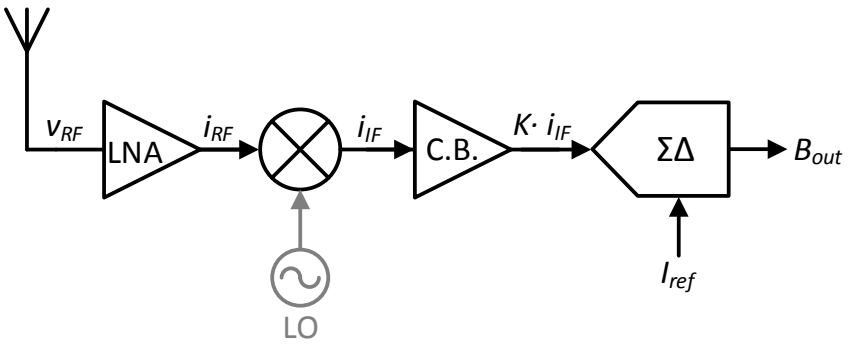


Figure 5.20: RF receiver schematic with CB and $\Sigma\Delta$

5.4.1 Theoretical Analysis

The studied CB [31, 32], presented in Figure 5.21, consists in a flipped voltage follower current sensor (FVFCS) that operates as current mirror.

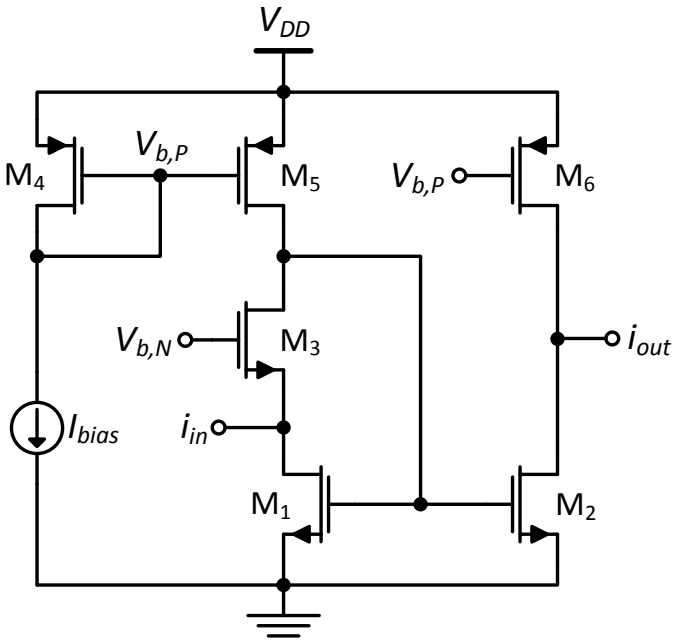


Figure 5.21: Current-buffer schematic

The transistor M_3 is in a feedback loop, with unitary gain, and does not conduct any AC current. This allows the circuit to have a very low input impedance, given by [32]

$$R_{in} \approx \frac{\frac{1}{g_{m3}}\left(1+\frac{r_{ds5}}{r_{ds3}}\right) \parallel r_{ds1}}{g_{m1}\left(r_{ds5} \parallel g_{m3}\cdot r_{ds3}\cdot r_{ds1}\right)}, \tag{5.2}$$

where g_{mi} and r_{dsi} are the transconductance and output resistance of transistor M_i, respectively. For the specific case where $r_{ds3} \approx r_{ds5}$,

$$R_{in} \approx \frac{2}{g_{m1}\cdot g_{m3}\cdot r_{ds3}}. \tag{5.3}$$

The output impedance of this configuration is given by

$$R_{out} \approx r_{ds2} \parallel r_{ds6}, \tag{5.4}$$

which leads to an high output impedance. Since an ideal current buffer has null input impedance and infinite output impedance (as an ideal current source), this circuit behaves almost like an ideal current buffer and is expected a minimum interference in the AFE and $\Sigma\Delta$ circuits.

By changing the bias current (I_{bias}) is possible to modify the input and output impedances, since $g_m \cong 2I_D/V_{Dsat}$ and $r_{ds} \propto L/I_D$ [15], with $I_D = I_{bias}$ for the the input stage and $I_D = I_{bias}/k$ for the output stage, where k is the CB multiplication factor. If I_{bias} increases,

the input impedance decreases and the output impedance also decreases, but the circuit's power consumption increases.

As explained before, this circuit has unitary gain, due to the feedback of the transistor M_3. However, the current range of the AFE circuit is usually different from the $\Sigma\Delta$ and there is the need to scale the gain of the CB. This can be achieved by changing the relation of the transistors $M_1 - M_2$ and $M_5 - M_6$. For example, if it is desired $i_{out} = k \cdot i_{in}$, $W_{M2} = k \cdot W_{M1}$ and $W_{M6} = k \cdot W_{M5}$, where W_{Mi} is the channel width of the transistor M_i . Thus, is possible to scale the current that passes through de output stage devices by a factor of k, relatively to the current of the input stage.

Regarding the supply voltage, this circuit can operate with very low values, since the maximum supply voltage (V_{DD}) necessary to guarantee that all transistors operate in the active region is given by the sum of the DC voltages of the input stage,

$$V_{DD,min} = V_{GS,M1} + V_{Dsat,M5} = 2V_{Dsat} + V_{Tn}. \tag{5.5}$$

For 65 nm CMOS technology, $V_{Tn} \approx 300$ mV. Obviously, a margin should be added to V_{DD} in order to guarantee that all the transistors are operating in the active region ($V_{DS} > V_{Dsat}$).

5.4.2 Simulation Results

Given that the mixer and $\Sigma\Delta$ circuits are differential, two identical CB (Fig. 5.21) were used for the interface between these two circuits. However, this analysis only consider one CB, for simplicity. This circuit was developed in CMOS 65 nm because the used $\Sigma\Delta$ was designed in this technology and all receiver's blocks need to use the same technology, in order to be possible to have a fully integrated RF receiver. To avoid short channel effects, and considering that this circuit operates at relatively low frequencies, all the transistors have a length of 150 nm. The dimensions and key parameters of all transistors are presented in Table 5.9.

Table 5.9: Current-buffer parameters

Device	W (μm)	L (μm)	ID (μA)	VDsat (mV)	gm (μS)
M_1	5	0.15	21.3	54	374
M_2	1.1	0.15	6.5	58	108.3
M_3	4	0.15	20	61	321.3
M_4	17	0.15	15	59	315.2
M_5	17	0.15	19.9	60	411.4
M_6	5.3	0.15	6.6	61	133.9

Since the bias current is small ($I_{bias} = 15\,\mu$A), the transistors need to have a low V_{Dsat} due to channel width limitations (specially the transistor M_2 that carries lower current). A possible solution to this restriction is increase I_{bias} but it leads to a decrease of the output impedance and more power consumption, as previously referred. Regarding the

input and output impedances, were obtained $R_{in} \approx 500\ \Omega$ and $R_{out} \approx 140\ k\Omega$, which means that the CB has a behavior similar to an ideal current source (relatively low input impedance and high output impedance).

Comparing the devices M_1 and M_2 is possible to conclude that $k \approx 0.3$, which means that the current at the output of the AFE is attenuated in order to the $\Sigma\Delta$ reach the full-scale and does not saturate, as will be demonstrated in the next section. In order to verify if the CB operation is within the expected, a pure sinusoid with $i_{in} = 30\ \mu$A and $f = 400$ kHz was injected in the circuit's input. The simulation results are shown in Figure 5.22. Comparing the input and output signals is possible to conclude that both signals have the same frequency and $i_{out} \approx 0.3 \cdot i_{in}$, as desired. The phase shift of the output signal is due to the CS transistor.

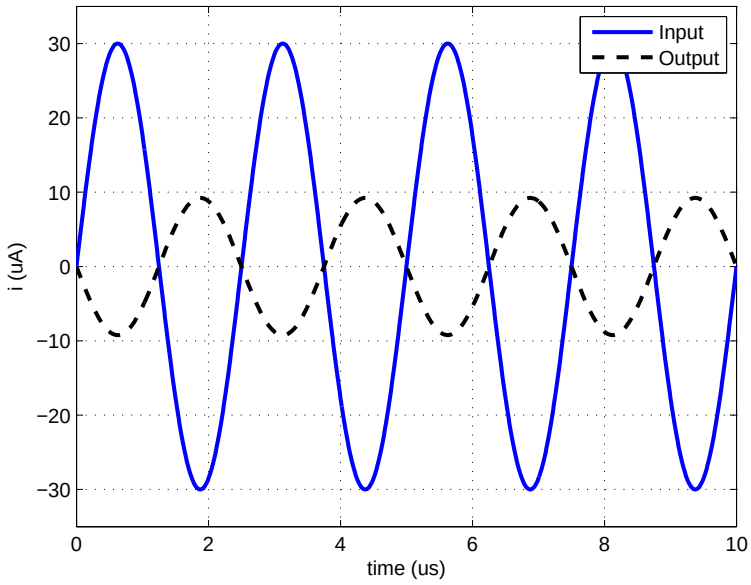


Figure 5.22: Current-buffer time response

5.5 Complete receiver with Sigma-Delta Modulator

The employed $\Sigma\Delta$ modulator, referred in [6], consists in a current-mode passive second-order continuos-time $\Sigma\Delta$, which allows to convert an analog current signal directly to the digital domain, avoiding the use of a TIA that introduces noise and increases the chip area and cost. In order to understand the circuit's behavior when it is fed by an ideal current source, an ideal sine wave was placed at its inputs, with $i_{in} = 7.5\ \mu$A and $f_{in} = 420$ kHz, with the $\Sigma\Delta$ reference current equals to $I_{ref} = 10\ \mu$A and a supply voltage of $V_{DD} = 1$ V. The obtained Fast Fourier Transform (FFT) is presented in Figure 5.23. Operating at full-scale, the $\Sigma\Delta$ has a resolution of 7.6 bits and an Signal-to-noise and Distortion Ratio (SNDR) $= 47.5$ dB. These results will serve as base of comparison to the complete receiver.

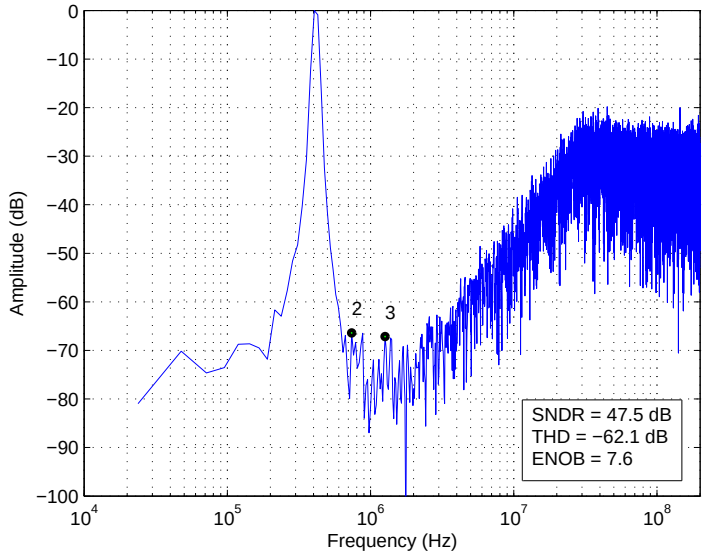


Figure 5.23: Output spectrum of the $\Sigma\Delta$ modulator fed by an ideal current source

As referred before, the receiver studied in this section (Figure 5.20) is identical to the receiver studied in section 5.3, without the ideal TIA block, but developed using CMOS 65 nm technology instead of CMOS 130 nm. Since both circuits have the same characteristics, the receiver of this section was not studied (except the LNA block in section 5.1.2) and its only purpose is to verify if is possible to integrate the $\Sigma\Delta$ at the receiver's output. For the complete receiver, shown in Figure 5.20, which uses the studied LNA and mixer, and with a CB supply voltage of 1 V, the $\Sigma\Delta$ FFT shown in Fig. 5.24 was obtained. For this simulation a pure sine wave with $v_{RF} = 880\ \mu$V and $f_{RF} = 600.42$ MHz was placed at the receiver's input. The LO has a frequency of $f_{LO} = 600$ MHz, which leads to a IF of 420 kHz.

Comparing with Figure 5.23, the ENOB decreases 1.4 bits, to 6.2 bits, and the SNDR decreases 8.6 dB, to 38.9 dB. This penalty in performance is expected because the AFE introduces a reasonable amount of noise to the desired signal and the CB has not null input impedance and infinite output impedance, like an ideal current buffer, and consequently has influence in the $\Sigma\Delta$ behavior, comparing with an ideal current source. For this supply voltage, the CB DC power consumption (for the single-ended version) is about $42\ \mu$W.

As referred in section 5.4.1, the CB can theoretically operate with very low supply voltages, in the order of milivolts. To analyze that characteristic, the supply voltage was reduced by a 100 mV step from 1 V to 400 mV, while keeping the same transistors size. The obtained results are presented in the Table 5.10.

For 400 mV it was impossible to guarantee that all the transistors operate in the active region and the resulting simulation was very poor. From 900 mV to 500 mV the obtained results are practically the same, with a penalty of 0.3 bits in the ENOB and 2 dB in SNDR. This means that the circuit performance does not depend of the supply voltage and is

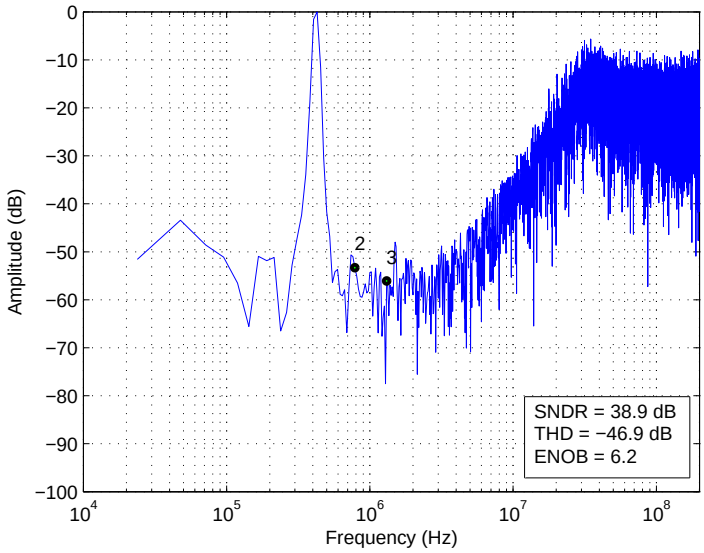


Figure 5.24: FFT of ΣΔ modulator driven by the complete studied receiver

Table 5.10: FFT of ΣΔ modulator for sub-1V supply voltages

V_{DD} (mV)	SNDR (dB)	THD (dB)	ENOB
900	37.8	-44.2	6.0
800	37.8	-47.2	6.0
700	37.1	-44.1	5.9
600	36.2	-43.3	5.7
500	35.8	-42.3	5.7

only necessary to guarantee that all the transistors operate in the desired region.

With $V_{DD} = 500$ mV, the CB DC power consumption (for the single-ended version) is about $21\ \mu$ W, which is the half comparing with the simulation with $V_{DD} = 1$ V.

6

Conclusions and Future Work

6.1 Conclusions

With the increase of wireless communications the frequency spectrum is becoming very crowded, leading to more interferences. To overcome this problem is necessary to employ filters that reject the unwanted signals at the receiver's input. However, traditional filters (e.g. SAW filters) are difficult to integrate in the receiver due to its complexity and area, which makes impossible to employ an IC with the complete receiver, and have associated problems related with impedance matching and cost.

In this work a wideband RF receiver was presented, based on the integration of high-Q passive BPF filters in circuit nodes. To achieve the desired attenuation, two high-Q BPF, based in a current-driven passive mixer, were integrated in a wideband balun-LNA nodes. One at the input, that also contributes to the impedance matching, and another at the cascodes' input nodes. The mixer also performs some filtering due the current-driven characteristics.

Regarding studied BPF, simulation results demonstrate that this filter is programmable and can be precisely tuned by the LO, with a penalty of about -1.82 dB in the overall circuit gain, for a filter with four phases. This filter presents an high Q factor and, since it is passive, has almost no DC power consumption and flicker noise, leading to low noise contributions. By employing a differential version of the filter is possible to filter signals located at the LO even order harmonics frequencies and obtain the double of the filter input impedance, comparing with the single-ended filter.

The integration of the studied high-Q BPF in the wideband balun-LNA allows to obtain a widely tunable narrowband balun-LNA that can attenuate out-of-band interferers

about 14 dB (for the 130 nm circuit), with respect to signals located at f_{LO}, with a minimum penalty in the circuit voltage gain and NF (3 dB and 1.5 dB respectively), comparing with the LNA only. Regarding the distortion and the nonlinearities, it was obtained $IIP_2 > +22$ dBm and $IIP_3 > -4$ dBm, which are significantly better values comparing with the LNA only and proves that the integration of the filters in the LNA increased the circuit linearity and allows to attenuate interferers located near the interesting frequency. Since the filters are passive, the LNA power consumption remains piratically the same. By employing this technique is possible to avoid the use of external filters at the input/output of the LNA, which require a multi chip circuit that has area and cost penalty. Thus, is possible to reduce the overall circuit area and costs, and allow the full integration of the receiver in the same chip. It was verified that exists a trade-off between the filters' performance and the NF of the LNA block, i.e. an increase of the filters' out-of-band attenuation leads to a reduction of the voltage gain at the desired frequencies and to the increase of the circuit's NF. Therefore, the filters should be projected according to the system specifications. A comparison between the used technologies (CMOS 130 nm and CMOS 65 nm) shows that both circuits have the intended operation but the 130 nm circuit is much better in terms of NF (about the half comparing with the 65 nm circuit).

Regarding the 130 nm mixer, was obtained a conversion gain of about -6.9 dB, NF < 6 dB and $IIP_3 > 17.45$ dBm, which means that the mixer is very linear and can handle large out-of-band interferers without corrupting the desired signal.

Simulation results of the complete receiver AFE, using CMOS 130 nm technology, show an $IIP_3 = 0.23$ dBm and a NF < 10 dB for IFs of interest. For an interferer located at 20 MHz of the desired signal, with the same amplitude, was obtained an attenuation of more than 20 dB, comparing with the signal of interest. with an attenuation of interferers located at 20 MHz from the desired signal of 20 dB. This receiver was projected to work at frequencies between 0.3 GHz and 1 GHz.

To allow the direct conversion of the current signal at the mixer's output to the digital domain, a current-mode $\Sigma\Delta$ was employed in the receiver. To perform the interface between the mixer and the $\Sigma\Delta$, a CB with high dynamic range was developed, which prevents that the $\Sigma\Delta$ loads the mixer, due to the different impedances of both blocks, and affects its functioning. This CB also allows to scale the current at the mixer's output in order to the $\Sigma\Delta$ operate at full-scale when the signal at the receiver's input is maximum.

The complete RF receiver, developed in 65 nm, causes a drop of 1.4 bits in the $\Sigma\Delta$ resolution, comparing with the $\Sigma\Delta$ driven by an ideal sine wave, being possible to achieve a resolution of 6.2 with CB and $\Sigma\Delta$ supply voltages of 1 V. Regarding the SNDR, it was obtained a value of 38.9 dB. This penalty is due to the noise introduced by the AFE and the CB and the fact that the CB has not null input impedance and infinite output impedance, as ideally desired. This means that the receiver AFE can be directly connected to a $\Sigma\Delta$ modulator without the use of additional blocks, like a TIA, that introduce more noise to the circuit and increase the chip area and cost.

6.2 Future Work

The realization of this work has introduced some interesting topics that can be further improved.

The widely tunable narrowband balun-LNA can be optimized for a specific application and compared with other existing circuits in order to understand the real advantages of this circuit.

The receiver with the $\Sigma\Delta$ modulator could be investigated and tuned in order to obtain a better overall performance and to understand the influence of the $\Sigma\Delta$ in the AFE behavior.

Since this work consisted only in theoretical and simulation results, future work should include the IC manufacture to validate the obtained results through measurements.

Finally, a future work can consist in the design of the RF transmitter for a complete transceiver front-end.

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Published Paper

"A Widely Tunable Narrowband Balun-LNA with Integrated Filtering"

A Widely Tunable Narrowband Balun-LNA with Integrated Filtering

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***Abstract*—A cascode balun-LNA with integrated out-of-band filtering for radio applications between 300 MHz and 1 GHz is proposed. First the high-Q bandpass filter (BPF) and the low noise amplifier (LNA) are analyzed, separately, in order to understand its characteristics and how both circuits can operate together. To allow maximum out-of-band interferers attenuation a single-ended and a differential filters are used in LNA, at the input and at the cascode devices, respectively. Using standard 130 nm CMOS technology operating at 1.2 V supply voltage, we obtained a voltage gain greater than 23.7 dB, noise figure (NF) lower than 3.3 dB, IIP2 $>+$ 22 dBm and IIP3 $>-$ 4 dBm. For out-of-band frequencies the interferers are attenuated, at least, by 14 dB relatively to the desired signals.**

***Index Terms*—CMOS, discrete filter, high-Q bandpass filter, impedance transformation, inductorless LNA, noise cancellation, N-path filter, SAW-less, tunable LNA, wideband matching.**

I. Introduction

One of the major problems of radio receivers are the out-of-band interferers, which can corrupt the desired signal. In narrowband receivers this problem is solved with external filters that are tuned for a specific frequency, but this kind of approach is ineffective for wideband receivers since a large number of frequencies are covered so it would be necessary to have multiple front-ends for the various bands. Using the filtering techniques presented in [1], [2] together with a balun-LNA is possible to avoid external filters, as SAW filters, since the filter band is precisely controlled by a clock frequency, thus resulting in a tuned narrowband LNA that works over a wide range of frequencies. The used LNA is based on [3] and accomplish conversion from single-ended to differential (balun), while performing noise cancellation, and wideband input matching through a common-gate (CG) stage, which is essential for wideband receivers. In order to achieve a higher voltage gain and a lower NF we use active loads in the LNA instead of the traditional resistors.

In this paper we propose, as far as the authors knowledge, the first balun-LNA with embedded N-path filtering which consists in a single-ended filter, that also contributes to input impedance matching, and a differential filter, in order to attenuate the out-of-band interferers.

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The paper is structured as follows. Section II reviews the high-Q BPF to show its characteristics and analyze the filter response and the influence of the number of phases on its behavior, in order to understand how it can be integrated in the LNA circuit. Section III reviews the balun-LNA and presents some modifications that were made to the circuit and the simulation results. In section IV we analyze the simulations results obtained for the filtered LNA and its advantages and drawbacks compared with the previous section. Finally, section V presents conclusions.

II. Integrated High-Q Bandpass Filter

The filter described in this section consists in a current-driven passive mixer, which performs impedance transformation. This is possible because this kind of mixer has no reverse isolation, which allows the frequency-translation of the baseband voltage to around ω_{LO} (and its odd harmonics) [4] that is precisely controlled by the local oscillator (LO) frequency. For example, if the baseband impedance (Z_{BB}) is a low-Q lowpass filter (LPF), the RF side impedance will be a high-Q BPF with a center frequency equals to ω_{LO}, as shown in Fig. 1. Therefore, this filter exhibits high-impedance for the desired signal frequencies (near ω_{LO}) and offers a low-impedance path to interferers that are located outside the filter cutoff frequency [5]. These characteristics makes this kind of filters ideal for wideband receivers where is desirable to have high-Q BPFs that can be precisely tuned according to the input signal frequency.

Since the filter is passive it is low power and has no flicker noise, because it is proportional to the bias current [6].

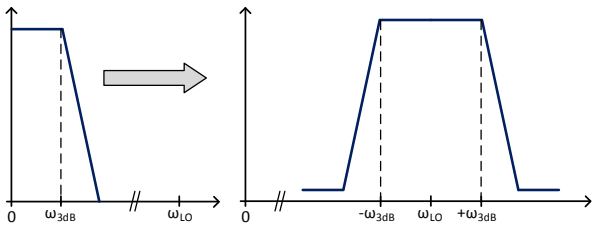
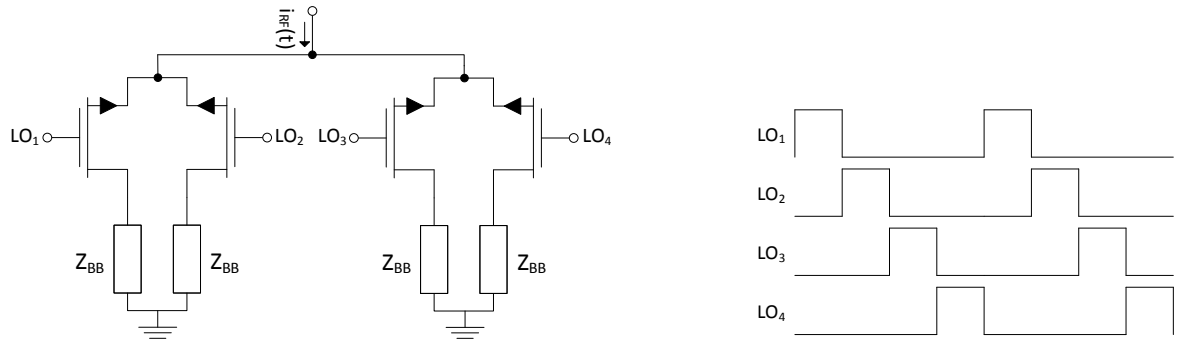


Fig. 1. LPF to BPF transformation



(a) (b)

Fig. 2. (a) Single-ended 4-phase High-Q BPF. (b) LOs waveform for a 4-phase filter

A. M-Phase Filtering

The basic structure of a High-Q BPF filter is shown in Fig. 2a. The Z_{BB} impedance is usually a capacitor (C_{BB}) or, if wider bandwidth is required, a parallel RC [5]. The LO produce rail-to-rail non-overlapped square waves with a ω_{LO} frequency and a duty cycle of $1/M$, as shown in Fig. 2b, where M is the number of phases of the filter.

Assuming that the switches are ideal with an on resistance equals to R_{SW}, the impedance of a single-ended M-phase high-Q BPF, for the frequency of interest ω_{LO}, is given by [1]:

$$Z_{in}(\omega) \cong R_{SW} + \frac{M}{\pi^2}\sin^2\left(\frac{\pi}{M}\right) \times [Z_{BB}(\omega-\omega_{LO}) + Z_{BB}(\omega+\omega_{LO})] \quad (1)$$

From the above equation is possible to note that a higher M increases the filter in-band impedance and from previous works [1] it is known that a higher M decreases the folding gain and moves the closest folding frequency component to $(M-1)\omega_{LO}$, avoiding the folding of interferers situated in some harmonics of ω_{LO} on top of the desired signal. To prevent image problems it is recommended to use at least $M = 4$.

For a MOS device, if $V_{DS} \approx 0$ (deep triode region) then the channel region behaves like a resistor R_{SW} that, for a NMOS, is expressed by

$$R_{SW} \approx r_{ds} = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{Tn})} \quad (2)$$

Keeping the length (L) of transistors constant if the width (W) is increased the resistance R_{SW} decreases and consequently the impedance $Z_{in}(\omega)$ decreases too, as expressed in (1). The main advantage of the triode region is that due to its properties the resulting filter is very linear.

B. Single-ended Implementation

A single-ended high-Q BPF, as shown in Fig. 2a, is proposed to be used at the input of the LNA and perform impedance matching while filtering the input signal.

Assuming that the LNA have an equivalent input impedance of $Z_L(\omega)$ and is connected to a filter as in Fig. 2a, the equivalent circuit can be shown in Fig. 3.

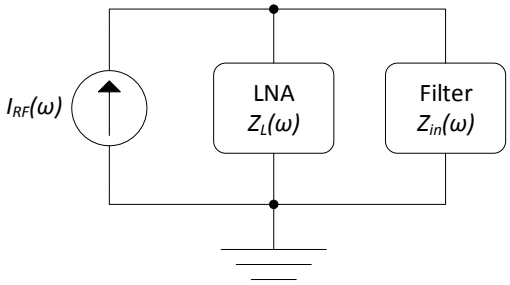


Fig. 3. Equivalent circuit of LNA input connected to high-Q BPF

From basic circuit analysis it is known that $\frac{V_{RF}(\omega)}{I_{RF}(\omega)} = Z_L(\omega) \parallel Z_{in}(\omega)$ and from (1) is possible to obtain (3) defined at top of the next page.

Considering a particular case where the LNA impedance, $Z_L(\omega)$, is equivalent to a resistor R_L and the impedance Z_{BB} is a capacitor C_{BB}, (3) can be expressed as [1]:

$$\frac{V_{RF}(\omega)}{I_{RF}(\omega)} \approx \frac{R_L}{R_L+R_{SW}} \times \left[R_{SW} + \frac{\frac{M^2}{\pi^2}\sin^2\left(\frac{\pi}{M}\right)R_L}{1+jM(R_L+R_{SW})C_{BB}(\omega-\omega_{LO})}\right] \quad (4)$$

From the previous equation is possible to note that to achieve the filter maximum performance the switches resistance R_{SW} should be close to zero and the LNA impedance R_L should have a large value in order to the filter exhibit a very low out-of-band impedance and a very large impedance for frequencies near ω_{LO}, filtering the out-of-band interferers and allowing the desired signal to flow almost completely through the intended circuit.

Since (4) results from an approximation of (3) the results obtained for large values of M tend to be more correct than

$$\frac{V_{RF}(\omega)}{I_{RF}(\omega)} \cong Z_L(\omega) \parallel \left(R_{SW} + \frac{M}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) \times [Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})] \right) \quad (3)$$

the results achieved with lower values because the effect of high order harmonics is less noticeable for bigger M [1].

Analyzing (4) is possible to verify that the circuit is acting as a BPF with the equivalent LPF bandwidth given by (5), as shown in Fig. 1.

$$\omega_{3dB} \approx \frac{1}{M(R_L + R_{SW})C_{BB}} \quad (5)$$

Considering that the filter is symmetric its bandwidth is approximately $2 \cdot \omega_{3dB}$. This shows that for a higher M the filter bandwidth is lower and the Q factor is higher since $Q = \omega_{LO}/(2 \cdot \omega_{3dB})$.

Thus, simulating the circuit of Fig. 3 and comparing with (4) is possible to verify that the results are pretty similar, as shown in Fig. 4, except for frequencies out-of-band of the filter where exists a little difference between the results mainly due to the fact that (4) is an approximation, as indicated before. The parameters used in this simulation are $R_L = 100\ \Omega$, $R_{SW} = 10\ \Omega$, $C_{BB} = 50$ pF, $\omega_{LO} = 600$ MHz and $M = 8$.

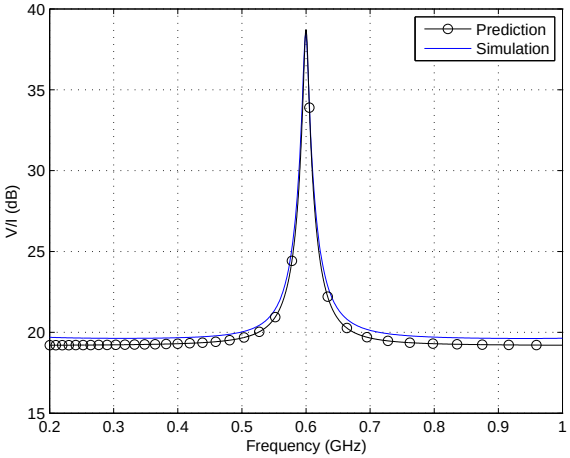


Fig. 4. Prediction of (4) *vs.* SpectreRF simulation results

In the simulation it was obtained a bandwidth of approximately 7 MHz with $Q = 84$, which is pretty similar to the prediction of (5), and the out-of-band impedance is nearly equal to $R_L \parallel R_{SW}$, as stated in (4).

The SpectreRF simulation was made through a PSS (with the LOs fundamental tones and no output harmonics) and PAC analysis with a DC current source (with PAC magnitude = 1) connected to the filter input. The LOs produce the waves shown in Fig. 2b with 1.2 V_{pp} and rise and fall times of 10 ps.

C. Differential Implementation

For differential nodes of LNA is necessary to use a differential filter, shown in Fig. 5. As expected, the impedance $Z_{in}(\omega)$

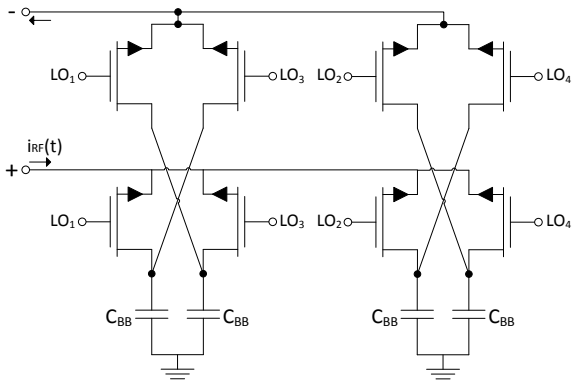


Fig. 5. 4-phase differential high-Q BPF

is similar to the single-ended version (equation (1)) but with twice the gain as stated in (6) [1].

$$Z_{in}(\omega) \cong 2R_{SW} + \frac{2M}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) \times [Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})] \quad (6)$$

Another advantage of differential filters is the fact that the even harmonics are canceled (including DC) [1], so the impedance seen around those harmonics is approximately zero (assuming $R_{SW} \approx 0$).

The analysis made in the previous subsection is valid for this implementation so the expected results are the same.

III. Cascode Balun-LNA

The LNA described in this section consists in a common gate (CG) and common source (CS) stages that are cascoded mainly to allow the use of the BPF described in section II-C, at the input of cascode devices, that is important to attenuate the out-of-band interferers. As explained in section II-B to achieve its maximum performance the filter needs to be in parallel with a high impedance so the cascode MOS transistors should have a low g_m since the impedance of this node is approximately $1/g_m$. To achieve the desired filtering the impedance of CG stage needs to be equal to the CS stage in order to the filter have the same impedance at both inputs. The CG stage performs wideband input impedance matching through its transconductance and the CS stage performs noise cancellation, since both stages have opposite phases.

In order to improve the LNA performance the resistors R_{CG} and R_{CS} described in [3] were replaced by PMOS devices, as shown in Fig. 6, working in triode region and acting as resistors. With this technique is possible to achieve a higher resistance with the same voltage dropped by the resistors, reducing the NF and increasing the voltage gain since $A_v \approx g_m \cdot R$.

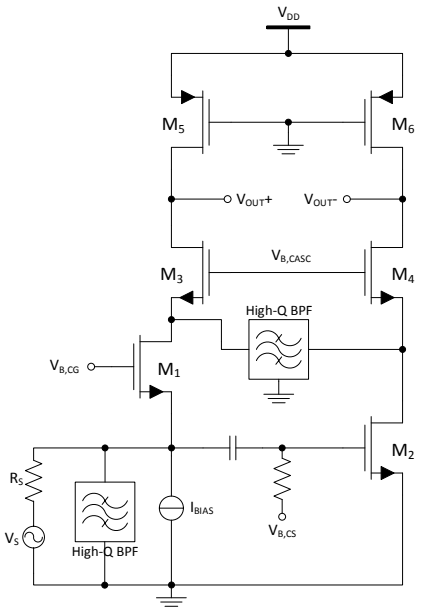


Fig. 6. Cascode balun-LNA with both filters

For the circuit of Fig. 6, but ignoring the both filters for now, the following simulation results were obtained:

TABLE I
LNA SIMULATION RESULTS

Freq. [GHz]	Volt. Gain [dB]	NF [dB]	S_{11} [dB]	Power [mW]	V_{DD} [V]	Tech. [nm]
0.3 - 1	$\approx$ 27	$<$ 2	$<$ -13.2	$\approx$3.6	1.2	130

To achieve these results all the transistors have the minimum channel length allowed by the technology (120 nm), in order to be possible to achieve higher frequencies, and W_{M1} = 75.2 μm, W_{M2} = 230.4 μm, $W_{M3,4}$ = 5.6 μm and $W_{M5,6}$ = 7.2 μm.

The Fig. 7 shows the NF for the working frequencies of LNA. Due to flicker noise the NF is higher for lower frequencies and between 300 MHz and 1 GHz is below 2 dB, which is quite acceptable.

IV. Cascode Balun-LNA with Filtering

To suppress the out-of-band interferers two filters were used. A single-ended (analyzed in section II-B) at the input of LNA and a differential (analyzed in section II-C) at the input of cascode stages, as shown in Fig. 6. Both filters have four phases in order to avoid image related problems as explained in section II-A. To understand the influence of these filters in the LNA response three different analyses were made. Only with the filter at the input, with the filter at cascode stages and with both filters.

A. LNA Response Analysis

As expected the filtered LNA gain have the same shape of Fig. 4 since the filters impedance is high for in-band

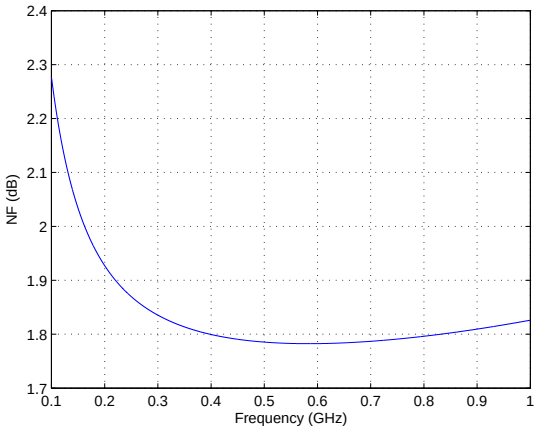


Fig. 7. LNA NF

frequencies and low for out-of-band frequencies, as shown in Fig. 8. Thus, the signals with frequencies near f_{LO} flow to the cascode MOS transistors and the undesired signals flow to the filters, and are not amplified, because its impedance is much lower than the transistors one.

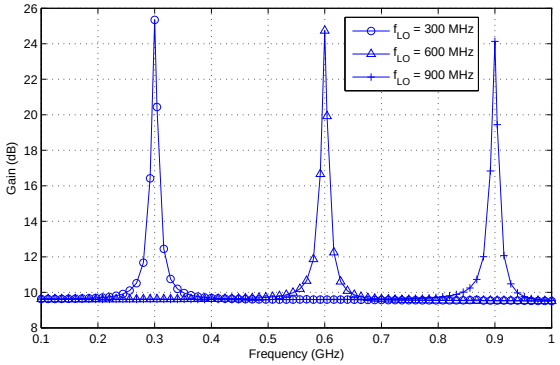


Fig. 8. LNA voltage gain, for multiple values of f_{LO}, with both filters

For those simulations the following bandwidths and Q factors were obtained:

TABLE II
FILTERED LNA BANDWIDTH AND Q FACTOR

f_{LO} (MHz)	300	600	900
Bandwidth (MHz)	5.7	6.1	6.6
Q factor	52.4	98.4	136.3

The bandwidth is almost constant for the entire LNA working band so as the f_{LO} is increased the Q factor gets higher. As expected, a high Q is obtained for all frequencies of interest.

Since out-of-band signals are corrupted by the filter the NF is much higher for those frequencies, as shown in Fig. 9. The S_{11} parameter have the same shape as NF because for the undesired frequencies the filters impedance is very low ($\approx$

R_{SW}) and since they are in parallel with LNA the equivalent input impedance is also very low resulting in a poor input matching and high S_{11}.

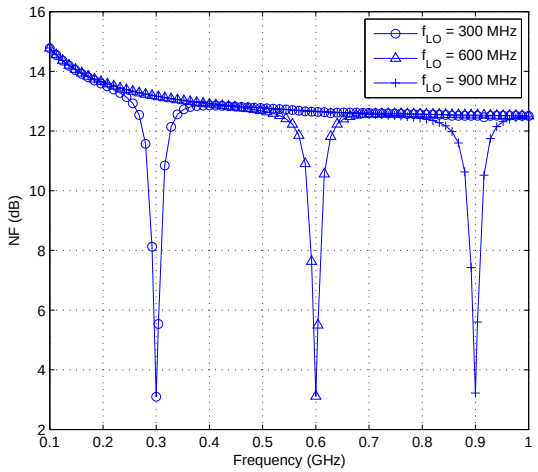


Fig. 9. LNA NF, for multiple values of f_{LO}, with both filters

B. Simulation Results

To understand the influence of the filters in LNA response it was made a frequency sweep, for the working band, to analyze the different parameters - gain, NF, S_{11}, IIP_2 and IIP_3.

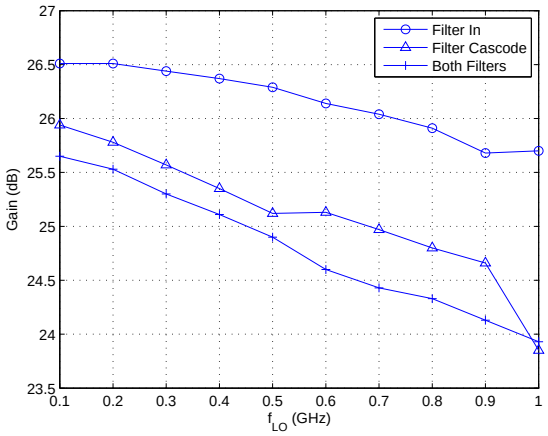


Fig. 10. LNA gain at f_{LO}

Comparing the gain at f_{LO} (Fig. 10) with the voltage gain of LNA (table I) it is possible to note that if the number of filters is increased the gain is lower, and for both filters the LNA voltage gain is about 3 dB lower in the worst case. This reduction of gain is related to the fact that the filter has not an infinite impedance at f_{LO} so the signal of interest does not flow completely through the cascode stages resulting in less amplification, as explained in section II-B.

Relatively to out-of-band gain (Fig. 11) is possible to verify that for both filters the LNA has a gain of about 10 dB so

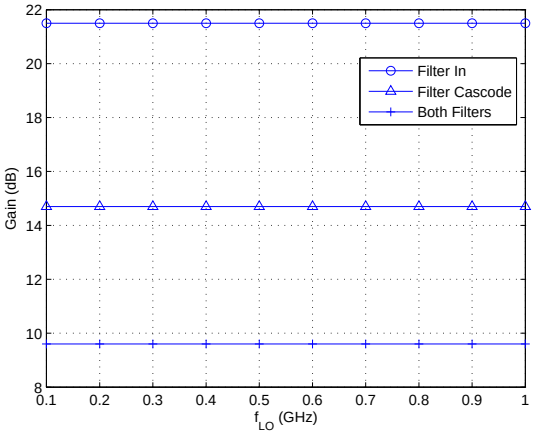


Fig. 11. LNA out-of-band gain

the interferers suffer an attenuation of approximately 14 dB, comparing with the signals at the desired frequencies. It's also possible to note that if two filters are used the out-of-band gain is much smaller than if only one filter is used and the gain at f_{LO} is only slightly reduced.

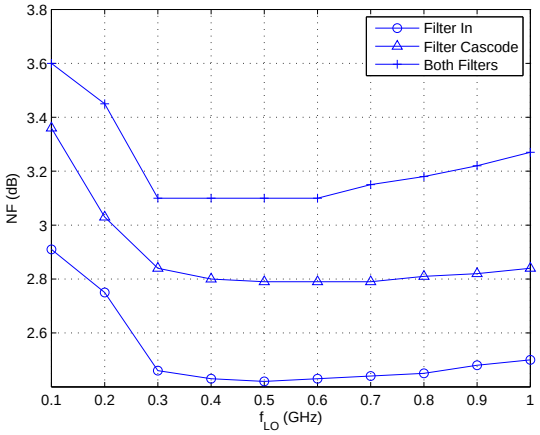


Fig. 12. LNA NF at f_{LO}

For the circuit with both filters the NF is about 1.3 dB higher than the LNA only (Fig. 7) and have the same shape due to the reasons explained before, as shown in Fig. 12. This noise increase is mainly due to the filter MOS switches thermal noise and, assuming that the transistors are in triode region, its current can be expressed by $I_d^2(f) = (4kT)/r_{ds}$ [7]. As expected, the differential filter contributes with more noise compared with single-ended filter since it has more transistors on at the same time. Comparing the thermal noise expression with (2) and (4) is possible to conclude that if R_{SW} is raised the NF decreases but the filter effect is less noticeable (less amplification at ω_{LO} and less attenuation of undesired signals), as explained in section II-B, so there is a trade-off between the filter performance and NF.

Regarding the LNA input, the Fig. 13 shows that it is

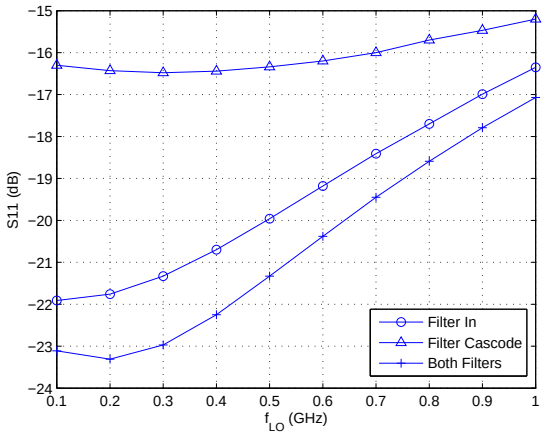


Fig. 13. LNA S_{11} at f_{LO}

matched to the antenna impedance for the entire LNA working band and using both filters $S_{11} < -17dB$ which is within the specifications for most applications.

Since the single-ended filter is in parallel with the LNA input its dimensions are limited to certain values because a very low R_{SW} will result in a low input impedance and consequently a poor matching for the frequencies near f_{LO}.

IIP2 and IIP3 simulations were made in order to understand the influence of the filtering in the even-order distortion and intermodulation problems. Two pure sinusoids were placed at the input of the LNA, one at f_{LO} and another at f_{LO} + 20 MHz. The LNA bandwidth is approximately 6 MHz as shown in table II.

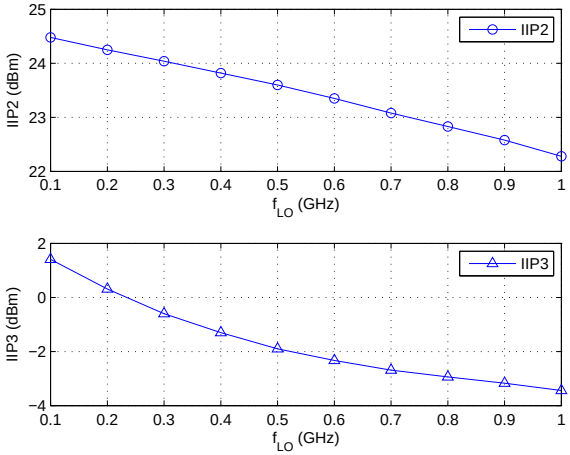


Fig. 14. LNA IIP2 and IIP3

As shown in Fig. 14 it was obtained an IIP2 $> +22$ dBm and an IIP3 > -4 dBm, which is within specifications for almost applications, for e.g. GSM and DVB-H [8].

V. Conclusion

In this paper we have analyzed the integration of high-Q BPFs in a balun-LNA. We demonstrate that is possible to attenuate the out-of-band interferers about 14 dB, with a minimum penalty in NF, reducing the voltage gain for the in-band frequencies less than 3 dB, comparing with the LNA. Regarding the intercept points we obtained IIP2 $> +$ 22 dBm and IIP3 $> -$ 4 dBm. Thus, it is possible to avoid the use of external filters at the input/output of LNA. We verified that exists a trade-off between the filters performance and the NF of the circuit therefore the filters should be projected according to the system specifications.

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