João Ricardo Carvalho Magalhães de Carvalho

Licenciado em ciências de engenharia eletrotécnica
e computadores

Design of a CMOS Amplifier for Breast Cancer Detection

Dissertação para obtenção do Grau de Mestre em
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Orientador: Prof. Doutor Luis Augusto Bica Gomes de Oliveira, FCT-UNL

Júri:

Presidente:	Prof. Doutor Pedro Miguel Ribeiro Pereira
Arguente:	Prof. Doutor João Pedro Abreu de Oliveira
Vogal:	Prof. Doutor Luis Augusto Bica Gomes de Oliveira

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I dedicate this thesis to my family and friends.

Acknowledgments

First I would like to thank my parents who have always been there for me, then I would like to thank professor Luis Oliveira for all the support and patience shown during this project.

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Resumo

Faculdade de Ciências e Tecnologia

Departamento de Engenharia Electrotécnica e de Computadores

Mestrado Integrado em Engenharia Electrotécnica e de Computadores

por João Ricardo Carvalho Magalhães de Carvalho

Nos detectores de radiação como o Positron tomography (PET), são utilizados amplificadores de transimpedância (TIA), que têm a função de transformar um sinal de corrente produzido por um fotodetector, num sinal de tensão com uma amplitude e forma desejada.

O amplificador de transimpedância deve ter o menor ruido possível, de forma a maximizar o sinal produzido. Nesta dissertação é proposta uma topologia de circuito onde é acrescentado um ramo auxiliar a entrada do conhecido TIA de feedback. No ramo auxiliar um bloco de transcondutância diferencial é utilizado para converter um sinal de entrada de tensão num sinal de corrente. Este sinal de corrente é em seguida convertida num sinal de tensão por um segundo amplificador de feedback, complementar ao primeiro, este sinal tem a mesma amplitude do produzido pelo ramo principal mas esta 180º fora de fase. Com este circuito o sinal de entrada do TIA aparece na saída como diferencial indo-se tirar partido deste facto para se tentar reduzir o ruido.

A topologia proposta é testada com dois dispositivos diferentes, o Foto díodo avalanche (APD), e o Fotomultiplicador de Sílico (SIPM). Das simulações concluímos que quando utilizamos o SIPM com Rx=20kΩ e Cx=50fF a relação sinal ruido aumenta, passando de 59 quando se usa apenas o feedback TIA, para 68.3 quando se utiliza o ramo auxiliar.

Os valores foram obtidos com um consumo total do circuito de 4.82mW. Apesar da relação sinal ruido ter melhorado no caso do SIPM, esta vem com um custo no consume total de energia.

Palavras chave

Fotodiodo avalanche (APD), Fotomultiplicadores de Sílico (SIPMs), Amplificadores de Transimpedância (TIA), Positron emission tomography (PET).

Abstract

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A transimpedance amplifier (TIA) is used, in radiation detectors like the positron emission tomography(PET), to transform the current pulse produced by a photo-sensitive device into an output voltage pulse with a desired amplitude and shape.

The TIA must have the lowest noise possible to maximize the output. To achieve a low noise, a circuit topology is proposed where an auxiliary path is added to the feedback TIA input, In this auxiliary path a differential transconductance block is used to transform the node voltage in to a current, this current is then converted to a voltage pulse by a second feedback TIA complementary to the first one, with the same amplitude but 180º out of phase with the first feedback TIA. With this circuit the input signal of the TIA appears differential at the output, this is used to try an reduced the circuit noise.

The circuit is tested with two different devices, the Avalanche photodiodes (APD) and the Silicon photomultiplier (SIPMs). From the simulations we find that when using s SIPM with Rx=20kΩ and Cx=50fF the signal to noise ratio is increased from 59 when using only one feedback TIA to 68.3 when we use an auxiliary path in conjunction with the feedback TIA.

This values where achieved with a total power consumption of 4.82mv. While the signal to noise ratio in the case of the SIPM is increased with some penalty in power consumption.

Keywords

Avalanche photodiodes(APD), Silicon photomultipliers (SIPMs), Transimpedance amplifier (TIA), Positron emission tomography (PET).

Contents

List of Figures

List of Tables

Abbreviations

APD	**A**valanche **P**hotodiode
ADC	**A**nalog-to-**D**igital **C**onverter
CS	**C**ommon **S**ource
CG	**C**ommon **G**ate
LNA	**L**ow **N**oise **A**mplifier
NF	**N**oise **F**igure
NMOS	**N**channel **M**etal-**O**xide-**S**emiconductor
OA	**O**perational **A**mplifier
PMOS	**P**channel **M**etal-**O**xide-**S**emiconductor
RCG	**R**egulated **C**ommon **G**ate
SIPM	**S**ilicone **P**hotomultiplier
TIA	**T**ransimpedance **A**mplifier
VCVS	**V**oltage **C**ontrolled **V**oltage **S**ource

Chapter 1

Chapter 1 Introduction

1.1 Motivation

Radiation detectors are used in medical imaging, nuclear science and optical fields. In this work the focus will be the use of radiation detectors in medical applications, for the detection of breast cancer, using positron emission tomography (PET).

Breast cancer is one of the leading causes of dead among women; one in eight women will develop breast cancer during their lives [1]. Earlier detection of breast cancer improves the chances of it being treatable, thus reducing the mortality rate [3].

The current standard method of detection for breast cancer is the x-ray mammography, this technique has some limitations, like the fact that in women with high breast density it becomes difficult to detect the presence of tumors [2] other limitation is the fact that a mammography is unable to distinguish between a benign or malign tumor, this leads to a excessive number of biopsies being done, the PET is a response to the limitations of the mammography [3].

The PET scanner main function is the detection of cancer cells, this is achieved by taking into account a biological particularity of the cancer cells, their metabolism is higher than that of a normal cell. This means cancer cells will need a bigger quantity of glucose to support their higher metabolism.

To detect these cells a patient is injected with ^{18}F-fluoro-deoxy-glucose (FDG) which is a glucose with radiation markers, this glucose is absorbed in greater quantity by the cancer cells, due to their higher metabolism, making their detection possible [3].

The radiation produced by the FDG is detected by the scintillating crystal at the front end of a radiation detector, this crystal transforms incident radiation in to a light pulse, this pulse is then detected by a light sensitive device such as an avalanche photodiode (APD) or a silicon photon multiplier (SIPM).

The light sensitive device converts the light pulse, produced by the scintillating crystal into a current pulse, this current pulse is then transformed into a voltage pulse by a transimpedance amplifier (TIA) with a desired amplitude and shape to be used by an analog to digital converter (ADC).

In Fig. 1.1 the full detection process is shown, from the moment when the scintillating crystal transforms incident radiation into a light signal, to when a transimpedance amplifier converts the current signal into a voltage pulse to be used by an ADC.

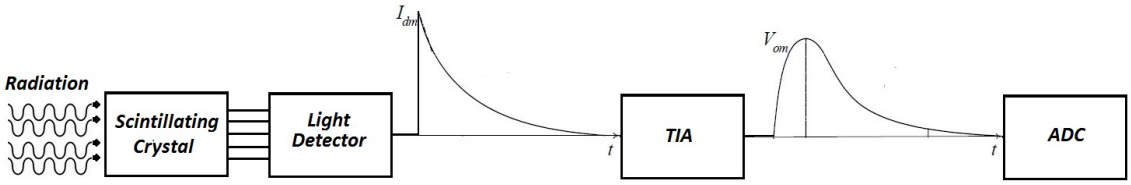

Figure. 1.1 - Radiation Detector

The most commonly used light detectors are the Avalanche Photodiodes (APD), recently a new type of photo detector emerged, the Silicon Photomultiplier(SIPM), this detector has several advantages over the APD, like, a much higher gain, and a lower biasing voltage [4], this advantages come with a cost, The SIPM have much higher capacitance than the APD, this makes the use of the existing TIAs with the SIPM problematic.

The amplitudes and peaking time of the voltage pulse, are limiting factors to the performance of the detector. If the amplitude of signal produced by the TIA is too low, or the peaking time too high, the detector is going to have a lower resolution. A lower resolution leads to an increase in the radiation dose needed to be administer, or a increase in the examination time, both of this option exposes the patient to a higher dose of radiation[5].

Due to what was described the transimpedance block is a limiting factor on radiation detectors.

1.2 Objectives

The objective of this thesis is design and test of a TIA circuit that is used to transform a current pulse generated by an APD and a SIPM in to a voltage pulse with a suitable amplitude and shape Fig. 1.2 producing the less amount of noise possible.

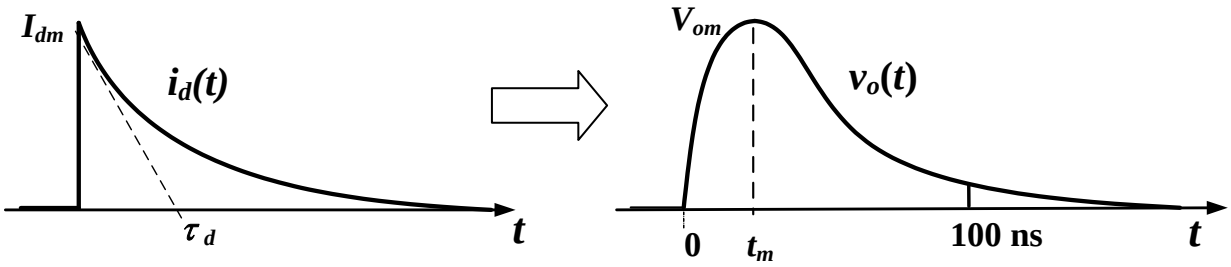

Figure. 1.2- TIA with input current pulse id and output pulse v0

From Fig. 1.2 we have I_{dm} the magnitude of the current pulse and τ_d the time constant, V_{om} the voltage pulse and t_m the peaking time of the voltage pulse.

In this work two light detectors are used in conjunction with the proposed TIA, the more widely used APD (Avalanche Photomultiplier) and the more recent SIPM (Silicon Photomultiplier). This is done to compare the signal to noise ratio we are able to achieve with the two detectors in conjunction with the proposed circuit.

The APD was assumed to have an input capacity $C_d = 10pF$, and current pulse amplitude of $I_d = 2.5\mu A$. The SIPM is considered to have an input capacity $C_d = 300pF$ and a current pulse amplitude of $I_d = 25\mu A$.

The output voltage pulse V_{out} should be above 300mV, the necessary voltage amplitude for the ADC, and the peaking time $t_p < 40$ns, this must be achieved with the lowest amount of power consumption possible while having low noise.

$$V_{out} > 300mV \tag{1.1a}$$

$$t_p < 40ns \tag{1.1b}$$

1.3 Thesis Organization

This thesis is divided in seven chapters, and, one appendix where noise equations for second order systems are deduced.

The first chapter starts with a small exposition of radiation detectors and the fields in which they are used, followed by the objectives and structure of this work, ending with a summary of the achieved results.

Chapter 2 consists of a brief overview of the function principles of photomultipliers, more specifically the APD (Avalanche Photomultiplier) and SPIM (Silicon Photomultiplier),

Chapter 3 is dedicated to the study of thermal noise in resistor and MOS transistors as well as flicker noise and noise cancelation.

On Chapter 4 two single stage amplifiers are study more specifically the Common-Source amplifier and the Common-Gate amplifier.

On Chapter 5 three existing TIA circuits are shown and, the feedback TIA, and the RCG TIA, for each one the transfer and noise function are deducted.

Chapter 6 is dedicated to the study of the proposed noise canceling circuit and its components, and the comparison between the use of and APD or a SIMP as the input photomultiplier.

Chapter 7 is where the make the final conclusions of the work done as well as plans for the future work that can be done in conjugation with was learned during this project.

1.4 Contributions

In this work it was shown that by using an auxiliary path on the feedback TIA we are able to reduce the signal to noise ratio of the feedback when using a SIPM from a signal to noise ratio of 59.3 to 68.3, this is achieved with a total circuit power consumption of 4.82mW.

CHAPTER 2

Chapter 2 Photon detection

2.1 Basics

The considered photo detectors have as the base a p-n junction photodiode, where an incident photon with sufficient energy generates a current pulse; this current is then used to measure the light passing through.

When a p-n junction photodiode is reversed biased, an electric field is created; this field causes the holes in the p-type and the electrons in the n-type material to move away from the junction, causing a widening in the depletion region Fig. 2.1.

When a photon of sufficient energy interacts with the field an electron-hole pair is created. The field created by the reverse bias forces the electron and the hole from the par to drift respectably to the n and p sides Fig. 2.1, this movement of the electrons and holes generates a flow of photocurrent in the external circuit [6].

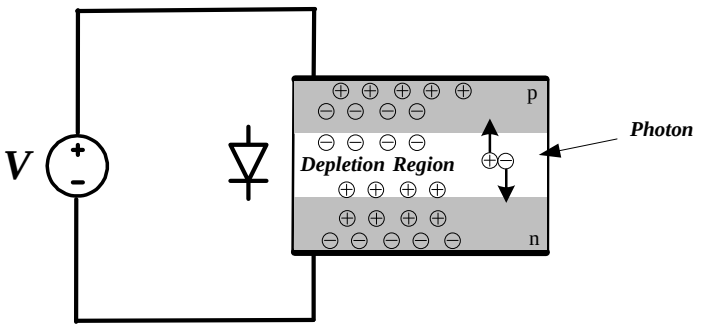

Figure. 2.1 - p-n photodiode

An electron-hole pair can also be created due to thermal variations, when this happens, a leakage current named dark current is created even when no light is present.

2.2.1-Avalanche Photodiodes (APD)

An APD is a p-n junction where the electric field is strong enough that a single charge carrier injected into the depletion layer, generates an electron-hole pair, that if created in the region of the strong electric field, has enough energy to generate another electron-hole pair by accelerating the electron or the hole with enough energy to impact in to the crystal lattice and through a process known as impact ionization generate another pair, thus generating an avalanche of secondary pairs [7].

This avalanche effect as two behaviors, one when the biased voltage is lower that the breakdown voltage, APD working in linear mode, and another then the biased voltage is higher that the breakdown voltage, the APD is working in Geiger mode.[7]

2.2.1.1- Linear Mode

If the biased voltage is lower that the breakdown voltage, the creation of new pair eventually starts to decline, because the rate at which new pair are created is lower than the rate at which they exit the high energy field region and are collected. This means that the number of pairs created by a single photon is limited to a fixed amount, for that reason the photocurrent generated is proportional to the incident flux of photons. In this mode of operation the internal gain is limited to M where M is the number of electron-hole pairs created on average by each absorbed photon and its value is in the order of tens or hundreds [7].

2.2.1.2- Geiger mode

In Geiger mode the biased voltage, is higher than breakdown voltage, this means that the electric field is so high that the avalanche created by a single charged carrier is self-sustaining. The rate at which new electro-hole pairs are created is higher than the rate a witch they are collected.

This self-sustaining avalanche causes a swift rise in the current .to the milliamp range in mere nanoseconds [8], Fig. 2.2 where the leading edge of the avalanche pulse marks the arrival time of the detected photon.

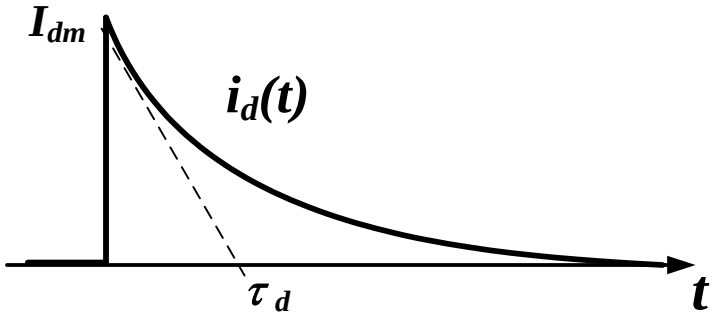

Figure. 2.2- Current Pulse

The current in a Geiger mode APD continues to flow until the avalanche is quenched by lowering the bias voltage to the same or below value of the breakdown voltage, this can be achieved using a resistance in series with the APD. As the current grows the voltage drop on the resistance causes the quenching of the APD. This effect reduces the voltage dropped across the high-field region, therefore slowing down the rate of growth of the avalanche, until a steady-state condition is reached where the bias voltage is decreased to the breakdown voltage, stopping the avalanche.

In Geiger-mode there is a chance that the avalanche stops early and photons go undetected, The number of electron-holes pairs created is typically higher that 10^7, much higher than in linear mode [7].

One problem with this type of APD is that they cannot be used to detected light. Intensity, the electrical pulse produced by the detection of one or more photons is indistinguishable; they can only be used to detect the presence of a light signal [8].

In this work a simplified model for the APD is used Fig. 2.3, this circuit is used to simulate the current pulse similar to the one in Fig. 2.2

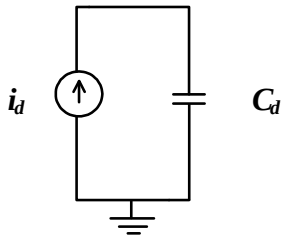

Figure. 2.3- APD simplified model

Where a current source i_d is in parallel with a capacitor C_d this basic circuit simulates the effects of an APD when the values of i_d and C_d are properly set. The values used where 2,5μA for the current source and 10pF for the capacitor.

2.2.2-Silicon Photomultipliers (SIPM)

SIPM are a recent and promising class of light sensors that are comprised of a series of self-quenching, Geiger-mode APD connected in parallel Fig. 2.3. [4],[9]

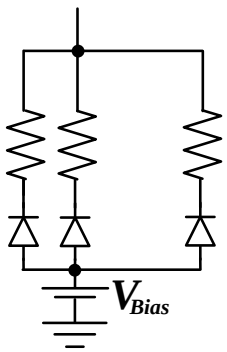

Figure. 2.4- Simplified SiPM structure

The parallel connection unlike the Geiger Mode APD allows the SIPM to carry information on light intensity. What makes this detectors so promising is its high quantum efficiency, the probability of a photon being absorbed in the active region of the device, the much higher gain when comparing with the linear APD, low bias voltage, insensitivity to magnetic fields, a good time resolution and a small size [9].

Similarly to the APD a simplified model of the SIPM is used, in the tests, this model is the same as the APD Fig. 2.2 but with different values. In the case of the SIPM we have for the current source $i_d = 25\,\mu\text{A}$ and for the capacitor $C_d = 300\text{pF}$ [10], this high value of C_d in conjunction with the high current pulse generated by the SIPM will complicate the use of existing TIA circuits.

CHAPTER 3

Chapter 3 Noise

Electronic noise is a random fluctuation in an electrical signal, these fluctuations are present in all electronic circuits, noise can be caused by physical phenomena due to the nature of the materials in use, or by external interferences.

Noise is random in nature, for that reason its instantaneous amplitude cannot be determined making its study somewhat difficult, while we cannot determine the noise amplitude, by observing noise signals for some time and using this data to create statistical models we are able to determine its average power [11],[12]

The presence of noise in electronic circuits is inevitable, for that reason it is important to analyze its impact on the degradation of the desired signals so that its effects can be minimized.

In this chapter the main noise sources in CMOS transistors are presented.

3.1 Thermal noise

Thermal noise, also called Jonhsom noise or Nyquist noise is the result of random thermal motion of charge carriers inside an electrical channel; this motion introduces a variation in the voltage measured across the conductor even when the average current is zero. The thermal noise power is proportional to the absolute temperature and can be quantified by,

$$P_{th} = kT\Delta f \tag{3.1}$$

where k is the Boltzmann constant, T the temperature in Kelvin and Δf the bandwidth of the system, to simplify it is assumed that $\Delta f = 1Hz$.

Resistor thermal noise can be modeled as a voltage source $\overline{v_n^2}$ in series with the resistor or a current source $\overline{i_n^2}$ in parallel as can be seen in Fig. 3.1.

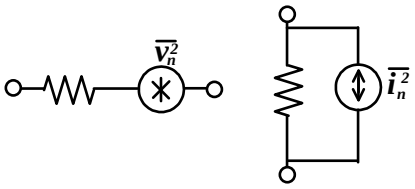

Figure. 3.1- Thermal noise resistor model

Where $\overline{v_n^2}$ and $\overline{i_n^2}$ are, respectively,

$$\overline{v_n^2} = 4KTR\Delta f, \tag{3.2}$$

$$\overline{i_n^2} = 4KT\frac{1}{R}\Delta f, \tag{3.3}$$

with the Boltzmann constant, $K = 1.38x10^{-23}\, J/K$ and T is assumed to be 300K.

Thermal noise in MOS transistors is also present due to carrier motion through the channel, thermal noise is the main source of noise in transistor, and can be modeled as a voltage source connected to the gate or a current source connected between the drain and source

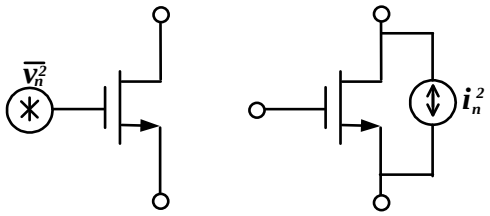

Figure. 3.2- MOSFET thermal noise model

If the transistors are operating in triode we have [13]

$$\overline{i_n^2} = 4KT\gamma g_{ds0}\Delta f, \tag{3.4}$$

$$\overline{v_n^2} = 4KT\gamma\frac{1}{g_{ds0}}\Delta f, \tag{3.5}$$

where g_{ds0} is the drain-source conductance and γ is the noise excess factor (NEF), which is 2/3, for long-channel MOSFET, in this work we assume that γ=1. In saturation $g_{ds} = g_m$ for that reason (3.4) and (3.5) can be written as [12]

$$\overline{i_n^2} = 4KT\gamma g_m \Delta f \tag{3.6}$$

$$\overline{v_n^2} = 4KT\gamma \frac{1}{g_m} \Delta f \tag{3.7}$$

where g_m is the transistor transconductance and γ is assumed to be 2/3 for long-channel transistors and higher for small submicron transistors.

3.2 Flicker Noise

Flicker noise in MOS transistors is caused by a physical phenomenon, this noise is believed to be caused by the imperfections on the interface between the gate oxide (SiO_2) and the silicon substrate (Si), this imperfections lead to charge carriers being randomly trapped and released causing the appearance of noise in the drain current.

This phenomenon is more prevalent at low frequencies, for this reason flicker noise is also called 1/f noise. Flicker noise is modeled as a voltage source in series with the gate and is given by [11]

$$\overline{v_n^2} = \frac{K}{C_{ox} W L} \frac{1}{f^c} \tag{3.8}$$

From (3.8) we have K that is a bias independent constant that varies with the technology in use, C_{ox} Is the gate oxide capacitance, W and L the width and length of the transistor. One way to reduce flicker noise is the use of a cleaner fabrication process; this reduces the value of K, thus reducing flicker noise. The exponent c varies between 0.7 and 1.2 but is usually closer to 1.

Flicker noise in p-channel devices is generally smaller than in n-channel devices of the same dimensions and fabricated with the same CMOS process, this is believed to be caused by the fact that in p-channel devices, the channel is farther away from the $Si - SiO_2$ interface, this decreases the likelihood of a charged carry being randomly trapped and released [12].

Flicker noise is still being actively studied, to better understand its origins, and how to better predict its appearance.

3.3 Noise Cancellation

RF receivers require LNAs with a sufficient large gain, a noise figure (NF) below 3 db, good linearity and a matching resistor that ensures impedance matching $Z_{IN} = R_S$,

The matching resistor on a LNA usually limits the achievable noise figure to 3dB, this matching resistor noise can be negated using a noise-cancelling LNA (NC-LNA), this is achieved by measuring the voltage at the RF node and the current passing through the matching resistor, as can be seen in Fig. 3.3 [14],[15].

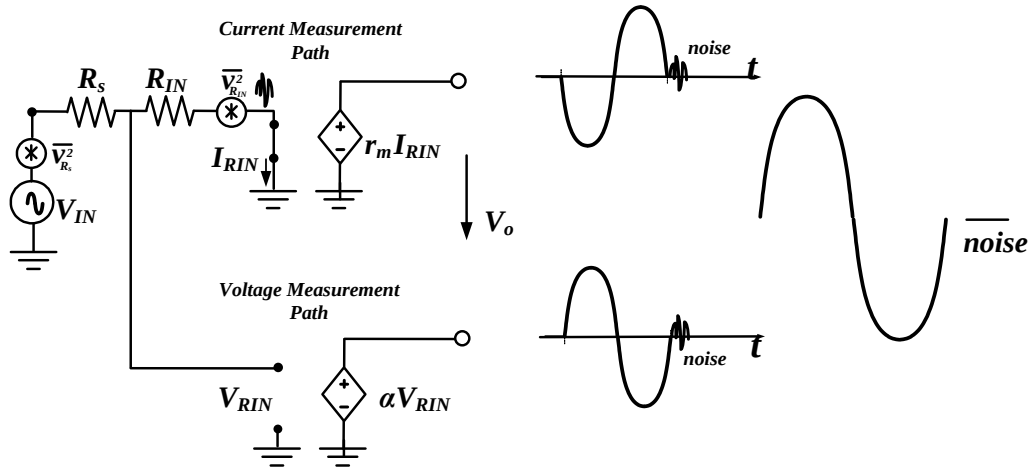

Figure. 3.3- Noise cancelling theory using.

The output signal of the NC-LNA of Fig. 3.3 is the difference between the voltage measurement path $\alpha V_{R_{IN}}$ and the current measurement path $-r_m I_{R_{IN}}$. knowing that the gain is

$$A_v = \frac{\alpha R_{IN} + r_m}{R_{IN} + R_S} \tag{3.9}$$

and the noise factor

$$F = 1 + \left|\frac{\alpha R_S - r_m}{\alpha R_{IN} + r_m}\right|^2 \frac{\overline{v_{R_{IN}}^2}}{\overline{v_{R_S}^2}} \tag{3.10}$$

If we set the relative gain of both the voltage measuring and current measuring paths so that we have

$$r_m = \alpha R_S \tag{3.11}$$

the input signal appears differential at the output while the matching resistor noise appears as common-mode. In Fig. 3.4 we can see the relation between the noise figure and the relative gain of the paths, when $r_m = \alpha R_S$ the noise figure equals zero.

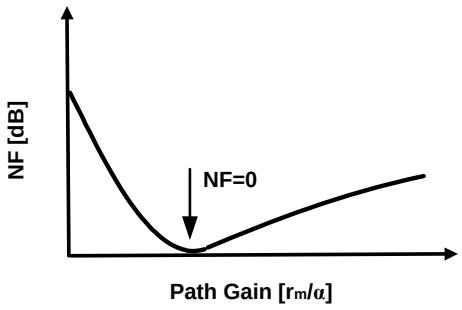

Figure. 3.4- Noise figure in relation with path gain.

In this work we have instead of a input resistance R_S a capacitance C_d.

CHAPTER 4

Chapter 4 Single stage MOS Amplifiers

4.1 Common Source Stage

The common-source amplifier Fig. 4.1 is a basic single-stage amplifier that converts variations in its gate-source voltage to a small drain current, this current flows through a resistor load to generate an output voltage, this stage as a high input and output impedance and voltage gain[11],[16].

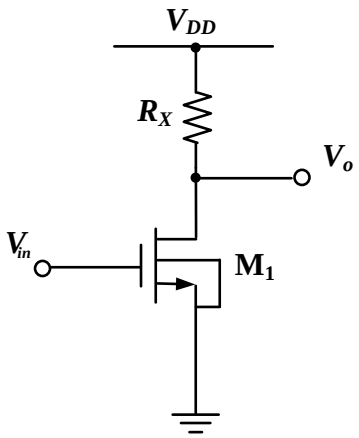

Figure. 4.1- Common Source amplifier with resistive Load

Since the bulk and source of the transistor are connected to the same voltage potential the body effect can be ignored during the study of the common-source.

4.1.1 Low frequency model neglecting r_0

First we are going to study the simplified low frequency model of the common-source where the transistor output impedance is neglected Fig. 4.2

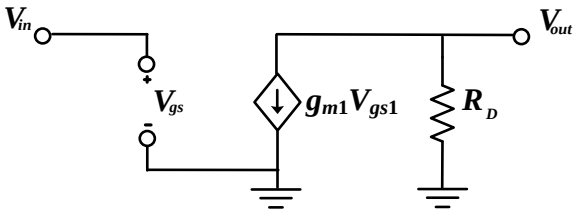

Figure. 4.2- Small-signal model of the Common-Source amplifier without r0

From the small-signal model we have

$$V_{out} = -g_m V_{in} R_D \tag{4.1}$$

From (4.1) the gain can be written as

$$A_s = \frac{V_{out}}{V_{in}} = -g_m R_D \tag{4.2}$$

4.1.2 Low frequency model with r_0

Now the small-signal model of the Common-Source amplifier taking into account r_0 Fig. 4.3 is analyzed

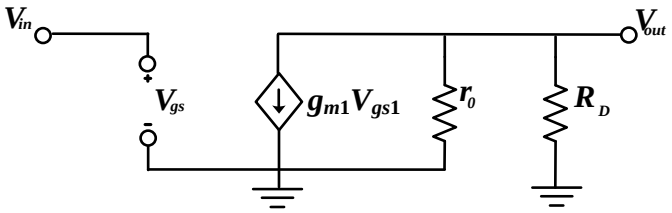

Figure. 4.3- Small-signal model of the common-source stage with r_0

From the circuit on Fig. 4.3 we can see that r_0 is in parallel with R_D so by using (4.2) and replacing R_D with the equivalent parallel resistance we obtain

$$A_s = \frac{V_{out}}{V_{in}} = -g_m(r_0 || R_D) \tag{4.3}$$

Replacing $r_0 || R_D$ we obtain

$$A_s = \frac{V_{out}}{V_{in}} = -g_m \frac{r_0 R_D}{r_0 + R_D} \tag{4.4}$$

4.2 Common Gate Stage

A Common-Gate amplifier produces an output at the drain by sensing the input signal at the source as can be seen in Fig. 4.4 [11],[16]. In addition to the gain the input impedance is also obtain for this amplifier.

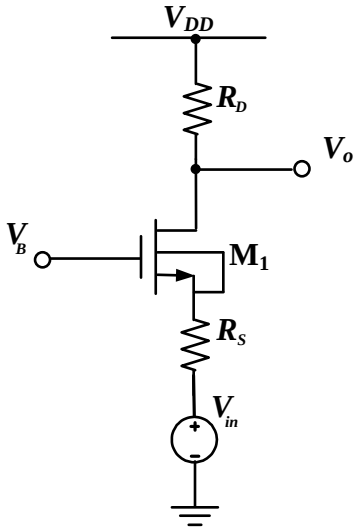

Figure. 4.4- Common Gate With Resistive Load

As was the case with the common-source amplifier we start by analyzing the simpler small-signal model of the common-gate without taking r_0 into account, from the circuit, we the equations of the gain and impedance. We then repeat the process for the circuit with r_0.

In the common-gate amplifier since the source is connected to a variable voltage source, and the bulk to a constant voltage source we have to take into account the body effect [16], the body effect is represented in the small signal model by an voltage controlled current source which depends on V_{bs} source-bulk voltage.

4.2.1 Low frequency model neglecting r_0

4.2.1.1 Gain

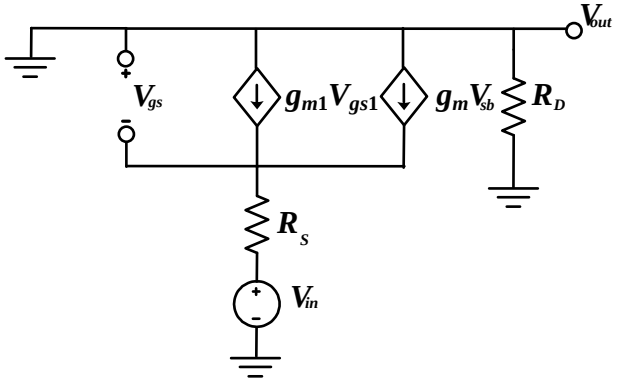

Figure. 4.5- Small signal model of the common-gate amplifier without r0

From Fig. 4.5 the current passing through R_s can be written as

$$i_s = -\frac{V_{out}}{R_D} \tag{4.5}$$

And

$$i_s = g_{m1}V_{gs} + V_{sb}g_{mb} \tag{4.6}$$

Since

$$V_{gs} = \frac{V_{out}}{R_D}R_S - V_{in} \tag{4.7}$$

If we replace (4.5) and (4.7) in (4.6) we obtain

$$A_v = \frac{V_{out}}{V_{in}} = \frac{(g_m + g_{mb})R_D}{(g_m + g_{mb})R_S + 1} \tag{4.8}$$

4.2.1.2 Input Impedance

In Fig. 4.6 it´s shown that the input impedance is viewed from the source of transistor

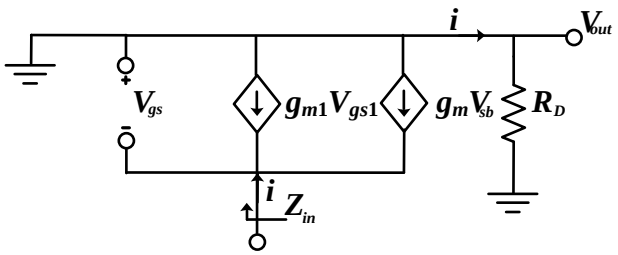

Figure. 4.6- Small signal model input impedance without r0

From Fig. 4.6 we can see that $V_{gs} = V_{in}$, for this reason (4.6) can be written as

$$i_s = V_{in}(g_{m1} + g_{mb}) \tag{4.9}$$

from (4.9) we can write Z_{in} as

$$Z_{in} = \frac{V_{in}}{i_{in}} = \frac{1}{(g_m + g_{mb})} \tag{4.10}$$

4.2.2 Low frequency model with r_0

4.2.2.1 Gain

The small-signal model of the Common-Source amplifier taking into account $r_0$can be seen in Fig. 4.7

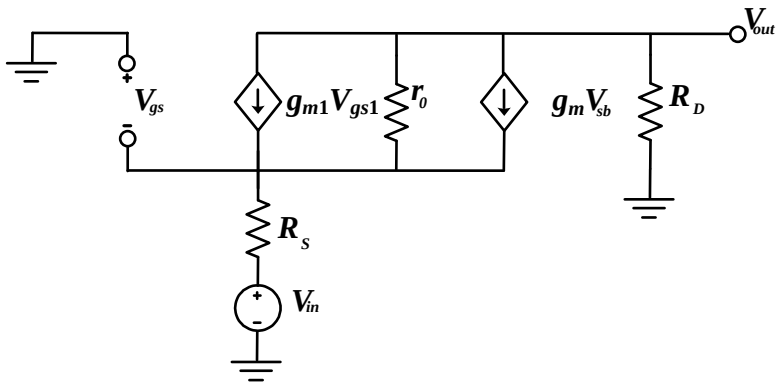

Figure. 4.7- Small signal of the common-gate amplifier with r0

From the circuit we can see that the current flowing through R_S is equal to the current flowing through R_D, so we have

$$i_s = -\frac{V_{out}}{R_D} \tag{4.11}$$

With i_s we can write V_{gs} as

$$V_{gs} = \frac{V_{out}}{R_D} R_S - V_{in} \tag{4.12}$$

Since the current through i_{ro} is equal to

$$i_{ro} = -\frac{V_{out}}{R_D} - V_{gs}(g_m + g_{mb}) \tag{4.13}$$

From the circuit V_{out} can be expressed as

$$V_{out} = r_0 i_{ro} + i_S R_S + V_{in} \tag{4.14}$$

Replacing (4.12) and (4.13) in (4.14) we have

$$\frac{V_{out}}{V_{in}} = \frac{(g_m + g_{mb})r_0 + 1}{r_0 + (g_m + g_{mb})r_0 R_s + R_s + R_D} R_D \tag{4.15}$$

4.2.2.2 Input Impedance

To obtain the impedance at the source taking into account r_0 we analyze the circuit of Fig. 4.8

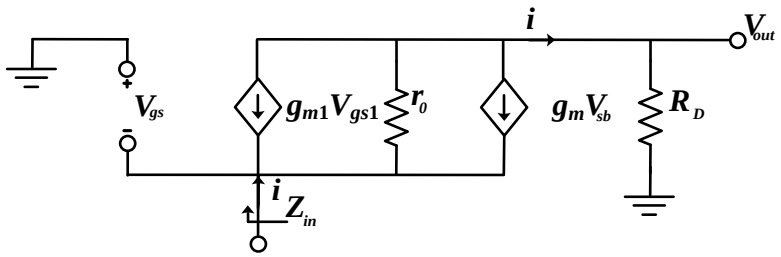

Figure. 4.8- Small signal model input impedance with r0

From the circuit in Fig. 4.8 we have that $V_{gs} = -V_{in}$ and since

$$V_{in} = R_D i_x + r_0 i_{ro} \tag{4.16}$$

with

$$i_{ro} = i_{in} + V_{gs}(g_m + g_{mB}) \tag{4.17}$$

we have

$$\frac{V_{in}}{i_{in}} = \frac{R_D + r_0}{1 + (g_m + g_{mb})r_0} \tag{4.18}$$

CHAPTER 5

Chapter 5 Transimpedance Amplifiers

In this chapter we are going to describe three existing types of transimpedance amplifiers used to transform the current signal produced by the APD or the SIPM into a voltage pulse with a suitable amplitude and shape. The circuits described n this chapter are; the feedback TIA, the Common Gate TIA and the Regulated Common Gate TIA.

5.1 Feedback TIA

The feedback TIA will be shown in a little more detail than the CG TIA and RCG TIA since this is the base of the proposed circuit.

The feedback TIA consists of an operational amplifier (OA) with a first order RC feedback loop as can be seen in Fig. 5.1.

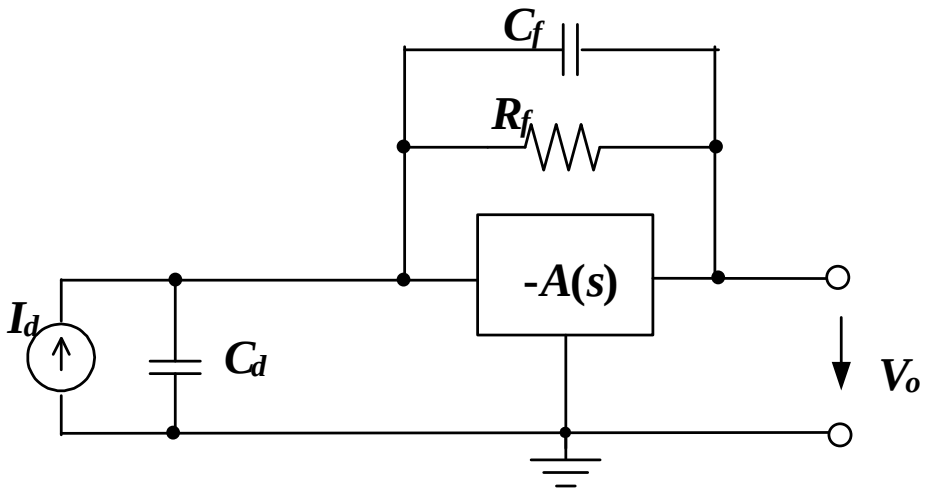

Figure. 5.1- Feedback TIA

5.1.1 Transimpedance function

If we assume that the OA present in the feedback is ideal, the transimpedance function is simply the feedback impedance Z_f [17],

$$Z_f(s) = \frac{V_o(s)}{I_d(s)}, \tag{5.1}$$

$$Z_f(s) = \frac{R_f}{1 + sR_fC_f}. \tag{5.2}$$

Since the first pole of the OA can be located close to the other poles of the circuit we cannot assume that the AO is ideal [18], for that reason the AO is assumed to have a dominant pole.

With a dominant pole the gain of the circuit can be written as

$$A(s) = \frac{A_0}{1 + s\tau_a} \tag{5.3}$$

where A_0 is the low-frequency gain of the OA and is assume to be much larger than one, $A_0 \gg 1$. We also know that the gain-bandwidth product of the OA is

$$B = \frac{A_0}{\tau_a} \tag{5.4}$$

From the circuit we have

$$V_0(s)\left(1 + \frac{1}{A(s)}\right)\left(\frac{1}{R_f} + sC_f\right) + \frac{V_0(s)}{A(s)} = I_d(s) \tag{5.5}$$

where

$$\frac{1}{A(s)} = \frac{1}{A_0} + sB^{-1} \tag{5.6}$$

and assuming that

$$A_0 \gg 1 \tag{5.7a}$$

$$C_d \gg C_f \tag{5.7b}$$

$$B^{-1} \gg R_fC_f \tag{5.7c}$$

we obtain [18],

$$\frac{V_0(s)}{I_d(s)} = \frac{R_f}{1 + sR_f\left(C_f + \frac{C_d}{A_0}\right) + s^2R_fC_dB^{-1}} \tag{5.8}$$

We have a two pole transimpedance function that can be written as

$$\frac{V_0(s)}{I_d(s)} = \frac{R_f}{(1+s\tau_1)(1+s\tau_2)} = \frac{R_f}{1+s(\tau_1+\tau_2)+s^2\tau_1\tau_2} \tag{5.9}$$

Comparing (5.9) with (5.8) we obtain

$$\tau_1 + \tau_2 = R_f\left(C_f + \frac{C_d}{A_0}\right) \tag{5.10a}$$

$$\tau_1\tau_2 = R_f C_d B^{-1}. \tag{5.10b}$$

Since τ_1 and τ_2 must be of the same order it is assumed that they are real an equal, with the same time constant. Since the proposed circuit is going to be tested with both an APD and a SIPM we are going to compare the two of them when using a feedback TIA.

When using an APD we have a low input capacitance $C_d = 10pF$ and a small current pulse $I_d = 2.5uA$. Making $R_f = 100k\Omega$ and $\tau_1 = \tau_2 = 10ns$ the minimum value needed to achieve the required peaking time, replacing the this values in (5.10a) and (5.10b), we easily obtain $\tau_1 = \tau_2 = 10ns$ with $C_f = 100fF$ and a $B^{-1} = 100ps$, both are acceptable values.

With the SIPM we have a much higher value of C_d, $C_d = 300pF$ and a smaller feedback resistance, $R_f = 100k\Omega$, replacing this values in (5.10b) for $\tau_1 = \tau_2 = 10ns$, we have $B^{-1} = 16ps$, this value of B is too small for the technology in use today, this means that then using a SIPM in conjunction with a feedback TIA, the time constant is going to be high.

. To allow for a higher value of *B* R_f can be lowered while maintaining the same pulse shape by using a second stage Voltage Controlled Voltage Source (VCVS) Fig. 5.2, with a voltage gain h. This second stage must be wide band enough to assure that the pulse shaping performed by the first stage TIA is not significantly affected.

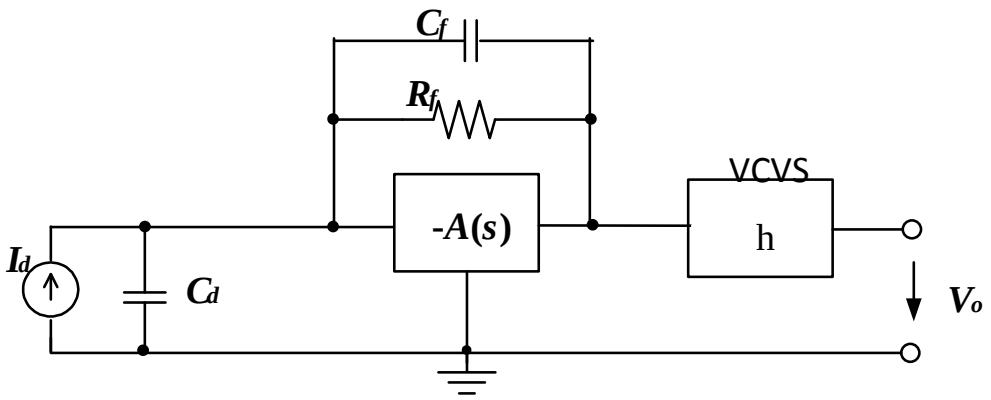

Figure. 5.2- Feedback with a VCVS

With the second stage VCVS (5.9) can be written as

$$\frac{V_0(s)}{I_d(s)} = \frac{R_m}{(1+s\tau_1)(1+s\tau_2)} \tag{5.11}$$

Where

$$R_m = hR_f \tag{5.12}$$

This method allows us to have a higher output voltage pulse while maintaining the same R_f.

5.1.2 Noise Analysis

The feedback TIA as two noise sources the OA and the resistor of the parallel RC circuit, the noise of the OA can be simulated as a voltage source at the input V_{na} and the noise generated by the resistor can be simulated by a current source I_{nf} in parallel with R_f, both noise sources can be seen in Fig. 5.3, Since we are going to use wideband TIAs flicker (or 1/f) noise is not considered.

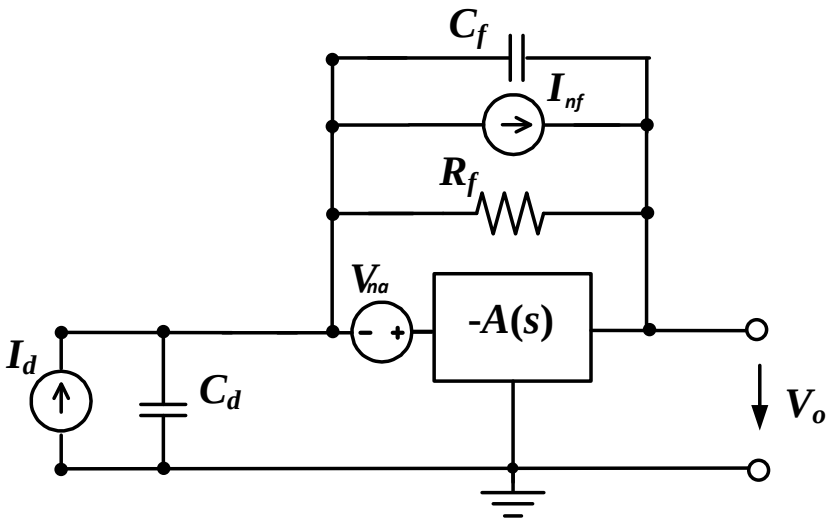

Figure. 5.3- Feedback TIA noise sources

5.1.2.1 Noise contribution of OA

The input transistor is assumed to be the dominant noise source of the OA, the spectral density of the input noise voltage of the OA $\overline{V_{na}^2}$ is

$$\overline{V_{na}^2} = 4KT\frac{\gamma}{g_{m\_in}} \tag{5.13}$$

Where g_{m_in} is the transconductance of the input transistor of the OA. First we are going to calculate the noise contribution of OA, for that reason we are going to ignore the current source I_{df} Fig. 5.3 while calculating the noise function N(s).

$$\left[V_0(s)\left(1+\frac{1}{A(s)}\right)+V_{na}(s)\right]\left(\frac{1}{R_f}+sC_f\right) = -sC_d\left(V_{na}+\frac{V_{no}}{A(s)}\right) \tag{5.14}$$

Assuming that

$$A_0 \gg 1 \tag{5.15a}$$

$$C_d \gg C_f \tag{5.15b}$$

$$B^{-1} \gg R_f C_f \tag{5.15c}$$

We have

$$N(s) = \frac{V_{no}(s)}{V_{na}(s)} = \frac{1 + sR_f C_d}{1 + sR_f\left(C_f + \frac{C_d}{A_0}\right) + s^2 R_f C_d B^{-1}} \tag{5.16}$$

N(s) has one zero and two poles and can be express as

$$N(s) = \frac{V_{no}(s)}{V_{na}(s)} = \frac{1 + s\tau_z}{1 + s(\tau_1 + \tau_2) + s^2\tau_1\tau_2} \tag{5.17}$$

Where

$$\tau_z = R_f C_d, \tag{5.18a}$$

$$\tau_1 + \tau_2 = R_f\left(C_f + \frac{C_d}{A_0}\right), \tag{5.18b}$$

$$\tau_1\tau_2 = R_f C_d B^{-1}. \tag{5.18c}$$

To obtain the rms output noise voltage equation (A.5) from the Appendix is used

$$V_{no\,rms}^2 = \frac{1}{\tau_1 + \tau_2}\left(1 + \frac{\tau_z^2}{\tau_1\tau_2}\right)\frac{1}{4}\overline{v_{na}^2} \tag{5.19}$$

From (5.18a) and (5.18c) we can write

$$\frac{\tau_z^2}{\tau_1\tau_2} = \frac{R_f^2 C_d^2}{B^{-1} R_f C_d} = \frac{R_f C_d}{B^{-1}} \tag{5.20}$$

Replacing (5.18b) and (5.20) in (5.19) and assuming $\gamma = 1$ we obtain

$$V_{no\,rms}^2 = \frac{R_f^2 C_d^2 kT}{gm(\tau_1 + \tau_2)\tau_1\tau_2} \tag{5.21}$$

When using an APD, assuming that $C_d = 10pF$, $R_f = 100k\Omega$,$\tau_1 = \tau_2 = 10ns$ and $gm = 5mS$ we obtain

$$V_{no\,rms} = 0.64mV$$

For the SIPM with that $C_d = 300pF$, $R_f = 20k\Omega$,$\tau_1 = \tau_2 = 10ns$ and $gm = 5mS$ we obtain

$$V_{no\,rms} = 3.86mV$$

5.1.2.2 Noise contribution of R_x

The noise generated by the resistor can be simulated by an current source I_{nf} in parallel with the resistor as can be seen in Fig. 5.3, where

$$\overline{i_{nf}^2} = 4kT\frac{1}{R_f} \tag{5.22}$$

The current source that simulates the noise produced by the resistor can be replace with two current sources Fig. 5.4. The current source that is connected to the output of the amplifier can be neglected since it is connected to a low impedance node [18], this means that we only have to consider the current source at the input, since this current source is in the same place as I_d the noise function can be written as

$$\frac{V_0(s)}{I_d(s)} = \frac{R_f}{(1+s\tau_1)(1+s\tau_2)} \tag{5.23}$$

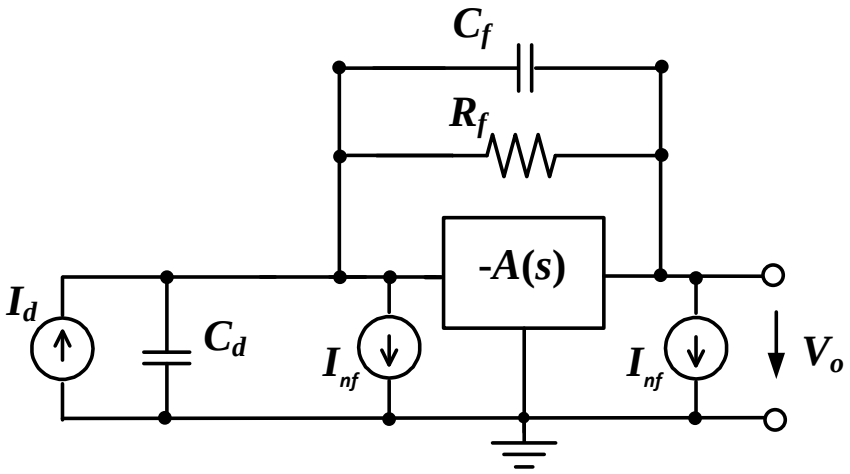

Figure. 5.4- Feedback TIA resistor noise

From the Appendix using equation (A.7) we have

$$V_{no\,rms}^2 = R_f^2\frac{1}{\tau_1+\tau_2}\frac{1}{4}\overline{i_{nf}^2} \tag{5.24}$$

replacing (5.22) on (5.24) we have

$$V_{no\,rms}^2 = R_f \frac{1}{\tau_1 + \tau_2} kT \tag{5.25}$$

When using an APD, assuming that $C_d = 10pF$, $R_f = 100k\Omega$,$\tau_1 = \tau_2 = 10ns$ and $gm = 5mS$ we obtain

$$V_{no\,rms} = 0.064mV$$

For the SIPM with that $C_d = 300pF$, $R_f = 20k\Omega$,$\tau_1 = \tau_2 = 10ns$ and $gm = 5mS$ we obtain

$$V_{no\,rms} = 0.144mV$$

The noise contribution of the resistors is very small in comparison to the noise of the OA, if we compare the two noise contribution we have

$$\frac{(v_{no\,rms}^2)_{OA}}{(v_{no\,rms}^2)_{R_f}} = \frac{\tau_z^2}{\tau_1 \tau_2} \frac{g_{m1}^{-1}}{R_f} \tag{5.26}$$

Replacing (5.20) on (5.26), assuming the use of an APD as the input with $g_{m1} = 5ms$ we get

$$\frac{(v_{no\,rms}^2)_{OA}}{(v_{no\,rms}^2)_{R_f}} = 20 \tag{5.27}$$

From (5.27) we can conclude than the noise contribution of the OA is dominant, for this reason, we are only going to take into account the noise generated by the OA in the feedback TIA.

5.2 Common Gate TIA

The Common-Gate TIA Fig. 5.5 is another type of TIA that can be used to transform the current pulse of a light sensitive device into a voltage pulse.

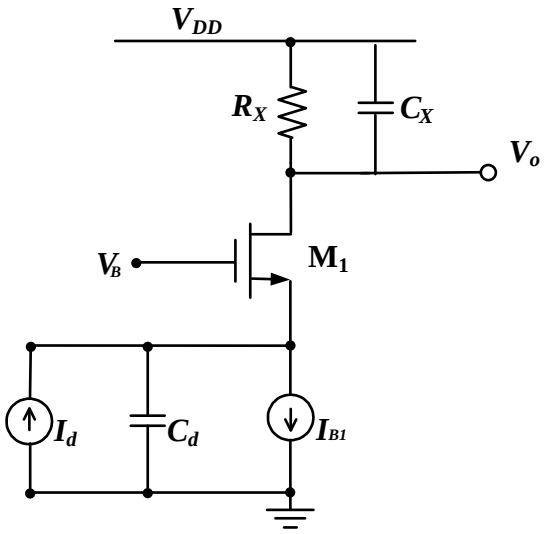

Figure. 5.5- Common Gate TIA

5.2.1 Transimpedance Function

Neglecting the body effect, the input impedance of the common-gate is approximately

$$Z_i \cong \frac{1}{g_{m1}} \tag{5.28}$$

from the circuit the current at the source of the transistor is [18]

$$I_s = -\frac{1}{1 + s g_{m1}^{-1} C_d} I_d \tag{5.29}$$

this current is the same as the one at the load impedance Z_x, this means that,

$$V_x = -I_s Z_x \tag{5.30}$$

with

$$Z_x = \frac{R_x}{1 + s R_x C_x} \tag{5.31}$$

Replacing (5.29) and (5.31) on (5.30) we obtain the transfer function,

$$\frac{V_0(s)}{I_d(s)} = \frac{R_x}{(1+sg_{m1}^{-1}C_d)(1+sR_xC_x)} = \frac{R_x}{(1+s\tau_1)(1+s\tau_2)} \tag{5.32}$$

From (5.32) we have two poles,

$$\tau_1 = g_{m1}^{-1}C_d \tag{5.33a}$$

$$\tau_2 = R_xC_x \tag{5.33b}$$

To keep the value of R_X low so as to keep the DC voltage drop in R_x low, a voltage post-amplifier can be connected to the output of the common-gate TIA as can be seen in Fig. 5.6, this amplifier would function in the same way as the one at the feedback TIA, by amplifying the output by a factor of h we can replace R_X for $R_m = hR_X$.

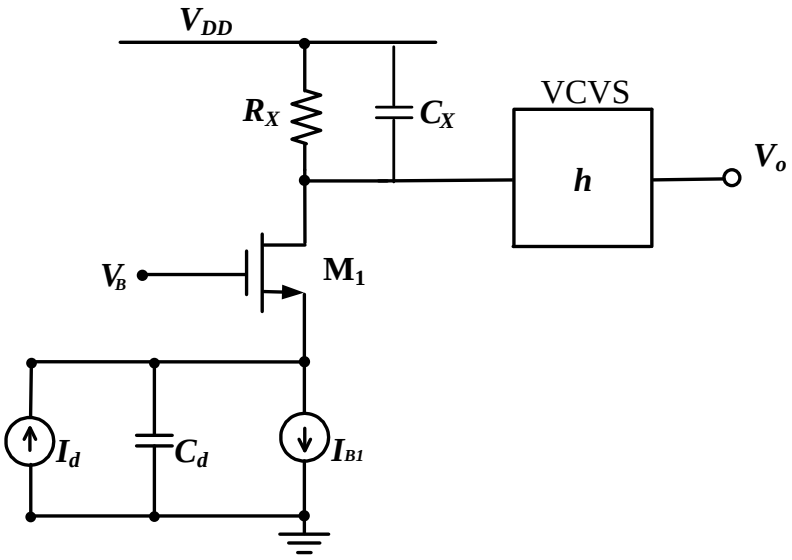

Figure. 5.6- Common-Gate with a voltage post-amplifier

With the post-amplifier the transfer is now

$$\frac{V_0(s)}{I_d(s)} = \frac{hR_x}{(1+sg_{m1}^{-1}C_d)(1+sR_xC_x)} \tag{5.34}$$

With a APD at the input we have $C_d = 10pF$ and $I_d = 2.5\mu A$ if we make $\tau_1 = \tau_2 = 10ns$ we obtain $g_{m1} = 1mS$ and we can use $C_X = 100fF$,$R_X = 100k$ with $h = 10$

Replacing the input APD by a SIPM means that now $C_d = 300pF$ and $I_d = 25\mu A$, for $\tau_1 = \tau_2 = 10ns$ we have $g_{m1} = 30mS$, this value of g_{m1} is too high for the current technology in use.

5.2.2 Noise Analysis

The Common-Gate TIA as three noise sources, the first one I_{B1} is the noise generated by the bias current source, the second one I_{n1} is the thermal noise generated by the M1 transistor, and finally I_{nX} represents the noise of the resistor R_X [19]. This three noise sources are shown in Fig. 5.7.

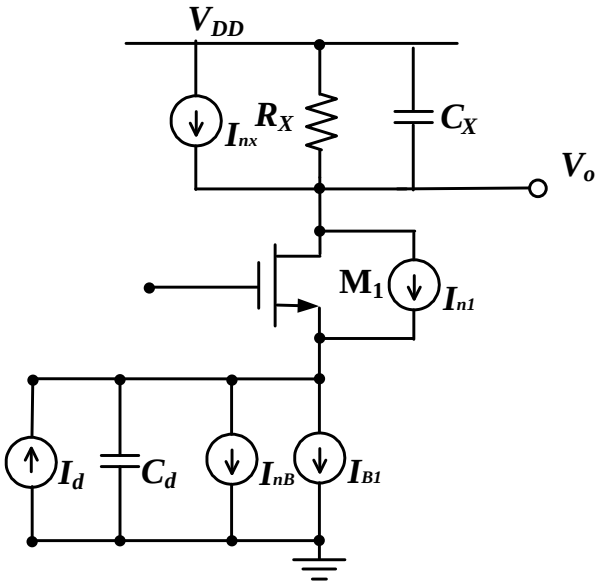

Figure. 5.7- Common Gate TIA noise sources

Where the respective spectral densities of each noise source are

$$\overline{i_{nX}^2} = 4kT\gamma R_x^{-1} \tag{5.35a}$$

$$\overline{i_{n1}^2} = 4kT\gamma g_{m1} \tag{5.35b}$$

$$\overline{i_{nB}^2} = 4kT\gamma g_{mB} \tag{5.35c}$$

Assuming that the MOS transistors noise coefficient is γ=1, and assuming that the bias current source I_{nB} is replaced by a transistor with a constant value of V_{gs} and g_{mb} transconductance, we have from [19] that for

5.2.2.1 Noise contribution of I_{nx}

In the case of I_{nx} we have

$$\frac{V_{no}}{I_{nX}} = \frac{hR_x}{\tau_2} \tag{5.36}$$

From equation (A.9) we have

$$V_{no\,rms}^2 = \frac{R_x kT}{\tau_2} \tag{5.37}$$

The noise generated by R_X cannot be minimized because it consists only of variables used to determine the circuit time constants.

5.2.2.2 Noise contribution of I_B

In the case of I_{nB} since it is in the same position as I_D we can use equation (5.32)

$$\frac{V_0(s)}{I_d(s)} = \frac{R_x}{(1+s\tau_1)(1+s\tau_2)} \tag{5.38}$$

in this case we have a two pole, using equation (A.7) and (5.35c) we have

$$V_{no\,rms}^2 = \frac{R_x^2 kT\, g_{mB}}{(\tau_1+\tau_2)} \tag{5.39}$$

where τ_1 and τ_2 are respectably (5.33a) and (5.33b). In this case the noise can be reduced by using a small value of g_{mB}, since this is the only variable on (5.39) that we can change without affecting the circuit time constant.

5.2.2.3 Noise contribution of I_{n1}

To calculate the noise contribution of I_{n1} the incremental circuit of Fig. 5.8 is used, there we have the incremental resistance of the bias current source R_{oB} and the transistor model resistance r_{o1}.

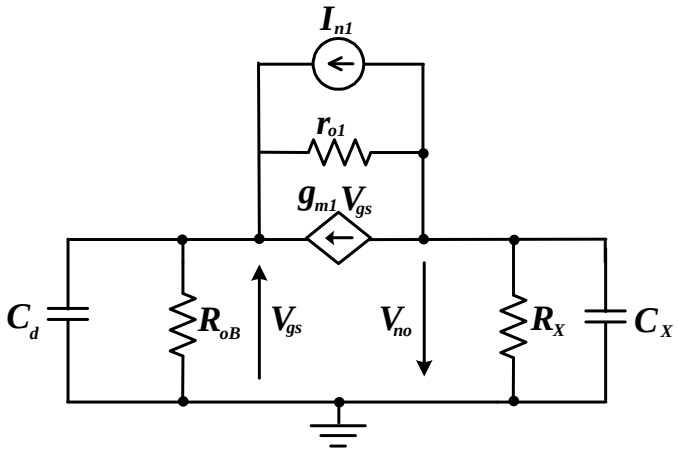

Figure. 5.8- Small signal model of the CG with I_{n1} noise source

Taking into account that $g_{m1} \gg r_{o1}^{-1}$ and $g_{m1} \gg R_{oB}^{-1}$ and assuming that $R_X r_{01}^{-1} \ll 1$ we have [19]

$$\frac{V_{n0}(s)}{I_{n1}(s)} = -\frac{R_X}{g_{m1}R_{oB}} \frac{1+s\tau_z}{(1+s\tau_1)(1+s\tau_2)} \tag{5.40}$$

Using equation (A.5) and knowing that $\tau_z = R_{oB}C_d$ and $\tau_z \gg \tau_1\tau_2$ we have

$$V_{no\ rms}^2 = \frac{R_x^2 C_d^2 kT}{g_{m1}(\tau_1 + \tau_2)\tau_1\tau_2} \tag{5.41}$$

From (5.28) the only way to minimize the noise contribution of I_{n1} is by increasing the value of g_{m1} but because of (5.35a) we are not free to change it without also changing the time constant.

5.3 Regulated Common Gate

The regulated Common-Gate TIA was developed as a response to the shortcomings of the common-gate TIA. The RCG TIA can be described as a common-gate stage (transistor M_1, with bias current $I_{B1}$and load resistor R_x), with a voltage amplifier with gain A (common-source transistor $M_2$with active load I_{B2}) Fig. 5.3 [19].

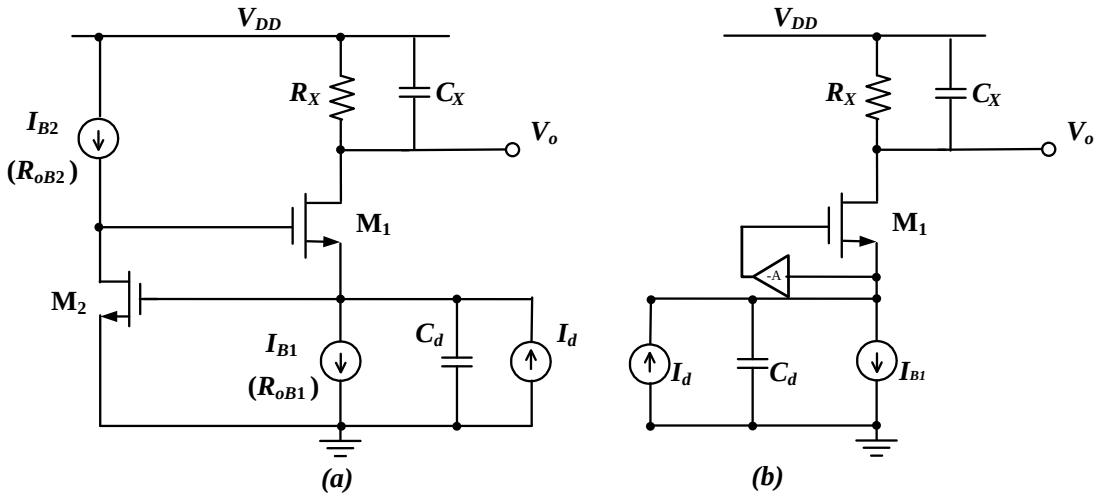

Figure. 5.9- Regulated Common Gate

In Fig. 5.9a we can see the RCG circuit and in Fig. 5.9b a simplified version where the feedback loop created by the extra voltage gain stage can be easily seen.

5.3.1 Transimpedance Function

We can see on Fig. 5.3b that the common-source transistor M_2 with active load I_{B2} is an amplifier stage with voltage gain A [19]

$$A = g_{m2}(r_{02}||R_{oB2}) \tag{5.42}$$

Where R_{oB2} is the incremental resistance of the load I_{B2} . The input impedance can be written as

$$Z_i = \frac{1 + Z_x/r_{01}}{(A+1)g_{m1}} \tag{5.43}$$

If we take into account that

$$g_{m1} \gg r_0^{-1} \tag{5.44a}$$

$$A \gg 1 \tag{5.44b}$$

$$|Z_x| \ll r_{01} \tag{5.44c}$$

(5.43) Can be simplified to

$$Z_i = \frac{1}{A g_{m1}} \tag{5.45}$$

From Fig. 5.9 since the input current I_d is divided between C_d and the input impedance we have for the incremental source current of M_1 [18]

$$I_{s1} = \frac{g_{m1}}{g_{m1}A + sC_d} = \frac{1}{1 + s\tau_1} I_d \tag{5.46}$$

This current flows through

$$Z_x = \frac{R_x}{1 + s\tau_2} \tag{5.47}$$

So from (5.46) and (5.47) we have

$$\tau_1 = \frac{C_d}{g_{m1}A} \tag{5.48a}$$

$$\tau_2 = R_x C_x \tag{5.48b}$$

The transimpedance function is then [18]

$$\frac{V_0}{I_d} = \frac{R_x}{\left(1 + s\frac{C_d}{g_{m1}A}\right)(1 + sR_xC_x)} = \frac{R_x}{(1 + s\tau_1)(1 + s\tau_2)} \tag{5.49}$$

The advantage of this circuit when comparing with the CG is that now τ_1 doesn't rely exclusively on g_{m1}, this means that for a maximum value of $A = 100$ we can have a much smaller g_{m1} while maintaining the same time constant.

With a SIPM at the input $C_d = 300pF$ and $I_d = 25\mu A$, and $A = 100$ for $\tau_1 = \tau_2 = 10ns$ we now have $g_{m1} = 0.3mS$ which is an acceptable value.

5.3.2 Noise Analysis

In the RCG TIA we consider the thermal noise generated by transistor M_1, M_2 and the noise generated by the bias current sources I_{B1}, I_{B2}, due to the wideband nature of the TIA in use, flicker (1/f) noise is neglected [18]. The noise contribution of resistor R_X is also neglected since the parasitic capacitance in parallel is assumed to make it non-dominant. The noise sources are shown in Fig. 5.10.

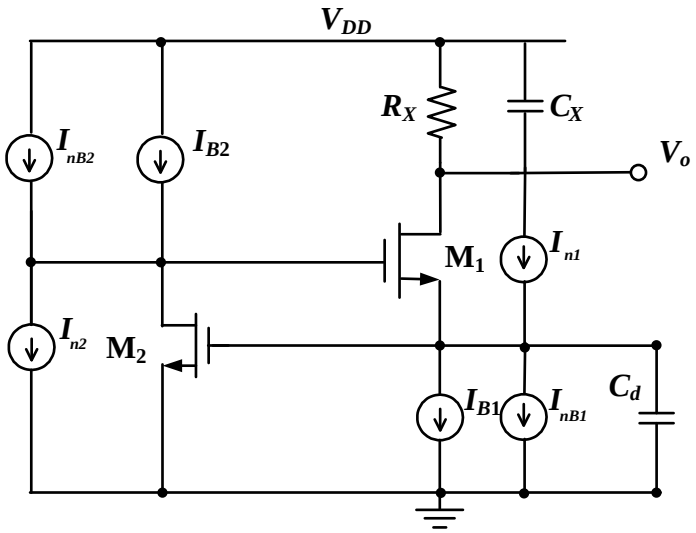

Figure. 5.10- RCG TIA incremental circuit with noise sources.

The spectral densities of the noise sources are

$$\overline{i_{n1}^2} = 4kT\gamma g_{m1} \tag{5.50a}$$

$$\overline{i_{n2}^2} = 4kT\gamma g_{m2} \tag{5.50b}$$

$$\overline{i_{nB1}^2} = 4kT\gamma g_{mB1} \tag{5.50c}$$

$$\overline{i_{nB2}^2} = 4kT\gamma g_{mB2} \tag{5.50d}$$

The equivalent noise circuit with the noise sources can be seen in Fig. 5.11.

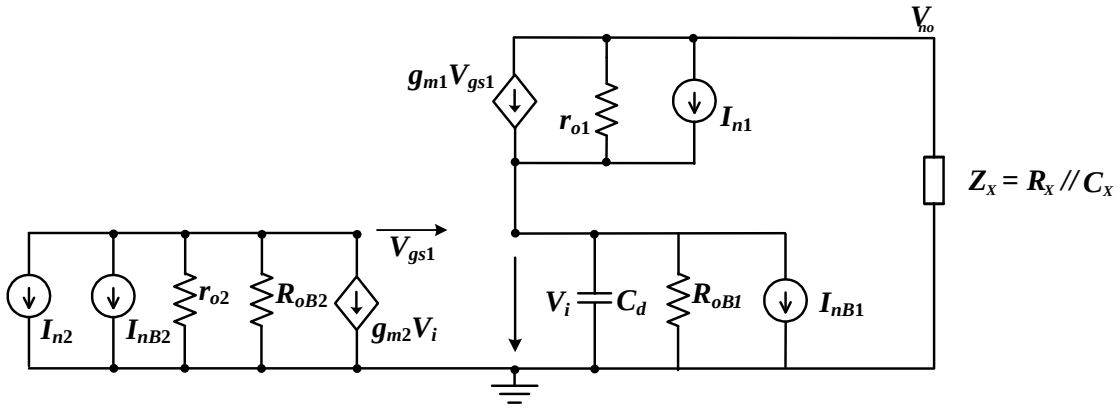

Figure. 5.11- Small signal model of the RCG with noise sources

5.3.2.1 Noise contribution of $\boldsymbol{I_{n1}}$

For the noise I_{n1} [18] assuming that

$$g_{m1}AR_{oB1} \gg R_X//r_{o1} \tag{5.51a}$$

$$g_{m1}AC_x \gg \frac{C_d}{r_{o1}} \tag{5.51b}$$

$$g_{m1}AR_{oB1} \gg 1 \tag{5.51c}$$

We have

$$\frac{V_{n0}(s)}{I_{n1}(s)} = \frac{R_X}{g_{m1}AR_{oB1}} \frac{1+s\tau_z}{(1+s\tau_1)(1+s\tau_2)} \tag{5.51}$$

Where

$$\tau_z = R_{oB1}C_d \tag{5.52}$$

With τ_1 and τ_2 from (5.48a) and (5.48b)

Using (A.5) on (5.51) to obtain the rms output noise voltage due to the common gate transistor noise we have

$$V_{no\,rms}^2 = \frac{R_x^2}{A^2 g_{m1}^2 R_{oB1}^2}\left(1+\frac{\tau_z}{\tau_1+\tau_2}\right)\frac{\tau_z^2}{\tau_1\tau_2}\frac{1}{4}\overline{i_{n1}^2} \tag{5.53}$$

Replacing (5.50a) and (5.52) on (5.54) and considering that $\tau_z \gg \tau_1\tau_2$ we obtain

$$V_{no\,rms}^2 = \frac{R_x^2 C_d^2 kT}{A^2 g_{m1}(\tau_1+\tau_2)\tau_1\tau_2} \tag{5.54}$$

5.3.2.2 Noise contribution of $\boldsymbol{I_{n2}}$

For the noise source I_{n2} we have [18]

$$\frac{V_{n0}(s)}{I_{n2}(s)} = \frac{R_X}{g_{m2}R_{oB1}} \frac{1+s\tau_z}{(1+s\tau_1)(1+s\tau_2)} \tag{5.55}$$

With τ_z, τ_1 and τ_2 from (5.52) (5.48a) and (5.48b), respectively

Using equation (A.5) the rms noise voltage due to M_2 is

$$V_{no\,rms}^2 = \frac{R_x^2}{g_{m2}^2 R_{oB2}^2}\frac{1}{\tau_1+\tau_2}\left(1+\frac{\tau_z^2}{\tau_1\tau_2}\right)\frac{1}{4}\overline{i_{n1}^2} \tag{5.56}$$

Replacing (5.52) and (5.50b) on (5.56) and considering that $\tau_z \gg \tau_1\tau_2$ we obtain

$$V_{no\ rms}^2 = \frac{R_x^2 C_d^2 kT}{g_{m2}(\tau_1+\tau_2)\tau_1\tau_2} \tag{5.57}$$

The noise contribution of I_{n2} can be decreased, by increasing the value of g_{m2}

5.3.2.1 Noise contribution of $\boldsymbol{I_{B1}}$

For the noise source I_{B1} since it is in the same place as I_d we use (5.49). Using equation (A.7) on (5.49) we obtain

$$V_{no\ rms}^2 = R_x^2 \frac{1}{\tau_1+\tau_2}\frac{1}{4}\overline{i_{nB1}^2} \tag{5.58}$$

Replacing (5.50c) on (5.58) we obtain

$$V_{no\ rms}^2 = \frac{R_x^2 kT g_{mB1}}{\tau_1+\tau_2} \tag{5.59}$$

5.3.2.1 Noise contribution of $\boldsymbol{I_{B2}}$

For the noise I_{B2} since it is in the same place as I_{n2} we use (5.55). Using equation (A.5) on (5.55) we obtain,

$$V_{no\ rms}^2 = \frac{R_x^2}{g_{m2}^2 R_{oB1}^2}\frac{1}{\tau_1+\tau_2}\left(1+\frac{\tau_z^2}{\tau_1\tau_2}\right)\frac{1}{4}\overline{i_{nB2}^2} \tag{5.60}$$

Replacing (5.52) and (5.50d) on (5.60) and considering that $\tau_z \gg \tau_1\tau_2$ we obtain

$$V_{no\ rms}^2 = \frac{g_{mB2} R_x^2 C_d^2 kT}{g_{m2}^2(\tau_1+\tau_2)\tau_1\tau_2} \tag{5.61}$$

To reduce the noise generated by I_{B2} we need to increase the ratio between g_{mB2} and g_{m2}

CHAPTER 6

Chapter 6 Proposed Circuit

In this chapter the proposed circuit is presented and studied, we start with a brief introduction to the circuit, then we deduce the transfer and noise function of the circuit, this is followed by the simulations results, where the circuit is tested with an APD and a SIPM at the input, the results are then compared with the known feedback circuit.
Finally the APD and the SIPM are compared with each other when in use with the same feedback values.

6.1 Feedback TIA with Auxiliary Path

The circuit in study consists of two feedback TIAs connected at the input with one of then having a extra transconductance block. The objective of this work is to, try and reduce the noise produced by the TIA, when used in conjunction with a photo-detector, by adapting a noise canceling circuit used in RF circuits,

This circuit has two path, the main path where we have a simple feedback TIA and an auxiliary path where a Gm block inverts the input voltage signal produced by the APD or SIPM into a current signal, this signal is then converted back to a voltage signal by a second feedback TIA complementary to the one presented on the main path, this results in a signal with the same amplitude but 180º out of phase [15]. During this work we will refer to the feedback TIA without the transconductance block as the main path and the TIA with the transconductance block at the input as the auxiliary path

In Fig. 6.1 the proposed circuit is shown, there the two paths the main an auxiliary path can easily be distinguished by the transconductance block on the auxiliary path

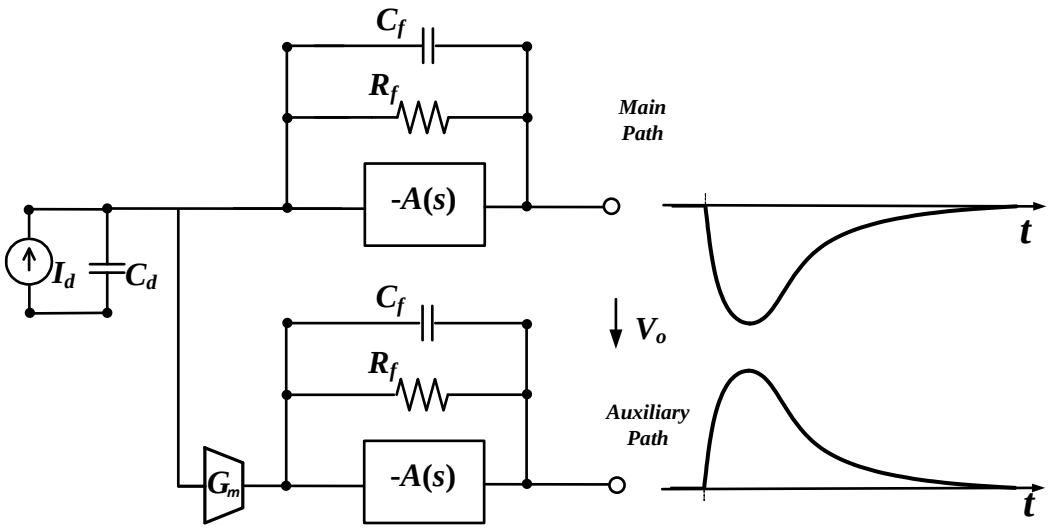

Figure. 6.1- Proposed circuit.

The transconductance block GM in Fig. 6.1 is in its simplest form a Class-AB CMOS inverter, as can be seen in Fig. 6.2, this block is used to invert the phase of the input signal by 180º without adding gain. In this circuit the voltage measurement is provided by the auxiliary path and the current measurement by the main path.[15]

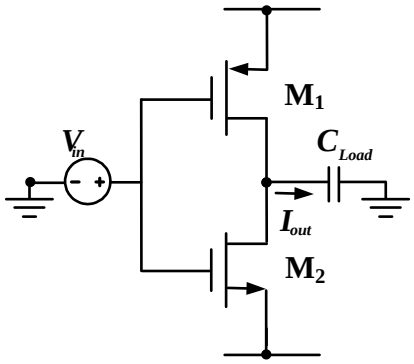

Figure. 6.2- Class-AB CMOS inverter

From Fig. 6.2 I_{out} can be written as

$$I_{out} = V_{in} g_m \tag{6.1}$$

The full GM circuit used in this work consists of six CMOS inverters, Inv1 trough Inv6. In this circuit the basic V-I conversion is performed by Inv1 and Inv2 and the network of Inv3 trough Inv6 functions as a low-ohmic load for common signals and a high-ohmic load for differential signals, this results in a controlled common-mode voltage level of the output. If the four inverters have the same supply voltage and are perfectly matched, all gm`s are equal.[15]

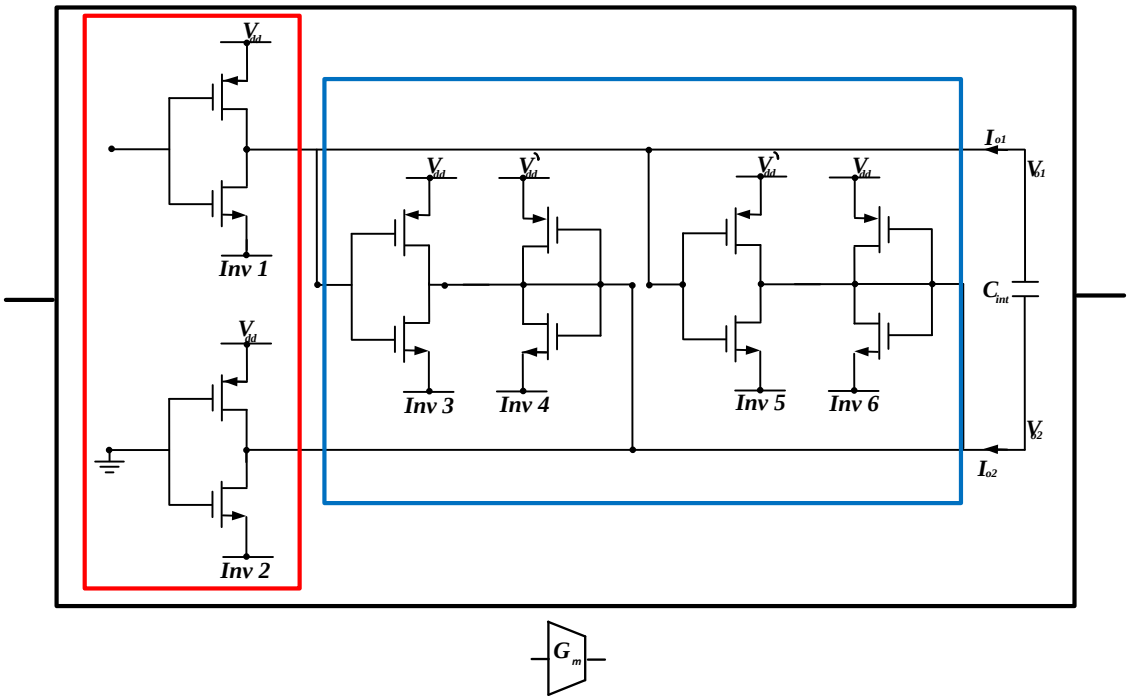

Figure. 6.3- Complete Transconductance element of the auxiliary path

The circuit shown in Fig. 6.3 as no internal nodes and has a good linearity in V-I conversion if the β factors of the n-channel and p-channel transistors are perfectly matched. [20]

The output differential current of the circuit Fig. 6.3 is

$$I_{out} = V_{in} g_{md} \tag{6.1}$$

Where $g_{md} \approx g_{m3} \approx g_{m4}$

For differential output signals V_{01} and V_{02} are virtually loaded with

$$R_{o1} = \frac{1}{gm_5 - gm_6} \tag{6.2a}$$

$$R_{o2} = \frac{1}{gm_5 - gm_6} \tag{6.2b}$$

And for common mode output signals

$$R_{o1} = \frac{1}{gm_5 + gm_6} \tag{6.3a}$$

$$R_{o2} = \frac{1}{gm_5 + gm_6} \tag{6.3b}$$

If Inverters 3 through 6 are perfectly matched and are supplied by the same voltage, they form a low-ohmic load for common-mode signals and a high-ohmic load for differential signals, this results in a controlled common-mode voltage level at the output.

The dc gain of the transconductor can be increased by loading the differential inverters Inv1 and Inv2 with a negative resistance, this can be achieved by making $g_{m3} = g_{m6} > g_{m4} = g_{m5}$, simply by making the width of Inv 4,5 slightly smaller than that of Inv 3,6. This negative resistance can be implemented without adding extra nodes to the circuit, this can be used to adjust the gain of GM to ensure that the input and output signals are as equal as possible. [20]

6.2 transfer function

We have for the main and auxiliary path the same transfer function as the one from the feedback TIA studied in chapter 3 but with opposite signs, assuming that the transconductance block inverts the phase by 180º without adding gain or adding internal nodes.

For the main path we have as was seen in chapter 5

$$\frac{V_0(s)}{I_d(s)} = -\frac{R_{fmain}}{1 + sR_{fmain}\left(C_{fmain} + \frac{C_d}{A_0}\right) + s^2 R_{fmain} C_d B^{-1}} \tag{6.2}$$

By comparison the transfer function of the auxiliary path is going to be equal but with a different sign

$$\frac{V_0(s)}{I_d(s)} = \frac{R_{f\text{auxiliary}}}{1 + sR_{f\text{auxiliary}}\left(C_{f\text{auxiliary}} + \frac{C_d}{A_0}\right) + s^2 R_{f\text{auxiliary}} C_d B^{-1}} \tag{6.3}$$

Combining the paths we obtain

$$A_T = A_{AUX} - A_{MAIN} \tag{6.4}$$

This means that when using this circuit we have double the voltage gain while using the same values as where used in the feedback TIA.

One problem with this circuit is the fact that it still relays on the feedback TIA, this means that we are still subject to the same limitations as was the case with feedback TIA studied in chapter 5, this means that when dealing with a SIPM at the input, the value of GBW necessary to achieved the required conditions is hard to achieve.

6.3 Noise Function

From [18] we know that the noise effect of the transconductance block on the main path is

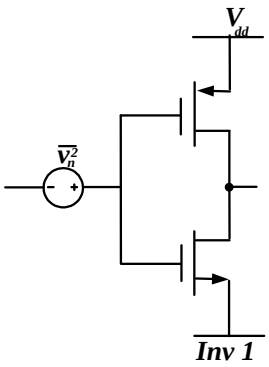

Figure. 6.4- Inverter noise contribution to the main path

Where

$$\overline{V_{ngm}^2} = 4KT\frac{\gamma}{g_{mPMOS} + g_{mNMOS}} \tag{6.5}$$

From [19] we now that the differential output noise of the transconductor of Fig. 6.3 is

$$\overline{I_{ngm}^2} = 4KT\gamma g_{mtotal} \tag{6.6}$$

Where g_{mtotal} is the total sum of all the transconductances of the six inverters present on the GM block, this will later be proven problematic when dealing with an APD an its low current pulse amplitude. The total noise sources of the full circuit can be seen in Fig. 6.5.

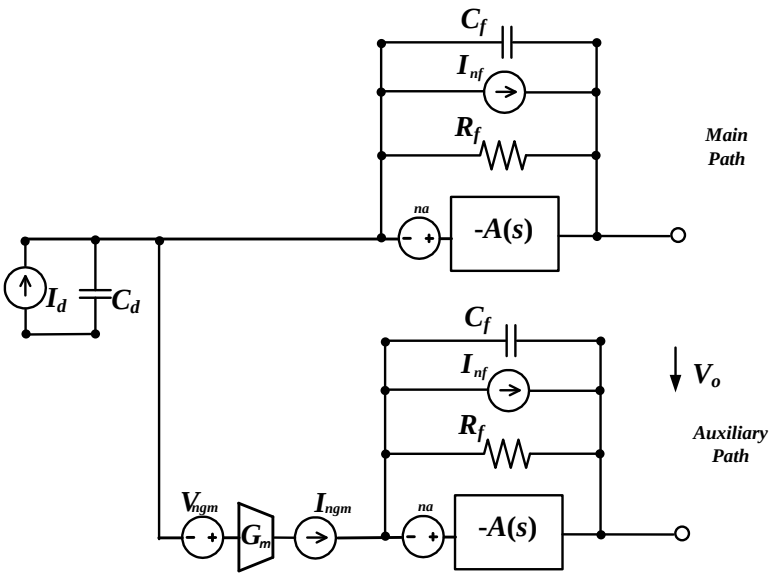

Figure. 6.5- Full circuit noise sources

6.3.1 Main path noise

In the main path we have as noise sources the GM block, the OA noise and the feedback resistor, as was shown in chapter 5 the feedback resistor can be ignored, since in the feedback TIA the noise caused by the OA is dominant, this leaves us with only the need to calculate the noise contribution of the OA and the GM

6.3.1.1 Noise contribution of GM

We start by calculating the noise impact of V_{ngm} on the main path, for that reason the other noise sources are going to be ignored for now; since V_{ngm} is in the same place as V_{na} we can use equation (5.18a) replacing V_{na} for V_{ngm} we have

$$N(s) = \frac{V_{no}(s)}{V_{ngm}(s)} = \frac{1 + s\tau_z}{1 + s(\tau_1 + \tau_2) + s^2\tau_1\tau_2} \tag{6.7}$$

From equation (A.5) from the appendix we have

$$V_{no\,rms}^2 = \frac{1}{\tau_1 + \tau_2}\left(1 + \frac{\tau_z^2}{\tau_1\tau_2}\right)\frac{1}{4}\overline{v_{ngm}^2} \tag{6.8}$$

From (5.17) and (6.5)with $\gamma = 1$ we obtain

$$V_{no\,rms}^2 = \frac{R_f^2 C_d^2 kT}{(g_{mN} + g_{mP})(\tau_1 + \tau_2)\tau_1\tau_2} \tag{6.9}$$

Assuming that $g_{mN} = g_{mP} = 5mS$ we have

For the APD with $R_f = 100k\Omega$, $C_d = 100fF$, $\tau_1 = \tau_2 = 10ns$

$$V_{no\,rms} = 0.45mV$$

And for the SIPM with $R_f = 20k\Omega$, $C_d = 50fF$, $\tau_1 = \tau_2 = 10ns$

$$V_{no\,rms} = 2.72mV$$

6.3.1.2 Noise contribution of OA

Now we only need to calculate the noise contribution of the OA from (5.21) we have with $\gamma = 1$

$$V_{no\,rms}^2 = \frac{R_f^2 C_d^2 kT}{g_{m1}(\tau_1 + \tau_2)\tau_1\tau_2} \tag{6.10}$$

Assuming that $g_{m1} = 5mS$ we have

For the APD with $R_f = 100k\Omega$, $C_d = 100fF$, $\tau_1 = \tau_2 = 10ns$

$$V_{no\,rms} = 0.643mV$$

With a SIPM with $R_f = 20k\Omega$, $C_d = 50fF$, $\tau_1 = \tau_2 = 10ns$

$$V_{no\,rms} = 3.86mV$$

6.3.2 Auxiliary path noise

In the auxiliary path we have to calculate the noise contribution of the OA and the GM, the resistor noise as was said before can be ignored.

6.3.2.1 Noise contribution of GM

We start by calculating the noise contribution of GM, since the current source that simulates the noise contribution of GM is in the same place as I_d as can be seen in Fig. 6.6, we can use equation (5.23)

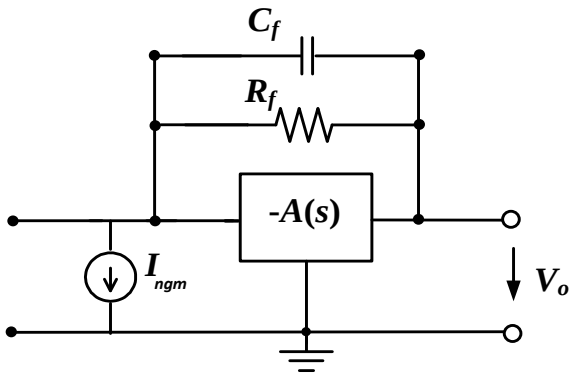

Figure. 6.6- Feedback TIA with GM noise

From the Appendix (A.7) we have for (5.23)

$$V_{no\,rms}^2 = \frac{R_f^2}{\tau_1+\tau_2}\frac{1}{4}\overline{\iota_{ngm}^2} \tag{6.11}$$

Replacing (6.6) in (6.11) we have

$$V_{no\,rms}^2 = \frac{R_f^2 kT g_{mtotal}}{\tau_1+\tau_2} \tag{6.12}$$

The value of $V_{no\,rms}^2$ is highly dependent on the feedback resistor, this means that when using an APD at the input $V_{no\,rms}^2$ can be very high due to the high values of $R_f$needed to compensate the low input signal generated by the APD. Assuming that $g_{mtotal} = 12ms$ we have;

For the APD with $R_f = 100k\Omega$, $\tau_1 = \tau_2 = 10ns$ and $g_{mtotal} = 12ms$

$$V_{no\,rms} = 4.9mV$$

For the SIPM with $R_x = 20k\Omega$, $\tau_1 = \tau_2 = 10ns$ and $g_{mtotal} = 12ms$

$$V_{no\,rms} = 0.99mV$$

As was expected we have a much higher value of $V_{no\,rms}$ when using an APD at the input, further on this relation between the noise generated by GM on the auxiliary path and the feedback resistor will be shown during the simulation.

6.3.2.2 Noise contribution of OA

Now that we have the noise generated by GM we only need to calculate the noise contribution of the OA from (5.21) we have with $\gamma = 1$

$$V_{no\,rms}^2 = \frac{R_f^2 C_d^2 kT}{g_{m1}(\tau_1 + \tau_2)\tau_1\tau_2} \tag{6.13}$$

In the case of the APD with $R_f = 100k$, $\tau_1 = \tau_2 = 10ns$ and assuming that $g_{m1} = 5ms$

$$V_{no\,rms} = 0.643mV$$

In the case of the SIPM with $R_x = 20k\Omega$, $\tau_1 = \tau_2 = 10ns$ and assuming that $g_{m1} = 5ms$

$$V_{no\,rms} = 3.86mV$$

6.4 Simulation result

6.4.1 Simulation Setup

The circuit in test was design using Cadence Virtuoso Analog Design Environment version 5.1.41,using 130µm transistor model Bsim version 3.3 with a 1.2V Vdd and simulated using Spectre Circuit Simulator version 7.11.

6.4.1.1 OA Block

The Operational amplifier in use is a Folded-Cascode Operational-transconductance amplifier (OTA) Fig. 6.7, with an open loop gain of 62dB. This amplifier was design and optimized as a project from design of analog circuits and Systems class, under the supervision of professor João Goes using Mathcad as can be seen in appendix B1.

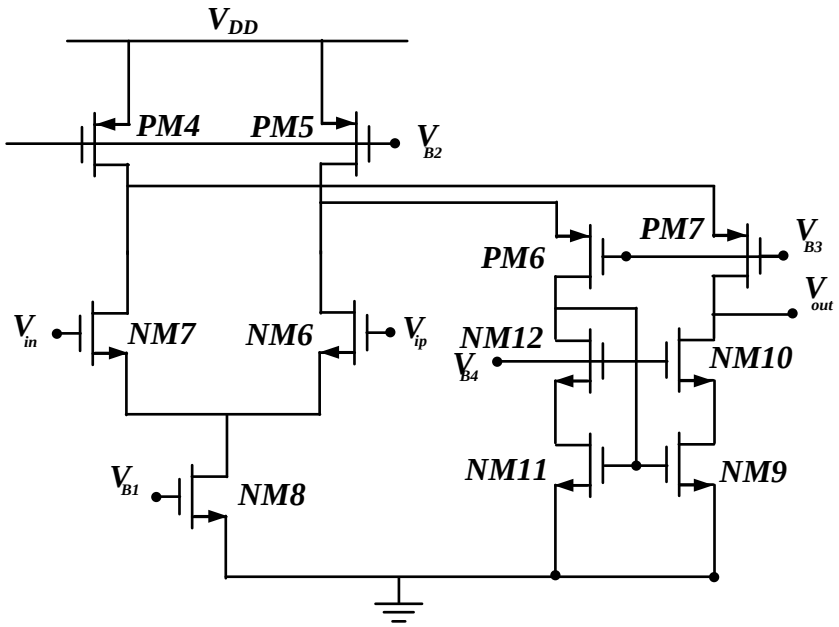

Figure. 6.7- Simplified Folded Cascode without polarizing circuit

When a feedback is applied to this amplifier, the gain decreases to 45.4 dB, when using a feedback with 100kΩ and 100fF, as is the case when an APD is in use, and to 31.4dB for a feedback of 20kΩ and 50fF, in the case of the SIPM.

We know from (5.10a) that this gain in the case of the SIPM is not big enough to ensure that $t_p < 40ns$, but since the circuit in study relays on the feedback TIA, and we know from chapter five that using a feedback TIA with a SIPM is not ideal, we are going accept that the time constant is above what was required an focus on whatever or not the signal to noise ratio is improved when a auxiliary path is used.

6.4.1.2 GM Block

From [20] we know that Inv 1,2,3,6 must have the same value and Inv 4,5 can be slightly smaller to increase the gain and that all transistors must be in saturation, the values used for GM during the simulations can be seen in table (6.1)

When dimension this circuit all the inverters 1 through 6 where assumed to be equal with n-channel W/L ratio of 12µm/3µm.

The widths of the p-channel devices are around 4.5 times larger than the n-channel widths to ensure $\beta_n = \beta_p$, this means that for the p-channel transistors we have a ratio of 54µm/3µm.

The length of the transistors was set at 3µm to minimize the effects of flicker noise in the circuit.

The values of inverters 4 and 5 where manual adjusted by simulating the circuit an comparing the input and output signals to ensure that the gain produced by the GM block was as close to one as possible.

The value of C_{int} was set to 1pA to reduce the impact of the GM block on the circuit time constants.

In table 6.1 we can see the values used for the length and widths of each inverter as well as the measured values for β and g_m.

Table 6.1- W/L values of the transconductance block

Cmos	L	W	β	gm
Inv 1 P	3µm	54µm	1.4m	1.05ms
Inv 1 N	3µm	12µm	1.4m	0.963ms
Inv 2 P	3µm	54µm	1.4m	1.05ms
Inv 2 N	3µm	12µm	1.4m	0.958ms
Inv 3 P	3µm	54µm	1.4m	1.05ms
Inv 3 N	3µm	12µm	1.4m	0.958ms
Inv 4 P	3µm	53.5µm	1.36m	1.1ms
Inv 4 N	3µm	11.5µm	1.38m	0.898ms
Inv 5 P	3µm	53.5µm	1.39m	1.04ms
Inv 5 N	3µm	11.5µm	1.34m	0.922ms
Inv 6 P	3µm	54µm	1.37m	1.11ms
Inv 6 N	3µm	12µm	1.44m	0.940ms

From [20] we know that in order for the GM block to have a good V-I conversion linearity and no internal nodes, we need to have $\beta_n = \beta_p$., in table 6 we can see that the values of β_n and β_p are almost perfectly match between each inverter.

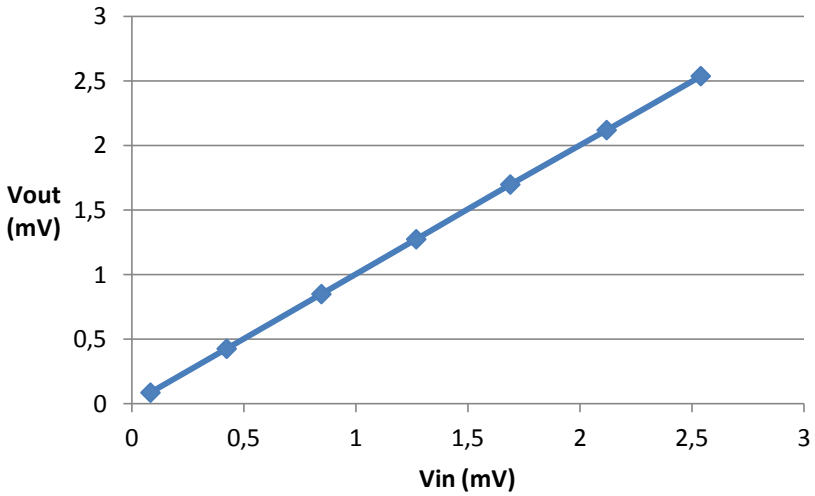

Figure. 6.8- Input and output of the GM block

From Fig. 6.8 we can observe that the output of the transconductance block is linear with the input as was needed. These values were obtained by increasing the current pulse in increments of 5uA, and measuring the response of the GM to then.

With these values we have for the APD a gain slightly bigger than one, and with the SIPM at the input a gain very close to one.

6.4.2 Using an APD at the input

We start the circuit simulations with an APD at the input, to simulate and APD the value of I_D was set to 2.5uA and the value of C_D to 10pF, as was seen in chapter 5 when using a APD at the input the values of R_f and C_f where set at 100kΩ and 100fF.

In Fig. 6.9 we can see the signal generated by APD I_in_ap and the output of the transconductance block gm_out

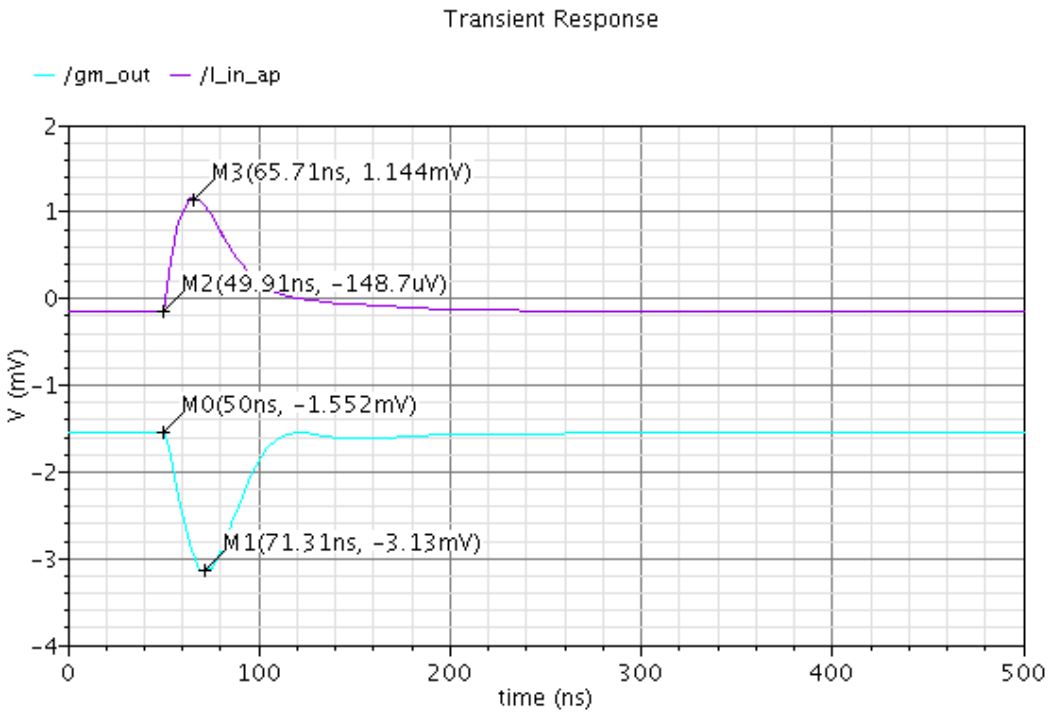

Figure. 6.9- Vin and Vout of the GM with an APD

From Fig. 6.9 we can see that the output signal of the GM block is 180 degrees out of phase while having a gain slightly larger than one. In Fig. 6.10 the outputs of the two feedback TIA are shown, finally in Fig. 6.11 we have the combined vout signal.

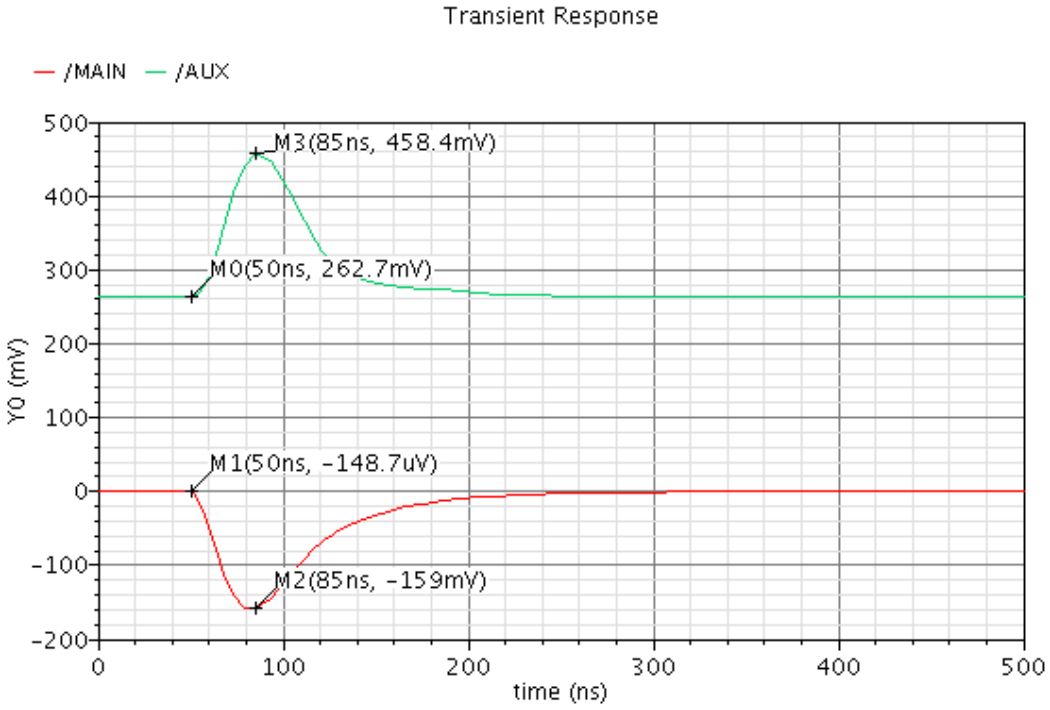

Figure. 6.10- Vout of the MAIN and AUXILIARY path with an APD

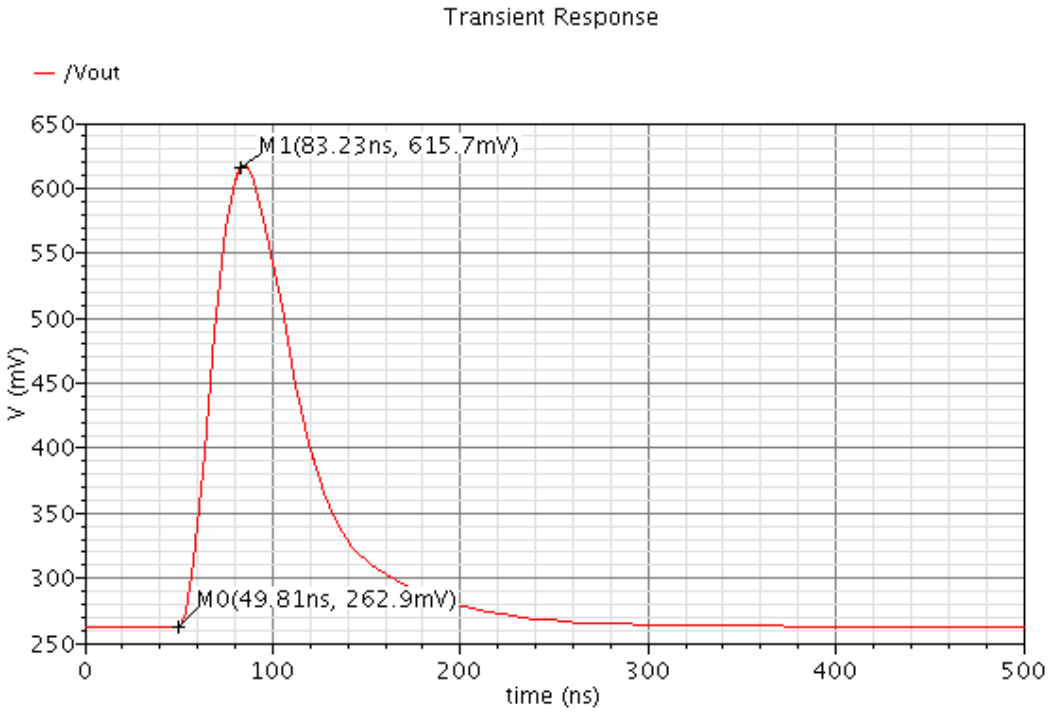

Figure. 6.11- Vout of the full circuit With an APD as the input

From Fig. 6.11 $t_p = 33.42\ ns$ witch is below 40ns one of the requirements of the circuit.

During the study of the feedback TIA it was shown that there was a need to use a post-amplifier in conjunction with the TIA so that we could maintain the desired pulse shape while maintaining C_f and B at reasonable values, since in this circuit the combination of the two paths is going to generate twice the output of a single feedback TIA there is less of a need for a post-amplifier.

In table 6.2 the noise values simulated for each individual path and for the full circuit can be seen. The values for the main and auxiliary path where obtain with each path isolated from the other.

Table 6.2- Noise when using 100kΩ/100fF

Circuit	Rms noise 1k-1G	Type of noise	Main source	Noise contribution	% of Total	Source
Main Path	1.63mV	Thermal	NM7	0.565 μV^2	21.12	MAIN OAMP
		Thermal	NM6	0.554 μV^2	20.74	MAIN OAMP
		Thermal	PM5	0.465 μV^2	17.39	MAIN OAMP
		Thermal	PM4	0.462 μV^2	17.29	MAIN OAMP
		Thermal	NM9	0.246 μV^2	9.22	MAIN OAMP
Auxiliary Path	5.35mV	Thermal	INV 1 N	1.80 μV^2	6.29	GM
		Thermal	INV 6 P	1.78 μV^2	6.21	GM
		Thermal	INV 5 N	1.72 μV^2	6.02	GM
		Thermal	INV 6 N	1.72 μV^2	6.00	GM
		Thermal	INV 1 P	0.169 μV^2	5.89	GM
Full Circuit	6.70mV	Thermal	NM7	3.09 μV^2	6.89	MAIN OAMP
		Thermal	NM6	3.06 μV^2	6.82	MAIN OAMP
		Thermal	PM5	2.55 μV^2	5.69	MAIN OAMP
		Thermal	PM4	2.53 μV^2	5.64	MAIN OAMP
		Thermal	INV 1 N	1.80 μV^2	4.03	GM

From table 6.2 we can observe that the smallest total noise value obtain is from the main path, this was expected as the main path consists only of the feedback TIA.

In the auxiliary path we have a much higher noise value, this is due, to the noise generated by the GM block in conjunction with the high resistor value in use on the feedback.

Finally we can see the noise of the full circuit, from the value of the total noise we can observe that there is noise canceling in effect since the total noise of the full circuit is smaller than the sum of each individual path.

To calculate the value of the single feedback path we use equation (6.10) with $gm_{in} = 2ms$ and $\tau_1 = \tau_2 = 20ns$ we have

$$V_{no\ OA} = 0.35mV$$

Multiplying this value by five we have

$$V_{no\ OA} = 1.75mV$$

Now to calculate the noise contribution of GM in the auxiliary path we are going to use equation (6.12). With $gm_{total} = 12ms$ and $\tau_1 = \tau_2 = 20ns$ we have

$$V_{no\ GM} = 3.5mV$$

Assuming that the auxiliary path feedback TIA has the same noise as the main path, the total noise of the auxiliary path can be achieved by adding the noise generated by the feedback $V_{no\ OA}$ with the noise generated by the GM block $V_{no\ rms}$

$$V_{no\ aux} = V_{no\ OA} + V_{no\ GM} = 1.75mV + 3.5mV = 5.25\ mV$$

Since the noise produced by the auxiliary path is so much higher than that of the main path any possible gain in noise canceling is lost as can be seen in table 6.3.

Table 6.3- Signal to Noise Comparison with an APD

Circuit	Main	Auxiliary	Full circuit	Ideal GM
Vout	158,5mV	195.9mV	352.8mV	360.9mV
Noise	1.63mV	5.35mV	6.70mV	3.77mV
S/N	97	36.6	52.6	95.7

In table 6.3 we have the signal to noise ratio of each individual path as well as that of the full circuit using the GM block previously shown and a VSCS that serves as an ideal GM block.

One thing that we have to take into account is that, while the noise of the full circuit is bigger than that of the individual path, the fact that the voltage amplitude is twice as big as to be taken into consideration.

From table 6.3 we can see that the best signal to noise ratio is achieved with the main path, while the worst by the auxiliary path, as expected the high noise value of the auxiliary paths means that the full circuit is going to have a worst signal to noise ratio that the main path as can be seen. The noise value for the ideal GM is very close to the noise of the main path, this means that the use of a auxiliary path in this case has almost no effect on the circuit.

To achieve a V_{out}signal with 300mv a smaller value of R_x, can be use, this eliminates the need of a post-amplifier, since reducing the value of R_x will improve the circuit time response, $R_x = 83k$ is enough to achieve the necessary output amplitude as can be seen In table (4)

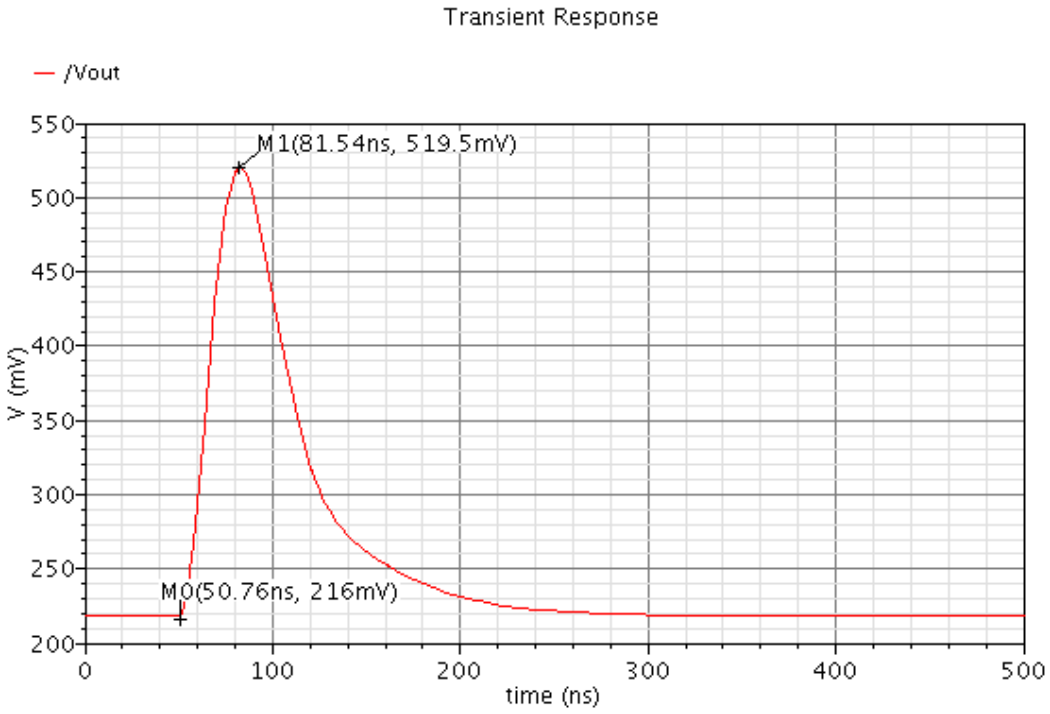

Figure. 6.12- Vout of full circuit when using 83k/100f

From Fig. 6.12 it is possible to see that with $R_x = 83k\Omega$ the value of Vout is approximately 300mV. As before in table 6.4 the noise values of each individual path as well as the full circuit are shown

Table 6.4- Noise when using an APD and 83kΩ/100fF

Circuit	Rms noise 1k-1G	Type of noise	Main source	Noise contribution	% of Total	Source
Main Path	1.58mV	Thermal	NM7	0.527 μV^2	21.09	MAIN OAMP
		Thermal	NM6	0.518 μV^2	20.72	MAIN OAMP
		Thermal	PM5	0.434 μV^2	17.37	MAIN OAMP
		Thermal	PM4	0.432 μV^2	17.29	MAIN OAMP
		Thermal	NM9	0.231 μV^2	9.24	MAIN OAMP
Auxiliary Path	4.69mV	Thermal	INV 1 N	1.39 μV^2	6.34	GM
		Thermal	INV 6 P	1.38 μV^2	6.27	GM
		Thermal	INV 5 N	1.33 μV^2	6.07	GM
		Thermal	INV 6 N	1.30 μV^2	6.06	GM
		Thermal	INV 1 P	0.129 μV^2	5.94	GM
Both Paths	5.92mV	Thermal	NM7	2.53 μV^2	7.22	MAIN OAMP
		Thermal	NM6	2.50 μV^2	7.14	MAIN OAMP
		Thermal	PM5	2.09 μV^2	5.97	MAIN OAMP
		Thermal	PM4	2.07 μV^2	5.91	MAIN OAMP
		Thermal	INV 1 N	1.39 μV^2	3.99	GM

From table 6.4 we can see that in proportion to the main path the noise in the auxiliary path is much smaller when compared to the value in table 6.2, this reinforces the fact that the noise contribution of GM on the auxiliary path is highly dependent on the value of R_x. The new signal to noise rations can be seen on table 6.5.

Table 6.5- signal to noise ratios for $V_{out} \cong 300mV$ with an APD

Circuit	Main	Auxiliary	Both Paths	Ideal GM
Vout	138.6mV	164.7mV	303.5mV	299mV
Noise	1.58mV	4.69mV	5.92mV	3.38mV
S/N	87.7	35	54.3	88.5

From table 6.5 we can concluded that while the signal to noise ratio of the full circuit is improved in relation to the main path, the noise generated by the GM block on the auxiliary path is still too high.

6.4.3 Using an SIPM at the input

The APD is now replaced by a SIPM at the input, to simulate a SIPM the value of I_D is set to 25uA and the value of C_D to 300pF, as was seen in chapter 5, when using a SIPM at the input the values of R_f and C_f are set at 20kΩ and 50fF,

In Fig. 6.13 we can see the signal generated by the SIPM I_in_si and the output of the transconductance block gm_out

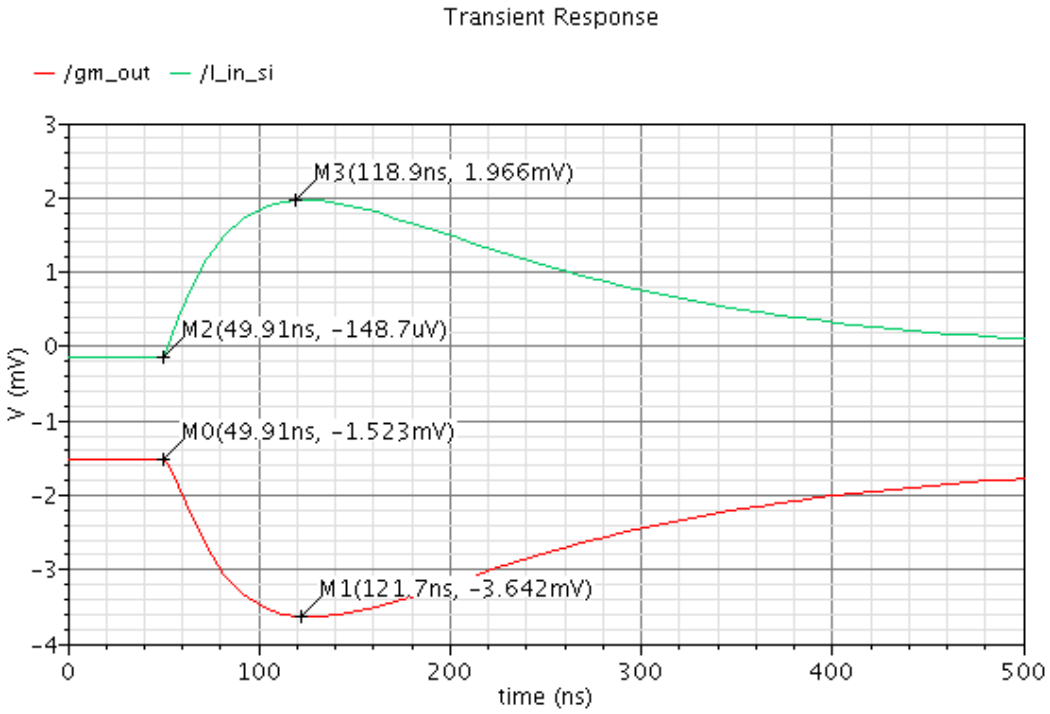

Figure. 6.13- GM Input and Output using a SIPM

From Fig. 6.13 we can see that the output of the GM block is equal to the input but 180º out of phase. In Fig. 6.14 the output values of the feedback TIAs in the main an auxiliary paths can be seen, finally in Fig. 6.15 we can observe the full circuit Vout.

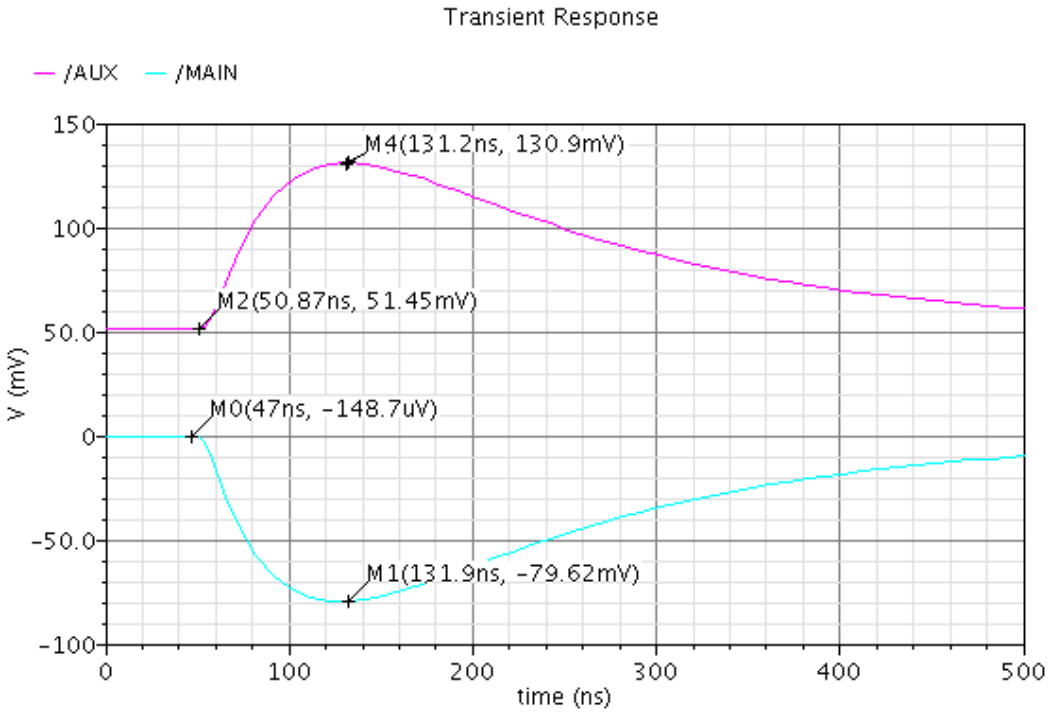

Figure. 6.14- Comparison between the Main and Auxiliary Path with a SIPM

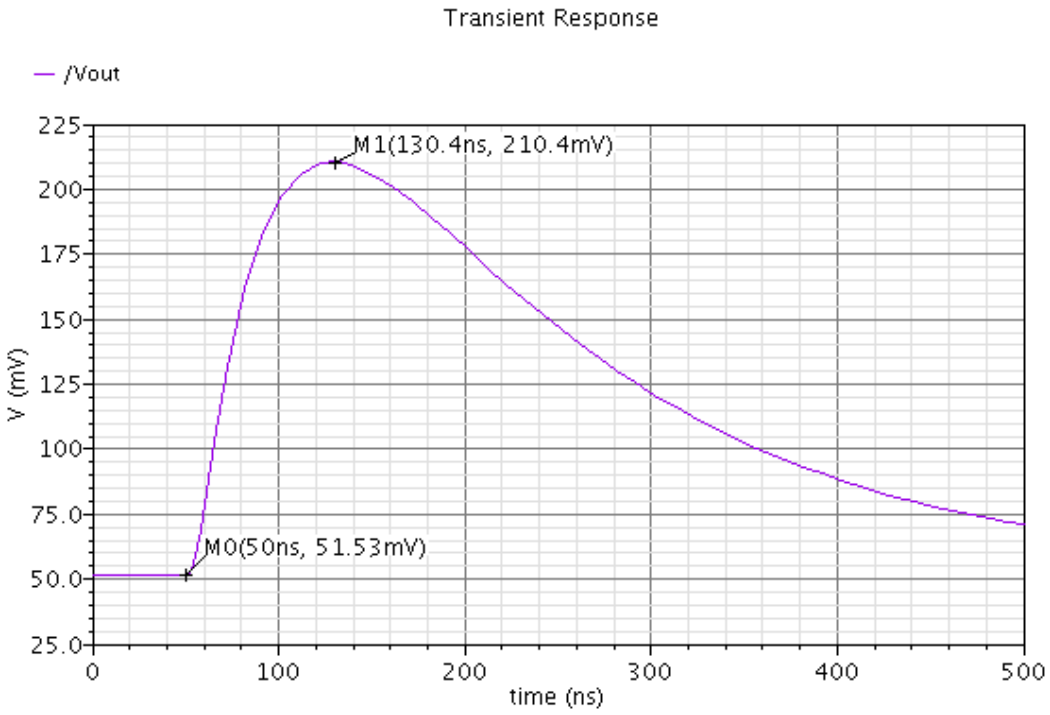

Figure. 6.15- SIPM full circuit Vout

From Fig. 6.14 and Fig. 6.15 it's possible to see that $t_p = 80ns$,has was expected since the gain of the OA in use is not big enough to compensate the high value of C_d.

In table 6.6 as before we can see the noise values for each individual path and for the full circuit. The values for the main and auxiliary path where obtain with each path isolated from the other.

Table 6.6- feedback noise values when using 20kΩ/50fF with a SIPM

Circuit	Rms noise 1k-1G	Type of noise	Main source	Noise contribution	% of Total	Source
Main Path	1.34mV	Thermal	NM6	0.366 μV^2	20.45	MAIN OAMP
		Thermal	NM7	0.361 μV^2	20.16	MAIN OAMP
		Thermal	PM4	0.307 μV^2	17.11	MAIN OAMP
		Thermal	PM5	0.298 μV^2	16.63	MAIN OAMP
		Thermal	NM9	0.169 μV^2	9.43	MAIN OAMP
Auxiliary Path	1.87mV	Thermal	NM7	0.275 μV^2	7.86	AUX OAMP
		Thermal	NM6	0.268 μV^2	7.63	AUX OAMP
		Thermal	PM4	0.229 μV^2	6.55	AUX OAMP
		Thermal	PM5	0.224 μV^2	6.38	AUX OAMP
		Thermal	INV 1 N	0.179 μV^2	5.12	GM
Both Paths	2.33mV	Thermal	NM6	0.384 μV^2	7.08	MAIN OAMP
		Thermal	NM7	0.379 μV^2	6.99	MAIN OAMP
		Thermal	PM4	0.321 μV^2	5.92	MAIN OAMP
		Thermal	PM5	0.313 μV^2	5.77	MAIN OAMP
		Thermal	NM7	0.275 μV^2	5.07	AUX OAMP

From table 6.6 we can observe that the smallest total noise value as was the case when using an APD is obtain from the main path,. In the auxiliary path we have a higher noise value due to the GM block, but unlike before the value of the resistor on the feedback is much smaller due to the much higher amplitude of the signal generated by the SIPM in comparison to the APD this leads to a much lower noise on the GM.

Finally we can see the noise of the full circuit, from the value of the total noise we can observe that there is noise canceling in effect since the total noise of the full circuit is smaller than the sum of each individual path, and since the noise of the full circuit is lower than two times the noise of a single path for twice the output signal we have a better signal to noise ratio with the full circuit than with only the main path.

Using equation (6.10) to calculate the noise of the single path with $\tau_1 = \tau_2 = 81ns$ and $gm_{in} = 2ms$ we have

$$V_{no\ rms} = 0.2635mV$$

Since the input transistor of the OA is responsible for about 20% of the noise for 100% we have

$$V_{no\ rms} = 0.2635 \times 5 = 1.317mV$$

For the auxiliary path using equation (6.12) with $gm_{total} = 12ms$ we obtain

$$V_{no\ rms} = 0.35mV$$

Assuming that the auxiliary feedback TIA has the same noise as the main TIA adding the two we have for the auxiliary path

$$V_{no\ rms} = 0.35 + 1.31 = 1.66mV$$

This values are similar to the ones obtain during the simulation.

In table 6.7 we have the signal to noise ratio of the main and auxiliary path as well as the ratio when the two are used together.

Table 6.7- Signal to Noise Comparison using a SIPM and 20kΩ/50fF

Circuit	Main	Auxiliary	Full circuit	Ideal GM
Vout	79.46mV	79,44mV	159.2mv	158.7mV
Noise	1.34mV	1.89mV	2.33mV	1.71mV
S/N	59.3	42,03	68.3	92.8

From table 6.7 we can see the signal to noise ratio of each individual path as well as that of the full circuit. Using both a non-ideal and a ideal GM block as was the case when testing with the APD. from the table we can see that the best signal to noise ratio is achieved with the full circuit, this means that we are able to reduce the noise by using this circuit. Like before the auxiliary path presents the worse signal to noise ratio as was expected.

When comparing the full circuit with an without the ideal GM, we can see that it's possible to further improve the S/N

To get 300mv of output amplitude, we can increase the feedback resistor to 38KΩ, the resulting voltage pulse can be seen in Fig. 6.16.

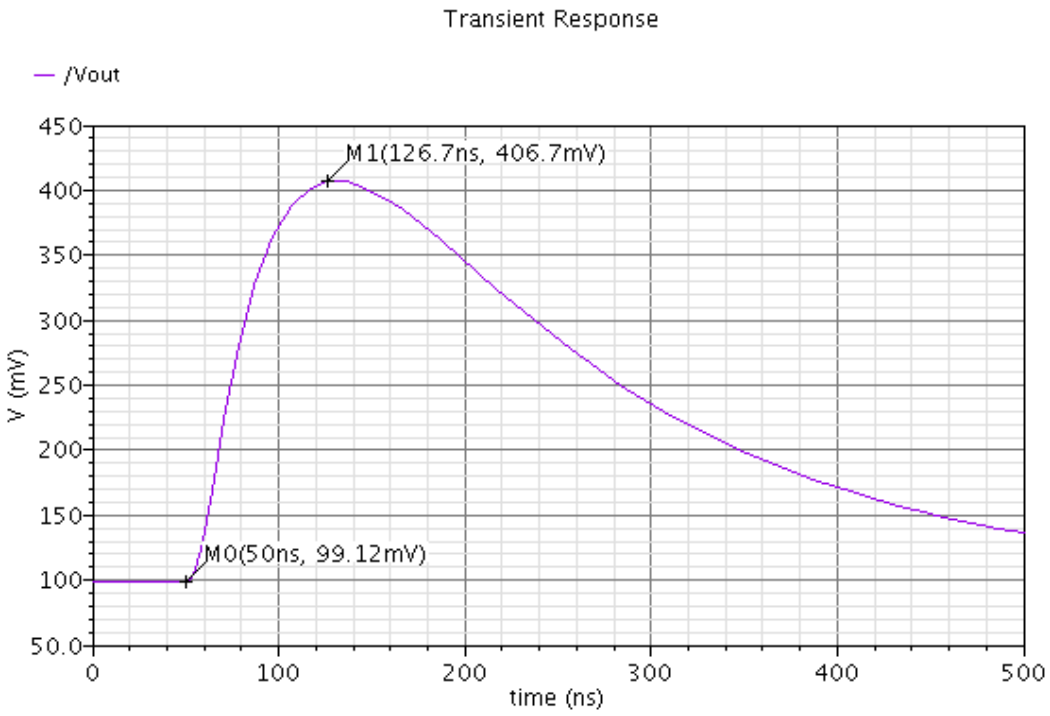

Figure. 6.16- Vout when using 38k/50f in the feedback with a SIPM

Normally a VCVS post-amplifier would be used to prevent an increase in the circuit time constants by the increase of R_f, but since we are not concerned with the circuit time response in this case, increasing the value of R_f is a easy way to obtain a output voltage pulse of 300mV.

From the simulations we have

Table 6.8- Noise for 38kΩ/50fF with a SIPM

Circuit	Rms noise 1k-1G	Type of noise	Main source	Noise contribution	% of Total	Source
Main Path	1.88mV	Thermal	NM6	0.738 μV^2	20.80	MAIN OAMP
		Thermal	NM7	0.733 μV^2	20.64	MAIN OAMP
		Thermal	PM4	0.614 μV^2	17.30	MAIN OAMP
		Thermal	PM5	0.605 μV^2	17.05	MAIN OAMP
		Thermal	NM9	0.325 μV^2	9.17	MAIN OAMP
Auxiliary Path	3.03mV	Thermal	INV 1 N	0.551 μV^2	5.99	GM
		Thermal	INV 6 p	0.544 μV^2	5.91	GM
		Thermal	INV 6 N	0.527 μV^2	5.73	GM
		Thermal	INV 5 N	0.526 μV^2	5.72	GM
		Thermal	INV 5 P	0.516 μV^2	5.61	GM
Both Paths	3.63mV	Thermal	NM6	0.798 μV^2	6.04	MAIN OAMP
		Thermal	NM7	0.793 μV^2	6.00	MAIN OAMP
		Thermal	PM4	0.663 μV^2	5.02	MAIN OAMP
		Thermal	PM5	0.653 μV^2	4.95	MAIN OAMP
		Thermal	INV 1 N	0.55μV^2	4.16	GM

From table 6.8 we can see that the increase of R_x has a big impact on the noise as was expected, in table 6.9 we have the signal to noise ratio of the three cases.

Table 6.9- Signal to noise ratio for 38kΩ/50fF

Circuit	Main	Auxiliary	Both Paths
Vout	153.4mv	155mv	306mv
Noise	1.88mV	3.08mV	3.63mV
S/N	81	50.32	84.2

From table 6.9 we can see that increasing the resistor from 20kΩ to 38kΩ is enough to achieved a signal amplitude of 306mv. Even with the effect on GM of the new resistor the signal to noise ratio is still better when the full circuit is used.

6.4.4 Comparing APD with SIPM

Now we are going to directly compare the APD and the SIPM, in this comparison the same feedback circuit is used in conjunction with each device.

The chosen feedback parameters where, $R_f = 20k\Omega$ and $C_f = 50fF$. This values were chosen for two motives, the low value of R_f need to minimize the noise of GM, and second because since the parameter we are interested in is the signal to noise ratio, the amplitude an time response of the circuit are not important.

We start by simulating the APD with this values, the simulation results can be seen in Fig. 6.17 where the output of each TIA is compared and Fig. 6.18 where the full circuit output signal can be seen.

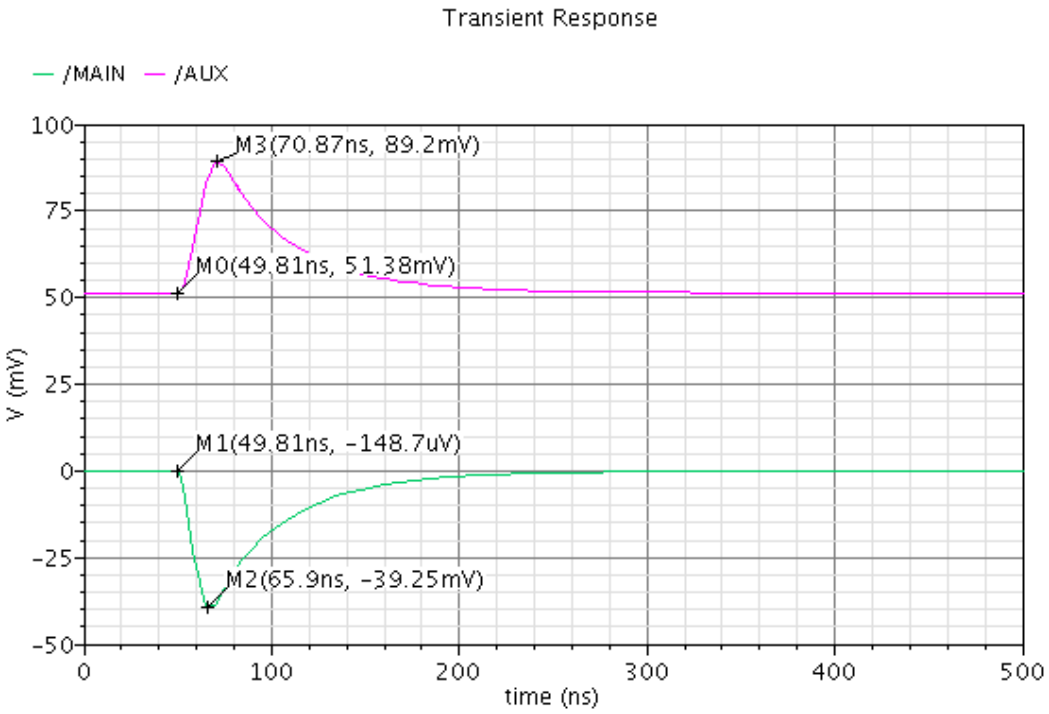

Figure. 6.17- APD with a 20k/100f as the feedback

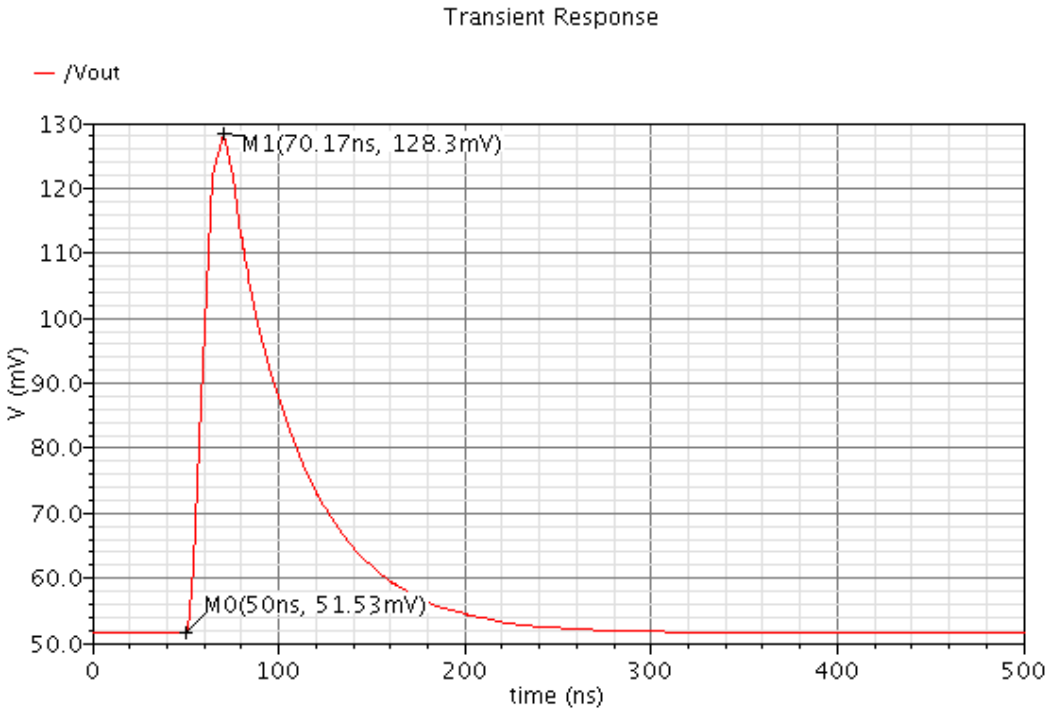

Figure. 6.18- Full circuit Vout with an APD and 20k/50f

From the simulations we obtain

Table 6.10- APD 20kΩ/50fF

Circuit	Rms noise 1k-1G	Type of noise	Main source	Noise contribution	% of Total	Source
Main Path	1.29mV	Thermal	NM7	0.337 μV^2	20.21	MAIN OAMP
		Thermal	NM6	0.331 μV^2	20.09	MAIN OAMP
		Thermal	PM4	0.278 μV^2	16.90	MAIN OAMP
		Thermal	PM5	0.274 μV^2	16.64	MAIN OAMP
		Thermal	NM9	0.158 μV^2	9.59	MAIN OAMP
Auxiliary Path	1.86mV	Thermal	NM7	0.274 μV^2	7.93	AUX OAMP
		Thermal	NM6	0.266 μV^2	7.70	AUX OAMP
		Thermal	PM4	0.228 μV^2	6.61	AUX OAMP
		Thermal	PM5	0.222 μV^2	6.43	AUX OAMP
		Thermal	INV 1 N	0.176 μV^2	5.10	GM
Both Paths	2.56mV	Thermal	NM7	0.622 μV^2	9.51	MAIN OAMP
		Thermal	NM6	0.616 μV^2	9.42	MAIN OAMP
		Thermal	PM4	0.514 μV^2	7.86	MAIN OAMP
		Thermal	PM5	0.513 μV^2	7.84	MAIN OAMP
		Thermal	NM9	0.279 μV^2	4.27	MAIN OAMP

In table 6.10 we, again can see, as was the case in table 6.4 that by decreasing the value of R_x the noise on the auxiliary path is going to be substantially smaller than that of table 6.2. In table 6.11 we can see the signal to noise ratio when using an APD at the input with a feedback of 20KΩ/50fF

Table 6.11- APD 20kΩ/50fF

Circuit	Main	Auxiliary	Full circuit
Vout	39,1mV	37,8mV	76,77mV
Noise	1.29mV	1.89mV	2.56mV
S/N	30.3	20	30

From table 6.11 we can see that the signal to noise ratio in this case when using an APD is smaller, than when a single feedback TIA is used. In the case of the SIPM we have

Table 6.12- SIPM 20kΩ/50fF

Circuit	Main	Auxiliary	Full circuit
Vout	79.46mV	79,44mV	159.2mV
Noise	1.34mV	1.89mV	2.33mV
S/N	59.3	42,03	68.3

Comparing the values on table 6.11 to table 6.12, we can see that when using the same GM and the same feedback gain, we have a worse signal to noise ratio on the APD , this is due to the much smaller amplitude current pulse produced by the APD, from table 6.11 and 6.12 we can observe that the noise values on both cases are very similar, but the signal amplitude in the case of the SIPM is superior, this means that for nearly the same amount of noise we are going to have a much bigger signal amplitude with the SIPM, this leads to a better signal to noise ratio.

The higher signal amplitude in the case of the SIPM means that the circuit is less affected by the extra noise generated by the GM block, this means that in the case of the SIPM we have a better signal to noise ratio when using both paths.

CHAPTER 7

Chapter 7 Conclusions

In this work we tried to reduce the feedback circuit noise of the TIA by adding an auxiliary path. this circuit was tested with an APD and a SIPM.

The addition of an extra path did not reduce the noise of the feedback TIA, when an APD was used as the input, the low amplitude current pulse produced by the APD in conjunction with the noise produced by the GM block due to the high value of R_x needed to compensate for the low amplitude, means that we are unable to achieve a better signal to noise ratio when using an auxiliary path in conjunction with the feedback TIA instead of a simple feedback TIA.

On the other hand with a SIPM as the input we were able to achieve a better signal to noise ratio using the auxiliary path in conjunction with the feedback TIA , this was due to the much higher signal amplitude ten times as high as the amplitude produced by the APD this means that the noise produced by the GM block doesn't have the same impact on the overall circuit noise as was the case with the APD.

With a SIPM we were able to reduce the signal to noise ratio from 59 to 68.3. This noise reduction comes at the cost of increased power consumption, total circuit power consumption of 4.81 mW.

Current technology makes the use of SIPMs with feedback TIAs impractical, this is due to the very high value of GBW need to compensate, the very high value of C_d, the input capacitance of the SIPM, This problem may be solved in the future with the use of 28nm technology, thus making this circuit a valid solution for the use with SIPMs.

APPENDIX A1

APPENDIX A1

Noise in Second-Order Networks

If we consider an input noise source with a spectral density $\overline{x_n^2}$ the resulting output noise will have a spectral density $\overline{y_n^2}$ [11] where the noise function N(s) is used to relate $\overline{x_n^2}$ with $\overline{y_n^2}$ using

$$\overline{y_n^2} = |N(s)|^2_{s=j2\pi f}\overline{x_n^2} \tag{A.1}$$

And an output rms noise $y_{n\,rms}^2$

$$y_{n\,rms}^2 = \int_0^\infty \overline{y_n^2}\mathrm{df} \tag{A.2}$$

If x_n is white noise with a spectral density $\overline{x_n^2}$ then from (A.1) we obtain

$$y_{n\,rms}^2 = \overline{x_n^2} \int_0^\infty |N(s)|^2_{s=j2\pi f}\mathrm{df} \tag{A.3}$$

If we have two poles and one zero N(s) can be written as

$$N(s) = N_0 \frac{1+s\tau_z}{(1+s\tau_1)(1+s\tau_2)} \tag{A.4}$$

From [17] we know that $y_{n\,rms}^2$ can be written as

$$y_{n\,rms}^2 = N_0^1 \frac{1}{\tau_1 + \tau_2}\left(1 + \frac{\tau_z^2}{\tau_1\tau_1}\right)\frac{1}{4}\overline{x_n^2} \tag{A.5}$$

if the transfer function only has two poles and no zero, or the zero is at a much higher frequency that the poles we replace $\tau_z = 0$ in (A.4)

$$N(s) = N_0 \frac{1}{(1 + s\tau_1)(1 + s\tau_2)} \tag{A.6}$$

From [17] $y_{n\,rms}^2$ can be written as

$$y_{n\,rms}^2 = N_0^1 \frac{1}{\tau_1 + \tau_2}\frac{1}{4}\overline{x_n^2} \tag{A.7}$$

In the case where there is only one pole or one dominant pole we have for N(s)

$$N(s) = N_0 \frac{1}{(1 + s\tau_1)} \tag{A.8}$$

From [17] we know that $y_{n\,rms}^2$ is

$$y_{n\,rms}^2 = N_0^1 \frac{1}{4\tau}\overline{x_n^2} \tag{A.9}$$

APPENDIX B1

APPENDIX B1

Optimization of a Folded-Cascode OTA Using Mathcad

The circuit of the Folded-Cascode OTA can be seen in Fig. B.1,

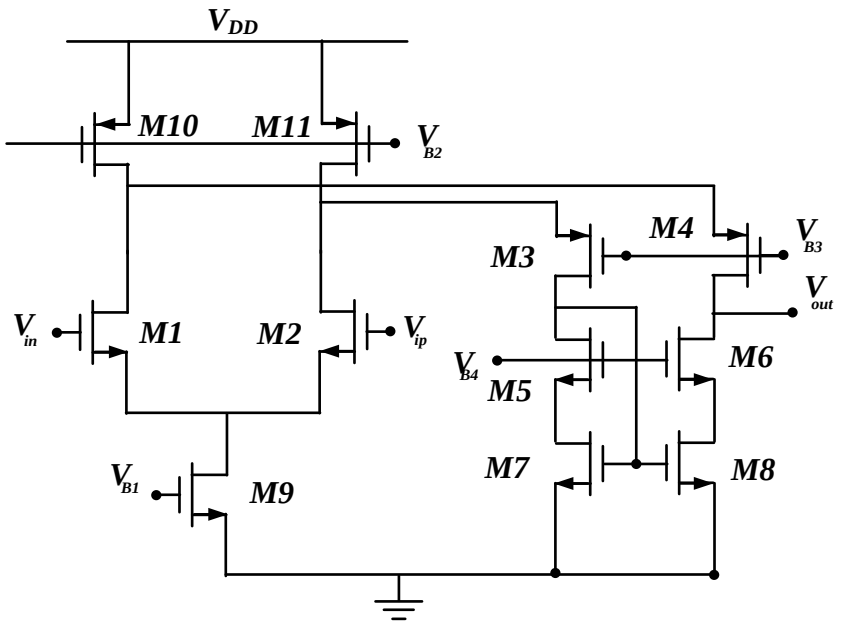

Figure: B.1- Folded-Cascode Amplifier

By analyzing the circuit in Fig. B1 and using as input variables on Mathcad

$$i = 1\ldots100 \tag{B.1a}$$

$$V_{Dsat_i} = 50mV + \frac{i}{100}150mV \tag{B.1b}$$

$$L_i = 0.48\mu m + \frac{i}{100}1.4\mu m \tag{B.1c}$$

$$I_i = 10\mu A + \frac{i}{100}500\mu A \tag{B.1d}$$

we are able to define the parameters of the circuit. To define the gain of the circuit we use [21],

$$\text{gain}(I_B, V_{Dsat1}, V_{Dsat4}, V_{Dsat6}, L1, L4, L6, L8, L11) = \frac{gm\left(\frac{I_B}{2}, V_{Dsat1}\right) BefN}{g_{oP}(I_B, V_{Dsat}, L1, L4, L11) + g_{oN}(I_B, V_{Dsat6}, L6, L8)} \tag{B.2}$$

Using (8.2) and the variables (8.1) we are able to plot the graph in Fig. B.2 and B3. Analyzing Fig. B2 we can conclude that, to maximize the value of the gain, the V_{Dsat} from transistors M1, M4 and M6 have to be small.

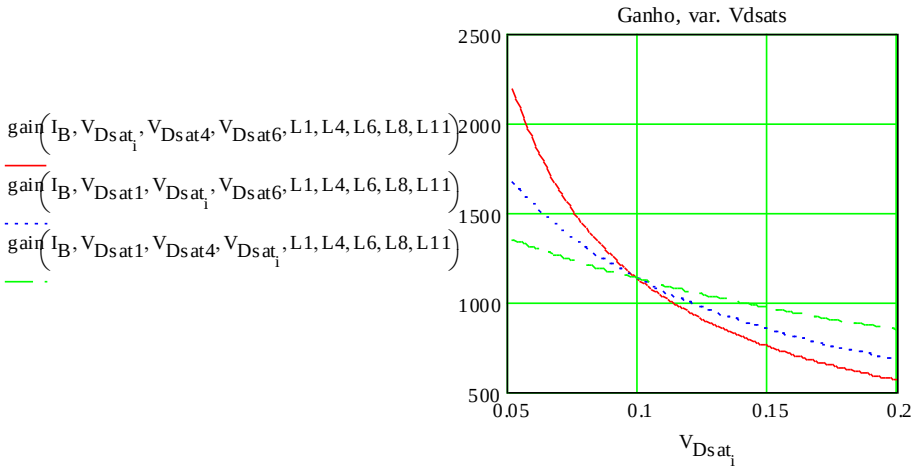

Figure. B.2- Gain in relation to V_{Dsat}.

Alternatively we can increase the channel length of transistors M1, M4, M6, M8 and M11 to increase the gain as can be seen in Fig. B.3

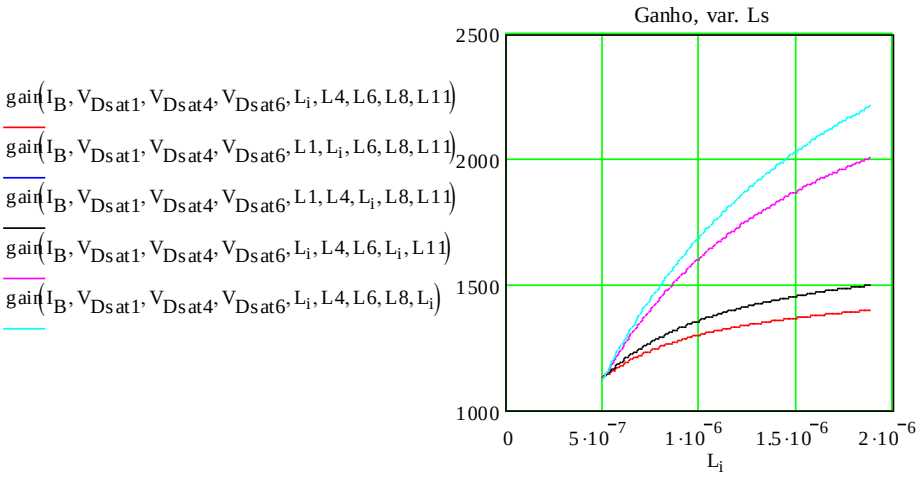

Figure. B.3- Gain in relation to Channel Length.

To define the value of GBW we use [21],

$$GBW(I_B, V_{Dsat1}, V_{Dsat6}, V_{Dsat4}, L6, L4) = \frac{gm\left(\frac{I_B}{2}, V_{Dsat1}\right) BefN}{C_{out}(I_B, V_{Dsat6}, V_{Dsat4}, L6, L4)2\pi} \quad \text{(B.3)}$$

Appling the same process used for the gain we are able to plot the graph in Fig. B.4, from this graph we can conclude that to achieve a high value of GBW, the value of V_{Dsat1} should be small.

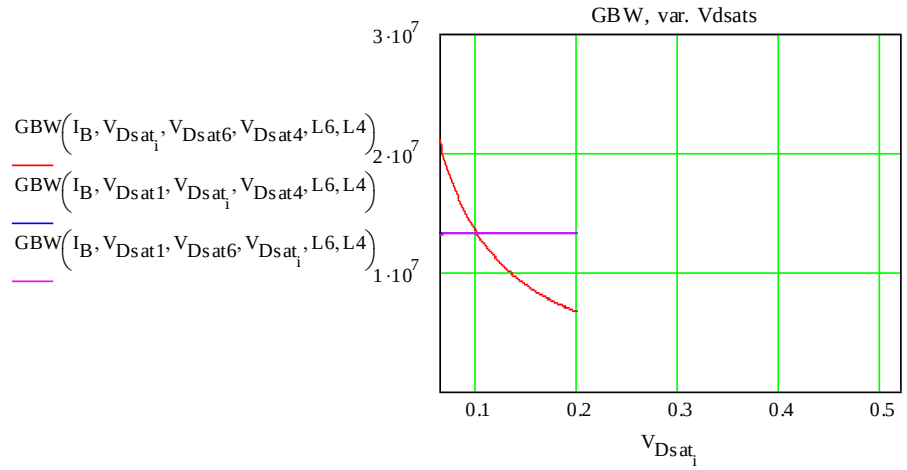

Figure: B.4- GBW in relation to V_{Dsat}.

Now we are going to define the frequency of the second pole using [21],

$$fp2(I_B, V_{Dsat1}, V_{Dsat4}, V_{Dsat11}, L1, L4, L11) = \frac{gm\left(\frac{I_B}{2}, V_{Dsat4}\right) BefP}{C_{dif}(I_B, V_{Dsat1}, V_{Dsat4}, V_{Dsat11}, L1, L4, L11)2\pi} \quad \text{(B.4)}$$

Using (B.4) we are able to plot the graphs on Fig. B.5 and Fig. B.6. From Fig. B.5 we observe that the increasing the value of V_{Dsat1} of transistors M4 and M11 we increase the frequency of the pole.

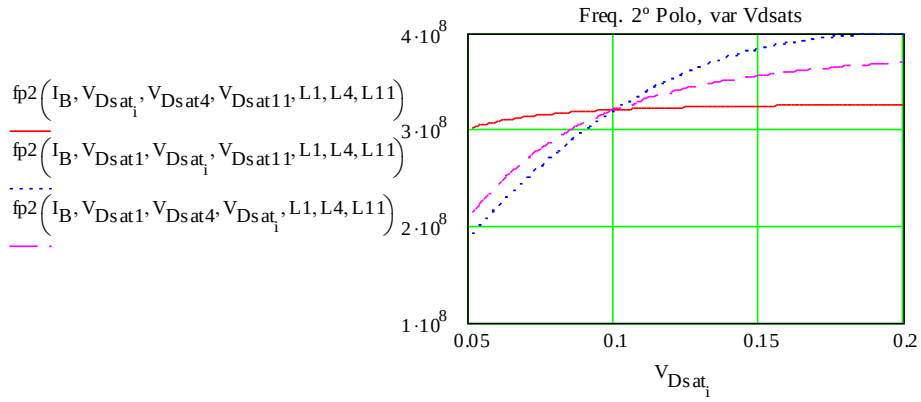

Figure. B.5- 2º pole frequency in relation to V_{Dsat}.

On the other hand increasing the channel length of transistors M4 and M11 decreases the frequency of the pole as can be seen in Fig. B.5.

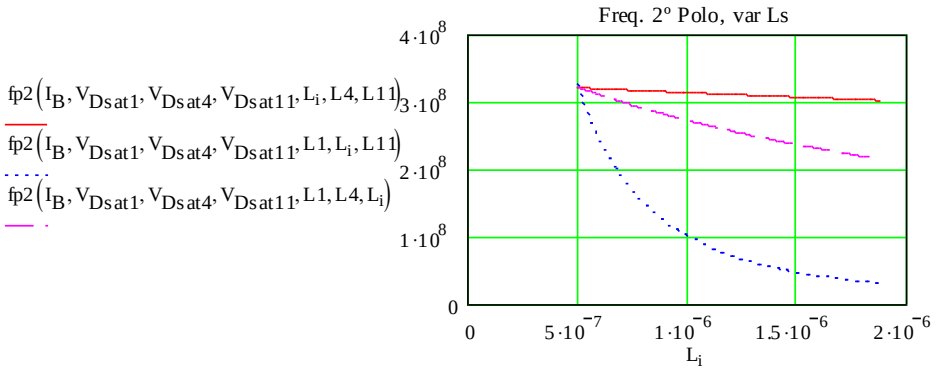

Figure. B.6- 2º pole frequency in relation to channel length.

By analyzing the previous graphs we are able to optimize the folded-cascode amplifier to suit our needs.

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REFERENCES

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