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Design of Analog-to-Digital Converters with Embedded Mixing for Ultra-Low-Power Radio Receivers

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"The arc of the moral universe is long, but it bends toward justice." — Martin Luther King, Jr.

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Abstract

In the field of radio receivers, down-conversion methods usually rely on one (or more) explicit mixing stage(s) before the analog-to-digital converter (ADC). These stages not only contribute to the overall power consumption but also have an impact on area and can compromise the receiver's performance in terms of noise and linearity. On the other hand, most ADCs require some sort of reference signal in order to properly digitize an analog input signal. The implementation of this reference signal usually relies on bandgap circuits and reference buffers to generate a constant, stable, dc signal. Disregarding this conventional approach, the work developed in this thesis aims to explore the viability behind the usage of a variable reference signal. Moreover, it demonstrates that not only can an input signal be properly digitized, but also shifted up and down in frequency, effectively embedding the mixing operation in an ADC. As a result, ADCs in receiver chains can perform double-duty as both a quantizer and a mixing stage. The lesser known charge-sharing (CS) topology, within the successive approximation register (SAR) ADCs, is used for a practical implementation, due to its feature of "pre-charging" the reference signal prior to the conversion. Simulation results from an 8-bit CS-SAR ADC designed in a 0.13 µm CMOS technology validate the proposed technique.

Keywords: Analog-to-digital converter (ADC), charge-sharing (CS), embedded down-conversion, successive approximation register (SAR), radio receivers, variable references

Resumo

No campo dos receptores rádio, os métodos de conversão para frequências mais baixas tipicamente dependem de um (ou mais) estágios explícitos de mistura, antecedendo o conversor analógico-digital (ADC). Estes estágios contribuem não só para a dissipação de potência global mas também têm um impacto na área e podem até comprometer a performance do receptor em termos de ruído e linearidade. Por outro lado, a maior parte dos ADCs requer algum tipo de sinal de referência para digitalizar adequadamente um sinal de entrada analógico. A implementação deste sinal de referência tipicamente recorre a circuitos *bandgap* e *buffers* de referência para gerar um sinal dc constante e estável. Ignorando esta abordagem convencional, o trabalho desenvolvido nesta tese visa explorar a viabilidade por detrás do uso de um sinal de referência variável. Além disso, demonstra que um sinal de entrada não só é devidamente digitalizado, mas também transladado para cima e para baixo na frequência, incorporando na prática a operação de mistura num ADC. Como resultado, ADCs em cadeias de recepção podem assim executar uma dupla tarefa, tanto como quantizador como estágio de mistura. A menos conhecida topologia de partilha de carga (CS), dentro dos ADC de registo de aproximação sucessiva (SAR), é usada para a implementação prática, dada a sua caracteristica de "pré-carregamento" do sinal de referência antes da conversão se efectuar. Resultados de simulação de um ADC CS-SAR de 8-bits projectado numa tecnologia CMOS de 0.13 µm validam a técnica proposta.

Palavras-chave: Conversor analógico-digital (ADC), partilha de carga (CS), conversão para baixo, registo de aproximações sucessivas (SAR), receptores rádio, referências variáveis

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Acronyms

ΣΔM	Sigma-Delta Modulator.
ADC	Analog-to-Digital Converter.
BB	Baseband.
BER	Bit Error Rate.
BPΣΔM	Bandpass Sigma-Delta Modulator.
CR	Charge-redistribution.
CS	Charge-sharing.
CT	Continuous Time.
DAC	Digital-to-Analog Converter.
DCR	Direct Conversion Receiver.
DNL	Differential Non-Linearity.
DSP	Digital Signal Processor.
DT	Discrete Time.
DUT	Device Under Test.
ENOB	Effective Number of Bits.
ESD	ElectroStatic Discharge.

FFT	Fast Fourier Transform.
FIR	Finite Impulse Response.
FOM	Figure-of-Merit.
GBW	Gain Bandwidth Product.
GSM	Global System for Mobile Communications.
IF	Intermediate Frequency.
IIP	Input Intercept Point.
INL	Integral Non-Linearity.
LNA	Low Noise Amplifier.
LNTA	Low Noise Transconductance Amplifier.
LO	Local Oscillator.
LSB	Least Significant Bit.
MDAC	Multiplying Digital-to-Analog Converter.
MSB	Most Significant Bit.
NF	Noise Figure.
OFDM	Orthogonal Frequency Division Multiplex.
OpAmp	Operational Amplifier.
PAPR	Peak-to-Average Power Ratio.
PFD	Phase Frequency Detector.
PLL	Phase-Locked Loop.

RF Radio Frequency.

S/H Sample-and-hold.
SAR Successive Approximation Register.
SDR Software-Defined Radio.
SFDR Spurious-Free Dynamic Range.
SNDR Signal-to-Noise-plus-Distortion Ratio.
SNR Signal-to-Noise Ratio.

THD Total Harmonic Distortion.

VCO Voltage-Controlled Oscillator.

Chapter 1

Introduction

1.1 Motivation

There is an increasing demand for flexible mobile terminals capable of accommodating various functions together, either already existent or currently under development. Transceivers within these terminals should achieve this without an increase in cost and area. Software-Defined Radio (SDR)s aim to ease the design of such transceivers, by having a highly reconfigurable and programmable hardware controlled by software [1, 2].

One of the goals of a SDR is to move the ADC the closest possible to the antenna, as shown in Fig. 1.1, capable of dealing with a wide frequency band and accommodate several standards, like Global System for Mobile Communications (GSM) and WiFi.

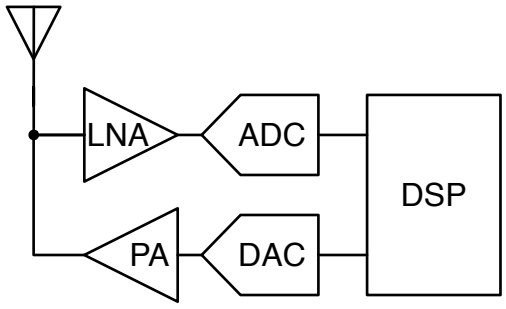


Figure 1.1: Software-Defined Radio Model, based on [1].

Following this idea, the Radio Frequency (RF) front-end (mainly the antenna and the Low Noise Amplifier (LNA)) should have a wide bandwidth and reasonable gain. Moreover, a good matching is required for all the spectrum in which the receiver operates, which is not as easy to do as with narrowband applications. One solution could be the use of wideband LNAs with multiple narrowband inputs, thus lowering the noise, but with a complex design resulting in higher area and overall cost [3]. On the other hand, RC LNAs have a very simple and inherently wideband design, but the Noise Figure (NF) is a serious predicament. In recent years wideband LNAs with noise and distortion cancelling designed with passive loads have been proposed, at the expense of high power consumption [4].

Another design challenge behind a wideband receiver relies on the fact that since it is fully exposed to the spectrum, it is subjected to several out-of-band interferers who have a direct impact on the dynamic range, Signal-to-Noise-plus-Distortion Ratio (SNDR) and Bit Error Rate (BER) of the system. In order to cope with this, techniques such as N-path filtering [5] and N-path mixing [6] have garnered significant attention in recent years.

When implementing a system in the SDR direction, different architectures have been exploited, such as the homodyne, superheterodyne and low-IF receiver chains. Another technique, called subsampling, can also be used. In the last decade, some works suggest that connecting the antenna directly to a passive mixer without an RF LNA can provide significant benefits, such as extremely low power [7] or greatly increased tuning range and linearity [8]. Improved passive mixing with embedded filtering low-IF architectures are also being pursued, such as the case of [9], in which, MOS parametric amplification provides additional gain in the RF signal path.

At the same time, various sampling techniques [10] including one where a Sigma-Delta Modulator ($\Sigma\Delta$M) operates at non-DC frequencies (behaving as a bandpass filter rather than a lowpass) [11] have been presented as solutions for an SDR. However, $\Sigma\Delta$Ms suffer from limited dynamic range and in many cases also from excessive power consumption.

As demonstrated in [12], the ADC block is of paramount importance and a key component in any SDR, as it performs the task of sampling the input signal and deliver such samples to the Digital Signal Processor (DSP) side of the receiver. For a SDR receiver, this

block's specifications become even more demanding in terms of bandwidth, noise and distortion, as it should be capable of covering a wide spectrum with unwanted interferers and blockers.

In earlier architectures, the ADC was usually placed after a series of blocks such as the LNA, mixing stages and RF filters. As a result, these blocks would have a more critical NF as the input signal is more sensitive to the noise contribution of earlier stages, according to the Friis formula. However, in a SDR implementation, the noise contribution of the ADC becomes inherently more significant to the Signal-to-Noise Ratio (SNR).

Moreover, the input signal cannot exceed the dynamic range of the ADC, or else clipping occurs, resulting in an output signal with a large error, leading to a degradation of the SNR. This is more noticeable in standards that employ multi-carrier transmission schemes to support their physical layer, such as Orthogonal Frequency Division Multiplex (OFDM), who present large peak-to-average values, commonly measured by Peak-to-Average Power Ratio (PAPR).

Also, the sampling clock of the ADC is typically generated using a Phase-Locked Loop (PLL). The phase noise characteristic of this PLL is critical as well, as it contributes to the displacement of the sampling clock edges from the ideal locations leading to sampling errors. This timing jitter is also more critical in high-speed ADCs, limiting its effective resolution [13].

The distortion introduced by non-linearities in the ADC is also a factor that must be taken into account, as the high-power harmonics cannot be ignored and severely impact the Total Harmonic Distortion (THD), and subsequently the SNDR. The two major types of non-linearity errors in ADCs are the Differential Non-Linearity (DNL) and Integral Non-Linearity (INL).

Moving the ADC closer to the antenna, if anything, will worsen the impact of each of these issues. Furthermore, the most obvious way of bringing the ADC to the frontend of the receiver would be to increase its sampling frequency and resolution, both of which increase power consumption and given current state-of-the-art technology limitations, this option remains impractical.

1.2 Research Question & Hypothesis

Through the work done in this thesis, the candidate aims to answer the following research question:

> *Due to its intrinsic characteristic of an analog voltage divider, can an ADC be used to embed a downconversion stage (mixer) of a traditional superheterodyne receiver chain, while simplifying/optimizing it in terms of power, noise, linearity and chip area?*

This research question can be addressed considering the following hypothesis:

> *Since there is no mandatory reason to use a constant reference signal in the ADC, if this signal is split into a constant term and a signal term provided by a Local Oscillator (LO), it is possible for an ADC to embed the mixing function, simplifying the hardware requirements of a receiver chain (through the elimination of the mixer), thus lowering its power consumption and chip area while reducing noise and improving linearity.*

1.3 Original Contributions

The major contribution of this work is the development of an ADC capable of operating as both a quantizer and downconverter, with the latter function being entirely made possible through the use of variable reference signals.

Being the first of its kind (to the best of the author's knowledge) the viability of this approach, weather it being theoretical or the physical implementation itself, had to be confirmed. As such, a complete mathematical analysis was done initially, together with the design and simulation of a high-level receiver model. The results of this work were published in [14].

Given the approach's particularity of the use of a variable reference signal, not all conventional ADC architectures can be considered candidates for its use. The Pipeline architecture's feasibility in particular, was investigated in the early stages of this work. Some of the conclusions drawn were published in [15]. Furthermore, still in the field of Pipeline ADCs, a mismatch-insensitive 1.5-bit Multiplying Digital-to-Analog Converter

(MDAC) with unity feedback factor was also proposed, envisaging significant power savings through the combination of three particular techniques, which can be found in [16].

Settling on the use of a Charge-sharing (CS)-Successive Approximation Register (SAR) architecture for the circuit-level implementation, an 8-bit ADC was designed, coupling the proposed technique with the subsampling approach. In this fashion, the sampling frequency requirements for the ADC can be relaxed, whilst reducing the out-of-band noise density at the output, when compared to pure subsampling implementations. Circuit-level simulations yielded a performance compatible with near 8-bits of effective resolution. These results were published in [17]. Furthermore, it should be stated that some blocks within the designed ADC, such as the comparator, where sized following the design methodology proposed in [18].

The list of publications that are a direct result of the work developed during this thesis is summarized next:

[14] — **N. Pereira**, J. Goes, L. B. Oliveira, and R. Dinis. "Analog-to-Digital Converters with embedded IF mixing using variable reference voltages." In: 2014 IEEE International Symposium on Circuits and Systems (ISCAS). 2014, pp. 89–92. DOI: 10.1109/ISCAS.2014.6865072

[15] — J. Goes and **N. Pereira**. "Low-Power, High-Speed and High-Effective Resolution Pipeline Analog-to-Digital Converters in Deep Nanoscale CMOS." In: High- Performance AD and DA Converters, IC Design in Scaled Technologies, and Time-Domain Signal Processing. Edited by P. Harpe, A. Baschirotto and K. Makinwa. Springer, Cham, 2015, pp. 3–24. DOI: 10.1007/978-3-319-07938-7_1

[16] — **N. Pereira**, J. Goes, M. Rodrigues, and P. Faria. "A new mismatch-insensitive 1.5-bit MDAC with unity feedback-factor and enhanced performance." In: 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS). 2014, pp. 375–378. DOI: 10.1109/ICECS.2014.7050000

[17] — **N. Pereira**, H. Serra, and J. Goes. "A two-step radio receiver architecture fully embedded into a charge-sharing SAR ADC." In: 2017 IEEE International

Symposium on Circuits and Systems (ISCAS). 2017, pp. 1–4. DOI: 10.1109/ISCAS.2017.8050563

[18] — J. L. A. de Melo, **N. Pereira**, P. V. Leitão, N. Paulino, and J. Goes. "A Systematic Design Methodology for Optimization of Sigma-Delta Modulators Based on an Evolutionary Algorithm." In: IEEE Transactions on Circuits and Systems I: Regular Papers 66.9 (2019), pp. 3544–3556. DOI: 10.1109/TCSI.2019.2925292

Additionally, a prospective journal paper disclosing the results obtained from an 8-bit fully-differential CS-SAR ADC, coupled with a signal PLL that generates the variable reference on-chip, was submitted and accepted (pending some corrections) at the International Journal of Circuit Theory and Applications (IJCTA), being on the final stages of publication at the time of writing of this thesis. The submitted document can be found in appendix A and contains much of the results disclosed in chapter 5.

1.4 Thesis Outline

This thesis is organized in 6 chapters, including this Introduction. The remaining chapters can be resumed as follows:

Chapter 2 presents a comprehensive literature review of radio receivers and the most usual ADC architectures used on them. First, the more traditional approaches in the design of a receiver chain are detailed, such as the Superheterodyne and Homodyne topologies. This is followed by a discussion of recent concurrent techniques and designs, such as Subsampling and Mixer-first. Advantages and challenges behind each one are also given. Afterwards, a brief explanation of the most basic analog-to-digital conversion concepts is given, before a more in-depth analysis on each architecture commonly used in radio applications is made. These include, but are not limited to, the SAR topology. In it a distinction is made between the Charge-redistribution (CR) and CS principles. The chapter ends with a comparison between ADC architectures, taking into account their respective advantages and downsides;

Chapter 3 expands further on the CS-SAR ADC. Its mode of operation is explained, together with the effects of non-idealities, such as comparator noise and offset or mismatch between capacitors, on the overall performance of the converter. Different alternatives for the switching scheme in the Digital-to-Analog Converter (DAC) array are presented, in order to reduce its impact on the overall area. Next, a brief review of the reported CS-SAR ADC in literature with measurement results is made;

Chapter 4 describes the proposed embedded mixing technique from a mathematical point of view, where equations are drawn that prove its viability. It being a significant shift from traditional "static" references, a set of considerations on a number of design challenges are also drawn. Taking into account the unique requirements behind the proposed technique, choosing the right ADC architecture to implement it is key. Bridging the gap between this chapter and the previous, the main reasons behind the adoption of the CS-SAR topology as the architecture of choice are also presented here;

Chapter 5 focuses on the design of a complete 8-bit fully-differential CS-SAR ADC that resorts to the proposed embedded mixing technique to operate as both a quantizer and a downconverter. Since a common and reasonable question behind the proposed technique is the implementation of the variable reference signal, the design includes a integer-N PLL that provides a on-chip solution. The layout considerations are also disclosed. Post-extraction simulations show that the proposed ADC is able to reach 8-bits of effective resolution whilst operating at a moderate speed of 50 MS/s, while also effectively downconverting a high-frequency signal;

Chapter 6 briefs the document's conclusions and points out the direction for future work.

Chapter 2

Literature Review

In this chapter, a brief overview of receiver architectures and conventional ADC structures is made. In Section 2.1, the basic Homodyne and Heterodyne architectures are presented, together with a brief distinction between Narrowband and Wideband receivers. This is followed by a discussion of emerging trends, such as the Mixer-first solution or the MOS Parametric Amplification technique. The below Nyquist's rate approach, more commonly known as Subsampling, is also detailed.

Section 2.2 focuses on the ADC block, its main performance limitations and how each architecture is better applicable to a radio receiver. Some of the discussed architectures are the Pipeline and SAR ADC. A greater detail on CS-SAR ADCs is given in chapter 3, since it is the architecture of choice for the implementation of the proposed approach in this work.

2.1 Receiver Architectures

Modern day battery-powered handheld devices are expected to support a wide variety of radio technologies. At the same time, high data rates with reduced latency must be guaranteed, while keeping in mind production costs. These specifications become even more challenging with the advent of 5G, scheduled to have 1.9 billion subscribers by the end of 2024, with over 10 million subscriptions projected worldwide until the end of the present year of 2019 [21].

Traditional receivers, which were designed taking into account specific standards, would pick up a *narrowband* signal, resorting to dedicated SAW filters to suppress out-of-band noise and interference [22]. Now, the research focus is on SAW-less *wideband* receivers (with maximum hardware reuse in mind) capable of withstanding broadband noise and high-power blockers [23]. The latter becomes even more of an issue when considering low-voltage constraints of ultra-scaled CMOS.

Conventional radio receivers (starting in the early 20^{th} century) typically employ one of two techniques: the homodyne and heterodyne designs. Regardless of the one chosen, there are usually three core building blocks in these receivers: the LNA, the Mixer and the ADC, in this particular order (with some in between/embedded filtering). The LNA amplifies the low-power signal received at the antenna, which is subsequently shifted to a lower frequency (not necessarily Baseband (BB)) than that of the carrier by the Mixer and finally digitized by the ADC in order to be processed by a DSP.

For a digitally encoded signal, the RF receiver typically employs digital filters within a DSP to perform the demodulation of such signal. In order to retain both the amplitude and phase of the RF signal, two mixers are used: one for the in-phase (I) and another for the quadrature (Q) BB output. Hence, quadrature down-conversion is needed since two sideband generally form around any RF carrier frequency. Thus, for a digitally encoded signal, a single mixer is not enough as this would result in the loss of one of the sidebands. Instead, an I/Q demodulator is required, in order to demodulate the information contained in both I and Q signal components [2].

2.1.1 Superheterodyne

Superheterodyne receivers, proposed by Armstrong in 1918 [24], characterize themselves by incorporating at least two mixing stages. In other words, there will be several mixers, filters, LOs and amplifiers in a single receiver chain, as depicted in Fig. 2.1. This increase in stages carries with it higher selectivity and sensitivity. Here, the first LO generates a signal with a frequency that is offset by a fixed amount from the desired signal, giving rise to an Intermediate Frequency (IF). The IF is a heavily critical parameter in the superheterodyne architecture, as both image and interferer issues can be more or less suppressed according to it [25].

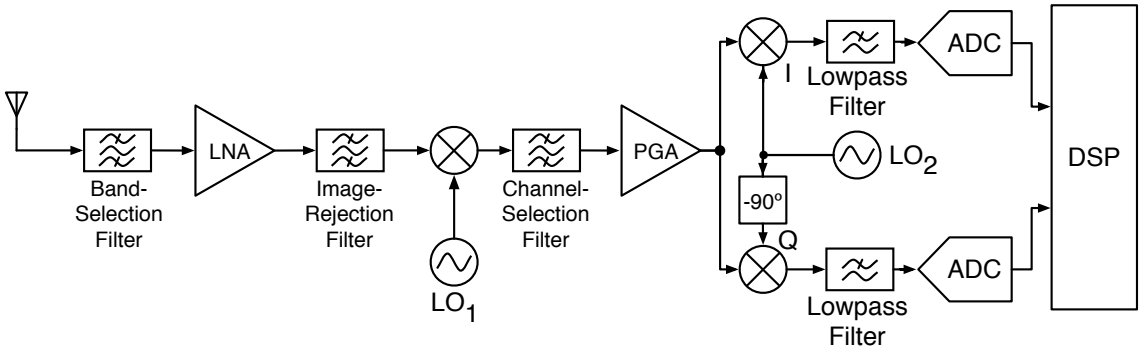


Figure 2.1: Superheterodyne Receiver.

The image issue is an unwanted signal present at the output of the mixing stage, originated from the fact that two different input frequencies can produce the same IF. This stems from the fact that the mixed frequencies give rise to a term that is the sum of the two, and another that is the difference. If the image power is higher than the desired signal power, it may cause resolution challenges for the ADC [26].

To avoid this issue, it is common to find an image rejection filter placed before the mixer. If the IF is fairly high, this filter is easier to design and the image is suppressed. However, interferers should not be disregarded, since they too are down-converted to IF. To remove them, a channel select filter can be employed. But in this case, it is preferable to use a lower IF, as it reduces the demand on such filter and relaxes the requirements for the ADC. Hence, there is an important trade-off when choosing IF [26, 27].

The distortion caused by interferers is even more critical when wideband receivers are considered, as selective RF pre-filtering cannot be performed prior to downconversion since it would limit their operating frequency range. To cope with this, it is customary to use harmonic-reject mixers, with recent works [28] showing that non-uniform LO phase spacing can yield better gain and phase mismatch robustness over equally spaced LO phases.

The main advantage behind the use of a Superheterodyne approach resides on the fact that DC offsets and flicker noise do not interfere heavily with the signal.

2.1.2 Homodyne

Conversely, the Homodyne receiver, also known as Zero-IF or Direct Conversion Receiver (DCR), directly converts the incoming RF signal to a much lower BB frequency recurring to a single mixing stage, as shown in Fig. 2.2. This frequency translation is achieved by mixing the RF signal with a LO signal with an identical (or nearly identical) frequency (hence the name "homodyne").

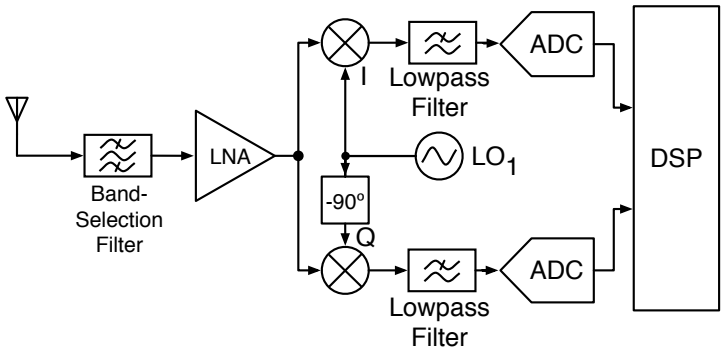


Figure 2.2: Homodyne Receiver.

In this approach, the receiver design is greatly simplified, as it only requires a single mixing stage. Also, it circumvents the image problem, as opposite to the heterodyne approach, since the LO frequency is equal to that of the carrier. With a direct down-conversion it is also customary to use lowpass filters after the mixing stage to remove unwanted high frequency components.

However, homodyne receivers present several issues, caused primarily by LO leakage, in which the LO energy is coupled to the I/Q demodulator either through the antenna or another path, hence creating a DC offset signal, and various noises sources at DC, like flicker ($1/f$) noise [2, 27].

Still, given the current interest in pursuing multi-mode and multi-band receivers, the DCR has garnered enormous attention. This is due to the fact that it enables low power consumption, maximum hardware sharing between RF and BB sections, has an easy and flexible frequency planning and allows for the use of minimal external components [10].

2.1.3 Low-IF

In the interest of designing an architecture that combines the advantages of the aforementioned receivers and tries to avoid their disadvantages, the Low-IF architecture presents itself as a special case of the superheterodyne receiver. Illustrated in Fig. 2.3, it is capable of effectively rejecting the image without using filters, while mitigating the disadvantages of the homodyne receiver (DC offsets, $1/f$ noise, etc) at the same time.

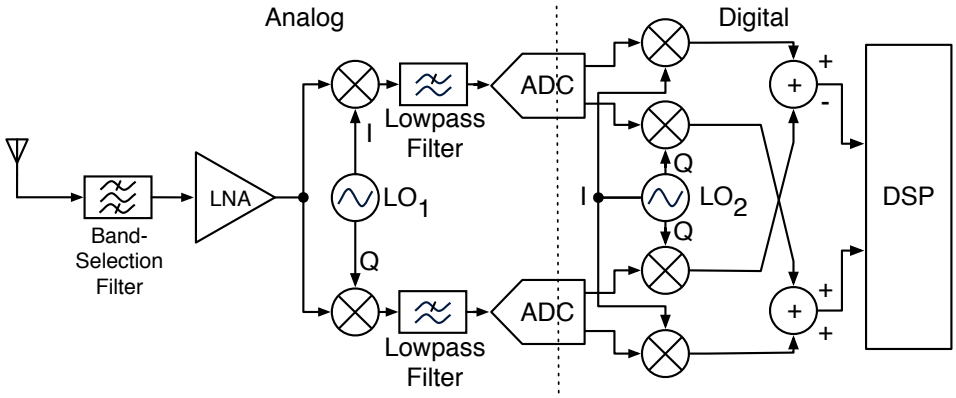


Figure 2.3: Low-IF Receiver, adapted from [29].

As stated before, quadrature carriers are necessary in modern modulation schemes, and in low-IF receivers they have an additional use: image rejection. To do so, two image reject mixing techniques, proposed by Hartley [30] and Weaver [31], can be used. But this image rejection might be incomplete due to any un-balance between the I and Q signal paths (both in phase and amplitude), i.e. "I-Q mismatch", translating into distortion leading to a degradation of the SNDR/BER of the receiver.

Regardless of the structure adopted, in multiband systems with a wide range of frequencies to process, significant design constraints are imposed on the receiver front-end. One of the options is to use several front-ends arranged in parallel, tuned to each frequency standard, using distinct matching networks and narrowband LNAs [32], at the cost of hardware reuse.

In alternative, wideband LNA with impedance matching and reasonable NF (below 3 dB) have been proposed in the last decade, most notably [33] that uses an amplifier with resistive feedback and [4] that resorts to a common-gate-common-source topology to achieve noise cancellation of the common-gate stage, provided accurate matching.

In [34] a zero-IF SDR with harmonic recombination and split front-end is presented,

being capable of effectively rejecting blockers present at third and fifth harmonics of the input frequency by over 70 dB, with the aid of tuned Gm-cells. Also a high second-order Input Intercept Point (IIP) and out-of-band third-order IIP are obtained through calibration. The combination of these techniques allow for the receiver to be completely SAW-less. Still, *gm-C* biquads are power hungry blocks due to their high Gain Bandwidth Product (GBW) and scale poorly with low power supplies in nanoscale CMOS technologies.

A Discrete Time (DT) Superheterodyne receiver is presented in [35], where the signal is sampled at four times the LO frequency. This is done in order to avoid any aliasing up to three times the carrier frequency. Although the circuit is capable of achieving competitive NF and gain, the area and power consumption are still quite relevant.

Recently, a SAW-less superheterodyne architecture with harmonic rejection was proposed in [36]. As opposed to [34], no calibration is required. Instead, a octal charge-sharing bandpass filter coupled with cascaded harmonic-rejection stages, lead to a robust filtering of images and both in-band and out-of-band blockers. Also, the use of a highly linear wideband LNA allows for a high third-order IIP and a borderline competitive NF. Still, the LNA amounts for 25-to-40 % of the power consumption in the overall receiver.

Overall, these designs still require significant amounts of power to operate at RF frequencies as well as significant area usage, despite the absence of SAW filters. The LNA proves itself to be one of the key contributors to the overall power and there is a clear trend on forgoing active mixers in favour of passive ones in order to achieve acceptable linearity.

2.1.4 Emerging Techniques

From the 20^{th} century onwards the core idea behind both homodyne and heterodyne designs (i.e. the core structure) remained as an LNA-Mixer-ADC set in that specific order. Recent advances in radio receivers however, prove that there is great benefit in shifting these blocks around and sometimes even renouncing one of them. As such, this section presents some of the most well-renowned approaches that fall outside of the traditional receiver scheme.

2.1.4.1 A) Mixer-first Receivers

Looking at the DCR structure, one could assume that under proper circumstances a mixer coupled with an LO would suffice. Being the most power-hungry stage of a radio receiver, the RF front-end can greatly benefit from the removal or shifting of the LNA to BB as shown in 2.4, in terms of power consumption, tuning range and linearity.

The usage of passive mixers further enhances power savings and also leads to severely low flicker noise (one of the key downsides of zero-IF architectures), since there is no DC current flowing [37]. Moreover, with gate lengths reaching ever smaller dimensions, these passive mixers can operate at higher frequencies with better linearity, which is an increasingly challenging feature in modern day radio receivers. However, passive mixers pose the issue of conversion loss, which leads to lower SNDR.

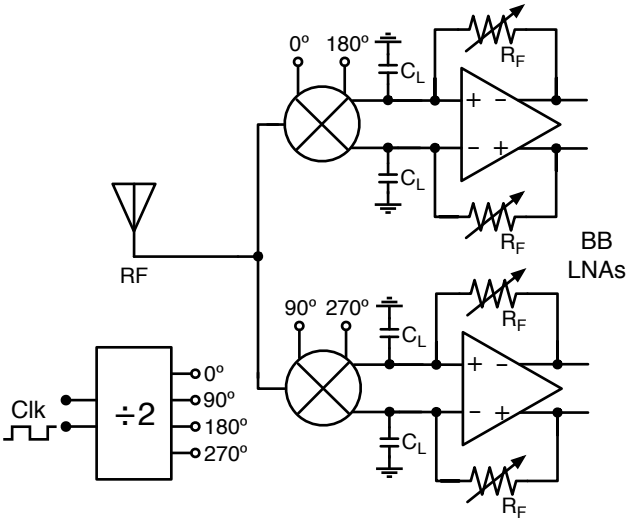


Figure 2.4: Example of a 4-Path Mixer-First receiver, where the LNA has been moved to operate in BB.

In the context of current-driven passive mixers, a detailed analysis [38, 39] shows how to optimize a mixer-first front-end for maximum gain and minimum NF, by properly deriving the downconversion transfer function (TF). It is mathematically derived why passive mixers driven with 25% duty-cycle quadrature clocks present significant advantages over 50% ones, such as unequal high- and low-side conversion gains, unexpected second-order IIP and third-order IIP numbers, and IQ crosstalk.

In [7], a 130 nm 2.4 GHz transceiver with fully passive front-end is designed, completely removing the LNA from the structure, which operates between a low-IF and

zero-IF scheme. The usage of a quadrature sampling Mixer allows for very low power consumption as well as image rejection and even-order cancellation. The use of quadrature clocks helps in coping with conversion loss, as an increase in gain by 3 dB is achieved. The DCR circuit proposed in [8] further expands on that, by carefully tuning the mixer core for high linearity and low NF.

In [40, 41], a passive-mixer-first LNA-less receiver front end is presented. Thanks to N-path filtering and its transparency property (i.e., capacity to pass the impedance presented at one port to the another) the receiver has a reasonable input impedance matching across the spectrum and high out-of-band third-order IIP (+25 dBm), but at the expense of NF. This is due to the lack of an LNA block. Furthermore, the noise generated by the BB amplifiers end up dominating and there is also the chance of large LO feed-through to the antenna.

A mixer-first exploiting negative conductance is presented in [42], in such a way that the distortion currents induced by the finite operational amplifier (OpAmp) gain can be cancelled. This leads to a significant improvement of the in-band third-order IIP (over +20 dBm) of the receiver. However, this comes at the expense of NF and power consumption.

In [43] a noise-cancelling receiver consisting on two paths, main and auxiliary, is proposed. The noise contribution of the mixer-first main path can be cancelled after being subtracted from the auxiliary path, which contains a gm-block. The noise generated by the G_m stage in the auxiliary path is the only significant noise source of the receiver. As a result it has a reported NF below 2 dB and a 0-dBm blocker NF of 4 dB, for a 1.3 V supply.

2.1.4.2 B) MOS Parametric Amplification

The main issue with a passive mixer approach, coupled with a removal of the LNA, is that the RF front-end shows a severe lack of amplification of the low-power signal. This becomes more critical due to the conversion losses introduced that further compromise the SNR of the complete receiver.

One technique that deals with this issue is the MOS Parametric Amplification, where at its core a MOS transistor has its drain and source shorted together and thereby operates as a three-terminal MOS variable capacitor (varactor). The concept of varactors, in the

field of parametric amplification, was studied in detail in 1948 by Van der Ziel [44]. In 1957, the parametric amplification principle was applied in a solid-state continuous-time microwave amplifier, and experimentally demonstrated by Suhl [45] and Weiss [46]. Since then, a few implementations were reported, using diodes as the variable reactances connected in distributed electromechanical structures. A good example is the travelling wave parametric amplifier designed in 1969 [47].

Almost three decades later, it was demonstrated that to control the oscillation frequency, junction diodes are inferior to MOS varactor devices [48, 49]. These have a wide capacitance range, since complementary structures (N-type and P-type) are available, and three-terminal operation with non-intrusive biasing is possible. Taking advantage of the fact that a voltage sampled at the gate of a MOS capacitor rises when the channel charge is withdrawn, it is possible to achieve moderate gain in the signal path and improved noise performance.

In 2003, a DT low-gain amplifier using parametric amplification has been described [50], in which a three-terminal MOS varactor has been used. This is the natural choice for analog and mixed-signal building blocks, as was demonstrated by the implementation of a complete switched-capacitor (SC) finite-impulse-response (FIR) filter [51], where two complementary MOS varactors, each composed by an NMOS-PMOS transistor pair, are arranged in a anti-parallel fashion, with their respective sources connected to their drains. Using a two-phase scheme where the devices operate in two different regions (strong inversion and depletion), the overall capacitance decreases. Hence, the charge left in the sampling capacitor is reduced, yielding a voltage gain of at least 6 dB in the mixer.

Other building blocks for analog signal processing have been proposed since [9, 52–54]. All practical realizations of the DT parametric amplification concept are, so far, limited to low to moderate frequencies [50, 51], using only mature CMOS technologies. Examples are the passive SC mixer in [9] and the Nyquist-rate pipeline ADC in [54]. In [9] the structure is slightly modified with the NMOS and PMOS capacitors being placed in parallel and the drains no longer connected to the sources. Instead, floating terminals are used (as shown in Fig. 2.5) to make the overall parametric amplifier more parasitic-insensitive, reducing the loading effects. This results in a structure that improves on the results by 3 to 4 dB on the gain and by 1 to 2 dB in the NF.

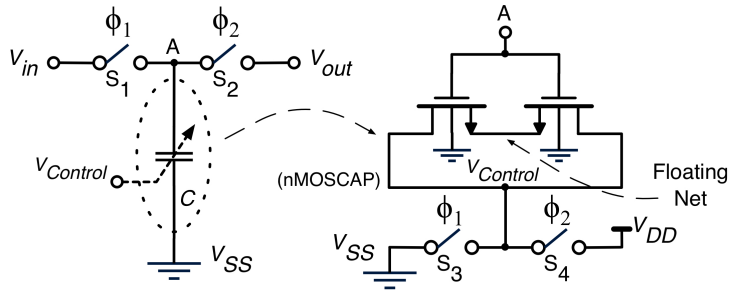


Figure 2.5: MOS parametric amplifier using two separated devices with a floating terminal, adapted from [9].

Despite the advantages in terms of gain boosting and noise reduction, the adoption of this parametric amplification approach inevitably leads to more power consumption, when compared to standard passive mixing stages, with it being a significant drawback. Furthermore, the MOS varactor amplification region is rather limited, yielding a reduced input dynamic range.

2.1.4.3 C) Subsampling

Another technique called subsampling (also known as undersampling or bandpass sampling) can be used, with the advantage of greatly relaxing the requirements for the ADC and potentially removing the Mixing stage altogether. This is detailed next.

From the Nyquist criterion it is known that for a signal to be properly digitized, i.e. without loss of information, it must be sampled at a rate of at least twice the bandwidth of the signal itself. Hence, if a signal with a certain center frequency B_{RF} and bandwidth BW is considered, it is not mandatory for the sampling rate f_s to be of at least twice the center frequency. Instead, by using a sampling rate that is far smaller than the Nyquist rate but only slightly above two times the bandwidth of the modulated signal, i.e. 2BW $< f_s \ll 2B_{RF}$, the sampling rate requirements for the ADC can be greatly relaxed. This is the premise behind the subsampling approach.

The subsampling receiver, illustrated in Fig. 2.6(a), consists on a Sample-and-hold (S/H) circuit preceding the ADC that samples the incoming signal at a much lower rate than its carrier frequency, but higher than the bandwidth of the modulated signal itself. Consequently, the incoming RF signal can be down-converted to IF or directly to BB,

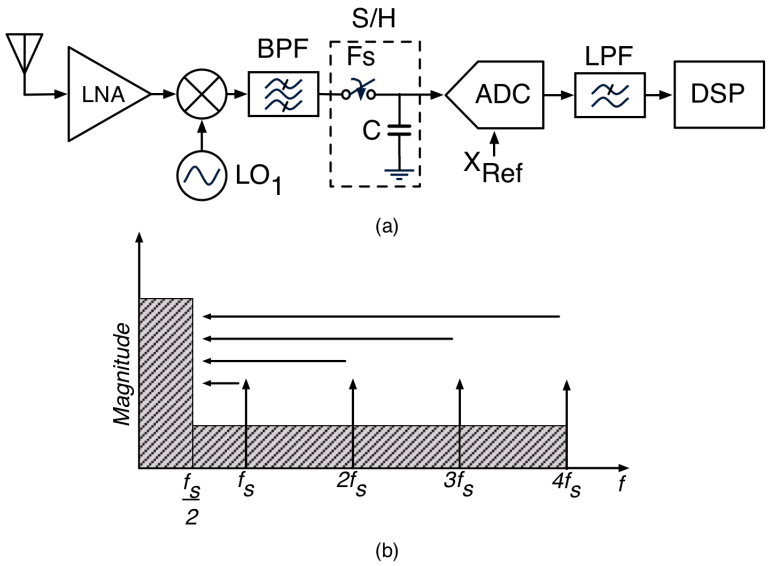


Figure 2.6: (a) Subsampling Receiver, adapted from [55] (b) Noise-folding effect.

eliminating the need for an additional mixer in the receiver chain. Nevertheless, the bandwidth of this sampling circuit must be at least equal to the maximum input signal frequency.

The frequency at which the signal is sampled is related to the its BW by the subsampling ratio m, defined as $m = \frac{BW}{2 \cdot f_s}$.

In addition, f_s should verify the following conditions in order to avoid image overlap:

$$\frac{2 \cdot f_H}{n} \leq f_s \leq \frac{2 \cdot f_L}{n-1}, \tag{2.1}$$

where n is the integer given by

$$1 \leq n \leq \frac{f_H}{f_H - f_L} = \frac{f_H}{BW}, \tag{2.2}$$

where f_H and f_L represent the upper and lower band frequency, respectively [56]. This limitation of f_s to a certain range of values ends up imposing certain design constraints.

Subsampling degrades the SNR essentially due to two main reasons that escalate with the m used:

- Firstly, the higher m is (i.e., a subsequent lower f_s), more out-of-band noise (from DC to the input analog bandwidth of the ADC) is aliased into the BB, increasing its density at the output (Fig. 2.6 (b)) by a factor of $2m$ [26, 57]. This effect is commonly

named noise-folding. One of the major noise sources here is the kT/C noise added by the sampler itself.

- Moreover, there is a high sensitivity to the timing jitter associated with the sampling clock [58], as it can be shown that the clock phase noise power is "amplified" by a factor of m^2 [59].

These shortcomings can by dealt with, but with the added cost of designing high-Q filters to be used before sampling and selecting low phase noise oscillators, to limit the out-of-band noise and the timing jitter respectively.

2.1.4.4 D) Bandpass Sigma-Delta Modulator

Whatever the architecture chosen for it, the ADC commonly used in a receiver operates at DC, being thought of as a BB device. Still, there is no particular reason for why it cannot be used in higher frequencies, being particularly useful in IF-to-digital conversion.

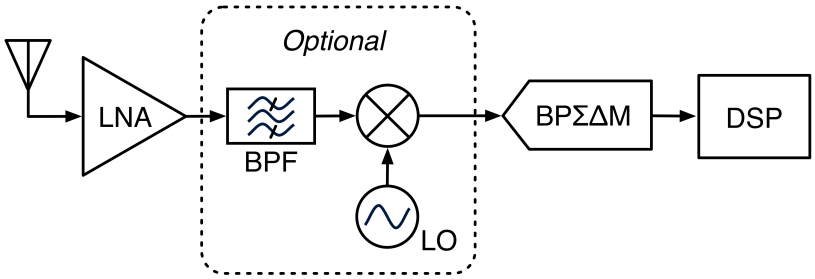


Figure 2.7: Example of a Receiver where the ADC operates directly at IF.

As such, the use of Bandpass Sigma-Delta Modulator (BPΣΔM) [60] has garnered particular attention in recent years, due to the noise-shaping feature of the ΣΔM architecture itself. With it it's possible to push the quantization noise up and down in frequency and thereby leave an (ideally) "noise-free" region for the signal. In practice a signal centered at the frequency f_c applied to a noise-shaping loop operating at a f_s sampling rate results in a digital output placed at $f_s - f_c$. An inherent advantage of operating at higher frequencies is the fact that the impact of $1/f$ noise becomes negligible.

Continuous Time (CT) implementations have significant advantages over their DT counterparts, such as low power consumption and supply voltage, high sampling frequency and bandwidth and inherent anti-aliasing filtering, which removes the need for

an explicit anti-alias filter (AAF). As such, CT-BPΣΔM are preferably used, despite their higher sensitivity to jitter and process variations. Also, in these architectures the noise generated by the loop filter as well as in the DAC is critical and must be minimized.

The sampling frequency f_s of a BPΣΔM is usually chosen to be 4 times the center frequency f_c, although higher f_s can be used in order to improve the SNDR. Still, due to the high frequencies involved, these ADCs were commonly implemented in SiGe BiCMOS technologies in the early 2000's. For a CMOS implementation the use of subsampling becomes a viable solution.

In [11] an undersampled CT-BPΣΔM implemented in 130 nm CMOS and operating over the industrial, scientific and medical (ISM) bands is proposed. As with most SDR architectures, it uses LC-tank resonators, as these are more suitable for high frequency applications. Here the authors propose the use of a raised-cosine feedback DAC to cope with a reduction on the quality factor of the noise transfer function. However, this approach yields a more complex design, as the loop filter coefficients increase making the modulator even more sensitive to technology process variations.

The flexibility of this approach can be limited if the modulator and filter are designed for a specific f_c, which forces the RF receiver of a SDR to use a programmable frequency synthesizer in order to place the signal band within the operating frequency range of the BPΣΔM. This led to the development of reconfigurable BPΣΔMs with a tunable notch frequency.

In [61] a second-order reconfigurable BPΣΔM with a 0.8-to-2 GHz tunable notch frequency and 41 mW power consumption is presented. The loop filter is integrated together with a quadrature PLL (which consumes slightly above 25 % of the power of the overall modulator) to allow quadrature phase synchronization between a raised-cosine feedback DAC and the embedded quantizer. In [62] a synthesis methodology for the design of LC-based CT-BPΣΔM with programmable notch frequency is presented, with a tuning range from 0.1 f_s to 0.4 f_s.

One of the main issues behind the use of LC-tank resonators resides on their large silicon area and poor quality factor of on-chip inductors. An alternative, as proposed in [63], is the use of single-opamp resonators. Also, the use of a single DAC with duty-cycle-control reduces the number of DACs in the modulator. These enhancements lead to

significant power and area savings, but at the cost of tuning range which is only limited here to 40 MHz.

2.1.5 Summary

The current section presented the core fundamentals behind radio architectures for SDR applications. Although radio receivers have been around for decades, there is still a long path to follow until the SDR as envisioned in the 90's is achieved. To that end, several architectures can be used, with the homodyne and heterodyne approaches as options.

Recent trends have shown that DCRs, despite their disadvantages in terms of DC noise sources such as flicker, can be competitive in today's market when up against heterodyne designs. However, for a classic LNA-Mixer-ADC structure, the LNA proves to be a significant power hungry block. So, in the interest of power and area savings, alternatives that exclusively resort to a Mixer-ADC set have been exploited.

Passive Mixer-first solutions lead to significant power savings and improved linearity, with the added benefit of low $1/f$ noise. Their inherent downside, the absence of signal amplification, can be dealt with the use of parametric amplification at the expense of power consumption.

Another solutions, Subsampling and BP$\Sigma\Delta$M, aim to remove the Mixer stage from the receiver, leaving its operation to the S/H block or the ADC itself. In the former, the signal is undersampled, relaxing the ADC requirements but at the cost of noise-folding and increased sensitivity to the sampling clock jitter. In regards to the latter, BP$\Sigma\Delta$Ms resort to their loop filter and noise-shaping characteristics to both downconvert the signal and digitize it. The lack of flexibility in this approach led to an interest in the development of reconfigurable modulators with a tunable feature.

Despite the approach taken (homodyne or heterodyne), a mixing stage and filtering blocks are always required between the antenna and the ADC, making the SDR goal of moving the latter closer to the former still not a reality.

2.2 Analog-to-Digital Converters and their Applicability in Receiver Architectures

As stated in previous chapters, the ADC is one of the fundamental blocks in a receiver chain. Its main function is to convert the continuous-time, continuous amplitude signal at its input to a discrete sequence of digital words, by means of a sampler and a quantizer. The former performs time discretization while the latter does amplitude discretization. In the following section the main parameters and metrics that characterize an ADC (in general) are presented. This is followed by the discussion of several ADC topologies, together with their potential applicability to a SDR. Each of these topologies usually trades accuracy for speed, and as a result, some are more suited for high-frequency high-resolution designs than others.

2.2.1 ADCs Main Principles

An ideal ADC has a input-output transfer curve, assuming an uniform quantization, that can be represented by a staircase function. This is exemplified in Fig. 2.8, where a 3-bit ADC is considered, as an example.

Here, the sampled input signal of the ADC[1] is mapped to a corresponding digital output. The input signal range, bounded by the minimum value V_{min} and the maximum value V_{max}, is designated as the input full-scale range (FSR) of the ADC. For a B-bit resolution ADC, the FSR is divided into 2^B equally sized code bins. The change in voltage required to guarantee a transition from one code bin to the next is called the Least Significant Bit (LSB) voltage, V_{LSB}. Hence, these three quantities are related by Eq. 2.3.

$$V_{LSB} = \frac{\text{FSR}}{2^B} = \frac{V_{max} - V_{min}}{2^B} \tag{2.3}$$

It should be noted that ADCs don't have a one-to-one input-output mapping, meaning that several input voltages (within a certain interval, related to V_{LSB}) result in the same digital output. As such, every ADC has an inherent error denominated **quantization error**, which ideally should be bounded by $\pm\frac{1}{2}V_{LSB}$. This particular error, illustrated in

[1] ADCs can be designed for voltage or current signals at its input. For the sake of simplicity, henceforth we assume signals represented as voltages.

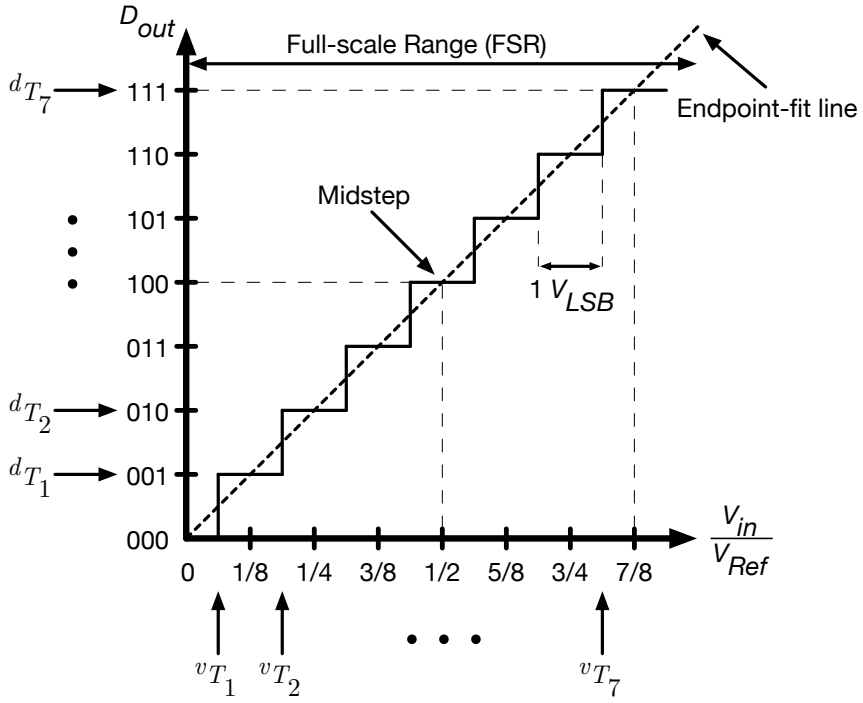


Figure 2.8: Input-output conversion characteristic of an ideal 3-bit ADC.

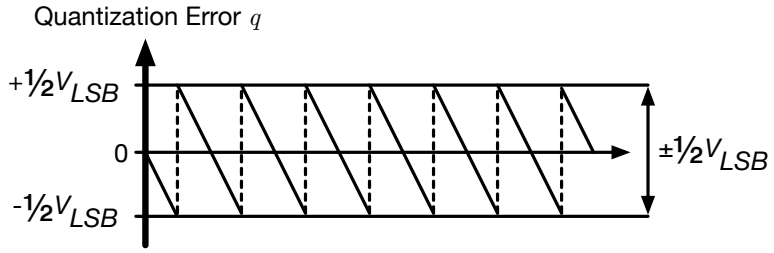


Figure 2.9: Quantization Error of an ideal 3-bit ADC.

Fig. 2.9, represents the difference between the staircase function and the endpoint-fit line in Fig. 2.8.

Under specific input voltages, such a ramp signal or a noisy sinusoidal wave[2], this quantization error q can be understood as a continuous random variable uniformly distributed between $\pm\frac{V_{LSB}}{2}$. In these circumstances, it follows that the root-mean-square (rms) value of the quantization error is given by Eq. 2.4.

$$q_{rms} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.4}$$

[2]Both these types of signals are commonly used to evaluate the static and dynamic performance parameters of an ADC, as discussed later on this chapter.

Considering that the rms value of a full-scale input sinusoidal signal is $\frac{\text{FSR}}{2\cdot\sqrt{2}}$, the maximum theoretical SNR for a B-bit ADC is given by Eq. 2.5.

$$SNR_{max} = 20 \cdot \log\left(\frac{\frac{\text{FSR}}{2\cdot\sqrt{2}}}{\frac{V_{LSB}}{\sqrt{12}}}\right) \simeq 6.02 \cdot \text{B} + 1.76 \qquad \text{(dB)} \tag{2.5}$$

Besides the SNR, an ADC can be characterized by several other performance metrics. These are usually split in two main groups:

- Static performance parameters which mainly inform on how accurate the actual ADCs transfer curve is when compared to the ideal one. These are usually measured using a DC, ramp or a low frequency signal. Examples are the offset and gain errors, as well as the differential and integral nonlinearities (DNL and INL, respectively);
- Dynamic performance parameters that evaluate the behaviour of the ADC as the amplitude or frequency of the input signal changes, since the components within the ADCs circuitry have finite bandwidth and can only process a finite set of amplitudes, bounded by (and usually just a fraction of) the supply rails. As a result, these are obtained through the use of high frequency input signals. Among them, the SNR, THD, Spurious-Free Dynamic Range (SFDR), SNDR and Effective Number of Bits (ENOB) are the most used.

2.2.2 Static Performance Parameters

Since the static performance is evaluated by the ADCs input-output conversion, a 3-bit ADC is again considered.

2.2.2.1 Offset Error

This error can be interpreted as the horizontal difference between the first transition level of a real ADC and its ideal counterpart. Graphically, the input-output characteristic is shifted horizontally from the ideal curve (Fig. 2.10), meaning that there is a slight deviation for a 0 V analog input. Its expression is given by Eq. 2.6.

$$\Delta_{offset} = \frac{v_{T_1} - v_{T_{1_{ideal}}}}{V_{LSB}} \qquad \text{(LSB)} \tag{2.6}$$

where v_{T_1} and $v_{T_{1_{ideal}}}$ represent the real and ideal initial transition of the ADC.

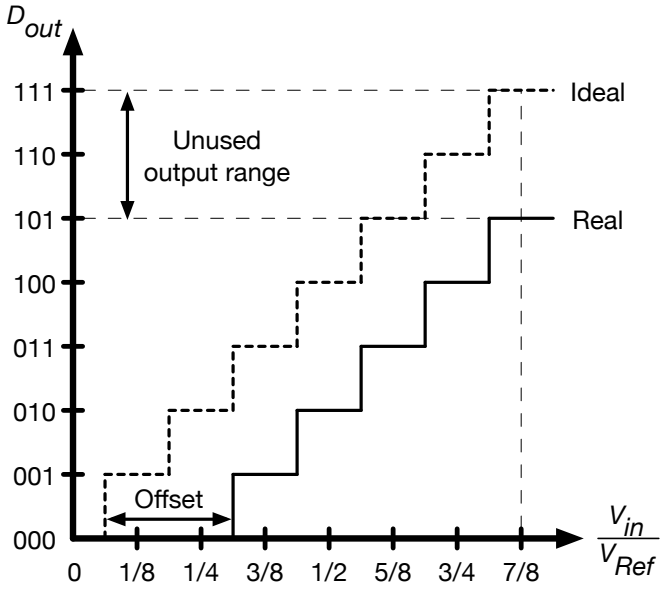


Figure 2.10: Offset Error (grossly exaggerated) in a 3-bit ADC.

2.2.2.2 Gain Error

This error is defined as the slope difference of the midpoint interpolating line in both characteristics (Fig. 2.11).

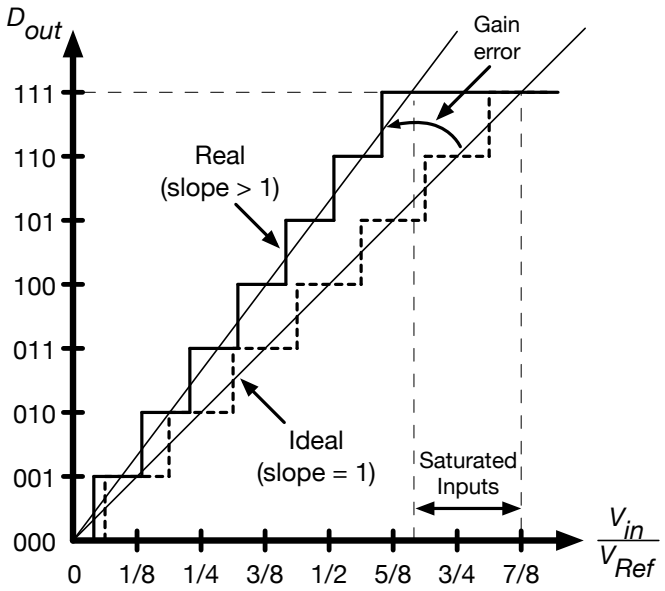


Figure 2.11: Gain Error (grossly exaggerated) in a 3-bit ADC.

For the ideal case, this slope is unity. In cases where the converter has a gain under unity, its output range is limited, as it may occur that not all the outputs are mapped to

an input voltage. This is further aggravated if it also presents an offset error. On the other hand, if the converter has a gain beyond 1, the output value saturates before the input voltage reaches its maximum. The gain error can be calculated by Eq. 2.7.

$$\Delta_{gain} = \frac{d_{T_{2^B-1}} - d_{T_1}}{v_{T_{2^B-1}} - v_{T_1}} \qquad \text{(LSB)} \tag{2.7}$$

where B is the ADC resolution.

2.2.2.3 Differential Nonlinearity

As illustrated in Fig. 2.12, DNL errors occur whenever the difference between consecutive transitions deviates from the ideal value of 1 LSB. Since the DNL error varies between consecutive transitions, it is represented by a vector. Either it or the worst-case scenario (i.e., the maximum DNL value) is used to characterize the ADC. Also, before determining the DNL for each code, offset and gain errors are removed, via the use of the endpoint-fit line (which connects, in a straight line, the first and last output codes).

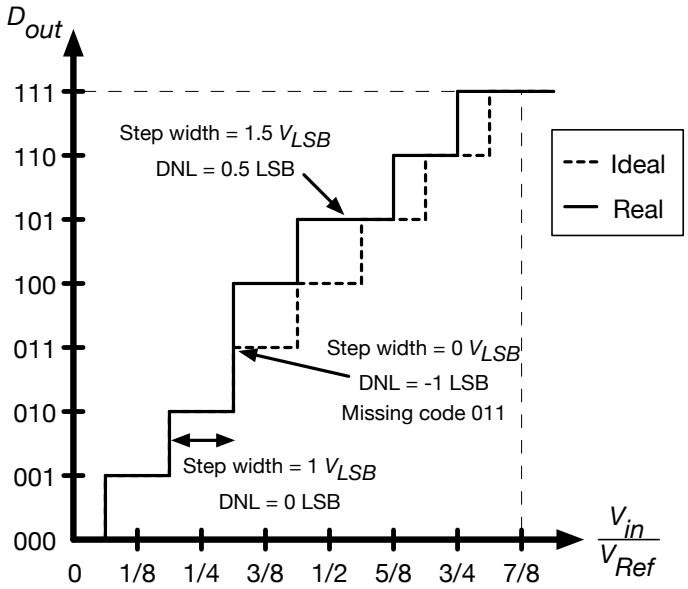


Figure 2.12: DNL in a 3-bit ADC.

The DNL formula can be expressed as Eq. 2.8.

$$\text{DNL}(i) = \frac{v_{T_{i+1}} - v_{T_i}}{\Delta} - 1 \quad \text{(LSB)}, \quad i = 1, ..., 2^B - 2 \tag{2.8}$$

From Eq. 2.8, special situations occur if the following is verified:

- DNL(i) = 0: two consecutive transitions are equal to 1 LSB.
- DNL(i) = -1: two consecutive transitions are equal, meaning that, for consecutive inputs, the output code "jumps" from $v_{T_{i-1}}$ to $v_{T_{i+1}}$, bypassing code v_{T_i}, which effectively is a *missing code*.
- DNL(i) $\geq$ +1: two consecutive transitions are larger than 1 LSB. This indicates the possibility (but not certainty) of missing codes.

Since the presence of DNL errors result in a input-output curve that's different from the ideal quantizer curve, the quantization noise introduced by it (also designated as "DNL noise") further degrades the SNDR.

2.2.2.4 Integral Nonlinearity

INL measures the deviation of a code transition from its actual to its ideal location. This deviation is given by the difference from the midpoint interpolating line of the actual input-output characteristic to the endpoint-fit line (Fig. 2.13), which is again used to eliminate gain and offset errors. Just as with the DNL, either the entire vector or the worst-case scenario is reported.

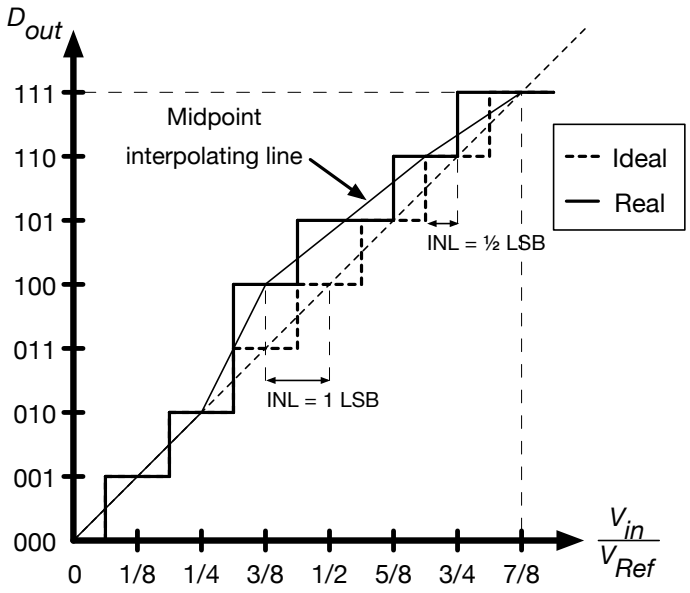


Figure 2.13: INL in a 3-bit ADC.

To derive the INL, one can either use Eq. 2.9 or estimate it as the cumulative sum of the DNL (Eq. 2.10).

$$\mathrm{INL}(i) = \frac{v_{T_i} - V_{LSB}(i-1) - v_{T_1}}{V_{LSB}} \quad \text{(LSB)}, \quad i = 1, ..., 2^B - 1 \tag{2.9}$$

$$\mathrm{INL}(i) = \sum_{j=1}^{i-1} \mathrm{DNL}(j), \quad i = 2, ..., 2^B - 1 \tag{2.10}$$

INL errors exhibit a relationship with harmonic distortion. In other words, a large INL indicates that there is a large deviation of the conversion characteristic to the ideal one, hinting at a possible large amount of distortion, which will reflect itself in both SNDR and THD.

2.2.3 Dynamic Performance Parameters

An ADCs dynamic performance can be characterized in the frequency domain through the Fast Fourier Transform (FFT) algorithm. The most common method relies on a sinusoidal wave used as the input of the ADC, which generates a quantized output. Once applied to the FFT algorithm, a spectrum of the quantized input signal is produced.

In order to minimize spectral leakage[3], it is recommended to coherently sample the input signal. This is achieved through a relationship between the input frequency f_{in}, the sampling frequency f_s, the number of cycles in the sampled set N_c and the number of samples N_s, given by Eq. 2.11. This equation holds true for the case when a sine wave signal is used.

$$f_{in} = \frac{N_c \cdot f_s}{N_s} \tag{2.11}$$

To reduce computation time but still capture enough samples (i.e., at least one per output code), the minimum value for N_s should be higher than roughly 2^{B+2}. It is also recommended that this number of samples is a power of two number [64].

If, for some particular reason, the input signal is not coherently sampled, *windowing* can be used as an alternative to minimize spectral leakage. There are several windows

[3]Spectral leakage indicates that the power of fundamental tones and their respective harmonics (the signal) is spread over other bins of the spectrum.

that can be used, each one more applicable to specific characteristics of the Device Under Test (DUT) [65].

Next, the most common dynamic performance parameters used are described, with the aid of an hypothetical FFT of the output of an ADC, shown in Fig. 2.14.

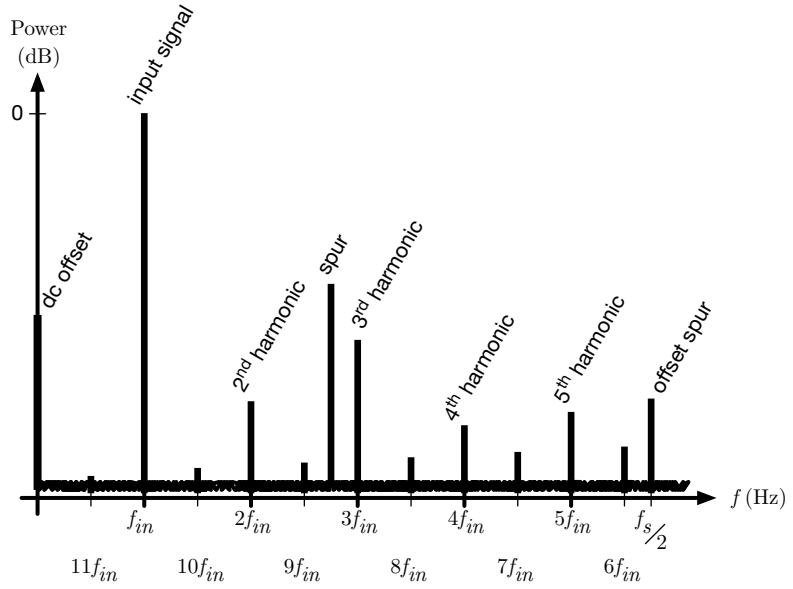


Figure 2.14: Example of an FFT of a ADC.

2.2.3.1 Signal-to-Noise Ratio

The SNR is the ratio of the signal power P_s to the noise power, which considers the contributions of clock jitter, spurious tones and thermal noise but excludes DC, signal and harmonic components, as given by Eq. 2.12.

$$\text{SNR} = \left(\frac{P_s}{P_{non-harmonic\ noise}} \right) \tag{2.12}$$

In theory, the maximum SNR that an ADC can achieve, when only quantization noise is taken into account (also known as SQNR), was calculated earlier (Eq. 2.5).

In the field of digital transmission, a sort of normalized SNR measure known as E_B/N_0, is defined as the ratio between the average bit energy and the one-sided power spectral density of the channel noise. It proves particularly useful when comparing the BER performance of different digital modulation schemes and is also frequently expressed in decibels.

2.2.3.2 Total Harmonic Distortion

Under a non-ideal ADC, tones appear at multiples of the input signal's frequency, called harmonics. THD measures the ratio of the sum of these harmonics' power P_H to the signal's power, as given by Eq. 2.13.

$$\text{THD} = \frac{\sum_{i=2}^{N_h} P_H(i)}{P_s} \tag{2.13}$$

where N_h represents the number of harmonics considered inside the band of interest, with the iterator i starting at 2 since we are not considering the power of the fundamental.

THD is highly dependent on the input signal. Distortion becomes more pronounced at higher frequencies and large amplitudes. Harmonic components indistinguishable from the converter's noise floor can be ignored from the THD computation.

2.2.3.3 Spurious-Free Dynamic Range

This parameter measures the ratio between the signal's power and the largest magnitude of any spectral component, excluding the DC component (which can be either a spurious tone or an input signals' harmonic), and is given by Eq. 2.14.

$$\text{SFDR} = \frac{P_s}{\max\left(P_{spectrum(f)}\right)}, \quad f \in \{1, ..., f_s/2\} \setminus \{f_{in}\} \tag{2.14}$$

If at low amplitudes a spurious tone could be responsible for limiting the SFDR, at higher frequencies the main culprit is probably an harmonic.

2.2.3.4 Signal-to-Noise-and-Distortion Ratio

SNDR is an extension of the SNR in that it includes the contribution of the distortion components of the THD, thus representing a more complete indication of the overall dynamic performance of the ADC. This results in a ratio of the signal's power to the noise and distortion's power and is given by Eq. 2.15.

$$\text{SNDR} = \frac{P_s}{\sum_{i=2}^{N_h} P_H(i) + P_{jitter} + P_{thermal\ noise} + P_q} = -10\log\left\{10^{\frac{-\text{THD}}{10}} + 10^{\frac{-\text{SNR}}{10}}\right\} \tag{2.15}$$

where P_{jitter}, $P_{thermal\ noise}$ and P_q represent the jitter's noise power, the thermal noise power and the quantization (with the contribution of DNL errors) noise power respectively.

2.2.3.5 Effective Number Of Bits

To properly characterize a converter, it is important to determine the real resolution of the converter, as even if the ADC is initially designed to achieve a resolution of B bits, noise and distortion inevitably lower its performance. A good indicator for the ENOB is to take Eq. 2.15 and solve it for B, resulting in Eq. 2.16.

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02} \quad \text{bits} \tag{2.16}$$

2.2.4 A/D Converters

ADCs are commonly separated into two main groups: the Nyquist rate and the Oversampling Data Converters. The latter distinguish themselves from the former by sampling a signal at a frequency much higher than the Nyquist rate which, as stated by the Nyquist criterion, is the minimum rate at which a signal can be sampled in order to avoid aliasing.

2.2.4.1 Parallel "Flash" ADC

For high-speed architectures, the fastest and most straight-forward to implement is the parallel (flash) topology. It consists on a bank of comparators in parallel, with one of their inputs directly connected to the input signal, while the other is connected to a different node of a resistor string, as displayed in Fig. 2.15.

As a result, this architecture behaves like a thermometer, where every comparator with a voltage V_{rX} higher than the input signal will have a "1" output, while the remaining have an output of "0".

Despite having the fastest conversion speed of any Data Converter topology, if the application requires a resolution of B bits, the number of comparators is equal to 2^B-1 in a conventional structure. Such specification severely hinders this topology in terms of area and power consumption as, for instance, a mere 6-bit resolution needs 63 comparators to operate.

The Two-Step Flash topology alleviates the number of comparators needed, by quantizing the input in two steps. In its most simple implementation, one quantizer decides

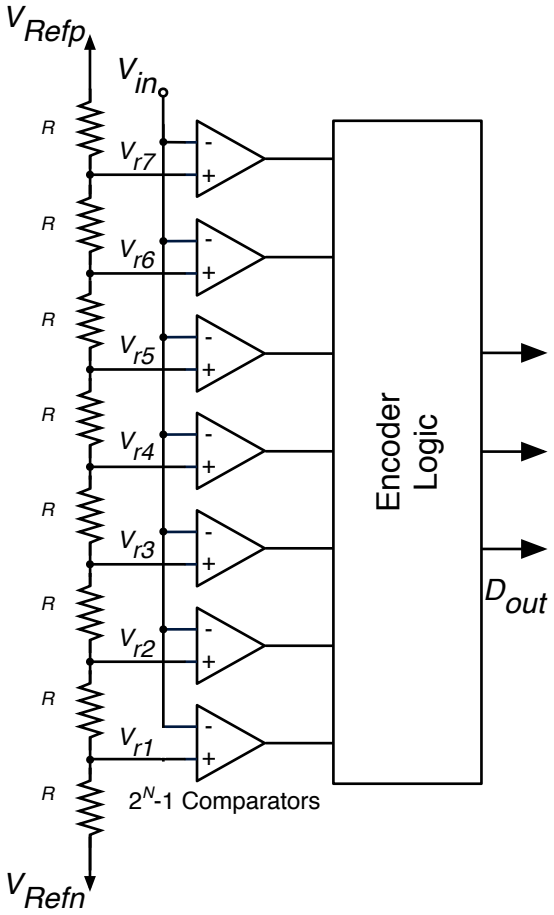


Figure 2.15: Schematic of a 3-bit Flash ADC.

the Most Significant Bit (MSB)s, while other determines the LSBs from the amplified residue voltage. This residue voltage is obtained via the subtraction of the MSBs from the original sampled input. To do so, a local DAC, a subtractor and a residue amplifier are used, with these three blocks commonly known together as the multiplying-DAC (MDAC). When compared to the original Flash ADC, this alternative reduces the number of comparators by $2^{\frac{B}{2}} - 1$, effectively reducing the area usage the higher the resolution. As a trade-off, latency is increased by half a clock cycle.

For SDRs the necessary number of comparators in the Flash architecture is a prohibitive feature, as moderate-to-high resolutions are needed whilst the design itself should be as compact and energy-efficient as possible, leaving this architecture to be used in high-speed low-resolution applications. There are also other issues when designing flash ADCs, such as their high parasitic load at the input node and the potential for bubble and flashback errors.

The works reported in literature that employ a flash ADC [66, 67] don't extend beyond a 6-bit resolution, regardless of the techniques used to reduce its number of comparators or lower its power consumption and input capacitance.

2.2.4.2 Pipeline ADC architecture

Following the Two-Step architecture, when several stages are arranged together in series, each responsible for quantizing B bits and generating an amplified residue to be quantized by subsequent ones, a structure known as the pipeline ADC is reached. This has the benefit of relaxing each individual stage's requirements and simplifying its implementation.

As opposed to the Two-Step topology, each stage is constantly resolving the next input sample, not waiting for the residue of a certain sample to reach the end of the pipeline to keep processing data. As a result, the latency of this converter grows with the number of stages in the converter and is therefore higher than the Two-Step approach.

A traditional pipeline ADC stage consists on a S/H, a local quantizer and an MDAC, as shown in Fig. 2.16.

The local quantizer is usually a flash, as each stage typically quantizes 1 to 4 bits, most commonly being 1.5-bit. The accuracy of the MDAC, imposed by capacitor mismatch and finite DC gain of the residue amplifier, usually limits the linearity of the ADC. Similarly to the Two-Step converter, the gain of the residue amplifier is designed to be of 2^{B_j}, with B_j being the resolution of the current local stage. This is so that the residue's dynamic range matches the full scale range of the converter, easing the implementation of subsequent quantizers.

One of the advantages of using this architecture is the capability of significantly increasing the sampling frequency. Still, due to technology scaling the design of high-gain high-speed residue amplifiers at low supply voltages is becoming increasingly more difficult. In this context, in [16] a mismatch-insensitive 1.5-bit MDAC with unity feedback factor, that relies on the lossless bottom-plate sampling (LBPS) technique [69] to relax the DC gain, gain non-linearity and noise requirements of the residue amplifier is proposed. In short, the error present at the summing-node of the main amplifier is sampled and amplified through an auxiliary amplifier, which is then subtracted at the bottom-plate

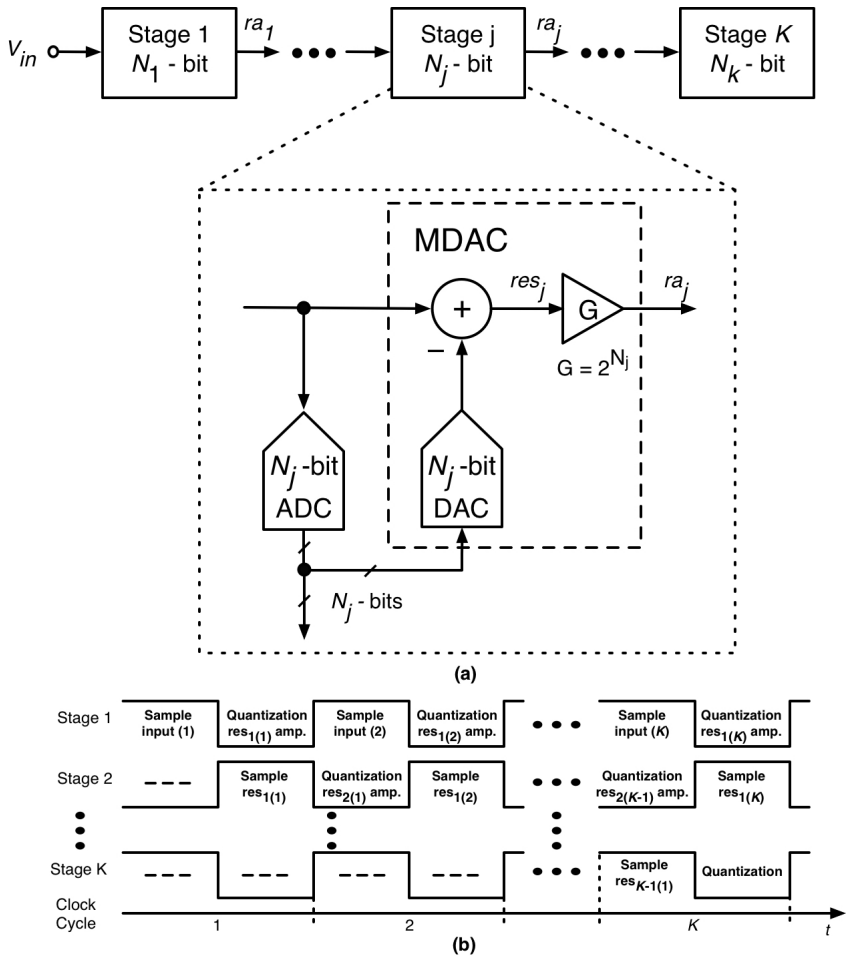


Figure 2.16: The Pipeline ADC: (a) Block diagram of a stage, exemplifying its building blocks (b) Timing diagram. Adapted from [68].

of the sampling capacitors of the following stage. As a result, a low gain, poor linearity and noisy amplifier can be used. The additional power consumption presented by the auxiliary amplifier is compensated by using a far less power-hungry main amplifier.

The replacement of the local Flash quantizers by SAR ADCs has also been pursued in recent years, as a way to improve the energy-efficiency of this structure, as reported in works [70, 71], while also lessening the impact of comparator noise in the overall performance of a conventional SAR structure.

2.2.4.3 Successive-Approximation ADC

Successive-Approximation ADCs are one of the architectures of choice for applications that require both a moderate resolution (8 to 12 bits) and speed (ranging from tens of kSps to tens of MSps) at a low power operation. They are widely regarded as the data

converters that provide the best energy efficiency, due to their scaling-friendly nature. In other words, their switching-intensive mode of operation coupled with lack of amplifier usage matches quite well with the trend of faster transistors with lower intrinsic gain ($\frac{gm}{gds}$).

In its most simple form, it requires a S/H circuit, a single comparator, a DAC (that can itself embed the S/H function) and a digital control logic known as SAR, as shown in Fig. 2.17.

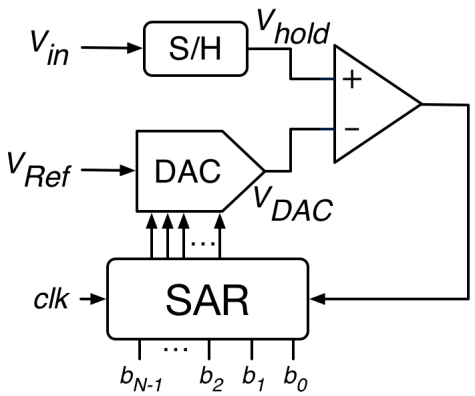


Figure 2.17: Schematic of a N-bit SAR ADC.

It operates on the basis of a binary search, trading speed for accuracy. One bit is resolved in each cycle based on the comparison results between the input signal and the DAC output voltage, which is set by the control logic. After each cycle the search range is halved, and this occurs until every bit has been resolved.

This process is illustrated in Fig. 2.18, where an input signal of 0.4V is applied to a 4-bit quantizer. During the first cycle, the search range is the entire input range (0V to 1V), and to determine if the input sits on the upper or lower half of the search range, 0.5V is used as a reference. Since 0.4V < 0.5V, the MSB is set as "0" and the search range is reduced to the lower half in the following cycle, where 0.25 is now used as a reference. Now 0.4V > 0.25V, hence the current bit is set to "1" and the following cycle operates in the interval [0.25V - 0.5V]. Proceeding similarly for the remaining bits, the converter outputs the code "0110".

Since this topology spends a cycle for each bit of resolution, it is significantly less time-efficient than the original flash ADC, much like the pipeline ADC, with latency increasing

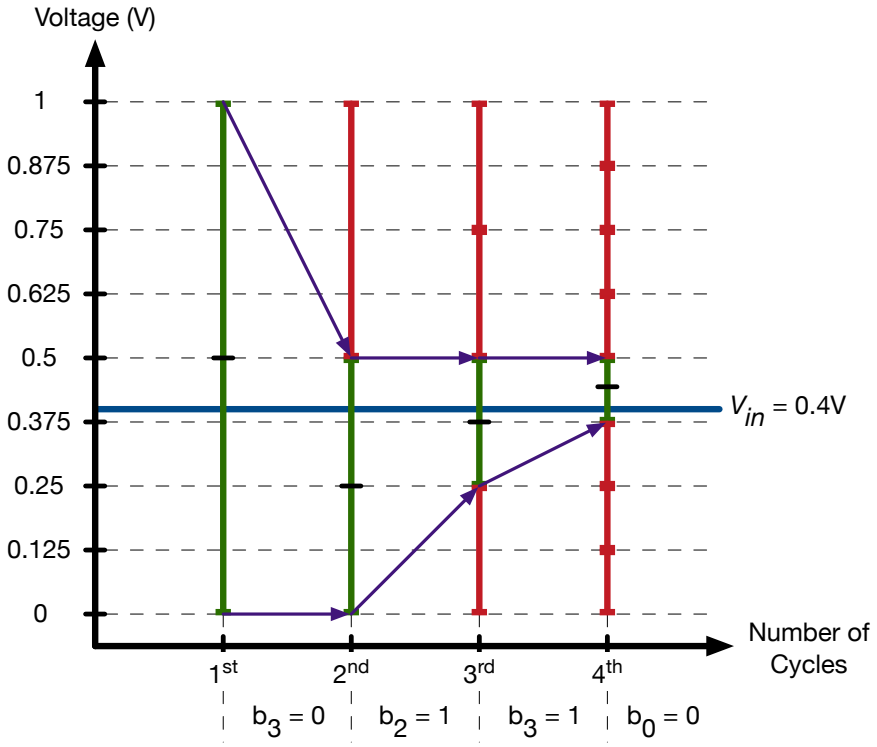


Figure 2.18: Waveforms illustrating the binary search method in a 4 bit quantizer and an input signal of 0.4V.

with the number of comparisons. However, it presents a linear growth of comparisons relative to the resolution (B comparisons for B bits), as opposed to the exponential function of the flash structure, making it rather energy-efficient.

The resolution of a SAR ADC is typically limited to 10–12 bits due to two factors: one is the non-linearity due to DAC mismatch and the other is the SNR limited by comparator noise. Conventional ways to solve DAC mismatch in SAR ADCs are either by factory trimming or by digital calibration. The SNR limitation imposed by comparator noise becomes critical in advanced processes because of the reduced supply voltage and signal swing[4].

In most recent SAR ADCs dynamic comparators are used, with no quiescent current. They impact the overall performance on noise, power and speed. As for the SAR itself, the design is not problematic as it can be easily implemented with logic gates, regardless of the algorithm used. Recent designs employ full-custom controllers implemented in

[4]One solution is pipelining with residue amplifiers to suppress comparator noise during LSB decisions, with the aforementioned "Pipeline-SAR" approach.

transistor-level as opposed to gate-level, in order to further improve the performance of the controller [72].

As mentioned, the DAC can be considered the most critical block of the SAR ADC, as it is one of the main sources of power consumption and also dictates the conversion speed and linearity of the converter. Adding to that is the noise contribution that is even more significant whenever the S/H functionality is merged into it.

The majority of SAR ADCs use DACs that work under the CR scheme, but an alternative approach based on CS is also viable, although underexploited[5]. Both schemes are shown in Fig. 2.19, for a N-bit capacitor array.

In the CR scheme, the voltage at the bottom plate of the capacitors in the capacitive array (the one **not** connected to the comparator's input) is varied while the total capacitance of the DAC is kept unchanged throughout the conversion. This capacitive array is usually arranged in a binary weighted fashion, although there are a few examples in literature where non-radix-2 architectures are used. This is mainly done to ease the matching requirements for the array, but come at the cost of larger digital circuit complexity [75].

In the radix-2 domain, several array arrangements have been proposed with the end goal of optimizing energy efficiency and area, most based on three structures: the conventional binary-weighted (CBW) capacitive array, the binary-weighted with attenuation (BWA) capacitive array and the split binary-weighted (SBW) capacitive array. In [76] an extensive overview of these structures is presented, and the author refers to it for further information.

An inherent advantage of the CR scheme is that the S/H functionality can be merged into the capacitive array, at the cost of extra switches, though it should be stated that as a consequence the DAC noise will manifest itself on the converter's output. In the CS scheme however, this functionality is not performed by the DAC capacitive array as a consequence of the scheme itself. Instead, it explicitly requires a dedicated set of capacitors for it. As opposed to the CR scheme, here the capacitors that make up the array are precharged to a voltage beforehand, and are subsequently connected to the DAC

[5]Oversampling SARs should also be briefly mentioned: here noise-shaping is used to average out both comparator thermal and flicker noise to higher frequencies, thus overcoming the SNR limitation and leading to a significantly high resolution ($>$ 16b) albeit at relatively low sampling frequencies ($\approx$ 1MHz), forgoing any kind of factory trimming or digital calibration [73, 74].

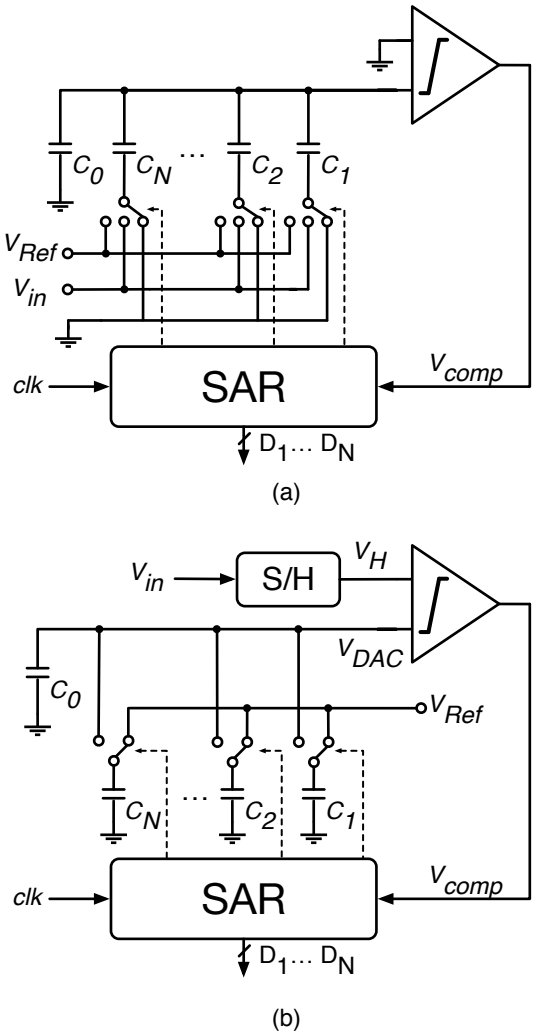


Figure 2.19: Operation modes of a charge-based SAR ADC: (a) Charge Redistribution (b) Charge Sharing.

nodes, effectively increasing its total capacitance during the conversion. With the input signal sampled onto the sampling capacitors, the MSB is directly evaluated, thus forgoing an explicit MSB capacitor. As a result, the DAC array size is smaller than that in a CR scheme despite the addition of explicit S/H capacitors.

Fast-settling Operational Amplifier (OpAmp)s are commonly used to generate both the input and reference voltages, in the CR scheme, able to settle their outputs fast enough while driving large capacitive loads. In contrast, the CS scheme working under a charge-based operation, resorts to simple passive switches to add or subtract charges to the DAC nodes, since the respective capacitors were already charged during the sampling phase, where the settling time is more relaxed. Thus, the only active element is the comparator

itself, responsible for most of the power consumption in the architecture. Still, one must take into account the offset in the comparator, as the ADC behaves in a nonlinear fashion due to the time-varying total capacitance characteristic. The other significant drawback of this characteristic is that as the voltage seen by the comparator steadily declines, this scheme has higher noise sensitivity than the charge-redistribution one.

An important feature of the CS switching scheme is that the input range of the ADC is not confined to the value of its reference voltage, which is quite useful when dealing with PAPR issues which are fairly common in modern-day radio receivers due to the widespread use of multi-carrier transmission schemes such as OFDM.

The CS-SAR ADC architecture in particular will be discussed more in depth in the following chapter.

2.2.4.4 Oversampled Data Converters and $\Sigma\Delta$ Modulation

With technology scaling enhancing the capabilities of digital circuits, oversampling converters have the advantage of relaxing the requirements on the analog side of the circuit at the expense of more complex digital circuitry, trading conversion time for resolution. Furthermore, the requirements on the AAFs are greatly relaxed and most of the time these converters can avoid the need for the S/H block.

Oversampling in itself consists on sampling the input signal at a rate much higher ($>$ 10) than its Nyquist rate and consequently spreading the quantization noise over a wider frequency interval (as it is seen as white noise), leading to an improvement in SNR. In particular, $\Sigma\Delta$Ms resort to feedback where the difference (Δ) between both the output and the input signals is calculated and subsequently integrating (Σ) it. Coupled with oversampling, it is then possible to push the quantization noise out of the frequency band of interest, a process called noise-shaping.

When considering BP$\Sigma\Delta$M one must also take into account that the performance (both in terms of stability and noise) of a N-th order bandpass filter is equivalent to that of a N/2-th order lowpass filter. This means that high order ($>$ 3) $\Sigma\Delta$Ms are almost mandatory, with stability becoming a major issue. As they present a highly non-linear block (the quantizer), it is quite difficult to find the best sizing that ensures stability for every input and leads to the best performance possible, limiting its SNR. This becomes

Table 2.1: Summary of ADCs used in radio applications

	Flash	Pipeline	SAR	Sigma-Delta
Conv. Method	Direct Search	Parallel structure	Binary Search	Oversampling
Speed	High	Medium	Low	Low to Medium
Power	High	Medium	Low	Medium
Resolution (b)	≤ 6	≤ 14	≤ 12	≤ 20

even more critical when modern day communication standards are considered, with high PAPR values, that can easily saturate the converter.

A list of works in the field of radio applications that rely on BP$\Sigma\Delta$M was discussed earlier in subsection 2.1.4.4.

2.2.5 Summary

The latter part of the current section focused on the most used ADC architectures for radio receivers, and these are briefly summarized in Table 2.1.

Looking at most converters reported from the year 1997 onwards, in both International Solid-State Circuits Conference (ISSCC) and Symposium on VLSI Circuits (VLSIC), and plotting each converter's resolution versus its sampling speed (Fig. 2.20), it's possible to observe that the architectures more suited for specifications such as moderate-to-high resolution (> 8 bits) and moderate-to-high-speed (> 10 MS/s), are indeed either the Pipeline and SAR structures. Despite $\Sigma\Delta$Ms reaching resolutions in the 12-to-16 bit interval, they are noticeably slower, usually more power-hungry and present limited dynamic range, the latter being a consequence of the notorious potential for instability that characterizes this architecture. Considering that BP$\Sigma\Delta$Ms require double the order of their BB equivalents in order to reach a similar performance, this becomes even more of a issue.

Between Pipeline and SAR ADCs, the former are the ones that usually present higher conversion rates. However, the residue amplifier design becomes more stringent at deep sub-micron processes (45nm process and below). The option of replacing the low-resolution flash quantizer by a low-resolution SAR quantizer in each pipeline stage becomes a viable option, due to the scale-friendly nature of the SAR ADC. This "Pipeline-SAR" approach can yield converters with 10-to-12 bit resolution with sampling rates up to 250 MS/s [78, 79].

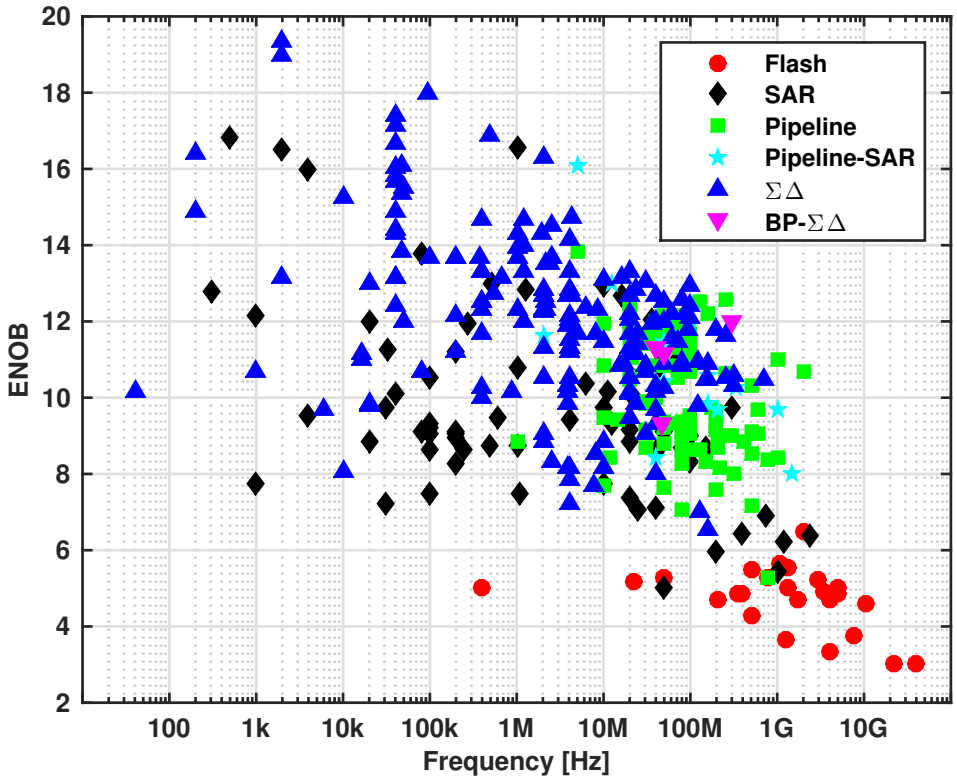


Figure 2.20: Summary of ADCs published in ISSCC and VLSIC from 1997 to 2019 [77].

The thought behind "Pipeline-SAR" approaches highlights the SAR ADC itself and how it is consensually regarded as the most energy-efficient scheme among the known data converter topologies, able to achieve a moderate resolution and speed. Recent works report performances exceeding 11 bits of resolution whilst operating at a sampling speed of 70 MHz [80].

Among SAR ADCs, the DAC of CS schemes has a smaller area when compared to its CR counterpart. Furthermore, both the S/H and the DAC capacitors sample the input signal and the reference voltage at the beginning of the conversion, in a single clock-cycle. This modified "pre-charge" feature of the CS-SAR ADC is particularly useful for implementing the proposed downconversion technique, and it will be detailed in chapter 3, together with the main characteristics of a CS-SAR implementation.

CHAPTER 3

THE CS-SAR ADC

As detailed in 2.2.4.3, the CS scheme presents notable advantages over its CR counterpart, in the context of ADCs for radio applications. In this chapter, a more comprehensive overview of the CS-SAR ADC is given, where its main advantages and drawbacks are presented.

Most of the equations shown were already extensively derived in [81], as prior to it the available theoretical material in the field of CS-SAR ADCs was quite scarce. Thus, this chapter focuses most on their analysis and main takeaways.

3.1 CS-SAR ADC: A Review

3.1.1 Mode of operation

To more easily understand the operation of a CS-SAR ADC, Fig. 3.1 illustrates an 4-bit fully differential implementation together with its conversion procedure. Notice that despite it being a fully differential implementation, a single capacitor bank is used, unlike CR-SAR ADCs which require two.

At the start of the conversion, two actions take place simultaneously: the input signal is sampled into the S/H capacitors while the capacitors in the array are pre-charged to the reference voltage V_{Ref} (Fig. 3.1(a)). In the next cycle the comparator is activated, with

the voltage at its inputs being the one fed by the S/H (Fig. 3.1(b)). As a result, the MSB is immediately decided in this comparison and, according to the result, charge is added or subtracted via the largest capacitor in the array being placed in a parallel or anti-parallel fashion, respectively, to the S/H. In this example, charge is added (Fig. 3.1(c)). In the following cycles this procedure is repeated for the remaining bits, lasting until the LSB is decided. In the illustration, charge is subtracted in the following two cycles, by placing the respective capacitors in anti-parallel (Fig. 3.1(d),(e)). With each bit evaluated, the differential voltage at the comparator's input decreases towards zero while its common mode voltage is kept constant and equal to that of the input signal. The digital word at the output consists on the stored comparison results.

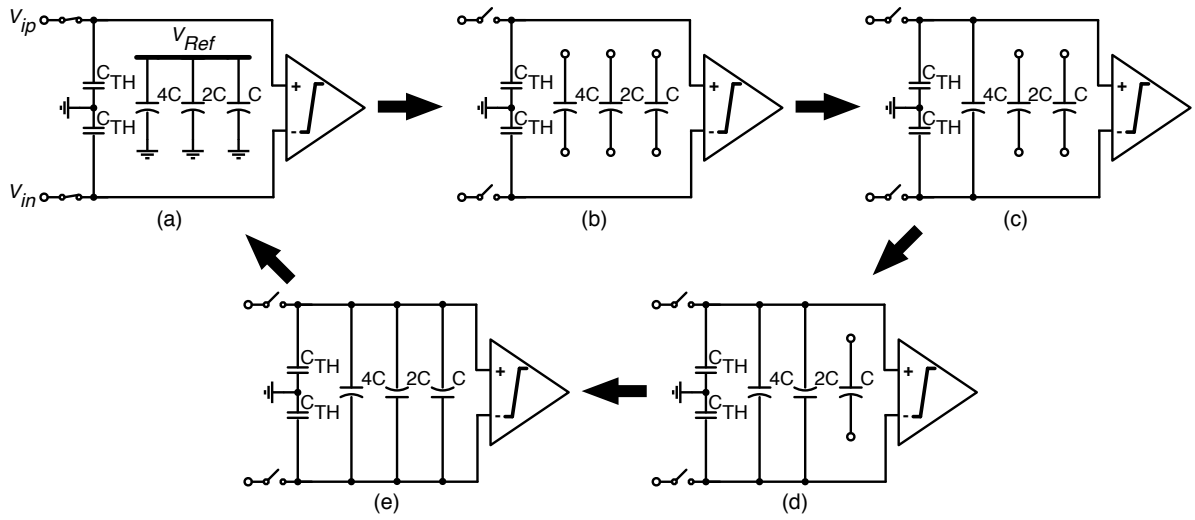


Figure 3.1: Conversion procedure for a 4-bit CS-SAR ADC example.

3.1.2 Advantages, Drawbacks & Effects of Non-Idealities

Since the MSB is decided right after sampling, as a consequence of the CS scheme itself, there's no need for a MSB capacitor in the DAC array. This, coupled with the fact that only a single capacitor bank is required for a fully differential implementation, results in the DAC of the CS-SAR ADC having a significant smaller area than its CR-SAR counterpart.

While it's true that the CS-SAR requires an explicit S/H which has to be accounted for in the total area and that, in some cases, might be made larger than the overall DAC capacitance (increasing the input buffer power consumption), its requirements are far

less stringent in terms of matching. This holds true even for resolutions of 8-bit and beyond. Also, being less sensitive to parasitics, capacitors with higher densities can be used, reducing the impact on the ADCs total area.

As detailed in [81], the gain error caused by mismatch between both S/H capacitors and between the S/H capacitors and the total DAC capacitances can be considered negligible (around 1%), for an 8-bit implementation with a S/H capacitance of 256 fF. On the other hand, the ENOB obtained when taking into account the mismatch between the DAC capacitors themselves can be considered roughly the same as the one obtained for the CR topology, for equally sized DAC arrays[1]. In other words, for resolutions up to 9-bit, the maximum drop-off is of roughly 1-bit when considering a standard deviation of the unit capacitor of 10%. For higher resolutions, the drop-off can be as severe as a 2-bit loss.

When it comes to the effect of parasitics in the capacitors, in the event that these are balanced, no linearity errors arise. However, as it is most likely, in the presence of unbalanced parasitics, the drop in ENOB is lower than 0.2 bits for designs up to 10 bits of resolution. For higher resolutions (≤ 12), the performance drop remains under 0.6 bits. All these conclusions are drawn assuming an worst-case scenario, where there is total unbalance between the capacitor plates and where the average parasitic is considered five times larger than the DAC capacitor. Furthermore, the effect of parasitics on the common-mode voltage can also be considered negligible.

By connecting one capacitor at a time to the DAC nodes with each conversion cycle, the DACs total capacitance is constantly increasing, which poses two significant design challenges. The first is that the voltage seen by the comparator is steadily attenuated, since its value is given by the ratio of charge and capacitance ($q = C \cdot V$) and C is increasing, making the topology less noise tolerant. The second issue with this time-varying behaviour is that the ADC becomes nonlinear in the presence of comparator offset. The analysis on the impact of both these issues (as well as the influence of mismatch and parasitics detailed before) is thoroughly done in [81], and the author refers to it for further information.

[1] Since the number of required unit capacitors is four times smaller in the CS topology than in a differential CR implementation, the unit capacitor of the DAC is made four times larger, so that the total DAC capacitance and area are identical.

It's shown in [81] that both the worst-case DNL and INL occur at the MSB transition and their expression is given by Eq. 3.1 and Eq. 3.2 respectively:

$$|\delta_{max}| = \frac{|V_{OS}|}{\gamma \cdot V_{LSB}} \tag{3.1}$$

$$\phi_0 = -\frac{V_{OS}}{\gamma \cdot V_{LSB}} \tag{3.2}$$

where γ is given by the ratio of the S/H capacitance over two times[2] the total DAC capacitance, i.e., $\gamma = \frac{C_{SH}}{2 \cdot C_{DAC}}$ and V_{OS} is the input-referred offset voltage.

Although the SAR ADC architecture ensures monotonicity, missing codes might occur. However, if Eq. 3.3 is verified, the absence of missing codes is guaranteed as the ratio between both quantities is less than 1.

$$|V_{OS}| < \gamma \cdot V_{LSB} \tag{3.3}$$

In other words, if $\gamma = 1$, as long as the comparator offset is smaller than V_{LSB}, each output code has at least an input voltage assigned to it. Due to the comparator offset, the ADC transfer curve presents an offset given by Eq. 3.4.

$$\text{ADC}_{\text{offset}} = \left(1 + \frac{1}{\gamma}\right) \cdot V_{OS} \tag{3.4}$$

As a result of all of these calculations, the expected maximum achievable effective resolution for a B-bit CS-SAR ADC with comparator offset can be approximated by Eq. 3.5.

$$\text{ENOB} \approx B - log_4\left(1 + 2^{3-B}\left(\frac{4}{9}\phi_0^3 + \phi_0^2 + \frac{B}{6}\phi_0\right)\right) \tag{3.5}$$

From all these equations, it becomes clear that an increase in the value of γ (i.e., a larger difference between the S/H and the DAC capacitances) leads to an improved tolerance to comparator offset, which in turn means that the ADC presents a better performance.

Moreover, when both the CS- and CR-SAR topologies are simulated side-by-side to quantify the impact of noise, it becomes apparent that the former performs worse than the latter, when subjected to the same noise sources. These simulations only account for

[2] To account for the fact that a single capacitor array is used in a differential topology.

comparator noise, as it dominates over thermal noise. This implies that the comparator used in a CS-SAR design has more stringent noise specifications, for the same resolution, when compared to the CR architecture. On the other hand, as in the case of the comparator offset, factor γ can be used to improve the performance of the CS scheme to that of the CR-SAR.

In the CS scheme, the entire energy consumption of the reference source takes place only during the pre-charge cycle, as each capacitor in the array is charged to the reference voltage and all the charge is drained at once. In the following cycles, each capacitor is simply connected to the DAC nodes via switches, taking on a complete passive behaviour. This is contrasted with the CR scheme, where some charge is drained in every step which dictates that the reference buffer is kept running for the entire operation. In the CS-SAR case, the reference buffer needs to be active only during a fraction of the conversion's entire time.

Expanding on this feature, one may employ duty-cycling during the reference generation or relaxing the reference buffer itself, resulting in power savings. In the case of the former, the reference circuit toggles between the "on" and "off" state when in the pre-charge and the charge processing cycles, respectively. In the case of the latter, a reference buffer with higher output impedance can be used. Although the time required to pre-charge the DAC capacitances is increased, the duration of charge processing is kept unchanged.

3.1.3 Switching scheme

Since the CS-SAR relies on a charge-based operation, i.e, it operates under binary-weighted values of charge instead of binary-values of capacitance, it's possible to reduce the total capacitance of the array by using multiple pre-charge voltages. Three different approaches are described next. As an example, an 8-bit CS-SAR ADC is considered. Only the capacitor array and the pre-charge switches are shown.

- **1-step pre-charge scheme**

The simplest approach consists on all the binary-weighted capacitors in the array being charged to the same reference voltage, such as V_{DD}. This is illustrated in Fig. 3.2, where C_0 is the unit capacitor.

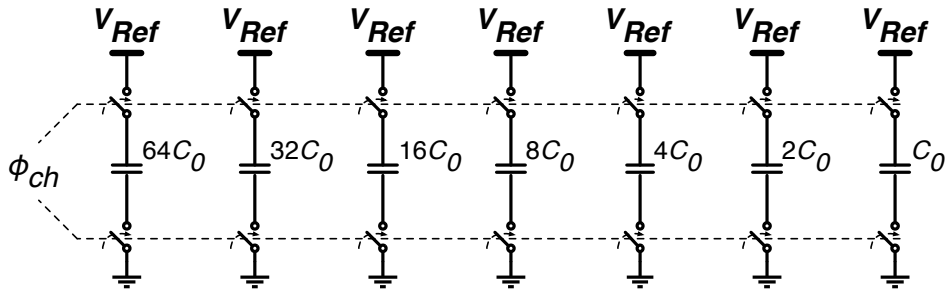


Figure 3.2: 1-step pre-charge scheme.

This scheme occupies the most area out of all proposed in literature, and in that sense, is the most inefficient.

- **1-step pre-charge scheme with V_{CM} for the LSB**

Similar to CR-SAR schemes, the use of a complementary reference level can prove useful for area-efficient designs. This is illustrated in Fig. 3.3.

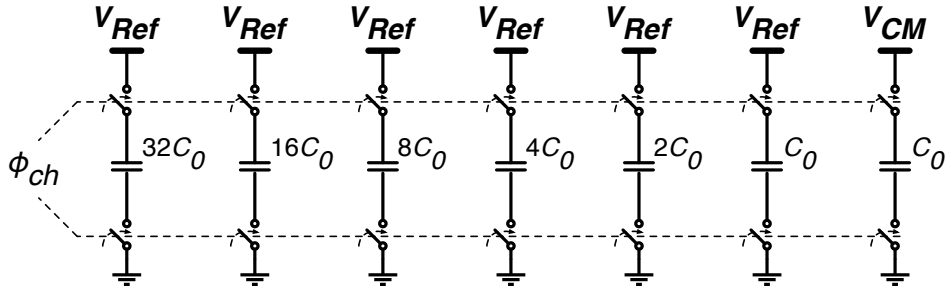


Figure 3.3: 1-step pre-charge scheme with V_{CM} for the LSB.

In particular, if V_{CM} is used as half of V_{Ref}, the size of the capacitor array can be reduced by a factor of 2.

- **Multi-step pre-charge scheme**

Usually, two constraints determine the size of the capacitors: device mismatch and unit capacitor size. For high-resolution compact designs, the latter can become impractical, as this may result in a unit capacitor with a size of a few fF.

As a way around this issue, a multi-step LSB pre-charge scheme can be used, as shown in Fig. 3.4. In this example the charge in the LSB capacitor is shared with two other equally sized auxiliary capacitors.

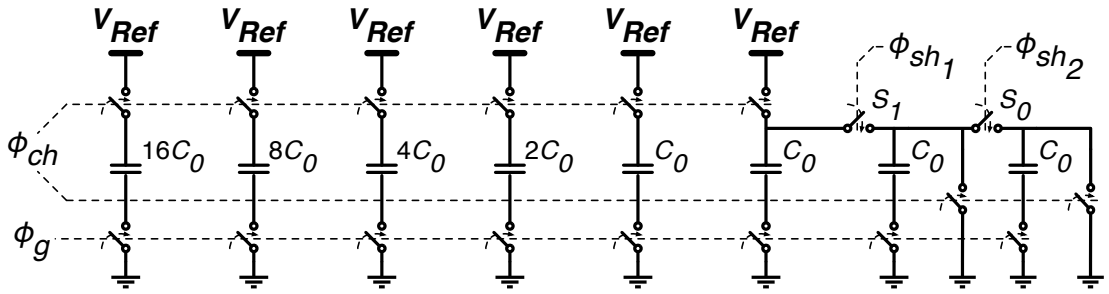


Figure 3.4: Multi-step pre-charge scheme.

The procedure is as follows: initially all the MSB capacitors are charged to the reference voltage, typically V_{DD}. Afterwards, the MSB switches are disconnected and the LSB capacitor shares its charge with an auxiliary capacitor, with the same capacitance value. This means that the charge is split equally between them. This behaviour is equivalent to having the LSB capacitor charged to half of V_{Ref}, as with the previous scheme.

This switching scheme can easily be extended to more steps, significantly reducing the total size of the capacitor array while maintaining the unit capacitor size modest.

3.1.4 ADC conversion gain

A significant feature of the architecture is that its input range isn't confined to the reference voltage range, as opposed to CR-SARs. In them, the voltage sources connected to the bottom-plate of the DAC capacitors (that are usually ground and V_{Ref}) dictate the range of voltages that the ADC can treat. Instead, operations in CS-SARs depend strictly on the values of charge, and the ratio between the S/H's charge and the DAC's charge defines the conversion gain.

As shown in [81], assuming that the DAC array follows a binary weighted structure in a B-bit resolution ADC, this gain can be defined as follows:

$$G_{ADC} = \frac{2^{B+1} C_u}{C_{SH}} = \frac{V_i}{V_{Ref}} \tag{3.6}$$

with C_u representing the unit capacitor and C_{SH} the S/H capacitors.

Under a differential operation, if both input signals have its common mode set to $\frac{V_{DD}}{2}$ and are bounded to V_{DD} and 0 (in phase opposition), the maximum input voltage V_i is of $2V_{DD}$. This also leads to, ideally, the best possible SNR for the ADC. Given that the reference voltage V_{Ref} is commonly set to V_{DD}, it follows that Eq. 3.6 simplifies to Eq. 3.7.

$$G_{ADC} = 2 = \frac{2^{B+1} C_u}{C_{SH}} \tag{3.7}$$

In these circumstances, one may then determine the relationship between the S/H capacitors and the unit capacitor C_u, which is given by Eq. 3.8.

$$C_{SH} = 2^B C_u \tag{3.8}$$

It follows that, for a constant input range, the S/H capacitances scale linearly with the reference voltage.

While in some applications, this can be used to reduce both the size of the S/H capacitors and power consumption by using smaller reference voltages (as is the case of circuits that work with significantly small input signals), it's also possible to use this feature to extend the ADCs dynamic range and enable it to operate with over-rail inputs.

This is of particular interest in the context of radio applications, as 4G and 5G networks usually resort to multi-carrier modulations in order to cope with the high data rates and spectral efficiency demands. These modulations are known to present high PAPR, placing stringent requirements on the circuits that drive the input signal. Aside from PAPR reduction techniques proposed in literature, having an ADC that can operate with over-rail input signals is quite an advantage over other competitive architectures.

3.2 State of the Art in CS-SAR ADCs

The state of the art in CS-SAR ADC is presented next. The first reported work in the field dates back to 2007, and since then only a few designs were published in literature, meaning that the architecture is fairly recent. Complete ADC designs are highlighted, as opposed to works focused mainly on the SAR controller or comparator. In addition, only works that report measured results from a manufactured prototype are considered. These works are presented in chronological order.

3.2.1 Craninckx and van der Plas [82]

The first CS-SAR ADC reported in literature [82], consists on a 9-bit ADC with a conversion rate of 50 MSps and a Figure-of-Merit (FOM) of 65 fJ/conversion-step in 90 nm CMOS. Given that power consumption in conventional CR-SAR approaches is dominated by the required fast-settling amplifiers to generate both input and reference signals, here the authors intended to design an alternative, where the only active element is the comparator. Thus, a power consumption of 0.290 mW is reported.

To further reduce power consumption, an asynchronous logic controller is used as opposed to a synchronous one, which would require a high-speed clock. This controller dictates the total conversion time ($\sim$ 20ns) and subsequently the maximum sampling speed of the converter. To reduce latency, two passive S/H stages are pipelined, allowing for one to track the input for the following conversion while the other holds the current sample until the end of the conversion. Since the charge on the back-end S/H is half of that transferred from the front-end S/H, the signal evaluated by the comparator has a 6 dB drop.

A 4-step pre-charge scheme is employed in the DAC, resulting in a total of 35 unit capacitors, with a size of 64 fF. The dynamic comparator used has a programmable capacitor array to calibrate the comparator's offset voltage. Comparator noise becomes the dominant factor in performance, leading to a ENOB of 7.8.

3.2.2 Giannini et al. [83]

One of the key limiting factors in terms of resolution for SAR ADCs is the comparator noise, that tends to worsen with technology scaling. To that regard, in [83] the authors' approach to mitigate this impact relies on the use of two parallel comparators. One of the comparators is designed for high-noise and low-power, that decides all of the bits except for the LSB. The other, a low-noise high-power comparator is used to determine the LSB and perform an additional comparison (if needed) to detect a possible error committed during the first phase. If that is the case, a digital addition/subtraction is performed on the final N-bit word. This correction accounts for thermal noise and other sources, as static non-linearities, so long as they don't exceed 1 LSB.

The time-interleaved sampling circuit includes a circuit to lower the common-mode voltage of the signal processed by the comparator, increasing the V_{GS} on the switches and consequently reducing their on-resistance. With time-interleaving the 6 dB drop-off reported in the prior design is mitigated. As a result, a 9-bit CS-SAR ADC operating at 40 MSps, burning 820 µW from a 1 V supply is reported. The converter, fabricated in 90 nm CMOS, reaches a FOM of 54 fJ/conversion-step.

3.2.3 Tsai et al. [84, 85]

In [84], an 8-bit 40 MSps CS-SAR ADC that consumes 113 µW from a 1 V supply is presented. A dedicated comparator decides the MSB right after sampling. As opposed to the previous work, the MSB capacitors in the DAC array are used as the second set of capacitors that sample the charge of the S/H. Consequently, the size of these capacitors is increased twofold and an additional comparator is required for the remaining decisions.

Here, the capacitive array is pre-charged to the common-mode voltage V_{CM} and each DAC cell has a structure where two capacitors are placed in series. The idea here is to have energy recycling by charging the capacitor connected to the positive node of the DAC from a residual charge to the pre-charge voltage, as opposed to charging it from 0. This is possible due to the fact that the signals at the comparator inputs converge to a positive voltage at the end of the conversion. Not only does this result in energy savings in the order of 67% but the settling response is also faster. The measured prototype, in a

90 nm CMOS process, achieves a FOM of 20 fJ/conversion-step.

Expanding on the idea of residual charge re-usage first reported in [84], a reference-free 9-bit CS-SAR ADC with a 1.5 MSps conversion rate for wireless telemetry is proposed in [85]. Here, the proposed CS-SAR has two identical binary-weighted capacitor arrays side-by-side, each performing as the sampling capacitor and the DAC array alternately. When cascading both arrays, the residual charge on the sampling capacitors is effectively boosted to the desired reference voltage, in a charge-pump fashion. Removing the reference supply entirely means that the corresponding switching energy is zero. Implemented in a 180 nm CMOS process, this circuit reaches a FOM of 32 fJ/conversion-step when the sampling speed is lowered to 2.2 kSps.

3.2.4 Malki et al. [86]

The work presented in [86] consists on a CS-SAR ADC with a 10-bit resolution that operates up to 80 MSps. The notable feature behind this design is the use of a variable-gain transconductor on its sampling front-end, converting the input voltage into a current that is then integrated onto the sampling capacitors. Hence, a power-hungry voltage buffer is not required and issues such as clock jitter, time skew and switch resistance become less critical.

Another particularity is the fact that due to this current-integrating mode the output amplitude is dependent on the input frequency. This current integration introduces a *sinc* ($\frac{sin(x)}{x}$) behaviour, with its notches located at multiples of $1/T_{integ}$, with T_{integ} representing the integration period. This means that whenever the integration time matches or is a multiple of the input signal period, the output charge is zero. However, in the context of RF applications, this can be exploited as a way to attenuate interferers and blockers at higher frequencies.

Non-linear MOS capacitors (MOSCAPs) are used in the S/H instead of MOMs in order to relax the comparator noise requirements. During integration, these are biased in the inversion region to achieve good linearity and switched to depletion mode before the conversion takes place, thereby increasing the ADCs voltage swing and reducing the comparator's noise requirements. It should be mentioned that this approach is possible due to the charge-based characteristic of the CS-SAR ADC. The DAC array follows a

4-step pre-charge scheme, with a total of 67 unit capacitors, each with a size of roughly 30 fF. In a 40 nm CMOS process, the measured prototype consumes around 1.45 mW with a 1.1 V supply, reaching a FOM of 85 fJ/conversion-step.

3.2.5 Nakane et al. [87]

A triple-mode transceiver for GSM, WCDMA and LTE that resorts to a 12-bit CS-SAR ADC is proposed in [87]. Its reconfigurability allows it to operate and meet the demands of such standards in both noise and speed. To cope with the stringent comparator noise requirements, a time-interleaved S/H with passive amplification is used. In short, two connected capacitors are placed in parallel during sampling and alternate to a series connection once the conversion starts.

Furthermore, a non-binary capacitor array with digital correction is used. The non-binary structure compensates for insufficient DAC settling and its capacitors are charged by a on-chip regulator. Radix and time-interleaved mismatch are corrected in a foreground manner.

According to the standard operating at a given instant, a dynamic comparator with offset cancellation structure achieves the noise and speed requirements by changing the load capacitance of both the preamplifier and latch stages.

Measured results from a prototype fabricated in 65 nm CMOS yield a FOM of 42.4 fJ/conversion-step when configured for the GSM standard, operating at 52 MSps, drawing a current of 3.2 mA from a 1.25 V supply. When WCDMA/LTE is considered, the power increases to 5.9 mW and the resulting FOM is 111.3 fJ/conversion-step.

3.2.6 Rabuske and Fernandes [88]

In [88], a 9-bit 1 MSps CS-SAR ADC that strictly uses MOSCAPs in the DAC capacitor array is proposed. The non-linearity of these elements is exploited with the goal of lowering the architecture's sensibility to noise and comparator offset. With better matching characteristics and higher capacitance density than MOMs, it's also possible to reduce the DAC area. The DAC capacitor array follows a straightforward binary-weighted distribution.

Moreover, a configurable S/H is used to allow operation beyond the supply rails range. To do so, three binary-weighted capacitors can be added to the overall sampling capacitance while the S/H switches are driven by a boost-and-bootstrap circuit that ensures signals larger than the supply voltage are properly converted, even if this voltage is as low as 0.6 V. For such a supply, the input swing of the ADC is increased to around 1.7 V_{pp}, a 40% improvement over regular rail-to-rail implementations.

Under a 130 nm CMOS process, the fabricated prototype draws a current of around 4.6 µA from a 0.6 V supply, allowing it to reach a significantly low FOM of 7.8 fJ/conversion-step.

3.2.7 Venca et al. [89]

Since the reference generator is effectively disconnected from the DAC array during the bit trials, there is a significant area saving in the reference generator circuit. To this end, the authors of [89] exploit this advantage to design a hybrid 10-bit CS-CR SAR ADC, where the 4 MSBs are dictated by the CS section, while the remaining 6 LSBs are decided by the CR elements. This is done to mitigate the sensitivity to parasitics in the LSB capacitors that would rise if top plate switches were used.

The 10-bit SAR is used in a subrange scheme, as a coarse ADC, together with a ΣΔM that acts as a fine ADC. The residual error generated by the SAR ADC, due to factors such as the input-referred thermal noise of the comparator, is dealt with by the ΣΔM. However, the comparator requires offset calibration, in order to prevent saturation of the ΣΔM.

The fabricated 12-bit ADC occupies an area of 0.04mm^2, in a 28nm CMOS process, with a power consumption of 17.5mW from a dual 1.2V/1.5V supply. Operating with a sampling rate of 600 MSps, it reaches a FOM of 68 fJ/conversion-step.

3.2.8 Summary

The performance of measured CS-SAR ADCs reported in literature is shown in Table 3.1. Since this architecture forgoes the usage of high-speed power-hungry amplifiers in order to meet its low power consumption, the performance is mainly defined by the comparator offset and noise. Still, most of them are able to meet speeds in the order of tens of MSps while reaching 8 bits of linearity.

In [82], the sensitivity to offset is mitigated by foreground calibration of the comparator, through the addition of capacitances to the faster branch, thus slowing it down. Also, despite not generating an internal high-speed clock, the converter reaches a sampling speed of 20 MSps thanks to the use of an asynchronous controller. However, comparator noise defines the overall performance.

To reach a compromise between low power and noise sensitivity in the comparator, the authors in [83] resort to two comparators in parallel: a faster more noisy one that decides the majority of the bits and another, more accurate one, to determine the LSB and detect possible noise-induced errors. They also time-interleave the two S/H stages. In contrast, in [84] the MSB capacitor in the DAC array is used to function also as a secondary S/H capacitor.

In [86], a variable-gain transconductor is used on the sampling front-end. This aids in the extending of the dynamic range of the ADC. Coupled with the fact that the S/H presents a *sinc* behaviour that can be exploited to tune out interferers and blockers, this is an attractive solution for RF applications. However, this comes at the cost of limited input bandwidth.

Still in the context of radio applications, [87] presents a triple-mode transceiver that employs a non-binary weighted DAC array to compensate for insufficient DAC settling. Mismatches are corrected digitally. A reconfigurable comparator with foreground offset cancelation is used. According to the mode (GSM/WCDMA/LTE) in which the transceiver is operating, the pre-amplifier and latch's load capacitance is changed, so that the comparator operates in low-noise/middle-speed (GSM) or moderate-noise/high-speed (WCDMA/LTE).

In the field of low-voltage low-power applications, the authors of [88] report a CS-SAR

ADC that uses MOSCAPs in the DAC array, in detriment of linear capacitors. Albeit at a sampling rate of 1 MSps, the converter is able to become more robust to comparator offset and noise. A programmable S/H enables the extension of the ADCs dynamic range. To date, this converter has the lowest FOM among the reported CS-SAR ADCs.

Finally, in [89] the authors resort to a CS-SAR to simplify the reference generator circuit design. However, the CS-SAR is only responsible for deciding the 4 MSBs out of a total of 10. The remaining 6 LSBs are determined by its CR counterpart. This hybrid ADC is used in conjunction with a $\Sigma\Delta$M, in a subranging scheme. While this design is not simply based on a CS scheme, it highlights its inherent advantage in terms of relaxing the requirements in the reference generation.

Table 3.1: Summary of state-of-the-art ADCs and respective performance.

Reference	[82]	[83]	[84]	[85]	[86]	[87]	[88]
Process	90 nm CMOS	90 nm CMOS	90 nm CMOS	180 nm CMOS	40 nm CMOS	65 nm CMOS	130 nm CMOS
Supply (V)	1	1	1	1	1.1	1.25	0.6
Area (mm2)	0.08	0.09	0.056	0.3	0.08	0.044	0.046
Resolution	9-b	9-b	8-b	9-b	10-b	12-b	9-b
f_s (Msps)	20	40	40	1.5	80	80	1
Power (µW)	290	820	113	20.5	5990	5900	2.78
ENOB	7.8	8.56	7.1	7.51	8.71	9.37	8.48
FOM (fJ/c.s.)	65	54.3	20.6	79	85	111.3	7.8

Chapter 4

The Embedded Mixing Technique

In the interest of developing alternative methods to radio receivers to those already existing, as presented in chapter 2, in this chapter the ADCs capability of accommodating both the quantization and downconversion operations through the use of variable reference signals is investigated. Such feature would enable a significant simplification of the receiver, as a design block with the single purpose of mixing the input signal with the LO signal would no longer be required. Consequently, advantages in terms of power consumption and chip area (among others) are expected, while keeping (or possibly enhancing) the flexibility of the ADC to cope with different standards.

Next, the embedded mixing technique is described. Since this method is a significant shift from those currently used, it is first discussed from a mathematical point of view, where equations are drawn that show how the use of a variable reference voltage can indeed shift a signal centered at the frequency f_c to an intermediate frequency f_{IF} or even directly to BB. Design considerations are given afterwards. Finally, a discussion is made regarding the ADC architecture best suited to implement the proposed technique. An 8-bit CS-SAR ADC designed around *quasi-ideal* blocks is used as an example that demonstrates its viability.

4.1 Mathematical Background

The proposed thesis takes advantage of the fact that the ADC is in itself, mathematically, an analog voltage divider that performs the division of the analog input signal $X_{in}(t)$ by a constant reference $X_{Ref}(t)$, as shown in Eq. 4.1.

$$\mathrm{D_{out}}(n) = \frac{X_{in}(t)}{X_{Ref}(t)} \tag{4.1}$$

The reference can be either a voltage or a current, but for the remainder of this analysis a "voltage-mode" realization is considered (i.e. $X_{Ref} = V_{Ref}$). In "current-mode" realizations of ADCs, the reference is a current rather than a voltage.

The result of this division is then quantized into discrete amplitudes. Here, $X_{in}(t)$ is assumed to be well-behaved, i.e., it presents no singularities and is well defined, as most modern-day communication analog signals are. Still, any system that is capable of performing the division operation is naturally capable of doing the multiplication operation (as it can be understood as a division by the inverse of the factor we want to multiply), thus performing the primary operation of any mixing stage.

In ADCs, the reference voltage is typically provided from a stable low-noise bandgap-type voltage-reference circuit. However, since there is no known binding rule that states that this reference voltage must be entirely constant, it is possible to split it in two signals: a constant voltage (still generated by a bandgap reference circuit), added to a signal term provided by a LO (varying over time). Thus, this 'normalized' reference voltage can be written as Eq. 4.2:

$$V_{Ref}(t) = \alpha + \beta \cdot \cos(2\pi f t + \varphi) \tag{4.2}$$

where α is the constant voltage provided by the bandgap reference circuit, and β, f and φ are the amplitude, frequency and phase of the signal generated by the LO. Notice that, in typical SC implementations of "voltage-mode" ADCs, the $V_{ref}(t)$ voltage will need to be sampled-and-held by a SC branch. This is valid for all A/D architectures employing DACs in their conversion algorithm.

The variable reference $V_{Ref}(t)$ reaches its maximum value when $\cos(2\pi f t + \varphi) = 1$. In that circumstance, $V_{Ref}(t) = \alpha + \beta$. As a result, for designs with a voltage supply of V_{DD}, this variable reference is set to reach a peak value of V_{DD} as well. In other words, if the

design has a voltage supply of 1.2 V, as is the case with most current designs in standard CMOS processes (e.g. 130-nm, 65-nm), the sum of α and β when $\cos(2\pi f t + \varphi) = 1$ is of 1.2 V. Nevertheless, this technique can be extended to different values of V_{Ref}, a feature that meshes well with the aforementioned CS-SAR topology.

Replacing Eq. 4.2 in Eq. 4.1 and working the resulting expression leads to Eq. 4.3:

$$\mathrm{D_{out}}(n) = \frac{X_{in}(t)}{\alpha + \beta \cdot \cos(2\pi f t + \varphi)} = \frac{X_{in}(t)}{\alpha} \cdot \left(\frac{1}{1 + \frac{\beta}{\alpha} \cdot \cos(2\pi f t + \varphi)} \right) \tag{4.3}$$

If the term $\frac{\beta}{\alpha} \cdot \cos(2\pi f t + \varphi)$ is assumed to be the variable x, the second term of Eq. 4.3 resembles the function $1/(1+x)$. Its MacLaurin series[1] is known and is given by Eq. 4.4:

$$\frac{1}{1+x} = 1 - x + x^2 - x^3 + x^4 - x^5 + ... = \sum_{n=0}^{\infty} (-1)^n \cdot x^n, |x| < 1 \tag{4.4}$$

Applying this line of thought to Eq. 4.3 leads to Eq. 4.5:

$$\begin{aligned} \mathrm{D_{out}}(t) = \frac{X_{in}(t)}{\alpha} \cdot \left(\frac{1}{1 + \frac{\beta}{\alpha} \cdot \cos(2\pi f t + \varphi)} \right) = \frac{X_{in}(t)}{\alpha} - \boldsymbol{X_{in}(t) \cdot \frac{\beta}{\alpha^2} \cdot \cos(2\pi f t + \varphi)} + \\ + \frac{X_{in}(t)}{\alpha} \cdot \left(\frac{\beta}{\alpha} \cdot \cos(2\pi f t + \varphi) \right)^2 - \frac{X_{in}(t)}{\alpha} \cdot \left(\frac{\beta}{\alpha} \cdot \cos(2\pi f t + \varphi) \right)^3 + ... \\ , |\beta| < |\alpha| \end{aligned} \tag{4.5}$$

From Eq. 4.5, it is shown that the crossed products originated by the series expansion, give rise to terms composed by the input signal multiplied by the signal term provided by the LO. The bold term in (4.5), $X_{in}(t) \cdot \frac{\beta}{\alpha^2} \cdot \cos(2\pi f t + \varphi)$, gives the desired down-converted signal. Therefore, this shows, at least theoretically, that it is possible for the ADC to frequency translate an incoming signal, thus embedding the mixing function.

A simplified block diagram of the proposed architecture is shown in Fig. 4.1, where α is the constant reference voltage provided by a bandgap circuit and the ADC acts as both a quantizer and a down-conversion stage. It should be highlighted that the variable reference signal can be generated either on-chip (via a PLL circuit) or off-chip.

[1] In mathematics, a MacLaurin series consists on a representation of a certain function as an infinite sum of terms calculated from the values of the function's derivatives centered at 0 (which is a special case of the Taylor Series) as follows:

$f(x) = f(0) + f'(0) \cdot x + \frac{f''(0)}{2!} \cdot x^2 + \frac{f^{(3)}(0)}{3!} \cdot x^3 + ... + \frac{f^{(n)}(0)}{n!} \cdot x^n + ...$

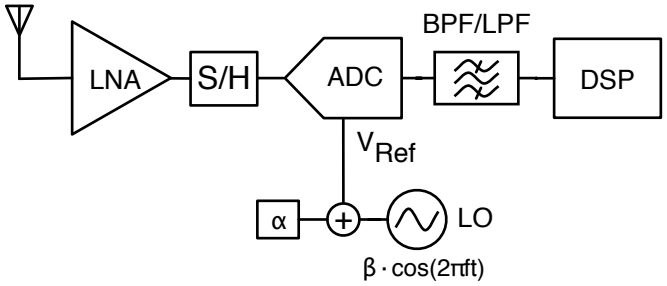


Figure 4.1: Embedded mixing receiver architecture.

4.1.1 "Two-step" approach

Notwithstanding this inherent downconverting feature of an ADC, its general mode of operation remains the same, i.e., it first samples the analog signal at its input and then proceeds to quantize it. What this means is that if the ADC is to downconvert an incoming high-frequency signal, such as those following certain communication standards like GSM or Wi-Fi, it has to sample it first. To do so without loss of information, the ADC has to satisfy the Nyquist sampling theorem, which would imply a significantly high sampling rate (> 1 GHz) for the S/H subcircuit in order to avoid aliasing.

Although these high speeds can be achieved by the Parallel "Flash" ADC topology, it comes at the cost of prohibitively low resolutions (< 8 bits), disqualifying it from consideration. On the other hand, both Pipeline and SAR structures, due to current technology limitations, are unable to reach such speed demands. Consequently, the first limitation that arises from the proposed Embedded Mixing method is that it poses stringent requirements on the ADCs sampling rate.

However, if this sampling rate f_s is below the signal's Nyquist rate but at least twice its bandwidth BW, it is still possible to down-convert the signal without loss of information, as the subsampling approach shows. The main downsides here reside on the noise-folding and timing jitter sensitivity, both escalating with the subsampling ratio m used, as explained in section 2.1.4.3. Furthermore, the f_s used in this approach is limited to a certain range of values, thus imposing certain design constraints.

Despite its shortcomings, merging the subsampling approach with the Embedded Mixing method can be seen as an effective way to mitigate the speed demands placed on the S/H circuitry. As a result, the downconversion process can be carried out in two different steps as illustrated in Fig. 4.2.

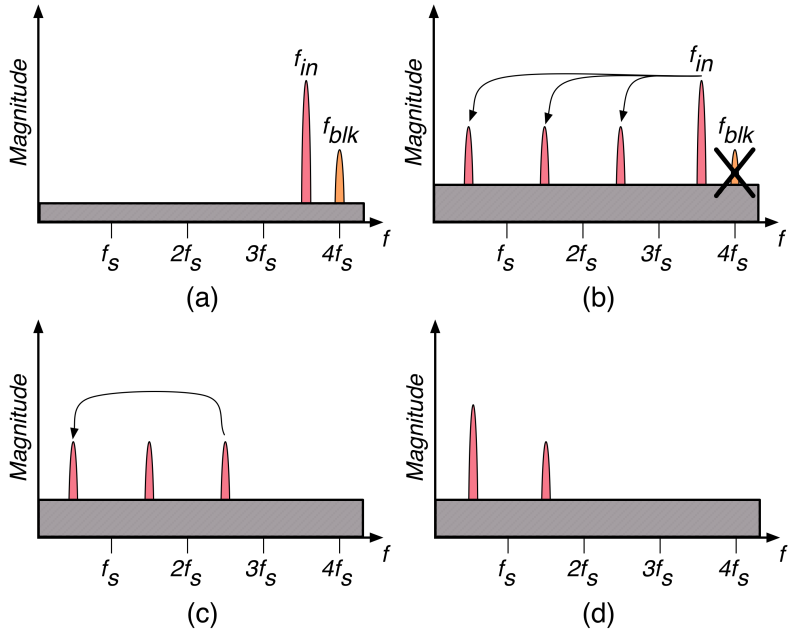


Figure 4.2: Proposed "two-step" down-conversion method with blocker rejection: (a) Signal & interferer at the input (b) 1st downconversion together with rejection of interferers centered at multiples of f_s (c) 2nd downconversion through the use of a variable reference, in the format (d) Spectrum at the output.

First, the front-end S/H capacitor(s) performs subsampling of the analog input signal to both IF and BB, according to the f_s chosen. As long as f_s verifies Eq. 2.1, image overlap is avoided. For improved performance, the S/H can be replaced by a SC Finite Impulse Response (FIR) filter responsible for tuning out blockers and other interferers. This feature will be expanded on later in this chapter, where the notches of a 4-Tap Time-Interleaved FIR Filter can be tuned in order to be placed at the same frequency of an hypothetical interferer.

Next, during the quantization phase, the signal at IF is shifted down into the BB with the aid of a variable reference signal, being summed to the signal already at the BB. This sum needs to be accurate, at the risk of creating a two-tone signal at DC (the subsampled input signal and a replica of it slightly shifted in frequency).

This "two-step" downconversion method is slightly different from what is proposed in [90, 91], where two separate subsampling stages are considered. The advantages behind it is that a small m (i.e., a higher f_s on the S/H) can be used, reducing the number of times the out-of-band noise is "folded" back and keeping the sensitivity to the timing

jitter as low as possible, and no more critical than that of common subsampling receiver schemes. Also, this lifts the f_s restrictions on the S/H, imposed by the subsampling approach (since the signal is now not down-converted straightly to BB), as long as it satisfies the Nyquist criterion.

The proposed technique, coupled with the subsampling approach on the front-end, can be seen as particularly suited for moderate-frequency communication standards (hundreds of MHz), as despite the noise-folding effect, the noise will be distributed over a wider frequency range lowering its impact on the overall SNR. Furthermore, the requirements for the oscillator that generates the variable component of the reference signal, in terms of both amplitude and phase noise, are as stringent as a regular LO used in a mixing stage are.

Using the ADC as both a downconverter and a quantizer, it's possible to completely remove the mixing stages from the system, leading to significant power and area savings. Moreover, from the RF front-end perspective it follows that both the overall NF and linearity (mainly the IP_3) will be defined solely by the preceding LNA. This is contrasted with most receiver chains, where although the LNA, following the Friis' formula, dominates the overall contribution to the NF, the latter stages contribution to the overall IP_3 are more significant over the first ones.

4.2 Design Considerations

Moving away from traditional dc-only reference signals, this Embedded Mixing technique presents the designer with a new set of variables and challenges. In that spirit, this section focuses on their analysis and proposes some solutions to those more prominent.

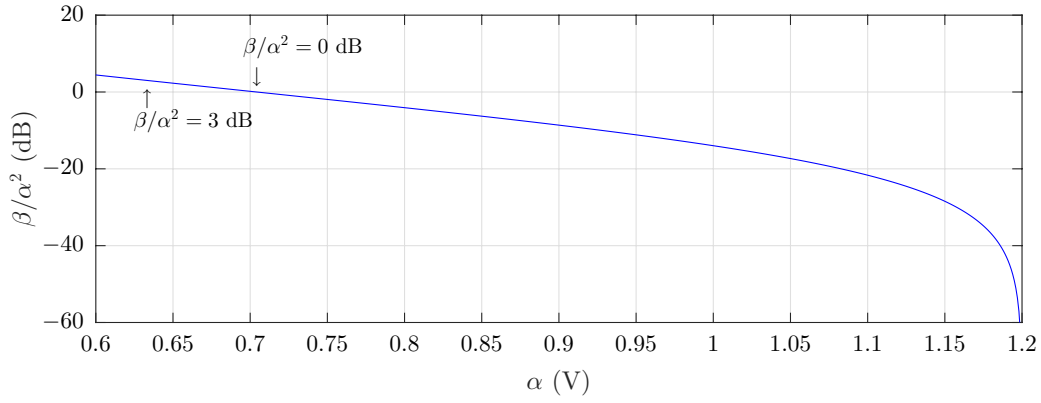
4.2.1 Impact of factor β/α^2 and subsequent terms in Eq. (4.5)

The input signal might suffer an attenuation as it is multiplied by the β/α^2 term, as shown in Eq. 4.5. This happens as long as $\beta < \alpha^2$. However, knowing that $\beta + \alpha = V_{DD}$ at peak value, i.e. $\cos(2\pi f t + \varphi) = 1$ and if one considers that $\beta = \alpha^2$ and $V_{DD} = 1.2V$, it can easily be demonstrated that for $\beta \simeq 0.5$ the input signal will not suffer such attenuation. Under these circumstances the condition of $\beta < \alpha$ still holds true (since $\alpha \simeq 0.7$) and the

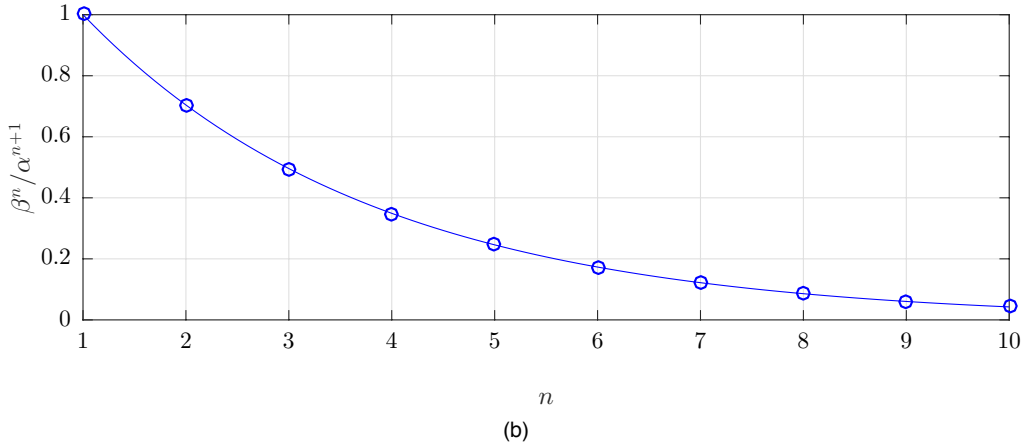
dynamic range of the ADC is not wasted.

Furthermore, with the embedded mixing technique it is possible to slightly relax the gain requirements (or accommodate for a gain drop-off) of previous stages (such as the LNA or the S/H). For instance, if one chooses to use the values of 630 mV and 570 mV for α and β respectively, the input signal would be amplified by more than 3 dB. This is a significant advantage over passive mixers, where conversion losses have to be accounted for. Also, in regards to active mixers, significant advantages are obtained in terms of cost, power consumption and area, as already stated.

Fig. 4.3(a) shows how this factor varies for a given α. Note that values below 0.6 are not plotted, as that would render Eq. 4.5 false, i.e., β would have a larger value than α.



(a)



(b)

Figure 4.3: Impact of factor β^n/α^{n+1}: (a) Signal amplification for a specific α (b) Attenuation of unwanted terms, for $\beta/\alpha^2 = 1$.

As with mixer-like nonlinear components, unwanted harmonics and intermodulation products are generated. These also need to be filtered at the output. For these terms, the

factor β^n/α^{n+1} is not a problem as its value gradually becomes less significant and rapidly decays to zero (as shown in Fig. 4.3(b) for $\beta/\alpha^2 = 1$), i.e., interferers would see its power be attenuated in relation to the input signal's power.

4.2.2 LO specifications and requirements

Most state-of-the-art precise oscillators provide an output signal with a maximum amplitude ranging from -10 dBm to +10 dBm. Thus, for state-of-the-art designs, the values required for β are perfectly achievable by modern state-of-the-art oscillators.

However, if the design requires a low amplitude for the LO (i.e., < 0 dBm), this would result in an attenuation of the input signal, as mentioned above. A way to circumvent this issue would be to slightly increase the voltage gain (VG) of the preceding LNA in a logarithmically proportional fashion, through Eq. 4.6.

$$\mathrm{LNA}_{\mathrm{VG\ increase}}\ (\mathrm{dB}) = \left| 20 \cdot \log_{10} \frac{\beta}{\alpha^2} \right| \tag{4.6}$$

Eq. 4.6 rapidly grows with α^2 and it fast becomes unacceptable to push the LNA gain above 20 dB due to several reasons, such as power and distortion increase. Thus, one may choose to distribute the required gain between the LNA and the S/H. This relaxes the requirements for the LNA while the design of a S/H with 6 dB gain is fairly easy to accomplish in a SC implementation.

Nonetheless, the requirements for the LO that generates the variable reference voltage aren't any more stringent than those of the common LOs used in a typical mixing stage. This means that the phase noise (PN) of this LO is no more critical than that of state-of-the-art LOs and amplitude noise, albeit existent, is of minor concern as shown in [92].

4.2.3 Synchronism between the Input signal and the Reference signal

When employing the proposed technique, a common issue arises: since a portion of V_{Ref} is varying over time, its value at each sampling instant will vary, which would undoubtedly lead to conversion errors. Also, a slight phase shift would also result in different values for V_{Ref}. Both these issues can be observed in Fig. 4.4.

In order to guarantee that the V_{Ref} value considered at each sampling instant is the same, but that the proposed technique still applies, the LO frequency used should be

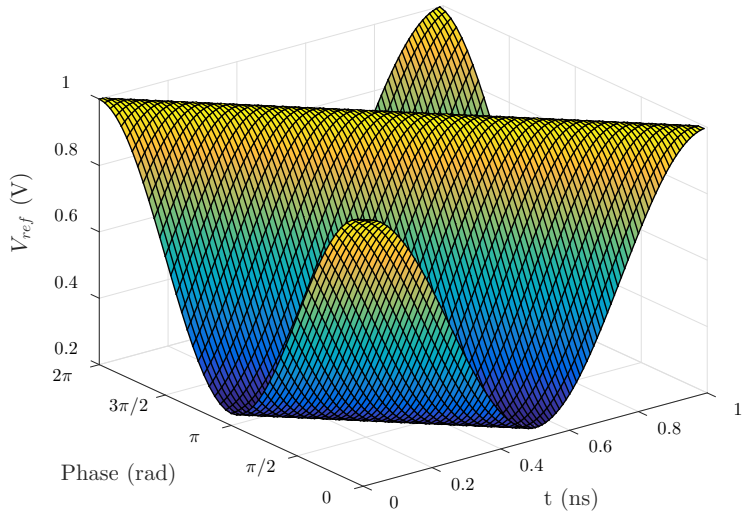


Figure 4.4: Mesh plot of $V_{Ref}(t)$ variation over time and phase, for $\beta/\alpha^2 = 1$.

a multiple of the f_s of the ADC. In that case, by matching the sampling instant with the instant where V_{Ref} has its peak value, a constant V_{Ref} would be ensured for every conversion and (ideally) no errors would occur. This could be achieved by a PLL, where the V_{Ref} signal would be synchronized to the incoming signal.

An alternative to this solution consists on "saving" the reference voltage, regardless of its frequency, in a bank of capacitors at the beginning of each conversion cycle. This is a distinctive feature of the CS-SAR ADC topology, where in a single clock-cycle the DAC capacitors are "pre-charged" with a given voltage, ensuring that during each conversion the V_{Ref} is kept constant.

4.2.4 Quantizer's Dynamic Range

A vast majority of current day wireless communications standards (such as DVB-T [93], 3GPP LTE [94] and WiMAX [95]) employ multi-carrier transmission schemes, like OFDM [96], to support their physical layer. This is because multi-carrier schemes are known to be very robust against severe time dispersion effects of multipath propagation without requiring complex receiver implementation. In particular, the main reasons behind the use of OFDM reside on its high spectral efficiency, its facility to cope with frequency-selective channels without the need for complex equalization processes and its simplicity of implementation [25].

However, these schemes and specifically OFDM present a critical issue: their transmitted signal presents large peak values to their average value (around 12 dB), i.e. a high PAPR. In practice, it can be up to N times the average power (where N is the number of carriers). This translates into severe amplification difficulties and strong nonlinear distortion effects at the transmitter output and also requires for the ADC in the receiver chain to have a higher dynamic range in order to cope with the requirements of having a small probability of clipping events, at the expense of the degradation of the SNR. Otherwise, if the PAPR is reduced it is possible for a system to either transmit more bits per second, transmit the same bits per second but with lower power consumption or both. Recently, several PAPR reduction techniques have been proposed for OFDM [97–99]. Still, by moving the ADC closer to the frontend of the receiver chain, its dynamic range must be able to accommodate both weak and strong signals.

4.3 The ADC Architecture of Choice

Taking into account all of the aforementioned design considerations, somewhat specific to the proposed Embedded Mixing technique, the ideal candidate among ADC architectures has to be selected out of the plethora of choices, with some presenting features that fit better than others.

The usage of variable references is conceptually applicable in every known flash-based ADC architecture. Furthermore, high speeds can be achieved with a significantly low latency. However, these come at the cost of resolution and area. As detailed in section 2.2.4.1, Flash topologies are quite power-hungry despite its simple implementation. All these downsides disqualify this architecture from consideration.

When the Pipeline scheme is considered, despite the increased latency, high resolutions (> 10.5b) and speeds (> 160 MS/s) can be achieved. At first glance, the Pipeline ADC might look like the perfect candidate for the implementation of the proposed Embedded Mixing technique. Yet, technology scaling imposes a significant challenge in the design of high-gain high-speed residue amplifiers at low supply voltages. Furthermore, in a Pipeline ADC the reference is based on the input sample and each stage of the converter is processing a different sample at the same point in time. Therefore, this would require not one but N variable references, where N is the number of stages in the pipeline. This is a significant area and power overhead.

When it comes to $\Sigma\Delta$ Modulators, this architecture can be seen not as a candidate but more as the existing alternative in the field of IF-to-digital conversion. But despite the reported high resolutions (> 12b), the potential for instability and consequently the limited dynamic range, cannot be ignored, aggravated by the fact that several communication standards employ multi-carrier modulations with high PAPR.

The last scheme to be considered, the SAR ADC, not only is considered as the most energy efficient but can also present competitive resolutions (> 8b) and speeds (> tens of MSps).

In particular, between the CR and CS approaches, the latter has a number of distinctive features that make it the candidate best suited for the proposed technique:

i) it can operate with over-rail inputs, by properly setting the ADC conversion gain, which then dictates the sizing of the unit capacitor in the DAC array and the sampling capacitors;

ii) it is suited for low power applications, not requiring amplifiers of any sort and the reference buffer does not need to be active during the whole conversion;

iii) since the entire array is pre-charged to the reference during the sampling phase, a single reference generation circuit is required. This ensures that each sample is properly quantized with every bit in the output word considering the same reference value.

With this in mind, the CS-SAR architecture is chosen to implement the Embedded Mixing technique. Next, an 8-bit CS-SAR ADC is designed (as an example) with the aid of *quasi-ideal* blocks, to verify the validity of the proposed technique.

4.3.1 Example with 8-bit CS-SAR ADC

Despite all the mathematical proof behind the proposed technique, it is essential to verify how this concept translates to circuit-level. As a matter of fact, in [14] high-level models were designed to represent three distinct approaches when it comes to a receiver chain: the commonly used and well established Low-IF architecture, followed by a Subsampling implementation. Both are contrasted with the Embedded Mixing Technique. Not only is the proposed technique shown to be viable, but it is also concluded that the impact in performance due to phase noise in the local oscillator of the variable reference voltage is comparable to that in traditional receiver chains.

Moving into circuit level design, where factors such as thermal noise and parasitics have to be accounted for, an 8-bit fully differential CS-SAR ADC that resorts to the proposed technique to downconvert a high frequency signal is designed to demonstrate its viability. The block diagram of this two-step downconverting radio receiver (single-ended implementation) fully embedded into a CS-SAR ADC is shown in Fig. 4.5.

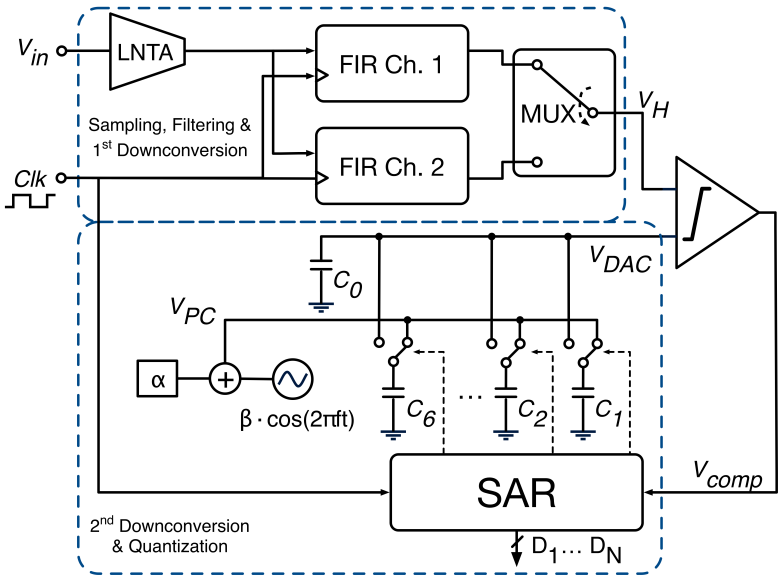


Figure 4.5: Block diagram of a two-step downconverting radio receiver, fully embedded into a CS-SAR ADC, with optional embedded filtering.

Here the input signal is assumed to be available right after the Low Noise Transconductance Amplifier (LNTA). The first downconversion step is performed by an n-tap FIR filter, that serves the additional purpose of filtering out blockers and/or interferers.

4.3.1.1 4-Tap Time-Interleaved FIR Filter

The block diagram of the 4-tap FIR filter used, as an example, in the proposed architecture, is shown in Fig. 4.6.

During the sampling period T_s, the output current of a LNTA is integrated n times into sampling capacitor C_S using specific weights, which are controlled by the LNTA.

The filter works with three different clock phases: the reset phase, in which the sampling capacitor C_S is reset to remove the memory effect from the previous sample; the (successive weighted) integration phase, where the current generated by the LNTA is integrated into the sampling capacitor during period T_i; and the readout phase, where the charge stored in C_S is read by the subsequent circuit [100].

Since T_s determines where the frequency folding occurs and T_i the location of the zeros, it is convenient that $T_i = T_s$. Due to the need for reset and readout phases, time-interleaving is used. Considering the output current of the LNTA during the k^{th} integration phase as $i_k(t) = gm \cdot w_k \cdot e^{j\omega t}$, the voltage in the C_S capacitor after k integration clock

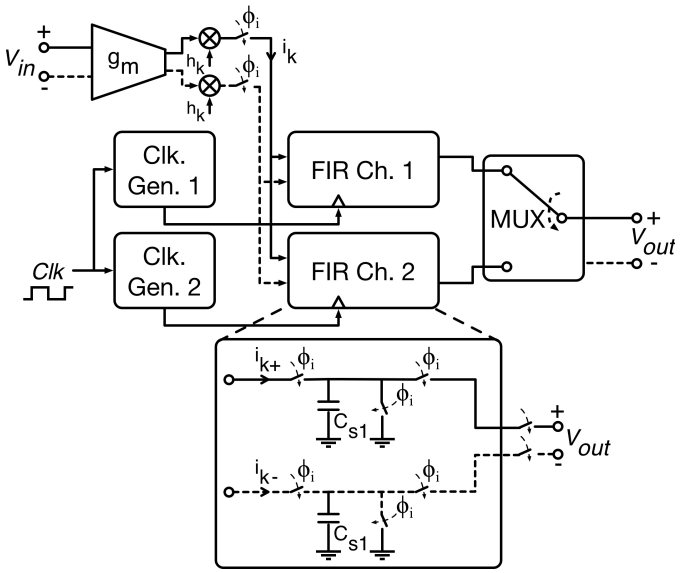


Figure 4.6: Implemented 4-Tap Time-Interleaved FIR Filter, with one channel expanded.

phases is given by Eq. 4.7.

$$v_{out}(nT_s) = \frac{gm}{C_S}\sum_{k=0}^{n-1}\left(w_k \int_{nT_s+kT_f}^{nT_s+kT_f+T_i} e^{j\omega t}dt\right) \tag{4.7}$$

where T_f includes the integration time and the dead time between integration phases. Considering $z = e^{j\omega T_f}$, the magnitude of the transfer function H is given by Eq. 4.8.

$$|H(j\omega)| = \frac{gmT_i}{C_s} sinc\left(\frac{\omega T_i}{2}\right)\sum_{k=0}^{n-1} w_k z^{-k} = H_{sinc}\cdot H_{FIR} \tag{4.8}$$

Using Eq. 4.8, by changing the weights w_k, it is possible to move the location of the notches and even the type of filtering function (lowpass, bandpass, etc.) that the FIR implements, allowing for the placement of notches in all frequencies in which interferences/blockers may occur. As it is, the implemented front-end FIR filter has the frequency response shown in Fig.4.7, acting as intended (i.e., bandpass filter).

4.3.1.2 8-bit Converter

The DAC array of the designed 8-bit fully-differential CS-SAR ADC follows a conventional structure (Fig. 3.2), composed by binary weighted MIMCAPS and the front-end 4-tap FIR filter (i.e. the modified S/H) capacitors C_s have a size given by 2^B C_u, with C_u representing the unit capacitor in the array. The SAR register has been implemented in

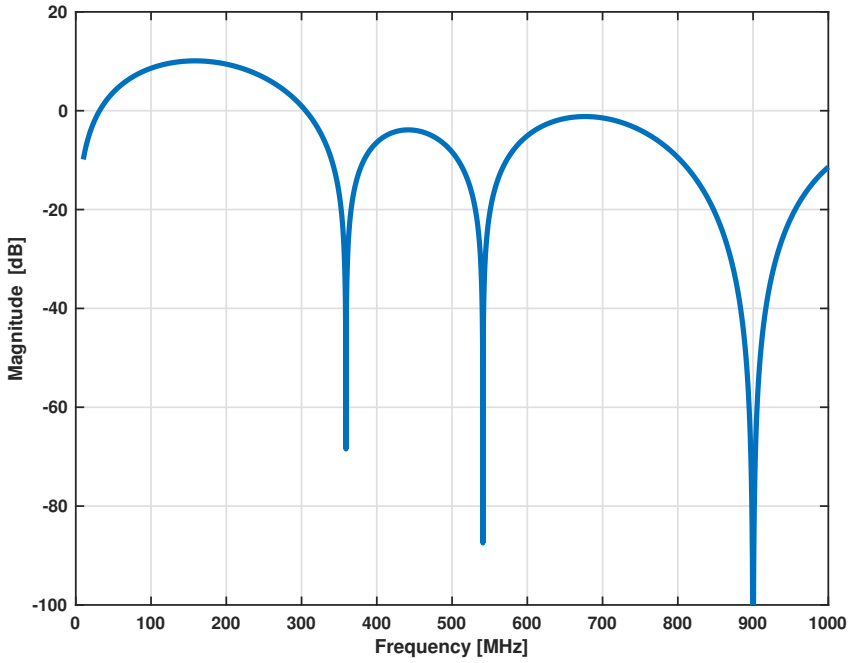


Figure 4.7: Input-output transfer characteristic of the implemented 4-tap FIR filter.

VERILOG and both the comparator and switches have been also modelled using *quasi-ideal* blocks from a standard library. Again, the main purpose of this design is to demonstrate the viability, at circuit level, of the proposed Embedded Mixing technique.

The timing diagram of the receiver is shown in Fig. 4.8. Signals $L_{1\text{-}4}$ and $T_{1\text{-}4}$ represent the four integration phases in each channel of the FIR Filter. The readout phase has a duration of roughly $3T_i$. The "pre-charge" cycle occurs concurrently with the last integration phase of each channel, L_4 and T_4.

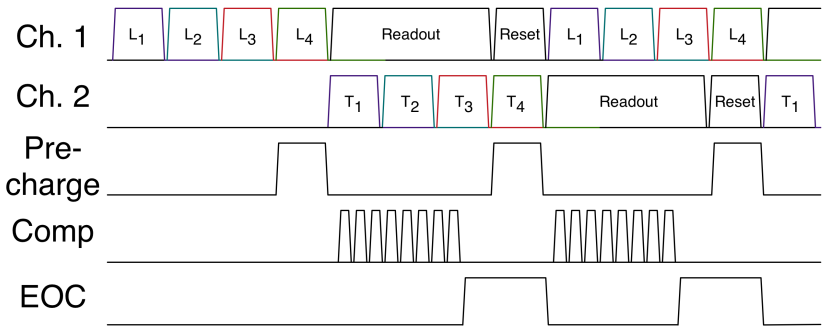


Figure 4.8: Illustrative timing waveforms during the circuit operation (Comp – comparison phases latching the comparator; EOC – end of conversion).

A single-tone input signal (f_{in}) of 10 MHz is considered, modulated with a single carrier wave of 880 MHz and with a channel BW of 200 kHz, emulating the GSM 900 standard in terms of frequency bands. For the 4-tap FIR filter a downsampling factor of $m = 8$ is considered (i.e. $f_s = 225$ MHz). As a result, the signal is initially downconverted, simultaneously, to BB and to IFs of 440 and 460 MHz. Through a reference signal with a DC voltage of 800 mV coupled with an AC sine-wave component with an amplitude of 200 mV and a frequency equal to IF (here the IF of 440 MHz was chosen), the Embedded Mixing technique, applied in the second downconversion step, allows for the signal present at IF to be further downconverted to BB, being summed to the signal previously downconverted by the subsampling FIR stage during the first step. The FFT plot of the output signal of the proposed circuit is shown in Fig. 4.9.

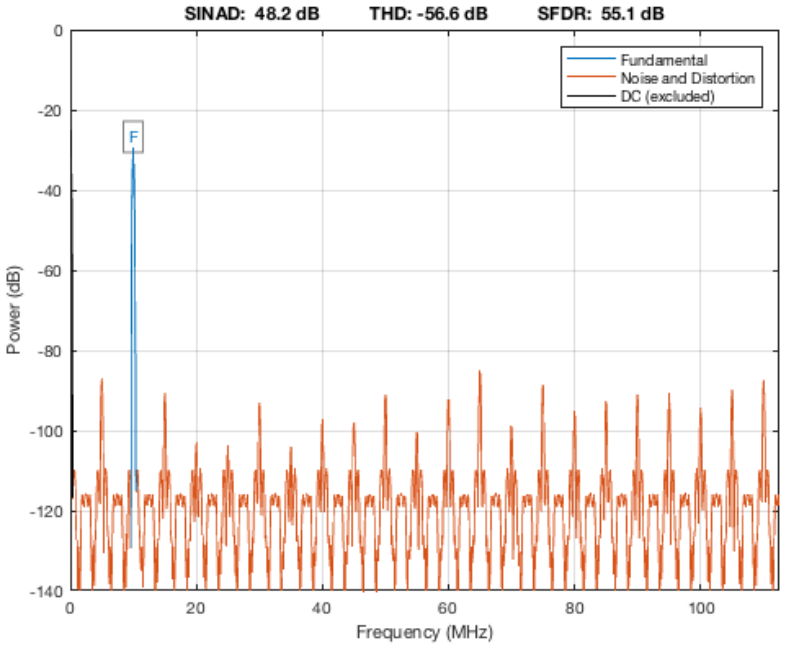


Figure 4.9: Electrically simulated Spectrum (complete receiver circuit), for f_{in} = 10 MHz, f_c = 880 MHz and f_{VRef} = 440 MHz (2^{11} points, Blackmann-Harris window).

The achieved SFDR, THD and SNDR are 55.1 dB, -56.6 dB and 48.2 dB, respectively. It should be noted that since *quasi-ideal* behaviour models have been used, even-order harmonics are negligible (as expected) and the performance of the circuit is mainly limited by the 3rd-order harmonic as well as frequency components present at multiples of $f_{in}/2$. The latter are a direct consequence of the subsampling approach and the m used. Regardless, the impact of these components would be more dramatic in conventional

subsampling approaches, as m would be necessarily higher and more than one subsampling stage would be used. Hence, this structure is able to comply with almost 8-bits of effective resolution while also entirely renouncing conventional mixing stages.

Chapter 5

An 8-bit 50 MHz CS-SAR ADC with Embedded Downconversion

Following the Embedded Mixing technique presented in the previous chapter and taking advantage of the distinctive features that make the CS-SAR ADC the ideal candidate for its on-circuit implementation, this chapter details the design of an 8-bit fully-differential converter with a sampling rate of 50 MHz that operates under a 1.2 V supply in a 0.13 µm CMOS process. In order to provide an on-chip solution for the variable reference generation, a signal PLL is used. In the interest of designing a complete LNA + ADC + PLL receiver set, a custom LNA [101] preceding the ADC was used. Its design falls out of the scope of this document and the author refers to it for further information.

5.1 Operation Principle

Illustrated through waveforms in Fig. 5.1, the operation of the proposed CS-SAR ADC can be described as follows: First, a conversion is requested when the "clk" signal is switched to logic "1", with the S/H tracking the input signal while the DAC capacitor bank is pre-charged to the reference voltage V_{Ref}. Although this reference voltage is varying, the same value is stored in each capacitor once the respective switches are opened via the "clk" signal being pulled down. Similarly, nodes $V_{cp,cn}$ hold the sampled input

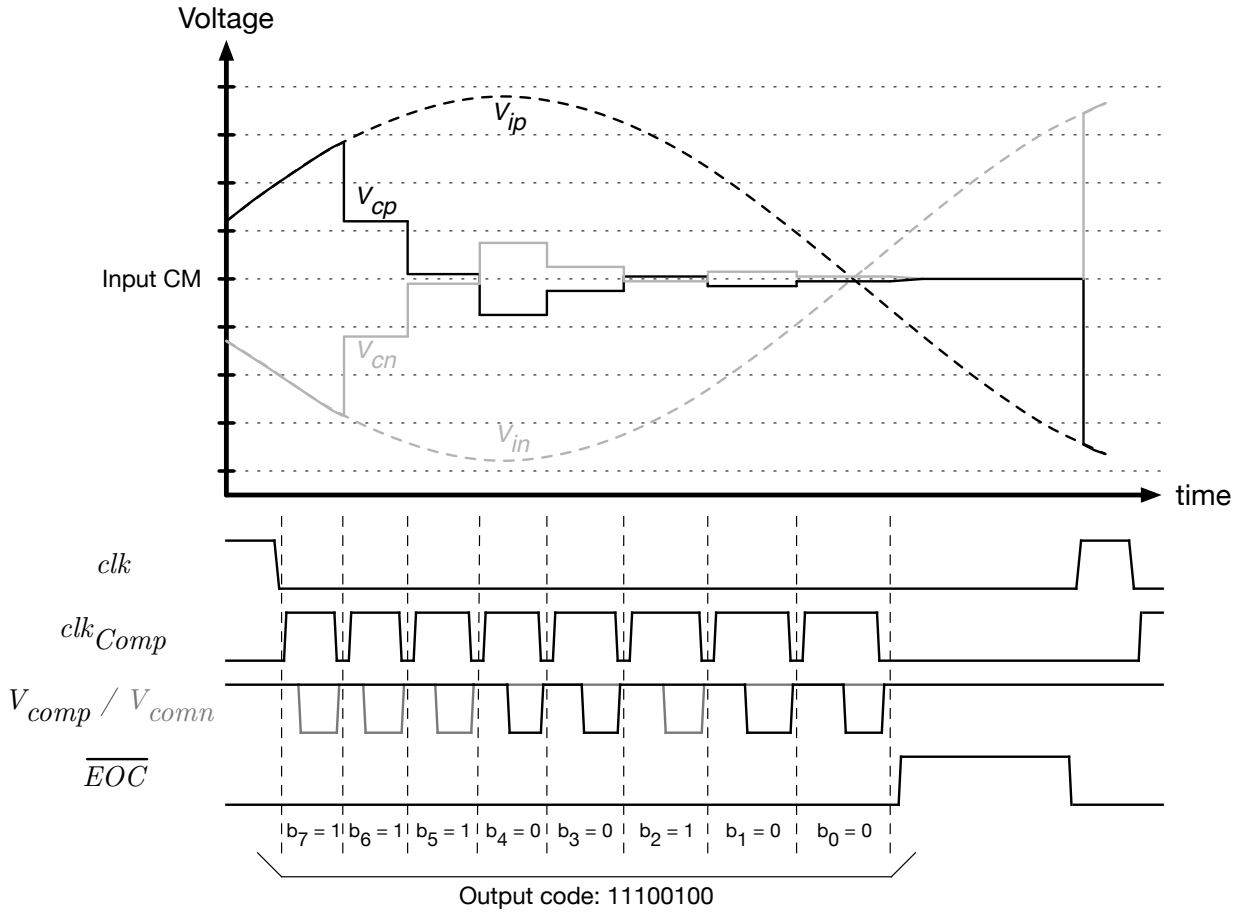


Figure 5.1: Illustrative waveforms and timing diagram of the 8-bit CS-SAR ADC operation. Greyed out signals represent a signal's counterpart.

voltage. As such, the MSB is directly evaluated, with the comparator being triggered by the controller. In accordance with the comparison result, the SAR determines the summation or subtraction of charge from the $V_{cp,cn}$ nodes and directs the larger capacitor in the DAC to be connected in a parallel or anti-parallel manner, through the respective switches. This process is repeated for the subsequent bits while the voltage difference between nodes V_{cp} and V_{cn} gradually decays to zero. The SAR controller is responsible for storing each bit's respective value. Once the 8-bit word has been decided, the 'end-of-conversion' is flagged at the "$\overline{\text{EOC}}$" output.

5.2 CS-SAR ADC implementation

The proposed ADC topology is depicted in Fig. 5.2. It follows a conventional structure of a S/H block followed by a binary-weighted DAC, a comparator and the successive approximation logic. Voltage boosters are used to improve the linearity of the DAC switches, while the comparator is activated through a self-timing feedback loop with controllable delay. Next, the design of each block is detailed.

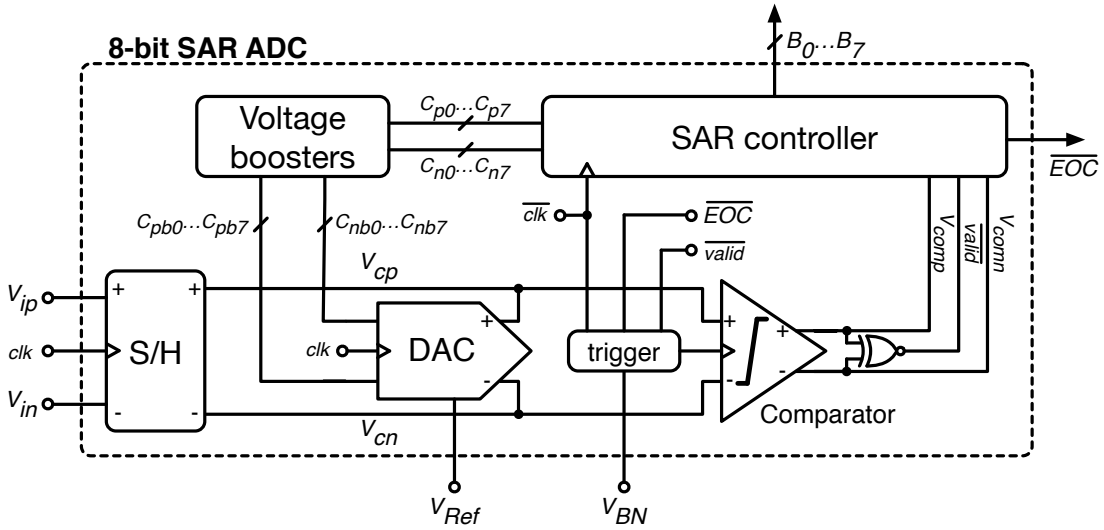


Figure 5.2: Proposed 8-bit CS-SAR ADC diagram.

5.2.1 S/H

The input passive S/H circuit, illustrated in Fig. 5.3, comprises a simple set of NMOS switches, bootstrapped to ensure proper operation and linearity throughout the entire input range [0V - 1.2V], together with dummies to reduce charge injection. Each sampling capacitor has a value of around 1.27 pF.

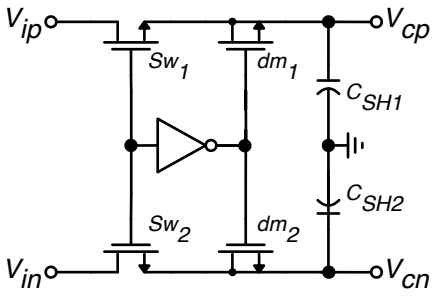


Figure 5.3: Schematic of the implemented S/H circuit (bootstrapping circuit not shown).

5.2.2 DAC

In conventional binary-weighted arrays, an N-bit ADC would require a DAC with a size of $2^N \cdot C_u$, with C_u representing the unit capacitor. Hence, to reduce the overall DAC area, a charge-partitioning scheme similar to the one used in [82] is employed. Here, the 3 LSB capacitors (C_3, C_2 and C_1), together with auxiliary capacitor C_0, have a size of $C_u \approx$ 20 fF, the minimum allowed by the technology[1] for metal-oxide-metal (MOM) capacitors. The remaining capacitors (C_7, C_6, C_5 and C_4) have a value of approximately 320, 160, 80 and 40 fF respectively. The DAC array is illustrated in Fig. 5.4.

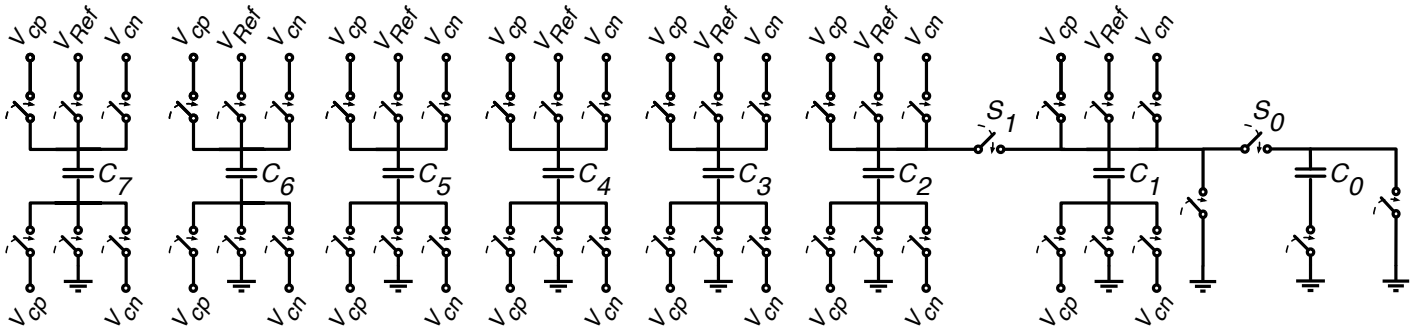


Figure 5.4: Schematic of the 7-bit DAC. (Dummies and control signals not shown).

Since the switches that add or subtract charge to the $V_{cp,cn}$ nodes remain connected until the end of the conversion, dummy switches are not required (as there is no charge injection onto the nodes due to these switches). On the other hand, pre-charge switches only stay connected during the sampling period, hence dummies are used. All of these switches are just NMOS transistors, as opposed to transmission gates. This is intentional, as despite its independent on-resistance, transmission gates require a control signal and its complement, and the latter does not come for free (as one might assume) in this topology. In other words, the circuit complexity would increase just to accommodate them, with a significant increase in area as well.

[1] UMC L130 Mixed-Mode/RF

5.2.2.1 Voltage Boosters

Most switches in this design resort to small NMOS transistors. To ensure proper operation, each is driven by bootstrapped voltages. To that end, the bootstrapping circuit [102], shown in Fig. 5.5, is used.

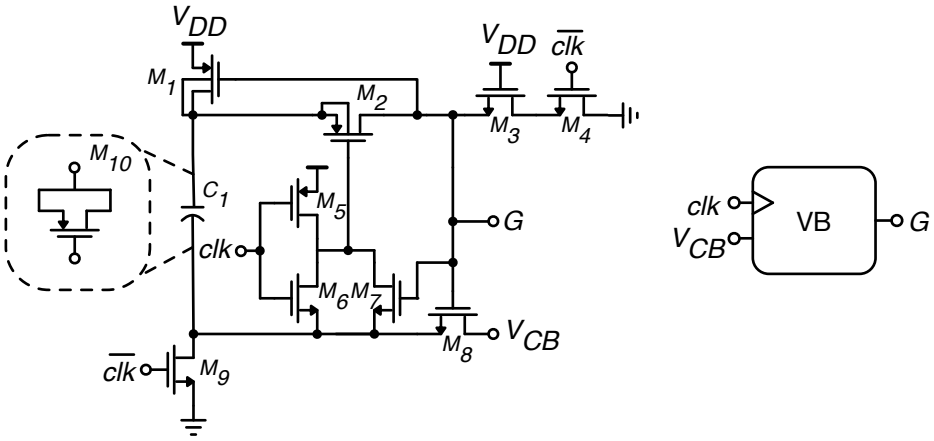


Figure 5.5: Schematic of the voltage boosting circuitry employed in the ADC (single instance).

The goal of this circuit is to "boost" the voltage at the gate of each switch by summing an external voltage, V_{CB}, to it, thereby improving the switch linearity. This voltage is generated and controlled off-chip. Both the S/H and DAC "clk" switches, as well as the switches that connect each capacitor to the $V_{cp,cn}$ nodes require bootstrapping. So, in total, 18 voltage boosters are used in this design.

It operates in two phases: during the first phase, capacitor C_1 is charged to the supply voltage V_{DD} through transistors M_1 and M_9. In the meantime, the output node is grounded by transistors M_3 and M_4. Once the clock signal toggles to "high", capacitor C_1 is placed in series with the external voltage V_{CB}, leading to a voltage at the output node G of $V_{DD} + V_{CB}$, effectively "boosting" the gate voltage of the switch driven by this circuit.

5.2.3 Comparator

The dynamic comparator [103, 104] widely known in literature as the StrongARM, is used, as shown in Fig. 5.6. This architecture relies on a positive feedback loop to improve speed and provide rail-to-rail outputs. The use of back-to-back inverters yields zero static power consumption.

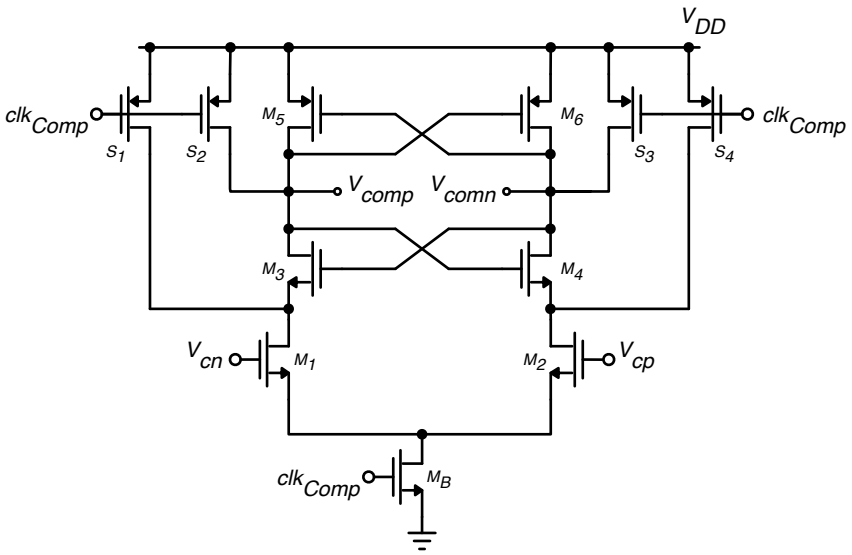


Figure 5.6: StrongARM latch topology used.

All transistors have minimum length (0.12 µm), with the input pair ($M_{1,2}$) having a width of 30.4 µm. The input pair sizing is critical, as it defines both the voltage gain and the input-referred noise. The comparator presents a (simulated) input-referred noise of 0.15 mV, which is below the estimated quantization noise of ≈ 1.35 mV $\left(\frac{V_{LSB}}{\sqrt{12}}\right)$ and limits the maximum achievable ENOB to around 7.9 bits, according to [81]. The comparison is guaranteed to occur in less than 0.2 ns.

5.2.3.1 Self-timing feedback loop

The comparator self-timing feedback loop, shown in Fig. 5.7, resorts to a 3-input AND gate with a controllable delay.

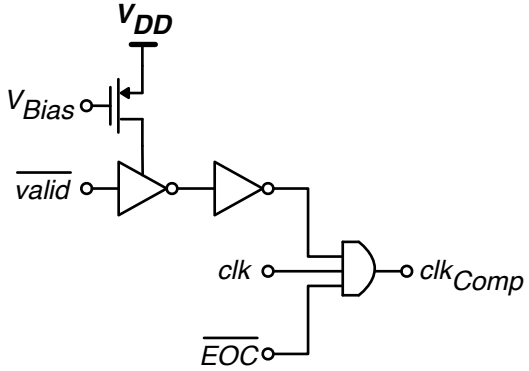


Figure 5.7: Comparator's self-timing feedback loop.

The comparator is triggered each time that all the following signals have their logic

level set to "high": clk, $\overline{\text{EOC}}$ and $\overline{\text{valid}}$. The first is pretty self-explanatory: it prevents the comparator from being activated while the converter is still sampling the input signal and once that period ends, the MSB can be decided. Signal "$\overline{\text{EOC}}$" is used to prevent comparisons after the 8-bit word has been found. Finally, "$\overline{\text{valid}}$" indicates if both comparator's outputs are equal (in reset state) or not (a comparison as successfully been performed), through an XNOR gate. In other words, in order for a new comparison to be performed, the previous has to be completed. This signal is fed into a pair of inverters, with the first one being a current-starving variant. The PMOS controls the fall time (to accommodate for the comparison time) via the gate voltage V_{Bias}, generated externally. The rise time is kept unchanged in order to enable the following comparison as soon as possible.

5.2.4 SAR

The SAR controller is a critical block in the design, with its main function being to perform the binary search. Although synchronous controllers can be employed, they rarely are the most power efficient solution. On the other hand, designing a controller based on standard cells can be rather intuitive and easy, but at the cost of area optimization. Thus, in order to improve both power and area efficiency, full-custom self-timed controllers are usually the architecture of choice. Here, the controller shown in Fig. 5.8 [88] is used.

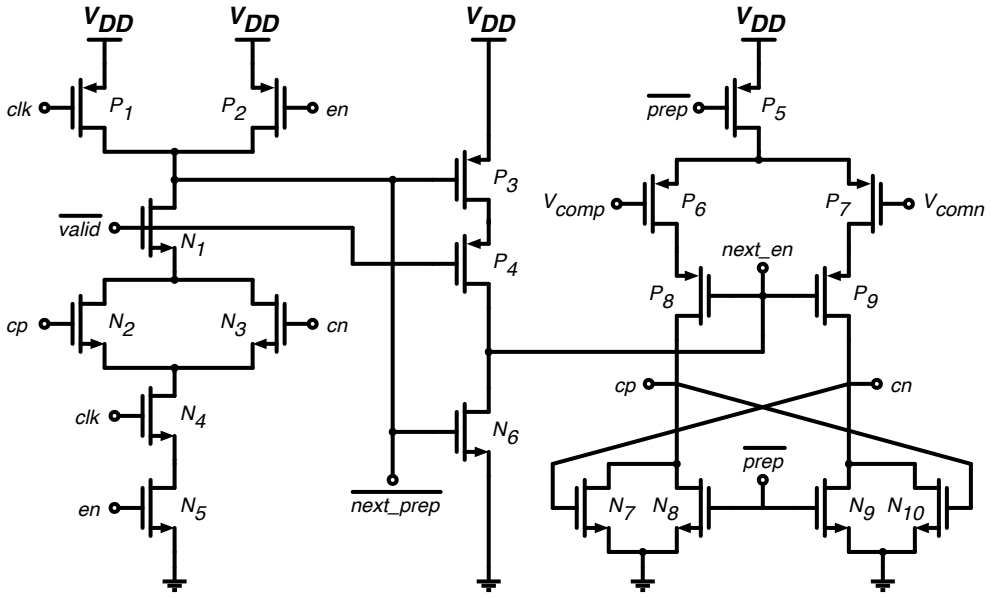


Figure 5.8: Schematic of a single cell of the SAR controller.

The controller is composed by a set of 8 instances of the logic circuit shown in Fig. 5.8, based on a true-single-phase-clocked (TSPC) latch. The controller itself requires 4 inputs: both comparator's outputs V_{comp} and V_{comn} and signal "$\overline{\text{valid}}$", as well as the sampling clock "clk". As its outputs, control signals c_{pK} and c_{nK} (with K ranging from 0 to 7) for every bit are generated, with each comparison performed. Internally, each instance also generates the signals required to trigger the following one. The last instance also outputs the "$\overline{\text{EOC}}$" signal, which indirectly prevents the controller from being activated once all the bits have been resolved.

Transistors $N_1 - N_6$ and $P_1 - P_4$ form the TSPC latch, followed by a differential regenerative stage composed by transistors $N_7 - N_{10}$ and $P_5 - P_9$. The pair $M_{N2,3}$ main purpose is to allow the discharge of "$\overline{\text{next\_prep}}$" only after the respective c_p or c_n are set. These signals are also responsible for connecting the respective DAC capacitance in a parallel (c_p) or anti-parallel (c_n) fashion. The feedback loop created by transistors N_8 and N_9 prevents fluctuation on the respective nodes, setting c_p to either logic "1" or logic "0" and c_n to its respective complement and storing the result. The feedback arrangement cuts off the dc patch between V_{DD} and ground, preventing static power drain.

5.3 Integer-N PLL implementation

To provide an on-chip solution for the variable reference signal generation, a dedicated signal PLL is used [105]. The topology is based on an integer-N charge pump PLL [106]. It generates high frequency, low distortion and low jitter amplitude controlled IQ sinusoidal signals, which in turn are used as differential variable references. The use of this PLL comes with the added benefit of forgoing dedicated bandgap circuits and reference buffers. The block diagram of the PLL is detailed in Fig. 5.9, with a brief description of each block given next.

This PLL takes four external signals: The external reference current PLL_{IRef} sets an independent reference current that is then mirrored and distributed to the internal blocks that compose the PLL, via a global biasing circuit. The designed PLL is flexible enough to generate output frequencies around 250 and 500 MHz, enough to accommodate input signals under carrier waves tenfold that of the sampling frequency of the designed ADC.

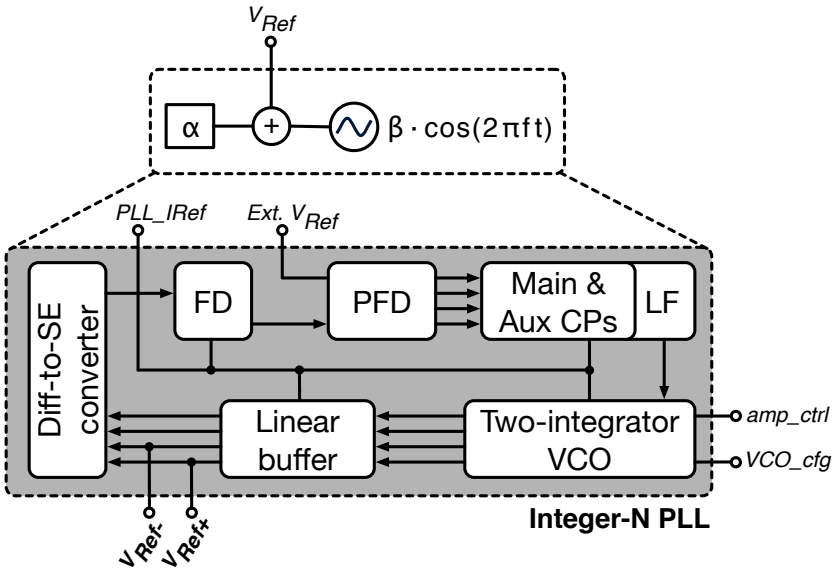


Figure 5.9: Integer-N PLL topology diagram (global biasing circuit not shown).

The desired range of output frequencies is determined by signal VCO_{cfg}, which is set by an external switch. The amplitude of the generated sine wave signals is set by the amp_{ctrl} pin. These signals are generated based on an external low frequency reference clock, Ext. VRef. Thus, the only off-chip component required is a stable low frequency reference clock. This can be implemented by a inexpensive crystal oscillator.

5.3.1 Phase Frequency Detector

A sequential three-state Phase Frequency Detector (PFD), based on a dual D-type flip-flop structure [107], is employed. The schematic is depicted in Fig. 5.10. Signal v_{div} comes from the frequency divider (FD) in Fig. 5.9.

It uses an asynchronous race-free design. When compared to conventional NAND-based designs, this PFD minimizes the perturbation in the loop filter voltage by reducing the simultaneous activation of signals "up" and "$down$" during the steady state operation of the PLL. Hence, jitter performance is improved.

A significant delay between signals $up/down$ and their negated versions $\overline{up}/\overline{down}$ would lead to systematic imbalances in the operation of the charge pumps that follow, increasing the reference spurs of the PLL. In order to shorten (and possibly eliminate) the difference between signals, a pair of transmission gate and CMOS inverter are used to equalize the respective propagation delays.

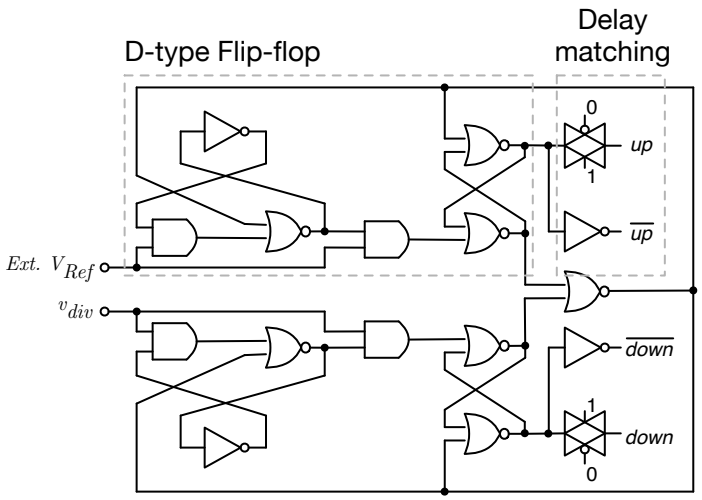


Figure 5.10: Schematic of the phase frequency detector.

5.3.2 Charge Pumps & Loop Filter

A conventional third-order passive loop filter is used, in conjunction with a main and auxiliary charge pumps, as shown in Fig. 5.11. These charge pumps follow a capacitance multiplication scheme, proposed in [108], that aims to alleviate the total capacitance of the integrated loop filter, reducing its area overhead by a factor of roughly $\sim 20\%$ in this particular design. The main and auxiliary charge pumps are similar in design with the latter being a scaled down version of the former.

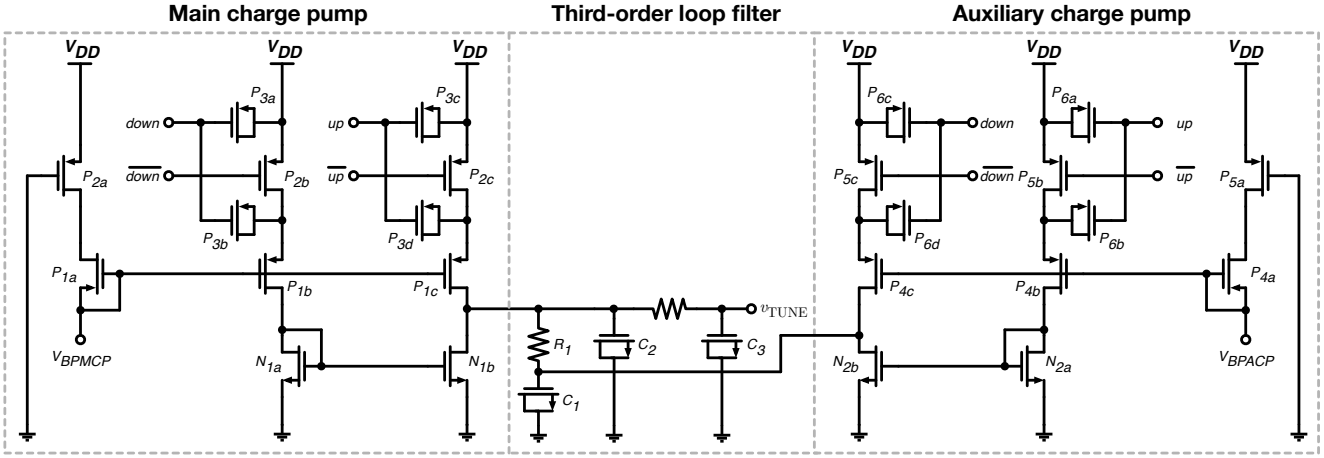


Figure 5.11: Schematic of the charge pumps and third-order passive loop filter. The biasing voltages V_{BPMCP} and V_{BPACP} are generated from the biasing circuit and the external reference current PLL_{IRef}.

The loop filter has a transfer function given by Eq. 5.1.

$$\frac{V_{out}}{I_{in}} = \frac{1}{s\cdot(C_1+C_2+C_3)} \cdot \frac{1+s\cdot R_1\cdot C_1}{\left[1+s\cdot\frac{R_1\cdot C_1\cdot(C_2+C_3)+R_2\cdot C_3\cdot(C_1+C_2)}{C_1+C_2+C_3}+s^2\cdot\frac{R_1\cdot R_2\cdot C_1\cdot C_2\cdot C_3}{C_1+C_2+C_3}\right]} \tag{5.1}$$

The poles and zero in this equation, as well as the dc gain, dictate most of the dynamic properties of the PLL, such as its stability. Consequently, the sizing of the loop filter components was optimized to meet a bandwidth of 200 kHz and a Butterworth filter response.

5.3.3 Two-integrator VCO

Between *LC* and *RC* oscillators, the former has a superior phase noise performance. However, it falls short in terms of tuning range and area overhead, when compared to the latter. Out of the known RC oscillator topologies, the two-integrator Voltage-Controlled Oscillator (VCO) emerges as the one capable of generating low distortion sinusoidal signals, since it can operate in the linear regime [27], while also having a wide tuning range. Thus, it is a suitable candidate to generate the IQ signals used in the variable reference.

The schematic of the implemented two-integrator VCO is illustrated in Fig. 5.12. It is preceded by an input rail-to-rail buffer and a voltage-to-current (V/I) converter. These two blocks are also briefly detailed next.

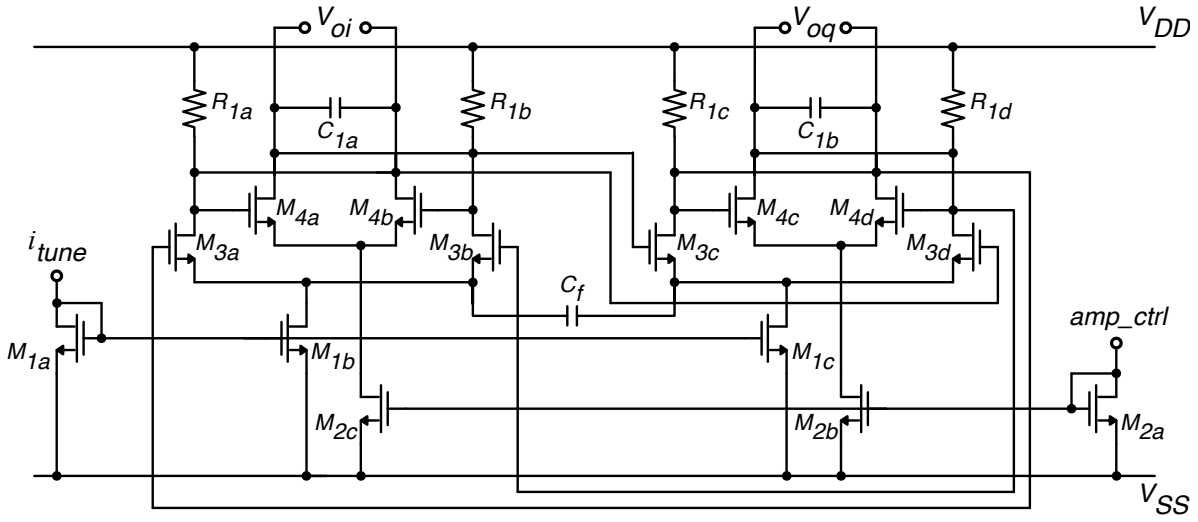


Figure 5.12: Schematic of the two-integrator oscillator, adapted from [105].

It is composed by a couple of differential pairs and a pair of switched-capacitor banks. Two additional differential pairs, with their outputs cross-coupled to the inputs, implement negative transconductance to compensate the losses due to the biasing resistors R_{1a-d} and also provide amplitude control of the output signals, via the external signal *amp_ctrl*. This, in turn, allows the oscillator to operate in the linear regime.

The filtering capacitor C_f reduces the distortion of the generated signals, by attenuating the amplitude of the second harmonic present on this nodes, in a low-pass filtering manner.

When in linear operation, the two-integrator VCO generates quadrature sinusoidal output signals $V_{oi,oq}$. The oscillation frequency is given by Eq. 5.2:

$$f_{\text{osc}} = \frac{g_{\text{m3}}}{2\pi C_1} \tag{5.2}$$

where $C_1 = C_{1a} = C_{1b}$ and g_{m3} is the transconductance of each integrator's differential pair. This transconductance can be adjusted by means of the independent reference current *i_tune*, that mirrors the external reference current PLL_{IRef}.

In accordance with *VCO_cfg*, the VCO operates around either one of two tuning characteristics, 250 (*VCO_cfg* = 1) or 500 MHz (*VCO_cfg* = 0). When operating at 250 MHz, the VCO has a gain K_{VCO} of about 125 MHz/V, that roughly doubles to around 250 MHz/V once the 500 MHz tuning characteristic is selected. In practice, the capacitance value of the switched-capacitor banks $C_{1a,b}$ "seen" by the VCO is halved, from 1.3 to 0.65 pF.

To tune the oscillation frequency inside a given characteristic, the reference current[2] *i_tune* is adjusted accordingly. This current is produced by the preceding V/I converter, since the output of the loop filter is a voltage. In order to use the entire voltage swing available by the charge pumps, an input rail-to-rail buffer is also used. The schematic for the V/I converter and rail-to-rail buffer is shown in Fig. 5.13.

The V/I converter is built around a voltage-controller resistor, implemented here by PMOS transistors $P_{1,2}$. Diode-connected transistor P_2 helps linearising the V/I transfer characteristic. Resistors $R_{1,2}$ act as a 2/3 voltage divider, mapping the voltage range of

[2] In advanced CMOS technologies, it is preferable to perform this tuning in the current domain, since it offers a wider tuning range and better linearity.

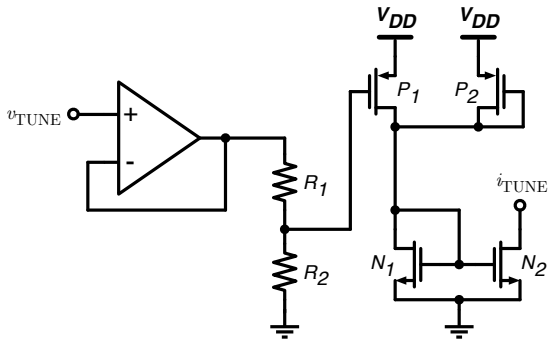


Figure 5.13: Schematic of the rail-to-rail buffer and V/I converter.

[0V - 1.2V] at the output of the buffer to a maximum voltage range of [0V - 0.8V] at the output of the divider.

5.3.4 Frequency Dividers

A programmable frequency divider, based on a modular structure consisting of a chain of 2/3 divider cells connected like a ripple counter is used. Each cell is built using four D-type flip-flops and three AND gates. This frequency divider, by means of 6 control bits, allows integer frequency division from 32 to 127.

5.3.5 Linear Buffer

Since the output of the integer-N PLL is to be connected to the DAC array, a simple source follower does not suffice, due to its high output resistance. A modified super source follower [109], shown in Fig. 5.14, is used to output the variable reference voltage generated by the VCO around a certain common-mode voltage, without penalty in regards to the output voltage swing.

Considering that the output common-mode voltage is, in practice, the α component of the variable reference voltage, the modified super source follower is biased with a voltage of $\alpha + V_{GS}$, where here V_{GS} is the gate-source voltage of transistors $N_{2a,b}$. To do so, a high-pass RC network, composed by capacitor C_{1a} and resistors $R_{1a,b}$ for the positive path (and C_{1b} and $R_{1c,d}$ for the negative path) are used.

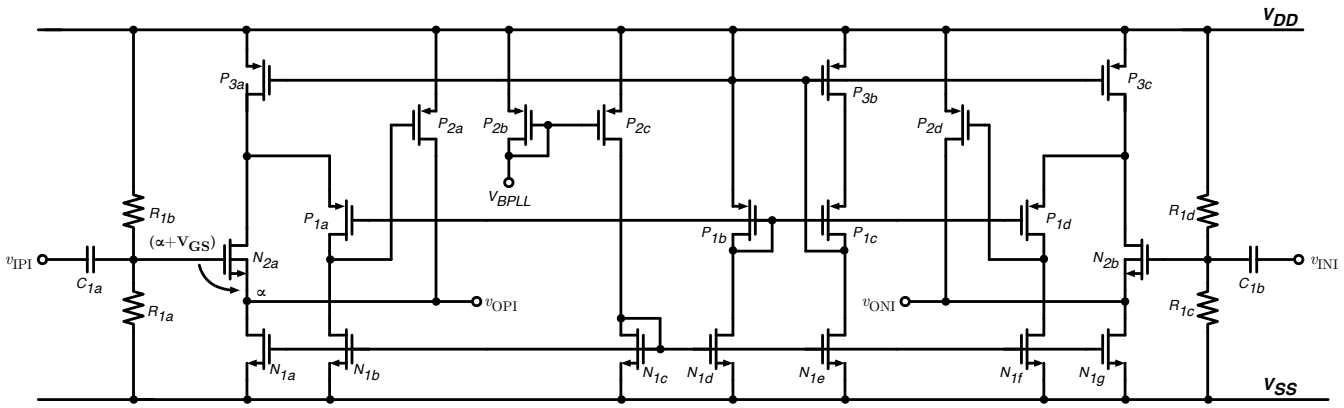


Figure 5.14: Schematic of the pseudo-differential linear buffer. The biasing voltage V_{BPLL} is generated from the biasing circuit and the external reference current PLL_{IRef}.

5.4 Layout

Before presenting the obtained results, some layout considerations regarding both the 8-bit converter and the integer-N PLL are drawn. Afterwards, a brief discussion regarding the I/O ring is given. Every circuit was designed in a 0.13 µm CMOS process, using the Virtuoso® XL Layout Editor. The silicon chips were sent to fabrication to the UMC foundry.

5.4.1 Layout Considerations for the 8-bit CS-SAR ADC

- The S/H capacitors were implemented by metal-insulator-metal (MIM) structures, due to their high capacitance density per µm^2. With the layout finished and the respective parasitic capacitances and resistors extracted, the S/H was simulated with a coherently sampled maximum amplitude input signal at near-Nyquist frequency. As shown in Fig. 5.15, the S/H alone presents a SNDR of about 64 dB, compatible with 10 effective bits of linearity, guaranteeing a safety linearity margin for the 8-bit converter;

- The DAC capacitor bank was laid out in a *common-centroid* configuration (Fig. 5.16), in order to minimize mismatch effects. Here, due to the stringent limitations in terms of spacing between adjacent capacitors for MIMCAPs, MOMCAPs were used instead. It should be noted that during the layout phase, the DAC was implemented

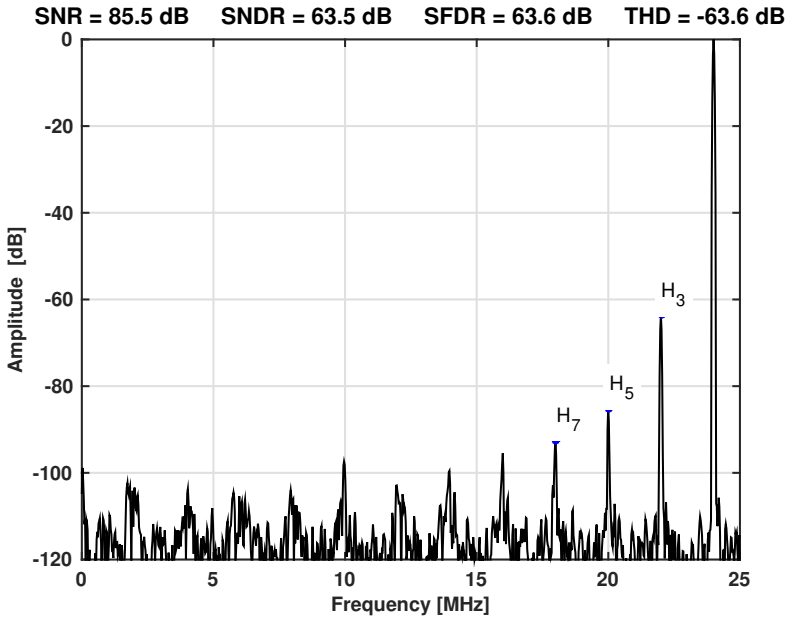


Figure 5.15: Post-layout simulated output spectrum, for a near-Nyquist frequency input signal (2048 points).

C_0	C_7	C_7	C_7	C_2
C_7	C_6	C_6	C_6	C_7
C_7	C_6	C_5	C_5	C_7
C_7	C_4		C_4	C_7
C_7	C_5	C_5	C_6	C_7
C_7	C_6	C_6	C_6	C_7
C_3	C_7	C_7	C_7	C_1

Figure 5.16: *Common-centroid* layout of the 7-bit DAC.

with both MIMs and MOMs, with the former severely impacting the performance of the overall converter, lowering its resolution by around 2-bit;

- In this design, capacitor C_1 in each voltage booster cell (Fig. 5.5) was implemented by a metal-oxide-semiconductor capacitor (MOSCAP). It is essentially a MOS transistor with the drain and source shorted, presenting the highest capacitance density among the integrated capacitors and very good matching characteristics. However, the capacitance value is highly non-linear, changing drastically with the gate voltage. Hence, it is mostly used in applications where the accuracy of the capacitor is not critical. The layout of a single voltage booster is shown in Fig. 5.17;

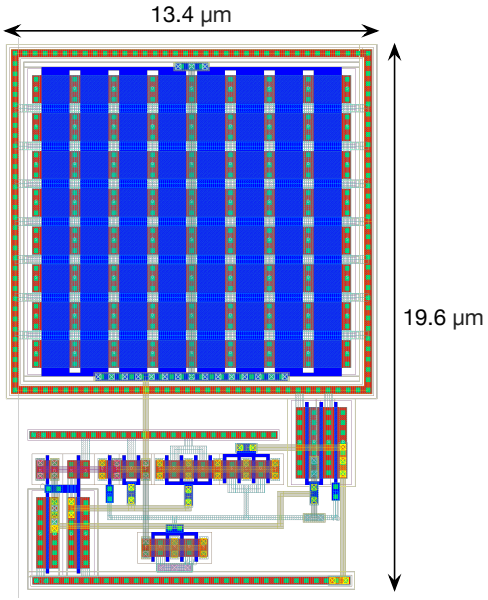


Figure 5.17: Layout of the voltage boosting circuitry employed in the ADC (single instance).

- The layout of the comparator (Fig. 5.6) is particularly important, given the fact that it is the only active element inside the ADC and therefore its noise and offset are the main factor that dictates performance in a CS approach. To that end, the input pair was laid out in a *common-centroid* fashion, as shown in Fig. 5.18. A pair of inverters in series is used to regenerate the clock signal and make up for route delays;

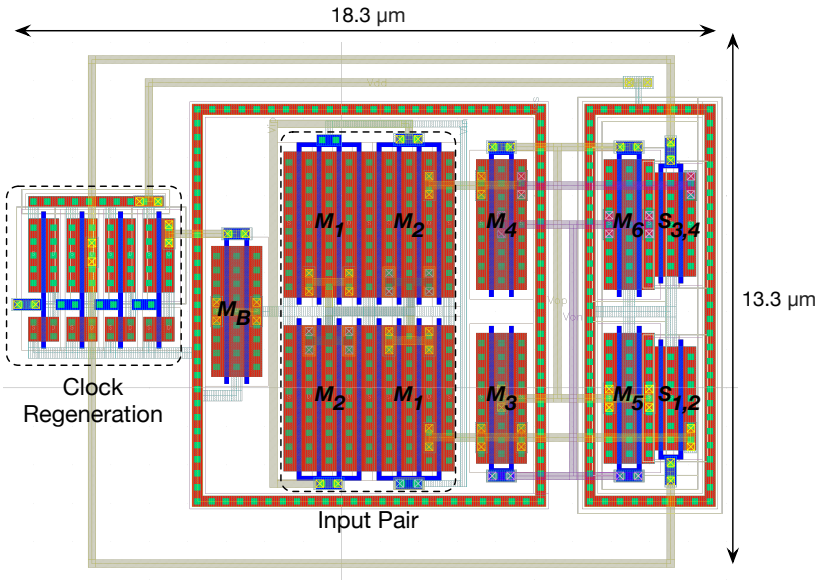


Figure 5.18: Layout of the comparator employed in the ADC.

- The SAR layout (Fig. 5.19) was done with minimal area usage and symmetry in mind. As such, transistors sharing the same signal were placed together and a standard cell frame is considered, so that each instance of the controller can be easily placed next to another. All transistors are sized with minimum length (0.12 µm) and the PMOS transistors' width are three times the NMOS (0.64 µm).

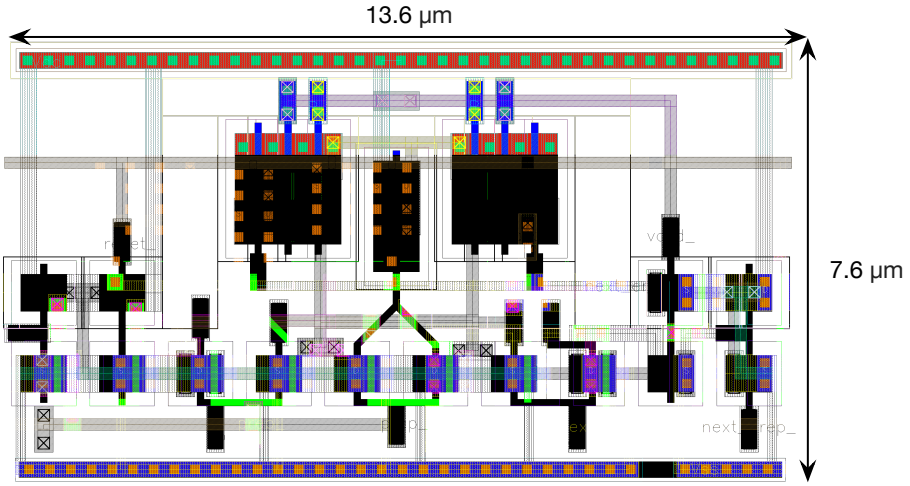


Figure 5.19: Layout of a single cell of the SAR employed in the ADC.

5.4.2 Layout Considerations for the integer-N PLL

- The layout of the PFD takes into account the matching between logic paths "up" and "$down$", in order to minimize the skew between them. Otherwise, the following charge pump operation would be adversely affected;

- Regarding the charge pumps and loop filter, the former require an accurate matching among the current mirrors, while the latter uses MOSCAPs to implement the respective capacitors, in order to reduce as much as possible, the area occupied;

- The filtering capacitor C_f used in the two-integrator VCO is implemented with an array of N+/Nwell MOS varactors[3], having a smoother C-V characteristic and lower channel resistance than a conventional MOSCAP;

- Inside the PFD, the transistors that make up each 2/3 divider cell are sized with the minimum aspect ratio allowed, with PMOS having three times the width of the

[3]Formed by thin gate-oxide over Nwell, with N+ implants at both ends of the Nwell.

NMOS, in order to make up for the former's holes low mobility[4];

- Complementary paths (positive & negative) of the modified super source follower, used as a linear buffer between the integer-N PLL and the ADCs DAC array, are laid out as symmetrical as possible.

5.4.3 I/O Pad Ring

Shown in Fig. 5.20, the I/O pad ring is composed of a set of IP cells[5] with ElectroStatic Discharge (ESD) protection. The ring itself must be continuous, in order for the ESD to be in full effect, which is ensured with specific corner cells and fillers placed between adjacent I/O cells.

Three sensitive ring sections exist: one for the sensitive signals of the employed LNA, one for the ADC and another for the PLL. Therefore, in order to minimize the noise propagation due to the supply and ground rings that power up the digital I/O buffers, strategically placed cut cells are used, hence separating the power supply domains. These cut cells are connected to the VCCKHB/GNDKHB cells (ADC_VDDD and ADC_VSSD respectively) with very low resistance lines, guaranteeing the continuity of the I/O ring.

Although different power and ground names are present within the same sensitive ring section (such as ADC_VDDA and ADC_VDDM or PLL_VDDA and PLL_VDDD), they are connected together through the I/O ring. The digital I/O buffers are powered by specific power/ground cells, VCC3IOHB and GND3IOHB (VDD3IO and VSS3IO respectively). The required number of these cell pairs is dictated by the I/O-to-power/ground ratio, that informs on the maximum number of buffers that can be powered by a single pair. In this work, only eight 3.3V output buffers are required (the digital output bits). Thus, a single power/ground pair is needed. The digital input, *VCO_cfg*, resorts to a XMHB cell that has an internal Schmitt trigger circuit enable in order to reduce this buffer's sensitivity to noise.

The pads are distributed around the I/O ring in such a way that sensitive signals are properly separated. In other words, digital-related pads are placed on the top and right

[4]This holds true for mature CMOS technologies, such as 130 and 90 nm. At lower nodes (< 45nm) the difference in mobility is nearly negligible and NMOS and PMOS are sized equally.

[5]Faraday Technology Corporation

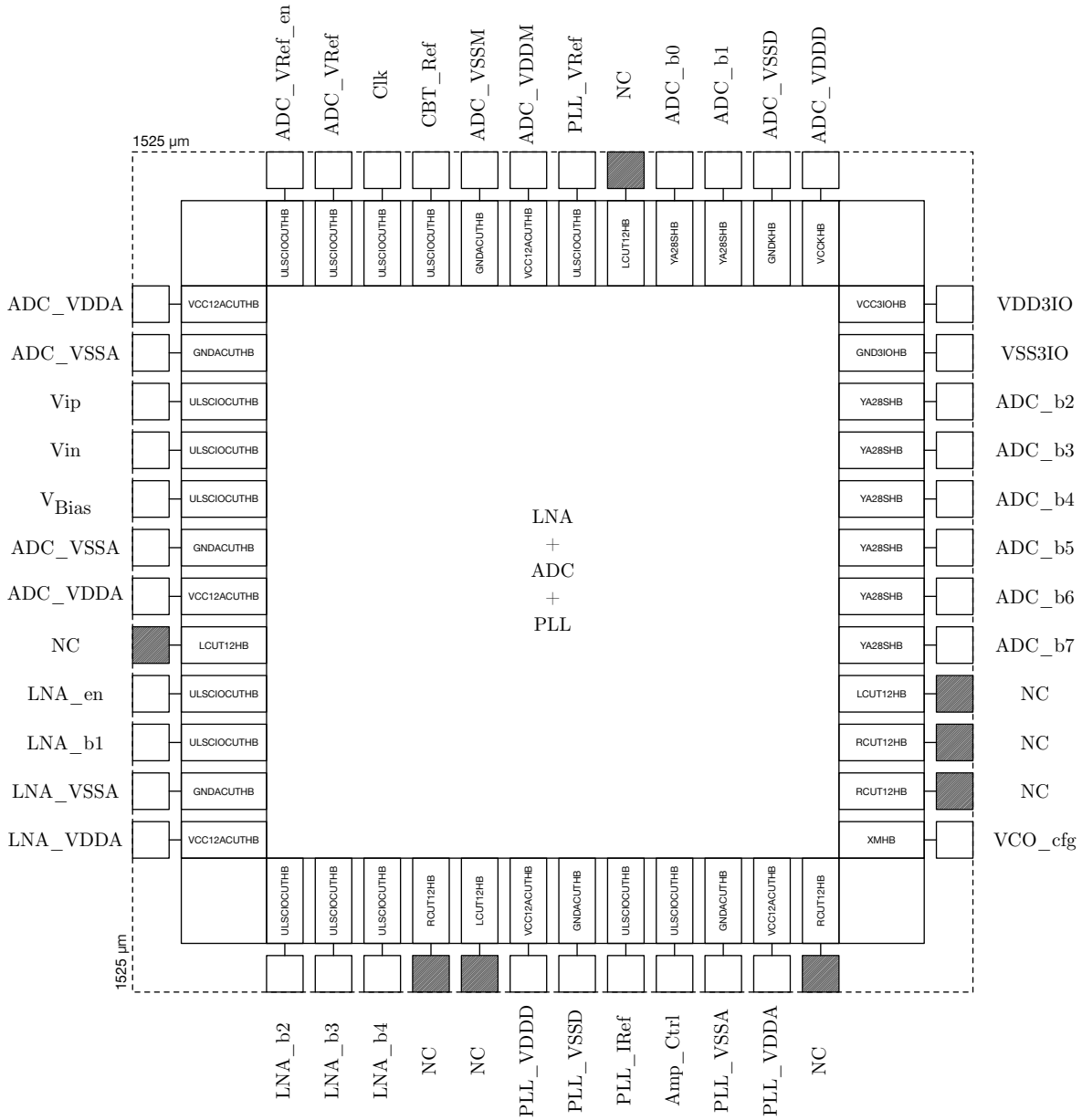


Figure 5.20: Pads distribution around the I/O ring. Bonding pads named 'NC' are not connected during wire bonding.

sides of the ring. Analog pads, more sensitive to noise, are distributed along the bottom and left sides of the ring. The description of each pad is given in Table 5.1.

Table 5.1: Description of the chip pads.

Pad name	**Description**
ADC_VDDA	1.2 V analog supply for the 8-bit CS-SAR ADC.
ADC_VSSA	Analog ground for the 8-bit CS-SAR ADC.
ADC_VDDM	1.2 V mixed-signal supply for the 8-bit CS-SAR ADC.
ADC_VSSM	Mixed-signal ground for the 8-bit CS-SAR ADC.
ADC_VDDD	1.2 V digital supply for the 8-bit CS-SAR ADC.
ADC_VSSD	Digital ground for the 8-bit CS-SAR ADC.
VDD3IO	3.3 V digital I/O supply.
VSS3IO	Digital I/O ground.
Vip/Vin	Positive/negative analog input.
Clk	Clock input.
ADC_b0 ... ADC_b7	Digital output bits, from LSB to MSB.
ADC_VRef	(Optional) external variable reference voltage.
ADC_VRef_en	Control pin that enables/disables the integer-N PLL.
CBT_Ref	External voltage used on the Voltage Boosters. Nominally 1 V.
V_Bias	External voltage used on the Comparator's self-timing feedback loop.
PLL_VDDA	1.2 V analog supply for the integer-N PLL.
PLL_VSSA	Analog ground for the integer-N PLL.
PLL_VDDD	1.2 V digital supply for the integer-N PLL.
PLL_VSSD	Digital ground for the integer-N PLL.
PLL_VRef	External (low frequency) reference signal.
PLL_IRef	Reference current for the integer-N PLL. Nominally 20 µA.
Amp_Ctrl	Amplitude control for the VCO of the integer-N PLL.
LNA_VDDA	1.2 V analog supply for the LNA.
LNA_VSSA	Analog ground for the LNA.
LNA_en	Control pin that enables/disables the LNA.
LNA_b1 ... LNA_b4	Biasing signals for the LNA.
NC	Not connected.

5.5 Post-layout simulation results

The circuit layout of both the ADC and PLL is shown in Fig. 5.21. The ADC core occupies an area of ~0.033 mm^2 (225 µm x 145 µm), while the PLL core occupies an area of ~0.039 mm^2 (138 µm x 282 µm).

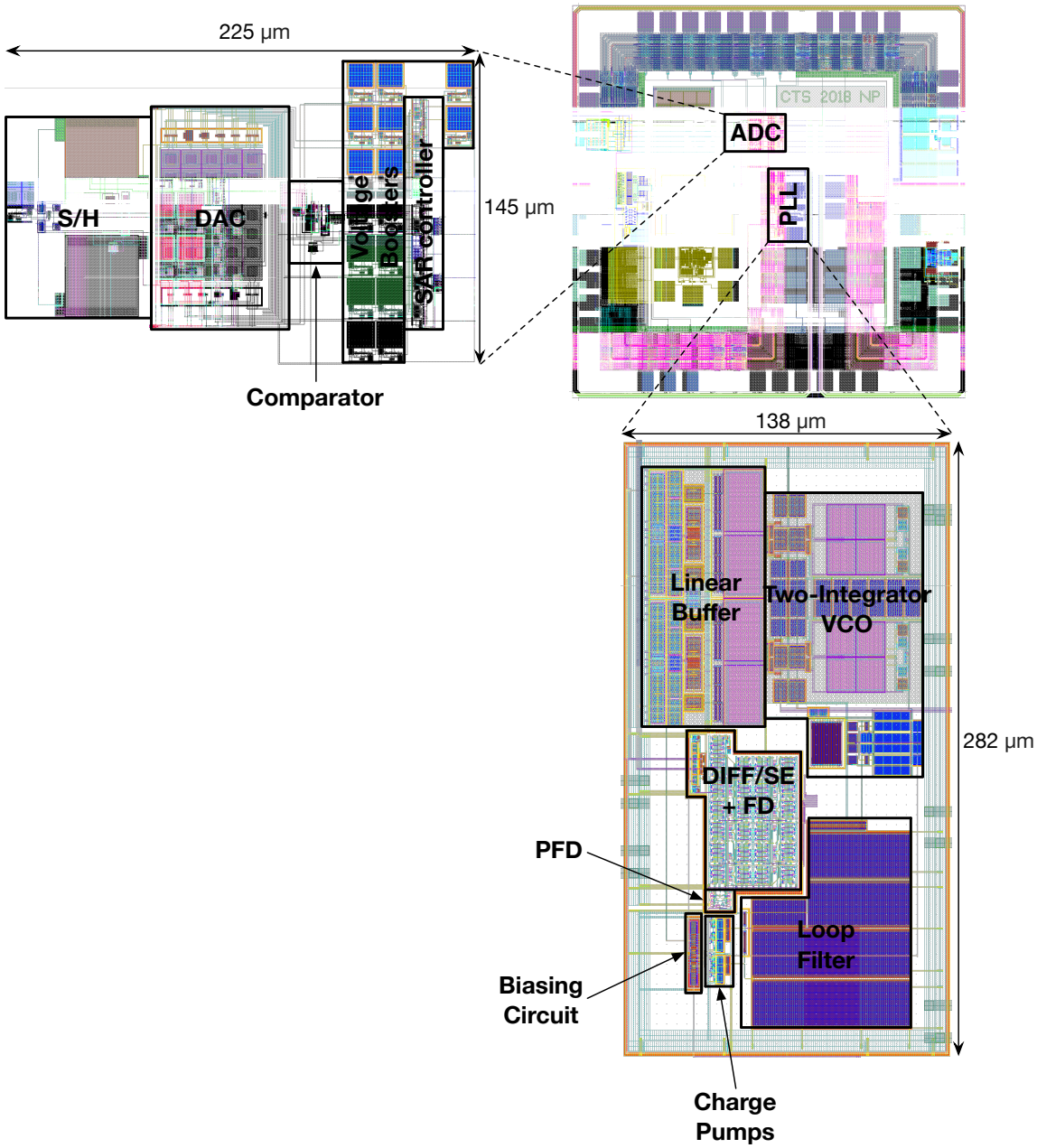


Figure 5.21: Layout of the 8-bit Charge-Sharing ADC.

A sinusoidal input near-Nyquist (~ 24 MHz) was used, under a carrier wave of 200 MHz, for 50 MS/s of sampling frequency. This results in a downsampling factor m of 8.

The varying reference voltage, generated by the PLL, had a common-mode of 700 mV (α) with an amplitude of 500 mV (β) and frequency of 150 MHz. The values for α and β are selected based on Fig. 4.3(a), ensuring that the input signal does not suffer any major attenuation. The FFT plot of the ADC is shown in Fig. 5.22.

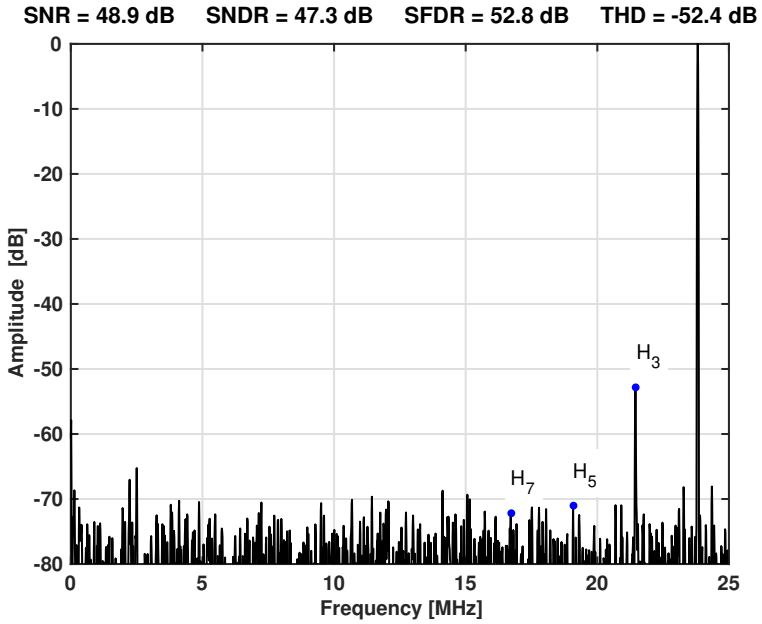


Figure 5.22: Simulated output spectrum, for a near-Nyquist frequency input signal (4096 points).

The achieved SFDR, THD, SNR and SNDR are 52.8 dB, -52.4 dB, 48.9 dB and 47.3 dB, respectively. Thus, the converter reaches around 7.6 bits of effective linearity. When a standard DC reference voltage is considered, for the same ADC and input signal, the ENOB drops to 7.2 bits.

In Fig. 5.23, the SNDR and SFDR are shown for different values of input frequency, all under a carrier wave of 200 MHz. It can be observed that the converter presents a minimum effective linearity close to 8 bits in the entire frequency input range.

The distribution of the power consumption of the overall converter is illustrated in Fig. 5.24. Under a 1.2V supply, a total power dissipation of 900 µW is estimated. As expected, the most power-hungry block is the comparator, as the DAC behaves in a passive fashion during the decision cycles, only burning power in the pre-charge cycle. It should be highlighted that roughly a quarter (~ 240.7 µW) of the power is consumed by the bootstrapping circuitry. Regardless, the advantage of forgoing an explicit mixing stage

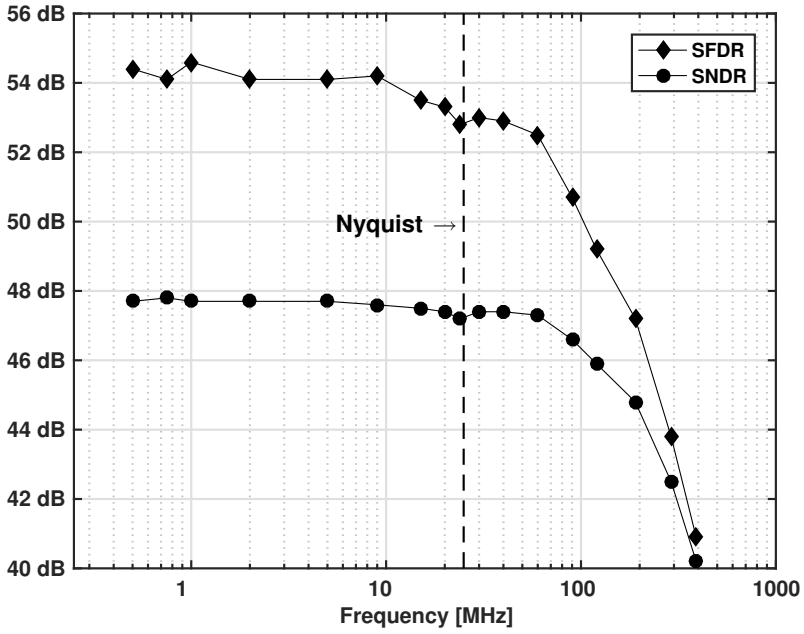


Figure 5.23: Simulated SNDR and SFDR as a function of the input frequency.

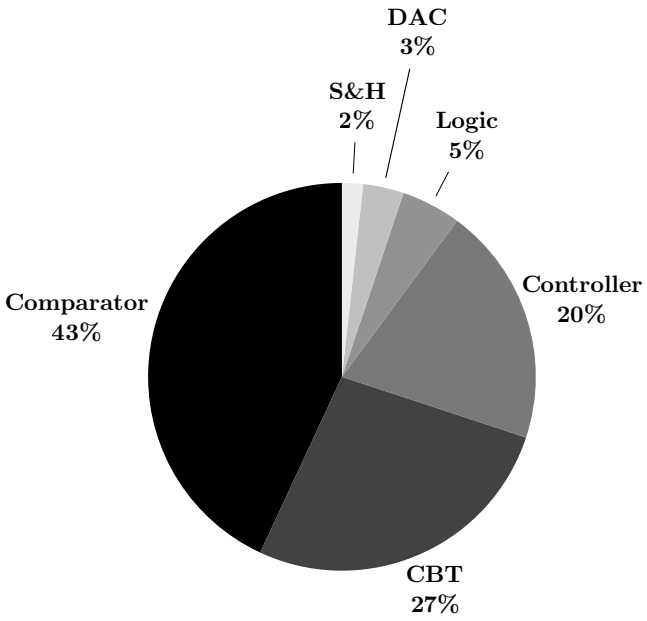


Figure 5.24: Power consumption distribution of the designed 8-bit CS-SAR ADC.

and the inherent power saving that comes with it, due to the proposed technique, should be kept in mind. Moreover neither a bandgap circuit nor reference buffers are required since the PLL provides the reference voltage.

Chapter 6

Conclusions

Modern radio receivers are increasingly shifting away from conventional structures such as superheterodyne and homodyne. In that sense, several alternatives have been developed in recent years, such as the mixer-first or the BP$\Sigma\Delta$M topologies. This thesis contributed to this topic by proposing a completely original technique, based on the usage of variable references applied to an ADC.

The work developed so far can be divided into two major objectives: Primarily, the validity of the proposed "embedded mixing" technique had to be verified, through mathematical methods. Also, being a new approach on how the reference signal is thought of, poses additional design considerations such as the requirements for the variable reference signal itself. Moreover, due to these particular set of demands behind the proposed technique, the ADC architecture most fitted for its implementation had to be selected. This was presented in Chapter 4, together with a design example considering *quasi-ideal* blocks, to demonstrate early circuit-level results.

The secondary objective revolved around the design, implementation and layout of an 8-bit fully-differential CS-SAR ADC together with a signal PLL (to provide an on-chip solution to the generation of the variable reference signal), disclosed in Chapter 5. Post-layout results prove the viability behind the "embedded mixing" technique,

although these would be further enforced with measurement results. The CS-SAR topology presents a set of characteristics that mesh quite well with the proposed technique, such as the "pre-charging" of the DAC array. Furthermore, in the context of radio applications, this topology (albeit not explored in this work) has the capability of extending the converter's input range and therefore better cope with large input swings (i.e., a high PAPR), a common trait in modern communication standards.

It should be stated that the developed work focused mainly on the proof-of-concept of the technique, with concerns such as offset cancellation in the comparator or a competitive FOM achievement not being a main priority.

During the early stages of the developed work, high-level models[1] for three receiver architectures were designed: Superheterodyne, SubSampling and the Embedded Mixing receiver (Fig. 4.1). Behavioural simulations run with these models considered both a single-tone input signal and one under a multi-carrier transmission scheme (OFDM). In the latter case, the BER performance was also contrasted between each receiver. Findings show that the proposed technique outperforms the other two. Unfortunately, during that stage, the Pipeline ADC was still seen as the ideal candidate for the "embedded mixing" technique, something that later was found to not be the case. This is due to the fact that the reference signal in a Pipeline ADC is based on the input sample and each stage of the converter is processing a different sample at the same point in time. Hence, these high-level models and the respective findings had to be partially discarded and not fully disclosed in the core of this document, notwithstanding their importance.

The proposed "embedded mixing" technique, as it is, might not look as competitive as other approaches in modern day radios. However, an interesting parallel can be drawn, regarding the SAR architecture itself. Although early reports date back to 1947 and CMOS designs appearing in the 1970s, the SAR topology stayed "in the shadows" of other architectures such as the Flash or Pipeline ADCs. Only during the beginning of the present century was their potential for low power consumption recognized [112]. As a matter of fact, it is not uncommon for innovative works in the field of data converters to be overlooked and fail to gain traction at the time of publication, as demonstrated in [113]. In that context, the usage of variable references has the potential to carve its

[1] For *MATLAB* [110] and *Simulink* [111]

own niche, due to some attractive features such as the capability of removing explicit mixers altogether from a receiver chain.

6.1 Suggestions for Future Work

During the study of the proposed technique and the development of the ADC, some interesting considerations for future work can be drawn:

- First and foremost, obtaining measurement results from the designed prototype should be the next logical step. Although this was initially one of the major goals behind this work, due to time constraints and other factors such was, ultimately, not possible;
- An interesting approach on the topic of variable references is to verify how the circuit performs if subjected to a different kind of variable reference signal, such as a square wave or a sawtooth wave;
- The main focus of this work was to prove that it is possible for an ADC to also act as a downconversion stage. Consequently, some design improvements such as the inclusion of some sort of comparator offset calibration or exploiting the capability behind the CS-SAR topology to operate with over-rail inputs, were put aside. However, future designs can have improved performance if such options are considered;
- The "embedded mixing" technique is conceptually applicable to every known flash-based converter, and this work focused on its implementation in the context of radio applications. However, it might prove its value in other application fields.

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Appendix 1 - Article submitted to IJCTA

This work explores the capability behind an ADC to incorporate not only the quantization operation but also the downconversion operation, usually assigned to mixing stages preceding or following the ADC itself in a receiver chain.

To do so, the authors resort to the charge-sharing scheme in SAR ADCs (instead of the most common charge-redistribution scheme) and take advantage of several particularities that fit well with the proposed "embedded downconversion" technique. Furthermore, to provide an on-chip solution for the generation of the variable reference voltage, the authors employ an integer-N PLL.

Designed in a 130-nm process, the 8-bit 50MS/s ADC uses an active area of 0.033 mm^2, while the PLL occupies an area of 0.0389 mm^2. Post-layout simulations (after running parasitics extraction) validate the approach, where an ENOB of 7.6 bits across the input frequency range is obtained.

This is a complete original research performed by the authors. In other words, outside previously published conference articles by them on this topic, there are no journal articles addressing this particular "embedded downconversion" method, to the best of their knowledge.

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RESEARCH ARTICLE

A Charge-Sharing Analog-to-Digital Converter with Embedded Downconversion using a Variable Reference Voltage

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Summary

In the field of radio receivers, down-conversion methods usually rely on one (or more) explicit mixing stage(s) before the analog-to-digital converter (ADC). These stages not only contribute to the overall power consumption but also have an impact on area and can compromise the converter's performance in terms of noise and linearity. As an alternative, we propose a receiver architecture that considers the ADC as both a quantizer and a down-converter block. This is achieved through the use of a variable reference signal (in this case, a voltage), as opposed to classic time-invariant reference signals. When embedded into a charge-sharing (CS) successive approximation register (SAR) ADC, this varying reference voltage is "saved" in the digital-to-analog converter (DAC) capacitor bank during the sampling phase, preventing any conversion errors. Furthermore, a phase-locked loop (PLL) is used in order to provide an on-chip solution for the generation of this variable reference voltage, which also removes the need for dedicated bandgap circuits and reference buffers. Post-layout simulations of an 8-bit 50 MS/s CS-SAR ADC show that the proposed "embedded mixing" technique is able to downconvert a high-frequency signal whilst also increasing the effective-resolution by around 0.5 bits, when compared to a standard DC reference voltage.

KEYWORDS:
analog-to-digital converters, charge-sharing, embedded down-conversion, SAR, receivers, variable references

1 | INTRODUCTION

Modern day battery-powered handheld devices are expected to support a wide variety of radio technologies. At the same time, high data rates with reduced latency must be guaranteed, while keeping in mind production costs. These specifications become even more challenging with the advent of 5G, scheduled to have 1.9 billion subscribers by the end of 2024, with over 10 million subscriptions projected worldwide until the end of the present year of 2019[1].

Early receivers used in these devices typically adopted one of two standard architectures namely, superheterodyne (illustrated in Fig. 1) and direct or low-IF downconversion. However, the research is now focused in SAW-less wideband receivers (with maximum hardware reuse in mind) capable of withstanding broadband noise and high-power blockers. Down-conversion is performed by one or more mixing stages (i.e., mixers) resulting in conversion losses (more noticeable when passive approaches are considered) and additional noise and distortion to the circuit.

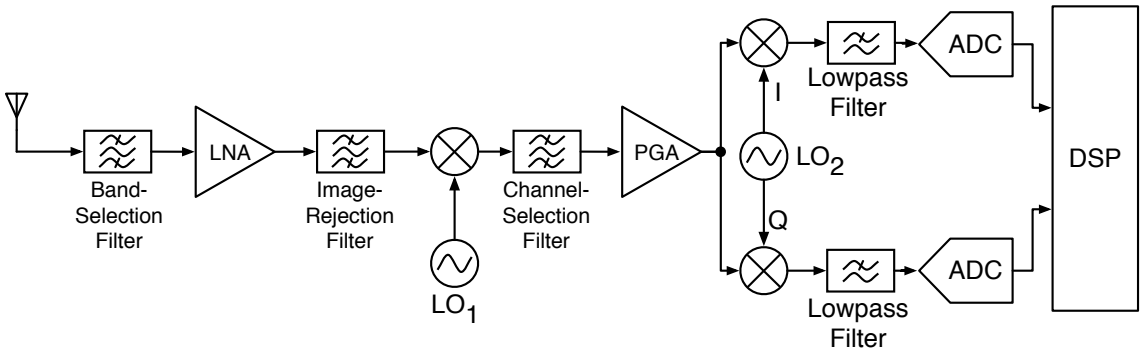

FIGURE 1 Superheterodyne Receiver.

The subsampling approach, also known as undersampling or bandpass sampling, can be used with the advantage of greatly relaxing the requirements for the analog-to-digital converter (ADC), particularly its sampling frequency f_s. However, the performance is degraded mainly due to two reasons: noise-folding and high sensitivity to the timing jitter associated with the sampling clock[2].

At the same time, in order to cope with the aforementioned transmission demands, communication standards usually resort to multi-carrier modulation schemes, such as Orthogonal Frequency-Division Multiplexing (OFDM), to support their physical layer[3]. These are known to present a significant Peak-to-Average Power Ratio (PAPR) which places stringent requirements on the circuits following the antenna, in particular the ADC, since these high input swings can easily drive it into saturation.

The architectures previously mentioned consider the ADC as a baseband (BB) device, since the design of high-resolution low-power data converters that operate at substantial higher frequencies (from hundreds of MHz to GHz) fast becomes an almost impossible task, given current technology and architecture limitations. As an alternative, due to its noise-shaping feature, Sigma-Delta Modulators ($\Sigma\Delta$M) designed to function as a bandpass (BP) filter rather than a lowpass can be used for IF-to-digital conversion. Drawbacks include limited dynamic range (with larger signals easily driving the modulator into instability) and excessive power consumption.

However, the ADC itself can perform, simultaneously, both quantization and downconversion operations. As conceptually proposed in[4] and electrically simulated with quasi-ideal blocks in[5], the use of variable reference signals (instead of the standard constant values) allows for the downconversion of the input signal to either IF or directly into DC. Being an analog divider (from a mathematical point of view) the ADC can, in fact, also behave as an analog multiplier, i.e., the core operation in a mixing stage.

In this paper, a hybrid and "explicit-mixers free" receiver architecture is proposed, in which the downconversion function is considered in a two-step mode of operation. Post-layout simulations show that by embedding the proposed solution into a slightly modified 8-bit charge-sharing (CS) successive approximation register (SAR) ADC, a signal-to-noise ratio (SNR) of 48.9 dB, a signal-to-noise-and-distortion ratio (SNDR) of 47.3 dB, a total-harmonic-distortion (THD) of -52.4 dB and a Spurious-Free Dynamic Range (SFDR) of 52.8 dB are achievable, resulting in a receiver architecture that forgoes conventional mixer blocks and, therefore, with simplified hardware requirements.

The remainder of this paper is organized as follows. Section 2 provides a brief overview of possible solutions in the field of IF-to-digital conversion. Next, section 3 details the mathematical background behind the proposed "embedded downconversion" technique, together with design considerations. In section 4 the design of an 8-bit CS-SAR ADC is presented, together with the design of a dedicated signal phase-locked loop (PLL) to provide the variable reference voltage. The respective post-layout electrical simulations are shown in section 5, together with the layout of the complete circuit. Finally, section 6 draws the main conclusions of this work.

2 | THE CS-SAR ADC AS AN IF-TO-DIGITAL CONVERTER

Moving the ADC to the forefront of the receiver brings its fair share of design challenges, namely an (expected) higher sampling rate and increased sensitivity to blockers and interferers. Nevertheless the attractiveness of reducing (or even removing) the

mixing stages, coupled with the potential for reconfigurability of the converter's tuning range, makes alternatives such as BP-ΣΔM quite interesting. Other possible candidate is the proposed usage of variable references, conceptually applicable in every known flash-based ADC architectures, but best suited for a CS implementation of a SAR ADC.

2.1 | BP-ΣΔM approach

BP-ΣΔM are usually the architecture of choice when it comes to IF-to-digital conversion. By pushing the quantization noise up and down in frequency, an (ideally) "noise-free" region can then accommodate the received signal and the impact of DC non-idealities, such as flicker noise, becomes negligible. Continuous-time implementations are preferred over discrete-time, presenting advantages in terms of power consumption and inherent anti-aliasing filtering, to name a few.

For a given N-th order bandpass solution, its performance is the same as its $\frac{N}{2}$-th order lowpass equivalent. This means that high-order (> 3) modulators are almost mandatory, indirectly impacting the receiver's dynamic range due to their potential for instability. This becomes a major downside in the context of communication standards that present high peak values, as is the case with OFDM. Furthermore, the design of modulators with fixed notch frequencies demands that the RF receiver uses a widely programmable frequency synthesizer. As an alternative, reconfigurable BP-ΣΔMs with tunable notch frequency have been pursued in recent years[6,7,8], with some resorting to LC-based loop filters who have a direct impact on the silicon area and may be subjected to poor quality factor of on-chip inductors.

2.2 | CS-SAR approach

The market for moderate resolution (8 to 12 bits) and speed (1 to 100 MS/s) data converters under a low power operation is mostly dominated by SAR ADCs. Their switching-intensive mode of operation coupled with the absence of amplifiers matches very well with the trend of faster transistors with lower intrinsic gain, resulting in high energy efficiency.

Within the SAR ADC, most digital-to-analog converters (DAC) employ a charge-redistribution (CR) switching scheme[9], where the total capacitance is kept unchanged throughout the conversion and the sample-and-hold (S/H) functionality can be merged into the array[1]. In the CS switching scheme[10], however, the capacitive array is pre-charged to a voltage beforehand, in a single clock cycle. Afterwards, each capacitor in the array is connected in parallel or anti-parallel fashion to the DAC nodes (in accordance to the decision made by the comparator in each cycle) effectively adding or subtracting charge, respectively. This means that the total capacitance of the DAC increases progressively during the conversion. As a consequence of the scheme itself, explicitly dedicated S/H capacitors are needed. The switching schemes for both CR and CS-SAR architectures are illustrated in Fig. 2.

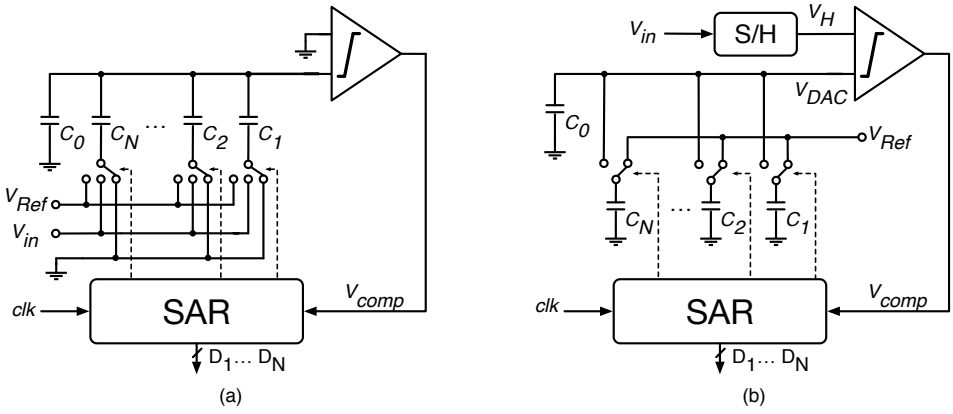

FIGURE 2 Operation modes of a charge-based SAR ADC (single-ended implementation): (a) Charge Redistribution (b) Charge Sharing.

[1]This capacitive array is usually arranged in a binary weighted fashion, although non-radix-2 architectures can also be used to ease the matching requirements, at the expense of larger digital circuit complexity.

The addition of S/H capacitors, in itself, is not a major drawback since the most significant bit (MSB) can be directly evaluated, with the input signal sampled onto these capacitors. Also, in fully differential implementations a single capacitor bank is required, as opposed to the CR-SAR, resulting in a DAC with a rather small area. However, the DACs time-varying behaviour poses two significant design challenges in terms of noise sensitivity and comparator offset, with the latter leading to the ADC presenting a nonlinear behaviour.

A distinctive feature of the CS scheme is that its input range isn't confined to the reference voltage range (as opposed to its CR counterpart), as the conversion gain is defined by ratios of charge instead of voltages. Consequently, with proper sizing of the S/H capacitors in relation to the unit capacitor C_u, the ADC can then operate with over-rail input signals. This is shown in[11], whereby a configurable S/H with 3 binary weighted input capacitances extends the converter's input range to 1.7 V_{pp}, despite a voltage supply of 0.6 V. As a result, the CS-SAR ADC can better accommodate the wide swings, i.e. PAPR, of modern communication standards, and avoid a significant drop-off in SNR.

The entire energy consumption of the reference source takes place only during the pre-charge cycle, when each capacitor is charged to V_{Ref}. This is due to the fact that in the following decision cycles each capacitor is simply connected to the DAC nodes via switches, taking on a complete passive behaviour. In other words, the reference buffer just has to be active during a fraction of the conversion's full cycle. This particularity can be expanded, either by employing duty-cycling or relaxing the reference buffer, to save power. Also, the "pre-charge" feature of the CS-SAR ADC is, in itself, quite useful for implementing the IF-to-digital downconversion based on reference voltages. The proposed new approach is detailed in the following section.

3 | EMBEDDED DOWNCONVERSION ARCHITECTURE

The usage of a variable reference is a significant shift from the traditional method. Consequently, the mathematical viability of this downconversion technique is first discussed, followed by some considerations regarding the design challenges it presents.

3.1 | Mathematical Background

In the interest of moving the ADC closer to the antenna, we take advantage of the fact that it is in itself, mathematically, an analog voltage divider that performs the division of the analog input signal $X_{in}(t)$ by a constant reference voltage $V_{Ref}(t)$ (or current[2]), as shown in (1). The result of this division is then quantized into discrete amplitudes. Here, $X_{in}(t)$ is assumed to be well-behaved, i.e., it presents no singularities and is well defined, as most communication analog signals are.

$$D_{out}(n) = \frac{X_{in}(t)}{V_{Ref}(t)} \tag{1}$$

Regardless, any system that is capable of performing the division operation is naturally capable of doing the multiplication operation (as it can be understood as a division by the inverse of the factor we want to multiply), thus performing the primary operation of any frequency translation (mixing) stage.

In ADCs, the reference voltage is typically provided from a stable low-noise bandgap-type voltage-reference circuit. However, since there is no known binding rule that states that this reference voltage must be entirely constant, it is possible to split it in two signals: a constant voltage (still generated by a bandgap reference circuit), added to a signal term provided by a local oscillator (LO) (varying over time). Thus, this 'normalized' reference voltage can be written as (2):

$$V_{Ref}(t) = \alpha + \beta \cdot \cos(2\pi f t + \varphi) \tag{2}$$

where α is the constant (DC) voltage provided by a bandgap reference circuit (or equivalent) and β, f and φ are the amplitude, frequency and phase of the signal generated by the LO[3]. Note that $V_{Ref}(t)$ reaches its maximum value when $\cos(2\pi f t + \varphi) = 1$. In that circumstance, $V_{Ref}(t) = \alpha + \beta$. With current designs in standard CMOS processes (e.g. 130-nm, 65-nm) typically holding 1.2 V of power supply (V_{DD}), this value is considered for V_{Ref}. Nevertheless, this technique can be extended to different values of V_{Ref}.

[2]In this paper, for the sake of simplicity, it is considered that the reference is a voltage. In "current-mode" realizations of ADCs the reference is a current rather than a voltage.

[3]Notice that in typical switched-capacitor (SC) implementations of "voltage-mode" ADCs, the $V_{ref}(t)$ voltage is normally sampled-and-held by a SC branch. This is valid for all A/D architectures employing DACs in the conversion algorithm.

Replacing (2) in (1) and working the expression leads to (3):

$$D_{out}(n) = \frac{X_{in}(t)}{\alpha + \beta \cdot \cos(2\pi f t + \varphi)} = \frac{X_{in}(t)}{\alpha} \cdot \left(\frac{1}{1 + \frac{\beta}{\alpha} \cdot \cos(2\pi f t + \varphi)} \right) \tag{3}$$

If the term $\frac{\beta}{\alpha} \cdot \cos(2\pi f t + \varphi)$ is assumed to be the variable x, the second term of (3) resembles the function $\frac{1}{(1+x)}$. Its MacLaurin series[4] is known and is given by (4):

$$\frac{1}{1+x} = 1 - x + x^2 - x^3 + x^4 - x^5 + ... = \sum_{n=0}^{\infty} (-1)^n \cdot x^n, |x| < 1 \tag{4}$$

Applying this line of thought to (3) leads to (5):

$$D_{out}(t) = \frac{X_{in}(t)}{\alpha} \cdot \left(\frac{1}{1 + \frac{\beta}{\alpha} \cdot \cos(2\pi f t + \varphi)} \right) = \frac{X_{in}(t)}{\alpha} - \boldsymbol{X_{in}(t) \cdot \frac{\beta}{\alpha^2} \cdot \cos(2\pi f t + \varphi)} + \frac{X_{in}(t)}{\alpha} \cdot \left(\frac{\beta}{\alpha} \cdot \cos(2\pi f t + \varphi) \right)^2 + \\ - \frac{X_{in}(t)}{\alpha} \cdot \left(\frac{\beta}{\alpha} \cdot \cos(2\pi f t + \varphi) \right)^3 + \frac{X_{in}(t)}{\alpha} \cdot \left(\frac{\beta}{\alpha} \cdot \cos(2\pi f t + \varphi) \right)^4 + ... \quad , |\beta| < |\alpha| \tag{5}$$

From (5), it is shown that the crossed products originated by the series expansion, give rise to terms composed by the input signal multiplied by the signal term provided by the LO. The term in bold in (5), $X_{in}(t) \cdot \frac{\beta}{\alpha^2} \cdot \cos(2\pi f t + \varphi)$, gives the desired down-converted signal. Therefore, this proves that it is possible for the ADC to frequency translate an incoming signal, thus embedding the mixing function.

A simplified block diagram of the proposed architecture is shown in Fig. 3, where α is the constant reference voltage provided by a bandgap circuit and the ADC acts as both a quantizer and a down-conversion stage. Naturally, this technique presents a set of challenges, which are addressed below.

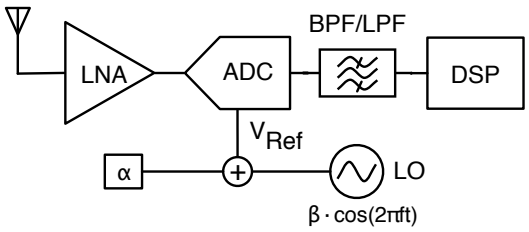

FIGURE 3 Embedded mixing receiver architecture.

3.2 | Design Considerations

3.2.1 | Impact of factor β/α^2 and subsequent terms in Eq. (5)

The input signal might suffer an attenuation as it is multiplied by the β/α^2 term, as shown in (5). This happens as long as $\beta < \alpha^2$. However, knowing that $\beta + \alpha = 1.2$ at peak value, i.e. $\cos(2\pi f t + \varphi) = 1$ and if one considers that $\beta = \alpha^2$, it can easily be demonstrated that for $\beta \simeq 500$ mV the input signal will not suffer such attenuation. Under these circumstances the condition of $\beta < \alpha$ still holds true (since $\alpha \simeq 700$ mV) and the dynamic range of the ADC is not wasted. These values can be fine tuned if external references are used.

Furthermore, with the embedded mixing technique it is possible to slightly relax the gain requirements (or accommodate for the gain error) of previous stages, such as the low-noise amplifier (LNA) or the S/H. For instance, if the values of α and β are properly adjusted (630 and 570 mV, respectively, as an example), the input signal can be (theoretically) amplified by about 3

[4] In mathematics, a MacLaurin series consists on a representation of a certain function as an infinite sum of terms calculated from the values of the function's derivatives centered at 0 (which is a special case of the Taylor Series) as follows:
$f(x) = f(0) + f'(0) \cdot x + \frac{f''(0)}{2!} \cdot x^2 + \frac{f^{(3)}(0)}{3!} \cdot x^3 + ... + \frac{f^{(n)}(0)}{n!} \cdot x^n + ...$

dB. This is a significant advantage over passive mixers, where conversion losses have to be accounted for. Also, in regards to active mixers, significant advantages are estimated in terms of cost, power consumption and area. Fig. 4(a) shows how this factor varies for a given α. It should be noted that values below 0.6 are not plotted, as that would render Eq. (5) false, i.e., β would have a larger value than α.

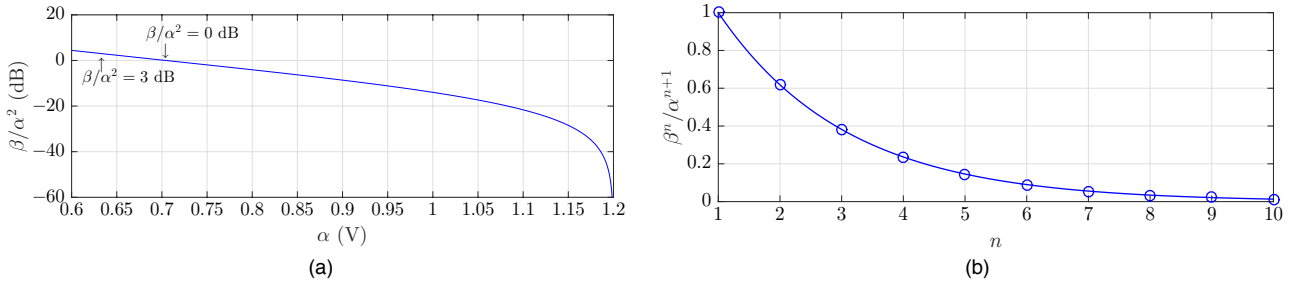

FIGURE 4 Impact of factor β^n/α^{n+1}: (a) Signal amplification for a specific α (b) Attenuation of unwanted terms, for $\beta/\alpha^2 = 1$.

As with mixer-like nonlinear components, unwanted harmonics and intermodulation products are generated. These also need to be filtered at the output. For these terms, the factor β^n/α^{n+1} is negligible as its value gradually becomes less significant and rapidly decays to zero (as shown in Fig. 4(b)), i.e., harmonics have their power attenuated in relation to the input signal's power.

3.2.2 | LO specifications

Most state-of-the-art precise oscillators provide an output signal with a maximum amplitude ranging from -10 dBm to +10 dBm. Thus, for state-of-the-art designs, the values required for β are perfectly achievable by modern-day oscillators.

However, if the design requires a low amplitude for the LO (i.e., < 0 dBm), this would result in an attenuation of the input signal, as mentioned above. A way to circumvent this issue would be to slightly increase the voltage gain of the preceding LNA in a logarithmically proportional fashion, through (6).

$$\text{LNA}_{\text{VG increase}}\ (\text{dB}) = \left| 20 \cdot \log_{10} \frac{\beta}{\alpha^2} \right| \tag{6}$$

Eq. (6) rapidly grows with α^2 and it fast becomes unacceptable to push the LNA gain above 20 dB due to several reasons, such as power and distortion increase. Thus, one may choose to distribute the required gain between the LNA and the S/H. This relaxes the requirements for the LNA while the design of a S/H with 6 dB gain is fairly easy to accomplish in a SC implementation.

Nonetheless, the requirements for the LO that generates the variable reference voltage aren't any more stringent than those of the common LOs used in a typical mixing stage. This means that the phase noise (PN) of this LO can present a similar value to those of state-of-the-art LOs and amplitude noise, albeit existent, is of minor concern as shown in [12].

3.2.3 | Synchronism between Input and Reference

When employing the proposed technique, a common issue arises. Since V_{Ref} is varying over time, its value at each sampling instant will vary, which would undoubtedly lead to conversion errors. Furthermore, a slight phase shift would also result in different values for V_{Ref}. Both these issues are illustrated in Fig. 5.

In order to guarantee that the V_{Ref} value considered at each sampling instant is the same, but that the proposed technique still applies, there are two, non mutually exclusive, possible solutions.

First, the LO frequency used should be a multiple of the f_s of the ADC. In that case, by matching the sampling instant with the instant where V_{Ref} has its peak value, a constant V_{Ref} would be ensured for every conversion and no errors would occur. This could be achieved by a PLL, where the V_{Ref} signal would be synchronized to the incoming signal.

Secondly, if the reference voltage is charged beforehand onto a set of capacitors, its value is kept throughout the conversion. This is the case with the CS-SAR scheme, as detailed in section 2.2, where the DAC capacitor bank is "pre-charged" with a given reference voltage. When sizing these capacitors, the conversion rate of the ADC must be taken into account, in order to ensure complete settling.

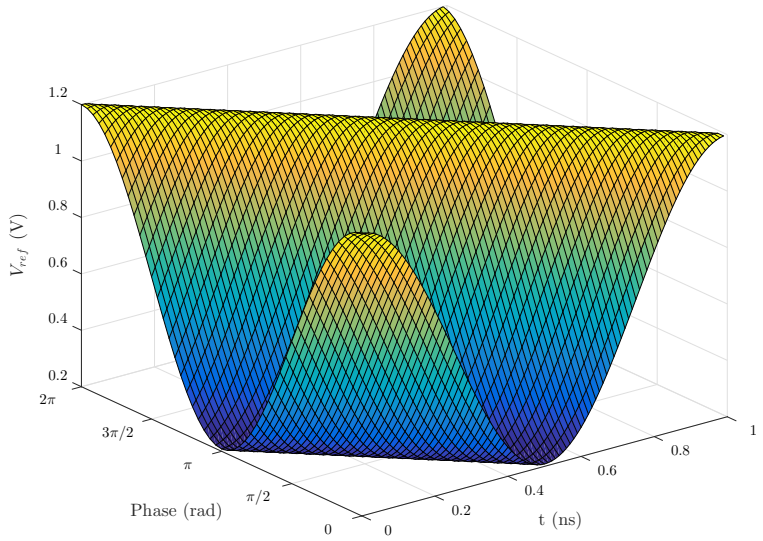

FIGURE 5 Mesh plot of $V_{Ref}(t)$ variation over time and phase, for $\beta/\alpha^2 = 1$.

3.2.4 | Quantizer's Dynamic Range

Several popular wireless communications standards (e.g., DVB-T[13], 3GPP LTE[14] and WiMAX[15]) employ multi-carrier transmission schemes[5], such as OFDM, to support their physical layer. Their PAPR can be up to N times the average power (where N is the number of carriers).

This translates into severe amplification difficulties and strong nonlinear distortion effects at the transmitter output and also requires for the ADC in the receiver chain to have a higher dynamic range in order to cope with the requirements of having a small probability of clipping events, at the expense of the degradation of the SNR. Otherwise, if the PAPR is reduced it is possible for a system to either transmit more bits per second, transmit the same bits per second but with lower power consumption or both. Recently, several PAPR reduction techniques have been proposed for OFDM[16,17,18].

Again, the CS-SAR scheme presents itself as an attractive solution in this regard, being able to operate with over-rail input signals and fitting quite well with the proposed method, as described in 2.2.

3.3 | "Two-step" downconversion method

An inherent limitation of the Embedded Mixing architecture is that the down-conversion only occurs at the quantization phase, meaning that the signal at the sample phase is not yet down-converted. For certain standards, like GSM or WiFi, this would imply a high sampling rate for the ADC or the preceding S/H circuit (of at least 2 GHz), in order to avoid aliasing, which is unfeasible due to current technology limitations.

Baring this in mind, if the f_s is below the signal's Nyquist rate but at least twice its bandwidth (BW), it is still possible to down-convert the signal, as the subsampling approach shows. The main downsides here reside on the noise-folding and timing jitter sensitivity, both escalating with the subsampling ratio m used. In other words, the higher m is (i.e., a subsequent lower f_s), more out-of-band noise is aliased into the baseband, increasing its density at the output by a factor of $2m$ (illustrated in Fig. 6), while the clock phase noise power is "amplified" by a factor of m^2. Furthermore, the f_s used in this approach is limited to a certain range of values, thus imposing certain design constraints.

Instead, one can look at the down-conversion process as a two-step procedure, where the signal is initially shifted to an intermediate frequency (IF) by the S/H (during the sampling phase) and then placed on baseband by the ADC (during the quantization phase) through the use of variable references, as proposed here. The S/H can also optionally be replaced by a simple SC finite impulse response (FIR) filter responsible for tuning out blockers and other interferers. This approach is slightly different from what has been proposed in[19,20], where two separate subsampling stages are considered.

[5] Multi-carrier schemes are known to be very robust against severe time dispersion effects of multipath propagation without requiring complex receiver implementation. In particular, OFDM's advantages rely on high spectral efficiency, its facility to cope with frequency-selective channels without the need for complex equalization processes and its simplicity of implementation.

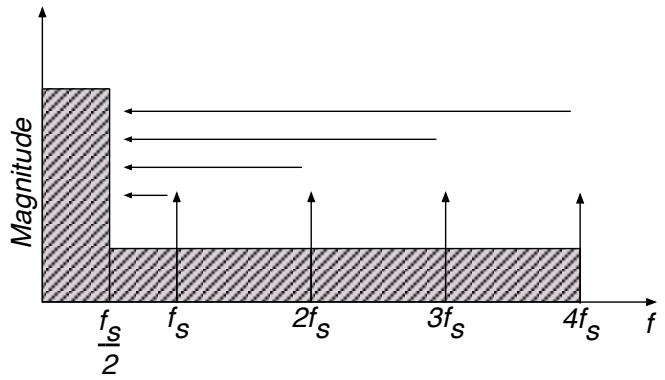

FIGURE 6 Illustration of the noise-folding effect, common in Subsampling approaches.

The advantages behind this would be that a small m (i.e., a higher f_s on the S/H) can be used, reducing the number of times the out-of-band noise is "folded" back and keeping the sensitivity to the timing jitter as low as possible, and no more critical than that of common Subsampling receiver schemes. Also, this lifts the f_s restrictions on the S/H, imposed by the subsampling approach (since the signal is not directly down-converted to baseband), as long as it satisfies the Nyquist criterion.

This technique can be seen as particularly suited for moderate-to-high frequency communication standards (from high MHz to some GHz), as despite the noise-folding effect, the noise will be spread over a wider band lowering its impact on the overall SNR. Also, for these standards, the oscillator that generates the variable component of the reference can be made very precise. With this approach it's possible to completely remove explicit mixing stages from the system, leading to significant power and area savings. Moreover, from the RF front-end perspective it follows that both the overall Noise Figure (NF) and linearity (mainly the IP_3) will be defined by the preceding LNA. This is contrasted with most receiver chains, where although the LNA, following the Friis' formula, dominates the overall contribution to the NF, the latter stages contribution to the overall IP_3 are more significant over the first ones.

4 | 8-BIT CS-SAR ADC

To validate the proposed method, an 8-bit fully-differential CS-SAR ADC with a sampling rate of 50 MS/s was designed in a 130-nm CMOS process. The architecture is depicted in Fig. 7. It's comprised by a S/H, a binary-weighted capacitive DAC, the SAR logic and a comparator. In order to generate an on-chip variable reference voltage, an integer-N PLL was also designed, but the design is flexible enough to accommodate for external references by means of an input-multiplexer circuit.

The operation principle of the proposed ADC is as follows: Initially, a conversion is requested when the "clk" signal is switched to logic "1", with the S/H tracking the input signal while the DAC capacitor bank is pre-charged to the reference voltage V_{Ref}. Once "clk" is pulled down, nodes $V_{cp,cn}$ hold the voltage on the sampling capacitors. The capacitor bank is, at this moment, charged with the reference voltage. Next, the MSB is directly evaluated, with the comparator being triggered by the controller and instructing the SAR to add or subtract charge from the $V_{cp,cn}$ nodes, by connecting the first capacitor in the bank in a parallel or anti-parallel fashion. This process is repeated for the subsequent bits, each being stored in the controller and, once finished, the 'end-of-conversion' is flagged at the "$\overline{EOC}$" output.

4.1 | Sample-and-Hold

The input passive S/H circuit comprises a simple set of NMOS switches, bootstrapped to ensure proper operation and linearity throughout the entire input range, together with dummies to reduce charge injection. The capacitors have a total capacitance value of about 1.1 pF. The bootstrapping circuit[21] is used on both the S/H and DAC "$\overline{clk}$" switches, as well as the switches that connect a given capacitor to the $V_{cp,cn}$ nodes. When simulated at a near-Nyquist frequency (~ 24 MHz), the S/H alone presents a SNDR of around 64 dB, compatible with 10 effective bits of linearity, guaranteeing a safety linearity margin for the 8b CS-SAR ADC.

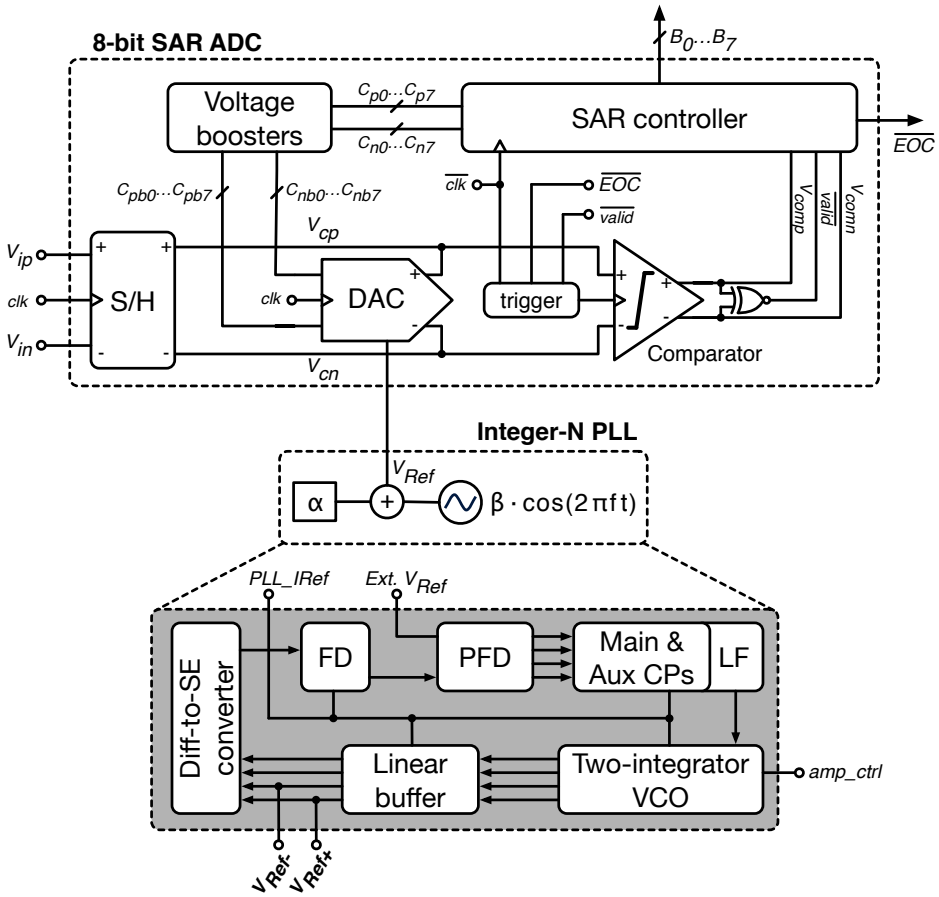

FIGURE 7 Proposed 8-bit CS-SAR ADC & integer-N PLL topology diagram.

4.2 | Binary-weighted capacitive DAC

In conventional binary-weighted arrays, an N-bit ADC would require a DAC with the size of $2^N \cdot C_u$, with C_u representing the unit capacitor. To reduce the overall DAC area, we employ a charge-partitioning scheme similar to the one used in [10] (illustrated in Fig. 8), where the 3 least significant bit (LSB) capacitors (and an auxiliary capacitor) have a size of $C_u \approx 20$ fF (the minimum allowed by the technology for MOMCAPs), and thus the total size of the capacitor bank is of 578 fF. The DAC switches that add or subtract charge to the $V_{cp,n}$ nodes stay connected until the end of the conversion. Consequently, dummy switches are only used for the pre-charge switches. All of these switches are just NMOS transistors, as opposed to transmission gates, avoiding the need for the generation of complementary signals (since these don't come for free in the CS-SAR topology) and reducing complexity.

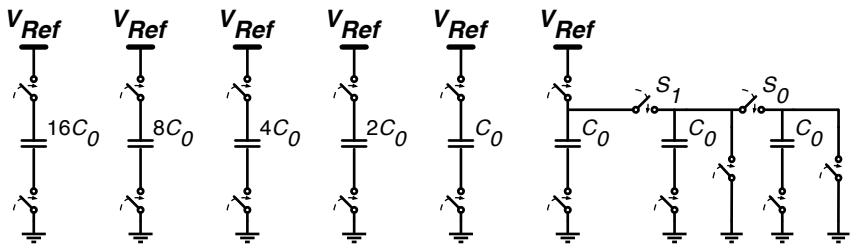

FIGURE 8 Employed multi-step pre-charge scheme in the capacitive array. The charge in the LSB capacitor is shared with two other equally sized auxiliary capacitors.

4.3 | Comparator

The dynamic comparator[22] widely known in literature as the StrongARM, was used, as shown in Fig. 9. This architecture relies on a positive feedback loop to improve speed and provide rail-to-rail outputs. The use of back-to-back inverters yields zero static power consumption. All transistors have minimum length (0.12 µm), with the input pair having a width of 30.4 µm. The input pair is critical, as it defines both the voltage gain and the input-referred noise. The comparator presents a (simulated) input-referred noise of 0.15 mV, which is below the estimated quantization noise of ~1.35 mV ($\frac{V_{LSB}}{\sqrt{12}}$) and limits the maximum achievable ENOB to around 7.9 bits. The comparison is guaranteed to occur in less than 0.2 ns and is triggered (through a 3-input AND-gate) each time that all the following signals have their logic level set to 'high': $\overline{clk}$, $\overline{EOC}$ and $\overline{valid}$. The latter indicates if both comparator's outputs are equal (in reset state) or not (a comparison as successfully been performed), through an XNOR gate.

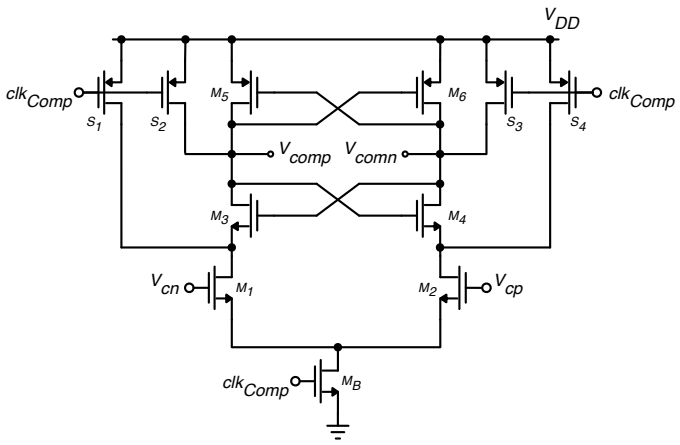

FIGURE 9 StrongARM latch topology used.

4.4 | SAR controller

In order to improve power and area efficiency, a self-timed controller is used[11]. Based on a TSPC latch, it requires a single clock signal, it being the sampling clock ("clk"). The binary search circuit has 8 instances, each resolving one bit. Using a full-custom design, as opposed to a standard cells implementation, is significantly more energy efficient.

4.5 | Integer-N PLL

A topology based on an integer-N charge pump PLL[23] is used to generate high frequency, low distortion and low jitter amplitude controlled IQ sinusoidal signals. These signals are generated based on an external low frequency reference clock (*Ext.* V_{Ref}), provided by common crystal oscillators. The intent of this PLL is to provide an on-chip solution for the generation of the variable reference signal.

The block diagram of the PLL is detailed in Fig. 7, with a brief description of each block given next:

- A sequential three-state Phase and Frequency Detector (PFD), based on a dual D-type flip-flop structure, with reduced perturbation of the loop filter voltage, leading to improved jitter performance of the PLL;
- A conventional third-order passive loop filter (LF) is used in conjunction with a main and auxiliary charge pumps. These charge pumps follow a capacitance multiplication scheme, proposed in [24], that aims to alleviate the total capacitance of the integrated loop filter, reducing its area overhead by a factor of roughly $\sim 20\%$ in this particular design. This loop filter uses a third-order transfer function to better attenuate the effects of charge pump imbalance;
- A two-integrator voltage-controlled oscillator (VCO), illustrated in Fig. 10, to generate low distortion quadrature sinusoidal signals ($V_{oi,oq}$), composed by a couple of differential pairs and a pair of capacitors. This VCO is responsible for

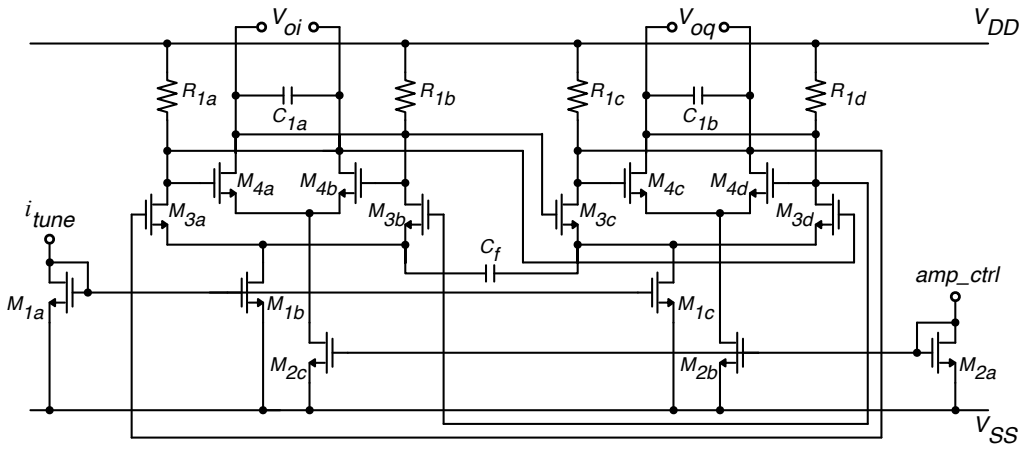

FIGURE 10 Schematic of the two-integrator oscillator, adapted from[23].

implementing the $\beta \cdot \cos(2\pi f t + \varphi)$ part of V_{Ref} in Eq. (2). Two additional differential pairs, with their outputs cross-coupled to the inputs, implement negative resistances to compensate the losses due to the biasing resistors and also provide amplitude control of the output signals. This, in turn, allows the oscillator to operate in the linear regime;

- A modified super source follower[25] is used to output the variable reference voltage generated by the VCO with the desired output common-mode voltage, without penalty in regards to the output voltage swing. Therefore, this buffer is responsible for implementing the α part of V_{Ref} in Eq. (2);
- A programmable frequency divider (FD), based on a modular structure consisting of a chain of 2/3 divider cells connected like a ripple counter. Each cell is built using four D-type flip-flops and three AND gates.

The (differential) sine wave(s) at the output of the PLL can reach a frequency of approximately 500 MHz, enough to accommodate input signals under carrier waves tenfold that of the sampling frequency of the designed ADC, and is given by:

$$f_{\text{osc}} = \frac{g_{\text{m3}}}{2\pi C_1} \tag{7}$$

where $C_1 = C_{1a} = C_{1b}$ and g_{m3} can be adjusted by means of the independent reference current i_{tune}. Filtering capacitor C_f reduces the distortion of the generated signals. The amplitude of the output sine wave signals (i.e., the value of β) can be adjusted by an external signal, *amp_ctrl*.

5 | SIMULATION RESULTS & LAYOUT

Fig. 11 shows the ADC layout and the allocation of the blocks. Both the DAC capacitor bank and the input pair of the latch comparator were laid out in a *common-centroid* configuration in order to minimize mismatch effects. Designed in a 130-nm process, the ADC uses an active area of 0.033 mm^2 (225 µm x 145 µm), while the Integer-N PLL occupies an area of 0.0389 mm^2 (138 µm x 282 µm). The DAC array occupies an area of 50 µm x 63 µm, roughly 10% of the ADC's total area.

With 1.2 V of supply voltage, a coherently sampled sinusoidal input near-Nyquist (~ 24 MHz) was used, under a carrier wave of 200 MHz, for 50 MS/s of sampling frequency. This results in a downsampling factor m of 8. The varying reference voltage, generated by the integer-N PLL, had a common-mode of 700 mV (α) with an amplitude of 500 mV (β)[6] and a frequency of 150 MHz.

The output spectrum is shown in Fig. 12. The post-layout simulated ENOB is 7.6 bits, while SNR, SNDR, SFDR, and THD are 48.9 dB, 47.3 dB, 52.8 dB and -52.4 dB, respectively. When a standard DC reference voltage is considered, for the same ADC and input signal, the ENOB drops to 7.1 bits. In Fig. 13, the SNDR and SFDR are shown for different values of input frequency, all under a carrier wave of 200 MHz.

[6]These values are selected in accordance with Fig. 4(a) in order for the input signal to not suffer any major attenuation.

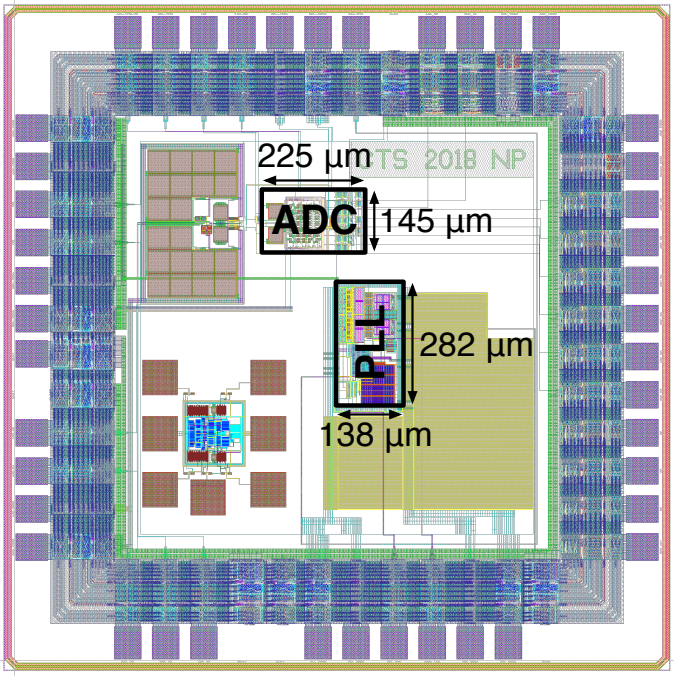

FIGURE 11 Layout of the proposed 8-bit CS-SAR ADC and Integer-N PLL, in a 130-nm CMOS process.

Performing a power consumption estimation from the post-layout simulations shows that the most power-hungry block is the comparator, as expected, since the DAC behaves in a passive fashion during the decision cycles, only burning power in the pre-charge cycle. It also highlights that roughly a quarter of the power is consumed by the bootstrapping circuitry. Regardless, the advantage of forgoing an explicit mixing stage and the inherent power saving that comes with it, due to the proposed technique, should be kept in mind. Moreover neither a bandgap circuit nor reference buffers are required since the PLL provides the reference voltage.

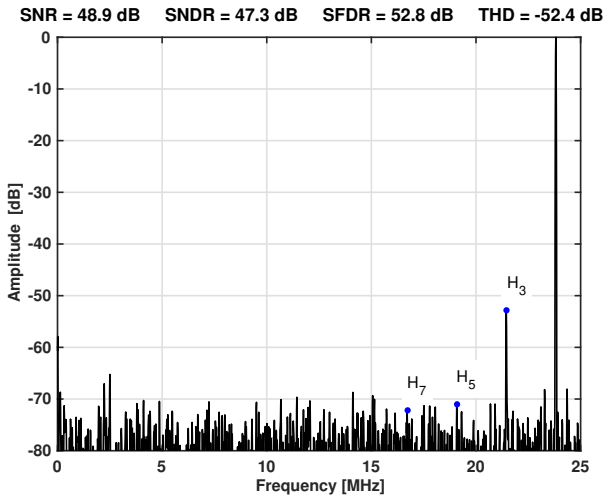

FIGURE 12 Post-layout simulated output spectrum, for a near-Nyquist frequency input signal (4096 points).

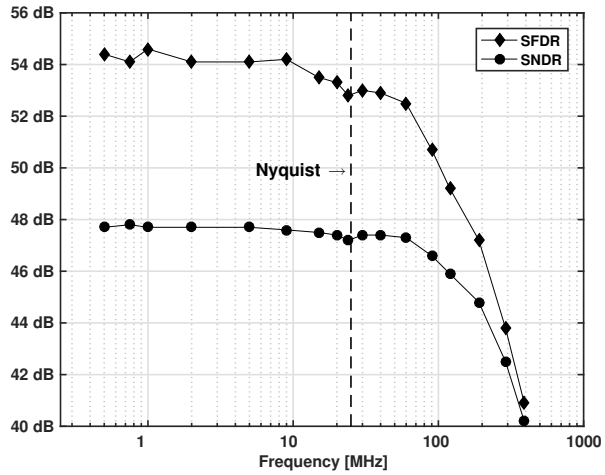

FIGURE 13 Simulated SNDR and SFDR as a function of the input frequency.

6 | CONCLUSIONS

A CS-SAR ADC that relies on the concept of variable reference voltages to embed the downconversion operation is presented. Inherent features of the CS scheme, such as the "pre-charge" of the DAC capacitors and over-rail operation, merge quite well with the proposed embedded downconversion approach and its applicability in radio applications. A mathematical analysis behind the approach, together with design considerations, is given. To provide an on-chip answer for the variable reference, an integer-N PLL is also designed. Post-layout simulations validate the approach, for an 8-bit 50MS/s CS-SAR ADC that occupies an active area of 0.0375 mm^2, while reaching an ENOB of 7.6 bits across the input frequency range.

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