Fábio Daniel dos Santos Vidago

Licenciado em
Ciências da Engenharia Electrotécnica e de Computadores

A Downconversion Beamforming RF Front-End in 130 nm CMOS technology

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Orientador: Prof. Dr. João Pedro Abreu de Oliveira, Prof. Auxiliar, Universidade Nova de Lisboa

Júri:

Presidente:	Prof. Dr. Paulo Miguel de Araújo Borges Montezuma de Carvalho
Arguente:	Prof. Dr. Luís Augusto Bica Gomes de Oliveira
Vogal:	Prof. Dr. João Pedro Abreu de Oliveira

FACULDADE DE CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

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"The scientists of today think deeply instead of clearly.
One must be sane to think clearly,
but one can think deeply and be quite insane."
- Nikola Tesla

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Abstract

Due to the exponential growth of wireless data communications an increasing number of components compete for space in the frequency spectrum. Nowadays, different approaches have been addressed in order to overcome this problem. One of these approaches is using spatial filters instead of time-domain ones. Since most wireless devices operate by transferring/receiving signals to/from all directions, interfering signals are becoming an increasing problem. Thus steering the transmission/reception of signals in a specific direction alleviates this problem, which is performed by employing multiple antennas.

In the scope of the spatial filtering approach, a 1 GHz downconvertion 4-element phased array receiver front-end is presented in this thesis, implemented in 130 nm Complementary Metal Oxide Semiconductor (CMOS) technology. The phase shifting of the beamforming receiver is implemented with a switched-capacitor vector modulator, that excels in its linearity and low power consumption. This receiver also provides a spatial rejection of more than 20 dB and good input matching.

Keywords: CMOS, MIMO systems, Beamforming, Phased arrays, RF receiver, Spatial filtering, Mixer, Phase-shifter, Switched-capacitor, Vector modulator.

RESUMO

O crescimento exponencial das comunicações sem-fio levou a um decréscimo na disponibilidade do espectro de frequências. Hoje em dia várias abordagens diferentes têm sido alvo de grande atenção e desenvolvimento, com o intuito de resolver este problema. Uma dessas abordagens é, em vez de aplicar filtros temporais, aplicar filtros espaciais. Tendo em conta que os aparelhos sem-fio transmitem/recebem sinais para/de todas as direções, os sinais interferentes são cada vez mais problemáticos. Portanto, uma forma de resolver este problema é direcionando a recepção/emissão numa direção específica, para tal é necessário empregar várias antenas.

No âmbito da abordagem em filtros espaciais, um receptor de RF do tipo *downconvertion* de 1 GHz com quatro antenas em fase é apresentado nesta tese, implementado em tecnologia *CMOS* de 130 nm. O desvio de fase para o construtor de feixe do receptor é implementado com um circuito do modulador vectorial em condensadores-comutados, que proporciona um baixo valor de consumo de potência e alta linearidade. Este receptor proporciona uma rejeição espacial de mais de 20 dB e uma boa adaptação de impedância de entrada.

Palavras-chave: *CMOS*, Sistemas *MIMO*, Construtor de feixe, Antenas em fase, Receptor RF, Filtragem espacial, Misturador, Desvio de fase, Condensadores-comutados, Modulador vectorial.

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GLOSSARY

IIP_3 Input Third Order Intercept Point.

IP_3 Third Order Intercept Point.

OIP_3 Output Third Order Intercept Point.

P_{1dB} 1 dB Compression Point.

ADC Analog-to-Digital Converter.

AF Array Factor.

AFE Analog Front-End.

BPF Band-Pass Filter.

CG Conversion Gain.

CMFB Common-Mode Feedback.

CMOS Complementary Metal Oxide Semiconductor.

DC Direct Current.

DOA Direction-Of-Arrival.

F Noise Factor.

GBW Gain-Bandwidth Product.

HPBW Half-Power Beamwidth.

IC Integrated Circuit.

IF Intermediate Frequency.

IM Intermodulation.

KCL Kirchhof Current Law.

KVL Kirchhof Voltage Law.

LNA Low-Noise Amplifier.

LO Local Oscillator.

LPF Low-Pass Filter.

MIMO Multi-Input Multi-Output.

MOSFET Metal Oxide Semiconductor Field-Effect Transistor.

NF Noise Figure.

NMOS N-type Metal Oxide Semiconductor.

NRZ Non-Return-to-Zero.

OpAmp Operational Amplifier.

PMOS P-type Metal Oxide Semiconductor.

PSD Power Spectral Density.

RF Radio Frequency.

RZ Return-to-Zero.

SNR Signal-to-Noise Ratio.

TIA Trans-Impedance Amplifier.

WPAN Wireless Personal Area Network.

CHAPTER 1

INTRODUCTION

1.1 Motivation

The last decades have seen the rapid rise of wireless data communications. Throughout the years, in order to improve signal transmission, one of the approaches has been to increase signal bandwidth and/or spectral efficiency. But aggressive bandwidth increase leads to one problem, spectrum unavailability. In order to solve this problem Multi-Input Multi-Output (MIMO) systems were proposed. These systems promised to improve signal transmission and enhance data bit-rates, through the use of multiple antennas, in the transmission and/or emission ends [1, 2]. However the support for this kind of system for the consumer electronics market has only recently started [3].

MIMO systems aren't as recent as one might think. In the early 1940s some radar systems, employing multiple antennas, were proposed to enhance reception, enable direction finding and increase jamming immunity. The technique that enabled the control of these MIMO systems was called beamforming. But only since 1990 have these systems become the target of heavy investigation. Nowadays MIMO systems have become an essential element of wireless communications standards, including Wi-Fi, 3G, 4G and in the future Massive MIMO has been regarded as a promising model for the high capacity demanded by 5G [4, 5]. For improved link reliability some wireless communication standards have already adopted beamforming, for example the IEEE 802.15.3c Wireless Personal Area Network (WPAN), and since this protocol suffers from heavy signal path loss, over 16 antennas may be employed for multi-gigabit data rate [6].

Beamforming is a signal processing technique which uses an array of sensors to perform spatial filtering. This is a technique that is useful in many scientific areas where radio or sound waves are employed, such as radar, sonar, ultrasonic imaging, astronomy, geophysical exploration and wireless communications [7, 8]. In this dissertation, the later application is the most relevant. Thus, the array of sensors, previously mentioned, are

antennas. Beamforming is a technique that can be employed to emit or receive a signal, its main goal is to achieve spatial selectivity to improve signal strength by rejecting interfering signals.

Figure 1.1 illustrates the block diagram of a typical digital-MIMO receiver and a analog beamforming receiver. In each design the Analog Front-End (AFE) amplifies and filters the incoming signal from each antenna, the signals then travel to each Analog-to-Digital Converter (ADC), where they're converted into the digital domain, processed and the MIMO computation and decoding is performed. It's rather obvious that each path in the MIMO system works much in the same way as a single-antenna system, up until the digital domain, thus the receiver is susceptible to interferers. These interferers may prove critical since it might put the ADC in a tight spot, and impose strict requirements upon its dynamic range. However, in the analog beamformer alternative, these interferers are ideally rejected, which in turn relaxes some the requirements of the ADC.

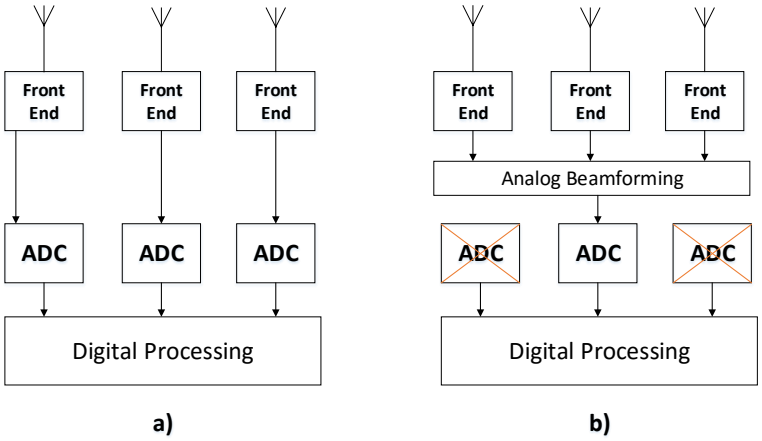

Figure 1.1: a) Digital-MIMO beamforming receiver. b) Analog beamforming receiver.

The term beamforming comes from the fact that spatial filters were designed to create beams in a desired direction. For example in figure 1.2, the radiation pattern of the device is so that the emission of energy is maximized at a 0^o angle, forming a beam of energy in that direction, thus "beamforming".

Beamforming is especially useful when working with systems that receive spatially propagating signals, because if an interferer signal occupies the same frequency band as our desired signal, a temporal filter might not be enough to separate the signal from interference.

Spatial filtering might also be achieved by physically moving the antennas, but in some applications the antennas might be static and such a technique might not be effectively employed.

A more effective approach to spatial filtering is using the beamformer to control the phase and amplitude of the signal at each antenna in the array, in order to create a pattern where the waves constructively and destructively interfere with each other in such a way

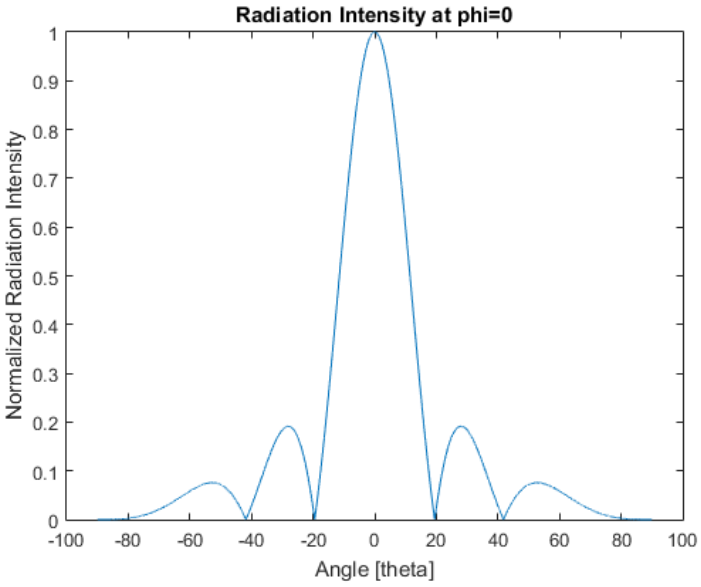

Figure 1.2: Example of a radiation pattern.

that the radiation pattern might be changed to achieve a better transmission or reception of the signal.

In an array of multiple antennas, if correctly designed, instead of receiving/emitting multiple independent signals, we can achieve a single narrower and more powerful signal beam pattern in one direction. In this case, beamforming can be achieved simply by employing a phase shift in the signal of each antenna to produce a beam in the desired direction, this array of antennas is called a Phased Array Antenna.

Besides the main lobe in the radiation pattern, side-lobes and nulls can also be controlled to ignore certain interferers in one particular direction while maintaining reception in others. This is also valid and useful on signal transmission.

Beamformers might be fixed or adaptive, the former uses fixed values for weightings and time-delays (or phasings), the latter adapts its values in real time, through the analysis of the signal received by the array, improving interference rejection. The adaptive process can be computationally intensive and some dedicated hardware processing might be required in order to effectively update the array's weightings and phasings.

Beamforming has been the target of a lot of research each with different approaches, some based on injection locking [9], phase selection [10] and vector modulation. Within the vector modulation there are also some slight differences, such as cartesian combining [1, 11, 12], all-passive switched-capacitor [13, 14] and switched approximate sine weighting [14–16]. Most of the mentioned approaches share the fact that the signals are processed in the continious-time domain, but since CMOS technology is being optimized for digital processing in the discrete-time domain. In this thesis a topology based on the latter is presented, where discrete-time phase shifters are implemented.

1.2 Thesis Outline

This thesis is divided in five chapters, the introduction being the first one, the rest is organized as follows:

Chapter two covers all the basic concepts of beamforming as well as some Radio Frequency (RF) design parameters. In this part all the required concepts of phased antenna arrays are explained, these important topics will be used in order to design the receiver in the following chapters.

Chapter three presents all the necessary steps in order to design each block of the receiver as well as give an overview of the architecture . In this chapter all the equations used in the design of the receiver are presented and all the topologies used for each block introduced.

Next, in chapter four all the simulations necessary in order to analyse the receiver and each of its blocks are presented along with all the relevant results. Some of these simulations are: impedance matching, voltage gain, noise figure and compression point.

The last chapter of this thesis, chapter five, evaluates the most important results obtained and some ideas for the optimization of the receiver as a whole and some of its blocks are proposed, as well as some interesting improvements.

CHAPTER 2

PHASED-ARRAY RECEIVER DESIGN

It is crucial, in order to understand how a beamforming AFE receiver is implemented, to comprehend some analog phased-array antenna receiver fundamental properties. Thus, in this chapter some basic beamforming concepts will be briefly explained. This chapter also has the purpose of introducing some basic principles of RF electronic circuits. These basic concepts will be used in the explanation of the design of each block in the receiver, in chapter 3.

2.1 Beamforming

Let's start by observing figure 2.1, that depicts a simplified schematic of a beamformer. As we can observe there are N antennas and each has a weight of a applied to its signal, thus the output at time t is given by the linear combination of the N antennas

$$s_{out}(t) = \sum_{n=0}^{N-1} a_n \times s_n(t)\,. \tag{2.1}$$

Since each antenna is equally spaced from each other, a distance of d meters, a signal travelling with a Direction-Of-Arrival (DOA) of θ degrees, figure 2.2, will travel slightly different distances in order to meet each antenna in the array, lets call the difference in distance the length on the n-th antenna l_n given by

$$l_n = n \cdot d \sin(\theta)\,, \tag{2.2}$$

this difference in distance causes in each antenna a certain time delay proportional to the extra length l_n. Since the waves travel at the speed of light c ($\approx 3 \times 10^8$ m/s), the delay in the n-th antenna τ_n is

$$\tau_n = \frac{l_n}{c} = \frac{n \cdot d \sin(\theta)}{c}\,. \tag{2.3}$$

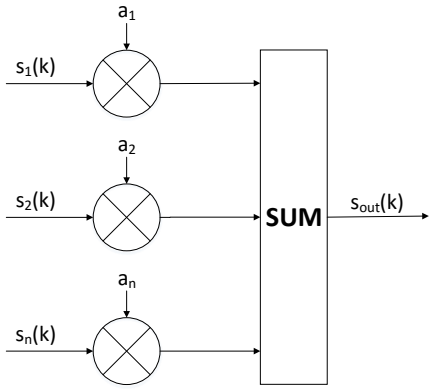

Figure 2.1: Simplified block diagram of a beamformer.

Supposing that a signal with amplitude A and frequency f is sensed by the first antenna ($n = 0$) its expression, in phasor form, is given by

$$s_0(t) = A\cos(2\pi ft) = Re\{A.e^{j2\pi ft}\}\,, \tag{2.4}$$

thus the signal wave sensed by the n-th antenna is

$$s_n(t) = A\cos[2\pi f(t+\tau_n)] = Re\{A.e^{j2\pi f(t+\tau_n)}\}\,, \tag{2.5}$$

since $\lambda = c/f$, combining equations 2.3 and 2.5 yields

$$s_n(t) = Re\{A\cdot e^{j2\pi ft}\cdot e^{j2\pi n\cdot\frac{d}{\lambda}\sin(\theta)}\}\,, \tag{2.6}$$

lastly combining 2.6 and 2.1 yields

$$s_{out}(t) = Re\left\{A\cdot e^{j2\pi ft}\sum_{n=0}^{N-1} a_n \times e^{j2\pi n\cdot\frac{d}{\lambda}\sin(\theta)}\right\}\,. \tag{2.7}$$

In conclusion the difference in the DOA of the signal wave, induces a different time of arrival between the antennas which in turn is transformed into an extra phase term.

2.1.1 Beam Steering

Now that we have the resulting signal of the beamformer from equation 2.7, we can proceed to the beam steering mathematics. In order to do so, a_n must be quantized, first this weight's objective is to null the time delays τ_n, due to the antenna spacing, thus we have

$$a_n = e^{-j2\pi\cdot\frac{d}{\lambda}u_0}\,, \tag{2.8}$$

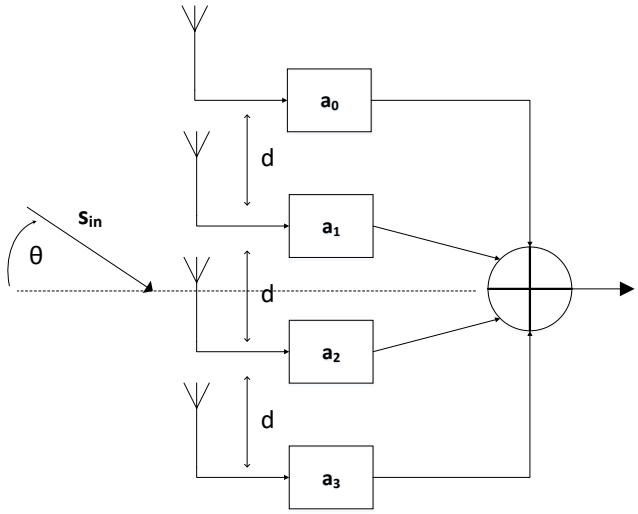

Figure 2.2: Wave signal with a DOA of θ degrees in a 4-element phased array receiver.

where for simplicity's sake $u_0 = \sin(\theta_0)$, this substitution is called sine space or direction cosine space [p. 17][17]. After these weights are applied the signals in each antenna are aligned in time. In other words, the time delays generated through the element spacing, in each signal path are compensated in order to coherently combine the signals at the output [18]. After defining a_n, looking back at equation 2.7, its value is maximized for a DOA of θ_0. The effect of the weights summing is called Array Factor (AF) and it is basically responsible for the variable gain as a function of the DOA [p. 286][19]. The array factor is defined as

$$AF(u) = \sum_{n=0}^{N-1} e^{j2\pi n \cdot \frac{d}{\lambda}(u-u_0)} . \tag{2.9}$$

A typical response of the array factor as a function of the DOA is illustrated in figure 2.3. In this plot a larger lobe, the absolute maximum, can be found, its called the main beam, some lesser lobes can also be found, they're defined as sidelobes. There are even some spots in the plot where the gain is zero, these are called the nulls. In essence, the array factor is the one responsible for the spatial filtering, the weights it adds in each path for each antenna govern the main beam, sidelobes and nulls, in order to direct the former to the wanted signal and the latter to the interferers.

When evaluating an AF one important parameter is the beamwidth, defined as the angular distance between two opposite points with the same maximum value. The Half-Power Beamwidth (HPBW) is the point at which the beam pattern assumes a value of half the maximum gain ($\approx$ -3 dB) [p. 42][19] . The equation that defines an HPBW is given by [p. 300][19]

$$u_{-3dB} \approx 1.391 \frac{\lambda}{\pi N d} . \tag{2.10}$$

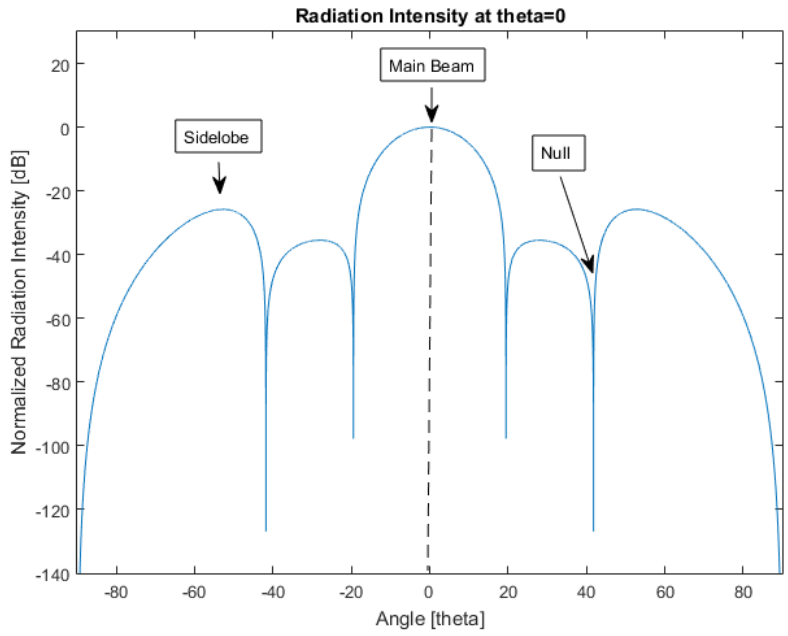

Figure 2.3: Array factor plot of a 4-antenna phased array.

Another important point about the array factor, is that the higher the ratio of d/λ is, the thinner the main beam becomes. If one wishes to design the narrowest main beam possible, the space between the antennas needs to be maximized. But there's an important side-effect to take into account. As d/λ increases, additional main beams may appear, these secondary main lobes positioned at directions other than θ_0, are defined as grating lobes. Thankfully, an equation exists to predict the appearance of these grating lobes, given by [20]

$$u = u_0 + i \cdot \frac{\lambda}{d}, \tag{2.11}$$

where $i \in \mathbb{Z}$, thus in order prevent the appearance of grating lobes a restriction to the maximum antenna spacing is imposed by

$$\frac{d}{\lambda_{min}} \leq \frac{1}{2}. \tag{2.12}$$

This restriction alters the definition of the array factor of 2.9, since λ_{min} is the wavelength for the maximum frequency of interest f_0, thus AF is rewritten as

$$AF(u) = \sum_{n=0}^{N-1} e^{j\pi n \cdot \frac{f}{f_0}(u-u_0)}. \tag{2.13}$$

This way the spacing for the antennas is selected in such a way that it will always be at the most half the wavelength at the highest frequency of interest, f_0 [14].

2.1.2 Directivity

The directivity D of an antenna is an important metric to describe it. It is derived from the beamwidth and, simply put, is the ratio between two signals of the same power, from an anisotropic antenna (a beam directed in a certain direction) for a certain DOA and an ideal isotropic antenna (the signal is radiated equally to all directions). It is defined as

$$\int_{-\pi}^{\pi} D(\theta) d\theta = 1\,, \tag{2.14}$$

for a scanning angle of $[-180^\circ;\ +180^\circ]$.

It is obvious to conclude that since the AF governs the beamwidth and optimal DOA, it directly influences the directivity. Thus substitution in 2.14 yields

$$\int_{-1}^{1} |AF(u)|^2 du = \int_{-\pi}^{\pi} \cos(\theta) \cdot |AF(\theta)|^2 d\theta = \sum_{n=0}^{N-1} |a_n|^2\,, \tag{2.15}$$

$$\int_{-\pi}^{\pi} \left[\cos(\theta) \cdot |AF(\theta)|^2 / \sum_{n=0}^{N-1} |a_n|^2 \right] d\theta = 1\,, \tag{2.16}$$

where the first part of the integral "$\cos(\theta)$" is defined as the directivity of an element in the phased array D_E, and the rest of the integral is defined as D_A, the array directivity, normalized by the summed power of the weights. Since the element directivity is, in essence, constant through all phased-array antennas, the array directivity is the most important value to report.

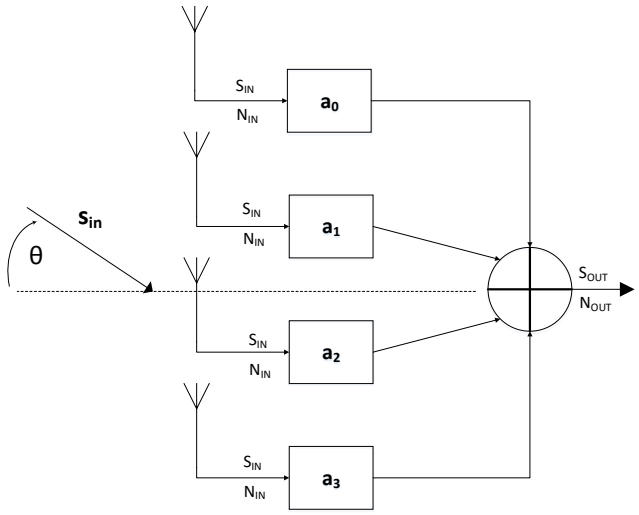

Figure 2.4: Signal power and noise in a phased-array antenna.

Now that D_A has been defined the next step is to take a look at the power that each antenna receives, figure 2.4. After having their respective weights a_n applied, and also

after summing the resulting signal power is

$$S_{out}(\theta) = S_{in} \cdot |AF(\theta)|^2 . \tag{2.17}$$

After computing the power of the signal the next step is to quantize the noise output, that encapsulates the circuits' input-referred noise as well as the noise due to signal propagation. The noise power is

$$N_{out} = N_{in} \cdot \sum_{n=0}^{N-1} |a_n|^2 . \tag{2.18}$$

The ration between 2.17 and 2.18 is the Signal-to-Noise Ratio (SNR) [1], which is equal to

$$\frac{S_{out}}{N_{out}}(\theta) = \frac{S_{in}}{N_{in}} \cdot \left[|AF(\theta)|^2 / \sum_{n=0}^{N-1} |a_n|^2 \right] = \frac{S_{in}}{N_{in}} \cdot D_A . \tag{2.19}$$

Equation 2.19 yields an extremely important result, the array directivity D_A, is directly proportional to the SNR. Furthermore, the D_A can be interpreted as an improvement over the SNR of a single element antenna [14]. This happens because since the noise present in each path can be considered uncorrelated to each other [21], thus if N antennas are used in the receiver the SNR can be improved by $10 \cdot \log(N)$. In conclusion for each doubling in the number of antennas in the phased array, the SNR of the receiver improves 3 dB [1, 16, 18].

2.1.3 Null Steering

In order to improve spatial selectivity there is a technique called Amplitude Tapering, that seeks to reduce the sidelobes' amplitudes [22, 23]. However there is a trade-off, because amplitude tapering reduces the array directivity, which means that the main beamwidth widens, this trade-off worsens as the number of antennas diminishes. Still, this technique can achieve a -10 dB drop in sidelobe amplitude below the main beam, in a phased-array with four antennas.

In any case, if the environment only has a single more powerful interferer signal, a null can be placed in its direction, achieving an effective rejection, this technique is called Null Steering [21]. As was mentioned in 1.1, beamformers can be fixed or adaptive, and whether the direction of the interferer is known a-priori or calculated a-posteriori, is what defines them.

Looking at figure 2.5, AF_{quies} represents the array factor steered to u_0, and u_{int} the direction of the interferer. The objective is to introduce a null in AF_{quies} at u_{int} without disturbing the gain of the main beam steered towards u_0. Thus a AF_{int} is created steered towards u_{int}, with its main beam maximum scaled to $AF_{quies}(u_{int})$, thus when subtracting

[1] Noise in a circuit, as a whole, and SNR, in particular, will be explained in 2.2.3

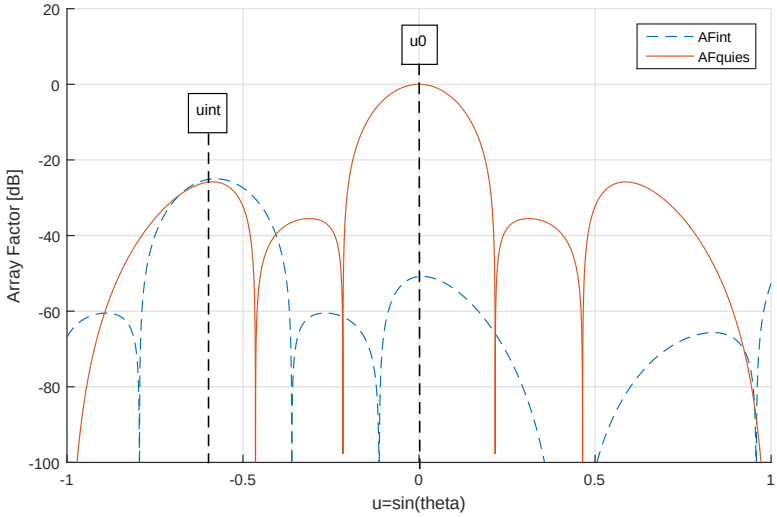

Figure 2.5: Array factors needed for null steering.

the two array factors a null is introduced in u_{int}. $AF_{null}(u)$, the resulting array factor is given by

$$AF_{null}(u) = AF_{quies}(u) - AF_{int}(u) = AF_{uni,u_0}(u) - AF_{uni,u_0}(u_{int}) \cdot \frac{1}{N} AF_{uni,u_{int}}(u)\,. \quad (2.20)$$

This is only possible because the array factors have an important property, they're linear. As in, a linear combination of array factors is equal to an array factor with the linear combination of the weights a_n. For the resulting AF, its main beam remains unaltered and at u_{int} a null is present. Although if a sidelobe is present at $AF_{int}(u_0)$, the pretended main beam will have a small gain loss of approximately 1 dB.

In conclusion, in order to improve spatial selectivity, for phased-array antennas with few elements it is preferable to use the null steering approach, however in receivers with more antennas, and many smaller interferers, amplitude tapering might be the most attractive technique.

2.2 Basic Concepts

2.2.1 Impedance Matching

When designing a Low-Noise Amplifier (LNA), there are many important parameters that need to be taken into account. One of these important parameters is impedance matching. Its importance stems from the fact that it is the process to reduce input return loss. When working with RF signals, since $\lambda = c/f$, the signal's wavelength is such that, in practice the antenna signal must travel a considerable distance in the printed-circuit board. Thus any deviation between the impedance of the antenna and the input impedance of the LNA

will increase the power reflection. If a portion of the signal's power is reflected back to the antenna, it means that less power is transferred to the receiver.

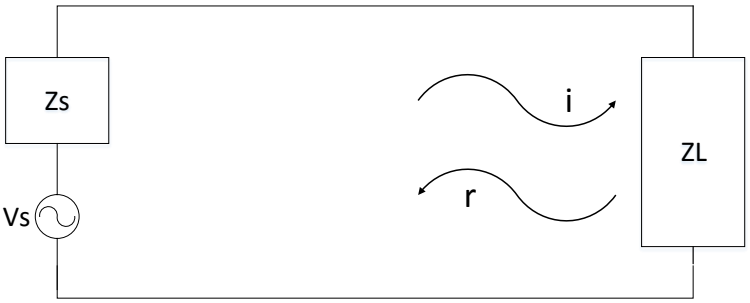

Figure 2.6: Example of incident and reflected waves in a generic circuit.

Figure 2.6 shows the equivalent circuit to analyse this phenomenon. To better understand the relation between impedance matching and the reflection coefficient Γ, let us analyse the next equation:

$$\Gamma = \left| \frac{Z_{in} - R_S}{Z_{in} + R_S} \right|^2 \tag{2.21}$$

Since the impedance of an antenna is usually 50 Ω ($R_S = 50\ \Omega$), one can plot the reflection coefficient Γ in the Z_L plane, thus:

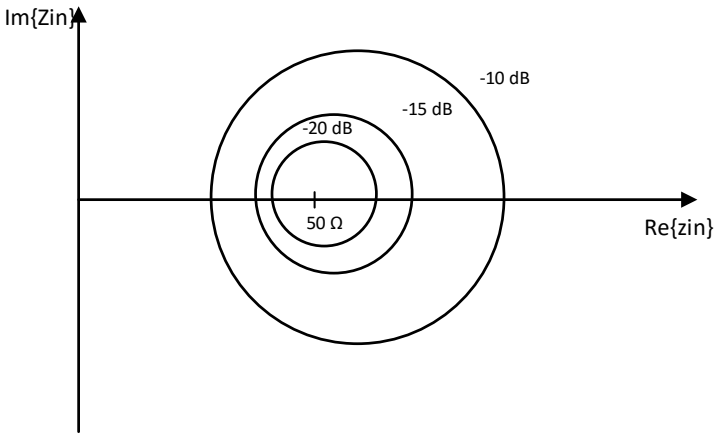

Figure 2.7: Plotted circles of constant values of Γ in the Z_L plane.

In figure 2.7 each circle represents a constant value of Γ. Through figure 2.7 and equation 2.21, one can observe that to minimize reflection and thus maximize the signal power transfer, one must simply design the input impedance of the LNA to be equal to the antenna output impedance $Z_S = Z_L$.

In practice, achieving perfect impedance matching is impossible, nevertheless a value of -10 dB for Γ is a typically acceptable value, since it signifies that only one tenth of

power is reflected, although one should strive to reduce this value further as to allow some safety margin. In conclusion designing LNAs requires circuit techniques that provide a 50Ω input resistance and near zero input reactance, without the noise that a 50Ω resistor provides [p. 266][24].

2.2.2 Scattering Parameters

Scattering parameters or S-Parameters, are a mathematical aid to ease the measurement of power quantities when designing high-frequency circuits. There are two main reasons to preferring the use of power quantities over voltage or current ones. Firstly, measuring the average power is easier than measuring a voltage or current. Secondly, usually the traditional design is based around the power transfer between circuit stages. These S-parameters, that are a result of the power analysis of a circuit, are used to describe the stage.

To better understand S-parameters, let's look at figure 2.8. In this figure we can denote a generalization of a two-port network, where the incident and reflected waves at the input port, P_1^+ and P_1^-, respectively, are present. Similarly, P_2^+ and P_2^- represent the incident and reflected waves at the output port, respectively [p. 72][24].

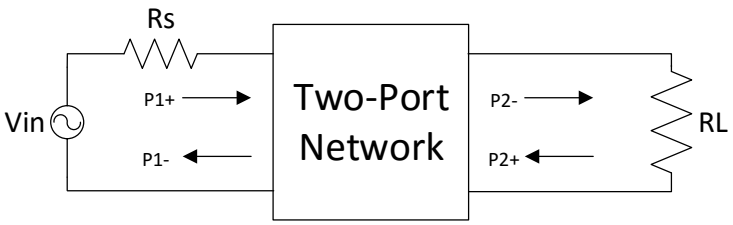

Figure 2.8: A two-port network

.

These four quantities, above described are related to one another through the S-parameters of the network, where:

$$P_1^- = S_{11}P_1^+ + S_{12}P_2^+ \tag{2.22}$$

$$P_2^- = S_{21}P_1^+ + S_{22}P_2^+ \tag{2.23}$$

Another representation for this relation is through a scattering matrix:

$$\begin{bmatrix} P_1^- \\ P_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \times \begin{bmatrix} P_1^+ \\ P_2^+ \end{bmatrix} \tag{2.24}$$

The next figure, 2.9, serves as a visual aid in order to have a more intuitive notion of what each parameter represents.

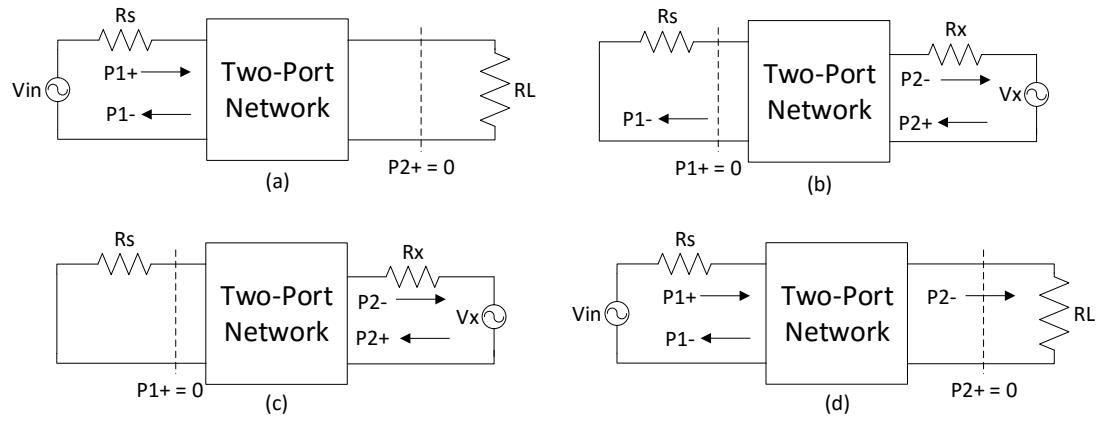

Figure 2.9: Two-port networks where circuits *a*, *b*, *c*, and *d* represent each scatter parameter.

As we can observe from figure 2.9 S_{11} is related with the reflected and incident waves at the input port, meaning the input reflection coefficient, which represents input matching accuracy

$$S_{11} = \frac{P_1^-}{P_1^+}|_{P_2^+=0}\,. \tag{2.25}$$

S_{12} is related with the reflected wave at the input port and the incident wave of the output port. This parameter can be interpreted as the "reverse isolation" of the system, meaning how much of the output signal travels backwards to the input source

$$S_{12} = \frac{P_1^-}{P_2^+}|_{P_1^+=0}\,. \tag{2.26}$$

Similarly to S_{11}, S_{22} is the related with the incident and reflected waves at the output port, thus it also represents a reflection coefficient but this time for output matching

$$S_{22} = \frac{P_2^-}{P_2^+}|_{P_1^+=0}\,. \tag{2.27}$$

Lastly, S_{21} is related with the incident wave on the load and the incident wave of the input. Thus this parameter represents the power gain of the circuit

$$S_{21} = \frac{P_2^-}{P_1^+}|_{P_2^+=0}\,. \tag{2.28}$$

Since modern RF design doesn't strive for between-stage matching, S_{11} and S_{21} are the most important parameters. As most circuits include reactive and/or active components one can easily conclude that s-parameters aren't scalar quantities, but often frequency dependent values (dependent of $j\omega$). It is important to point out that henceforth, s-parameters will be expressed in dB

$$S_{mn}|_{dB} = 20\log|S_{mn}|\,. \tag{2.29}$$

2.2.3 Noise

Noise is random, this means that the instantaneous value of noise cannot be predicted. It's an extremely important phenomenon to study when designing a RF system, since in an ideal world without noise or distortion, communication would be possible over any distance. In this chapter some basic notions about noise will be briefly explained.

As previously mentioned noise is random so, one might wonder how to properly study this phenomenon. The answer is simple because noise components in electrical circuits have a constant value of average power [p. 37][24], thus it can be defined as follows:

$$P_n = \lim_{T\to\infty} \frac{1}{T} \int_0^T x^2(t)dt\,. \tag{2.30}$$

One might reach the conclusion that studying noise in the time-domain is ineffective, however in the frequency domain, more useful and insightful information can be extracted. If the values for all frequency components of a noise signal are measured, the result is called the Power Spectral Density (PSD). The resulting plot of the PSD is the average power of the noise signal over the frequency.

In the next two sections, two main noise sources will be explained, since they're the most important and the ones primarily taken into account throughout the circuit's design. These two sources are: thermal and flicker noise.

Thermal Noise

This phenomenon occurs because the ambient temperature, creates random agitations in the charge carriers and thus, noise. In a resistor this noise value can be modelled by a Thevenin equivalent circuit with a voltage source of $\overline{V_n^2} = 4kTR_1$, or the Norton equivalent with a parallel current source of $\overline{I_n^2} = 4kT/R_1$, figure 2.10. Where k is the Boltzmann constant, T the temperature measured in $Kelvin$ and R_1 is the resistance of the component, in this example a resistor. The last sentence leads to an interesting conclusion: the device doesn't need to contain an explicit resistor to exhibit thermal noise.

In a Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) transistor, operating in the saturation region, the thermal noise can be roughly described as a current source between the source and drain terminals, alternatively it can be approximated by a voltage source in series with the transistor's gate, as shown in figure 2.11.

The value of the noise equivalent current source is:

$$\overline{I_n^2} = 4kT\gamma g_m\,, \tag{2.31}$$

and the equivalent voltage source is:

$$\overline{V_n^2} = 4kT\gamma/g_m\,. \tag{2.32}$$

Where g_m is the transistor's transconductance, and γ is the excess noise coefficient. Its value ranges from 2/3 up to 2, for long-channel and short-channel devices, respectively, however

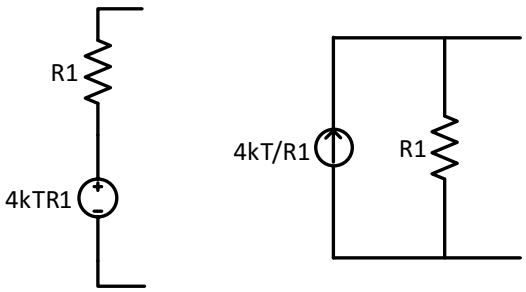

Figure 2.10: Equivalent circuit of the thermal noise effect on a resistor.

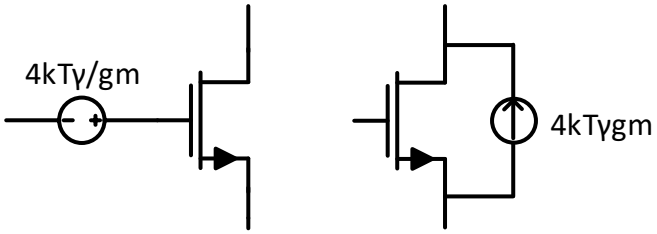

Figure 2.11: Equivalent circuit of the thermal noise effect on a MOSFET transistor.

γ is usually obtained by measurements. The gate resistance is another noise source, but its value is many times smaller than the “drain-source” current source equivalent, so it is omitted [p. 43][24].

Flicker Noise

Flicker noise is another type of noise that MOSFET transistors suffer from, it is modelled by a voltage source in series with the transistor’s gate [2], and its PSD is given by:

$$\overline{V_n^2} = \frac{K}{WLC_o x}\frac{1}{f}. \tag{2.33}$$

In the previous equation K is a process dependent constant, usually lower for P-type Metal Oxide Semiconductor (PMOS) than N-type Metal Oxide Semiconductor (NMOS), $C_o x$ is the gate oxide capacitance, W is the channel bandwidth, L its length and f the frequency. As we can observe there is a $1/f$ relation, because of this flicker noise is sometimes referred to as "$1/f$ noise".

[2] Much like thermal noise, flicker noise can also be modelled by a current source between the drain and source terminals.

An interesting observation is that, when plotted, flicker and thermal noise intercept at a certain point of frequency, called the corner frequency, f_c. Figure 2.12 illustrates this effect:

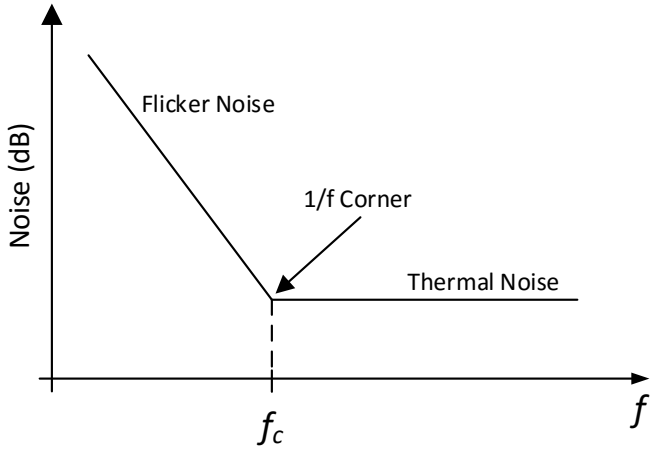

Figure 2.12: Illustration of noise in logarithmic scale *vs*. frequency.

Since the circuit presented in this dissertation is an RF designed circuit, one might wonder the relevance of flicker noise at higher frequencies due to its $1/f$ relation. This effect isn't negligible, since in can reach the RF range.

Noise Measurements

Above some of the basic concepts of how to modulate noise in a circuit were explained. Based on those explanations, this section will briefly introduce how noise is measured in a circuit.

The first step is to refer the noise of the circuit to the input. This is done because analysing the noise values at the output can be inconclusive, since an output with a high noise value might occur because of the high gain of the circuit and not necessarily a high noise. Figure 2.13 shows how this is modelled.

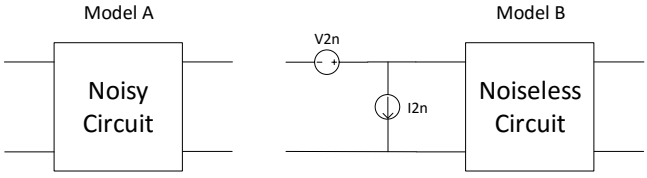

Figure 2.13: Circuit equivelent of input referred noise in a circuit.

This model has a series voltage source and a parallel current source, followed by a noiseless circuit. The former is equivalent to dividing the output noise by the voltage gain, the latter is obtained by dividing the output noise by the circuit's transimpedance

gain. Since at high frequencies these input-referred sources prove difficult to compute, a concept was introduced that allows an easier measurement of the noise performance in a circuit. This metric is called the Noise Figure (NF), or Noise Factor (F) [3].

In circuit design one might, instead of trying to measure the noise level itself, measure the SNR. SNR is the signal power divided by the noise power. If the input and output SNR are the same, it means the circuit is noiseless, but to quantify how noisy it is, noise factor is expressed as

$$NF = \frac{SNR_i}{SNR_o}. \tag{2.34}$$

In a noiseless circuit the previous equation is equal to one. NF is the F expressed in decibels, since each SNR is a dimension of power, it is defined as:

$$NF|_{dB} = 10log\frac{SNR_i}{SNR_o}. \tag{2.35}$$

A receiver usually has a chain with many stages, so it is important to compute the NF of the overall cascade, in terms of each stage. For example in a two stage cascade the total noise figure is given by

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{A_{P1}}. \tag{2.36}$$

One thing that is important to note is that the NF of the second stage has in its denominator the available power gain of the first stage, A_{P1}, but the NF of the first stage has no dependencies of the following stage. Generalizing for m stages we have

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{P1}} + ... + \frac{NF_m - 1}{A_{P1} \times ... \times A_{P(m-1)}}. \tag{2.37}$$

The previous expression is called Friis' equation [25]. An important conclusion is, that the noise contribution of each stage decreases as the total gain of the preceding stage cascade increases. However if a stage suffers from attenuation the noise figure contribution of the succeeding stages rises. This also means that the first stage of the receiver, usually the LNA, is the most important, noise-wise, since it has no dependencies besides itself, and its gain directly influences the total noise of the cascaded stages.

2.2.4 Nonlinearities

When a RF circuit is designed it is usually based around linear models for small signal operations, but some nonlinearities can occur and lead to some interesting phenomena not anticipated by the linear models, for example we assume that most amplifiers have a fixed gain for a certain frequency range, however this isn't always so. In this section some nonlinearities will be briefly explained, these metrics will be used at a later part of this work to evaluate the linearity of some blocks.

[3] The difference between the two is explained further ahead

Gain Compression

One of the nonlinearities is the assumption that the small signal gain of a circuit is independent of the present harmonics. But this is not the case when working with non-ideal components. If the amplitude of a harmonic is high enough, it can lead to compressive behaviour in the amplifier, meaning that as the input amplitude rises the gain decreases.

This effect is quantified by the 1 dB Compression Point (P_{1dB}), it is defined as the point at which the input signal causes the gain to drop by 1 dB. The value for the compression point isn't chosen arbitrarily, because a 1 dB compression point represents a 10% reduction in the gain, and it is a very important metric to characterize RF circuits and systems [p. 18][24].

Compression can be expressed in terms of voltage or power quantities although from this point onward whenever compression is discussed it will always be in terms of power quantities.

In figure 2.14 we plot the input power *vs* the output power, and its result as we can observe, is a line and its slope is the gain. As the input power continues to rise, upon reaching a certain value the gain begins to decrease, as explained above the amplifier goes into compression, and at the point at which the power drops 1 dB below the expected value we can find the circuit's 1 dB compression point.

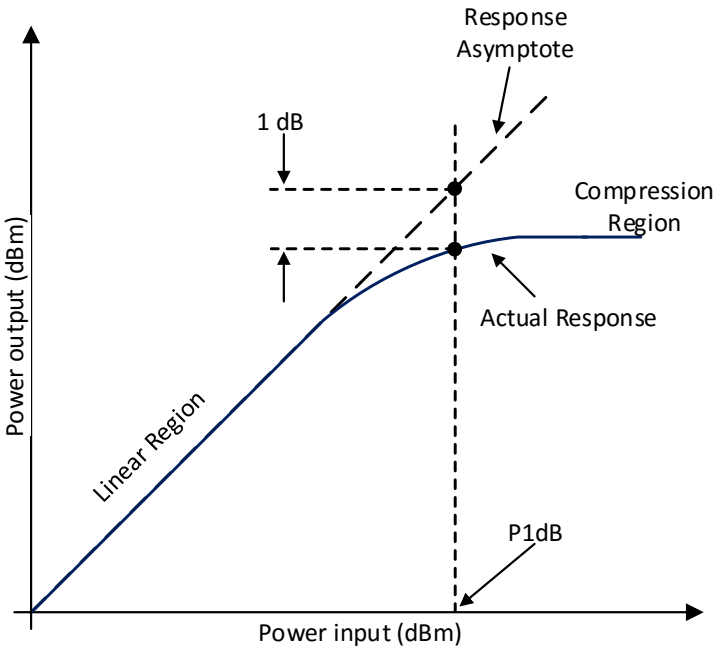

Figure 2.14: Illustration of the 1 dB compression point.

As it was mentioned, the gain flattens, meaning that the amplifier becomes saturated, this is a very important phenomenon because the response of a saturated amplifier is non-linear, leading to signal distortion, harmonics and even Intermodulation (IM) products.

Thus, if the compression point is known we can restrict the input levels to prevent the saturation of the amplifier and its non-linear consequences.

It is also important to note that 1 dB compression point can also be specified in terms of the output level at which it occurs, analysing the compression point in terms of input or output power depends on the application either in the transmission or receiving path.

This characteristic is measured by driving a sine wave at the input of the amplifier for a certain frequency and plotting its response, meaning the output power, thus creating the graphic of the figure 2.14.

In conclusion, the higher the P_{1dB}, the more linear and robust an amplifier is.

Intermodulation Products

In this section another important consequence of a circuit's nonlinearity will be briefly explained. When two signals are applied to a nonlinear system, its output can exhibit components that result from the mixing of its inputs, this is called intermodulation product.

To better understand the effects of intermodulation let us take for example two signals with frequencies of ω_1 and ω_2. When applied to a nonlinear system these frequencies are multiplied and new signals are produced with a frequency of $\omega_1 - \omega_2$ and $\omega_1 + \omega_2$, that can be easily filtered. However, higher order mixing can occur which produces potentially interfering signals close to our work frequency that may not be easily filtered. Usually the most worrisome are the third-order IM products, $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$, of which the most possible to occur within the system's frequency range are $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$[4]. Figure 2.15 illustrates this phenomenon:

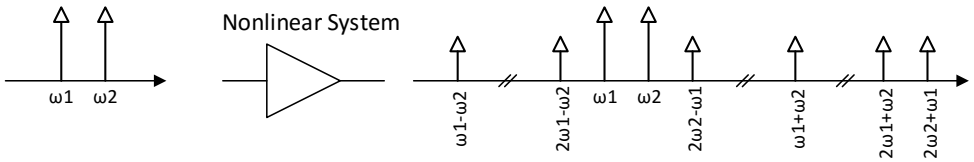

Figure 2.15: Illustration of the intermodulation phenomenon.

As we can observe if ω_1 is close to ω_2, the third order products $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ will also be close to our signal making it extremely hard or even impossible to filter.

Now that we have acknowledged the importance of intermodulation products, the next step is to find a method to measure them. This metric exists and it is called the Third Order Intercept Point (IP_3). The concept of the IP_3 originates from the fact that if the power or amplitude of the input signal rises, its intermodulation products rise more sharply, thus the IM products eventually become equal to that of our signal of interest. On a logarithmic scale, the third order products increase at a rate three times higher than that of first-order products (the input signals), because of the mathematics of mixing [pg. 21][24].

[4]Higher order products also exist but usually they lie far away in terms of frequency, thus heavily filtered by the system's own dynamic.

Similarly to the P_{1dB} explained in the previous section, plotting the output power versus the input power of our fundamental signal power and also the third-order signal power, we can find the point where these intersect and it's called the IP_3, figure 2.16 is an example of an IP_3 plot.

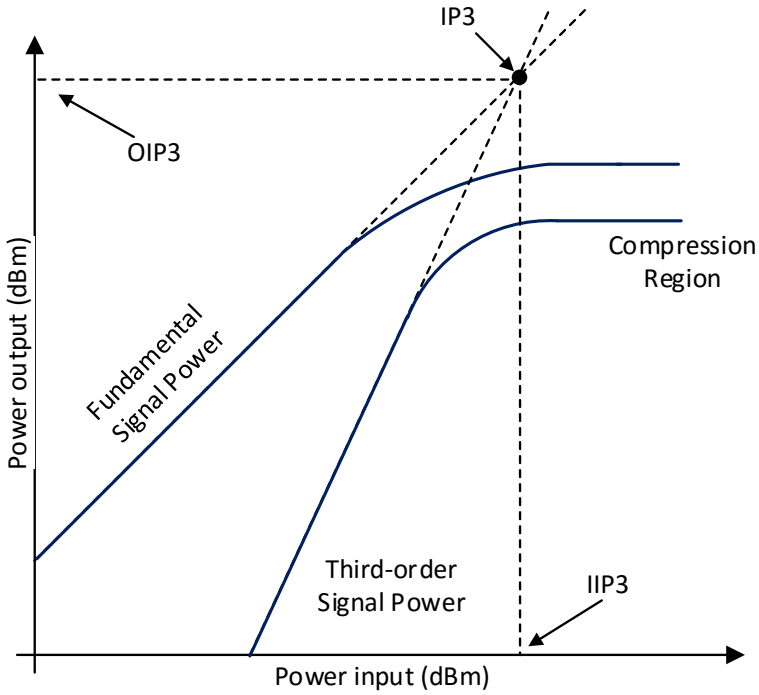

Figure 2.16: Illustration of the third order intercept point.

The value of IP_3 can be read with reference to the input or output powers, called Input Third Order Intercept Point (IIP_3) or Output Third Order Intercept Point (OIP_3), respectively. From this point onward in this thesis IP_3 will be written rather than IIP_3, since the input will be the reference of interest.

As we can observe from the figure 2.16, if compression happens before the intersection one can extrapolate these plots according to their slopes to find the theoretical point of intersection, the IP_3. Regardless of whether the IP_3 occurs before or after compression, this is an important method of determining the linearity of an amplifier. It is obvious to conclude that the higher the IP_3 value of a system the more linear it is and the lower intermodulation distortion it has.

CHAPTER 3

BEAMFORMING RF FRONT-END DESIGN

In the previous chapter the basic concepts required to design the AFE were introduced. In this chapter the necessary steps for the design of each block in the receiver will be explained. Figure 3.1, schematically depicts the architecture intended for the beamforming RF front-end.

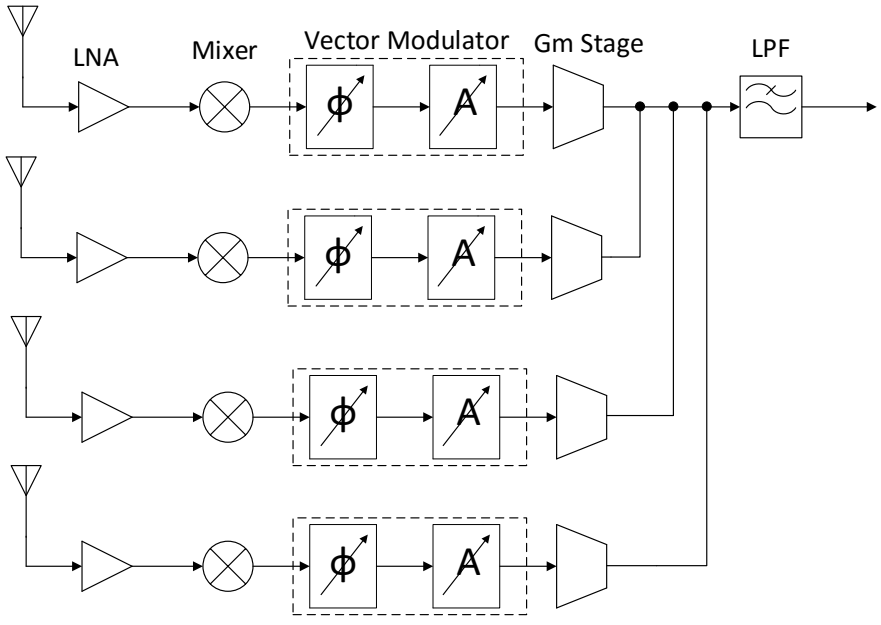

Figure 3.1: Architecture of the 4-element beamforming AFE.

Two slightly different architectures were implemented in this thesis. The first works as follows: in each of the four elements, a transconductance LNA performs input impedance matching and amplifies the signal received from the antenna, converting it into a current

signal. Then a passive single-balanced mixer with four paths, controlled by 4 out-of-phase 25% duty-cycle LOs, generate four different signals, in-phase (I+), quadrature (Q+, 90°), opposed-phase (I-, 180°) and quadrature opposed-phase (Q-, 270°). The following block, the TIA converts the current signals from the mixers to voltage signals that are fed into the switched-capacitor vector modulator, that performs the phase-shifting. Next the Gm-stage, converts the signals into the current domain in order to sum the signals from the four elements, finally the signal are converted back into the voltage domain through load resistors and filtered with a Low-Pass Filter (LPF) to remove the higher frequency harmonics.

Since this architecture didn't yield the pretended results, a second more simple one was implemented, the second one is very similar to the first, and it works as follows: the LNA performs a voltage amplification, the double-balanced mixer operates in the voltage domain, providing the same outputs (I+, I-, Q+ and Q-), a simple ideal voltage buffer separates the mixer and the phase shifter, and as with the first architecture the same gm stage performs element summing in the current domain, the resistors convert the signals back into the voltage domain and a LPF filters the unwanted higher frequencies.

3.1 Common-Source Low-Noise Amplifier

The Low-Noise Amplifier is usually the first stage of a receiver, thus its role is a critical one for the overall performance. As seen in section 2.2.3, through the Friis' equation 2.37, to minimize the overall NF of the receiver the LNA must be designed to have a high gain and low NF, since it directly affects the succeeding stages' noise performance. In a typical RF receiver a total noise figure of 6 to 8 dB is to be expected, for which the LNA's contribution is of about 2 to 3 dB [p. 255][24], leaving the rest to the subsequent blocks.

One might deduce that the gain should be as high as possible to minimize the NF of the receiver. But this leads to a decrease in linearity, so a compromise must be made between minimizing the noise contribution of the subsequent stages and the linearity of the receiver.

Another important aspect to take into account is the power transfer from the antenna to the next stages, thus, as explained in the section 2.2.1, a good input matching must be achieved. In essence, the input resistance of the LNA must be 50 Ω and the reactance must be close to zero.

These three previous properties, especially the input-matching, limit the choice for the LNA topology. Thus, the chosen amplifier topology for the receiver is an inductively degenerated common-source cascode LNA, as shown in figure 3.2. This is one of the most popular narrowband approaches, it provides a high output resistance, high gain, low noise and good input matching. Being a narrowband topology it means that input impedance matching is only required for a given frequency.

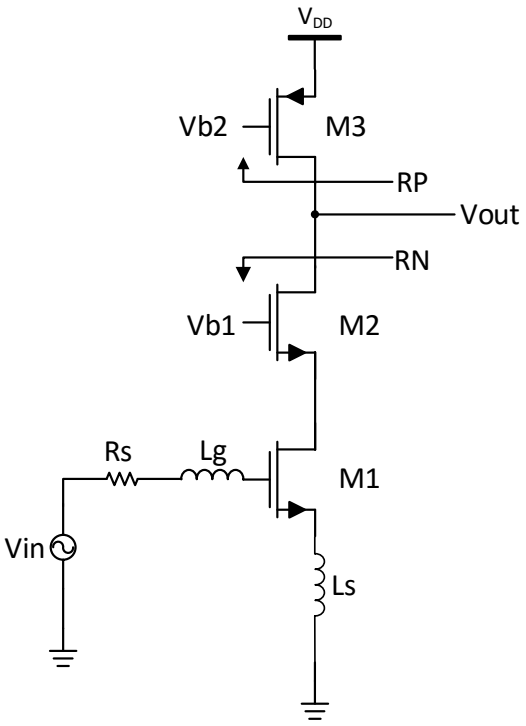

Figure 3.2: Common-source LNA topology.

Gain

The first step in the LNA design was to compute its gain, as such the DC gain of this LNA topology is given by

$$Av = \frac{V_{out}}{V_{in}} = gm_1 \times R_{out}\,, \tag{3.1}$$

where gm_1 is the transconductance of the transistor M_1 and R_{out} is the output resistance.

The resistance R_{out} is the parallel of two resistances, R_P and R_N, the impedances of the PMOS transistor M_3 and the cascode impedance of transistors M_1 and M_2, respectively. Thus

$$R_{out} = R_P \parallel R_N\,, \tag{3.2}$$

where $R_P = rds_3$ and

$$R_N = rds_1 \cdot \frac{gm_2}{gds_2}\,, \tag{3.3}$$

where $gds_2 = 1/rds_2$. In conclusion to maximize the LNA's gain, one must choose the transistors' sizes in order to maximize their transconductance and drain-source resistance. A reasonably high DC gain is to be expected, since it is one of this topology's strong suits.

Biasing

It's been established that the LNA's transistors need a high transconductance in order to achieve a high gain, which means that the transistors need a reasonable value for its drain-source current, I_{ds}. The M_1 and M_3 are each biased with a $1:1$ ratio current-mirror. These two transistors impose the necessary current in the LNA, so the biasing of M_2 is done by simply connecting its gate to V_{DD}.

Impedance Matching

As it can be seen in figure 3.2, the circuit uses reactive components, in this case two inductors, to perform impedance matching. In order to compute the input impedance of the LNA, the small signal model must be drawn and analysed. Figure 3.3 illustrates this very model, where the transistor's gate-drain and source-bulk parasitic capacitances, C_{gd} and C_{sb}, respectively , were neglected.

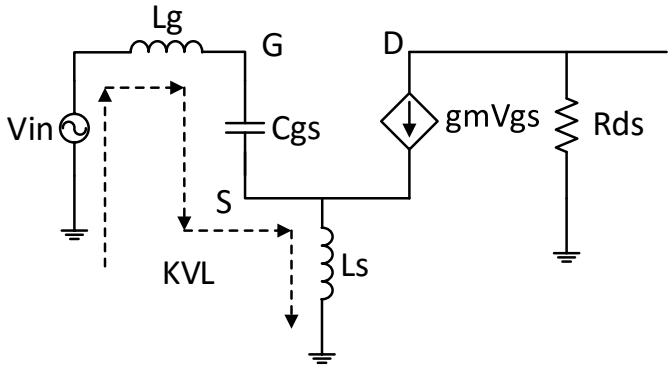

Figure 3.3: LNA small signal model for input resistance computation.

To find the expression of the input impedance of the LNA Z_{in}, the Kirchhof Voltage Law (KVL) was applied, yielding:

$$
\begin{aligned}
V_x &= V_{L_g} + V_{C_{gs}} + V_{L_s} \\
V_x &= I_x \cdot j\omega L_g + V_{gs} + (I_x + gmV_{gs}) \cdot j\omega L_s \\
V_{gs} &= I_x \cdot \left(-j\frac{1}{\omega C_{gs}}\right) \\
V_x &= I_x \cdot j\omega L_g + I_x \cdot \left(-j\frac{1}{\omega C_{gs}}\right) + I_x \cdot j\omega L_s + gm \cdot I_x \cdot \left(-j\frac{1}{\omega C_{gs}}\right) \cdot j\omega L_s \\
Z_{in} &= \frac{V_x}{I_x} = j\omega L_g + \left(-j\frac{1}{\omega C_{gs}}\right) + j\omega L_s + gm \cdot \frac{L_s}{C_{gs}} \\
Z_{in} &= \frac{gmL_s}{C_{gs}} + j\left[\omega(L_g + L_s) - \frac{1}{\omega C_{gs}}\right]
\end{aligned}
\tag{3.4}
$$

After deducing the expression for Z_{in}, the next step is to equate the real and imaginary parts, to 50 Ω and 0 Ω, respectively.

$$\frac{gmL_s}{C_{gs}} = 50\Omega \Leftrightarrow L_s = \frac{50 \cdot C_{gs}}{gm}\,. \tag{3.5}$$

The previous equation is used in order to fix the value for L_s, now in order to null the imaginary part of Z_{in}

$$\omega(L_g + L_s) - \frac{1}{\omega C_{gs}} = 0 \Leftrightarrow L_g = \frac{1}{\omega^2 \cdot C_{gs}} - L_s\,. \tag{3.6}$$

A quick look at equation 3.5 leads to an interesting conclusion, since a transistor's C_{gs} is usually very small, sometimes a few fF of capacitance only, and the gm is usually lower then a couple dozen mS, this means that L_s must have an extremely low inductance, probably below 100 pH. Also in RF Integrated Circuit (IC) design a bond wire is inevitable in packaging, and it must be taken into account. This bond wire usually has an inductance no lower than a couple hundread pH to a few nH. These facts in conjunction lead to a paradox, on one hand we need a rather low value of inductance to achieve input matching, on the other hand, we already have an inductance of a couple nH present. An important question arises, how can a 50 Ω resistance be obtained?

Looking back at the real part of equation 3.5, one might reduce gm or increase C_{gs} accordingly, to try to raise L_s. The easiest method is usually to place a capacitor of a few pF between the source and gate of the transistor in order to artificially increase C_{gs}, which means that L_s can assume higher values. In this case the bond wire's inductance serves as the inductor L_s.

The L_g inductor is off-chip so there are fewer restrictions for its inductance value, achieving higher values of Q which is the inductor's quality factor given by

$$Q = \frac{\omega L}{R_s}\,, \tag{3.7}$$

where ω is the operating frequency, L the inductance value and R_s the equivalent series resistance of the inductor's windings.

Noise

Lastly, to find this topologies' NF let's start by looking at figure 3.4. The current source I_{n1} represents the noise source of the transistor M_1, and I_{out} the output of the LNA[1], thus

$$I_{out} = gmV_{gs} + I_{n1} \Leftrightarrow V_{gs} = \frac{I_{out} - I_{n1}}{gm}\,. \tag{3.8}$$

Similarly to the input impedance calculation steps for equation 3.4, the KVL yields

$$V_{in} = s(R_s + sL_g)V_{gs}C_{gs} + V_{gs} + sL_s(I_{out} + sV_{gs}C_{gs})\,, \tag{3.9}$$

[1] R_s is the resistance of the voltage source, meaning, the antenna resistance usually 50Ω but L_s is the inductor connected to the transistor's source.

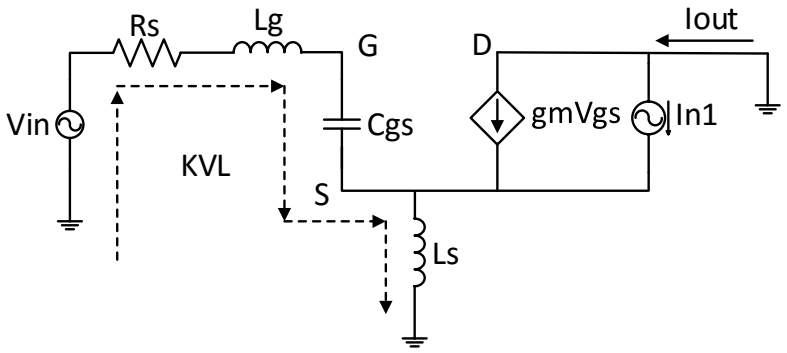

Figure 3.4: LNA small signal model for NF calculation.

since substitution of V_{gs} from 3.8, yields

$$V_{in} = sL_sI_{out} + \left[s^2(L_s + L_g)C_{gs} + 1 + sR_sC_{gs}\right] \cdot \frac{I_{out} - I_{n1}}{gm}\,, \tag{3.10}$$

as it was previously mentioned when discussing input matching, L_s and L_g were designed to resonate with C_{gs} at ω_0, meaning that $(L_s + L_g) \cdot C_{gs} = \omega_0^2$, thus if $s = j\omega_0$

$$s^2(L_s + L_g) \cdot C_{gs} + 1 = 0\,, \tag{3.11}$$

and the substitution of 3.11 into 3.10 gives

$$V_{in} = I_{out} \cdot \left(j\omega_0 L_s + \frac{j\omega_0 R_s C_{gs}}{gm}\right) - I_{n1}\frac{j\omega_0 R_s C_{gs}}{gm}\,. \tag{3.12}$$

In the last equation the coefficient of I_{out} represents the transconductance gain of the circuit, given by

$$\left|\frac{I_{out}}{V_{in}}\right| = \frac{1}{\omega_0\left(L_s + \frac{R_sC_{gs}}{gm}\right)}\,. \tag{3.13}$$

As previously stated the circuit's been input matched and one of the conditions for input matching was that $gmL_s/C_{gs} = R_s$, and also since $gm/C_{gs} \approx \omega_T$ is the maximum switching frequency of the transistor, its substituion in 3.13 gives

$$\left|\frac{I_{out}}{V_{in}}\right| = \frac{\omega_T}{2\omega_0} \cdot \frac{1}{R_s}\,. \tag{3.14}$$

This last equation raises an important conclusion, when input matched, the transconductance gain of the circuit is independent of L_s, L_g and gm. The next step is to null V_{in}, so from equation 3.13 we have the output noise from transistor M_1

$$|I_{n,out}| = |I_{n1}| \cdot \frac{R_sC_{gs}}{gmL_1 + R_sC_{gs}}\,, \tag{3.15}$$

and much like it was done for the transconductance gain of the circuit, since $gmL_s/C_{gs} = R_s$, the previous equation yields:

$$|I_{n,out}| = \frac{|I_{n1}|}{2}\,, \tag{3.16}$$

from 2.31 in section 2.2.3, we have

$$\overline{I_n^2} = 4kT\gamma g_m\,. \tag{3.17}$$

Thus, dividing the output noise current by the transconductance gain of the circuit and by $4kTR_s$ while adding 1 to the final result, the expression for the LNA's noise is given by equation 3.18 [p. 289] [24]

$$F = 1 + gmR_{in}\gamma\left(\frac{gm\omega_0}{C_{gs}}\right)^2\,. \tag{3.18}$$

This last expression, which as previously stated only holds true if the circuit is impedance matched at the resonating frequency, shows that this topology can provide low noise values [p. 289][24].

3.2 Mixer

The mixer is a very important stage in receiver or transmitter architectures, because it performs a frequency translation by multiplying two waveforms, as shown in figure 3.5.

There are two kinds of mixers, upconversion and downconversion, used in the transmit and receive paths, respectively. In this dissertation a downconversion mixer was designed to convert a RF signal into an Intermediate Frequency (IF) signal. There are also two other main categories for classifying mixers, passive and active, the former uses transistors operating as switches, the latter uses transistors that operate as amplifiers. Since passive mixers have low power consumption a passive topology was chosen, explained below.

The mixer has three ports, two inputs and an output. In the downconversion case, the former are the RF and Local Oscillator (LO) ports, and the latter is the IF port. As illustrated in figure 3.5, for example, if the LO signal is $V_{LO}(t) = \cos(2\pi f_{LO}t)$, and the RF is $V_{RF}(t) = \cos(2\pi f_{RF}t)$, the IF signal will be given by

$$V_{IF}(t) = \frac{K}{2}[\cos(2\pi(f_{RF} - f_{LO})t) + \cos(2\pi(f_{RF} + f_{LO})t)]\,, \tag{3.19}$$

where K is the mixer's conversion loss. The desired frequency component of equation 3.19 is the IF one ($f_{IF} = f_{RF} - f_{LO}$), this component can be isolated through the use of a LPF.

There are some important performance parameters that need to be taken into account when designing the mixer. As it was explained in section 2.2.3, through Friis' formula 2.37, in the receive chain the noise of the mixer is divided by the gain of the LNA. However one should always strive to contain the NF. The mixer's NF is usually greater than 8 dB, in any case it should be designed for a NF value under 15 dB, a typical value in IC design.

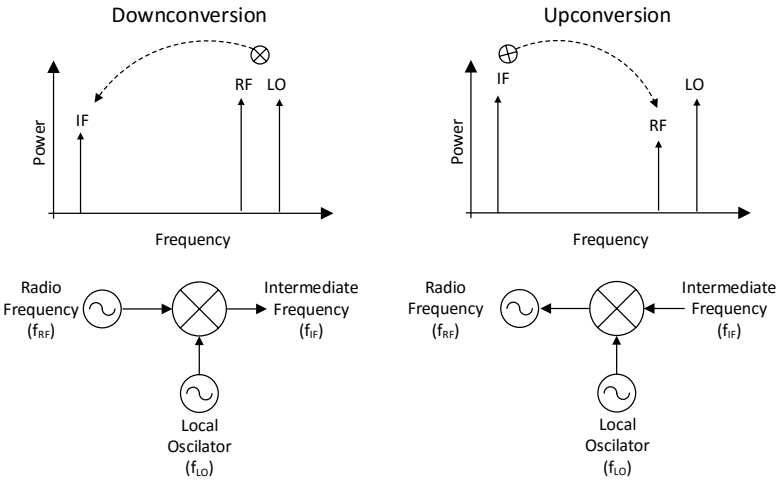

Figure 3.5: Graphic representation of the mixer operation.

As with the noise, the IP_3 of the mixer is also divided by the LNA's gain. This leads to a compromise between noise and linearity, a consequence of this is that the design of the mixer and the LNA are linked. It's common to, while designing the mixer, return to the LNA's design in order to achieve a higher gain to compensate a poor noise or linearity performance by the mixer.

Clock Feedthrough

When designing a mixer, especially if realized by a MOSFET, unwanted coupling between the inputs and outputs of the device may occur, because the transistors have parasitic capacitors. What this means is that if the capacitances are large enough, the LO signal might, for example travel to the RF and/or IF ports. This effect is called port-to-port feedthrough, graphically represented in figure 3.6. The LO to RF feedthrough is prejudicial since it produces offsets in the IF port and LO signals back to the antenna, on the other hand the LO to IF feedthrough can usually be suppressed through a LPF [24].

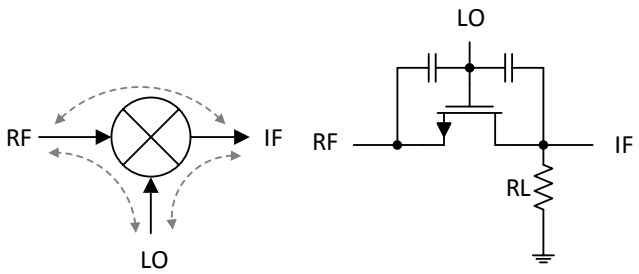

Figure 3.6: Feedthrough representation in a mixer.

To better understand how to avoid port-to-port feedthrough let's take a look at equation

3.20 which characterizes the MOSFET capacitances in the saturation region [p. 124][26]

$$C_{gs} = C_{gd} = W \cdot L \cdot C'_{ox}\,, \tag{3.20}$$

where W and L are the transistor's channel width and length, respectively and C'_{ox} is the device capacitance per unit of area. So in order to reduce port-to-port feedthrough, one must simply take special care with the device size.

Looking back at the circuit in figure 3.6, it's easy to denote that this simple mixer topology, since it operates with single-ended RF and LO inputs, discards the RF signal every half of a LO period. In order to eliminate this efficiency deficit, another mixer can be added to the RF port, with a differential LO input, this topology illustrated in figure 3.7 is called a passive single-balanced mixer [p. 355][24].

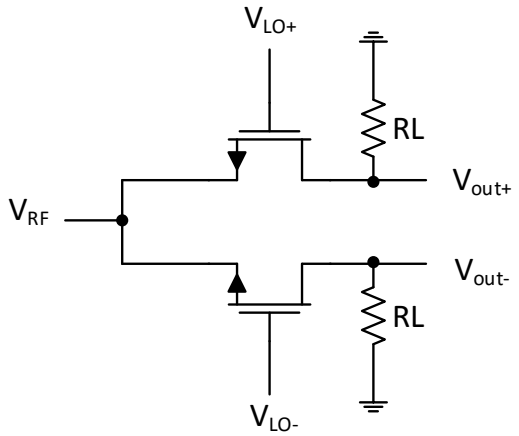

Figure 3.7: Single-balanced mixer.

Besides doubling the conversion gain (or increasing by 6 dB), the single-balanced mixer also provides differential IF outputs with a single-ended RF input.

Another more advanced topology where two single-balanced mixers are employed to reduce and sometimes eliminate LO-IF feedthrough also exists and it's called a double-balanced mixer, the circuit is illustrated in figure 3.8. Mixers, broadly speaking, can also be separated into two categories, passive and active. Each of these categories can be implemented as single-balanced or double-balanced. The main difference is that passive mixers don't employ transistors that operate as amplifiers, while the active counterparts do. In this thesis a passive mixer topology was chosen, for its lower power consumption, leaving the other blocks in the AFE to accommodate the receiver gain.

Conversion Gain

Another important performance parameter of the mixer is the Conversion Gain (CG), which is the ratio between the input and output of the mixer, the RF and IF signals, the LO signal isn't taken into account for the conversion gain calculation, because it serves

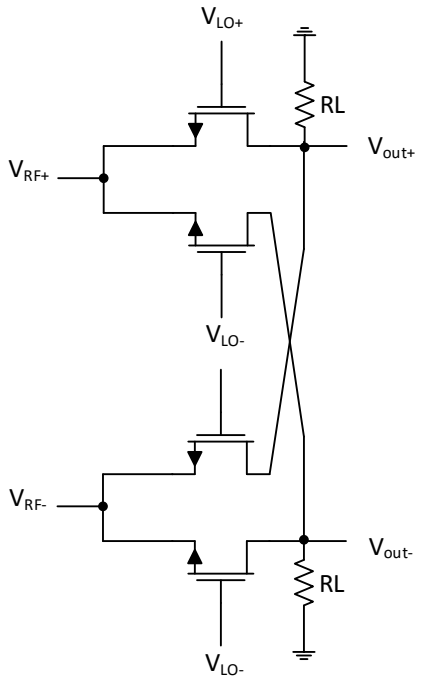

Figure 3.8: Double-balanced mixer.

only as an auxiliary tool for downconversion, it carries no relevant information. Thus the CG expression is

$$CG|_{dB} = 20\log\left(\frac{V_{IF}}{V_{RF}}\right). \tag{3.21}$$

A typical value of CG for a mixer topology, illustrated in figure 3.6, is $1/\pi$ ($\approx$ -10 dB), since the single- balanced topology has a twice the gain, the CG amounts to $2/\pi$ ($\approx$ -4 dB).

The mixer of figure 3.6, is sometimes called a Return-to-Zero (RZ) mixer because the output is zero when the switch is turned off ($V_{LO} = 0$). One way to improve its gain is to swap the resistor with a capacitor, thus obtaining a passive Non-Return-to-Zero (NRZ), sampling or sample-and-hold mixer, figure 3.9 [27]. This improved topology has a higher gain because the output is held and not reset, when the switch is off.

The conversion gain of this circuit is

$$CG_{NRZ} = \sqrt{\frac{1}{\pi^2} + \frac{1}{4}} \approx 0.5927 \approx -4.54dB \tag{3.22}$$

A NRZ version for the single-balanced mixer also exists and it also has twice the gain of the single-path NRZ counterpart, thus having a gain of $2 \times CG_{NRZ} = 1.1854 \approx 1.477$ dB . This is a very interesting result, because having a conversion gain higher than unity is remarkable on a passive mixer topology. And as previously stated, having a gain higher than unity is beneficial in terms of the receiver's NF, through equation 2.37, which makes this topology very attractive in RF design.

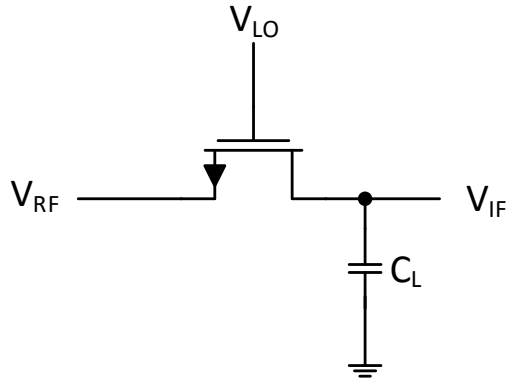

Figure 3.9: Non-return-to-zero mixer.

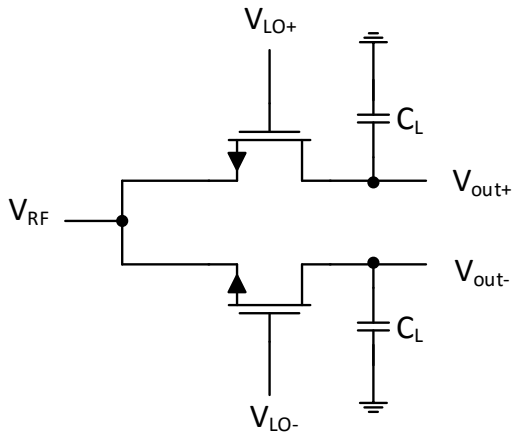

Figure 3.10: Single-balanced non-return-to-zero mixer.

The double-balanced variant, however has no gain improvements when swapping the resistors with capacitors, because the capacitors much like the resistors play no role, since each output is equal to one of the inputs, at any point in time. This means the gain is about 5.5 dB lower than the NRZ single-balanced counterpart.

Noise

Now that the simple and single-balanced topologies, either RZ or the NRZ variant have been introduced, let's take another look at input referred noise of each topology. The input-referred noise of a RZ mixer is

$$\overline{V_{in}^2} = 2\pi^2 kT[(R_{on} \parallel R_L) + R_L]\,, \tag{3.23}$$

where R_{on} is the on-resistance of the device and R_L the load resistance value. Usually $R_{on} \ll R_L$, thus we have

$$\overline{V_{in}^2} = 2\pi^2 kTR_L \approx 20kTR_L\,. \tag{3.24}$$

If correctly designed the on-resistance of the switch plays no part in the noise figure of the mixer, although any load resistance ($4kTR_L$) when input referred has its noise power amplified by a factor of 5 [p. 358][24]. The NRZ counterpart, where the load resistors were swapped for load capacitors, has the following expression for the input-referred noise

$$\overline{V_{in}^2} = kT\left(11.12R_{on} + \frac{2.85}{2C_L f_{LO}}\right), \tag{3.25}$$

however the single-balanced variant has a conversion gain twice as high, which means the input-referred noise will be reduced by a factor of 2, thus the input-referred noise for the single-balanced NRZ mixer is

$$\overline{V_{in}^2} = kT\left(5.54R_{on} + \frac{1.48}{2C_L f_{LO}}\right), \tag{3.26}$$

meaning that the weight of the on-resistance of this switch in the single-balanced counterpart is half of the NRZ mixer.

A lower noise value and a value for the CG higher than unity, on a passive device, make the passive single-balanced non-return-to-zero mixer an extremely attractive choice for the AFE.

3.3 Trans-Impedance Amplifier

When working with mixers that operate with "signal currents", a device is needed to convert the current to a voltage signal. This device is called a Trans-Impedance Amplifier (TIA), implemented with an Operational Amplifier (OpAmp), as shown in figure 3.11.

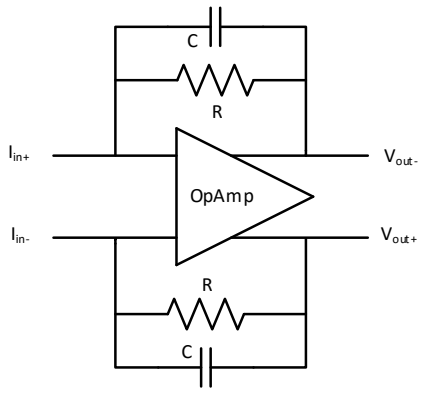

Figure 3.11: Transimpedance amplifier circuit.

The chosen topology was a two-stage OpAmp, illustrated in figure 3.12. The first stage of the OpAmp is a common-source folded cascode that excels at providing a high voltage gain, over 60 dB, and a high output impedance. A high voltage gain is indeed needed of the OpAmp, since through the Miller effect the input resistance is divided by the voltage gain, after closing the loop and a low input resistance is important for the TIA to convert a

signal from the current to the voltage domain. The second stage is a simple common drain stage, with a gain close to unity, whose main objective is to lower the output impedance of the TIA, while maintaining a high gain. Thus the first stage accommodates the OpAmp gain, while the second one servers as a buffer. In the first stage the PMOS transistors M_{10}, M_{11}, M_3 and M_4, create a cascode configuration to increase output impedance, the NMOS transistors M_5, M_6, M_7 and M_8, have the same objective as the PMOS counterparts.[2]

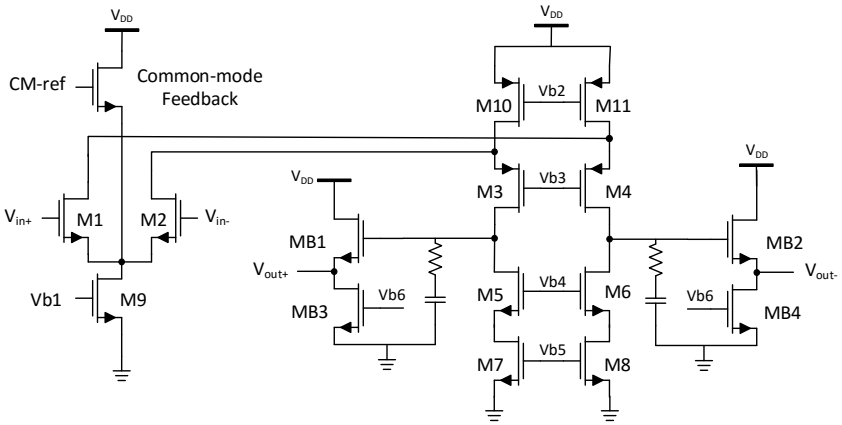

Figure 3.12: Operational amplifier circuit.

Common Mode Voltage

The common mode voltage is maintained by the Common-Mode Feedback (CMFB), which is a single transistor. The CMFB device's gate is connected to the common-mode voltage reference and its source is connected to M_1 and M_2's sources, the OpAmp input common node. Implementing a CMFB with a just a single transistor is only possible because the inputs and outputs of the OpAmp share the same common-mode voltage, owing to the fact that there is no Direct Current (DC) flowing through the *RC* feedback network [28].

Although this technique to maintain common mode voltage with a single transistor is a very simple and efficient method, it is also an open-loop implementation, which means that if the OpAmp while operating abandons the common mode voltage, it doesn't have a feedback in order to readjust itself. Thus, the open-loop single transistor method was abandoned in favour of a tried and true feedback circuit to maintain the common mode reference voltage illustrated in figure 3.13.

This circuit works as follows, since the TIA is differential two resistors were connected to each output and signal sensed between them is fed back into a the negative port of a simpler OpAmp with a lower gain, and the reference voltage into the positive port. The output of this common mode OpAmp is connected to the current source which in turn adjusts the common mode voltage, through its current.

[2]The reason why a high output resistance is desirable is explained below when computing the voltage gain.

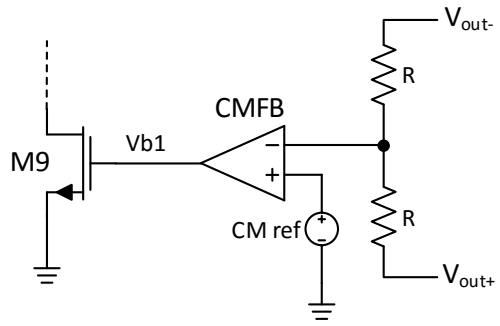

Figure 3.13: Common-mode feedback circuit.

Gain

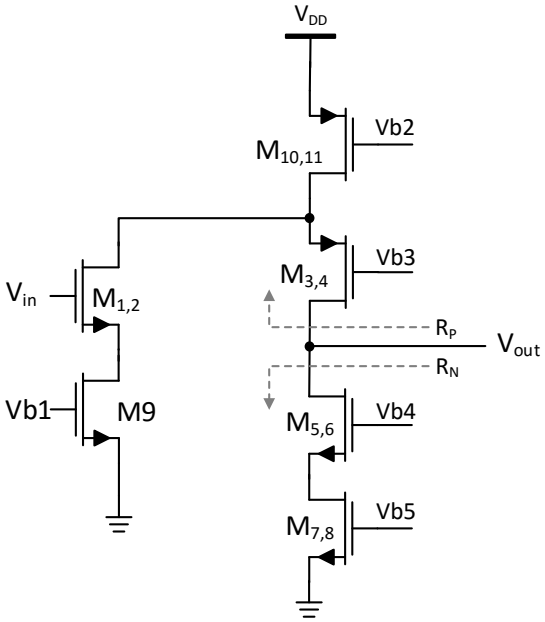

Figure 3.14: Simplified schematic of the OpAmp.

In order to compute the OpAmp's gain, a simplified model of the circuit was considered, as shown in figure 3.14, this is only possible due to the folded nature of the amplifier. The expression for the first stage of the OpAmp's DC gain, much like the LNA in section 3.1, is given by:

$$|Av| = \left|\frac{V_o}{V_i}\right| = gm_1 \times R_{out}\,, \tag{3.27}$$

where $R_{out} = R_P \parallel R_N$. These two impedances, represented in figure 3.14 are the cascode impedances of the PMOS and NMOS transistors, respectively. Thus $R_P = (R_{ds1} \parallel R_{ds10} \cdot$

$gm_3 R_{ds3}$) and

$$R_P = (R_{ds1} \parallel R_{ds10}) \cdot gm_3 R_{ds3}\,, \tag{3.28}$$

and

$$R_N = (R_{ds7}) \cdot gm_5 R_{ds5}\,. \tag{3.29}$$

Only the gain of the first stage has been calculated because, ideally the gain of the common-drain topology is unity. However the gain of the second stage, even if not exactly unity, won't impact the overall gain of the OpAmp, so a small drop of 1 to 3 dB is to be expected.

Gain-Bandwidth Product

Another important metric of an amplifier is the Gain-Bandwidth Product (GBW), the GBW is defined as the product between the open-loop gain, in this case $|Av|$ and the circuits' dominant pole f_o

$$GBW = |Av| \times f_o\,. \tag{3.30}$$

Since the circuits gain has been previously calculated, all that's left is to compute the circuits dominant pole, f_0 located in the output node, which is given by

$$f_o = \frac{1}{2\pi \cdot R_{out} \cdot C_{out}}\,, \tag{3.31}$$

where R_{out} has been calculated above in equations 3.29 and 3.28, and C_{out} is the total capacitance in the output node, given by

$$C_{out} = C_L + C_{db5} + C_{db3} + C_{gd5} + C_{gd3}\,, \tag{3.32}$$

where C_L is the load capacitance, and the rest of the capacitances are the transistors M_3 and M_5 drain-bulk and gate-drain parasitic capacitances. The GBW expression in 3.30 can be simplified into

$$GBW = \frac{gm_1}{2\pi \cdot C_{out}}\,. \tag{3.33}$$

In-between the common-gate cascode stage and the common-drain stage there is a RC series that cannot be ignored, because it serves as a frequency compensator, through its values the circuits' dominant pole f_o can be adjusted, modifying the phase margin and GBW as needed.

3.4 Switched-Capacitor Vector Modulator

The objective of the switched-capacitor vector modulator is to perform the phase shift and amplitude control in the phased-array antenna in order to achieve spatial selectivity, in other words, the beamformer itself.

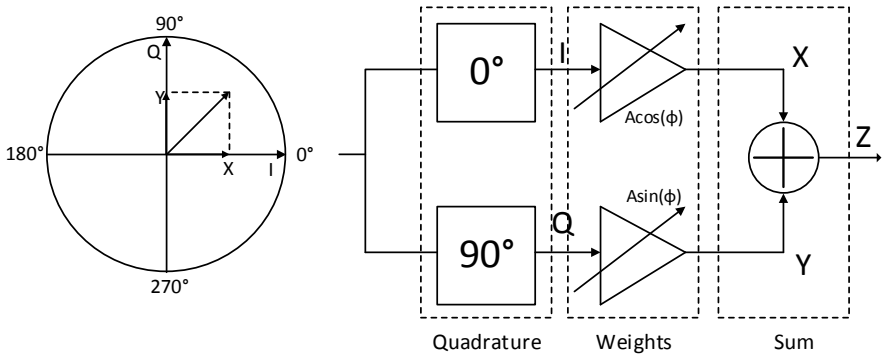

Figure 3.15: Vector modulator principle.

The way this phase shifter operates is through vector modulation, in order to better understand this concept consider the following equation

$$\sin(\omega t + \phi) = \sin(\phi) \times \cos(\omega t) + \cos(\phi) \times \sin(\omega t)\,, \tag{3.34}$$

where a signal with phase ϕ is de-constructed into a sum of two parts: (1) a signal with no phase shift "$\sin(\phi) \cdot \cos(\omega t)$" and (2) a signal with a 90° phase shift "$\cos(\phi) \cdot \sin(\omega t)$". Figure 3.15, illustrates this decomposition, in the real and imaginary axis. A vector to a point Z in the phasor diagram corresponds to the sum of a real (X) and an imaginary (Y) part, thus

$$\begin{aligned} \vec{Z} &= X + jY \\ X &= I \cdot A\cos(\phi) \\ Y &= Q \cdot A\sin(\phi) \end{aligned} \tag{3.35}$$

X and Y, are defined as the scaled version of the I (In-phase) and Q (Quadrature), respectively, of the input signal. In practice, there are three steps to apply vector modulation to the input signal: (1) generate an in-phase and quadrature version of the signal, (2) apply the weights (phase and amplitude) to obtain X and Y, (3) sum X and Y to obtain Z, the phase shifted signal.

Since the signal has to be downconverted from RF to IF, one way to approach the I and Q signal generation is to move the phase shifting and amplitude scaling into the IF domain, and utilize a downconversion mixer topology that provides both in-phase and quadrature signals, much like the single-balanced and double-balanced topologies, presented in section 3.2. This is only possible since, the phase shift required for beamforming can be moved from the RF domain into th IF domain without affecting the beam pattern [14]. Looking at the phase diagram in figure 3.15, it is apparent that negative I an Q signals are mandatory in order to achieve full 360° phase shifting range. These are obtained by interchanging differential signal lines.

Sine/Cosine Generation

It's been established that both sine and cosine functions need to be implemented in order to perform the signal phase shift and that uniform steps are preferred. There are multiple ways to implement such functions, the most common topologies use uniform steps, but one must be cautious because the pretended weight points may fall in-between such steps, decreasing accuracy. On the other hand if too many uniform steps are used to implement the vector modulator weights, some may remain unused, decreasing efficiency.

The approach adopted in this thesis was to produce non-uniform steps that mimics the sine and cosine functions, all the while producing uniform steps in phase. The transfer function used for this purpose was

$$\sin\left(\alpha \cdot \frac{\pi}{2}\right) \approx \frac{7}{4} \cdot \frac{\alpha}{\alpha + 3/4}, \tag{3.36}$$

where $\alpha = [0, 1]$, this range of α corresponds to a phase shift range of $0°$ to $90°$. The $3/4$ factor in the denominator was chosen in order to adjust the crossover point half way, to improve approximation. The $7/4$, on the other hand, was introduced to correctly scale the gain of the transfer function for $\alpha = 1$. To prove that this is a valid approach, in figure 3.16, comparing the sine and approximated sine responses one can reach the conclusion that it is indeed a rather acceptable approximation.

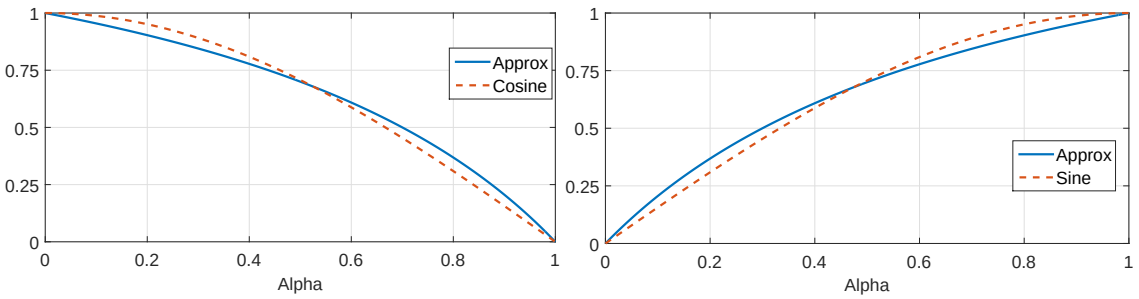

Figure 3.16: Comparison between the sine and cosine functions and the approximated transfer function.

In order to create a transfer function to approximate the cosine function, one must simply remember that

$$\cos\left(\alpha \cdot \frac{\pi}{2}\right) = \sin\left(\frac{\pi}{2} - \alpha \cdot \frac{\pi}{2}\right) = \sin\left((1-\alpha) \cdot \frac{\pi}{2}\right), \tag{3.37}$$

thus combining 3.36 and 3.37 yields

$$\cos\left(\alpha \cdot \frac{\pi}{2}\right) \approx \frac{7}{4} \cdot \frac{(1-\alpha)}{(1-\alpha) + 3/4}. \tag{3.38}$$

The comparison of this transfer function and the cosine is also shown in figure 3.16.

Vector Modulator Implementation

A big advantage of this approximation is that it can be implemented with a 2-phase switched-capacitor circuit, as shown in figure 3.17. In phase one the αC capacitor is charged with a voltage V_{in}, thus $Q_1 = \alpha C \cdot V_{in}$, and also the fixed capacitor $3/4C$ is discharged to ground. In phase two charge redistributes itself in order for the voltages in the capacitors to be equal. So the charge in the second phase is $Q_2 = (\alpha C + 3/4C) \cdot V_{out}$. Through the law of charge conservation $Q_1 = Q_2$, yielding

$$\alpha C \cdot V_{in} = (\alpha C + 3/4C) \cdot V_{out} \Leftrightarrow \frac{V_{out}}{V_{in}} = \frac{\alpha C}{(\alpha C + 3/4C)} \Leftrightarrow \frac{V_{out}}{V_{in}} = \frac{\alpha}{\alpha + 3/4}. \tag{3.39}$$

An important observation of the last equation is that it only depends on the value of α, as long as the capacitor ratios are accurately defined which in IC they usually are. Thus a uniform step in α corresponds to a uniform step in phase and also a uniform step in capacitance. As was previously demonstrated, in the beginning of this section, the X and Y vectors need to be summed in order to obtain Z, the phase shifted signal, given by equation 3.35. This is done is by connecting the X and Y terminals, because since the circuit operates with two phases, the signal present at Z will either the X or Y, the purpose of the capacitor C_Z is to serve as a LPF, effectively averaging the X and Y signals, this capacitor has the value of $3/8C$ to reach a trade-off between phase and gain error.

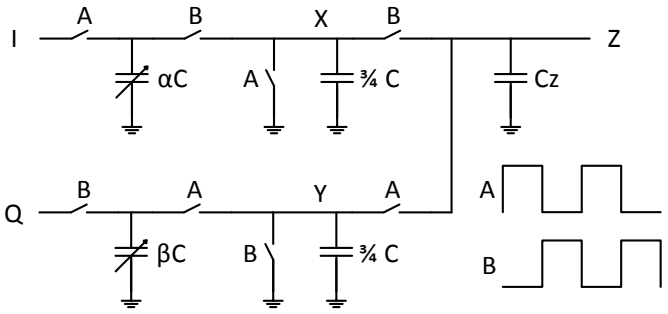

Figure 3.17: Sine an cosine approximation circuit.

It was stated above that a uniform step in α corresponds to a uniform step in capacitance. This last sentence leads to an interesting conclusion, since capacitance steps are uniform, a simple capacitor bank is more than enough to implement the α-variable capacitors, as illustrated in figure 3.18. With three bits to control the capacitor bank, each quadrant is divided into 8 equal parts, which means a minimum phase step of $\Delta\theta = 90^\circ/8 = 11.25^\circ$, and in order to avoid overlap of quadrants in the real and imaginary axes, the capacitors are quantized between $1/16C$ and $15/16C$. Thus with three bits $b_0b_1b_2 = 000 \Rightarrow \alpha = 1/16 \Rightarrow \phi = 5.625^\circ$ and $b_0b_1b_2 = 111 \Rightarrow \alpha = 15/16 \Rightarrow \phi = 84.375^\circ$. The other 3 quadrants are obtained with a sign selection circuit at the output of the mixer, by interchanging the differential signal outputs [14]. One conclusion is that the more bits we have at our disposal the more accurate the phase shifter is.

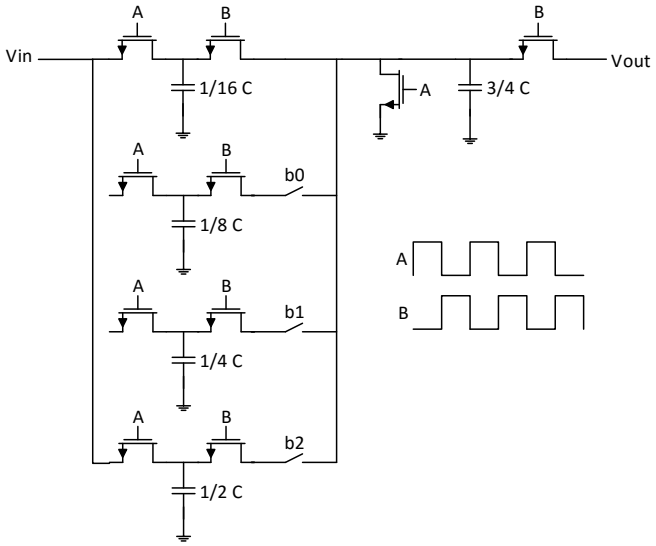

Figure 3.18: Variable capacitor implementation.

The amplitude control required for the null steering mentioned in section 2.1.3, is implemented by simply multiplying the amplitude A with both α and β, yielding:

$$\begin{aligned} \alpha &= A \times \left(\phi \cdot \frac{2}{\pi} \right) \\ \beta &= A \times \left[(1-\phi) \cdot \frac{2}{\pi} \right] \end{aligned} \tag{3.40}$$

Calculating the effect of null steering is a rather hard task, but there is a way to estimate the worst-case scenario, when it is required to insert a null in the direction of a grating lobe. There is a straight connection between the quantization and side lobe levels [29], the equation that estimates the difference off heights between the main beam and the grating lobe QL in dB is given by

$$QL \approx 6 \cdot N_{bit} - 4\,, \tag{3.41}$$

where N_{bit} is the number of bits in the phase shifter. The vector modulator implemented in this thesis, has a 5 bit phase quantization, which through 3.41 yields a rejection of $5dB$.

Since the switches used in the phase shifting circuit are implemented in CMOS technology, special attention is required when choosing their size. Because as was stated in section 3.2, through equation 3.20, the parasitic capacitance of the transistors is directly proportional to their size. This parasitic capacitance can destroy the charge redistribution and alter the pretended transfer function explained above. Thus one of two methods can be applied: (1) scale the transistor's size with the capacitor sizes, in order to maintain the same capacitance ratio or (2) design the switches to minimize the parasitic capacitances in order for them to be negligible.

3.5 GM-Stage

In the RF domain, the LNA accommodates the AFE's low noise and gain, as well as input-matching, the mixer generates the I and Q signals and in the IF domain the switched-capacitor vector modulator, performs phase shifting, all that's left is to sum the signal elements as the last step of beamforming. Summing can be done either in the current or voltage domain, although according to Kirchhoff's rules summing in the voltage domain, requires a loop where the voltages are stacked, meaning that the more elements the phased-array has the higher the output voltage, but since there's a limited supply voltage of 1.2 V, this heavily restricts summing in the voltage domain.

On the other hand summing in the current domain is done by simply connecting all the nodes together. Since the phase shifting is accomplished in the voltage domain, the output of the vector modulator needs to be converted into a current signal. This is achieved through a Gm-stage, of figure 3.19, after summing,the output of this stage is then re-converted into a voltage signal through the load resistors R_{Load}. Computing the gain of this block is rather easy and it's given by

$$Av_{=}gm_{1,2} \times R_{Load}\,. \tag{3.42}$$

Special attention must be paid to the value of R_{Load}, because since there is a current source, I_s, the load resistor will also create an offset voltage proportional to the said current, which is $V_{offset} = I_s \cdot R_{Load}$. Thus in a circuit such as this these resistors usually have a rather low resistance value of a couple hundred Ohms.

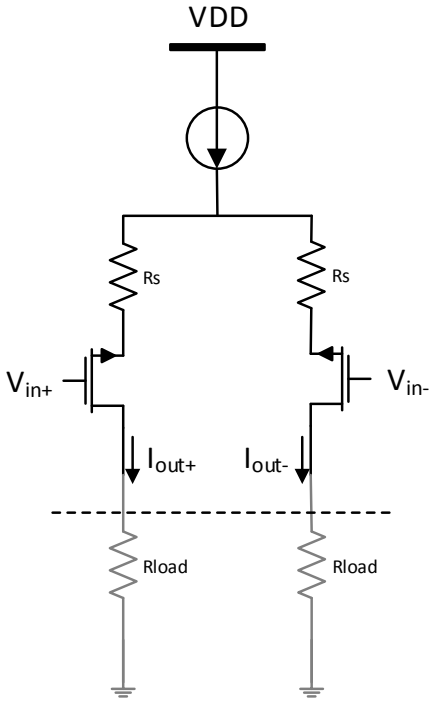

Figure 3.19: Gm-stage circuit.

A big advantage of current summing is that the output has a fixed voltage, regardless of the number of antenna elements. Furthermore, since all the R_{Load} resistors are connected in parallel, having a higher number of elements means that the total output impedance is lowered. Loosely speaking, it's as if the signals were being averaged instead of summed. This unlimited scalability in the number of elements, makes this approach quite attractive and the one adopted in this thesis.

3.6 Radio Frequency Filters

The filter in RF is an extremely important block, since the growth of wireless communications lead to limitations in the frequency spectrum. Thus, the carries' frequencies used to transmit information often lie close to each other, this leads to a higher number of interferers, near the frequency band of interest that need filtering. As the frequencies lies closer and closer to each other, a higher performance of the filters is required, this performance is measured through its quality factor, Q factor[3].

Filters implemented off-chip usually offer higher values of Q than their on-chip counterparts, with a trade-off that on-chip filters are cheaper and occupy a smaller area, with CMOS technology. Still there are a couple of techniques that can be used in order to augment the Q factor of on-chip filters but these usually degrade the linearity and noise [30]. When implemented either on or off-chip, a high-Q filter requires high-Q components, in order to achieve a high performance [31].

In this thesis a filter is required in the final part of the receiver, after the element summing, to filter the higher frequencies and conserve the IF signal as much as possible. There are two major possibilities, either a LPF or a Band-Pass Filter (BPF).

Band-Pass Filter

One of the filter possibilities that could be implemented is the BPF, that singles out a frequency band, rejecting all other frequencies, the frequency response of such a filter is shown in 3.20.

In order to analyse the performance of a BPF the above mentioned quality factor or Q factor can be determined through the next equation

$$Q = \frac{\omega_0}{BW}, \tag{3.43}$$

where ω_0 is the filter centre frequency, and BW the bandwidth, it is defined as $BW = \omega_2 - \omega_1$, the frequencies where the voltage magnitude falls $3dB$ below the maximum value. Figure 3.20 serves as a visual aid, where these values are illustrated. In conclusion, the higher the Q value, the sharper the filter will be, thus the better it's performance.

[3]Not to be mistaken with the inductor quality factor of equation 3.7 explained in 3.1.

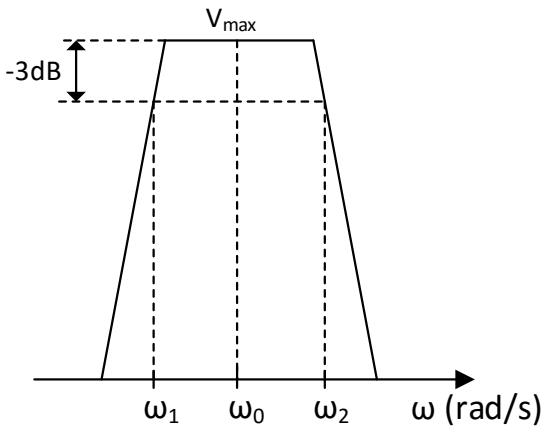

Figure 3.20: BPF frequency response.

Low-Pass Filter

Another type of filter and the one adopted in this thesis is the LPF, this filter is designed to block the frequencies that lie higher than the frequency of interest. The simplest way to implement such a filter is through a simple *RC*-circuit, defined as a 1st order LPF, as shown in figure 3.21.

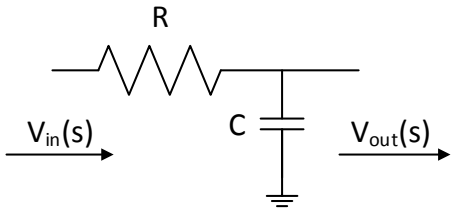

Figure 3.21: LPF circuit.

To evaluate this filter's behaviour let's start by determining its transfer function. Applying the Kirchhof Current Law (KCL), yields

$$\begin{aligned} \frac{V_{in}(t) - V_{out}(t)}{R} &= \frac{V_{out(t)}}{Z_C} \\ Tf(s) = \frac{V_{out}(t)}{V_{in}(t)} &= \frac{Z_C}{Z_C + R}, \end{aligned} \tag{3.44}$$

where Z_C is the capacitor impedance given by $Z_C = 1/sC$ substitution in 3.44, gives

$$Tf(s) = \frac{1/sC}{1/sC + R} = \frac{1/RC}{s + 1/RC}. \tag{3.45}$$

Plotting 3.45, yields the LPF's frequency response, figure 3.22, where the circuits only pole $p_1 = 1/RC$ controls the cut-off frequency ω_f, the point after which the gain will decrease

20 dB/decade. Analysing the LPF frequency response, its easy to denote that only the higher frequencies are filtered, as explained above.

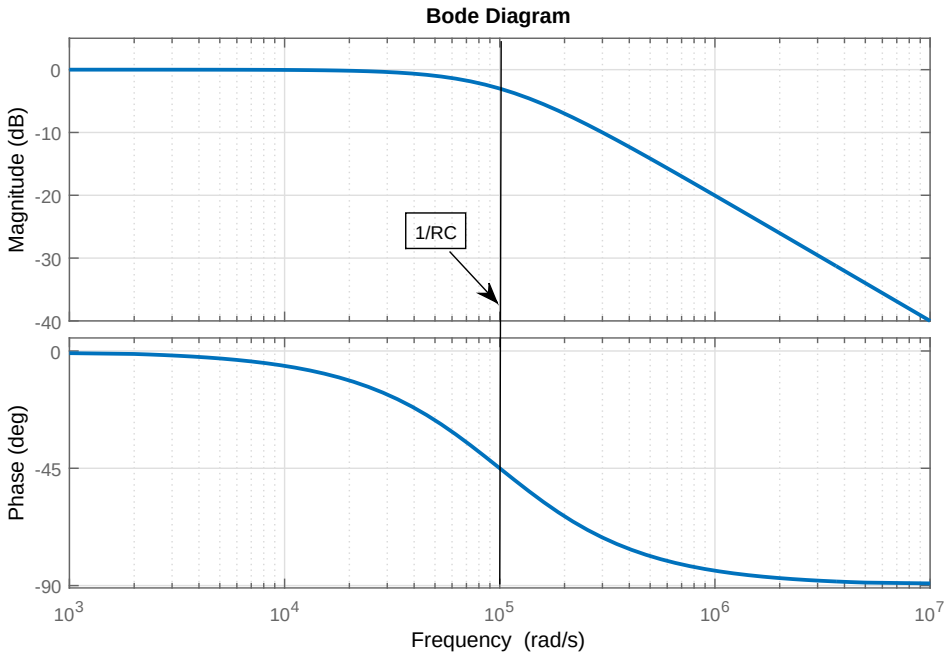

Figure 3.22: LPF frequency response.

Unlike the BPF, there is no definition for a 1st order LPF Q factor, because Q is inversely proportional to the system's damping, and a 1st order LPF only has one real pole, since real poles have the highest damping factor, the Q of the RC filter is the "lowest possible". In other words, this topology does not have a very high performance, on the other hand, it's very easy to implement and has a low power and area usage. Thus, it was the topology used in this thesis since the most troublesome frequencies that need filtering, lie higher in the frequency spectrum.

CHAPTER 4

BEAMFORMING RF FRONT-END SIMULATION AND RESULTS

The previous chapter introduced the equations and some concepts that were taken into account when designing the receiver. In this chapter the simulation and results of each of the receiver's blocks will be presented, as well as the whole receiver. The RF of the AFE is 1 GHz, the LO frequency is 990 MHz, which leaves us a IF of 10 MHz. The circuits were implemented in 130 nm CMOS technology, the transistor models used to simulate the receiver were the *"BSIM3V3"*.

4.1 Low-Noise Amplifier

The low-noise amplifier, illustrated in figure 4.1, was designed with a few characteristics in mind for example gain, impedance matching and noise figure. With this in mind the following sizes for the transistors were obtained:

Table 4.1: LNA transistor size parameters.

Transistor	Width (μm)	Length (nm)	Fingers	Current (mA)	Region
M_1 (NMOS)	115	130	16	1.3	Saturation
M_2 (NMOS)	115	130	16	1.3	Saturation
M_3 (PMOS)	82	200	10	1.3	Saturation

The transistors were kept in the saturation region of operation, in order to increase the gm of transistor M_1 ($gm_1 \approx 19$ mS), the current I_d, was also adjusted to increase the transconductance of M_1 and at the same time try not to push the static power consumption of the LNA. The adopted channel-length L of the cascode transistors, M_1 and M_2, was the minimum possible, in order to reduce the parasitic capacitances and have the maximum available switching speed. Since M_3 is a current source, its L was slightly increased to

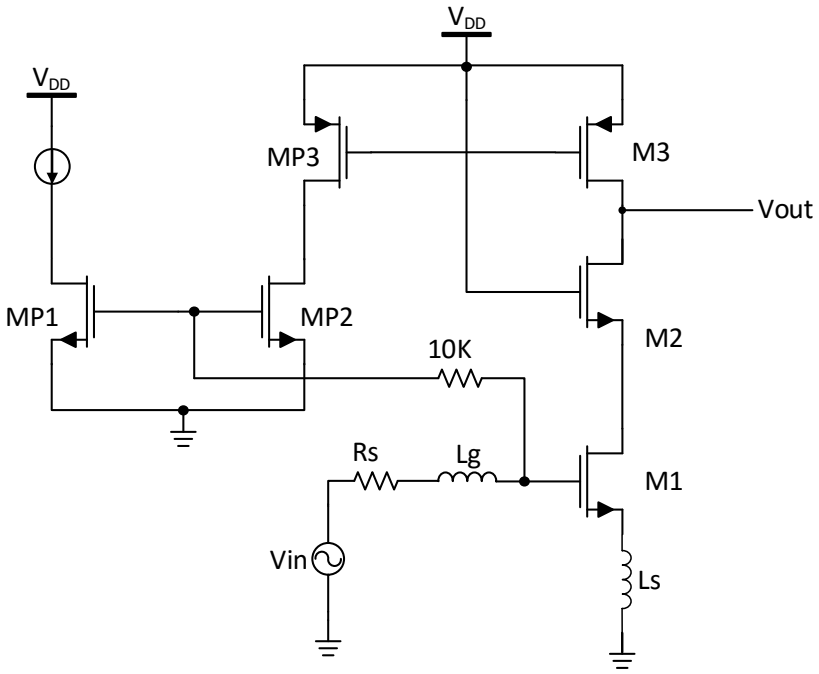

Figure 4.1: LNA circuit.

increase the output resistance. The channel-width was only chosen in order to maximize gm_1.

In accordance to equations 3.6 and 3.5 in section 3.1, the circuit's inductors were calculated and, through simulation, adjusted. The inductance values obtained were: $L_g = 40.729$ nH and $L_s = 2.712$ nH. In order to prove that the the LNA was correctly input-matched, two simulations were performed, the LNA input resistance and S_{11}.

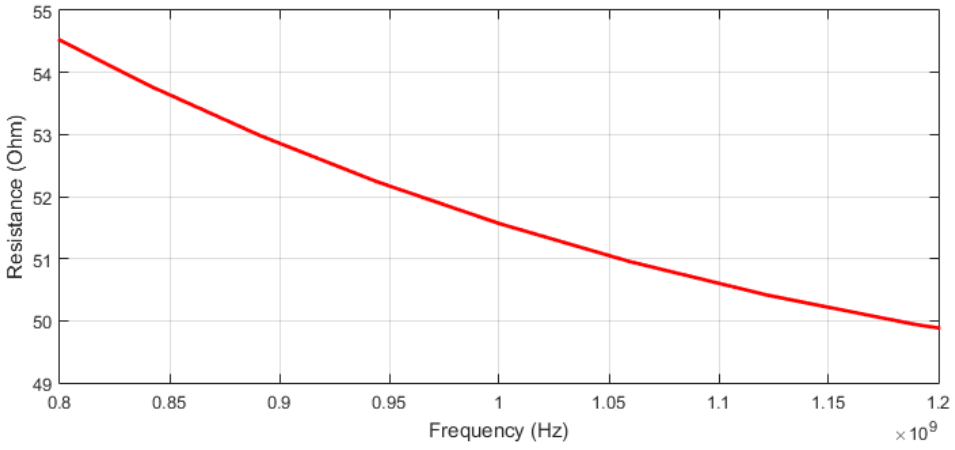

Figure 4.2: Plot of the input resistance of the LNA.

In figure 4.2 one can denote that the input resistance of the LNA is $R_{in} \approx 51.5\ \Omega$, this value although not exactly equal to the antenna's assumed output resistance of 50 Ω is still

a good value. To validate the previous statement the S_{11} was plotted in figure 4.3, where it yielded a value of $S_{11} < -31$ dB, this proves that the LNA was properly input matched.

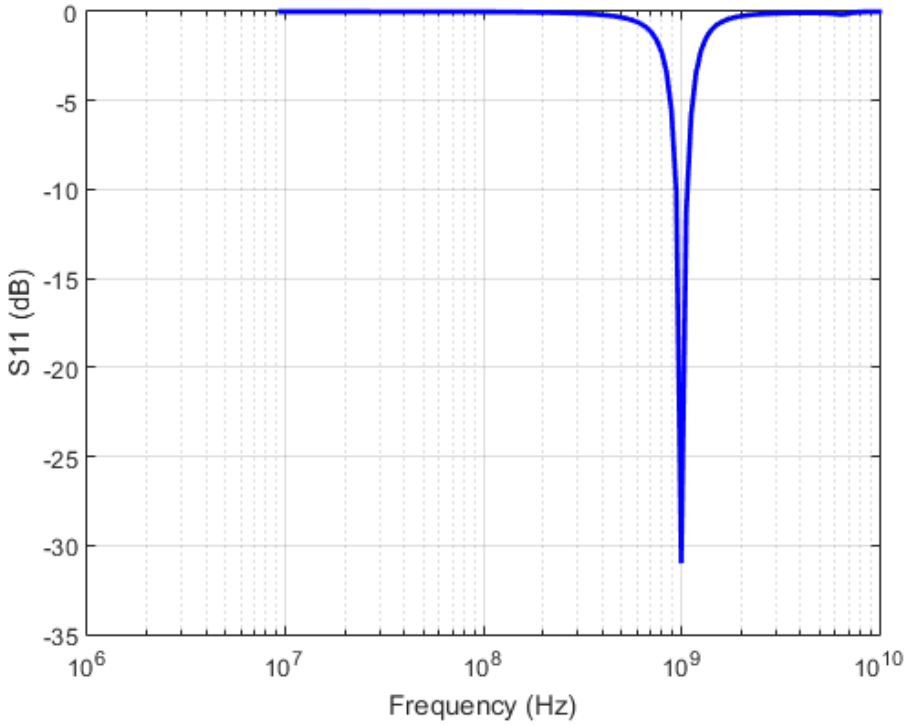

Figure 4.3: Plot of the S_{11} of the LNA.

Now that the input impedance has been analysed the next step is to evaluate the LNA's gain, thus an AC simulation was performed its result presented in figure 4.4. In figure 4.4 one can denote that the gain of the LNA is a bit over 23 dB, a reasonable value. The shape of the AC response is typical narrowband response with a spike in the working frequency of $f_{RF} = 1$ GHz. Lastly the noise figure of this device was simulated, the result is plotted in 4.5.

The value of noise figure achieved in the LNA is of about 2.2 dB at 1 GHz, a relatively low value of noise. This level of noise is as predicted in 3.1, where it was stated that the LNA noise contribution is usually between 2 and 3 dB.

In order to analyse the LNA's linearity the 1dB-compression point simulation was ran, yielding the results illustrated in figure 4.6, achieving a value of -18.5 dBm, a rather low value, meaning that the LNA might reach saturation given a strong enough input signal.

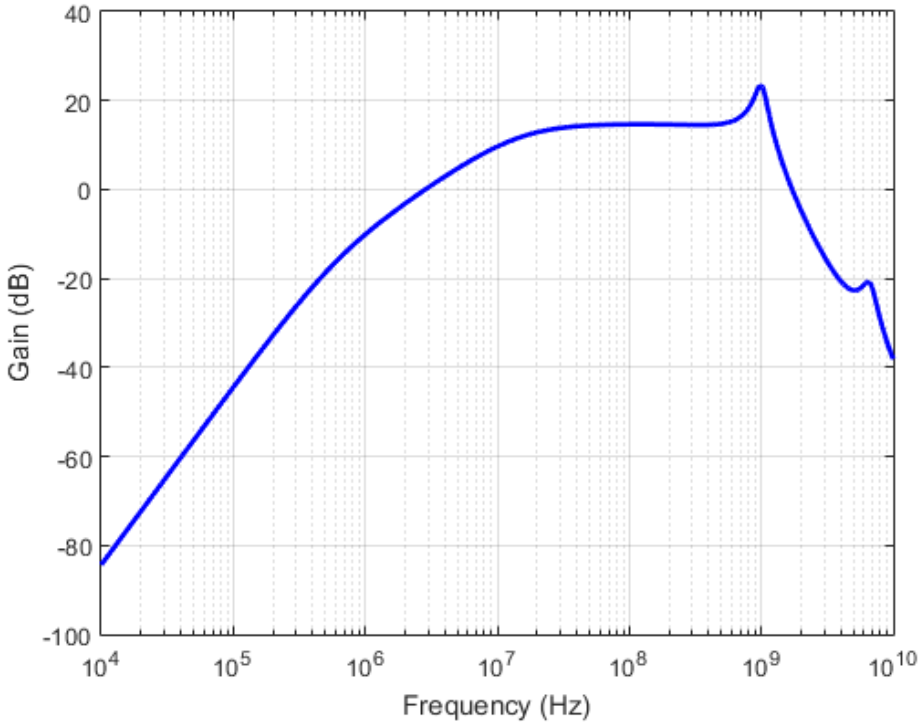

Figure 4.4: Plot of the gain of the LNA.

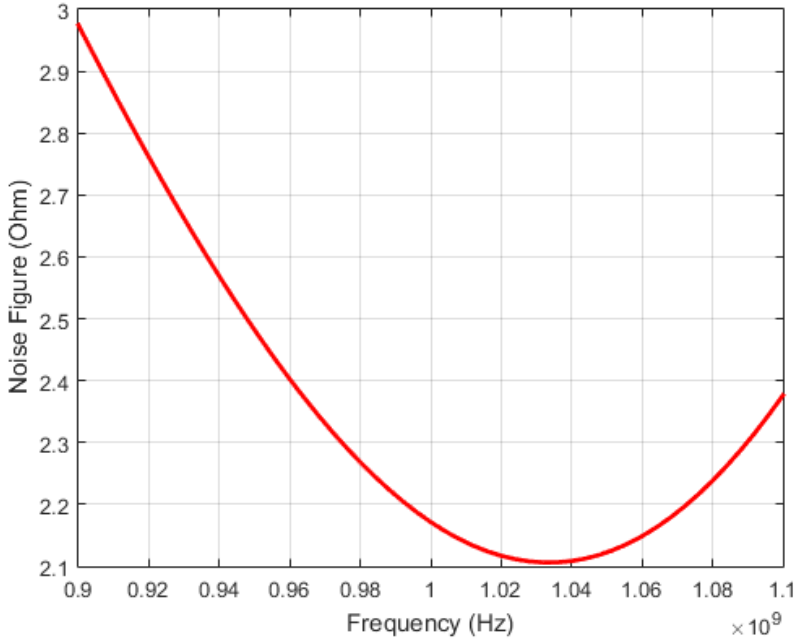

Figure 4.5: Plot of the noise figure of the LNA.

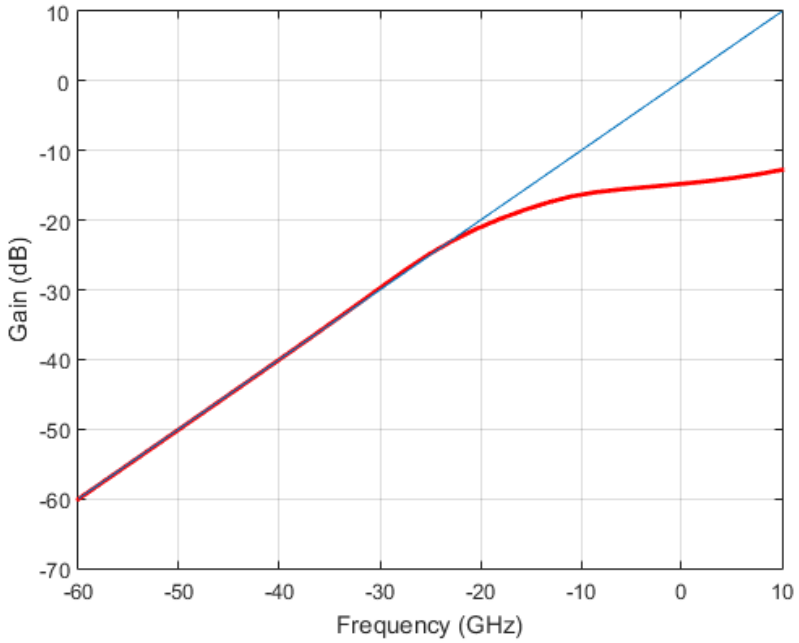

Figure 4.6: P_{1dB} simulation of the LNA.

4.2 Mixer

In the adopted mixer topology, shown in figure 4.7, the switches were implemented with NMOS transistors. Their sizes were adjusted in order to decrease their resistance, R_{ds}, because the channel width of the transistor is inversely proportional to the resistance. Nevertheless, special attention must be paid because larger transistors are costly area-wise and also the parasitic capacitance rises proportionally to the transistor's size. Channel length was kept at $L_{min} = 130$ nm for maximum switching speed. Table 4.2 presents the switches dimensions.

Table 4.2: Mixer's switches' size parameters.

Transistor	Width (μm)	Length (nm)	Fingers	R_{ds} (Ω)
$Sw_{1,2,3,4}$ (NMOS)	100	130	10	5.5

After achieving a low enough resistance, in this case $R_{ds} = 5.5\ \Omega$. The next step was to find the conversion gain of the mixer. With this in mind, the voltage spectrum was analysed to find the voltages of the pretended input and output frequencies, in this case, RF (1 GHz) and IF (10 MHz), respectively. The results are shown in figure 4.8 for the input and figure 4.9 for the output.

In figure 4.8 one can observe that the voltage at $1GHz$ is of $V_{1GHz} = -40$ dB and in figure 4.9 $V_{10MHz} \approx -42$ dB, through equation 3.21 explained in 3.2, the conversion gain

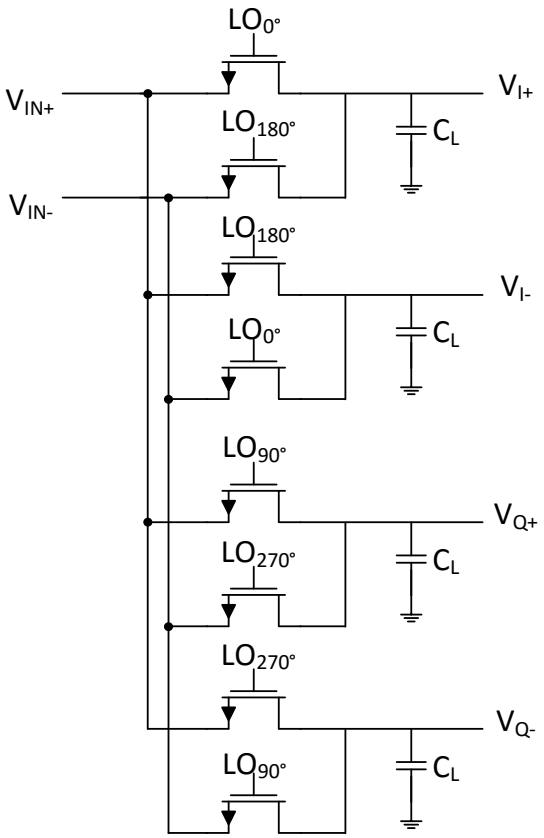

Figure 4.7: Implemented mixer topology.

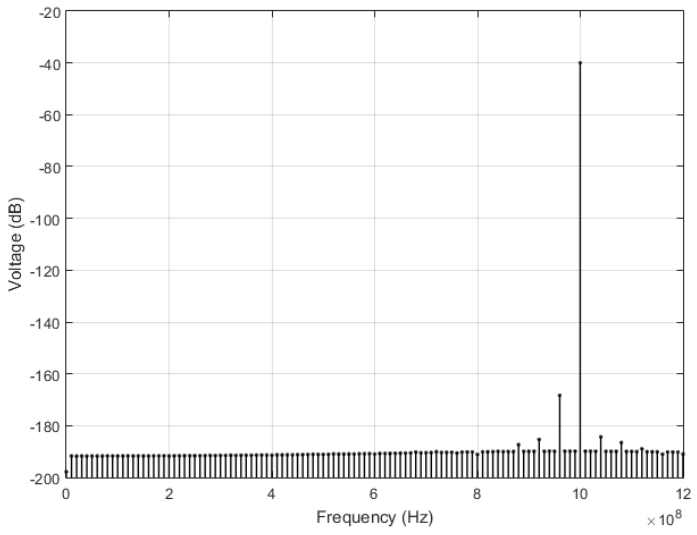

Figure 4.8: Voltage spectrum of the mixer input.

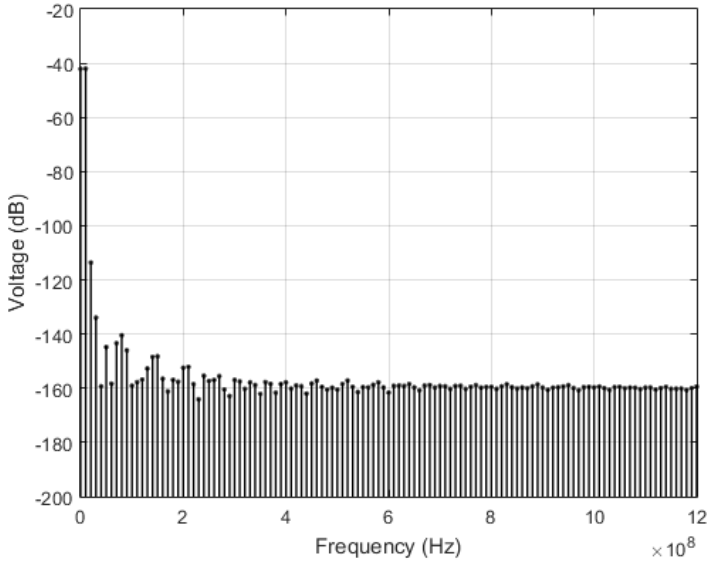

Figure 4.9: Voltage spectrum of the mixer output.

is given by:

$$CG|_{dB} = 20\log\left(\frac{V_{IF}}{V_{RF}}\right) \Leftrightarrow CG|_{dB} = -42 - (-40) = -2dB\,. \tag{4.1}$$

Although not exactly the theoretical value, it's still an good result.

The last step in the mixer design was to simulate the noise figure of the device, thus a noise simulation was ran, yielding the results illustrated in figure 4.10, where a value for NF of 3.5 dB can be observed. This result is slightly below the window of predicted values in 3.2, which means that the designed mixer has a considerably low noise value.

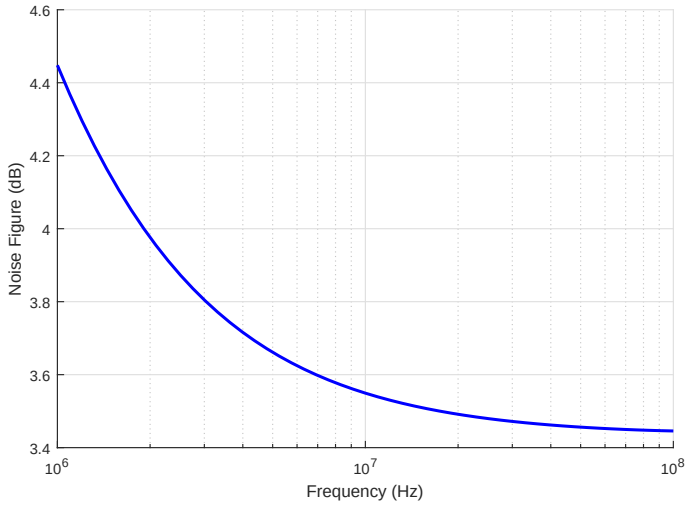

Figure 4.10: Noise figure plot of the mixer.

4.3 Transimpedance Amplifier

The transimpedance amplifier was designed according to the explanation of section 3.3, and the OpAmp topology is illustrated in figure 4.11. A quick comparison with the schematic presented in 3.3, reveals that the first transistors of the OpAmp, the input transistors M_1 and M_2 were swapped from NMOS to PMOS, because PMOS transistors suffer a lot less from flicker noise than the NMOS counterparts. Another change made to the initial design that only revealed itself meaningful during simulation was the second stage of the OpAmp. Initially the OpAmp would incorporate a common-drain stage to decrease the output impedance of the amplifier, while trying not to interfere with the transimpedance gain. This second stage proved to be noisy and was dropped.

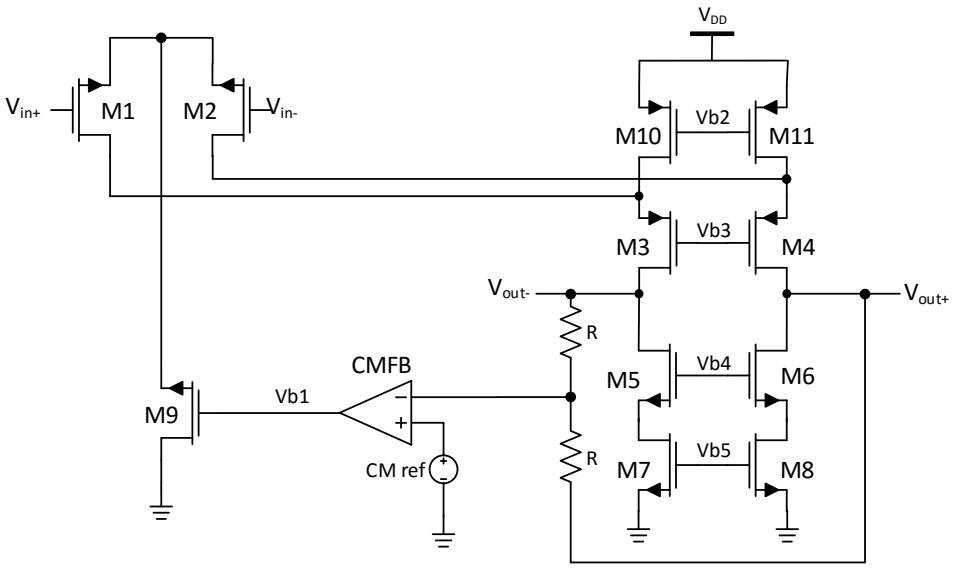

Figure 4.11: Implemented OpAmp circuit.

The OpAmp's transistors' dimensions and DC operating point are listed in table 4.3.

Table 4.3: OpAmp transistor size parameters.

Transistor	Width (μm)	Length (nm)	Fingers	Current (nA)
$M_{1,2}$(PMOS)	200	360	20	426
$M_{3,4}$(PMOS)	52	360	6	558
$M_{5,6}$(NMOS)	10	360	2	558
$M_{7,8}$(NMOS)	9	1000	2	558
M_9(PMOS)	100	1000	10	852
$M_{10,11}$(PMOS)	90	1000	9	984

After assuring the correct DC operating point for the TIA, the output signal was analysed in order to ascertain if the common-mode feedback was successfully maintaining the reference voltage of 600 mV.

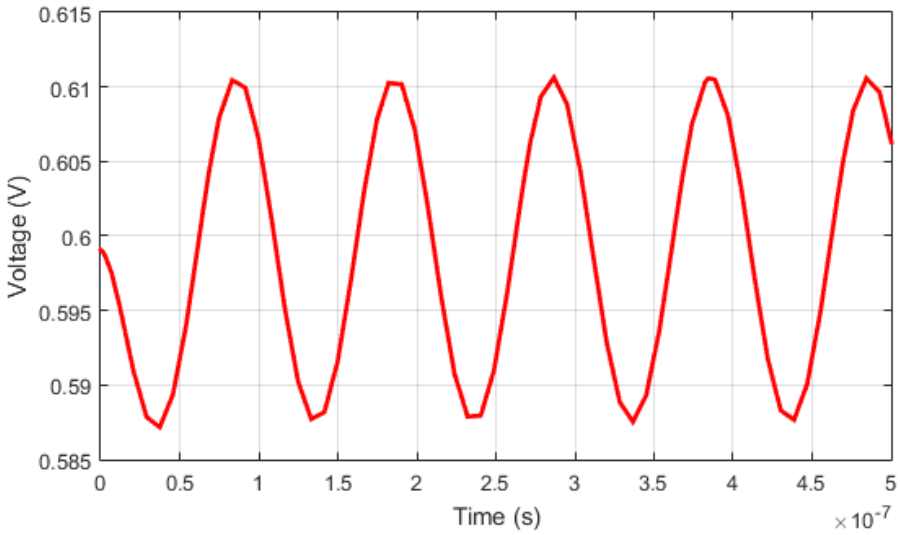

Figure 4.12: TIA time response.

As illustrated in figure 4.12, the output signal is indeed centred at 599 mV, which leads to the conclusion that the common-mode feedback circuit was successfully implemented.

The next simulation to be performed was the transimpedance gain and phase of the amplifier, 4.13.

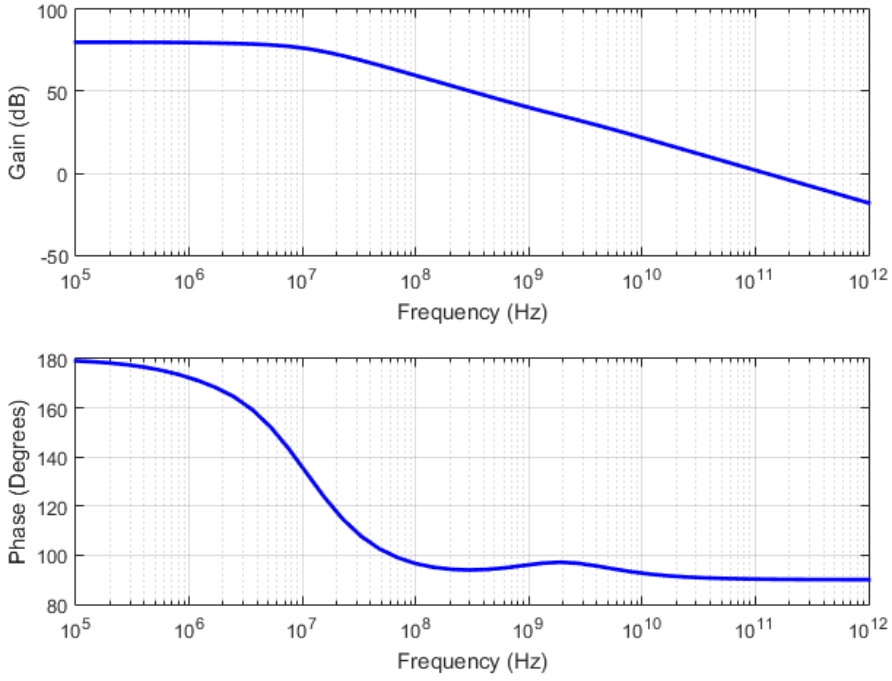

Figure 4.13: TIA gain and phase.

According to figure 4.13 the gain was of 83 dBΩ[1], since there is a pole at IF (10 MHz) the gain decays 3 dB and the TIA LPF-like frequency response filters the higher frequencies. In the phase diagram a 90° phase margin can be found, which means that the TIA is highly stable.

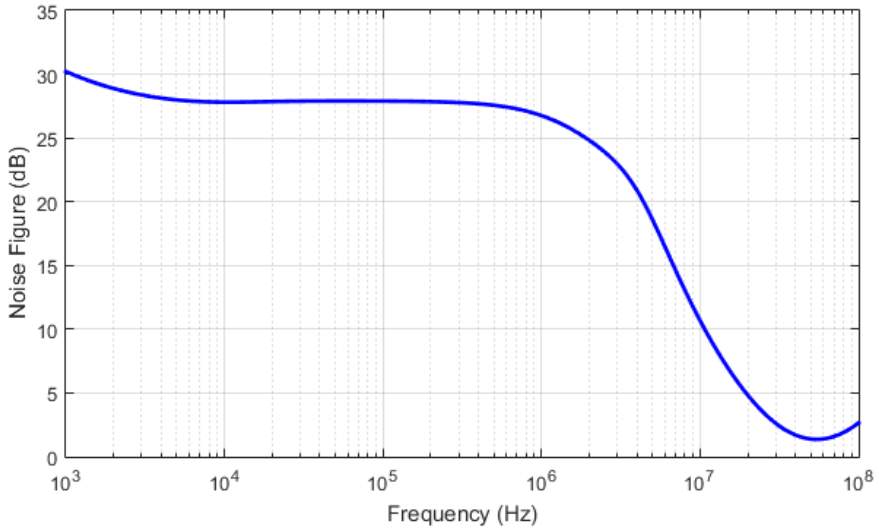

Figure 4.14: TIA noise figure.

The last simulation for the TIA was the NF, illustrated in figure 4.14, as mentioned above the TIA was very noisy during the early stages of design to a point where the very circuit had to be drastically altered. The initial value for the noise figure of the TIA was of about 40 dB, but after the topology changes it was reduced to about 11 dB, it's still a relatively noisy block.

[1]In this case, since this amplifier converts an input current into an output voltage, the gain is not adimensional like in a voltage/voltage amplifier.

4.4 Phase Shifter

The phase shifter is a crucial block in the beamforming receiver, since, in broad terms, it is in itself the beamformer. The delays it introduces allows the signals in each path to be combined according to their DOA. Figure 4.15 illustrates the implemented topology, a switched-capacitor vector modulator.

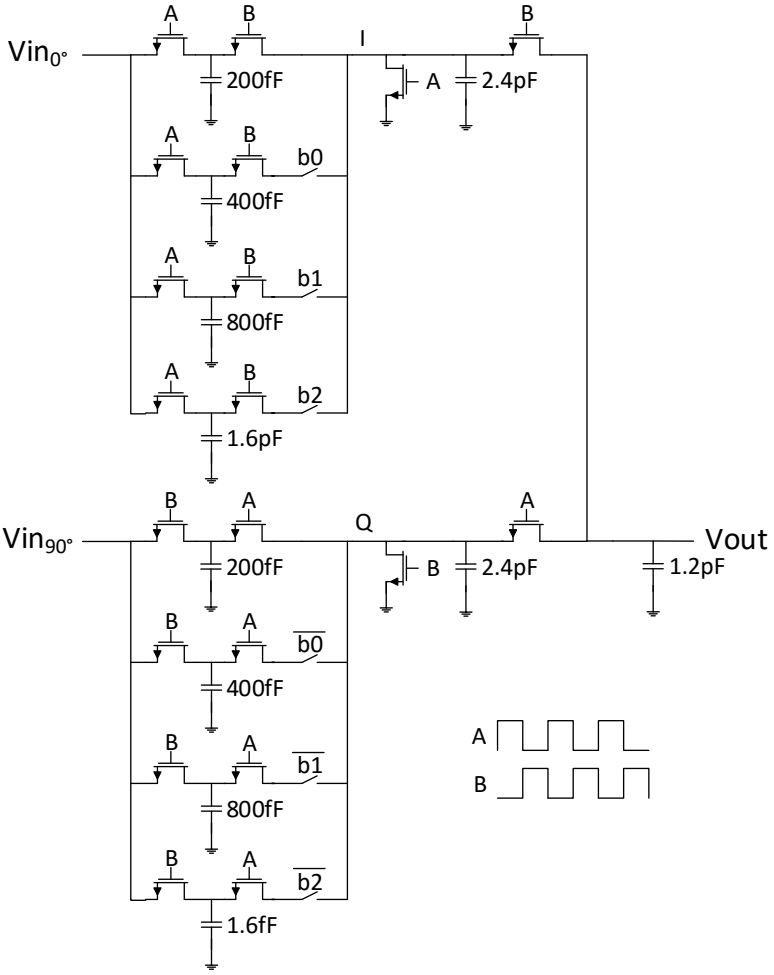

Figure 4.15: Switched-capacitor vector modulator.

The switches' dimensions had to be carefully chosen, because if the parasitic capacitances were large enough they might influence the circuits transfer function, defeating the purpose of the phase shifter. In order to avoid this effect there were two possible solutions, either scaling the transistors in each path in proportion to the capacitors, or minimize the parasitic capacitances of the transistors to a negligible value. The latter approach yielded the best results and was thus implemented. The dimensions of the switches are displayed in table 4.4.

In order to test the implementation of the vector modulator a couple of simulations were ran, the yielded results illustrated in figures 4.16 and 4.17.

Table 4.4: Phase shifter's switches' size parameters.

Transistor	Width (μm)	Length (nm)	Fingers
Sw (NMOS)	2	130	1

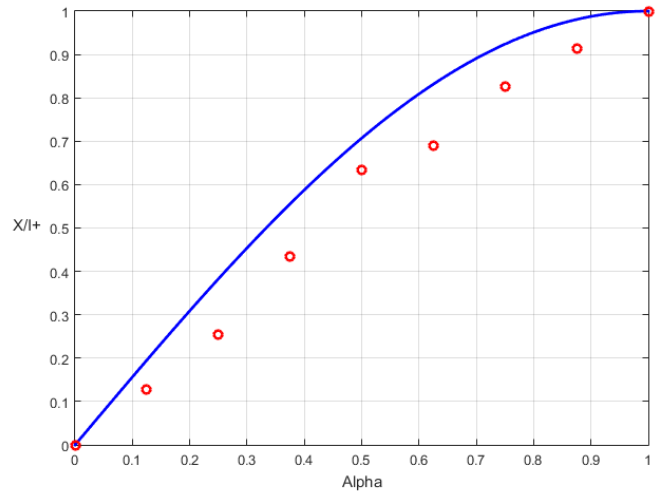

Figure 4.16: Vector modulator sine approximation.

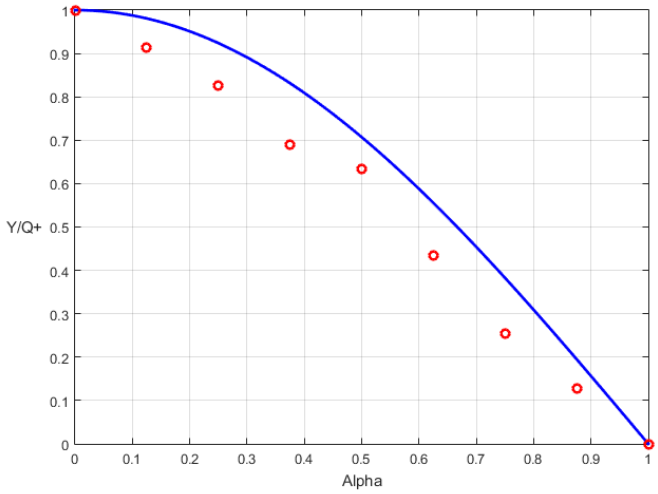

Figure 4.17: Vector modulator cosine approximation.

Figures 4.16 and 4.17, represent a comparison between the response of the sine and cosine waves between 0° and 90°, which is equivalent to an interval of $\alpha = [0, 1]$, and the obtained response of the transfer function in the X and Y paths, for all eight levels of the phase-shifter (3 bits). As it can be observed the approximation is slightly lower than it should, but it was still a reasonable result.

A noise figure simulation was also ran in order analyse the noise generated by the vector modulator, presented in figure 4.18.

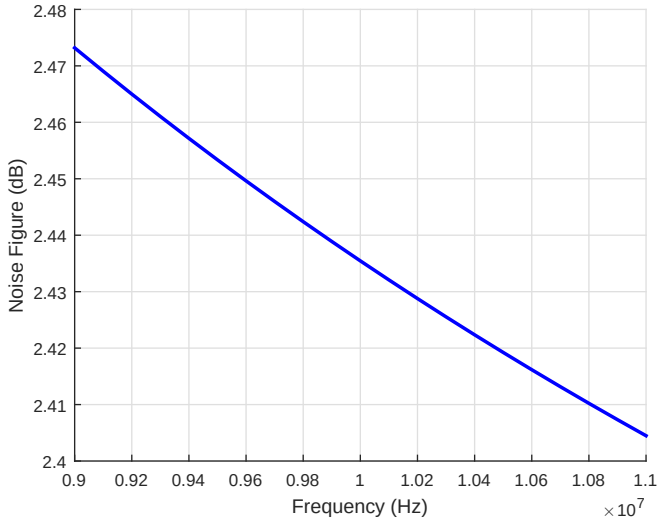

Figure 4.18: Vector modulator noise figure.

The value for the NF of the vector modulator present in figure 4.18 is of about 2.4 dB. However due to how this block operates, this value is inversely proportional to the value of α, the value present in figure 4.18 is the maximum value of NF, maximizing α yields the minimum value of NF for the vector modulator, approximately 1 dB.

4.5 Transconductance Stage

The last block of the AFE is the gm stage, of figure 4.19, since the purpose of this block is to simply provide the element summing in the current domain, it's gain isn't of special importance and was thus designed for unity gain, in order to minimize the load resistor to maintain the offset voltage in check.

The dimensions of the transistors used to implement this transconductance stage are listed in table 4.5.

Table 4.5: Gm stage size parameters.

Transistor	Width (μm)	Length (nm)	Fingers	Current (mA)	gm (mS)
$M_{1,2}$ (PMOS)	200	130	80	1.5	16.9

In order to verify the correct operation for the gm stage a simulation was ran, in which both the input and output voltages are present for comparison, of figure 4.20. A gain of a little bit over unity can thus be confirmed. It is important to note that in the simulation present in figure 4.20, the output voltage appears to have no offset, in truth this isn't so, there an offset voltage of $V_{offset} = I_{dc} \cdot R_{Load} = 1.5 \cdot 10^{-3} \times 200 = 300$ mV. This voltage level was removed for easier comparison in the V_{in} vs. V_{out} plot.

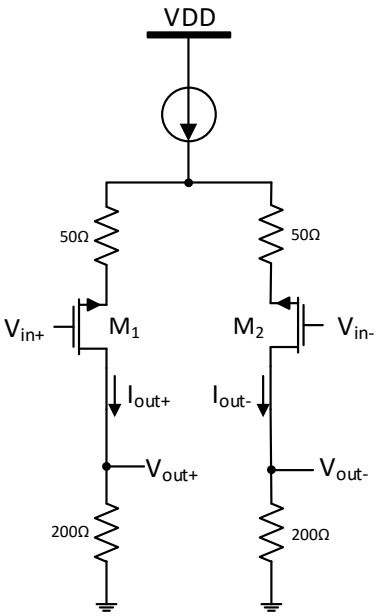

Figure 4.19: Implemented transconductance stage.

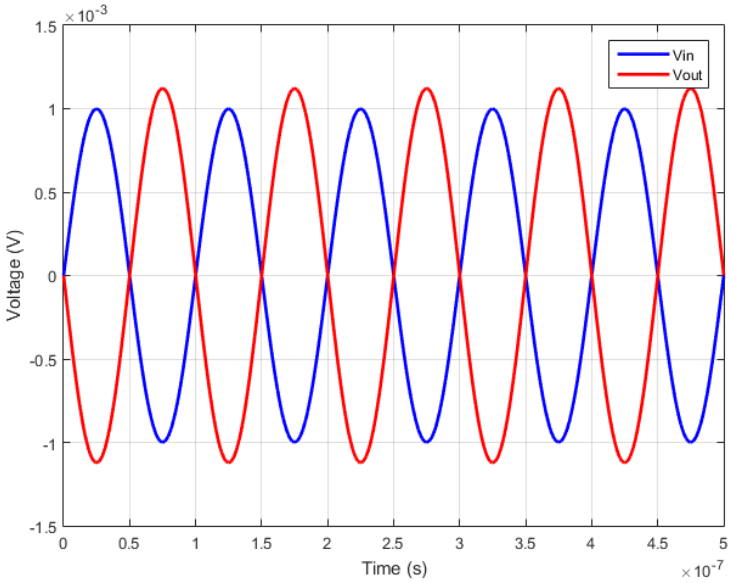

Figure 4.20: Input and output voltages comparison in the gm stage.

Another simulation was performed in order to analyse the noise figure of the block, the results it yielded are present in figure 4.21.

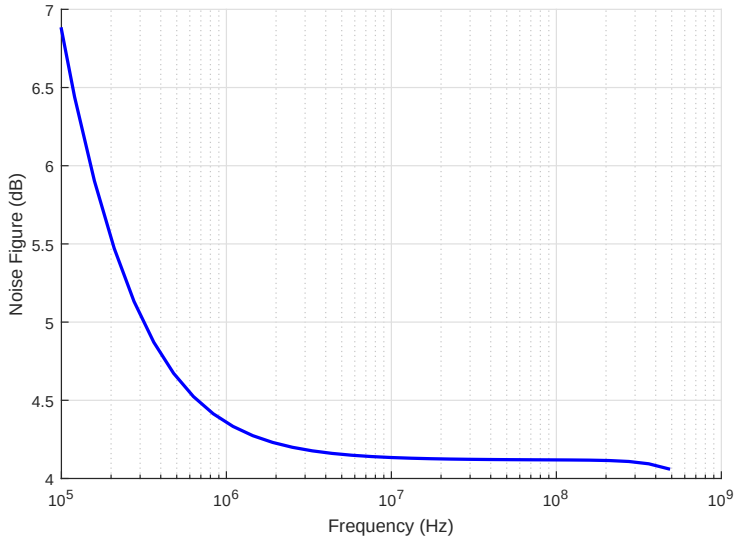

Figure 4.21: Noise figure of the gm stage.

As it can be observed in figure 4.21, the noise figure of the gm stage is about 4.2 dB, a reasonable result, this result is mostly due to the presence of the resistors, that are known to be prominent noise sources.

4.6 Complete Beamforming Receiver

After having analysed every block in the receiver, the complete AFE must be analysed, the final architecture is presented in figure 4.22.

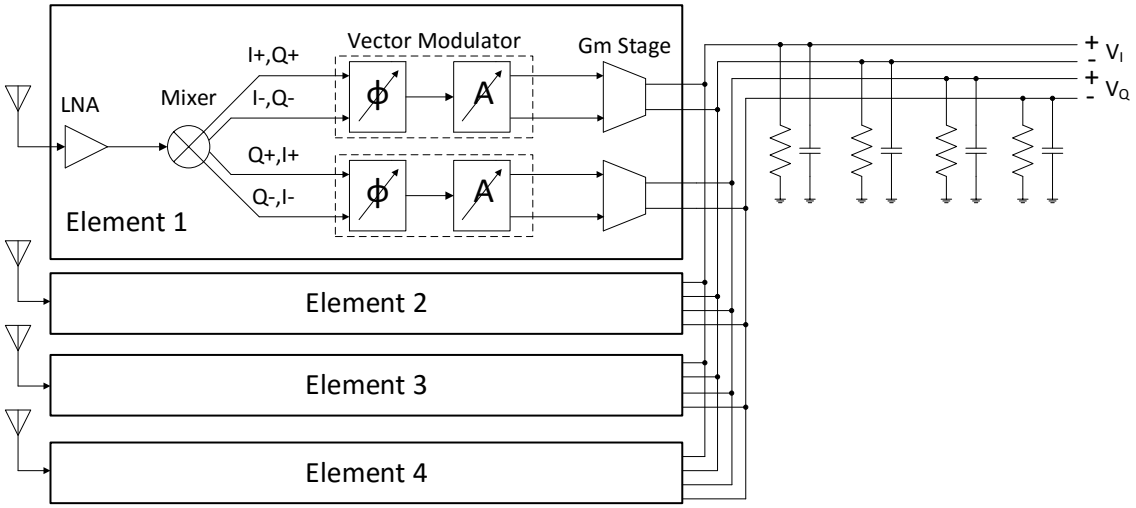

Figure 4.22: Beamforming architecture.

This is not a single element receiver owing to the fact that it employs four antennas to allow beamforming, thus special attention must be paid to how the various elements are connected. Since the antennas need to be spaced a distance of $\lambda/2$, to mimic the effect of the phase shift induced by the signal propagation, a simple phase shift was applied to each input source, given by

$$\phi_N = N \cdot \frac{d}{c} \cdot \sin\theta_0 = \begin{cases} \phi_0 = 0 \\ \phi_1 = \frac{1}{2f} \cdot \sin\theta_0 \\ \phi_2 = 2 \times \frac{1}{2f} \cdot \sin\theta_0 \\ \phi_3 = 3 \times \frac{1}{2f} \cdot \sin\theta_0 \end{cases} \tag{4.2}$$

In order to test the effect of beamforming various simulations were ran where in each a different value of DOA was applied, between $-90°$ and $90°$, then the normalised radiation intensity was calculated and plotted, yielding the graph of figure 4.24.

As it can be seen, comparing figures 4.24 and 4.23, both main beams are steered to $0°$, there's a rejection of at least 10 dB in the sidelobes at $\pm 45°$ and four nulls located at $\pm 30°$ and $\pm 90°$, although the beamwidth in the obtained AF is slightly larger than the expected result, the results are very similar and it can thus be concluded that the implemented circuit yeiled the expected results.

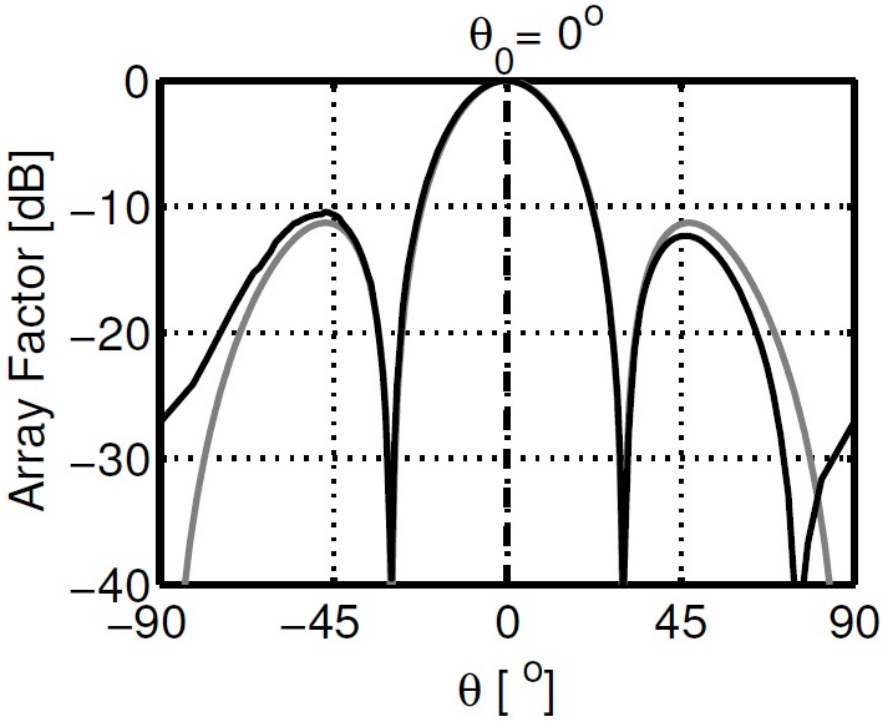

Figure 4.23: Expected array factor with the beam steered to 0°. (Adopted from [14])

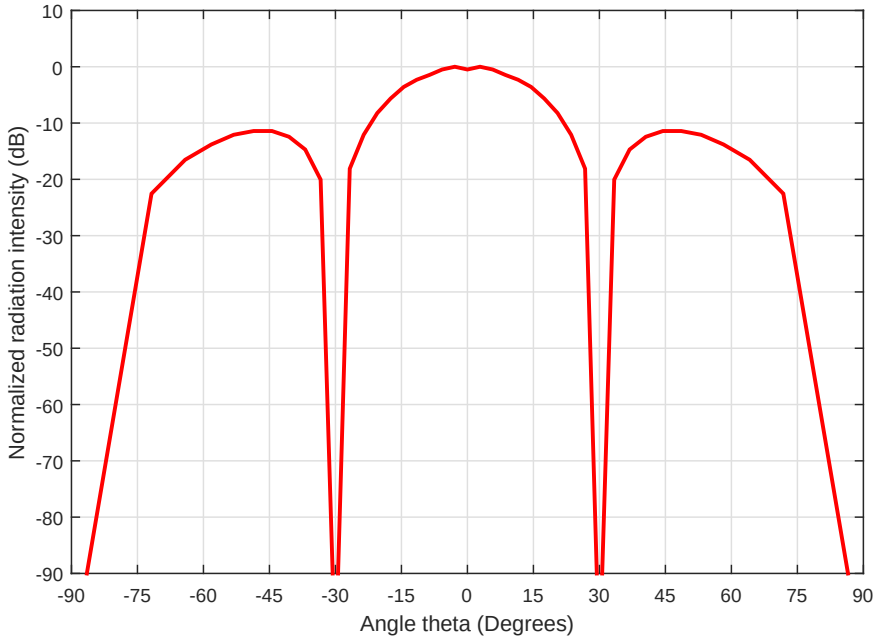

Figure 4.24: Implemented array factor with the beam steered to 0°.

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

The rapid rise of wireless communications in the last few decades, lead to the decrease of spectrum availability and to the increased demand for higher data rates, thus MIMO systems rose as a promising solution. These systems promised to increase signal transmission and enhance data bit-rates.

In this thesis a downconversion beamforming RF analog front-end was presented, this receiver technology employs multiple antennas in order to produce an effect of spatial selectivity. This technique can be interpreted as a spatial filter, because with the, above mentioned, spectrum unavailability ever more rigid requirements are imposed to temporal filters, making the temporal filter approach less appealing.

The receiver presented in this thesis, provides spatial selectivity that can be tuned for a given direction of arrival of the wanted signal, rejecting the interfering signals, incoming from different directions.

This receiver employs four antennas, each composed of a LNA, a double-balanced mixer, a phase shifter implemented with a switched-capacitor vector modulator and a transconductance stage for element summing in the current domain.

In regard to the various simulations that were performed in chapter 4, starting with the LNA, the input impedance of the circuit was well matched, the amplifier had a reasonable gain and low noise, on the other hand, the LNA linearity was rather low. The mixer had a reasonable conversion gain and a low noise figure value, the vector modulator also had a low noise value, although the sine and cosine implementation were a little bit off the target response. The last block, the gm stage had a reasonable noise figure value. The receiver as a whole achieved a rejection of at least 10 dB, which is a reasonable value when compared to other implementations [14].

5.2 Future Work

Throughout the design of the receiver presented in this thesis, there were some aspects that could see further improvement:

• The attempt to incorporate a TIA in the receive path instead of a voltage buffer didn't yield the expected results and was thus dropped, with proper optimization it could be an interesting and slightly different approach.

• The clock signals used in the circuit simulations were ideal sources, the implementation of the various clock signals also in 130 nm CMOS would've been interesting in order to further develop useful designing skills, and also to evaluate some non-ideal effects that can't be analysed with ideal sources.

• Creating an adaptive algorithm to work in conjunction with the designed beamformer, and control the phase shifting, for real time phase correction, would've been an extremely enthralling concept. Plus, the layout design of the receiver and IC fabrication in order to experimentally test the device would've been, given enough time and resources, really interesting, not only in terms of the thesis validation, but also in terms of valuable design skills acquisition.

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