NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF MATERIALS SCIENCE

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BSc in Micro and Nanotechnology Engineering

Multi-layered semiconductors for improved reliability and performance of amorphous oxide thin-film transistors

MASTER IN MICRO AND NANOTECHNOLOGY ENGINEERING

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Para mim.

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“A vida é feita de pequenos nadas.”
(Sérgio Godinho).

ABSTRACT

The continuous development of modern and flexible electronics requires thin-film transistors (TFTs) combining high performance, low power consumption, and reliable operation. Amorphous oxide semiconductors, particularly amorphous indium–gallium–zinc oxide (a-IGZO), have emerged as promising candidates due to their transparency, high carrier mobility, and compatibility with low-temperature processes. Nevertheless, challenges remain regarding stability and long-term reliability, which motivates strategies based on active layer engineering.

This dissertation explores the concept of dual-active-layer (DAL) TFTs to overcome intrinsic limitations of single-active-layer (SAL) structures. In this work, devices were fabricated combining a high-mobility semiconductor, amorphous indium–zinc oxide (a-IZO), with a lower-mobility but more stable semiconductor, a-IGZO. Two DAL configurations were studied: DAL_A, with a-IGZO as the layer closest to the gate dielectric and a-IZO on top, and DAL_B, with the opposite arrangement. Different a-IZO thicknesses (1 nm, 2 nm, and 5 nm) were investigated, and their performance compared to reference SAL a-IGZO TFTs of 40 nm (SAL_IGZO). In addition, a study on SAL structures with varying a-IGZO thicknesses was carried out to evaluate the impact of active layer scaling.

The results demonstrated that proper selection of thickness and layer order strongly impacts mobility, threshold voltage (V_{TH}), subthreshold swing (*SS*), and device stability. In particular, the DAL_B configuration with 5 nm of a-IZO delivered field-effect mobility (μ_{FE}) of ~47 $cm^2\ V^{-1}\ s^{-1}$, about twice the SAL_IGZO reference (~20 $cm^2\ V^{-1}\ s^{-1}$), but as a trade-off a negative V_{TH} shift occurs. 1 and 2 nm a-IZO layer did not yield a measurable dual-layer effect on μ_{FE}, but resulted in a significant improvement in PGBS stability compared to SAL device. Regarding SAL thickness, 25 nm enabled lower *SS*, more positive V_{TH} and superior stability under bias stress compared to 40 nm/15 nm thick devices.

Overall, active layer engineering demonstrated to be an effective route to mature oxide TFTs toward high-performance and reliable flexible electronics.

Keywords: Dual-Active layer, Thin-film transistors, a-IGZO, a-IZO

RESUMO

O desenvolvimento contínuo da eletrónica moderna e flexível exige transístores de película fina (TFTs) que combinem elevado desempenho, baixo consumo de energia e operação fiável. Os semicondutores de óxido amorfo, em particular o óxido de índio–gálio–zinco amorfo (a-IGZO), surgem como candidatos promissores devido à sua transparência, elevada mobilidade de portadores e compatibilidade com processos a baixa temperatura. Contudo, persistem desafios relativos à estabilidade e à fiabilidade a longo prazo, o que motiva estratégias baseadas na engenharia da camada ativa.

Esta dissertação explora o conceito de TFTs com dupla camada ativa (DAL) como forma de ultrapassar limitações intrínsecas das estruturas de camada ativa simples (SAL). Neste trabalho, fabricaram-se dispositivos combinando um semicondutor de elevada mobilidade, o óxido de índio–zinco amorfo (a-IZO), com um semicondutor de menor mobilidade mas mais estável, o a-IGZO. Estudaram-se duas configurações DAL: DAL_A, com a-IGZO como camada adjacente ao isolante de porta e a-IZO por cima, e DAL_B, com a disposição inversa. Investigaram-se diferentes espessuras de a-IZO (1 nm, 2 nm e 5 nm), comparando o seu desempenho com TFTs SAL de a-IGZO de 40 nm (SAL_IGZO) de referência. Adicionalmente, realizou-se um estudo de SAL com várias espessuras de a-IGZO para avaliar o impacto da redução da camada ativa.

Os resultados demonstram que a seleção adequada da espessura e da ordem das camadas influencia fortemente a mobilidade, *threshold voltage* (V_{TH}), *subthreshold swing* (*SS*) e a estabilidade do dispositivo. Em particular, a configuração DAL_B com 5 nm de a-IZO na camada inferior proporcionou um *field-effect mobility* (μ_{FE}) de ~47 $cm^2\ V^{-1}\ s^{-1}$, cerca do dobro da referência SAL_IGZO (~20 $cm^2\ V^{-1}\ s^{-1}$), mas provoca um deslocamento negativo acentuado da $V_{TH.}$ A camada de a-IZO com 1 e 2 nm não produziram um efeito mensurável de dupla camada, mas resulta numa melhoria significativa da estabilidade sob PGBS em comparação com o dispositivo SAL. Relativamente à espessura de SAL, os 25 nm permitiram obter uma SS mais baixa, um V_{TH} mais positivos uma estabilidade superior sob *bias stress tests* em comparação com os dispositivos de 40 nm/15 nm.

Palavras chave: Dupla camada ativa, Transístores de filme fino, a-IGZO, a-IZO

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ACRONYMS

a-IGZO	Amorphous Indium Gallium Zinc Oxide
a-IZO	Amorphous Indium Zinc Oxide
a-Si:H	Hydrogenated Amorphous Silicon
ALD	Atomic Layer Deposition
AOS	Amorphous Oxide Semiconductors
BG	Bottom Gate
C-V	Capacitance-Voltage
CB	Conduction Band
DAL	Dual-Active Layer
DI	Deionized
DIBL	Drain-Induced Barrier Lowering
DLW	Direct Laser Writing
EDS	Energy Dispersive X-ray Spectroscopy
FET	Field Effect Transistor
G	Gate
GD	Gate Dielectric
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NBS	Negative Bias Stress:
NGBS	Negative Gate Bias Stress
NIBS	Negative Illumination Bias Stress
PBS	Positive Bias Stress
PEB	Post-Exposure Bake

PECVD	Plasma-Enhanced Chemical Vapour Deposition
PGBS	Positive Gate Bias Stress
PR	Photoresist
RIE	Reactive Ion Etcher
S	Source
S/D	Source/Drain
SAL	Single-Active Layer
SB	Soft-Bake
SC	Semiconductor
SEM	Scanning Electron Microscopy
STEM	Scanning Transmission Electron Microscopy
TEM	Transmission Electron Microscopy
TFT	Thin-Film transistors
VB	Valence Band
TG	Top Gate

SYMBOLS

C_{OFF}	OFF-State Capacitance
C_{ON}	ON-State Capacitance
C_{ox}	Transistor Capacitance per Unit Area
C_P	Gate-to-Drain Parasitic Capacitance
C_S	Active-Layer Capacitance
I_{DS}	Drain-Source Current
$I_{DS\,lin}$	Drain-Source Current in the Linear Regime
$I_{DS\,sat}$	Drain-Source Current in the Saturation Regime
$I_{DS\,tri}$	Drain-Source Current in the Triode Regime
k_B	Boltzmann Constant
L	Channel Length
L_D	Debye Length
μ	Mobility
μ_{FE}	Field-Effect Mobility
μ_{sat}	Saturation Mobility
N_D	Bulk Donor Concentration
ρ	Bulk Resistivity
q	Elementary Charge
SS	Subthreshold Swing
t	Semiconductor Channel Layer Thickness
T	Temperature
V_{DS}	Drain-Source Voltage

V_{fb}	Flat-Band Voltage
V_{GS}	Gate-Source Voltage
$V_{GS\ stress}$	Stress Gate-Source Voltage
V_O	Oxygen Vacancies
V_{ON}	Turn-On Voltage
V_{OV}	Overdrive Voltage
V_{TH}	Threshold Voltage
W	Channel Width
ε	Relative Dielectric Permittivity
ε_0	Vacuum Permittivity
ε_S	Semiconductor Relative Dielectric Permittivity
$x_{acc\ max}$	Maximum Accumulation Layer Thickness

MOTIVATION AND OBJECTIVES

The continuous advancement of modern electronics requires devices that combine high performance, low power consumption, and cost-effective fabrication. These requirements are particularly crucial for flexible electronics, enabling applications such as flexible displays, wearable devices, Internet of Things (IoT) systems, radio-frequency identification (RFID) tags, and smart packaging.

To meet these needs, oxide thin-film transistors (TFTs), particularly those based on amorphous oxide semiconductors (AOS), have emerged as promising candidates thanks to their advantageous electrical properties, optical transparency, and favourable fabrication conditions. However, challenges remain in further improving their stability, reliability and performance. A promising strategy to address these limitations is layer engineering, whereby multiple semiconductor layers are combined to enhance the mobility and stability of the device. More recently, Wager et al. [1] demonstrated through analytical modelling and simulations that dual-layer TFTs achieve optimal mobility when carefully designed.

This motivates this work to explore the concept of dual-active layer (DAL) oxide TFTs, using a combination of a high mobility semiconductor, amorphous indium zinc oxide (a-IZO) with a lower mobility semiconductor, amorphous indium gallium zinc oxide (a-IGZO), with different designs and thicknesses within the existing baseline processes at CENIMAT to achieve high mobility and stable devices.

The first part of this study focuses on fabricating staggered bottom gate devices and producing a single-active layer (SAL) structure using a-IGZO as the semiconductor, as well as two types of dual-active layer (DAL) structure with different film thicknesses: one with a-IGZO in the bottom channel layer and a-IZO in the top channel layer (DAL_A), and the other with a-IZO in the bottom channel layer and a-IGZO in the top channel layer (DAL_B). The second part focuses on characterizing each sample and comparing the structures and active layer thicknesses. Finally, a study will be presented on future perspectives of the work carried out, which will include a comparison between SALs of a-IGZO with different thicknesses

1

INTRODUCTION

In this chapter, an introductory context will be given, focusing on TFTs operating principle, the importance of a-IGZO TFTs, and the need to introduce dual-active layer (DAL) technology. The chapter ends with a comparison study on DAL using a-IZO and a-IGZO films as semiconductors, with a particular emphasis on a recent study that motivates the objectives of this work.

1.1 Thin-film transistors (TFTs)

TFTs are a type of field-effect transistor (FET), thus their operating principle is analogous to that of the metal oxide-semiconductor field-effect transistor (MOSFET). However, in contrast to MOSFETs, TFTs can be made on any insulating or flexible surface that can withstand the manufacturing process. Furthermore, all the device layers are grown at lower temperature by vacuum or solution processing deposition techniques [2], [3], [4]. TFTs include three basic elements: (1) a thin semiconductor (SC) film (or active layer); (2) a dielectric layer; and (3) three electrodes (gate, drain and source) [5], [6].

1.1.1 TFTs operation principle

TFTs operation principle relies on the control of the flow of current between the source and drain electrodes (I_{DS}) by applying a voltage between gate and source electrodes (V_{GS}). The dielectric layer prevents direct current flow between semiconductor and gate while allowing electric field modulation [2], [4].

N-type semiconductor devices can present enhancement or depletion mode operation, depending if the threshold voltage (V_{TH}) is positive or negative, respectively. Enhancement mode devices reduce power dissipation and simplify circuit design and control, making them the preferred choice [7], [8]. The transistor is in cut-off when $V_{GS} << V_{TH}$, meaning there is no significant I_{DS} flowing and the device is considered being OFF. On the other hand, when $V_{GS} > V_{TH}$, the transistor is considered ON. TFTs have three distinct regions of functioning: the triode, the linear and the saturation regions, depending on the potential difference between source and drain (V_{DS}). If $V_{DS} < V_{GS} - V_{TH}$ the device is said to be working on the triode regime, with I_{DS} is defined by (1.1).

$$I_{DS\,tri} = \frac{W}{L}\,\mu_{FE}\,C_{ox}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS} \tag{1.1}$$

If $V_{DS} << V_{GS} - V_{TH}$ the device operates in linear regime and I_{DS} is defined by (1.2) where W is the channel width, L is the channel length, C_{ox} is the specific capacitance of the gate dielectric (GD) per unit area, and μ is the channel mobility. When $V_{DS} > V_{GS} - V_{TH}$ the device operates in saturation regime and I_{DS} is defined by (1.3) [9], [10].

$$I_{DS\,lin} = \frac{W}{L}\,\mu_{FE}\,C_{ox}(V_{GS} - V_{TH})V_{DS} \tag{1.2}$$

$$I_{DS\,sat} = \frac{W}{2L}\,\mu_{sat}\,C_{ox}\,(V_{GS} - V_{TH})^2 \tag{1.3}$$

As transistors are the fundamental building blocks of modern electronics, it is crucial to maintain precise control over their key parameters. Equations (1.2) and (1.3) can be used to extract the TFT DC parameters: threshold voltage (V_{TH}), carrier mobility (μ), subthreshold slope (SS) and On-Off ratio influence the devices regarding switching behaviour, power consumption, and speed [2].

- **Threshold voltage (V_{TH})**: it represents the minimum voltage that needs to be applied to the transistor´s gate terminal to induce the channel formation, allowing current to flow between the source and drain terminals.
- **Turn on voltage (V_{ON}):** it is the V_{GS} at which the transistor begins to conduct current.
- **Carrier Mobility (μ):** this is related to the efficiency of carrier transport in the semiconductor material, directly affecting the maximum I_D and the device operation frequency. This parameter can be influenced by various factors, such as temperature and doping concentration [4], [11]. Mobility of a TFT can be field-effect mobility (μ_{FE}) obtained in the linear regime (1.2) or can be saturation mobility (μ_{sat}) obtained in the saturation regime (1.3).
- **Subthreshold swing (SS):** this parameter represents the necessary increase in V_{GS} required to increase the I_D by one decade, which is a measure of how efficiently the transistor can turn on and off [12]. Smaller SS indicates high-quality interface between the GD and the semiconductor, characterized by lower trap densities, which contributes to reduced power consumption in circuit applications [4], [13].
- **On-Off Ratio:** it is the ratio of the maximum to the minimum I_{DS}. This parameter can be influenced by various factors such as the quality of the semiconductor material. For digital circuits, higher ratios ($\geq 10^6$) are typically required to ensure reliable operation. In analog circuits, values of $\geq 10^4$ are generally considered sufficient [4].
- **Stability:** it refers to how well a TFT maintains its performance over time when exposed to electrical stress, light or temperature. To evaluate stability, bias stressing tests are commonly used: gate bias stress is conducted to evaluate the degradation of key device metrics such as V_{TH}, SS and μ_{FE} under a continuous applied gate voltage, either of positive - Positive bias stress (PBS), or negative sign - Negative bias stress (NBS). These tests can also be accompanied by other external stressing factors such as light, temperature, or drain bias. For instance, negative illumination bias stress (NIBS) is an ubiquitous reliability test for TFTs aimed at display applications, due to exposure to white light from the backplane [14].

1.1.2 TFTs structures

The configuration of a TFT affects its key electrical parameters. Therefore, selecting an appropriate device structure is essential for optimizing performance in accordance with the demands of a specific application.

The most common planar TFT structures are bottom-gate (BG) and top-gate (TG) depending on the location of the gate electrode if it is deposited before or after the active layer, respectively. The BG and TG can be sub-classified either in staggered or coplanar, depending if the source/drain contacts are on the opposite or on the same side of the SC/GD interface, respectively [3], [4]. BG structure offer advantages such as simplified fabrication and enhanced device performance, however, effective passivation of the oxide semiconductor layer remains crucial for ensuring device stability [15]. There are some unconventional configurations such as Double-gate, being popular for enhanced static performance [10], Vertical or Quasi-Vertical TFTs [16], Corbino TFTs [17], Self-aligned TFTs [18], [19] and Dual-active layer TFTs [19].

(a) (b)

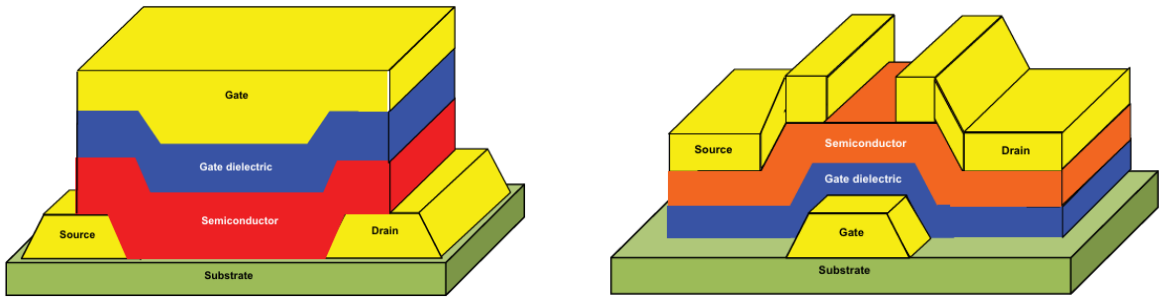


Figure 1 – Schematic diagrams of the most common planar TFT structures; (a) staggered top-gate, (b) staggered bottom-gate, adapted from [3].

1.2 Amorphous oxide semiconductors (AOS)

Several types of TFT technologies are widely used and among them metal oxide semiconductors are particularly noteworthy as they represent the best compromise between performance and large-area, low thermal budget compatibility [2], [20]. Table 1 provides a summary and comparison of the most important device properties for the established application.

Table 1 - Comparison between metal oxide semiconductors and other established TFT technologies based on [4], [20].

TFT properties	Metal oxide semiconductors	Amorphous silicon	Low temperature poly-crystalline silicon	Organic
Microstructure	Mainly amorphous	Amorphous	Poly-crystalline	Mainly poly-crystalline
Carrier mobility ($cm^2/V.s$)	10 ~ 100	0.1 ~ 1	50-100	0.1-10
Process complexity	Low	Low	High	Low
Processing Temperature (ºC)	RT to 350	150-350	350-500	RT to 250
Manufacturing cost	Low	Low	High	Low
Large-area scalability	High	High	Low	High
I_{off} current (A)	$\sim 10^{-12}$-10^{-11}	$\sim 10^{-11}$-10^{-10}	$\sim 10^{-10}$-10^{-9}	$\sim 10^{-10}$-10^{-8}
Device type	Mainly n-type	N-type	N- and p-type	Mainly p-type

Unlike crystalline materials, amorphous semiconductors possess structural disorders and high concentration of defects, such as varying bond lengths, bond angles, and coordination numbers, which introduce localized states within the energy gap. These localized states, particularly the so-called "band tail states" play a critical role in the optical and electrical behavior of amorphous semiconductors [21].

Most oxide semiconductors are n-type because they use electrons as transport pathways, which exhibit higher mobility than holes. This arises because their CB minimum are mainly formed by spatially overlapping metal cation s-orbitals, enabling relatively high electron mobilities. In contrast, hole transport through the valence band (VB) relies on localized and asymmetrical O 2p orbitals, which limits p-type performance. Consequently, developing p-type AOS TFTs remains challenging [9], [22], [23].

Nevertheless, AOS thin film has been demonstrated to offer a number of advantages when compared with other types of semiconductors, such as, they are wide band gap material (E_g > 3 eV), which means that it is transparent in a wide range of visible light. Secondly, it can be processed at low temperatures, making it suitable for flexible and cost-effective applications. The amorphous structure of these materials eliminates grain boundaries, thereby reducing charge trapping and enhancing uniformity over large areas. AOS materials also exhibit high carrier mobility (~10 $cm^2/V \cdot s$), significantly higher than a-Si:H, along with low off-state current (~10^{-12}-10^{-11}), which enhances energy efficiency [8], [24]. Furthermore, AOS TFTs exhibit excellent short-range uniformity in their electrical characteristics, minimizing local variations among neighboring devices and thereby enabling reliable performance in large-area circuits and display applications [25].

1.2.1 Importance of a-IGZO TFTs

a-IGZO, an n-type multicomponent AOS, have seen the most extensive research and applications of all oxide TFTs. a-IGZO is a complex oxide have unique properties, such as high carrier mobility, tunable composition, low processing temperatures, electrical stability, low *SS*, high energy band-gap (> 3ev) and high on-off ratio [26], [27].

These remarkable electrical properties of a-InGaZnO originate from the presence of **indium (In)** element, whose outer electron shell is composed by a 5s orbital. It is spherical and large, and thus the overlap of this orbital between neighboring In ions is significant, which act as channels for electron transport. More importantly, this overlap structure is very little affected by the degree of crystallization, so the electron transport channels still exist in the amorphous state. Some studies show that electronic structures and carrier transport mechanisms in a-IGZO are similar to single-crystalline IGZO because of these spherical s orbitals that are not affected by local distortion of the chemical bonds. Consequently, increasing In content can improve electron mobility but on the other hand, can shift V_{TH} to negative and raise sensitivity to various forms of stress [2], [27], [28].

The presence of **gallium (Ga)** in the material promotes the formation of a strong chemical bond with oxygen, suppressing the formation of oxygen vacancies, causing the improvement of TFTs stability and reducing its defects. The increases in the Ga content will reduce the free electron density, thus reducing mobility. A range of combinations and elemental ratios have been explored and reported, not only for a-IGZO TFTs but also for other AOS-TFTs. Achieving a balance between mobility and stability remains a key challenge [21], [24]. Moreover, it is imperative to acknowledge the function of **zinc oxide (ZnO)** in its capacity as a "network former". This role is believed to contribute to the stabilization of the amorphous structure, although its role is not completely clear [29].

Therefore, the inability of pure In_2O_3 and ZnO to form stable amorphous structures highlights the essential role of incorporating multiple metallic cations to enable the formation of stable and reliable amorphous semiconductors for device applications [30].

1.3 Single-active layer and Dual-active layer a-IGZO TFTs

A **single-active layer (SAL)** is a TFT design that employs a single layer of semiconducting material for the control of charge carrier flow. a-IGZO is commonly used in SAL TFTs because it can exhibit high mobility (>20 $cm^2/V \cdot s$) when an In-rich a-IGZO channel composition is employed [28], [29], [31]. However, in order to enhance the mobility of these SAL with increasing In content, the results show a decline in the off state current and thus in the on-off ratio, which negatively impacts device performance [28]. Furthermore, photo or bias stability is also worsened by higher indium levels, due to the formation of oxygen vacancies which, when exposed to light, release electrons and cause an undesirable shift in the V_{TH} [28], [32]. It is therefore challenging to achieve both high mobility while maintaining a reasonable V_{TH} and good stability in the devices.

To carry forward the development in mobility to the next levels, Kim et al. in 2008 [19] proposed the first **Dual-active layer (DAL).** These bilayer TFTs can be categorized into two types: heterojunction and graded. Heterojunction oxide TFTs are formed by combining different materials in the stack, i.e combines a high-mobility and high carrier concentration semiconductor, such as a-IZO [33], with a lower-carrier concentration AOS, such as a-IGZO. Over the past years, several more combinations of DALs were reported such as heterojunctions of IZO/Zinc tin oxide [1], IZO/Al-doped indium zinc oxide [34] and Indium tin oxide/IGZO [35]. The extensive range of available material combinations facilitates the advancement of electrical device performance through the continuous discovery and improvement of new materials. This double-channel structure offers the distinct advantage of enabling the control of electrical characteristics, chemical stability, and reliability in TFTs. The enhanced carrier mobility observed in dual-active layer TFT structures can be attributed to the difference in Fermi energy levels between the two materials forming the active layer. The stacking of these materials creates an offset in their band alignment, which generates a potential well that confines electrons in a two-dimensional electron gas (2DEG). This interface allows electrons to move freely while preventing them from escaping. As the difference in Fermi energy levels increases, the concentration of confined electrons rises, resulting in enhanced device mobility [36]. However, issues emerge with regard to band alignment between materials and their interfaces. Severe band misalignment, owed to semiconductors with very different work functions, can result in two parallel conduction channels and thus separate V_{TH} values. It is therefore essential to exercise careful control over these stacks, in terms of both thickness and electron density, in order to guarantee optimal device functionality [24].

As a solution to the issues, the concept of graded-active layer DAL formation has emerged. This type of stack is formed by two or more layers of the same material, promoting homogeneity and better interface properties. There is extensive research in an attempt to create these types of active layers via different methods: oxygen vacancy (Vo) concentration [30], [37], [38], [39], hydrogen annealing [40], [41], changes in the Ga and In molar ratio in each layer [33], [42]. However, these type of multi-layer TFTs have a limited choice of materials and a tight process control, for instance strict annealing conditions.

1.3.1 DAL of IZO/IGZO TFTs

Throughout the years, many studies comparing DAL TFTs and SAL TFTs have been carried out, especially those using an active layer architecture based on a combination a-IZO and a-IGZO. Table A. 1 (Appendix A.1) presents some studies comparing DAL of IZO/IGZO and SAL of a-IGZO, from which it can be concluded that DAL structures generally exhibit an increase in mobility, with a trade-off of negative shifts in V_{TH} and decreasing SS values, and smaller V_{TH} shifts under bias stress tests, when compared to SAL structures. Furthermore, the active layer structure of DAL devices reported so far positions the a-IZO near the G/GD interface, and then the a-IGZO, except the two last reports presented on Table A. 1 (Appendix A.1).

More recently, Wager *et al.* [1] have further explored the design and analysis of dual-layer TFT structures, presenting a model that contradicts the experimental results reported to date. By formulating a set of analytical equations and performing detailed simulations, the authors demonstrated that the optimal mobility performance in dual-layer TFTs (using a top-gate architecture) is achieved when the semiconductor with higher mobility is positioned further away from the GD and the lower mobility semiconductor is positioned nearest the GD, and that both layers should be made as thin as possible. They also emphasized the importance of using only 'short base' channel thicknesses (when the semiconductor layer is thin enough that the entire channel is influenced by the G voltage). These should be used when designing single-layer or dual-layer TFTs with optimal mobility performance, meaning that the total channel thickness must remain sufficiently small compared to the carrier diffusion length, so that all layers contribute effectively to conduction without introducing electrically inactive regions, improving performance.

However, it should be noted that this analytical model is based on highly idealized conditions. These include uniform donor density, well-defined permittivities and diffusion lengths, and negligible interface or bulk trapping, ion motion or bias-stress instabilities. While these assumptions enable a clean analytical treatment, they differ from the conditions commonly found in the experimental world.

2

MATERIALS AND METHODS

This chapter describes the system and conditions used in the deposition and characterization of a-IZO thin films and the SAL and DAL TFTs, fabricated throughout the course of this work.

2.1 a-IZO thin film fabrication

The fabrication of a-IZO thin films was carried out on 2.5 x 2.5 cm Corning glass substrates. These substrates were cleaned by submerging them in acetone, followed by isopropyl alcohol (IPA), using ultrasonic baths for 10 minutes each at 40 °C. Subsequently, the substrates were rinsed with deionized (DI) water and dried using a nitrogen gun. Finally, they were placed on a hot plate at 110 °C for at least 10 minutes and allowed to cool down to room temperature before use. This substrate cleaning methodology was kept the same for this entire work.

a-IZO thin films were deposited by RF magnetron sputtering with an AJA ATC-1300 F system. The depositions were carried out using a co-sputtering process utilizing In_2O_3 and ZnO 2" targets within an Ar and O_2 atmosphere, at room temperature, with gas flow rates maintained at 19.4 sccm and 0.6 sccm, respectively, while keeping a constant chamber pressure of 2.3 mTorr throughout the deposition. While the In_2O_3 target power was fixed at 64 W, three different ZnO power conditions were studied to enable different a-IZO compositions: 33 W, 16 W and 6 W.

Using shadow masks, 60 nm thick Mo contacts were sputtered with an AJA ATC-1800 F for the subsequent thin film electrical characterization, described in 2.3.1

2.2 TFTs fabrication

Both SAL TFTs and DAL TFTs were fabricated using a staggered bottom-gate configuration on cleaned 2.5 × 2.5 cm Corning glass substrates. All photolithographic processes described below were carried out using mask layouts designed for Direct Laser Writing (DLW). The patterns were defined using either the positive resist, AZ ECI 3012 PR, or the negative resist, AZ nLOF 2020, applied with a bench-mounted Suss LabSpin6 spin coater, and the developer used was the AZ 726 MIF.

Figure A. 1 in Appendix A.2 shows the schematic representation of the TFT fabrication process described below.

For the gate electrodes[1] (Step 1 in Figure A. 1), 60 nm of Mo was deposited in an Ar atmosphere using the AJA ATC 1800 F sputtering system, onto which a negative PR was spin-coated and then soft-baked (SB) at 110 °C for 2 min. Gate mask was exposed in a Heidelberg MLA150 DLW, followed by a post-exposure bake (PEB) for 2 min at 110°C and PR development for 15-20 s, without agitation. The sample was then rinsed with DI water and dried using a nitrogen gun. Afterwards, to transfer the pattern onto the respective metallic layer, the Mo was dry-etched using a Trion Phantom 3 reactive ion etcher (RIE) with SF_6 gas, applying 60 W for 200 s. The remaining resist was removed by immersing the samples in TechniStrip P1331 (Technic), heated to 80 °C, for 2–5 minutes. Subsequently the samples were dried on a hotplate for 2-3 min at 110 ºC.

The gate dielectric (GD) layer (Step 2 in Figure A. 1) consisted of 50 nm of Al_2O_3 deposited by Atomic Layer Deposition (ALD) using a Beneq TFS 200 system. For via opening, the corresponding mask was exposed onto a spin-coated positive photoresist, followed by an SB at 90 °C for 1 min and a PEB at 110 °C for 1 min. The resist was developed for 20-30 s with agitation, then rinsed with DI water and dried with a nitrogen gun. The Al_2O_3 was wet-etched with pure H_3PO_4 at 85 ºC. PR removal followed the same procedure described above for the gate electrode, and the samples were dried on a hotplate for 2-3 min at 110 ºC.

The semiconductor (SC) layer is deposited by sputtering and patterned through a lift-off process. First, a positive PR layer is patterned using the SC mask following the same lithographic procedure used for the GD. Before each thin-film deposition, an *in-situ* 10-minute plasma treatment was applied using Ar and O_2 flows of 20 sccm each, a substrate bias power of 10 W, and a pressure of 2.3 mTorr. For the SAL transistors (Step 3 in Figure A. 1), an a-IGZO thin film with a 2:1:1 In;Ga:Zn atomic ratio was deposited by co-sputtering using an AJA ATC-1300 F system equipped with three 2" targets (In_2O_3, Ga_2O_3 and ZnO). The deposition was performed in an Ar/O_2 atmosphere at room temperature, under the same conditions used for the a-IZO thin film described in section 2.1 In the case of DAL transistors (Step 4 in Figure A. 1), both the a-IGZO and a-IZO thin films were depsited sequentially without breaking vacuum. The pre-sputtering was carried out under the same conditions used for the first layer deposited in a specific sample. After deposition, the samples were immersed in P1331 stripper at 80-90 °C for 10-15 min with continuous agitation for PR removal (lift-off) and annealed at 300 ºC for 1 h on a hot plate.

Finally, 60 nm of Mo for source and drain (S/D) electrodes (Step 5/6 in Figure A. 1) were deposited employing the same sputtering system as for the gate electrodes and patterned through a lift-off process, similar to the one used for the SC layer. Subsequently, the samples were annealed at 180 ºC for 1 h.

A passivation step (Step 7 in Figure A. 1) was added to the SAL devices. This passivation layer is composed of a 1 µm thick parylene-C film deposited using a Parylene Coating System (PDS2010), followed by a 20 nm of Al_2O_3 deposited by ALD (Beneq TFS 200). The pad access mask was exposed onto a negative PR (AZ nLOF 2070) followed by an SB at 110 °C for 2 min and a PEB at 110 °C for 5 min, the development took around 2-3 min. The exposed areas were dry-etched, and any remaining

[1] The gate electrode fabrication process varied across batches. In some cases, instead of 60 nm, either 80 nm or 100 nm of Mo was deposited. In another batch, the gate consisted of a bilayer structure comprising 60 nm of Mo and 30 nm of a-IZO deposited on top, fabricated using a lift-off process. This variation mainly resulted from issues encountered during fabrication, as the Mo layer was prone to corrosion when exposed to the P1331 stripper for extended periods, which compromised pattern integrity.

resist was removed using the same procedure described previously. Finally, the devices underwent a post-fabrication annealing on a hot plate, at 180 °C for 1 hour.

2.3 Devices characterization

2.3.1 a-IZO thin films characterization

To determine the growth rate of the a-IZO films, the thickness of each thin film was measured using a DektakXT Bruker profilometer. Prior to the sputtering depositions, small marks were made on the silicon substrates using a permanent marker. After deposition, these marked areas were cleaned with acetone to create step-like profiles, which facilitated accurate thickness measurements. Hall effect measurements were taken with a Biorad/Nanometrics HL5500 Hall effect system. Scanning electron microscopy (SEM), with a Hitachi Regulus 8220 system, was employed to acquire energy dispersive X-ray spectroscopy (EDS) data of the a-IZO samples, with an accelerating voltage of 20 kV. This analysis enabled the quantification of the indium and zinc content (%In and %Zn, respectively) in the a-IZO films and the calculation of their atomic ratio.

2.3.2 TFTs characterization

The SAL and DAL devices were electrically characterized using either Keysight B1500A semiconductor parameter analyzer in conjunction with a Cascade Microtech EPS 150 manual probe station or an Agilent 4155C semiconductor parameter analyzer plus a Cascade Microtech M150 manual probe station, in order to extract transfer curves, both linear and saturation; output curves; Capacitance-Voltage (C-V), and stress tests.

The electrical stress test setup was conducted for an overdrive voltage (V_{OV}) of +5 V and -5 V, for PGBS and NGBS, respectively. The applied stress voltage is defined as $V_{GS\,stress} = V_{TH} + V_{OV}$. The measurements were conducted under conditions of darkness and ambient air. The transfer curves were recorded at regular intervals, initially at 0, 5, 10 minutes, and subsequently every 10 minutes, for a total stress time of 60 minutes. The gate bias is applied continuously throughout the stress period, with interruption solely occurring for the purpose of acquiring linear transfer characteristics. After stressing, the devices are grounded for a period of one hour, with the objective of monitoring recovery. Throughout the stress test, the devices were biased at a V_{DS} = 100 mV to monitor the drain current.

2.4 Preparation of a-IZO samples for STEM-EDS analysis

The fabrication of the a-IZO samples for Scanning transmission electron microscope (STEM) - EDS analysis was carried out on Transmission electron microscopy (TEM) half-grids containing carbon and silicon. A 100 nm Al_2O_3 layer was first deposited by ALD using a Beneq TFS 200 system to mimic the TFT stack, where a-IZO is grown. Subsequently, a-IZO films with nominal thicknesses of 1 nm, 2 nm, and 5 nm were deposited by the same process described above for the SC deposition using an AJA ATC-1300 F system.

3

RESULTS AND DISCUSSION

In this chapter, the characterization of the different TFTs batches will be presented. It starts with the analysis of the a-IZO films used in DALs, followed by a brief context on the methodology adopted for extracting TFT metrics and by a literature based comparative study. Subsequently, the electrical characterization of a-IGZO SAL TFTs with a 40 nm channel thickness is discussed. Next, the study of the different DAL TFTs fabricated and the comparison with the a-IGZO SAL is presented. Finally, a study of a-IGZO SAL active layer thicknesses is presented for future perspectives of this work.

Throughout this chapter, specific nomenclatures are adopted. **SAL_IGZO** refers to TFTs with a SAL of a-IGZO. Two types of DAL structures are considered: in **DAL_A**, a-IGZO is used as the bottom channel layer (near the GD) and a-IZO as the top channel layer (further the GD), while in **DAL_B** the configuration is inverted, with a-IZO as the bottom channel (near the GD) and a-IGZO as the top channel layer (further the GD). Different a-IZO thicknesses are also employed, namely **DAL_A_IZOthicknesses** or **DAL_B_IZOthicknesses**, where "IZOthicknesses" can vary between 1 nm, 2 nm and 5 nm, e.g. DAL_A_5 and DAL_B_5

3.1 a-IZO film study for DAL application

The study of a-IZO films for incorporation as the active layer in the DAL was conducted by maintaining the same In_2O_3 target power used for IGZO deposition (64 W), while varying the ZnO target power, without annealing. Table 2 summarizes the three different a-IZO films obtained, the deposition conditions, and the corresponding characterization results, including profilometry, EDS, and Hall effect measurements.

a-IZO 1 represents the same target power conditions used for a-IGZO deposition, showing the same In:Zn atomic ratio as these films. a-IZO 3 corresponds to the lowest ZnO target power achievable by the sputtering equipment, resulting in a 32:1 ratio with almost no Zn content in is constitution, while a-IZO 2 represents an intermediate case with a 9:1 ratio showing a significantly higher In content compared to Zn. Hall effect measurements reveal that a-IZO 3, with the highest In concentration, exhibited the lowest resistivity and the highest mobility, reflecting a significant increase in carrier density. A-IZO 2 presented intermediate behaviour, whereas a-IZO 1 showed the highest resistivity and lowest carrier concentration and Hall mobility. Additionally, the negligible Zn concentration of a-IZO 3 films raises concerns

regarding the temperature budget of the fabrication process, given than In_2O_3-rich films readily crystallize at temperatures as low as 150ºC [2].

Table 2 - Deposition conditions and characterization results of a-IZO films for application as the active layer in the DAL.

		a-IZO 1	a-IZO 2	a-IZO 3
Deposition conditions	ZnO target power (W)	33	16	6
	Deposition time (min)	25	25	20
Profilometry	Avg Measured Thickness (nm)	71.16 ± 2.40	58.27 ± 1.11	47.86 ± 3.18
	Growth rate (nm/min)	2.44	2.33	2.39
EDS	In (atomic %)	1.05	0.94	0.87
	Zn (atomic %)	0.57	0.10	0.03
	Atomic ratio (In/Zn)	2:1	9:1	32:1
Hall Effect	Sheet resistance (Ω/ sq)	2.32×10^{7}	5.04×10^{6}	4.59×10^{4}
	Bulk resistivity (Ω.cm)	172	30.1	0.22
	Hall coef. (m^2/C)	-1.85×10^{4}	-8.75×10^{3}	-126
	Hall mobility ($cm^2/V.s$)	8.42	18.95	27.83
	Sheet concentration (e/cm^2)	3.44×10^{10}	7.70×10^{10}	5.03×10^{12}
	Bulk concentration (e/cm^3)	4.71×10^{15}	8.00×10^{16}	1.05×10^{18}

Considering these results, one of the main objectives of incorporating a-IZO into DALs is to achieve high In content to enhance electron mobility, while preserving amorphous structure. Therefore, IZO 2 was selected as the most suitable film for integration into DAL structures.

3.2 Electrical parameters extraction

This section provides the methodology followed for extracting the electrical parameters of the DAL and SAL TFTs that will be presented and analyzed in the following sections.

Firstly, the oxide capacitance (C_{ox}) was obtained from C–V measurements by evaluating the total gate capacitance in the ON and OFF states of the device. Specifically, the total capacitance is measured when the TFT is turned ON (C_{ON}) and when it is turned OFF (C_{OFF}), and C_{ox} is then calculated according to (3.1), respectively. In this work, C–V curves were acquired at 1 kHz, 10 kHz and 100 kHz to assess the frequency dependence of the oxide and interface response (Appendix A.3). The extracted C_{ox} values were approximately 140 nF/cm² and relative dielectric constant (ε) of around 8 which is consistent with the expected capacitance of Al_2O_3 GD deposited by ALD at our center [43], [44].

$$C_{OX} = \frac{C_{ON} - C_{OFF}}{WL} \tag{3.1}$$

From the linear curves *SS*, Off current (I_{OFF}), On-Off ratio, μ_{FE}, V_{TH} and V_{ON} were extracted and μ_{sat} was extracted from the saturation curves The *SS* values were determined by (3.2). On-Off ratio is defined as the ratio between the highest and lowest recorded I_{DS} in the linear region. Here, I_{OFF} corresponds to the drain current measured in V_{ON} (when the current begins to increase), and the On current (I_{ON}) is defined as the drain current at V_{GS} = 5 V, ensuring that the device is in the fully On state.

$$SS = \left(\frac{d \log(I_D)}{dV_G}\Big|_{max} \right)^{-1} \quad (3.2)$$

μ_{FE} is given by (3.3) and μ_{sat} given by (3.4), and the maximum value is extracted as the μ_{FE} and μ_{sat} of the respective device, not considering evident noise-related spikes.

$$\mu_{FE} = \frac{\frac{dI_D}{dV_{GS}}}{V_{DS} C_{ox} \frac{W}{L}} \quad (3.3) \qquad \mu_{sat} = \frac{\left(\frac{d\sqrt{I_D}}{dV_{GS}} \right)^2}{\frac{1}{2} C_{ox} \frac{W}{L}} \quad (3.4)$$

The V_{TH} parameter is the maximum of the second derivative of $I_{\mathrm{DS\,lin}}$ determined according to (3.5). V_{ON} is extracted when there is a transition from the OFF state to the ON state, at the exact moment when the current begins to increase ($I_{DS\,lin} = I_{OFF}$), as seen in the transfer curve, represented in semi-log scale.

$$V_{TH} = \frac{d^2 I_{DS\,lin}}{dV_{GS}{}^2} \quad (3.5)$$

3.3 Literature based comparative study

Following recent studies on DAL TFTs, a brief analysis was carried out to define the active layer thicknesses for the transistors fabricated in this work. In 2021, M.M Billah et al. [45] and J. B. Kim et al. [46], both from the same research group, showed their self-aligned coplanar TG TFTs with a dual-channel architecture could achieve higher μ_{FE} than single-channel ones, while maintaining a positive V_{TH} and low I_{OFF}. In their study, they compared a single channel a-IZO layer of 16 nm with a dual channel of a-IZO and a-IGZO stack of 16 nm and 10 nm, respectively.

Based on this work, we started by fabricating a SAL TFT of only a-IZO film (**SAL_IZO**) with 26 nm, a single active layer of a-IGZO film (**SAL_IGZO**) with 26 nm, and two types of dual active layers with a total thickness of 26 nm: 16 nm of a-IZO and 10 nm of a-IGZO. The **DAL_A** sample places the a-IGZO layer at the interface with the GD, while the **DAL_B** sample positions the a-IZO layer near that interface.

From Figure 2, it is evident that the SAL_IZO, DAL_A and DAL_B devices do not exhibit a proper turn-off state, as the channel remains conductive even under strongly negative V_{GS}. This behaviour suggests that the a-IZO film is a degenerately doped semiconductor, in which the Fermi level resides within the CB due to the high concentration of free carriers, limiting the gate's capacity to fully modulate the channel. In contrast, the SAL_IGZO device demonstrates superior control of channel conduction, with a clearer transition between operating regions.

The resistivity values in Table 3, extracted from the source/drain conduction path of the TFTs, confirm that the higher conductivity of a-IZO film dominates the behaviour of DAL devices, regardless of its position in the layer stack. Based on these findings, we hypothesize that, i) the a-IZO yields active layers with excess carriers and/or ii) the thickness proportion of IGZO/IZO is unsuitable for the specific electrical characteristics of these films. Thus, it was decided to resort to the base process at CENIMAT and modify it to include very thin layers of IZO 2 in both DAL_A and DAL_B configurations.

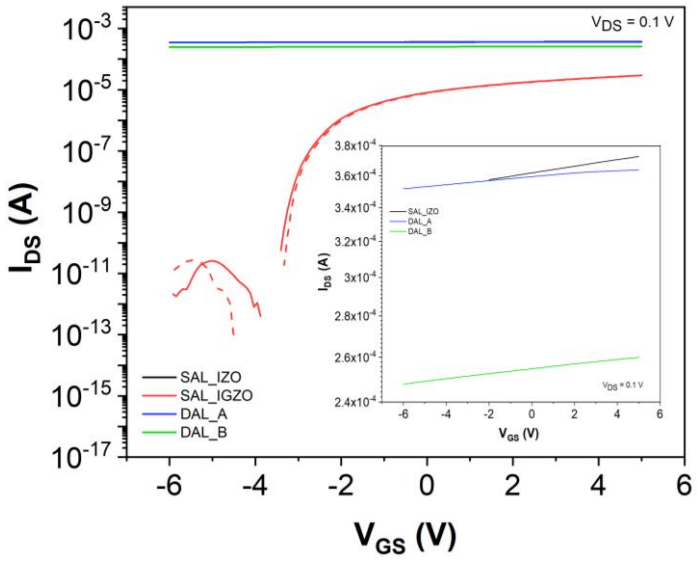


Figure 2 - Linear transfer characteristic curves of SAL and DAL TFTs, with *W/L* = 320/20 µm/µm. The full and dashed lines represent the forward and backward sweep, respectively. The inset shows an amplified view of the linear transfer curves for the SAL_IZO and DAL devices.

Table 3 - Bulk resistivity (ρ) values for SAL_IZO sample and the DAL samples.

Samples	ρ (Ω.cm)
SAL_IZO	1.01×10^{-2}
DAL_A	7.70×10^{-3}
DAL_B	9.66×10^{-3}

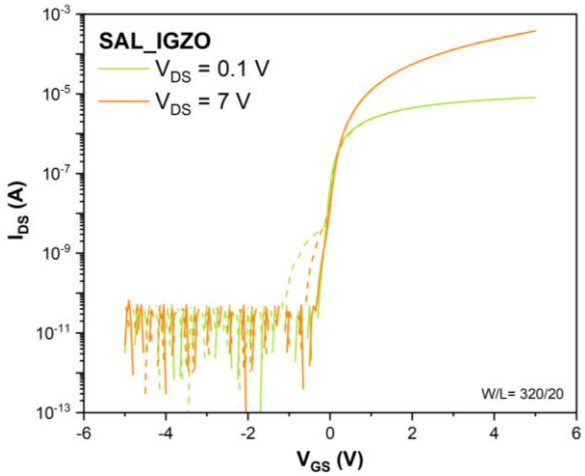
3.4 a-IGZO SAL with 40 nm of active layer

The study of a-IGZO films was conducted based on previous studies carried out at CENIMAT. This SAL device has an active layer of 40 nm with an a-IGZO film with an atomic ratio In:Ga:Zn = 2:1:1 and the sample were fabricated without a passivation layer.

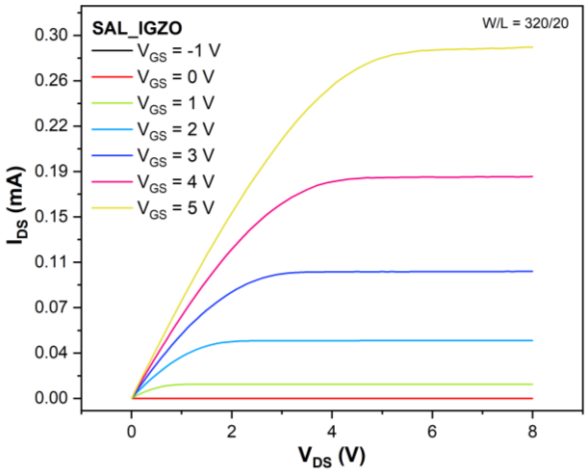
Based on Figure 3 (a) and (b), the SAL_IGZO devices with a 40 nm active layer exhibits a regular characteristic, with a discernible transition between depletion and accumulation regimes, with minimal variation between linear and saturation modes. The devices present minimal clockwise hysteresis, with $\Delta V_{ON} = (0.48 \pm 0.34)$ V. Figure 3 (c) demonstrates that the hump in the reverse-sweep transfer is a sweep dynamics/bias stress artefact, given that its magnitude decreases as the V_{GS} step increases (transfer acquisition takes less time), the hump on the reverse sweep is diminished. The metrics, Table 4, for the SAL_IGZO devices are as follows V_{TH} close to 0 V, a V_{ON} -0.31 V, and an μ_{FE} of ~20 cm²/V·s. In addition, the device shows a low off current (~10 pA), a high on/off ratio (~10^6), and a *SS* ~ 0.1 V/dec, all of which typical values for a-IGZO TFTs [24].

These results confirm that this active layer thickness provides both good switching behaviour and sufficiently high carrier transport, making it a suitable reference for future comparisons of results. For this reason, the total thickness of the active layer was kept at 40 nm in the subsequent studies on DAL TFTs.

(a)



(b)



(c)

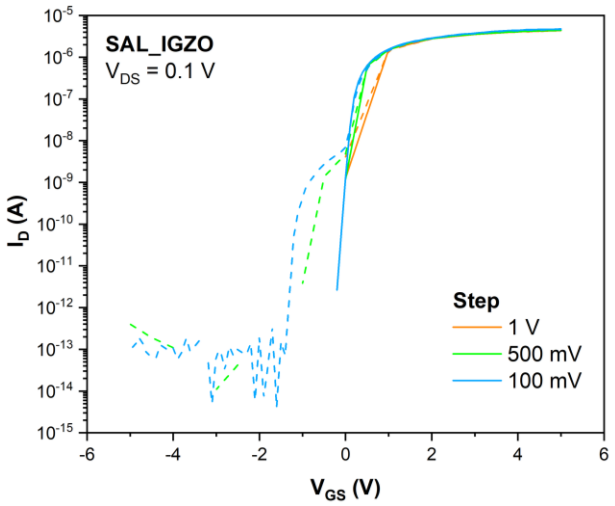


Figure 3 - SAL_IGZO characteristic curves for W/L = 320/20 µm/µm. The full and dashed lines represent the forward and backward sweep, respectively. (a) Linear and saturation transfer; (b) Output; (c) Linear transfer at V_{DS} = 0.1 V using different V_{GS} step sizes.

Table 4 -Average electrical parameters for SAL_IGZO.

TFT parameters	SAL_IGZO
V_{TH} (V)	-0.04 ± 0.12
V_{ON} (V)	-0.31 ± 0.12
μ_{FE} (cm²/V.s)	19.9 ± 1.18
μ_{sat} (cm²/V.s)	18.2 ± 2.51
SS (V/dec)	0.10± 0.03
Off current (A)	$(2.72\pm1.61)\times10^{-11}$
On-Off ratio	$(1.10\pm2.02)\times10^{6}$

In addition, bias-stress tests are essential to assess the operational stability of AOS TFTs. Under PGBS, the SAL devices (transfer curves in Figure A. 3 (a) of Appendix A.4) show clear positive shift on the V_{TH} during stress phase, although the lack of a passivation layer develops humps in the subthreshold region that grow with stress time and largely subside after recovery phase (Figure A. 3 (b) in Appendix A.4). This behaviour is consistent with a two channel scenario in unencapsulated devices: ambient H_2O/O_2 species adsorb on the back channel, creates more charging surface states and a parasitic conduction path that runs in parallel with the front gate induced channel. Back-channel passivation is known to suppress both the hump and the some amount of the bias-induced ΔV_{TH} [47]. Under NGBS, the SAL devices (transfer curves in Figure A. 3 (c) of Appendix A.4) show a clear negative shift of the transfer curves during stress, and an efficient recovery process (Figure A. 3 (d) in Appendix A.4)).

Figure 4 shows that, under PGBS, the SAL_IGZO reference undergoes a positive V_{TH} shift that grows with stress time, reaching ΔV_{TH} = 2.25 V after 60 minutes. During recovery, the shift partially relaxes to ΔV_{TH} = 1.83 V after 60 minutes. For NGBS test the device ΔV_{TH} drifts negatively to – 2.00 V after 60 minutes. In the beginning of the recovery phase, a sharp extra negative transient appears (ΔV_{TH} = - 3.05 V), followed by slow relaxation, ΔV_{TH} = - 2.09 V after 60 minutes. Supposedly, good quality AOS TFTs should show little to none NGBS instability, because a-IGZO has no significant hole concentration and hole injection into the GD is energetically unfavorable in the dark, the dominant process is limited electron de-trapping, so only small, often reversible negative shifts are expected [42]. In our case, the large negative drift is best explained by exposure of the backchannel to air during stress measurements. More concretely the presence of H_2O in the back-channel (adsorbed from air) promotes donor-like surface states and thus supply electrons to the active layer, effectively shifting $V_{TH.}$ negatively [42]. Consistent with this interpretation, when NGBS measurements are performed in vacuum (0.5 mbar) the negative shift is strongly suppressed (Figure 4 and transfer curves in Figure A. 3 (e) and (f) of Appendix A.4), indicating that the anomaly is atmosphere-induced rather than intrinsic to hole transport in a-IGZO and GD.

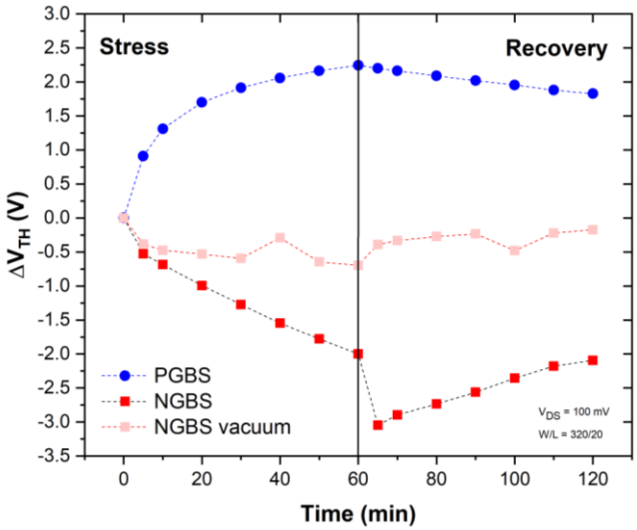


Figure 4 - ΔV_{TH} for the SAL_IGZO TFT for different stress and recovery times, for W/L = 320/20 µm/µm, under PBGS and NGBS.

3.5 DAL TFTs: a-IZO thickness and active layer stack

As previously stated, and according to the model proposed by Wager et al.[1], the most favourable mobility in DAL TFTs is achieved by placing the high-mobility semiconductor (a-IZO) further away from the GD/SC interface, while ensuring that this layer remains as thin as practicable. Contrarily, the most widely accepted methodology for DAL TFTs places the high-mobility semiconductor closer to the G/GD interface (see subsection 1.3.1). To clarify the underlying DAL mobility-enhancement mechanism, both architectural approaches were experimentally implemented in this work. Based on the trends observed in the previous chapter, the study begins with thin a-IZO layers in both configurations. All of these DAL TFTs were fabricated without a passivation layer.

3.5.1 Impact of 1 nm a-IZO

To begin studying the DAL structures, 1 nm of a-IZO film was incorporated in the DAL stack. From an initial analysis, the electrical performance of the DAL_A_1 and DAL_B_1 (Figure 5) reveals that both devices show regular switching behaviour, though with distinct characteristics. Figure 5 (a) and (c) showcase the transfer curves of DAL_A_1 and DAL_B_1 devices, respectively, in both linear and saturation regimes. The output curves (Figure 5 (b) and (d)), show the expected saturation behaviour, and I_{DS} of the same order of magnitude of SAL_IGZO under equal bias conditions.

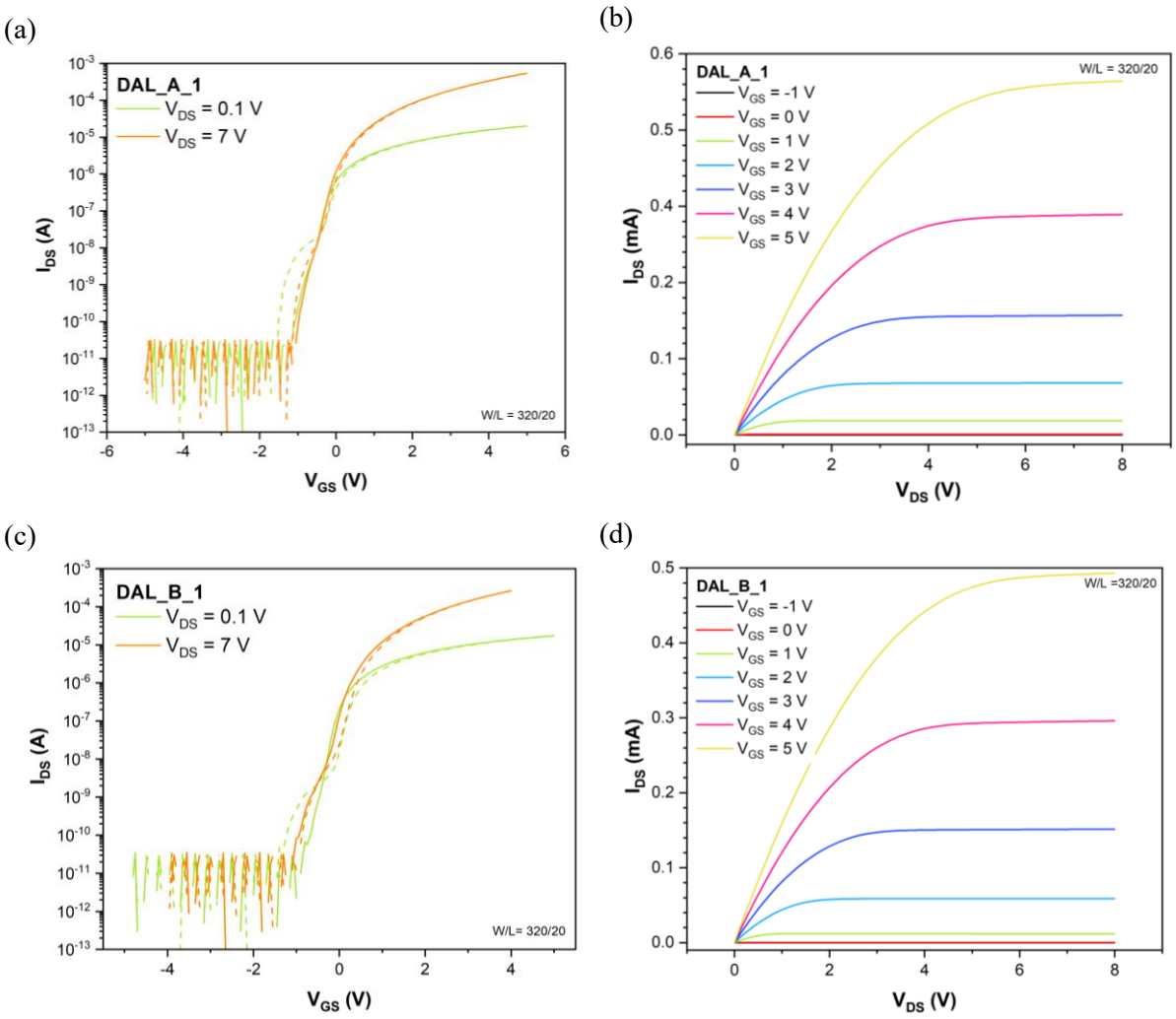


Figure 5 - DAL characteristic curves for W/L = 320/20 µm/µm. The full and dashed lines represent the forward and backward sweep, respectively. (a) DAL_A_1 linear and saturation transfer; (b) DAL_A_1 output; (c) DAL_B_1 linear and saturation transfer; (d) DAL_B_1 output.

Figure 6 compares the transfer characteristics of the SAL_IGZO, DAL_A_1, and DAL_B_1 devices and the μ_{FE} curves. From Figure 6 (b) is clear that DAL and SAL devices present similar curves shapes. Numerical data for this comparison can be found in Table 5. A difference in V_{ON} is observed among the three structures. The SAL_IGZO presents the most positive values, consistent with its single-channel configuration due to its lower carrier density in the active layer, compared to DAL devices. In contrast, both DAL structures present a shift in V_{ON} towards more negative voltages, which can reflect the influence of the ultrathin a-IZO layer. Moreover, both DAL structures exhibit an increase in SS compared to

the SAL device, along with a greater variation in this parameter. Since smaller *SS* values indicates good interface between GD/SC with smaller trap densities [35], the observed degradation can be attributed to an increase of interface states due to the introduction of the a-IZO layer and to non-uniform charge carrier distribution along the active layer and throughout the sample, since the 1 nm a-IZO film is unlikely to form a continuous layer. Regarding the mobility performance, the DAL structures present a slight improvement in μ_{FE}, raizing values from 19.9 cm^2/V.s (SAL_IGZO) to 21.5 cm^2/V.s and 23.5 cm^2/V.s, for DAL_A_1 and DAL_B_1, respectively. For the μ_{sat} the same behaviour is shown, the DAL devices have slight improvements than the SAL device.

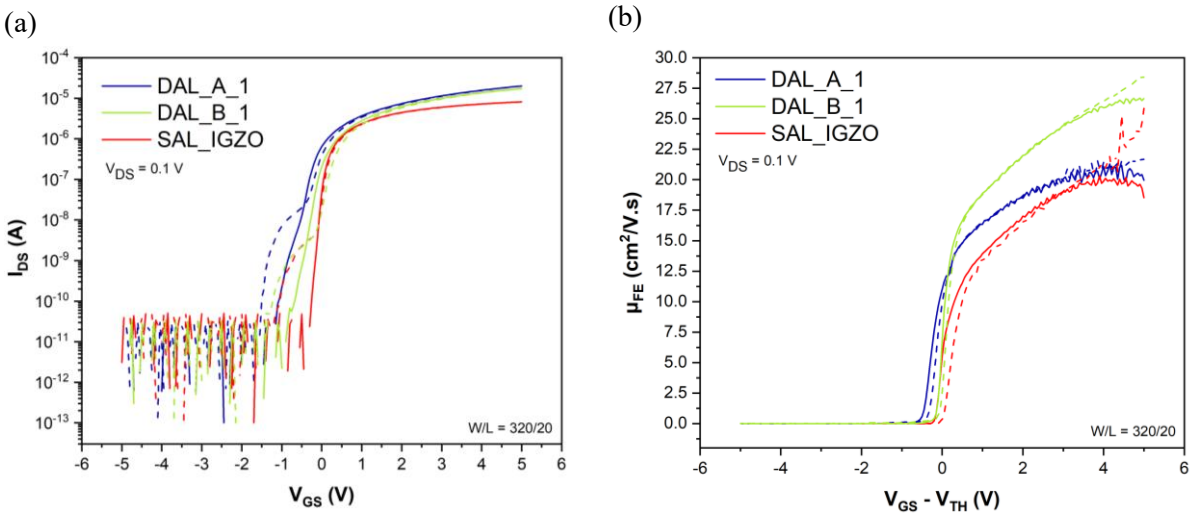


Figure 6 – In linear regime (V_{DS} = 0.1 V) for SAL_IGZO, DAL_A_1, and DAL_B_1 devices with *W/L* = 320/20 µm/µm. The full and dashed lines represent the forward and backward sweep, respectively. (a) Linear transfer characteristics; (b) Field effect mobility

Table 5 - Comparative analysis of the average parameters for SAL_IGZO, DAL_A_1, and DAL_B_1 devices.

TFTs parameters	V_{TH} (V)	V_{ON} (V)	μ_{FE} (cm^2/V.s)	μ_{sat} (cm^2/V.s)	SS (V/dec)	Off current (A)	On-Off ratio
DAL_A_1	-0.23±0.13	-1.08±0.26	21.5±2.72	23.5±1.31	0.19±0.11	(3.80±2.15)×10^{-11}	(4.58±5.62)×10^5
DAL_B_1	-0.05±0.06	-0.94±0.25	23.5±1.97	25.0±1.16	0.18±0.04	(3.65±1.41)×10^{-11}	(4.82±2.33)×10^5
SAL_IGZO	-0.04±0.12	-0.31±0.12	19.9 ± 1.18	18.2±2.51	0.10±0.03	(2.72±1.61)×10^{-11}	(1.10±2.02)×10^6

For the off-current, DAL devices exhibit Off current in the same order of magnitude (~ 10^{-11}) compared to SAL_IGZO, yet the On-off ratios are slightly worse. This follows from the higher *SS* and V_{ON} shifts in the DALs, which raise subthreshold current and reduce effective drive at a given overdrive.

Overall, these results indicate that although the DAL configurations, particularly DAL_B_1, show slightly higher mobilities with a less negative V_{ON} compared to DAL_A_1, the improvement in mobility is not significant when compared with the SAL_IGZO reference. On the other hand, deterioration is observed in other parameters, such as *SS* and Off current. Therefore, the introduction of a 1 nm a-IZO layer does not bring a clear performance advantage. Furthermore, considering that 1 nm of a-IZO was deposited by sputtering, it is likely that the deposition time was insufficient to ensure a continuous and uniform film, which may further compromise device performance and increase variability (further discussion provided ahead in subsection 3.5.5).

3.5.2 Impact of 2 nm a-IZO

Building on the previous analysis with 1 nm of a-IZO, the study was extended to DAL structures incorporating a 2 nm a-IZO layer. The motivation for this increase in thickness lies in the potential improvement of film continuity and uniformity, since ultrathin sputtered layers may not always form homogeneous coverage.

Figure 7 confirms that the DAL devices with 2 nm of a-IZO operate as functional TFTs, exhibiting the expected transfer and output characteristics. The transfer curves (Figure 7 (a) and (c)) show that both DAL_A_2 and DAL_B_2 present well defined switching behaviour, while the output characteristics (Figure 7 (b) and (d)) demonstrate proper channel modulation and clear current saturation with increasing gate bias, confirming effective channel formation in both structures.

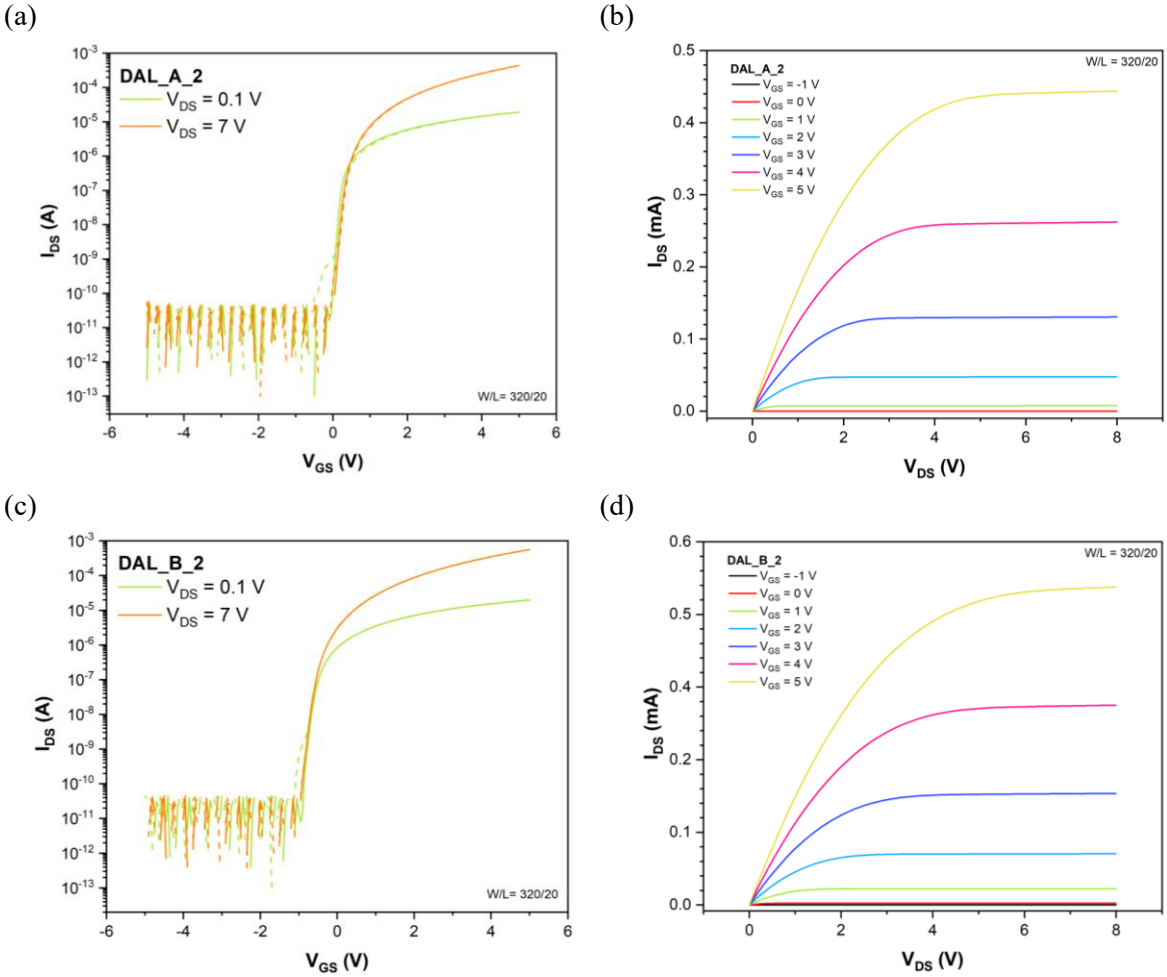


Figure 7 - DAL characteristic curves for *W/L* = 320/20 µm/µm. The full and dashed lines represent the forward and backward sweep, respectively. (a) DAL_A_2 linear and saturation transfer; (b) DAL_A_2 output; (c) DAL_B_2 linear and saturation transfer; (d) DAL_B_2 output.

Figure 8 show the transfer curves of DAL_A_2 and DAL_B_2 in comparison with SAL_IGZO. It is visible that the V_{ON} of DAL_A_2 remains very similar to that of the SAL reference, while DAL_B_2 exhibits a modest shift to more negative values (V_{ON} = - 1.18 V), being consistent with a higher carrier density at the GD/SC interface when the a-IZO is placed adjacent to the GD. Figure 8 (b) shows curves

with similar shapes and indicates that both DAL do not demonstrate improvement in μ_{FE} relative to SAL devices.

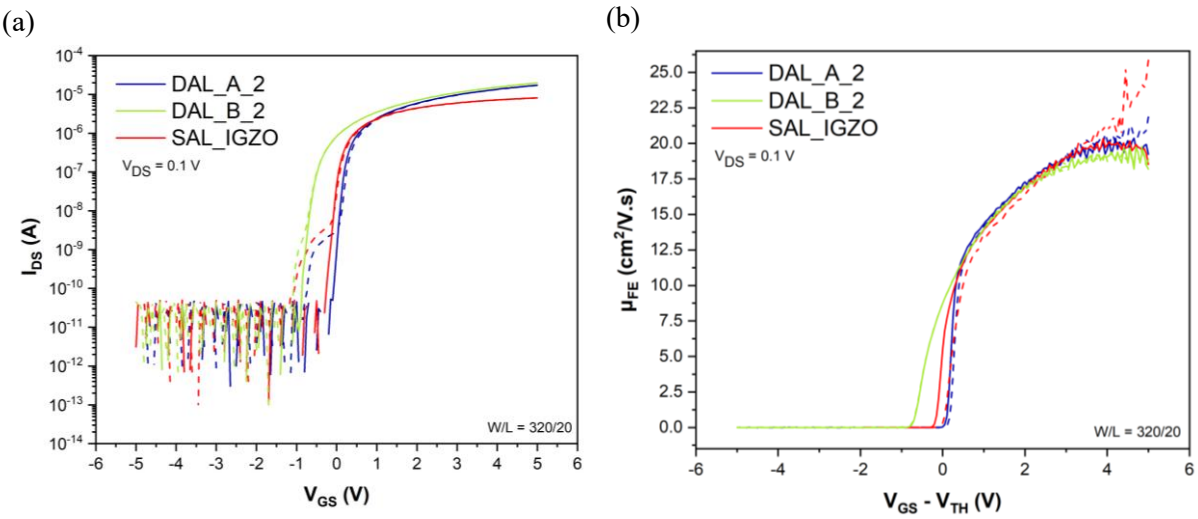


Figure 8 - Linear transfer characteristic curves at V_{DS} = 0.1 V for SAL_IGZO, DAL_A_2, and DAL_B_2 devices with W/L = 320/20 µm/µm. The full and dashed lines represent the forward and backward sweep, respectively. (a) Linear transfer characteristics; (b) Field effect mobility.

In terms of V_{TH}, whereas the SAL remains close to zero, DAL_A_2 shifts slightly positively, and DAL_B_2 shifts negatively. Whilst these variations are not highly significant, they do serve to confirm that the introduction and positioning of the a-IZO layer can subtly influence the onset and threshold behaviour of the devices. Comparing the electrical parameters of the devices in Table 6, it is clear that the implementation of a 2 nm a-IZO layer does not provide any significant enhancements. The μ_{FE} and μ_{sat} remain essentially unchanged across the samples. Larger SS values are shown for the DAL structures, especially in DAL_B_2. As previously mentioned, this increase can be attributed to the interface states introduced by the a-IZO layer, resulting in less uniformity in the charge carrier distribution in the active layer [48], The improvement from 1 nm to 2 nm is consistent with better continuity of the a-IZO layer, so this affect is less visible with 2 nm than with 1 nm, i.e the SS is higher for DAL_B_1 than for DAL_B_2. Moreover, DAL_A_2 presents lower SS (0.12 V/dec) than DAL_B_2 (0.17 V/dec), as DAL_A_2 has a-IGZO at the interface with the gate dielectric. Regarding, Off-current DAL devices exhibit the same order of magnitude (~ 10^{-11}) than SAL.

Table 6 - Comparative analysis of the average parameters for SAL_IGZO, DAL_A_2, and DAL_B_2 devices.

TFTs parameters	V_{TH} (V)	V_{ON} (V)	μ_{FE} ($cm^2/V.s$)	μ_{sat} ($cm^2/V.s$)	SS (V/dec)	Off current (A)	On-Off ratio
DAL_A_2	0.29±0.11	-0.08±0.23	20.25±2.19	22.0±0.93	0.12±0.03	(2.24±1.43)×10^{-11}	(8.02±2.88)×10^5
DAL_B_2	-0.65±0.11	-1.18±0.22	19.71±4.59	21.6±2.38	0.17±0.04	(4.10±2.95)×10^{-11}	(5.85±5.16)×10^5
SAL_IGZO	-0.04±0.12	-0.31±0.12	19.9 ± 1.18	18.15±2.51	0.10±0.03	(2.72±1.61)×10^{-11}	(1.10±2.02)×10^6

Summarizing, positioning of the a-IZO film in the structure is found to produce minor alterations in electrical parameters. Placing a-IZO film at the GD interface increases the interfacial electron density and shifts V_{ON} to negative values. In contrast, placing the a-IGZO film at the interface, interfacial electron density is lower, preserving the V_{ON} close to zero and lower SS values.

Thus, although 2 nm ensures more uniform coverage than 1 nm (further discussion provided ahead in subsection 3.5.5), its incorporation does not yield a clear performance benefit compared with the SAL_IGZO. This outcome is consistent with the limits of RF-sputtering at low thickness; films tend to grow via nucleation followed by coalescence and subsequent thickness grow. For 1 or 2 nm depositions, the short deposition time limited the film coalescence, leaving a partially discontinuous interface that increases trap density and degrades *SS* [49].

3.5.3 Impact of 5 nm a-IZO

Finally, the DAL study was extended to devices incorporating a 5 nm a-IZO film layer. Figure 9 presents the electrical characteristics of DAL_A_5 and DAL_B_5. The transfer curves (Figure 9 (a) and (c)) show that when the a-IZO thickness is 5 nm, the contribution of the a-IZO layer to the TFT performance becomes significantly more pronounced. Specifically, both DAL_A_5 and DAL_B_5 display characteristic humps in the transfer characteristics, which can be attributed to the coexistence of two conduction paths: one associated with the a-IGZO layer and another with the a-IZO layer. According to Wager et al. [1], mobility is maximized when the higher-mobility layer (a-IZO) is placed the furthest away from the GD and both layers are kept very thin (short-base). Our results do not showcase that optimization scenario: for the DAL_A_5 structure, a continuous a-IZO path forms, and parallel-channel conduction emerges, hence the strong hump-like characteristics (with a current level of ~ 10^{-7} A for V_{DS} = 0.1V) in both forward and reverse sweeps. Moreover, in the DAL_B_5 configuration (with the a-IZO as bottom channel layer), while the a-IGZO top layer contributes little to the subthreshold behavior, thereby suppressing the hump effect (lower current level of ~ 10^{-8} A for V_{DS} = 0.1V) compared to DAL_A_5. Consistently, DAL_A_5 exhibits a much larger hump than DAL_B_5 because the 5 nm top a-IZO behaves as a parasitic back-channel that turns on in parallel with the gate-controlled channel, producing a two-step onset. In DAL_B_5, placing a-IZO at the GD interface puts it under direct electrostatic control, so turn-on is essentially single-step and the hump is markedly suppressed across both sweep directions and V_{DS}.

Moreover, also from Figure 9 (a) and (c), it is possible to observe that DAL_A_5 devices show a more pronounced difference in the V_{ON} for linear and saturation regimes, when compared to DAL_B_5. This phenomenon is widely reported for short-channel FETs (L < 5-10 μm for AOS TFTs [50], [51]) and it is known as drain-induced barrier lowering (DIBL), meaning that the drain electric field poses an influence on the onset gate voltage for channel formation, leading to an earlier turn on at higher drain biases. Given that the *L* of the devices shown herein is 20 μm and that other DAL and SAL structures did not present this behaviour, we hypothesize that this DIBL-like effect arises from the DAL structure itself, i.e. a-IZO as the backchannel material. This same effect has been reported for plasma-enhanced chemical vapour deposition (PECVD) SiO_2 passivated a-IGZO TFTs [51]. The DIBL-like effect is attributed to the inhomogeneity of donor states at the top a-IGZO interface arising from the interaction of PECVD precursors/plasma species with the a-IGZO backchannel, which creates regions with significantly different effective charge densities. As a result, the channel forms a series/parallel network of conductive regions that collectively establish the electron pathway from source to drain, which lead to the stronger influence of drain bias in V_{ON}, as well as degradation of *SS* and, potentially, the formation of more pronounced hump-like transfer characteristics.

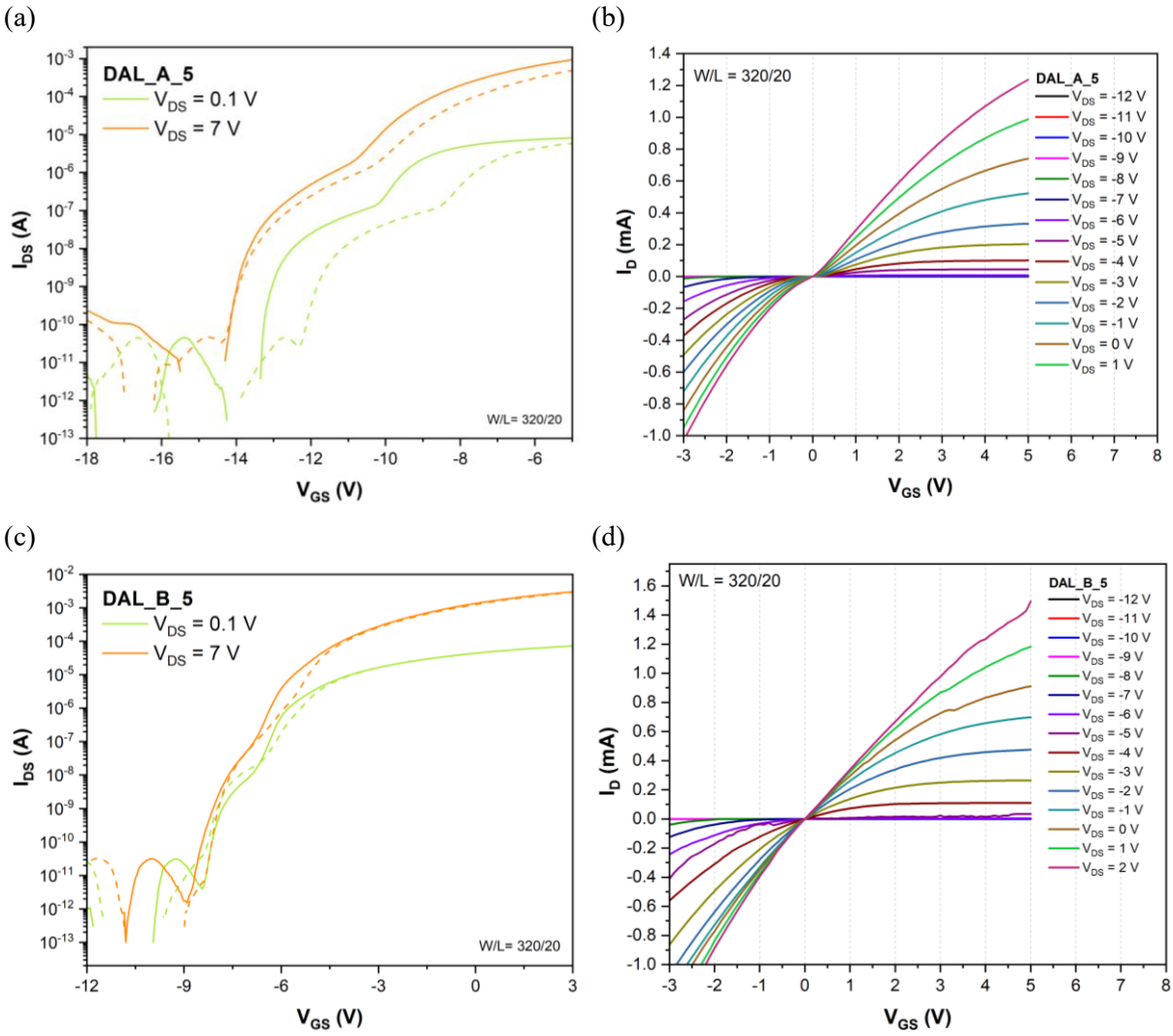


Figure 9 - DAL characteristic curves for *W/L* = 320/20 µm/µm. The full and dashed lines represent the forward and backward sweep, respectively. (a) DAL_A_5 linear and saturation transfer; (b) DAL_A_5 output; (c) DAL_B_5 linear and saturation transfer; (d) DAL_B_5 output.

The output curves (Figure 9 (b) and (d)) confirm that both configurations yield ohmic contacts. Compared with DAL_A_5, DAL_B_5 delivers a similar drive current at a given V_{GS}. The fluctuations observed in the output curve of DAL_B_5 are attributable to measurement artefacts, i.e. vibrations of the tips.

Figure 10 (a) evidence the negative shift of the V_{ON} in the DAL devices compared with the SAL_IGZO. Analyzing the electrical parameters of the different devices presented in Table 7, distinctions emerge between the DAL and SAL structures. In terms of mobility, DAL_B_5 exhibits a remarkable enhancement, with μ_{FE} ~ 47 cm^2/V.s, twice the value obtained for SAL_IGZO. This result proves that when a-IZO is placed close to the GD/SC interface, it provides enhanced carrier transport. The μ_{sat} follows a similar trend, reinforcing the stronger transport contribution of the a-IZO bottom layer in DAL_B_5.

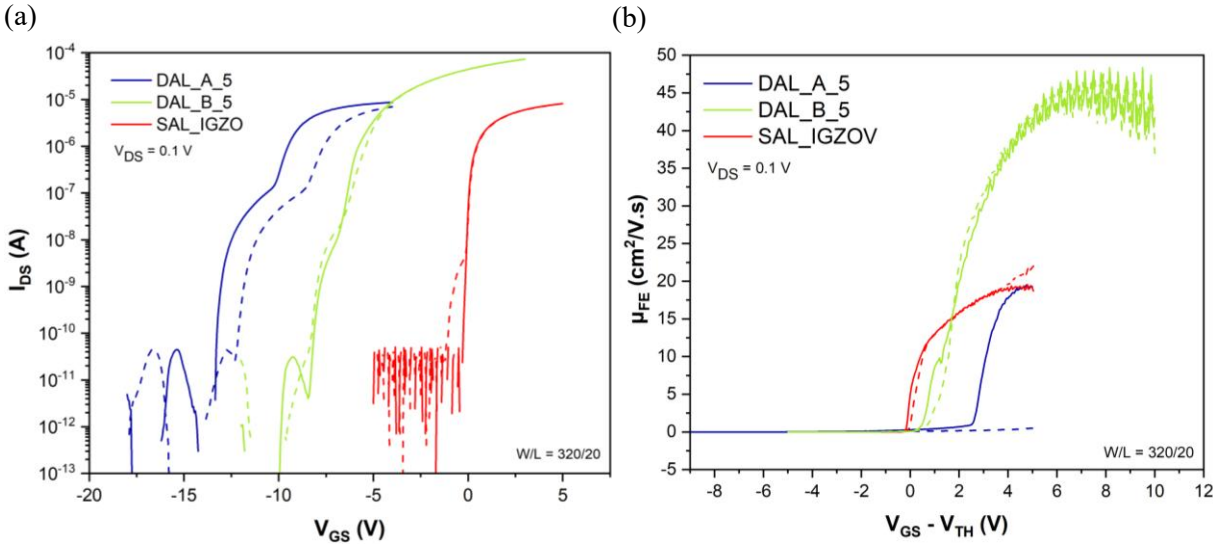


Figure 10 - Linear transfer characteristic curves at V_{DS} = 0.1 V for SAL_IGZO, DAL_A_5, and DAL_B_5 devices with W/L = 320/20 µm. The full and dashed lines represent the forward and backward sweep, respectively. (a) Linear transfer characteristics; (b) Field effect mobility.

In contrast, DAL_A_5 shows μ_{FE} values close to those of the SAL device, confirming that in this configuration channel transport is still primarily governed by a-IGZO, with the 5 nm a-IZO layer acting as a secondary channel. According to the analytical model proposed by Wager et al. [1], the 'short base' channel thickness regime occurs when the semiconductor channel layer thickness (t) is less than or equal to the maximum accumulation layer thickness ($x_{acc\ max}$), defined as 2.22 times the Debye length (L_D), which is given by $L_D = \sqrt{\frac{\varepsilon_S \varepsilon_0 k_B T}{q^2 N_D}}$, where ε_S is the semiconductor relative dielectric constant, ε_0 is the vacuum permittivity, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge and N_D is the bulk donor concentration. The $N_{D,IGZO}$ = - 9×10^{16} cm^{-3} and $N_{D,IZO}$ = - 1.91×10^{17} cm^{-3}, obtained through Mott-Schottky analysis of C-V data of the SAL_IGZO and DAL_A_5, respectively (performed in collaboration with another researcher in the team – analysis present in Appendix A.5), assuming $\varepsilon_{IZO} = 13.6$ and $\varepsilon_{IGZO} = 12.8$ [1], were obtained $L_{D,IZO}$ = 10.1 nm and $L_{D,IGZO}$ = 14.3 nm, which in turn yields $x_{acc\ max,IZO}$ = 22.4 nm and $x_{acc\ max,IGZO}$ =31.6 nm. Given that t_{IZO} = 5 nm and t_{IGZO} = 35 nm, the a-IZO layer satisfies the 'short base' criteria, while the a-IGZO layer does not.

With t_{IZO} = 5 nm and $L_{D,IZO}$ = 10.1 nm, the a-IZO film is fully electrostatically controllable by the G field, therefore, placing IZO at the dielectric produces an accumulation layer directly within the high-mobility layer, explaining the observed mobility improvement for the DAL_B_5. In contrast, t_{IGZO} = 35 nm exceeds $L_{D,IGZO}$ = 14.3 nm, so the G field and carrier accumulation are confined to the a-IGZO, meaning that a-IZO is not under sufficient electrostatic control in DAL_A structure to provide a higher μ_{FE} (i.e the GD field is screened by the a-IGZO layer). Nevertheless, the addition of the a-IZO layer in both stacks increases the net electron density, causing the observed negative shift in V_{TH}.

However this DAL_A_5 device exhibits a higher μ_{sat}, compared with the SAL_IGZO, this behavior has already been reported on IGZO/IZO DAL TFTs where it has been proven that having a lower conductivity (a-IGZO) as bottom channel layer can generate higher μ_{sat} values, because the a-IZO film under the S/D contacts provides a low resistivity lateral path, easing carrier injection/spreading into the modulated a-IGZO channel, again cutting access resistance and raising the apparent μ_{sat} [52].

Regarding *SS*, for both DAL devices the values are not applicable (NaN), the subthreshold region is non-monotonic due to parallel IGZO/IZO conduction and trapping, producing multiple local slopes and sign changes in $d\log(I_{DS})/dV_{GS}$. As a result, a single *SS* is not physically meaningful.

The Off-currents of SAL_IGZO and DAL_A_5 devices present values on the same order, but DAL_B_5 exhibits lower values (~ 10^{-12} A), yet On-off ratios are much larger in DALs compared with SAL, driven mainly by their substantially higher I_{ON} within the measurement overdrive voltage.

Table 7 - Comparative analysis of the average parameters for SAL_IGZO, DAL_A_5, and DAL_B_5 devices.

TFTs parameters	V_{TH} (V)	V_{ON} (V)	μ_{FE} (cm^2/V.s)	μ_{sat} (cm^2/V.s)	SS (V/dec)	Off current (A)	On-Off ratio
DAL_A_5	-9.06±1.81	-13.3±2.61	20.44±5.09	30.07±3.29	NaN	(2.33±2.56)×10^{-11}	(9.54±0.15)×10^6
DAL_B_5	-6.48±0.70	-9.15±1.67	47.31±7.55	55.82±1.35	NaN	(6.93±5.38)×10^{-12}	(1.66±1.61)×10^7
SAL_IGZO	-0.04±0.12	-0.31±0.12	19.9 ± 1.18	18.15±2.51	0.10±0.03	(2.72±1.61)×10^{-11}	(1.10±2.02)×10^6

In conclusion, these results demonstrate that the positioning and thickness of the a-IZO and a-IGZO film is decisive. When positioning the a-IZO with 5nm as the bottom channel layer, it enhances carrier transport but with a trade-off in V_{ON}/V_{TH} shifting through negative values. Contrarily, when the a-IZO film is positioned as the top layer, it introduces dual-channel behaviour without providing significant transport gains, because the a-IGZO layer does not present a 'short base' channel thickness behaviour.

To further support these observations from the all DAL devices behaviour, the C-V characteristics were analyzed to evaluate how effectively each stack configuration enables charge accumulation in the active-layer. Figure 7 (a) and (b) show that devices with 1 nm and 2 nm a-IZO showed no noticeable V_{fb} shift, regardless of the DAL configuration, when compared with SAL_IGZO. In contrast, the DAL_B_5 device exhibited an accumulation behaviour similar to the SAL_IGZO reference, with a clear V_{fb} shift, consistent with the formation of a more effective conduction channel.

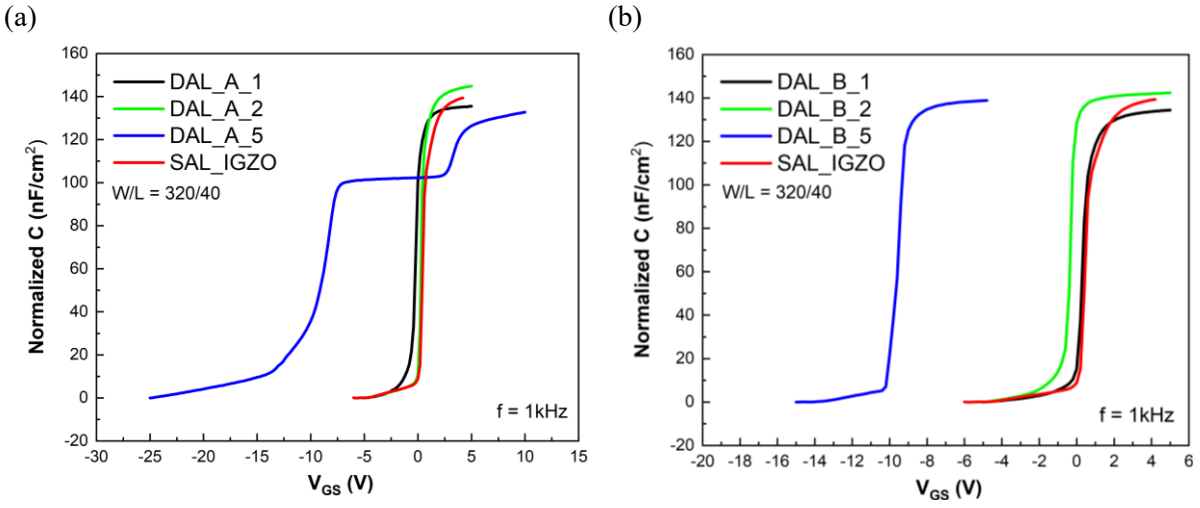


Figure 11 - Normalized capacitance–voltage (C–V) characteristics at 1 kHz for the DAL TFTs compared with the SAL_IGZO device with W/L = 320/40 µm.: (a) DAL_A configuration and (b) DAL_B configuration.

However, DAL_A_5 device indicates limited charge accumulation in the a-IZO layer. Its C–V curve exhibits an initial strong accumulation occurs in the a-IGZO layer, but incomplete because these layer screens part of the G field from the upper a-IZO layer (consistent with the previously discussed 'short-

base' criteria). These C–V results reinforce the conclusion that both the position and effective thickness of the a-IZO layer govern the degree of charge modulation and, ultimately, the performance of DAL TFTs.

3.5.4 Testing the reliability of DAL TFTs: PGBS

Bias-stress testing is essential for TFTs for circuitry applications. As an example: under PGBS, the AMOLED driving TFT must deliver a stable current throughout OLED emission, so any ΔV_{TH} directly impacts luminance uniformity [14]. Accordingly, bias-stress test were performed on the previously characterized DAL devices to evaluate their electrical stability and assess the influence of channel configuration on ΔV_{TH} behaviour.

From Appendix A.6 and A.7, Figure A. 7 and Figure A. 8 illustrate the time dependence of the transfer curves for DAL_A and DAL_B devices with 1 nm and 2 nm a-IZO layers, respectively, under PGBS. In both 1 nm and 2 nm samples, a rightward shift is clearly more pronounced in DAL_A configuration than DAL_B.

The comparison of PGBS between samples of 1 nm and 2 nm a-IZO film in Figure 12 , represents the time evolution of the ΔV_{TH}, showing that DAL_A_1, ΔV_{TH} = 2.32 V after 60 minutes of stress and DAL_A_2, ΔV_{TH} = 2.37 V after 60 minutes of stress, exhibit similarly behaviour than SAL_IGZO sample (ΔV_{TH} = 2.25 V). However, during recovery phase, DAL_A_1 shows a little stronger recovery than the other two samples. By contrast, DAL_B configuration shows a clear improvement in the stability of the TFTs, DAL_B_1 shows smallest ΔV_{TH} shift, ΔV_{TH} = 1.30 V after 60 minutes of stress and when the a-IZO layer is increased to 2 nm the shift is even smaller, DAL_B_2 shows a ΔV_{TH} = (0.27±0.10) V. For recovery both DAL_B samples presented a nearly returns to the initial state (ΔV_{TH} = (0.35±0.17) V).

Although the ultrathin a-IZO layer did not improve device performance in our earlier metrics, it clearly affects PGBS stability, concluding that placing a-IZO as bottom-layer improves bias-stress stability by lowering interface trap density [35], [42], whereas placing a-IGZO as bottom-layer electron trapping is not suppressed, so the device remains SAL-like. In addition, these results are consistent with a thickness/continuity effect of the ultrathin a-IZO layer: while 1 nm a-IZO is prone to discontinuous coverage, 2 nm a-IZO may be closer to a quasi-continuous film, hence the improved PGBS stability for the latter, providing a higher number of free carriers to fill GD/SC interfacial electron traps which are the main responsible for PGBS [45], [46].

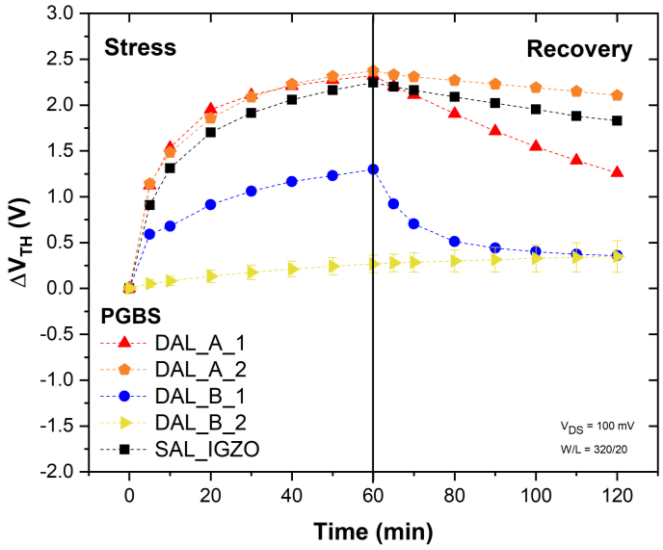


Figure 12 - ΔV_{TH} behaviour for 1 nm and 2 nm a-IZO for different stress and recovery times, for W/L = 320/20 µm/µm, under PBGS.

For the 5 nm-thick a-IZO film, from Appendix A.8, shows the time dependence of the transfer curves for DAL_A_5 sand DAL_B_5 device under PGBS. In stress phase, DAL_A_5 (Figure A. 9), exhibits a pronounced right shift, with a slower and incomplete recovery. In contrast, DAL_B_5 shows almost no measurable shift during the stress time. Regarding the dual-channel behaviour, for DAL_A_5 devices the 2nd derivative method does not yield an unambiguous threshold voltage (Figure A. 10 in Appendix A.8). We therefore assessed bias-stress stability using the shift of the turn-on voltage.

Figure 13 shows the time evolution of the ΔV_{ON} shift for DAL_A_5 and the ΔV_{TH} shift for SAL_IGZO and DAL_B_5. Under PGBS, DAL_A_5 shifts left, ΔV_{ON} = - 1.2 V after 60 minutes of stress, once the bias is released, ΔV_{ON} flips positive and ends near 1.60 V at the end of recovery phase, probably the a-IZO top layer promotes electron trapping in a-IZO/SD interface or in a-IGZO/a-IZO interface. DAL_B_5 presents exhibit nearly no ΔV_{TH} shift compared with SAL_IGZO, after 60 minutes of stressing ΔV_{TH} = - 0.10 V and at the end of recovery phase, ΔV_{TH} = -0.18 V.

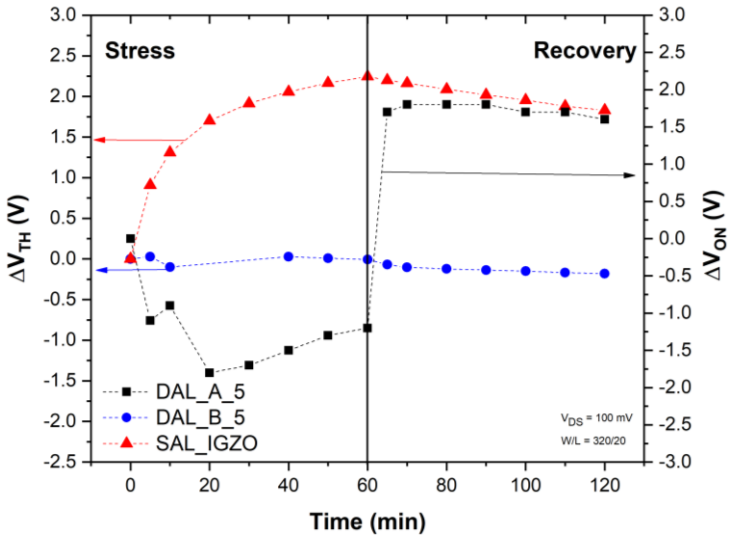


Figure 13 - ΔV_{TH} and ΔV_{ON} for DAL_A_5 and DAL_B_5 TFTs for different stress and recovery times, for W/L = 320/20 µm/µm, under PBGS.

Finally, it has finally been demonstrated that DAL provides a significant improvement when submitting bias-stress tests to study TFTs reliability. However, this enhancement is only observed when the higher mobility semiconductor (a-IZO) is placed near the GD interface, a channel is formed under direct gate control and interfacial trapping is suppressed, yielding minimal ΔV_{TH} during stress and small residuals after recovery. Furthermore, placing the a-IZO film near S/D interface performance and stability are compromised, for thinner and discontinuous films (1 and 2 nm) similar behaviours to SAL are shown, but for 5 nm thickness, this layer acts as a parasitic back channel, making V_{TH} extraction ambiguous and degrading stability.

3.5.5 a-IZO films conformality verification

In order to verify the continuity and conformality of the ultrathin a-IZO layers (1, 2 and 5 nm), STEM – EDS mapping was performed.

The EDS elemental maps, Figure 14, help confirm that as the thickness increases, so does the amount of In and Zn present in the film. Table 8 offers a quantitative analysis of the percentage of each element in each sample. It is evident that at 1 nm there is no Zn signal detected, indicating that the material consists of only minor atomic percentages of In, which is consistent with the phenomenon of discontinuous coverage. At 2 nm, there is an increase in both elements, indicating improvements in continuous coverage. At 5 nm, the maps present a greater quantity of both elements, suggesting the possibility of the formation of a continuous film The microstructural characterization trends provide corroboration of the device data. Improved coverage, DALs performance and stability are evident.

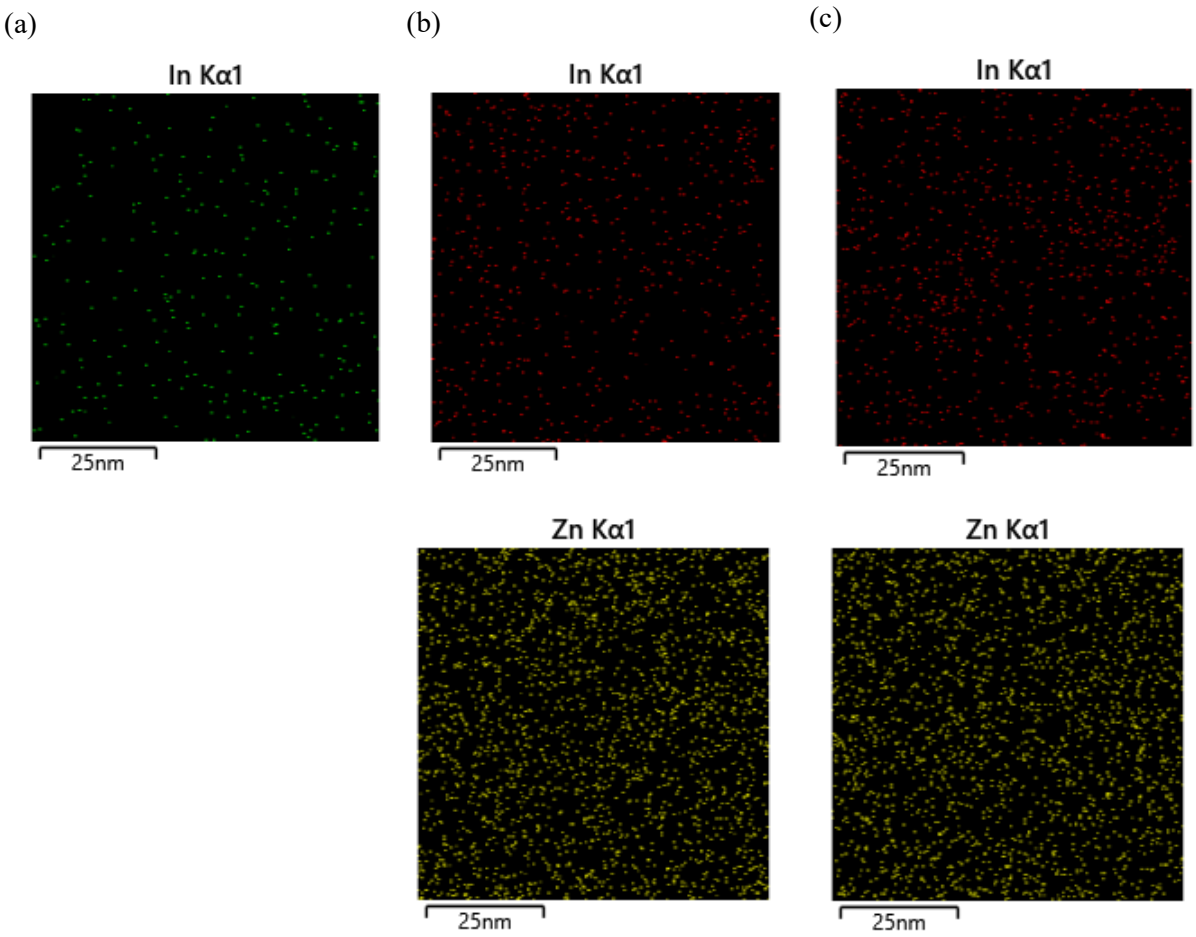


Figure 14 - EDS elemental maps of In and Zn for the a-IZO film with thicknesses of (a) 1 nm, (b) 2 nm and (c) 5 nm.

Table 8 - Quantitative atomic percentage of In and Zn element in each sample.

a-IZO thisckness	**1 nm**	**2 nm**	**5 nm**
In (atomic %)	0.10	0.41	0.87
Zn (atomic %)	0.00	0.03	0.04

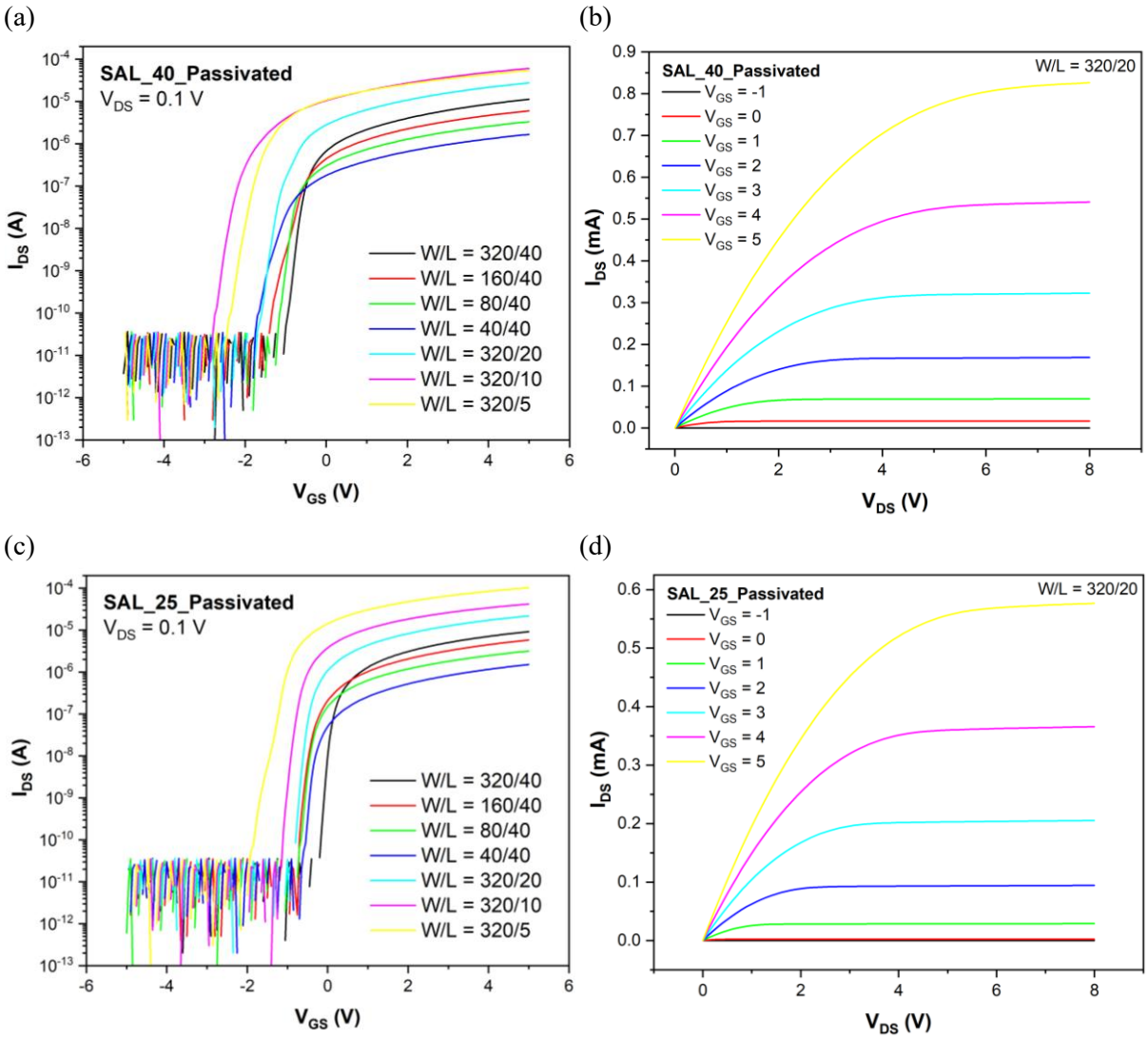
3.6 a-IGZO SAL active layer thickness variations

A systematic study of active-layer thickness in single-layer a-IGZO TFTs was performed as a complementary investigation aimed at guiding future optimization of DAL structures. Wager et al. [1] also suggest in their article that optimal mobility performance occurs when the low mobility semiconductor is employed further the GD/SC interface and made as thin as practicable. Thus, a-IGZO SALs with different active layer thicknesses were fabricated, including the encapsulation step, and characterized: with 40 nm that underwent semiconductor annealing for 17 hours (**SAL_40_Passivated**); with 25 nm (**SAL_25_Passivated**), 15 nm (**SAL_15_Passivated**) and 5 nm (**SAL_5_Passivated**). Given the relatively thin active layers, encapsulation was employed to prevent interactions with adsorbed H_2O and O_2 species at the backchannel and thus their influence on device metrics [53].

From the linear transfer curves of the different samples (Figure 15 (a), (c) and (e)), it is evident that the influence of transistor dimensions (*W/L*) on the V_{ON} is more pronounced in devices with thicker

active layers. For instance, SAL_40_Passivated shows a greater variation of V_{ON} across different *W/L* ratios, especially with variation in transistor length, while SAL_15_Passivated remains more stable, almost independent of geometry, except when L = 5 µm. This behaviour can be attributed to the larger channel volume in thicker layers, where scale effects become more evident. In devices with thicker active layers, the increased absolute value of oxygen vacancies and/or electron taps increase the sensitivity of the charge distribution to the effective channel geometry, making variations in *W/L* more impactful. In contrast, thinner active layers confine carriers closer to the dielectric interface of the gate, where electrostatic gate control dominates and suppresses geometric dependence [54], [55].

The output curves (Figure 15 (b), (d) and (f)) demonstrate well saturated behaviour from the samples, confirming good channel control, as the active layer thickness decreases the saturation current systematically drops, consistent with the reduced carrier density/volume conduction in thinner a-IGZO films.



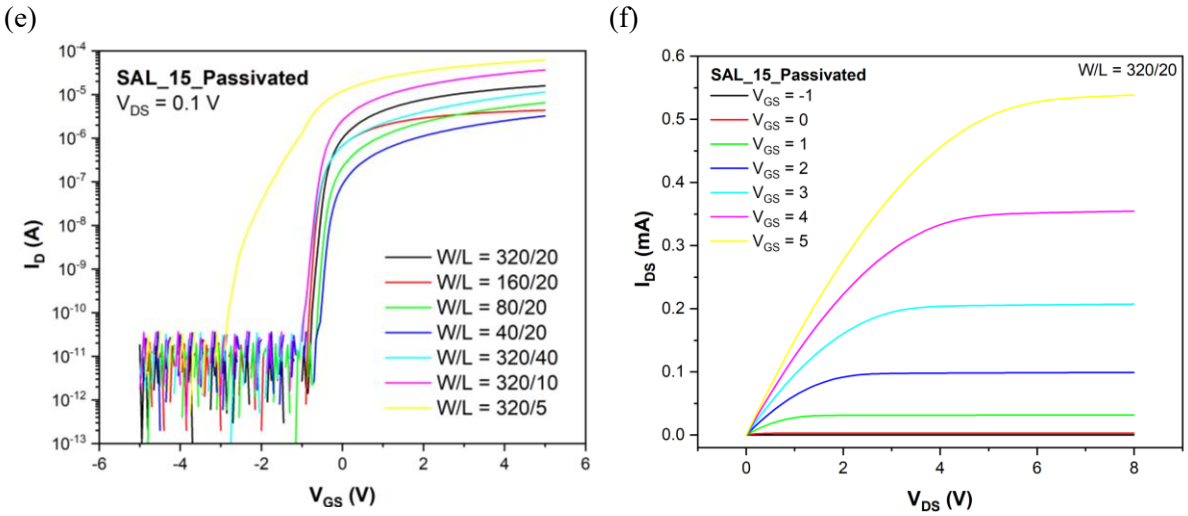


Figure 15 - Transfer characteristics at V_{DS} = 0.1 V for different W/L ratios and output characteristics at W/L =320/20 µm/µm (a) SAL_40_Passivated linear transfer curve; (b) SAL_40_Passivated output curve; (c) SAL_25_Passivated linear transfer curve; (d) SAL_25_Passivated output curve; (e) SAL_15_Passivated linear transfer curve; (f) SAL_15_Passivated output curve.

When this analysis was extended to SAL_5_Passivated, only preliminary data was obtained (Figure 16). This showed significantly degraded performance, with high noise and poor current modulation. While these results are less conclusive, they are consistent with the observed thickness dependence and further highlight that 5 nm (fabricated via sputter deposition) is not a viable thickness for well performing devices.

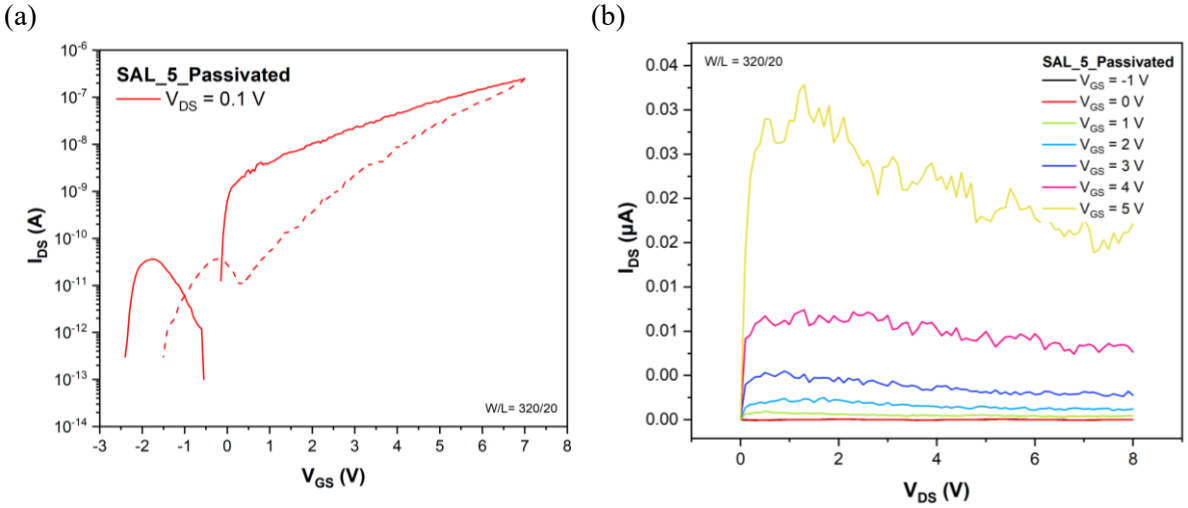


Figure 16 - SAL_5_Passivated characteristics for W/L = 320/20 µm/µm (a) Linear transfer at V_{DS} = 0.1 V; (b) Output.

Table 9 presents the comparison of the averaged electrical parameters of the different SAL samples (compiled from the values shown in Table A. 2, Table A. 3 and Table A. 4 in Appendix A.9). The results clearly indicate that with decreasing active layer thickness, thinner a-IGZO channels tend to shift positively V_{TH} and V_{ON}. This can be mainly attributed to the large absolute number of free electrons within

the oxide semiconductor volume. Consequently, μ_{FE} is expected to decrease with decreasing thickness; however, both SAL_40_Passivated and SAL_25_Passivated exhibit mobilities of approximately ~23 cm²/V·s. Reducing the channel thickness to 15 nm further decreases the mobility to ~17 cm²/V·s. A similar trend is observed for $\mu_{sat.}$ Although SAL_25_Passivated shows almost identical mobility to SAL_40_Passivated, the thinner channel achieves a significantly lower *SS* (0.14 V/dec vs. 0.23 V/dec), reflecting the higher ability of the gate field to fully modulate the entire active layer lower thicknesses. Regarding Off-current, the devices with 40 nm and 25 nm show similar off-currents on the order of 10^{-11}, whereas the device with 15 nm exhibits an order of magnitude decrease (~10^{-12} A).

Table 9 - Comparative analysis of the averaged parameters for the different SAL samples.

TFTs parameters	V_{TH} (V)	V_{ON} (V)	μ_{FE} (cm^2/V.s)	μ_{sat} (cm^2/V.s)	SS (V/dec)	Off current (A)	On-Off ratio
SAL_40_Passived	1.16±0.22	1.94±0.37	22.5±6.32	21.3±3.36	0.23±0.07	(2.85±0.99)×10^{-11}	(9.83±9.28)×10^5
SAL_25_Passived	0.45±0.20	0.98±0.68	22.6±1.97	23.5±2.98	0.14±0.08	(3.67±1.48)×10^{-11}	(8.63±0.10)×10^5
SAL_15_Passived	0.49±0.20	0.67±0.77	17.3±4.57	19.3±3.26	0.11±0.01	(3.24±2.06)×10^{-12}	(8.46±7.87)×10^6

In conclusion, when considering only the DC parameters, SAL_15_Passivated exhibits the best overall compromise, as it promotes improvements across all key electrical parameters, geometric variability, with only a slight degradation in mobility. Additionally, reducing the active layer thickness from 40 nm to 25 nm does not compromise performance, indicating that further increasing the thickness offers no significant benefit. These findings are consistent with the obtained $L_{D,IGZO}$ = 14.3 nm and $x_{acc\ max,IGZO}$ =31.6 nm. (subsection 3.5.3), highlighting that both 25 nm and 15 nm thick active layers provide better electrostatic control over the active layer, thus greatly reducing *SS.* Moreover, reduction in active layer thickness brings important technological advantages such as reduced deposition time, lower material consumption, and easier processing steps (e.g., semiconductor lift-off).

3.6.1 Effects of active layer thickness on stability

Figure A. 11 and Figure A. 12, from Appendix A.10, shows the time dependence of the transfer curves for the different SALs devices, except for SAL_5_Passivated, under PGBS and NGBS, respectively.

As illustrated in Figure 17 (a), the ΔV_{TH} for the SAL devices under PGBS is demonstrated for the stress and recovery phases. The largest ΔV_{TH} was observed for the SAL_15_Passivated sample (ΔV_{TH} 2.31 V after 60 minutes of stress), while the smallest ΔV_{TH} was noticed for the SAL_40_Passivated sample (ΔV_{TH} = 1.38 V after 60 minutes of stress). During the recovery phase, all TFTs partially relax, converging to 1.29 to 1.10V, respectively. Hence, the magnitude of ΔV_{TH} during PGBS for the a-IGZO SALs devices decreases with the increasing thickness of the active layer. This behaviour has already been reported for indium-gallium-tin oxide TFTs, and was attributed to fact that thicker films contain a lower number of OH acceptor-like traps and a higher proportion of oxygen-vacancy donors [56]. Additionally, thicker active layers can act as an effective barrier against ambient species, such as O_2 and H_2O molecules, limiting influence on the gate-induced accumulation at the GD/SC interface [56].

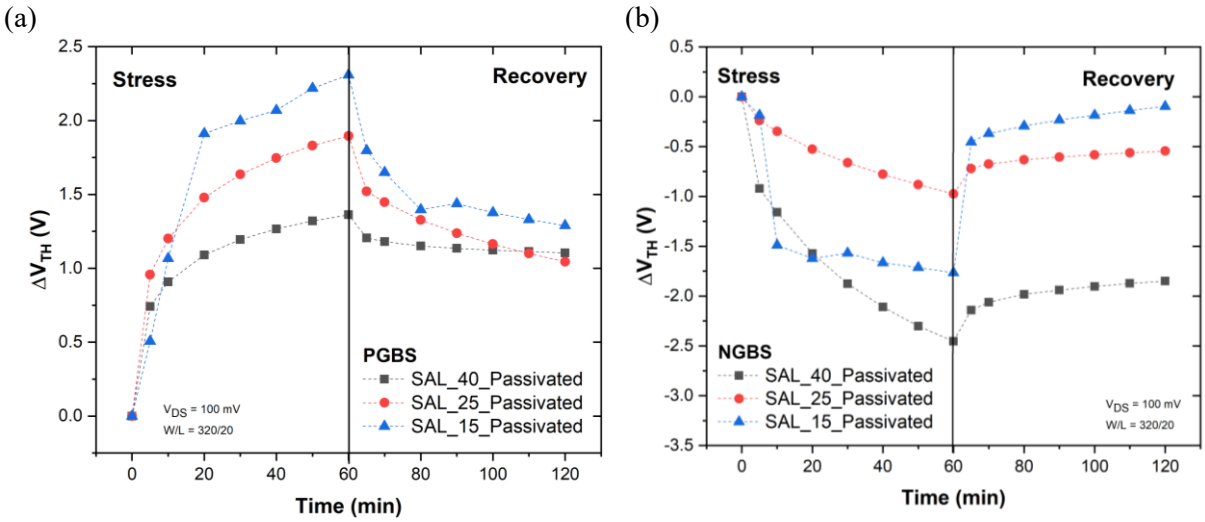


Figure 17 - ΔV_{TH} for the a-IGZO SAL TFTs with different active layer thicknesses for different stress and recovery times, for W/L = 320/20 µm/µm, under (a) PBGS and (b) NGBS.

Regarding NGBS, as previously mentioned it is well known that high-quality a-IGZO TFTs should not present any significant ΔV_{TH} during these tests. Figure 17 (b) shows that the largest shift occurs for SAL_40_Passivated (ΔV_{TH} = - 2.45 V after 60 minutes of stress), followed by SAL_15_Passivated (ΔV_{TH} = - 1.77 V after 60 minutes of stress), whereas the SAL_25_Passivated shows the smallest shift (ΔV_{TH} = - 0.97 V after 60 minutes of stress). During the recovery phase, SAL_40_Passivated and SAL_25_Passivated displays a smooth, moderate recovery with the smallest residual shift, instead SAL_15_Passivated shows a strong recovery toward less negative. The pronounced shift observed for SAL_40_Passivated can be correlated with passivation effects. There is a degradation of *SS* during stress, this parameter increases from ~0.14 V/dec at 0 min to ~0.22 V/dec after 60 min of stress, indicating the creation of additional trap states at the interface between the a-IGZO/parylene passivation film As previously demonstrated in section 3.4, such instabilities are not associated with donor state creation and/or hole injection into the gate dielectric (as the instability is suppressed in vacuum ambient), confirming that the degradation originates from upper interface with the passivation layer. Nevertheless, these traps introduced are not permanent, since *SS* recovers to its initial value (~0.14 V/dec at 120 min) [57]. On the other hand, for 25 and 15 nm the SS degradation is not noticeable during stress, with their transfer curves exhibiting parallel shifts, meaning that passivation effects are less pronounced in thinner layers.

Overall, although the magnitude of ΔV_{TH} should decrease as the active layer becomes thinner, the 25 nm film delivers the best NGBS stability among these samples. This can be explained by the fact that, unlike the 25 nm device, the SAL_15_Passivated sample shows an abrupt negative shift of V_{TH} within the first 10 min of stress, suggesting that its thinner active layer is more susceptible to species diffusion e.g. hydrogen between passivation/channel region. This diffusion process is reversible when the electric stress is removed, because nearly full recovery of V_{TH} is achieved [58].

Finally, by combining the conclusions drawn from the DC parameter analysis and the bias-stress stability test, the active layer thickness of approximately 25 nm represents the most favorable trade-off for the a-IGZO TFTs fabricated at CENIMAT. From a circuit design point of view, the 15 nm film offers better geometry-independent V_{TH} is crucial for reproducibility and scaling. Thus, the optimal thickness ultimately depends on the intended application.

4

CONCLUSIONS AND FUTURE PERSPECTIVES

This dissertation investigated the role of active layer engineering in AOS TFTs, focusing on SAL devices based on a-IGZO and DAL architecture combining a-IZO and a-IGZO films. The central motivation was to determine whether dual-layer designs could simultaneously enhance charge transport while preserving or even improving device stability, compared with conventional single-layer references.

The initial benchmark with a 40 nm a-IGZO active layer. This structure presented a μ_{FE} of approximately 20 $cm^2\ V^{-1}\ s^{-1}$, a *SS* close to 0.10 V dec^{-1}, a V_{TH} and V_{ON} close to zero (- 0.04 V and - 0.31, respectively) and a low Off-current on the order of 10^{-11} A, at measurement/equipment resolution. These values confirmed that the 40 nm channel thickness ensures both adequate transport and good switching performance and stability, establishing this sample as a reliable benchmark for subsequent DAL investigations.

When DAL structures were introduced, the performance strongly depended on both the thickness of the a-IZO film and its position relative to the GD interface. For the thinnest films, with only 1 nm and 2 nm of a-IZO, the electrical characteristics remained similar to those of the SAL reference, with no clear advantage in terms of mobility or negative impact on threshold control. The results suggest that such thin sputtered layers are likely discontinuous and do not form an effective dual channel, which compromises their contribution to carrier transport. In these cases, *SS* values tended to increase, and Off currents were slightly higher, reinforcing the absence of measurable benefits. However when the stability is accessed, under PGBS, the DAL_B configuration showed remarkable improvements, especially DAL_B_2, presenting ΔV_{TH} shifting near zero for DAL_B_2, while DAL_A presents similar bahaviour to the SAL. For thicker a-IZO with 5 nm, dual-channel behaviour became evident. The DAL_B_5 structure, in which the a-IZO was placed adjacent to the GD exhibited enhancement in μ_{FE}, reaching ~ 47 $cm^2\ V^{-1}\ s^{-1}$, more than twice that of the 40 nm SAL reference and a lower Off-current on the order of 10^{-12} A. Nevertheless, the trade-off was a negative shift in V_{TH} and V_{ON} (- 6.48 V and - 9.15, respectively). Conversely, the DAL_A_5 configuration, with a-IGZO near the GD interface and a-IZO on top, showed a more pronounced negative shift on the V_{TH} and V_{ON} (- 9.06 V and – 13.3, respectively), but did not show meaningful mobility gains, μ_{FE} reaching ~ 21 $cm^2\ V^{-1}\ s^{-1}$. These findings demonstrate that DAL performance critically depends on layer order and the thickness combination between the stacks, such that thicker a-IGZO or thinner a-IZO layers do not limit the G electrostatic control modulation or

the promotion of a continuous film, respectively.In general, the DAL stacks show improvements in PGBS stability, especially the DAL_B configuration, which exhibits a near-zero ΔV_{TH} shift, whereas DAL_A behaves similarly to the SAL, for thinner layer of a-IZO film (1 and 2 nm).

Complementary studies on SAL devices with different a-IGZO thicknesses provided further insight into scaling limits. Devices with 40 nm and 25 nm layers showed comparable mobilities of ~ 23 $cm^2 V^{-1} s^{-1}$. However, the 25 nm sample displayed superior *SS* (~0.14 V dec^{-1}), a V_{TH}, and better NGBS stability than the 40 nm and 15 nm samples, making it the most balanced configuration among the SAL structures.

To sum up, active-layer engineering is shown to be an effective yet delicate route toward performance improvement in oxide TFTs. Only specific combinations of thickness and layer arrangement yield meaningful advantages, and these must be weighed against stability trade-offs.

From these conclusions, several perspectives for future work can be drawn:

- Future work should focus on further investigating the semiconductor physics governing carrier transport and charge distribution in these multilayer architectures. Such analysis is essential to clarify why, under the present fabrication conditions, the DAL configurations did not consistently yield the expected mobility enhancement while still providing notable stability improvements.
- A more rigorous optimization of DAL architectures. Building upon the conclusions drawn from the short-base regime analysis, future optimization should aim to reduce the total active-layer thickness so that both semiconductors fall within the electrostatically controlled region. Therefore, the total channel thickness should be decreased to approximately 25 nm (building on the SAL thickness study), maintaining a thin (≈ 5 nm) a-IZO sublayer to preserve sputtering uniformity, and both layer orders should be systematically compared to evaluate the electrostatic and transport balance between them. As an alternative pathway, a lower-conductivity a-IZO formulation should be explored and the stack re-balanced so that a-IZO becomes the dominant semiconductor, rather than a-IGZO, while preserving adequate V_{TH}. In parallel, an effective back-channel passivation should be implemented to suppress surface adsorption of oxygen and moisture and thereby limit the formation of parasitic channels. Finally, reliability must be assessed more comprehensively using stress protocols that better emulate active-matrix operation (e.g., as light, temperature, pulse-stress).
- Further progress will benefit from more extensive simulation and modeling. Analytical approaches, such as those presented by Wager et al.,[1] have already guided the positioning of layers, but discrepancies remain between theory and experimental results. Future models should incorporate more realistic device conditions. including interface traps, back-channel effects, dielectric imperfections and bias-stress behaviour, to better reflect experimentally observed performance. To overcome the limitations of sputtering depositions when targeting highly uniform and continuous thin AOS channels, atomic layer deposition (ALD) emerges as a conformal [59], Å-scale controlled method with excellent step coverage and in composition/thickness tuning, enabling engineered dual-channel stacks that raise mobility while improving stability [60], [61], [62].

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In this work, generative artificial intelligence tools, namely Chat GPT, were used for grammatical review, text formulation and text organization. These tools were employed under the author´s supervision, and all generated content was checked for accuracy. The authorship and validation of the content remain entirely the responsibility of the author, and the use of artificial intelligence complies with institutional standards of academic integrity.

A

APPENDIX

A.1 Comparative literature data on SAL and DAL oxide TFTs

Table A. 1 - - Comparative studies of DAL (IZO/IGZO) and SAL (IGZO) TFTs and their impact on electrical performance and stability.

Study/Approach			TFT parameters							Stress stability tests
			Thickness	V_{TH} (V)	μ_{FE} ($cm^2/V.s$)	μ_{sat} ($cm^2/V.s$)	SS (V/dec)	Stability (V)	$I_{on/off}$ ratio	
S. I. Kim et al. (2008) [19]	**SAL**	GIZO	700 Å	-0.60	19.18	-	0.19	1.5	-	Positive and negative bias stress: V_{GS} = ±10 V; V_{DS} = 0 V
	DAL	IZO/GIZO	50 Å/700 Å	0.31	51.3	-	0.19	0.5	-	
		ITO/GIZO	50 Å/700 Å	0.50	104		0.25	0.75		
S. Jeon et al. (2010) [63]	**SAL**	IGZO	50 nm	2.5	-	10	-	-	10^8	-
	DAL	IZO/IGZO	5 nm/50 nm	1.3	-	30	-	-	10^8	
M. A.Marrs et al. (2011) [52]	**SAL**	IGZO	20 nm	~8-10	-	1.2	-	~0.5/~1	8.5×10^9	Positive and negative bias stress: V_{GS} = ±10 V; V_{DS} = 0 V for 10 min
	DAL	ZIO/IGZO	5 nm/45 nm	~2-3	-	18	-	~0.5/ ~0.8	2×10^9	
Jae Chul Park and Ho-Nyeon Lee (2012) [64]	**SAL**	GIZO	60 nm	1.88	20.9	-	-	~ -1.8	~ 1×10^{10}	Negative bias illumination stress (NBTIS): V_{GS} = -20 V, V_{DS} = 10 V; green LED driven by a 5-mA current.for 10000 s
	DAL	IZO/GIZO	5 nm/60 nm	1.57	47.7	-	-	~ -1.2	~ 1×10^{10}	
X. Ding et al.(2014) [65]	**SAL**	a-IGZO	22 nm	2.8	7.4	-	0.16	0.54	$>10^7$	Positive bias temperature stress (PBTS): V_{GS} = +20 V and T = 293 K to 353K
	DAL	IZO/IGZO	5 nm/17 nm	0.8	14.4		0.13	0.51	$>10^7$	
M.M Billah et al. (2021) [45]	**SAL**	a-IGZO	40 nm	0.10	10.3	-	0.18	-	$\approx10^8$	-
		a-IZO	10 nm	-0.5	36.5		0.20		$\approx10^7$	
	DAL	IGZO/IZO	10 nm/16 nm	0.40	33.8	-	0.18	-	$\approx10^8$	
		IZO/IGZO	16 nm/10 nm	2.30	49.5		0.18		$\approx10^9$	
J. B. Kim et al. (2021) [46]	**SAL**	a-IZO	16 nm	0.04	37.0	-	0.20	-	$I_{OFF} = 3.5\times10^{-11}$ A	-
	DAL	IZO/IGZO	16 nm/10 nm	2.10	50.3	-	0.14	-	$I_{OFF} = 6.5\times10^{-13}$ A	

A.2 SAL and DAL TFTs fabrication steps

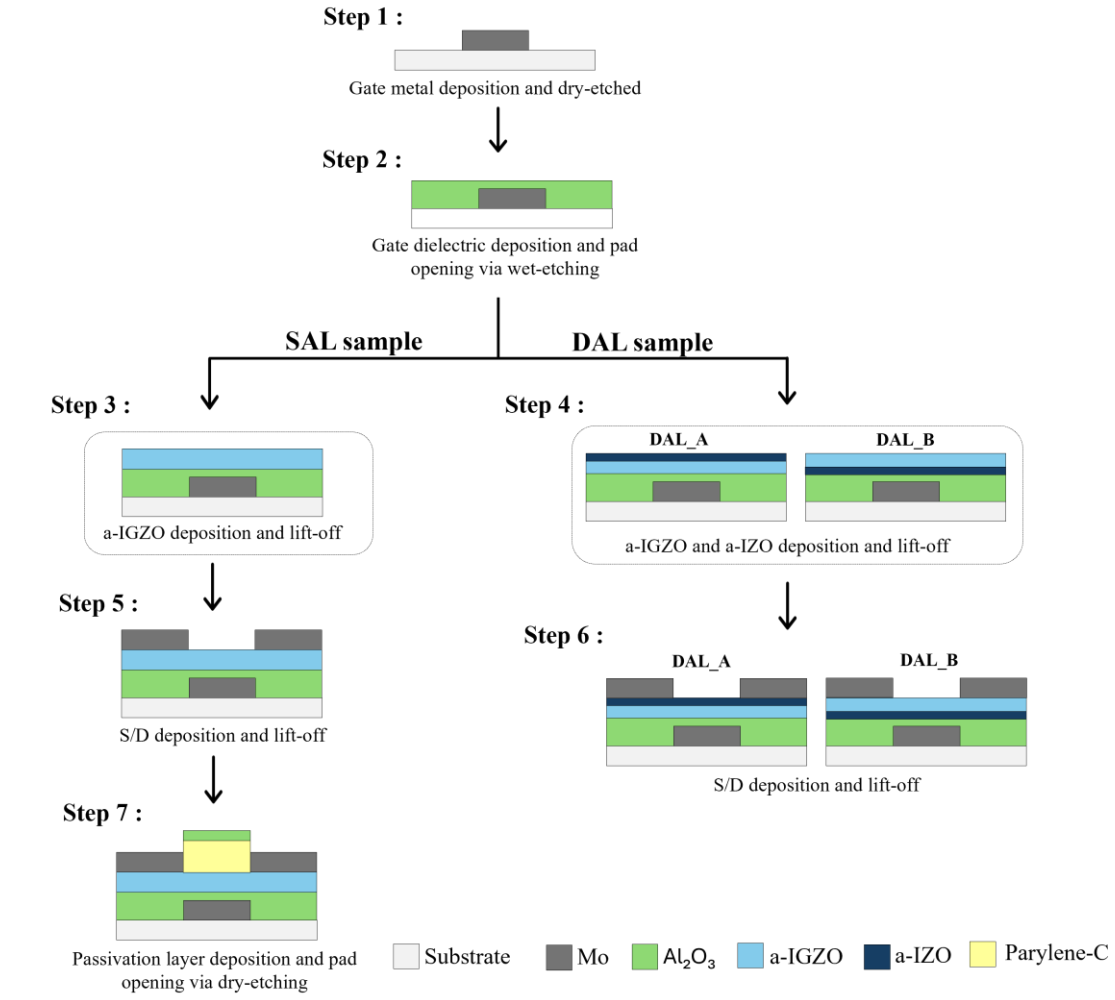

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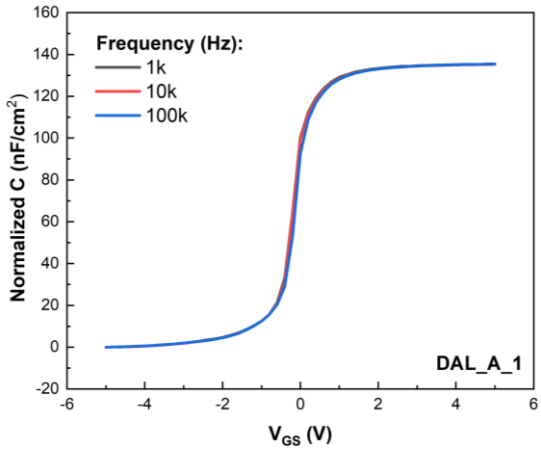
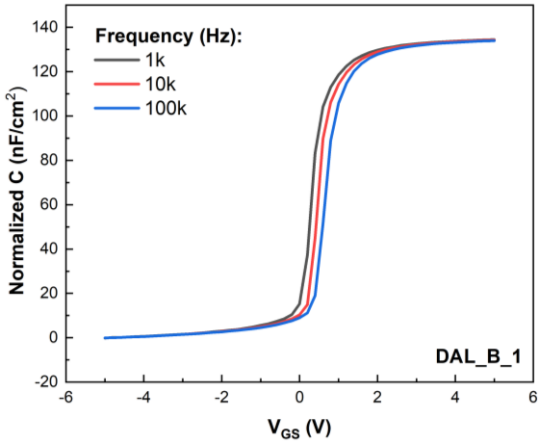
Figure A. 1 - Schematic diagram of the main fabrication steps for SAL and DAL TFTs with a bottom-gate staggered architecture.

A.3 C-V plots for SAL_IGZO and DAL devices

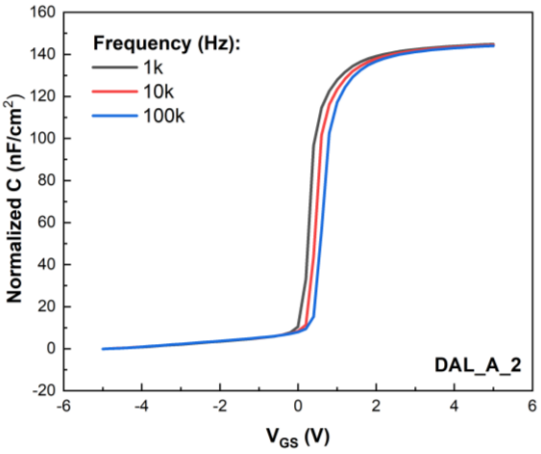
(a)



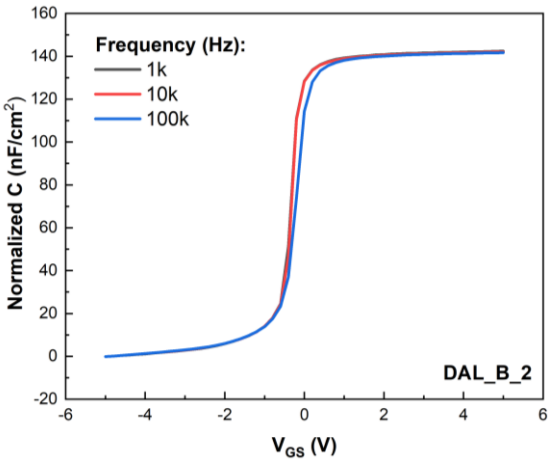
(b)



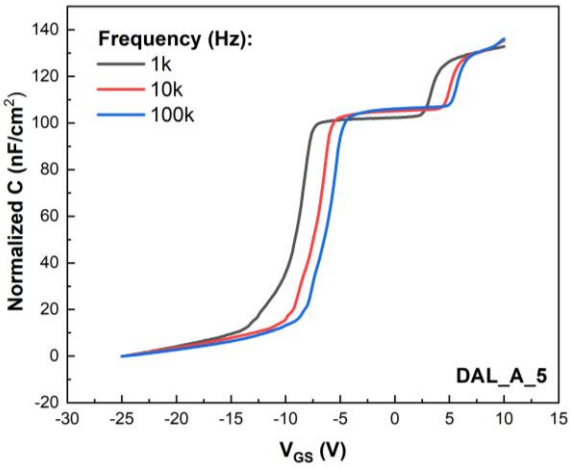
(c)



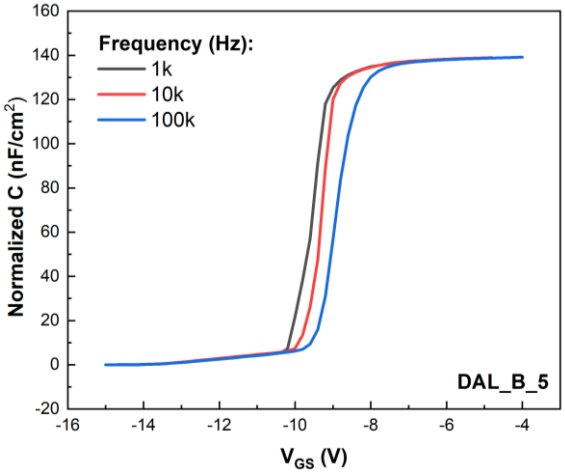
(d)



(e)



(f)



(g)

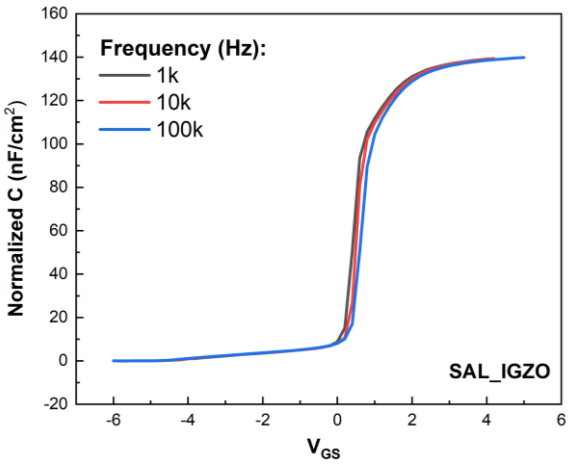
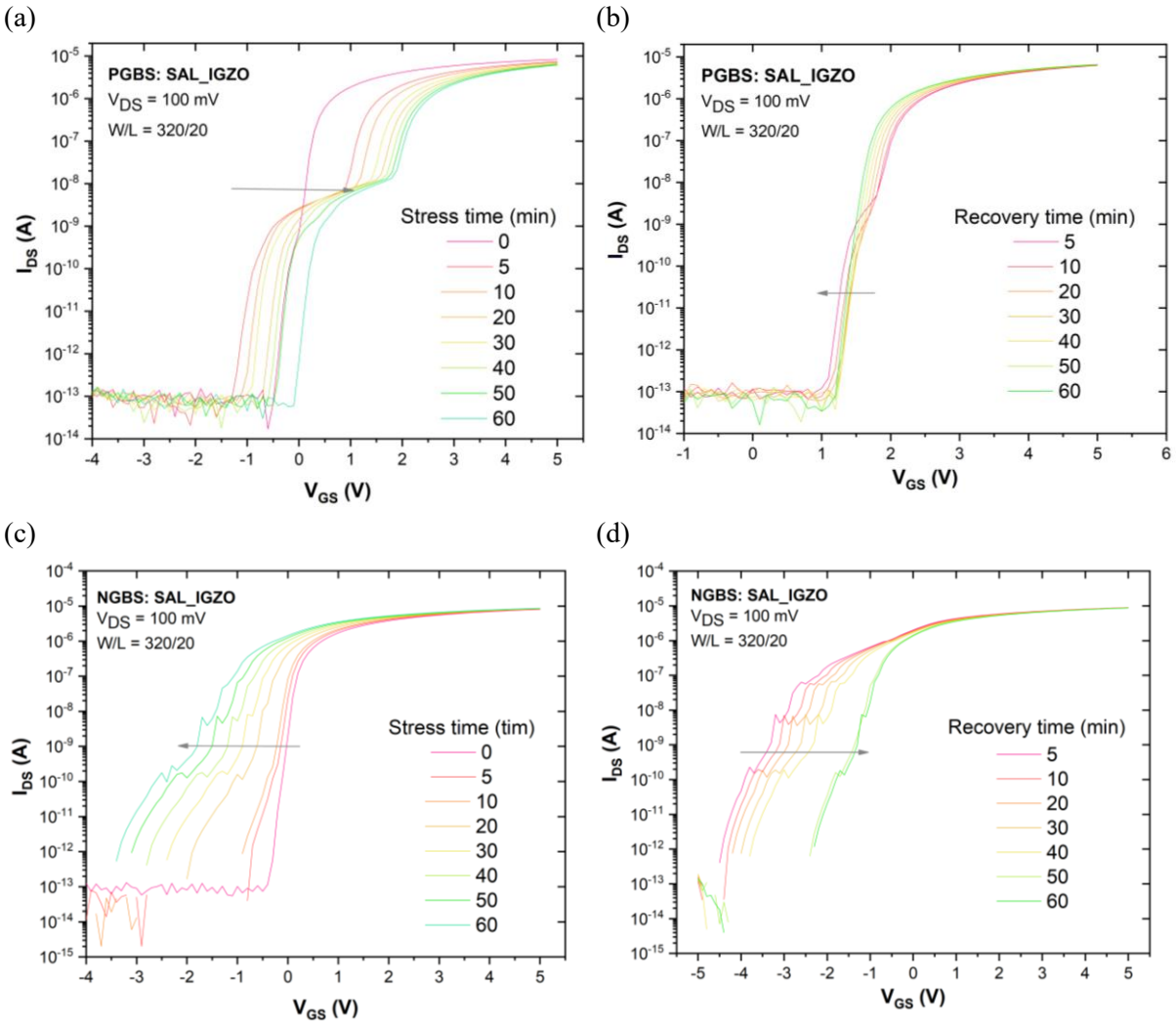


Figure A. 2 - Normalized C–V characteristics measured at 1 kHz, 10 kHz and 100 kHz for sample (a) DAL_A_1, (b) DAL_B_1, (c) DAL_A_2, (d) DAL_B_2, (e) DAL_A_5, (f) DAL_B_5 and (g) SAL_IGZO.

A.4 PGBS and NGBS for reference SAL_IGZO with 40 nm and unencapsulated

The bias stress tests were performed on this SAL device for transistors with dimensions of *W/L* = 320/20 µm/ µm. For the PGBS, a gate bias voltage of 5 V was applied ($V_{GS\ stress}$ = 5V), and taken from - 5 V to 5 V. On other hand, for the NGBS a - 5 V was applied to the gate ($V_{GS\ stress}$ = - 5V), taken from 5 V to - 5 V. The sweeps were done at V_{DS} = 0.1 V in both tests.



(e)[2] (f)[3]

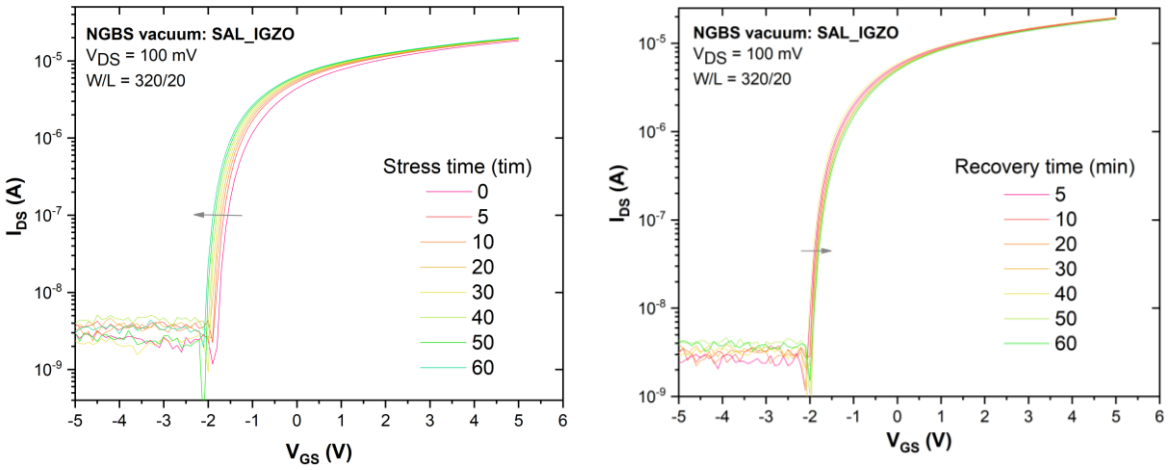


Figure A. 3 - Transfer characteristics of SAL_IGZO, for *W/L* = 320/20 µm/µm, under PGBS, NGBS and NGBS in vacuum at $V_{GS\ stress}$ = 5 V and $V_{GS\ stress}$ = - 5 V, respectively: (a) PGBS stress phase, (b) PGBS recovery phase, (c) NGBS stress phase and (d) NGBS recovery phase, (e) NGBS stress phase in vacuum, (f) NGBS recovery phase in vacuum.

[2] Measurements were performed with a Keithley 4200-SCS Semiconductor Characterization System coupled to a Janis ST-500 cryogenic probe station. Due to differences in integration time between the different semiconductor parameter analyzers, it was chosen to keep the same acquisition time of 4s in all the stress transfer characteristics. For sub-nA currents, the Keithley 4200-SCS takes a significantly longer time, hence the off current is limited to 1-10nA.

[3] Measurements were performed with a Keithley 4200-SCS Semiconductor Characterization System coupled to a Janis ST-500 cryogenic probe station. Due to differences in integration time between the different semiconductor parameter analyzers, it was chosen to keep the same acquisition time of 4s in all the stress transfer characteristics. For sub-nA currents, the Keithley 4200-SCS takes a significantly longer time, hence the off current is limited to 1-10nA.

A.5 Mott–Schottky C–V Analysis of the SAL_IGZO

C–V measurements were performed on TFTs (W = 320 µm; L = 40 µm) electrically configured as metal–insulator–semiconductor (MIS) capacitors. Measurements were carried out using Keysight B1500A equipped with a capacitance measurement unit (CMU). A sinusoidal AC bias with amplitude of 50 mV was superimposed upon a DC gate voltage sweep.

For this analysis, we normalized the measured capacitance (C) by subtracting the gate-to-source and gate-to-drain parasitic capacitance (C_P). In this case, C_P is considered as the off-state capacitance and was taken from the average of the initial 10 capacitance data points, with a gate voltage sweep from -6 to 6, while the MIS is still under depletion. The normalized capacitance (C-C_P) voltage curve is demonstrated on Figure A. 4.

(a) (b)

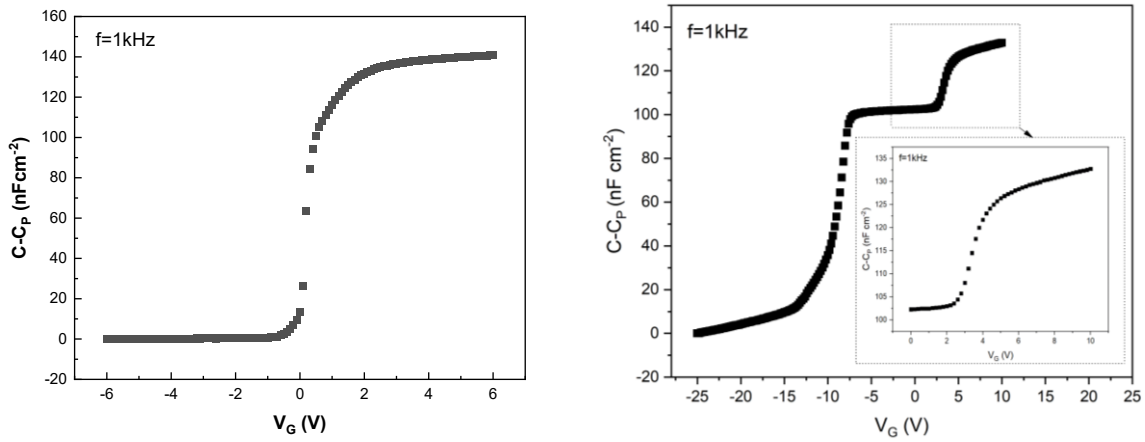


Figure A. 4 - Normalized capacitance–voltage (C–C_p) characteristic MIS capacitor measured at 1 kHz of the (a) SAL_IGZO and (b) DAL_A_5.

To extract the active layer carrier density through Mott-Schottky analysis, it is necessary to remove the contribution of GD and interface traps to the overall capacitance. Therefore, we considered the MIS-connected TFT as a series of GD capacitance (C_{ox}) with the active layer capacitance (C_S). Thus, we get:

$$C - C_p = \frac{C_s C_{ox}}{C_s - C_{ox}} \tag{1}$$

We considered C_{ox} as the maximum capacitance reached in full accumulation, therefore it was taken as the average of the last 10 data points of the same gate voltage sweep. Thus, it was possible to extract C_S – voltage curves (Figure A. 5).

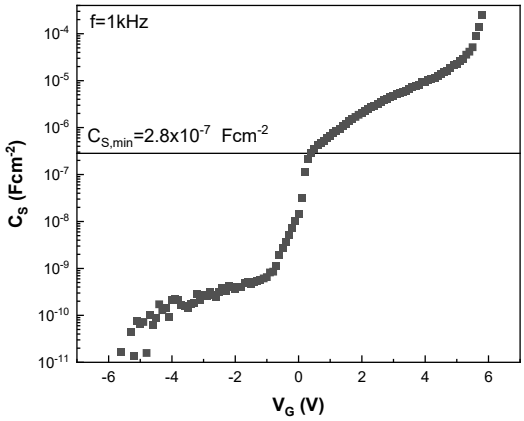


Figure A. 5 - Active-layer capacitance (C_s)–voltage curve of the SAL_IGZO MIS capacitor measured at 1 kHz.

A key concept for this analysis is the minimum semiconductor capacitance ($C_{S,min}$). Because charge may accumulate at the semiconductor under gate modulation, no upper bound exists for C_S. However, a lower bound is imposed by the semiconductor thickness (t): once the entire layer is depleted, the minimum capacitance is reached. Any measured capacitance below this limit cannot originate from the semiconductor and thus reflects extrinsic contributions from gate dielectric or interface charges. Mathematically, $C_{S,min}$ is given by (2).Consequently, only capacitance values above $C_{S,min}$ is valid for extracting the carrier density via Mott–Schottky analysis. For this, we take the reciprocal of C_S squared, which is given by (3), where V_{fb} is the flat-band voltage.

$$C_{S,min} = \varepsilon_S \varepsilon_0 / t \tag{2}$$

$$\frac{1}{C_s^2} = \frac{2}{q\varepsilon_s\varepsilon_0 N_D}(V + V_{fb}) \tag{3}$$

Therefore, we extracted N_D from the slope of the linear region of the Mott-Schottky plot (Figure A. 6). An identical analysis workflow (C-V extraction, CS determination and Mott-Schottky fitting was also applied to the DAL_A_5.

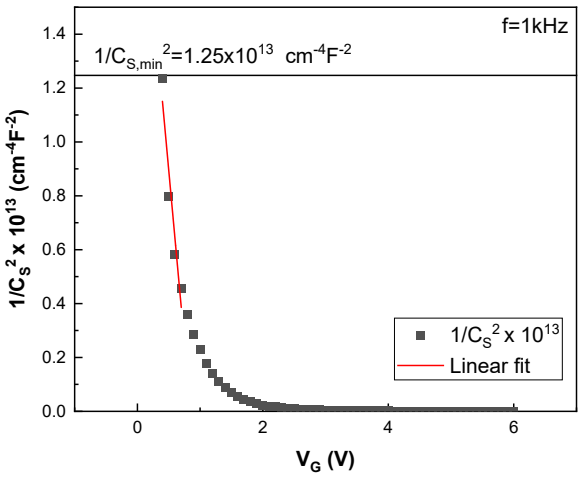


Figure A. 6 - Mott–Schottky (1/C_s^2 vs V_G) curve of SAL_IGZO measured at 1 kHz.

A.6 PGBS for DAL with 1 nm of a-IZO

The bias stress tests were performed on these DAL_A_1 and DAL_B_1 devices for transistors with dimensions of *W/L* = 320/20 µm/µm. For the PGBS, a gate bias voltage of 5 V was applied ($V_{GS\ stress}$ = 5V), and taken from - 5 V to 5 V, under a condition of V_{DS} = 0.1 V.

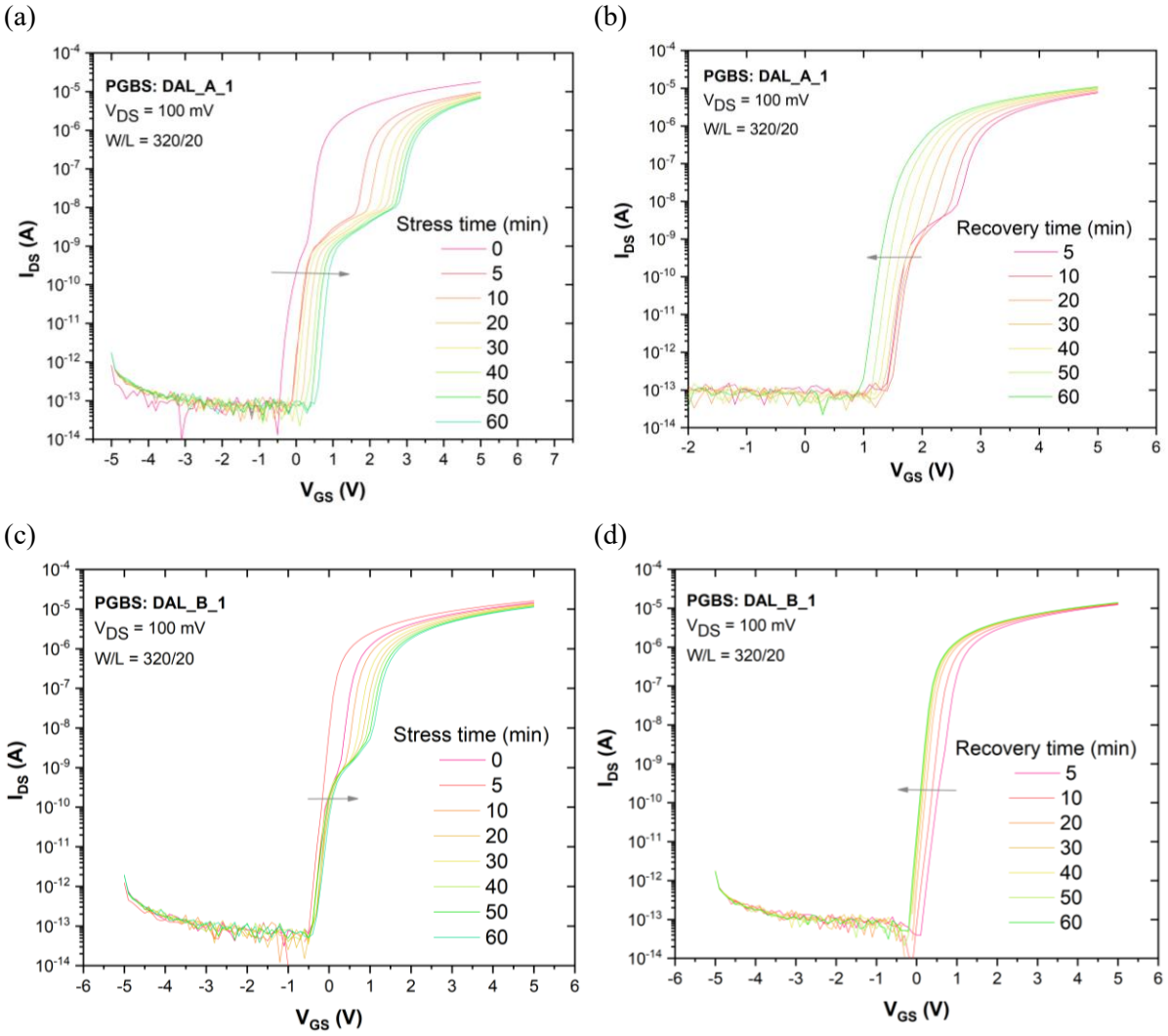


Figure A. 7 - Transfer characteristics of DAL_A_1 and DAL_B_1 under PGBS at $V_{GS\ stress}$ = 5 V, for *W/L* = 320/20 µm/µm: (a) DAL_A_1 stress phase, (b) DAL_A_1 recovery phase, (c) DAL_B_1 stress phase, (d) DAL_B_1 recovery phase.

A.7 PGBS for DAL with 2 nm of a-IZO

The bias stress tests were performed on these DAL_A_2 and DAL_B_2 devices for transistors with dimensions of W/L = 320/20 µm/ µm. For the PGBS, a gate bias voltage of 5 V was applied ($V_{GS\,stress}$ = 5V), and taken from - 5 V to 5 V, under a condition of V_{DS} = 0.1 V.

(a)[4] (b)[5]

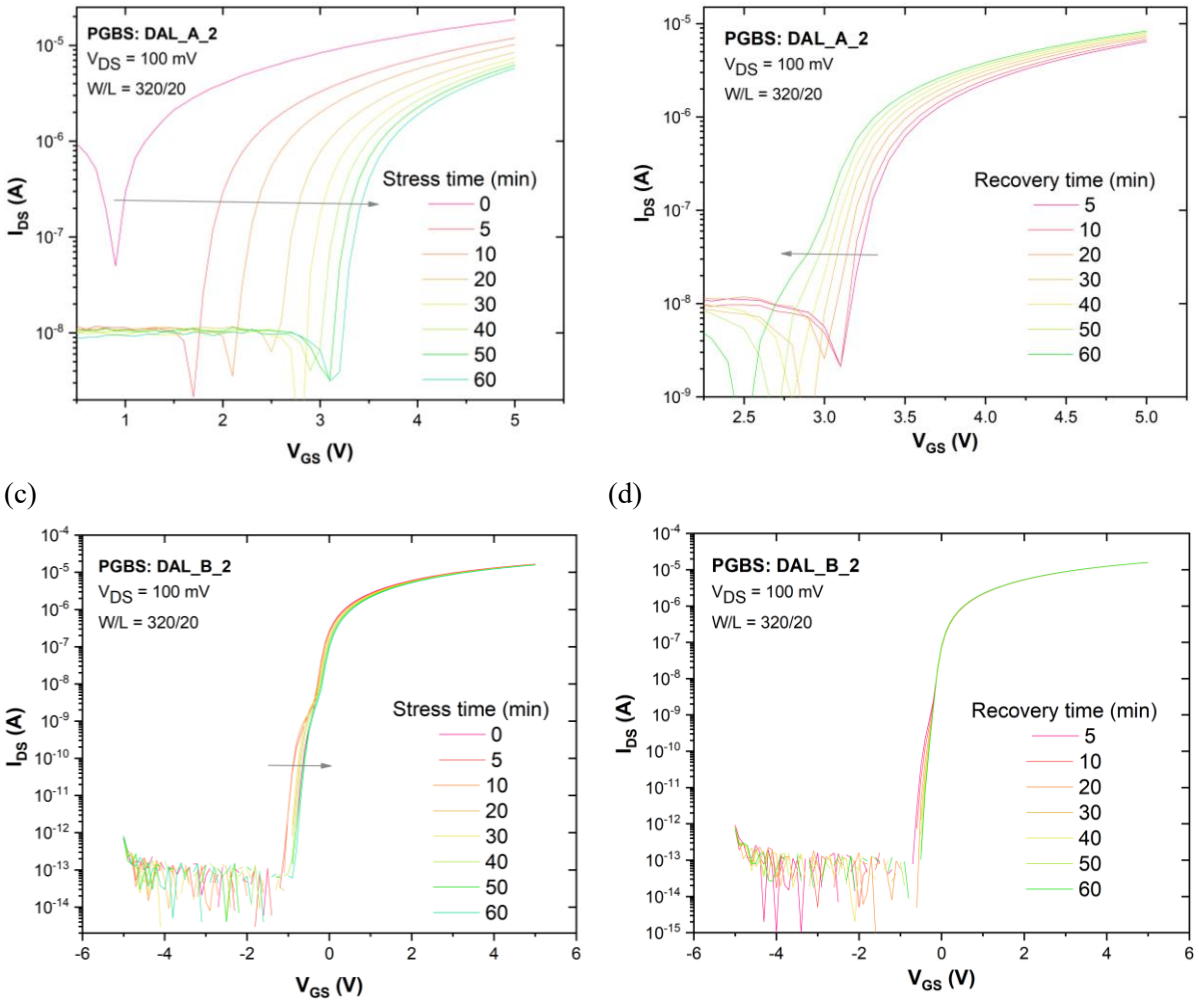


Figure A. 8 - Transfer characteristics of DAL_A_2 and DAL_B_2 under PGBS at $V_{GS\,stress}$ = 5 V, for W/L = 320/20 µm/µm: (a) DAL_A_2 stress phase, (b) DAL_A_2 recovery phase, (c) DAL_B_2 stress phase, (d) DAL_B_2 recovery phase.

[4] Measurements were performed with a Keithley 4200-SCS Semiconductor Characterization System coupled to a Janis ST-500 cryogenic probe station. Due to differences in integration time between the different semiconductor parameter analyzers, it was chosen to keep the same acquisition time of 4s in all the stress transfer characteristics. For sub-nA currents, the Keithley 4200-SCS takes a significantly longer time, hence the off current is limited to 1-10nA.

[5] Measurements were performed with a Keithley 4200-SCS Semiconductor Characterization System coupled to a Janis ST-500 cryogenic probe station. Due to differences in integration time between the different semiconductor parameter analyzers, it was chosen to keep the same acquisition time of 4s in all the stress transfer characteristics. For sub-nA currents, the Keithley 4200-SCS takes a significantly longer time, hence the off current is limited to 1-10nA.

A.8 PGBS for DAL with 5 nm of a-IZO

The bias stress tests were performed on these DAL_A_5 and DAL_B_5 devices for transistors with dimensions of *W/L* = 320/20. For the PGBS, a gate bias voltage of – 8 V and – 3 V was applied to DAL_A_5 and DAL_B_5, respectively, and taken from -20 V to 5 V, under a condition of V_{DS} = 0.1 V.

The small perturbations visible in the DAL_B_5 stress curves (Figure A. 9 (c)) at 20 and 30 minutes are measurement artefacts: external mechanical vibrations coupled into the probe station slightly modulated the tip–pad contact, introducing transient current fluctuations that distort the traces. Therefore, these artefacts are not intrinsic to the device nor the measurement and do not affect the overall conclusions.

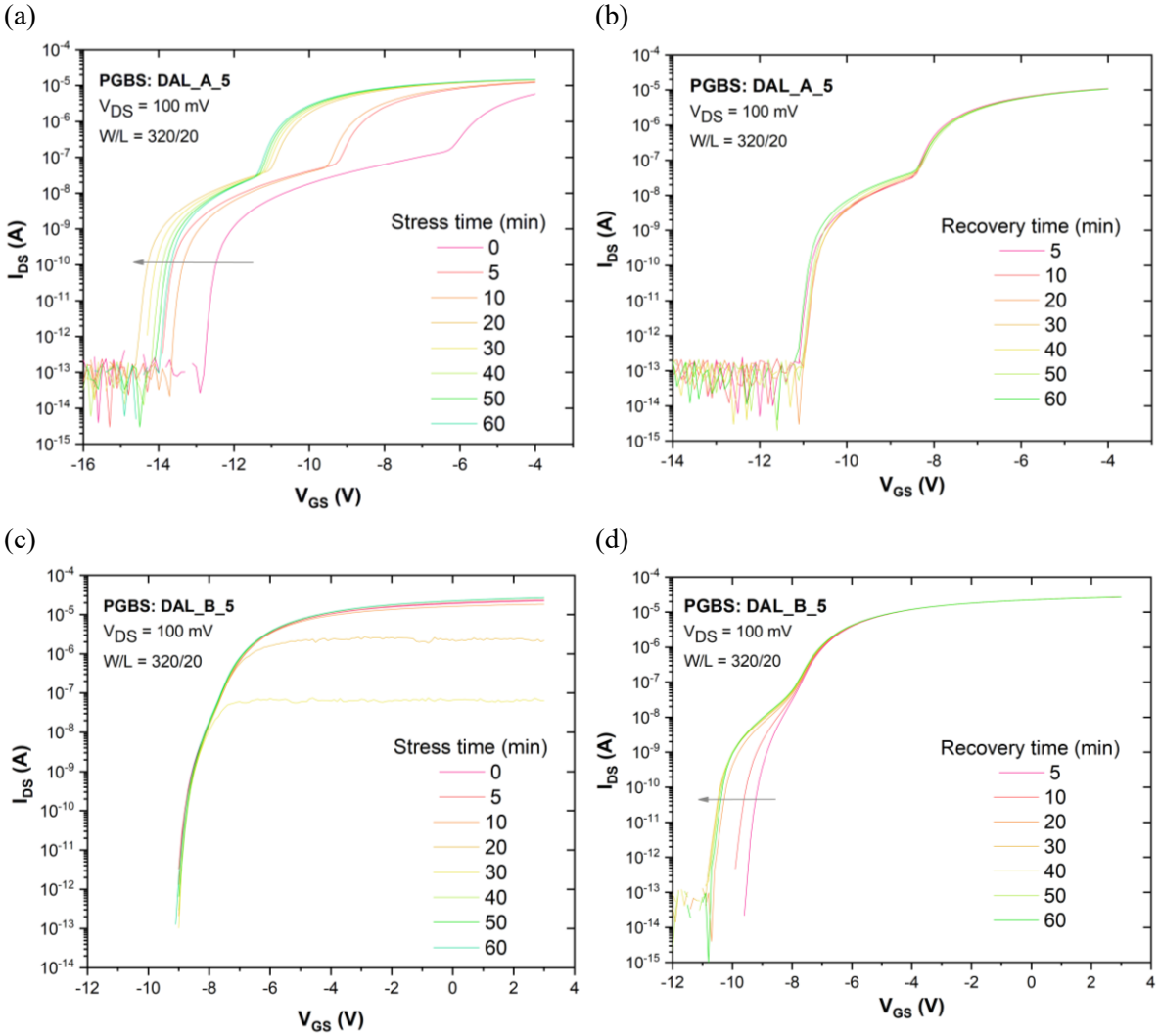


Figure A. 9 - Transfer characteristics of DAL_A_5 and DAL_B_5 under PGBS at $V_{GS\ stress}$ = - 8 V and $V_{GS\ stress}$ = - 3 V, respectively, for *W/L* = 320/20 µm/µm: (a) DAL_A_5 stress phase, (b) DAL_A_5 recovery phase, (c) DAL_B_5 stress phase, (d) DAL_B_5 recovery phase.

(a) (b)

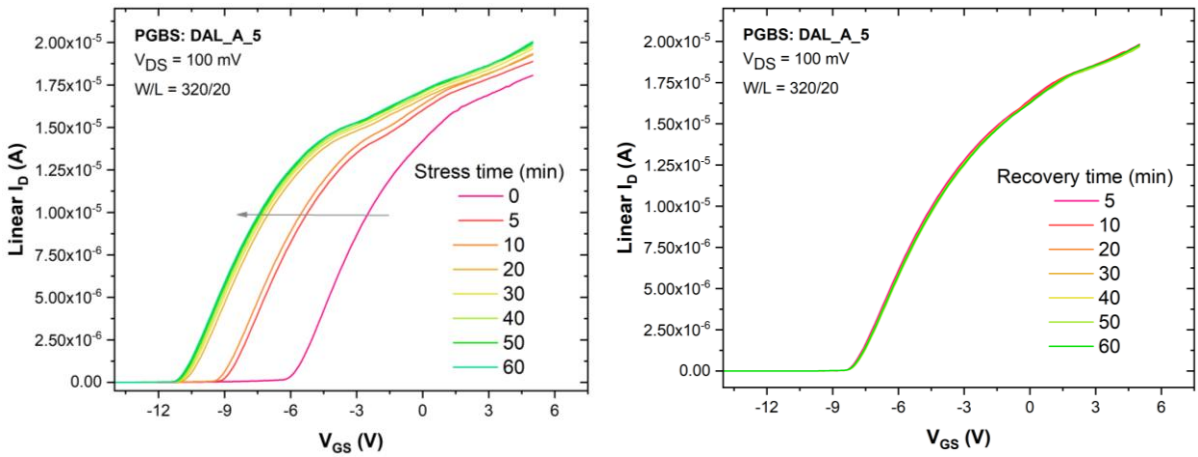


Figure A. 10 – Linear fit of transfer characteristics for DAL_A_5 under PGBS at $V_{GS\,stress}$ = - 8 V, for W/L = 320/20 µm/µm: (a) DAL_A_5 stress phase, (b) DAL_A_5 recovery phase.

A.9 Detailed electrical parameters of a-IGZO SAL TFTs

Table A. 2 - Electrical parameters of SAL_40_Passivated TFTs with different *W/L* ratios.

TFT Dimensions (µm/µm)	V_{TH} (V)	V_{ON} (V)	μ_{FE} (cm^2/V.s)	μ_{sat} (cm^2/V.s)	SS (V/dec)	Off current (A)	On-Off ratio
W/L = 320/40	-0.78±0.29	-1.21±0.25	23.7±1.84	19.8±3.77	0.15±0.03	$(3.63±2.70)\times10^{-11}$	$(5.17±3.66)\times10^{5}$
W/L = 160/40	-1.08±0.46	-1.89±0.61	24.7±5.61	23.1±0.79	0.26±0.05	$(1.31±1.77)\times10^{-11}$	$(1.38±1.09)\times10^{6}$
W/L = 80/40	-1.08±0.27	-1.84±0.60	25.9±1.09	24.1±0.69	0.31±0.17	$(1.99±1.50)\times10^{-11}$	$(1.55±0.71)\times10^{5}$
W/L = 40/40	-1.35±0.02	-2.08±0.25	27.1±1.02	22.9±0.91	0.32±0.09	$(3.50±1.36)\times10^{-12}$	$(6.55±4.52)\times10^{4}$
W/L = 320/20	-1.08±0.24	-1.96±0.35	23.2±3.37	21.6±3.42	0.19±0.03	$(4.07±0.72)\times10^{-11}$	$(5.91±0.71)\times10^{5}$
W/L = 320/10	-1.40±0.33	-2.32±0.44	24.6±2.67	23.0±2.24	0.19±0.00	$(9.07±0.99)\times10^{-11}$	$(2.66±0.14)\times10^{6}$
W/L = 320/5	-1.32±0.03	-2.25±0.20	8.49±2.25	14.3±4.81	0.18±0.02	$(3.03±0.30)\times10^{-11}$	$(1.51±0.09)\times10^{5}$

Table A. 3 - Electrical parameters of SAL_25_Passivated TFTs with different *W/L* ratios.

TFT Dimensions (µm/µm)	V_{TH} (V)	V_{ON} (V)	μ_{FE} (cm^2/V.s)	μ_{sat} (cm^2/V.s)	SS (V/dec)	Off current (A)	On-Off ratio
W/L = 320/40	-0.17±0.16	-0.57±0.24	22.9±1.77	20.2±3.50	0.13±2.12	$(5.66±2.19)\times10^{-11}$	$(2.07±0.65)\times10^{5}$
W/L = 160/40	-0.35±0.08	-0.63±0.12	20.6±5.33	21.3±3.72	0.11±0.01	$(5.17±4.04)\times10^{-11}$	$(1.84±1.75)\times10^{6}$
W/L = 80/40	-0.38±0.06	-0.67±0.04	24.7±0.81	23.1±0.79	0.10±0.01	$(2.68±0.83)\times10^{-11}$	$(1.10±0.89)\times10^{5}$
W/L = 40/40	-0.38±0.06	-0.60±0.07	25.9±0.23	24.1±0.69	0.11±0.01	$(1.70±0.34)\times10^{-12}$	$(9.19±1.88)\times10^{4}$
W/L = 320/20	-0.47±0.04	-0.79±0.05	21.3±1.18	22.9±0.91	0.10±0.01	$(3.29±2.87)\times10^{-11}$	$(9.69±4.82)\times10^{5}$
W/L = 320/10	-0.65±0.04	-1.13±0.10	21.3±2.18	23.3±1.94	0.12±0.02	$(2.64±0.63)\times10^{-11}$	$(1.81±0.41)\times10^{6}$
W/L = 320/5	-0.78±0.46	-2.45±0.25	21.8±1.07	29.5±3.85	0.33±0.21	$(4.59±2.74)\times10^{-11}$	$(2.67±1.73)\times10^{5}$

Table A. 4 - Electrical parameters of SAL_15_Passivated TFTs with different *W/L* ratios.

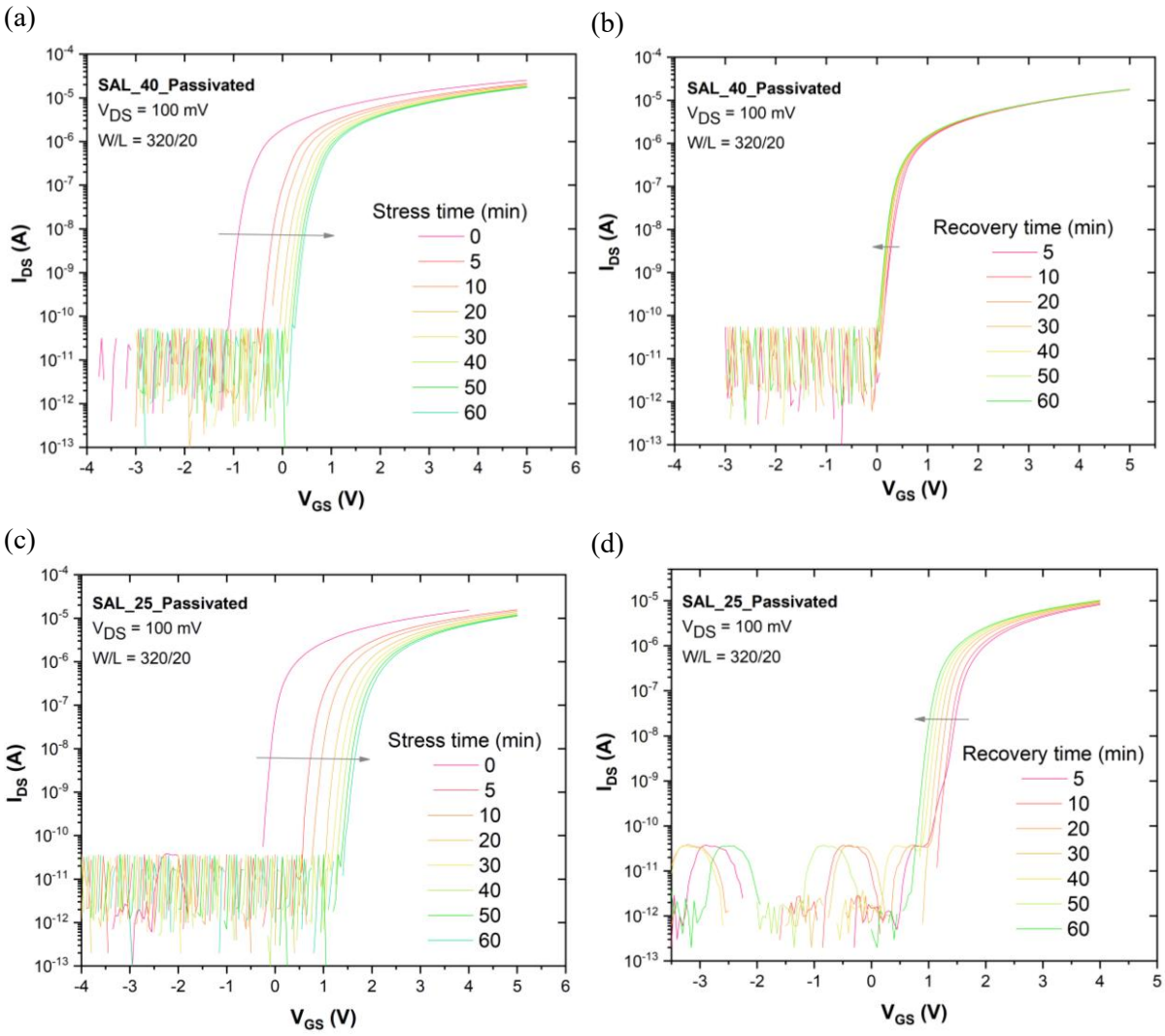
TFT Dimensions (µm/µm)	V_{TH} (V)	V_{ON} (V)	μ_{FE} (cm^2/V.s)	μ_{sat} (cm^2/V.s)	SS (V/dec)	Off current (A)	On-Off ratio
W/L = 320/20	-0.44±0.07	-0.82±0.07	14.3±2.70	16.5±4.76	0.11±0.04	$(9.71±4.72)\times10^{-12}$	$(1.46±1.47)\times10^{6}$
W/L = 160/20	-0.49±0.07	-0.79±0.04	15.4±5.08	18.1±5.30	0.10±0.09	$(1.82±1.10)\times10^{-11}$	$(4.48±0.23)\times10^{6}$
W/L = 80/20	-0.40±0.01	-0.67±0.03	25.3±1.90	24.9±0.13	0.10±0.02	$(2.77±0.93)\times10^{-11}$	$(3.46±0.76)\times10^{5}$
W/L = 40/20	-0.32±0.14	-0.62±0.01	14.8±1.99	23.3±1.04	0.12±0.02	$(3.18±1.67)\times10^{-11}$	$(8.39±4.35)\times10^{5}$
W/L = 320/40	-0.33±0.10	-0.63±0.03	19.5±3.40	22.0±1.77	0.11±0.01	$(1.44±0.74)\times10^{-11}$	$(8.35±4.15)\times10^{5}$
W/L = 320/10	-0.58±0.04	-1.01±0.09	14.8±3.07	18.2±4.83	0.12±0.02	$(6.54±2.66)\times10^{-11}$	$(5.82±4.61)\times10^{5}$
W/L = 320/5	-0.90±0.14	-2.75±0.14	16.5±3.70	18.8±5.08	0.52±0.28	$(4.13±1.57)\times10^{-11}$	$(2.15±1.39)\times10^{5}$

A.10 Stress tests on a-IGZO SALs TFTs: PGBS & NGBS

PGBS and NGBS tests were performed on these SAL devices for transistors with dimensions of *W/L* = 320/20 µm/ µm. For the PGBS, a gate bias voltage of 5 V was applied ($V_{GS\,stress}$ = 5V), and taken from 5 V to -5 V. On other hand, for the NGBS a – 5 V was applied to the gate ($V_{GS\,stress}$ = - 5V), taken from – 5 V to 5 V. The sweeps were done at V_{DS} = 0.1 V in both tests.

PGBS

Under PGBS, all transfer curves of the SAL devices (Figure A. 11) exhibit a positive shift that increases with stress time. On the other hand, during recovery, a fast partial recovery occurs within the first few minutes, followed by a slower relaxation phase.



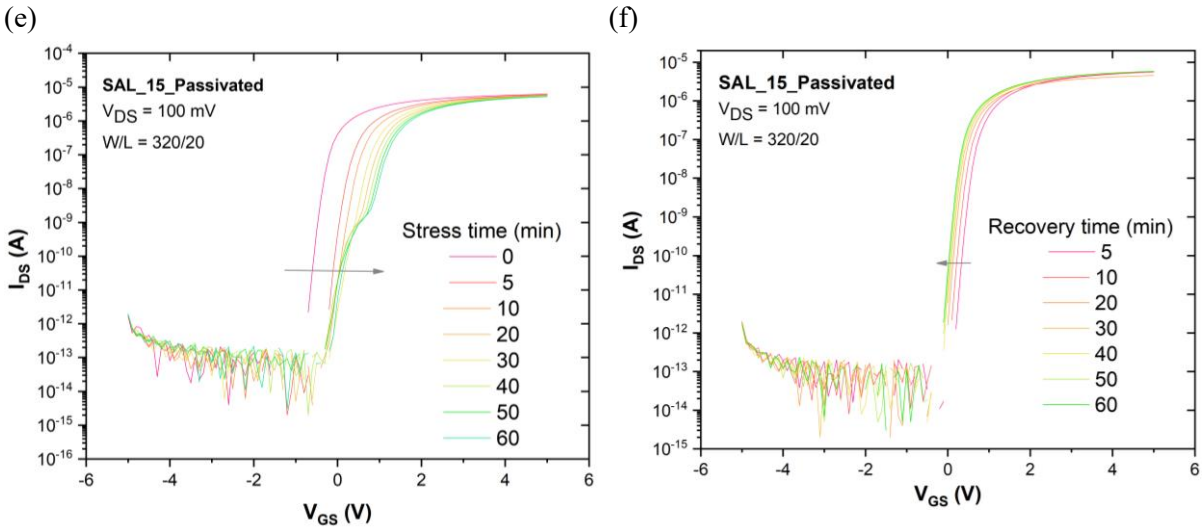
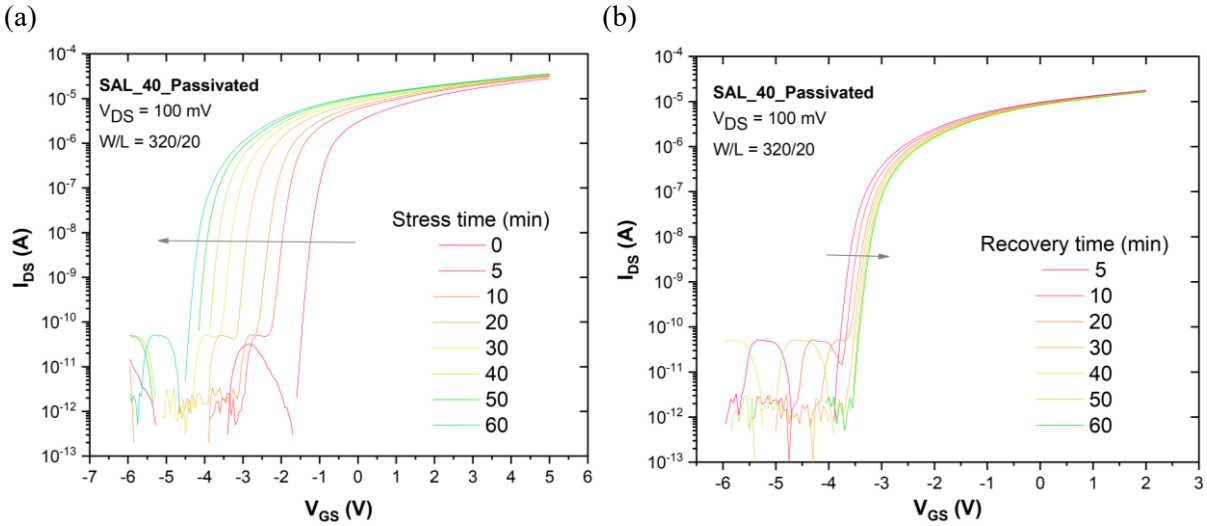


Figure A. 11 – Transfer characteristics of SAL TFTs under PGBS at $V_{GS\ stress}$ = 5 V, for W/L = 320/20 µm/µm: (a) SAL_40_Passivated stress phase, (b) SAL_40_Passivated recovery phase, (c) SAL_25_Passivated stress phase, (d) SAL_25_Passivated recovery phase, (e) SAL_15_Passivated stress phase, (f) SAL_15_Passivated recovery phase.

NGBS

Under NGBS, all transfer curves of the SAL devices (Figure A. 12) exhibit a negative shift that increases with stress time. On the other hand, during recovery, the curves gradually drift back toward the pre-stress position, but recovery is not complete.



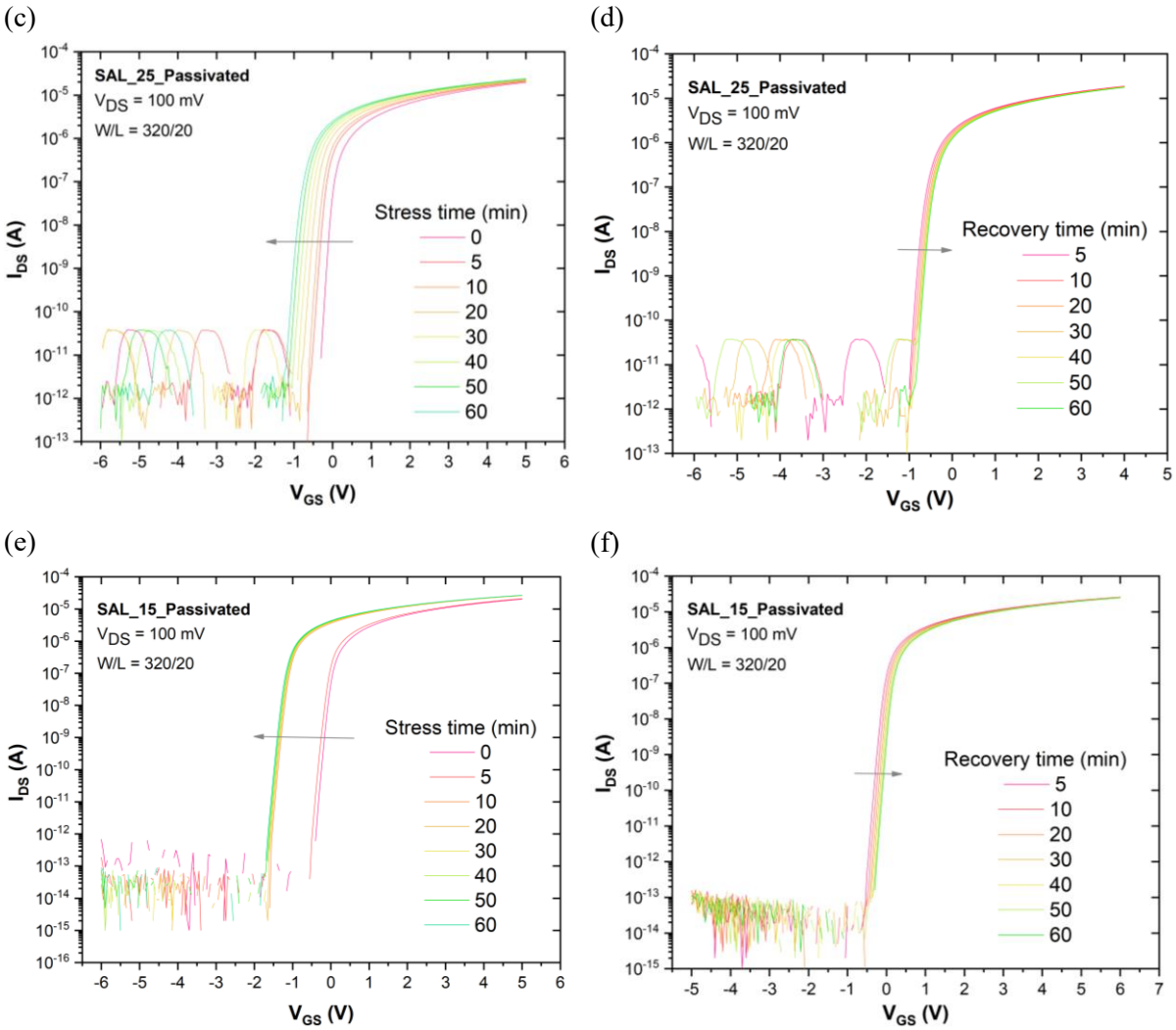


Figure A. 12 - Transfer characteristics of SAL TFTs under NGBS at $V_{GS\ stress}$ = - 5 V with *W/L* = 320/20 µm/µm: (a) SAL_40_Passivated stress phase, (b) SAL_40_Passivated recovery phase, (c) SAL_25_Passivated stress phase, (d) SAL_25_Passivated recovery phase, (e) SAL_15_Passivate stress phase, (f) SAL_15_Passivate recovery phase.