NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

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Bachelor of Science in Electrical and Computer Engineering

SUSTAINABLE SOLUTION-BASED ELECTRONIC COMPONENTS: MEMRISTORS AND DIODES

MASTER IN ELECTRICAL AND COMPUTER ENGINEERING

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"Try and leave this world a little better than you found it, and when your turn comes to die, you can die happy in feeling that at any rate, you have not wasted your time but have done your best."

— Robert Baden-Powell

(Founder of the international Scouting Movement, writer, artist and British Army officer)

Abstract

Memristors and diodes created through solution-based methods hold significant promise in meeting various demands of the Internet of Things (IoT), including the need for high device density and ultra-low power consumption, all achieved through cost-effective and straightforward fabrication techniques. In this research, we employ a combustion synthesis process to generate thin films of MoO_3 for bipolar memristors and Zinc Tin Oxide (ZTO) for Schottky diodes, through solution processing.

To enhance their effectiveness in memristor and diode devices, we investigate various factors, including the alteration of the molar concentration, the number of layers deposited, and the annealing temperature. Memristors that feature a lower number of layers and higher molar concentration exhibit several advantageous characteristics, including lower operational voltage, robust endurance, excellent yield, and the ability to retain their properties for up to 10^3 seconds under ambient air conditions. From a diode perspective, the ones that feature a lower annealing temperature show more promising characteristics, like lower operational voltage, robust endurance, excellent yield, and a rectification ratio of up to 10^9, under air conditions. MoO_3-based memristors with 0.2 M of molar concentration and with 1 deposited layer annealed at $250°C$ came to be the best condition. Diodes based on (75%/25%) ZTO with 0.2 M of molar concentration and with 8 deposited layers annealed at $250°C$ also came to be the best condition. The obtained outcomes are highly encouraging, and they outperform the existing state-of-the-art standards, in ZTO-based and MoO_3-based device cases, presented in this document.

Keywords: MoO_3, ZTO, solution-based methods, bipolar memristors, Schottky diodes, IoT, combustion synthesis process

Resumo

Memristores e diodos criados através de métodos baseados em processos de solução têm um grande potencial para atender a vários requisitos da *IoT*, incluindo a necessidade de alta densidade de dispositivos e baixo consumo de energia, tudo isso alcançado por meio de técnicas de fabricação económicas e simples. Nesta pesquisa, utilizamos um processo de síntese por combustão para criar filmes finos de MoO_3 para memristores bipolares e ZTO para diodos *Schottky*, por meio de processamento de soluções. Para melhorar a eficácia desses dispositivos (memristores e diodos), investigamos vários fatores, incluindo a alteração da concentração molar, o número de camadas depositadas e a temperatura de tratamento térmico. Os memristores que possuem um menor número de camadas e uma maior concentração molar exibem várias características vantajosas, incluindo uma tensão operacional mais baixa, resistência robusta, excelente rendimento e a capacidade de manter as suas propriedades até 10^3 segundos em condições de pressão e temperatura ambiente. Do ponto de vista dos diodos, aqueles com uma temperatura de tratamento térmico mais baixa apresentam características mais promissoras, com uma tensão operacional mais baixa, resistência robusta, excelente rendimento e uma razão de retificação até 10^9, em condições de pressão e temperatura ambiente. Memristores à base de MoO_3 com uma concentração molar de 0,2 M, com 1 camada depositada e tratada a $250°C$ revelaram-se a melhor opção. Diodos baseados em (75%/25%) ZTO com uma concentração molar de 0,2 M, com 8 camadas depositadas e tratadas a $250°C$ também se revelaram a melhor opção. Os resultados obtidos são muito encorajadores e superam os padrões existentes do estado-da-arte, tanto nos casos do dispositivo baseado em ZTO como no dispositivo baseado em MoO_3 apresentados neste documento.

Palavras-chave: MoO_3, ZTO, processos de solução, memristores bipolares, diodos *Schottky*, *IoT*, processo de síntese por combustão

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Acronyms

AI Artificial Intelligence *(pp. 1, 7, 9)*
ATO Antimony Tin Oxide *(p. 16)*

CBRAM Conductive Bridge RAM *(p. 13)*
CC Current Compliance *(pp. 34, 36, 39, 41, 67)*
CMOS Complementary Metal-Oxide-Semiconductor *(pp. 1, 9, 12, 14)*
CPU Central Processing Unit *(pp. 5, 6)*

DC Direct Current *(pp. 36, 41, 42, 44, 61)*

ECM Electrochemical Metallization Mechanism *(pp. 12, 13)*
EG Ethylene Glycol *(p. 21)*

FPGAs Field Programmable Gate Arrays *(pp. 6, 7)*
FTO Fluorine Doped Tin Oxide *(p. 16)*

GST Tellurium-based Chalcogenides *(p. 19)*

HRS High Resistance State *(pp. 12, 13, 36)*

IGZO Indium Gallium Zinc Oxide *(pp. 1, 10, 11, 18, 19, 37)*
IoT Internet of Things *(pp. ix, xi, 1, 7, 25)*
IPA Isopropyl Alcohol *(p. 24)*
ITO Indium Tin Oxide *(pp. 15, 16)*

LNO Lanthanum Nickel Oxide *(p. 16)*
LRS Low Resistance State *(pp. 12, 13, 36)*

MIM Metal-Insulator-Metal *(p. 13)*

NVM Non-Volatile Memory *(pp. 5, 12)*

OTS Ovonic Threshold Switching *(p. 11)*

PCM Phase Change Material *(p. 19)*
PCRAM Phase Change RAM *(pp. 12, 19)*
PIM processing-in-memory *(p. 6)*
PMC Programmable Metallization Cells *(p. 13)*
PVD Physical Vapor Deposition *(pp. 24, 26)*

RAM Random Access Memory *(pp. xxii, 1, 12)*
RRAM Resistive RAM *(pp. 1, 9, 10, 12, 19)*
RS Resistive Switching *(pp. 18, 36)*
RV Read Voltage *(p. 36)*

SCS Solution Combustion Synthesis *(p. 1)*
SDS Sodium Lauryl Sulfate *(p. 21)*
SEM Scanning Electron Microscopy *(p. 18)*
SSD Solid-State Drive *(p. 12)*
STT-MRAM Spin-Transfer Torque Random Access Memory *(p. 12)*

TAOSs Transparent Amorphous Oxides Semiconductors *(pp. 17, 18)*
TCM Thermochemical Mechanism *(pp. 12, 13)*
TFT Thin-film Transistors *(pp. 17, 18)*

VCM Valence Change Mechanism *(pp. 12, 13, 18)*

XRD X-Ray Diffraction *(p. 18)*

ZTO Zinc Tin Oxide *(pp. ix, xi, xv, xvi, 1, 10, 11, 18, 21–33, 39–42, 44, 46, 47, 49–51, 63)*

Symbols

V_o	Oxygen Vacancies *(p. 38)*
k_B	Boltzmann constant *(pp. 44, 46)*
A	Ampere *(pp. 34, 39, 41, 67)*
A^*	Effective Richardson constant *(p. 44)*
ϕ_B^{eff}	Effective barrier height *(pp. 44, 45)*
ϕ_B^m	Mean barrier height *(pp. xix, 44, 45)*
E	Electric field *(p. 46)*
ε_0	Vacuum permittivity *(p. 46)*
ε_r	Relative permittivity *(p. 46)*
η	Ideality factor *(p. 44)*
eV	Electron volt *(pp. 11, 18)*
i	Current *(pp. 3, 44)*
J	Current density *(p. 44)*
m^*	Effective electron mass *(p. 44)*
m_0	Free electron mass *(p. 44)*
N_c	Effective density *(p. 46)*
μ	Electron mobility *(p. 46)*
$R_{ON/OFF}$	On/Off resistance ratio *(pp. 36, 50)*

ϕ	Flux *(pp. 3, 4)*
ϕ_B	Schottky barrier height *(p. 44)*
ϕ_t	Energy level of the traps *(p. 46)*
q	Charge *(pp. 3, 4, 44, 46)*
R	Resistance *(p. 5)*
ρ_2	Linear voltage dependency of ϕ_B^m *(p. 45)*
ρ_3	Linear voltage dependency of σ_B^2 *(p. 45)*
rpm	Rotations per minute *(pp. 21–23, 28, 29)*
R_s	Series resistance *(pp. 42, 44, 45, 51)*
s	Second *(pp. 28, 29, 36, 50)*
σ_B	Standard deviation *(pp. xix, 44, 45)*
T	Temperature *(pp. 44, 46)*
v	Voltage *(p. 3)*

Chemical Symbols

Ag	Silver *(pp. xvi, 11, 15, 16, 27–29, 34, 37–42, 50)*
Ag_xO	Oxidized Silver *(pp. 10, 11)*
Al	Aluminum *(pp. 15, 16)*
Au	Gold *(pp. xv, xvi, 15, 16, 28, 29, 34–37, 39, 40, 50)*
$CH_3OC_2H_4OH$	2 - Methoxyethanol *(pp. 22, 23, 49)*
$CO(NH_2)_2$	Urea *(pp. 23, 49)*
Cu	Copper *(pp. 15, 16)*
$H_{24}Mo_7N_6O_{24}.4H_2O$	Ammonium Molybdate Tetrahydrate *(p. 21)*
H_2O	Water *(pp. 21, 24, 49)*
MoO_3	Molybdenum Trioxide *(pp. ix, xi, xv, xvi, 1, 18, 19, 21–28, 30, 31, 33–40, 49–51, 63)*
N_2	Nitrogen *(p. 32)*
NH_4NO_3	Ammonium Nitrate *(p. 23)*
Ni	Nickel *(p. 15)*
Pt	Platinum *(pp. xv, xvi, 15, 16, 24, 25, 27–29, 34–42, 44)*
$SnCl_2.2H_2O$	Tin (II) Chloride Dihydrate *(pp. 22, 23)*
TaN	Tantalum Nitride *(pp. 15, 16)*
Ti	Titanium *(pp. xv, xvi, 15, 16, 24, 25, 27–29, 34–42, 50)*
W	Tungsten *(p. 16)*

$Zn(NO_3)_2.H_2O$	Zinc Nitrate Hexahydrate *(pp. 22, 23)*
ZnO	Zinc Oxide *(pp. 9, 10)*

1 Introduction

1.1 Motivation and Objectives

Recently, the emergence of new technologies in the IoT and wearables has brought about a new era of electronic devices and their applications. In this realm, memristor-based in-memory processing systems have become a preferable architecture over the traditional Von Neumann's design due to their unique characteristics such as low power consumption and high-speed processing. This is especially crucial for edge computing in IoT systems, where real-time scenarios and Artificial Intelligence (AI) tasks require massive computing and parallel processing. Memristive devices have found their use in digital gates, as well as in reconfigurable logic circuits, due to their small size and efficiency.

Furthermore, the compatibility of memristors or Resistive RAM (RRAM) with traditional Complementary Metal-Oxide-Semiconductor (CMOS) has also driven the development of CMOS hybrid integrated circuits.

With the need for large-scale and cost-effective production of customized devices, there is a growing need to explore techniques for producing memristors on demand.

This technology can be fabricated by solution-based processes, which are considered promising methods due to their uniform and pure thin films, and the need for low temperatures to be performed. Another advantage is the lower costing process and the more straightforward fabrication method, not ruling out the similarity of reliability of those processes using vacuum.

In the past, the Indium Gallium Zinc Oxide (IGZO) solution-based memristor was studied using metal nitrates as precursors with the benefits of a Solution Combustion Synthesis (SCS) to produce the active layer of the RRAM devices. The objective of this work is, by using the same techniques, to replace the IGZO layer with ZTO and/or MoO_3, which require fewer raw materials and have been found

to exhibit high memristive behavior and are thus critical for use in memristive devices.

1.2 Document outline

The thesis is divided into the following chapters: Chapter 2 presents the main theoretical aspects of the memristor, their practical applications as well as some of the materials to fabricate them, including the ones used in this thesis. Chapter 3 presents the methods of manufacturing and characterization of memristors and diode devices. Chapter 4 shows the results of all made tests during the device's characterization and their interpretation. Chapter 5 presents the final conclusion of the thesis and some possible future improvements and work.

2

The Memristor and its Applications

2.1 Description of a memristor

There are three passive basic elements well known in the electronic community, resistors, capacitors, and inductors. These three two-terminal components are defined by the relation between two of the variables from $\{v, i, q, \phi\}$, as v, i, q and ϕ are basic variables of circuit theory, representing voltage, current, charge and flux, respectively. For instance, the relation between $\{v, i\}$ is characterized by the element called resistor, the relation $\{v, q\}$ by a capacitor, the relation $\{i, \phi\}$ by an inductor. We can also deduce that the relation between $\{v, \phi\}$ and between $\{i, q\}$ is given by 2.1 and 2.2 respectively. Those mathematical relations are, more clearly, shown in figure 2.1.

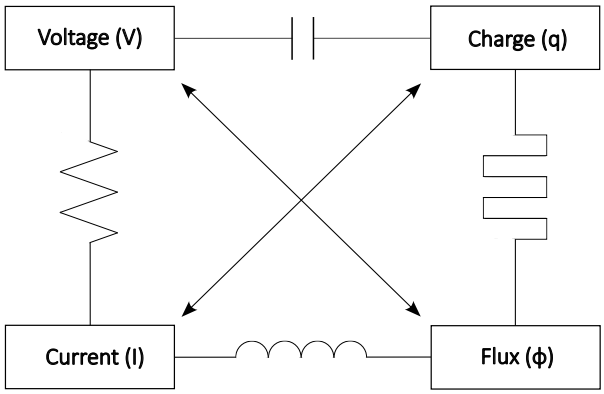


Figure 2.1: Relation between passive elements.

$$\phi(t) = \int_{-\infty}^{t} v(\tau)\, d\tau \tag{2.1}$$

$$q(t) = \int_{-\infty}^{t} i(\tau)\, d\tau \tag{2.2}$$

We can notice that one relation between these four circuit variables is missing in this electronic context, that is because the $\{q, \phi\}$ relation is characterized by an element introduced and called memristor (figure 2.2). This term comes from the combination of two well-known terms, a concatenation of "memory resistor", the fourth circuit element, in which the voltage of a charge-controlled memristor and the current of a flux-controlled memristor can be defined by the equations 2.3 and 2.4 respectively, based in the mathematical definition in [2].

$$v(t) = M(q(t)) \times i(t) \text{ where } M(q) \equiv \frac{d\phi(q)}{dq} \tag{2.3}$$

$$i(t) = W(\phi(t)) \times v(t) \text{ where } W(\phi) \equiv \frac{dq(\phi)}{d\phi} \tag{2.4}$$

Being $M(q(t))$ the incremental memristance and $W(\phi(t))$ the incremental memductance.

In line with [3], this element was introduced for logical consistency and symmetry considerations.

Indeed, the memristor's resistance depends on the amount of charge that has traversed the circuit. When an electric current moves in a particular direction, the resistance escalates, but when the current moves in the opposite direction, the resistance diminishes. Yet, it is important to note that resistance cannot be negative. When the flow of current stops, the resistance maintains the same value it possessed before. This signifies that the memristor retains a recollection of the most recent current that coursed through it [4].

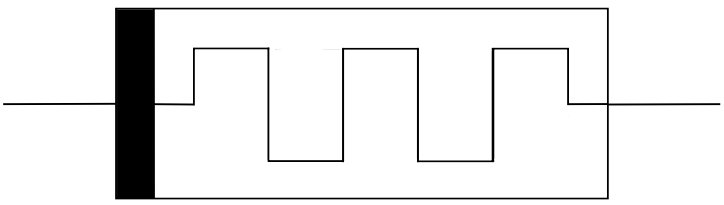


Figure 2.2: Memristor symbol.

Memristor has been primarily introduced by Leon O. Chua in 1971 [2], but only in 2008 this type of passive device was presented with a physical model by the HP Lab's scientists [5]. With that, it was discovered, by an analytical example, that the phenomenon of memristance arises naturally in nanoscale systems where the

movement of electrons and ions in the vapor-deposited are linked and controlled by a bias voltage.

$$v = R\,(w) \times i \text{ where } \frac{\mathrm{d}w}{\mathrm{d}t} = i \tag{2.5}$$

This analytical function presented in 2.5 is Ohm's law with an addition of a state variable of the device (w), that only charge is acceptable. R represents a value of resistance that varies based on the device's internal state.

According to [3] the memristor can be used as a binary Non-Volatile Memory (NVM). It means that two different values of resistance are chosen to code the binary states "0"and "1". This ultimately results in a multitude of applications such as a new type of memory and the creation and implementation of more powerful and efficient neural networks, as these types of devices can simulate the behavior of synapses that are found in our brain [6]. Following the same line of thought, memristors can be used as an element to construct digital logic gates and to implement neural networks, which improves the energy efficiency and speed for pattern recognition analysis with machine learning algorithms [7].

Furthermore, this element contributes to more applications such as in the field of neuromorphic computing, due to the parallelism achieved in computing with these devices, where, also, the information is stored, avoiding data movement and memory limitations in traditional digital computing, such as the well-known Von Neumann architecture.

2.2 Memristor-based system

Von Neumann's architecture (figure 2.3) consists of a computer architecture, which has as components the Central Processing Unit (CPU) part, the memory, and the I/O part, the last component for communication with external devices. In this architecture, the CPU retrieves instructions from memory, performs operations and several calculations on certain data, and stores the corresponding results back in memory [8].

Over the past few years, this type of architecture was the benchmark for most computer concepts, mainly because of the ability to modify its instructions, meaning that the instructions and data are stored in the same memory, which can be accessed by the CPU. This particularity allows for much greater flexibility in programming [9].

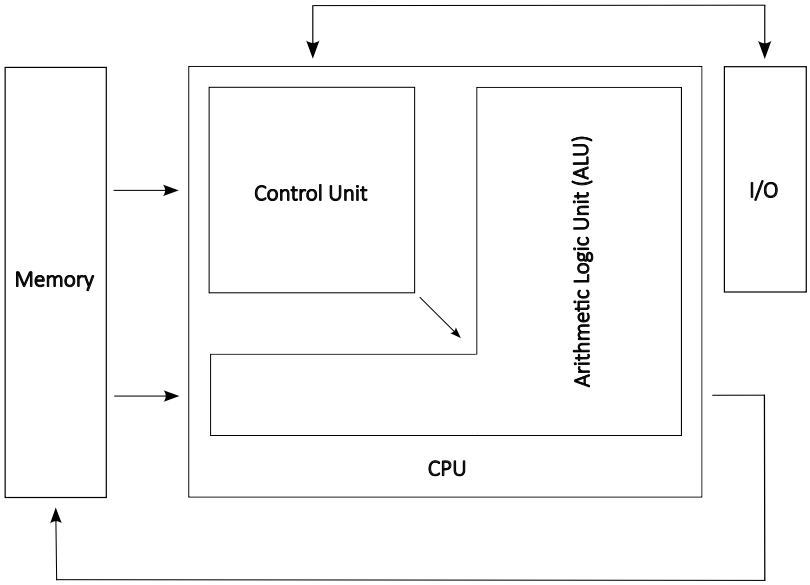


Figure 2.3: Traditional Von Neumann architecture.

However, there are some drawbacks. The main drawback is that Von Neumann's architecture lacks parallelism. In other words, with this architecture, the CPU can only execute one instruction at a time. The CPU is idle until the data is retrieved from memory, which means that the CPU is unable to work on multiple tasks simultaneously. This is Von Neumann's architecture bottleneck. Another problem with this architecture is the fact that memory and CPU are separated, which increases the time of operations. The data has to be transferred back and forth between the memory component and the processing unit (CPU). Resulting in a lack of efficiency (over 100 times less efficient than processing-in-memory (PIM) architectures) and slowing the process down [10, 11].

In order to improve energy efficiency, improve the processing time of instructions and data, and have the ability to perform several tasks at the same time, the need arose to find new solutions for solving Von Neumann's problems. This includes the emergence of non-Von Neumann architectures with PIM technology, such as neural network processors, quantum computers, Field Programmable Gate Arrays (FPGAs), DNA computing, and memristor-based systems. The last is the one we will focus on the most.

Each one of these recent architectures has different characteristics.

- **Neural network processors** - Designed and used for running artificial neural networks and optimized for matrix multiplications, which are a key operation in many neural network algorithms, this architecture must be general to

support a wide range of applications and, at the same time, the design must be efficient, to match neural network's characteristics [12];

- **Quantum computers** - Use quantum-mechanical phenomena, such as superposition and entanglement, to solve operations. This type of architecture can perform those operations much faster than the traditional computer with Von Neumann architectures [13];

- **FPGAs** - Semiconductor devices that allow reconfiguration to perform several digital logic functions. With this capability, it is possible to reprogram these architectures to do different tasks. These logic blocks can be, for example, a simple transistor or even a complex microprocessor. It can also implement several combinational and sequential logic functions [14];

- **DNA computing** - This type of architecture uses DNA, molecular biology, and biochemistry instead of silicon-based computer technologies, providing a high information storage capacity and low energy dissipation during processing. Also, it has the benefit of solving complex problems and presenting different possible solutions, all at once and with parallelism [15].

- **Memristor-based systems** - These architectures use memristors, a basic circuit element that remembers its previous state, and are useful in several applications, such as neural network computations, memory storage, signal processing, robotics, and in pattern recognition. In the field of neural networks, this type of architecture can improve performance and capabilities, such as energy efficiency, a more compact computing system, the capability of parallel processing, and a relevant reduction of active power needed for implementing a basic neuron function [7].

Based on this last architecture, and taking into account the world of IoT, which aims to interconnect physical objects, such as devices equipped with sensors and internet connectivity, with the purpose of sharing data and being controlled remotely, the edge computing in these IoT systems has to be more power efficient and have higher processing speeds than the conventional technology, to manage the usually limited resources in real-time scenarios and AI tasks. The referred world has grown so big and with such significant progress, that the need for massive computing and parallel processing became a reality, due to deep learning which involves large data sets and a multilayer network structure. One way to achieve these requirements is the use of a memristor-crossbar system, represented in figure 2.4 [16].

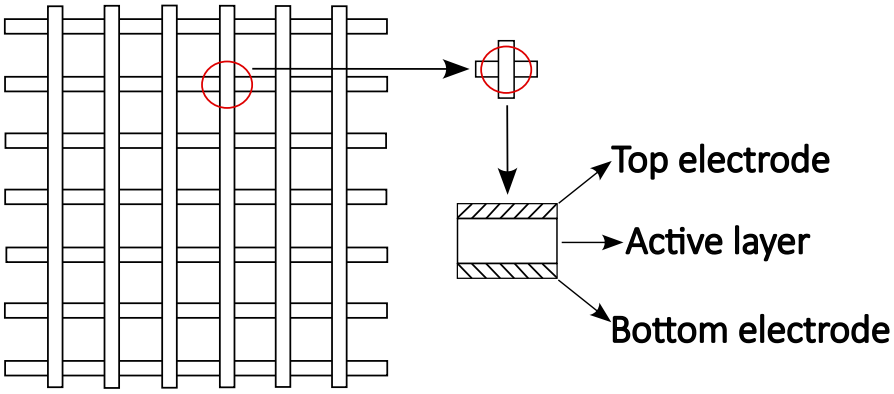


Figure 2.4: Memristor crossbar representation.

When using memristive crossbar arrays, beyond the various applications, mentioned before, and advantages, like more efficiency in algorithms implementation with less power consumption, this system has a major challenge that hinders the effectiveness of a memristor crossbar array. This obstacle is called the sneak path current issue and leads to a reduction in the array's reliability by introducing errors when programming or reading the resistance levels of memristors [17].

It has been studied and efforts have been made to solve this sneak path current issue. With this in the realm, architectures and structures were developed to overcome the problem, like including one-transistor one-memristor (1T1M), one-diode one-memristor (1D1M), and one-selector one-memristor (1S1M). Apart from these multi-device systems, single ones are studied, more specifically, self-rectifying memristors and self-selective memristors. These last structures have received more attention due to their simpler architectures [17].

The objective of this work is to develop bipolar memristors, that can be integrated into crossbars with the need of a transistor to overcome the sneak path current issue and diodes, that being integrated with a unipolar memristor it is possible to overcome the same current issue.

However, to implement the unipolar/bipolar memristors into crossbars, and to solve the sneak path problem, a second device is needed. Usually, the transistor is used integrated with a bipolar memristor, due to its ability to behave like a switch, this makes an active crossbar with a 1T1M structure. More specifically, when the series field-effect transistor is turned ON, it essentially acts as a highly conductive wire. As a result, the voltage can completely pass through the memristor, regardless of the bias voltage's polarity. This makes it easier to switch the state of the memristor. Conversely, when the series field-effect transistor is in the OFF state, very little current flows through the cell, and there is virtually no voltage drop across the memristor. By intentionally controlling the ON and OFF states of these

transistors, it becomes possible to accurately choose a specific memory cell.

The other two structures, mentioned before, 1S1M and 1D1M (integrated with a unipolar memristor) have been attracting more attention due to their higher density potential than the previous 1T1M structure. Being a two-terminal device requires less space than three-terminal devices, that is the case of transistors in the 1T1M structure.

In the case of the 1D1M, connecting these two devices in series shows a resistive switching behavior which has rectifying properties, allowing the resolution of the sneak path issue. To achieve these properties, the most important factor is the rectification ratio, which is the ratio between the current flowing in one direction and the opposite direction. A higher rectification ratio is crucial because it helps prevent unwanted currents and enables the use of larger arrays of passive crossbars. Additionally, we need to pay attention to the forward current density because a high forward current is required to activate the series memristor. Having a higher forward current density allows us to make smaller diode cells and achieve a greater level of integration [17, 18]. This type of structure is also useful due to its endurance, compatibility with CMOS technology, and low-temperature fabrication process.

For the diode in a 1D1M RRAM structure, you would typically use a p-n junction diode or a similar type of diode that provides rectification characteristics. The choice of diode depends on the specific requirements of your RRAM device, such as switching speed, voltage levels, and operating temperature. Below are some common types of diodes that can be used in 1D1M RRAM structures.

- **P-N Junction Diode** - This is a basic diode consisting of a p-type and an n-type semiconductor material. It provides good rectification properties and is commonly used in various electronic devices. In [19] the successfully fabricated ZnO-based p-n diode exhibited both impressive rectifying properties and enhanced resistance stability. This stability is attributed to the nanowire structure, which serves as a source for supplying and storing oxygen ions, ultimately enhancing the reliability of the switching process. This structure holds significant promise for enabling extensive integration on a large scale and has the potential to find applications in the realm of 5G technology combined with AI in the future.

- **Schottky Diode** - Schottky diodes have a metal-semiconductor junction and are known for their fast switching speeds. They are often used when high-speed switching is required in RRAM devices. In addition, this type of diode offers numerous benefits when compared to P-N junction diodes, such as

reduced voltage drop, rapid recovery times, minimal junction capacitance, and straightforward manufacturing procedures, as said in [20].

- **Zener Diode** - Zener diodes are used for voltage regulation and can also be used in RRAM structures for specific applications where voltage regulation is necessary.

  In contrast to conventional P-N junction diodes that are not suitable for serving as a selector device in bipolar RRAM applications, the Zener diode allows current to flow in the forward direction like a typical diode and also in the reverse direction if the voltage exceeds the breakdown threshold. Consequently, it is worthwhile to explore the viability of employing a Zener diode as the selector device for high-density bipolar RRAM cross-bar configurations [21].

- **Tunnel Diode** - Tunnel diodes can exhibit negative differential resistance, which can be advantageous in certain RRAM applications. However, they are less common in RRAM devices compared to other diode types.

The choice of diode should be made based on the specific requirements of your RRAM device, such as the desired switching characteristics, voltage levels, and operating conditions. Additionally, the compatibility of the diode with the materials and processes used in RRAM fabrication is crucial.

Schottky diodes, also known as Schottky barrier diodes or hot carrier diodes, are semiconductor devices that have a unique junction formed between a metal and a semiconductor material, unlike regular P-N junction diodes, which have a junction between two different types of semiconductor materials (p-type and n-type). This metal-semiconductor junction creates a Schottky barrier, which is responsible for the diode's distinctive properties. This is the type of diode that has the focus of this work, as the type of device manufactured and characterized later in this document, based on ZTO solution.

In past research, more specifically in [22] was fabricated a silver oxide Schottky diode based on ZnO. This study showed that it was possible to obtain a very high rectifying ratio between the OFF and ON states of the Schottky diode, this value exceeded 8 orders of magnitude at approximately 1 V.

Moreover, in [22] it was observed a reduction in oxygen vacancies at the boundary between Ag_xO and single crystalline ZnO when oxygen was introduced during the deposition of Ag_xO and, consequently, in [23] it was manufactured and characterized Ag_xO/IGZO and it was possible to observe that the electrical

characteristics underwent a significant transformation, transitioning from Ohmic behavior in Ag/IGZO to Schottky behavior in Ag_xO/IGZO. This change was marked by a rectification ratio of 1.9×10^8, a Schottky barrier height of 0.96 eV, and an ideality factor of 1.03.

These studies were the background to the Schottky ZTO-based diode manufactured in this work.

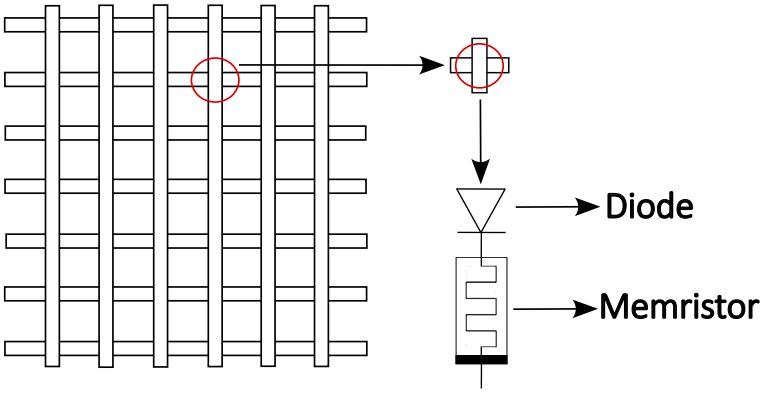


Figure 2.5: 1D1M crossbar representation.

In terms of the 1S1M structure, in order to make large-scale arrays more energy-efficient and improve the performance of programming and reading data from individual cells, it is crucial to develop selector devices with strong nonlinearity. Over the past years, extensive research has been conducted on nonlinear selectors utilizing the tunneling barrier, Ovonic Threshold Switching (OTS), and p-/n-combination.

The nonlinearity observed in tunneling barrier selectors arises from their inherent physical properties. These selectors generate sharp, high currents without requiring additional assistance from Joule heating. Furthermore, their performance remains consistent across various temperatures, which is advantageous for minimizing energy consumption and accommodating various temperature conditions. Tunnel selectors also exhibit impressive speed and reliability.

However, there is a drawback associated with tunneling barrier selectors – they necessitate a high-temperature fabrication process, which limits their potential for further integration. Therefore, there is a need to explore the development of tunneling barrier selectors that can operate effectively at lower temperatures [17].

This document also presents the development of a diode device that can be integrated with a unipolar memristor to overcome the sneak path issue. This diode is mentioned and carefully studied later in this document.

When talking about resistive switching devices, RRAM is commonly referred to because of its ability to integrate architectures with CMOS technology as said previously in 2.2, due to its simple structure, low power consumption, high density and operation speed, characteristics that have potential to be a choice of the upcoming generation of NVM solutions [24].

Within the domain of NVM devices, NAND Flash memories have been used as the most popular memory. That happens because of their low power consumption which makes this flash technology difficult to unseat. In the realm of corporate data storage, such as with flash-based Solid-State Drive (SSD) configurations, extensive parallel processing is already being employed to provide a superior level of input/output operations per second (IOPS) at lower energy consumption and cost compared to all other currently viable and feasible technologies [25, 26].

Nevertheless, as previously mentioned, memristive RAM arises as a promising technology for NVM devices, such as magnetoresistive and atomic configuration ones.

In magnetic memristive memory, the data bits are stored using magnetic states, and with this concept, the Spin-Transfer Torque Random Access Memory (STT-MRAM) was developed. It offers near-zero standby power consumption, low read access time, and small area requirement [27].

In the atomic memristive configuration area, such as RRAM or Phase Change RAM (PCRAM), outperform NAND Flash memories by offering equivalent characteristics but with superior switching speed, durability, and potential for future scalability. In addition, these devices have the capability to retain intermediate resistance levels due to their operation involving the reconfiguration of atomic structures, granting them a broader range for data storage [28]. More specifically, in RRAM, the memory exhibits an electrical reversible mechanism known as "resistive switching"that transitions between a Low Resistance State (LRS) and a High Resistance State (HRS) [29]. For this, a variety of atomic memristive devices can be split into various types of redox-based resistive mechanisms that are responsible for switching between these HRS and LRS by forming and disrupting conductive filaments when subjected to temperature and/or electrical voltage. The redox-based resistive mechanisms are named, Electrochemical Metallization Mechanism (ECM), Valence Change Mechanism (VCM), and Thermochemical Mechanism (TCM), all these types have their own advantages and drawbacks depending on the tasks that are supposed to perform in particular conditions and applications.

Nevertheless, the ECM and VCM are preferable types, due to their functionalities and reliability [30].

The ECM also known as Programmable Metallization Cells (PMC) or Conductive Bridge RAM (CBRAM), consists of a bipolar switching, where the formation and rupture of metallic filaments or the conductive filament (CF) are observed and therefore the short-circuit (SET) and the disconnection (RESET) of the memristive device is also observed, defining the two states of high resistive state (HRS) and the lower one (LRS) [30]. When an electrical voltage is applied, the electroforming process involves the ionization of metal atoms, leading to the migration of metal cations through the resistive switching layer. This, in turn, induces changes in internal resistance. Typically, electrolytic materials with high ion conductivity and low electron conductivity are selected to manufacture ECM devices [29].

The TCM consists of a unipolar switching triggered by Joule heating, more specifically electrode metal diffusion with current compliance (SET) and then a thermal dissolution of the filament with higher heating (RESET). Due to this mechanism, unipolar switching occurs, as said primarily, in which the formation and dissolution of the conductive filament appear in the same polarity, solely dependent on the voltage level [31].

Finally, VCM consists of a bipolar switching induced by the migration of oxygen under an electric field - when an increase in the number of missing oxygen atoms (in metal-rich areas) leads to a rise in conductivity and the creation of conductive pathways, the SET state is active. When oxidation of the filament is observed, the RESET state is active [32].

After some study, it was observed that ECM demonstrates a better performance compared to the VCM, this ECM showed a lower variability and a lower bit-error-rate (BER) for cycling and retention due to larger ON/OFF ratio.

These various memristive devices/types are split by fabrication material, and likewise modulation geometries, there are advantages and drawbacks that differ by the need in different applications and operations [33].

Electrical stimulated resistive switching behavior described previously, presents two distinct types depending on the operating voltage polarity required for resistively switching Metal-Insulator-Metal (MIM) systems. One of them is called unipolar, and this type is visualized when the switching process is not impacted by the positive or negative nature of the voltage and current signals involved. The other type is called bipolar, on the other hand, this is a type of resistive switching where the setting to an ON state takes place when the voltage has a certain polarity and the resetting to an OFF state occurs when the voltage has the opposite

polarity [34]. This last switching behavior is described in figure 2.6, where is easily observed a hysteresis loop in the bipolar type of switching.

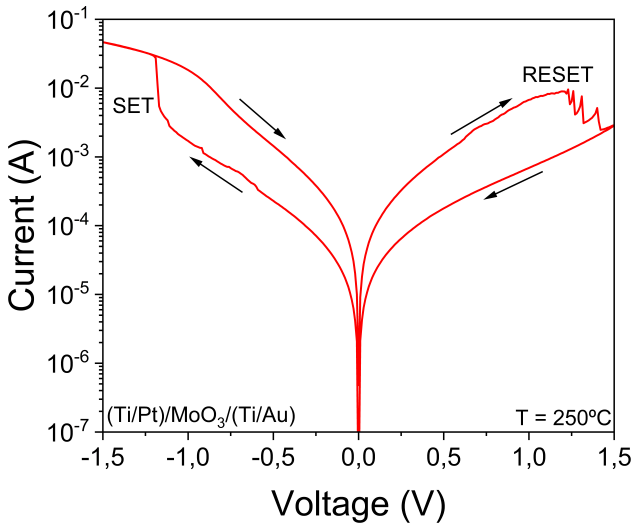


Figure 2.6: Bipolar switching behavior.

Additionally, memristors have better process compatibility with traditional semiconductor technology (CMOS) than with newer technologies such as quantum computing, molecular computing, quantum dots, and spin-wave devices [35]. This compatibility, for example, contributes to the use of CMOS hybrid integrated circuits for reconfigurable logic, which was fabricated by integrating memristor-based crossbars onto a foundry-built CMOS platform [36].

With that has emerged a need to explore some techniques to produce customized devices on demand, in large quantities, and as cheaply as possible.

2.3 Fabrication techniques

These resistive switching devices, as observed in figure 2.7, are composed of a top, a bottom electrode layer, and an active layer, as a sandwich layer. These top and bottom layers can be composed of several different metals and conductive polymers, while the active layer can be made of a metal oxide, polymer, or dielectric [37, 38]. The active layer can be composed of organic or inorganic rectifying materials.

More clearly, organic materials, such as polymers, are attractive due to their flexibility and low cost, but they can suffer from reliability and stability issues due to the influence of temperature, humidity, and other environmental factors.

Inorganic materials, such as metal oxides, have high stability and reliability, but they tend to be more expensive and less flexible than organic materials.

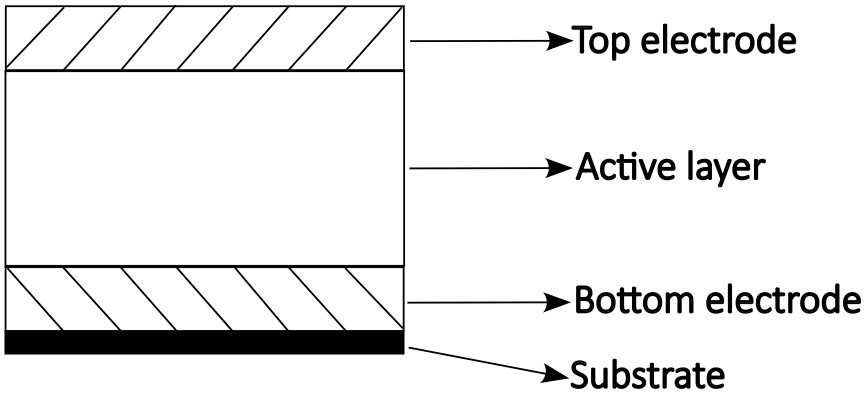


Figure 2.7: Cross-sectional view of a memristor.

Additionally, the formation of metal oxides often requires high temperatures, which can be difficult to achieve in a cost-effective manner. To summarize, organic materials have the benefit of being easily produced with simple methods and require lower costs, but inorganic materials are more stable in terms of switching. On the other hand, organic materials have a higher degree of mechanical flexibility [39].

To attain the majority of these characteristics in inorganic substances, the production techniques that primarily utilize vacuum methods must be shifted to solution-based methods, such as coating and printing techniques [28] that have advantages like flexibility, non-toxicity and a lower cost compared with the vacuum method.

The configuration of the two electrode layers mentioned before is crucial to the resistive switching behavior of these devices, in addition to the active material present in the solution. There are two distinct electrode configurations that have been documented in the literature: symmetrical and asymmetrical [24, 28].

These symmetric devices are made of equal metals as bottom and top electrodes and are placed symmetrically in the memory cell. This results in an equal distribution of the current and therefore reduces the potential for imbalances or short-circuits, as well as this type is easier to fabricate, as both electrodes can be manufactured using the same process. Nevertheless, symmetric electrode configurations tend to have lower switching performance compared to asymmetric configurations, which can limit their use in high-speed applications [28]. These referred materials could be based on inert metals, such as Au, TaN and Pt or active and oxidizable metals, like Al, Indium Tin Oxide (ITO), Ni, Ti, Cu and Ag.

Asymmetric electrode configuration is based on different positive and negative (top and bottom) electrode materials with different shapes and sizes, which can

result in improved performance and energy density. Unlike the symmetric configuration, this configuration presents an improved switching performance, achieved by varying sizes and shapes of different electrodes materials, and increased reliability, taking into account that with different materials is possible to achieve major stability and resistance uniformity. However, this type of configuration requires more manufacturing complexity, with more different materials needed to produce these devices, and some instability is observed [28]. These materials could be based on inert-inert, like Pt-Au; based on inert-active, such as Pt-Al, Pt-Ti, Au-Al, Pt-Ag, Au-Ag, and TaN-Cu or based on active-active, for example, Cu-Al, Cu-Ag, Ti-Cu, W-Al, Lanthanum Nickel Oxide (LNO)-Al, Fluorine Doped Tin Oxide (FTO)-Ti, FTO-Al, Antimony Tin Oxide (ATO)-Cu, ITO-Ag, ITO-Al, and ITO-Ti.

In the fabrication process, various methods of memristor fabrication are presented and discussed.

There are two main types of memristors, printed, and vapor-deposited ones, which vary in size and have different advantages and disadvantages.

Printed memristors are larger, low cost, compared with vapor-deposited ones, can be fabricated with flexible substrates (making them ideal for applications where flexibility is required, like wearables and many other gadgets), are non-toxic, have the ability of large-scale integration (memristors can be printed onto large areas, enabling high-density integration and scalability), and high customizability rate (allows customization of the memristor's properties, which gives more freedom for optimization in specific applications).

Vapor-deposited fabrication offers higher performance; and increased reliability, due to the use of inorganic materials that are less susceptible to wear and tear; scalability, in other words, these memristors are made using established semiconductor fabrication processes that make it easier to scale up the production; and improved compatibility, this last because vapor-deposited memristors are compatible with a wide range of materials and fabrication processes, making it easier to integrate other devices.[38].

For this, called vapor-deposited memristors, fabrication techniques, such as Physical Vapor Deposition (PVD) [40], Chemical Vapor Deposition (CVD) [41], Photolithography [42], Electron Beam Lithography (EBL) [42], Dry Etching [43], Wet Etching [43], Atomic Layer Deposition (ALD) [44], Nanoimprint Lithography [45], Soft Lithography [45]; is commonly used.

In turn, printed memristors have different fabrication techniques already used, these techniques are divided into non-contact fabrication methods, which usually

refer to methods that do not require physical contact to be made with memristor material. The electrical properties of the memristor are controlled through the application of electrical fields, optical signals, or magnetic fields. This enables more precise control of the memristor's properties without the risk of damage caused by contact with metal electrodes, and contact fabrication methods that refer to a method in which electrical contacts are made directly into the memristor material to control its electrical properties. This typically involves depositing metal contacts onto the memristor material and patterning them using lithography [38]. As non-contact fabrication, such as inkjet printing [46], electrohydrodynamic technique [37], aerosol-jet (AJP) [47], slot-die coating [48], and 3D printing. On the other hand, contact fabrication consists of gravure printing [49], offset printing [50], flexographic printing [51], micro-contact [52] and nano-contact printing, dry transfer printing, spin coating printing [53], screen printing [54], and electrostatic spray technique.

For vapor-deposited memristors, these previously mentioned vacuum methods result in top-notch devices that perform well and can be relied upon. However, there are downsides to these approaches, including their high cost, time-intensive nature, and the need for a controlled setting.

To surpass these issues, solution-based processes are used. This manufacturing process is not only simpler and more cost-effective, but it also operates at lower temperatures (in the majority a range from 200ºC and 500ºC [28]). Moreover, the device's performance rivals that of its counterparts crafted within vacuum environments. With this last process is possible to attain extensive area production without the need for costly techniques by using the coating and printing techniques [55–59] mentioned before.

In this document, the focus is on solution-based processes. This process is commonly used in organic solar cells, Thin-film Transistors (TFT)'s, and flexible displays, being the TFT's not only one example of the use of this process but also stands as the most extensively researched outcome [60]. This changed at the time of the discovery of the resistive switching device, also known as the memristor. Affordable techniques offer the potential to create such resistive switching devices, presenting a hopeful avenue for the advancement of flexible electronics. Presently, the predominant method employed is spin coating which is widely investigated for use in transparent electric devices like Transparent Amorphous Oxides Semiconductors (TAOSs) [61]. Nevertheless, the aspiration for the future lies in the adoption of printing techniques that align with large-scale production, aiming to fabricate these devices [28].

2.3.1 Zinc Tin Oxide

ZTO which is one the solutions that we can call by TAOSs which have wide applications in the microelectronic industry, such as in flat-panel displays, electromagnetic shielding, organic light-emitting diodes, electrochromatic windows as well as active channel material for TFT [61]. This solution-based material has the advantage of using material that exists in abundance, unlike IGZO (also a TAOSs material) or other solution-based materials and has the advantage that it can be manufactured without the use of thermal treatment, and therefore, the possibility of using flexible plastic substrates or even paper [62].

This material is transparent for visible light, amorphous, and can be handled at lower temperatures (compared to silicon) [63]. Zinc tin oxide has the quality of having a wide bandgap, typically 3.35–3.89 eV [64], which makes it possible to make smaller, faster, more reliable, and more efficient than silicon-based materials. Apart from this, TAOSs is recognized for producing exceptionally large ON/OFF ratios, as evidenced by diodes with rectification ratios of 10^6. These use cases demonstrate the material's capacity to transition from an insulating state to a metallic conductor through the modulation of the Fermi level [62].

Furthermore, Scanning Electron Microscopy (SEM) images reveal that the ZTO thin film coatings are exceptionally consistent and free of imperfections in their texture, also these devices exhibited functionality in a Resistive Switching (RS) mode akin to filamentary VCM-type which was regulated by inherent dopants, such as oxygen vacancies. The X-Ray Diffraction (XRD) pattern displays a wide and minor peak within the range of $20° \sim 28°$, suggesting that the spin-coated ZTO thin films are predominantly lacking a crystalline structure and are instead mostly amorphous. Besides, the spectrum illustrates that the ZTO thin film exhibits exceptional transparency, allowing $\sim$ 95% of visible light to pass through it (400 - 700 nm)[61, 62].

This material has mainly been employed as transparent conductors in gas sensors, and more recently, as pathways for TFTs [61].

2.3.2 Molybdenum Trioxide

MoO_3 is a compound composed of molybdenum and oxygen atoms. It can exist in several crystalline forms, including orthorhombic, monoclinic, and hexagonal structures. However, when prepared in amorphous form (lacking a regular, repeating crystal lattice), it becomes suitable for various applications in electronics, especially as a TAOSs.

Previously, extensive research has been conducted on using Tellurium-based Chalcogenides (GST) as a Phase Change Material (PCM). GST demonstrates rapid and dependable reversible phase transitions, resulting in high-speed performance and exceptional durability in GST-based PCRAM. Nonetheless, amorphous GST possesses a low crystallization threshold, resulting in inadequate thermal stability and subsequently compromising data retention capabilities [65, 66]. Recently, there have been reports of IGZO exhibiting resistive switching through a phase transition, transitioning from an amorphous state to a crystalline state, but in matters of phase change through temperature, IGZO has a high melting point, around $1900°C$, resulting in substantial energy consumption during the amorphization process. Among the many oxide materials available, MoO_3 stands out due to its comparatively modest melting point of approximately $800°C$ [67], which is not significantly different from that of a conventional PCM like GST, that is around $630°C$ [66].

In addition, to overcome these issues, the Mo-oxide film, with a composition closely resembling MoO_3, exhibited a substantial difference in resistance and superior thermal stability when compared to traditional GST chalcogenide PCM. To add, the resistance difference observed in the Mo-oxide memory device is significantly greater compared to that of conventional GST PCM, over 10^2 and 10^3. Consequently, it stands out as a prospective oxide-based PCM for PCRAM applications, offering enhanced data reading reliability and a higher data retention temperature [66]. Likewise, with this MoO_3 solution, the projected maximum temperature at which data can be reliably retained for a period of 10 years is $179.7°C$ according to the literature. This data retention ability of the amorphous Mo-oxide, as it is initially deposited, surpasses that of conventional Phase Change Materials (PCM) like GST by a significant margin [66].

Overall, these findings suggest that the Mo-oxide film holds great promise as an oxide-based PCM for applications in PCRAM.

As previously mentioned in 2.2, the sneak path current issue is a significant drawback on future crossbar array applications, leading to a misreading of the memory array's state. It was also mentioned that the addition of a second device in series, such as a diode, transistor, or selector, overcomes this issue of leakage current. Likewise, new problems can arise, including increased manufacturing complexity, elevated production expenses, and reduced RRAM storage density.

Recently MoO_3, which has a self-rectifying behavior was introduced as a material with the potential to solve these issues, making it possible to fabricate a necessary self-rectifying RRAM, that can prevent the sneak path without the need

for an extra device. Consequently contributes to a high-density memory array [68].

3

Materials and Methods

In this chapter, it is presented a resume of all procedures and materials used. This includes the preparation of the Zinc Tin Oxide (ZTO) and MoO_3 solutions, their fabrication, and afterwards, the fabrication and characterization of ZTO diodes, and MoO_3 bipolar memristors.

ZTO diodes were developed and characterized by altering the annealing temperature at the manufacturing stage. Likewise, to fabricate and characterize the bipolar memristors with MoO_3, variation in the molar concentration and the number of active layers was studied. The main goal was to identify the optimal conditions for creating a high-performing diode and memristor in terms of electrical capabilities.

3.1 Precursor Solutions Preparation

In this section, the preparation of the solutions of ZTO and MoO_3 are described. Subsequently, these solutions will be deposited by the spin-coating technique in desired substrates, to act as the active layers of the devices proposed for manufacture, namely diodes and bipolar memristors.

3.1.1 Molybdenum Trioxide Precursor Solution Preparation

The MoO_3 synthesis is composed of 6 main steps. In the first approach, the Ammonium Molybdate Tetrahydrate ($H_{24}Mo_7N_6O_{24}.4H_2O$) is weighed and placed in a flask, then, with a syringe's help, a certain quantity of ultrapure water (H_2O) is added, and in the same way, Ethylene Glycol (EG). This approach is made with a ratio between ultrapure water (H_2O) and EG of 80:20 (%). After this process, the solution was magnetically stirred at 450 rpm for 5 min, and then the Sodium

Lauryl Sulfate (SDS) was added, knowing this last reagent is used to improve the subsequent deposition on the substrate. After that, the final solution was, again, magnetically stirred at 450 rpm for a day (24 hours). The above-mentioned solution was deposited and is represented in 3.1, which is the glass flask prepared to store the solution until the deposition on the desired subtract.

Quantities are measured and calculated in order to make a solution for a certain concentration previously thought. In this particular case, two different molar concentrations were studied, 0.1 M and 0.2 M, tested, and characterized afterwards, to be more precise. In the deposition process, these molar concentrations were followed up by two different numbers of active layers (1 active layer for the MoO_3 solution with 0.2 M of molar concentration, and 2 active layers for the MoO_3 solution with 0.1 M of molar concentration).

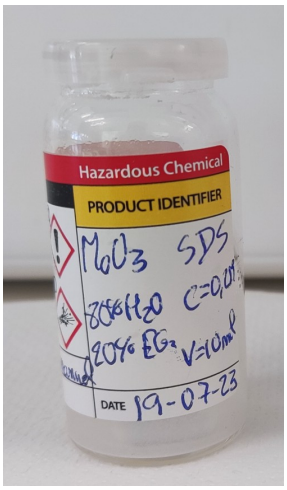


Figure 3.1: MoO_3 solution flask.

3.1.2 Zinc Tin Oxide Precursor Solution Preparation

The ZTO synthesis is composed of 12 main steps. This synthesis process is different from the MoO_3 one, mainly because it is composed of two separate syntheses, which in the end are combined into one. Of these mentioned syntheses, one is based on Zinc Nitrate Hexahydrate ($Zn(NO_3)_2.H_2O$), and the other is Tin (II) Chloride Dihydrate ($SnCl_2.2H_2O$).

In the first place, it is required the weighing of Zinc Nitrate Hexahydrate ($Zn(NO_3)_2.H_2O$) and the reagent is placed in a glass flask. In order to finish this first synthesis, a certain quantity of 2-Methoxyethanol ($CH_3OC_2H_4OH$) is added as the solvent of the solution. After this process, the solution is magnetically

stirred at 450 rpm for 5 min. The above mentioned process is similar to the one described in the previous section 3.1.1, to produce a consistent and see-through solution.

The other synthesis is based on weighing a certain quantity of Tin (II) Chloride Dihydrate ($SnCl_2.2H_2O$) and place in a separate glass flask. The next step is adding Ammonium Nitrate (NH_4NO_3) to this last flask, before adding the 2-Methoxyethanol ($CH_3OC_2H_4OH$) in the same way as the previous synthesis. After the mixing of this last solution at 450 rpm for 5 min (for the same purpose as before), the two solutions were put together in a single flask, and then a certain quantity of Urea ($CO(NH_2)_2$) was added, to enable the production of ZTO with a molar concentration of 0.2 M. This last compound is used for the combustion reaction and serves as a fuel to the two precursor solutions. This solution has a ratio of 75:25 (%) between the Zinc Nitrate Hexahydrate ($Zn(NO_3)_2.H_2O$) solution and the Tin (II) Chloride Dihydrate ($SnCl_2.2H_2O$) solution.

To finish the ZTO solution, and in the same way as the MoO_3 synthesis, the final solution is magnetically stirred at 450 rpm for a day (24 hours). The final solution is presented in 3.2, in the same way as the previous MoO_3 solution, in a glass flask, ready to be stored and subsequently deposited in the desired subtract.

Quantities are measured and calculated in order to make a solution for a certain concentration previously thought. Likewise MoO_3, the ZTO solution was tested and characterized, but in this case, by varying the annealing temperature (250°C, 300°C), in the deposition process of the active layers.

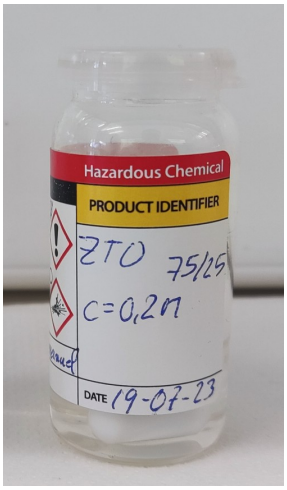


Figure 3.2: ZTO solution flask.

3.2 Thin Film Deposition and Devices Fabrication

This section presents the substrate preparation and cleaning processes, the deposition of the previously made solutions, and the devices' final result. The process of solution deposition, namely the spin-coating technique [53], and the Electron Beam Lithography (EBL) [42] which is the film deposition technique, is here described and explained.

For top and bottom electrode deposition Electron Beam Evaporation (e-beam) was used, which consists of a Physical Vapor Deposition (PVD) technique.

This physical deposition method is a technique used for depositing thin films of material onto various substrates.

In E-Beam PVD or Electron Beam Evaporation, a target anode is bombarded with a high-energy electron beam generated by a charged tungsten filament. The electron beam transfers energy to the target material, causing its atoms to undergo a phase transition from solid to gaseous. These vaporized atoms then travel through the vacuum chamber and condense onto nearby surfaces, including the substrate, forming a thin film.

The process occurs under high vacuum conditions to prevent interference from gas molecules. The vacuum chamber is typically designed to provide line-of-sight access between the target and the substrate, allowing the vaporized atoms to coat the desired areas. The resulting film is generally uniform and adheres well to the substrate.

The above-mentioned technique offers advantages like precise control over film composition, high deposition rates, and the ability to deposit materials with high melting points.

It is worth noting that E-Beam PVD is just one of several PVD techniques available, each with its own advantages and applications. Other PVD methods include sputtering, evaporation, and ion plating.

The process of preparation and cleaning of the corning glass [69] is similar on both the devices with the active layer of ZTO and the MoO_3 device, as the bottom layer is the same in the two device types, which is composed of Ti and Pt.

The cleaning process consists of laying all the corning glass substrates (area of $2.5 \times 2.5 cm^2$) in an ultrasonic bath at $60°C$ in acetone for 10 min, followed by a similar treatment in Isopropyl Alcohol (IPA). Subsequently, the substrates undergo cleaning with deionized water (H_2O) and then are dry by placing them on a hotplate at $110°C$ for 10 min.

After the cleaning procedure, glass substrates are used as the substrate for manufacturing the bottom electrode and coated with 30 nm-thick layer of Ti and 45 nm-thick of Pt through e-beam evaporation [42], as seen in 3.3. To prepare the substrates for film deposition, they underwent a 30-min Ultraviolet (UV)/Ozone surface activation process with a lamp placed at a distance of 8 cm and at room temperature, using a PSD-UV Novascan system.

This procedure makes the upcoming deposition method easier, namely the thin-film spin-coating technique that is used to deposit the ZTO and the MoO_3 solutions in the desired substrates.

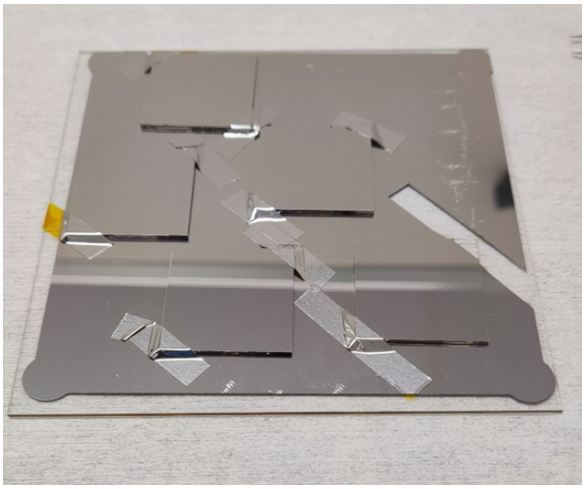


Figure 3.3: Bottom electrode deposition by e-beam.

The previously mentioned spin-coating technique is widely used in thin film fabrication. It involves the application of a liquid precursor or solution onto a substrate, which is then rapidly rotated to spread the liquid into a thin and uniform film. The centrifugal force generated by the spinning motion helps in achieving a uniform film thickness and morphology. This technique is commonly used in the fabrication of electronic devices, including memristors.

In the context of this work, spin-coating is being proposed as a deposition technique for the fabrication of sustainable printed memristors using metal oxides, in the first place. By using a relatively inexpensive and versatile deposition technique like spin-coating, it may be possible to produce memristors on unconventional substrates for Internet of Things (IoT) applications and wearables, and reduce the associated costs and carbon footprint. However, further research and development are needed to optimize the spin-coating technique for memristor fabrication and to ensure that the resulting devices meet the requirements for artificial synapses.

One of the main advantages of spin-coating is its simplicity and versatility. The technique can be used to deposit a wide range of materials, including metal oxides such as ZTO and MoO_3, which are being investigated for memristor and diode fabrication. Spin-coating also allows for precise control over the thickness and uniformity of the deposited film, which is important for the performance and reliability of electronic devices. Additionally, spin-coating is relatively inexpensive compared to other deposition techniques, such as PVD, which has been used in the past to fabricate bipolar memristors based on MoO_3 solution and diodes based on ZTO solution.

The spin-coating process typically involves the following steps.

- **1. Substrate preparation** - The substrate on which the thin film will be deposited is thoroughly cleaned to remove any impurities or contaminants. It is important to ensure a clean and smooth substrate surface to achieve a high-quality film. This is ensured by exposure to UV radiation to achieve better adherence at the time of deposition. In this case, a PSD-UV Novascan system was used, as previously said, at room temperature for 30 min.
- **2. Deposition** - A small amount of the solution is dispensed onto the center of the substrate, which is then rapidly spun using a spin coater or spin coater system. As the substrate spins, the centrifugal force spreads the solution outward, forming a thin film that coats the entire substrate surface. The spinning speed and duration are critical parameters that determine the film's thickness and uniformity.
- **3. Solvent evaporation** - After the deposition, the spinning is continued for a certain period of time to allow the solvent to evaporate. The evaporation process should be controlled to avoid defects such as cracks or pinholes in the film. Elevated temperature or controlled ambient conditions may be employed to accelerate the drying process, depending on the specific materials used.
- **4. Film annealing** - Finally, the film is subjected to a post-annealing process to enhance its crystallinity or remove any residual solvents. This step can be performed by heating the substrate to a specific temperature for a predetermined time. For this process, a simple heating plate was used.

The spin-coating technique process is repeated until all layers are deposited with the difference that a UV treatment between layers is not done.

Spin-coating offers several advantages as a deposition technique. It is relatively simple, cost-effective, and allows for rapid deposition of uniform thin films over large areas. It is widely used in various applications, including semiconductor devices, photovoltaics, organic electronics, and optical coatings. However, spin-coating is limited to producing thin films with thicknesses in the range of tens of nanometers to a few micrometers.

Continuing with the fabrication procedure, but even before applying the spin coating deposition, Kapton tape was used to mask one side of the substrates. This was done to facilitate access to the bottom electrode during electrical characterization.

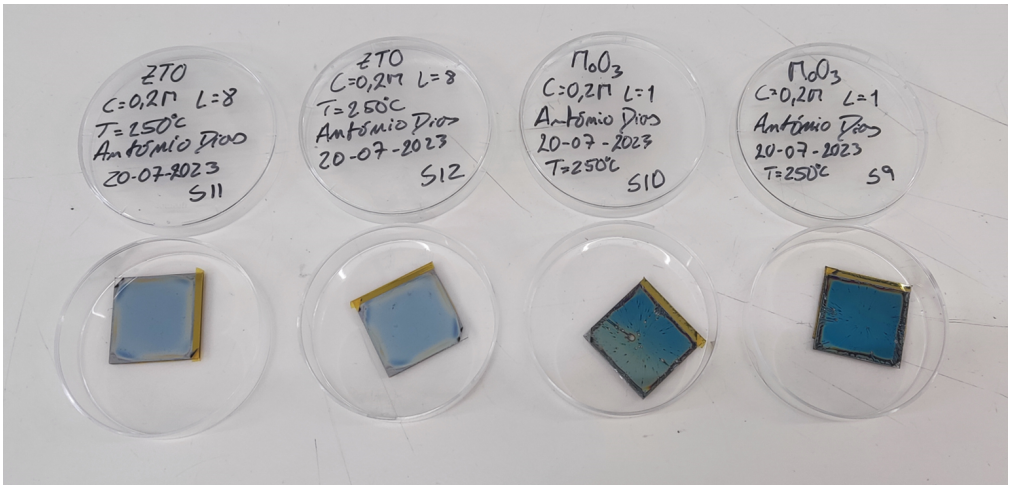


Figure 3.4: MoO_3 and ZTO samples after spin-coating deposition.

3.2.1 Molybdenum Trioxide Thin Film Deposition and Devices Fabrication

In the MoO_3 spin-coating deposition, there were two solutions to be tested, depending on the molar concentration of the previously made solution, as well as the number of layers deposited in the Ti/Pt or Ag substrates, as said in 3.1.1.

In the solution preparation phase, two different concentration solutions were made, one of 0.1 M and one of 0.2 M, to be tested and to be able to use the most precise and efficient concentration for the work proposed. With the help of a 0.2 µm hydrophilic filter, which was used to filter the MoO_3 precursor solutions made in 3.1.1, the solution was deposited by spin-coating technique on the bottom substrate. For this phase, 1 or 2 layers were deposited, depending on the molar

concentration of the precursor solution. In particular, it was deposited 1 layer of solution with a molar concentration of 0.2 M, and 2 layers with the remaining solution with a molar concentration of 0.1 M.

During the spin-coating process, the solution layers were spread at the same time as the substrate spun at a speed of 3000 rpm with an acceleration of 2000 rpm/s, producing a thin film of MoO_3 on the desired substrate, with the help of the spin coater of Laurell Technologies. Immediately afterwards, the substrate is annealed on a hotplate at 250°C for 5 min. To continue with the solution deposition and prepare the next layer deposition, the substrate underwent a 15-min UV treatment at room temperature to enhance the bonding of the following layers. This process is repeated until all layers are spread in the substrate that acts as a bottom electrode. To finalize the deposition of the solution, the substrate is heated for 1 hour on a hotplate, at the same temperature as before, 250°C.

The device fabrication is finished with a deposition of a top contact, this 200 nm-thick Ag or 6 nm-thick Ti/ 60 nm-thick Au electrode is deposited with the same technique previously used in the bottom contact, the Electron Beam Evaporation (e-beam). This deposition was made using a shadow mask and with this technique the top contact patterns forms a 6×6 grid, yielding a total of 36 operational devices within each sample 3.5 with a diameter of 0.5 mm for each device.

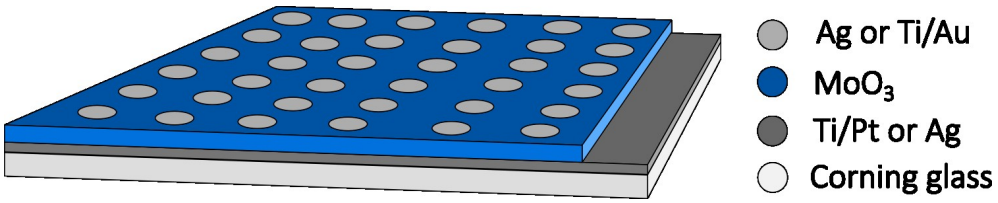


Figure 3.5: Representation of MoO_3 sample with 36 devices.

Samples were made of 0.1 M with 2 active layers and samples of 0.2 M with 1 layer, both of them with an annealing temperature of 250°C, with a structure of Corning glass/$Ti/Pt/MoO_3/Ag$, Corning glass/$Ti/Pt/MoO_3/Ti/Au$ or Corning glass/Ag/ $MoO_3/Ti/Au$.

3.2.2 Zinc Tin Oxide Thin Film Deposition and Devices Fabrication

In the ZTO spin-coating deposition, other two solutions were made to be tested, but in this case, depending on the annealing temperature between layers

of the solution deposition previously explained, in this case with the same molar concentration of ZTO solution. This deposition was made on the same substrate as before, the Ti/Pt or Ag substrate.

The molar concentration used in this deposition was 0.2 M as said and explained in 3.1.2. With the help of a 0.2 µm hydrophilic filter, which was used to filter the ZTO precursor solution, the solution was deposited by spin-coating technique on the bottom substrate, with the help of vacuum. For this phase, 8 layers were deposited.

During the spin-coating process, the solution layers were spread at the same time as the substrate spun at a speed of 2000 rpm with an acceleration of 1500 rpm/s, producing a thin film of ZTO on the desired substrate, with the help of the spin coater of Laurell Technologies. Immediately afterwards, the substrates are annealed on a hotplate at 250°C or at 300°C for 5 min. To continue with the solution deposition and to prepare the next layer deposition the substrate underwent a 5-min UV treatment at room temperature in order to enhance the bonding of the following layers. This process is repeated until all layers are spread in the substrate that acts as a bottom electrode. To finalize the deposition of the solution, the substrate is heated for 1 hour in a hotplate, at the same temperatures as before, 250°C or 300°C.

The device fabrication is completed with a deposition of a top contact, this Ag or Ti/Au electrode is deposited with the same technique previously used in the bottom contact, the Electron Beam Evaporation (e-beam). This deposition was made using a shadow mask and with this technique the top contact patterns form a 6×6 grid, yielding a total of 36 operational devices within each sample 3.6.

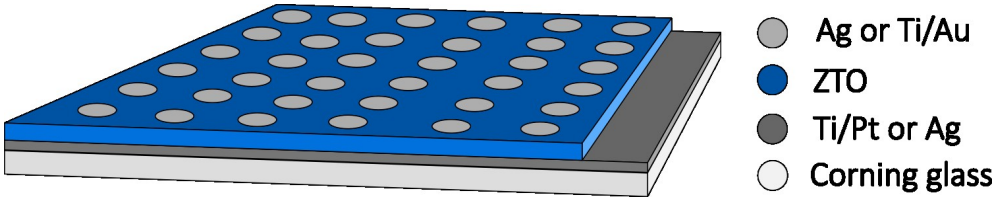


Figure 3.6: Representation of ZTO sample with 36 devices.

Samples were made of 0.2 M with 8 active layers, one with an annealing temperature of 250°C between layers and for the final annealing, the other with an annealing temperature of 300°C, with a structure of Corning glass/Ti/Pt/ZTO/Ag, Corning glass/Ti/Pt/ZTO/Ti/Au or Corning glass/Ag/ZTO/Ti/Au.

The final result, after the deposition of Ag, is shown below in 3.7.

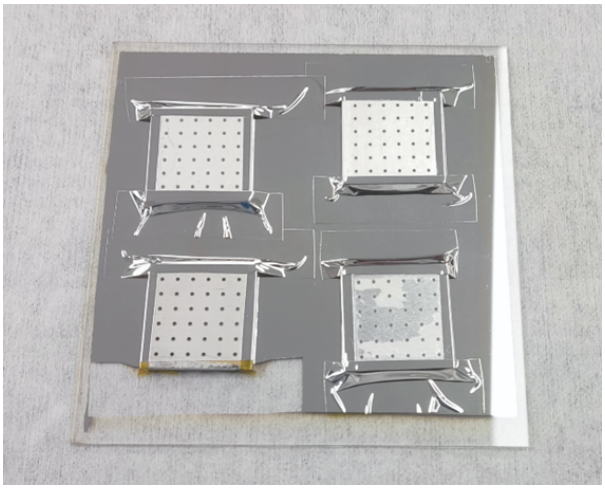


Figure 3.7: Samples after final e-beam deposition.

All the devices' structures and their manufacture characteristics are resumed in table II.1 on annex II.

3.3 Molybdenum Trioxide and Zinc Tin Oxide Devices Characterizations

After device fabrication, it was performed an electrical characterization of the previously made samples, of both MoO_3 and ZTO devices. In this process, the Keithley 4200 SCS semiconductor parameter analyzer is connected to a Janis ST-500 microprobe station in order to measure the current-voltage (I-V) characteristics of the samples.

In order to better visualize the test setup, the image 3.8 shows the main components used in the tests carried out, which:

- **1** - Janis ST-500 microprobe station.
- **2** - Tip connected to the top electrode.
- **3** - Camera with zoom, focus, and light.
- **4** - Tip connected to the grounded bottom electrode.
- **5** - Light switcher and intensity controller.
- **6** - Camera display screen.
- **7** - Cryogenic controller (Lakeshore 336 Temperature Controller).
- **8** - Keithley 4200 SCS semiconductor parameter analyzer.

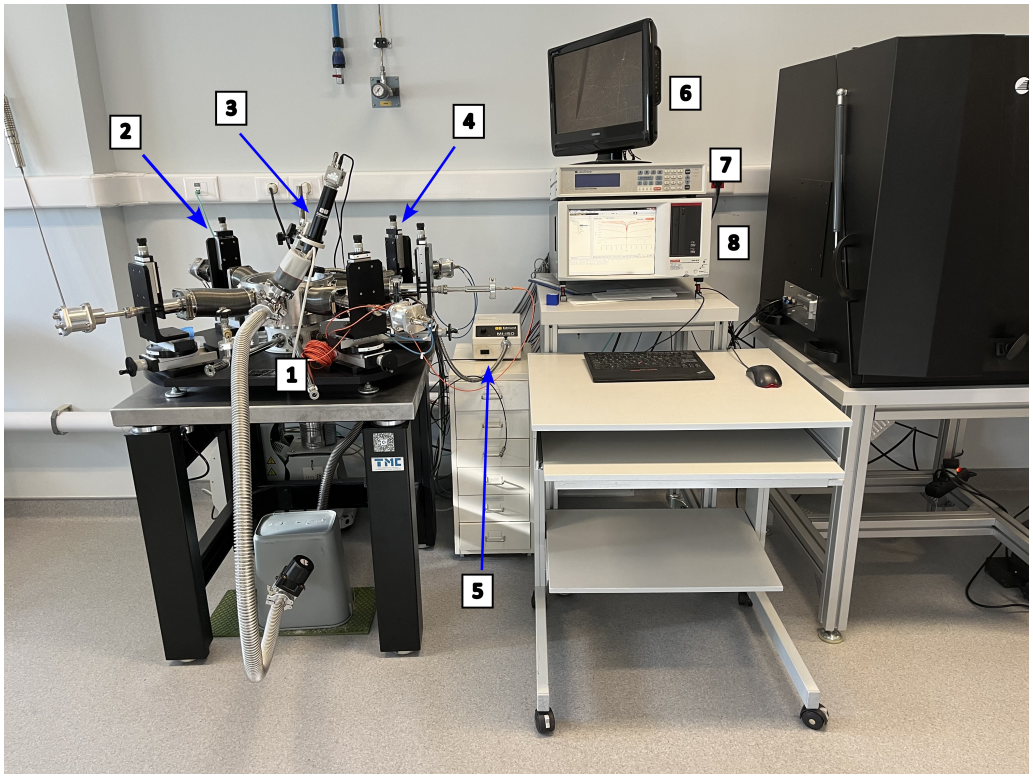


Figure 3.8: Test setup for I-V characterization and for temperature analysis.

Firstly, the MoO_3 and ZTO samples were placed in the probe station and analyzed at room temperature. The top electrode received an applied voltage while the bottom electrode remained grounded, as shown in 3.9. Through the Keithley software, it was possible to visualize the I-V curve, do cycle tests to study the endurance, and retention tests to characterize the MoO_3 bipolar memristors regarding its time of preserving its last state.

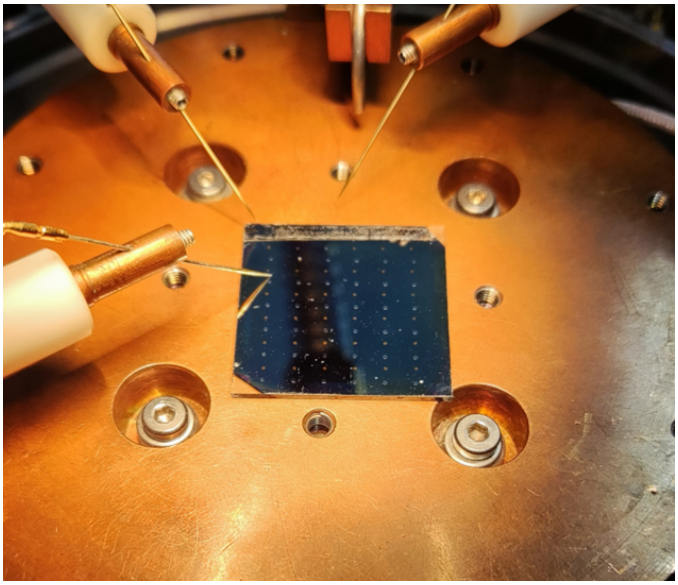


Figure 3.9: Sample in probestation.

At a later stage, a temperature variation analysis was made for the ZTO-based diodes. At a vacuum ambient, these samples were cooled with the help of nitrogen (N_2) at a minimum temperature of 150 K and, then, heated to a maximum temperature of 355 K, being the temperature controlled by a Cryogenic controller (Lakeshore 336 Temperature Controller), the setup for this test is presented in figure 3.10.

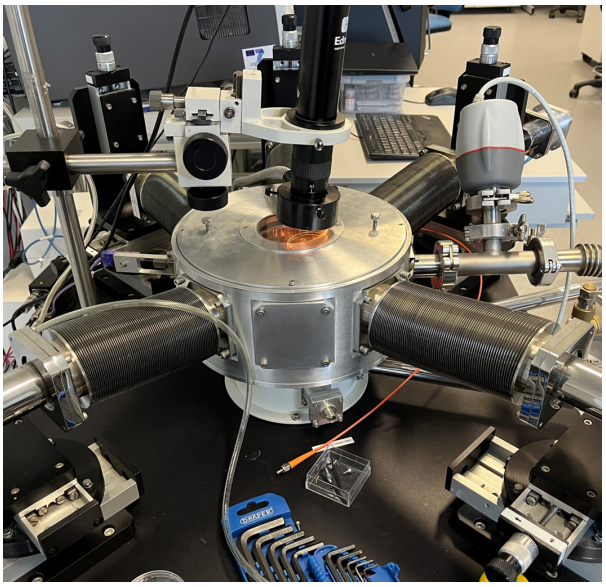


Figure 3.10: Probestation for temperature analysis.

4

Results and Discussion

This chapter provides an in-depth examination of the findings related to the analysis of solutions and thin films, as well as the evaluation of the electrical properties of the manufactured MoO_3-based bipolar memristors and Zinc Tin Oxide (ZTO)-based diodes.

The primary objective of this research was to enhance the performance of the active layer in solution-based MoO_3 thin films and explore their potential uses in bipolar memristors and the active layer in solution-based ZTO thin films to explore their Schottky Diode potential. An essential component of this investigation involved conducting electrical assessments, specifically by measuring the current-voltage (I-V) characteristics of each device. This analysis provided valuable insights into the electrical properties, behavior, and potential applications of these devices.

Later a temperature analysis was tested in the ZTO-based case, where it was possible to study the behavior of these devices based on the variation of temperature, in a vacuum environment.

4.1 Molybdenum Trioxide Memristors Electrical Characterization

Based on this MoO_3, in solution preparation 3.1.1 there were produced two different solutions, differing in molar concentration, one of them with 0.1 M and the other with 0.2 M. Later, these two different concentration solutions were deposit by spin-coating technique into the desired corning glass substrates. In the 0.1 M molar concentration case were deposited two layers of the MoO_3 solution, and in the 0.2 M solution case only one layer of the mentioned solution was deposited.

These two different proportion solutions made it possible to study the best and most efficient way of bipolar memristor production. Besides the active layer solution variation, the bottom and top electrodes were changed to enable the best performance for these memristors.

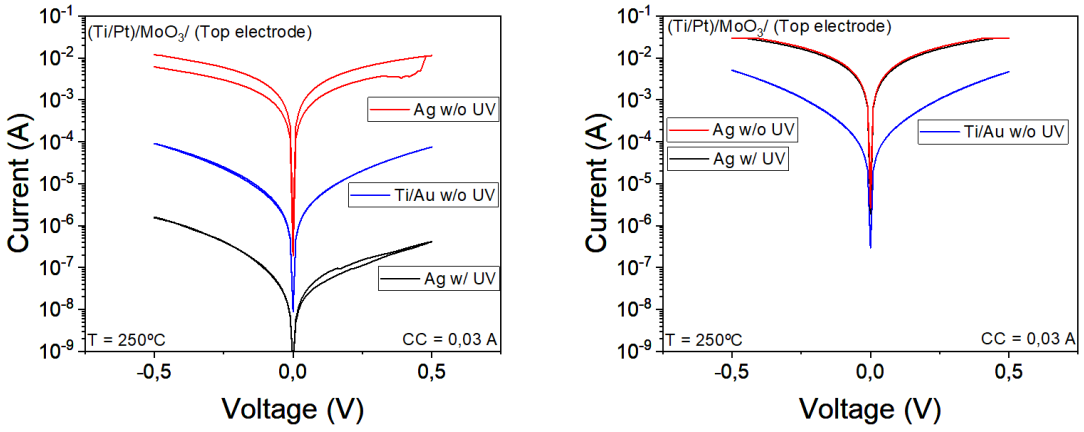
Different configurations with this MoO_3 active layer were tested, namely, $(Ti/Pt)/\ MoO_3/(Ti/Au)$, $(Ti/Pt)/MoO_3/Ag$, and $Ag/MoO_3/(Ti/Au)$, all these with a bottom electrode/active layer/top electrode structure.

All the above-mentioned devices were characterized and tested to see the different behaviors.

4.1.1 Direct Current (DC) sweep measurements

In a first stage, a pristine test was made for all devices, which became the first I-V curve to be seen in the majority of the tested devices. With this curve, we find out if the device is electrical insulating, conducting, or simply in short-circuit. For this test, a voltage was systematically varied from -0.5 V to 0.5 V while maintaining a Current Compliance (CC) for most cases at 0.03 A. The use of CC limit is essential to safeguard against any abrupt and severe device failures.

The 4.1 shows an example of the pristine state of the devices fabricated based on the active layer with MoO_3.



(a) C=0.2M / Nº layers=1 (b) C=0.1M / Nº layers=2

Figure 4.1: Pristine state of MoO_3 memristors, differentiated by molar concentration, number of layers, and top electrodes. (a) Molar concentration = 0.2 M; Number of layers = 1. (b) Molar concentration = 0.1 M; Number of layers = 2.

Right from the pristine graphs is possible to see, and as expected, a higher conductivity in 4.1b, when a lower molar concentration of MoO_3 is used in all the different top electrodes, even with different numbers of active layers deposition.

For this reason and for memristor purposes, the molar concentration and the number of layers tested and graphically represented in 4.1a appear to be promising, due to the lower conductivity and behavior presented firstly in the Ti/Au top electrode case.

This sample was subject to some other tests, namely electroforming. Later cycle tests were made to characterize the endurance of the devices and finished with a retention test that characterizes the reliability of the produced devices.

Being 4.1 graphs an example of a device from various samples, pristine state maps of these samples were made to see the behavior of all devices MoO_3 active layer based, these maps are in annex III more specifically in III.2, III.3, III.6. The described procedure made possible an overview of the devices that had some resistive behavior and others already in short-circuit.

As previously said, an electroforming step 4.2 was made to form a conductive filament that stimulates a resistive switch in the device, which characterizes the behavior of a typical memristor. This procedure occurs in the same environmental conditions as the pristine state test.

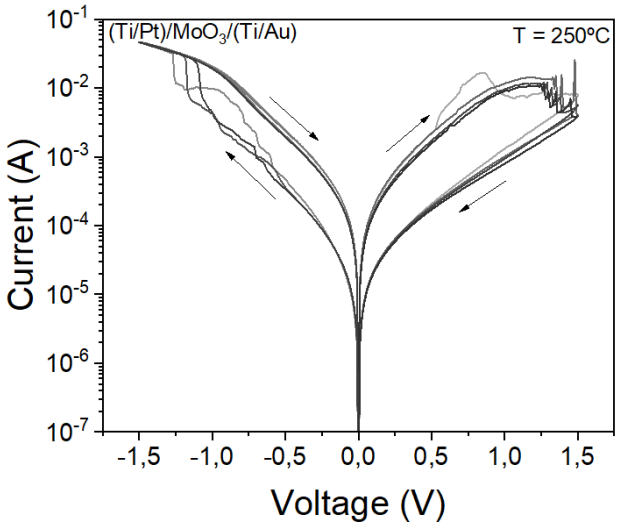
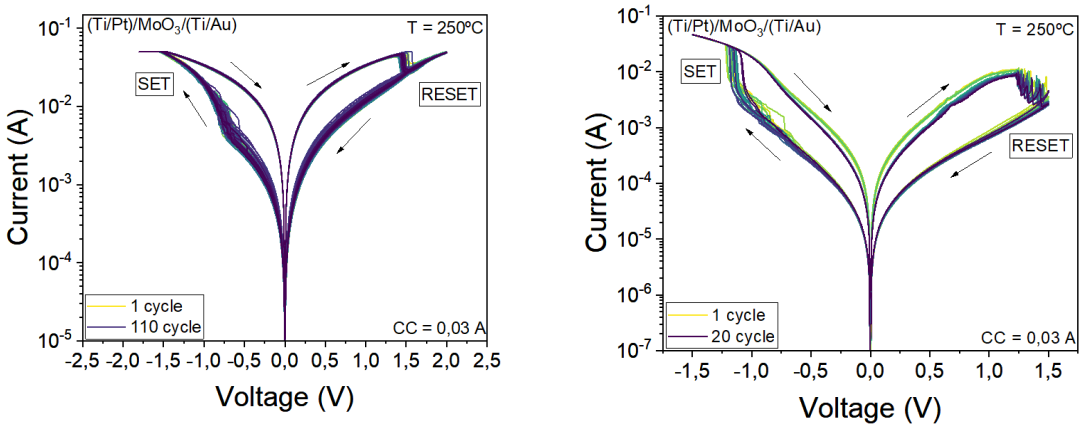


Figure 4.2: I-V characteristics of electroforming example of $(Ti/Pt)/MoO_3/(Ti/Au)$ 1-layer device with Molar Concentration = 0.2 M.

In this graphical representation of MoO_3-based memristor, the electroforming curves make it possible to see that a switching behavior occurs while applying a certain voltage in either positive or negative polarity. More specifically, the 1-layer device with an annealing temperature of 250°C and a molar concentration of 0.2 M, appears to be switched ON (form a conductive filament) by applying a negative voltage of 1 V and switched OFF at a positive voltage of 1.5 V.

Following the electroforming process, the Resistive Switching (RS) characteristics were examined through endurance tests, graphically represented in 4.3. The current-voltage (I-V) curves were generated by performing successive Direct Current (DC) sweeps while maintaining a constant CC. In all test conditions, the memristors exhibited bipolar RS behavior, manifesting as a rapid transition to the set state when subjected to negative polarity and a more gradual reset when exposed to positive bias.



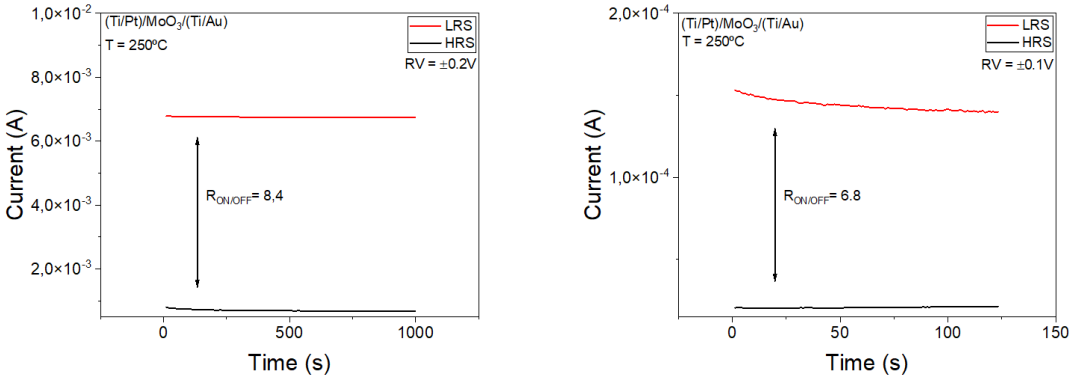
(a) (b)

Figure 4.3: I-V characteristics of endurance test of $(Ti/Pt)/MoO_3/(Ti/Au)$ 1-layer device with Molar Concentration = 0.2 M. (a) 110 cycle switching state test. (b) 20 cycle switching state test.

This particular device is an example of the majority of tested samples. They present, as expected from the electroforming phase (4.2), a RS behavior that switches ON and OFF while applying a certain voltage, this occurs with stability and shows, in the majority of cases, reliability.

To assess the stability of the devices, retention tests were conducted, as depicted in 4.4. The test was carried out in ambient air conditions for a duration of 125 s, with a Read Voltage (RV) maintained at ±0.1 V for the 4.4b device and 10^3 s with a RV maintained at ±0.2 V for the 4.4a device. The outcomes reveal robust stability in both the Low Resistance State (LRS) and High Resistance State (HRS) with residual deterioration over time mainly in the 4.4b and an almost perfect data retention in 4.4a. This suggests that the fabricated devices can be classified as non-volatile memories.

This retention test also shows a lower $R_{ON/OFF}$ of 6.8 for 4.4b device and a higher $R_{ON/OFF}$ of 8.4 for 4.4a device. Besides these devices' stability and non-volatility, the $R_{ON/OFF}$ are much lower than other devices from the lecture, for



(a) (b)

Figure 4.4: Retention test of $(Ti/Pt)/MoO_3/(Ti/Au)$ 1-layer device with Molar Concentration = 0.2 M. (a) related to the device of figure 4.3a. (b) related to the device of figure 4.3b.

example on the Indium Gallium Zinc Oxide (IGZO)-based memristors [70]. A way of improving this ratio in these memristive devices would be testing other layouts by changing the number of semiconductor's layers and/or testing other materials to the electrodes layers.

4.2 Molybdenum Trioxide Memristors Electrical Characterization with Ag top electrode

After tests and characterizations done with $(Ti/Pt)/MoO_3/(Ti/Au)$-based bipolar memristors, it was tested a possible and promising $(Ti/Pt)/MoO_3/Ag$ structure approach. This approach comes regarding the more sustainability of Ag and the possibility and ease of printing Ag rather than (Ti/Au).

For the presented reason, the Ag top electrode device with MoO_3 solution was studied and characterized, due to its promising manufacturing process.

4.2.1 Direct Current (DC) sweep measurements

Keeping in line with the previously tested devices, the pristine test was made to allow an overall view of the behavior of all devices from the manufactured samples, and this was done by applying the same -0.5 V to 0.5 V voltage values, as seen in 4.1. The molar concentration and number of layers deposited were chosen in the same line of thought as previously explained in 4.1.1. With that, the device chosen to proceed with the remaining tests and characterizations was the one with

the higher molar concentration and with one layer of MoO_3 solution as the active layer.

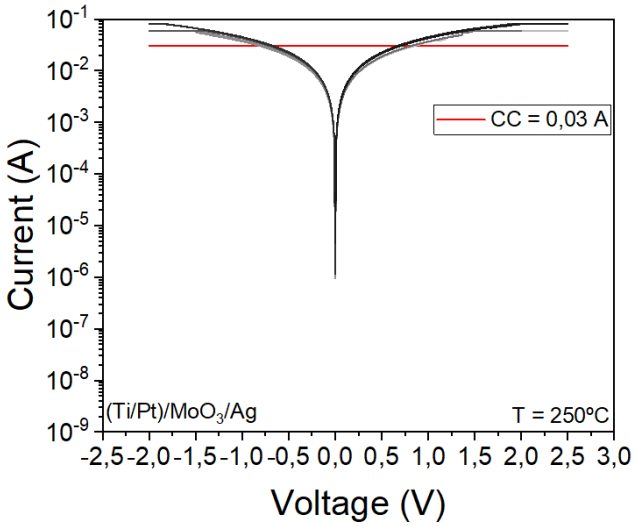


Figure 4.5: Electroforming example of $(Ti/Pt)/MoO_3/Ag$ one active layer device with a molar concentration of 0.2 M and 30-min UV final treatment.

In the same way, and with a 30 min-UV exposure with the help of PSD-UV Novascan system, mainly in 4.1a, it is possible to see a reduction of conductivity with the Ag oxidation, which leads to a decrease of V_o and a higher resistance [71]. In a memristor, achieving insulating characteristics is crucial, while simultaneously ensuring a sufficient V_o is present to allow current flow and enable alteration of its resistance state upon the application of a certain voltage.

For this reason and for memristor purposes, the molar concentration and the number of layers tested and graphically represented in 4.1a appears to be promising, due to the conductivity and behavior presented in the Ag top electrode with UV treatment case. This sample was subject to some other tests, namely electroforming, and later cycle tests to characterize the endurance of the devices.

As previously said, an electroforming step was made to form a conductive filament that leads to stimulating a resistive switch in the device which characterizes the behavior of a memristor. This procedure occurs in the same environmental conditions as the pristine state test represented in 4.1.

As seen in the 4.5 graph, the electroforming was made and it is possible to see that this particular device, which is a sample of an overall view of all Ag top electrode memristor sample's devices, is in short-circuit. This helps to conclude a high conductivity and a lack of resistive behavior that characterizes a common

memristor. For this reason and with this structure it is possible to affirm the inability to continue further tests.

4.3 Zinc Tin Oxide Diodes Electrical Characterization

Based on this ZTO solution, prepared before and described in 3.1.2 there were produced two different devices, differing in annealing temperature between each layer deposition, one of them with 250°C and the other with 300°C. As said in 3.2.2, this procedure was made with the spin-coating technique that was used to deposit all layers into the desired corning glass substrates. 8 layers of ZTO solution were deposited in both procedures with different annealing temperatures in either case.

These two different methods made it possible to study the best and most efficient way of this Schottky diode production. Besides different annealing temperatures, there were tested various configurations with this ZTO active layer, namely, (Ti/Pt)/ZTO/(Ti/Au), (Ti/Pt)/ZTO/Ag, and Ag/ZTO/(Ti/Au), all these configurations with a bottom electrode/active layer/top electrode structure.

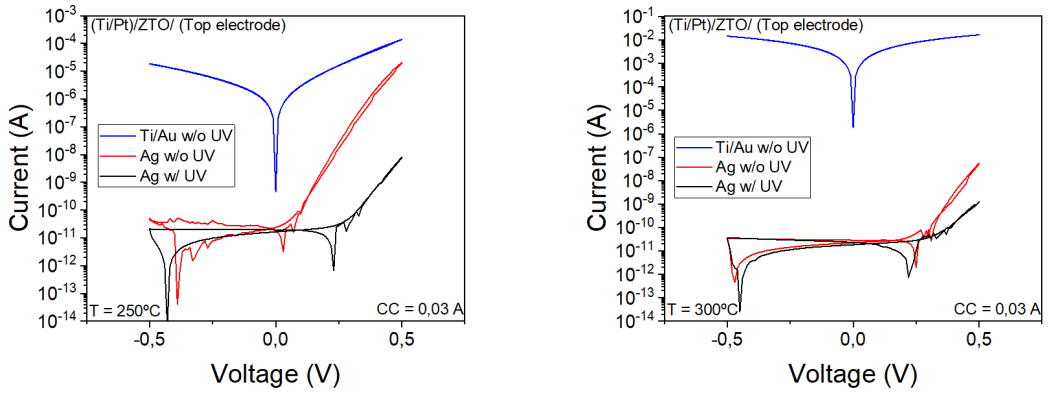
All these devices were studied and characterized to see their different behaviors and it was possible to conclude that (Ti/Pt)/ZTO/Ag was the promising device, due to the rectification ratio and behavior between the reverse polarity and the forward polarity.

4.3.1 Direct Current (DC) sweep measurements

In a first stage, and taking the same approach as before in the MoO_3-based devices, a low-voltage primary test was made for all devices, which became the first I-V curve to be seen in the majority of the tested diodes. With this curve, we find out if the device is electrical insulating, conducting, or simply in short-circuit. For this test, a voltage was systematically varied from -0.5 V to 0.5 V while maintaining a CC for most cases at 0.03 A. The use of CC limit, like in previous device tests, is essential to safeguard against any abrupt and severe device failures.

The 4.6 shows an example of the low-voltage primary test of the devices fabricated based on the active layer with ZTO.

Right from the primary test graphs is possible to see a higher conductivity and rectification in 4.6a when a lower annealing temperature is used in between the spin-coating active layer deposition using ZTO solution. This is a reality because the primary tests show that in the 4.6b, more specifically in the



(a) Annealing temperature of 250°C. (b) Annealing temperature of 300°C.

Figure 4.6: Pristine state of ZTO diodes, differentiated by annealing temperature, and top electrodes.

(Ti/Pt)/ZTO/(Ti/Au) case, all devices were in short-circuit, and consequently unusable.

For this reason and for diodes purposes, the annealing temperature tested and graphically represented in 4.6a appears to be promising, due to the conductivity, rectification, and behavior presented firstly in the Ag top electrode without the 30-min UV treatment case. Therefore, this sample was subject to some other tests in order to characterize the device. Later cycle tests were made to characterize the endurance and finished with a temperature analysis test that characterized the endurance and behavior of the manufactured devices by varying the ambient temperature in vacuum.

Being 4.6 graphs an example of a device from various samples, primary test maps of these samples were made to see the behavior of all devices ZTO active layer based, being presented in annex III more specifically in III.4, III.5, III.7. This procedure made possible an overview of the devices that had some diode behavior and others already in short-circuit.

As previously said and in the same way as before using MoO_3-based devices, a characterization step 4.7 was made to form a conductive filament that stimulates the diode behavior from a certain applied voltage. This procedure occurs in the same environmental conditions as the primary tests.

In this graphical representation of ZTO-based diode, the I-V characteristic curve makes it possible to see that the device starts its behavior highly resistive at a negative polarity and, for a certain positive voltage, becomes highly conductive, describing a diode normal behavior. More specifically, the 8-layer device with the annealing temperature of 250°C and a molar concentration of 0.2 M appears to

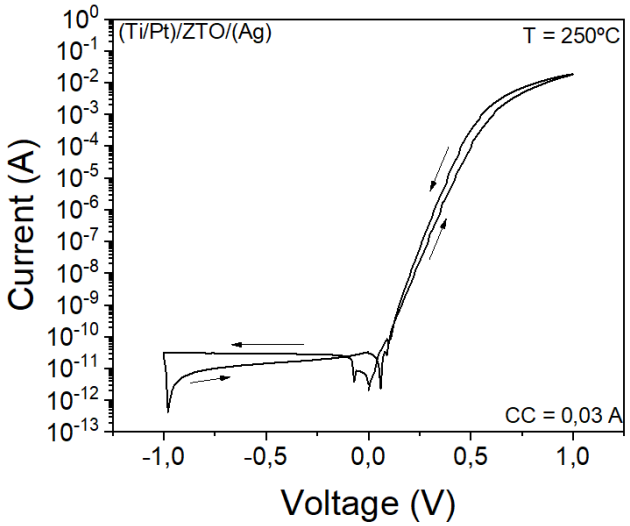


Figure 4.7: I-V characteristics example of (Ti/Pt)/ZTO/Ag 8-layer device with Molar Concentration = 0.2 M; annealing temperature of 250°C.

became highly conductive by applying a positive voltage of 0.1 V.

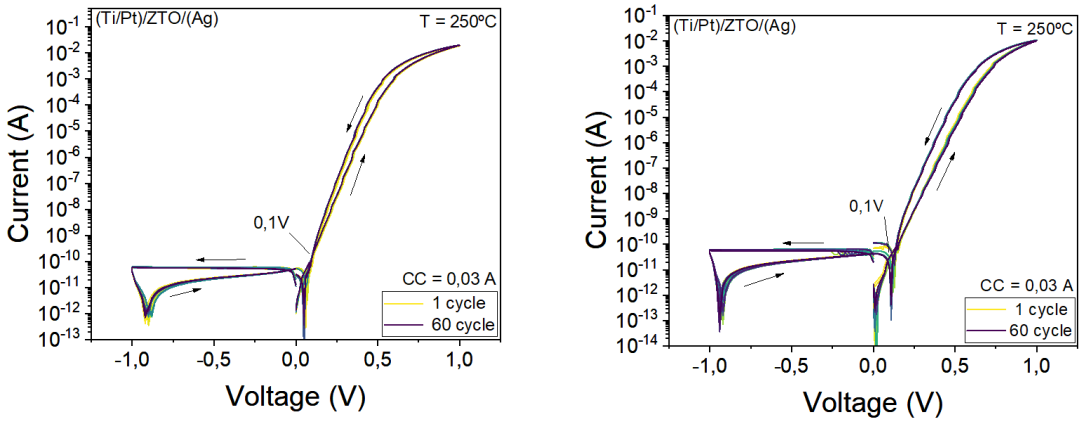
Following the characterization process, the endurance of the forward/reverse polarity cycle was tested in the same way as the previous ON/OFF switching state in memristor devices, these tests are graphically represented in 4.8.

The current-voltage (I-V) curves were generated by performing successive DC sweeps while maintaining a constant CC. In all test conditions, the diodes exhibited a high rectification ratio between the reverse and forward polarities, more specifically, and possible to see in 4.8a, a stable reverse polarity current at 3×10^{-11} A, and rapid transition to forward polarity at a voltage of 0.1 V with a maximum current at 2×10^{-2} A at 1 V. This made possible a rectification ratio of $\approx 10^9$.

The particular devices shown in 4.8 are an example of the majority of tested samples. They present, as expected from the characterization phase (4.7), a forward/reverse polarity switch behavior that occurs when applying a certain voltage, in this case 0.1 V, with stability.

4.3.2 Temperature Analysis

In the concluding phase of this ZTO-based Schottky diode characterization, it was conducted a temperature analysis to understand and investigate how the charge conduction properties of the manufactured diodes behaved. To conduct



(a) (b)

Figure 4.8: I-V characteristics of endurance test of (Ti/Pt)/ZTO/Ag 8-layer device with Molar Concentration = 0.2 M and a annealing temperature of 250°C.

this test, we utilized the optimal device configuration 4.8a, consisting of an 8-layer device annealed at 250°C with a molar concentration of 0.2 M and with a rectification ratio up to $\approx 10^9$ in ambient conditions. The measurements were carried out in a vacuum environment with the help of Keithley 4200 SCS connected to a Janis ST-500 microprobe station and with the temperature controlled by a Cryogenic controller (Lakeshore 336 Temperature Controller).

A dual DC sweep was made by varying the ambient temperature. The temperature range explored during this analysis ranged from a minimum temperature of 150 K and, then, heated to a maximum temperature of 355 K.

To compare the different behaviors according to temperature variation, a graphical representation of the dual DC sweep between -1 V to 1 V is presented in appendix A in figure A.1.

The graphical representation A.1 shows some loss of rectification ratio due to the increase of leakage current on the reverse polarity. Besides this leakage current increase, the conductivity of the forward polarity increases with the temperature, revealing a low and almost no rectification ratio at the lower temperature of 150 K. The mentioned rectification ratio of the device increases with the temperature as the leakage current decreases and the positive polarity current increases. Additionally, it is possible to see, in higher temperatures, a series resistance, R_s which describes the final behavior in the conductive part of the device, approximately from 0.7 V to 1 V at the highest temperatures tested.

To conclude with the A.1 graph analysis, the variation of temperature in a vacuum environment shows a significant variation in the conducting phase of the

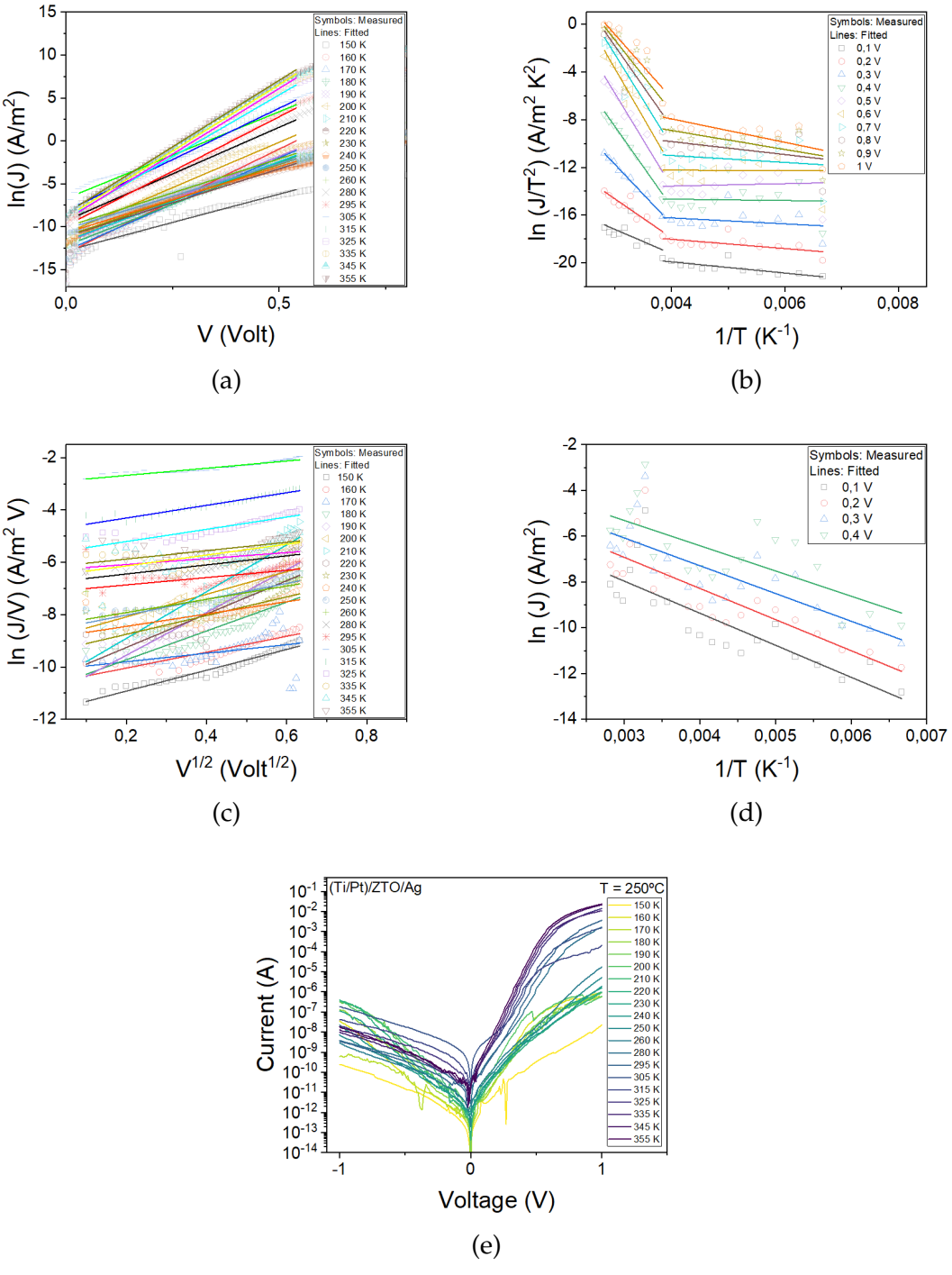


Figure 4.9: Conduction mechanism of the ZTO diode device. (a) Voltage dependency based on the Schottky emission process at positive voltage. (b) Temperature dependency based on the Schottky emission process at positive voltage. (c) Voltage dependency based on the Poole-Frenkel emission process at negative voltage. (d) Temperature dependency based on the Poole-Frenkel emission process at negative voltage. (e) Diode's measured I–V characteristics by varying temperature.

ZTO-based Schottky diode as well as in the higher resistive state, concluding in a sharp variation of rectification ratio, when comparing with normal conditions environment seen in 4.8a.

Based on the figure A.1, in appendix A and to explore the functionality of the diode-based device in the forward direction, it was examined the temperature and voltage dependence behavior of the I-V characteristics for both the conducting forward polarity and the higher resistive state, this last with the leakage current associated. The two previously mentioned conductive states are represented with a single DC sweep in 4.9e, where, in the positive voltage side a dominant factor in conduction is thermionic/Schottky emission. This indicates that the primary factor restricting conduction is the Schottky-like barrier at the ZTO-Pt interface. In the context of thermionic emission, the current density, denoted as J is defined in 4.1 in which T is the temperature, ϕ_B is the Schottky barrier height, k_B is the Boltzmann constant, q is the elementary charge, V is the voltage, R_s is the series resistance, i is the current, η is the ideality factor, and A^* is the effective Richardson constant. This last value is defined by the equation 4.2, where m_0 is the free electron mass and m^* is the effective electron mass, which, with this ZTO films is equal to 0.3 free electron masses (m_0).

$$J = A^* \times T^2 exp(-\frac{\phi_B}{k_B T}) \times [exp(q\frac{V - R_S i}{\eta k_B T}) - 1] \tag{4.1}$$

$$A^* = \frac{4\pi q k^2 m^*}{h^3} = \frac{120 m^*}{m_0} \tag{4.2}$$

The curves presented in both 4.9b and 4.9a figures support the fact that thermionic emission is the conduction mechanism in this conductive state of this device, for resembling the characteristics of standard Schottky emission presented in [72] and [73]. Additionally, in the region with a Schottky emission mechanism, there are two linear fittings in temperature dependence graphs, seen in figure 4.9b and in the same way, in voltage dependency, in figure 4.9a. In this last graphical representation, the mentioned aspect occurs only for higher temperatures, farewell due to the presence of R_s (series resistance) which becomes quite pronounced, probably related to the metal contacts, where the higher the temperature, the greater the resistance of the metal layer.

From the equation 4.1 and as seen in 4.10, the temperature dependence of the Schottky barrier is shown as not homogeneous, by assuming a Gaussian distribution presented in 4.3, where ϕ_B^{eff} is the effective barrier height, ϕ_B^m is the mean barrier height and σ_B the standard deviation. The effective barrier height

(ϕ_B^{eff}) is reduced compared to the mean value (ϕ_B^m), allowing charge carriers to preferentially pass through regions with lower barriers.

This barrier height was calculated disregarding the resistance in series (R_s) observed in higher temperatures, in figure 4.9e. With calculations regarding the R_s is possible to characterize the temperature dependence of the ideality factor that is described by the equation in 4.4, where ρ_2 is the linear voltage dependency of ϕ_B^m and ρ_3 is the linear voltage dependency of ${\sigma_B}^2$, as seen in [73, 74].

The table 4.1 summarizes the values obtained with this model.

$$\phi_B^{eff} = \phi_B^m - \frac{\sigma_B^2}{2k_BT} \tag{4.3}$$

$$\eta = \frac{1}{1 - \rho_2 + \frac{\rho_3}{2k_BT}} \tag{4.4}$$

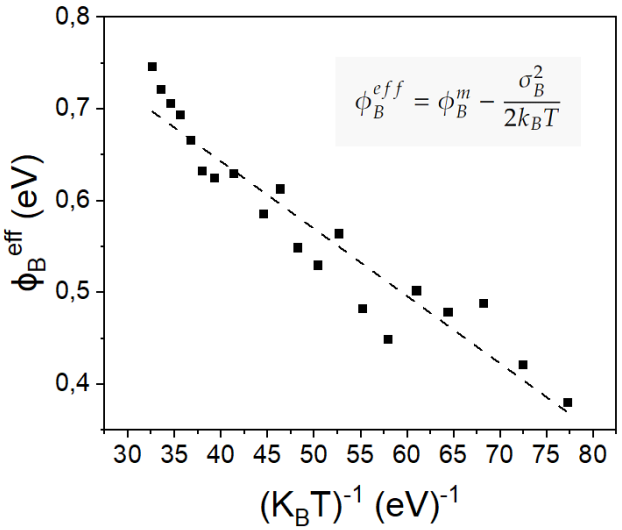


Figure 4.10: Temperature dependence of the effective barrier height.

Table 4.1: Mean Schottky barrier height (ϕ_B^m), standard deviation (σ_B).

ϕ_B^m (eV)	σ_B (eV)
0.937	0.121

The observed current in 4.9e between 0 V and ≈ 0.4 V in the higher resistive state exhibited a significant dependence on temperature. This behavior was found to align with Poole-Frenkel emission, and the curves representing the modeled data are shown as lines in figure 4.9c and figure 4.9d, being the voltage dependency

and the temperature dependency, respectively. These last graphs resemble the characteristics of standard Poole-Frenkel emission presented in [72] and [73], following the equation in 4.5 which, q is the elementary charge, μ is the electron mobility, N_c is the effective density of states for electrons in the conduction band, E is the electric field, ϕ_t is the energy level of the traps, ε_r is the relative permittivity of ZTO, ε_0 is the vacuum permittivity, k_B is the Boltzmann constant and T is the temperature.

$$J = q\mu N_c E \times exp[-q\frac{(\phi_t - \sqrt{\frac{qE}{\pi\varepsilon_r\varepsilon_0}})}{k_B T}] \tag{4.5}$$

It was not possible to find a standard emission characteristic for the remaining range of voltage, from ≈ 0.4 V to 1 V, where the leakage current increases.

To have a different and more complete view of the behavior of these devices according to temperature variation in a vacuum environment, the graph 4.11 shows the variation of maximum current in the conducting state (forward polarity) depending on temperature increase, and the correspondent minimum of leakage current on the higher resistive state (reverse polarity).

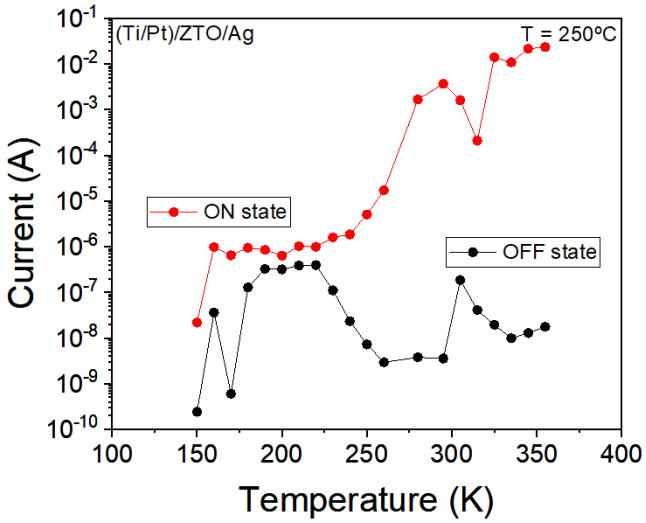


Figure 4.11: Rectification ratio by varying ambient temperature while in vacuum.

According to the graph presented in 4.11 it is possible to see that with low temperatures, more specifically between 150 K and 230 K, there was almost no rectification, and therefore there was no diode behavior. After increasing the temperature to higher values (approaching ambient temperature), the rectification ratio becomes more expressive, namely after 230 K, as expected, the conductivity

increases with the temperature in the conductive state of the tested ZTO-based Schottky diode. The tendency is to continue increasing the conductivity until the loss of device properties.

After seeing, in a vacuum environment, this drastic diode's conductivity behavior changes with the temperature variation, it was tested the effect of vacuum environment compared with air environment at the same temperature of 295 K, and the graphical representation of this comparison is presented in 4.12. Being this device an example of an entire sample, the sample's pristine map comparison is presented in annex III more precisely in figure III.8.

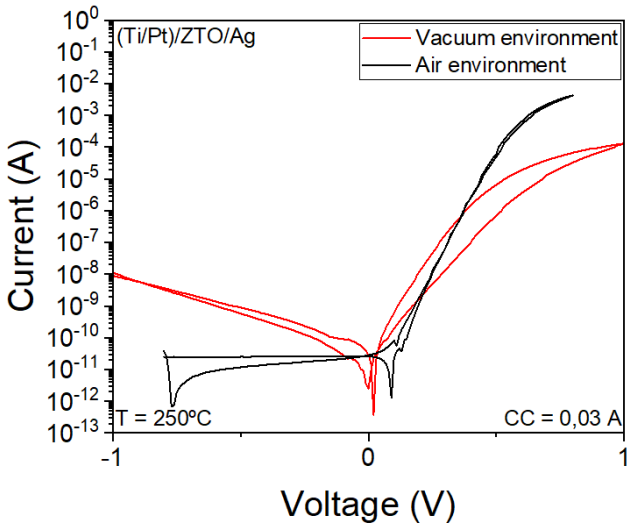


Figure 4.12: Different environment comparison in ZTO-based Schottky diode.

With the two curves' representation regarding the same device, it is possible to conclude a notable change in the diode behavior. On the reverse polarity, the conductivity increases significantly and in the forward polarity the behavior is the opposite, namely, the conductivity decreases. These changes lead to a significant reduction in the rectification ratio and, consequently, a reduction in the diode's properties.

5

Conclusion and Future Perspectives

This study primarily revolved around the creation and examination of solution-based MoO_3 bipolar memristors and solution-based ZTO Schottky diodes. Additionally, it aimed to enhance the performance of the active layer by generating MoO_3 thin films with varying molar concentrations, and number of layers. Likewise, generating ZTO thin films with varying annealing temperatures in the deposition process. The focus was also on the manipulation of the top and bottom metal contacts that were studied for the optimal combination in order to achieve the best performance.

To begin, MoO_3 solutions were prepared with molar concentrations of 0.1 M and 0.2 M using H_2O as a solvent of the solution. With the same approach, the ZTO solution was prepared with a molar concentration of 0.2 M using urea ($CO(NH_2)_2$) as fuel and 2-Methoxyethanol ($CH_3OC_2H_4OH$) as solvent.

Subsequently, memristors and diodes were constructed on a glass substrate. This involved employing e-beam evaporation to apply the electrodes and using spin-coating to layer multiple ZTO and MoO_3 coatings, which were then subjected to annealing each layer and final annealing at 250°C for MoO_3-based memristors and 250°C or 300°C for ZTO-based diodes.

A significant aspect of this research involved electrical characterization, which allowed us to explore the behavior of either memristor or diodes and their potential applications. Initially, our focus was identifying the conditions that yielded the highest number of functional devices by examining pristine maps and overall yield.

The findings indicated that, firstly, in MoO_3-based memristors, increasing the molar concentration to 0.2 M and depositing only 1 layer of solution was beneficial

in all cases, both with the Ag and (Ti/Au) top contact, which subsequently concluded that the (Ti/Au) contact becomes better in all the tested conditions, both in terms of endurance and yield. The other tested samples showed a short-circuit condition that makes it impossible to use for memristor purposes. However, with 30-min UV treatment in Ag top electrode sample, the conductivity showed a decreasing behavior which is promising for further electrical characterization tests.

Subsequent cycling tests demonstrated robust endurance and exhibited a retention capability up to 10^3 s with an $R_{ON/OFF}$ ratio of 10^1. Consequently, it was concluded that the optimal condition for achieving acceptable bipolar memristors was a device comprising 1 layer and annealed at 250°C with a (Ti/Au) top contact.

In ZTO-based diodes, decreasing the annealing temperature to 250°C for the 8 layers ZTO deposition with a molar concentration of 0.2 M, turns out to be the best option for diodes production. It was also concluded that the Ag top electrode had the highest rectification ratio and the best endurance of all structures and tested samples. Cycling tests, likewise in MoO_3-based memristors, demonstrated a rectification ratio up to $\approx 10^9$ with great endurance.

Later, temperature variation test in ZTO-based diodes conclude an accentuated behavior variation upon different temperatures. The leakage current increases with lower ambient temperatures and, consequently, the device loses its diode properties. With the temperature increase this leakage current decreases and the opposite occurs in the forward polarity. Additionally, it was characterized and studied the emission process of either positive or negative polarity, being a thermionic or Schottky emission for positive voltages, and in negative voltages, the main behavior was characterized by the Poole-Frenkel emission process. Finally, it was possible to conclude a variation in the diode behavior when subjected to a vacuum environment, with the lack of air the conductivity increases in the reverse polarity and decreases in the forward polarity.

In conclusion, this study represents a significant stride towards the future of electronics by seamlessly integrating solution-based devices, emerging memory technologies, and neuromorphic applications. It has been demonstrated that solution-based memristors can match the electrical performance of vacuum-fabricated counterparts while causing minimal environmental impact and offering cost advantages. Moreover, this approach opens up the potential for scalability and cost-effective large-scale production through the utilization of printing techniques.

5.1 Future Perspectives

Despite the significant advancements achieved in this study, there are still unresolved questions and uncharted avenues for further exploration. Building upon the findings presented here, several recommendations for future research include:

- **Calculations regarding resistance in series (R_s) for the ideality factor calculations.** Previously, in the thesis, the calculation of the Schottky effective barrier height for the diode-based device was made without considering the R_s in higher temperatures of the forward polarity. By considering the R_s, either the effective barrier height or the ideality factor calculations are possible with more precise values, as noted in the article [73, 74].
- **Enhance the manufacturing procedure by decreasing the annealing duration.** Currently, besides the 30-min UV treatment and a final annealing of 1 hour of all samples, each MoO_3 layer requires 5 min of annealing and an additional 15 min of UV treatment, likewise, each ZTO layer requires 5 min of annealing and an additional 5 min of UV treatment, making the process excessively time-consuming.
- **Create memristors and diodes with a similar structure through inkjet printing.** Utilizing the identical MoO_3 and ZTO solutions to formulate the ink may offer a solution to address the issue of sample uniformity.
- **Lower the processing temperature required for MoO_3 memristors and ZTO diodes by integrating thermal annealing with UV irradiation.** This approach will ensure their suitability for use with affordable and flexible substrates.

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A

I-V curves by temperature variation in vacuum environment

To study the diode behavior in temperature variation from 150 K to 355 K, this graphical representation was made. It is possible to see a dual DC sweep from -1 V to 1 V.

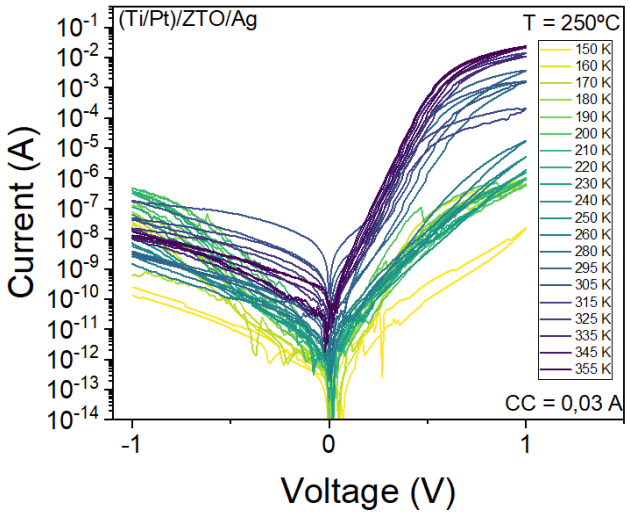

Figure A.1: I-V characteristics by varying the ambient temperature.

APPENDIX A. I-V CURVES BY TEMPERATURE VARIATION IN VACUUM ENVIRONMENT

I

Annex 1 ZTO and MoO_3 Synthesis

The necessary values for the solution's synthesis of ZTO and MoO_3 are presented in I.1 and I.2 respectively.

Table I.1: Synthesis calculations for ZTO solution.

Solvent	Precursor	Volume (L)	ZnO/SnO Ratio
2-methoxyethanol	Zinc nitrate hexahydrate	0,0075	75%
2-methoxyethanol	Tin (ll) chloride dihydrate	0,0025	25%

Precursor	Molar concentration (mol/L)	Molar mass (g/mol)	Mole ratio	n (mol)	Mass (g)
Zinc nitrate hexahydrate	0,2	297,48	1	0,0015	0,44622
Urea	0,2	60,06	5/3	0,0025	0,15015
Tin (ll) chloride dihydrate	0,2	225,64	1	0,0005	0,11282
Ammonium nitrate	0,2	80,043	1	0,0005	0,04002
Urea	0,2	60,06	1/3	0,000167	0,01001

Table I.2: Synthesis calculations for MoO_3 solution.

Solvent	Volume (L)	Molar mass (g/mol)
H_20	0,008	18,01528

Precursor	Molar concentration (mol/L)	Volume (L)	Molar mass (g/mol)	n (mol)	Mass (g)
Ammonium molybdate tetrahydrate	0,2		1235,94	0,002	2,47188
Ethylene glycol (EG)		0,002	62,07		
Dodecyl sulfate sodium salt (SDS)	0,2		288,38		0,05000

II

Annex 2 Manufactured samples resume

All the made samples are represented in II.1.

Table II.1: Samples produced by structure and manufacture properties.

Sample $N°$	Active layer	Bottom electrode	Top electrode	$N°$ of layers	Molar concentration	Annealing temperature
S1	MoO_3	Ti/Pt	Ti/Au or Ag	1	0,2	250°C
S2	MoO_3	Ti/Pt	Ti/Au or Ag	2	0,1	250°C
S3	ZTO	Ti/Pt	Ti/Au or Ag	8	0,2	300°C
S4	ZTO	Ti/Pt	Ti/Au or Ag	8	0,2	250°C
S5	ZTO	Ag	Ti/Au	8	0,2	250°C
S6	MoO_3	Ag	Ti/Au	1	0,2	250°C
S7	MoO_3	Ag	Ti/Au	1	0,2	250°C
S8	ZTO	Ag	Ti/Au	8	0,2	250°C
S9	MoO_3	Ti/Pt	Ag	1	0,2	250°C
S10	MoO_3	Ti/Pt	Ag	1	0,2	250°C
S11	ZTO	Ti/Pt	Ag	8	0,2	250°C
S12	ZTO	Ti/Pt	Ag	8	0,2	250°C

III

Annex 3 Pristine maps

Figures III.2, III.3, III.4, III.5, III.6, III.7 display the pristine maps of all working samples under investigation, the remaining samples described in annex II.1 were unable to characterize due to manufacturing problems or for being redundant. In III.8 the sweep comparison between two distinct environments, normal air and vacuum conditions is presented.

In all the tested samples, the voltage was swept between -0.5 V to 0.5 V or -0.8 V to 0.8 V, while the CC was set at 3 mA.

Figure III.1 shows the layout of a normal sample and the placement of the devices in it. This figure also shows where the Kapton tape was placed to protect and to make it possible to reach the bottom contact of the devices.

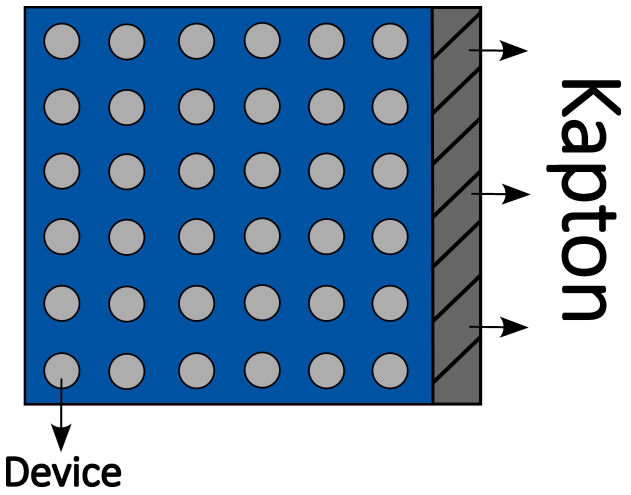

Figure III.1: Representation of a manufactured sample with Kapton tape.

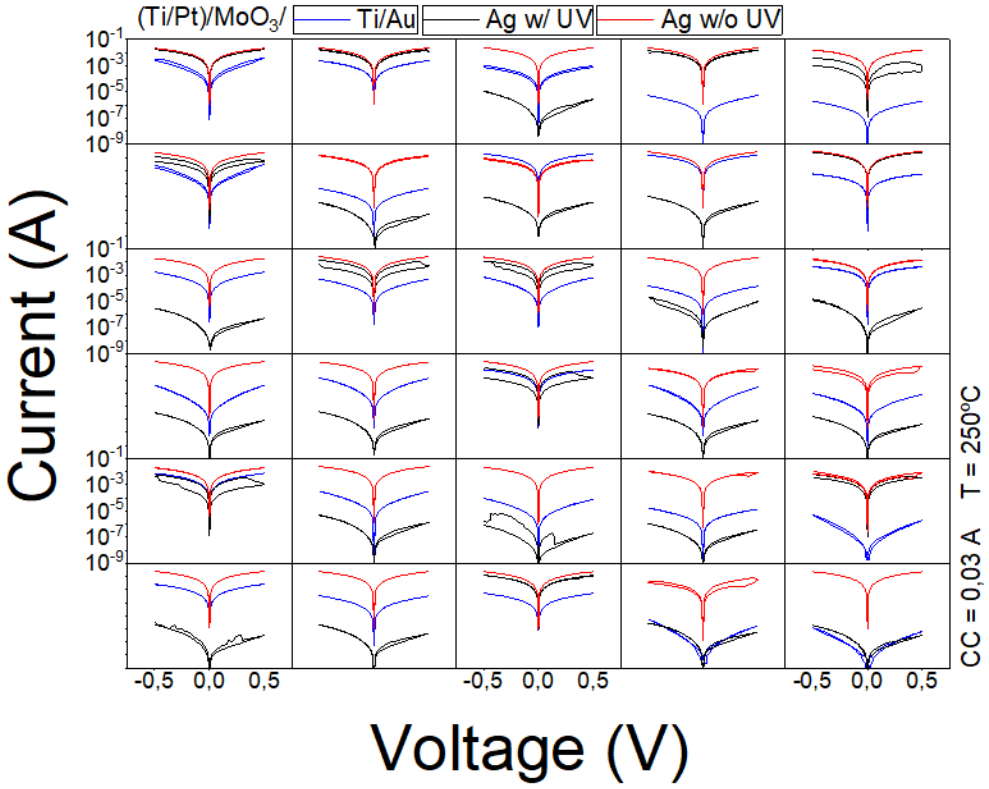

Figure III.2: Pristine map of sample 1: (Ti/Pt)/MoO_3/(Ti/Au) (blue); (Ti/Pt)/MoO_3/Ag after 30-min UV treatment (black); (Ti/Pt)/MoO_3/Ag (red). An active layer of MoO_3 with a molar concentration of 0.2 M and 1 layer deposited annealed at 250°C.

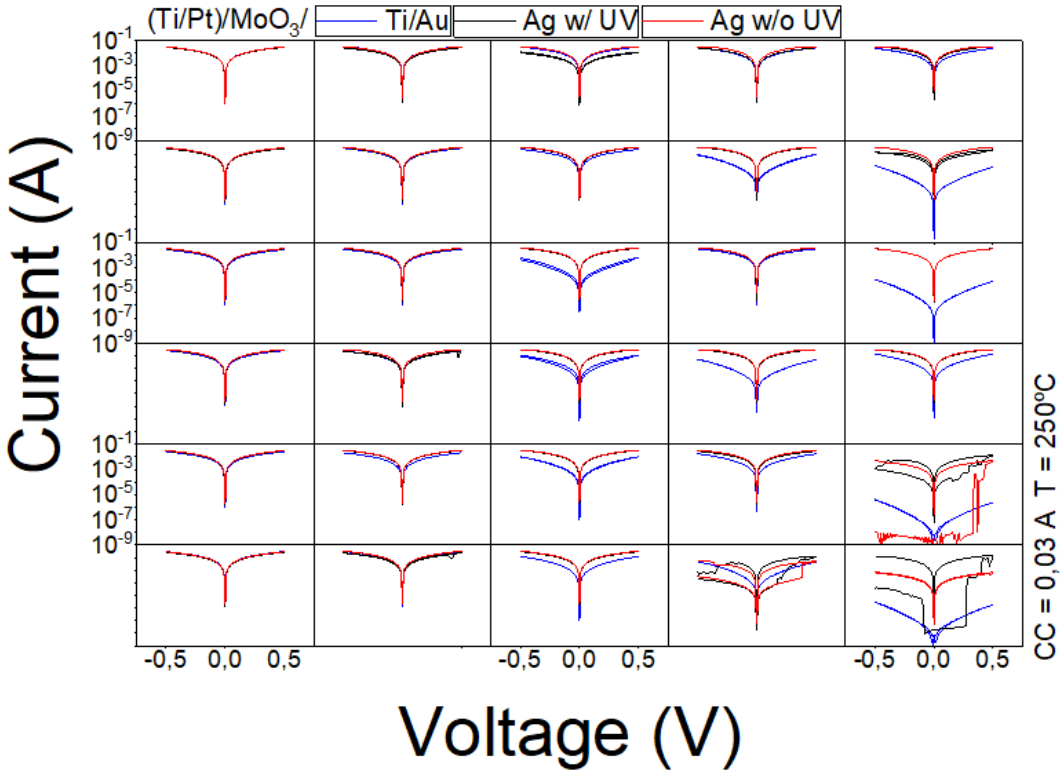

Figure III.3: Pristine map of sample 2: (Ti/Pt)/MoO_3/(Ti/Au) (blue); (Ti/Pt)/MoO_3/Ag after 30-min UV treatment (black); (Ti/Pt)/MoO_3/Ag (red). An active layer of MoO_3 with a molar concentration of 0.1 M and 2 layers deposited annealed at 250°C.

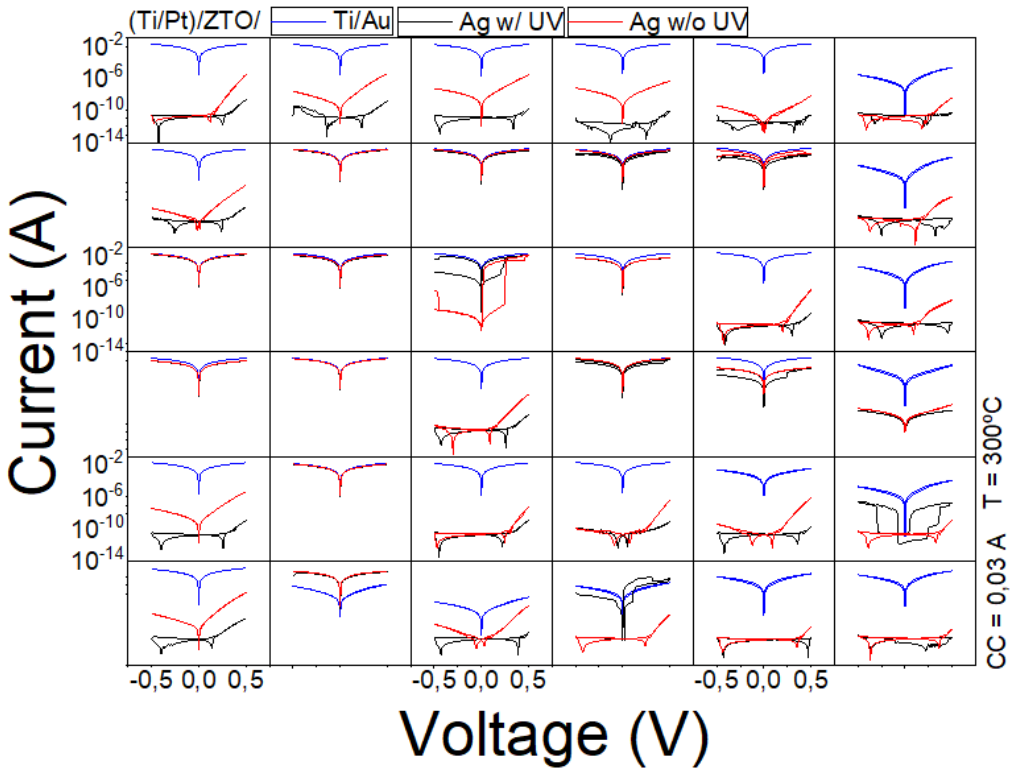

Figure III.4: Pristine map of sample 3: (Ti/Pt)/ZTO/(Ti/Au) (blue); (Ti/Pt)/ZTO/Ag after 30-min UV treatment (black); (Ti/Pt)/ZTO/Ag (red). An active layer of ZTO with a molar concentration of 0.2 M and 8 layers deposited annealed at 300°C.

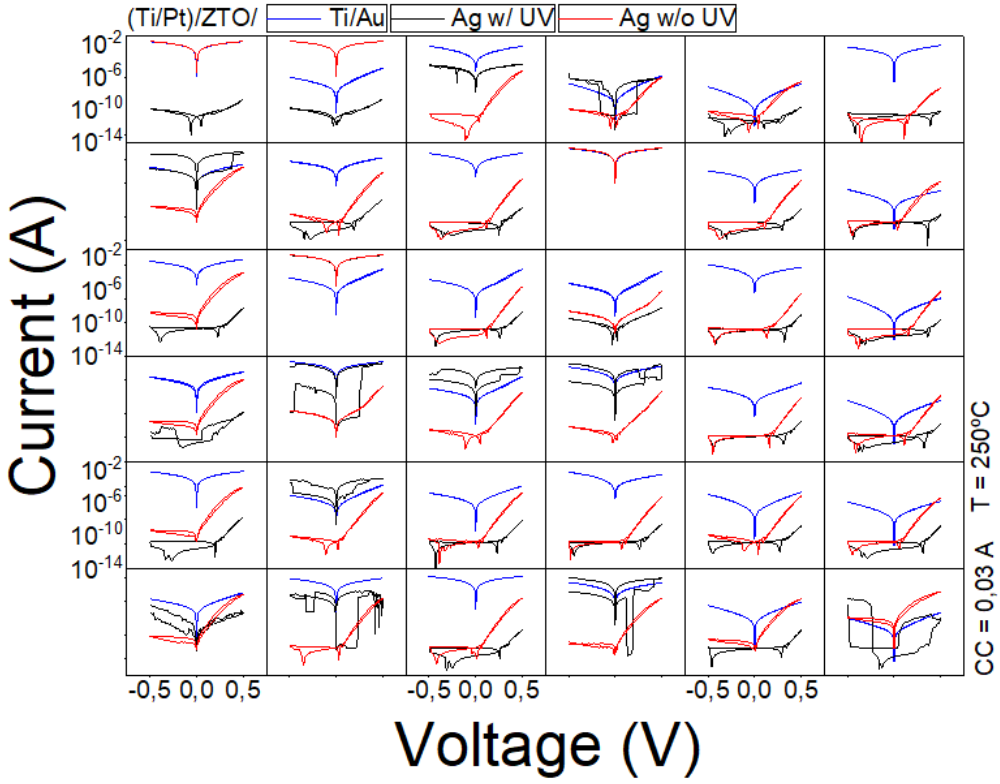

Figure III.5: Pristine map of sample 4: (Ti/Pt)/ZTO/(Ti/Au) (blue); (Ti/Pt)/ZTO/Ag after 30-min UV treatment (black); (Ti/Pt)/ZTO/Ag (red). An active layer of ZTO with a molar concentration of 0.2 M and 8 layers deposited annealed at 250°C.

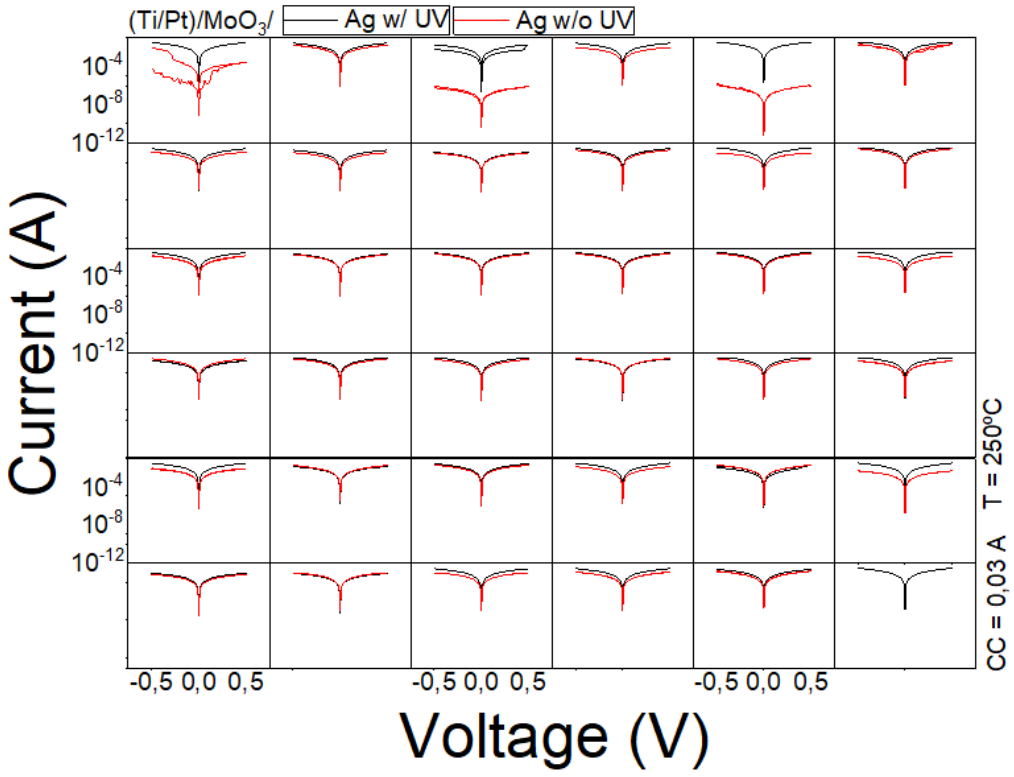

Figure III.6: Pristine map of sample 10: (Ti/Pt)/MoO_3/Ag after 30-min UV treatment (black); (Ti/Pt)/MoO_3/Ag (red). An active layer of MoO_3 with a molar concentration of 0.2 M and 1 layer deposited annealed at 250°C.

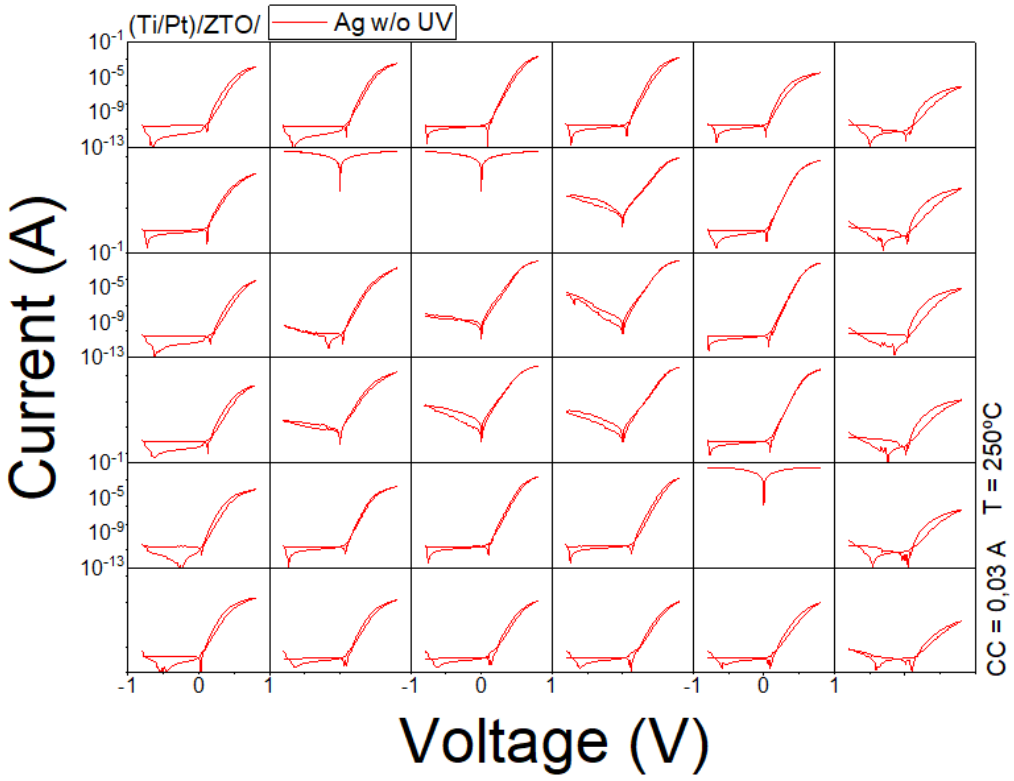

Figure III.7: Pristine map of sample 11: (Ti/Pt)/ZTO/Ag. An active layer of ZTO with a molar concentration of 0.2 M and 8 layers deposited annealed at 250°C.

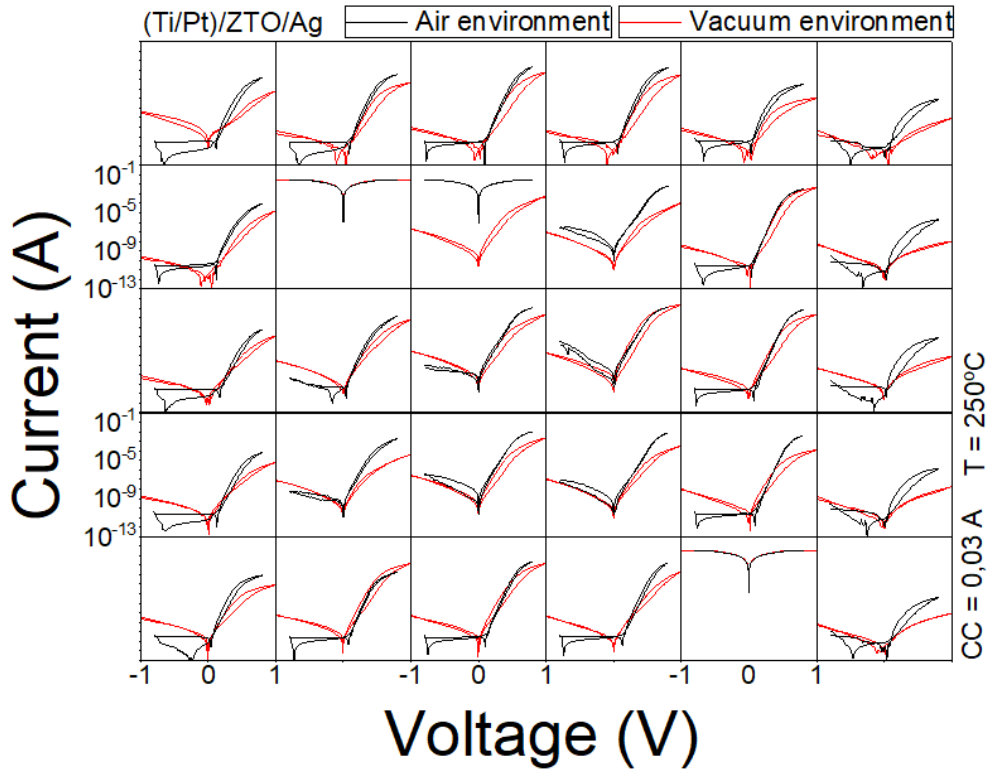

Figure III.8: Pristine map of sample 11: Different environment comparison in ZTO-based Schottky diode. Air environment (black) and vacuum environment (red). An active layer of ZTO with a molar concentration of 0.2 M and 8 layers deposited annealed at 250°C.