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Bachelor in Micro and Nanotechnologies Engineering

Enhancing the Bandwidth of a-IGZO TFT Amplifiers Using Circuit Design Techniques

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"If you think you can do a thing or think you can't do a thing, you're right."

- Henry Ford

Acknowledgments

Finalizing this thesis ends a chapter of my life that I'm so grateful to cherish. This section is reserved to mention and acknowledge those that were important to the completion of this final task. For that, I would like to thank:

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Abstract

Amorphous oxide thin-film transistor (TFT) technology has become central in flexible and low-cost electronic applications. However, there are some limitations of the technology for circuit implementation, particularly the lack of stable and reproducible p-type oxide TFTs, limited speed due to poor semiconductor mobility and to large channel lengths when compared to single crystalline Si devices. These limitations demand novel circuit design techniques using only n-type TFTs to achieve high-speed circuits meeting the requirement of practical applications. This work aims to improve the low unity current gain frequency of operation of a-IGZO based amplifiers using only circuit-based techniques, without changing the device structure, fabrication steps and materials. To achieve this objective, a generated negative capacitance is connected in parallel to the output node of an oxide TFT based amplifier, reducing the total effective capacitance present at this node. The output pole is shifted to a higher value, improving significantly the frequency response of the amplifier.

Simulations in Cadence environment were performed in five different amplifier structures, employing a-IGZO TFTs based on an in-house model developed with artificial neural networks. Up to three-fold improvement on bandwidth was verified, with minimal increases in power consumption and chip area. The concepts explored here are thus quite relevant to enhance low-MHz range circuits, as required for RFID and biomedical applications.

Keywords: Negative Miller Capacitance Compensation; a-IGZO TFT; Unity Current Gain Frequency; Circuit Design Technique.

Resumo

A tecnologia de transístores de filme fino (TFT) baseados em óxidos amorfos tem-se tornado central em aplicações eletrónicas flexíveis de baixo custo. No entanto existem limitações da tecnologia quanto à implementação em circuitos, tais como a falta de TFTs de óxidos de tipo-p estáveis e reproduzíveis, limites na velocidade do dispositivo devido à baixa mobilidade do semicondutor e grandes dimensões do dispositivo quando comparadas com dispositivos de Si cristalino. Estas limitações requerem técnicas de design de circuitos inovadoras que apenas utilizem transístores de tipo-n capazes de permitir a criação de circuitos de altas velocidades que cumpram os requisitos das aplicações práticas. Este trabalho procura melhorar a baixa frequência de ganho de corrente unitário de funcionamento dos amplificadores baseados em a-IGZO, usando apenas técnicas de design de circuito, sem mudar a estrutura do dispositivo, passos de fabricação, condições do processo e materiais. Para atingir este objetivo, uma capacitância negativa é conectada em paralelo ao nó de output de um amplificador baseado em TFTs de a-IGZO, reduzindo a capacitância total presente neste nó. Isto causa uma mudança do polo do output para valores mais elevados, melhorando significativamente a resposta em frequência do amplificador.

Simulações em ambiente Cadence foram realizadas em cinco estruturas diferentes, utilizando TFTs de a-IGZO baseados num modelo caseiro desenvolvido com redes artificiais neurais. Melhorias de banda até três vezes o valor original são reportadas, com aumentos mínimos de consumo de energia e de área ocupada. Os conceitos aqui explorados são relevantes para a melhoria de circuitos com operação a poucos MHz, como é necessário para RFIDs ou aplicações biomédicas.

Palavras-Chave: Compensação com Capacitâncias Negativas de Miller; a-IGZO TFT; Frequência de Ganho Unitário de Corrente; Técnica de Design de Circuito.

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Symbols

A_f	Feedback Gain
C_{ox}	Gate dieletric capacitance per unit area
f_T	Unity current gain frequency
gm	Transistor's transconductance
g_{ds}	Transistor's channel conductance
I_{DS}	Current flow between the drain and source
V_{DS}	Voltage between drain and source
V_{GS}	Voltage between gate and source
V_T	Threshold voltage
μ_{FE}	Field-effect mobility
μ_{SAT}	Saturation mobility

Acronyms

a-Si:H	Hydrogenated Amorphous Silicon
a-IGZO	Amorphous Indium-Gallium-Zinc-Oxide
AOS	Amorphous Oxide Semiconductor
AMOLED	Active Matrix Organic Light-Emitting Diode
ANN	Artificial Neural Network
CMFB	Common Mode Feedback
CMOS	Complementary Metal-Oxide Semiconductor
DRC	Design Rule Check
EC	Equivalent Circuit
FET	Field Effect Transistor
GBW	Gain Bandwidth Product
LTPS	Low-Temperature Polycrystalline Silicon
LVS	Layout Versus Schematic
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NCG	Negative Capacitance Generator
OTFT	Organic Thin-Film Transistor
RFID	Radio Frequency Identification
SRAM	Static Random-Access Memory
TFT	Thin-Film Transistor
ZTO	Zinc-Tin Oxide

1 Motivation and Objectives

In the past few years, there has been a renewed importance in amorphous Indium-Gallium-Zinc-Oxide Thin-Film (a-IGZO) thin-film-transistor (TFT) technology. It shows outstanding electrical characteristics when compared to other TFT technologies that allow flexible electronics, such as, amorphous silicon or organic-based semiconductors. Coupling this fact with the possibility of low-temperature fabrication in low-cost large-scale environment creates a whole new range of applications. Examples such as RFID [1] or biomedical wearables [2] require oxide TFT circuits (especially OpAmps) operating at MHz ranges, while state of the art work is mostly limited to kHz ranges [2–4] due to inherent technology limitations and parasitics due to large device dimensions.

This substantial effort to enhance even further the performance levels of flexible, low-cost technology must be divided into different areas, such as picking the right semiconductors, optimizing the various fabrication steps and developing new circuit design techniques. With a-IGZO TFTs having a mobility at least one order of magnitude lower than the complementary metal-oxide semiconductor (CMOS) devices there is a demand for high-speed design techniques at circuit level [5]. The main objective of this work will consist in translating a negative Miller capacitance technique, that has been applied successfully in CMOS circuits as a bandwidth enhancer, to amorphous oxide semiconductor (AOS) TFT technology as to mitigate one of the major drawbacks that are present in this field.

The application of this novel technique to a-IGZO TFT based circuit blocks throughout this work is done through various steps such as the design and simulation confirmation of a working negative Miller capacitance generator in CMOS technology, followed by the design of various amplifiers based in a-IGZO TFTs but instead with nMOS transistors, which operate under a much more precise and studied model. This negative capacitance will then be connected to the outputs of the different amplifiers, as a proof of concept. After the confirmation, this technique will then be translated into a-IGZO TFT based amplifiers.

2 Introduction

In this chapter an introductory overview of the major topics addressed in this thesis will be given, focusing the oxide TFT's technological evolution and current state of the art, most common structures, operation principle and limitations of the technology in circuit design. There is a constant need for the enhancement of the properties of the circuits based on this technology. For that purpose, novel circuit design techniques must be studied.

One main area in which TFTs are being widely used is in flexible and transparent technology, due to the ability of low-cost and low-temperature fabrication, allowing for production over a large area in flexible substrates.

2.1. The Evolution of the TFT Technology

In the past few years, research involving all the different segments of the TFT technology has been blooming [6]. a-Si:H, organic and low-temperature polycrystalline silicon TFTs (LTPS TFTs) are a few examples of these advances [7]–[10]. There isn't, however, a technology that simultaneously allows large-scale fabrication, flexible substrates, and optimal electrical performance.

All these factors taken into consideration lead to the pursuit of new technologies. This is how the focus on oxide TFTs started to grow in the last years. While presenting a low production cost and processing temperatures, oxide TFTs have shown outstanding mobility values compared to its counterparts, coupled with large scale fabrication [11]–[13]. Oxide TFTs started gaining ground with Nomura et al. in 2003 [12] with a single-crystalline IGZO semiconductor layer TFT that, while displaying a great electrical performance with a mobility of 80 $cm^2\ V^{-1}\ s^{-1}$, still required a processing temperature of 1400°C, and later in 2004 [13], when the same group presented results with an amorphous IGZO based TFT fabricated at room temperature, capable of showing a mobility of 9 $cm^2V^{-1}s^{-1}$, threshold voltage of 1 to 2 V and an on/off ratio of 10^3. In Table 2.1 it is possible to observe a summary of the different TFT technology characteristics. With each passing year, oxide TFTs are becoming more central due to the exceptional inherent properties. The most studied and therefore optimized oxide TFT is based on the a-IGZO semiconductor. There are, although, other very promising oxide TFTs

based on other oxides such as ZnO, with a processing temperature of 90 °C and a 7.53 $cm^2 V^{-1} s^{-1}$ mobility [14] or zinc-tin-oxide (ZTO) showing a mobility of 27.3 $cm^2 V^{-1} s^{-1}$ with a 500°C processing temperature [15]. The search for p-type oxide TFTs is also ongoing, as oxide p-type TFTs using SnO_x were reported presenting a 0.87 $cm^2 V^{-1} s^{-1}$ mobility with a maximum processing temperature of 400 °C [16].

Table 2.1 - Comparison of TFT technologies with different semiconductor layers, based on [6]–[8], [10], [11], [17], [18].

	Oxide TFT	a-Si:H TFT	LTPS TFT	Organic TFT
Mobility ($cm^2 V^{-1} s^{-1}$)	<60	<1	<100	<10
Aging Stability	Good	Good	Good	Poor
Processing Temperature (°C)	RT - 300	200-300	<500	RT
Fabrication Process	Sputtering, Printing or Solution-based	PECVD	Laser Excimer & CVD	Evaporation, Printing or Solution-based
Uniformity	Good	Good	Poor	Poor
Flexibility	Yes	No	No	Yes
Transparency	Yes	No	No	Yes
Device	NMOS	NMOS	CMOS	PMOS

Oxide TFTs based in a-IGZO do present great electrical properties, as seen in [19]. The different fabrication processes are also being expanded, such as solution-based processes, where the ability to not use photolithographic masks makes this a low-cost process. Y. S. Rim *et. al.* produced, at room temperature, an a-IGZO TFT through solution-based processes, with a mobility of 22.16 $cm^2 V^{-1} s^{-1}$. Combining all these different factors turns oxide-based TFTs into a very promising technology for circuit integration in the most varied applications such as RFID tags [1], biomedical wearable devices [2], AMOLED backplanes [20] or even touch sensors [21].

2.2. Different TFT Structures and Operation Principle

The TFT is essentially a FET, comprised of three terminals, the gate, source and drain electrodes, a semiconductor layer and a dielectric layer. The semiconductor layer is placed

between the drain and the source terminals while the dielectric layer is placed between the semiconductor layer and the gate terminal. The most common setups of these layers can be seen in Figure 2.1, the architectures vary from each other through the location of the three terminals relative to the semiconductor layer.

TFTs operate through the control of current flow (I_{DS}) between the drain and source terminal by the voltage applied to the gate and drain terminal (V_{GS} and V_{DS}), exactly like other FET devices. Considering an n-type TFT, its operation principle is defined as enhancement mode (usually called as normally off), or as depletion mode (in this case normally on), if the threshold voltage value (V_T) is positive or negative, respectively. Generally, the enhancement mode of operation is preferred since it requires no voltage value applied at the gate to turn the transistor off, minimizing power dissipation and simplifying circuit design, as opposed to depletion mode [22].

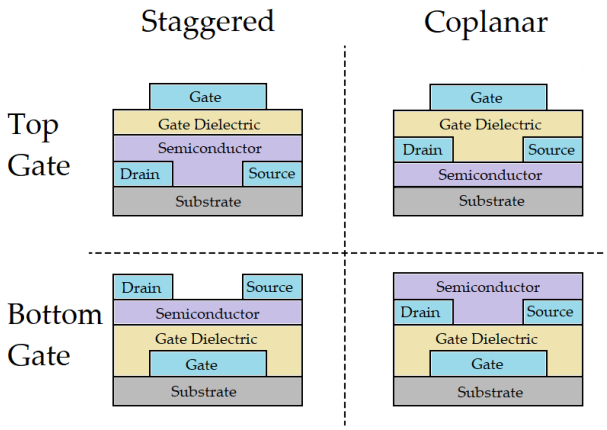

Figure 2.1 – Cross sectional schematic of the four most used setups in n-type TFT, based on [11].

If $V_{GS} \ll V_T$ the transistor is in its off state or subthreshold region, as there is almost no conductive channel between the source and drain, resulting in a very low I_{DS} value. If there is a positive value of voltage between the drain and source (V_{DS}), and $V_{GS} > V_T$ the transistor will be in it's on state. This is due to the electrons in the semiconductor (which is inherently n-type) accumulated near the dielectric and semiconductor interface which forms a conductive channel, resulting in a current flow from drain to source.

The IV characteristic curves of an a-IGZO TFT can be seen in Figure 2.2, and through the output characteristics (b) it is possible to define the two different regimes. The linear regime

can be observed when $V_{DS} < V_{GS} - V_T$, which results in a linear increase in I_{DS}, and can be expressed by:

$$I_{DS} \approx \mu_{FE}.C_{ox}\frac{W}{L}((V_{GS} - V_T)V_{DS}) \tag{2.1}$$

where C_{ox} is the gate dielectric capacitance per unit area in F/cm², μ_{FE} is the field-effect mobility in $cm^2\,V^{-1}\,s^{-1}$ and W and L are the width and length of the TFT channel, respectively.

The other regime occurs when $V_{DS} > V_{GS} - V_T$, and the TFT is said to be in saturation mode. The TFT's semiconductor layer close to the drain becomes depleted and the pinch-off effect takes place. Saturation mode is highly relevant for amplifier implementation and can be represented by:

$$I_{DS} \approx \mu_{SAT}.C_{ox}\frac{W}{2L}(V_{GS} - V_T)^2 \tag{2.2}$$

where μ_{SAT} is the saturation mobility in $cm^2\,V^{-1}\,s^{-1}$.

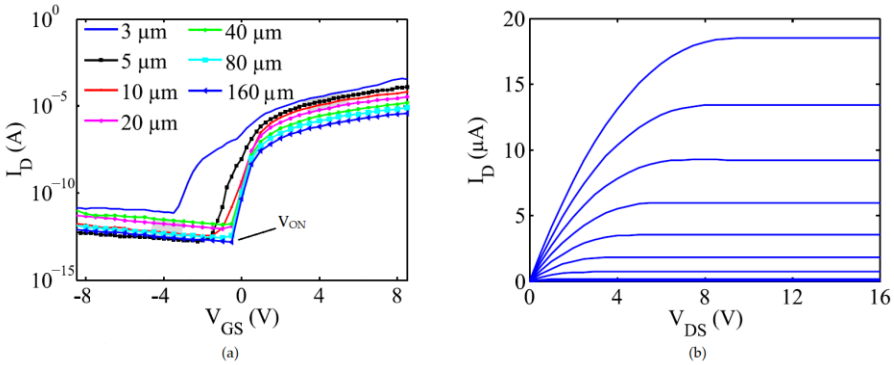

Figure 2.2 – Measured characteristic curves of an a-IGZO TFT, adapted from [23]. (a) Transfer characteristics with different TFT channel lengths, with V_{DS} = 16 V and W = 20 µm. (b) Output characteristics with V_{GS} from -2 V to 8 V values for L = 40 µm.

2.3. Challenges of AOS TFT Based Amplifiers

The unity current gain frequency (f_T) dictates the maximum frequency at which the TFT behaves in an expected way, limiting its efficient use. This value can be expressed by:

$$f_T \approx \frac{g_m}{2\pi C_G} \tag{2.3}$$

where g_m is the TFT's transconductance and C_G is the total gate capacitance.

The limitations present in a-IGZO based amplifiers have their origin in the large parasitic capacitances that exist in oxide TFTs, as seen in the general expression for most amplifiers of the output dominant pole:

$$\omega_{Pout} = \frac{1}{2\pi R_{eqOut} C_{eqOut}} \tag{2.4}$$

where R_{eqOut} is the equivalent output resistance and C_{eqOut} is the equivalent output capacitance at the output node to the ground.

Due to low intrinsic mobility caused by the amorphous nature of the oxide, one way to increase the bandwidth of oxide TFT based amplifiers is by decreasing the overall effective capacitance present at the output node from the TFTs. Several techniques in this topic have been studied. Dual-gate a-IGZO TFTs [24] increases transconductance, compensating the high parasitic capacitance values, at a cost of extra steps in the fabrication process. Self-aligned and stripe patterned source/drain TFTs can be part of high-speed circuits [25], [26] as the parasitic capacitances are reduced through the much smaller overlaps between gate and contacts, however, these techniques require a much higher resolution, different fabrication conditions and steps resulting in higher costs. Even though smaller TFT dimensions and smaller overlaps can also be a path to reduce parasitics [23], this method creates new obstacles such as non-idealities in smaller transistor dimensions, as well as resulting in a higher cost of fabrication due to more expensive facilities.

Our proposal, further expanded in chapter 4, is to decrease the output effective capacitance without changing the device's characteristics through a circuit design technique named negative Miller capacitance compensation. By adding a generated negative capacitance in parallel to the output node, a negative value of capacitance appears in the expression of C_{eqOut}, reducing its overall magnitude and therefore increasing the value of frequency at which the dominant pole is located, resulting in a larger bandwidth of operation. This can be seen through the new expression of the dominant pole:

$$\omega_{Pout} = \frac{1}{2\pi R_{eqOut}(C_{eqOut} + C_{Ieq})} \tag{2.5}$$

where C_{Ieq} is the resultant capacitance from the negative Miller compensation as seen later in expression 4.3. This technique has been widely applied in CMOS technology, however, its application in TFT is completely novel and will be studied for the first time in this work.

3 Methodology

3.1. Simulation Conditions and Tools

All the designs and simulations were performed mainly using the software from Cadence Design Systems. The schematics and layout designs for each structure were created using the Virtuoso System Design Platform, while the simulations for each respective circuit were performed in the Spectre Circuit Simulator.

In this work, as discussed before, nMOS and a-IGZO TFTs were used. The models used for CMOS transistors is the 130nm model. For a-IGZO TFTs, the used model was developed in-house using artificial neural network (ANN) based equivalent circuits (EC) in order to predict the static and dynamic behavior of the device. In this model, an EC is constructed from the device structure, as lumped elements which are individually modeled using ANN. These elements are later connected as part of the EC and implemented in Verilog-A [27].

All the size values for the different transistors were obtained via the interpretation of the transfer function for the different amplifiers, in order to obtain the best possible gain. None of the amplifiers were designed with output impedance loads, so a smaller *GBW* is expected after fabrication.

As for the different layout designs, the process design kit (PDK) is based on the in-house existing at CEMOP/UNINOVA. Errors such as misalignment of the masks are one of the safety factors that are considered in the PDK. In order to confirm that the layouts are properly designed features such as design rule check (DRC) and layout versus schematic (LVS) were used.

The DRC is a set of rules imposed by the limitations in the fabrication process, that need to be followed by the schematic. These rules consider parameters such as maximum and minimum overlap between Source/Drain and Gate layers, minimum separation between each via in the same layer, minimum width of a via of a single layer or even the minimum width of a hole in M_1 in order to connect the Source/Drain to Gate layers.

The LVS compares the designed layout to the equivalent schematic, checking if every component and electrical connections between each component are present. This way it is possible to know if the layout going into fabrication is completely correct and matches the schematic perfectly.

4 Results and Discussion

This chapter is divided into four major parts. The first part will consist of the explanation of the theory behind the negative Miller compensation circuit design technique and its effect on the amplifier's frequency response, as well as its application in a real-world a-IGZO based circuit. It will be followed by a very small part dedicated to a proof of concept in CMOS technology. This is due to the availability of much more precise CMOS transistor models. In the third chapter, there will be various subsections dedicated to the method of operation of each amplifier, layout and to the results and analysis of the negative Miller compensation technique applied to each amplifier.

4.1. Negative Capacitance Generation

The negative capacitance generation technique is extensively studied for CMOS technologies and can be employed by several different circuit topologies. The chosen circuit topology for generating negative capacitance will be discussed a few sub-chapters below.

4.1.1. Miller theorem

The Miller theorem establishes that if there is a floating impedance connected to two different voltage sources in series, it can be replaced by two different impedances connected to the ground. This theorem is widely used in circuit analysis, such as analysis of feedback based circuits and amplifiers at higher frequencies [28]. This theorem's visual representation can be seen in Figure 4.1, where C is the floating impedance. As expected, the feedback capacitor, when employed between the input and the output nodes of an amplifier, can be represented as a capacitance between the input node and the output node to the ground, C_{M1} and C_{M2} respectively. The value of the output capacitor is closer to the value of the capacitor C and both are represented as follows:

$$C_{M1} = C(1 - A) \tag{4.1}$$

$$C_{M2} = C\left(1 - \frac{1}{A}\right) \tag{4.2}$$

where A is the gain of the amplifier.

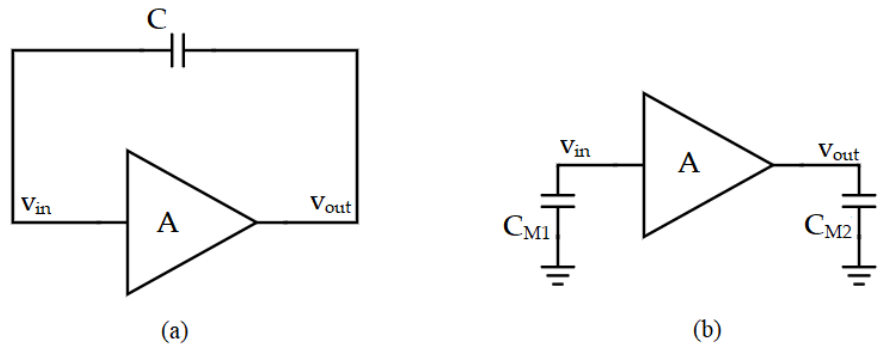

Figure 4.1 - (a) Amplifier schematic with a feedback capacitor and (b) equivalent circuit schematic representing the Miller effect.

Negative Miller capacitance generation, in this case, due to the use of negative capacitance, is based on the Miller effect theory, where the impact of the feedback capacitance is shown on the input capacitance. For this effect to take place, the capacitor must be connected around a non-inverting amplifier with a gain A≫1. This leads to the final value of the equivalent input capacitance (C_{Ieq}) at the NCG, not taking the amplifier into account, which would be mathematically expressed by:

$$C_{Ieq} = C_{Input} + (1 - |A|)C \tag{4.3}$$

where C_{Input} is the input capacitance of the NCG structure and is smaller than C. By the expression 4.3, it is then possible to see that applying this technique in the output of an amplifier would result in the removal of the undesired capacitance at that node. The negative value of the equivalent input capacitance when added in parallel with the output capacitance of the amplifier denies the parasitic capacitance at the output node of the amplifier, resulting in an increase of the bandwidth of the amplifiers, as seen in expression 2.5.

4.1.2. Negative Capacitance Generator

Negative capacitance can be achieved through different structure setups. It is known that negative capacitances can be created using a cross-coupled capacitance pair in a positive feedback loop configuration [29]. The most common structures can be observed in Figure 4.2, where the optional inductors in (b) and (c) are used to increase the bandwidth.

In this work, in order to simplify the fabrication of the circuit and to keep the power consumption and chip area low, the used negative capacitance generator (NCG) is seen in

Figure 4.2 (a). The integration of the NCG in the circuit block is achieved by connecting its output to the matching output of the amplifier, as seen in Figure 4.3. This way the NCG is separated from the main amplifier as a way to avoid more parasitic capacitances originated from the cross-coupling capacitor [30]. To match the biasing of the NCG to the amplifier there is a need to adjust the load resistor, however, that also changes the gain of the NCG. Different values of load resistance are used throughout this work.

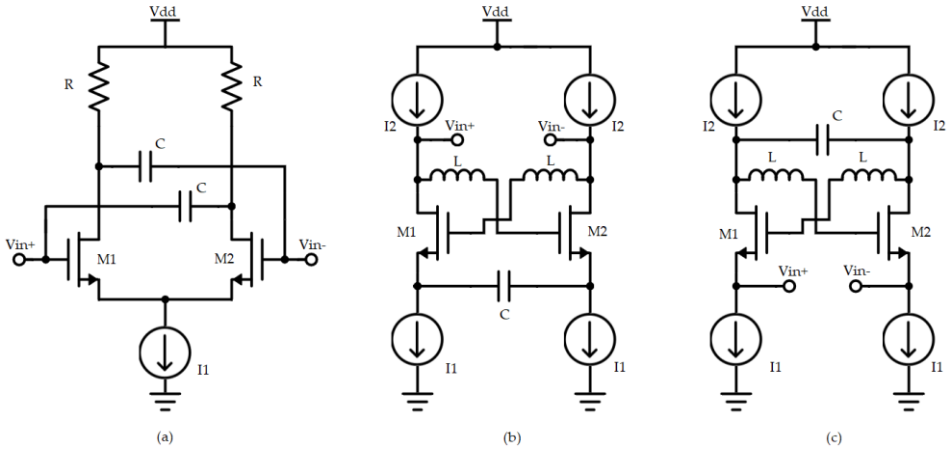

Figure 4.2 - Schematic of different negative capacitance generators. (a) Differential NC pair. (b) Drain input cross-coupled NC circuit. (c) Source input cross-coupled NC circuit. Adapted from [31].

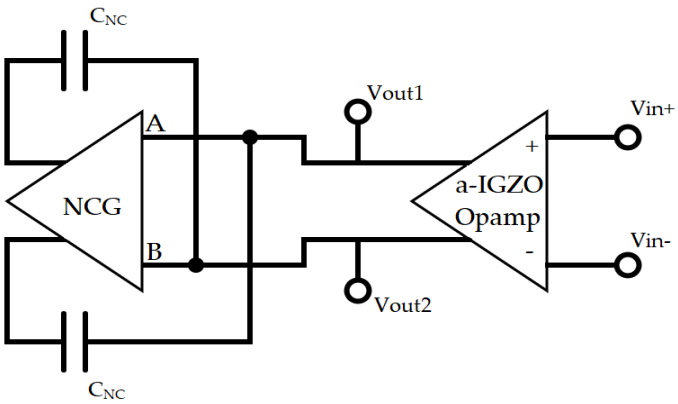

Figure 4.3 - Block diagram of the NCG integrated with the amplifier.

4.2. CMOS Proof of Concept

Taking into consideration all the work done on this topic some structures were designed and tested along with the use of negative capacitance, only using CMOS technology. This step was performed based on the availability of highly precise metal oxide semiconductor field-

effect transistor (MOSFET) models. The design of the NCG structure in CMOS technology is replicated from Figure 4.2 and can be seen in Figure A.1.

The obtained negative capacitance values for five different cross-coupling capacitors and respective frequency responses can be observed in Figure 4.4. As expected, higher values of capacitance correspond to higher values of negative capacitance, however, it does come at a cost of smaller *GBW* and chip area. Smaller capacitances also mean a higher *GBW* and chip area but this comes at a heavy cost of phase margin. For this reason, and for the fact that the impact in the amplifier's bandwidth is minimal, 50fF cross-coupling capacitors were chosen for the CMOS amplifier.

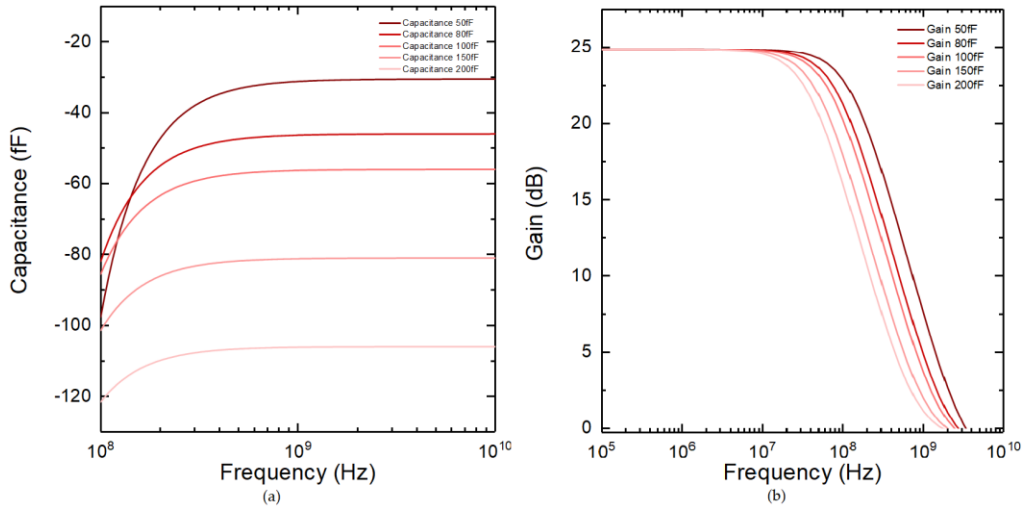

Figure 4.4 - (a) Simulated negative capacitance values for different pairs of cross-coupling capacitors and (b) respective frequency response.

4.2.1. Single-ended Cascode with Bootstrapping

To test the effect of the NCG, a simple single-ended cascode with bootstrapping only using nMOS (derived from the lack of p-type transistors in amorphous oxide technology) was designed based on [3]. For the simple purpose of proof of concept, in this section there will only be a display of results. Detailed circuit analysis of this amplifier operation can be found further in sub-chapter 4.3.3., corresponding to the same circuit but in a-IGZO technology. The schematic of the amplifier designed in CMOS technology can be found in Figure A.2.The gain and phase of the amplifier before and after the application of the NCG can be seen in Figure 4.5.

Through the gain and phase curves, it is possible to see everything that was predicted before. In the phase curve in Figure 4.5 (b) it is possible to see the first pole in the left being pushed to lower frequencies and the second, dominant pole pushed to higher frequencies, resulting in an increase in f_T as seen in (a). Since the gain of the NCG was 24.9 dB when biased to match the amplifier and the amplifier presented a 32.8 dB gain when combined the amplifier's gain will decrease to 29 dB. Through the application of the NCG, the *GBW* increased from 67.2 MHz to 106.8 MHz, showing a 59% increase in the maximum frequency of operation, while only increasing power consumption from 0.2 mW to 0.38 mW. The minimum feature size present is 500 nm and a maximum of 1.8 V for power supply was used.

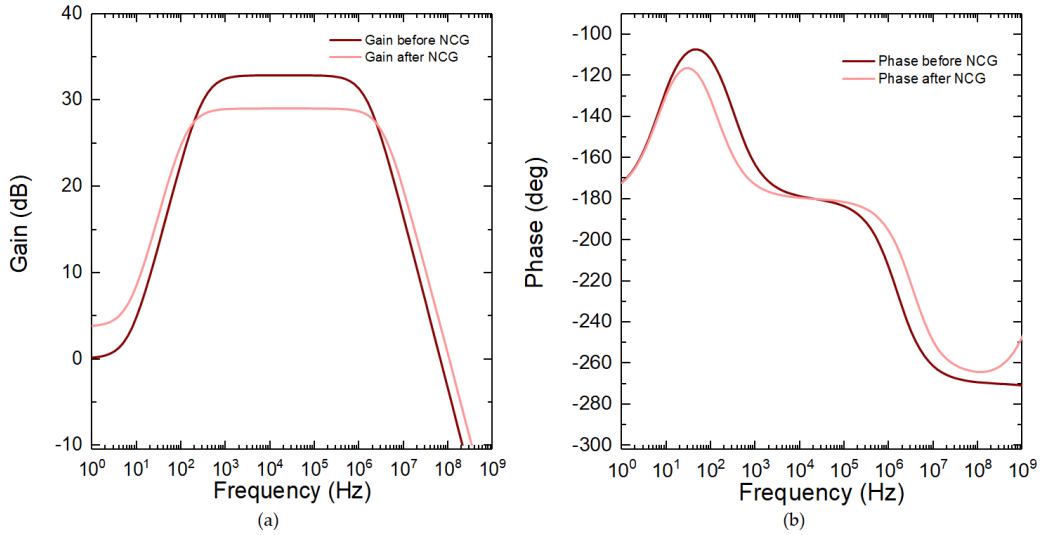

Figure 4.5 - MOSFET amplifier before and after the NCG application (a) Gain. (b) Phase.

In the next chapter, after proving that the technique can be used only using n-type transistors, the same NCG structure was designed using a-IGZO TFTs with the objective of increasing the *GBW* without sacrificing other parameters such as gain or power consumption.

4.3. Bandwidth Enhancement of a-IGZO TFT based amplifiers with NCG

In this sub-chapter, a detailed analysis of the NCG and each different amplifier in a-IGZO technology will be presented as well as the schematic and layout designs, to understand how the negative capacitance would affect its performance. The results from the application of the NCG in the different amplifiers will be presented and analyzed, complemented by a

comparison with current state-of-the-art literature. To avoid repetition, a more in-depth analysis is done for the first amplifier. The circuit schematics of the application of the NCG in Virtuoso software can be seen in Annex A. All the transistors dimensions for the a-IGZO NCG and different amplifiers can be found in Table B.1 in Annex B.

4.3.1. Negative Capacitance Generator

The structure used for negative capacitance generation in a-IGZO technology is the same as seen in Figure 4.2. The first part of the NCG design was to confirm that it did generate a negative capacitance and which capacitance values for the cross-coupling capacitors would be best suited for the use in this project. The gain, phase, and generated negative capacitance value can be observed in Figure 4.6. It is possible to observe through the different curves that this NCG behaves the same way as the NCG in CMOS technology. We can observe how the dominant pole is shifted for higher frequencies for lower capacitance values, leading to a higher *GBW*, in the phase and gain curves respectively.

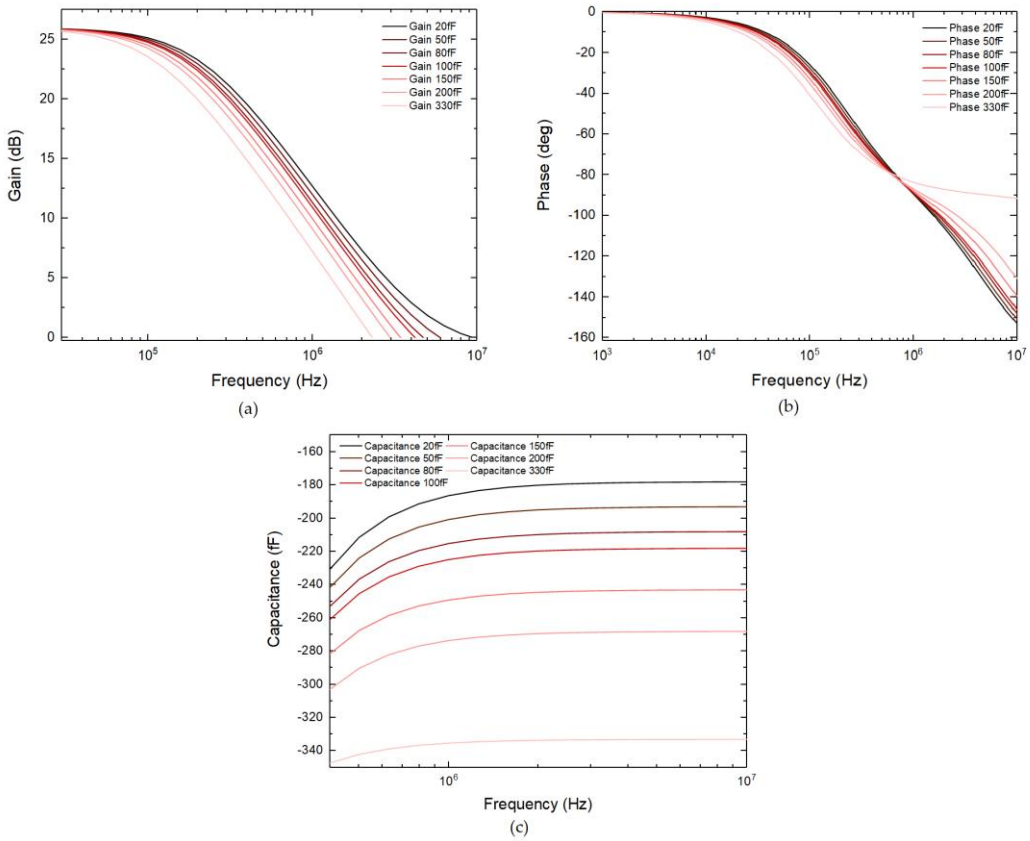

Figure 4.6 - Different circuit characteristics for each value of cross-coupling capacitors dimensions in the NCG. (a) Gain. (b) Phase. (c) Generated capacitance.

Keeping in mind the final objective of this work, in order to ensure a good performance and stability in the fabricated a-IGZO based amplifiers, the phase margin of the NCG for different values of capacitance in the cross-coupling capacitors was studied, and the results can be observed in Figure 4.6 (b). If a smaller value was to be used, the *GBW* of the amplifiers would see a bigger increase, but this does come at a cost of much smaller phase margin in the NCG, leading to greater instabilities.

For each different application of the NCG, a different load resistor value was used in order to ensure proper biasing, which also affects the phase margin. In order to keep the phase margin always above 60°, no matter the application, the chosen capacitance values for the cross-coupling capacitors in this part of the project was 100fF and 330fF. Two different values were used and studied in the NCG in order to get the best results from each different amplifier. The gain of the NCG isn't affected by the dimensions of the cross-coupling capacitors.

Table 4.1 – Parameter comparison for different capacitance values of the cross-coupling capacitors.

	20fF	50fF	80fF	100fF	150fF	200fF	330fF
GBW (MHz)	9.50	5.99	4.73	4.23	3.45	2.98	2.32
Phase Margin (°)	28.55	43.89	54.08	59.98	70.03	78.05	92.38

For higher values of cross-coupling capacitor dimensions, the second pole shifts for higher frequencies as seen in Figure 4.6 (b). The effect of higher capacitance values in the phase curves doesn't seem to have any implications when applied to the amplifiers other than the lower expected impact in the *GBW* value. These values of higher capacitance do show a higher phase margin and, if high enough, this higher value can have a positive impact in the phase margin of the amplifier itself, as seen further in this chapter. In Figure 4.6 (a), as expected, the flatband gain remains the same for lower frequencies, but the *GBW* does decrease due to higher impedances introduced by the bigger capacitors. In Figure 4.6 (c), it is possible to see how the generated capacitances are larger than observed in MOS technology in Figure 4.4 (a) due to the larger impedances resultant from the TFT's low mobility and gate overlap capacitances.

The designed layout for the NCG that was later applied to all the a-IGZO based amplifiers can be seen in Figure 4.7, with an area of approximately 0.12 mm^2. Further study into the

capacitance generated by the NCG must be done, in order to comprehend how the unavoidable parasitic capacitances from the overlaps of the different vias impact the general performance of the circuit and its application.

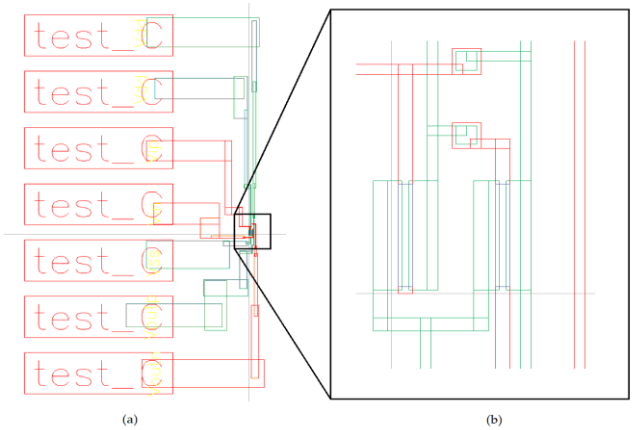

Figure 4.7 - (a) NCG full layout design with external pads. (b) NCG detail.

4.3.2. Positive Feedback Differential Amplifier

The positive feedback differential amplifier is a circuit topology that has been extensively studied [2], [8], [32]. The schematic and small-signal equivalent can be seen in Figure 4.8. Vout+ and Vout- are the differential outputs of the amplifier while Vin+ and Vin- are the differential input voltages. The operation of the amplifier is heavily based on g_m cancellation of the load transistors (M3 and M4). The feedback formed by M6-M10 has a feedback gain (A_f). This value must be ensured to be lower than 1, in order to keep the amplifier stable and still maintain a high gain.

Through the small-signal equivalent, where V_{G3} is equal to V_{out} times the feedback gain, it is possible to extract the transfer function:

$$A_V = \frac{g_{m1}}{(1 - A_f)g_{m3} + g_{ds1} + g_{ds3}} \tag{4.4}$$

where g_{ds} is the channel conductance.

The dominant pole's expression is seen in equation 4.4. In this case R_{eqOut} and C_{eqOut} are:

$$R_{eqOut} = r_{01} || \left[\frac{1}{(1-A_f)gm_3} || r_{03} \right], \quad C_{eqOut} \approx C_L + C_{gd1} * (1 - A_1) + C_{gs6} \tag{4.5}$$

with A_1 being the gain of the transistor M1.

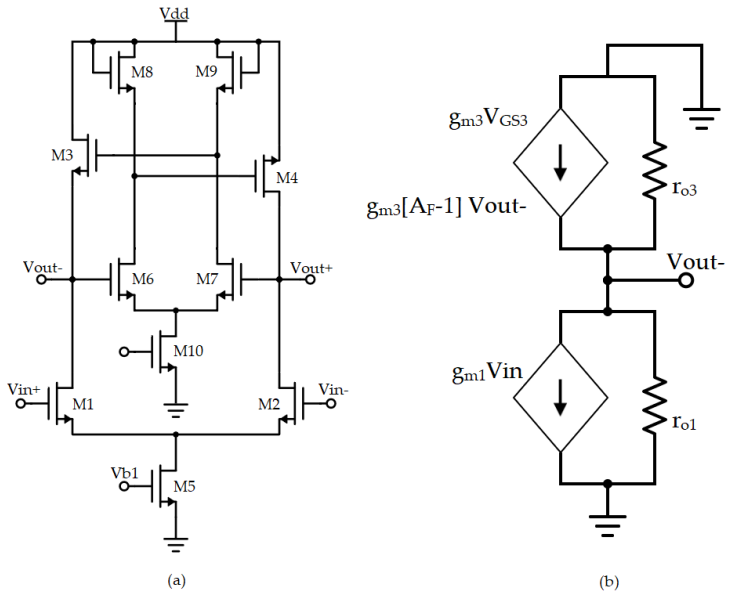

Figure 4.8 - Positive feedback based differential amplifier (a) schematic and (b) small-signal equivalent.

The final layout of this structure with NCG integration can be found in Figure 4.9.

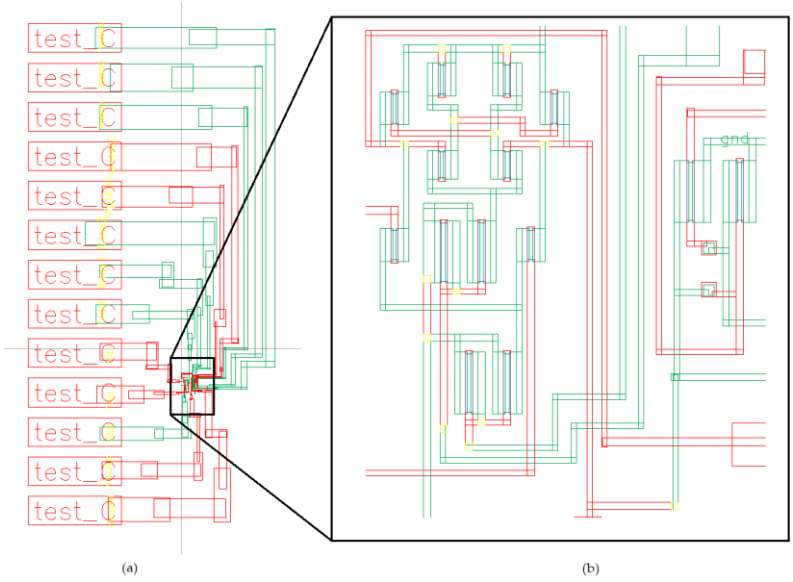

Figure 4.9 - (a) Positive feedback based amplifier with NCG full layout design with external pads. (b) Amplifier plus NCG detail.

4.3.2.1. Positive feedback differential amplifier frequency response

The obtained curves resulting from the connection of the outputs of the two NCGs to the outputs of the amplifier can be seen in Figure 4.10. From the gain frequency response it is possible to observe how the pole is shifted forwards, increasing *GBW*. The value of the resulting gain evens out between the gain of the amplifier and the gain of the NCG, decreasing or

increasing. In this case, the gain decreases due to a smaller NCG gain value. In most cases throughout this work, this happens due to the need for proper biasing and a certain value of the load resistor in the NCG, locking the obtainable gain to that value.

Higher gain can be obtained using a larger power supply, although that does come at a cost of much larger power consumption. Without the NCG the amplifier was showing a 35.8 dB flatband gain with a *GBW* of 481 kHz. The value of the gain decreases to 27.6 dB since the NCG presents a 25 dB gain. The amplifier with the NCGs shows a 1.50MHz *GBW* for the 100fF NCG and 1.22 MHz for the 330fF NCG. This was achieved with a power consumption increase from 0.5 mW to 0.8 mW and a chip area increase from 0.84 mm^2 to 1.39 mm^2. The amplifier used a 10 V power supply while the NCG used a 15 V power supply. A minimum feature size of 10 μm was used. The value of the load resistor in the NCG for correct biasing is 1.0134 MΩ. It is possible to see in Table 4.2 all the summarized simulation results.

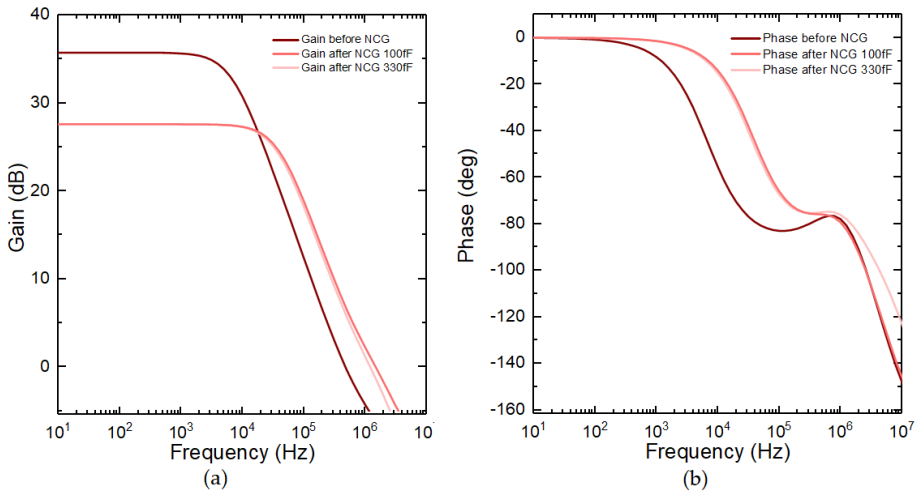

Figure 4.10 - Positive feedback amplifier with and without NCG application (a) gain plots, and (b) phase plots.

These results are subject to change in fabricated circuits due to an introduction of parasitic capacitances resulting from the interception of the different metal vias in different layers. All the observed results were expected, the increase in *GBW* coupled with the decrease of gain due to the smaller NCG gain. It is very important to note one important effect that occurs when using different values for cross-coupling capacitance. When bigger capacitors in the NCG are used, the equivalent output capacitance will be higher (as seen in expression 4.3).

Table 4.2 - Summary of the results obtained from the simulated application of the NCG to the positive feedback based amplifier.

		Gain (dB)	Phase Margin	*GBW*	Pwr consumption	Chip area	Min. feature size
Before NCG		35.7	102°	481 kHz	0.5 mW	0.84 mm²	10 µm
After NCG	100fF	27.6	94.2°	1.50 MHz	0.8 mW	1.39 mm²	10 µm
	330fF		102.3°	1.22 MHz			

If this value is much higher than the output capacitance shown by the amplifier when integrating the NCG, instead of having a smaller positive capacitance, the output node will experience a very high negative capacitance. This means that the capacitance value from the cross-coupling capacitors must be carefully tailored to each amplifier in order to obtain the smallest output capacitance while maintaining a proper phase margin as explained before. In this case, since the amplifier has a high enough phase margin, we can opt to use the NCG with the smaller capacitance, achieving a much higher *GBW*.

4.3.3. Single-ended and Differential Cascode with Bootstrapping

The cascode with bootstrapping structure was adapted from [3]. A single-ended and a differential design were analyzed and simulated, and their schematic and respective small-signal equivalent can be found in Figure 4.11. A differential version was developed to observe the differences from single-ended to differential when applying the NCG, as well as to have to ability to test a more robust structure with increased noise immunity. Regarding the single-ended variant, this structure operates with the transistors M1, M2, and M3 in saturation, where the transistors M4 and M5 are in cut-off due to being in series with a capacitor and high-impedance branches from M2 and M3. The output signal is fed back to M2 and M3 through the feedback circuit created by the capacitors and the bias transistors M4 and M5 [3].

The feedback path can be described through Figure 4.11 (d), where the biasing transistors (M4 or M5) can be described by a parallel combination of the off resistance (R_{off}) with the off capacitance (C_{off}) in series with the capacitor C. The feedback gain (A_f) is kept at a value near 1 and is expressed by:

$$A_f = \frac{v_4}{v_o}, \qquad v_4 = v_o \frac{(R_{off} || \frac{1}{sC_{off}})}{\frac{1}{sC} + (R_{off} || \frac{1}{sC_{off}})} = v_o \frac{1}{1 + \frac{C_{off}}{C}} \tag{4.6}$$

Through the small-signal equivalent circuit the gain of the amplifier is:

$$i_o \approx \frac{g_{ds}^2}{g_m} v_o, \quad R_L = \frac{v_o}{i_o} \approx g_m r_{ds}^2, \quad \frac{v_o}{v_{in}} = -g_m (r_{ds} || g_m r_{ds}^2) \tag{4.7}$$

The equivalent output resistance (R_{eqOut}) and equivalent output capacitance (C_{eqOut}) can be expressed by:

$$R_{eqOut} = r_{01} || R_L, \quad C_{eqOut} \approx C_L + C_{gd1} * (1 - A_1) + C_{gs2} + C//C \tag{4.8}$$

where A_1 is the gain of the transistor M1.

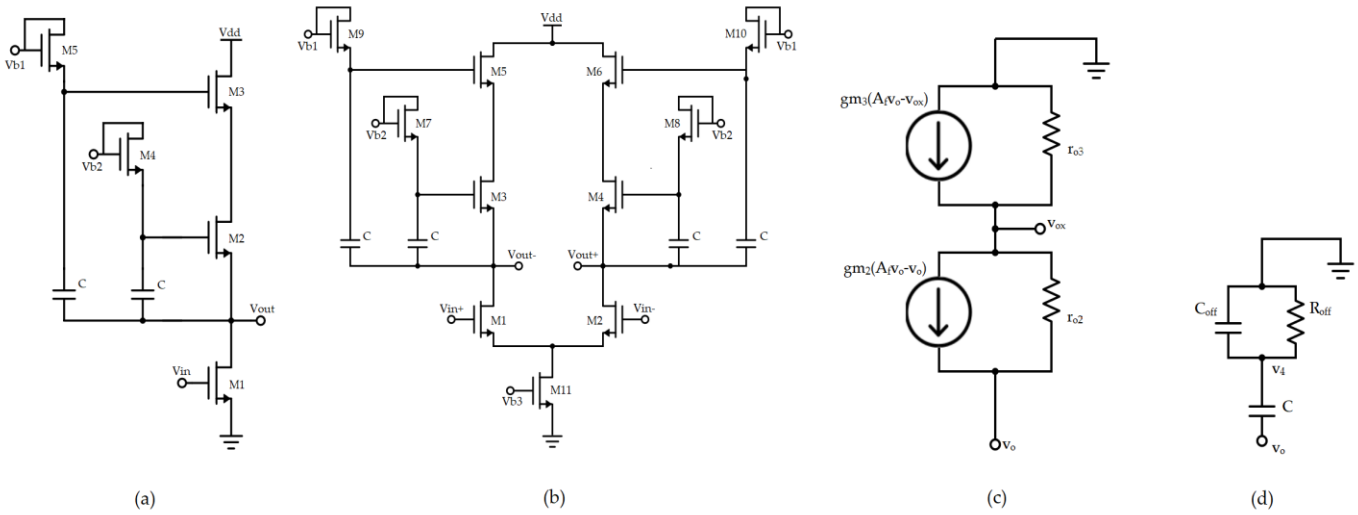

Figure 4.11 - (a) Single-ended and (b) differential cascode with bootstrapping schematic. (c) Single-ended cascode with bootstrapping small-signal equivalent and (d) feedback path schematic.

The final layout of both structures with NCG integration can be found in Figure 4.12.

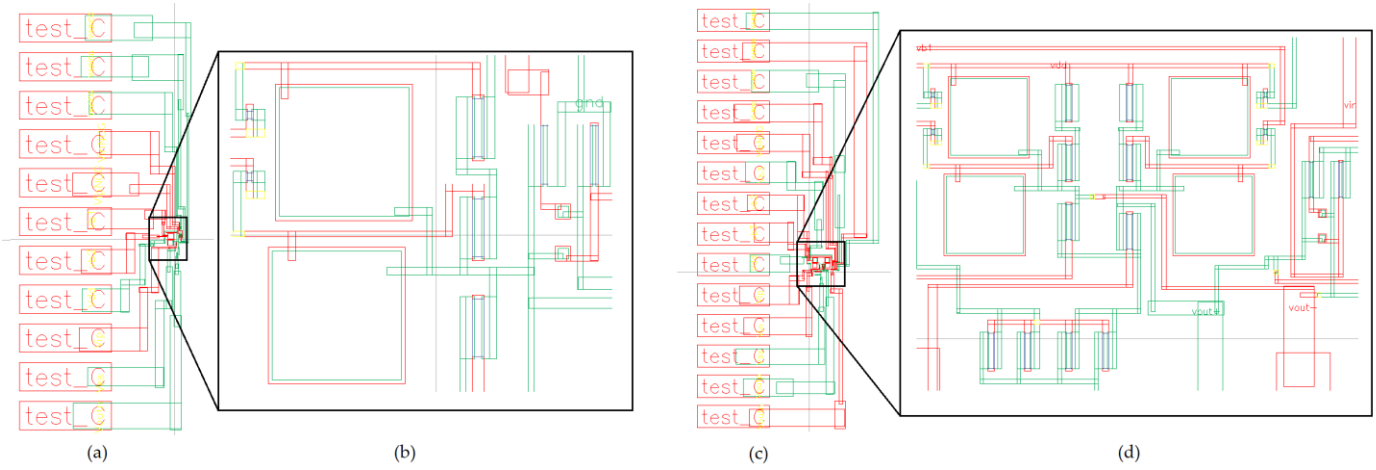

Figure 4.12 - (a) Single-ended cascode with bootstrapping with NCG full layout design with external pads. (b) Amplifier plus NCG detail. (c) Differential cascode with bootstrapping with NCG full layout design with external pads. (b) Amplifier plus NCG detail.

4.3.3.1. Single-ended and differential cascode with bootstrapping frequency response

The obtained curves resulting from the connection of the outputs of the two NCGs to the outputs of the two amplifiers can be seen in Figure 4.13.

The results obtained were as expected. Regarding the single-ended variant of the structure, the gain increases after the integration since the gain of the NCG is 29.6 dB. The same happens for the differential variant, with an NCG gain of 31 dB. In the single-ended structure, the output capacitance is low enough that the NCG with 330fF will generate a much higher output negative capacitance. This way, the output node will be experiencing a higher absolute capacitance than before the integration of the NCG, decreasing the *GBW*. For this, it is advisable to use the 100fF NCG for the single-ended structure. The integration of the NCG in this structure also shifts the first pole to the left, this way the low-frequency value of *GBW* ceases to exist, resulting in better control of the operation of the amplifier at lower frequencies.

In the differential structure, since the output capacitance is larger than the 330fF NCG's negative output capacitance, it is possible to observe positive results regarding f_T. This way it is possible to use the 100fF NCG in both structures. A power supply of 15 V was used for the amplifiers, while the NCG required 17 V. The value of the load resistor in the NCG for correct biasing is 1.2 MΩ for the single-ended structure and 1 MΩ for the differential structure. The achieved positive results can be observed in Table 4.3.

Table 4.3 - Summary of the results obtained from the simulated application of the NCG to the Single-ended and differential cascode with bootstrapping.

			Gain (dB)	Phase Margin	*GBW*	Pwr consumption	Chip area	Min. feature size
Single ended	Before NCG		26.0	68°	Low: 60 Hz High: 3.35 MHz	0.4 mW	0.93 mm²	20 μm
	After NCG	100fF	27.6	65°	3.67 MHz	0.74 mW	1.29 mm²	20 μm - Amp
		330fF		79°	2.29 MHz			10 μm - NCG
Differential	Before NCG		22.5	66.6°	Low: 81 Hz High: 2.26 MHz	0.87 mW	2.69 mm²	20 μm
	After NCG	100fF	26.0	63.4°	3.05 MHz	1.21 mW	3.18 mm²	20 μm - Amp
		330fF		79.8°	2.86 MHz			10 μm - NCG

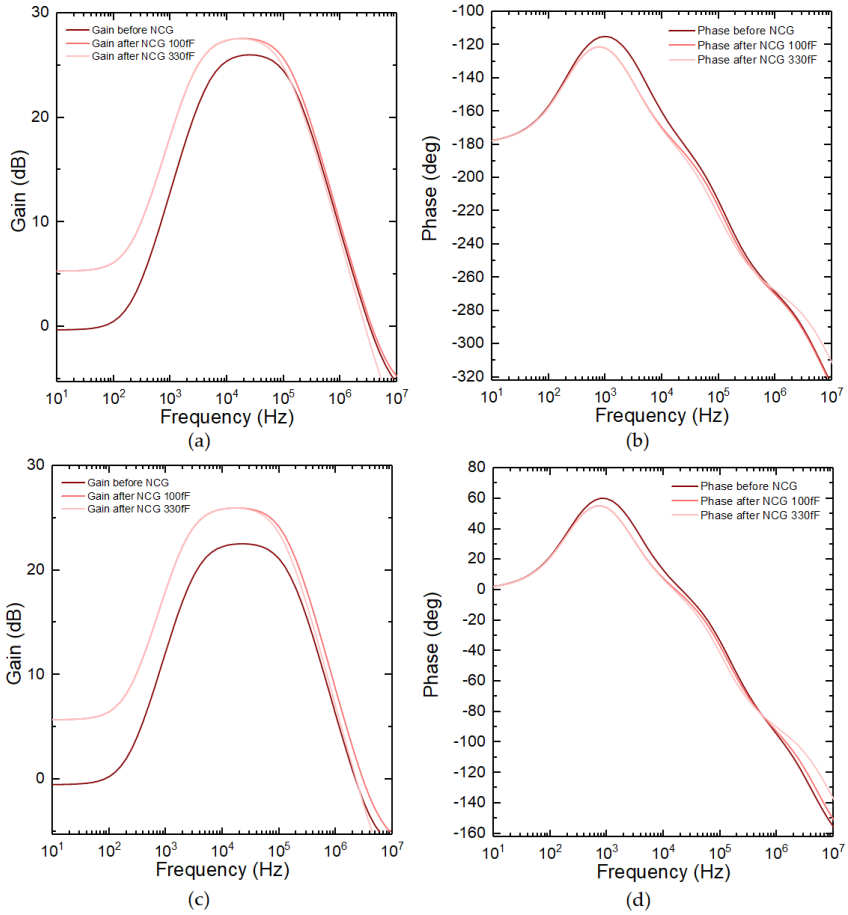

Figure 4.13 - Single-ended cascode with bootstrapping with and without NCG application (a) gain, and (b) phase frequency response plots. Differential cascode with bootstrapping with and without NCG application (c) gain, and (d) phase frequency response plots.

4.3.4. Amplifier Using Bootstrap Gain Enhancement and Common Mode Feedback

This amplifier structure using bootstrap gain enhancement and common-mode feedback (CMFB) has been adapted from a dual-gated pentacene-based OTFT amplifier from [9]. In this block, seen in Figure 4.14, several techniques were used such as bootstrapping of the transimpendance in order to have a higher gain than a diode-connected load, CMFB to increase the tolerance to V_T variations and a differential to single-ended converter stage.

The transistors M1 to M4, M7, and M10 to M13 operate in the saturation region, while M8 and M9 operate in linear mode. The CMFB loop is formed through transistors M8 and M9. The working method of this technique implies that if there is a positive variation in Vout, the current passing through M8 and M9 will increase, which leads to an increase in I_{DS7}. Since I_{DS7}

is the sum of I_{DS1} and I_{DS2} this will lead to an increase in the voltage drop in the load transistors M3 and M4, which will lower Vout as seen in expression, denying the positive variation seen in the beginning. The opposite happens for negative variations of Vout.

$$V_{out} = V_{DD} - V_{GS_{Load}} \tag{4.9}$$

The feedback (A_f) given from the bootstrapping structure is explained through Figure 4.14 (b) and is given by:

$$V_x = \frac{C * V_{out}}{C + C_{DiodeM5}} \Leftrightarrow \frac{V_x}{V_{out}} = \frac{C}{C + C_{DiodeM5}} = A_f \tag{4.10}$$

The amplifying done by this block is also based on g_m cancellation of the load transistors and it can be obtained mathematically through Figure 4.14 (c), where:

$$V_{G3} = V_x - V_{out} = (A_f - 1)V_{out} \tag{4.11}$$

which will result in:

$$\begin{gathered} g_{m1}V_{in} + V_{out}(g_{ds1} + g_{ds3}) + \big(1 - A_f\big)V_{out}g_{m3} = 0 \Leftrightarrow \\ \Leftrightarrow \frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{\big(1 - A_f\big)g_{m3} + g_{ds1} + g_{ds3}} \end{gathered} \tag{4.12}$$

If $A_f \approx 1$ then $g_{m1} \gg g_{ds1} + g_{ds3}$ which will result in high gain. The equivalent output resistance (R_{eqOut}) and equivalent output capacitance (C_{eqOut}) can be expressed by:

$$R_{eqOut} = r_{01} || r_{03}, \quad C_{eqOut} \approx C_L + C_{gd1} * (1 - A_1) + C_{gs3} + C \tag{4.13}$$

where A_1 is the gain of the transistor M1.

The method of operation of the differential to single-ended stage, comprised by the transistors M10 to M13 is given by:

$$\frac{g_{m12}r_{ds10}}{1 + g_{m12}r_{ds10}} * V_{out+} \approx 1 * V_{out+}, \quad V_{out} = V_{out-} - V_{out+} \tag{4.14}$$

due to $g_{m12}r_{ds10} \gg 1$.

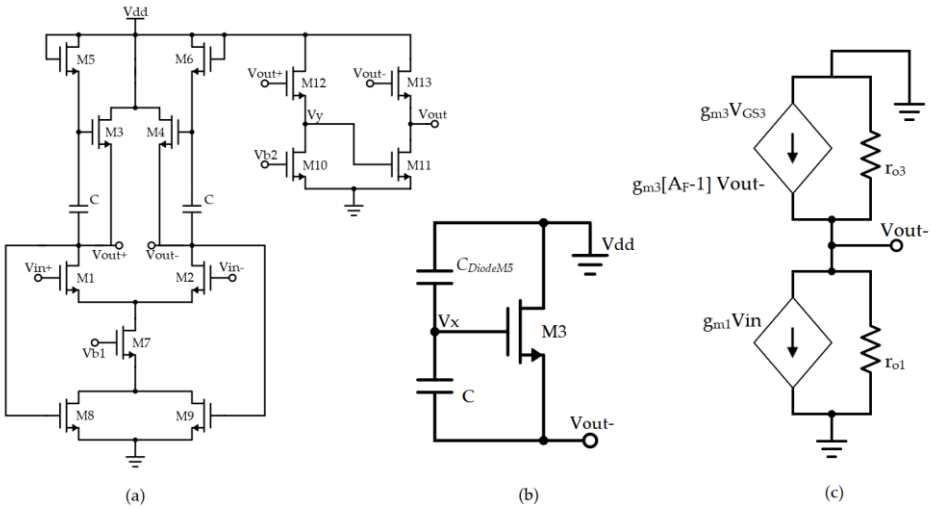

Figure 4.14 - Amplifier using bootstrap gain enhancement and CMFB (a) schematic, (b) feedback path, and (c) small-signal equivalent circuit for the differential output.

The final layout of this structure with NCG integration can be found in Figure 4.15.

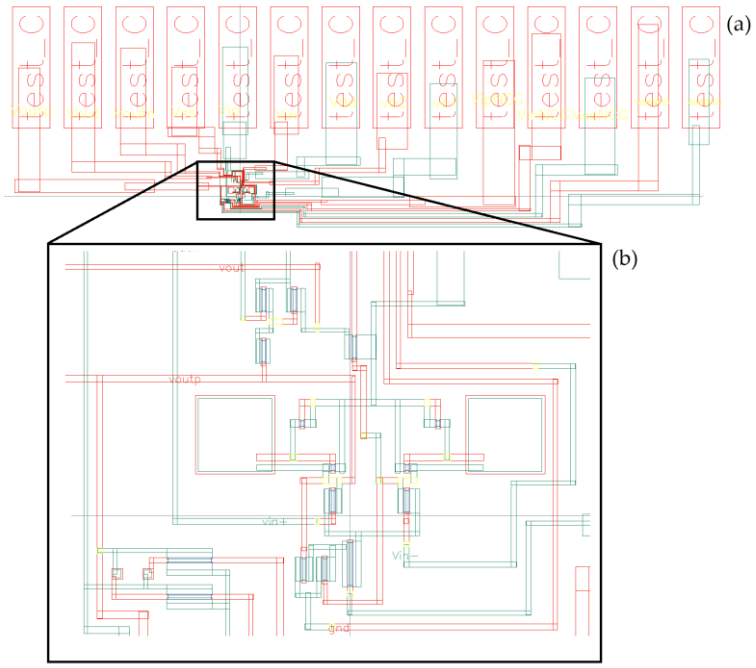

Figure 4.15 - (a) Bootstrap gain enhancement with CMFB based amplifier with NCG full layout design with external pads. (b) Amplifier plus NCG detail.

4.3.4.1. Amplifier using bootstrap gain enhancement and common mode feedback frequency response

The obtained curves resulting from the connection of the outputs of the two NCGs to the outputs of the amplifier can be seen in Figure 4.16.

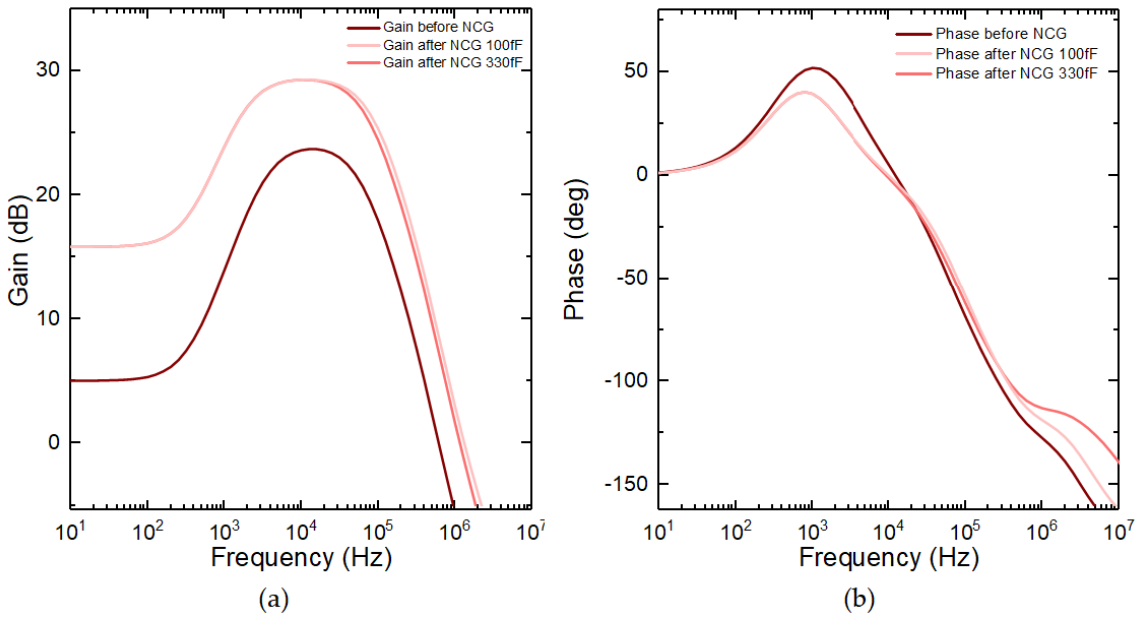

Figure 4.16 - Amplifier using bootstrap gain enhancement and CMFB with and without NCG application (a) gain, and (b) phase frequency response plots.

The gain of the amplifier after the integration increases due to higher NCG gain. As expected, the *GBW* value increases more for the 100fF than for the 330fF cross-coupling capacitors. Since the phase margin of this circuit is 60°, using the 100fF NCG is not advisable since the phase margin after the integration lowers to 58°, creating potential instabilities. However, after fabrication and the introduction of parasitic capacitances, using the 100fF NCG may reveal other results. The phase also behaves as expected. The first pole at the 1 kHz mark is shifted to the left, while the second pole near the 10 kHz mark is shifted to the right, increasing the bandwidth of the circuit. Upon application of the NCG, the *GBW* of the amplifier is increased from 619 kHz to 1.17 MHz for the 330fF NCG and to 1.34 MHz for the 100fF NCG, while increasing power consumption from 0.23 mW to 0.53 and chip area from 2.1 mm^2 to 2.8 mm^2. A 10 V power supply was used for the amplifier, while the NCG required a 15 V power supply.

In this amplifier, the differential outputs of the NCG are connected to the differential outputs of the first stage. If the connection was made to the single-ended stage since it acts as a buffer, the NCG would have no effect and no positive results would be visible, not to be confused with a single-ended application, which has already provided good results as seen in

sub-chapter 4.4.2. before. This way the bootstrapping capacitors and differential stage parasitic capacitances are canceled by the negative capacitance generated, increasing the bandwidth.

Table 4.4 - Summary of the results obtained from the simulated application of the NCG to the amplifier with bootstrapping gain enhancement and CMFB.

		Gain (dB)	Phase Margin	*GBW*	Pwr consumption	Chip area	Min. feature size
Before NCG		23.7	60.0°	619 kHz	0.23 mW	2.1 mm²	10 µm
After NCG	100fF	29.3	58.3°	1.34 MHz	0.53 mW	2.8 mm²	10 µm
	330fF		66.5°	1.17 MHz			

4.3.5. Pseudo CMOS Based Amplifier

The pseudo-CMOS based amplifier has been adapted from [4]. This structure, seen in Figure 4.17 (a) uses a pseudo-CMOS inverter as a load for the transistors M1 and M2. Its method of operation is essentially the same as the positive feedback-based amplifier and the bootstrap gain enhancement with CMFB amplifier, as it is also based in g_m cancellation of M4. The higher load impedance provided by the pseudo-CMOS configuration will provide a higher open-loop gain than a simple diode-connected load inverter. After several simulations, it was found that the best results in denying the output capacitance would be obtained if the outputs of the NCG were connected to the output of the second stage.

Assuming V_x is a multiplier of the feedback gain obtained from the circuit formed by M1, M6 and M3 then the expression for the gain of the first stage is:

$$\frac{Vy}{Vin} = A_V = \frac{-g_{m2}}{(1 - A_f)g_{m4} + g_{ds2} + g_{ds4}} \tag{4.15}$$

When ensuring that $A_f \approx 1$, and if $g_m \gg g_{ds}$ then the gain will be mainly dependent on the transconductance of M2.

The equivalent output resistance (R_{eqOut}) and equivalent output capacitance (C_{eqOut}) can be expressed by:

$$R_{eqOut} = r_{012} || r_{013}, \quad C_{eqOut} \approx C_L + C_{gd13} * (1 - A_{13}) + C_{gs12} \tag{4.16}$$

where A_{13} is the gain of M13.

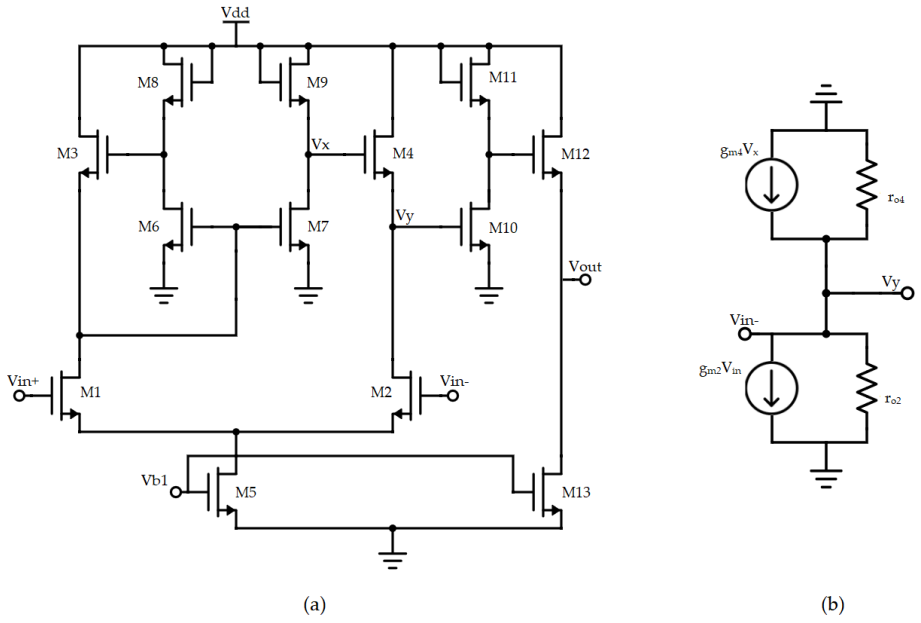

Figure 4.17 - Pseudo-CMOS based amplifier (a) schematic and (b) small-signal equivalent circuit for the first stage output.

The final layout of the structure can be found in Figure 4.18.

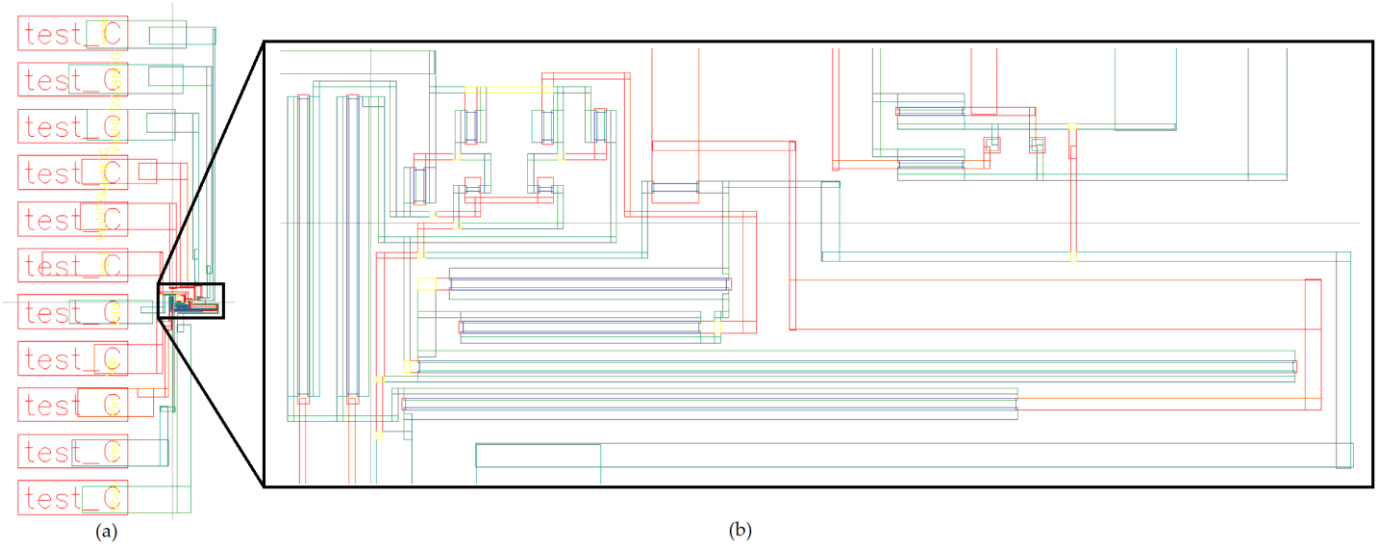

Figure 4.18 - (a) Pseudo-CMOS based amplifier with NCG full layout design with external pads. (b) Amplifier plus NCG detail.

4.3.5.1. Pseudo CMOS frequency response

The obtained curves resulting from the connection of the outputs of the two NCGs to the outputs of the amplifier can be seen in Figure 4.19.

The gain of the amplifier increases as expected upon the integration of the NCG, since it displayed a greater gain. Regarding f_T, the increase happens as expected, as the 100fF NCG provides a greater increase in f_T in comparison to the 330fF NCG. The phase curve in this amplifier sees a change when comparing the different sizes of cross-coupling capacitors as the 330fF NCG. The pole is shifted more to the right because there is the use of a smaller 100fF cross-coupling capacitance, as mentioned before.

This pole, however, is accompanied by a zero to its right that when shifted to the right by the 100fF NCG is affected by two poles, which doesn't happen in application of the 330fF NCG, since the zero that accompanies the pole moves far away enough from its base position, but not far enough as the 100fF NCG to go unnoticed. This causes what can be seen around the 1 MHz mark in the phase frequency response plot of the application of the 330fF NCG.

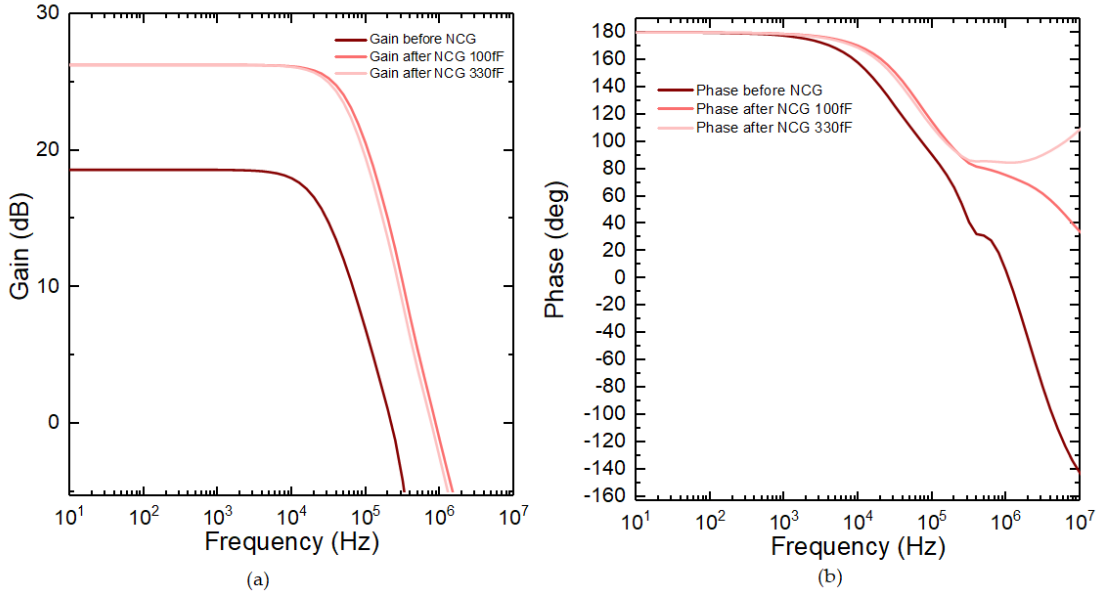

Figure 4.19 - Pseudo-CMOS based amplifier with and without NCG application (a) gain, and (b) phase frequency response plots.

Table 4.5 - Summary of the results obtained from the simulated application of the NCG to the Pseudo-CMOS based amplifier.

		Gain (dB)	Phase Margin	*GBW*	Pwr consumption	Chip area	Min. feature size
Before NCG		18.6	118°	223 kHz	1.6 mW	1.97 mm²	10 µm
After NCG	100fF	26.3	95°	892 kHz	1.8 mW	2.60 mm²	10 µm
	330fF		77°	775 kHz			

5 Conclusions and Future Perspectives

The work done for this dissertation had the main focus on increasing the frequency of operation of a-IGZO based amplifier structures, without changing any of the device's intrinsic properties. This was achieved using negative Miller capacitance compensation.

First, there was the need to fully understand the Miller's theorem, and how it was possible to generate a negative capacitance. This was first tested in standard 130 nm CMOS models that have been broadly studied and therefore are much more accurate. This provided a basis in how the application of a negative capacitance worked in several simple amplifier blocks, and what it was to be expected when a-IGZO TFTs were used. To generate a negative capacitance there is a need for a feedback capacitor connected around a non-inverting amplifier with gain $A \gg 1$, for this a simple differential amplifier with cross-coupling capacitances was used. The cross-coupling capacitors dictate how much negative capacitance is generated, as well as the load resistor since the equivalent output capacitance varies is multiplied by the gain of the structure.

In a CMOS based single-ended cascode with bootstrapping, an increase of 59% in the value of *GBW*, from 67.2 MHz to 106.8 MHz was obtained with a minimal impact on power consumption and chip area. The final gain obtained is dependent on the gain of the NCG, although this gain can be controlled through higher or lesser power supplies.

In a-IGZO TFT technology, five different amplifiers were tested with and without the application of the NCG, the obtained results before and after the application of the NCG compared with state-of-the-art literature can be seen in Table 5.1. It is possible to see how the unity current gain frequency increases for each different amplifier when the output capacitance is denied by the applied negative capacitance. Some amplifiers, such as the positive feedback amplifier report 200% increases in the *GBW* value, while other amplifiers that show a higher base *GBW* don't report such a high increase due to the effectiveness of the NCG at higher frequencies. The gain of the NCG is fixed due to the need to have a matching bias with the amplifier, however, this can be changed by increasing the power supply of the NCG.

It is expected that these structures when fabricated will report a smaller *GBW* when compared to the simulations, due to all the parasitic components that are related to the fabri-

cation of circuits, such as parasitic capacitances resulting from the overlap of different metallization layers. This also impacts the performance of the NCG as proved before, as higher parasitic capacitances will decrease its impact on the amplifier performance.

Table 5.1 – State of the art, and simulation values before and after NCG comparison for the different amplifiers. State of the art examples include output loads and are fabricated circuits. (a) Positive feedback differential amplifier. (b) Single-ended cascode w/ bootstrapping. (c) Differential cascode w/ bootstrapping. (d) Amplifier using bootstrap gain enhancement and CMFB. (e) Pseudo-CMOS based amplifier.

	(a)			(b)			(c)		(d)		(e)		
	w/o NCG	w/ NCG	[2]	w/o NCG	w/ NCG	[3]	w/o NCG	w/ NCG	w/o NCG	w/ NCG	w/o NCG	w/ NCG	[4]
GBW (MHz)	0.48	1.50	0.20	3.35	3.67	0.02	2.26	3.05	0.62	1.17	0.22	0.89	0.03
Gain (dB)	35.7	26.7	10.0	26.0	27.6	22.0	22.5	26.0	23.7	29.3	18.6	26.3	22.5
Phase Margin (°)	102	94	X	68	65	X	67	63	60	67	118	95	X

State of the art results tends to have smaller *GBW* due to being fabricated real-world circuits and including large output impedance loads. Taking these results into account, using this technique can result in very high increases in *GBW* while not tampering with the inner structure of the a-IGZO TFT. This means that employing this technique can be extremely favorable in the future of amorphous oxide TFT based structures, as an intrinsic disadvantage of it can be denied by the simple use of a negative capacitance generator. Considering that this is a flexible technology with enormous potential, this increase in *GBW* can be useful for a plethora of applications such as low-cost RFID and biomedical devices and apparel, flexible displays or any type of circuit employing AOS TFTs that relies on its frequency of operation.

Further tests need to be conducted in order to prove its efficiency in real-world applications, as well as if this technique can be applied in the various nodes of the amplifiers instead of just the output. New techniques can be used for the negative capacitance generation such as the use of different NCG as seen in Figure 4.2, in order, as these have been studied for CMOS technology, and its benefits can be of good use in TFT applications.

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A Cadence Virtuoso Schematics

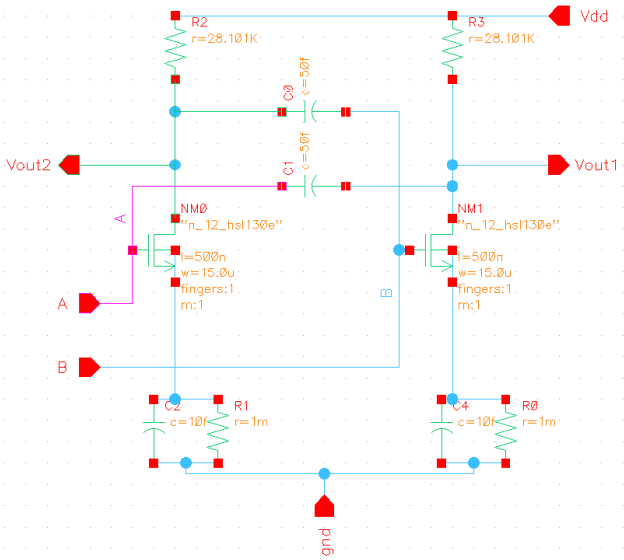

Figure A.1 - NCG schematic using MOSFETs.

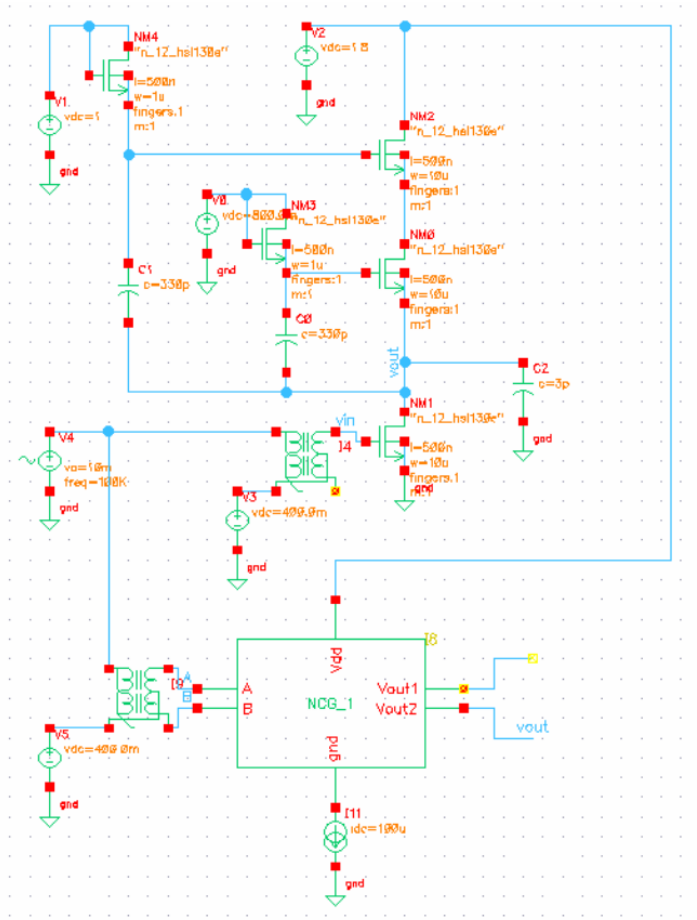

Figure A.2 - Single-ended cascode with bootstrapping schematic with NCG, using MOSFETs.

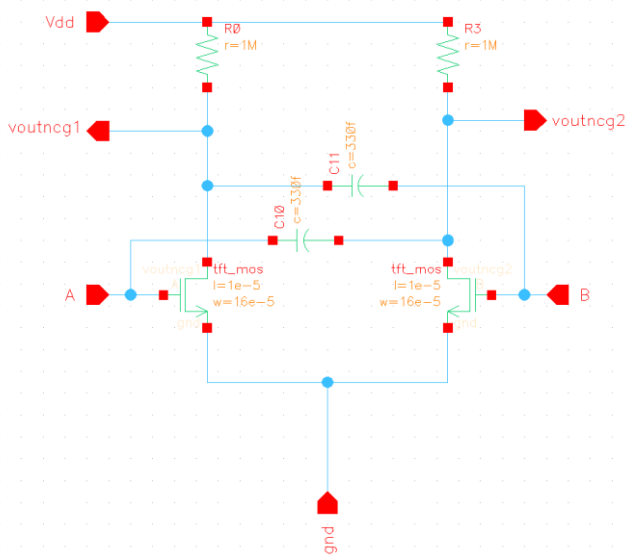

Figure A.3 - NCG schematic using a-IGZO TFTs.

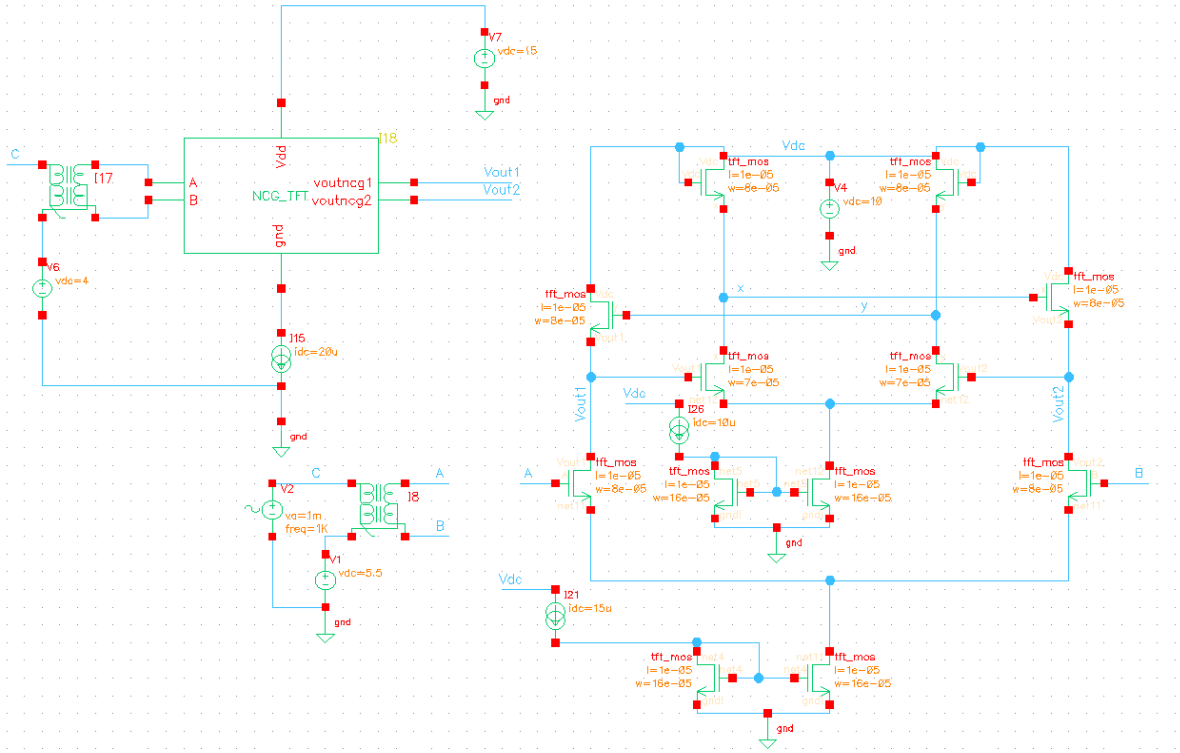

Figure A.4 - Positive feedback based amplifier schematic using a-IGZO TFTs.

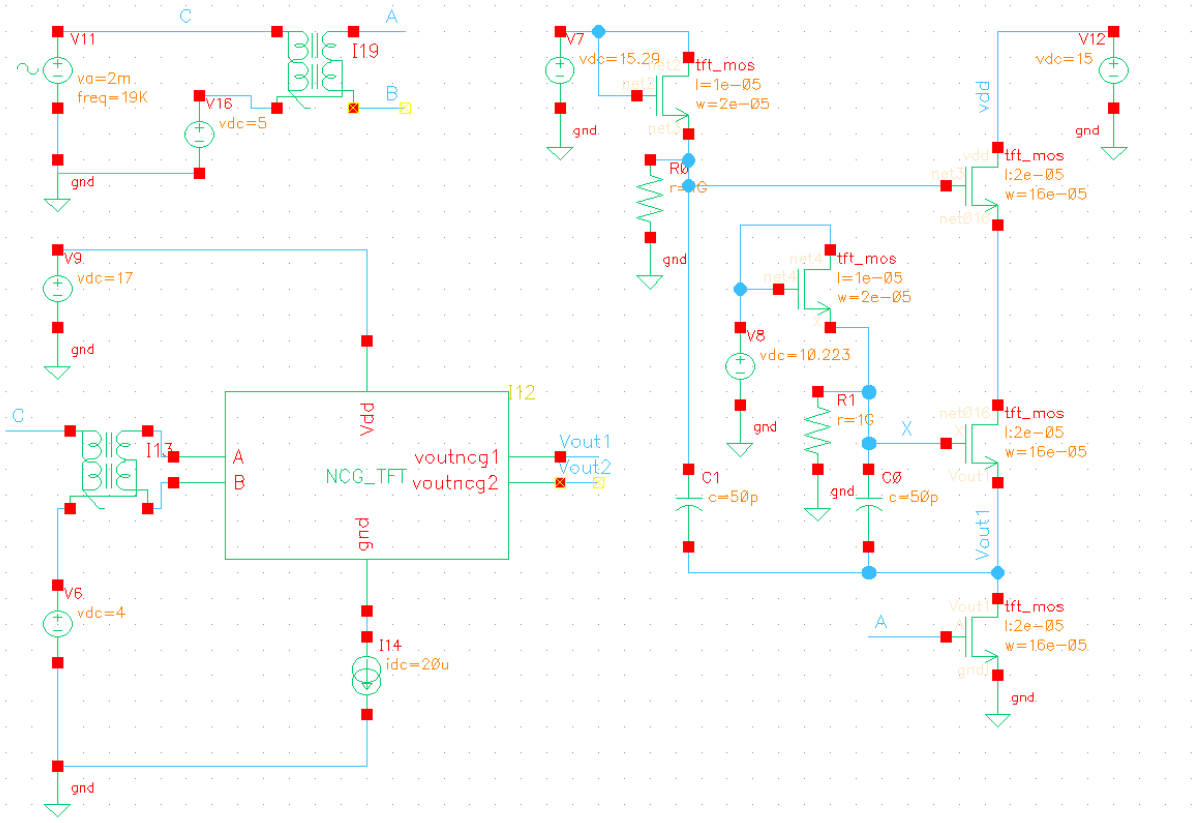

Figure A.5 - Single-ended cascode with bootstrapping schematic using a-IGZO TFTs.

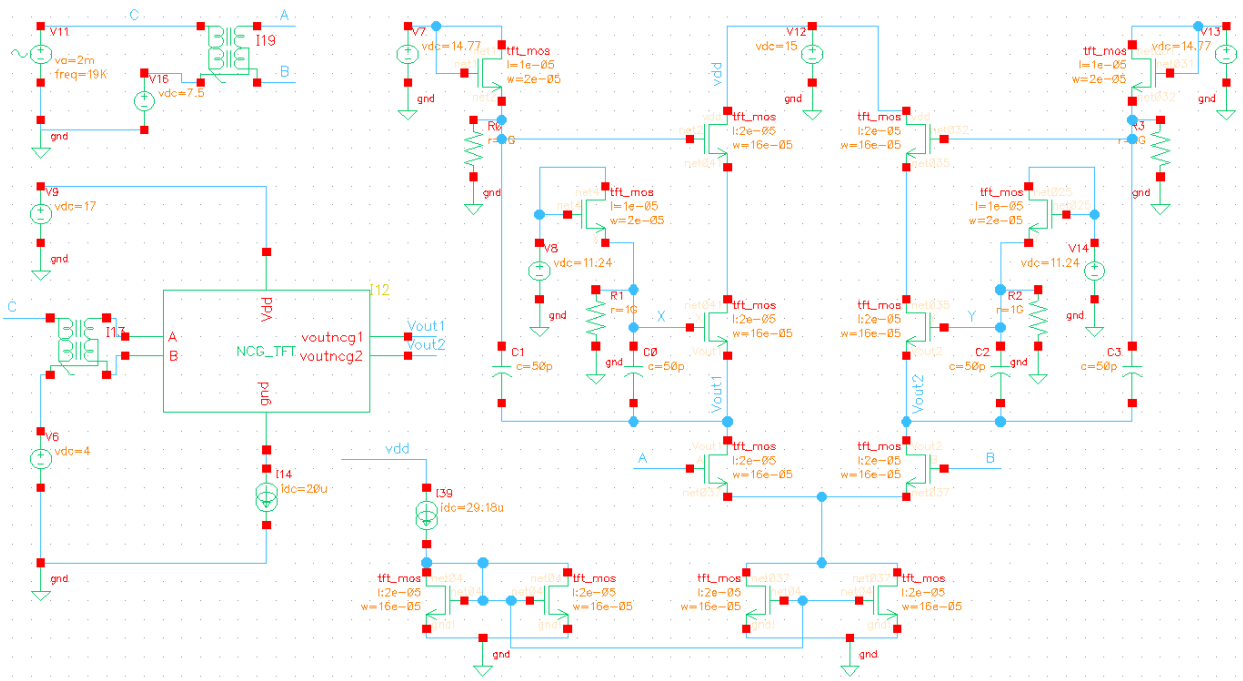

Figure A.6 - Differential cascode with bootstrapping schematic using a-IGZO TFTs.

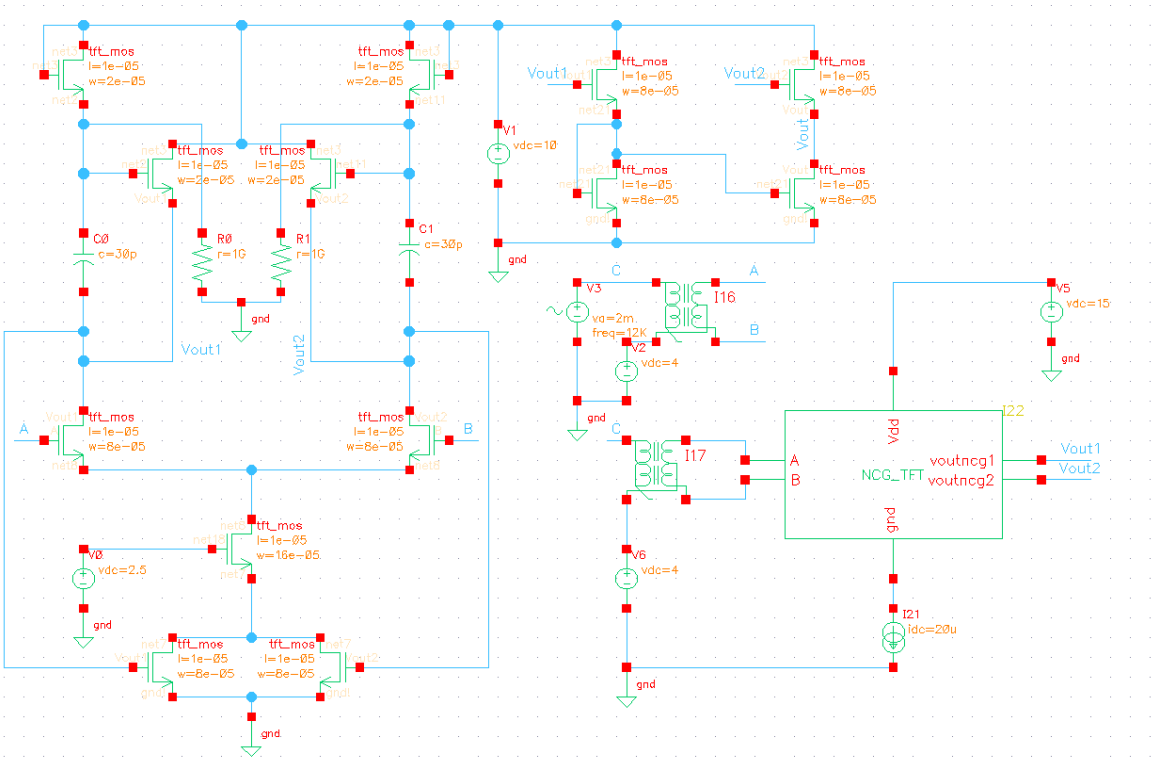

Figure A.7 - Gain enhacement with common-mode feedback amplifier using a-IGZO TFTs.

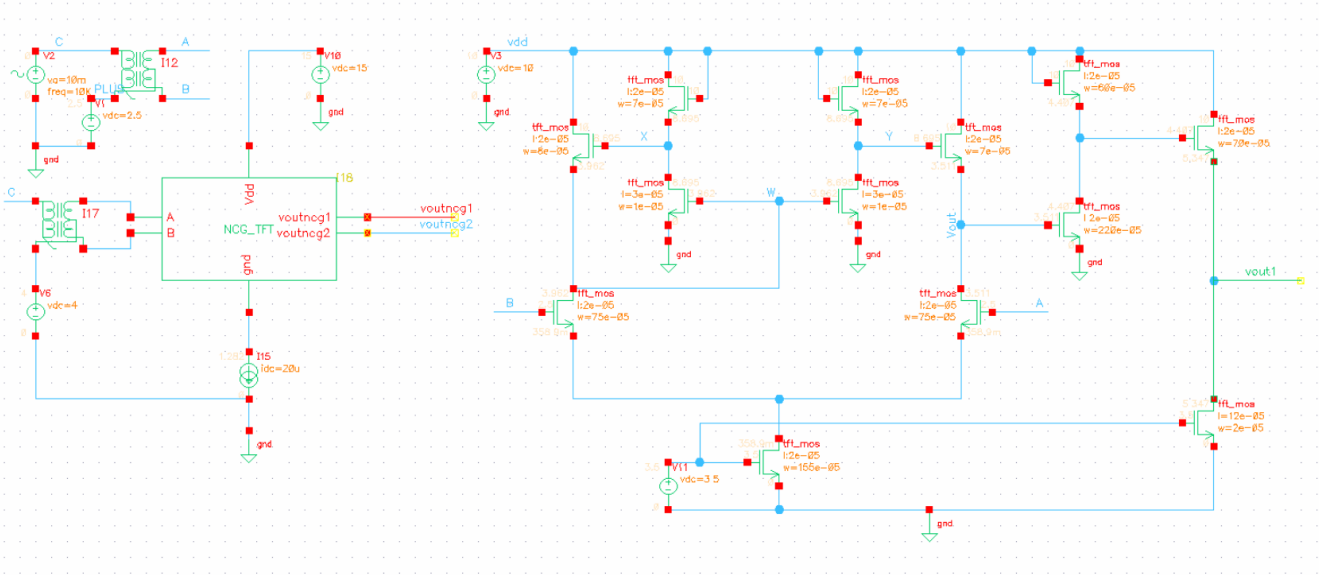

Figure A.8 - Pseudo-CMOS based amplifier using a-IGZO TFTs.

B Component Dimensions

Table B.1 – Different component dimensions for the a-IGZO NCG and the different amplifiers.

	Transistors	Width	Length	NCG Load Resistor value	Transistor Count
Negative Capacitance Generator	M1, M2	160 µm	10 µm	//////////////	2
Positive Feedback Differential Amplifier	M1, M2, M3, M4, M8, M9	80 µm	10 µm	1.0134 MΩ	10
	M6, M7	70 µm	10 µm		
	M10, M5	160 µm	10 µm		
Cascode with bootstrapping single-ended	M1,M2,M3	160 µm	20 µm	1.2 MΩ	5
	M4, M5	20 µm	10 µm		
Cascode with bootstrapping differential	M1, M2, M3, M4, M5, M6	160 µm	20 µm	1 MΩ	14
	M7, M8, M9, M10	20 µm	10 µm		
Gain Enhancement with CMFB	M1, M2, M8, M9, M10, M11, M12, M13	80 µm	10 µm	916.3 kΩ	13
	M3, M4, M5, M6	20 µm	10 µm		
	M7	160 µm	10 µm		
Pseudo CMOS	M1, M2	750 µm	20 µm	965.3 kΩ	13
	M3	80 µm	20 µm		
	M4, M8, M9	70 µm	20 µm		
	M5	1550 µm	20 µm		
	M6, M7	10 µm	30 µm		
	M10	2220 µm	20 µm		
	M11	600 µm	20 µm		
	M12	700 µm	20 µm		
	M13	20 µm	120 µm		