NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF MATERIALS SCIENCE

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SELF-ALIGNED AND SUB-µm OXIDE TFTS: TCAD SIMULATION AND FABRICATION

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“I didn’t fail 1,000 times. The light bulb was an invention with 1,000 steps.”
- Thomas Edison

Abstract

Amorphous indium gallium oxide (a-IGZO) thin-film transistors (TFTs) have seen extensive research and applications over the past years. The application of these devices in high-speed circuitry is yet to be optimised since these still suffer from large channel lengths (L), overlap capacitances, and contact resistances. In this study, the use of self-aligned (SA) and sub-µm a-IGZO TFTs is proposed and explored.

The first part of this work encompasses a comprehensive technology computer-aided design (TCAD) study of three different device structures, by exploring the aforementioned effects. It was found that SA top-gate homojunction (with doped source/drain areas) TFTs result in the best electrical performance, due to neglectable parasitic capacitances and high-quality semiconductor/metal interfaces. Corbino TFTs with outer electrode as drain configuration exhibit infinite output resistance, which is ideal for amplifier applications. In the scope of SA top-gate TFT fabrication, a method of doping a-IGZO with Ar plasma was established, resulting in sheet resistances of 639 Ω/□. After optimizing lithographic processes, devices with $L = 0.6$ µm were fabricated by direct laser writing (DLW). Although it was not possible to attain fully functional miniaturized a-IGZO TFTs, similar processes yielded devices with field-effect mobility of 7.6 cm^2/V.s and transit frequency of 0.19 MHz for $L = 40$ µm. Fabricated TFTs exhibited hump-like transfer characteristics, attributed to edge effects, back-channel conduction, or shallow donor states in a-IGZO

Keywords: a-IGZO, channel length, DLW, self-aligned, high frequency

Resumo

Transístores de filme fino (TFT) de oxido de índio-gálio-zinco (a-IGZO) têm sido extensamente investigados nos últimos anos. Contudo, ainda não são aplicados a circuitos de altas frequências pois a sua frequência de operação é significativamente limitada por elevadas resistência de contacto, capacidades parasitas e canais longos. Neste trabalho, configurações de TFT auto-alinhadas com tamanhos de canal submicrométricos serão exploradas.

A primeira parte deste trabalho engloba o estudo de três estruturas de TFT diferentes por *technology computer-aided design* (TCAD), explorando a minimização dos efeitos acima enunciados. TFTs de estrutura auto-alinhada *top-gate* com semicondutor dopado nas zonas de fonte e dreno apresentam a melhor performance estática e dinâmica, devido ao efeito negligenciável das capacidades de sobreposição e à melhor interface entre o semiconductor e o metal de fonte e dreno. TFTs Corbino apresentam resistência de saída infinita quando o elétrodo exterior é polarizado como o dreno, o que é bastante vantajoso para aplicações em amplificadores. Para o fabrico de TFTs auto-alinhados foi estabelecido um método para dopar a-IGZO com plasma de Ar, resultando em resistências folha de 639 Ω/□. Após otimização dos processos fotolitográficos usando escrita direta por laser obtiveram-se comprimentos de canal (L) de 0.6 µm. Embora não tenha ainda sido possível obter dispositivos miniaturizados funcionais, processos similares em TFTs com $L = 40$ µm resultaram em mobilidades de feito de campo de 7.6 $cm^2/(V.s)$ e frequências de trânsito de 0.19 MHz. Os dispositivos apresentaram características de transferência com um perfil de bossa, efeito atribuído a TFTs parasitas, condução pela parte posterior do canal ou estados dadores superficiais no a-IGZO.

Palavras-chave: a-IGZO, tamanho de canal, DLW, auto-alinhado, alta frequência

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Acronyms

2D	Two Dimensional
3D	Three Dimensional
ADL	Atomic Layer Deposition
a-IGZO	Amorphous Indium Gallium Zinc Oxide
AOS	Amorphous Oxide Semiconductors
BG	Bottom Gate
BF	Butterfly-type TFTs
BUV	Backside UV
CAD	Computer-Aided Design
C-f	Capacitance-Frequency
CLM	Channel Length Modulation
C-V	Capacitance-Voltage
CVD	Chemical Vapor Deposition
CWM	Channel Width Modulation
DI	Deionized
DLW	Direct Laser Writing
DUV	Deep Ultra Violet
EBL	Electron-Beam Lithography
EDS	Energy Dispersive X-Ray Spectroscopy
EUV	Extreme Ultra Violet
FIB	Focused Ion-Beam
GD	Gate Dielectric
IE	Inner electrode (Corbino TFTs)
IoT	Internet of Things
IPA	Isopropyl Alcohol
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OE	Outer Electrode (Corbino TFTs)
PEB	Post-Exposure Bake
PET	Polyethylene Terephthalate

PI	Polyamide
PR	Photoresist
QVTFT	Quasi-Vertical Thin-Film Transistor
R&D	Research and Development
RC	Rectangle-type TFTs
S/D	Source/Drain
SA	Self-Aligned
STG	Staggered
TCAD	Technology Computer-Aided Design
TFT	Thin-Film Transistor
TG	Top Gate
TLM	Transmission Line Method
UV	Ultraviolet
VLSI	Very Large-Scale Integration
VTFT	Vertical Thin-Film Transistor

Symbols

$A_{\mathrm{ov\ total}}$	Total overlap area
C_{GD}	Gate-to-drain capacitance
C_{GS}	Gate-to-source capacitance
C_{OFF}	OFF-state capacitance
C_{ON}	ON state capacitance
C_{P}	Parasitic capacitance
C_{ch}	Channel capacitance
C_{ov}	Overlap Capacitance
C_{ox}	Transistor's capacitance per unit area
E_{G}	Band gap
E_{GD}	Energy that corresponds to the Gaussian distribution peak for donor-like states
$I_{\mathrm{DS\ lin}}$	Drain-to-source current in the linear regime
$I_{\mathrm{DS\ max}}$	Maximum drain-to-source current
$I_{\mathrm{DS\ sat}}$	Drain-to-source current in the saturation regime
I_{DS}	Drain-to-source current
L_{eff}	Effective channel length
L_{min}	Minimum channel length
L_{ov}	Overlap length
N_{C}	Density of states in the conduction band
N_{D}	Donor carrier concentration
N_{GA}	Total density of acceptor-like states in a Gaussian distribution
N_{GD}	Total density of donor-like states in a Gaussian distribution
N_{TA}	Density of acceptor-like states in the tail distribution at the conduction band edge
N_{TD}	Density of donor-like states in the tail distribution at the valence band edge
N_{V}	Density of states in the valence band
R_{A}	Access resistance
R_{C}	Contact resistance
R_{G}	Gate resistance
R_{S}	Source resistance
R_{T}	Total resistance

R_1	Inner radius (Corbino TFTs)
R_2	Outer radius (Corbino TFTs)
T_{max}	Maximum processing temperature
V_{GS}	Gate-to-source voltage
V_O	Oxygen vacancies
V_{TH}	Threshold voltage
W_{GD}	Characteristic decay energy for a Gaussian distribution of donor-like states
W_{TA}	Characteristic decay energy for the tail distribution of acceptor-like states
W_{TD}	Characteristic decay energy for the tail distribution of donor-like states
W_{eff}	Effective channel width
X_1	Misalignment margin
f_T	Transit frequency
$f_{T\,max}$	Maximum transit frequency
g_{ds}	Drain-to-source conductance
r_{DS}	Drain-to-source resistance
r_{ch}	Channel resistance
ε_r	Dielectric constant/Relative dielectric permittivity
$\mu_{FE\,max}$	Maximum field-effect mobility
μ_{FE}	Field-effect mobility
μ_H	Hall mobility
μ_{SAT}	Saturation mobility
μ_{eff}	Effective saturation mobility
μ_n	Electron mobility
μ_p	Hole mobility
σ_T	Cross-section carrier capture.
ϕ_{Gate}	Gate work function
ϕ_{Mo}	Molybdenum work function
$\phi_{S/D}$	Source/drain work function
ΔL	Channel Shortening Factor
K	Thermal conductivity
L	Channel length

$\boldsymbol{SS}$	Subthreshold swing
$\boldsymbol{T}$	Temperature
$\boldsymbol{W}$	Channel width
$\boldsymbol{gm_{SAT}}$	Saturation transistor transconductance
$\boldsymbol{\lambda}$	Channel length modulation factor
$\boldsymbol{\mu}$	Mobility
$\boldsymbol{\rho}$	Resistivity
$\boldsymbol{\chi}$	Electron affinity

1. Motivation and objectives

Oxide thin-film transistors (TFTs) have been successfully employed as flat-panel display backplanes for the past few years. However, there are far more applications of oxide TFTs, such as Internet of Things (IoT) and the implementation on large-area flexible circuitry. In fact, over the years, both digital and analog building blocks have been shown in flexible substrates using oxide TFTs [1]. Operating frequencies are limited to the kHz regime as a consequence of the relatively low mobilities of these metal oxides, usually large channel length (L) and large overlap capacitances (C_{ov}) [1,2]. A significant rise in mobility (μ) would imply opting for other semiconductors, such as poly-Si, trading-off large-area and flexible substrate compatibility [3]. However, the latter limitations can be overcome by device structure, process optimization, and improved lithographic tools [1,4].

An interesting lithography process to study different TFT architectures and explore sub-µm channel lengths is Direct Laser Writing (DLW). DLW is a lithographic technique that can deliver very small feature sizes without the complexity of more advanced photolithography systems. Also, the avoidance of photomasks and the versatility of this technique are key advantages for research and development (R&D) purposes.

The purpose of this thesis is to improve the operating frequency of amorphous indium-gallium-zinc oxide (a-IGZO) TFTs. Two different routes will be taken simultaneously, ultimately aiming for this same objective. This work is going to explore the fabrication of devices with micrometric and even sub-micrometric L via DLW while concurrently employing self-aligned (SA) device architectures to decrease C_{ov}. Both of these approaches together are expected to improve a-IGZO TFTs' AC performance.

The first part of this study is based on technology computer-aided design (TCAD) simulations of different TFT device structures to infer their electrical metrics. Following that, a process to dope a-IGZO after deposition is explored, in the scope of the implementation of SA top-gate (TG) TFTs. Next, every step of the fabrication process is optimized to achieve micrometric lengths via DLW, from layout design to tailoring DLW conditions and lithographic process. The ideal doping conditions and the optimized fabrication process are then utilized for the fabrication of the SA TG devices.

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2. Introduction

Oxide TFTs have seen a lot of interest both from academia and industry over the past 20 years, with major companies already integrating this technology in display backplanes, for example. However, advances in oxide TFTs are still essential to achieve high-performing, low-cost, transparent, and flexible electronics.

In this section, introductory context will be given, focusing on TFTs' operating principle, the major limitations of this technology in the scope of high-speed applications, and ways to overcome them. An insight on DLW, the central fabrication technique of this thesis will also be given. The chapter ends with a brief introduction of TCAD tools for oxide TFT simulation.

2.1. Thin-film transistors (TFTs)

TFTs are in the family of field-effect transistors, so its operating principle is much alike the metal-oxide-semiconductor field-effect transistor (MOSFET). However, unlike MOSFETs, TFTs can be built in any type of insulating substrate, as long as it can endure all the fabrication steps. TFTs are composed of three electrodes – gate, drain, and source. In between drain and source, a semiconductor layer is placed, and a dielectric layer is placed between the semiconductor and the gate electrode [3].

2.1.1. TFTs operating principle

The basic operation principle relies on the modulation of the current flowing through source and drain terminals (I_{DS}) by capacitive injection of carriers close to the semiconductor/dielectric interface, which is achieved by applying a potential difference between gate and source electrodes (V_{GS}) [1,3].

Considering an n-type semiconductor, devices can be defined as working in enhancement or depletion mode, depending on whether the threshold voltage (V_{TH}) is positive or negative, respectively. It is important to note that devices working in enhancement mode minimize power dissipation and simplify circuit design, so these are generally preferred [3,5].

The device is considered OFF if $V_{\mathrm{GS}} << V_{\mathrm{TH}}$, so little to no I_{DS} flows. Contrarily, if $V_{\mathrm{GS}} > V_{\mathrm{TH}}$, the device is considered ON due to charge accumulation in the semiconductor near the semiconductor/dielectric interface, forming a conductive path between source and drain – the channel. Depending on the potential difference between source and drain (V_{DS}) it is possible to differentiate three distinct operating regions. If $V_{\mathrm{DS}} < V_{\mathrm{GS}} - V_{\mathrm{TH}}$ the device is said to be working on the triode regime and $I_{\mathrm{DS\,tri}}$ is defined by (1), where W corresponds to channel width, L is channel length (distance between drain and source), μ_{FE} is field-effect mobility and C_{ox} is the gate dielectric (GD) capacitance per unit area. If $V_{\mathrm{DS}} \ll V_{\mathrm{GS}} - V_{\mathrm{TH}}$, the device is said to be in its linear regime and the $V_{\mathrm{DS}}/2$ term is neglectable, so $I_{\mathrm{DS\,lin}}$ is given by (1.1) [1,5].

$$I_{\mathrm{DS\,tri}} = \frac{W}{L}\mu_{\mathrm{FE}}C_{\mathrm{ox}}\left(V_{\mathrm{GS}} - V_{\mathrm{TH}} - \frac{V_{\mathrm{DS}}}{2}\right)V_{\mathrm{DS}} \tag{1}$$

$$I_{\mathrm{DS\,lin}} = \frac{W}{L}\mu_{\mathrm{FE}}C_{\mathrm{ox}}(V_{\mathrm{GS}} - V_{\mathrm{TH}})V_{\mathrm{DS}} \tag{1.1}$$

The third regime is named saturation mode and takes place when $V_{\mathrm{DS}} > V_{\mathrm{GS}} - V_{\mathrm{TH}}$. $I_{\mathrm{DS\,sat}}$ is defined by (2) [1]. μ_{SAT} is the saturation mobility.

$$I_{\mathrm{DS\,sat}} = \frac{W}{2L}\mu_{\mathrm{SAT}}C_{\mathrm{ox}}(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 \tag{2}$$

In short-channel devices, for higher values of V_{DS}, equation (2) needs to be modified to accommodate for a non-ideal effect which causes the shortening of the channel length by ΔL – the so-called channel length modulation (CLM). The effective channel length (L_{eff}) is given by $L_{\mathrm{eff}} = L - \Delta L$. For these conditions, (2) becomes (3), where λ is the CLM parameter. λ is inversely proportional to L, being significantly more relevant

as devices scale down [1].

$$I_{\mathrm{DS\,sat}} = \frac{W}{2L}\mu_{\mathrm{SAT}}C_{\mathrm{ox}}(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2(1 + \lambda V_{\mathrm{DS}}) \quad (3)$$

2.1.2. Short channel and self-aligned a-IGZO TFTs

In MOSFETs, high-speed operations have been enabled mainly due to device miniaturization, i.e. a decrease in L. This not only allows for higher operation frequencies but also for lower power consumption and very-large-scale integration (VLSI) [6]. Although the lithographic tools exist for fabricating TFTs with very short L, this technology faces other problems that are discussed in this section.

2.1.3. Parasitic effects on TFT technology and transit frequency

While static performances of oxide TFTs have been intensively researched and reported, there is still a lack of reports concerning the AC performance of these devices. Understanding and improving AC metrics is vital to ensure high-frequency oxide TFTs. On this matter, it is both relevant and helpful to resource to the TFT small-signal equivalent circuit, shown in Figure 1. R_{G}, R_{D}, R_{S} correspond to the gate, drain and source resistance, respectively, while r_{DS} is the output resistance ($g_{\mathrm{DS}} = \frac{1}{r_{\mathrm{DS}}}$ is the device's conductance). C_{GS} and C_{GD} are source/drain (S/D) to gate parasitic capacitances (C_{P}), respectively, and g_{m} is the device's transconductance [1].

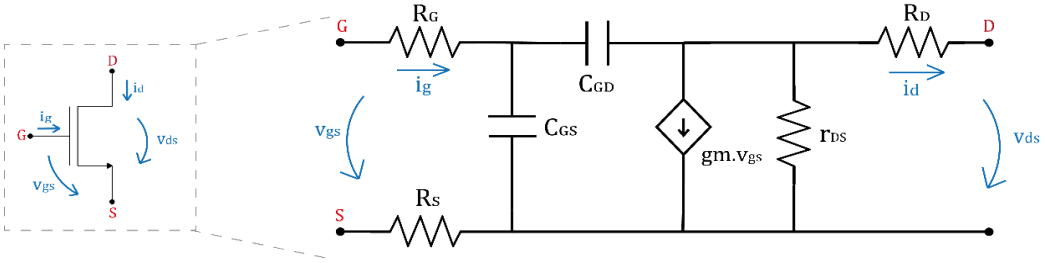

Figure 1 - Small signal equivalent circuit of TFTs. Adapted from [1].

For short-channel devices, contact resistance (R_{C}) is a very important parameter since a high value can completely degrade its DC and AC performance. R_{C} depends not only on the S/D material, its interface with the semiconductor but also the contact area [1]. While R_{C} can be lowered by increasing the S/D area, it is not ideal in terms of VLSI or parasitic capacitances. Other good options for lowering R_{C} are: proper selection of S/D material and/or doping the area of the semiconductor directly in contact with the S/D metal. R_{C} can be extracted by the transmission line method (TLM), where linear transfer curves of devices with different L are used to infer the total resistance (R_{T}). R_{T} is given by (4), where r_{ch} is the channel resistance [1].

$$R_{\mathrm{T}} = r_{\mathrm{ch}} + R_{\mathrm{C}} = r_{\mathrm{ch}} + R_{\mathrm{S}} + R_{\mathrm{D}} \quad (4)$$

One other key parameter that is critical for TFT miniaturization is S/D to gate C_{ov}. S/D electrodes extend over the semiconductor active area and the gate electrode, creating a parasitic capacitor in which the other plate is the gate electrode. It arises from the fabrication process, namely from device layout and mask alignment. Large overlap lengths (L_{ov}), meaning large C_{ov} can significantly lower the operating frequency of TFTs. C_{ov} is calculated by extracting the total gate capacitance $C_{\mathrm{G}} = C_{\mathrm{GS}} + C_{\mathrm{GD}}$, from capacitance-voltage (C-V) characteristics at low V_{GS}. C_{G} is given by (5), where C_{ch} is the channel capacitance and $A_{\mathrm{ov\,total}}$ is the total overlap area between source, drain, gate, and semiconductor [1].

$$C_{\mathrm{G}} = C_{\mathrm{ch}} + C_{\mathrm{ov}} = C_{\mathrm{ox}}WL + C_{\mathrm{ov}} = C_{\mathrm{ox}}A_{\mathrm{ov\,total}} \quad (5)$$

Transit frequency (f_{T}) is one of the most important TFT parameters since it quantifies the device's speed. f_{T} is defined as the unity gain frequency of the scattering parameter H_{21} – the frequency at which H_{21}

equals one. Mathematically, it is given by (6), where μ_{eff} is the effective mobility, given by (7), in the case of operation in saturation regime [1,2].

$$f_{\text{T}} = \frac{g_{\text{m sat}}}{2\pi C_{\text{G}}} \propto \frac{\mu_{\text{eff}}}{L(L + 2L_{ov})} \tag{6}$$

$$\mu_{\text{eff}} = \frac{2L}{WC_{\text{ox}}} \frac{d^2 I_{\text{DS sat}}}{dV_{\text{GS}}^2} \tag{7}$$

From (6) and (7), it is possible to infer that, beyond semiconductor choice (i.e. its mobility), reducing L greatly raises f_{T}. On the other hand, large L_{ov} can degrade the AC performance due to high C_{ov}. Simultaneously, a reduced L_{ov}, meaning a high R_{C}, is also detrimental for short-channel TFTs' ($L < 1$ µm) AC performance. R_{C} becomes critical since its value may surpass r_{ch}, resulting in poor electrostatic control of the channel and μ_{eff} drop [7].

2.1.4. Device structure and self-aligned processes

Device configuration in TFT technology can affect some of the key electrical parameters above discussed. Therefore, proper structure selection is vital to ensure optimisation regarding device application.

Traditionally, device structure can be made either top or bottom gate, depending on whether the gate electrode is placed above or below the semiconductor, respectively. In addition, depending if the source and drain electrodes are on the same or opposite side of the channel interface, devices are referred to as coplanar or staggered (STG), respectively (Figure 2 a-d). Bottom-gate (BG) devices are known for an easier fabrication process and superior performance; however, passivation of the oxide semiconductor is vital. Double-gate configurations are also possible, being popular for enhanced static performance (Figure 2 e) [1,3]. Vertical or quasi-vertical TFTs (VTFTs/QVTFTs) have also been reported, aiming to achieve very short L. Here, L is no longer defined lithographically but by the thickness of a spacing layer between source and drain (Figure 2 f). The major challenge with non-planar structures is the process-induced contamination, which severely degrades electrical performance. Moreover, the device structure itself further complicates proper S/D to gate alignment [4,8]

Corbino TFTs are three-dimensional (3D) circular-shaped devices, in which there are two concentric electrodes for S/D – an inner (IE) and an outer (OE) one (Figure 2g). The gate electrode is usually adjacent to the substrate and defines the whole TFT perimeter [9]. As previously stated, short-channel devices suffer from CLM at the saturation regime. In Corbino TFTs, when the OE is defined as the drain and the IE as the source, W decreases with the decrease of L, so that the W/L ratio is not changed after pinch-off. This effect results in negligible CLM and thus, infinite r_{DS}, making this configuration ideal for applications such as amplifiers and display drivers. L is given by (8), where R_2 and R_1 are the outer and inner radii, respectively. W is calculated as a function of geometrical parameters R_2 and R_1 and considering a radial electric field (9). As W depends on the geometrical factors R_2 and R_1, effective W (W_{eff}) depends on ΔL – resulting in the phenomenon of channel width modulation (CWM). Simplistically, CLM is cancelled by CWM in Corbino TFTs with OE as

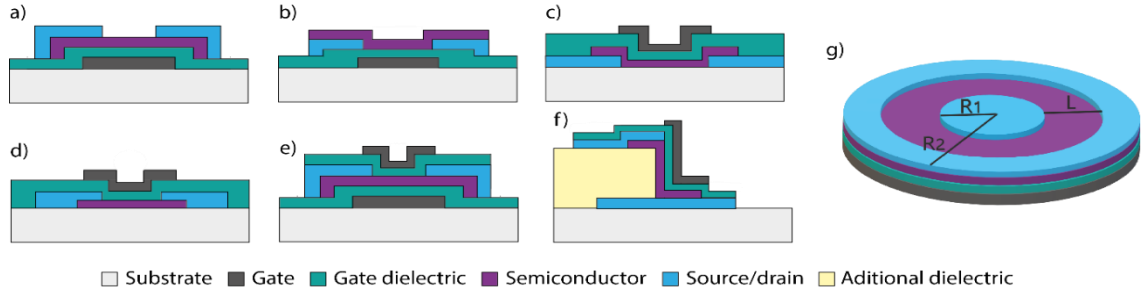

Figure 2 - Schematic cross section of different TFT configurations. a) STG BG; b) Coplanar BG; c) STG TG; d) Coplanar TG; e) Double-gate; f) Vertical TFT; g) Corbino TFT. Adapted from [8],[9].

drain configuration [9].

$$L = R_2 - R_1 \tag{8}$$

$$W/L = \frac{2\pi}{\ln(R_2/R_1)} \tag{9}$$

To improve TFTs' AC performance, a widely explored path is SA processes. These reduce L_{ov} thus C_{ov}. SA TFTs can be achieved via two main approaches: SA TG homojunction TFTs or SA TFTs by backside ultraviolet (UV) exposure.

SA TG homojunction TFTs rely on building the gate and S/D areas on the same plane. This way, S/D to gate C_P is negligible. These structures are usually built in a coplanar configuration, where the outermost parts of the semiconductor are heavily doped to form S/D regions, lower R_C and access resistance (R_A) (Figure 3 a). The gate stack, i.e. gate electrode and GD, are used as protective layers to avoid doping of the central area of the semiconductor layer, meaning that gate and S/D areas are SA. Here, L is no longer defined by the distance between source and drain electrodes, but by the length of the gate electrode [10].

SA TFTs by backside UV (BUV) exposure are BG devices and the fabrication processes take advantage of the UV transparency of the substrate, semiconductor, and GD. Essentially, the opaque gate electrode acts as a UV mask (Figure 3 b) when exposing a layer of positive photoresist (PR). The PR immediately above the gate electrode is not exposed, thus it protects this area from the S/D electrode deposition. This ensures that, after lift-off, S/D electrodes and gate suffer from minimal misalignment [11].

Considerable amounts of reports have been produced regarding the fabrication of sub-µm and SA a-IGZO TFTs. Table 1 summarizes device structure, fabrication processes, L and electrical performance metrics.

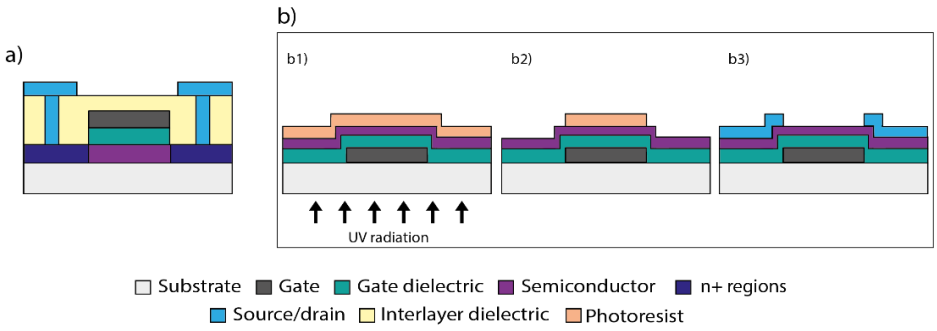

Figure 3 - Schematic cross-section of SA TFTs. a) SA TG homojunction TFTs; b) Process flow of SA TFTs by backside UV exposure. Adapted from [10],[11].

Table 1 – Reports regarding sub-µm and SA TFTs and respective metrics, with different device structures and fabrication processes. ALD – Atomic Layer Deposition; EBL – Electron-beam Lithography; FIB – Focused Ion beam; PET - Polyethylene terephthalate; PI – Polyamide; T_{max} – Maximum processing temperature.

Ref.	Structure	Process	Substrate	L (µm)	μ_{FE} (cm²/V.s)	V_{TH} (V)	f_T (Hz)	T_{max} (°C)
[12]	VTFT	ALD	PI	0.2	6.6	1.5	20 M	180
[13]	STG TG	DLW	PI	0.28	1.1	3	80 M	150
[14]	STG BG	FIB	PI	0.16	4	-22	6 M	150
[15]	STG BG	BUV	PET	0.8	8	-0.5	1.1 G	250
[16]	STG BG	EBL	Si	0.36	1.18	1.8	1.14 G	200

2.1.5. a-IGZO and source/drain formation by doping

Several semiconductors are widely known for their TFT applications, such as a-Si:H, poly-Si, or even organic ones. However, amorphous oxide semiconductors (AOS) seem to be the best compromise between

electrical and optical properties, large-scale applications, and low thermal budgets and production costs [3].

Namely, a-IGZO TFTs have seen the most extensive research and applications of all oxide TFTs. a-IGZO is a complex oxide that can withstand high μ despite amorphous structure, room temperature deposition compatibility, low voltage operation, low leakage currents, low fabrication costs, and visible light transparency [5]. The conductivity of a-IGZO films can be tuned by adjusting atomic ratios, for example [3]. Both oxygen vacancies (V_O) and hydrogen (H^+) act as donors, being responsible for the conductivity [5].

Considerable amounts of reports have been produced regarding the formation of highly doped S/D regions for homojunction TFTs (both BG and TG). Different doping methods have been reported, including plasma treatments, hydrogen or fluorine diffusion, metal reaction, ion implantation, and deep ultraviolet (DUV) treatments [10,17–20]

Amongst all these possibilities, plasma treatments are an effective, easy, fast, and low-cost option. Several plasmas can be used, including Ar, He, hydrogen-based plasmas such as H_2, and fluorine-based plasmas (CF_4/O_2 mixture, for example). Ar and He plasmas create V_O in a-IGZO via bond breaking. The relatively weak In-O bond is broken through ion bombardment, creating V_O and an In-rich surface, which both contribute to higher conductivity [10].

2.2. Direct laser writing

Traditional photolithography relies on transferring the pattern of a mask to a photoactive polymer (photoresist). UV light is shone through the slits of the mask, and the solubility of the PR is changed. The remaining pattern is then used to aid in device-structuring processes, such as etching or lift-off. For R&D, mask cost can be very considerable, since changing the desired design results in the need for a new mask set. In addition, traditional optical mask aligners using mercury light sources are usually limited to resolutions worse than 1 µm, with improved resolutions requiring the use of more complex setups such as deep or extreme UV (DUV or EUV) lithography tools [21].

Direct laser writing (DLW) is a type of maskless lithography, where sub-µm structuring is achieved through exposing PR using focalized laser radiation. A laser head of UV wavelength scans the substrate, following the desired computer-aided design (CAD) layout. DLW is interesting compared to traditional photolithography and even amongst other maskless lithography techniques since it provides low-cost, high-resolution, easy, and versatile prototyping. However, depending on pattern size and density, DLW lithography is far slower than traditional photolithography [22].

2.3. TCAD

TCAD refers to a set of tools that allow for the simulation of 2D or 3D semiconductor devices at a physical level. TCAD simulations can provide deep physical and electrical insight on any type of device, given that appropriate materials, structures, and physical properties are declared. TCAD tools are extremely valuable to understand the impact of different device architectures, material properties, and to improve fabrication processes. Given material choice and structure definition freedom, TCAD tools are helpful since they allow for a significant reduction in fabrication costs and time when developing or improving a new technology [23,24].

Concerning the development of sub-µm and SA a-IGZO TFTs, TCAD can predict the electrical characteristics of the SA TG homojunction, SA TFTs by backside UV exposure architectures or even Corbino TFTs. Moreover, in the specific case of SA TG homojunction TFTs, TCAD can be used to investigate the level of doping of S/D areas necessary to achieve satisfactory electrical performance. Gathering insight into devices with sub-µm channel lengths, into the impact of R_C and C_{ov} on f_T, and the eventual appearance of short-channel effects is also a key advantage of using TCAD in this work.

3. Materials and methods

In this section, the methodology adopted for TCAD simulation of a-IGZO TFTs is firstly described. Then, the procedure used to fabricate and characterize a-IGZO samples doped by Ar-plasma is reported. Finally, the chapter ends by describing the fabrication process of both SA TG TFTs by DLW and STG BG TFTs by traditional mask alignment.

3.1. TCAD simulations

For this work, Silvaco's Atlas™ TCAD was used. The user interface is made through the DeckBuild™ software, where structures, material properties, and solving methodologies are declared. Three different TFT structures were studied: staggered BG (STG BG), SA TG, and Corbino. Three different L values were studied for each structure (L = 5; 1 and 0.6 µm). Also, the impact of R_C in each structure was simulated, with R_C assuming the values of 0; 1 µ; 10 µ; 0.1 m and 1 mΩ.cm^2. L_{ov} was only varied for the STG BG structure, in the values of 0; 0.5; 1; 3 and 5 µm. For the SA TG structure, the concentration of donor dopants (N_D) in the S/D regions was varied in decade increments, from 10^{15} to 10^{20} cm^{-3}. W was fixed at 80 µm for STG BG and SA TG structures. Simulated TFTs featured a-IGZO as the semiconductor, in a 30 nm film with μ = 10 cm^2/V.s. All contacts were declared as 60 nm Mo and the chosen GD was Ta_2O_5, with a thickness of 60 nm and a dielectric constant (ε_r) of 25. The mesh is created in order to allow for more simulation points on interest areas, such as the semiconductor/dielectric interface and the semiconductor and S/D interface. Simulation parameters are present in Annex 1.

3.2. a-IGZO doping tests

The fabrication of Ar-doped a-IGZO test samples was carried on 2.5 × 2.5 cm Corning glass as a substrate. Cleaning methodology was kept the same for this entire work. Substrates were firstly cleaned with acetone in an ultrasound bath for 10 min, and then with isopropyl alcohol (IPA) following the same procedure. Substrates were then cleaned with deionized (DI), dried with the aid of a nitrogen gun, and placed on a hot plate for 20 min, at 120 °C.

A 40 nm a-IGZO (2:1:1 atomic ratio) thin film was sputtered with an AJA ATC-1300 F, using a three-target system, in an Ar and O_2 atmosphere[1]. The Ar doping process was carried out using a Trion Phantom 3 reactive ion etcher. Gas flow rate and pressure were kept at 10 sccm and 20 mTorr, respectively. Power and time conditions were varied. For 60 W, treatment times were the following: 30; 60; 150;180; 240; 300; 420 and 600 s. For a power 250 W, treatment times of 20; 30; 40; 60; 120 and 300 s were employed. Finally, after doping, 100 nm thick Al contacts were deposited via e-beam evaporation (using a homemade e-beam setup), using two different types of shadow masks (Annex 2). Samples were characterized using a Keysight B1500A semiconductor parameter analyzer in conjunction with a Cascade Microtech EPS 150 manual probe station and a Biorad/Nanometrics HL5500 Hall effect systems.

3.3. TFT fabrication

Both SA TG TFTs and BG TFTs were fabricated during this work. BG TFTs were produced to infer the R_C between the doped a-IGZO and the Mo contacts, and the dopant diffusion length in a-IGZO, through the TLM. All metal layers/contacts in both structures are made out of 60 nm Mo, deposited by sputtering in an Ar atmosphere using an AJA ATC 1800. The positive resist used was always AZ ECI 3012 PR, the negative

[1] The process for a-IGZO deposition by sputtering was optimised to yield 30 nm films, however, after ellipsometry measures, the thickness of the deposited films was found to be 40 nm.

resist was AZ nLOF 2020 and the developer used was the AZ 726 MIF, all by Merck.

Final devices of both configurations were electrically characterized using the same probe station and semiconductor parameter analyser as in section 3.2. Transfer curves, both linear and saturation; output curves; Capacitance-Voltage (C-V), and Capacitance-frequency (C-f) curves were extracted. All micrographs were taken with a Zeiss Axioscope 5 optical microscope. Scanning Electron Microscopy (SEM) and Energy Dispersive X-ray Spectroscopy (EDS) were performed using a Zeiss Auriga CrossBeam system and an Oxford X-Max 150 detector with Aztec software, respectively.

Despite Ta_2O_5 being used as the GD in TCAD simulations, its implementation on SA TG TFTs was conditioned by its lack of etching selectivity with SF_6 gas compared to Mo, since the gate electrode act as a mask for dielectric etching in this structure. Thus, both Al_2O_3 and parylene-C were adopted as GD for TFT fabrication.

3.3.1. SA TG TFTs

SA TG TFTs were fabricated by DLW. Layouts for DLW were designed in Adobe Illustrator© and KLayout©. In this section, all the lithographic steps were achieved using the Heidelberg µPG 101 Tabletop Micro Pattern Generator. There are two writing heads available: the 20 mm head, with a minimum structure size of 5 µm; and the 2 mm head, with a minimum structure size of 0.6 µm. Laser parameters with the 2 mm head were optimized to achieve 0.7 µm resolutions on 60 nm Mo samples, sputtered on previously cleaned Corning glass. To achieve such high resolutions, PR thickness, post-exposure bake (PEB) and developer concentration also had to be tailored. Optimised laser parameters were used as follows: for the 2 mm head, 15 mW at 52% duty cycle with −1.5 focus, for both positive and negative PR; for the 20mm head, 22 mW at 80% duty cycle and −2 focus for positive PR and 50mW at 81% duty cycle and −2 focus for negative PR.

The fabrication of SA TG TFT started with cleaning two 5 × 5 cm Corning glass substrates. Positive PR was spin-coated and soft-baked at 90 °C for 1 min. Afterward, semiconductor mask was patterned on both samples, with the 2 mm head, followed by PEB at 110 °C for 1 min and development for 1 min. Next, a 40 nm a-IGZO film was deposited, using the same methodology as in section 3.2. The samples underwent lift-off in acetone and then immersed in IPA for cleaning. Some PR spots were very crosslinked due to the action of the plasma during a-IGZO sputtering, so the samples were submerged in TechniStrip P1316 (Merck), at 75 °C for 5 min. Samples were annealed at 180 °C for 1 h on a hot plate, corresponding to the highest temperature step in this fabrication process. The two samples were then coated with different GD: one with 50 nm of Atomic Layer Deposition (ADL)-grown Al_2O_3 (using a Beneq TFS 200) – Sample 1TG; and the other with 300 nm of parylene-C deposited via chemical vapor deposition (CVD) in a Speciality Coating PDS-2010 Parylene coater and using silane as an adhesion promoter – Sample 2TG. DPX-C (Galentis) was used as the parylene precursor. Next, a Mo film was deposited as the gate layer. Negative PR was spin-coated to result in a 1.2 µm thick layer and soft-baked at 110 °C for 2 min. Gate mask was exposed with the 2 mm head and PEB was performed at 115 °C for 2 min. Samples were developed in a diluted solution of 3:1 developer to DI water, for 210 s. Afterward, Mo was dry-etched using SF_6 gas. Parylene-C was also dry-etched but with O_2 gas. Al_2O_3 was wet-etched with the developer. a-IGZO was Ar doped with the same pressure and gas flow rate as in section 3.2, at 250 W for 30 s. At the end of this process, the remaining PR was removed. Next, both samples underwent a 1.2 µm parylene-C deposition, acting as the interlayer dielectric. The vias mask was exposed onto positive PR with the 20 mm head and vias were opened via dry-etching of parylene-C. Due to the possibility of filling the V_O created during doping with the O_2 plasma, an additional 30 s Ar doping treatment was employed. The remaining PR was removed. Next, Mo was deposited and the contacts mask was exposed onto negative PR. Mo was dry-etched and PR was removed. Schematic process flow can be found in Annex 3.

3.3.2. BG TFTs

A 10 × 10 cm Corning glass substrate was cleaned, onto which the gate pattern was exposed on positive PR, using a Suss MA6 UV mask aligner. Mo was deposited and then lifted off. The sample was split into four different pieces: two underwent the Al_2O_3 ALD deposition (samples 1BG) and on the remaining a film of parylene-C was deposited (samples 2BG). Depositions were simultaneous with SA TG TFTs samples. Next, the vias mask was patterned on positive PR. Parylene-C was dry-etched and Al_2O_3 was wet-etched with pure H_3PO_4 at 80 °C. Then, the a-IGZO layer was deposited and structured via lift-off using positive PR. TechniStrip P1316 was used as before. Samples were annealed like previously described. S/D mask was patterned onto positive PR and all samples underwent the same a-IGZO doping process as the SA TG TFTs. Afterward, Mo was deposited and S/D electrodes were then structured by lift-off. Finally, a 1.2 µm thick parylene-C film was used as device passivation. The pad access mask was exposed onto positive PR and parylene-C was dry-etched. Schematic process flow can be found in Annex 4.

4. Results and discussion

This chapter starts by providing a brief context on the methodology followed for extracting TFT metrics. Then, TCAD simulation results for STG BG, SA TG and Corbino structures are presented and discussed, followed by a comparison between the major electrical metrics of these three TFT structures. The impacts of R_C, L_{ov} and L shortening are discussed. Afterward, the results of a-IGZO doping by Ar plasma are explored. In the scope of sub-µm SA TG TFT fabrication by DLW, the results of optimised fabrication processes and DLW conditions are also presented. At last, the electrical characterization results of both SA TG TFTs by DLW and STG BG TFTs by traditional mask alignment are presented and discussed.

4.1. Electrical parameters extraction

This section provides the methodology followed for extracting TFT metrics, for both TCAD and fabricated devices. Example transfer, output, C-V, and C-f curves are depicted in Figure 4 a) through d), respectively.

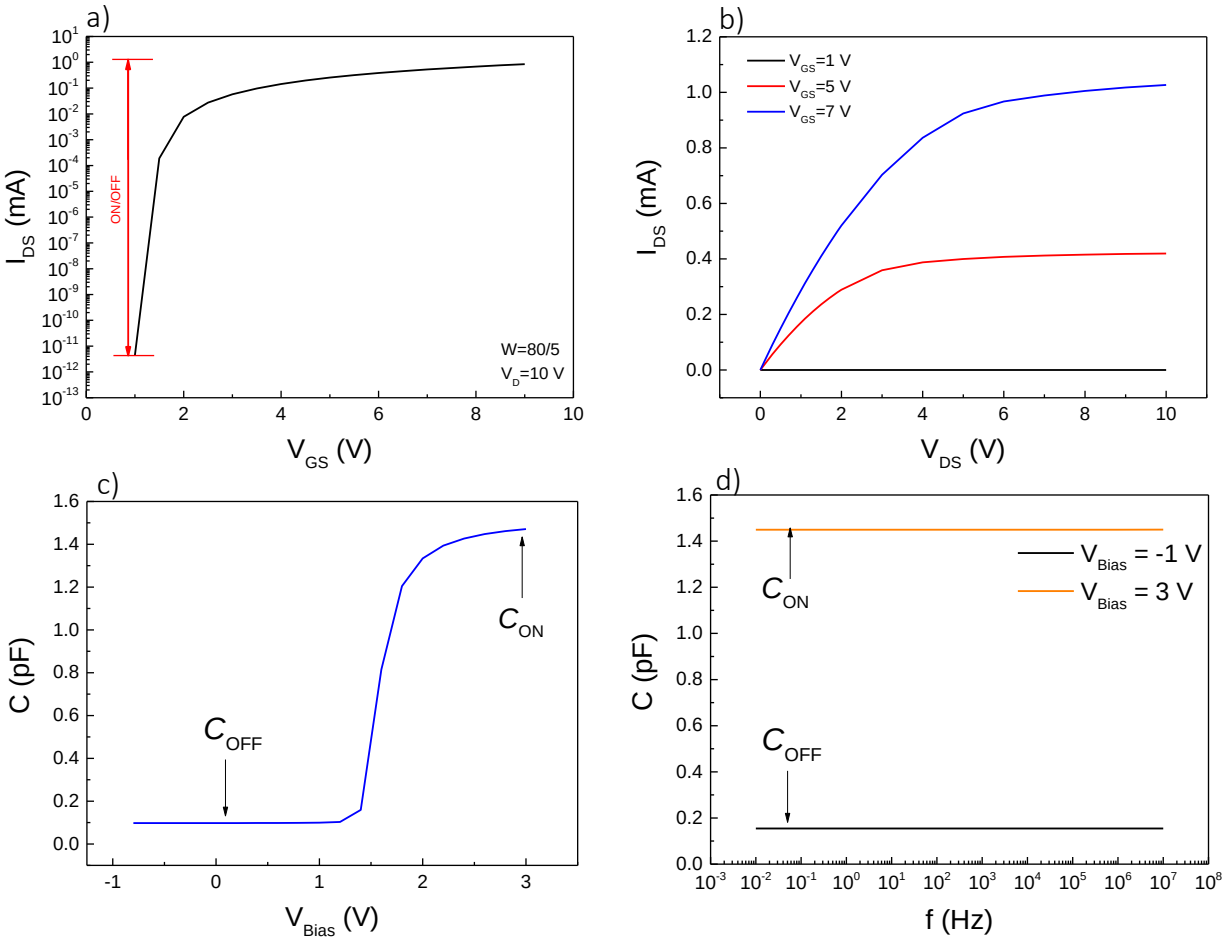

Figure 4 - Example TFT characteristics. a) Transfer; b) Output; c) Capacitance-Voltage; f) Capacitance-frequency.

From the linear transfer curves, subthreshold swing (SS), ON/OFF, μ_{FE} and V_{TH} were extracted. SS is defined as (10) [3]. ON/OFF is simply the ratio between the ON current and the OFF current of the device (Figure 4 a) [3]. μ_{FE} is the first derivative of (1.1), adjusted for the device geometrical features, C_{ox} and V_{DS} [3]. So, μ_{FE} is given by (11). V_{TH} is the maximum of the second derivative of $I_{DS\,lin}$ (12).

$$SS = \left(\frac{d\,(\log I_{DS\,lin})}{dV_{GS}}|_{max}\right)^{-1} \tag{10}$$

$$\mu_{FE} = \frac{dI_{DS\,lin}}{dV_{GS}} \frac{L}{WC_{ox}V_{DS}} \tag{11}$$

$$V_{TH} = \frac{d^2 I_{DS\,lin}}{dV_{GS}^2} \tag{12}$$

μ_{SAT}, μ_{eff} and gm_{SAT} were extracted from the saturation characteristics. μ_{SAT} is obtained the same way as μ_{FE} only for the saturation regime [3]. Thus, μ_{SAT} is given by (13). μ_{eff} was calculated through (7). gm_{SAT} is given by (14) [1].

$$\mu_{SAT} = \left(\frac{d\sqrt{I_{DS\,sat}}}{d\,V_{GS}}\right)^2 \frac{2L}{WC_{ox}} \tag{13}$$

$$gm_{SAT} = \frac{dI_{DS\,sat}}{dV_{GS}} \tag{14}$$

From the output curves, it is possible to extract TFTs conductance (g_{ds}) [1].

$$g_{ds} = \frac{dI_{DS}}{dV_{DS}} \tag{15}$$

The devices' intrinsic gain (A_V) is given by (16) [1].

$$A_V = \frac{gm_{SAT}}{g_{ds}} \tag{16}$$

Parasitic capacitance (C_P) is the total gate capacitance when the device is OFF (C_{OFF}), while C_{ON} is the total gate capacitance when the device is ON. C_{ox} is given by (17). Both of these metrics can be extracted from both C-V and C-f curves, given the appropriate gate bias conditions to ensure ON and OFF states [8]. C_G is obtained through (5). In SA TG TFTs, C_{ov} is considered as zero.

$$C_{ox} = \frac{C_{ON} - C_{OFF}}{WL} \tag{17}$$

In TCAD simulations, f_T is the frequency at which the current gain of the H_{21} scattering parameter equals one, at $V_{GS} = 7$ V and $V_{DS} = 10$ V. For SA TG TFT characterization, f_T was calculated through (6).

4.2. TCAD simulation

4.2.1. Staggered bottom-gate

The AC performance of the STG BG structure can easily suffer from the effects of L_{ov}, due to device layout or even mask alignment. The declared TCAD structure is depicted in Figure 5. The overlap between the S/D electrodes and the semiconductor was always kept at 1.5 µm, which is a reasonable value for the lower limit of these overlap lengths when considering layouts for TFTs fabricated via traditional mask alignment techniques.

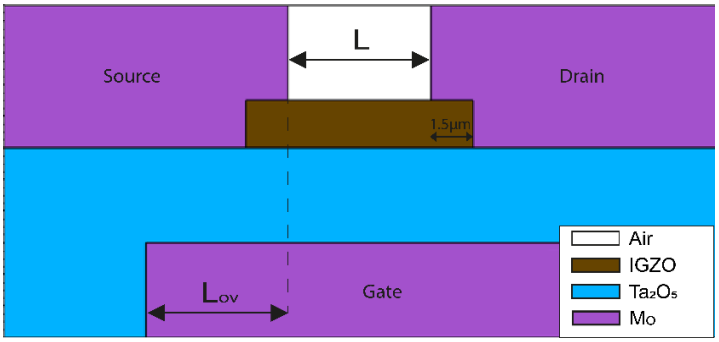

Figure 5 - Schematic cross section of the STG BG structure declared in TCAD.

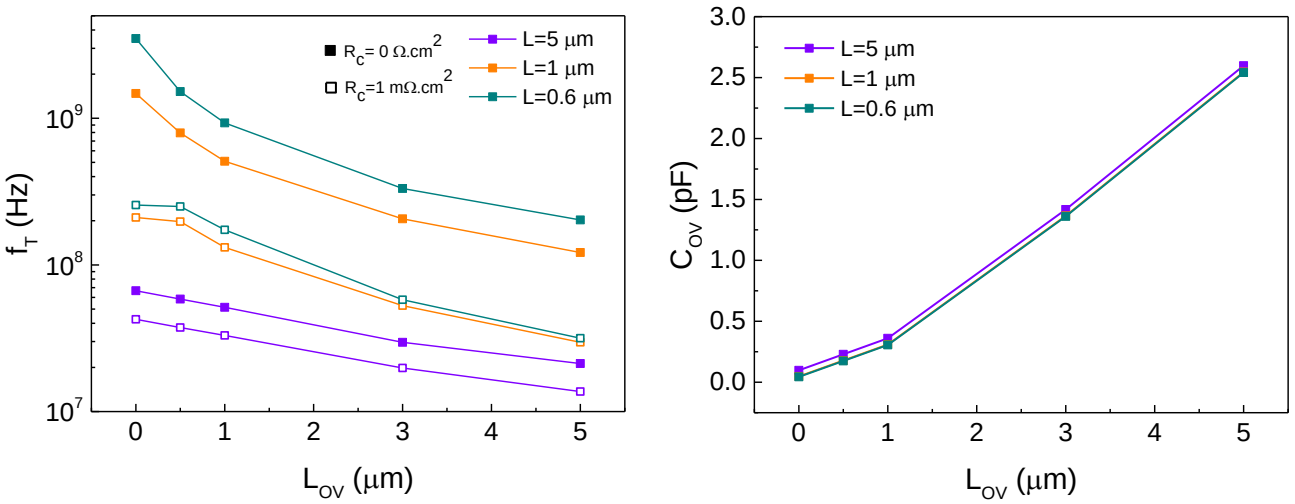

Figure 6 - Dependence of f_T and C_{ov} on L_{ov} in the STG BG structure. Lines are indicative.

The dependence of f_T on L_{ov} for extreme conditions of R_C is depicted in Figure 6. Smaller L and low R_C result in the highest f_T. Decreasing L_{ov} greatly raises f_T for both $R_C = 0$ Ω.cm^2 and $R_C = 1$ mΩ.cm^2. It is for smaller L devices that this difference is more significant since decreasing L_{ov} from 5 µm to 0 µm increases f_T by 17 times for $L = 0.6$ µm and only by 3 times for $L = 5$ µm. However, decreasing L_{ov} past 0.5 µm while maintaining a high R_C produces no effect on f_T, especially for $L < 1$ µm. In a real fabrication scenario, a proper trade-off between R_C and C_{ov} must be made since these have an opposite dependency with L_{ov}. Very short L_{ov}, thus short overlap areas are ideal to decrease C_{ov} however, a smaller contact area effectively increases R_C [7]. It is also worth noting that the effect of R_C on f_T is also L dependant. By raising from 0 to 1 mΩ.cm^2, f_T drops by 1.57 times for $L = 5$ µm, by 7 times for $L = 1$ µm and by 14 times for $L = 0.6$ µm. This indicates

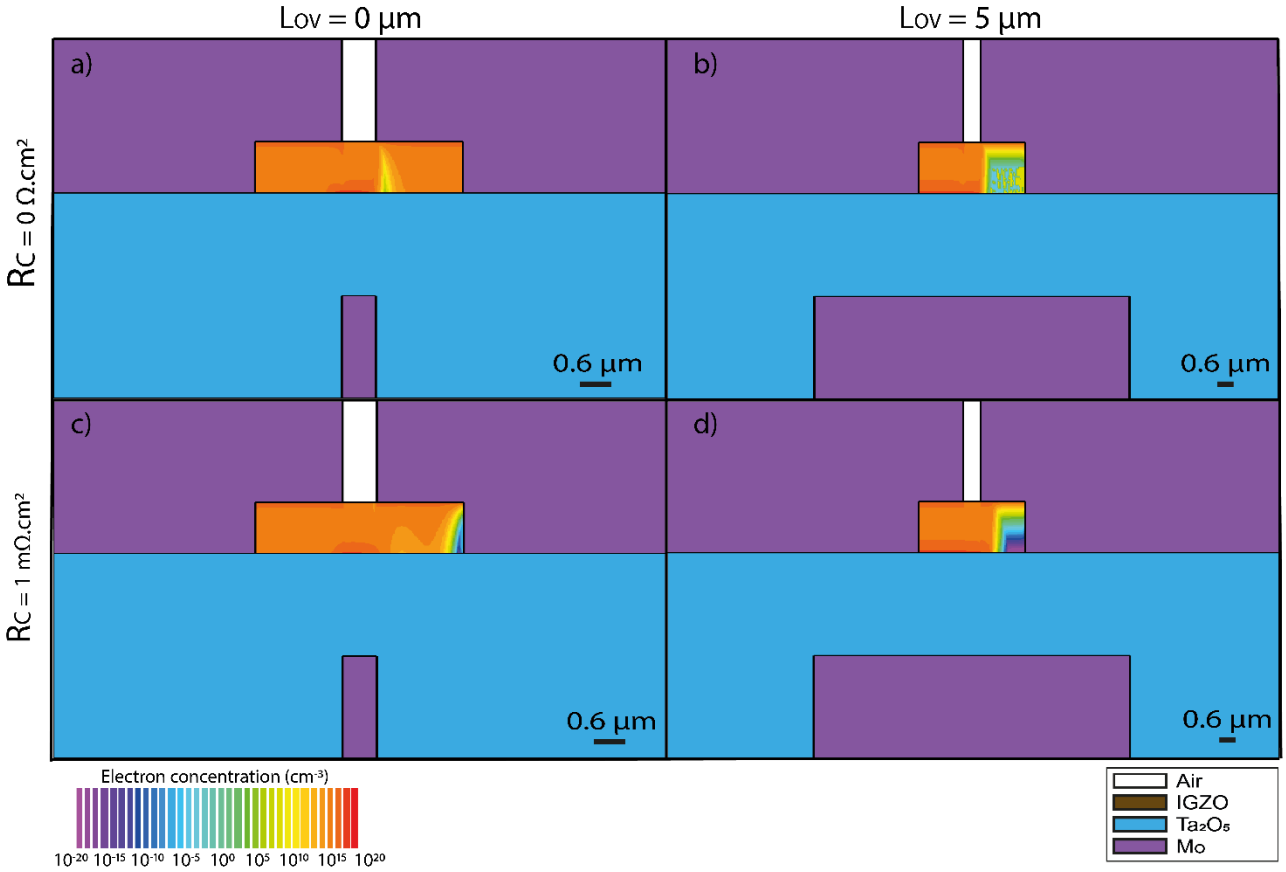

Figure 7 - Electron concentration distribution in IGZO for different L_{ov} and R_C combinations in the STG BG structure, for $V_{GS} = 7$ V, $V_{DS} = 10$ V and $L = 0.6$ µm. a) $L_{ov} = 0$ µm and $R_C = 0$ mΩ.cm^2; b) $L_{ov} = 5$ µm and $R_C = 0$ Ω.cm^2; c) $L_{ov} = 0$ µm and $R_C = 1$ mΩ.cm^2; d) $L_{ov} = 5$ µm and $R_C = 1$ mΩ.cm^2.

that R_C has a bigger impact on STG BG devices with smaller L. This effect has been reported several times and it is attributed to R_C surpassing r_{ch}, allowing for less voltage to reach the active layer since, unlike r_{ch}, R_C does not scale with L [7,21]

Figure 7 shows the electron concentration in a-IGZO, for $V_{GS} = 7$ V, $V_{DS} = 10$ V and $L = 0.6$ µm. When L_{ov} and R_C both equal zero, device shows the common pinch-off profile near the drain, with an approximate 0.2 µm wide zone somewhat depleted of electrons. However, for higher L_{ov}, the depletion zone widens, taking up the whole overlap length between the drain electrode and the semiconductor (which are themselves overlapped with the gate electrode), about 1.5 µm. Furthermore, this region becomes even more depleted of electrons. Given that the electric field between drain and gate is much smaller than the one between source and gate, higher L_{ov} allows for a higher extension of the depletion region underneath the drain. Higher R_C also further decrease electron concentration and shift the depletion region to the right. For the case where L_{ov} and R_C are the highest, the depletion zone is about 0.7 µm wide, and presents the lowest electron concentration.

4.2.2. SA TG TFTs

For the SA TG TFT structure, the formation and the effectiveness of the highly doped S/D areas are the biggest concern. Otherwise, high R_A will negatively impact electrical performance. While both R_A and R_C result on degraded DC and AC performance on SA TG TFTs, R_A simply refers to the resistance of the IGZO S/D regions and it can be seen as two series resistors connecting the active layer and the S/D electrodes. Whilst R_C is a property of the semiconductor/metal interface. R_A depends on the conductivity of the doped IGZO, and thus is inversely proportional to N_D.

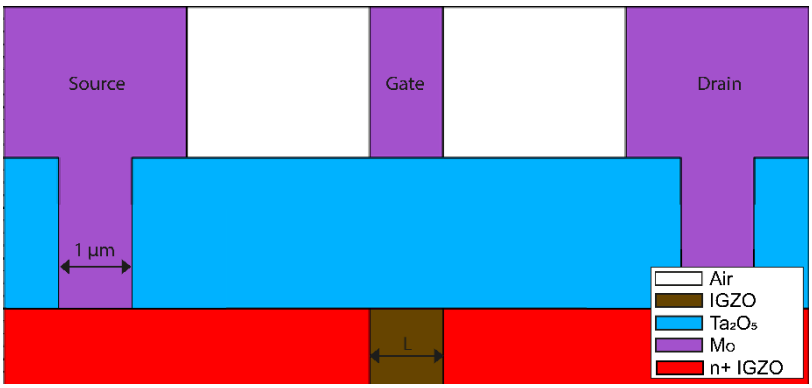

Figure 8 - Schematic cross section of the SA TG structure declared in TCAD.

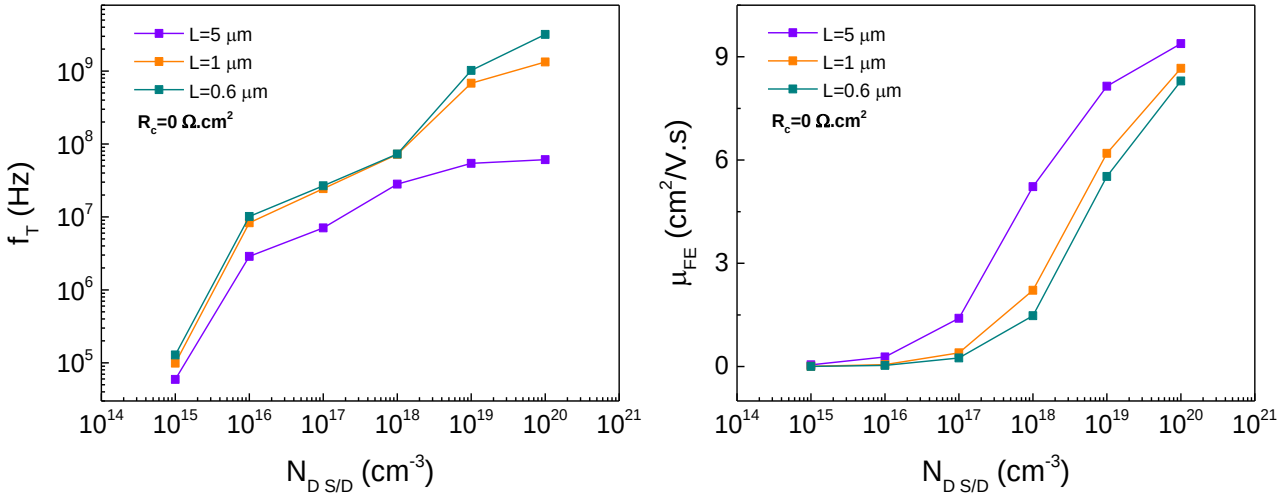

Figure 9 - f_T and μ_{FE} dependency on N_D of the S/D areas, for different L values. Lines are indicative.

The obtained TCAD structure for the SA TG TFT is depicted in Figure 8. The values of μ_{FE} and f_T for different N_D are depicted in Figure 9, for an ideal case of no R_C. μ_{FE} and f_T both increase with N_D. It is notorious that high levels of doping (> $N_D = 10^{19}$ cm^{-3}) are required to attain the same electrical performance as the STG BG architecture, with μ_{FE} values tending closer to the electronic μ defined for a-IGZO (10 cm^2/Vs). Increasing N_D has a higher impact on f_T for smaller L devices, since these are more affected by R_C, and doping of the a-IGZO S/D areas effectively decreases R_C by making a better semiconductor/metal interface and lowering R_A of these devices.

Figure 10 shows the electron concentration in a-IGZO, for $V_{GS} = 7$ V, $V_{DS} = 10$ V and $L = 5$ µm, for different N_D. It seems as lower N_D favours the formation of depletion areas in the n$^+$ a-IGZO/ a-IGZO interfaces when the device is biased in the saturation regime, which results in higher R_A. Additionally, lower doping levels of the S/D areas result in less carrier concentration in the active region, since less drain voltage is capable of actually reaching the active layer. These two factors contribute to lower μ_{FE} thus lower f_T. The presented results prove that appropriate doping techniques and studies must be carried out to successfully implement this structure in real-device fabrication. It was found that N_D values around 10^{20} cm^{-3} resulted from highly conductive Ar-doped a-IGZO films as shall be discussed further ahead.

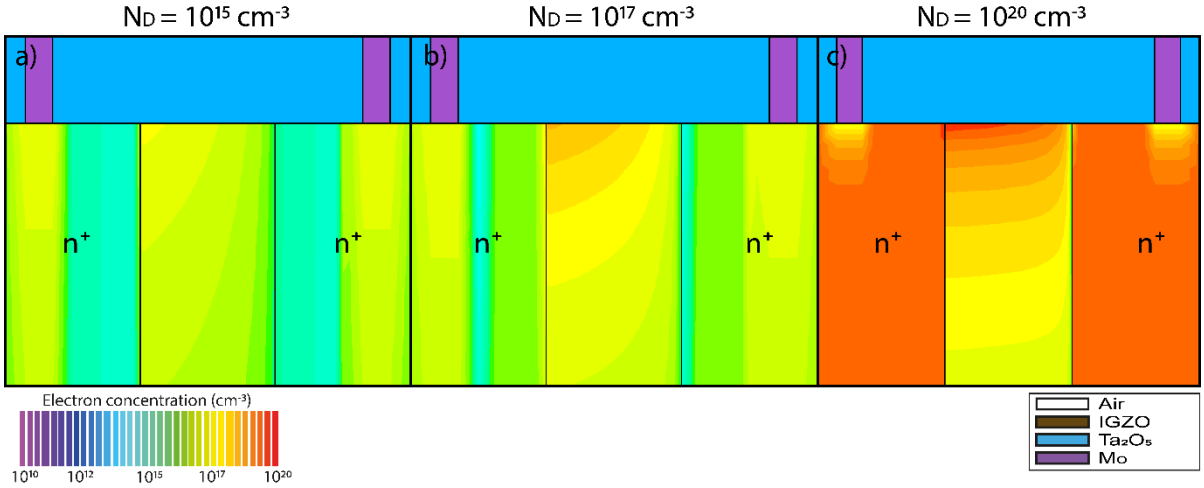

Figure 10 - Electron concentration distribution in IGZO for different N_D in the STG BG structure, for $V_{GS} = 7$ V, $V_{DS} = 10$ V and $L = 5$ µm. a) $N_D = 10^{15}$ cm^3; b) $N_D = 10^{17}$ cm^3; c) $N_D = 10^{20}$ cm^3.

4.2.3. Corbino TFTs

The declared TCAD structure for Corbino TFTs is depicted in Figure 11. The width of the IE and OE was kept at 5 µm. Corbino TFTs are notable due to the asymmetry between IE and OE that rises at high V_{DS}. Since CLM is negligible for the OE drain configuration, it is interesting to study the shortening of L in these devices.

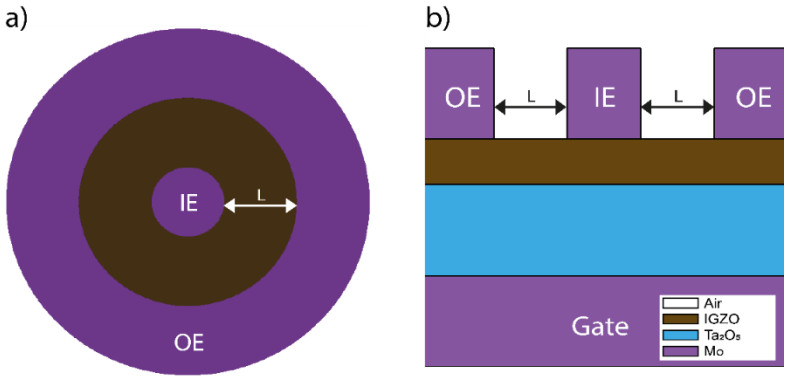

Figure 11 - Schematic of the Corbino structure declared in TCAD. a) Top-view; b) Cross-section.

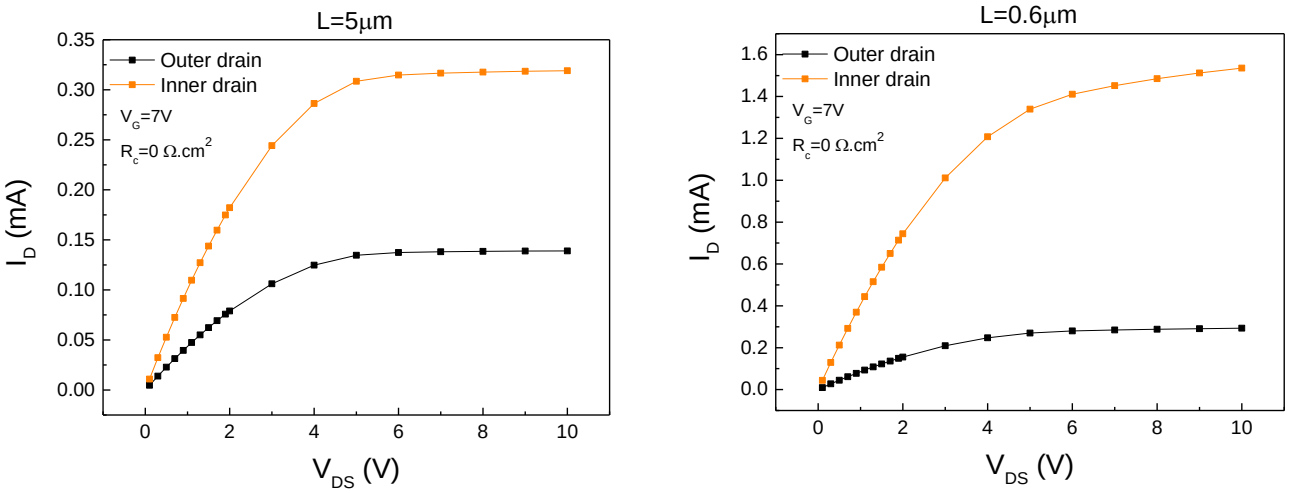

Figure 12 - Output characteristics of Corbino TFTs, for OE and IE drain configurations.

Figure 12 shows simulated output curves with the OE as the drain or as the source. The IE drain configuration results in higher I_{DS} currents, being around 5 times higher than for the OE drain configuration, for $L = 0.6$ µm at $V_{\mathrm{DS}} = 10$ V. However, especially for smaller L, the OE configuration presents the advantage of nearly infinite r_{DS} which is one of the short-channel effects that seriously impacts the performance of scaled-down devices for amplifier or display driver circuits, for example [9].

Electron concentration on a-IGZO, for Corbino TFTs with OE drain and IE drain configurations are present in Figure 13. Pinch-off regions lay in distinct areas of the semiconductor depending on drain configuration, which is unlike what happens for regular rectangular TFTs, where drain and source bias configurations are perfectly symmetric. More importantly, due to Corbino's TFT geometry, the area of the device where the pinch-off occurs is what gives it its unique electrical characteristics. In the IE drain configuration, the depletion area occupies the inner portion of the channel, raising R_1 by $\Delta L_{\mathrm{inner}}$. On the other hand, when the OE is the drain, R_2 lowers by $\Delta L_{\mathrm{inner}}$. $(W/L)_{eff}$ for the IE and OE drain conditions are given by (18) and (19), respectively. Since $R_2 > R_1$, $(W/L)_{\mathrm{eff\,inner}}$ greatly raises with $\Delta L_{\mathrm{inner}}$. Concurrently, assuming $\Delta L_{\mathrm{outer}} << R_2$, $(W/L)_{\mathrm{eff\,outter}}$ only increases slightly with $\Delta L_{\mathrm{outer}}$. This is why, for the OE drain configuration, CLM is compensated by CWM, and thus, r_{DS} is infinite beyond pinch-off [9,25].

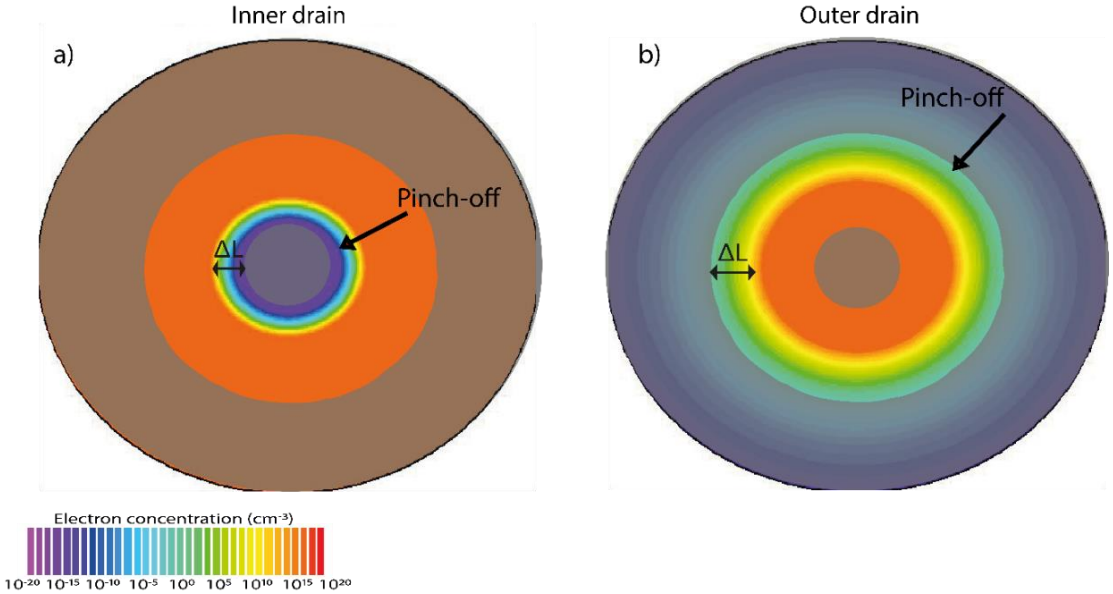

Figure 13 - Electron concentration distribution on a-IGZO, at $V_{\mathrm{GS}} = 7$, $V_{\mathrm{DS}} = 10$ V for $L = 5$ µm. a) IE drain and b) OE drain configuration. Shaded regions correspond to IE and OE.

$$(W/L)_{\text{eff inner}} = \frac{2\pi}{\ln\left(R_2/(R_1 + \Delta L_{\text{inner}})\right)} \quad (18)$$

$$(W/L)_{\text{eff outer}} = \frac{2\pi}{\ln\left((R_2 - \Delta L_{\text{outer}})/R_1\right)} \quad (19)$$

4.2.4. Comparisons between structures

In this section, a comparative analysis of the most important electrical metrics of the three different TFT structures will be given. Note that, for this comparison, Corbino TFTs were biased with the OE drain configuration.

4.2.4.1. Maximum electrical performance

Maximum f_T, μ_{FE} and I_{DS}, in this work, happen for ideal conditions, meaning zero L_{ov} in the case of the STG BG structure, and zero declared R_C for all three structures. $L_{ov} = 0$ µm for STG BG TFTs is used here merely for comparison sake, and it should be noted that f_T values hereby presented for this structure represent a superior limit that is not attainable for fabricated devices.

Table 2 - $f_{T\,max}$, $\mu_{FE\,max}$, $I_{DS\,max}$ and $(g_{m\,SAT}/g_{ds}) \times L/W$ for STG BG (L_{ov}=0), SA TG and Corbino TFTs.

	$f_{T\,max}$ (Hz)			$\mu_{FE\,max}$ (cm²/V.s)		
L (µm)	STG BG	SA TG	Corbino	STG BG	SA TG	Corbino
5	60.7M	61M	0.3M	9.8	9.4	9.6
1	1.5G	1.3G	1.9M	9.1	8.7	9.2
0.6	3.5G	3.2G	3.2M	8.6	8.3	8.9
	$I_{DS\,max}$ (mA)			$A_V \times L/W$		
L (µm)	STG BG	SA TG	Corbino	STG BG	SA TG	Corbino
5	1.0	0.9	0.32	783	2941	1462
1	5.0	4.3	1.10	465	544	747
0.6	8.1	6.9	1.82	322	302	638

Table 2 summarizes $f_{T\,max}$, $\mu_{FE\,max}$, maximum drain current ($I_{DS\,max}$ @ V_{GS} =7V and V_{DS} = 10 V) and normalized A_V for each architecture and L. Maximum f_T ($f_{T\,max}$) is the highest for STG BG and SA TG architectures, 3.5 GHz and 3.2 GHz, respectively, being significantly lower for the Corbino TFT. $f_{T\,max}$ increases with decreasing L for all structures. For Corbino TFTs, sufficient metal line width for the IE and OE is necessary to achieve low R_C, thus sufficient μ_{FE} and I_{DS}. Here, the use of 5 µm width metal lines negatively impacts $f_{T\,max}$, due to a significant rise in overlap area and thus C_{ov}. Maximum μ_{FE} ($\mu_{FE\,max}$) is lower for the SA TG structure than for the STG BG one, since the former structure always imposes some level of R_A. $\mu_{FE\,max}$ is very similar for the same L across all strucutres. STG BG structure is capable of achieving higher values of $I_{DS\,max}$. The Corbino structure presents the advantage of having nearly double the A_V for $L = 0.6$ µm when compared to the other architectures.

4.2.4.2. Impact of contact resistance

Figure 14 shows the impact of R_C on f_T and μ_{FE}, for the different L and structures. N_D for the SA TG structure was kept at 10^{20} cm^{-3}, resulting in R_A =130 Ω, which in this case is equivalent to 10.4 nΩ.cm² at the n⁺ a-IGZO/Mo interface (considering the 1 µm contact width and $W = 80$ µm). Therefore, R_A is much lower than any of the declared R_C. Thus, the impact of R_C always superimposes that of R_A, unless for R_C = 0 Ω.cm². For relatively large L, such as $L = 5$ µm, R_C barely affects f_T and drops μ_{FE} around 3 times at most, for the

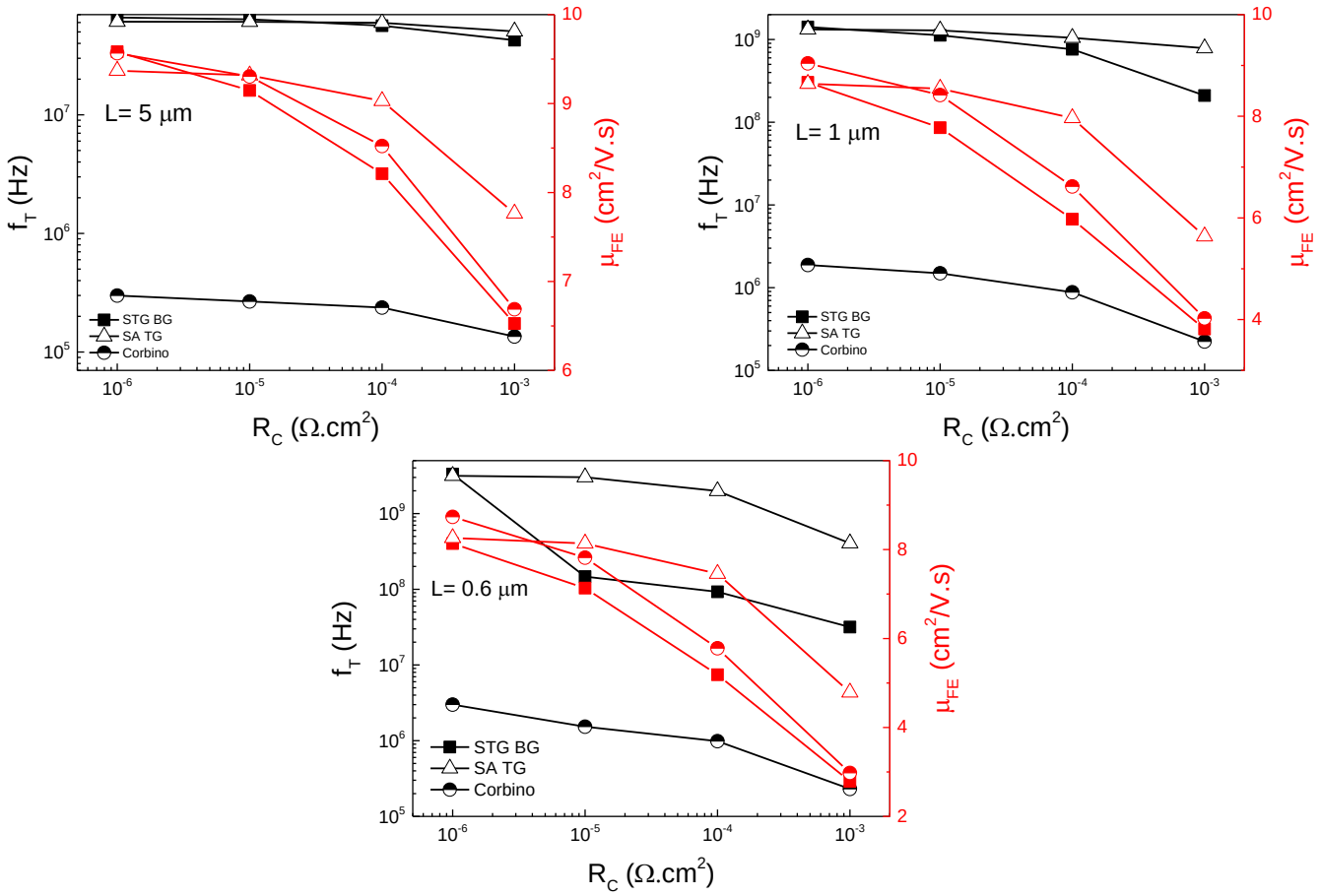

Figure 14 - Dependence of f_T and μ_{FE} on R_C, for the STG BG, SA TG and Corbino structures and different L. Lines are indicative.

STG BG and Corbino architectures, and only 1.5 times for SA TG. For $L = 0.6$ µm, increasing R_C drops f_T and μ_{FE} the highest. However, for all L values, it is noticeable that the SA TG structure is the least affected by R_C. Effectively, the increased carrier concentration of the S/D areas in SA TG TFTs promotes electron injection into the drain terminal and, with small enough R_C, direct tunnelling at the n^+ a-IGZO/Mo interface may occur [26].

Table 3 shows the ratios of f_T and μ_{FE} with 1 and 0 mΩ.cm² of distributed R_C. These values reiterate that devices with smaller L are more affected by high R_C and that the SA TG structure is more advantageous to minimize these effects than its counterparts. This proves that the interface semiconductor/metal in oxide TFTs greatly benefits from localized doping of the semiconductor, creating a more ohmic contact and enhancing dynamic and static device performance. With decreasing L, f_T and μ_{FE} ratios all decrease, in different proportions depending on the structure, reinforcing the idea that R_C optimization is vital to take full advantage of sub-micron oxide TFTs.

Table 3 - $f_T^{R_C=1\ m\Omega.cm^2}/f_T^{R_C=0\ \Omega.cm^2}$ and $\mu_{FE}^{R_C=1\ m\Omega.cm^2}/\mu_{FE}^{R_C=0\ \Omega.cm^2}$ for STG BG (L_{ov}= 0 µm), SA TG and Corbino TFTs.

	$f_T^{R_C=1\ m\Omega.cm^2}/f_T^{R_C=0\ \Omega.cm^2}$ (%)			$\mu_{FE}^{R_C=1\ m\Omega.cm^2}/\mu_{FE}^{R_C=0\ \Omega.cm^2}$ (%)		
L (µm)	STG BG	SA TG	Corbino	STG BG	SA TG	Corbino
5	63	83	43	67	83	71
1	14	59	12	43	67	43
0.6	7	13	7	33	59	33

4.2.4.3. Output characteristics

Figure 15 shows a comparison between output curves for all devices, for the cases of null and high R_C.

It is noticeable that higher R_C causes the current crowding effect, i.e. the linear region of the output curve has a less steep slope and is dragged to higher V_{DS}.

Regarding the levels of I_{DS}, STG BG devices have the highest I_{DS} for all L values when $R_C = 0\ \Omega.cm^2$. However, when R_C becomes significant, the highly doped areas present in the SA TG structure form a better semiconductor/metal interface, making the effects R_C on I_{DS} values less noticeable, as discussed. It is also worth noticing that, despite being less affected by R_C, SA TFTs will always have more R_A since the effective S/D metal contacts are not in direct contact with the active layer. The R_A value depends essentially on the doping level of the S/D areas and it can have a more detrimental impact than R_C on DC and AC metrics of these devices, if not low enough. Current crowding is also present in Corbino devices, however to a much lesser extent than for the STG BG or SA TG architectures (saturation regime starts at lower V_{DS} for Corbino TFTs with $R_C = 1\ m\Omega.cm^2$).

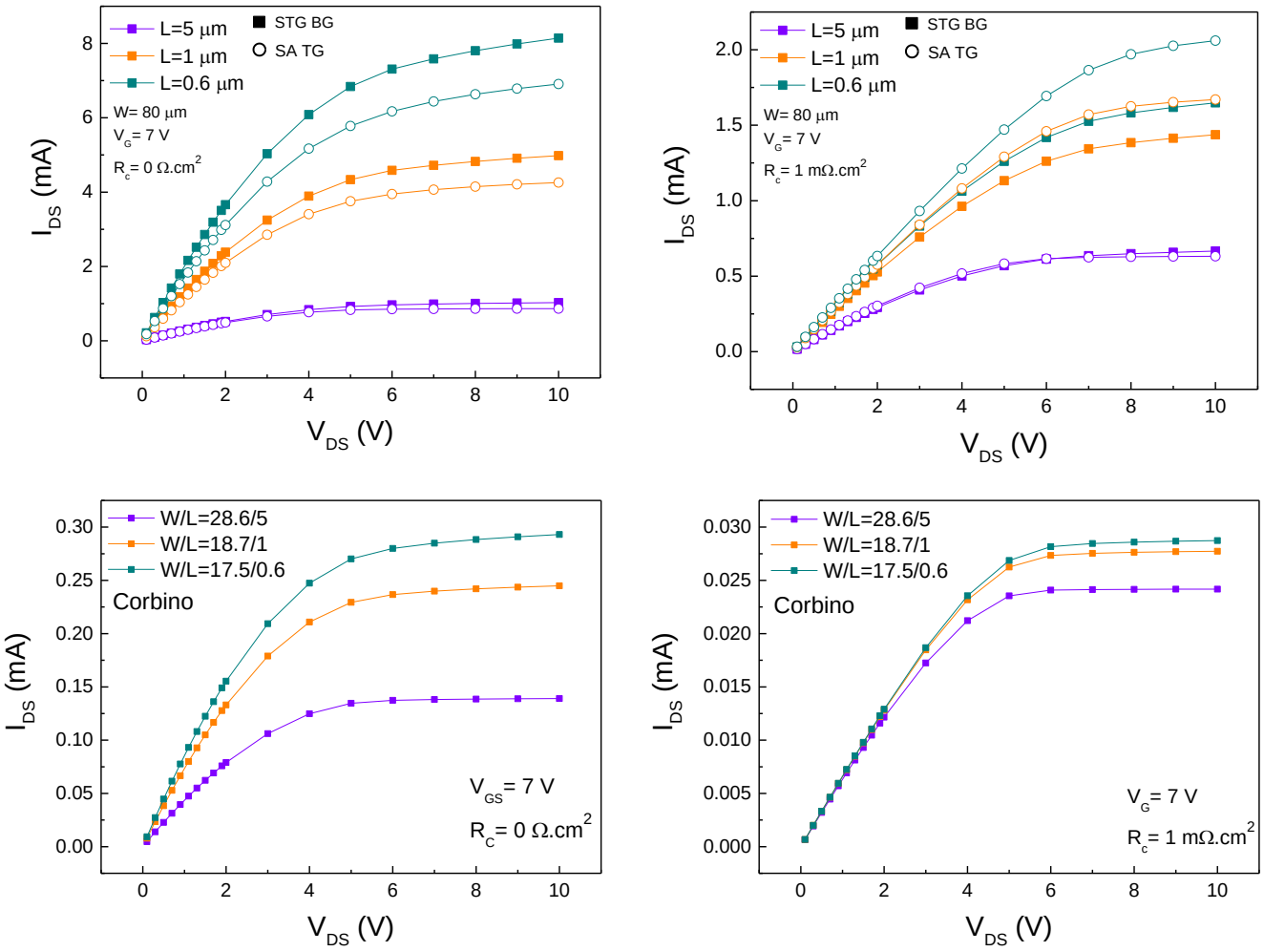

Figure 15 - Output characteristics for STG BG, SA TG and Corbino structures and different L, for $R_C = 0\ \Omega.cm^2$ and $R_C = 1\ m\Omega.cm^2$

4.3. Ar plasma doping

Ar plasma treatments showed to be effective at lowering a-IGZO sheet resistance (R_S). Results obtained via IV measurements on the probe stations and Hall effect measurements of R_S were found to be very similar, considering a 40 nm a-IGZO film. It was not possible to measure the electrical characteristics of a-IGZO films without doping as their resistance was too high.

Figure 16 a) shows R_S dependence on plasma treatment time for both employed plasma powers. For a

power of 60 W, R_S is the lowest for treatment times ranging from around 300 to 420 s, resulting in a R_S value of about 715 Ω/□. R_S values saturate from a treatment time of 150 s onwards. For a power of 250 W, the lowest value of R_S is 639 Ω/□ and is found at a treatment time of 30 s. Nevertheless, R_S values are very similar, ranging from 30-60 s treatment time. For higher treatment times, the high-power plasma much likely becomes too aggressive on the a-IGZO thin film, probably permanently damaging its chemistry or effectively physically etching the whole thickness of the film.

TCAD simulation results show an inversely proportional relationship between a-IGZO's resistivity (ρ) and N_D, up to a 10^{21} cm^{-3} carrier concentration (Figure 16 b). The results obtained through Hall measurements are reasonably coincident with this linear tendency, for both Ar plasma powers. The condition used in SA TG TFT fabrication (250W 30s) showed $N_D = 3\times10^{20}$, $\rho = 2.8\times10^{-3}$ Ω.cm and Hall mobility (μ_H) of 8.9 cm^2/V.s.

Some fabricated samples were left exposed to air for one week and were characterized via I-V characteristics again. A trend of resistance values doubling was observed, thus R_S and ρ values as well. This indicates that the highly conductive films eventually reach equilibrium with air, with some of the V_O being filled within this time frame, diminishing the number of free carriers available in IGZO. Still, considering the entire fabrication process of the SA TG TFT stack, this effect is less prone to happen, as the highly doped regions of IGZO are covered with interlevel dielectric and metal layers.

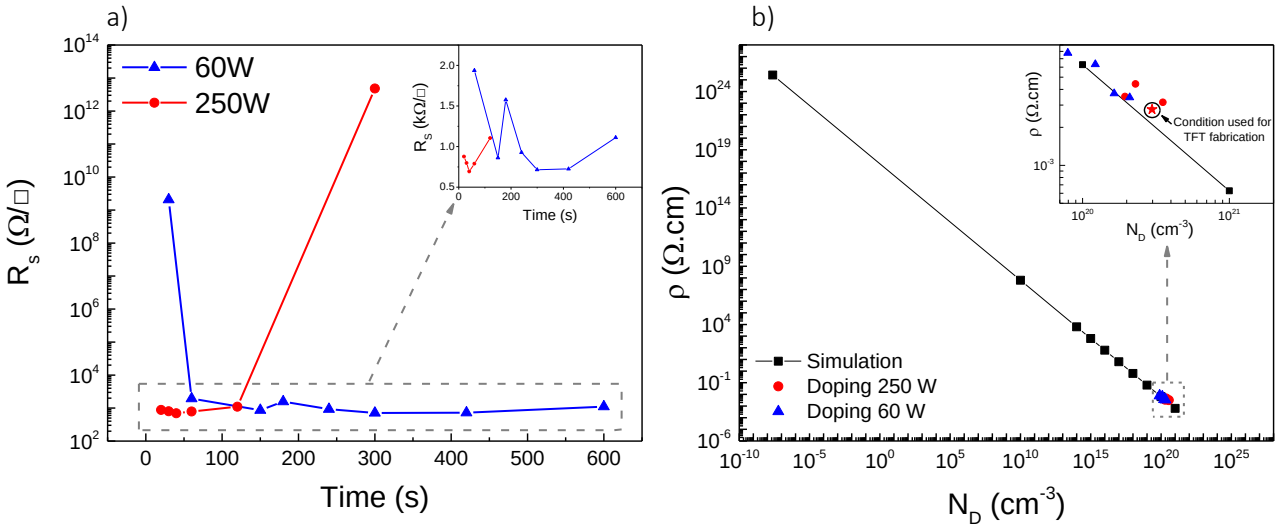

Figure 16 - a) IGZO R_S as a function of Ar treatment power and time. b) IGZO ρ dependence on N_D (simulated) and experimental points.

4.4. SA TFTs

Since SA TFTs were a new type of device configuration at CENIMAT (Centro de Investigação de Materiais), tasks such as layout design and optimization of the lithographic steps were required. Critical lithographic steps for this structure are the definition of the semiconductor pads with positive PR and the definition of the gate electrode for sub-µm TFTs with negative PR. The schematic cross-section of this device structure is present in Figure 3 a).

4.4.1. Layout design

SA TG TFTs layout is present in Figure 17. Two types of semiconductor pad structures were designed: one with 250 µm × 250 µm S/D (Figure 18 a), aiming to reduce R_C and R_A; and other where the pad width is constant and corresponds to the W of that device (Figure 18 b). The former structure will be referred to as butterfly (BF) and the latter will be called rectangle (RC).

Devices outlined with the dashed line in Figure 17 were fabricated: L of 80; 60; 40; 20; 10; 5; 3; 2; 1.5;

1 and 0.7 µm for W = 80 µm and L of 2; 1.5, 1 and 0.7 µm for W = 30 µm, for both semiconductor structures. Test structures for measuring the isolated electrical properties of the doped a-IGZO, gate, and contact metals were also designed.

In the BF structures, W is defined only by the central part of the semiconductor and not the pads. Thus, to ensure that W is uniform from drain to source, a misalignment margin (X_1 = 1 µm) was given for each side, concerning the gate electrode (Figure 18 a$_1$). Individual layouts for each layer can be found in Annex 5.

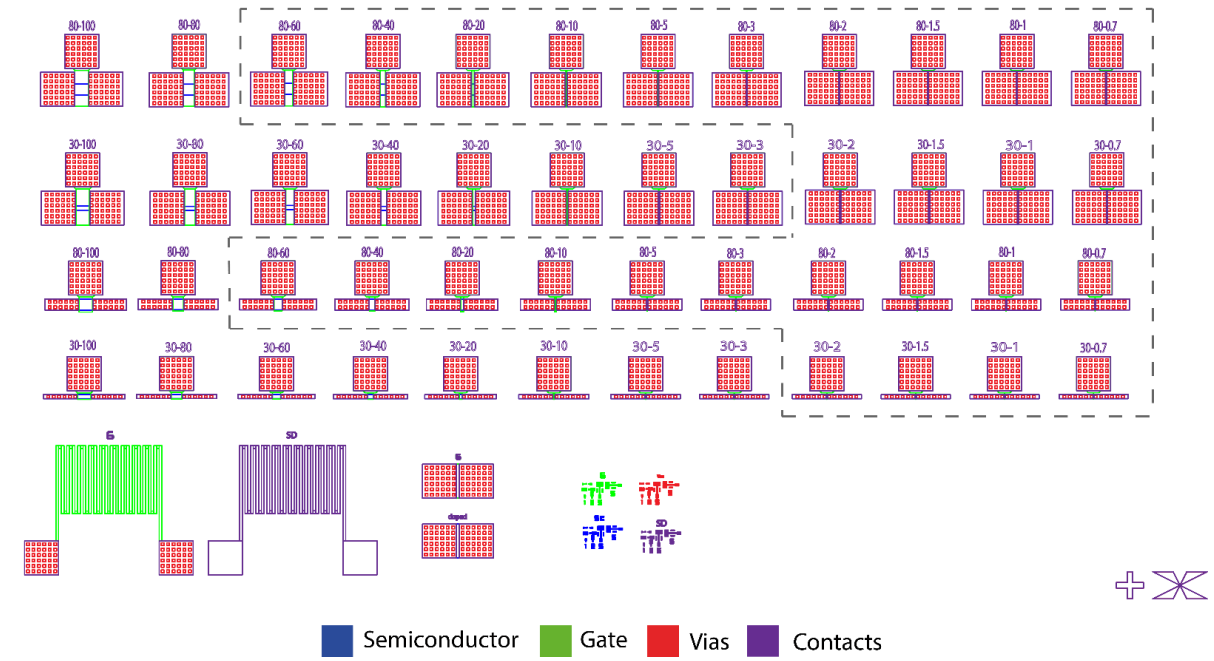

Figure 17 – Designed layout for SA TFTs.

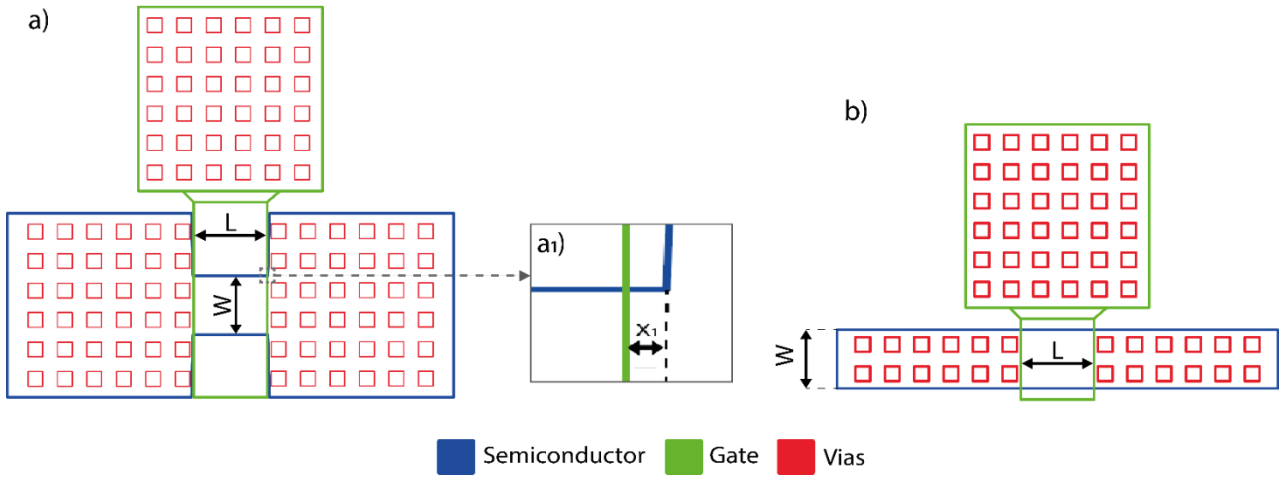

Figure 18 - a) BF-type SA TFTs; a1) Misalignment margin (X_1) related to the gate electrode; b) RC-type SA TFTs.

4.4.2. Definition of the semiconductor layer

For the BF structure, DLW conditions had to be optimized for positive PR (AZ ECI 3012). The minimum feature size required for the semiconductor layer was equal to the minimum designed L (L_{min} = 0.7 µm) plus two times X_1, totaling 2.7 µm. Figure 19 shows an example of the BF structure, for W = 30 µm and L = 0.7 µm. Figure 19 a) is the designed layout and Figure 19 b) shows the a-IGZO BF structure, after lift-off. The layout was transferred correctly onto positive PR, with the minimum feature size

of 2.7 µm being achieved for the aforementioned DLW laser conditions.

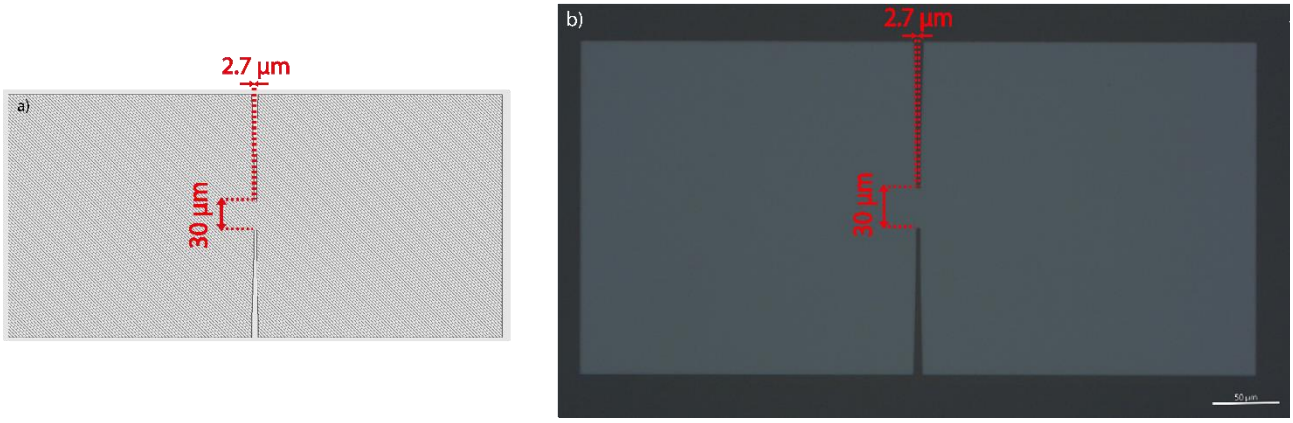

Figure 19 - BF-type semiconductor structure with minimum feature size. a) Layout; b) Micrograph of DLW patterned IGZO layer.

4.4.3. Definition of the gate electrode

In SA TG TFTs, L is ultimately defined by the gate length. Thus, it was imperative to optimize laser conditions before TFT fabrication, to achieve sub-µm devices. Lithography optimization was carried on 60 nm Mo, sputtered on Corning glass, to mimic the conditions of TFT fabrication.

The layouts used for these resolution tests are present in Figure 20. The layout in Figure 20 a) was used for the first resolution tests and later on it was updated for the layout in Figure 20 b), since the latter took much less time to expose. However, no influence on the obtained resolutions should result from this layout change, since the success of these resolution tests was measured by the width of the two rightmost lines. These lines were used to infer the minimum feature sizes for each DLW laser condition and had a projected width of 1 µm and 0.7 µm, respectively from left to right.

Figure 21 a) shows the micrograph of the obtained pattern with the mentioned laser conditions, patterned onto 1.2 µm thick AZ nLOF 2020 and developed with undiluted AZ 726 MIF for 15s, followed by Mo dry-etching and PR removal. 0.765 µm wide lines were obtained, being this value in line with what was deemed necessary for devices with L_{min} and with the equipment resolution. However, reproducibility tests failed due to the hard-to-control development process. More specifically, development time was hard to control with such a narrow time window, and a few extra seconds caused the high-resolution lines to completely vanish. To counteract this, the developer was diluted in DI water and resolution tests were repeated. The development process was much easier to control, with development time rising to 210 s. However, as shown in Figure 21 b), the achieved resolutions were not as high, with both line widths raising about 210 nm, totalling

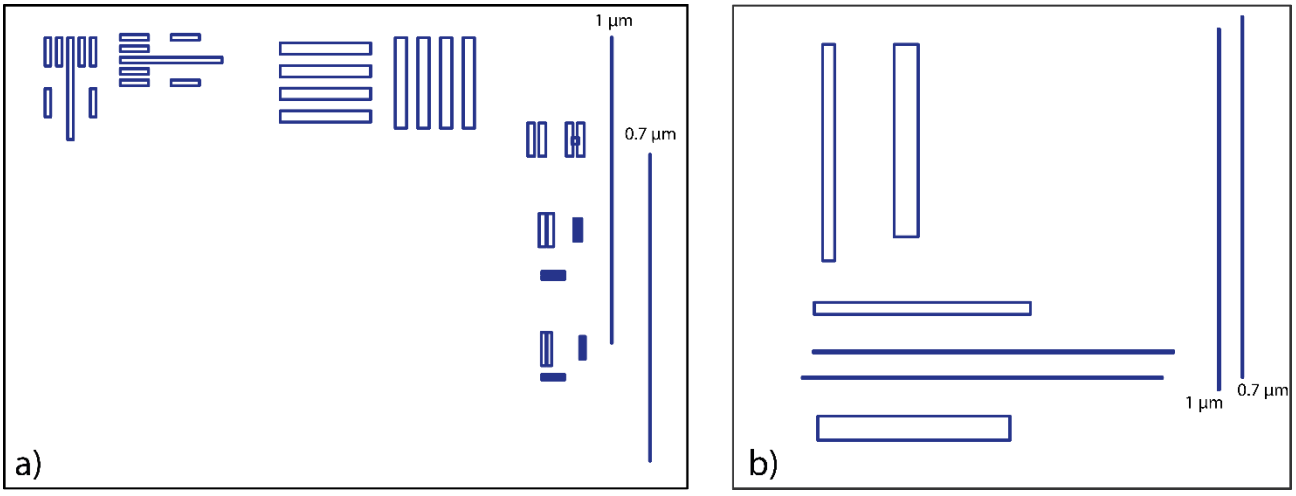

Figure 20 - Layouts for resolution tests with DLW.

0.91 µm for the projected 0.7 µm line. Nevertheless, this was a far more controllable and reproducible process and it was adopted for SA TG TFT fabrication.

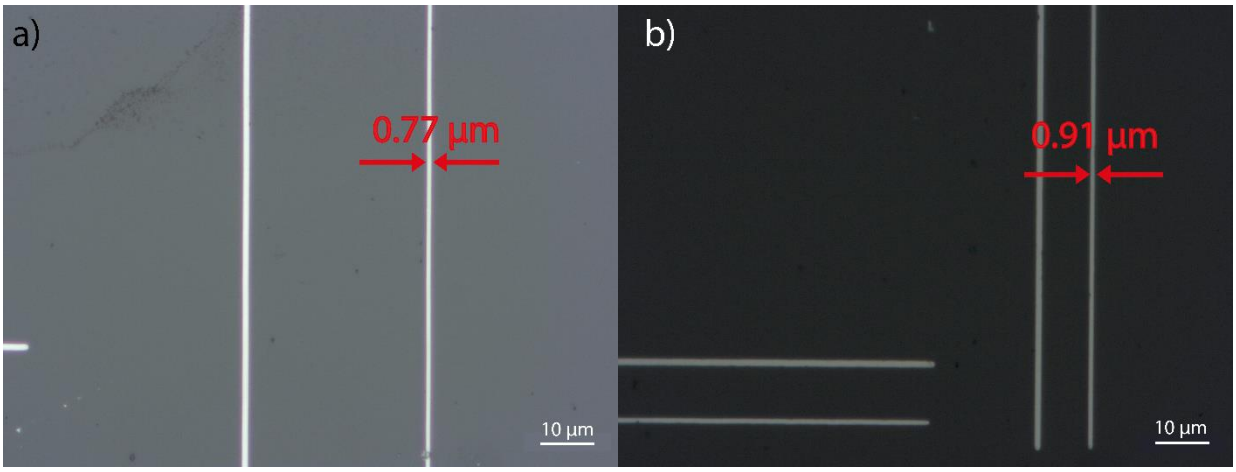

Figure 21 - Micrographs of the DLW patterned Mo lines on Corning glass. a) Developed with undiluted developer for 15 s; b) Developed with 3:1 developer to DI water for 210 s.

4.4.4. SA TG TFTs fabrication

4.4.4.1. Gate Layer

After a-IGZO pad definition, deposition of dielectrics, and Mo, the gate layer was defined using the aforementioned optimized process for nLOF 2020. Figure 22 a) and b) show an overview of SA TG TFTs after patterning the gate electrodes by dry-etching. Figure 23 c) and d) show the devices with the projected $L_{\min}$ of 0.7 µm, for samples 1TG and 2TG respectively. Sample 1TG showed a $L_{\min}$ of around 0.64 µm and in sample 2TG that value was reduced to 0.52 µm. This discrepancy was consistent across different measurements. Such differences in the minimum feature size, especially when compared to the 0.9 µm obtained in the resolution tests could hypothetically be explained by the differences in thermal conductivity (K) of the different layers.

Accordingly, Figure 23 a) shows a schematic cross-section of the different layers comprising the resolution test samples and samples 1TG and 2TG. K_{Mo} =138 W/m.K[2], whilst $K_{Al_2O_3}$ ranges from 12 to 38.5 W/m.K[1] and $K_{Parylene-C}$ = 0.082 W/m.K[3]. nLOF series resists are very sensitive to the PEB step and, as depicted in Figure 23 b), a 10 °C difference in PEB temperature can result in a narrower base of the PR lines, with nearly half the width than the top[4]. Given the fact that the lowest obtained minimum feature sizes were for sample 2TG – in which parylene-C acts as the GD – it is reasonable to assume that, due to parylene's lower K, the PEB was performed at a lower temperature than the projected 115 °C, thus resulting in a PR profile with a narrower base, which would allow for narrower Mo lines after dry-etching.

To confirm this hypothesis, two samples were fabricated: one with p-type Si wafer as a substrate and the other with Kapton tape glued onto Corning glass. Both samples underwent a 60 nm Mo deposition and the resolution tests mask (Figure 20) was used to pattern nLOF 2020. DLW conditions, soft-bake, PEB, and development procedure were kept the same as in the fabrication of SA TG TFTs.

[2] Engineering ToolBox, "Thermal Conductivity Coefficients for common Solids, Liquids and Gases." https://www.engineeringtoolbox.com/thermal-conductivity-d_429.html (accessed Nov. 11, 2021).

[3] Para-Coat Technologies, "Parylene Thermal Properties." https://pctconformalcoating.com/parylene/parylene-thermal-properties/ (accessed Nov. 11, 2021).

[4] Merck KGaA, "Technical Datasheet - AZ® nLOF™ 2000 Series ." Accessed: Nov. 11, 2021. [Online]. Available: https://www.microchemicals.com/micro/tds_az_nlof2000_series.pdf

Micrographs of Mo lines on both samples after dry-etching and PR removal are present in Figure 24. Si sample underwent SEM characterization, due to the very small feature sizes. The 0.7 µm projected lines on the Si (Figure 24 a) sample showed an average width of 0.45 µm with a standard deviation of 0.04 µm, across the whole sample. Measurements driven from optical and electronic microscopy imaging were also coincident. The 0.7 µm projected lines presented a mean width 0.69 µm for the Kapton sample (Figure 24 b), with a standard deviation of 0.15 µm across the whole sample. This higher standard deviation probably results from the unevenness of the glued-on Kapton tape substrate versus a crystalline Si wafer. Since K_{Si} =150 W/m.K[1] is much greater than the thermal conductivities of Corning glass and Kapton tape ($K_{Corning}$ = 1.31 W/m.K[5]; K_{Kapton} =0.12 W/m.K[6]), the stated hypothesis was not confirmed with these tests. This highlights that, before the patterning of the gate electrodes, test samples (employing similar material stacks) should always be performed to assess the suitable development time and conditions for the desired feature sizes. This is known

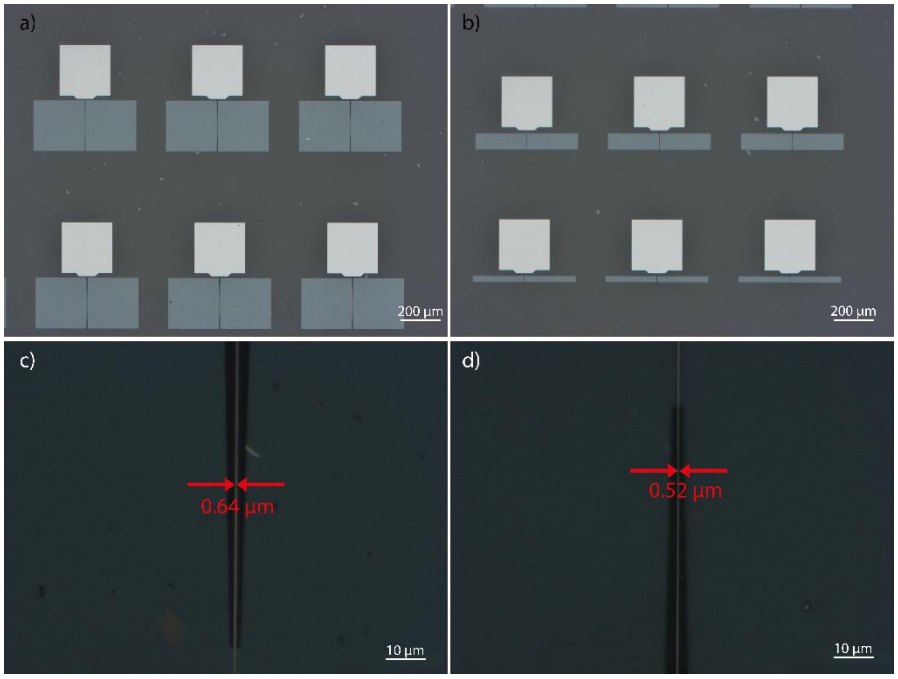

Figure 22 - Micrographs of SA TFTs after gate layer patterning by DLW. a) overview of the BF-type structures; b) Overview of the RC-type structures; c) 100x zoom on the gate electrode for projected L = 0.7 µm in Sample 1TG, showing a L = 0.64 µm; d) 100x zoom on the gate for projected L = 0.7 µm in Sample 2TG, showing a L = 0.52 µm.

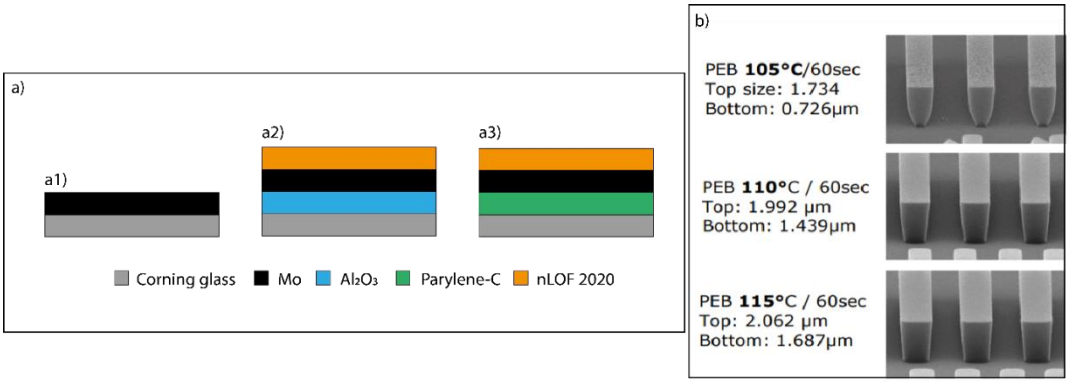

Figure 23 - a) Schematic cross-sections. a1) DLW resolution test samples; a2) SA TG TFTs with parylene-C as the gate dielectric (Sample 2TG); a2) SA TG TFTs with Al2O3 as the gate dielectric (Sample 1TG). b) PEB temperature influence on AZ nLOF 2020 profile. Adapted from [3].

[5] AZO Optics, "Physical and Mechanical Properties of Corning Glass ULE by Insaco," 2021. https://www.azooptics.com/Article.aspx?ArticleID=250 (accessed Nov. 11, 2021).

[6] Dupont, "Material Properties - Polyimide." https://www.mit.edu/~6.777/matprops/polyimide.htm (accessed Nov. 11, 2021).

to be required for such critical fabrication steps when working near the limit resolution of said lithographic processes[3]. Other properties such as surface roughness or energy of the material on which nLOF is deposited can also affect line resolution. Nevertheless, it should be noted that all the fabrication steps for SA TG TFTs are compatible with flexible electronics and, as shown by the tests carried on the Kapton substrate, sub-µm feature sizes can be achieved with good quality on flexible substrates.

Figure 24 c) shows some nLOF residue still left on the sample. The PR becomes heavily cross-linked after Mo dry-etching with SF_6 and is hard to fully remove it even after immersing the sample in acetone for a long time. However, this is hard to observe in optical microscopy. For further process optimization it is suggested to use a stronger PR stripper or even O_2 plasma to ensure minimal organic residue contamination on fabricated devices [5].

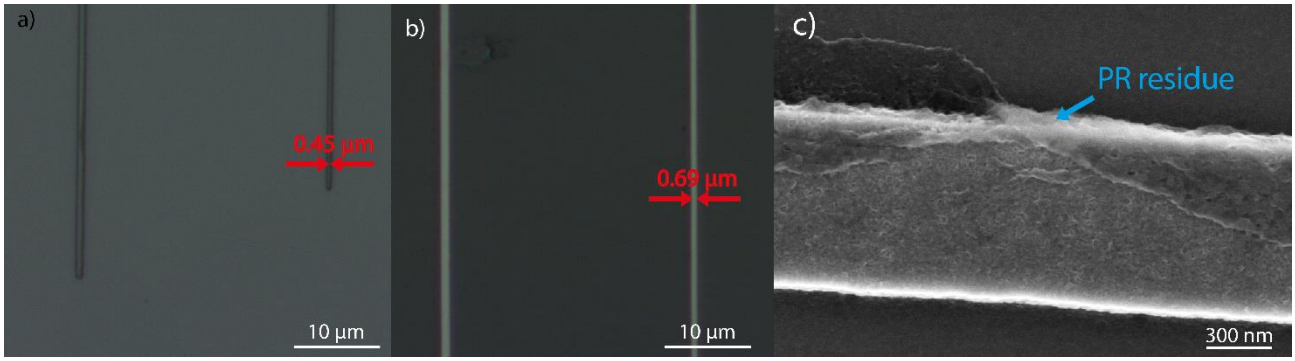

Figure 24 - Micrographs of Mo lines on a) Si susbtrate; b) Corning + Kapton substrate. c) SEM micrograph of Mo lines on Si, depicting PR residue.

4.4.4.2. Contacts layer

Figure 25 a) and b) show samples 1TG and 2TG after contact pad definition, respectively. It is possible to see that contact pads are poorly defined and most are short-circuited (Figure 25 c), for both samples. Nevertheless, sample 2TG showed a worse pad definition than its counterpart. This happened for the TFTs themselves and also for the test structures. This result was attributed to the high power (175 W) used in Mo sputtering process on top of the interlayer dielectric. The high-power plasma probably randomly removed sizable chunks of the interlayer, leaving its surface very uneven in terms of roughness. Thus, it was impossible to perform lithography with quality afterward. Lowering the power of the Mo sputtering deposition would at least attenuate this issue, despite leading to a slightly more resistive Mo thin-film. However, these changes could not be implemented on time, due to the proximity of the delivery date of this document.

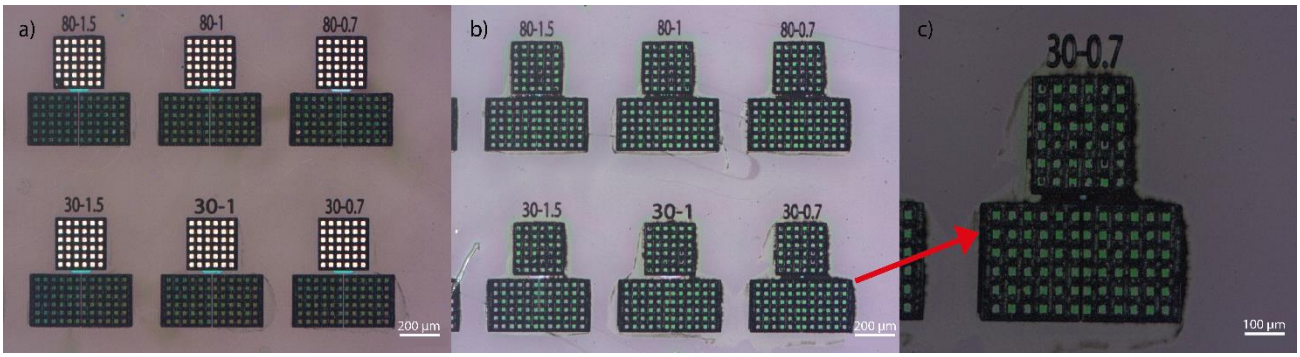

Figure 25 – Finalized SA TG TFTs, after contact pad fabrication. a) Sample 1TG; b) Sample 2TG c) BF-shaped device of sample 2TG, showing short-circuited contact pads

4.4.5. Electrical characterization

4.4.5.1. Linear and saturation transfer characteristics

As aforementioned, most fabricated devices were short-circuited by the end of the fabrication process,

however, it was possible to electrically characterize the following TFTs in sample 1TG: $W/L = 80/60$ and $W/L = 80/40$, for BF structure and $W/L = 80/60$ for the RC structure. As for sample 2TG, all devices were short-circuited and/or presented high gate leakage currents (I_G). This is certainly related to the sensitivity of parylene-C to the Mo sputter deposition. Mo is deposited at two different steps on top of parylene-C, in sample 2TG: when constructing the gate stack and when depositing contacts. Damaging the parylene-C layer at the former step would effectively result in high I_G since it acts as the GD. The poor lithography resolution resulting from damaging the interlayer dielectric at the latter step results in short-circuited contact pads. Accordingly, all the presented electrical measurement results in this section refer to sample 1TG.

Before TFT characterization, it is important to perform a set of measurements to achieve device stabilization and extract reliable results. Example stabilization curves are presented in Figure 26 for $W/L = 80/60$ RC-shaped device. Stabilization curves for all devices looked rather similar. All characteristics show a hump-like profile. This phenomenon has been attributed to parasitic TFTs, edge effects, formation of defects in the semiconductor or back-channel conduction, under positive gate bias stress tests with either temperature or illumination [27].

The transfer profile shows two distinct behaviours. In the first part of the curve, measurements are very coincident and, from the hump forward, transfer characteristics show a right-shift. The right-shift behaviour is well known and is related to electron trapping at the semiconductor/dielectric interface [28]. Due to the distinct characteristics of the pre and post-hump characteristics, it is plausible to assume that a parasitic TFT might be present. More specifically, the hump behaviour can arise from edge effects, which themselves are related to the slanted edges of the semiconductor layer in the W direction (Figure 27). It was reported that these edges presented higher carrier densities than the central part of the semiconductor and thus acted as parasitic TFTs [28,29]. To rule out atomic composition issues with the a-IGZO film, EDS analysis was performed, showing a 2:1:1 InGaZn atomic ratio, as projected. However, it is not possible to infer the cause of these hump characteristics with certainty, due to lack of additional analysis and low TFT statistical sample size.

Post-stabilization linear and saturation transfer curves are presented in Figure 28, respectively. BF-shaped devices showed higher I_G than the RC-shaped TFTs. However, it is not possible to infer if this is a direct cause of the semiconductor pad structure itself due to the reduced statistical sample. High I_G could also be related to the existence of conductive paths between S/D and gate contact pads.

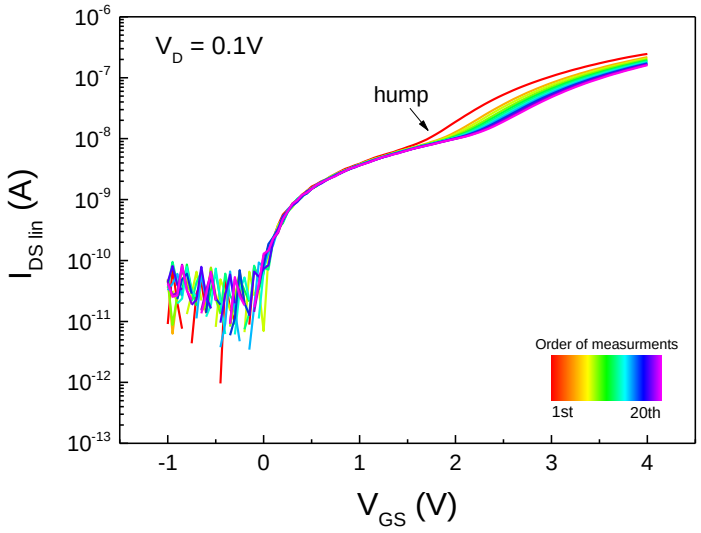

Figure 26 - Linear transfer stabilization curves for sample 1TG. Example for $W/L = 80/60$ RC-type device.

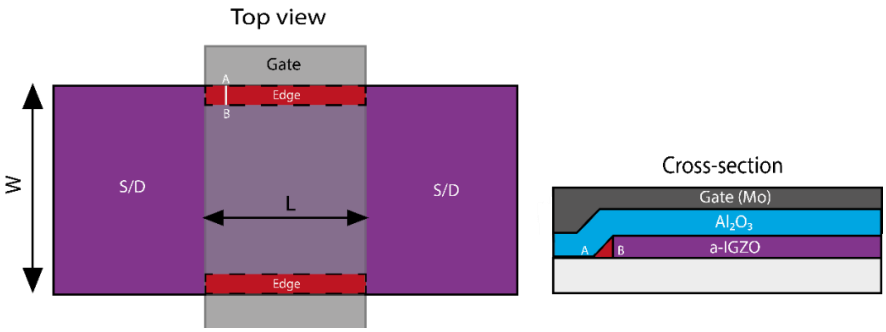

Figure 27 – Top view and cross-section schematic of the edge effects. Adapted from [28].

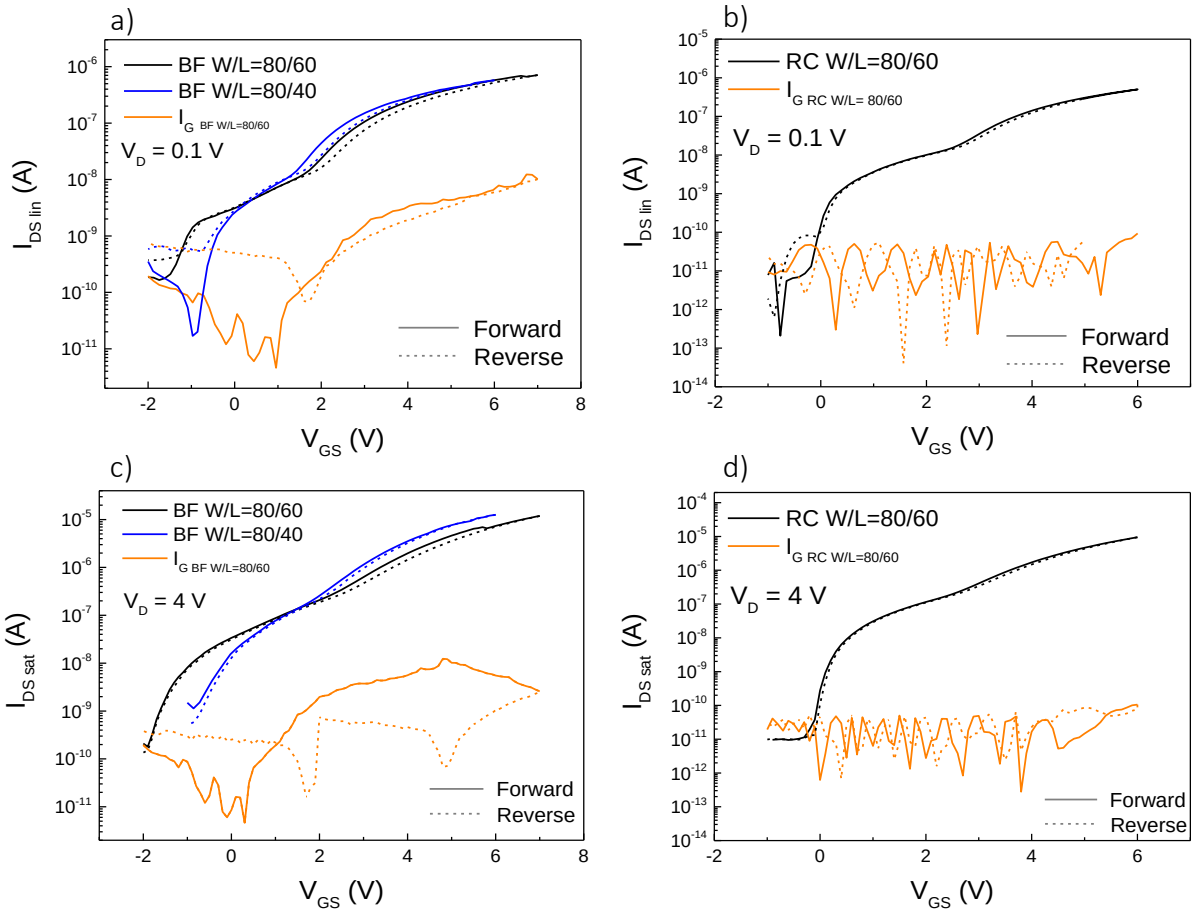

Figure 28 - Transfer characteristics for sample 1TG, with W/L = 80/60 for both BF and RC shaped TFTs and W/L = 80/40 for BF-shaped TFTs. a) Linear transfer in BF-shaped devices; b) Linear transfer in RC-shaped devices; c) Saturation transfer in BF-shaped device.

4.4.5.2. C-V and C-f curves

C-V and C-f curves are essential to gather information about TFTs' C_P/C_{ov} and about C_{ox}. Examples of the obtained C-V and C-f curves are depicted in Figure 29, for the BF-shaped device with $W/L = 80/60$. The obtained results were consistent amongst all devices, and the average values obtained were: $C_P = 0.52$ pF and $C_{ox} = 137$ nF/cm^2 (at 1 kHz). Values extracted from C-V and C-f curves showed concordance. The hysteresis present in the C-V curve is related to electron trapping at the semiconductor/dielectric interface. Note that device stabilization was not performed prior to C-V curve extraction, thus explaining the appearance of hysteresis here, unlike what is shown for the transfer characteristics. Since there are no overlaps between S/D and gate electrodes in SA devices, the obtained C_P value can result either from the measurement equipment resolution or from the eventual diffusion of a-IGZO dopants from the S/D areas to the active layer. This

diffusion could effectively create C_{GS} and C_{GD} parasitic capacitors, in which the capacitance value would depend on the diffusion length. Additionally, dopant diffusion would reduce L_{eff} [30]. The assessment of C_P for devices with different W and L would clarify the origin of this capacitance.

C-f curve in accumulation ($V_{Bias} = 4$V) (Figure 29 b) shows a decrease in capacitance as the frequency increases. It has been reported that, for a-IGZO TFTs, the capacitance dependence on frequency can be related to the frequency response of the trapped charges. With increasing frequency, trap states are unable to follow the applied voltage, thus their contribution to semiconductor capacitance decreases, resulting in a decrease of measured capacitance. This effect has also been attributed to the finite resistance of the a-IGZO channel in accumulation [31,32]

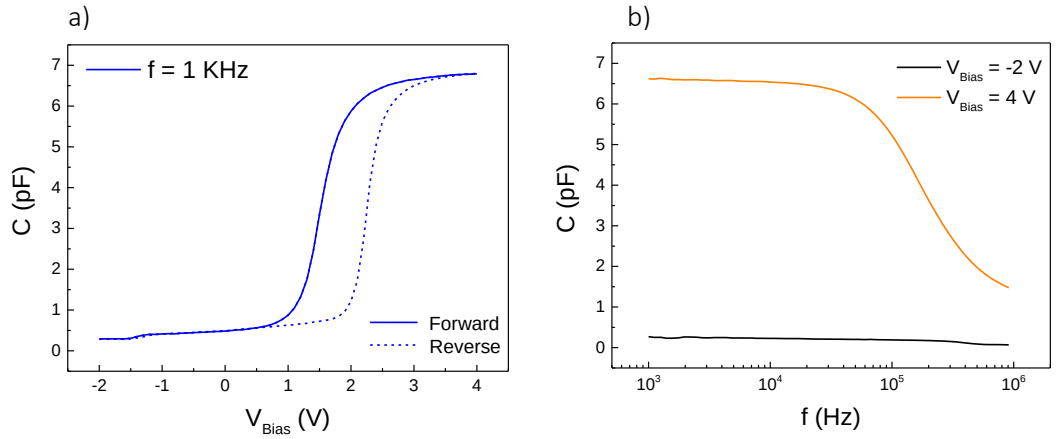

Figure 29 - Capacitance characteristics for SA TG TFT, BF shaped device with $W/L = 80/60$ a) C-V; b) C-f.

4.4.5.3. Output curves

Output curves can be found in Figure 30. BF-type TFT with $W/L = 80/40$ shows some current crowding, indicating a higher R_C. This is probably due to the unevenness of the Mo contacts since the other

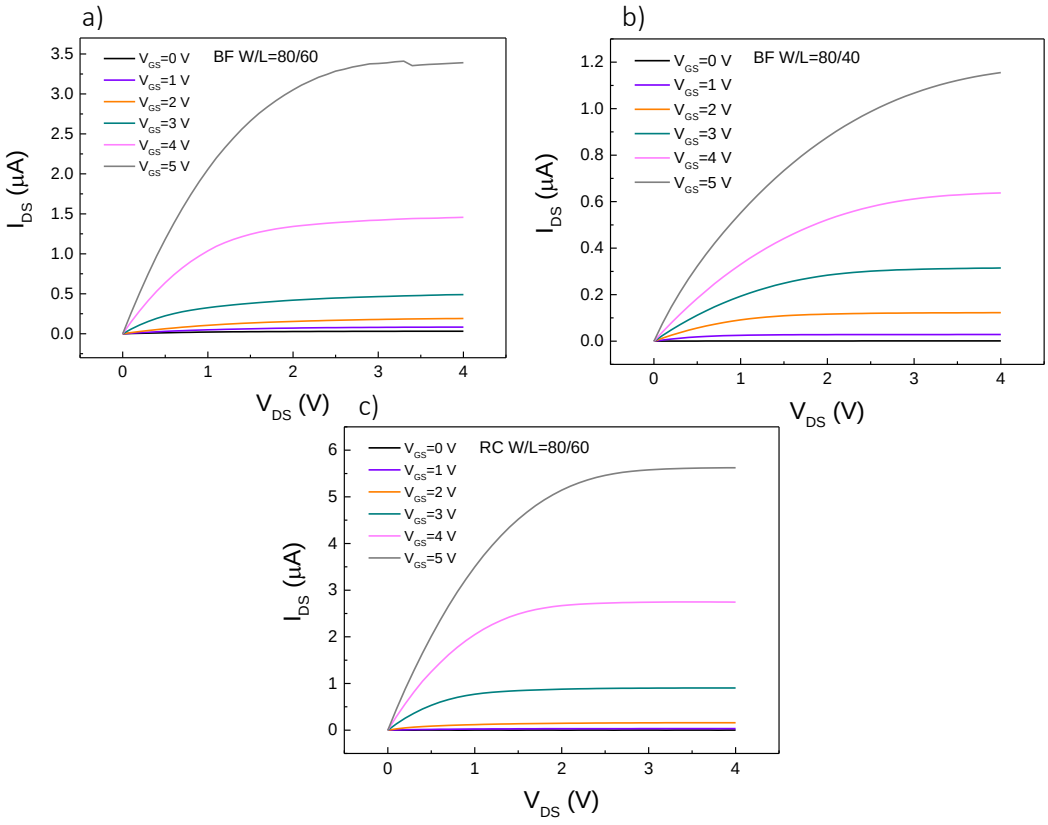

Figure 30 - Output characteristics for sample 1TG. a) BF-shaped device with W/L = 80/60; b) BF-shaped device with W/L = 80/40; c) RC-shaped device with W/L = 80/60.

TFTs show good output characteristics without signs of high R_C. This means that the interface n^+ IGZO/Mo has small R_C and that the doped a-IGZO areas themselves are highly conductive, resulting in a low R_A. This is also apparent from the reasonable values of μ_{FE} obtained for these devices, shown in Table 4. However, it is not possible to infer the actual values of R_C through the TLM since just a few devices work properly. Additionally, BF-type TFT with $W/L = 80/40$ shows lower output current than the ones with $L = 60$ µm, while an opposite result would be expected. This further indicates that the Mo contacts layer is probably very uneven.

4.4.5.4. Summary of electrical characteristics

Table 4 presents the obtained average values for V_{TH}, μ_{FE}, μ_{SAT}, μ_{eff}, ON/OFF, SS, gm_{SAT}, C_G, f_T and normalized $\boldsymbol{A_V}$. The average obtained ε_r for Al_2O_3 was 7.7. V_{TH} values are positive, meaning the devices work in enhancement mode. All μ and SS values are very reasonable and are on par with other reported a-IGZO TFTs [1]. ON/OFF values are very small. This is certainly related to the small W/L of the characterised devices, resulting in a low ON I_{DS}. Another aspect impacting this are the large OFF I_{DS}. (Figure 26), because of the large I_G that arises due to damaged GD by the high-power deposition of the gate electrode. Considering the large L of the devices, the obtained values for f_T are reasonably high when compared with other reports [1].

Table 4 – Obtained average values of V_{TH}, μ_{FE}, μ_{SAT}, μ_{eff}, ON/OFF, SS, gm_{SAT}, C_G, f_T and $A_V \times L/W$ for sample 1TG

Device	$\boldsymbol{W}$ **(µm)**	$\boldsymbol{L}$ **(µm)**	$\boldsymbol{V_{TH}}$**(V)**	$\boldsymbol{\mu_{FE}}$ **(cm²/V.s)**	$\boldsymbol{\mu_{SAT}}$ **(cm²/V.s)**	$\boldsymbol{\mu_{eff}}$ **(cm²/V.s)**	**ON/OFF**
BF	80	60	2.4	10.2	6.9	15.2	10^3
		40	1.9	7.6	4.9	13.7	10^4
RC		60	3	11.3	7.7	13.7	10^4
Device	$\boldsymbol{W}$ **(µm)**	$\boldsymbol{L}$ **(µm)**	$\boldsymbol{SS}$ **(V/dec)**	$\boldsymbol{gm_{SAT}}$ **(µS)**	$\boldsymbol{C_G}$ **(pF)**	$\boldsymbol{f_T}$ **(MHz)**	$\boldsymbol{A_V \times L/W}$
BF	80	60	0.510	4.88	6.6	0.12	6619
		40	0.195	5.28	4.4	0.19	3522
RC		60	0.178	5.70	6.6	0.14	8066

4.5. BG TFTs

BG TFTs were fabricated with an STG configuration. It is important to note that these devices were fabricated with the same processes as the SA TG, including doping in the S/D a-IGZO regions that contact Mo. This was simply because, for TLM, a big sample size of devices was needed, which would take too long

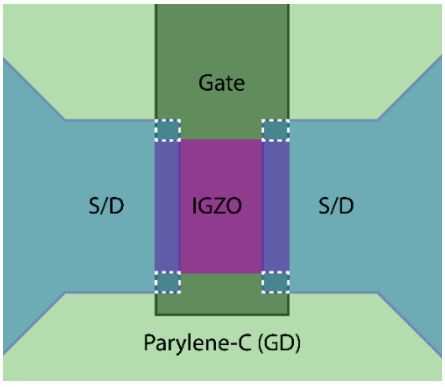

Figure 31 – Layout schematic for STG BG TFTs, depicting the areas where S/D metal deposition may cause removal of the parylene-C gate dielectric layer (in dashed white).

if fabricated by DLW. Thus, it was decided to use a traditional mask aligner for this case, since very high resolutions were not a major concern.

The schematic cross-section of these devices is present in Figure 2 a). Much like what was reported for sample 2TG, sample 2BG also presented a high I_G and thus it was impossible to extract any quality electrical measurements. In the case of the STG BG structure, there are some layout areas (highlighted by the dashed lines in white in Figure 31) where S/D Mo is deposited on top of both the dielectric and the gate electrodes, which may explain the high I_G.

As for the Al_2O_3 STG BG samples (samples 1BG), output and transfer curves are presented in Figure 32, for a $W/L = 20/5$. Effects of a high R_C are observable in the linear regime, with severe current crowding. As a consequence, devices presented low μ_{FE} values of around 1 $cm^2/V.s$ and $\mu_{SAT} = 7.8$ $cm^2/V.s$. μ_{SAT} values are similar to those found for SA TG TFTs. All devices presented nearly the same characteristics, thus it was impossible to use them to infer about the R_C of the n^+ a- IGZO/Mo interface through the TLM. The origins of R_C and of the non-saturation behaviour are most likely related to process-induced contamination. It is worth mentioning that transfer curves do not show a pronounced hump profile like in SA TFTs. a-IGZO was deposited under the same conditions of SA TG and STG BG devices, so this makes it even more plausible that the hump profile seen in SA TG TFTs is related to edge effects or back-channel conduction rather than with defect generation in a-IGZO.

Figure 33 shows a C-V curve for a STG BG device with $W/L = 320/20$. C_P is 6.7 pF, which is nearly 13 times higher than in SA TG TFTs, demonstrating the effectiveness of the latter structure for reducing overlap capacitances.

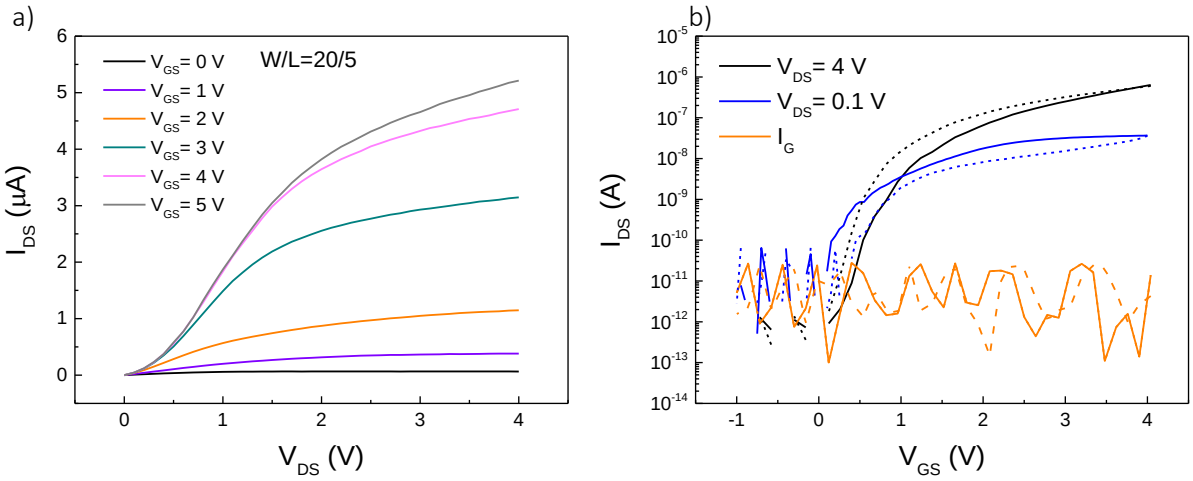

Figure 32 - Characteristics of sample 1BG for W/L = 20/5. a) Output; b) Linear and saturation transfer.

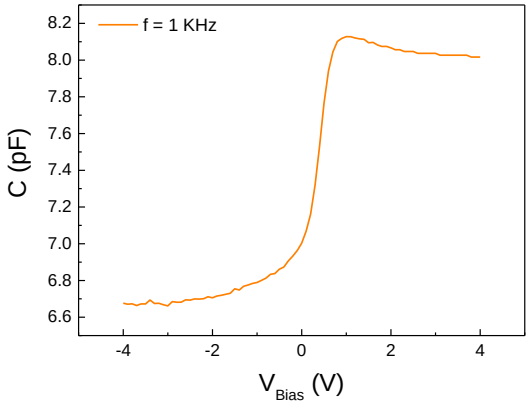

Figure 33 – C-V characteristic for STG BG device with $W/L = 320/20$.

5. Conclusions and future perspectives

The main focus of this work was to study different TFT device structures and evaluate their impact in terms of both AC and DC metrics, for future integration in high-speed flexible circuits.

TCAD simulation results showed that SA TG structures are very advantageous to eliminate the effect of C_{ov} and achieve higher electrical performance. For non-SA structures, careful optimization of L_{ov} must be conducted, given the opposite relationship that C_{ov} and R_C have with this geometrical feature. Furthermore, it was demonstrated that increasing N_D on S/D areas forms a better semiconductor/metal interface, attenuating the effects of R_C, besides providing a smaller R_A in SA TG TFTs versus undoped a-IGZO. Additionally, a-IGZO doping at the S/D interfaces could be applied to STG BG TFT structures and even Corbino TFTs by protecting the active layer region and treating with Ar plasma the exposed a-IGZO before S/D contacts deposition.

OE drain configuration Corbino TFTs are promising for scaled-down a-IGZO TFTs in applications where high r_{DS} is of major concern and current output is not as significant. Despite, the die-size of these devices is significantly larger than traditional TFT architectures. A reasonable contact metal width is necessary to not cap mobility values. Thus, an interesting research topic may rely on the investigation of short-channel Corbino TFTs with doped semiconductor at the semiconductor/drain/source interfaces. The big overlaps between gate and S/D are another drawback of this architecture. Perhaps another route worth exploring is Corbino TFTs fabricated by SA backside UV exposure.

a-IGZO doping by Ar plasma proved to be an easy and effective manner of increasing N_D, resulting in films with very low $\rho = 2.8\times10^{-3}$ Ω.cm, corresponding to $N_D = 3\times10^{20}$. These levels of doping provided R_A that do not limit DC and AC performances, even when considering lower L devices. Despite this, the stability of the electrical properties of the obtained films when left exposed to air is not the best, thus proper device passivation must be employed to assure that minimal gaseous exchanges occur once TFTs are fully fabricated.

The full process for SA TG was conceptualized and optimized. Proof-of-concept SA TG TFTs were successfully fabricated via DLW and characterized, with $W/L = 80/60$ and $W/L = 80/40$. μ_{eff} as high as 15.2 cm^2/V.s, as well as enhancement mode operation and satisfactory AC performance given device size. Output curves showed no signs of R_C, indicating the effectiveness of the S/D Ar doped regions.

Resolutions as high as 500 nm were achieved via DLW. Despite the impossibility of characterizing the short-channel SA TFTs, step-by-step analysis give good indications that these devices are achievable by making minor changes to the fabrication process. Unfortunately, it was not possible to remake those devices within the time frame of this dissertation.

Moving forward, the SA TG fabrication process should be optimised in the following aspects, before directing the focus to flexible electronic applications:

- Designing the layouts with a ground-signal-ground (GSG) contact pad structure to allow for AC characterization and S-parameter extraction [13];
- Investigate the cause of the hump-like characteristics. Due to the behaviour of the stabilization characteristics, parasitic TFTs and/or edge effects are the most likely cause of this phenomenon. When these effects are present, the hump generally appears at the same current for devices with different W. When the hump is caused by defects of the semiconductor or back-channel conduction, the current at which the hump appears is W dependant. Fabricating SA TG TFTs with an array of W values would allow inferring the causes of the hump-characteristics [27–29].

- Carrying out a more in-depth analysis of the discrepancies between minimum feature sizes in the different samples. This could be done by reproducing the process for both Al_2O_3 and parylene-C dielectrics several times and accompanying each TFT sample with a "dummy" sample that would undergo all the same depositions and process steps and evaluating the minimum feature sizes. With sub-µm features, lithography processes can be too volatile and hard to control, so statistical sampling is vital to either implement a solid and reproducible process or to make effective changes. Additionally, SEM imaging of all different samples would help gather a better and more error-free understanding on minimum feature sizes, since features under 1 µm are reaching the limits of optical microscopy.
- Protecting the active layer from process-induced contamination is of uttermost importance, due to IGZO's sensitivity to solutions commonly used for lithographic purposes [11]. This could be done by two main routes: by employing a thin dielectric channel protection layer or by using a thick and more resistant PR more indicated for lift-off, to avoid serious crosslinking. To apply the former method, the dielectric would have to form a good interface with a-IGZO and have reasonable chemical resistance. Al_2O_3 is a great candidate, however, this thin layer would have to be dry-etched from the S/D areas to avoid damage in the a-IGZO layer underneath and to make access for the doping process. As for the latter method, negative resists are known to be more mechanically and chemically resistant than their positive counterparts. However, using a negative resist for lift-off of the semiconductor layer would require a significantly longer exposure time in the DLW equipment, since it would imply exposing the negative of the semiconductor layout.
- Fabricating devices of different L and the same W with the same process flow is very important to infer dopant diffusion to the active layer and R_C in SA TFT (through TLM). This will be especially relevant for the devices with smaller L. Besides, inferring about R_C at the n+ a-IGZO/ Mo interface is useful to determine which pad structure (BF or RC type) is the most suitable for these TFTs. If the mentioned interface presents high R_C values, the BF-type layout is more interesting given that the contact area is bigger. However, in circuit implementation, the die-size of these devices will be much larger compared to the RC-type ones, which makes them less ideal for implementation in high-density circuitry.

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Annexes

Annex 1 – Parameters for TCAD simulation

Table A.1 – TCAD simulation parameters for IGZO.

E_G (eV)	E_{GD} (eV)	N_C (cm^{-3})	N_{GA} (cm^{-3}/eV)	N_{GD} (cm^{-3}/eV)	N_{TA} (cm^{-3}/eV)	N_{TD} (cm^{-3}/eV)	N_V (cm^{-3})
3.1	2.9	10^{18}	0	0	0	0	4.5×10^{21}
W_{GD} (eV)	**W_{TA} (eV)**	**W_{TD} (eV)**	**μ_n ($cm^2/V.s$)**	**μ_p ($cm^2/V.s$)**	**σ_T (cm^{-2})**	**χ (eV)**	
0.1	0.1	0.1	10	0.1	10^{-15}	4.16	

Table A.2 – Contact, dielectric, and temperature parameters for TCAD simulation.

ϕ_{Mo} (eV)	4.53
ϕ_{Gate} (eV)	4.53
$\phi_{S/D}$ (eV)	4.16
ρ_{Mo} (μΩ.cm)	5.2
$\varepsilon_{r\,Ta_2O_5}$	25
T (K)	300

Annex 2 – Shadow masks for E-beam evaporation

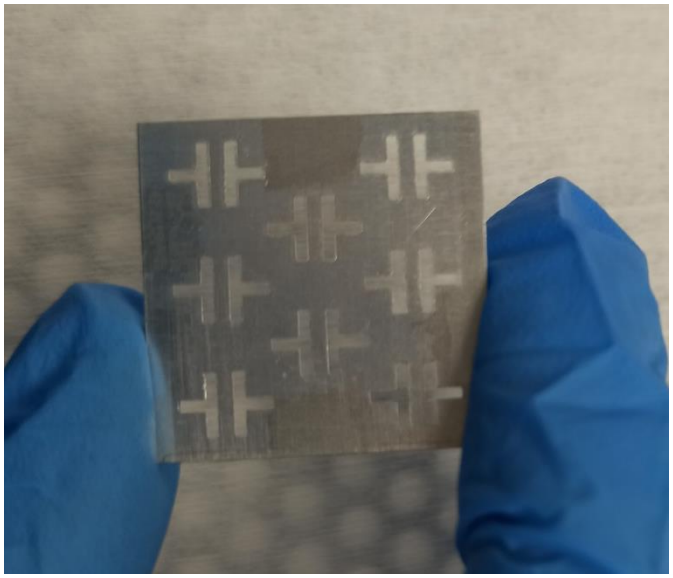

Figure A.1 – Shadow mask used for e-beam evaporation (probe station samples).

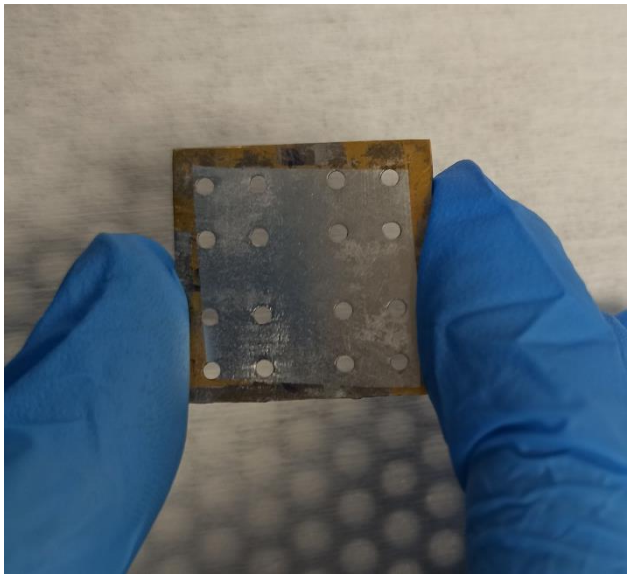

Figure A.2 – Shadow mask used for e-beam evaporation (Hall effect samples).

Annex 3 – SA TG TFTs process flow

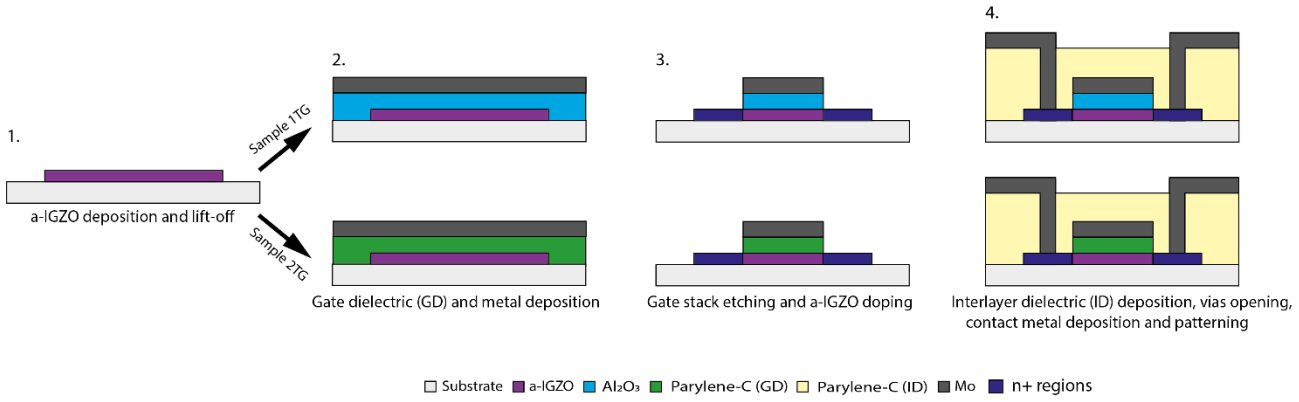

Figure A.3 – Schematic process flow of SA TG TFT fabrication.

Annex 4 – STG BG TFTs process flow

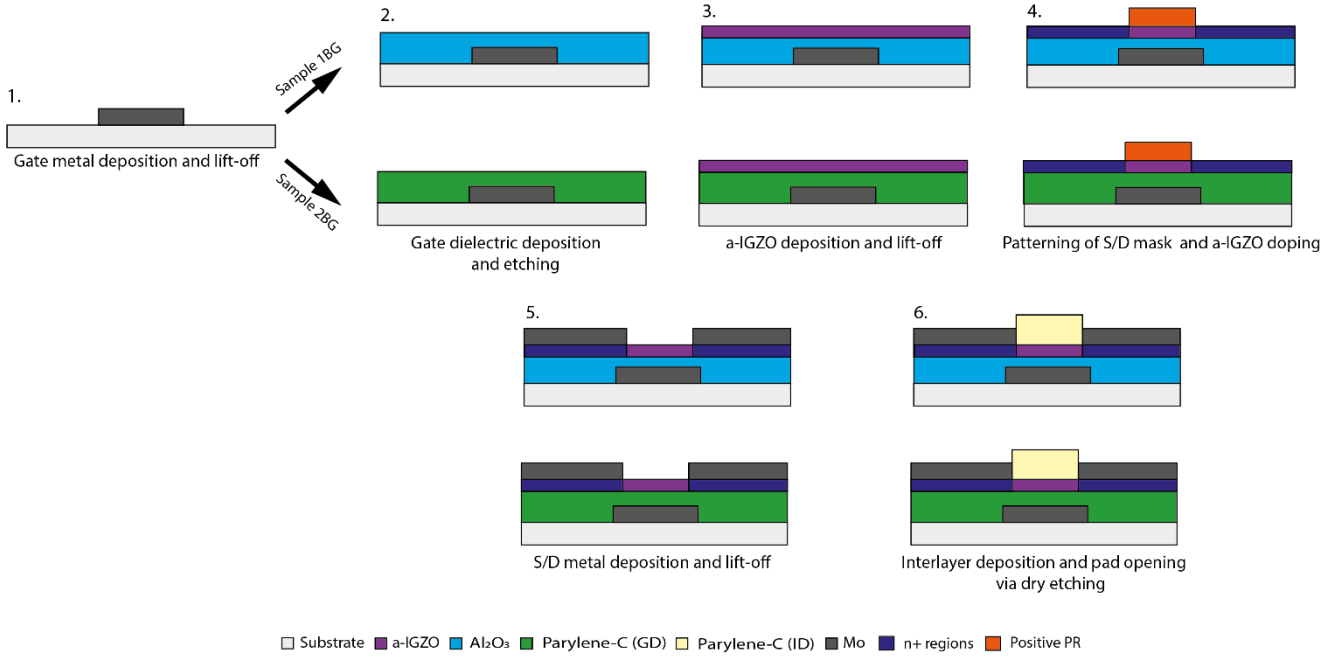

Figure A.4 – Schematic process flow of STG BG TFT fabrication.

Annex 5 – SA TG TFTs layouts

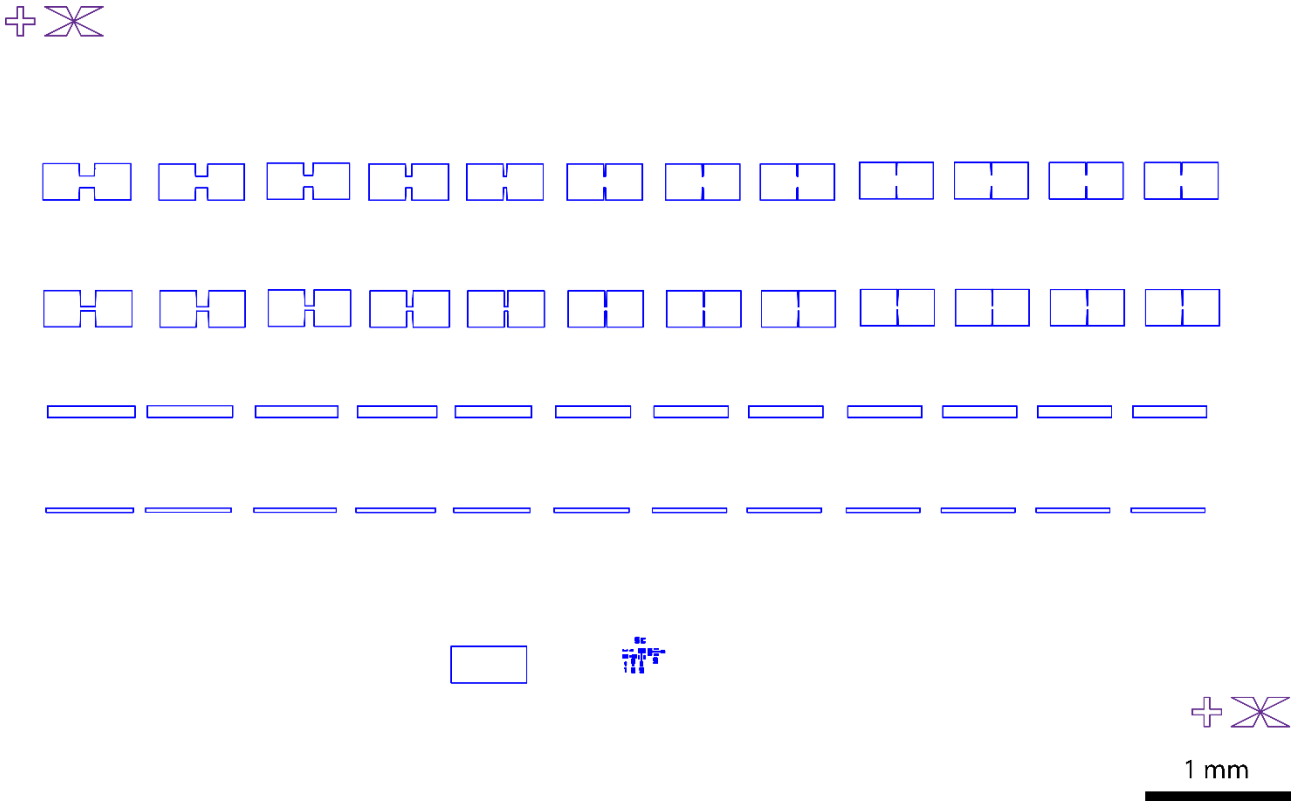

Figure A.5 – Semiconductor layer layout for SA TG TFTs.

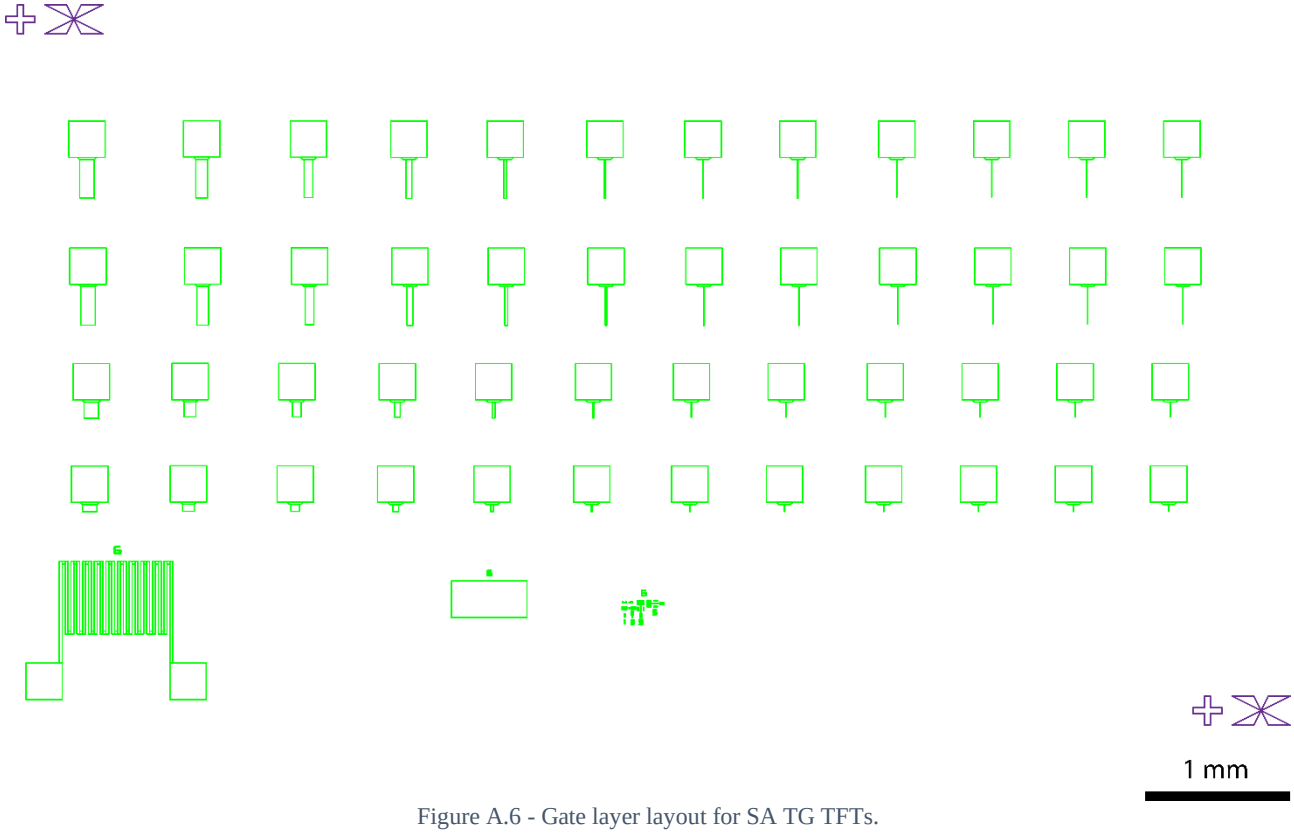

Figure A.6 - Gate layer layout for SA TG TFTs.

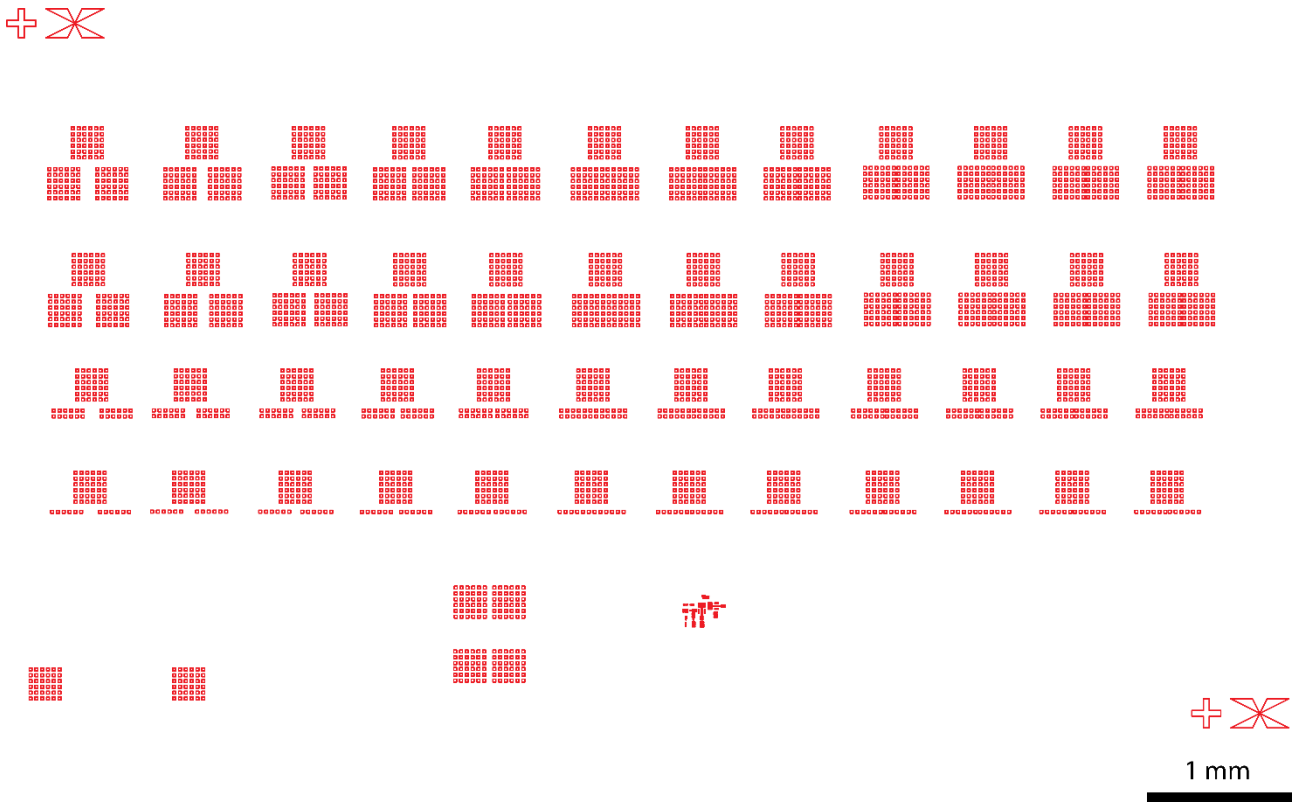

Figure A.7 – Vias layer layout for SA TG TFTs.

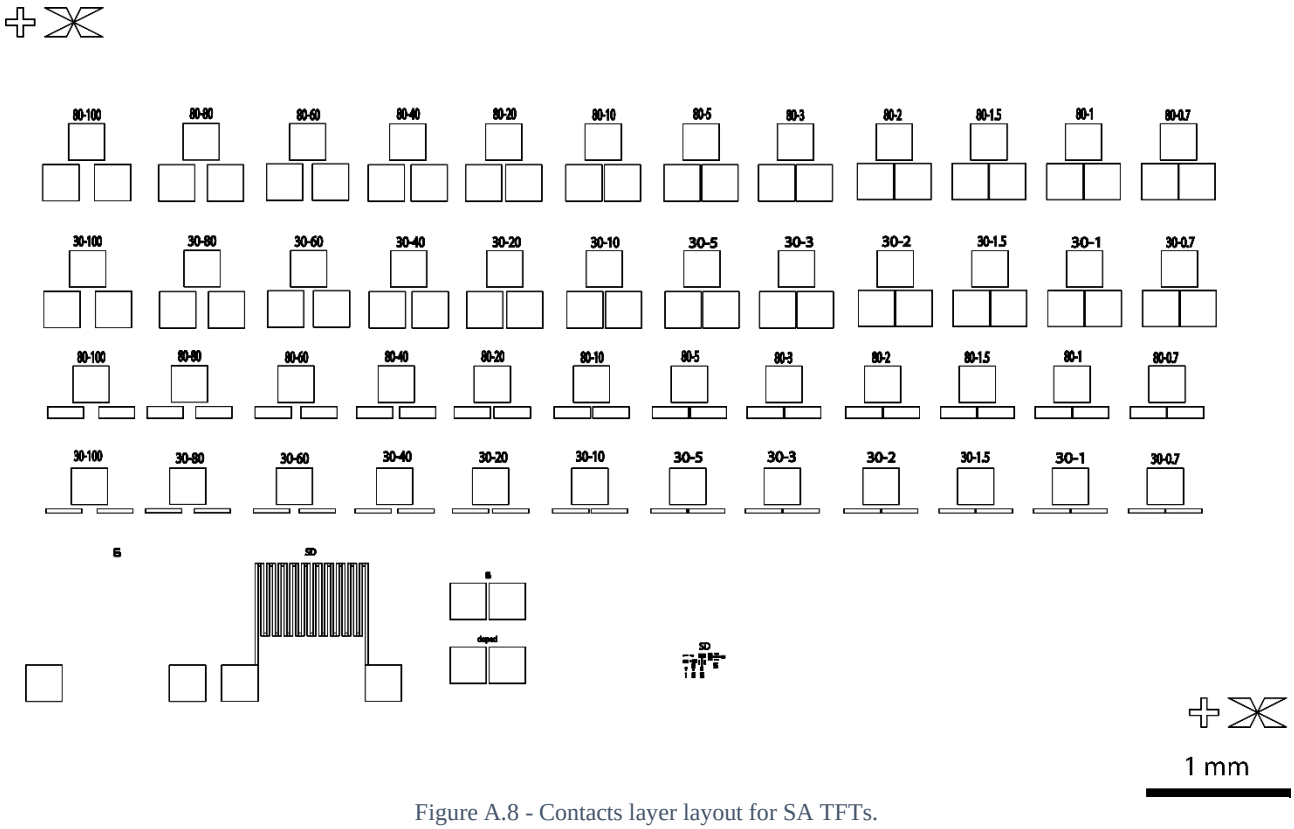

Figure A.8 - Contacts layer layout for SA TFTs.