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Solution-based IGZO nanoparticles memristor

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Abstract

This work aims to characterize Indium-Gallium-Zinc-Oxide nanoparticles (IGZOnp) as a resistive switching matrix in metal-insulator-metal (MIM) structures for memristor application. IGZOnp was produced by low cost solution-based process and deposited by spin-coating technique. Several top and bottom electrodes combinations, including IZO, Pt, Au, Ti, Ag were investigated to evaluate memory performance, yield and switching properties. The effect of ambient and annealing temperature using 350 ºC and 200 ºC was also analysed in order to get more insight into resistive switching mechanism.

The Ag/IGZOnp/Ti memristor structure annealed at 200 ºC exhibits the best results with a large yield. The device shows a self-compliant bipolar resistive switching behavior. The switching event is achieved by the set/reset voltages of -1 V/+1 V respectively with an operating window of 10, and it can be programmed for more than 100 endurance cycles. The retention time of on and off-states is up to 10^4 s. The obtained results suggest that Ag/IGZOnp/Ti structure could be applied in system on a panel (SoP) as a viable device.

Keywords: IGZO nanoparticles, solution-base, bipolar resistive switching, Valence Change Memory, self-compliant.

Resumo

Este trabalho visa à caracterização de nanopartículas de óxido de índio-gálio-zinco (IGZOnp) como uma matriz de comutação numa estrutura metal-isolante-metal (MIM), para aplicações como memristores. As IGZOnp foram produzidas por processos químicos de baixo custo e depositados por técnica de *spin-coating*. Para avaliar a performance das memórias, foram investigados os rendimentos e propriedades de comutação para vários tipos de elétrodos inferiores e superiores incluindo combinações de IZO, Pt, Au, Ti, Ag. O efeito ambiente e temperaturas de recozimento utilizando de 350 ºC a 200 ºC, foi também analisada de modo a obter mais informações sobre o mecanismo de comutação resistivo.

O memristor com a estruturas de Ag/IGZOnp/Ti recozidos a 200 ºC exibem os melhores resultados com um elevado rendimento. O dispositivo revela um comportamento de comutação resistiva bipolar de *self-compliant*. A operação de comutação é atingida por tensões de set/reset de -1 V/+1 V respetivamente com uma janela de operação de 10, e pode ser programada por mais de 100 ciclos de resistência. O tempo de retenção no estado on e off chegam aos 10^4 s. Os resultados obtidos sugerem que a estrutura de Ag/IGZOnp/Ti pode ser aplicada em *system on a panel* (SoP) como um dispositivo viável.

Palavras-chave: Nanopartículas de IGZO, à base de solução, RRAM, comutação resistiva bipolar, Valence Change Memory, self-compliance.

List of abbreviations

AE – Active Electrode
AFM - Atomic force microscopy
a-IGZO – amorphous - Indium Gallium Zinc Oxide
ALD - Atomic Layer Deposition
CBRAM – Conductive bridge random access memory
CE – Contra Electrode
CF – Conductive Filament
DLS - Dynamic light scattering
DRAM - Dynamic random access memory
DSC-TG - Differential scanning calorimetry and thermogravimetry
ECM - Electrochemical metallization memory
EDS - Energy-dispersive X-ray spectroscopy
FeRAM – Ferroelectric Random Access Memory
FTIR - Fourier Transformed Infra-Red
HCS - High Conductive State
HRS – High Resistance State
HRTEM – High Resolution Transmission electron microscopy
IGZO – Indium Gallium Zinc Oxide
IGZOnp - Indium Gallium Zinc Oxide nanoparticles
IoT – Internet of Things
LCS – Low Conductive State
LRS – Low Resistance State
MIM – Metal-insulator-metal
MLC – Multilevel cell
MRAM – Magnetic Random Access Memory
NVM – Non-volatile memory
OxRAM - Oxide-based Random Access Memory
PCM – Programmable metallization cell
PC-RAM – Phase-change - Random Access Memory
Rms – Surface roughness (Root mean square)
rpm – Rotations per minute
RRAM – Resistive Random Access Memory
RT – Room Temperature
SCLC - space-charge-limited conduction
SEM - Scanning electron microscopy
SMU - Source measure unit
SoP – System on a Panel
SRAM - Static random access memory
SSD – Solid State Drive
TE – Top Electrode
TFT – Thin Film Transistor
ULSI – Ultra-large-scale-integration
UV – Ultraviolet
VCM – Valence Change Memory
Vis – Visible
VO – Oxygen Vacancies
XPS - X-ray photoelectron spectroscopy
XRD – X-Ray Diffraction

List of Symbols

C.C. – Current Compliance
φ – Magnetic Flux
q – Charge
M – Memristance
α – absorption coefficient
hv – photon energy
Eg – Band gap
V_{SET} – Set Voltage
V_{RESET} – Reset Voltage

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1. Motivation and objectives

Resistive Random Access Memories (RRAM) development has received a lot of attention by the scientific community in the past few years. Until now the most reliable and efficient technology for storage information was based on floating gate devices build on silicon technology, like flash drives and solid state drives (SSD). Therefore, due to Moore's law limitations there are a necessity to look for alternative architectures and new types of memories.

To suppress this problem and increase the speed and performance, keeping the same evolution rhythm, several types of non-volatile memories (NVM) have been developed. From which RRAM received a huge highlight as it consists a two terminal device with metal-insulator-metal (MIM) structure, allowing ultra-large-scale-integration (ULSI) densities. Other advantages like faster switching, low-operation voltage and longer storage time, support the idea that the future of storage devices rely on RRAM. This would generate the control of an enormous market, which involves all consumer electronic products from computing technology to health care. Furthermore, it would expand even more the internet of things (IoT) advent, becoming clear the huge economic motivation to create such devices.

Furthermore, it is important to notice the growing interest in flexible, printable and transparent electronics subject, which promises a huge impact on society. Therefore, it is propitious a compatibility from these new memories devices with this kind of technologies. Since Indium Gallium Zinc Oxide (IGZO) is one of the most efficient and investigated material regarding those topics, it will be studied in this master thesis. Adding the peculiarity of being solution based, obtained through hydrothermal process in nanoparticles form, which will act as switching layer in RRAM.

The main objective of this work focus on development, analysis and optimization of a non-volatile RRAM in a simple device configuration like MIM structure where solution based IGZO nanoparticles (IGZOnp) acts as insulator layer, normally used as semiconductor. In order to achieve a solid study over this devices, several steps were taken, such as:

- RRAM fabrication with different types of metal and transparent conductive oxide electrodes and consequent study over conductive mechanism.
- Temperature, solvents presence and vacuum influence on device performance and yield.
- Transition from bipolar to unipolar.
- Current Compliance influence.

All devices will be characterized with aim to record: set voltage, reset voltage, minimum read voltage, operation window. Being also submitted to retention and endurance tests.

Additionally, a comparative report to a MIM-double layer device produced at Universität *Darmstadt* will be performed and discussed.

2. Introduction

2.1. Non-volatile memory device

Memories devices are categorized into two: volatile and non-volatile. In volatile memories with which is possible to achieve fast operations, although there is a need to refresh periodically the storage cell, retaining the information which fades when the power supply is turned off. Static random access memory (SRAM) and dynamic random access memory (DRAM) are good examples. Non-volatile Memory (NVM) devices do not lose the information even after removing the power supply, however they operate slowed than volatile memories. Memories such as magnetic tapes, floppy disks, optical disks and flash memories are types of NVM [1], [2].

Motivated by silicon technology limitations, mainly the feature sizes, the scientific community have research and developed new types of NVM where the most relevant can be present as: (1) magnetic (MRAM), (2) phase change (PCM-RAM, PCRAM or PRAM), (3) ferroelectric (FeRAM) and (4) resistive (RRAM) random access memories [1].

2.2. Resistive Random Access Memories

From all the emerging NVM referred, RRAM stands out as the most promising one. This fact is supported by its simple capacitor-like structure, composed by two electrodes and an insulator or semiconducting layer arranged between the electrodes. It is commonly known as MIM structure capable to be used as a cross point structure, allowing ultra-high density without using access devices. Adding the possibility of being compatible with silicon technology and the advantages of fast operations, low power consumption and simple fabrication process, it is easy to perceive a future for RRAM as a cheap universal memory technology [1], [3]–[5].

As it is explicit in the name, Resistive RAM include memories that store information by changing the MIM cell resistance. This behavior is controlled by applying different voltages at the device terminals. Usually a RRAM memory cell can have two resistive states: high-resistance state (HRS) (or low-conductive state LCS) and a low-resistance state (LRS) (or high-conductive state HCS), representing a logic value “0” or “1” respectively. In this case the cell is called single level cell (SLC). There are also memories cell that can achieve more than two resistive states being designated by multilevel cell (MLC) [1], [6]–[8].

2.2.1. RRAM classification

RRAM can be classified in two categories depending on the switching mechanism. If the cell changes its resistance by cation motion is often designated as electrochemical metallization memory (ECM), atomic switch, or conductive bridge RAM (CBRAM). The second category relies on anionic-based device where the switching process is driven by oxygen ion motion (or oxygen vacancy, VO) these devices are called valence change memory (VCM) or oxide-based RAM (OxRAM) [1], [9]. There are also reports where both mechanism work together to improve the device performance [10].

Electrochemical metallization system

In this system a MIM cell is compose of two different electrodes: an electrochemical active metal, such as Ag, Cu, or Ni, and an electrochemically inert, where Au, Pt, Ir, W, can be used as

counter electrode (CE). Also, the thin film sandwiched between these two metals should allow a M^{Z+} ion conduction [9], [11].

To occur the set mechanism, i.e. switch the cell resistance from HRS to LRS, three steps must be considered: (1) over a bias at AE (active electrode), takes place a metal anodic dissolution which generates metal cations (M^{Z+}) and equivalent number of electron (Z^{+}) in the following equation $M \rightarrow M^{Z+} + Ze^{-}$; (2) M^{Z+} migration through the electrolyte/insulator layer by an electric field; (3) active metal reduction and electrocrystallization at CE, forming a filament, which preferentially grows from CE to AE, in the following equation $M^{Z+} + Ze^{-} \rightarrow M$ [1], [5], [9]. A metal filament formation can also occur from AE to CE in specific cases where selenides and sulfides are used as insulator materials, due to a M^{Z+} smaller diffusion coefficient [9], [11].

When the filament reaches the AE the cell resistance switch from HRS to LRS, since electrons can move freely across the bridge. In order to recover the HRS it is usually applied a sufficient opposite voltage bias which beyond an electronic current in the filament, will create an electrochemical current responsible for the filament dissolution. It is also important to retain that switching speed is mainly driven by kinetics from the previous (1) and (3) steps [1], [5], [9].

Valence change system

In contrast to ECM which are cation based systems, valence change system is characterized by oxygen vacancies (V_O) migration, created though anions movements. Generally, oxides are the most common switching media for these devices, such as TiO_x [12], [13], NiO_x [14], [15] , HfO_x [16], [17] , TaO_x [18], [19]. It is possible to divide VCM in two groups: (1) interface- and (2) filament-type.

Interface-type definition comes from the entire cell area involvement in the switching behavior, since the LRS is inversely proportional to the cell area. This type of device is generally composed by a metal-oxide ohmic contact and on the other electrode a metal-oxide schottky contact which allows RS behavior. The switching mechanism takes place when a negative voltage is applied to the electrode with schottky barrier on the oxide, which leads to an V_O accumulation. With the end of V_O from the opposite electrode, a higher electric field will result in a V_O depleted zone beneath the V_O-rich interface layer, leading to a HRS. Applying a positive voltage to metal-oxide schottky barrier will cause a reverse process resulting in a LRS [4], [5], [9], [20].

Regarding filament-type VCM, the mechanism behind resistive switching depends on formation and rupture of conductive filaments in the switching layer. For this reason, there is no or a very weak dependency between the resistance at LRS and cell area. It is possible to use p-type or n-type semiconductors to achieve the filament formation, since both can present abundant cation vacancies and anion vacancies, respectively [4], [5], [9], [20].

If the switching layer is composed of a p-type semiconductor, then the filament formation happens through a positive bias application at the top electrode (TE) which causes an oxygen ion migration from near crystal defects, such as V_O and grain boundaries, to the TE and accumulating in its vicinity, resulting in abundant cation vacancies, Figure 2.1 (b). Consequently, some of these vacancies can develop into nuclei that will grow preferentially due to effectively electrical field concentration and act as anode extension. This leads to a full filament formation which causes the device enter in a LRS, Figure 2.1 (c). When a negative bias voltage is applied to the TE a Joule heat phenomenon causes oxygen ions mobility acceleration which will migrate toward the CE and be stored in interface switching layer/CE or CE grain boundaries. Subsequently, this

process will reduce the cation vacancies concentration in conductive filament (CF) resulting in its rupture, near the cathode, switching the device from LRS to HRS, Figure 2.1 (d) [4], [5], [9], [20].

In the case of n-type switching layer, as it has many V_O, when a positive bias is applied to the TE, these V_O will migrate towards the CE and accumulate in its vicinity Figure 2.1 (f). This will form a nuclei of n-type semiconducting CFs which will grow and act as a cathode extension. The completion of this process will lead to a change in resistance state from HRS to LRS. Since this type of filament grows from the cathode to the anode, the thinner part will be located at the anode, Figure 2.1 (g). This part is easily ruptured by a negative bias over the TE, as the bias leads to a localized Joule heating resulting in a significant mobility acceleration of V_O towards the TE conducted by the electrical field. At the TE these V_O will be eliminated by the presence of stored oxygen. Again, the filament disruption leads to a switching mechanism from LRS to HRS, Figure 2.1 (h) [4], [5], [9], [20].

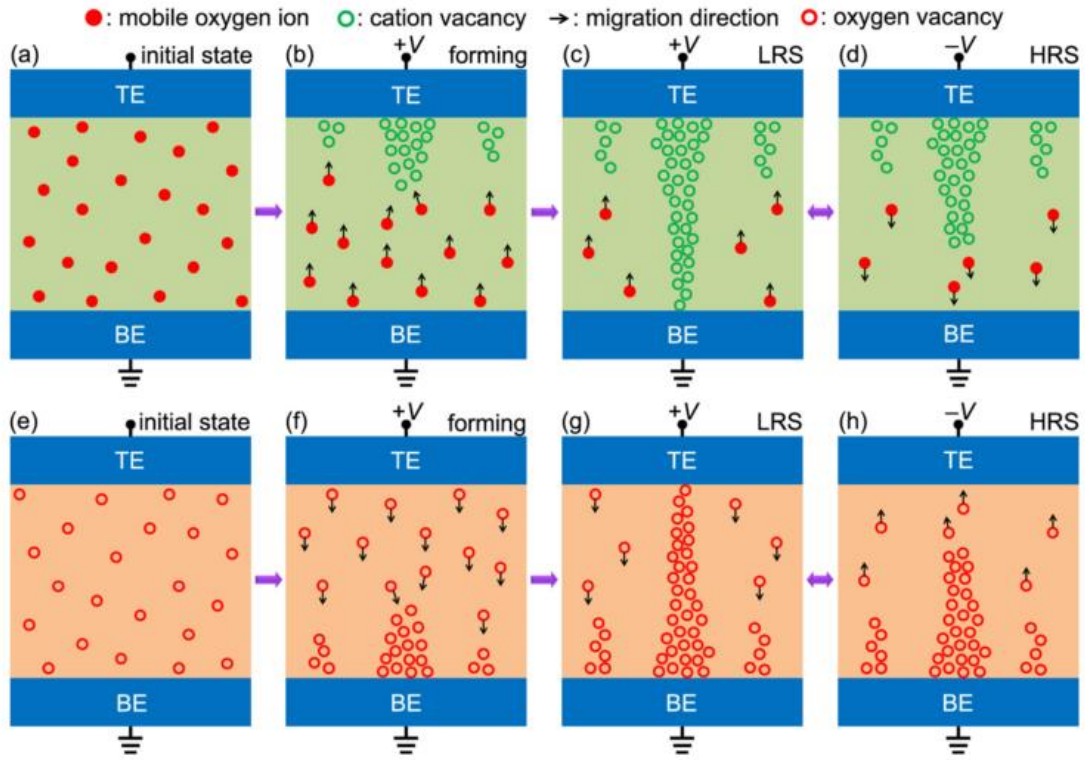

Figure 2.1– (a-d) Schematic of a VCM in p-type semiconductor, (a) mobile oxygen ions randomly distributed, (b) nucleation and cation vacancy filament growth from anode to cathode, (c) CF achieving LRS, (d) CF rupture achieving HRS. (e-h) Schematic of a VCM in n-type semiconductor, (e) V_Os randomly distributed, (f) nucleation and V_Os CF formation from cathode to anode, (g) CF achieving LRS, (h) CF rupture achieving HRS [9].

2.3. Memristor

Memristor corresponds to the fourth basic circuit element, aside of (1) resistor, (2) capacitor and (3) inductor, predicted by Professor Leon Chua in 1971 [21], due to the studied symmetry between all this devices. It consists in a nanodevice capable of recording the voltage or current applied to itself [1], [21], [22]. Its behavior can be described by the equation (2.1) where the electrical charge is related to the magnetic flux.

$$\mathrm{d}(\varphi) = M \cdot \mathrm{d}(q) \text{ (memristance)} \tag{2.1}$$

With its hysteretic behavior is possible to use the described device as a nonvolatile memory. In fact, is particularly useful because it can store and process multilevel resistance values as well as analog values. [5]

Although the memristor has been theorized in the 70s, only in 2008 was announced the first memristor fabrication, by HP Lab. This device consisted in a MIM structure, where “M” is Pt and the “I” a TiO_2 thin film. The mechanism behind the memory cell is explained by the switching from low conductivity to high conductivity. This event can happen due to TiO_2 stoichiometry, an exact 2:1 ratio of oxygen to titanium, shows an insulator characteristic though a conductive phenomenon takes place if the TiO_2 loses some oxygen resulting in an oxygen-deficient titanium oxide (TiO_{2-x}) [1], [22].

To achieve the described process, it is necessary a positive voltage bias applied to the top electrode, resulting in a doping front movement, i. e. the oxygens move towards the insulator part leaving a doped region behind, which consequently causes a cell resistance drop. If a negative bias is provided to the TE, then the oxygens will move toward TiO_{2-x} zone generating TiO_2 and so increasing the overall resistance, as it is shown in Figure 2.2 [1], [22].

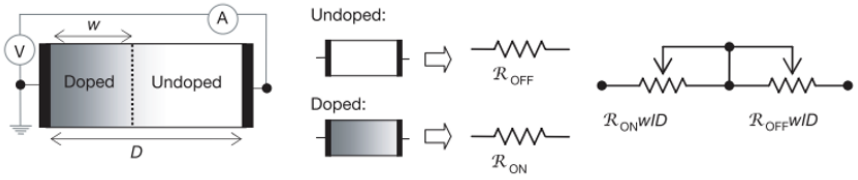

Figure 2.2 - Diagram of a coupled variable-resistor model for a memristor where V is voltmeter and A an ammeter, with the respective equivalent simplified circuit, resulting in a $R_{ON}wID$ and $R_{OFF}wID$ series [22].

The resulting I-V characteristics can be seen in Figure 2.3 where (a) represents the predicted memristor behaviour by Strukov et. al. [22] and a real memristor result from a Pt-TiO_{2-x}-Pt achieved by Stewart et. al. [23].

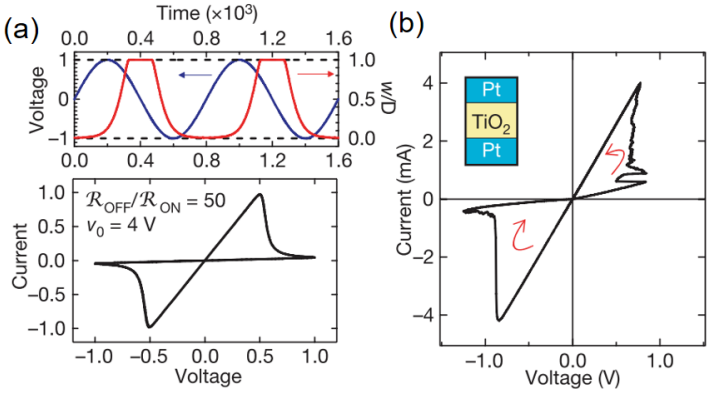

Figure 2.3 - Linear I-V characteristics of a TiO_2 memristor device: (a) Simulation plotting voltage stimulus (blue) and corresponding change in the normalized state variable w/D (red) versus time and resultant I-V characteristic; (b) experimental I-V characteristic of a Pt/TiO_{2-x}/Pt [22], [23].

2.4. RRAM operations

As it is expressed previously, low and high resistance states, so-called “LRS” and “HRS” can be achieved by different voltage bias applications. There are two basic operations can be considered: set and reset. It is called a set process when the cell passes from HRS to LRS, and

reset when the cell shifts from LRS to HRS. The RRAM are categorized in two operation types: unipolar resistive switching and bipolar resistive switching [1], [22].

Unipolar behavior occurs when the switching procedure does not depend on the polarity of the applied programming voltage. Also, set process should have a certain current compliance (C.C.) to prevent the definitive short circuit of the cell. Reset voltage is always below the set voltage and do not need any kind of C.C. because it occurs at higher currents, Figure 2.4 (a) [1], [22].

Contrary to the previous operation, bipolar switching take place with a set voltage polarity different from the reset voltage polarity. The set process need C.C., and the reset do not need it, for the same reason as before, Figure 2.4 (b) [1], [5].

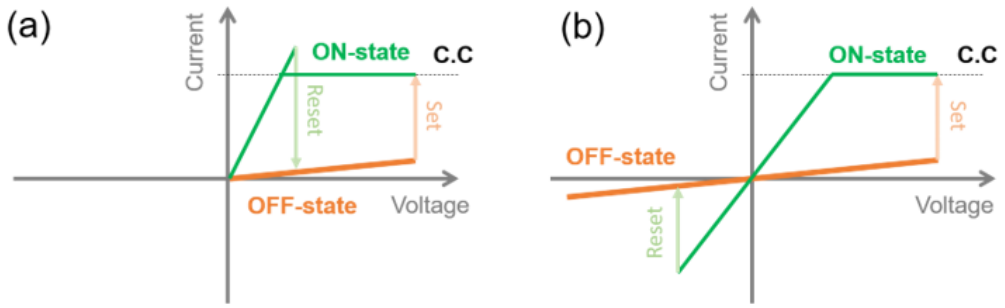

Figure 2.4 – Schematic of I-V linear curves for (a) unipolar behavior and (b) bipolar behavior. C.C represent the current compliance required to protect the memory cell from break down, during set process.

2.5. IGZO as a RRAM switching layer

IGZO is one of the most studied and well documented oxide materials for TFTs applications since it can present high mobility, allowing also high flexibility, high transparency and is compatible with low-temperature fabrication process. With this characteristics, it is easy to conclude that is an optimal material to applied in systems on a panel (SoP) [24], [25]

The study over IGZO memory devices for a compatible usage in SoP did not start with resistive memories, instead the first device with an IGZO layer was a floating gate type memory develop in 2008 by Huaxiang Yin at. al. [26]. Only in 2010 start to appear developments on IGZO based RRAM with studies over bipolar behavior in full transparent devices [27], [28], unipolar behavior [19] and electrode influence [29]. In the following years more studies where made with this oxide, analyzing filament nature [30], achieving flexible devices [31], and more reports on the ways to improve this type of RRAM [8], [32]–[34].

Inspired on previous IGZO solution based TFT (Thin Film Transistor), Moon-Seok Kim and his team developed IGZO solution based RRAM [35]. However, the obtained results did not exceed one order of magnitude regarding the operation window. Moreover, Wei Hu [36] and his group were able to acquire a RRAM device by low temperature process, in this case, a photochemical solution deposition, resulting in uniform performance as well as a stable distribution of LRS and HRS. State of the art on *a*-IGZO RRAM devices (sputtered and solution-based) are shown in Table 7.1 in Annex A.

Until now there are no reports on IGZO nanoparticles applied to RRAM and for this reason opportunity arise to demonstrate the performance of these devices with such material produced with low-cost processes.

3. Materials and Methods

In order to produce IGZO nanoparticle switching layer in a Resistive Radom Access Memory (RRAM) it was used a process developed by Santos et. al. [37], proven to work as semiconductor layer in electrolyte-gated transistors. However, in the present work it will be studied as an insulator layer in the same way as *a*-IGZO RRAM. Thus, to optimize the yield and performance some parameters were analysed such as annealing temperature and consequent presence of ethylene glycol. Also, an *a*-IGZO RRAM was produced for comparison with the obtained results.

3.1. IGZO Nanoparticles Preparation and characterization

IGZO nanoparticles were prepared with gallium nitrate hydrate ($Ga(NO_3)_3 \cdot xH_2O$, Sigma-Aldrich, 99,9%), indium acetate ($In(CH_3COO)_3$, Sigma-Aldrich, 99,99%) and zinc acetate ($Zn(CH_3COO)_3 \cdot 2H_2O$, Sigma-Aldrich, 99%) precursors in a molar ratio 3:6:2, respectively. The mixture was dissolved in 2-methoxyethanol (6 ml, Sigma-Aldrich, 99,5%) and ethanolamine (0.2 mL, Fluka, 98%) as a cation reductor was added to the solution before left stirring at 50 ºC for 1 h. The final solution was transferred to a 23 mL of PTFE (polytetrafluoroethylene) chamber, set inside a stainless steel autoclave (4745 general purpose vessel, Parr) and placed in an oven (L3/11/B170, Nabertherm) at 180 °C for 24 h. The resulted products were collected by centrifugation at 4000 rpm for 5 min (F140, Focus instruments) and dispersed in ethanol (20 mL).

Structural and morphological characterization of IGZO nanoparticles was performed by scanning electron microscopy (SEM, Carl Zeiss AURIGA) equipped with energy-dispersive X-ray spectroscopy (EDS), where a sacrificial layer of carbon has been previously deposited (quorum q150t es). EDS was used to determine the average atomic weigh from 10 samples, Annex B.

Fourier Transformed Infra-Red (FTIR, Thermo Nicolet 6700 Spectrometer) spectroscopy data was recorded using an Attenuated Total Reflectance (ATR) sampling accessory (Smart iTR) equipped with a single bounced diamond crystal (4500 to 525 cm^{-1}). These results can be consulted in, Annex C. Optical band gap was performed in Perkin Elmer lambda 950 UV/VIS/NIR spectrophotometer resulting in 3.74 eV, Annex D.

The nanoparticles were deposited on a silicon substrate for the x-ray diffraction (XRD) measurements being scanned in the 5-65º 2θ range with a step 0.033º in a PANalytical's X'Pert PRO MRD diffractometer with CuKα radiation, Annex E. The IGZO thin film surface roughness was analysed by atomic force microscopy (AFM) in a commercial microscope, Asylum research MFP-3D, on IZO thin film and examined in data analysis software (Gwyddion). Dynamic light scattering (DLS) technique using W130i Avid Nano, was employed to record the nanoparticles hydrodynamic diameter, Annex F.

3.2. IGZO Thin Film Deposition and Characterization

To deposit the nanoparticles is necessary to create an ink, for that, ethylene glycol (Carlo Erba, 95,5%) was mixed with the nanoparticle dispersion in a 0.4:1.6 proportion, respectively, and left stirring for 24 h. Then was sonicated for 2 min and filtered with a 0.45 μm porous diameter filter (Sartorius CA). The deposition process was performed by spin coating 4 layers at 2000 rpm during 35 s and dried at 100 ºC for 1 min between each layer. The annealing process was made

after the fourth deposition at 350 ºC and 200 ºC for 1 h. Notice that the IGZO ink was deposited on different substrate materials depending on the device construction under study.

Moreover, IGZO inks were characterized by differential scanning calorimetry and thermogravimetry (DSC-TG, model STA 449 F3 Jupiter, Netzsch) with the solution in air with a heat ramp of 5 ºC/min starting from room temperature up to 550 ºC. These results can be consulted in annex G.

3.3. RRAM assembly and characterization

Metal-insulator-metal (MIM) structures were fabricated by depositing different types of bottom electrodes on glass substrates (1737, Corning). In this case, (1) titanium (6 nm) and gold (60 nm); (2) titanium (6 nm) and platinum (60 nm); and (3) titanium (60 nm) were deposited by e-beam evaporation (homemade apparatus). Also, it was used an IZO (indium zinc oxide, 140 nm) layer deposited by radio frequency (13.56 MHz) magnetron sputtering (homemade apparatus), using a ceramic oxide target of In_2O_3:ZnO (89.3:10.7 weight fraction, Super Conductor Materials, Inc., 99.99%) at room temperature in the presence of a mixture of argon (20 sccm) and oxygen (0.4 sccm) at a deposition pressure of 2×10^{-3} Pa with a r.f. power of 75 W and a target−substrate distance of 15 cm [38].

Secondly, IGZO ink was deposited by spin coating process, previously described. Additionally, the devices for comparison made of *a*-IGZO switching layer were sputtered onto bottom electrodes using a IGZO (2:1:2) commercial ceramic target (LTS Chemical, Inc.) by a r.f. magnetron sputtering (AJA 1300-F system), without intentional substrate heating for 13 min and 30 s, under an air flow of 14 sccm and oxygen of 0.5 sccm, final pressure of 0.3 Pa, and a power of 100 W to achieve 30 nm thickness [39].

Finally, the top electrode (TE) deposition was executed in the same way as the bottom electrodes (BE), where (1) silver (60 nm); (2) titanium (6 nm) and gold (60 nm); and (3) titanium (60 nm) were used in different substrates. The final structure can be visualized in Annex H.

3.4. Electrical IGZO RRAM characterization

IGZO RRAM electrical characterization was performed using a semiconductor characterization system (Keithley 4200SCS). These two terminal devices were connected to source measure unit (SMU) onto top and bottom electrode with the objectives to investigate: (1) set voltage, (2) reset voltage, (3) operation window, (4) retention time and (5) endurance.

Set voltage is executed applying positive sweep voltage on TE, with a fixed C.C. Starting always with 0 V to +1 V and going back to 0 V. The C.C. should be the smallest possible to achieve low power consumption [40], between 1 µA to 10 mA range.

The reset voltage is performed also applying negative voltage sweep on TE, stating from 0 V to -1 V back to 0 V, without C.C. In case the reset process does not occur the voltage is increased. In some cases, the polarization for set and reset follow an opposite polarization, i. e. set is performed with negative voltages and reset is performed with positive voltage.

The I-V characteristics was always performed without delay time. Retention times test for both ON/OFF states where performed under a +0.1 V or -0.1 V constant voltage bias and the corresponding current value was recorded every 60 s.

4. Results and discussion

This chapter addresses all the electrical characterizations of various IGZO RRAM types and configuration, where two structures will be taken as standard devices: (1) Ti/IGZOnp/Ti (from top contact to bottom contact) and (2) Ag/IGZOnp/Ti associated behaviours. Both standard memories present an area of 1.96×10^{-4} cm^2, were annealed at 350 ºC, and analysed in air at room temperature (RT). We note that some variations in structure or and the fabrication parameters may occur during the work in order to achieve a more complete study based on IGZO RRAM.

4.1. Memory cell activation

4.1.1. Forming

A forming step is required for the activation of the switching property, regardless the type of RRAM in the case of presenting a filament behavior [9]. This forming step corresponds to the first set process applied to the device. For this phenomenon to occurs a larger electrical field is required than the consecutives set processes. The cell will be formed from pristine state to low resistive state (LRS) by formation of the nanoscale filament. Then the on-state can be erased to high resistive state (HRS) by application of voltage bias at the opposite polarity.

Thenceforth, set and reset processes only occur in the weakest filament location within a small area, explaining the low voltage operation, after the first cycle [9]. Also, the forming is always performed with C.C. to avoid a filament overgrowth which otherwise could provoke a short circuit. Figure 4.1 identify the typical (a) unipolar and (b) bipolar behavior with the formation step in linear plot.

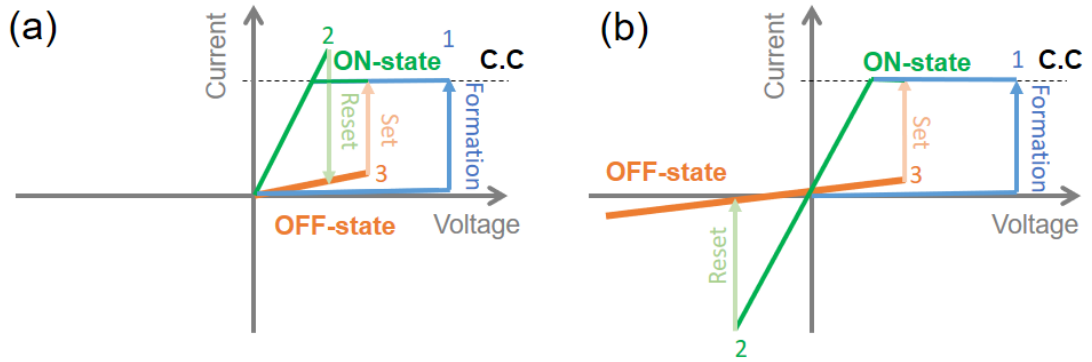

Figure 4.1 – Linear I-V (a) unipolar and (b) bipolar behaviours with typical forming steps (blue). The numbers indicate the occurrence order for (1) forming, (2) reset and (3) set, respectively.

Figure 4.2 depicts two typical and distinct forming behaviours obtained for bipolar mechanism (a) Ti/IGZOnp/Ti and (b) Ag/IGZOnp/Ti, along this work. Figure 4.2 (a) present a similar mechanism to the one already represented in Figure 4.1 (b) considered to be a usual electroforming step and set/reset process for TI/IGZOnp/Ti devices. We note that for symmetric structure with both inert electrodes (Ti) the electroforming can be executed applying positive or negative polarization.

On the other hand, Figure 4.2 (b) shows a curious mechanism where the electroforming can be performed for lower C.C. than the consecutive cycles. Also, this forming step does not achieve the high conductive state (HCS), instead it only defines the low conductive state LCS, supported by the fact that arrow 3 is more compatible with arrow 6 than the HCS (set process

after arrow 6). Any reset attempt to achieve the same resistance as the one in pristine state is impossible even for higher reset voltages. By other words, the consecutive reset (arrows 4 and 5) is enable to drop the HCS to a conductive state equivalent to the pristine state. This effect limits the operating window to 10 or 10^2 in the best cases. Moreover, the electroforming polarization has a preferential polarization in order to occur, this fact is commonly seen in Conductive Bridge Random Access Memory (CBRAM) since one side has an active electrode which diffuses through the insulator matrix. The true mechanism will be explained in later sections.

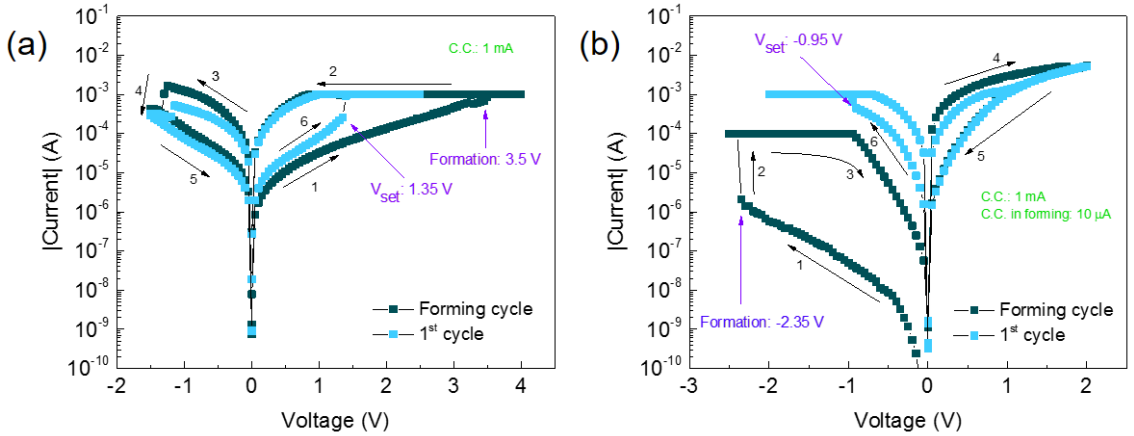

Figure 4.2 - I-V characteristics containing forming and first cycle for (a) Ti/IGZOnp/Ti and (b) Ag/IGZOnp/Ti, depicting two distinct bipolar behaviours.

4.1.2. Pre-forming

There is also a mechanism identified as pre-forming where the pristine state is in LRS instead of HRS, meaning that the cell has a filament formed before any electrical field application. It is speculated that such filament is created during annealing or deposition processes, and can rely on top electrode diffusion and/or vacancies defects within the switching layer due to temperature and/or lower thickness. However, the pre-formed state should be reset to LCS satisfying the memory criteria, i. e., should be able to operate normally regarding endurance cycles and retentions.

Since this phenomenon takes place during fabrication it is impossible to control and it may appear in different current states. As it starts with LRS a reset process with extra electrical field is needed, compared to the consecutive reset processes, in order to disrupt the filament and converting the cell into a working device.

Figure 4.3 represents a typical pre-forming behaviour where the first step (1) is a reset process performed with negative voltage, -7.35 V, and a current value of 67 mA. Meaning that a high power is required to activate the cell. Furthermore, in order to achieve to memory performance a forming step of 4.73 V was needed.

Consequent set and reset cycles show a usual bipolar behaviour, between -2 and 2 V, highlighting that even after two non-ideal and stochastic process (pre-forming and forming) resistance switching can be occurred.

It is unknown for the author if there is any report over the pre-forming subject, since the memory performance can be drastically affected after the pre-form reset. One may also think it is a short circuit due to the similarities. In fact, pre-forming is an undesirable characteristic considering the need of a high electrical field in order to rupture the pre-existing filament(s).

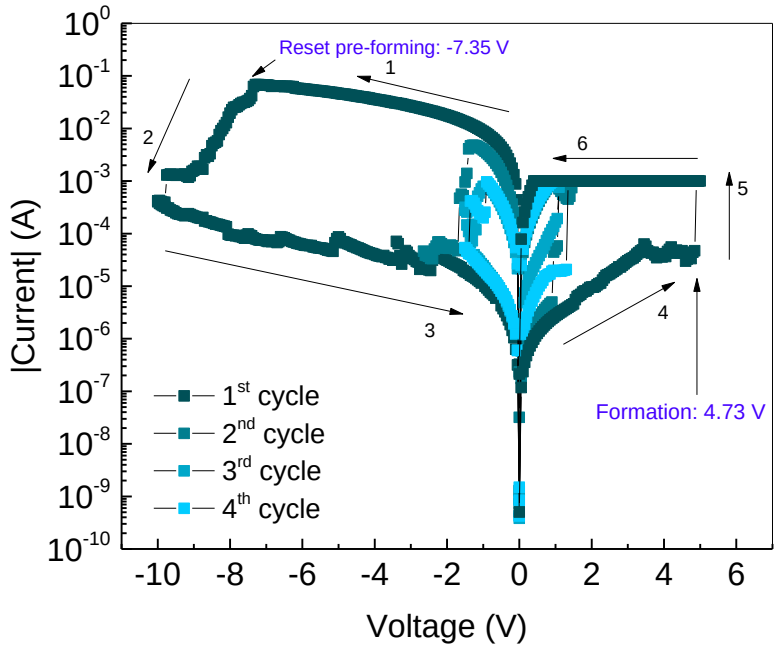

Figure 4.3 - I-V characteristics of Au/Ti/IGZOnp/Ti annealed at 200 ºC, showing a pre-forming and consecutive forming mechanism. The depicted arrows (1-6) demonstrate the orientation in which the memory is operated.

4.1.3. Free forming

Finally, there are reports where RRAM do not need electroforming, i. e. present a forming free mechanism [28], [34]. From a practical point of view forming free is an interesting feature since allows lower operation power by eliminating the forming step. Consequently, resulting in a more stable resistive switching [7], [41], [42], theoretically causing lager endurance.

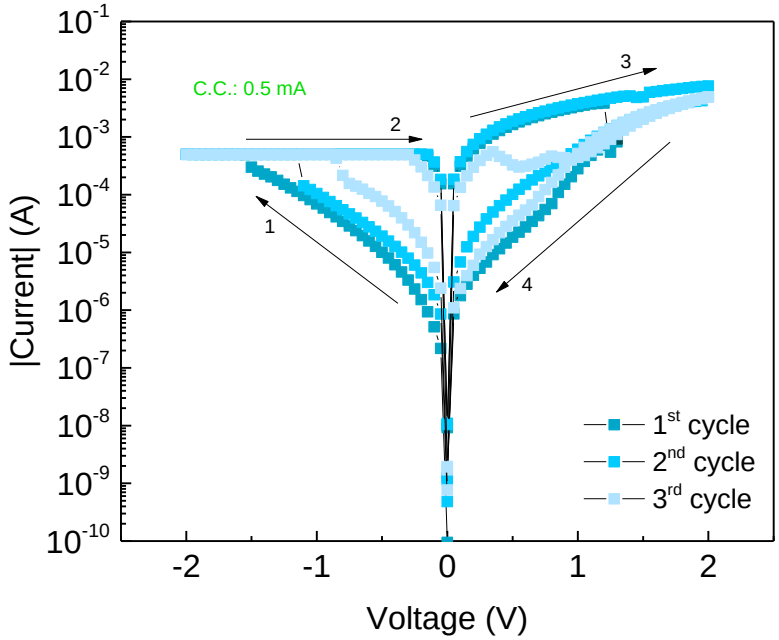

Figure 4.4 - I-V characteristic of Ag/IGZOnp/Ti annealed at 350 ºC showing a free forming behaviour.

In this work, it was possible to achieve a forming free memory with the Ag/IGZOnp/Ti device annealed at 350 ºC, depicted in Figure 4.4. Forming free behavior is discerned by looking at the

similarity in the first two set cycles. Since both first and second set cycles follow the same LCS (arrow 1) preforming the set in a very similar voltage, 1.5 V and 1.1 V respectively.

It is suggested that the reason for a forming free behavior in IGZOnp solution based memories rely on specific IGZOnp thickness, consequent number of nanoparticles in a certain volume as well as number of defects after annealing. Nevertheless, the appearance of forming free memories where rare and only occur for Ag/IGZOnp/Ti.

4.2. Electrical characterization of standard IGZOnp memristors

4.2.1. IGZO nanoparticles RRAM with inert electrodes

In order to IGZO nanoparticles act as a switching layer in an valence change memory (VCM) device it is necessary to be sandwiched by two inert electrodes, hence a Ti/IGZOnp/Ti structure annealed at 350 ºC was fabricated. The correspondent electrical characterization is depicted in Figure 4.5, where (a) represents an endurance test over 100 cycles in sweep voltage mode. Set process is performed at 1.25 V in the first cycle, with a tendency to increase along the number of cycles. Reset process occurs between -0.8 V and -1.5 V.

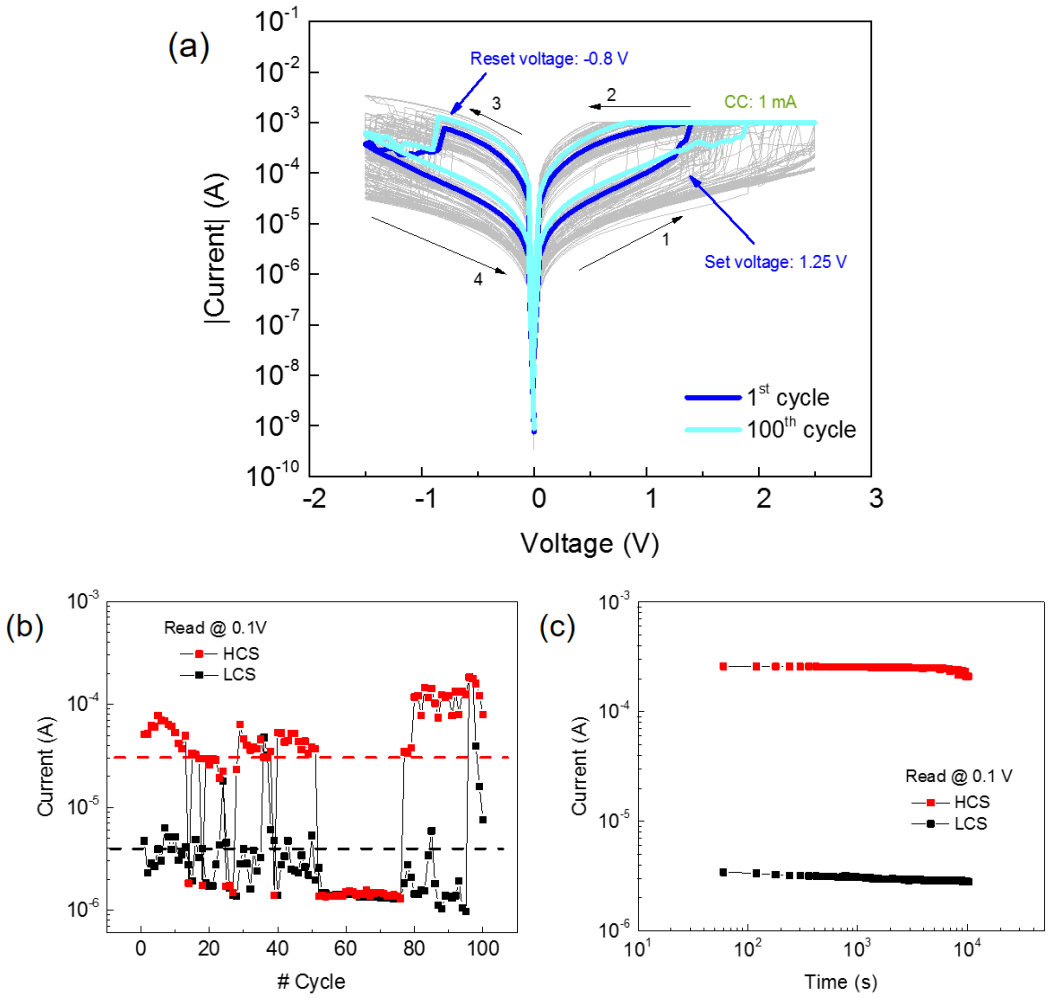

Figure 4.5 - (a) Typical I-V characteristic of Ti/IGZOnp/Ti annealed at 350 ºC over 100 cycles and respective, set and reset voltages indicated by a deep blue arrow, represent the respective value for each process in the first cycle. (b) Endurance characteristics at read voltage of 0.1 V at room temperature. (c) Typical retention characteristics read at -0.1 V at RT.

Arrows 1 to 4 represent the counterclockwise hysteresis direction. In fact, the hysteresis could be made with a clockwise direction (not shown) since this structure is a symmetric and operated as oxide based RAM (OxRAM). The respective electroforming process is already shown in Figure 4.2 (a) occurring at 3.5 V with 1 mA C.C.

Figure 4.5 (b) represents the alternated conductive value read with 0.1 V after each set and reset process that should correspond to HCS and LCS respectively. It is possible to distinguish two different levels with a ON/OFF ratio of one order of magnitude despite the unstable behavior. Notice that from cycle 52 to 72 the memory stopped working. This issue could rely on insufficient applied power for those cycles. Yet it regains the memory ability in the consecutive operations.

Figure 4.5 (c) is referent to a typical retention test executed over 10^4 s, being visible a stable behavior for both HCS and LCS.

4.2.2. IGZO nanoparticles RRAM with active electrode

It is expected that a metal-insulator-metal (MIM) structure including IGZO nanoparticles with an active electrode on top acts as a CBRAM, in the same way that an *a*-IGZO sputtered memory in the same conditions does [8].

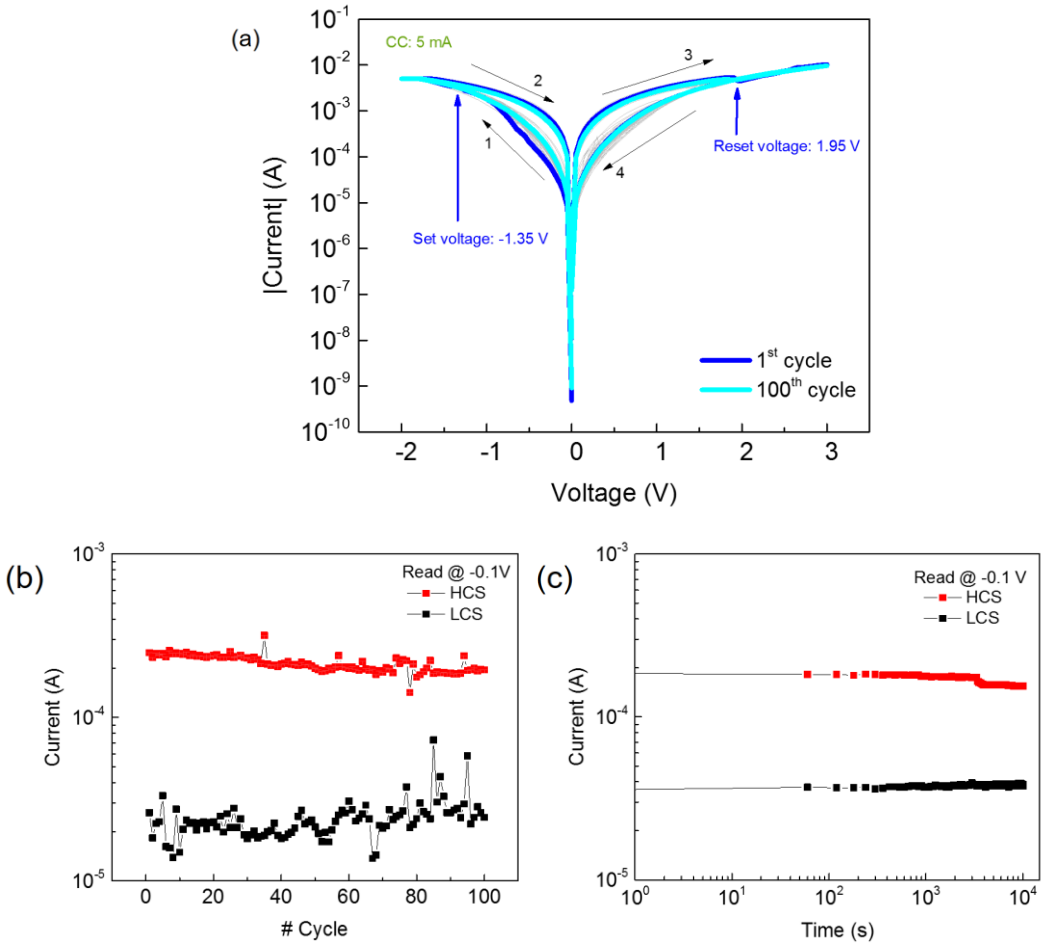

Figure 4.6 – (a) Typical I-V characteristic of Ag/IGZOnp/Ti annealed at 350 ºC over 100 cycles and respective, set and reset voltages indicated by a deep blue arrow, represent the respective value for each process in the first cycle. (b) Endurance characteristics at read voltage of -0.1 V at RT. (c) Typical retention characteristics read at -0.1 V at RT.

In order to show a conductive bridge mechanism, IGZO nanoparticle layer need to behave as an amorphous thin film acting as a matrix for fast ion transport [5]. Although this layer takes an important role in the overall switching mechanism, the main focus is given to the active electrode, since it will drift through the IGZOnp matrix creating a filament. However, the true mechanism behind the switching operation is reveled to be different from the expected ECM behavior, which will be discussed in later sections.

Figure 4.6 (a) depicts a 100 cycles endurance test in sweep voltage mode applied to Ag/IGZOnp/Ti device annealed at 350 ºC. Set process is performed at -1.35 V approximately and reset occurs at 1.95 V. The represented arrows (1-4) demonstrate the hysteresis direction needed in order to have a working memory, as it was described in section 4.1.1, further details will be discussed in the conduction mechanism section (section 4.3.2). Respective cell activation is similar to the one represented in Figure 4.2 (b), however the first C.C. value is 0.5 mA instead of 10 µA.

It is possible to see in Figure 4.6 (b) that the analysed device endured for 100 cycles with a more stable behaviour than the OxRAM studied in section 4.2.1. Furthermore, the ON/OFF ratio is fixed with a 10 value during the endurance test.

Figure 4.6 (c) demonstrate a stable behavior during the retention test over 10^4 s.

4.3. Conduction mechanisms

4.3.1. Ti/IGZOnp/Ti devices

Until this point it was referred that memories with both inert contacts and an oxide as switching layer acted as a VCM. In this section we present the conduction mechanism of the Ti/IGZOnp/Ti devices.

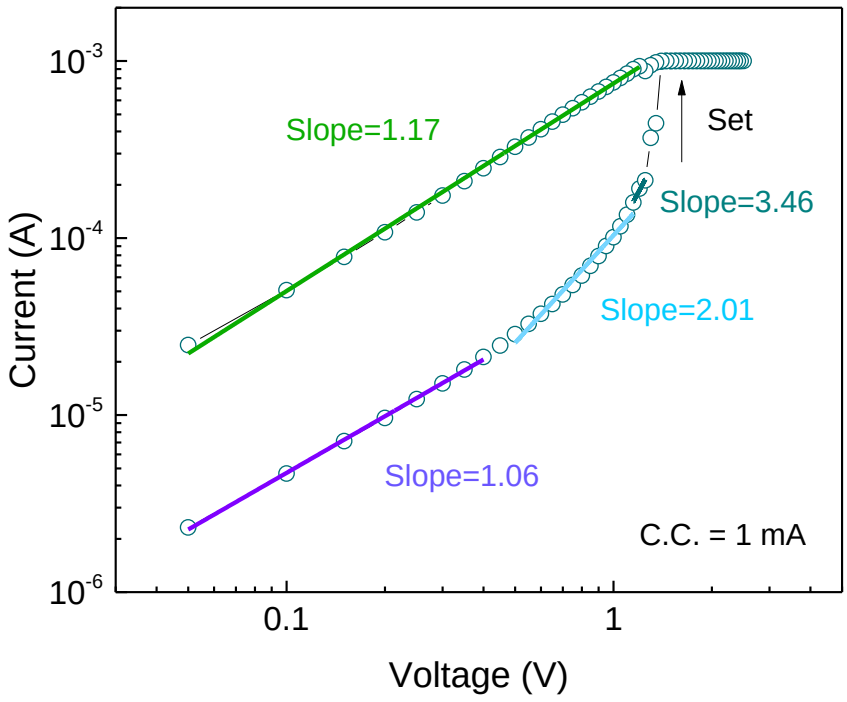

Figure 4.7 - I-V characteristics of Ti/IGZOnp/Ti structure plotted in log-log scale, showing a SCLC mechanism.

In order to determine the conductive mechanism is necessary to plot the first set I-V characteristics in a log-log scale, as it is represented in Figure 4.7, and analyse the respective fittings to determine the carrier transport. At LCS the curve reveals a linear ohmic behavior since it presents an approximate slope of 1, from 0 to 0.4 V. An ohmic behavior is characterized by the mobile electrons movement in the conduction band [27], and holes in the valence band. It can also suggest that the density of thermally generated free carriers inside the switching layer is larger than the injected carriers [43].

From 0.4 V to 1.15 V the curved can be fitted with a slope of 2, which is in accordance to Child's square law ($I \propto V^2$), where the current becomes dominated by injected electrons. Consequently, injected electrons can be divided into two groups, one will occupy the traps and the other will act as free electrons. When all the traps are filled with electrons, than the last region is reached in accordance to steep increase region ($I \propto V^n$, n>2) allowing the shift between LCS to HCS [44].

The referred three regions: (1) ohmic, (2) Child's law and (3) steep increase, belong to space-charge-limited conduction (SCLC) mechanism, as represented on Figure 4.8 where the traps in bulk are the key factor to the switching operation [8]. These results are in agreement with the ones obtained by similar *a*-IGZO memories sandwiched by inert electrodes [28], [36].

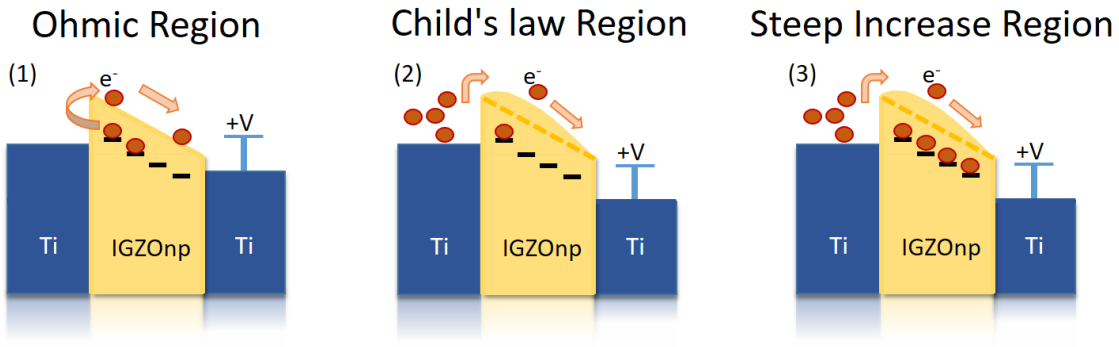

Figure 4.8 - Schematic of SCLC mechanism composed by (1) ohmic region, (2) Child's law region and Steep Increase region.

On the other hand, HCS only shows ohmic behaviour, indicating the presence of highly conductive paths during the switching event [34]. Furthermore, the difference between the ON and OFF state suggests a confined effect in the HCS rather than homogenously distributed [8].

The filament nature can only be determined by fitting a I-T characteristic at HCS and support from X-ray photoelectron spectroscopy (XPS) as well as High Resolution Transmission electron microscopy (HRTEM). Those tests were not performed due to time and/or equipment restrictions. As the previous mechanisms for LCS and HCS matches with studies already made [28], [36] it is expected that the nature of the filaments are similar to oxygen vacancies.

4.3.2. Ag/IGZOnp/Ti devices

Notice that Ag/IGZOnp/Ti devices operate with set process in negative voltage and reset with positive voltage, shown in Figure 4.6 (a). Which is the opposite of Ti/IGZOnp/Ti memories and Ag/*a*-IGZO memories [8]. This phenomenon suggests that instead of Ag filament the switching mechanism is effectuated with V_O. Supported by the fact that Ag needs positive voltage application to turn into Ag^+ and diffuse. On the other hand, V_O migration do not need a specific polarization since the switching mechanism occurs in the IGZOnp layer instead of an electrode.

The previous notion of a dominant V_O switching mechanism can be explained by the test depicted in Figure 4.9. In Figure 4.9 (a) set and reset process occurs with positive and negative voltage sweep application, respectively (arrows 1-4), as expected from a usual voltage application in case of VCM or ECM mechanisms. Consequently, if a positive voltage is applied to the memory, it gets a second reset (arrows 5, 6 Figure 4.9 (a)) instead of a set process. In turn, if a negative voltage is then applied a set process (arrows 7, 8, Figure 4.9 (b)) is followed by a reset process (arrows 9, 10, Figure 4.9 (b)).

Thus, it is noticeable a preferential VCM mechanism with preferential set at negative voltage and reset at positive voltage. Excluding any ECM mechanism occurrence.

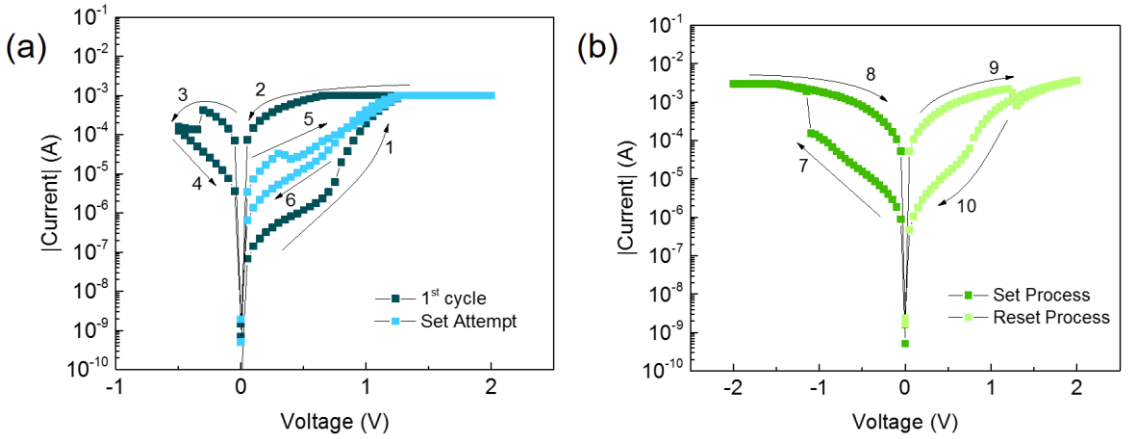

Figure 4.9 - I-V characteristic of Ag/IGZOnp/Ti device showing a swift to a preferential set process with negative voltage aplication on AE.

Regarding the conductive mechanisms both set with positive and negative voltages present a SCLC behaviour, depicted in Figure 4.10, as reported by previous works [8], [28].

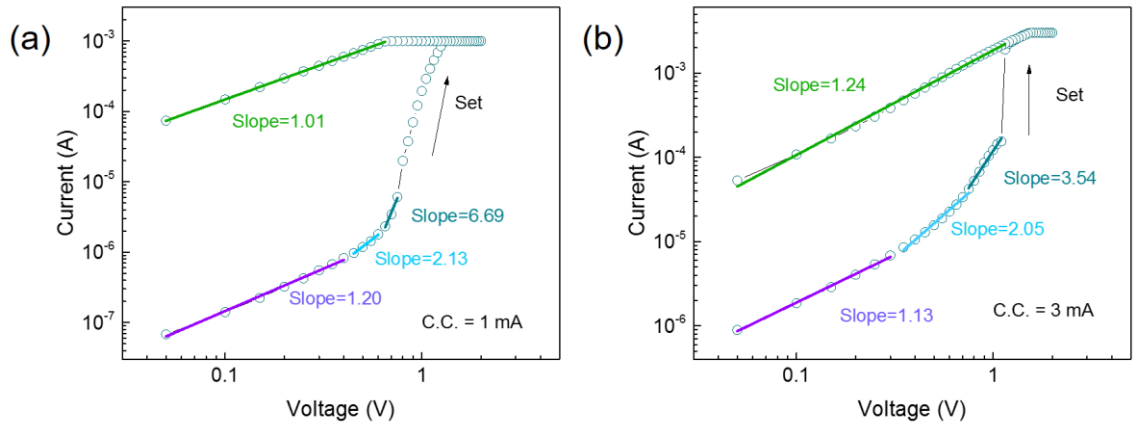

Figure 4.10 - I-V characteristics of Ag/IGZOnp/Ti structure plotted in log-log scale, showing a SCLC mechanism in both (a) ECM and (b) VCM regime.

Furthermore, oxygen vacancies conducting filaments (CF) are formed at higher voltages in the range of 0.2 V to 1 V than metallic CF approximately in the range of 1 to 1.5 V [45]. In addition, conventional CBRAM devices show larger ON/OFF ratios compared to OxRAMs. Here, the LCS and HCS are maintained with an ON/OFF ratio of slightly more than one order of magnitude Ag/IGZOnp/Ti devices which is desirable for practical application [46]. We note that the Ag/IGZO form a Schottky contact as already known in literatures [46], [47] leading to difficult forming process at the positive polarity.

Combining the above results, we suggest that VCM is the responsible resistive switching mechanism.

4.4. Air and Vacuum influence

Air and vacuum influence were tested for OxRAM devices with the Ti/IGZOnp/Au/Ti configuration since these memories are not passivated. Furthermore, there are reports showing an atmospheric impact on the device performance, mostly over VCMs [28], [48], [49].

In this case, all devices present an area of 3.3×10^{-3} cm^2 and were annealed at 350 ºC, the analysis under vacuum were performed with a pressure of 3.33×10^{-4} mBar.

Taking into account that spin coating process can influence the thickness along the substrate and consequently the devices performance, exactly half of the devices were analysed under air (rows 1 to 3) and vacuum conditions (rows 4 to 6) of the same substrate, shown in Annex I.

Based on the overall results provided by the working devices in Annex I, it is difficult to assume an existence of atmospheric influence, since it is impossible to make a statistical analysis with a 19% yield associated with very different RS results. This low yield equally achieved in both air and vacuum devices can be explained by a non-uniform nanoparticle coating, which conceded different thicknesses in the nanoparticle layer over the substrate.

Nevertheless, it is depicted in Figure 4.11 the best results for each case, (a) air and (b) vacuum. From the data shown in Table 4.1 it is possible to confirm that C.C. under vacuum conditions can be one order of magnitude lower than in air conditions. Meaning that the power consumption will be also one order of magnitude lower.

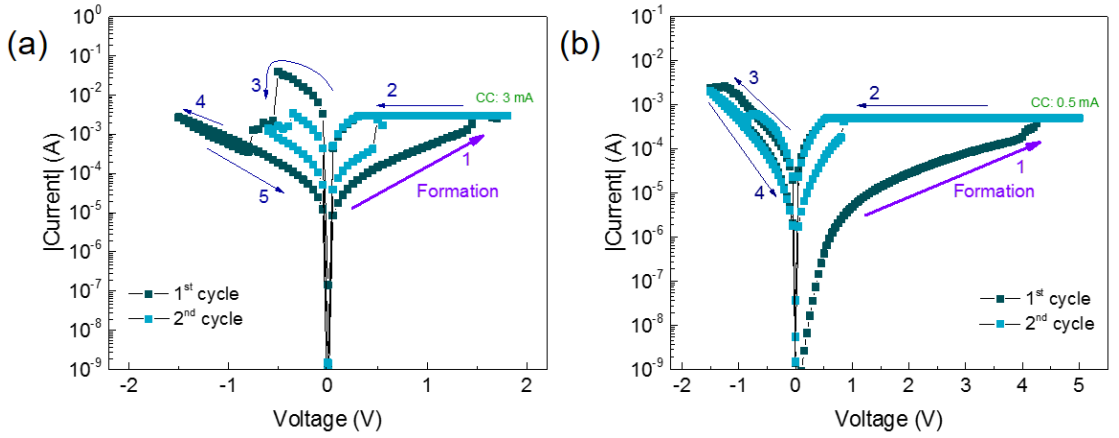

Figure 4.11– I-V characteristics of Ti/IGZOnp/Au/Ti first and second cycle (a) under air and (b) vacuum.

Table 4.1 - Electrical characteristics for the devices depicted in Figure 4.11.

	C. C.	Forming	Set Voltage	Reset Voltage	Read Voltage	Operating Window
Air	3 mA	1.45 V	0.5 V	-0.35 V	0.1 V	10
Vacuum	0.5 mA	4.25 V	0.8 V	-0.8 V	0.1 V	10

This fact can be supported by a larger initial resistance which allows a formation process for smaller C.C. but for higher voltages. In the other hand, because the device working in vacuum shows higher resistance at pristine state compared to the working device in air, it needs a larger C.C. in order to show a significant operation widow (≥10).

Also, notice that Figure 4.11 (a) presents a low forming voltage compared to those in Annex A, allowing reduced damage from the forming process.

Nonetheless, there is no difference between the all working Ti/IGZOnp/Au/Ti memories in relation to the operating window at 0.1 V read voltage.

4.5. Effect of annealing temperature

The devices were also produced with an annealing temperatures of 200 ºC to be compared with the previous 350 ºC annealed Ti/IGZOnp/Ti and Ag/IGZOnp/Ti structures. Lower process temperatures can unlock advantages since the fabrication process is cheaper and can be possible to integrate the memories on flexible substrates.

This test will also indicate if there is some influence regarding the ethylene glycol present in the IGZOnp layer, since 200 ºC is an insufficient temperature to degradate the ethylene glycol (annex G) [37]. As previously in this section all devices present the same dimension of 1.96×10^{-4} cm^2.

4.5.1. Ti/IGZOnp/Ti annealed at 200 ºC

Figure 4.12 (a) depicts a Ti/IGZOnp/Ti structure annealed at 200 ºC over 100 cycles as an endurance test, in sweep voltage mode. Set process occurs with positive voltage between 0.8 and 1.3 V and reset voltage appears for -1 to -1.5 V. The hysteresis direction is represented by the arrows (1-6), in a counterclockwise direction as usual, however it can be performed in the opposite direction due to the use of inert electrodes in both sides of IGZOnp, in the same manner as the previous Ti/IGZOnp/Ti annealed at 350 ºC.

Respective cell activation was already presented in Figure 4.3 as a pre-forming mechanism with a consecutive forming appearing at 4.73 V applying 1 mA C.C.

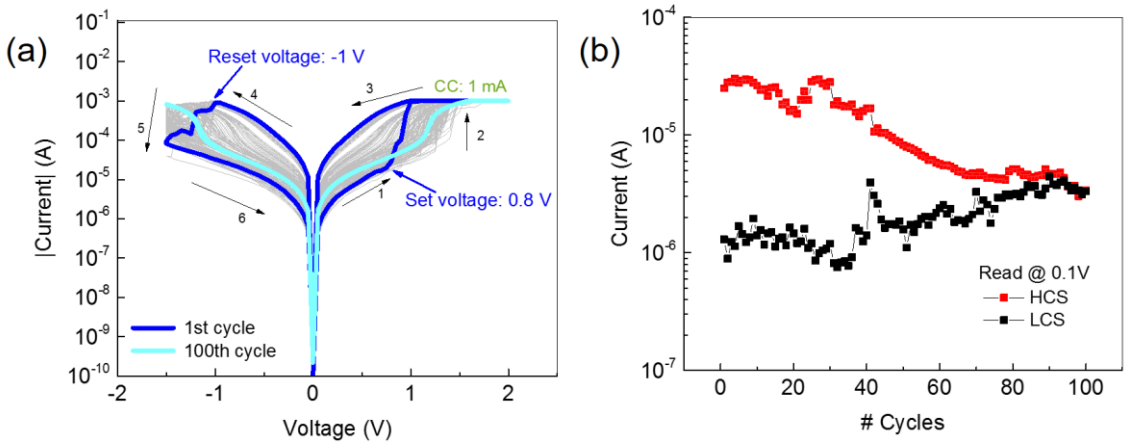

Figure 4.12 – (a) I-V characteristic of Au/Ti/IGZOnp/Ti annealed at 200 ºC over 100 cycles and respective, set and reset voltages indicated in blue represent the minimum value for each process; (b) endurance characteristics at read voltage of 0.1 V.

Figure 4.12 (b) represents the correspondent conductive value read at 0.1 V after each set and reset, equivalent to LCS and HCS respectively. It is possible to confirm an ON/OFF ratio > 10 until the 40th cycle, after which both LCS and HCS start to gradually degrade, also shown in Figure 4.12 (a) by the set and reset shift to higher values. This phenomenon can be explained by the performance drop due to overpower during pre-forming reset and consecutive forming, as seen in Figure 4.3.

From a subtract with 36 devices only two were working and both of them with pre-forming state. The rest of the devices were short circuited leading to the conclusion that IGZOnp thickness was too thin and/or there were to many pre-formed filaments for the reaching to hard breakdown. Due to the low yield no retention test was performed.

Conductive mechanism depicted in Figure 7.9 is in accordance with the SCLC as expected, Annex J.

4.5.2. Ag/IGZOnp/Ti annealed at 200 ºC

I-V characteristic in Figure 4.13 (a) depicts an endurance test in sweep voltage mode over 100 cycles to a Ag/IGZOnp/Ti structure annealed at 200 ºC. Set is performed with negative polarization occurring between -1.15 V and -0.6 V. Reset is obtained with positive voltage in an interval of 0.9 V to 1.45 V. In this memory the hysteresis as to be the one represented by the arrows (1-4) due to the cell asymmetry. Otherwise set process would not occur as described in Section 4.3.2.

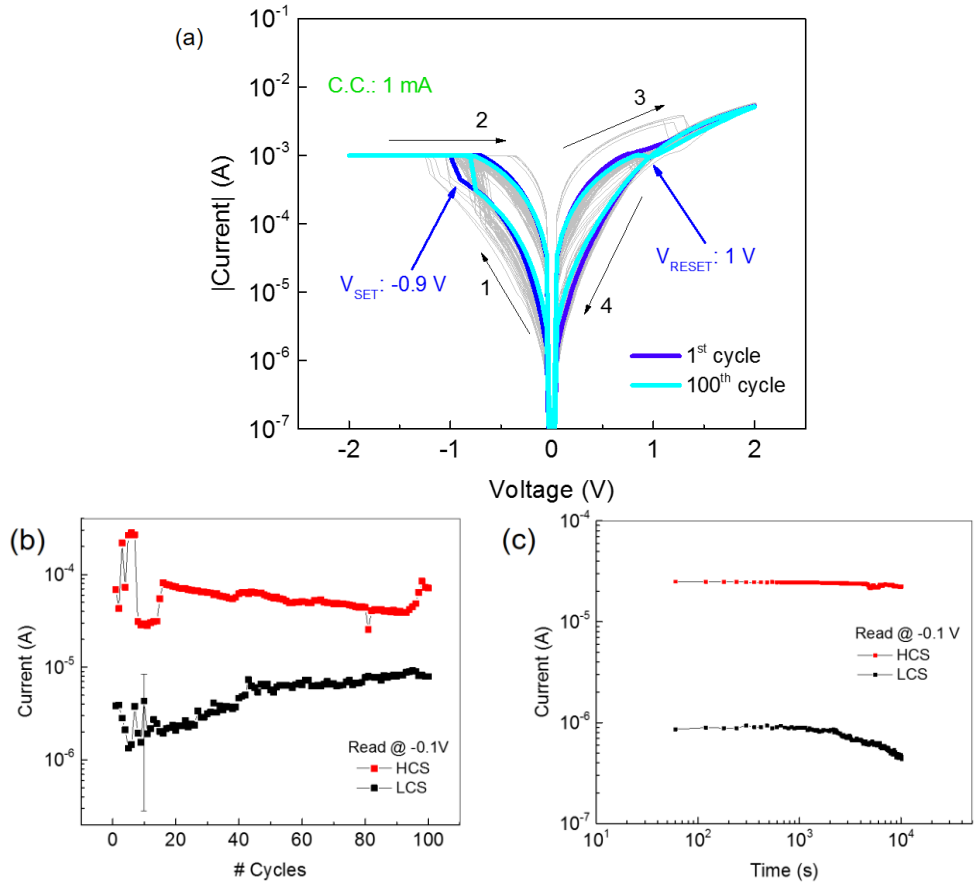

Figure 4.13 – (a) I-V characteristic of Ag/IGZOnp/Ti annealed at 200 ºC over 100 cycles and respective, set and reset voltages indicated in blue represent the value for each process in the first cycle; (b) endurance characteristics at read voltage of -0.1 V; and (c) retention characteristics read with a constant applied -0.1 V during 10^4 s.

In order to activate the cell a forming step was needed. Respective cell activation was already depicted in Figure 4.2 (b).

Figure 4.13 (b) shows the read values obtained during the endurance test. The operating window is more than one order of magnitude. Although there is a decreasing trend in ON/OFF ratio throughout the endurance test, the last cycles present a turning point in the previous trend suggesting a possible increase in further cycles.

Moreover, Figure 4.13 (c) depicts a retention characteristic executed for over 10^4 s in both HCS and LCS. The resistance state of the off-state shows a tendency to decrease even more in favour of higher on/off ratio. Suggesting a viable retention time superior to 10^4 since the HCS/LCS ratio is increased with time. Thus, this data supports a viable retention mechanism as the ratio is larger than 10 with a tendency to increase.

4.6. Ti/IGZOnp/Ti and Ag/IGZOnp/Ti performance comparison

At this point it is possible to evaluate the performance of both Ti/IGZOnp/Ti and Ag/IGZOnp/Ti and its respective temperature influence. In order to help visualizing all the results, the recorded values were depicted in Table 4.2. Notice that only the best devices for each structure with corresponding annealing temperature are included in the table. Also, the set and reset values are relative to the first cycle. It is important to refer that yield performance was calculated for devices showing stable and reliable ON/OFF states for approximately 5 cycles, due to time restrictions.

Table 4.2 - Performance comparison between Ti/IGZOnp/Ti and Ag/IGZOnp/Ti for 350 ºC and 200 ºC annealing temperatures (in red and green the worst and best resuls per line, respectively)

	Ti/IGZOnp/Ti		**Ag/IGZOnp/Ti**	
Annealing Temperature	350 ºC	200 ºC	350 ºC	200 ºC
Yield	20%	6%	64%	68%
C.C. in Forming	1 mA	1 mA	0.5 mA	10 µA
Forming	+3.5 V	+4.7 V	-1.85 V	-1.45 V
C.C.	1 mA	1 mA	5 mA	1 mA
Set Voltage	+1.25 V	+2.25 V	-1.35 V	-0.95 V
Reset Voltage	-0.8 V	-2.5 V	+1.95 V	+1 V
Read Voltage	+0.1 V	+0.1 V	-0.1 V	-0.1 V
Operating Window	<10	<10	10	10
Retention	10^4 s	-	10^4 s	10^4 s
Endurance	80/100	10	100	100

Regarding the yield, it is clear that devices with silver as top contact have a higher probability to work relatively to the ones with Ti on both electrodes. It is suggested that yield can be affected due to fabrication issues, mainly because spin coating can introduce thicker zones

than others in the same substrate. In Ti/IGZOnp/Ti devices there is also a possibility of an oxidation-reduction mechanism during the switching cycles in both electrodes may influence on device performance.

In the electroforming step the best results belong to Ag/IGZOnp/Ti devices where both C.C. and voltage is lower than Ti/IGZOnp/Ti. Ag/IGZOnp/Ti devices show higher resistivity prior the electroforming step. Therefore, lower compliance is sufficient to reach reliable resistive switching. The lower compliance is desirable for low consumption and potential risk of permanent breakdown. It leads to higher amount of endurance cycles.

Overall, it is perceived that Ag/IGZOnp/Ti annealed at 200 ºC devices present the best performance, low set and rest voltage, larger operating window for a low read voltage of -0.1 V, and stable endurance and retention.

4.7. Annealing temperature effect in IGZOnp films

In order to perceive what makes Ag/IGZOnp/Ti annealed at 200 ºC better than at 350 ºC, surface morphology analysis was performed on IGZOnp films, using AFM technique.

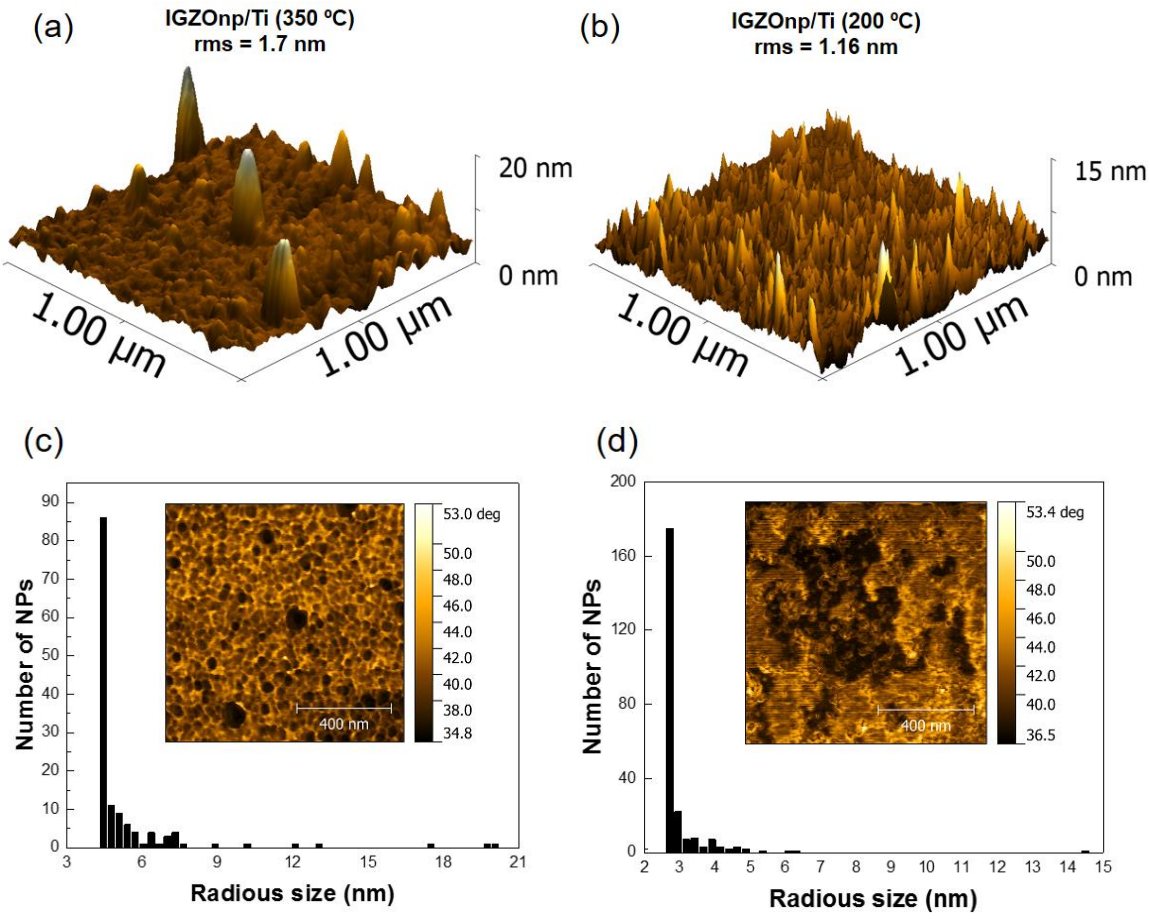

Figure 4.14 - Morphological characterization by AFM deflection images of 1 × 1 µm^2 IGZOnp on Ti annealed at (a) 350 ºC and (b) 200 ºC. Respective nanoparticles radius size distribution measured with Gwyddion software of IGZOnp on Ti annealed at (c) 350 ºC and (d) 200 ºC, the insert corresponds to the respective phase images.

From the Figure 4.14 is possible to perceive a small roughness, small nanoparticles size with good distribution as well as larger number of nanoparticles, in IGZOnp annealed at 200ºC. Supporting a notion of better film uniformity. The origin of a better film quality could rely not only on the lower temperature process but also on the ethylene glycol present in the film that prevents nanoparticles sintering by coating them.

4.8. Bipolar to unipolar transition

It is known that a memory can turn its behavior from bipolar to unipolar when a lager current compliance [50] or a larger voltage magnitude [36] is applied or also, if the memory has a symmetric structure it should present such behaviour [51].

In this case, as Ag/IGZOnp/Ti/Au annealed at 200 ºC showed the larger yield it was viable to test the transition between bipolar to unipolar. Figure 4.15 supports the fact that it is possible to obtain a unipolar behavior since (b)(unipolar) resulted from the same device in (a)(bipolar).

However, it is difficult to achieve such transition since set and reset processes occurs for similar voltages in absolute value (-0.85V to -1.3 V and 0.55V to 1.3V, respectively). Where normally to achieve unipolar for higher voltages in set process are needed, relatively to reset.

The bipolar to unipolar transition was only possible in a specific case where after approximately 40 endurance cycles the memory stopped working (not shown) since the last reset process lead to a LCS with a resistance similar to the one in pristine state. The equivalent state can be visible in Figure 4.15 where (a) starts in 1 with a current of 0.1 µA and (b) starts in 1 at 0.1 nA. This fact allowed the set voltage to be at -2 V (arrow 2) and a reset voltage at -1.6 V (arrow 5), completing a unipolar cycle. No forming step was required even with the resistance value equivalent to pristine state.

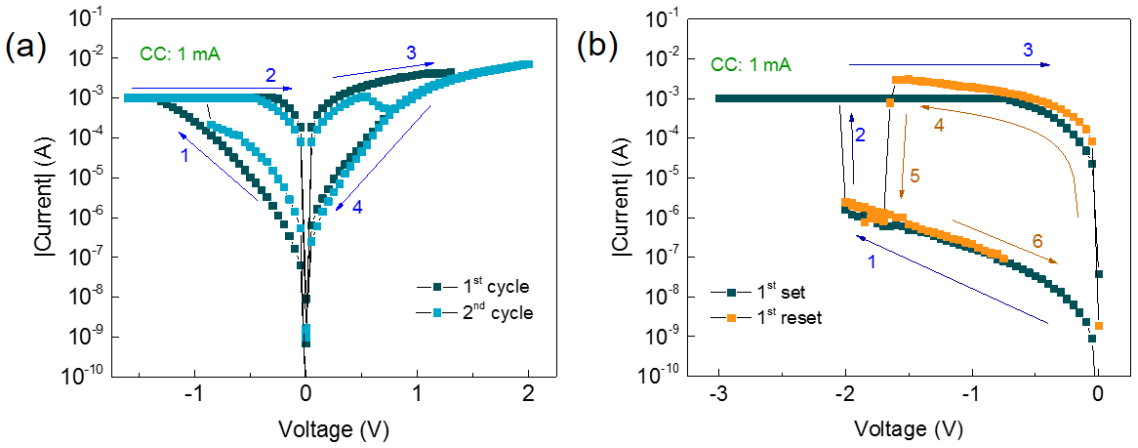

Figure 4.15 - Ag/IGZOnp/Ti cell I-V characteristics in (a) bipolar behaviour and (b) unipolar behaviour from the same device.

Although the unipolar mechanism is depicted in Figure 4.15 (b), not all Ag/IGZOnp/Ti memories function as such. As it is described before, only in the case of achieving a similar resistive state as the pristine it is possible to perform the device under unipolar mechanism. Moreover, this unipolar mechanism is unstable since only endures for 2 cycles, after which become bipolar. Given these points, Ag/IGZOnp/Ti memories work in stable mode as bipolar mechanism and it is very improbable to be subjected to thermal disruption [5] since the unipolar mechanism is unlikely to be achieved.

4.9. Current compliance influence

Current compliance can assume an important role regarding the future overall performance. In fact, as it was described in the last section, the C.C. for larger values can turn the device from bipolar to unipolar, which can reduce the device performance and endurance. Thus, it is significant to perform a study where is possible to identify the tuned C.C. which will allow the best endurance.

In order to study the most indicated current compliance to be applied at Ag/IGZOnp/Ti/Au annealed at 200 ºC, different devices were subjected to distinct CC values: 5 mA (b), 3 mA (c), 1 mA (d) and without C.C. (a) throughout an endurance test of 100 cycles at room temperature, as it is depicted in Figure 4.16. The insets in Figure 4.16 correspond to endurance characteristics of each respective I-V characteristics.

All I-V characteristics were made with the orientation illustrated in Figure 4.16 (a) represented by the arrows. Also, the forming process is not showed although it was needed a C.C. of 10 µA and -2 V to create a filament as it is shown in Figure 4.2.

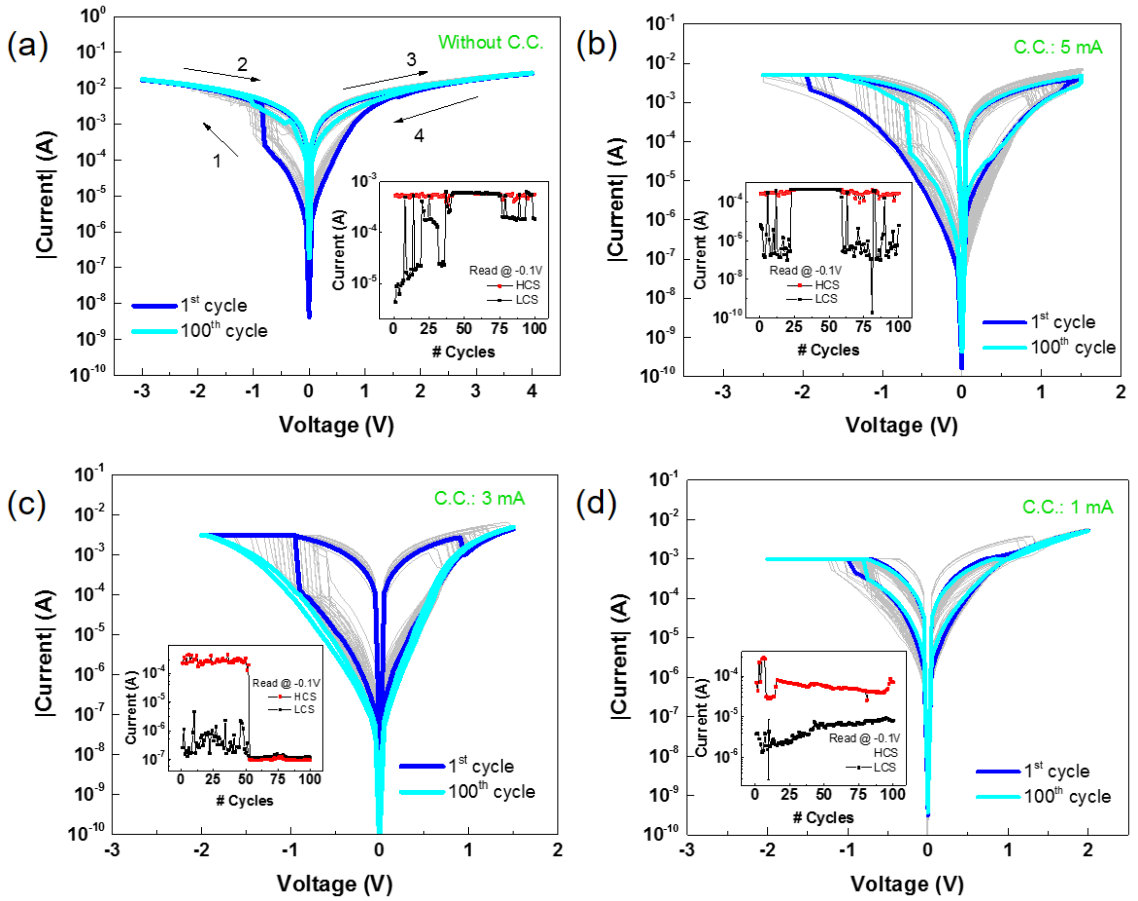

Figure 4.16 - Typical behaviour of Ag/IGZOnp/Ti/Au annealed at 200 ºC, subjected to 100 cycles with no C.C. (a) or distinct current compliances values: 5 mA (b), 3 mA (c) and 1 mA (d); and respective endurance characteristics (small inserted graphic).

Figure 4.16 shows that device switches between on and off states without the application of C.C. as already reported by different authors [7], [18], [52], [53].

In fact, a self-compliant memory can substantially simplify the circuit design for RRAM since allows one-resistor (1R) configuration being a good alternative to a one-transistor one-resistor (1T1R) configuration [54], and also can protect the cell from current overshoots during resistive switching cycles [7], [41], [42]. This fact is not supported by the depicted data in (a) since the reset ability was gradually lost in the firsts cycles which is due to a possible overpowered device.

Self-compliant mechanism could rely on small TiO_2 thickness layer, created during annealing process which acts as a series resistance, Annex K. Same mechanism was described by Maikap et. al. [54] for interfacial oxygen-rich TaO_x.

A better performance may be achieved with less positive and negative voltage in reset and set process since -2 V and 1.5 V can be enough for the device operation, as it is represented in Figure 4.16 (b). Notice that although it starts with a 5 mA C.C. the set voltage decreases and it loses the need of C.C. (see cycle 100). Even if the endurance characteristic shows an irregular stability, regarding the LCS, and it stops to reset at cycle number 23, this device presents the ability to recover the memory mechanism, can be seen at cycle number 60.

For Figure 4.16 (c) it is possible to confirm that 3 mA of C.C. are insufficient to reach a self-compliant mechanism. Moreover, it presents a 10^3 operating window even though the LCS is unstable. At cycle number 53 it suffers a possible internal breakdown preventing new set process. However, increasing the C.C. and voltage set can allow a memory recovery (not shown).

Despite the fact that all Ag/IGZOnp/Ti annealed at 200 ºC can show a self-compliant mechanism at approximately 4 mA, it is possible to conclude in Figure 4.16 (d) that 1 mA of C.C. is the best option to operate these memristors since was the only device which endured over 100 cycles with a stable difference ON/OFF ratio. This can be supported by a previous notion that providing low power (1 mA) prevents extensive cell damage, although it decreases the operating window.

As these memristors show different LCS depending on the applied C.C. it is possible that there is a multilevel state mechanism, yet no further tests were made.

4.10. Electrode material Influence

With the intention to evaluate the IGZOnp performance and its correspondent dependence on the electrode material various solution based structures were fabricated. Thus, in this section it is presented a brief summary of the collected data regarding the first cycles of: (1) Ag/IGZOnp/IZO, (2) Au/Ti/IGZOnp/Pt/Ti and (3) Ti/IGZOnp/IZO; with the two different annealing temperatures of 350 ºC and 200 ºC, as it is shown in Table 4.3.

It is important to refer that the collected data is taken from substrates with 25 devices each and three different diameters: 1.69 mm, 0.89 mm and 0.37 mm. Moreover, the subtracts maps is shown Annex L.

The reason for different devices sizes is explained by a possible area dependence regarding the HCS and LCS, meaning a non-filamentary conductive mechanism. Nevertheless, this fact cannot be proven due to the low yields and because the spin coating process can create zones with different thicknesses.

Table 4.3 is filled with a yield percentage as an approximated value to the unity, the C.C. is relative to the smallest value which allows a set process to occur, the set and reset values are

attributed for the largest voltage recorded during the first cycles, finally the read voltage is selected for the smallest value responsible to obtain a largest operating window possible in a tradeoff way. All the values from C.C., set voltage, reset voltage, read voltage and operating window are selected from the best memory in the subtract, also no forming values were recorded.

Table 4.3 - Comparison values of the first cycles from different devices using (1) Ag/IGZOnp/IZO, (2) Au/Ti/IGZOnp/Pt/Ti and (3) Ti/IGZOnp/IZO structures.

Structure	Au/Ti/IGZOnp/Pt/Ti		Ti/IGZOnp/IZO		Ag/IGZOnp/IZO	
Annealing temperature	350 ºC	200 ºC	350 ºC	200 ºC	350 ºC	200 ºC
Yield	4 %	4 %	12 %	50 %	24 %	12 %
Current compliance	1 mA	5 µA	10 µA	10 µA	0.5 mA	0.5 mA
Set voltage	+1.15 V	+2.05 V	-1.5 V	+2.2 V	-1.35 V	-1.75 V
Reset voltage	-1.3 V	-0.55 V	+0.2 V	-1.9 V	+1.2 V	+1.5 V
Read voltage	+0.04 V	+0.04	-0.1 V	+0.04 V	-0.1 V	-0.1 V
Operating Window	10^2	10^4	10^3	10^3	10^2	10^2

Observing all the devices at Table 4.3 it is possible to conclude that using a larger annealing temperature can reduce the set and reset voltages. This fact could rely on the possible ethylene glycol presence which prevents easy filament formation. Yet the used C.C. in Au/IGZOnp/Pt/Ti annealed at 350 ºC is three orders of magnitude higher than Au/IGZOnp/Pt/Ti annealed at 200 ºC meaning a much higher power consumption, also the device annealed at 200 ºC shows an operating window of 10^4.

Furthermore, Au/IGZOnp/Pt/Ti show the lowest read voltage in this work, which can be assure by the lowest resistance of top and bottom electrodes. Allowing a HCS permanence for values closer to 0V. It is important to refer that the low yield in platinum devices can be associated with a small Ti thickness causing a Pt detachment of the substrate, during the fabrication process. Consecutively, leading to a disruptor in more than 80% of the memory cells. Another advantage of annealing devices at 200 ºC is the fact that can grant a high yield visible in Ti/IGZOnp/IZO devices.

Comparing these results to the devices at Table 4.2 is possible to analyse a contradiction over the set/reset voltages for 350 ºC and 200 ºC of annealing temperature since Table 4.3 shows a trend for lower voltages at higher temperature. In other hand a larger yield is verified in both tables for lower annealing temperature. Again, memories with Ag/IGZOnp presented a negative formation suggesting a dominant VCM mechanism.

Is important to notice that although the results presented on Table 4.3 are better in comparison to Table 4.2 regarding C.C., read voltage and operating window. More studies need to be performed. Nevertheless, the main objective in this work was focus on the display parameters and not on endurance and retention evaluation.

4.11. Performance of sputtered *a*-IGZO memories

The Au/Ti/*a*-IGZO/Ti device structure was fabricated to match the previous solution based OxRAM for a more approximated comparison.

Figure 4.17 (a) shows endurance test performed over 100 cycles in sweep voltage mode at RT, being the set done with positive voltage and the reset with negative voltage, as it is represented by the arrows (1-7). Also, there is no preferential orientation regarding the set and reset, since the device presents a symmetric structure.

Notice that Figure 4.17 (a) device does not show any formation step, in other words it is a forming-free memory. This advantage in *a*-IGZO memories has already been studied and is explained by the abundant pre-existing oxygen-related defects controlled during *a*-IGZO sputtering deposition [34]. Thus it is possible to conclude that the proposed deposition parameters in terms of elements ratio and oxygen flow allow a forming-free *a*-IGZO OxRAM.

Another interesting fact about this device is the low C.C. of 10 µA compared to those in the state of the art *a*-IGZO memories contributing to a larger endurance. Regarding the set voltage, the firsts cycles appeared to be around 3 V although it gradually tends to lower values closer to 1 V in later cycles. In opposition, the reset voltage tends to start with a very fixed reset voltage of -0.4V for 80 cycles and then starting to descend for lower values.

It is possible to predict that both set and reset values are somehow correlated. However, it needs further study to reach to the most stable IGZO RRAM device. Figure 4.17 (b) confirms that the memory is robust and it still works after 100 cycles in sweep voltage with a very good retention result.

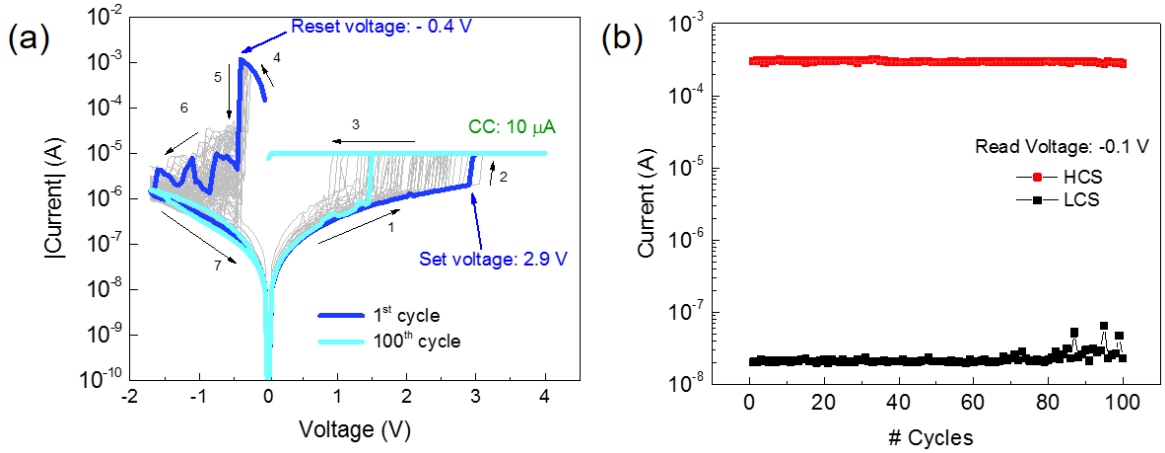

Figure 4.17 -(a) I-V characteristics of Au/Ti/*a*-IGZO/Ti device over 100 cycles and respective (b) endurance characteristics.

One may observe that after the set process in Figure 4.17 (a) a very straight line is represented (arrow 3) maintaining the C.C. value until it reaches 0 V. This fact is due to sudden filament formation responsible for decreasing the internal device resistance to a point beyond the C.C.. The corresponding conductive value is reveled at negative voltage (arrow 4). Consequently, giving a 10^4 ON/OFF ratio, shown in Figure 4.17 (b).

Because a very stable HCS is maintained even for voltages closer to 0 V, is theoretically possible to reduce the read voltage to half without changing considerably the HCS/LCS ratio.

In comparison to previous IGZOnp memories it is possible to identify a different behavior from *a*-IGZO which work as RRAM instead of memristors. suggesting that memristors are only achieved by nanoparticles in combination with Ti.

4.12. Pt/Al_2O_3/Cu_2O/ITO CBRAM

It was possible to obtain a peculiar Pt/Al_2O_3/Cu_2O/ITO memory made at Universität *Darmstadt*, where alumina layer is deposited by Atomic Layer Deposition (ALD). In fact, it was reported by Deuermeier et. al. [55] that a Cu_2O reduction takes place when a ALD layer is deposited on top, originating a thin Cu layer between Cu_2O and Al_2O_3. Thus Cu can be used as an active electrode, able to migrate through the alumina layer, acting as a CBRAM.

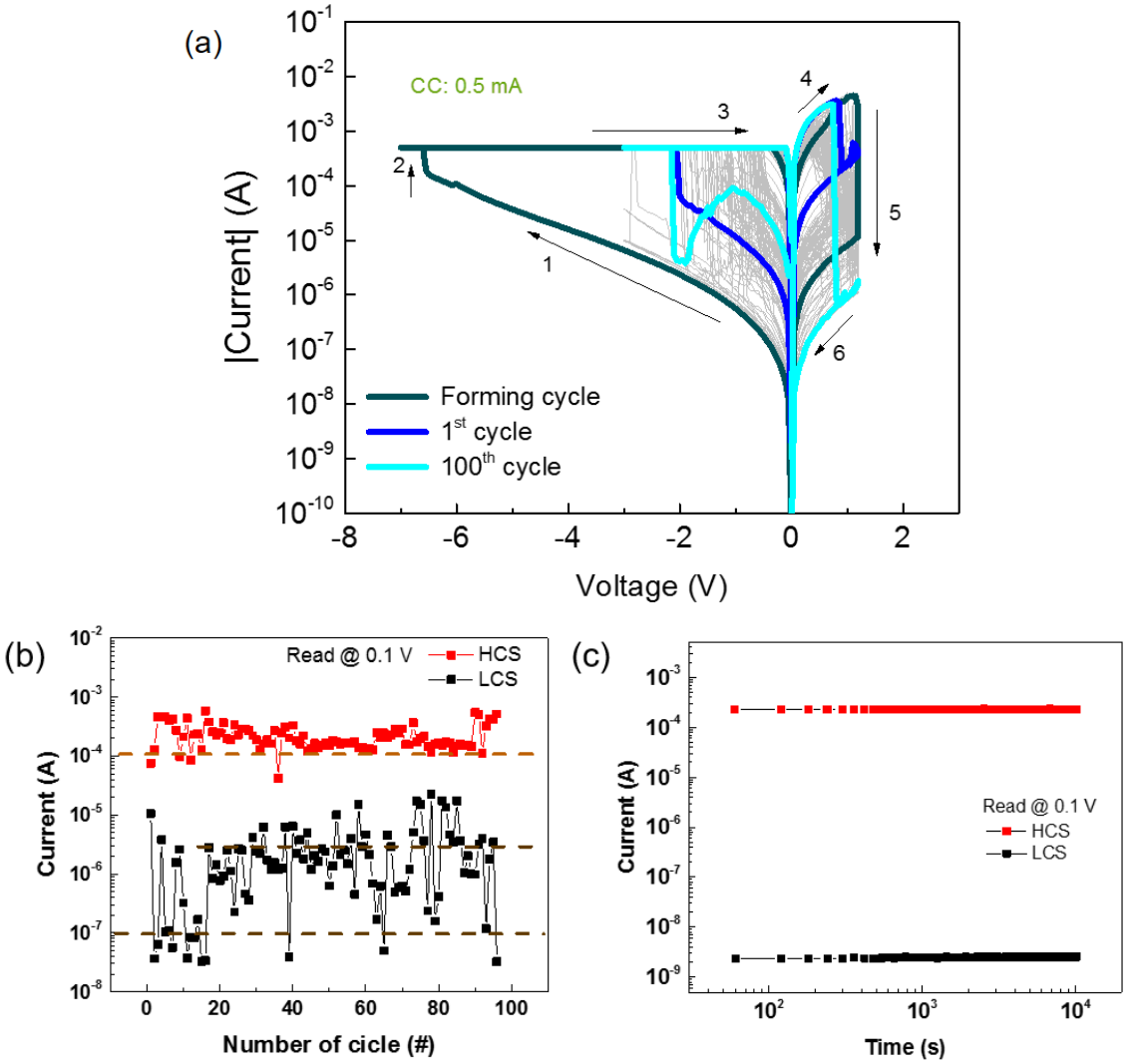

Figure 4.18 - (a) Pt/Al2O3/Cu2O/ITO I-V characteristic performed over 100 cycles, consequent (b) endurance characteristic with read voltage 0.1 V and (c) retention characteristic at RT with 0.1 V of read voltage during 10^4 seconds.

Figure 4.18 (a) depicts 100 cycles of an I-V characteristic in sweep voltage mode at RT. Before the first cycle it was needed a forming step for -6 V (not shown). Set and reset were performed with negative and positive voltage respectively with the direction represented from

arrows 1 to 6. The set with negative polarization is explained by the presence of Cu_2O/Cu on the bottom electrode, which will cause a Cu migration though the cell acting as a CBRAM.

The graph in Figure 4.18 (b) is obtained by a 0.1 V read voltage and it is visible that the memory worked during 100 cycles, however there was an instable behavior regarding the LCS and HCS with variations of three orders and two orders of magnitude, respectively. Moreover, it is possible to distinguish two different LCS yet they do not make this memory a MLC since it is an uncontrolled mechanism. Nevertheless, the medium value of the closest LCS with the HCS allows more than an operating window of 10, meaning it is a reliable memory.

Figure 4.18 (c) shows a very stable behavior in both HCS and LCS regarding the retention time over 10^4 seconds at room temperature allowing an ON/OFF ratio of 10^5.
All these results were consistent among the Pt/Al_2O_3/Cu_2O/ITO devices.

5. Conclusion and Future Perspectives

5.1. Final conclusions

In this work resistive switching memory potential of solution-based IGZOnp was fabricated and analysed.

Two memory structures were studied: Ti/IGZOnp/Ti and Ag/IGZOnp/Ti both annealed at 350 ºC. Those structures showed a memristor bipolar resistance switching mechanism. Retention times up to 10^4 s were observed for both memories. With exception of retention time in Ti/IGZOnp/Ti, the operation window for endurance tests and retention test in Ag/IGZOnp/Ti is one order of magnitude, for a read voltage of 0.1V. We showed that Ag/IGZOnp/Ti memories can withstand for more than 100 endurance cycles and Ti/IGZOnp/Ti devices can perform very well up to 80% of the cycles, demonstrating a self-healing mechanism. Conduction mechanism of the ON state is space-charge-limited conduction (SCLC). It suggests a switching mechanism based on oxygen vacancies, consistent to memories with *a*-IGZO.

Air and vacuum influence was studied, showing that devices work in both environments. However, no solid conclusion was taken since each device has its own IGZOnp thickness, and this could be the most significant parameter for the operation voltages.

Optimizing the process, we decreased the annealing temperature to 200 ºC for both devices structures: Ti/IGZOnp/Ti and Ag/IGZOnp/Ti. AFM analysis suggested that IGZOnp/Ti layers were more uniform and presented lower roughness in the case of 200 ºC of annealing temperature supporting a better behaviour in devices annealed at that temperature.

Ti/IGZOnp/Ti depicted low yield associated with an undesirable pre-forming phenomenon, which is explained by low thickness during fabrication. On the other hand, Ag/IGZOnp/Ti devices showed the best performance since the operation window was larger than one order of magnitude, retention time up to 10^4 s, more than 100 endurance cycles set and reset voltages of -1V/+1V for a current compliance of 1 mA.

Bipolar to unipolar transition was verified to be difficult to achieve with Ag/IGZOnp/Ti devices annealed at 200 ºC due to polarization symmetry in set/reset and also the need to operate with a resistance at LCS similar to the one at pristine state.

Current compliance study was performed for Ag/IGZOnp/Ti devices annealed at 200 ºC by 1mA, 3 mA, 5 mA and 10 mA compliance application. Applying 1 mA current compliance results into a long-lasting memory. Self-compliant mechanism was verified and its occurrence was noted between 3 mA and 10 mA. This phenomenon could be explained by series resistance afforded by a thin layer of TiO_X during the annealing process, protecting the device.

Other structures including: Ag/IGZOnp/IZO, Au/Ti/IGZOnp/Pt/Ti and Ti/IGZOnp/IZO were fabricated with the objective to obtain a basic analysis, to be compared with previous data. For these three devices annealing temperature of 350 ºC was determinant to achieve lower operation voltages.

To best the best of our knowledge, this is the first work that shows a memristor device based on IGZOnp fabricating with a low cost solution processing under annealing temperatures of 200 ºC. We believe that this device has a potential to be integrated in SoP technology.

5.2. Future perspectives

Although a lot was investigated regarding IGZOnp memristors and the results appear to be very promising for a solution-based device. In order to improve the switching performance, and a better understanding of physics behind the mechanism, some investigations and experiments are recommended. Thus, it is essential to perform XPS, HRTEM and I-T characteristics.

Electrical characterization using fast pulses to program devices (forming, write and erase processes) could also be useful since they provide an insight over the switching speeds and guaranty a last-longing device since the thermal component is eliminated, and consequently increasing the device endurance.

In order to increase the performance, it is suggested that a narrow approach to thickness should be done, including an ink-jet printing technique instead of spin coating. Ink jet should also allow to standardize the devices and diminish the size which theoretically will improve the yield.

Furthermore, a full transparent and flexible device could also be achieved by producing IGZOnp memories with transparent conductive oxides, like IZO and ITO.

With a full optimized device is expected that IGZOnp memristors should take a role in SoP as a viable memory organized as a passive or active matrix, and to be integrated with TFT that used the same material and/or production methods.

Devices based on Au-Ti/*a*-IGZO (ratio: 2:1:2)/Ti structure were also fabricated through the physical sputtering process as a sample of semiconductor switching matrix memory (OxRAM). In addition, we tested and analysed memory devices based on Al_2O_3, dielectric based device as a Conductive Bridge Random Access Memory (CBRAM).

Uniform memory performance was observed for *a*-IGZO memristors, and the memory window was much higher than IGZOnps devices. However, set voltage fluctuation was observed. Further study on different ratio of fabricating a-IGZO is recommended.

Moreover, CBRAM device also shows endurable resistive switching with a large window of on/off ratio. Although, it shows a non-controllable multi current levels. It can be related to the soft breakdown of dielectric which needs to be occurred at well-defined voltage to activate the memory cell.

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7. Annexes

Annex A

Table 7.1 – *a*-IGZO RRAM state of the art.

	2010 [27]	2010 [19]	2010 [29]		2011 [31]	2013 [32]	2014 [34]	2015 [8]	2016 [28]	2014 [36]
Structure	ITO/a-IGZO/ITO	Pt,Au,Al/a-IGZO/Pt/Ti	Ti/a-IGZO/TiN	Pt/a-IGZO/TiN	Cu/a-IGZO/Cu	TiN/Ti/IGZO/Pt	Ag/a-IGZO/Pt	Ag/SiO_2/IGZO/Pt/Ti	IZO/IGZO/ITO	Pt/IGZO/Pt
Ratio In:Ga:ZnO	1:1:1	1:1:2	1:1:1		-	-	2:2:1	1:1:2	-	1:1:1
Process	Sputtered	PLD	Sputtered		Sputtered	Sputtering	Sputtered	Sputtered	Sputtered	Photochemical solution deposition
Thickness	100 nm	100 nm	30 nm		60 nm	40 nm	30 nm	40 nm	25 nm	
Dimensions	$7.8x10^{-3}$ cm^2	-	0.64-64 μm^2		$7.8x10^{-3}$ cm^2	$3.1x10^{-3}$ cm^2	$7.1x10^{-3}$ cm^2	$7.8x10^{-3}$ cm^2	$4.2x10^{-3}$ cm^2	$7.1x10^{-3}$ cm^2
Operation type	bipolar	unipolar	bipolar	unipolar	unipolar	bipolar	bipolar	bipolar	bipolar	Unipolar and bipolar
Set Voltage	-1.5 V	3 - 4 V	+0.6 V	> +3 V	+1.5 V	+2.5 V	+0.8 V	+0.75 V	+0.83 V	+2 V
Reset Voltage	+ 3.5 V	0.4 V	- 1 V	+ 1 V	+0.5 V	-1.5 V	-1 V	MLC: -0.45 V, -0.65 V, -0.85 V	-0.76 V	-1 V
Forming Voltage	-	6.14 V	+ 6.4 V (With 0.1mA CC)	-	-	6 V	-	+ 2.5 V	Forming free	+9 V
Read Voltage	-0.2 V	-	+0.1 V	+0.1 V	-	+0.3 V	-0.1 V	-0.1 V	-	+0.2 V
Current Compliance	10 mA	10 mA	1 mA	1 mA	3 mA	10 mA	10 mA	0.1, 1 and 10 mA	10 mA	10 mA
Retention	10^4 s @ 90ºC	-	-	-	-	-	10^4 s @RT	10^4 s @ 85ºC	10^4 s @ 85ºC	10^4 s
Endurance	100 cycles	-	100 cycles		150 cycles	1000 cycles	-	100 cycles	10^6	100 cycles
Window	10^2	-	10^2	10^2	10^2 – 10^3	10	10^2	10^4	10^3	10

Annex B

IGZO nanoparticles morphological characterization through SEM visualization (Figure 7.1 (a,b)) and energy-dispersive X-ray spectroscopy (EDS) for chemical composition analysis (Figure 7.1 (c-f)).

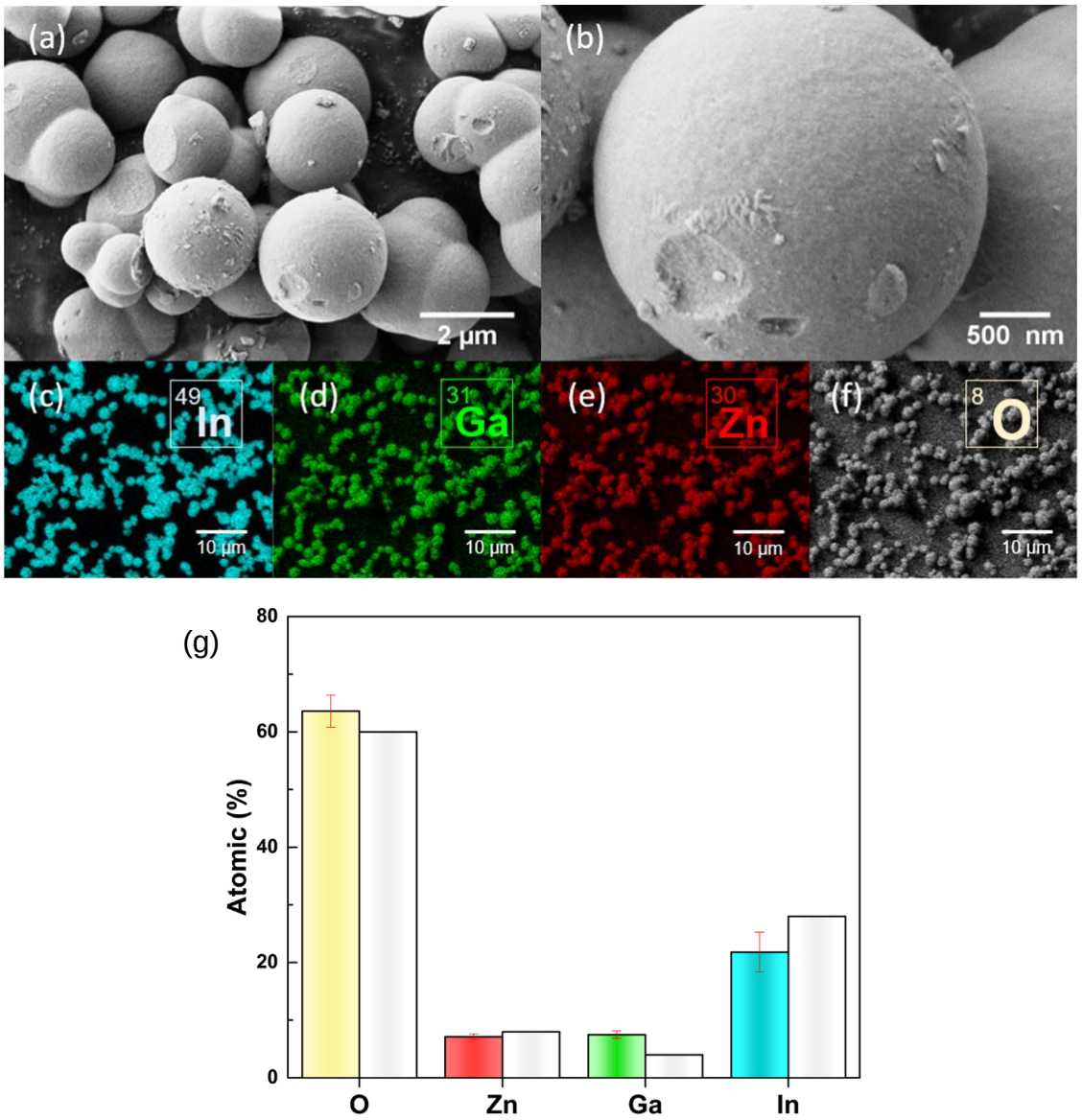

Figure 7.1- (a,b) SEM images of the small nanoparticles agglomerates with different magnifications; (c-f) EDS elements mapping; and (g) atomic percentages calculated as an average of 10 different samples of IGZO (coloured) and respective percentages before synthesis (blank).

From SEM images it is visible small nanoparticles agglomerates with a consistent size in the order of 2 µm [37]. Moreover, a uniform cation distribution is discernible in the element mapping (Figure 7.1 (c-f)). EDS demonstrate a 3:1:1 atomic ratio in In:Ga:Zn, instead of 7:2:1 used as initial precursors proportion. This can be explained by a mass percentage loss during the manufacturing process.

Annex C

FTIR-ATR spectra of IGZO nanoparticles, (Figure 7.2) after solvent evaporation at different temperatures for one hour. At 80 ºC is expected the ethanol evaporation remaining 2-metoxyethanol, ethanolamine and water, this effect is confirmed by a band at OH region (around 3350 cm^{-1} and 2500 cm^{-1}) and bands bellow 1800 cm^{-1}. Consecutive higher temperatures depicted a band decrease along the spectra, as expected. Notice that for 200 ºC occurs a total water evaporation and a partial evaporation of 2-metoxyethanol and ethanolamine. At 350 ºC any 2-metoxyethanol and ethanolamine can be detected represented by a flat spectra.

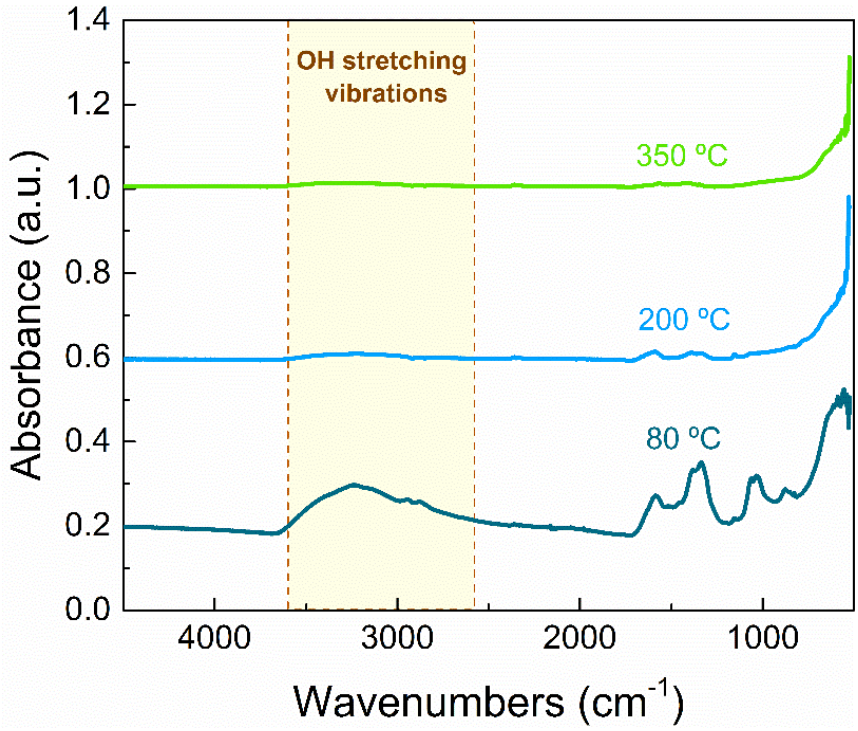

Figure 7.2 - FTIR-ATR spectra of IGZO nanoparticles after solvent evaporation at 80 ºC, 200ºC and 350ºC.

Annex D

In order to determine the IGZO nanoparticle optical band gap, Tauc's plot was used, recurring to the equation (7.1):

$$\alpha h\upsilon = \mathrm{A}(h\upsilon - Eg)^{n} \qquad (7.1)$$

Where α corresponds to the absorption coefficient, $h\upsilon$ is the photon energy, A is a constant and n depends on the type of optical transition. In this case $n = 2$ meaning an indirect allowed transition occurrence. From the linear fit in Figure 7.3 was possible to determine the optical band gap with 3.74 eV, which is a similar value to the one obtained by Santos et. al. [37].

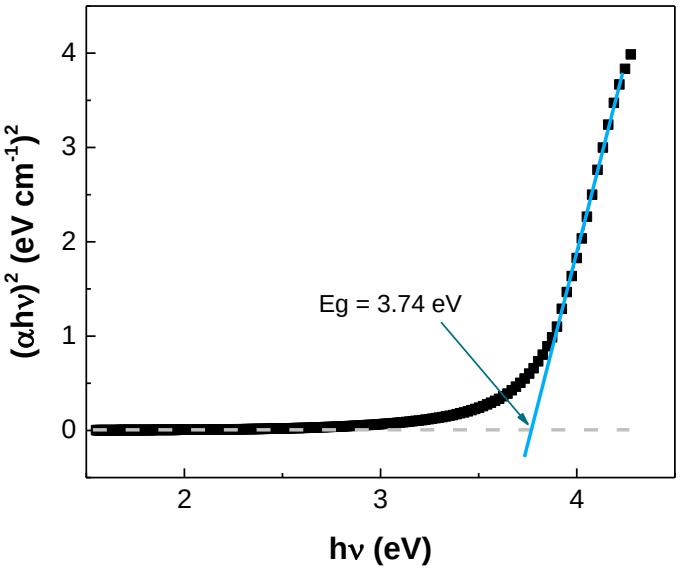

Figure 7.3 - Tauc's plot for IGZOnp dispersed in ethanol.

Annex E

XRD measurements of the IGZO nanoparticles thin film were performed at different annealing temperatures where it is possible to confirm the presence of the a-IGZO structure up to 350 ºC. The IGZO crystallization at 900 ºC was performed in order to identify the type of structure produced by this method where it is visible the presence of the three different oxides, as Figure 7.4.

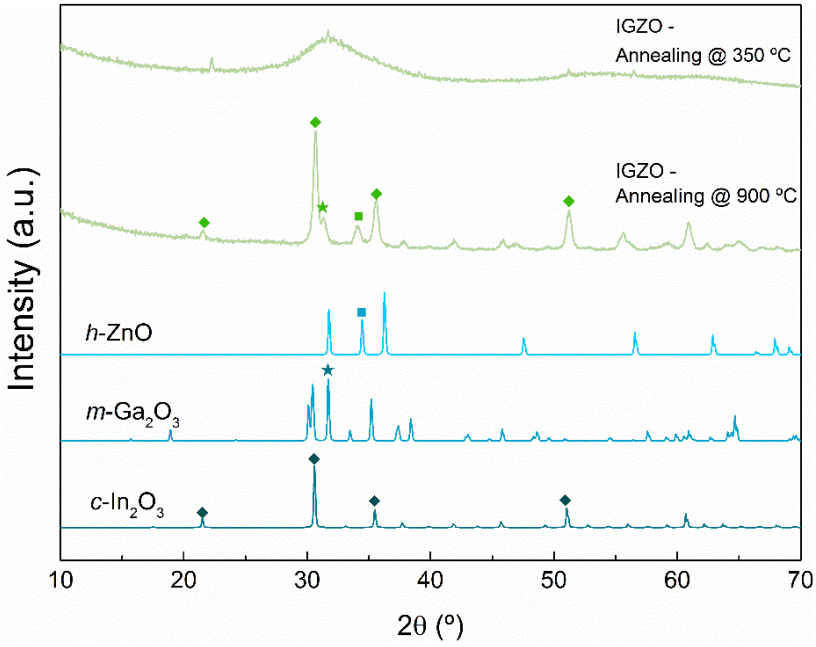

Figure 7.4 - XRD diffractograms of IGZO nanoparticles obtained after annealing at 350 ºC, IGZO nanoparticles after annealing at 900 ºC, and reference ICDD diffractograms of *h*-ZnO, *m*-Ga_2O_3 and *c*-In_2O_3 used for identification (file numbers 05−0664, 41−1103, and 06−0416, respectively).

Annex F

DLS measurements were performed with IGZO inks in different production steps to analyse the nanoparticle size distribution, Figure 7.5. Ideally the sonication step should lower the nanoparticle size distribution, however it is noticeable a rise in the size which can be explained by the nanoparticles impact causing agglomerations throughout the process. Though, after filtration the medium size becomes the same as before sonication. The hydrodynamic diameter is found around 100-300 nm which do not correspond to SEM (Annex B) and AFM (Figure 4.14) measurements. This is expected since the analysis is performed in the dispersions giving information on the inorganic core along with the solvent layer attached to the particle as it moves under the influence of Brownian motion [37].

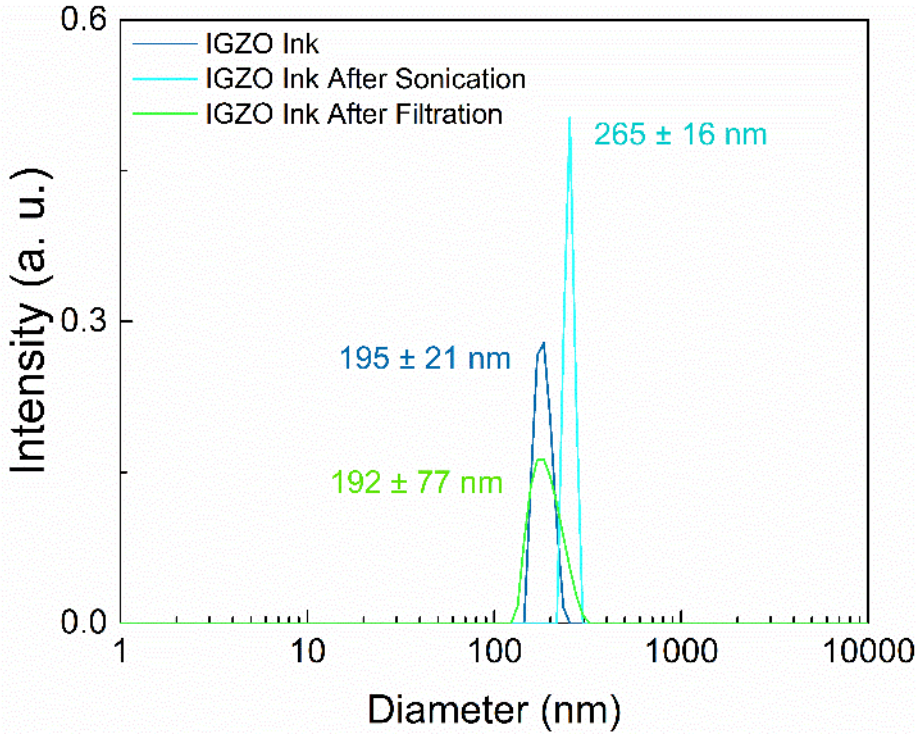

Figure 7.5 - DLS size distribution of IGZO ink before sonication, after sonication and after filtration.

Annex G

Thermal analysis of the prepared IGZO inks by DSC-TG experiment demonstrates that the ethanol ebullition occurs around 75 ºC and ethylene glycol degradation at 150 ºC, Figure 7.6. With this measurement was also possible to determine that 8.7% nanoparticles weight are loss during the filtering process with a 0.45 µm filter. Meaning that the IGZO ink has 5.4% in weight of nanoparticles after filtration. The increase in the heat flow after 300 ºC is an equipment misreading, since there is no weight loss at that temperature or beyond.

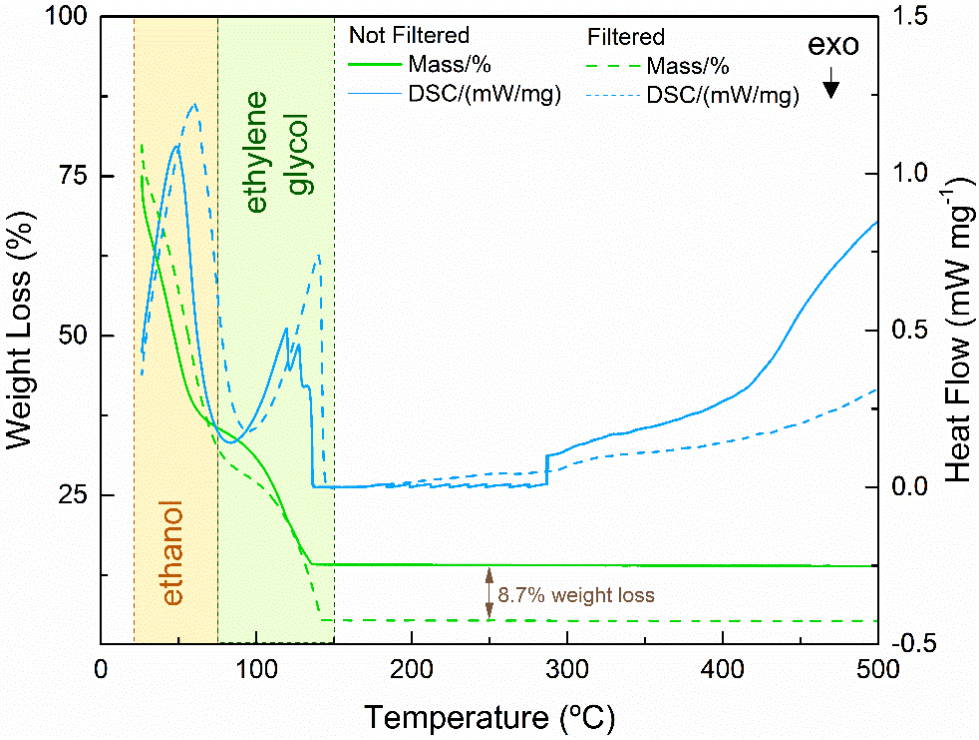

Figure 7.6 - DSC-TG results performed in air from ambient temperature to 500 ºC for filtered and not filtered IGZO inks.

Annex H

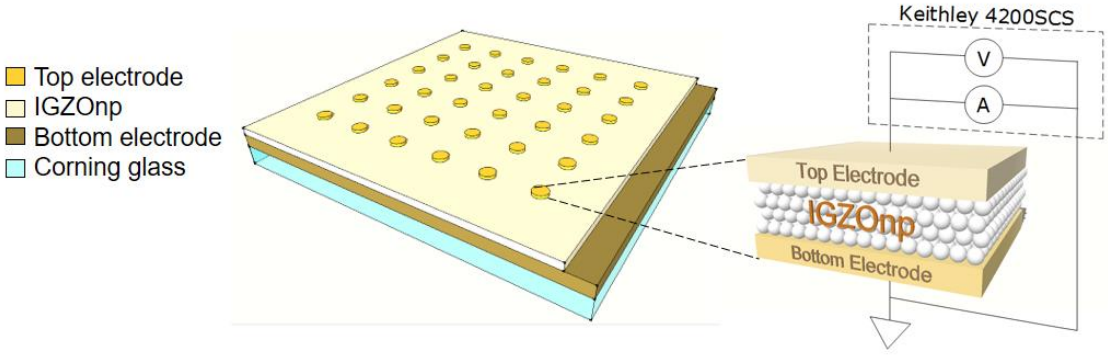

Figure 7.7 – Typical substract with 6x6 device matrix with layer identification, and respective device representation (right).

Annex I

Ti/IGZOnp/Au/Ti subtract map containing 36 devices each with $3.3x10^{-3}$ cm^2 of the titanium top contact. From row 1 to 3 I-V characteristic was made in air atmosphere and from row 4 to 6 I-V characteristic was made in vacuum ambient with $3.33x10^{-4}$ mBar.

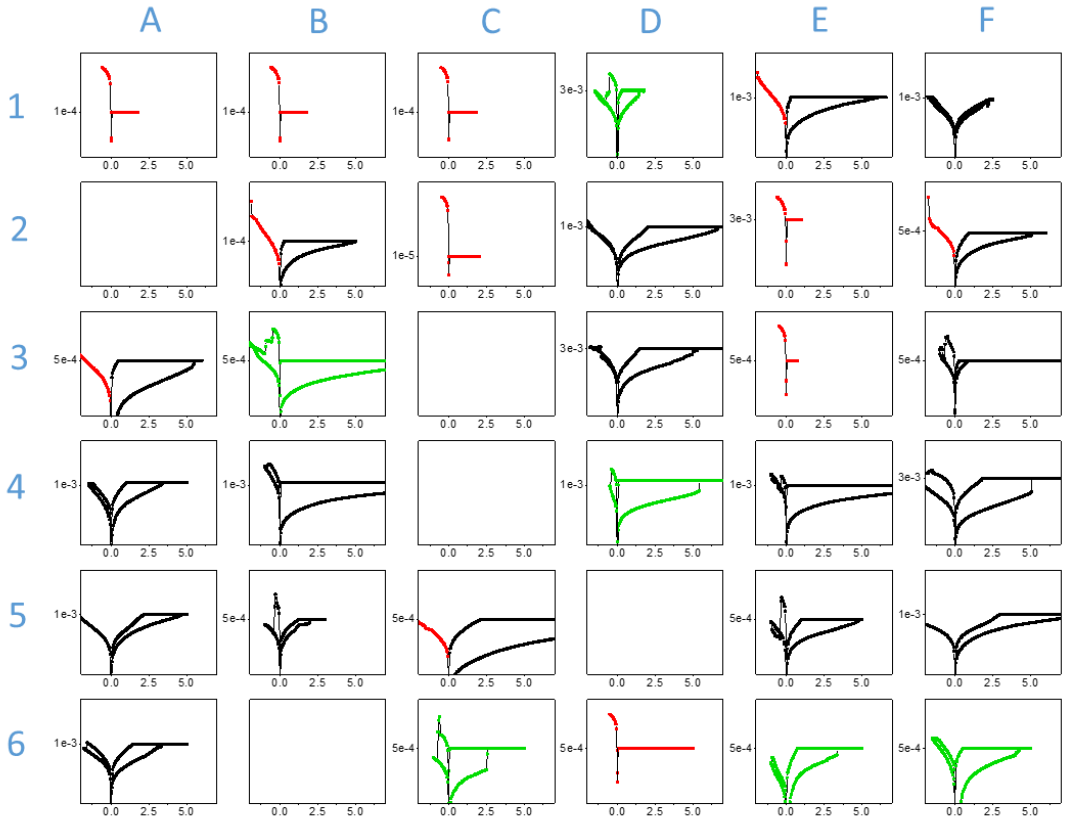

Figure 7.8 - Ti/IGZOnp/Au/Ti subtract map which shows the first cycle. Bipolar working devices (green); non stable devices (black); short circuits (red), devices not analysed (blank graphics).

The devices represented with a black I-V characteristics shown a non-stable behavior since only tolerate the first cycle (with forming) and so no further conclusions can be taken. Notice that some of the devices short circuited in a reset attempt evidencing a very sensitive RS. It is speculated that it can be explained by a small IGZOnp layer thickness which instead of causing a filament disruption, produce an opposite larger filament short circuiting the device.

Annex J

Conductive mechanism of Au/Ti/IGZO/Ti device annealed at 200 ºC.

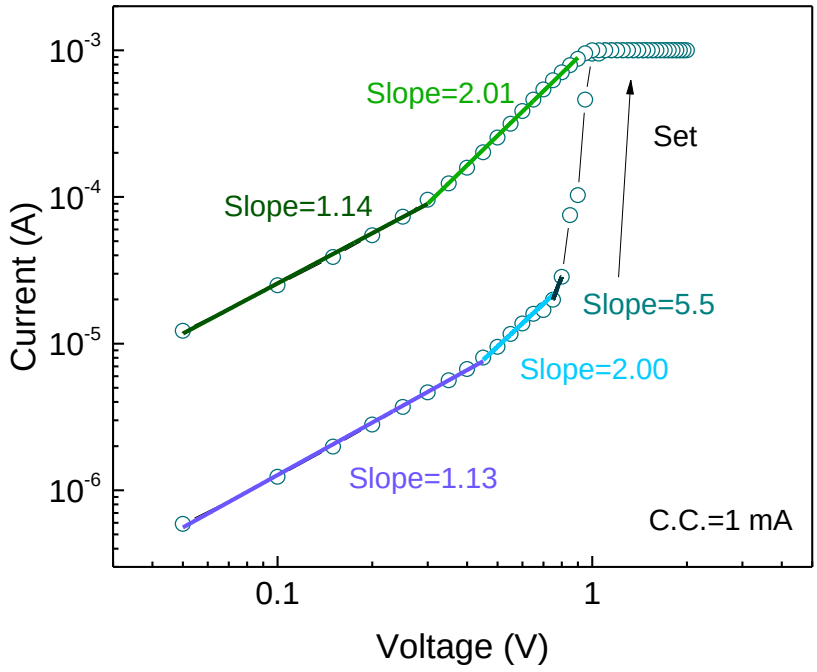

Figure 7.9 - I-V characteristics of Au/Ti/IGZOnp/Ti structure plotted in log-log scale to evaluate the conduction mechanism.

Annex K

Table 7. 2 - Approximated resistance values for each electrode used in IGZO memory devices.

Metal contact	Gold	Platinum	Silver	IZO	Titanium	Titanium after annealing (200 and 350 ºC)
Resistance [Ω]	1	2	1	500	2	200

The increase in Ti resistance after annealing can be associated to the Ti oxidation, and consequent TiO_2 thin layer formation.

Annex L

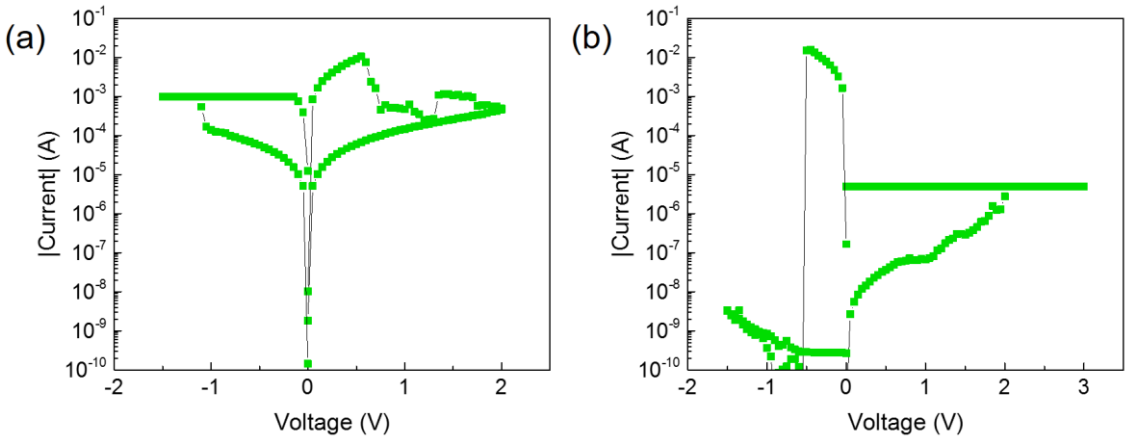

Figure 7.10 - I-V characteristics of Au/Ti/IGZOnp/Pt/Ti annealed at (a) 350 ºC with 1.68 mm and (b) 200 ºC with 0.89 mm.

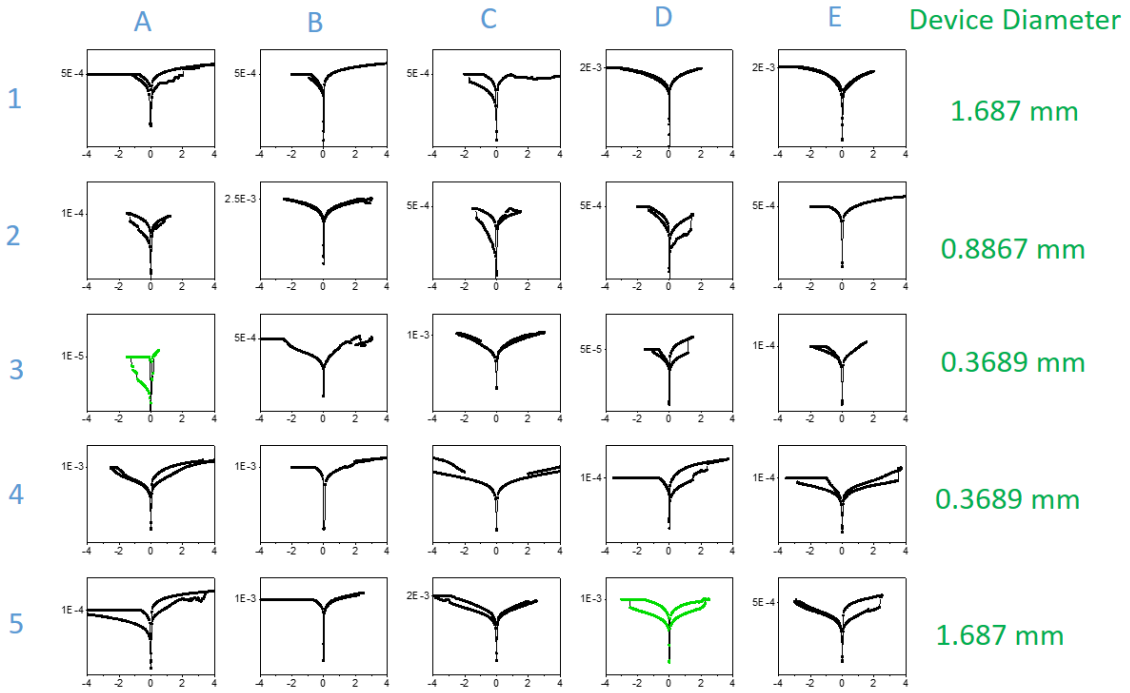

Figure 7.11 - I-V characteristics map of Ti/IGZO/IZO structures annealed at 350 ºC in green the bipolar memories and in black no memory behaviour displayed. The column in green represents the diameter used for the memories in the same row. The respective C.C. value for each device is displayed in the y axis.

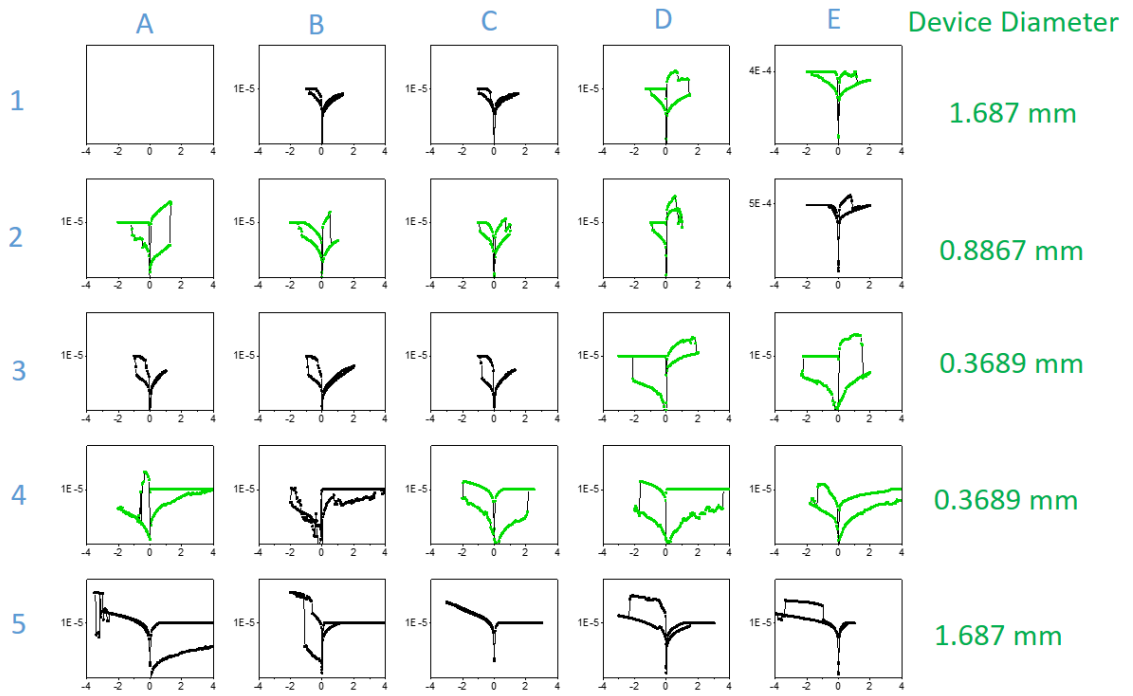

Figure 7.12 - I-V characteristics map of Ti/IGZO/IZO structures annealed at 250 ºC in green the bipolar memories and in black no memory behaviour displayed. The column in green represents the diameter used for the memories in the same row. The respective C.C. value for each device is displayed in the y axis. Blank graphic represents devices that were not analysed.

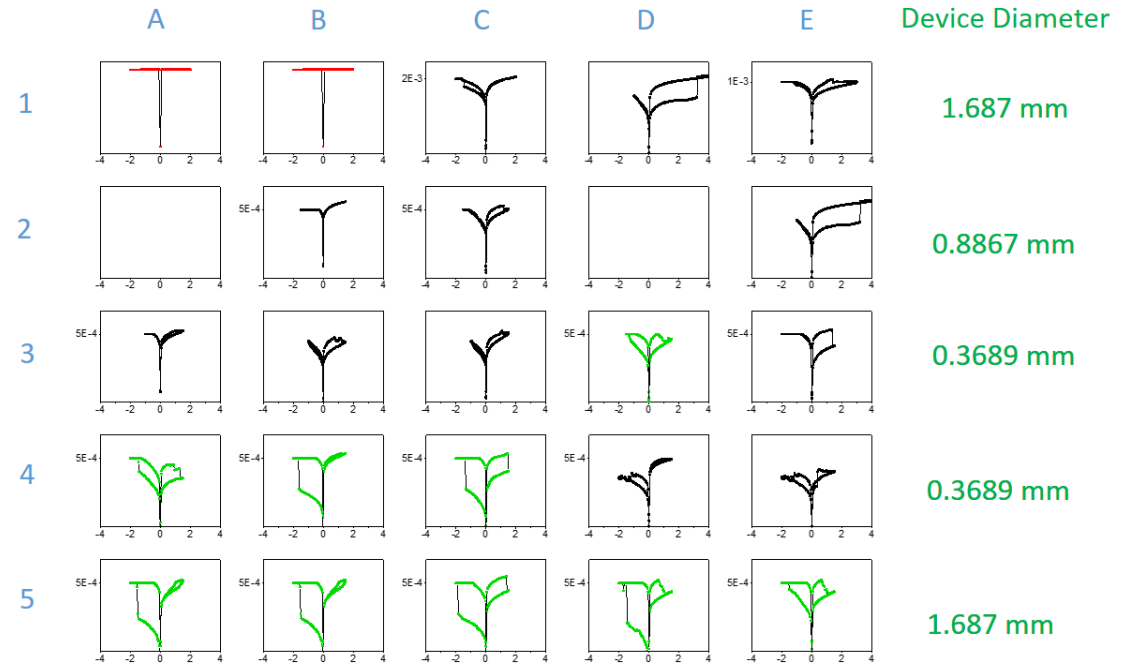

Figure 7.13 - I-V characteristics map of Ag/IGZO/IZO structures annealed at 300 ºC in green the bipolar memories, in black no memory behaviour displayed, in red short circuited devices. The column in green represents the diameter used for the memories in the same row. The respective C.C. value for each device is displayed in the y axis. Blank graphic represents devices that were not analysed.

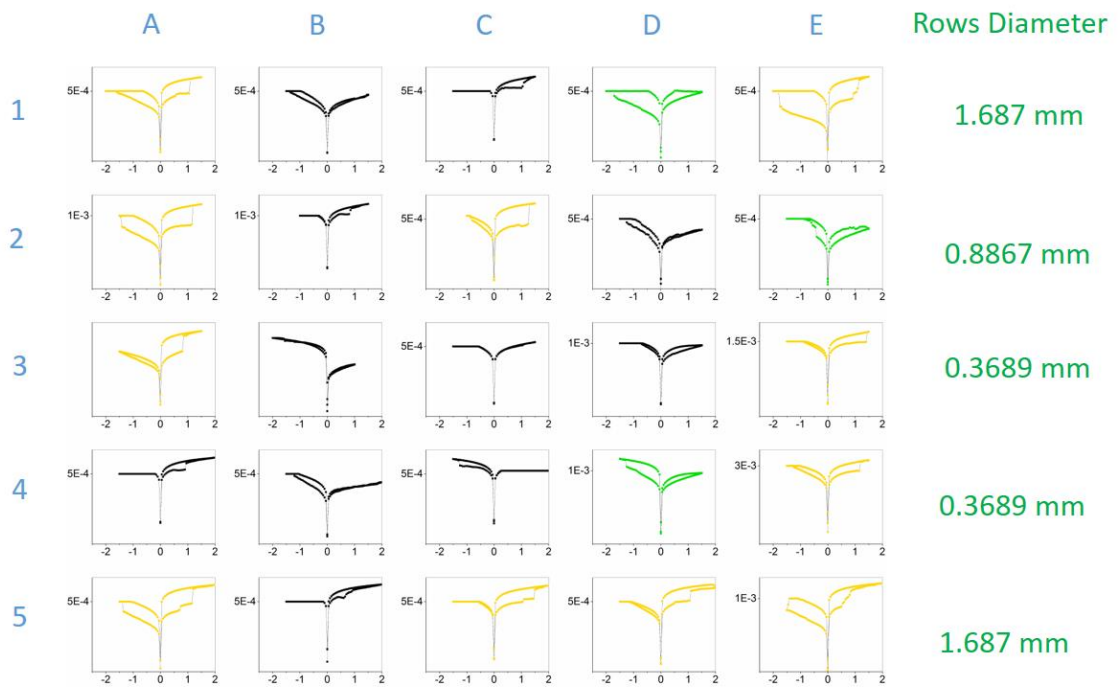

Figure 7. 14 - I-V characteristics map of Ag/IGZO/IZO structures annealed at 350 ºC in green the bipolar memories, in black no memory behaviour displayed, in light orange identifies a two regime memory[1]. The column in green represents the diameter used for the memories in the same row. The respective C.C. value for each device is displayed in the y axis. Blank graphic represents devices that were not analysed.

[1] It is identified a two regime memory since cell activation was performed with negative polarization, and the consequent positive voltage application revelled a set process instead of a reset, suggesting a silver filament formation. No more cycles were effectuated in order to identify the dominant conductive mechanism.