



DEPARTMENT OF ELECTRICAL
AND COMPUTER ENGINEERING

CAROLINA FILIPA RODRIGUES COELHO GOMES DE
ALMEIDA

BSc in Electrical and Computer Engineering

DEVELOPMENT OF IGZO THIN-FILM TRANSISTORS (TFT_s) COMPACT MODELS

MASTER IN ELECTRICAL AND COMPUTER ENGINEERING
SPECIALIZATION IN ELECTRONICS

NOVA University Lisbon
September, 2025

DEVELOPMENT OF IGZO THIN-FILM TRANSISTORS (TFTs) COMPACT MODELS

CAROLINA FILIPA RODRIGUES COELHO GOMES DE ALMEIDA

BSc in Electrical and Computer Engineering

Adviser: Maria Helena Silva Fino

Associate Professor, NOVA University Lisbon

Co-adviser: Pedro Miguel Cândido Barquinha

Associate Professor, NOVA University Lisbon

Examination Committee

Chair: Fernando Coito

Associate Professor, NOVA University Lisbon

Rapporteur: João Pedro Oliveira

Associate Professor, NOVA University Lisbon

Adviser: Maria Helena Silva Fino

Associate Professor, NOVA University Lisbon

Development of IGZO thin-film transistors (TFTs) compact models

Copyright © Carolina Filipa Rodrigues Coelho Gomes de Almeida, NOVA School of Science and Technology, NOVA University Lisbon.

The NOVA School of Science and Technology and the NOVA University Lisbon have the right, perpetual and without geographical boundaries, to file and publish this dissertation through printed copies reproduced on paper or on digital form, or by any other means known or that may be invented, and to disseminate through scientific repositories and admit its copying and distribution for non-commercial, educational or research purposes, as long as credit is given to the author and editor.

To my true family — born or found.

ACKNOWLEDGEMENTS

This thesis is the culmination of a long journey, not always an easy one, but a very special one. Along the way, I had the privilege of being supported by wonderful people who believed in me. I could not have accomplished this without all of you.

First, I would like to express my deepest gratitude to my advisor, Professor Maria Helena Fino, for her constant guidance, dedication, and tireless support throughout this project. I am also sincerely grateful to my co-advisor, Professor Pedro Barquinha, for providing all the TFT data that supported this work, as well as for his invaluable help.

To my parents, I owe a very special and heartfelt thank you for their unwavering support, endless patience, belief in me, and above all, for their unconditional love. You are my safe place.

To my true family, both the one I was born into and the one I have found along the way, I feel incredibly fortunate to have you all in my life.

A very special thank you to Volt and Ben, my four-legged emotional support and source of unconditional love, who accompanied me through every step of this journey and never left my side, no matter how long the study sessions lasted.

My deepest thanks also go to Rodrigo, the other element of my RC circuit, for being the best partner I could have asked for in both life and the lab. Thank you for continuously challenging me and celebrating my achievements with me.

To Miguel, Rodrigo, Inês, David, João, and Marco, some of the best surprises university has given me, thank you for becoming the family I chose, and the one I will carry with me forever. You made every step of this path more meaningful, and without you, none of these achievements would have been possible. I will always be grateful for the memories we created together.

To the wonderfully crazy souls who had the courage to choose me to guide them on their journey, a heartfelt thank you. You are always in my heart.

Finally, I cannot fail to thank Fátima and Patrícia for their constant encouragement and belief in me. To the entire Jumping Mind Academy, thank you for teaching me that true success is achieved with heart.

”

*“A mind needs books as a sword needs a whetstone,
if it is to keep its edge.”*

— **George R. R. Martin**

ABSTRACT

Indium–gallium–zinc oxide thin-film transistors (IGZO-TFTs) have emerged as a promising alternative to amorphous silicon TFTs in applications such as high-resolution displays and flexible, transparent electronic devices. In this work, a compact model for IGZO-TFTs is proposed, together with an automatic parameter extraction methodology based on experimental data from TFTs with varied geometries. The model was validated in terms of scalability and performance in both linear and saturation regimes, showing good accuracy when compared with laboratory measurements. Its implementation in Verilog-A enabled circuit-level simulations, demonstrating the robustness of the model for integration into Process Design Kits (PDKs) for IGZO-TFTs. The results highlight the potential of the model to accelerate the development of circuits based on IGZO-TFT technology.

Keywords: IGZO-TFT, Compact Model, Parameter Extraction, Amorphous Transistors, Small-Signal Model, PDK

RESUMO

Os transistores de óxido de índio-gálio-zinco de filme fino (IGZO-TFTs) surgem como alternativa promissora aos TFTs de silício amorfo em aplicações de ecrãs de alta resolução e dispositivos eletrónicos flexíveis e transparentes. Neste trabalho, propõe-se um modelo compacto para IGZO-TFTs e uma metodologia automática de extração de parâmetros a partir de dados experimentais de TFTs com geometrias variadas. O modelo foi validado quanto à escalabilidade e ao desempenho nos regimes lineares e de saturação, apresentando precisão quando comparado com os dados laboratoriais. A implementação em Verilog-A permitiu a simulação em nível de circuito, demonstrando a robustez do modelo para a integração em Process Design Kits (PDKs) de IGZO-TFTs. Os resultados obtidos evidenciam o potencial do modelo para acelerar o desenvolvimento de circuitos baseados em IGZO-TFTs.

Palavras-chave: IGZO-TFT, Modelo Compacto, Extração de Parâmetros, Transistores Amorfos, Modelo Pequenos Sinais, PDK

CONTENTS

List of Figures	ix
Acronyms	xv
Symbols	xvii
1 Introduction	1
1.1 Motivation	1
1.2 The History of TFTs	2
1.3 Objectives	3
1.4 Main Contributions	4
2 Background and Literature Review	5
2.1 Device Compact Modelling	5
2.2 MOSFET Compact Modelling	6
2.2.1 Shockley Model	6
2.2.2 Nth Power Law MOSFET Model	6
2.2.3 <i>Nexp</i> Model	7
2.2.4 EKV Model	8
2.3 TFT Compact Modelling	9
2.3.1 RPI Model	9
2.3.2 Surface-Potential-Based Compact Model	13
2.3.3 TFT Contact Resistances Model	15
2.3.4 CAMCAS Model	17
2.4 Conclusions	19
3 Fully Automatic Parameter Extraction Methodology	21
3.1 Dataset Description for Model Evaluation	21
3.2 Parameter extraction	22
3.3 Model Scalability and Behavior with Varying Channel Lengths	24

3.3.1	Results Achieved for Dataset 1	24
3.3.2	Results Achieved for Dataset 2	25
3.3.3	Results Achieved for Dataset 3	29
3.4	Conclusions on Model Scalability	31
3.4.1	Results Achieved	32
3.4.2	Validation of the Scalable Model	35
4	Small Signal Modelling	39
4.1	Small Signal Modelling for Thin-Film Transistors (TFTs)	39
4.1.1	From the General 3-Terminal Device Model to the TFT Small Signal Model	39
4.1.2	Adaptation Toward TFTs	41
4.2	Model Validation	44
4.2.1	Verilog-A Model Implementation	49
5	Conclusion	52
	Bibliography	54
	Appendices	
A	Transfer Characteristics Dataset 1	60
B	Transfer Characteristics Dataset 2	64
C	Transfer Characteristics Dataset 3	70
D	Dataset 3 DC Model Results	72
E	Scalable Coefficients	79
F	Verilog-A Model Implementation	85

LIST OF FIGURES

1.1	Timeline of TFT development	3
2.1	Transfer characteristic for different values of V_{gs} - Comparison for measured and modeled (using RPI model) for an a-Si:H TFT. Adapted from [48]	10
2.2	Measured and simulated $V_{th(L)}$ and the influence of the variation of the parameter P_{Vr} . Adapted from [49]	11
2.3	Measured and modeled data as function of channel length L for $V_{DS}=2$ V and $V_{GS}=5$ V with a constant channel width W . Adapted from [49]	11
2.4	Measured and simulated characteristics of the a-IGZO TFT with fixed dimensions. Adapted from [49]	12
2.5	Comparison between the experimental and modeled data - Transfer characteristics of IGZO. Adapted from [34]	15
2.6	TFT structure with contact resistance. Adapted from [51]	16
2.7	Transfer characteristic- a) with the conventional power-law models model for sub- and above-threshold; b) with unified model which can represent both regimes at the same time. Adapted from [35]	17
2.8	Comparison of modeled and measured data, for linear and saturation regimes. Adpated from [56]	19
3.1	Total TFT resistance vs TFT lenght for different V_{GS} to extract ΔL and R_{SD} , using a $V_{DS} = 0.1V$. The data corresponds to the device with $W = 50 \mu m$ and $L = 50 \mu m$ from Dataset 3, used here as an illustrative example.	23
3.2	Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 100 \mu m$ and $L = 20 \mu m$	35
3.3	Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 100 \mu m$ and $L = 10 \mu m$	35
3.4	Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 100 \mu m$ and $L = 5 \mu m$	36
3.5	Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 100 \mu m$ and $L = 20 \mu m$	36

3.6	Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$	37
3.7	Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$	37
3.8	Relative error of the scalable model for devices with $W = 100 \mu\text{m}$ and different channel lengths L	38
3.9	Relative error of the scalable model for devices with $W = 50 \mu\text{m}$ and different channel lengths L	38
4.1	Generic small-signal model for a three-terminal device, illustrating the configuration of gate, source, and drain terminals, as well as the principal small-signal parameters.	40
4.2	Simplified small-signal equivalent circuit for a three-terminal device, highlighting only the essential elements and parameters relevant to basic linear analysis.	41
4.3	TFT Small Signal Model	42
4.4	C-V characteristics illustrating the graphical extraction of C_{Low} , C_{High} , and C_{CH}	43
4.5	Comparison of measured data and modeled results for g_m with $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$	44
4.6	Comparison of measured data and modeled results for g_m with $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$	45
4.7	Comparison of measured data and modeled results for g_m with $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$	45
4.8	Comparison of measured data and modeled results for g_m with $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$	45
4.9	Comparison of measured data and modeled results for g_m with $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$	46
4.10	Comparison of measured data and modeled results for g_m with $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$	46
4.11	Relative error of g_m with $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$	47
4.12	Relative error of g_m with $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$	47
4.13	Relative error of g_m with $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$	48
4.14	Relative error of g_m with $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$	48
4.15	Relative error of g_m with $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$	49
4.16	Relative error of g_m with $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$	49
4.17	Verilog-A transfer characteristic (I_D vs V_{GS}) for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.	51
4.18	Experimental transfer characteristics for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.	51

A.1	Experimental transfer characteristics for devices with $L = 0.6 \mu\text{m}$ and widths $W = 80$ and $160 \mu\text{m}$	60
A.2	Experimental transfer characteristics for devices with $L = 0.6$ and $0.8 \mu\text{m}$. Top row: $W = 240 \mu\text{m}$ ($L = 0.6$) and $W = 50 \mu\text{m}$ ($L = 0.8$). Bottom row: $W = 100 \mu\text{m}$ ($L = 0.8$).	61
A.3	Experimental transfer characteristics for $W = 80 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ with V_{on} marked in both linear and saturation regions.	61
A.4	Experimental transfer characteristics with V_{on} marked for $W = 160 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ in both linear and saturation regions.	62
A.5	Experimental transfer characteristics with V_{on} marked for $W = 240 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ in both linear and saturation regions.	62
A.6	Experimental transfer characteristics with V_{on} marked for $W = 50 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ in both linear and saturation regions.	62
A.7	Experimental transfer characteristics with V_{on} marked for $W = 100 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ in both linear and saturation regions.	63
B.1	Experimental transfer characteristics for $W = 320 \mu\text{m}$ and $L = 5 \mu\text{m}$ in both linear and saturation regions.	64
B.2	Experimental transfer characteristics for $W = 320 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.	64
B.3	Experimental transfer characteristics for $W = 320 \mu\text{m}$ and $L = 20 \mu\text{m}$ in both linear and saturation regions.	65
B.4	Experimental transfer characteristics for $W = 320 \mu\text{m}$ and $L = 40 \mu\text{m}$ in both linear and saturation regions.	65
B.5	Experimental transfer characteristics for $W = 160 \mu\text{m}$ and $L = 5 \mu\text{m}$ in both linear and saturation regions.	65
B.6	Experimental transfer characteristics for $W = 160 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.	66
B.7	Experimental transfer characteristics for $W = 160 \mu\text{m}$ and $L = 20 \mu\text{m}$ in both linear and saturation regions.	66
B.8	Experimental transfer characteristics for $W = 160 \mu\text{m}$ and $L = 40 \mu\text{m}$ in both linear and saturation regions.	66
B.9	Experimental transfer characteristics for $W = 80 \mu\text{m}$ and $L = 5 \mu\text{m}$ in both linear and saturation regions.	67
B.10	Experimental transfer characteristics for $W = 80 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.	67
B.11	Experimental transfer characteristics for $W = 80 \mu\text{m}$ and $L = 20 \mu\text{m}$ in both linear and saturation regions.	67
B.12	Experimental transfer characteristics for $W = 80 \mu\text{m}$ and $L = 40 \mu\text{m}$ in both linear and saturation regions.	68

B.13	Experimental transfer characteristics for $W = 40 \mu\text{m}$ and $L = 5 \mu\text{m}$ in both linear and saturation regions.	68
B.14	Experimental transfer characteristics for $W = 40 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.	68
B.15	Experimental transfer characteristics for $W = 40 \mu\text{m}$ and $L = 20 \mu\text{m}$ in both linear and saturation regions.	69
B.16	Experimental transfer characteristics for $W = 40 \mu\text{m}$ and $L = 40 \mu\text{m}$ in both linear and saturation regions.	69
C.1	Experimental transfer characteristics for devices with $W = 100 \mu\text{m}$	70
C.2	Experimental transfer characteristics for short-channel $W = 100 \mu\text{m}$ and wide $W = 50 \mu\text{m}$ devices.	70
C.3	Experimental transfer characteristics for devices with $W = 50 \mu\text{m}$	71
D.1	Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$	72
D.2	Relative error of the model for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$	72
D.3	Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$	73
D.4	Relative error of the model for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$	73
D.5	Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$	73
D.6	Relative error of the model for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$	74
D.7	Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$	74
D.8	Relative error of the model for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$	74
D.9	Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$	75
D.10	Relative error of the model for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$	75
D.11	Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$	75
D.12	Relative error of the model for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$	76
D.13	Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$	76
D.14	Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$	76
D.15	Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$	77
D.16	Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$	77

D.17 Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$	77
D.18 Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$	78
E.1 Extracted scalable coefficients for V_{on} in both linear and saturation regimes.	79
E.2 Polynomial coefficients a , b , and c for V_{on}	80
E.3 Extracted scalable coefficients for α in both linear and saturation regimes. .	80
E.4 Polynomial coefficients a , b , and c for α	81
E.5 Extracted scalable coefficients for κ in both linear and saturation regimes. .	81
E.6 Polynomial coefficients a , b , and c for κ	82
E.7 Extracted scalable coefficients for G_0 in both linear and saturation regimes. .	82
E.8 Polynomial coefficients a , b , and c for G_0	83
E.9 Extracted scalable coefficients for I_{off} in both linear and saturation regimes.	83
E.10 Polynomial coefficients a , b , and c for I_{off}	84
E.11 Extracted linear approximations for ΔL and R_{SD} as functions of channel width W	84

LISTINGS

F.1	Modelo Verilog-A IGZO TFT	85
-----	-------------------------------------	----

ACRONYMS

a-IGZO	Amorphous Indium Gallium-Zinc Oxide
a:Si	Amorphous silicon
C-V	Capacitance-Voltage
CAD	Computer-Aided Design
CAMCAS	Cambridge Compact Analytical Semiconductor
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
DIBL	Drain-Induced Barrier Lowering
EKV	Enz-Krummenacher-Vittoz
FETs	Field Effect Transistors
I-V	Current-Voltage
IC	Integrated Circuits
IGZO	Indium Gallium-Zinc Oxide
IZTO	Indium Zinc Tin Oxide
LC	Low Current
LV	Low Voltage
MOSFETs	Metal Oxide Field Effect Transistors
MTR	Multiple Trapping and Release
NQS	Non-quasi-static
PDKs	Process Design Kits

RFID	Radio Frequency Identification
RPI	Rensselaer Polytechnic Institute
TFTs	Thin-film Transistors
TOS	Transparent Oxide Semiconductor
UMEM	Universal Method and Extraction Procedure
ZTO	Zinc Tin Oxide

SYMBOLS

C_{CH}	Channel Capacitance
C_{OV}	Overlap Capacitance
ΔL	Channel Length Variation
ε_{ox}	Absolute Permittivity of the Gate Insulator
g_m	Transconductance
I_{off}	Off Current
L	Channel Length
L'	Effective Channel Length
L_{CH}	Channel Length
L_{OV}	Overlap Length
R_c	Contact Resistance
R_D	Drain Resistance
R_{DS}	Drain-Source Resistance
r_o	Output Resistance
R_S	Source Resistance
R_{tot}	Total Resistance
t_{ox}	Gate Insulator Thickness
V_H	Largest value of gate-to-source voltage measured
V_{on}	On Voltage
V_t	Threshold Voltage

W Channel Width

INTRODUCTION

1.1 Motivation

The rapid evolution of nanotechnology has given rise to the development of emergent nano-devices that enable the implementation of new circuits capable of supporting the ever-growing panoply of applications supporting our everyday life.

Besides the need for having circuits capable of operating at higher frequencies and with lower power consumption, new applications have emerged (e.g., flexible display technologies, implantable electronics for improved medical imaging and diagnostics), raising a great interest for flexible and/or transparent devices [2].

Thin-film transistors (TFTs) and metal-semiconductor-insulator field-effect transistors (FETs) represent a ground-breaking technological advancement in the domain of flexible and wearable electronics [3], [4].

The advancement of technology, in conjunction with the emergence of next-generation materials such as IGZO, has led to a significant enhancement in the capabilities of TFTs. Indium-gallium-zinc oxide (IGZO) appears to be one of the most competitive alternative for the current trend of silicon (Si) based FETs applications, offering advantages like low-temperature production, high mobility, transparency, excellent uniformity and cost-effectiveness [5].

The absence of an open-source platform dedicated to IGZO TFT technology has slowed circuit design development relative to its CMOS counterparts. Moreover, the lack of robust modelling approaches hinders the integration of IGZO-TFTs into circuit design, thereby slowing technological progress. TFT circuits, when fabricated on flexible substrates, are particularly vulnerable to tensile forces, leading to variations in channel current. Such effects must be incorporated into models to ensure accurate circuit performance [6].

Consequently, the development of adaptable compact models is imperative for intermediate device physics in circuit design, ensuring strict alignment with the requirements of Computer-Aided Design (CAD) tools [7], [6].

1.2 The History of TFTs

TFTs are of significant importance in the field of electronics, particularly in the context of display manufacturing [8]. These devices find application in a variety of electronic products, including televisions, computer monitors and tablets [9]. The history of TFTs begins in 1930 when O. Heil [10] and J.E. Lilienfeld [11–13], patented a device that utilised a semiconductor in a configuration similar to modern transistors. Although it was not a TFT in the contemporary sense, this patent represented an important milestone in the future development of electronics.

In the 1960s, P.K. Weimer produced the first polycrystalline cadmium sulfide (CdS) TFT at RCA Labs [14], leading him to publish [15]. In the same decade, Boesen and Jacobs [16] provided an account of a TFT with a single-crystal ZnO semiconductor doped with lithium.

It was only in 1970 that Aoki and Sasakura reported their initial findings on a functioning TFT fabricated from hydrogenated amorphous silicon (a-Si:H), although its electrical performance was poor [17], [18]. In the late 1970s, there was a marked enhancement in the electrical performance of TFTs, attributable to the contributions of P. LeComber and W. Spear [19].

In the subsequent years, advancements in silicon-based semiconductor technology, particularly the development of polycrystalline silicon, led to improved transistor performance. However, this breakthrough was retarded by issues with uniformity, making it difficult to apply to large-scale display technology. As a result, researchers turned their attention to organic semiconductors, which could be fabricated at lower temperatures [20], [21]. Nevertheless, the attentions turned to oxide materials, which presents a low production cost and production temperatures, showing outstanding mobility values compared to the materials discussed before.

Hosono et al. were the first to report an IGZO TFT fabricated at room temperature, exploring the advantages of amorphous transparent conduction [22], [23]. The TFT developed by Hosono et al. was the first to demonstrate exceptional effectiveness in practical applications, incorporating on a transparent oxide semiconductor (TOS).

In recent years, both amorphous and crystalline metal oxide TFTs, especially those based on zinc oxide (ZnO) semiconductors, have gained significant interest. The materials under discussion have been demonstrated to be of great importance in industrial contexts, such as electronics and optical systems, owing to two of their distinctive features. Firstly, their high band gap. Secondly, their excellent optical transparency. Extensive research has been conducted on metal oxide semiconductors like IGZO, zinc tin oxide (ZTO), and indium-zinc tin oxide (IZTO) [24].

In particular, IGZO TFTs have recently been highlighted as very promising devices for transparent flexible applications [25–29]. Several applications of IGZO TFTs have been explored in the literature, including their use in logic gates [30], RFID tag logic circuits, ring oscillators [31] and in the implementation of MicroLEDs backplanes [32].

It is to be noted that although significant efforts are being dedicated to the techniques for implementing these devices, their integration into circuits relies on the availability of reliable compact models, which enable electrical simulation and optimization of the circuits to be designed.

Figure 1.1 shows a diagram indicating some landmarks recorded in the timeline of TFT development.

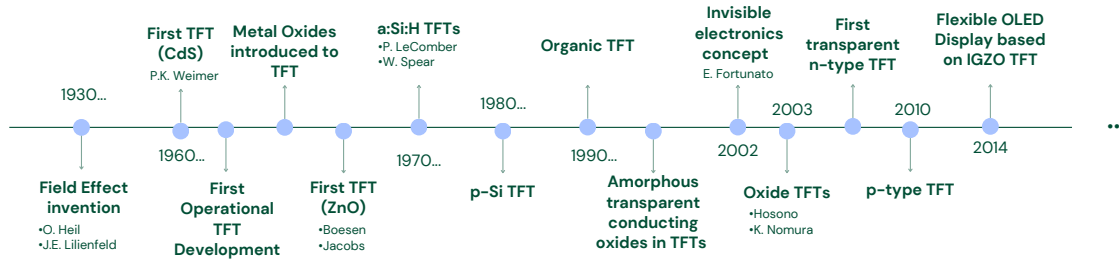


Figure 1.1: Timeline of TFT development

1.3 Objectives

The primary objective of this dissertation is to develop and validate a compact model for indium-gallium-zinc oxide thin-film transistors (IGZO TFTs), alongside an automatic parameter extraction methodology. This model aims to accurately represent the electrical behavior of IGZO TFTs under both linear and saturation regimes, making it suitable for integration into circuit simulation environments used in advanced electronics applications.

To support this objective, a comparative study of existing compact models for IGZO-based TFTs will be conducted, highlighting their advantages and limitations. The proposed modeling approach will rely on a set of experimental data obtained from IGZO TFTs that were electrically characterized at CENIMAT.

A key goal of this work is to bridge the gap between the physical understanding of device operation and the practical needs of circuit design. By establishing a robust and scalable compact modeling framework, this research seeks to enable the accurate prediction of device performance across various geometries and operating conditions.

The model will be designed with scalability in mind, allowing it to account for changes in channel dimensions without compromising accuracy. This feature is essential for supporting the design of circuits.

Additionally, small-signal modeling capabilities will be incorporated to facilitate AC circuit analysis.

Finally, the validity of the developed model will be demonstrated through electrical simulations, supported by its implementation in Verilog-A.

1.4 Main Contributions

The primary contribution of this dissertation is the development of a fully automatic modeling and parameter extraction strategy for Indium Gallium Zinc Oxide (IGZO) thin-film transistors (TFTs). This approach effectively characterizes device behavior in both linear and saturation regions of operation, covering both above-threshold and sub-threshold characteristics.

A key aspect of this work is the implementation of a semi-physical analytical description of the current-voltage characteristics, captured through a single unified expression applicable to all operational regions. The proposed methodology was rigorously validated against experimental data, achieving a relative error below 10% for $V_{GS} \geq 1V$ in both saturation and linear regimes.

The scientific validity and relevance of these contributions have been disseminated through the following peer-reviewed publication:

Paper: C. Almeida, P. Barquinha, and M. H. Fino, “Fully Automatic Modeling and Parameter Extraction of IGZO TFTs”, in *2025 9th International Young Engineers Forum on Electrical and Computer Engineering (YEF-ECE)*, Caparica / Lisbon, Portugal, 2025, pp. 169-174, doi: 10.1109/YEF-ECE66503.2025.11117522 [33].

BACKGROUND AND LITERATURE REVIEW

2.1 Device Compact Modelling

Compact modelling of integrated semiconductor devices constitutes a pivotal phase within the overall design cycle of contemporary integrated circuit (IC) products. The demand on accurate and efficient compact models is driven by increasing circuit operating frequencies, shrinking device tolerances, and the rising complexity of mixed-signal components. Therefore, these models should accurately replicate the electrical behaviour of device terminals while remaining computationally efficient, ensuring ease of parameter extraction and simplicity for simulation purposes.

Compact modelling began with metal-oxide-semiconductor field-effect transistors (MOSFETs), which served as the foundation for semiconductor device modelling. With the advance of technology and the emergence of new applications, there was a need to extend these modelling approaches to TFTs. While MOSFETs and TFTs share some operational principles, TFTs present unique characteristics that require specific modelling considerations, such as different material properties, fabrication processes, and operating mechanisms.

Over the last three decades, significant advances have been observed in TFT modelling for different types of technologies, such as amorphous silicon, polysilicon, organics and metal oxides. Highlighting the development of the RPI model at Rensselaer Polytechnic Institute, which has become a standard for modelling amorphous silicon (a-Si) TFTs and is widely accepted across numerous simulation platforms [34].

The development of transistor models typically combined physical and empirical approaches, with the aim to obtain a balance between accuracy and low complexity, by considering the behaviour of transistors across all operational regions. While the priority often lies in achieving high accuracy, the resulting models may not be fully physical, since it is not possible to fit these type of models with reasonable accuracy. However, understanding of underlying physics behind the device is crucial to avoid the excess of fitting parameters. Hence, the simulators commonly use a combination of the two approaches [35].

Design engineers rely on CAD software that incorporates these mathematical models to estimate and enhance circuit performance ahead of manufacturing.

The next sections will present the fundamental compact models developed for MOSFETs, which provide the theoretical foundation, followed by an exploration of how these models have been adapted and enhanced for TFT modelling to account for their unique characteristics.

2.2 MOSFET Compact Modelling

2.2.1 Shockley Model

Shockley Model, also known as the quadratic model, is the foundational and most well-known model for describing transistor behaviour in electronics circuits. This model was originally developed and proposed by William Shockley in the 1950s [36], and remains a cornerstone of transistor theory. The equations 2.1 are responsible for the mathematical description of the model across various operating regions (cutoff, linear, and saturation, respectively). One of the model's most distinctive characteristics, which is reflected in its name, is the quadratic relationship established between the drain current (I_D) and the gate to source voltage (V_{GS}), demonstrating that the current varies with the square of the applied voltage.

$$I_D = \begin{cases} 0 & \Leftarrow V_{GS} < V_{Th} \\ \mu C_{ox} \frac{W}{L} \times ((V_{GS} - V_{Th})V_{DS} - 0.5(V_{DS})^2)(1 + \lambda V_{DS}) & \Leftarrow V_{GS} \geq V_{Th} \wedge V_{DS} < (V_{GS} - V_{Th}) \\ 0.5\mu C_{ox} \frac{W}{L} \times (V_{GS} - V_{Th})^2(1 + \lambda V_{DS}) & \Leftarrow V_{GS} \geq V_{Th} \wedge V_{DS} \geq (V_{GS} - V_{Th}) \end{cases} \quad (2.1)$$

In 2.1, W represents the channel width, L the channel length, μ the channel mobility, C_{ox} gate dielectric capacitance per unit area and λ channel length modulation parameter [36].

This model has been widely used in circuit design with MOSFETs, as it is analytically simple and consequently easy to use in the calculations that support the design of elementary circuits (e.g., multi-stage amplifier).

Although this model continues to be widely used in introductory electronics courses, it presents very inaccurate results when applied to devices in micrometric technologies.

This limitation has led to the emergence of models with increased degrees of complexity, which will be described below.

2.2.2 Nth Power Law MOSFET Model

Over the years, the shrinking of transistor size has been a significant trend in the semiconductor industry, giving rise to Moore's famous Law [37], which predicts the doubling of the number of transistors in an IC approximately every two years.

However, this miniaturization has had profound implications for circuit design, mainly when working with smaller technology nodes, known in the industry as deep sub-micron technologies, since their transfer characteristics have shown a progressive deviation from the traditional quadratic function that characterized earlier transistor models. Instead, it becomes closer to a linear function, where the overdrive voltage (i.e., $V_{GS} - V_T$) is raised to a power approaching unity. This shift in transistor behaviour highlighted the limitations of existing models and created an urgent need for a new, more straightforward modelling approach that could more accurately approximate the actual behaviour of these devices. T. Sakurai and A. R. Newton introduced the Alpha-Power Law model, which aims to be applied to digital circuits. In [38], its application to the characterization of the behaviour of a CMOS Inverter is presented. Nevertheless, this model has limitations in the modelling of transistors in the triode region.

To overcome this limitation, a new model was proposed in 1991, the Nth Power Law, given by 2.2 to 2.5.

$$V_{Th} = V_{T0} \quad (2.2)$$

$$I_{Dsat} = \frac{W}{L_{eff}} B \times (V_{GS} - V_{Th})^n \quad (2.3)$$

$$I_D = \begin{cases} I_{Dsat} \left(2 - \frac{V_{DS}}{V_{DSat}}\right) \times \left(\frac{V_{DS}}{V_{DSat}}\right) & \Leftarrow V_{GS} \geq V_{Th} \wedge V_{DS} < V_{DSat} \\ I_{Dsat} (1 + \lambda V_{DS}) & \Leftarrow V_{GS} \geq V_{Th} \wedge V_{DS} \geq V_{DSat} \end{cases} \quad (2.4)$$

$$V_{DSAT} = K \times (V_{GS} - V_{Th})^m, \quad (2.5)$$

where V_{T0} is a parameter that describe the threshold voltage, L_{eff} are the effective channel length. The parameters B and n determine the threshold voltage saturation regime characteristic, while the parameters K and m controls the linear region characteristic.

This model was also successfully used in ring Voltage Controlled Oscillators (VCOs) in a 130 μm technology [39].

The need to characterize the operation of transistors in the sub-threshold region ($V_{GS} < V_T$) led to the emergence of the *Nexp* model.

2.2.3 *Nexp* Model

Nth Model, despite being one of the proposed models that most closely approximated transistor behaviour, showing high accuracy in the transistor's triode region, it still did not consider the sub-threshold region of operation. To solve this issue, M.H. Fino developed the *Nexp* model [40], building upon T. Sakurai and A.R. Newton's previous work [39]. This new model is specially designed for submicron devices in analog circuit design, producing highly accurate results when applied to MOSFETs either in strong, moderate or weak inversion operation regions.

The *Nexp* model's approach utilises exponential functions to characterize the fundamental relationship between drain current and gate-source voltage. This approach enables to smooth transitions between different MOSFET operating regions, while simultaneously achieving superior computational efficiency. The model's mathematical equations 2.6 and 2.7, leads to significantly improved simulation convergence characteristics, all while maintaining the high degree of accuracy that modern circuit design demands.

$$I_{DSAT} = \begin{cases} I_0 e^{\frac{V_{GS}-V_t}{N_s}}, & V_{GS} < V_{Th} \\ I_0 e^{m(\frac{V_{GS}-V_t}{\alpha N_s})^m}, & V_{GS} \geq V_{Th} \end{cases} \quad (2.6)$$

$$I_D = \begin{cases} I_{DSAT} (1 + \lambda V_{DS}), & V_{DS} \geq V_{DSAT} \\ I_{DSAT} \left(2 - \frac{V_{DS}}{V_{DSAT}}\right) \frac{V_{DS}}{V_{DSAT}}, & V_{DS} < V_{DSAT} \end{cases} \quad (2.7)$$

It should be noted that this model ensures continuity in the smooth transitions between the MOSFET operating regions (weak, moderate, and strong inversion), providing accuracy in the calculations of small-signal parameters, such as g_m and g_{ds} , which is essential for the characterization of circuit operation in incremental mode. In fact, this model was used in the analysis of a single-stage differential amplifier with an active NMOS load, using SMIC018 technology [40], as well as in calculation of delays for CMOS inverter gates with dimensions of $\frac{W}{L} = \frac{10\mu m}{1.2\mu m}$ and $\frac{W}{L} = \frac{5\mu m}{1\mu m}$ [41]. This model, however shows limitations regarding its scalability for different sizes of transistors when deep submicron technologies are to be considered.

For the characterization of circuits using deep submicrometric technologies, the EKV model, was proposed.

2.2.4 EKV Model

The initial EKV (Enz-Krummenacher-Vittoz) model was the earliest to propose a symmetric, bulk-referred approach to handling of the MOS transistor across all levels of inversion [42].

Recently, a physics-based charge modelling approach led to the development of EKV 2.6. In their work [43], the authors highlight the suitability of the EKV 2.6 model, in its simplest formulation, for the design and simulation of analog, high-speed digital, and mixed-mode IC and systems, particularly under low-voltage (LV) and low-current (LC) conditions. This model provides a continuous formulation of both large-signal and small-signal variables across all operating regions [42].

This approach offers high accuracy and analytical simplicity, as it relies on a smaller number of parameters compared to other models [44].

This model refers all terminal voltages to the local substrate. In this way, the intrinsic symmetry of the device is preserved [42].

EKV defines the drain current as the combination of a forward current controlled by the source, represented by I_F , and a reverse current controlled by the drain, represented by I_R . The I_D is expressed as $I_D = I_F - I_R$, where

$$I_{F(R)} = I_S \ln^2 \left(1 + e^{\frac{V_G - V_{TO} - nV_{S(D)}}{2nU_T}} \right) \quad (2.8)$$

V_{TO} is the gate-to-bulk threshold voltage defined with zero channel inversion charge, I_S is the specific current, U_T is the thermal voltage and n is the slope factor.

G. Machado, C. Enz, and M. Bucher implemented this model in PCM transistors using technologies of $0.8 \mu m$ BiCMOS, $2 \mu m$, $1.5 \mu m$ and $0.7 \mu m$ CMOS [43].

The EKV 2.6 model has evolved into a new version, EKV 3.0. The model being discussed is based on the surface potential method, paired with linearization of inversion charge in relation to surface potential, creating a reliable analytical framework for compact modelling. This ideal model is further extended to incorporate high-field phenomena in advanced deep submicron CMOS technologies. It preserves scalability across both channel length and width, requiring only a minimal set of parameters.

Enhancements in this model improve short-channel effects, including drain-induced barrier lowering (DIBL), charge modelling, and transcapacitances. It also incorporates non-quasi-static (NQS) effects and thermal noise, all of which are expressed within the same ideal model framework. Extensions for polydepletion and quantum effects serve as natural generalizations of this approach. Additionally, the local charge model is used to develop effective-field-dependent mobility expressions [45].

The EKV 3.0 model applies to a broad spectrum of CMOS technologies. More details on this model, including its parameters and equations, can be found in [46].

J. Bremer, T. Peikert, and W. Mathis applied the EKV 3.0 model to develop an analytical modelling approach for the C-V characteristics of inversion-mode MOS varactors and their application in RF VCO design, proving that the EKV-based modelling approach, produced simulation results closely matching those from Spectre across all transistor operation regions for both NMOS and PMOS varactors [47].

2.3 TFT Compact Modelling

The operational principles of both amorphous and polysilicon TFTs are comparable to those of MOSFETs, particularly in how the gate voltage regulates the current between the drain and source contacts. Despite this resemblance, the main difference between MOSFET and TFT is the absence of a substrate contact in TFTs, as well as the conduction mechanisms supporting their behaviour.

2.3.1 RPI Model

The threshold voltage in TFTs is usually extrapolated from current-voltage (I-V) curves at low bias.

For a:Si TFTs, the Fermi level gradually moves closer to the conduction region once the threshold is surpassed. This behaviour can be attributed to the relatively low characteristic temperature of the localized states, which is similar to the thermal temperature of the system.

Amorphous silicon also exhibits a bias stress effect, where the density of states can be altered by annealing the transistor while applying a gate bias. This change may result in the degradation of the sub-threshold slope, leading to affect the on-to-off current ratio of the device.

The Rensselaer Polytechnic Institute (RPI) model, as mentioned before, has gained recognition and has been widely used, for its ability to accurately capture TFTs essential properties. M. Shur et al. [48] has present the equations (2.9) for these model for amorphous TFTs.

$$I_D = \begin{cases} \mu_{FET} C_i \frac{W}{L} \times (V_{GS} - V_{Th}) V_{dse}, & V_{GS} \geq V_{Th} \\ q \mu_n n_{so} \left[\left(\frac{t_m}{d_i} \right) \left(\frac{V_{GS} - V_{fb}}{V_0} \right) \left(\frac{\epsilon_i}{\epsilon_s} \right)^{\left(\frac{1}{V_{Th}(2V_0 - V_{Th})} \right)} \right] \frac{W}{L} V_{dse}, & V_{GS} < V_{Th} \end{cases} \quad (2.9)$$

The dielectric thickness is represented by d_i while, ϵ_i and ϵ_s are the permittivities of the insulator and a-Si:H, respectively. The charge channel thickness and the dark sheet carrier density are represented by t_m and n_{so} , respectively, and are constants that depend on the material parameters. q is the elemental charge, μ_n is the total electron mobility, μ_{FET} is an effective mobility, and C_i is the gate insulator capacitance. $V_0 = \frac{E_{DD}}{q}$, where E_{DD} is the characteristic energy of the deep donor traps, V_{th} is the thermal voltage and V_{fb} is the flat band voltage.

Figure 2.1 shows the experimentally measured data, as well as the data resulting from applying the RPI model to an a-Si:H TFT with $W/L = 150/60\mu m$, on a logarithmic scale.

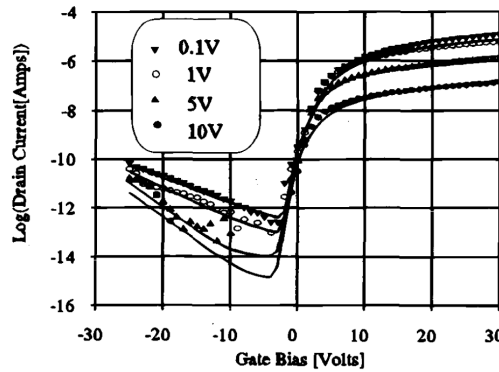


Figure 2.1: Transfer characteristic for different values of V_{gs} - Comparison for measured and modeled (using RPI model) for an a-Si:H TFT. Adapted from [48]

The improved RPI model for a-IGZO TFTs [49] was developed based on the standard RPI-aTFT explained before, adding new parameters and equations. The model combines

physics-based and empirical parameters to create a unified, continuous description of charge sheet density, leading to more precise current and signal parameter expressions. This improvement on the design of the model fits better for a-IGZO TFT devices than the majority of the models, offering higher accuracy and faster convergence.

A fundamental innovation in this refined model is its ability to address the channel-length dependency of the threshold voltage, a limitation that existed in the standard RPI-aTFT model, by combining binning techniques with new equations (2.10) integrated into the standard model [49].

$$V_{th(L)} = \begin{cases} P_{vr} \times \left[0.35 \times \left(1 + \frac{L_{Ref}}{L} \right) \right]^{\left(\frac{L_{Ref}}{L} \right)}, & L \leq L_{Ref} \\ P_{vr} \times 0.55, & L \geq L_{Ref} \end{cases} \quad (2.10)$$

P_{vr} is a parameter for use in statistical simulations of threshold voltage variations due to process variations and L_{Ref} the channel length reference [49].

Figure 2.2 represents the measured and simulated V_{th} data of the a-IGZO TFT devices with channel length variation (from $5\mu m$ to $50\mu m$), it is possible to note the influence of the process variations parameters P_{Vr} . Figure 2.3 shows the I_D (measured and fitted) vs the variation of the channel length L , for a constant value of W ($50\mu m$), V_{DS} (2 V) and V_{GS} (5 V), showing that the I_D is more precisely predicted in the triode and saturation region.

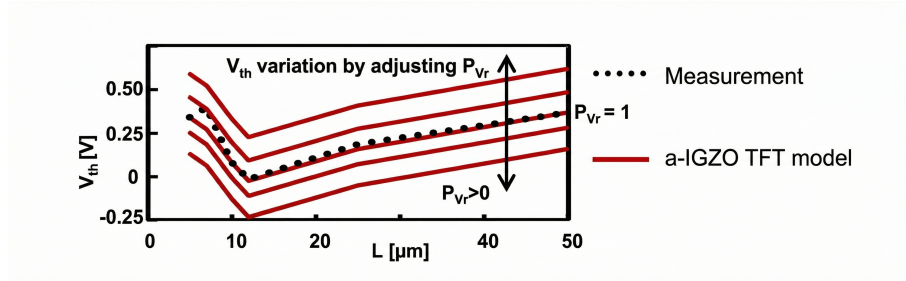


Figure 2.2: Measured and simulated $V_{th(L)}$ and the influence of the variation of the parameter P_{Vr} . Adapted from [49]

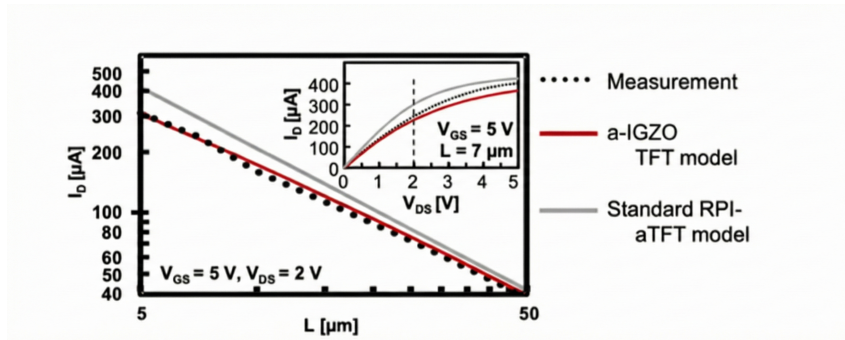


Figure 2.3: Measured and modeled data as function of channel length L for $V_{DS}=2$ V and $V_{GS}=5$ V with a constant channel width W . Adapted from [49]

Figures 2.4a and 2.4b show the measured and modeled characteristics of the a-IGZO TFT, for a device with $W = 50\mu m$ and $L = 5\mu m$. The new RPI model give a demonstration of high accuracy in the transition region from linear to saturation (the knee), which is crucial for analog circuit design [49].

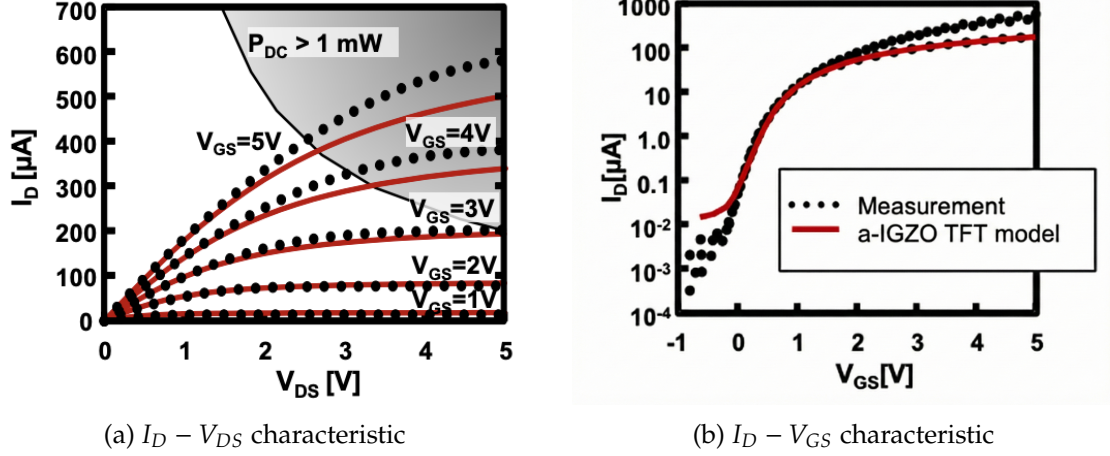


Figure 2.4: Measured and simulated characteristics of the a-IGZO TFT with fixed dimensions. Adapted from [49]

Table 2.1: Key model parameters. Adapted from [49]

Parameter	Description	Remarks	Unit
L	Length	Device dimension	μm
W	Width	Device dimension	μm
α_{Sat}	V_{DS} , sat parameter	Fitted	—
δ	Transition parameter	Fitted	—
γ	Power law mobility	Fitted	—
G_{Min}	Min. density of deep states	Fitted	—
M	Knee shape parameter	Fitted	—
μ_{Band}	Conduction band mobility	Fitted	m^2/Vs
I_{ol}	Zero bias leakage	Fitted	A
σ	Min. leakage current	Fitted	A
V_0	Characteristic voltage for deep states	Fitted	V
V_{fb}	Flat band voltage	Fitted	V
E_l	Act energy of hole leakage	Process given	—
E_μ	Field effect mobility act energy	Process given	—
ϵ	Rel. dielectric const. of substrate	Process given	—
ϵ_l	Rel. dielectric const. gate insulator	Process given	—
T_{ox}	Thin-oxide thickness	Process given	m

Table 2.1 lists the main parameters of the RPI-aTFT model. It should be noted that since this new model was obtained by combining binning techniques with the standard model, the values obtained for each parameter may vary depending on the size of the device, i.e., whether it is a short model or a long model.

In [49] this model was used in the characterization of a flexible Cherry-Hooper amplifier circuit designed on a 50 μm thick polyimide substrate (13.3 mm^2 area) utilising the IGZO TFT technology, as described in [50].

2.3.2 Surface-Potential-Based Compact Model

In order to obtain the parameters that characterize the simple TFT model, a model was developed, presented in 2018 by N. Lu, W. Jiang, Q. Wu, D. Geng, L. Li and M. Liu [34], which allows analyzing and extracting these parameters based on the drain current (I_{DS}) behaviour when the device is conducting. The transport properties in TFTs vary with different materials, however, the current-voltage behaviour can, to a first approximation, be described using the same formalism (equation 2.11). The following system describes the current expression in the active and saturation regions.

$$I_D = \begin{cases} \frac{WC_i}{L_{eff}} \times \mu_{eff} (V_{GS} - V_T - \frac{V_{DS}}{2\alpha}) V_{DS} (1 + \lambda V_{DS}), & V_{DS} \leq V_{DSAT} \\ \frac{WC_i}{2L_{eff}} \times \mu_{eff} \alpha (V_{GS} - V_T)^2 (1 + \lambda V_{DS}), & V_{DS} \geq V_{DSAT}, \end{cases} \quad (2.11)$$

where the the saturation voltage (V_{DSAT}) is represented by 2.12, α is a parameter that relates the saturation voltage to the gate overdrive, V_T is the threshold voltage, and α is the effect of channel modelling.

$$V_{DSAT} = \alpha \times (V_{GS} - V_T) \quad (2.12)$$

And 2.13 represents the effective mobility, where μ_0 is the low bias carrier mobility, V_{AA} is a empirical parameter and γ is a mobility enhanced factor.

$$\mu_{eff} = \mu_0 \times \frac{(V_{GS} - V_T)^\gamma}{V_{AA}^\gamma} \quad (2.13)$$

Note that the previous equation (2.11) takes into account the channel length modulation effect, with α being a fitting parameter. Considering 2.14 and 2.15, it is possible to obtain a more compact expression for the drain current at saturation, shown in 2.16.

$$K = \frac{W}{L_{eff}} \times \frac{\mu_0}{(V_{AA})^\gamma} C_i \alpha \quad (2.14)$$

$$m = 2 + \gamma \quad (2.15)$$

$$I_{DSAT} = K \times (V_{GS} - V_T)^m (1 + \lambda V_{DS}) \quad (2.16)$$

Combining 2.11, 2.13, 2.14 and 2.15, it is possible to obtain a more simplified expression for the drain current in the linear region, described in 2.17.

$$\begin{aligned}
 \frac{WC_i}{L_{eff}} \times \mu_{eff} \left(V_{GS} - V_T - \frac{V_{DS}}{2\alpha} \right) V_{DS} (1 + \lambda V_{DS}) &= \\
 = \frac{WC_i}{L_{eff}} \times \mu_0 \times \frac{(V_{GS} - V_T)^\gamma}{V_{AA}^\gamma} \left(V_{GS} - V_T - \frac{V_{DS}}{2\alpha} \right) V_{DS} (1 + \lambda V_{DS}) &= \quad (2.17) \\
 = K \times \frac{2}{\alpha} \times (V_{GS} - V_T)^{m-2} \times \left(V_{GS} - V_T - \frac{V_{DS}}{2\alpha} \right) V_{DS} (1 + \lambda V_{DS})
 \end{aligned}$$

Thus, the combination of 2.11 and 2.17 enables the formulation of a system of equations that characterizes I_D , minimizing the dependency on fitting parameters (equation 2.18).

$$I_D = \begin{cases} K \times \frac{2}{\alpha} \times (V_{GS} - V_T)^{m-2} \times \left(V_{GS} - V_T - \frac{V_{DS}}{2\alpha} \right) V_{DS} (1 + \lambda V_{DS}), & V_{DS} \leq V_{DSAT} \\ K \times (V_{GS} - V_T)^m (1 + \lambda V_{DS}), & V_{DS} \geq V_{DSAT} \end{cases} \quad (2.18)$$

Table 2.2 summarises the parameters required to use the proposed model.

Table 2.2: Model Parameters

Parameter	Remarks
L	Device dimension
W	Device dimension
V_T	Fitted
m	Fitted
K	Fitted
γ	Fitted
α	Fitted
λ	Fitted

In the case of IGZO, it generally operates in accumulation region, therefore, so it is not possible to define the threshold voltage. While the concept of threshold voltage varies with different materials, it remains a useful parameter for compact models, which is why TFTs made from different materials exhibit distinct behaviours.

On the other hand, compact models aim to accurately and physically describe the current-voltage characteristics of TFTs, thus, it is possible to combine MTR (multiple trapping and release) theory with surface potential to develop the compact model of IGZO TFTs [34].

N. Lu, W. Jiang, Q. Wu, D. Geng, L. Li and M. Liu, presented a current equation for IGZO TFT, using the gradual channel approximation presented in [34].

$$I_{ds} = -\mu_{eff} W Q_i \frac{dV}{dy} = -\mu_{eff} W Q_i \left(2\varphi_t \frac{C_i}{Q_i} + 1 \right) \frac{d\varphi}{dy} \quad (2.19)$$

By integrating 2.19 from $\varphi_s = \varphi_{ss}$ to $\varphi_s = \varphi_{sd}$, it is possible to obtain the static current of the a-IGZO TFTs expressed by 2.20.

$$I_{d0} = \mu_{\text{eff}} \frac{W}{L} \left[2\phi_t C_i (\phi_{sd} - \phi_{ss}) - \frac{1}{2} \left((V_g - V_{fb} - \phi_{sd})^2 - (V_g - V_{fb} - \phi_{ss})^2 \right) \right], \quad (2.20)$$

where Q_i is the sheet density of total induced charge in channel, ϕ_{ss} , ϕ_{sd} and ϕ_t are the surface potentials at the source and drain side and thermal voltage, respectively [34].

Figure 2.5 illustrates the transfer characteristics of IGZO transistor for different V_g values, as predicted by the proposed model.

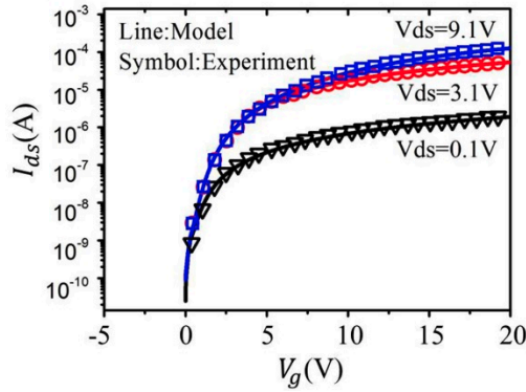


Figure 2.5: Comparison between the experimental and modeled data - Transfer characteristics of IGZO. Adapted from [34]

This model was utilised to deliver a physically consistent description of the device characteristics, facilitating accurate circuit-level performance predictions and supporting the design of RFID circuits for a-IGZO TFTs [inproceedingsSPB].

2.3.3 TFT Contact Resistances Model

In modern TFTs, due to channel miniaturization (reduction of L), the parasitic resistances of the drain and source are very important parameters. Research has shown that a source-and-gate resistance in series, along with the degradation of electron mobility, induces an effect similar to that observed in the transfer characteristic of a MOSFET [51]. Additionally, studies indicate that the presence of a series resistance leads to variations in the extracted V_T value [52]. Figure 2.6 shows the TFT structure of the model, illustrating both the intrinsic TFT and contact resistances. Based on this structure, it is possible to define the primed voltages V_{gs} and V_{ds} by the following equations [53]:

$$V_{gs} = V_{GS} - R_S I_D \quad (2.21)$$

$$V_{ds} = V_{DS} - (R_S + R_D) I_D \quad (2.22)$$

Considering the I_{Dsat} proposed in [51] and replacing V_{gs} with 2.21, a new I_{Dsat} Equation is obtained as:

$$I_{Dsat} = K(V_{GS} - R_S I_{Dsat} - V_t)^m \quad (2.23)$$

Equation 2.23 presents a recursive function dependent on I_{Dsat} . However, it can be rearranged to solve in order to V_{GS} , as shown below.

$$V_{GS} = R_S I_{Dsat} + V_t + \left(\frac{I_{Dsat}}{K} \right)^{\frac{1}{m}} \quad (2.24)$$

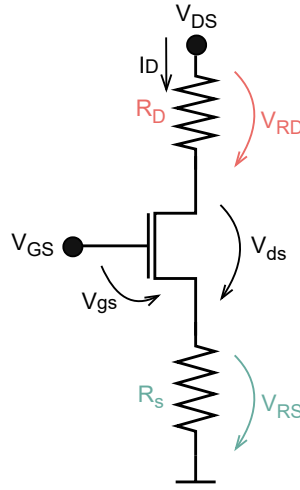


Figure 2.6: TFT structure with contact resistance. Adapted from [51]

For the evaluation of the series source contact resistance is used an auxiliar H function based on the Universal Method and Extraction Procedure (UMEM) which consists on the integration of the I_{Dsat} function [54].

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{Dsat} dV_{GS}}{I_{Dsat}}. \quad (2.25)$$

Substituting 2.24 into 2.25, results in

$$H = \frac{R_S I_D (m-1)}{2(m+1)} + \frac{V_{GS} - V_t}{m+1}, \quad (2.26)$$

Adelmo Ortiz-Conde et al. (2019) proposed a method for parameter extraction [51]. First, the parameters are numerically calculated using the H function, derived from the experimental data and 2.25. Next, the derivatives of H and I_{Dsat} with respect to V_{GS} are

numerically evaluated. Subsequently, the values of m and R_s are obtained through fitting. 2.26 is then fitted to the H function, and finally, the value of K is calculated with 2.21 and 2.23. Although this method appears effective for parameter extraction, it was concluded that it fails when applied to IGZO. Another parameter extraction method was proposed in [55] using Python, utilising two different TFT with dimensions of $\frac{W}{L} = \frac{50\mu m}{5\mu m}$ and $\frac{W}{L} = \frac{50\mu m}{10\mu m}$. However, no conclusions were presented regarding its application to IGZO TFTs.

2.3.4 CAMCAS Model

The CAMCAS (Cambridge Compact Analytical Semiconductor) model is a unified analytical approach developed for TFTs, with a particular focus on oxide semiconductors. This model aims to describe both operational regions (sub-threshold and above-threshold) through a single unified expression, where the reference voltage is defined as V_{on} rather than the traditional V_T [35],[56].

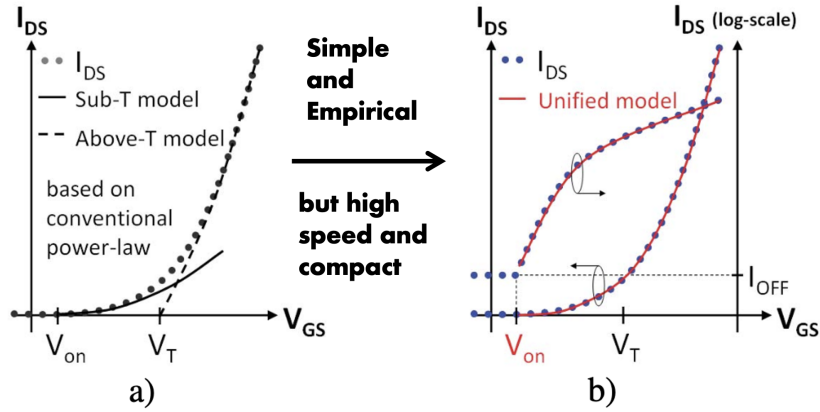


Figure 2.7: Transfer characteristic- a) with the conventional power-law models model for sub- and above-threshold; b) with unified model which can represent both regimes at the same time. Adapted from [35]

In Figure 2.7, the graphic a) illustrates the need for two models to represent the two different operational regimes. Here, V_{on} and V_T denote the on-voltage and threshold voltage, respectively. In contrast, for graph (b), only one model is required: a unified model capable of representing both the linear and saturation regimes simultaneously. To achieve this, a unified analytical approach developed specifically for amorphous oxide semiconductor TFTs and based on the methodology presented in [56] is adopted. This model is designed to describe both the sub-threshold and above-threshold operating regions through a single expression, as shown in Equation 2.27.

$$I_{DS} = G_0 \left(\frac{W}{L'} \right) \exp(\kappa(V_{GS} - V_{on})^\alpha) V'_{DS} + I_{off} \quad (2.27)$$

The parameters G_0 , κ , and α are related to trap states and are extracted from the model. Also, I_{off} represents the off-current, $L' = L - \Delta L$ where ΔL accounts for the channel

length variation. V'_{DS} is obtained with 2.28 and 2.29 for linear and saturation regimes, respectively.

$$V'_{DS} = V_{DS} - 2R_C I_{DS} \quad (2.28)$$

$$V'_{DS} = (V_{GS} - V_{on}), \quad (2.29)$$

where R_C is contact resistance. It is therefore possible to describe 2.27 for both the linear and saturation regions with 2.30 and 2.31.

$$I_{DS}^{\text{lin}} = G_0^{\text{lin}} \left(\frac{W}{L'} \right) \exp(\kappa_{\text{lin}}(V_{GS} - V_{on})^{\alpha_{\text{lin}}}) (V_{DS} - 2R_C I_{DS}) + I_{\text{off}} \quad (2.30)$$

$$I_{DS}^{\text{sat}} = G_0^{\text{sat}} \left(\frac{W}{L'} \right) \exp(\kappa_{\text{sat}}(V_{GS} - V_{on})^{\alpha_{\text{sat}}}) \times (V_{GS} - V_{on}) + I_{\text{off}}, \quad (2.31)$$

where G_0 , can be evaluated using 2.32 and 2.33 for linear and saturation regions, respectively.

$$G_0^{\text{lin}} \equiv \frac{I'_{DS}(V_{GS} = V_H)}{\left(\frac{W}{L'} \right) \exp(\kappa_{\text{lin}}(V_H - V_{on})^{\alpha_{\text{lin}}}) V'_{DS}} \quad (2.32)$$

$$G_0^{\text{sat}} \equiv \frac{I'_{DS}(V_{GS} = V_H)}{\left(\frac{W}{L'} \right) \exp(\kappa_{\text{sat}}(V_H - V_{on})^{\alpha_{\text{sat}}}) (V_H - V_{on})} \quad (2.33)$$

According to [56], the transition of output characteristics from the linear to saturation regimes is effectively captured by combining the corresponding drain current expressions (2.30 and 2.31) using harmonic averaging.

$$I'_{DS} \equiv ((I_{DS}^{\text{lin}})^{-m} + (I_{DS}^{\text{sat}})^{-m})^{\frac{-1}{m}}, \quad (2.34)$$

where m is a smoothness parameter describ by

$$m \equiv \frac{1}{\log_2(I_{\text{sat}}/I_s)} \quad (2.35)$$

The parameter I_{sat} is defined as I_{DS}^{sat} at $V_{DS} = V_{DS}(\text{max})$ and I_s is the drain current at which $I_{DS}^{\text{lin}} = I_{DS}^{\text{sat}}$.

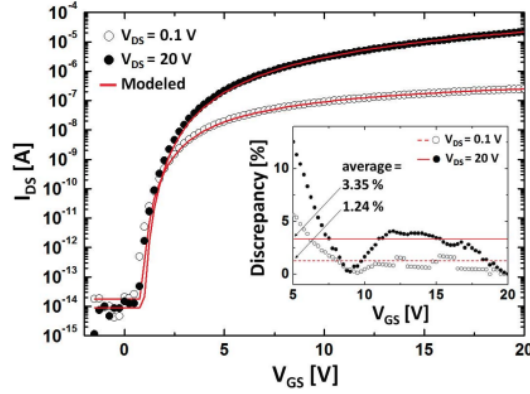


Figure 2.8: Comparison of modeled and measured data, for linear and saturation regimes. Adpated from [56]

Figure 2.8 present a good agreement with the measured $I_{DS} - V_{GS}$ behaviour, covering both linear and saturation region, yielding a discrepancy less than 4% [56].

Table 2.3: Extracted parameters from the CAMCAS Model for A-IGZO TFTS. Adpated from [56]

Parameters	Linear	Saturation	Unit
G_0	2.34×10^{-5}	1.62×10^{-5}	Ω^{-1}
κ	-10.8112	-13.4872	$V^{-\alpha}$
α	-0.5393	-0.5465	-

Table 2.3 present the typical parameters for each regime, for the exemple considered in [56]. In [35], a voltage amplifier was simulated in Verilog-AMS [57] using the CAMCAS model.

2.4 Conclusions

This chapter explored various compact models for semiconductor devices, such as MOS-FETs and TFTs.

Section 2.1 was dedicated to explaining the need for compact models to characterise the electrical behaviour of devices, allowing for more accurate and efficient simulation in ICs.

In 2.2, four existing compact models for MOSFETs were described, which have served as the basis for studying the most recent models that will be applied to TFTs. Each of these models has its own characteristics and applications, varying in complexity and precision, but they are still important today.

In 2.3, compact models of TFTs are discussed. These models differ in their approaches to describing charge mobility, threshold voltage, and contact characteristics, making them more suitable for specific applications and operating conditions. The comparison among these models reveals that while some provide a more efficient and rapid representation,

others offer a deeper understanding of the physical interactions involved in TFTs, thereby enabling more accurate modelling in practical applications.

The following chapter will be dedicated to the analysis of some models described in [2.3](#), as well as their implementation and validation. Testing these models will make it possible to validate their effectiveness, allowing the implications for real circuits and emerging devices to be explored.

FULLY AUTOMATIC PARAMETER EXTRACTION METHODOLOGY

This chapter details the methodological approach adopted for the development and validation of the CAMCAS compact DC model for IGZO thin-film transistors. It begins by describing a fully automated, Python-based technique for extracting key device parameters from experimental measurements. The model’s applicability is then assessed by comparing simulated results with measurement data. To ensure scalability and robustness for circuit design, this methodology is validated using three distinct datasets covering a range of device geometries.

3.1 Dataset Description for Model Evaluation

The experimental evaluation presented in this work is based on three distinct datasets of IGZO TFT devices, all of which were electronically characterized at CEMOP, NOVA FCT. Dataset 1 consists of TFT devices fabricated by an industrial process, while Datasets 2 and 3 include devices manufactured at NOVA FCT in the CENIMAT.

Table 3.1: Dataset 1

L [μm]	W [μm]				
	50	80	100	160	240
0.6		X		X	X
0.8	X		X		

Table 3.1 summarizes the geometries of the industrially-fabricated TFTs, indicating the available combinations of channel width and channel length. Tables 3.2 and 3.3 list the device geometries obtained from in-house fabrication, spanning a range of L and W . The diverse selection of channel dimensions across the three datasets enables a comprehensive study of model scalability as a function of device geometry.

Table 3.2: Dataset 2

L [μm]	W [μm]			
	40	80	160	320
5	X	X	X	X
10	X	X	X	X
20	X	X	X	X
40	X	X	X	X

Table 3.3: Dataset 3

L [μm]	W [μm]	
	50	100
5	X	X
10	X	X
20	X	X

3.2 Parameter extraction

The extraction of device parameters is a fundamental step in accurately characterizing and modeling transistor behavior. These parameters capture both intrinsic and extrinsic effects, enabling precise simulation and performance prediction across different operating conditions. The same procedure is systematically applied to all datasets under study, covering different combinations of W and L .

To accurately model I_{DS} as a function of V_{GS} for $V_{GS} \geq V_{on}$, the compact model uses expressions specific to the saturation and linear operating regions of the transistor. These equations facilitate the extraction of essential device parameters and enable detailed simulation of the transfer characteristics under varying applied voltages. Equation 3.1 describes the drain current behavior in the saturation regime, while Equation 3.2 captures the response in the linear regime.

$$I_{DS}(V_{GS}) = \left(\frac{I'_{DS}(V_H) - I_{off}}{e^{k_{sat}(V_H - V_{on})^{\alpha_{sat}}(V_H - V_{on})}} \right) e^{k_{sat}(V_{GS} - V_{on})^{\alpha_{sat}}(V_{GS} - V_{on})} + I_{off} \quad (3.1)$$

$$I_{DS}(V_{GS}) = \left(\frac{I'_{DS}(V_H) - I_{off}}{e^{k_{lin}(V_H - V_{on})^{\alpha_{lin}}(V_{DS} - 2R_C I'_{DS}(V_H))}} \right) e^{k_{lin}(V_{GS} - V_{on})^{\alpha_{lin}}(V_{DS} - 2R_C I'_{DS}(V_H))} + I_{off} \quad (3.2)$$

The first step considers the evaluation the channel length variation parameter (ΔL) as well as of the contact resistance ($R_{SD} = 2R_C$). As illustrated in Figure 3.1 the total resistance of the device, defined as $R_{tot} = V_{DS}/I_{DS}$, is plotted as a function of L for different values of V_{GS} , with a fixed V_{DS} , corresponding to the linear regime. The example

shown refers specifically to a device with $W = 50 \mu\text{m}$ and $L = 50 \mu\text{m}$ from Dataset 3, serving specifically as an illustrative case for the parameter extraction explanation. In this example, a constant drain-source voltage of $V_{DS} = 0.1 \text{ V}$ is maintained, corresponding to the linear operating regime for the device used as an example. For each value of V_{GS} , a linear fit of the experimental data was performed. The point of common intersection between all the fitted lines allows the simultaneous extraction of $(\Delta L, R_{SD})$.

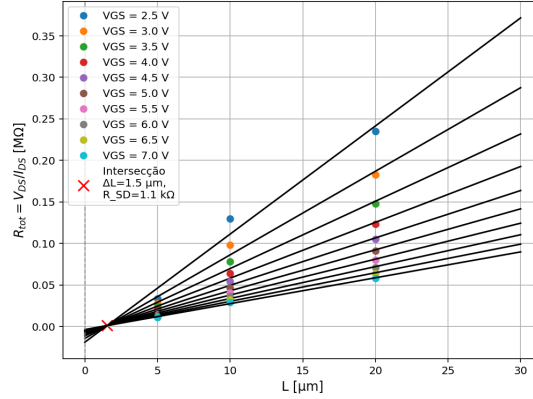


Figure 3.1: Total TFT resistance vs TFT length for different V_{GS} to extract ΔL and R_{SD} , using a $V_{DS} = 0.1 \text{ V}$. The data corresponds to the device with $W = 50 \mu\text{m}$ and $L = 50 \mu\text{m}$ from Dataset 3, used here as an illustrative example.

To extract the parameters V_{on} and I_{off} firstly, outlier data points that lacked physical meaning were removed, especially for very low V_{GS} values, where oscillations in I_{DS} between positive and negative values occurred. Subsequently, the derivative of I_{DS} with respect to V_{GS} was analyzed, and the first positive point in this derivative was identified as the onset point where the transfer characteristic began to increase, thus corresponding to the (V_{on}, I_{off}) point.

This approach represents a significant improvement over the method adopted in [56], where the values of V_{on} and I_{off} were estimated based on graphical inspection of the $I_{DS}(V_{GS})$ curves. In contrast to this empirical procedure, the methodology proposed here enables automatic parameter extraction, ensuring better accuracy and consistency in determining the device's characteristic parameters.

Building upon the previously extracted parameters, the coefficients κ_{lin} , α_{lin} , κ_{sat} , and α_{sat} , which are crucial for accurately describing the transistor's behavior in both the linear and saturation regimes, were subsequently evaluated. To achieve this, Eqs. 2.30 and 2.31 are reformulated in a way that allows for a direct and automated extraction of these coefficients, as represented in 3.3 and 3.4.

To calculate U_{sat} and U_{lin} , a current of $I'_{DS} = I_{DS} - I_{off}$ was considered.

$$U_{lin} \equiv \frac{I'_{DS}/V'_{DS}}{\frac{d(I'_{DS}/V'_{DS})}{dV_{GS}}} = \frac{1}{\alpha_{lin}\kappa_{lin}}(V_{GS} - V_{on})^{1-\alpha_{lin}} \quad (3.3)$$

$$U_{\text{sat}} \equiv \frac{I'_{DS}/(V_{GS} - V_{on})}{\frac{d(I'_{DS}/(V_{GS} - V_{on}))}{dV_{GS}}} = \frac{1}{\alpha_{\text{sat}} \kappa_{\text{sat}}} (V_{GS} - V_{on})^{1-\alpha_{\text{sat}}} \quad (3.4)$$

The behavior of U in both the saturation and linear regions, was analyzed by examining the relationship between $\ln(U)$ and $\ln(V_{GS} - V_{on})$, considering only valid data points where $U \geq 0$. Linear fitting of the experimental data revealed the relationship between these variables, where the slope of the fitted line corresponds to the parameter α , and the intercept on the vertical axis provides the coefficient k . Using this analytical approach, the parameter extraction becomes both consistent and automated. Specifically, from the linear regression slope (a), the parameter α was determined as $\alpha = 1 - a$, and the coefficient κ was computed from the intercept (b) using the relation $\kappa = \frac{1}{\alpha e^b}$.

Additionally, the parameter G_0 was determined based on Equations 2.32 and 2.33, using the previously extracted values of α and k , together with current and voltage data. The reference voltage V_H in these equations corresponds to the highest V_{GS} value.

3.3 Model Scalability and Behavior with Varying Channel Lengths

To further evaluate the robustness and applicability of the proposed extraction methodology, it is also important to analyze the scalability of the model and its behavior across different device geometries. For this purpose, three datasets with varying channel width and length were considered. This analysis particularly focused on comparing trends in parameter sets for W fixed and varying L , and vice versa, allowing direct assessment of scalability. Transfer characteristics for the three datasets considered in this study are provided in the Appendix for detailed reference.

3.3.1 Results Achieved for Dataset 1

This section presents the results obtained from applying the automated parameter extraction methodology to Dataset1, whose device dimensions (W and L) are detailed in Table 3.1. By analyzing the transfer characteristics obtained for this set of TFTs, presented in Appendix A, it can be inferred that higher values of V_{on} will be observed in the linear region for all devices. It was consistently observed across all the transfer characteristics that the onset of conduction in the linear region occurs at a higher gate voltage compared to the saturation region.

The extracted values shown in Table 3.4 and 3.5 confirm the previously observed trend in the transfer characteristics, with consistently higher turn-on voltages in the linear region compared to the saturation region. Dataset 1 considers variations with fixed channel length, which constrains the extraction to parameters related only to V_{on} . To extract the remaining parameters, a dataset with fixed channel width would be required.

Table 3.4: Extracted values of V_{on} and I_{off} for $L = 0.6 \mu\text{m}$.

$W (\mu\text{m})$	$L (\mu\text{m})$	V_{on} Linear [V]	V_{on} Saturation [V]
0.6	80	-0.25	-0.35
	160	-0.10	-0.20
	240	0.00	-0.30

Table 3.5: Extracted values of V_{on} and I_{off} for $L = 0.8 \mu\text{m}$.

$W (\mu\text{m})$	$L (\mu\text{m})$	V_{on} Linear [V]	V_{on} Saturation [V]
0.8	50	0.10	-0.05
	100	-0.10	-0.25

While Dataset 1 alone is insufficient for a full parameter extraction, the scalability of the model will be further assessed using Datasets 2 and 3.

3.3.2 Results Achieved for Dataset 2

This section evaluates the modeling results for Dataset 2, detailed in Table 3.2, providing an analysis of the results obtained from applying the model under study.

The experimental transfer characteristic data obtained for IGZO TFTs presented in Appendix B, revealed considerable variability and irregularities across devices with different W and L . This variability was especially evident at low gate voltages, where a wide dispersion of drain current values was observed. In several measurements, the behavior deviated from what is expected based on the underlying device physics, with occurrences such as unexpected jumps, oscillations, or non-monotonic variations in the drain current. Moreover, even devices with identical geometrical dimensions exhibited inconsistent measurement results. In some cases, individual curves appeared clearly shifted relative to others in the same group, or displayed outlier behavior, making it difficult to accurately determine key parameters such as the turn-on voltage. Some measured data also presented non-physical features, such as a decrease in drain current with increasing gate voltage over specific intervals, which is inconsistent with the expected operation of IGZO TFTs. These anomalies highlight the importance of a rigorous data selection process before proceeding with modeling and parameter extraction. Therefore, for each group of devices, the measured data that most closely aligned with ideal IGZO TFT behavior was carefully selected. Priority was given to curves with minimal dispersion, smooth and well-defined transitions between the cut-off, linear, and saturation regions, and an absence of abrupt or non-physical features. In particular, the dataset corresponding to the device with $W = 100 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ was excluded from the analysis, as its behavior did not conform to the expected characteristics of IGZO TFTs. This approach ensures that the modeling relies on data that accurately represents the actual device behavior and supports a robust and reproducible basis for parameter extraction.

Table 3.6: Extracted values of V_{on} in the linear and saturation regions for various W and L , from Dataset 2.

W (μm)	L (μm)	V_{on} Linear [V]	V_{on} Saturation [V]
320	5	-0.261	0.441
	10	1.079	0.806
	20	0.408	0.701
	40	-0.712	-0.132
160	5	1.38	1.48
	10	0.84	1.03
	20	1.14	1.36
	40	0.80	0.85
80	10	1.57	1.66
	20	1.80	1.85
	40	0.72	0.73
40	5	1.39	1.40
	10	1.44	1.55
	20	0.35	0.36
	40	0.72	0.73

Table 3.6 presents the extracted values of V_{on} in both the linear and saturation regions for the different combinations of W and L from Dataset 2. For $W = 320 \mu\text{m}$, the extracted V_{on} values exhibit a pronounced discrepancy between the linear and saturation regions. Furthermore, no clear trend can be established regarding which region consistently yields higher V_{on} values. For the remaining channel widths, the general trend is that V_{on} values are higher in the saturation region. It is also noteworthy that, in several cases, the extracted values from both regions are very close to each other, with only minor discrepancies. For parameter extraction, the highest value of V_{on} was considered, since the proposed model uses a single V_{on} value for both the linear and saturation regions. By adopting the maximum V_{on} value, it is ensured that both device regimes are in their conductive state at that specific gate-source voltage, allowing consistent modeling across different operational regions.

Table 3.7: Calculated values of ΔL and R_{SD} for different W , using Dataset 2.

W (μm)	ΔL (μm)	R_{SD} ($\text{k}\Omega$)
320	2.08	2.8
160	-4.6591	-9.2
80	3.3	6.4
40	-0.44	14.09

The calculated values of ΔL and R_{SD} for different channel widths exhibit significant variation. The parameter ΔL not only varies in magnitude but also changes sign depending on the width, indicating a non-uniform influence of channel width on the effective channel length correction. Specifically, for $W = 160 \text{ } \mu\text{m}$, ΔL takes on a strongly negative value, while for other widths such as $W = 80 \text{ } \mu\text{m}$ and $W = 320 \text{ } \mu\text{m}$, it is positive. Regarding the source-drain resistance R_{SD} , the values remain generally small, but an increase is observed for the narrowest devices ($W = 40 \text{ } \mu\text{m}$), suggesting that parasitic resistances become more significant as the device width decreases. It is important to highlight that, as discussed earlier, there is considerable discrepancy among measurements even within devices of identical geometry (same W and L). Consequently, the results presented here may lack full coherence, reflecting the inherent variability in experimental data. This variability emphasizes the need for caution when interpreting parameter extraction results and modeling IGZO TFTs, as the physical device behavior may be masked or distorted by measurement inconsistencies.

Table 3.8: Extracted model parameters for Dataset 2.

W [μm]	L [μm]	Linear			Saturation		
		α	κ	G_0	α	κ	G_0
320	5	-0.056	-42.881	2.54×10^{11}	-0.042	-96.244	8.13×10^{32}
	10	-0.520	-6.045	9.88×10^{-5}	-0.259	-8.701	1.15×10^{-3}
	20	-0.174	-10.003	1.77×10^{-2}	-0.432	-6.933	1.17×10^{-4}
	40	-0.011	109.871	5.33×10^{41}	-0.407	-8.180	2.31×10^{-4}
160	5	-0.395	-6.069	3.97×10^{-4}	-0.516	-6.696	1.76×10^{-4}
	10	-0.288	-6.912	1.16×10^{-3}	-0.374	-1.178	3.40×10^{-4}
	20	-0.311	-6.808	6.66×10^{-4}	-0.380	-6.633	1.16×10^{-3}
	40	-0.251	-8.657	3.55×10^{-3}	-0.180	-12.993	6.76×10^{-2}
80	10	-0.333	-7.021	3.95×10^{-4}	-0.366	-7.533	1.85×10^{-4}
	20	-0.356	-5.903	2.42×10^{-4}	-0.432	-5.794	6.71×10^{-5}
	40	-0.263	-7.877	1.39×10^{-3}	-0.211	-9.808	3.50×10^{-3}
40	5	-0.418	-5.868	2.10×10^{-4}	-0.520	-6.241	7.80×10^{-5}
	10	-0.185	-10.073	1.92×10^{-2}	-0.241	-9.738	3.51×10^{-3}
	20	-0.348	-6.409	3.63×10^{-4}	-0.346	-6.974	2.49×10^{-4}
	40	-0.263	-7.877	3.07×10^{-3}	-0.211	-9.809	7.71×10^{-3}

Table 3.8 summarizes the results obtained for all evaluated combinations of W and L , enabling a comprehensive comparison of the extracted parameters across the different device geometries analyzed.

When analyzing the parameters obtained for $W = 320 \text{ } \mu\text{m}$, it is evident that the extracted values exhibit a considerable deviation, which should not occur under ideal conditions. The values obtained for $W = 320 \text{ } \mu\text{m}$ and $L = 5 \text{ } \mu\text{m}$ do not reflect any

physical significance, particularly in regard to the parameters κ and G_0 in both the linear and saturation regions. The same issue is observed for $L = 40 \mu\text{m}$ in the linear region, where the extracted parameters also lack physical meaning. For $L = 10 \mu\text{m}$ and $L = 20 \mu\text{m}$, although the extracted parameter values are notably more satisfactory, there is a significant difference between them when the channel length is varied. According to theoretical expectations, the parameter G_0 should decrease as L increases. However, this trend is not observed in the saturation regime, where G_0 instead rises by nearly three orders of magnitude. Furthermore, the values of κ and α do not display any consistent trend with respect to changes in L . This lack of clear dependence and inconsistency across parameter values prevents any meaningful inference of scalability based on the extracted results.

Examining the extracted parameters for $W = 160 \mu\text{m}$ devices, a non-physical tendency is observed, G_0 increases with increasing channel length, while theoretically, it should decrease as L becomes larger. The values of κ and α fall within the typical range reported in the literature for IGZO TFTs, aside from $L = 10 \mu\text{m}$ and $L = 40 \mu\text{m}$ in saturation, where anomalous behavior is observed. However, there is no clear or systematic dependence of these parameters on channel length.

For $W = 80 \mu\text{m}$, as previously discussed, the dataset corresponding to $L = 5 \mu\text{m}$ was excluded due to its non-conformity with the expected device behavior. The G_0 parameter follows the physical trend, decreasing with increasing channel length, except at $L = 40 \mu\text{m}$, where this tendency is not observed. The extracted κ and α values fluctuate but generally remain within the typical range reported in literature and do not display abrupt jumps or physically inconsistent values, aside from the case of $L = 40 \mu\text{m}$ in saturation.

For $W = 40 \mu\text{m}$, a similar trend is observed as in other channel widths, except for $W = 320 \mu\text{m}$. The parameter G_0 follows the expected physical tendency with increasing channel length, except at $L = 40 \mu\text{m}$, where an abrupt jump of almost one order of magnitude is seen in both regimes, indicating a possible anomaly or outlier in the data. The κ and α parameters fluctuate with L , but do not exhibit strong correlation with channel length variation.

Overall, the extracted model parameters do not exhibit a consistent or reliable dependence on the geometrical dimensions of the devices.

To establish a robust relationship of scalability, it is essential to ensure uniform data across all device geometries and measurement conditions. Minor variations or irregularities in the experimental dataset can make it challenging to clearly identify physical trends or to extract model parameters with high reproducibility and physical significance.

Based on the current dataset, while some trends can be observed, the variability across devices limits the ability to draw definitive conclusions regarding the dependence of parameters on device geometry. As a result, any scalability assessments or model extrapolations should be approached with caution, acknowledging the influence of measurement variability on the results.

3.3.3 Results Achieved for Dataset 3

In this section, the focus is on presenting the results achieved for Dataset 3 detailed in Table 3.3 and its previous analyses. As with the previous datasets, the transfer characteristic plots for the devices measured in Dataset 3 are provided in Appendix C for reference. An examination of these characteristics indicates that Dataset 3 presents consistent behavior aligned with the expected physical operation of a TFT, making it suitable for further modeling and analysis. The comprehensive analysis includes both transfer characteristics modeling and output characteristics evaluation, with all detailed results presented in the Appendix D for complete reference.

Table 3.9: Extracted values of V_{on} in the linear and saturation regions for various W and L , from Dataset 3.

W (μm)	L (μm)	V_{on} Linear [V]	V_{on} Saturation [V]
100	5	-0.653	-0.818
	10	-0.521	-0.443
	20	-0.609	-0.543
50	5	-1.467	-1.534
	10	-0.146	-0.256
	20	-0.366	-0.410

The extracted V_{on} values from Dataset 3, presented in Table 3.9, reveal a consistent trend across both channel lengths and widths.

For both $W = 100 \mu\text{m}$ and $W = 50 \mu\text{m}$, the on-voltage remains negative in both linear and saturation regimes. For $W = 50 \mu\text{m}$, there is a clear trend in which the V_{on} values are systematically lower (more negative) in the saturation region compared to their linear counterparts. Furthermore, a general decrease in the absolute value of V_{on} with increasing channel length can be observed, which is typically associated with reduced short-channel effects and improved gate control.

As mentioned previously, the higher (less negative) of the two V_{on} values, between the linear and saturation regimes, was selected as the reference for subsequent model parameter extraction.

Table 3.10 presents the extracted I_{off} values corresponding to the maximum V_{on} identified for each device geometry. The off-current values vary with both L and W , with a general trend of increasing I_{off} for shorter channels.

Table 3.11 presents the calculated values of ΔL and R_{SD} for two different channel widths from Dataset 3. The values of ΔL are relatively close for both widths ($1.62 \mu\text{m}$ for $W = 100 \mu\text{m}$ and $1.54 \mu\text{m}$ for $W = 50 \mu\text{m}$), indicating a consistent systematic offset likely arising from the fabrication process. This indicates that devices across both widths were affected by comparable fabrication-induced variations, independent of their geometries. In terms of R_{SD} , a clear trend is observed, the resistance increases as the channel width

Table 3.10: Extracted values of I_{off} in the linear and saturation regions for various W and L , from Dataset 3. Values correspond to the current at maximum V_{on} .

W (μm)	L (μm)	I_{off} Linear [A]	I_{off} Saturation [A]
100	5	1.15×10^{-13}	1.50×10^{-12}
	10	2.51×10^{-12}	3.19×10^{-13}
	20	2.99×10^{-13}	2.76×10^{-14}
50	5	8.12×10^{-14}	2.55×10^{-12}
	10	8.20×10^{-14}	6.42×10^{-13}
	20	2.30×10^{-14}	1.23×10^{-12}

 Table 3.11: Calculated values of ΔL and R_{SD} for different W , using Dataset 3.

W (μm)	ΔL (μm)	R_{SD} ($\text{k}\Omega$)
100	1.62	0.75
50	1.54	1.13

decreases, which is consistent with physical expectations.

When compared to the values obtained in Dataset 2 (Table 3.7), the results from Dataset 3 appear more consistent and physically reasonable. In particular, the sign and magnitude of ΔL are coherent across geometries, and the values of R_{SD} are positive and within expected ranges.

 Table 3.12: Extracted model parameters (α , κ , and G_0) from Dataset 3, for various W and L , in both linear and saturation regimes.

W [μm]	L [μm]	Linear			Saturation		
		α	κ	G_0	α	κ	G_0
100	5	-0.427	-7.060	7.46×10^{-5}	-0.325	-8.492	7.37×10^{-5}
	10	-0.365	-6.973	1.87×10^{-4}	-0.241	-9.570	1.13×10^{-3}
	20	-0.378	-7.320	1.59×10^{-4}	-0.262	-10.031	8.32×10^{-4}
50	5	-0.409	-7.515	1.48×10^{-4}	-0.268	-10.478	1.24×10^{-3}
	10	-0.357	-7.539	2.44×10^{-4}	-0.286	-9.432	5.73×10^{-4}
	20	-0.369	-7.034	1.84×10^{-4}	-0.348	-7.609	1.23×10^{-4}

Table 3.12 summarizes the extracted model parameters for various channel widths and lengths, considering both the linear and saturation regimes.

For $W = 100 \mu\text{m}$, the values of α and κ remain relatively stable across the different channel lengths in the linear regime, with α around -0.37 and κ near -7 . However, in the saturation regime, κ shows an increasing magnitude with L . The parameter G_0 exhibits significant variation, particularly in saturation, where the value at $L = 10 \mu\text{m}$ is nearly an order of magnitude higher than others, indicating potential measurement inconsistencies

or external influences affecting the data.

For $W = 50 \mu\text{m}$, α shows minor variation with L in linear regime, ranging approximately from -0.37 to -0.41 , while κ remains fairly consistent around -7.5 . In saturation, however, κ varies more widely, and α shows no clear trend, fluctuating between -0.26 to -0.35 . The G_0 parameter again varies considerably, with the highest value at $L = 5 \mu\text{m}$.

Although no clear or systematic trends are observed in the extracted parameter values with respect to channel length or width, the results generally fall within the ranges reported in the literature for IGZO TFTs. Therefore, these extracted parameters will be used as the basis for developing the scalable models as functions of both W and L .

The modeled transfer characteristics show close agreement with experimental data across all device geometries in Dataset 3. The model reproduces the behavior of IGZO TFTs in both linear and saturation regimes, validating the robustness of the extraction methodology. All transfer characteristic comparisons between modeled and experimental data are presented in Appendix D, illustrating the model's accuracy throughout the operational range.

The relative error analysis indicates that the model maintains accuracy, particularly for low gate-source voltages ($V_{GS} < 1\text{V}$), where the errors predominantly remain below 10%. This performance in the low-voltage region is relevant for circuit applications operating at reduced supply voltages, which are increasingly common in modern electronic systems. The error distribution shows consistent behavior across different device geometries, with the smallest errors typically occurring in the region where the device transitions from off-state to on-state operation.

The $I_D(V_{DS})$ characteristics modeling shows that the model tracks the experimental data across the entire drain-source voltage range. The output characteristics comparisons, presented in the appendix, show that the model reproduces the linear-to-saturation transition and aligns with experimental measurements in both operational regimes. However, it is noteworthy that for drain-source voltages approaching 1V, a slight deviation between the model and experimental data is observed.

3.4 Conclusions on Model Scalability

As mentioned before scalability of compact models is a fundamental aspect of device characterization, since it ensures that parameters extracted from a limited set of measurements can be generalized to a broader range of geometries.

In this section, several key parameters were modeled as functions of the channel length L and the channel width W , based on the results obtained from the parameter extraction of Dataset 3.

The methodology followed a two-step process. First, as three distinct L values are available a quadratic fitting was considering. Then, since only two values of W were available a linear fitting was applied. The final outcome is a set of continuous, scalable models

that express each parameter as a bivariate function of (L, W) . This section consolidates the results into a unified mathematical formulation.

3.4.1 Results Achieved

As a first step, quadratic approximations in L were obtained for fixed $W = 50 \mu\text{m}$ and $W = 100 \mu\text{m}$, based directly on the parameter extraction from Dataset 3. These fits capture the dependence of each parameter on L and provide the foundation for the subsequent scalable bivariate models in both L and W , as represented in Equations 3.5 and 3.6 for a general parameter

$$X = a_1 L^2 + b_1 L + c_1 \quad (3.5)$$

where the channel length L depends linearly on W as:

$$L = a_2 W + b_2 \quad (3.6)$$

The resulting coefficient are presented in Table 3.13.

Building on these intermediate fits, the coefficients were expressed as linear functions of width, resulting in continuous models suitable for interpolation across different device geometries. The resulting models are summarized below.

The expressions for V_{on} as a function of both W and L are presented next.

Linear regime:

$$\begin{aligned} V_{\text{on, lin}}(L, W) = & (3.35 \times 10^{-4} W - 3.58 \times 10^{-2}) L^2 + (-9.78 \times 10^{-3} W + 1.04) L \\ & + (5.68 \times 10^{-2} W - 6.58) \end{aligned} \quad (3.7)$$

Saturation regime:

$$\begin{aligned} V_{\text{on, sat}}(L, W) = & (2.48 \times 10^{-4} W - 3.05 \times 10^{-2}) L^2 + (-7.33 \times 10^{-3} W + 8.93 \times 10^{-1}) L \\ & + (4.48 \times 10^{-2} W - 5.95) \end{aligned} \quad (3.8)$$

The expressions for α as a function of both W and L are presented below.

Linear regime:

$$\begin{aligned} \alpha_{\text{lin}}(L, W) = & (-2.80 \times 10^{-6} W - 6.33 \times 10^{-4}) L^2 + (8.20 \times 10^{-5} W + 1.79 \times 10^{-2}) L \\ & + (-7.00 \times 10^{-4} W - 4.65 \times 10^{-1}) \end{aligned} \quad (3.9)$$

Saturation regime:

$$\begin{aligned} \alpha_{\text{sat}}(L, W) = & (-2.17 \times 10^{-5} W + 9.13 \times 10^{-4}) L^2 + (7.34 \times 10^{-4} W - 3.77 \times 10^{-2}) L \\ & + (-4.27 \times 10^{-3} W - 4.53 \times 10^{-2}) \end{aligned} \quad (3.10)$$

The dependence of κ on W and L can be expressed as follows.

Table 3.13: Quadratic coefficients (a_1, b_1, c_1) for each parameter. Each row shows the coefficients in the form $X = a_1 L^2 + b_1 L + c_1$ for the specified W .

Parameter	Regime	W (μm)	a_1	b_1	c_1
V_{on}	Linear	100	-2.35×10^{-3}	6.16×10^{-2}	-9.02×10^{-1}
V_{on}	Linear	50	-5.67×10^{-3}	1.60×10^{-1}	-1.48×10^0
V_{on}	Saturation	100	-1.91×10^{-2}	5.50×10^{-1}	-3.74×10^0
V_{on}	Saturation	50	-1.81×10^{-2}	5.27×10^{-1}	-3.72×10^0
α	Linear	100	-9.13×10^{-4}	2.61×10^{-2}	-5.35×10^{-1}
α	Linear	50	-1.26×10^{-3}	3.57×10^{-2}	-4.72×10^{-1}
α	Saturation	100	-7.73×10^{-4}	2.20×10^{-2}	-5.00×10^{-1}
α	Saturation	50	-1.73×10^{-4}	-1.00×10^{-3}	-2.59×10^{-1}
κ	Linear	100	-3.47×10^{-3}	6.95×10^{-2}	-7.32×10^0
κ	Linear	50	1.13×10^{-2}	-3.85×10^{-1}	-6.85×10^0
κ	Saturation	100	3.69×10^{-3}	-6.01×10^{-2}	-7.31×10^0
κ	Saturation	50	-1.79×10^{-3}	2.36×10^{-1}	-1.16×10^1
G_0	Linear	100	1.69×10^{-6}	4.78×10^{-5}	-1.22×10^{-4}
G_0	Linear	50	-1.61×10^{-5}	4.52×10^{-4}	-1.79×10^{-3}
G_0	Saturation	100	-1.68×10^{-6}	4.44×10^{-5}	-3.20×10^{-5}
G_0	Saturation	50	5.89×10^{-6}	-2.22×10^{-4}	2.20×10^{-3}
I_{off}	Linear	100	-4.67×10^{-14}	1.18×10^{-12}	-4.61×10^{-12}
I_{off}	Linear	50	1.38×10^{-14}	-4.43×10^{-13}	3.37×10^{-12}
I_{off}	Saturation	100	-4.04×10^{-16}	6.22×10^{-15}	6.02×10^{-14}
I_{off}	Saturation	50	2.94×10^{-14}	-8.22×10^{-13}	5.93×10^{-12}

Linear regime:

$$\begin{aligned} \kappa_{\text{lin}}(L, W) = & (-1.43 \times 10^{-4}W + 1.08 \times 10^{-2}) L^2 + (2.59 \times 10^{-3}W - 1.90 \times 10^{-1}) L \\ & + (-2.80 \times 10^{-4}W - 7.29) \end{aligned} \quad (3.11)$$

Saturation regime:

$$\begin{aligned} \kappa_{\text{sat}}(L, W) = & (-2.62 \times 10^{-4}W - 1.49 \times 10^{-2}) L^2 + (-1.24 \times 10^{-2}W + 8.57 \times 10^{-1}) L \\ & + (9.53 \times 10^{-2}W - 16.4) \end{aligned} \quad (3.12)$$

The resulting models for G_0 , expressed in terms of W and L , are given next.

Linear regime:

$$\begin{aligned} G_{0,\text{lin}}(L, W) = & (-1.07 \times 10^{-10}W - 1.67 \times 10^{-6}) L^2 + (6.72 \times 10^{-8}W + 4.10 \times 10^{-5}) L \\ & + (-1.80 \times 10^{-6}W + 5.81 \times 10^{-5}) \end{aligned} \quad (3.13)$$

Saturation regime:

$$G_{\text{sat}}(L, W) = (-4.39 \times 10^{-7}W + 2.79 \times 10^{-5})L^2 + (1.35 \times 10^{-5}W - 8.96 \times 10^{-4})L + (-7.98 \times 10^{-5}W + 6.19 \times 10^{-3}) \quad (3.14)$$

The expressions for I_{off} as a function of both W and L are presented below.

Linear regime:

$$I_{\text{off,lin}}(L, W) = (-9.25 \times 10^{-16}W + 4.59 \times 10^{-14})L^2 + (2.35 \times 10^{-14}W - 1.17 \times 10^{-12})L + (-9.35 \times 10^{-14}W + 4.73 \times 10^{-12}) \quad (3.15)$$

Saturation regime:

$$I_{\text{off,sat}}(L, W) = (-3.11 \times 10^{-16}W + 4.49 \times 10^{-14})L^2 + (7.57 \times 10^{-15}W - 1.20 \times 10^{-12})L + (-5.11 \times 10^{-14}W + 8.48 \times 10^{-12}) \quad (3.16)$$

In addition, the parameters ΔL and R_{SD} depend solely on the channel width W . Since only two measurement points were available for each parameter, a simple linear fit was employed to obtain scalable models.

$$\Delta L(W) = 0.0016W + 1.46 \quad (3.17)$$

$$RSD(W) = -0.0076W + 1.51 \quad (3.18)$$

The comprehensive validation of these scalable parametric expressions across different device geometries is presented through detailed graphical analysis. Additional validation plots for the individual model parameters as functions of channel width and length are provided in Appendix E.

The current scalable models are calibrated to the available dataset of device geometries. Accordingly, the fitting functions and polynomial degrees are selected to match the resolution of the parameter space coverage, ensuring model stability within this range. Expanding the measurement matrix to a wider distribution of channel lengths and widths would allow for further refinement of the scalability analysis.

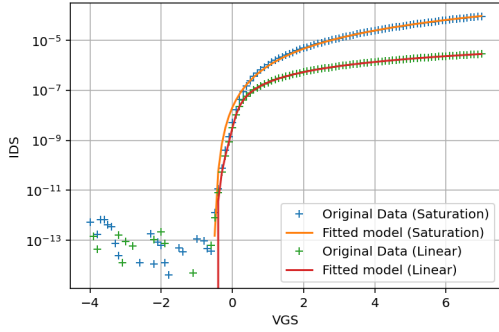
Data acquisition from devices fabricated on the same technology node and wafer is recommended to minimize process variability. This approach isolates intrinsic device behavior from process-induced variations.

To enable circuit-level design, the developed scalable models are incorporated in subsequent stages for circuit-level implementation using Verilog-A, providing a foundation for simulation tools that support design and optimization of thin-film transistor technologies.

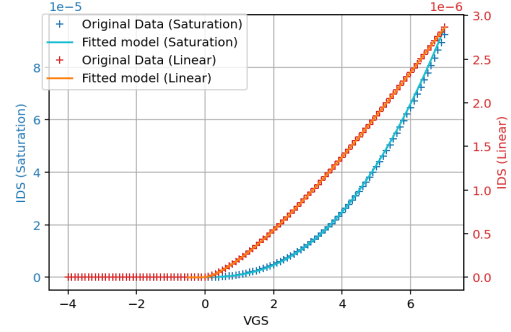
3.4.2 Validation of the Scalable Model

In this section we present the transfer characteristics obtained with the analytical expressions previously presented in 3.4.1 and using the considered model, against experimental values.

As illustrated in Figures 3.2–3.7 results confirm the approximation presented where, according to the relative errors in Figures 3.8 and 3.9, illustrate the accuracy of the approach when compared to the actual measured data.

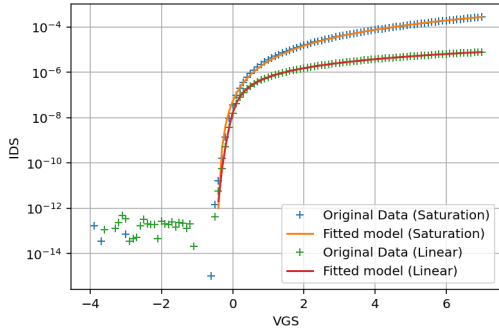


(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$, using a logarithmic scale.

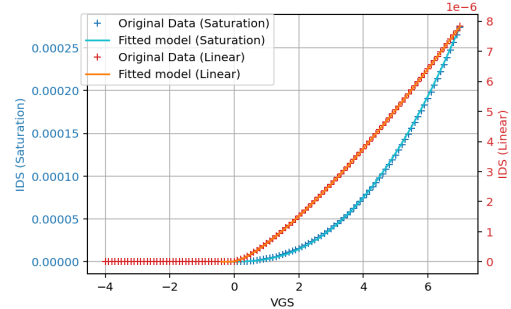


(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$, using linear scale.

Figure 3.2: Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$.



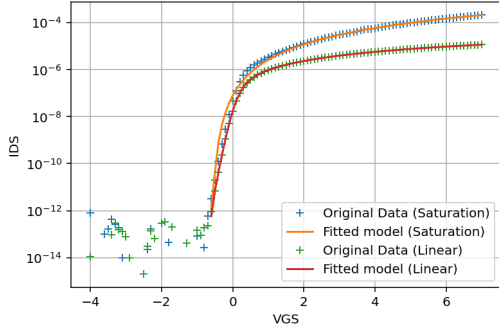
(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$, using a logarithmic scale.



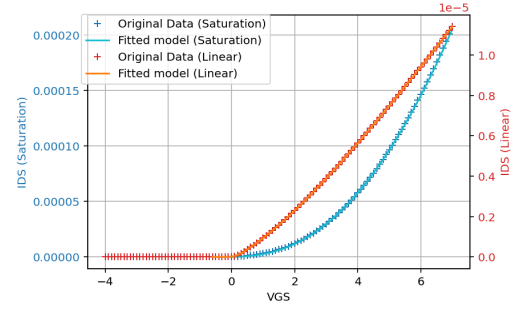
(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$, using linear scale.

Figure 3.3: Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$.

The comparative analysis between modeled results and experimental measurements shows a close correspondence across all six device configurations evaluated. Figures 3.2–3.7 indicate that the scalable model reproduces IGZO TFT operation, describing current levels, turn-on behavior, and regime transitions for each geometry. The model maintains accuracy across channel width and length variations, suggesting that the parametric

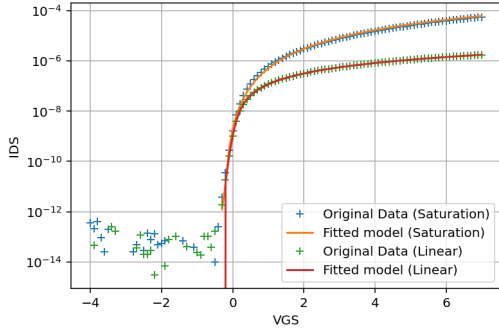


(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$, using a logarithmic scale.

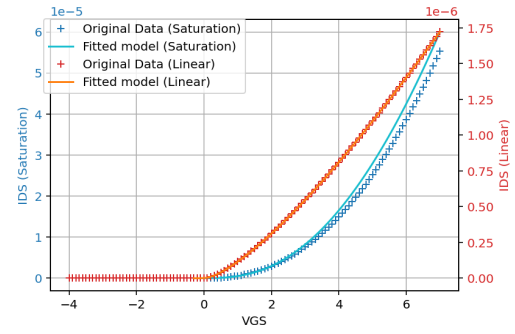


(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$, using linear scale.

Figure 3.4: Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$.



(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$, using a logarithmic scale.

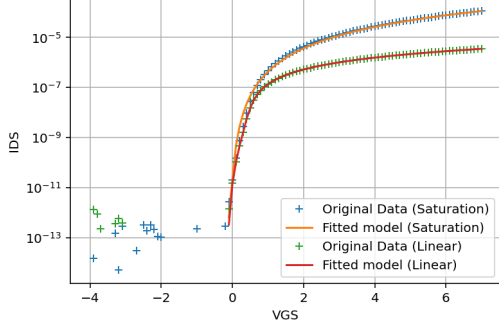


(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$, using linear scale.

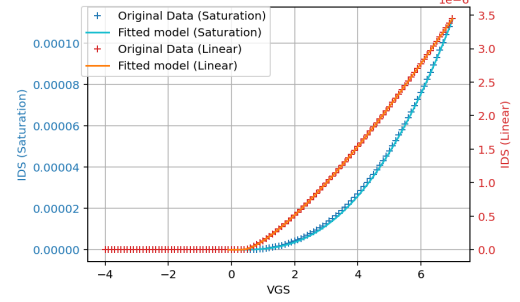
Figure 3.5: Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$.

scaling functions account for the underlying geometric dependencies.

As illustrated in 3.8 and 3.9, the scalable model shows relative errors predominantly remaining below 10% for V_{GS} above 1 V for most device geometries, showing consistent patterns across different dimensions. The model exhibits increased deviations near the turn-on region, which is consistent with the complexity of modeling the transition from off-state to on-state operation. The validation across multiple device geometries indicates that the bivariate parametric expressions account for the dependence of key model parameters on both channel width and length. Consequently, the scalable model provides a unified framework suitable for predicting device behavior across different channel dimensions while maintaining computational efficiency essential for circuit-level simulations.

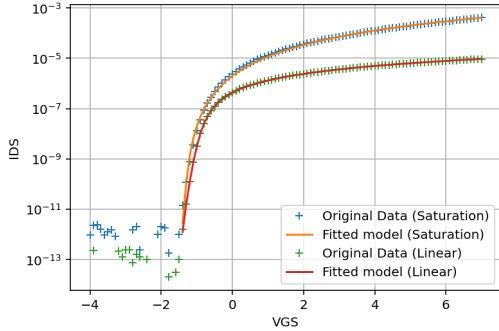


(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$, using a logarithmic scale.

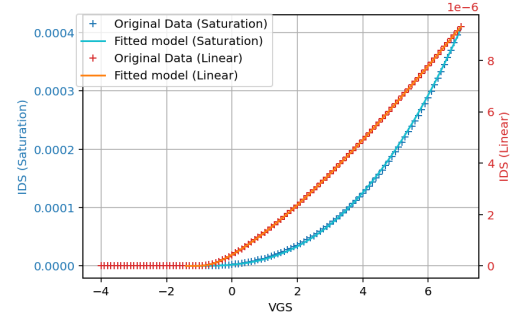


(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$, using linear scale.

Figure 3.6: Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$.



(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$, using a logarithmic scale.



(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$, using linear scale.

Figure 3.7: Modeled results for linear and saturation regimes using the scalable model, compared to the measured data for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$.

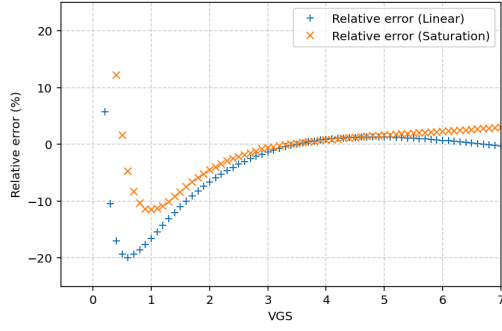
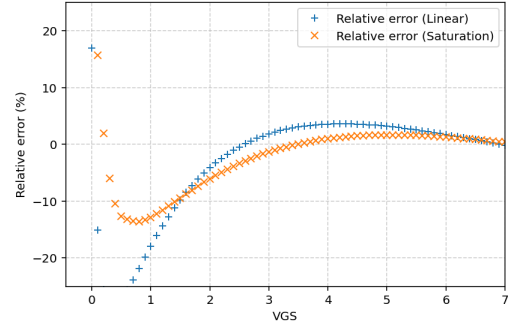
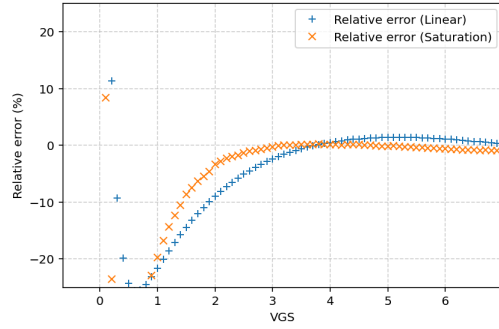

 (a) $W = 100 \mu\text{m}, L = 20 \mu\text{m}$

 (b) $W = 100 \mu\text{m}, L = 10 \mu\text{m}$

 (c) $W = 100 \mu\text{m}, L = 5 \mu\text{m}$

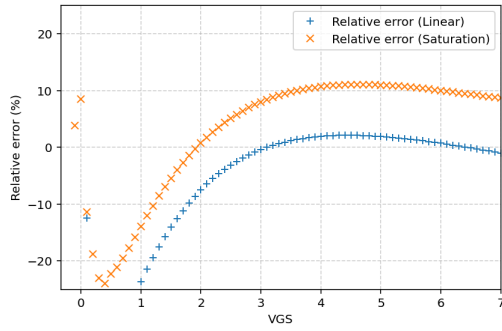
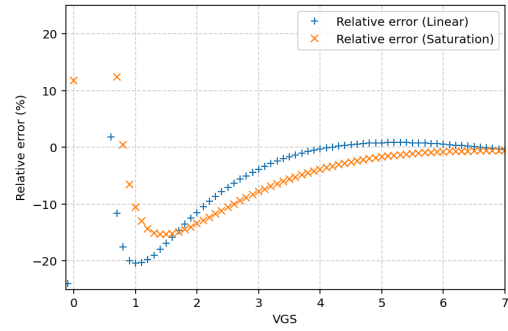
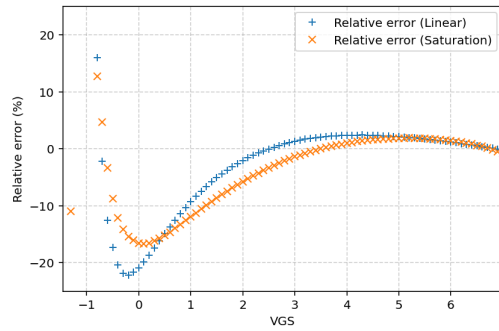
 Figure 3.8: Relative error of the scalable model for devices with $W = 100 \mu\text{m}$ and different channel lengths L .

 (a) $W = 50 \mu\text{m}, L = 20 \mu\text{m}$

 (b) $W = 50 \mu\text{m}, L = 10 \mu\text{m}$

 (c) $W = 50 \mu\text{m}, L = 5 \mu\text{m}$

 Figure 3.9: Relative error of the scalable model for devices with $W = 50 \mu\text{m}$ and different channel lengths L .

SMALL SIGNAL MODELLING

Small signal modelling analyzes electronic circuits under small variations around a specific operating point. Because semiconductor devices like transistors and diodes behave nonlinearly, exact analysis of large signals can be complex. However, for sufficiently small inputs, these devices can be approximated by linear models around the operating point, simplifying the analysis [58].

In this chapter, small signal modelling is applied to the previously established DC model to derive a linearized equivalent circuit that characterizes the device's response to small perturbations. The chapter also discusses the applicability and limitations of the small signal model within the specific context of the device under study.

4.1 Small Signal Modelling for Thin-Film Transistors (TFTs)

Small signal modelling simplifies the analysis of nonlinear devices by linearizing their behavior around a DC operating point, enabling tractable evaluation of dynamic circuit characteristics such as gain, input and output impedances, and frequency response. While traditional MOSFET small signal models are well established, applying them directly to thin-film transistors (TFTs) is inadequate because TFTs exhibit fundamentally different physical properties. In particular, the interfaces between the various materials in a TFT lead to much larger contact resistance, more prominent parasitic capacitances, and more stability issues. Accurate prediction and representation of TFT-based circuit behavior therefore demand models that explicitly account for these device-specific effects [34], [59].

4.1.1 From the General 3-Terminal Device Model to the TFT Small Signal Model

The small-signal modeling process for TFTs is grounded in a generic approach applicable to any three-terminal device. The foundational model, presented in Figure 4.1, considers voltages and currents at the gate (G), source (S), and drain (D) terminals, and can be summarized as:

$$\begin{cases} I_D = f_1(V_{GS}, V_{DS}) \\ I_G = f_2(V_{GS}, V_{DS}) \end{cases} \quad (4.1)$$

For small-signal analysis, variations about a DC bias point are considered, leading to linearized expressions:

$$\begin{cases} dI_D = \frac{\partial f_1}{\partial V_{GS}} dV_{GS} + \frac{\partial f_1}{\partial V_{DS}} dV_{DS} \\ dI_G = \frac{\partial f_2}{\partial V_{GS}} dV_{GS} + \frac{\partial f_2}{\partial V_{DS}} dV_{DS} \end{cases} \quad (4.2)$$

This yields the generic small-signal representation:

$$\begin{cases} i_d = g_{m1} v_{gs} + \frac{v_{ds}}{r_{o1}} \\ i_g = \frac{v_{gs}}{r_{o2}} + g_{m2} v_{ds} \end{cases} \quad (4.3)$$

Here g_{m1} and g_{m2} denote transconductance parameters, while r_{o1} and r_{o2} represent the output and gate resistances, respectively. For most field-effect devices, i_g is negligible and the model can be further simplified to:

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_o} \quad (4.4)$$

Next, Figure 4.1 shows a general small-signal model for any three-terminal device, illustrating all main voltage and current relationships between its terminals. Figure 4.2 presents a simplified version of this model, retaining only the essential components necessary for most practical small-signal analyses. These two diagrams provide a visual basis for understanding and further specializing small-signal models for specific devices such as TFTs.

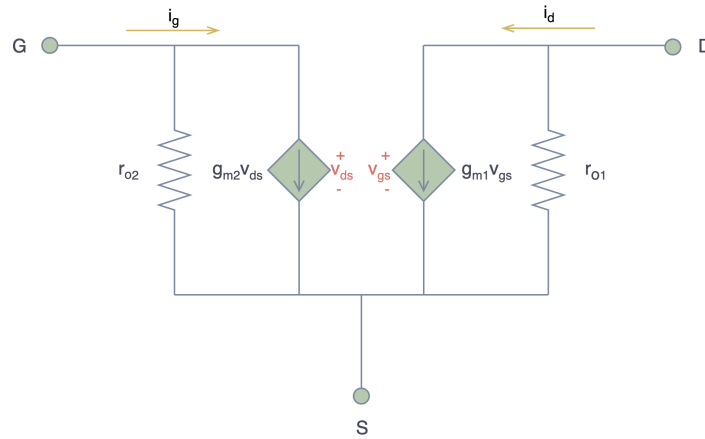


Figure 4.1: Generic small-signal model for a three-terminal device, illustrating the configuration of gate, source, and drain terminals, as well as the principal small-signal parameters.

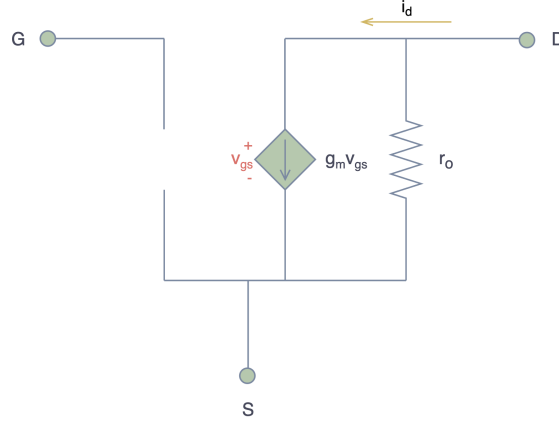


Figure 4.2: Simplified small-signal equivalent circuit for a three-terminal device, highlighting only the essential elements and parameters relevant to basic linear analysis.

4.1.2 Adaptation Toward TFTs

While the general hybrid- π framework applies to BJTs, MOSFETs, and TFTs alike, TFTs exhibit additional effects that distinguish them from traditional devices.

Notably, TFTs have significant contact resistances at the source and drain as well as at the channel interfaces, resulting in visible voltage drops that must be modeled explicitly as external series resistors.

Furthermore, TFTs often feature enhanced parasitic capacitances, including overlap capacitances between the gate-source and gate-drain terminals and channel capacitance, which tend to be larger due to the geometry and less precise process control typical of thin-film fabrication [58].

Figures 4.3 presents the midband small-signal equivalent circuit for a TFT. This model explicitly includes both the contact resistances at the source and drain (R_S , R_D), as well as the principal parasitic capacitances, the overlap at the source (C_{OVS}) and drain (C_{OVD}), and the channel capacitance (C_{CH}). The intrinsic transistor behavior is represented by the voltage-controlled current source ($g_m v_{gs}$) and output resistance (r_o). This configuration captures the main non-idealities characteristic of TFTs, such as significant contact resistance and distributed capacitances, which must be considered for accurate circuit modeling and performance prediction.

The behavior of each element in the TFT small-signal equivalent circuit can be rigorously quantified using the derivatives of the device's current-voltage characteristics with respect to the controlling voltages.

In both the saturation and linear regimes, the transconductance is formally expressed as the partial derivative of the drain current with respect to the gate-source voltage.

$$g_{m_{sat}} = \frac{dI_{D_{sat}}}{dV_{GS}} = \frac{G_{0_{sat}} W (\alpha_{sat} k_{sat} (V_{GS} - V_{on})^{\alpha_{sat}} + 1) e^{k_{sat}(V_{GS} - V_{on})^{\alpha_{sat}}}}{\Delta L} \quad (4.5)$$

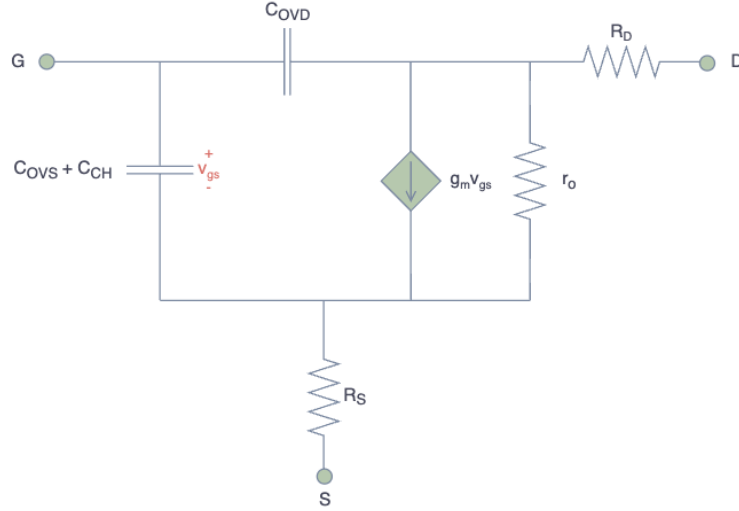


Figure 4.3: TFT Small Signal Model

$$g_{m_{lin}} = \frac{dI_{D_{lin}}}{dV_{GS}} = \frac{G_{0lin} W \alpha_{lin} k_{lin} (V_{GS} - V_{on})^{\alpha_{lin}-1} (-2I_{DS}R_C + V_{DS}) e^{k_{lin}(V_{GS}-V_{on})^{\alpha_{lin}}}}{\Delta L} \quad (4.6)$$

Equation 4.5 and 4.6 were derived by analytically differentiating the drain current equations of the model presented in 3.

The output resistance (r_o) can be calculated directly from the derivative of the measured I_{DS} versus V_{DS} , using Equation 2.34 for the drain current as the reference for this extraction.

$$r_o = \frac{dI_{DS}}{dV_{DS}} = -\frac{G_{0lin} W (B_1)^m ((B_1)^{-m} (B_2)^{-m} ((B_1)^m + (B_2)^m))^{-\frac{1}{m}} e^{k_{lin}(V_{GS}-V_{on})^{\alpha_{lin}}}}{((B_1)^m + (B_2)^m) (G_{0lin} W (2I_{DS}R_C - V_{DS}) e^{k_{lin}(V_{GS}-V_{on})^{\alpha_{lin}}} - I_{off}\Delta L)} \quad (4.7)$$

with

$$B_1 = \frac{G_{0sat} W (V_{GS} - V_{on}) e^{k_{sat}(V_{GS}-V_{on})^{\alpha_{sat}}} + I_{off}\Delta L}{\Delta L} \quad (4.8)$$

$$B_2 = -\frac{G_{0lin} W (2I_{DS}R_C - V_{DS}) e^{k_{lin}(V_{GS}-V_{on})^{\alpha_{lin}}} - I_{off}\Delta L}{\Delta L} \quad (4.9)$$

In adapting the small-signal model for TFTs, accurately determining parasitic capacitances such as overlap capacitances at the source (C_{OVS}) and drain (C_{OVD}), and the channel capacitance (C_{CH}), is crucial, as these elements dominate the device's frequency response and dynamic behavior.

Each overlap capacitance arises from the physical area where the gate electrode extends beyond the channel region and directly overlaps with the source or drain electrode, separated by the gate insulator. The values of these overlap capacitances can be evaluated using Equations 4.10 and 4.11 for gate-source and gate-drain capacitances, respectively.

$$C_{OVS} = \epsilon_{ox} \frac{W \cdot L_{OVS}}{t_{ox}} \quad (4.10)$$

$$C_{OVD} = \epsilon_{ox} \frac{W \cdot L_{OVD}}{t_{ox}} \quad (4.11)$$

Where ϵ_{ox} is the absolute permittivity of the gate insulator, W is the channel width, L_{OVS} , L_{OVD} are the overlap lengths of the gate over source and drain, respectively, and t_{ox} is the gate insulator thickness.

The channel capacitance is due to the gate's coupling to the channel region itself and is modeled as:

$$C_{CH} = \epsilon_{ox} \frac{W \cdot L_{CH}}{t_{ox}} \quad (4.12)$$

Where L_{CH} is the channel length. In practice, L_{CH} can often be approximated as $L - (L_{OVS} + L_{OVD})$.

The values of these capacitances can be practically extracted from capacitance–voltage (C–V) measurements, as illustrated by the typical C–V plot shown in Figure 4.4.

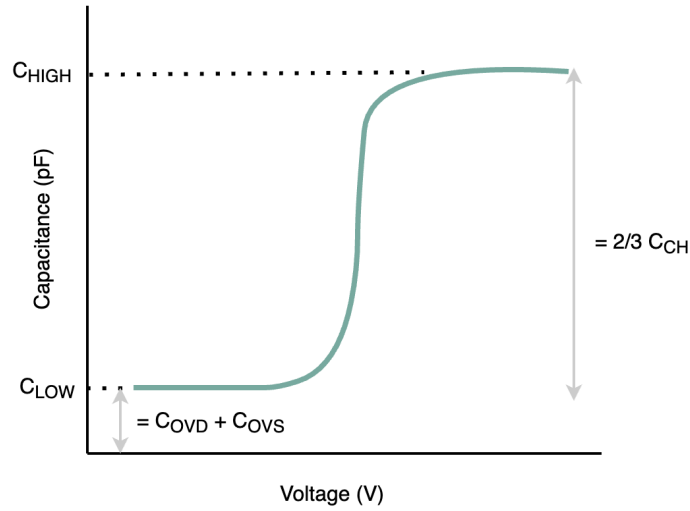


Figure 4.4: C–V characteristics illustrating the graphical extraction of C_{Low} , C_{High} , and C_{CH} .

At low gate voltage, where the channel is depleted or OFF, the measured capacitance stabilizes at a minimum value (C_{Low}). This value is dominated by the sum of the overlap capacitances between the gate-source and gate-drain electrodes.

$$C_{Low} = C_{OVD} + C_{OVS} \quad (4.13)$$

At high gate voltage, when a conductive channel forms, the capacitance increases and levels off at a higher plateau (C_{High}). This value now includes both the overlap capacitances and a fraction of the channel capacitance (C_{CH}).

$$C_{High} = C_{OVD} + C_{OVS} + \frac{2}{3} C_{CH} \quad (4.14)$$

By graphically measuring C_{Low} and C_{High} from the C–V curve, it is possible to directly calculate the channel capacitance using Equation 4.15.

$$C_{CH} = \frac{2}{3}(C_{High} - C_{Low}) \quad (4.15)$$

This procedure enables a straightforward, measurement-based extraction of the principal capacitances to be used in the small-signal TFT model.

4.2 Model Validation

The validation process employed a systematic approach utilizing Dataset 3, which provides experimental data for six distinct device geometries spanning channel widths of $W = 100 \mu\text{m}$ and $W = 50 \mu\text{m}$, with channel lengths ranging from $L = 5 \mu\text{m}$ to $L = 20 \mu\text{m}$. This diversity in device dimensions enables comprehensive assessment of the model's scalability and its ability to accurately capture the small-signal behavior across different aspect ratios and channel length modulation effects.

The validation methodology focuses on the accurate reproduction of transconductance characteristics, which represent the fundamental small-signal parameter governing the conversion efficiency between gate voltage variations and drain current changes. Both linear regime transconductance ($g_{m_{lin}}$) and saturation regime transconductance ($g_{m_{sat}}$) were evaluated to ensure comprehensive coverage of the device's operational envelope. For each device geometry, the extracted DC model parameters were utilized to calculate the theoretical transconductance values using the analytical expressions derived in 3.3.3. These calculated values were then compared against experimental measurements to assess the model's predictive accuracy and identify any systematic deviations.

Figures 4.5a–4.10a present the comparison between the modeled and measured data for $g_{m_{lin}}$, while Figures 4.5b–4.10b show the corresponding results for $g_{m_{sat}}$. In both cases, six plots are reported, one for each device geometry.

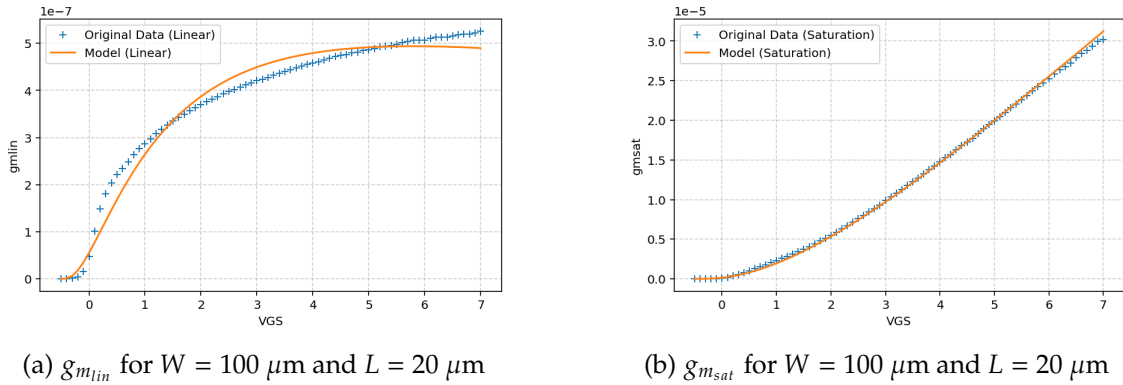
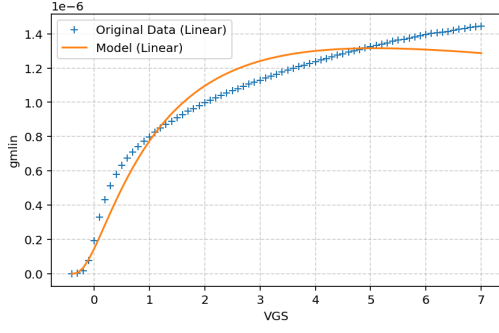
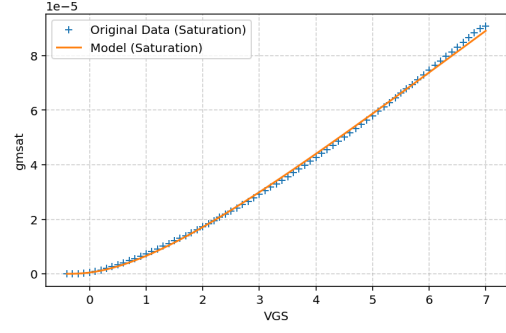
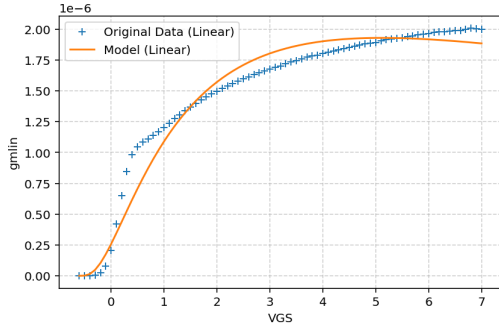
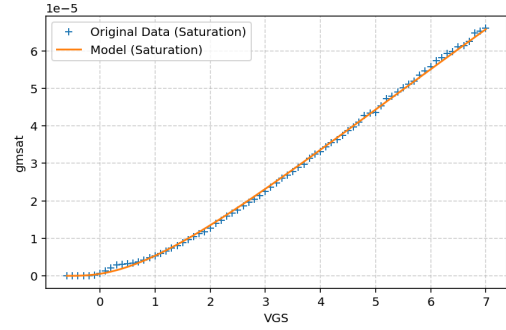
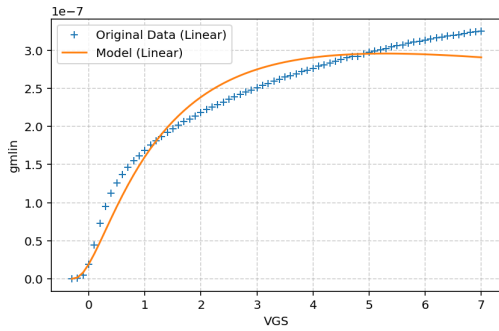
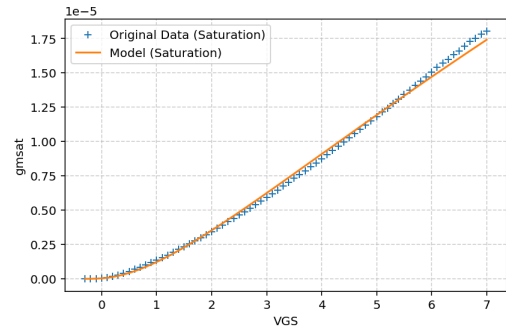


Figure 4.5: Comparison of measured data and modeled results for g_m with $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$.

(a) $g_{m_{lin}}$ for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$ (b) $g_{m_{sat}}$ for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$ Figure 4.6: Comparison of measured data and modeled results for g_m with $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$.(a) $g_{m_{lin}}$ for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$ (b) $g_{m_{sat}}$ for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$ Figure 4.7: Comparison of measured data and modeled results for g_m with $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$.(a) $g_{m_{lin}}$ for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$ (b) $g_{m_{sat}}$ for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$ Figure 4.8: Comparison of measured data and modeled results for g_m with $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$.

The comparison between modeled and measured transconductance in the linear regime, presented in 4.5a–4.10a reveals only moderate agreement, with systematic deviations that warrant careful consideration. Across all device geometries, the model captures the general $g_{m_{lin}}$ vs V_{GS} trend but increasingly underestimates the experimental g_m at higher gate voltages. The saturation regime transconductance comparison shows a

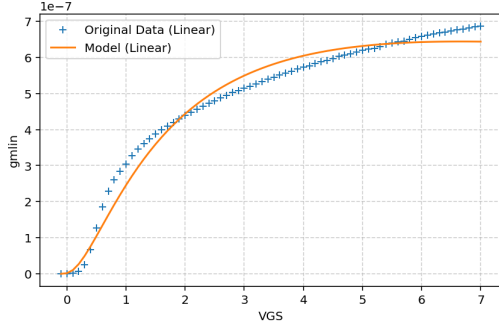
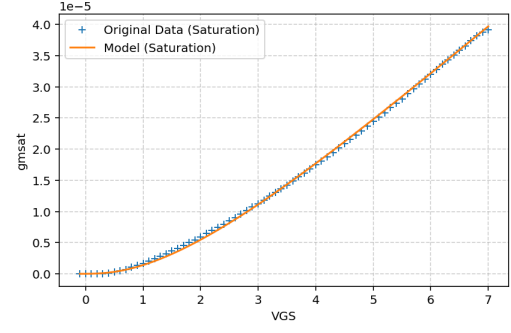

 (a) $g_{m_{lin}}$ for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$

 (b) $g_{m_{sat}}$ for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$

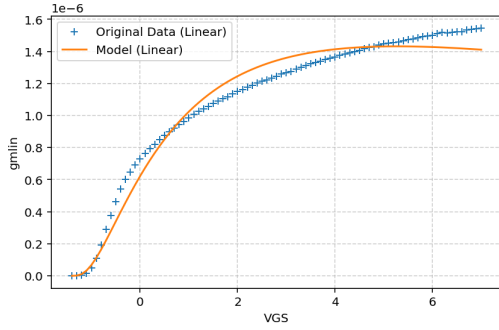
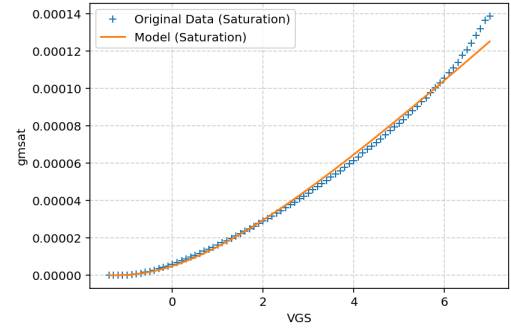
 Figure 4.9: Comparison of measured data and modeled results for g_m with $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$.

 (a) $g_{m_{lin}}$ for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$

 (b) $g_{m_{sat}}$ for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$

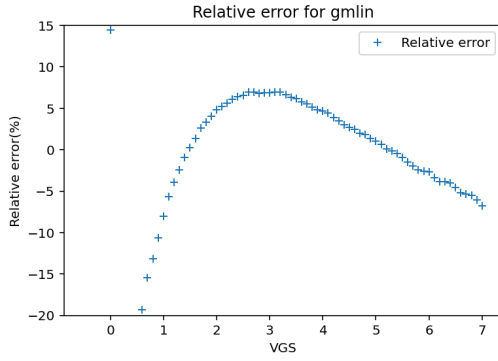
 Figure 4.10: Comparison of measured data and modeled results for g_m with $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$.

markedly closer match between model and experiment than in the linear regime. Across all six geometries, the model reproduces the $g_{m,sat}$ versus V_{GS} curves with minimal deviation. The linear dependence observed experimentally in this regime is accurately captured by the model.

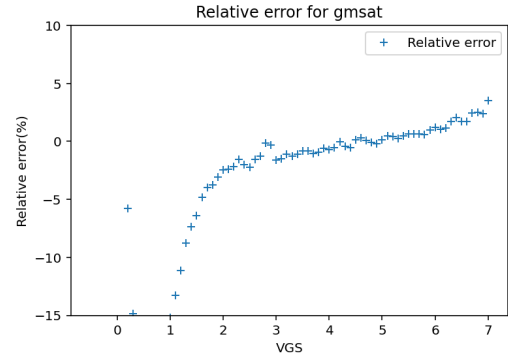
Overall, the model provides a reliable representation of the saturation-regime transconductance and captures the main trend of the linear-regime response, though with reduced accuracy at elevated gate voltages.

In addition to the direct comparison plots, Figures 4.11–4.16 display the relative error between modeled and experimental data for $g_{m_{lin}}$ and $g_{m_{sat}}$.

The analysis of the relative error in the linear regime transconductance reveals a consistent trend across all device geometries, the largest discrepancies occur near the turn-on region, where the model tends to underestimate the measured values. As the V_{GS} increases and the channel becomes fully formed, the error rapidly decreases and stabilizes at moderate levels. Shorter channel lengths generally exhibit slightly higher peak errors, while longer devices show improved accuracy once past the turn-on region. Similarly, narrower devices present somewhat larger deviations compared to their wider counterparts, although in all cases the relative error converges to within a few percent at

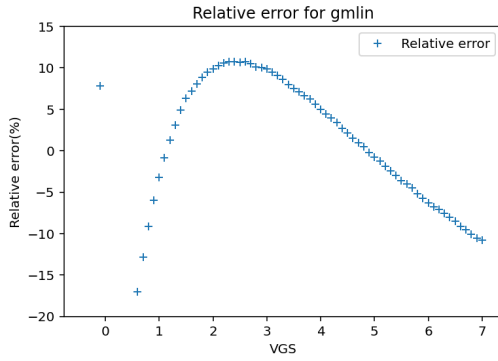


(a) Relative error of $g_{m_{lin}}$ for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$

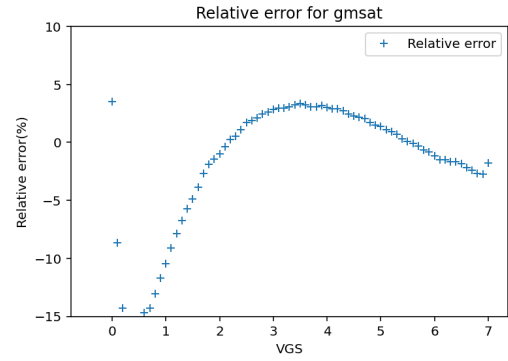


(b) Relative error of $g_{m_{sat}}$ for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$

Figure 4.11: Relative error of g_m with $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$.



(a) Relative error of $g_{m_{lin}}$ for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$



(b) Relative error of $g_{m_{sat}}$ for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$

Figure 4.12: Relative error of g_m with $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$.

high V_{GS} values. These results highlight that the model limitations are most pronounced during the onset of conduction, whereas its predictive capability improves significantly in the strong inversion regime.

In the saturation regime, the relative error remains tightly bounded across all geometries, confirming the robustness of the model under high V_{GS} values. As in the linear case, the largest deviations appear close to the turn-on region, but these quickly diminish as the V_{GS} increases. Beyond turn-on region, the error rapidly converges to within a few percent and stays remarkably stable over the full bias range. Longer channels generally yield slightly lower peak discrepancies, while narrower devices tend to show somewhat higher initial errors, yet in all cases the model maintains excellent predictive accuracy once the channel is well established. This consistency across dimensions highlights the reliability of the saturation regime parameterization and its suitability for capturing device behavior under strong inversion.

The extracted values of C_{OV} and C_{CH} for different channel widths and channel lengths are summarized in Table 4.1. These values were obtained based on Equations 4.10, 4.11, and 4.12, which describe the total gate capacitance as a function of the intrinsic channel

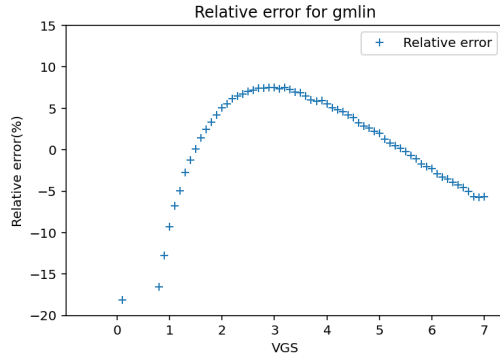
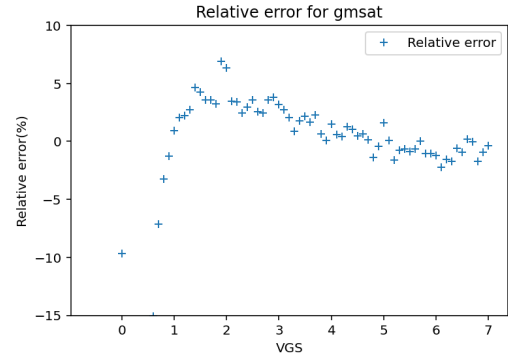

 (a) Relative error of $g_{m_{lin}}$ for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$

 (b) Relative error of $g_{m_{sat}}$ for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$

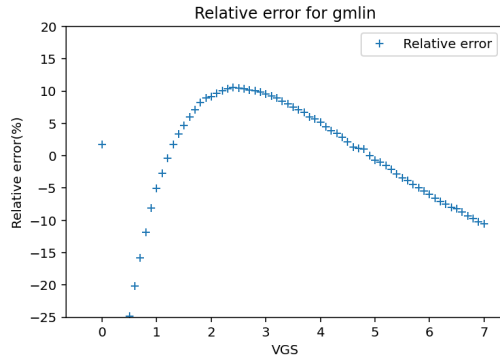
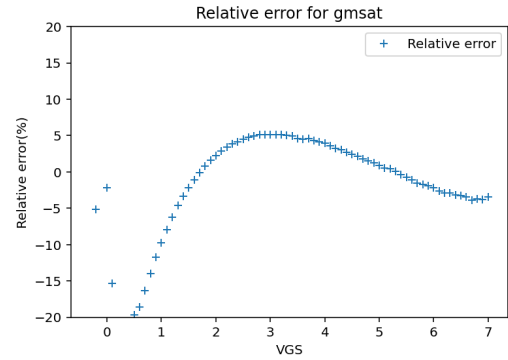
 Figure 4.13: Relative error of g_m with $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$.

 (a) Relative error of $g_{m_{lin}}$ for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$

 (b) Relative error of $g_{m_{sat}}$ for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$

 Figure 4.14: Relative error of g_m with $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$.

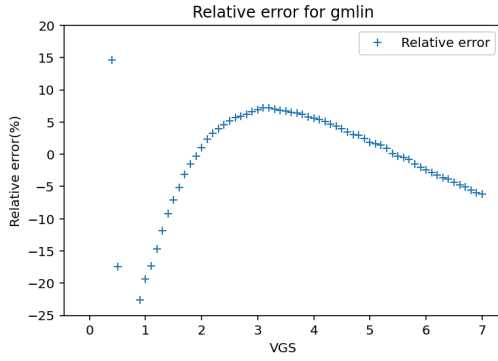
and overlap components.

For the calculation of the overlap capacitances, in the absence of layout information, the overlap lengths L_{OVS} and L_{OVD} were assumed to be equal to $\frac{L}{10}$, a commonly accepted approximation in such cases. As a result, the overlap source and drain capacitances were considered identical, and are hereafter represented by a single parameter C_{OV} .

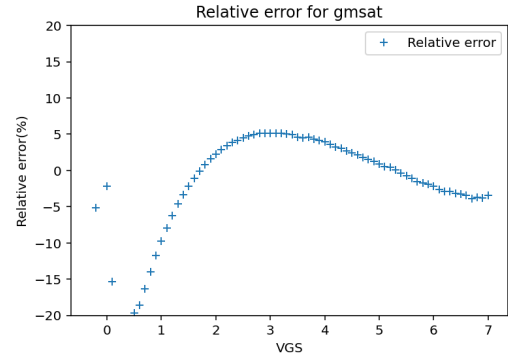
 Table 4.1: Extracted values of C_{OV} and C_{CH} for different W and L for IGZO TFTs.

$W (\mu\text{m})$	$L (\mu\text{m})$	$C_{OV} (\text{pF})$	$C_{CH} (\text{pF})$
100	5	0.017	0.138
	10	0.034	0.276
	20	0.069	0.552
50	5	0.009	0.069
	10	0.017	0.138
	20	0.034	0.276

The extracted parasitic capacitances fall squarely within the expected range for IGZO

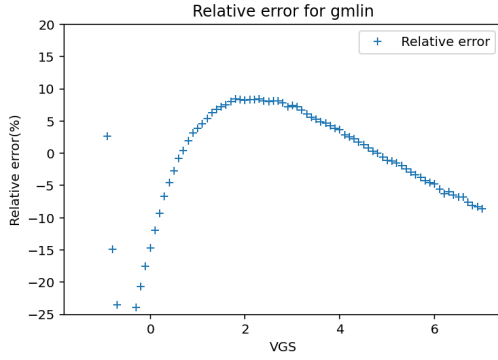


(a) Relative error of $g_{m_{lin}}$ for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$

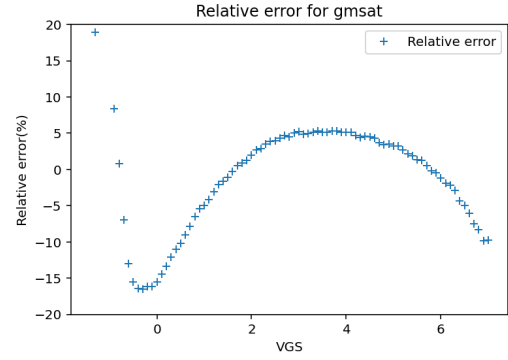


(b) Relative error of $g_{m_{sat}}$ for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$

Figure 4.15: Relative error of g_m with $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$.



(a) Relative error of $g_{m_{lin}}$ for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$



(b) Relative error of $g_{m_{sat}}$ for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$

Figure 4.16: Relative error of g_m with $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$.

TFT technology and thus validate the physical assumptions of our model. Both the overlap capacitance C_{OV} and the channel capacitance C_{CH} scale proportionally with device geometry, doubling approximately when either the channel length or width is doubled, which validates the extraction methodology. The absolute values are in line with typical ranges reported for this technology. Furthermore, the approximation of setting L_{OV} to 10% of the channel length provides good agreement. Consequently, these capacitance values provide a solid foundation for precise frequency-domain predictions and circuit simulations of IGZO TFTs.

Although direct C-V measurements were not available, the adopted approximation yielded results that align with theoretical expectations and are suitable for small-signal modeling.

4.2.1 Verilog-A Model Implementation

In this section, the compact IGZO TFT model developed for the DC operation is extended to include the intrinsic and parasitic capacitances required for accurate small-signal and

AC circuit simulations. The goal is to provide a robust behavioral description suitable for circuit simulation.

The Verilog-A module presented in Appendix F implements a three-terminal IGZO TFT (drain (d), gate (g), and source (s)) with configurable device parameters such as channel width (W), channel length (L), oxide relative permittivity (ϵ_{ox}), and oxide thickness (t_{ox}). The model incorporates scalable analytical functions for key parameters including turn-on voltage, alpha coefficients, kappa values, G_0 parameters, and off-currents, enabling flexible adaptation across different device geometries and process variations.

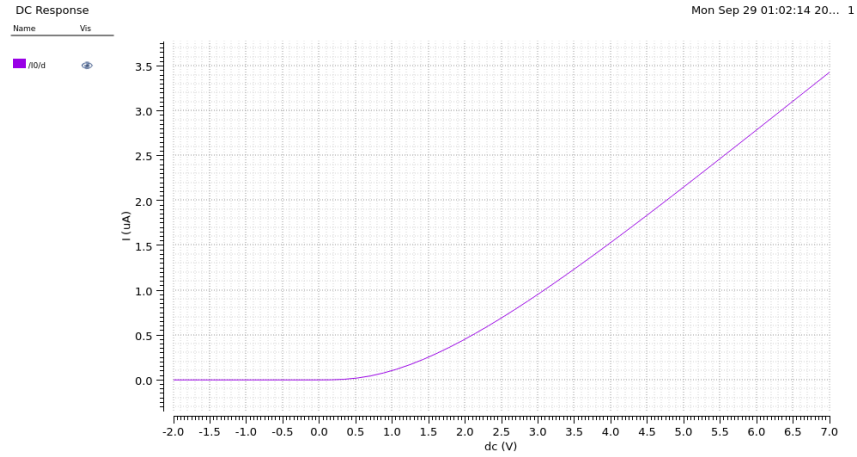
Dedicated analog functions encode the turn on voltage, and other fitting parameters extracted from the DC characteristics. These functions allow flexible adaptation of the model to process or geometry variations.

The capacitance modeling includes three critical components: overlap charges for gate-source and gate-drain terminals, and channel charge, computed based on the theoretical framework established in Equations 4.10, 4.11, and 4.12. The drain current calculation employs the unified approach described in 3.4.1, using a generalized smoothing expression to seamlessly transition between linear and saturation operating regimes.

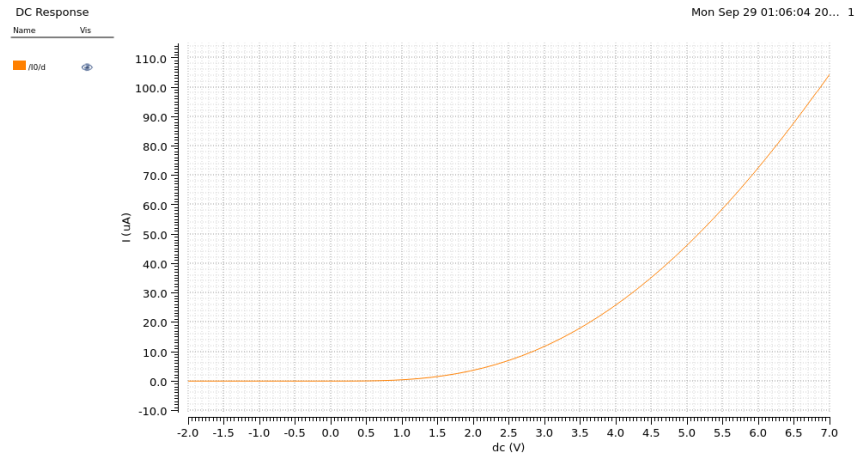
To confirm the accuracy and practical applicability of the developed IGZO TFT compact model, it was integrated into Cadence Virtuoso for circuit-level simulation. A test circuit was designed incorporating the IGZO TFT model to evaluate its behavior under typical operating conditions. The validation demonstrates excellent agreement between the Verilog-A simulation results (Figure 4.17) and experimental measurements (Figure 4.18) for a device with $W = 50\mu\text{m}$ and $L = 10\mu\text{m}$.

Both figures show transfer characteristics in linear and saturation regions, revealing excellent validation results where the Verilog-A model accurately reproduces the experimental current levels across the entire gate voltage range, with both linear and saturation curves showing nearly identical magnitudes. The model successfully captures the smooth transition from off-state to on-state operation.

The successful circuit-level validation in Cadence confirms the model's practical applicability for IGZO TFT circuit design and simulation. This implementation provides a robust foundation for integrating IGZO TFTs into PDKs, thereby facilitating more efficient electronic design workflows and enabling accurate performance prediction in practical circuit applications.



(a) Verilog-A transfer characteristic (I_D vs V_{GS}) for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$ in the linear region



(b) Verilog-A transfer characteristic (I_D vs V_{GS}) for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$ in the saturation region

Figure 4.17: Verilog-A transfer characteristic (I_D vs V_{GS}) for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.

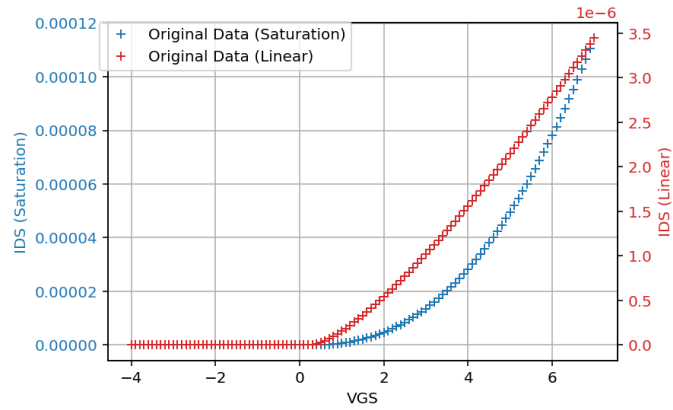


Figure 4.18: Experimental transfer characteristics for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.

CONCLUSION

This work has successfully developed and validated a compact, physics-based model for IGZO thin-film transistors. The main objectives were to formulate a unified drain-current model, based on CAMCAS, and to implement an automated parameter extraction procedure using measured data from devices with varying geometries. The proposed model accurately reproduces the transfer characteristics in both the linear and saturation regimes, with simulated currents closely matching experimental measurements, typically within a few percent error across most of the bias range. The study of the scalability of the model with respect to both channel width and length has been demonstrated by fitting the model parameters to expressions that capture their dependence on device geometry, thereby enabling prediction of device behavior for arbitrary geometries within the studied range. This compact model provides a unified framework that can predict IGZO-TFT behavior across different channel sizes while remaining computationally efficient for circuit simulation.

The model was implemented in Verilog-A and integrated into a circuit simulator to verify its practical applicability. A representative test circuit using a IGZO-TFT with $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$ demonstrated close agreement between simulation and measurement, with the transfer characteristics in both operating regimes showing nearly identical behavior. This Verilog-A implementation confirms that this model can be embedded in PDKs for IGZO technology, enabling designers to simulate complex circuits with realistic device behavior.

In addition to DC operation, a small-signal equivalent model was derived to support AC analysis. The computed transconductances were compared to measured values for multiple geometries. The results show that the saturation-region transconductance is reproduced with accuracy. However, in the linear regime, the model correctly predicts the general trend of $g_{m,\text{lin}}$ vs V_{GS} , although the error is larger near the turn-on voltage.

Despite these successes, some limitations remain. The automated extraction assumes uniform, well-behaved device data, but any irregularities (fabrication variations, measurement noise) can distort the fit. In this work, care was taken to select consistent data sets, but as noted in Chapter 3, experimental variations make it difficult to infer universal parameter

trends. In practice, maintaining model accuracy will require careful data validation and explicit consideration of process variations.

This thesis has met its objectives by developing a scalable compact model for IGZO TFTs and validating it across devices with different channel lengths and widths. The model demonstrates consistent scalability and accuracy in both linear and saturation regimes. Its Verilog-A implementation and successful circuit-level testing confirm that the model is suitable for integration into design flows for flexible electronics.

In addition to these results, several promising directions remain open for future development. A natural continuation is the full incorporation of the Verilog-A implementation into complete process design kits, enabling broader dissemination and adoption by circuit designers. Further enhancement of the physical description of the device is also desirable. Although the current model reproduces DC behavior with high accuracy, extending it to include bias-stress effects, temperature dependence, and charge-trapping mechanisms would improve its predictive capability under long-term and high-stress operating conditions.

The parameter-extraction methodology can also be refined. While the automated extraction process used in this thesis has proven effective, future work may explore advanced optimization techniques and the use of larger and more diverse datasets to obtain more precise geometry-dependent expressions.

By pursuing these directions, the compact model developed here can evolve into a more complete and versatile tool, supporting the reliable integration of IGZO TFTs into next-generation electronic systems and strengthening the link between device physics and practical circuit design.

BIBLIOGRAPHY

- [1] J. M. Lourenço. *The NOVAthesis L^AT_EX Template User's Manual*. NOVA University Lisbon. 2021. URL: <https://github.com/joaomlourenco/novathesis/raw/main/template.pdf>.
- [2] D. Corzo, G. Tostado, and D. Baran. "Flexible Electronics: Status, Challenges and Opportunities". In: *Frontiers in Electronics* 1 (2020-09), p. 594003. DOI: [10.3389/felec.2020.594003](https://doi.org/10.3389/felec.2020.594003).
- [3] R.-H. Horng. "Thin Film Transistor". In: *Crystals* 9.8 (2019). ISSN: 2073-4352. DOI: [10.3390/cryst9080415](https://doi.org/10.3390/cryst9080415). URL: <https://www.mdpi.com/2073-4352/9/8/415>.
- [4] M. Hussain and N. El-Atab, eds. *Handbook of Flexible and Stretchable Electronics*. 1st. CRC Press, 2019. DOI: [10.1201/b22262](https://doi.org/10.1201/b22262).
- [5] M. Simicic et al. "ESD study on a-IGZO TFT device architectures". In: *2018 40th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)*. 2018, pp. 1–7. DOI: [10.23919/EOS/ESD.2018.8509748](https://doi.org/10.23919/EOS/ESD.2018.8509748).
- [6] C. Ma et al. "IGZO-TFT-PDK: Thin-Film Flexible Electronics Design Kit, Standard Cell and Design Methodology". In: *IEEE Open Journal of Circuits and Systems* 2 (2021), pp. 757–765. DOI: [10.1109/OJCAS.2021.3123396](https://doi.org/10.1109/OJCAS.2021.3123396).
- [7] L. Shao et al. "Process design kit for flexible hybrid electronics". In: *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*. 2018, pp. 651–657. DOI: [10.1109/ASPDAC.2018.8297396](https://doi.org/10.1109/ASPDAC.2018.8297396).
- [8] H. He et al. "Trapped-Charge-Effect-Based Above-Threshold Current Expressions for Amorphous Silicon TFTs Consistent With Pao–Sah Model". In: *IEEE Transactions on Electron Devices* 61.11 (2014), pp. 3744–3750. DOI: [10.1109/TED.2014.2358619](https://doi.org/10.1109/TED.2014.2358619).
- [9] Y. W. Jeon et al. "Subgap Density-of-States-Based Amorphous Oxide Thin Film Transistor Simulator (DeAOTS)". In: *IEEE Transactions on Electron Devices* 57.11 (2010), pp. 2988–3000. DOI: [10.1109/TED.2010.2072926](https://doi.org/10.1109/TED.2010.2072926).
- [10] O. Heil. *Improvements in or relating to electrical amplifiers and other control arrangements and devices*. UK Patent GB439457A. Filed: 1934-03-02, Granted: 1935-12-06. 1935-12.

-
- [11] J. E. Lilienfeld. *Method and apparatus for controlling electric currents*. U.S. Patent 1,745,175. 1930-01.
- [12] J. E. Lilienfeld. *Amplifier for electric currents*. U.S. Patent 1,877,140. 1932-09.
- [13] J. E. Lilienfeld. *Device for controlling electric current*. U.S. Patent 1,900,018. 1933-03.
- [14] P. K. Weimer. "Proceedings of the Institute of Radio Engineers". In: *Proceedings of the Institute of Radio Engineers* 50 (1962), p. 1462.
- [15] P. K. Weimer. "The TFT A New Thin-Film Transistor". In: *Proceedings of the IRE* 50.6 (1962), pp. 1462–1469. DOI: [10.1109/JRPROC.1962.288190](https://doi.org/10.1109/JRPROC.1962.288190).
- [16] G. Boesen and J. Jacobs. "ZnO field-effect transistor". In: *Proceedings of the IEEE* 56.11 (1968), pp. 2094–2095. DOI: [10.1109/PROC.1968.6813](https://doi.org/10.1109/PROC.1968.6813).
- [17] A. Aoki and H. Sasakura. "Tin Oxide Thin Film Transistors". In: *Japanese Journal of Applied Physics* 9.5 (1970), p. 582. DOI: [10.1143/JJAP.9.582](https://doi.org/10.1143/JJAP.9.582). URL: <https://dx.doi.org/10.1143/JJAP.9.582>.
- [18] S. Kugler and K. Shimakawa. "Amorphous Semiconductors: Excerpt". In: *Amorphous Semiconductors*. Cambridge University Press, 2015. ISBN: 9781107019348. URL: https://assets.cambridge.org/9781107019348/excerpt/9781107019348_excerpt.pdf?cv=1.
- [19] P. le Comber, W. Spear, and A. Ghaith. "Amorphous-silicon field-effect device and possible application". In: *Electronics Letters* 15 (6 1979), pp. 179–181. DOI: [10.1049/el:19790126](https://doi.org/10.1049/el:19790126). eprint: <https://digital-library.theiet.org/doi/pdf/10.1049/el%3A19790126>. URL: <https://digital-library.theiet.org/doi/abs/10.1049/el%3A19790126>.
- [20] E. Fortunato, P. Barquinha, and R. Martins. "ChemInform Abstract: Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances". In: *Advanced materials (Deerfield Beach, Fla.)* 24 (2012-08), pp. 2945–86. DOI: [10.1002/adma.201103228](https://doi.org/10.1002/adma.201103228).
- [21] Y. Kuo. "Thin Film Transistor Technology—Past, Present, and Future". In: *The Electrochemical Society Interface* 22.1 (2013), p. 55. DOI: [10.1149/2.F06131if](https://doi.org/10.1149/2.F06131if). URL: <https://dx.doi.org/10.1149/2.F06131if>.
- [22] K. Nomura et al. "Thin-Film Transistor Fabricated in Single-Crystalline Transparent Oxide Semiconductor". In: *Science (New York, N.Y.)* 300 (2003-06), pp. 1269–72. DOI: [10.1126/science.1083212](https://doi.org/10.1126/science.1083212).
- [23] K. Nomura et al. "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors". In: *Nature* 432.7016 (2004), pp. 488–492. DOI: [10.1038/nature03090](https://doi.org/10.1038/nature03090). URL: <https://doi.org/10.1038/nature03090>.

- [24] B. K. Yap et al. "Recent advances of In₂O₃-based thin-film transistors: A review". In: *Applied Surface Science Advances* 16 (2023), p. 100423. ISSN: 2666-5239. DOI: <https://doi.org/10.1016/j.apsadv.2023.100423>. URL: <https://www.sciencedirect.com/science/article/pii/S2666523923000582>.
- [25] G. Lee et al. "High performance, transparent a-IGZO TFTs on a flexible thin glass substrate". In: *Semiconductor Science and Technology* 29.3 (2014), p. 035003. DOI: [10.1088/0268-1242/29/3/035003](https://doi.org/10.1088/0268-1242/29/3/035003).
- [26] M. Mativenga et al. "Fully Transparent and Rollable Electronics". In: *ACS Applied Materials & Interfaces* 7.3 (2015). PMID: 25526282, pp. 1578–1585. DOI: [10.1021/am506937s](https://doi.org/10.1021/am506937s). eprint: <https://doi.org/10.1021/am506937s>. URL: <https://doi.org/10.1021/am506937s>.
- [27] J. Yoon et al. "Deep-ultraviolet sensing characteristics of transparent and flexible IGZO thin film transistors". In: *Journal of Alloys and Compounds* 817 (2020), p. 152788. ISSN: 0925-8388. DOI: <https://doi.org/10.1016/j.jallcom.2019.152788>. URL: <https://www.sciencedirect.com/science/article/pii/S0925838819340344>.
- [28] S. R. Bhalerao, D. Lupo, and P. R. Berger. "Flexible Thin Film Transistor (TFT) and Circuits for Internet of Things (IoT) based on Solution Processed Indium Gallium Zinc Oxide (IGZO)". In: *2021 IEEE International Flexible Electronics Technology Conference (IFETC 2021)*. Vol. no. Di. IEEE, 2021, pp. 23–25. DOI: [10.1109/IFETC49530.2021.9580506](https://doi.org/10.1109/IFETC49530.2021.9580506).
- [29] H. Ning et al. "Transparent Flexible IGZO Thin Film Transistors Fabricated at Room Temperature". In: *Membranes* 12.1 (2022). ISSN: 2077-0375. DOI: [10.3390/membranes12010029](https://doi.org/10.3390/membranes12010029). URL: <https://www.mdpi.com/2077-0375/12/1/29>.
- [30] P. Wellenius, L. Lunardi, and J. Muth. "Transparent IGZO-based logic gates". In: *Ieee Electron Device Letters* 33 (2012-05), pp. 673–675. DOI: [10.1109/LED.2012.2186784](https://doi.org/10.1109/LED.2012.2186784).
- [31] F. Catania et al. "AC Performance of Flexible Transparent InGaZnO Thin-Film Transistors and Circuits". In: *IEEE Transactions on Electron Devices* 69 (2022-09), pp. 1–6. DOI: [10.1109/TED.2022.3193012](https://doi.org/10.1109/TED.2022.3193012).
- [32] V. Kumar, K. Behrman, and I. Kymissis. "Putting microLED technology on display". In: *Physics Today* 77.6 (2024-06), pp. 30–36. ISSN: 0031-9228. DOI: [10.1063/pt.bmot.fjtv](https://doi.org/10.1063/pt.bmot.fjtv). eprint: https://pubs.aip.org/physicstoday/article-pdf/77/6/30/20086332/30_1_pt.bmot.fjtv.pdf. URL: <https://doi.org/10.1063/pt.bmot.fjtv>.
- [33] C. Almeida and M. H. Fino. "Fully Automatic Evaluation of IGZO-TFT Model Parameters". In: *2025 9th International Young Engineers Forum on Electrical and Computer Engineering (YEF-ECE)*. 2025, pp. 169–174. DOI: [10.1109/YEF-ECE66503.2025.11117522](https://doi.org/10.1109/YEF-ECE66503.2025.11117522).

-
- [34] N. Lu et al. "A Review for Compact Model of Thin-Film Transistors (TFTs)". In: *Micromachines* 9.11 (2018). ISSN: 2072-666X. DOI: [10.3390/mi9110599](https://doi.org/10.3390/mi9110599). URL: <https://www.mdpi.com/2072-666X/9/11/599>.
- [35] X. Cheng et al. "TFT Compact Modeling". In: *Journal of Display Technology* 12.9 (2016), pp. 898–906. DOI: [10.1109/JDT.2016.2556980](https://doi.org/10.1109/JDT.2016.2556980).
- [36] W. Shockley. "A Unipolar "Field-Effect" Transistor". In: *Proceedings of the IRE* 40.11 (1952), pp. 1365–1376. DOI: [10.1109/JRPROC.1952.273964](https://doi.org/10.1109/JRPROC.1952.273964).
- [37] G. E. Moore. "Cramming more components onto integrated circuits, Reprinted from *Electronics*, volume 38, number 8, April 19, 1965, pp.114 ff." In: *IEEE Solid-State Circuits Society Newsletter* 11.3 (2006), pp. 33–35. DOI: [10.1109/N-SSC.2006.4785860](https://doi.org/10.1109/N-SSC.2006.4785860).
- [38] T. Sakurai and A. Newton. "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas". In: *IEEE Journal of Solid-State Circuits* 25.2 (1990), pp. 584–594. DOI: [10.1109/4.52187](https://doi.org/10.1109/4.52187).
- [39] M. H. Fino. "NMOS symmetric load ring VCOs modeling for submicron technologies". In: *Proceedings of SPIE - The International Society for Optical Engineering* 5837 (2005-06). DOI: [10.1117/12.608305](https://doi.org/10.1117/12.608305).
- [40] M. H. Fino. "A simple submicron MOSFET model and its application to the analytical characterization of analog circuits". In: vol. 1. 2005-01, I/115 –I/118 vol. 1. ISBN: 0-7803-9066-0. DOI: [10.1109/ECCTD.2005.1522923](https://doi.org/10.1109/ECCTD.2005.1522923).
- [41] T. Sakurai and A. Newton. "A simple MOSFET model for circuit analysis". In: *IEEE Transactions on Electron Devices* 38.4 (1991), pp. 887–894. DOI: [10.1109/16.75219](https://doi.org/10.1109/16.75219).
- [42] C. C. Enz, F. Krummenacher, and E. A. Vittoz. "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications". In: *Analog Integrated Circuits and Signal Processing* 8.1 (1995), pp. 83–114. DOI: [10.1007/BF01239381](https://doi.org/10.1007/BF01239381).
- [43] G. Machado, C. Enz, and M. Bucher. "Estimating Key Parameters in the EKV MOST Model for Analogue Design and Simulation". In: *Proceedings of the 1995 IEEE International Symposium on Circuits and Systems (ISCAS)*. Vol. 3. IEEE, 1995, pp. 1588–1591. DOI: [10.1109/ISCAS.1995.523456](https://doi.org/10.1109/ISCAS.1995.523456).
- [44] C. C. Enz. "A Short Story of the EKV MOS Transistor Model". In: *IEEE Solid-State Circuits Society Newsletter* 13.3 (2008), pp. 24–30. DOI: [10.1109/N-SSC.2008.4785778](https://doi.org/10.1109/N-SSC.2008.4785778).
- [45] M. Bucher et al. "EKV 3.0: An Analog Design-Oriented MOS Transistor Model". In: *2002 9th International Conference on Electronics, Circuits and Systems (ICECS)*. Vol. 2. IEEE, 2002, pp. 735–738. DOI: [10.1109/ICECS.2002.1046267](https://doi.org/10.1109/ICECS.2002.1046267).

- [46] A. Bazigos et al. *EKV3 MOSFET Compact Model Documentation, Model Version 301.02*. Technical Report. Ecole Polytechnique Fédérale de Lausanne (EPFL) and Technical University of Crete, 2008-01.
- [47] J.-K. Bremer, T. Peikert, and W. Mathis. “Analytical inversion-mode varactor modeling based on the EKV model and its application to RF VCO design”. In: *Proceedings of the 17th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2010*. 2010, pp. 64–69.
- [48] M. Shur et al. “SPICE Models for Amorphous Silicon and Polysilicon Thin Film Transistors”. In: *Journal of The Electrochemical Society* 144 (1997-08), pp. 2833–2839. DOI: [10.1149/1.1837903](https://doi.org/10.1149/1.1837903).
- [49] R. Shabanpour et al. “A transistor model for a-IGZO TFT circuit design built upon the RPI-aTFT model”. In: *2017 15th IEEE International New Circuits and Systems Conference (NEWCAS)*. 2017, pp. 129–132. DOI: [10.1109/NEWCAS.2017.8010122](https://doi.org/10.1109/NEWCAS.2017.8010122).
- [50] N. Munzenrieder, K. H. Cherenack, and G. Troster. “The Effects of Mechanical Bending and Illumination on the Performance of Flexible IGZO TFTs”. In: *IEEE Transactions on Electron Devices* 58.7 (2011), pp. 2041–2048. DOI: [10.1109/TED.2011.2143416](https://doi.org/10.1109/TED.2011.2143416).
- [51] R. Rodriguez-Davila et al. “A New Integration-Based Procedure to Extract the Threshold Voltage, the Mobility Enhancement Factor, and the Series Resistance of Thin-Film MOSFETs”. In: *IEEE Transactions on Electron Devices* 66.7 (2019), pp. 2979–2985. DOI: [10.1109/TED.2019.2913699](https://doi.org/10.1109/TED.2019.2913699).
- [52] A. Paterson and T. Anthopoulos. “Enabling thin-film transistor technologies and the device metrics that matter”. In: *Nature Communications* 9 (2018-12). DOI: [10.1038/s41467-018-07424-2](https://doi.org/10.1038/s41467-018-07424-2).
- [53] P. Servati, D. Striakhilev, and A. Nathan. “Above-threshold parameter extraction and modeling for amorphous silicon thin-film transistors”. In: *IEEE Transactions on Electron Devices* 50.11 (2003), pp. 2227–2235. DOI: [10.1109/TED.2003.818156](https://doi.org/10.1109/TED.2003.818156).
- [54] A. Cerdeira et al. “New procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions”. In: *Solid-State Electronics* 45.7 (2001), pp. 1077–1080. ISSN: 0038-1101. DOI: [https://doi.org/10.1016/S0038-1101\(01\)00143-5](https://doi.org/10.1016/S0038-1101(01)00143-5). URL: <https://www.sciencedirect.com/science/article/pii/S0038110101001435>.
- [55] M. H. Fino. “Optimization-based Determination of TFT Contact Resistances in Python”. In: *2022 29th International Conference on Mixed Design of Integrated Circuits and System (MIXDES)*. 2022, pp. 57–60. DOI: [10.23919/MIXDES55591.2022.9837978](https://doi.org/10.23919/MIXDES55591.2022.9837978).

- [56] S. Lee et al. "Unified Analytic Model for Current–Voltage Behavior in Amorphous Oxide Semiconductor TFTs". In: *Electron Device Letters, IEEE* 35 (2014-01), pp. 84–86. DOI: [10.1109/LED.2013.2290532](https://doi.org/10.1109/LED.2013.2290532).
- [57] Accellera Systems Initiative. *Verilog-AMS Language Reference Manual*. Version Standard 2.4.0. 2014. URL: <https://images.accellera.org/downloads/standards/vams/VAMS-LRM-2-4.pdf>.
- [58] X. Cheng, S. Lee, and A. Nathan. "TFT Small Signal Model and Analysis". In: *IEEE Electron Device Letters* 37.7 (2016), pp. 890–893. DOI: [10.1109/LED.2016.2575924](https://doi.org/10.1109/LED.2016.2575924).
- [59] R. Vatsyayan and S. A. Dayeh. "A Comprehensive Large Signal, Small Signal, and Noise Model for IGZO Thin Film Transistor Circuits". In: *IEEE Transactions on Electron Devices* 70.9 (2023), pp. 4647–4654. DOI: [10.1109/TED.2023.3284803](https://doi.org/10.1109/TED.2023.3284803).

TRANSFER CHARACTERISTICS DATASET 1

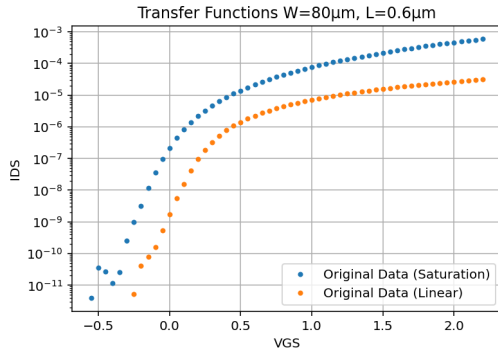
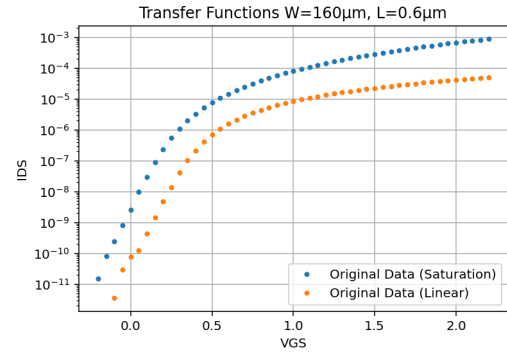
(a) $W = 80 \mu\text{m}$, $L = 0.6 \mu\text{m}$ (b) $W = 160 \mu\text{m}$, $L = 0.6 \mu\text{m}$

Figure A.1: Experimental transfer characteristics for devices with $L = 0.6 \mu\text{m}$ and widths $W = 80$ and $160 \mu\text{m}$.

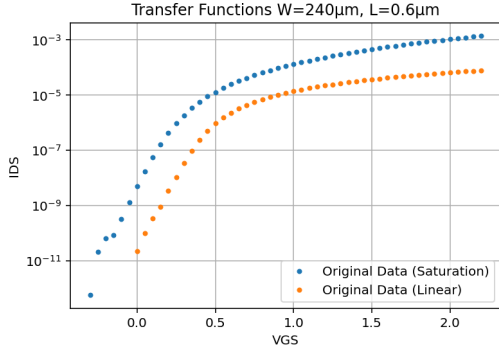
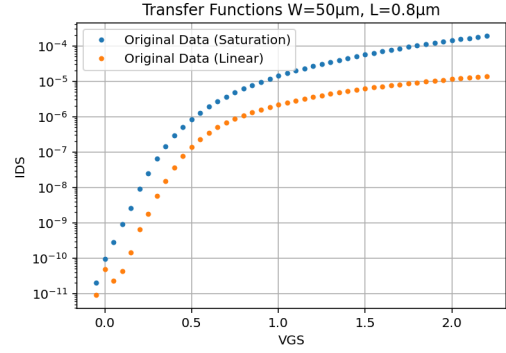
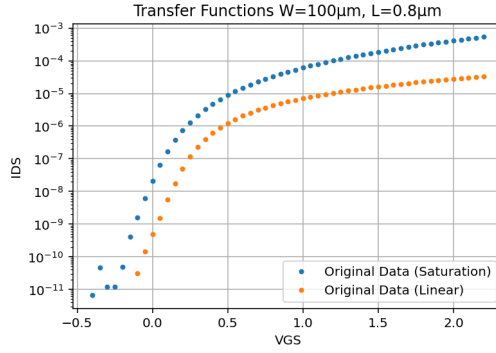

 (a) $W = 240 \mu\text{m}$, $L = 0.6 \mu\text{m}$

 (b) $W = 50 \mu\text{m}$, $L = 0.8 \mu\text{m}$

 (c) $W = 100 \mu\text{m}$, $L = 0.8 \mu\text{m}$

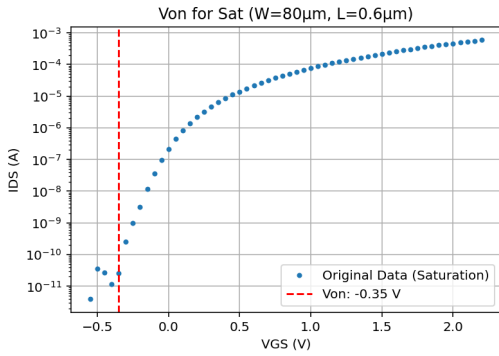
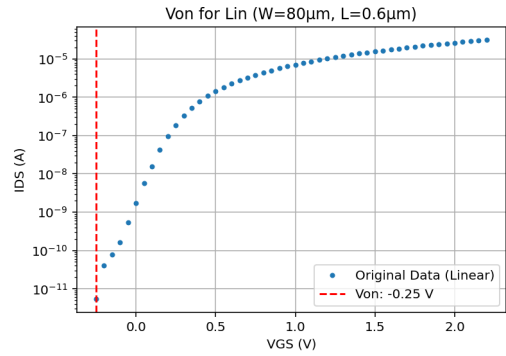
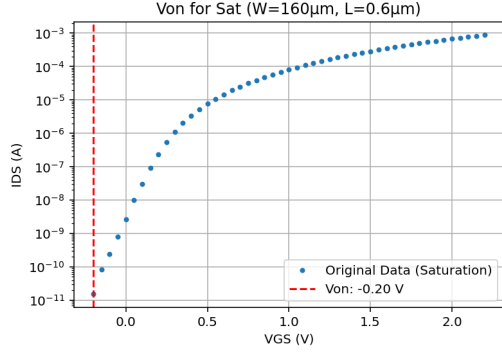
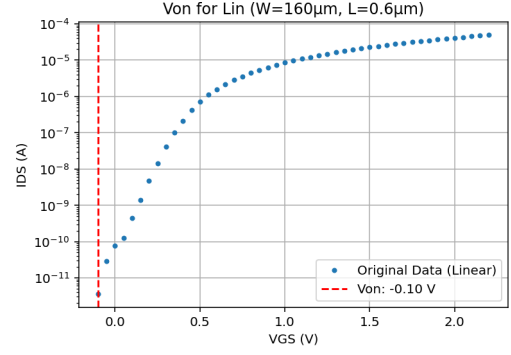
 Figure A.2: Experimental transfer characteristics for devices with $L = 0.6$ and $0.8 \mu\text{m}$. Top row: $W = 240 \mu\text{m}$ ($L = 0.6$) and $W = 50 \mu\text{m}$ ($L = 0.8$). Bottom row: $W = 100 \mu\text{m}$ ($L = 0.8$).

 (a) Experimental transfer characteristic (I_D vs V_{GS}) with V_{on} marked for $W = 80 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ in the saturation region

 (b) Experimental transfer characteristic (I_D vs V_{GS}) with V_{on} marked for $W = 80 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ in the linear region

 Figure A.3: Experimental transfer characteristics for $W = 80 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ with V_{on} marked in both linear and saturation regions.

APPENDIX A. TRANSFER CHARACTERISTICS DATASET 1

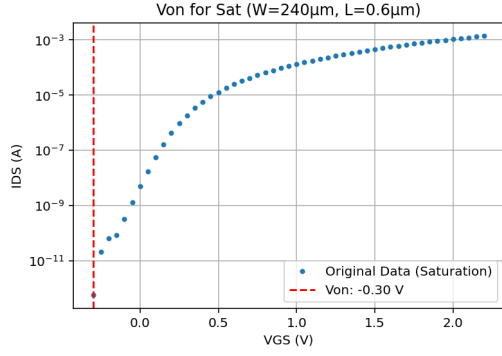


(a) Experimental transfer characteristic (I_D vs V_{GS}) with V_{on} marked for $W = 160 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ in the saturation region

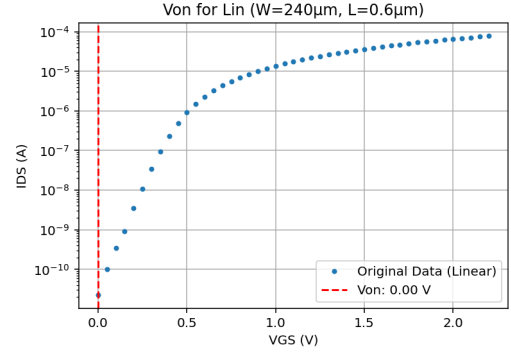


(b) Experimental transfer characteristic (I_D vs V_{GS}) with V_{on} marked for $W = 160 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ in the linear region

Figure A.4: Experimental transfer characteristics with V_{on} marked for $W = 160 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ in both linear and saturation regions.

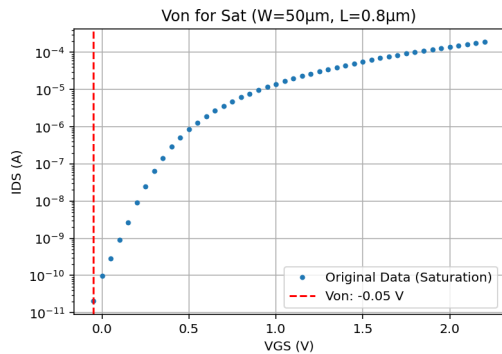


(a) Experimental transfer characteristic (I_D vs V_{GS}) with V_{on} marked for $W = 240 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ in the saturation region

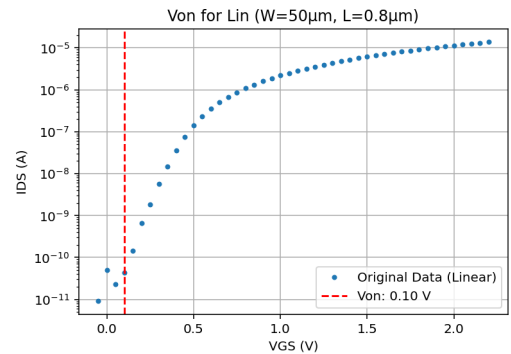


(b) Experimental transfer characteristic (I_D vs V_{GS}) with V_{on} marked for $W = 240 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ in the linear region

Figure A.5: Experimental transfer characteristics with V_{on} marked for $W = 240 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ in both linear and saturation regions.

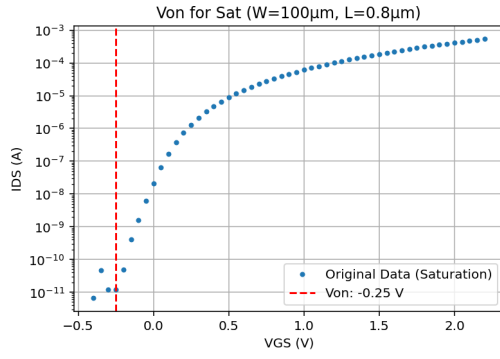


(a) Experimental transfer characteristic (I_D vs V_{GS}) with V_{on} marked for $W = 50 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ in the saturation region

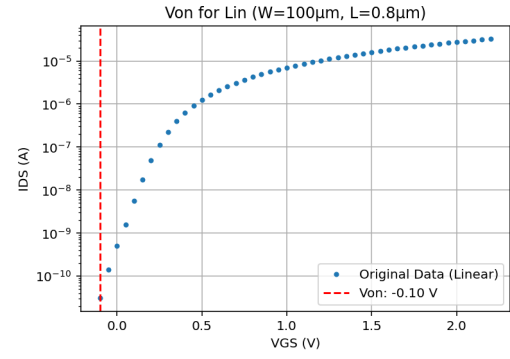


(b) Experimental transfer characteristic (I_D vs V_{GS}) with V_{on} marked for $W = 50 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ in the linear region

Figure A.6: Experimental transfer characteristics with V_{on} marked for $W = 50 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ in both linear and saturation regions.



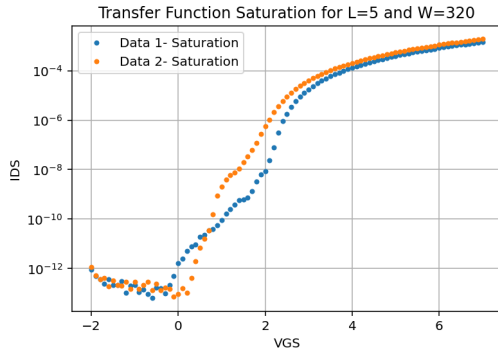
(a) Experimental transfer characteristic (I_D vs V_{GS}) with V_{on} marked for $W = 100 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ in the saturation region



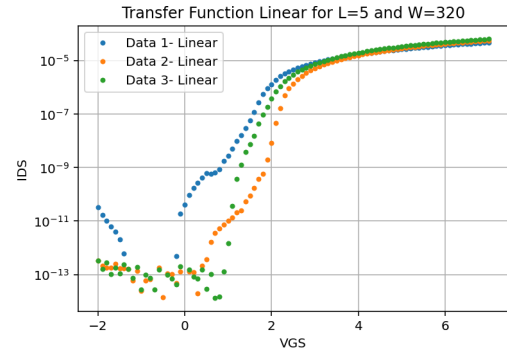
(b) Experimental transfer characteristic (I_D vs V_{GS}) with V_{on} marked for $W = 100 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ in the linear region

Figure A.7: Experimental transfer characteristics with V_{on} marked for $W = 100 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ in both linear and saturation regions.

TRANSFER CHARACTERISTICS DATASET 2

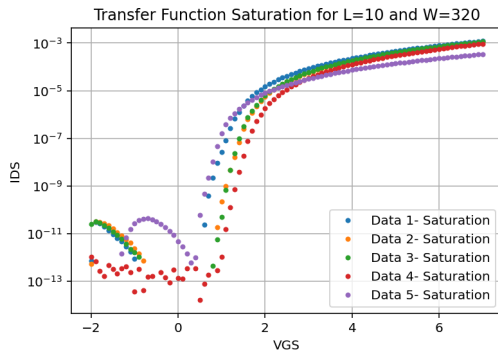


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 320 \mu\text{m}$, $L = 5 \mu\text{m}$ in the saturation region

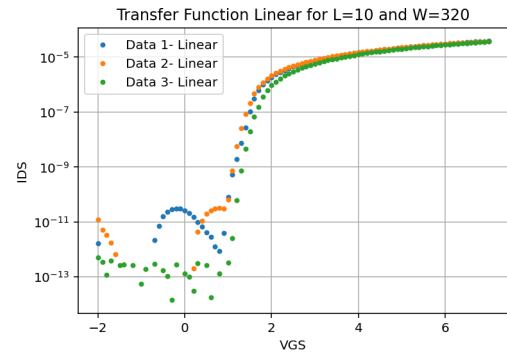


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 320 \mu\text{m}$, $L = 5 \mu\text{m}$ in the linear region

Figure B.1: Experimental transfer characteristics for $W = 320 \mu\text{m}$ and $L = 5 \mu\text{m}$ in both linear and saturation regions.

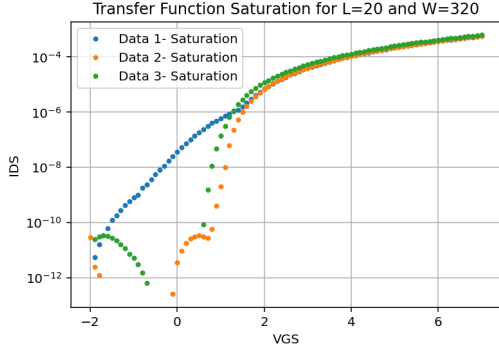


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 320 \mu\text{m}$, $L = 10 \mu\text{m}$ in the saturation region

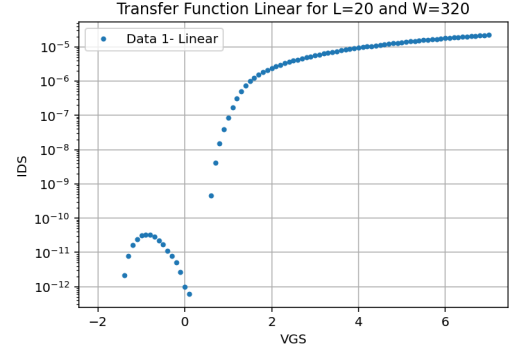


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 320 \mu\text{m}$, $L = 10 \mu\text{m}$ in the linear region

Figure B.2: Experimental transfer characteristics for $W = 320 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.

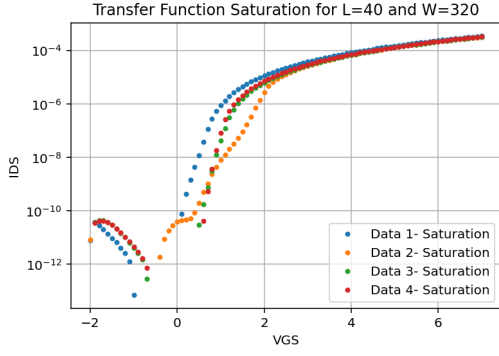


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 320 \mu\text{m}$, $L = 20 \mu\text{m}$ in the saturation region

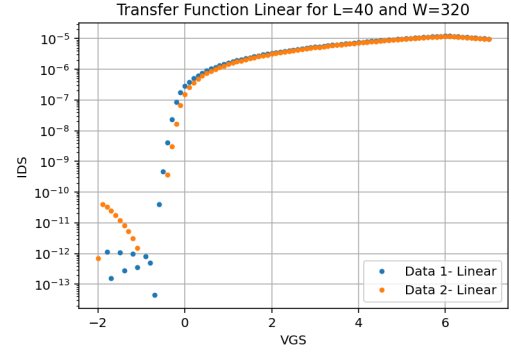


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 320 \mu\text{m}$, $L = 20 \mu\text{m}$ in the linear region

Figure B.3: Experimental transfer characteristics for $W = 320 \mu\text{m}$ and $L = 20 \mu\text{m}$ in both linear and saturation regions.

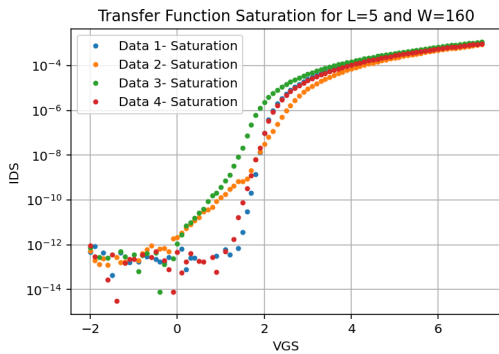


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 320 \mu\text{m}$, $L = 40 \mu\text{m}$ in the saturation region

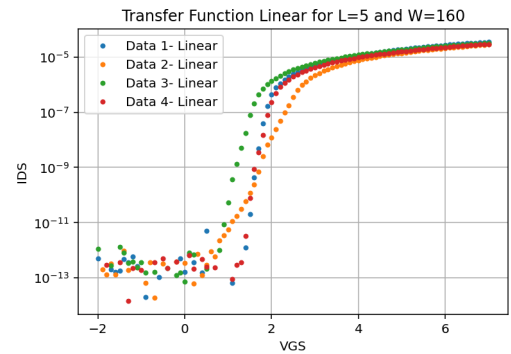


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 320 \mu\text{m}$, $L = 40 \mu\text{m}$ in the linear region

Figure B.4: Experimental transfer characteristics for $W = 320 \mu\text{m}$ and $L = 40 \mu\text{m}$ in both linear and saturation regions.



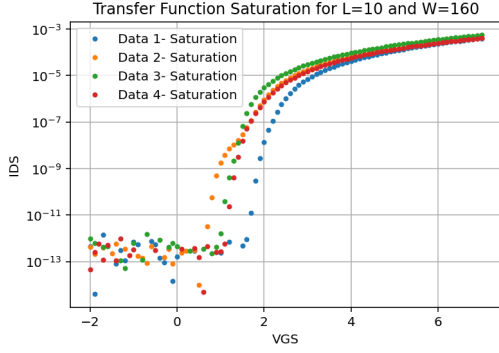
(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 160 \mu\text{m}$, $L = 5 \mu\text{m}$ in the saturation region



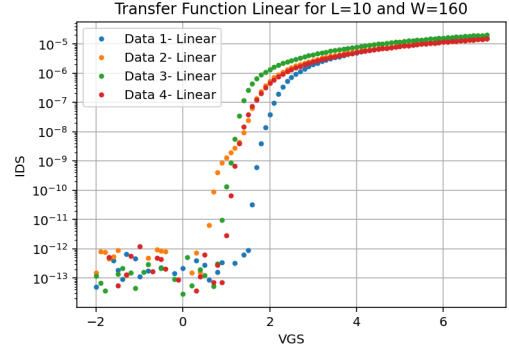
(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 160 \mu\text{m}$, $L = 5 \mu\text{m}$ in the linear region

Figure B.5: Experimental transfer characteristics for $W = 160 \mu\text{m}$ and $L = 5 \mu\text{m}$ in both linear and saturation regions.

APPENDIX B. TRANSFER CHARACTERISTICS DATASET 2

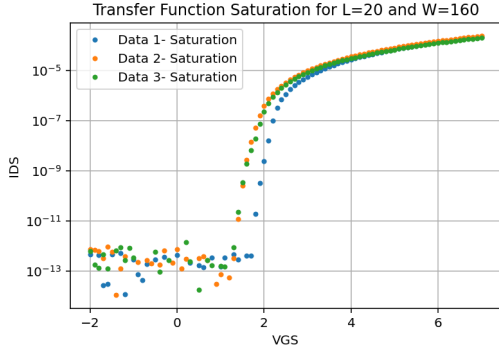


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 160 \mu\text{m}$, $L = 10 \mu\text{m}$ in the saturation region

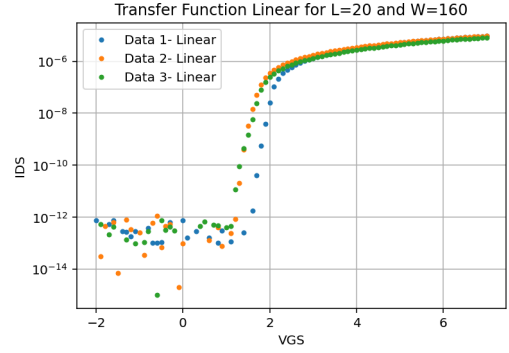


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 160 \mu\text{m}$, $L = 10 \mu\text{m}$ in the linear region

Figure B.6: Experimental transfer characteristics for $W = 160 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.

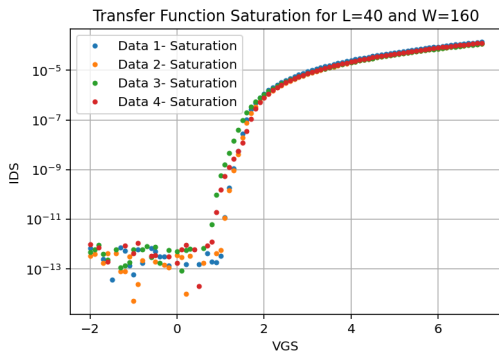


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 160 \mu\text{m}$, $L = 20 \mu\text{m}$ in the saturation region

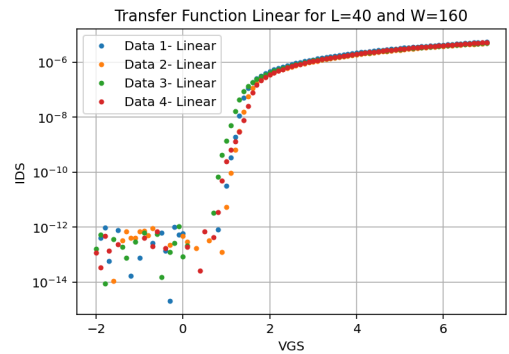


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 160 \mu\text{m}$, $L = 20 \mu\text{m}$ in the linear region

Figure B.7: Experimental transfer characteristics for $W = 160 \mu\text{m}$ and $L = 20 \mu\text{m}$ in both linear and saturation regions.

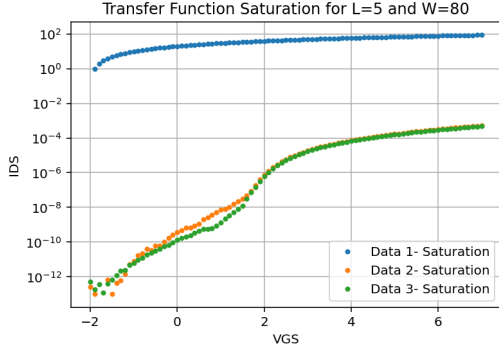


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 160 \mu\text{m}$, $L = 40 \mu\text{m}$ in the saturation region

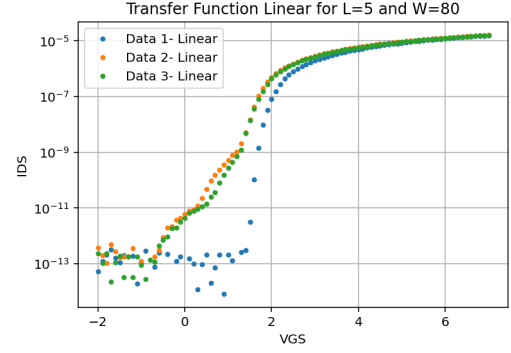


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 160 \mu\text{m}$, $L = 40 \mu\text{m}$ in the linear region

Figure B.8: Experimental transfer characteristics for $W = 160 \mu\text{m}$ and $L = 40 \mu\text{m}$ in both linear and saturation regions.

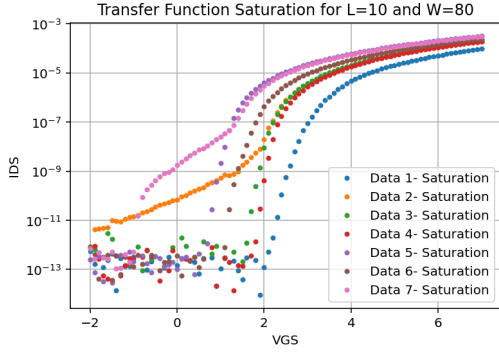


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 80 \mu\text{m}$, $L = 5 \mu\text{m}$ in the saturation region

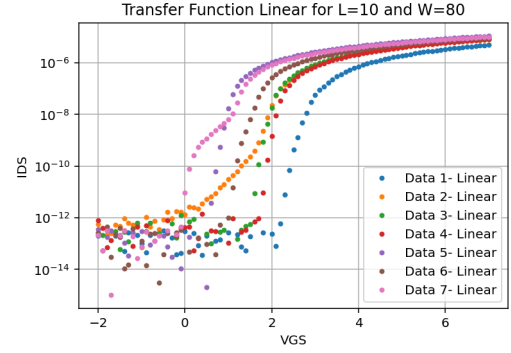


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 80 \mu\text{m}$, $L = 5 \mu\text{m}$ in the linear region

Figure B.9: Experimental transfer characteristics for $W = 80 \mu\text{m}$ and $L = 5 \mu\text{m}$ in both linear and saturation regions.

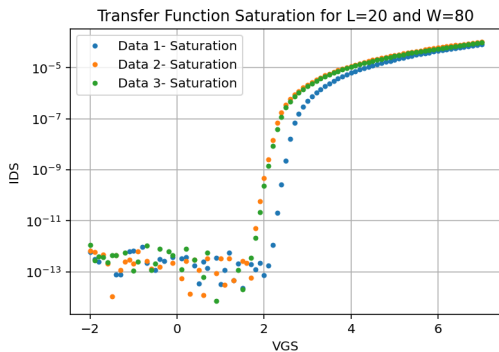


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 800 \mu\text{m}$, $L = 10 \mu\text{m}$ in the saturation region

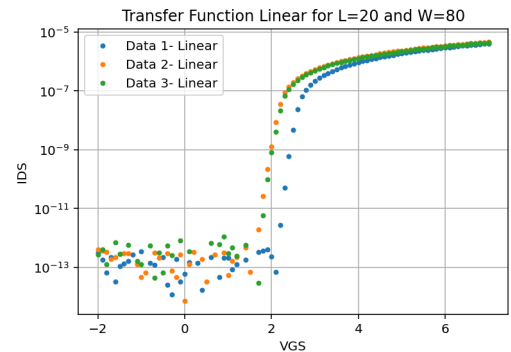


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 80 \mu\text{m}$, $L = 10 \mu\text{m}$ in the linear region

Figure B.10: Experimental transfer characteristics for $W = 80 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.



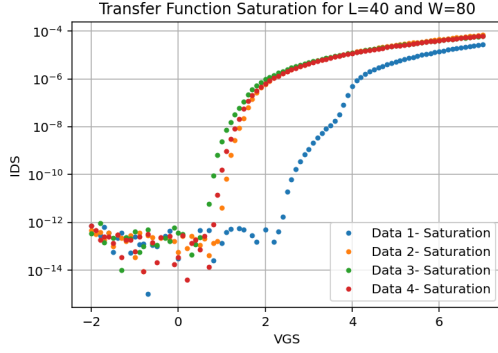
(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 80 \mu\text{m}$, $L = 20 \mu\text{m}$ in the saturation region



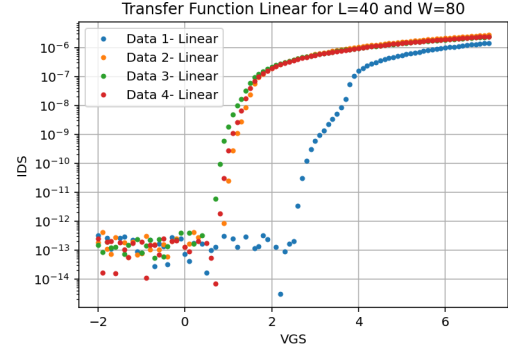
(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 80 \mu\text{m}$, $L = 20 \mu\text{m}$ in the linear region

Figure B.11: Experimental transfer characteristics for $W = 80 \mu\text{m}$ and $L = 20 \mu\text{m}$ in both linear and saturation regions.

APPENDIX B. TRANSFER CHARACTERISTICS DATASET 2

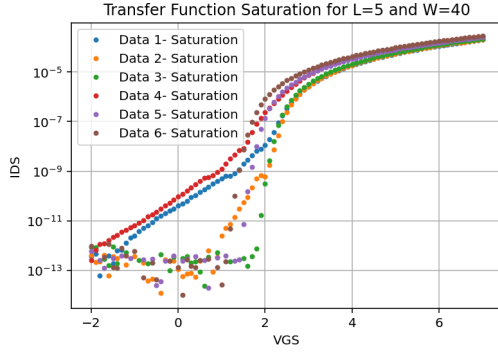


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 80 \mu\text{m}$, $L = 40 \mu\text{m}$ in the saturation region

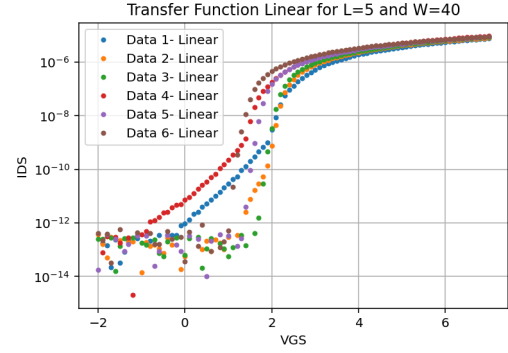


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 80 \mu\text{m}$, $L = 40 \mu\text{m}$ in the linear region

Figure B.12: Experimental transfer characteristics for $W = 80 \mu\text{m}$ and $L = 40 \mu\text{m}$ in both linear and saturation regions.

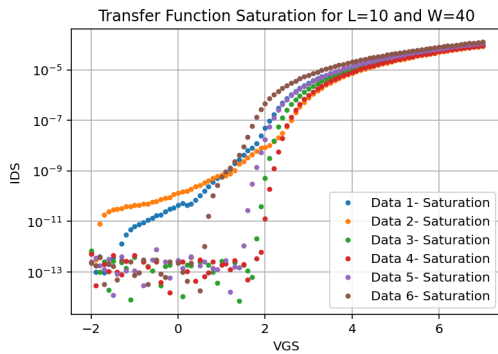


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 40 \mu\text{m}$, $L = 5 \mu\text{m}$ in the saturation region

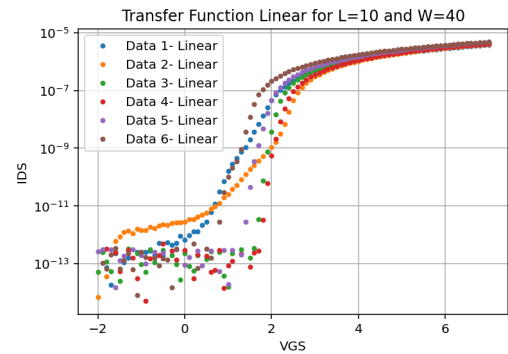


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 40 \mu\text{m}$, $L = 5 \mu\text{m}$ in the linear region

Figure B.13: Experimental transfer characteristics for $W = 40 \mu\text{m}$ and $L = 5 \mu\text{m}$ in both linear and saturation regions.

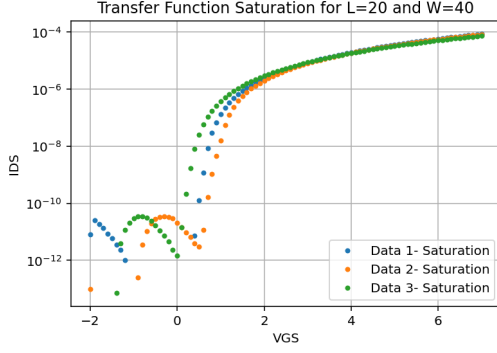


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 40 \mu\text{m}$, $L = 10 \mu\text{m}$ in the saturation region

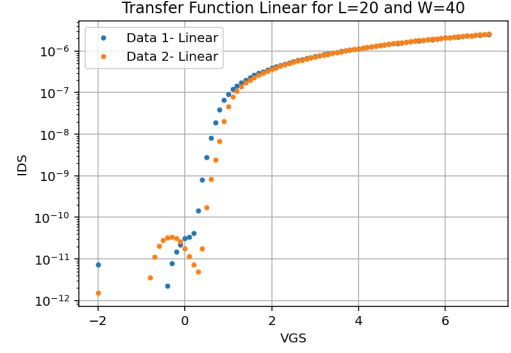


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 40 \mu\text{m}$, $L = 10 \mu\text{m}$ in the linear region

Figure B.14: Experimental transfer characteristics for $W = 40 \mu\text{m}$ and $L = 10 \mu\text{m}$ in both linear and saturation regions.

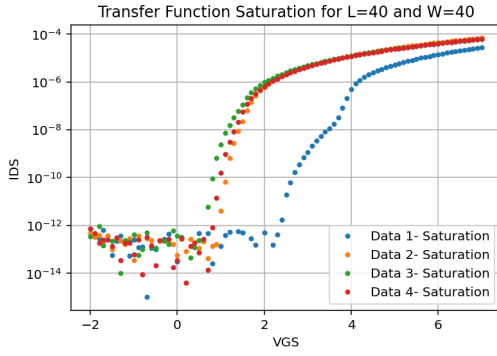


(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 40 \mu\text{m}$, $L = 20 \mu\text{m}$ in the saturation region

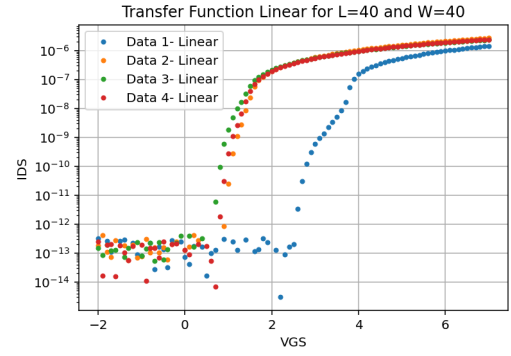


(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 40 \mu\text{m}$, $L = 20 \mu\text{m}$ in the linear region

Figure B.15: Experimental transfer characteristics for $W = 40 \mu\text{m}$ and $L = 20 \mu\text{m}$ in both linear and saturation regions.



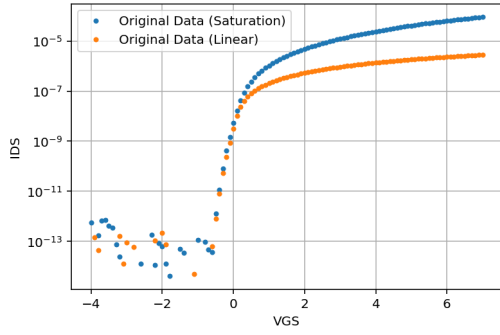
(a) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 40 \mu\text{m}$, $L = 40 \mu\text{m}$ in the saturation region



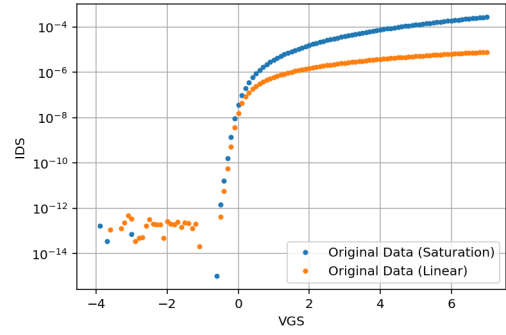
(b) Experimental transfer characteristic (I_D vs V_{GS}) for $W = 40 \mu\text{m}$, $L = 40 \mu\text{m}$ in the linear region

Figure B.16: Experimental transfer characteristics for $W = 40 \mu\text{m}$ and $L = 40 \mu\text{m}$ in both linear and saturation regions.

TRANSFER CHARACTERISTICS DATASET 3

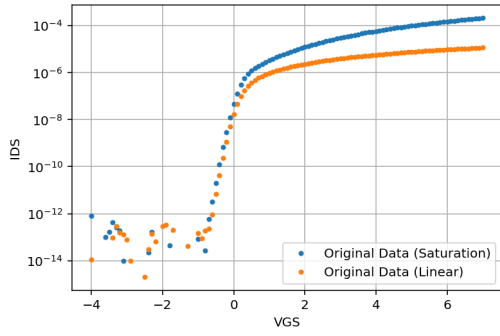


(a) $W = 100 \mu\text{m}$, $L = 20 \mu\text{m}$

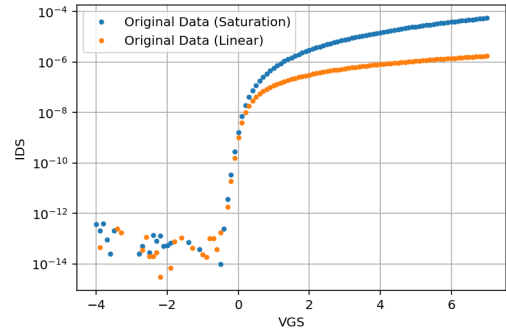


(b) $W = 100 \mu\text{m}$, $L = 10 \mu\text{m}$

Figure C.1: Experimental transfer characteristics for devices with $W = 100 \mu\text{m}$.

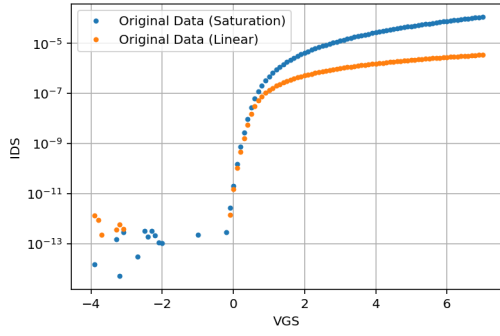
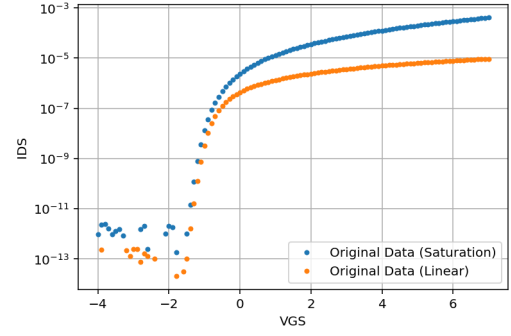


(a) $W = 100 \mu\text{m}$, $L = 5 \mu\text{m}$

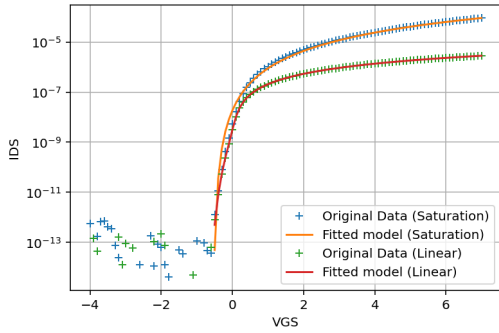


(b) $W = 50 \mu\text{m}$, $L = 20 \mu\text{m}$

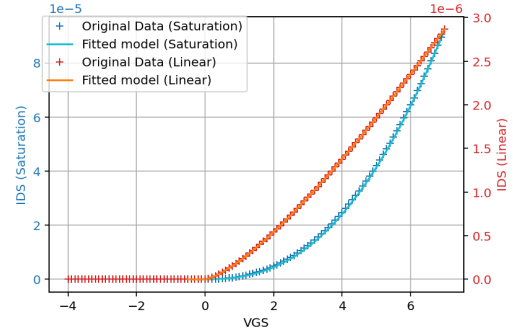
Figure C.2: Experimental transfer characteristics for short-channel $W = 100 \mu\text{m}$ and wide $W = 50 \mu\text{m}$ devices.

(a) $W = 50 \mu\text{m}$, $L = 10 \mu\text{m}$ (b) $W = 50 \mu\text{m}$, $L = 5 \mu\text{m}$ Figure C.3: Experimental transfer characteristics for devices with $W = 50 \mu\text{m}$.

DATASET 3 DC MODEL RESULTS



(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$, using a logarithmic scale.



(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$, using linear scale.

Figure D.1: Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$.

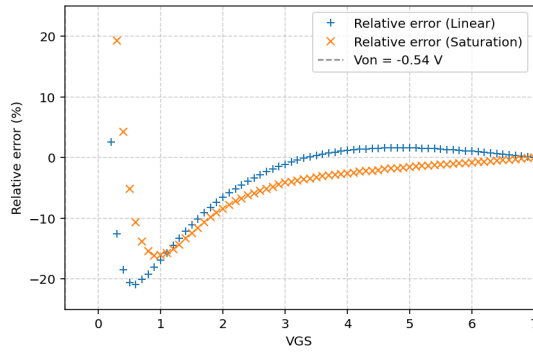
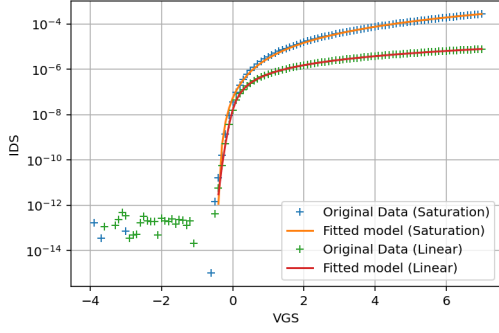
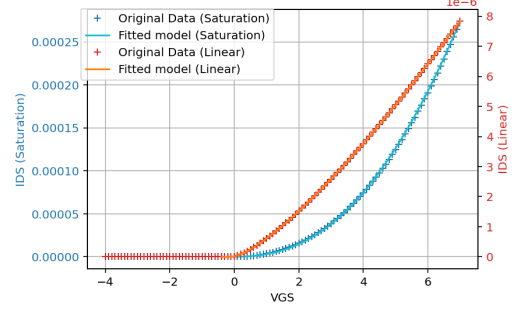


Figure D.2: Relative error of the model for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$.



(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$, using a logarithmic scale.



(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$, using linear scale.

Figure D.3: Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$.

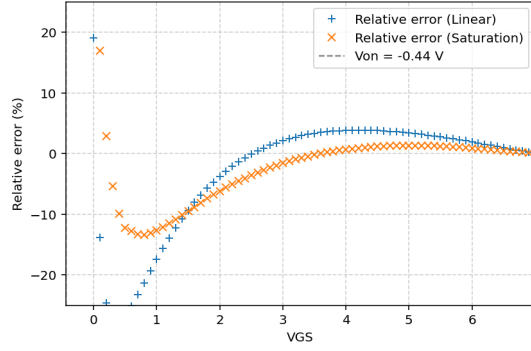
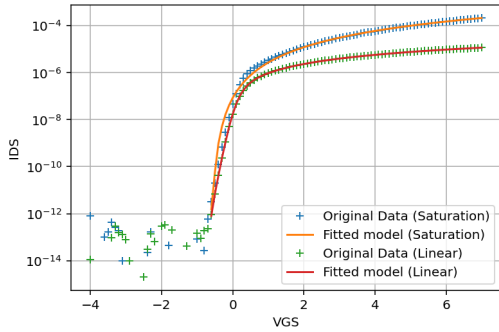
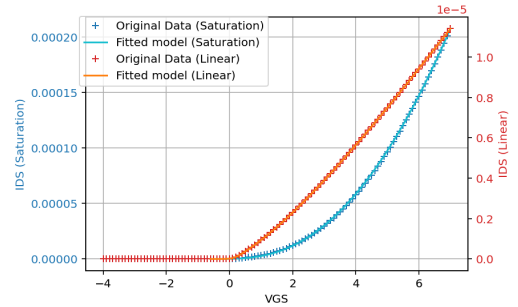


Figure D.4: Relative error of the model for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$.



(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$, using a logarithmic scale.



(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$, using linear scale.

Figure D.5: Modeled results for linear and saturation regimes compared to the measured data for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$.

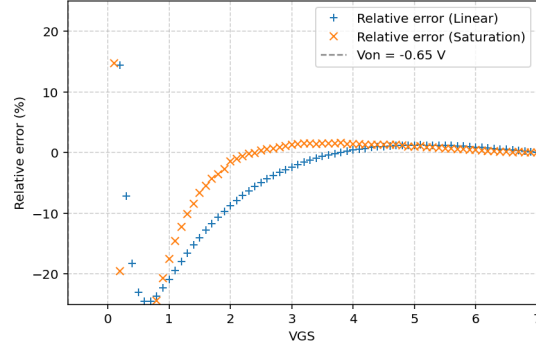
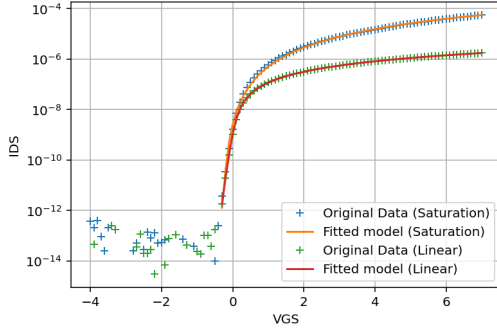
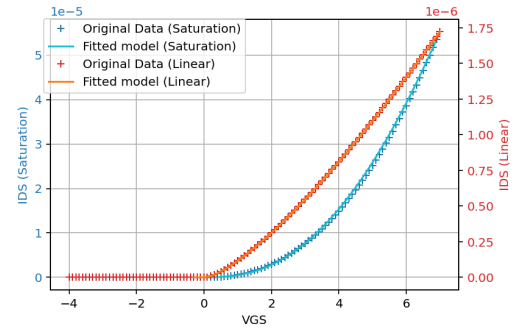


Figure D.6: Relative error of the model for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$.



(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$, using a logarithmic scale.



(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$, using linear scale.

Figure D.7: Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$.

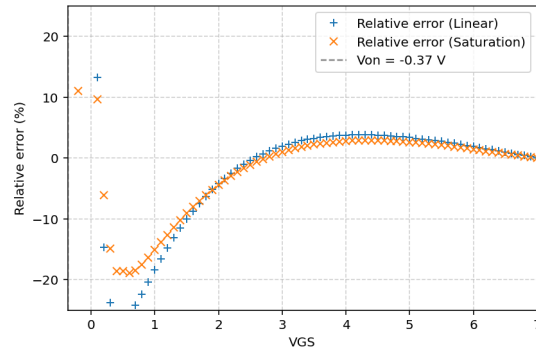
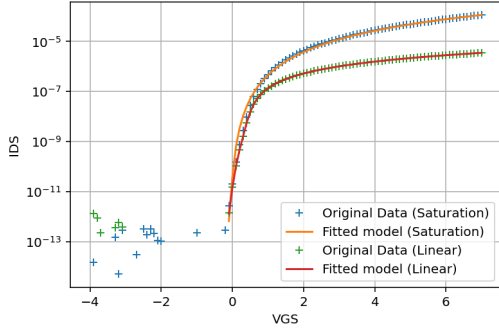
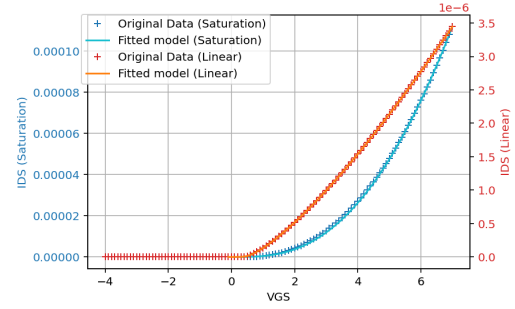


Figure D.8: Relative error of the model for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$.



(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$, using a logarithmic scale.



(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$, using linear scale.

Figure D.9: Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$.

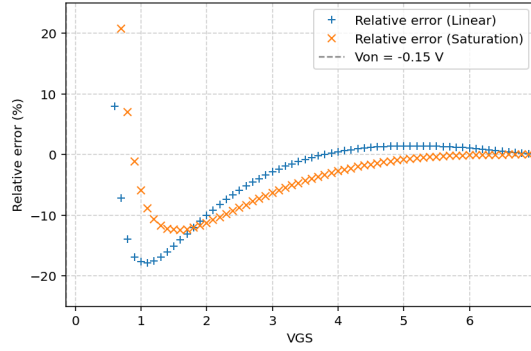
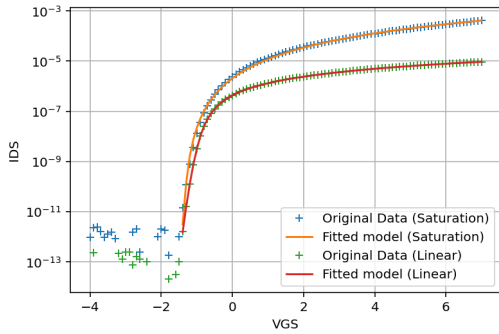
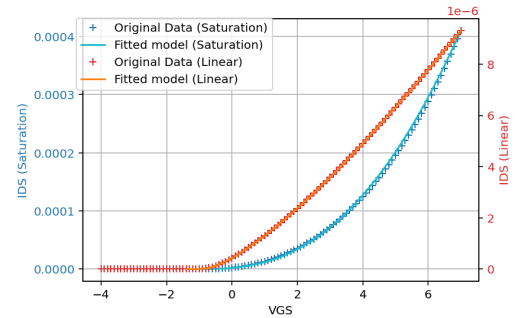


Figure D.10: Relative error of the model for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$.



(a) Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$, using a logarithmic scale.



(b) Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$, using linear scale.

Figure D.11: Modeled results for linear and saturation regimes compared to the measured data for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$.

APPENDIX D. DATASET 3 DC MODEL RESULTS

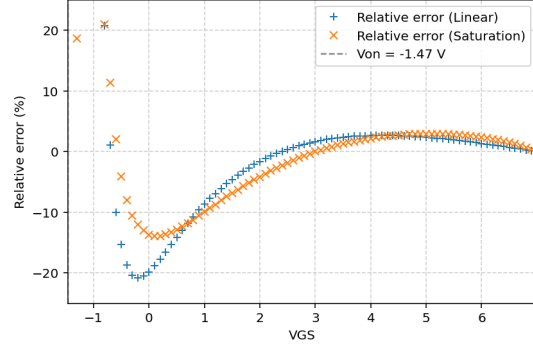
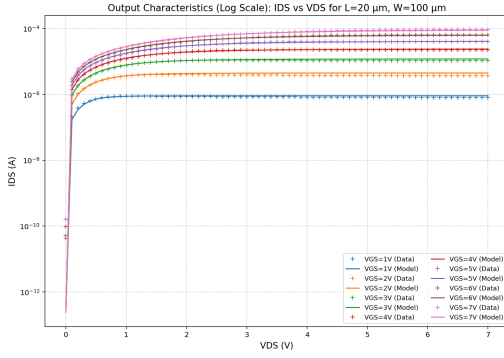
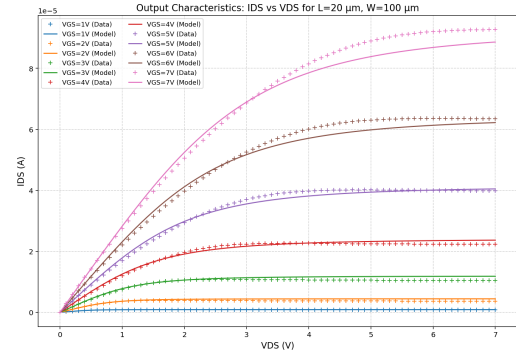


Figure D.12: Relative error of the model for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$.

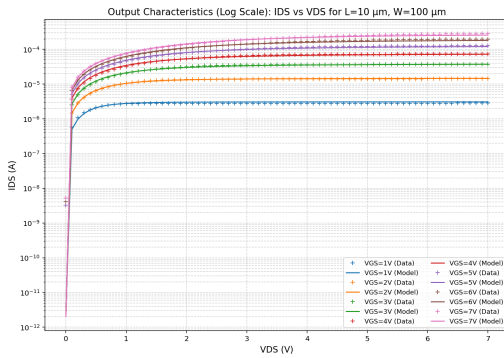


(a) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$ using the unified model, in logarithmic scale.

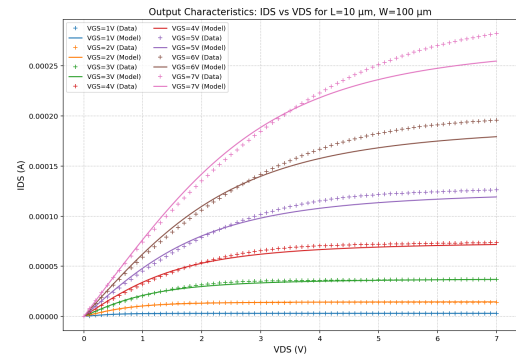


(b) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$ using the unified model, in linear scale.

Figure D.13: Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 100 \mu\text{m}$ and $L = 20 \mu\text{m}$.

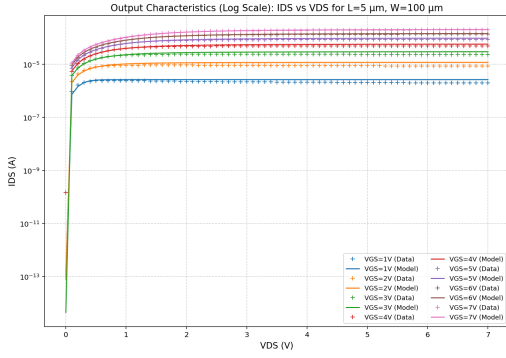


(a) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$ using the unified model, in logarithmic scale.

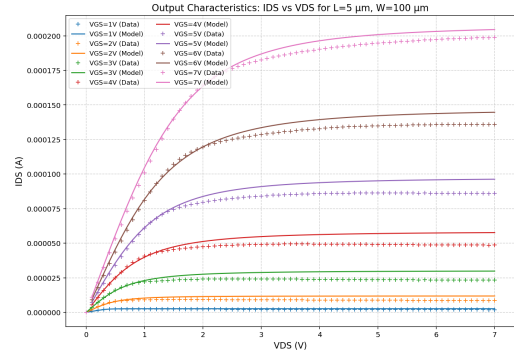


(b) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$ using the unified model, in linear scale.

Figure D.14: Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 100 \mu\text{m}$ and $L = 10 \mu\text{m}$.

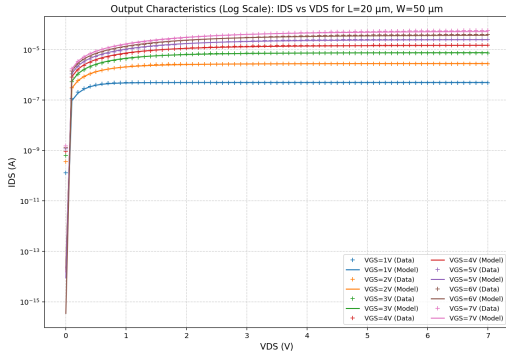


(a) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$ using the unified model, in logarithmic scale.

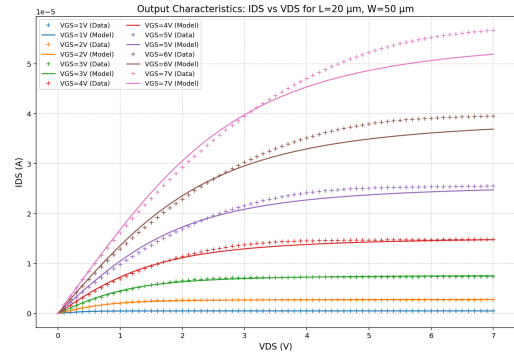


(b) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$ using the unified model, in linear scale.

Figure D.15: Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 100 \mu\text{m}$ and $L = 5 \mu\text{m}$.

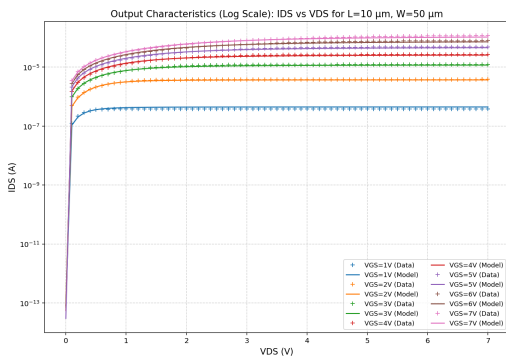


(a) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$ using the unified model, in logarithmic scale.

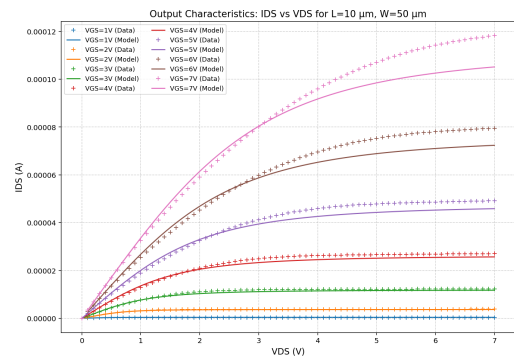


(b) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$ using the unified model, in linear scale.

Figure D.16: Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 50 \mu\text{m}$ and $L = 20 \mu\text{m}$.

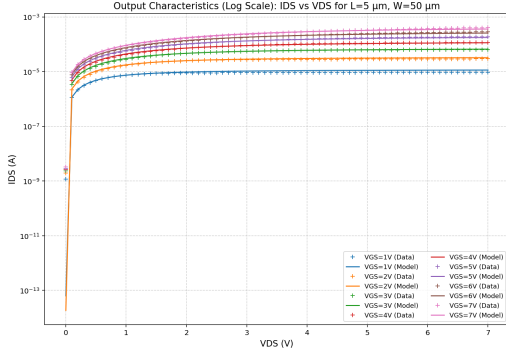


(a) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$ using the unified model, in logarithmic scale.

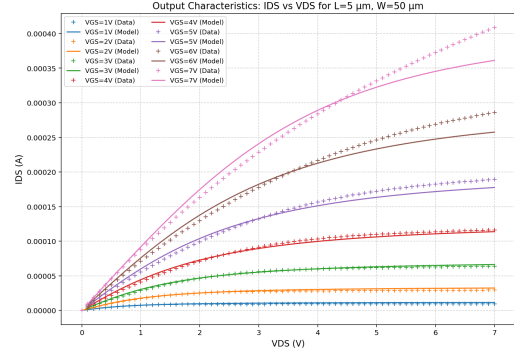


(b) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$ using the unified model, in linear scale.

Figure D.17: Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 50 \mu\text{m}$ and $L = 10 \mu\text{m}$.



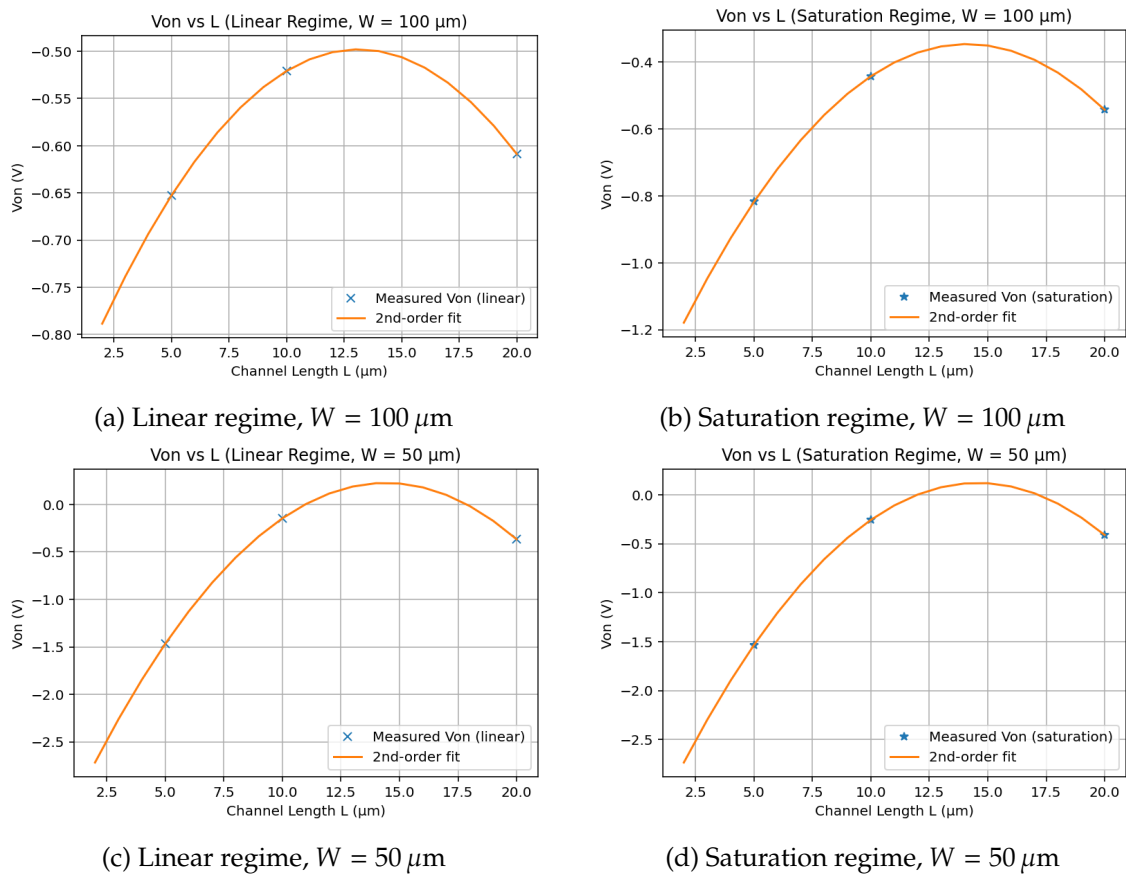
(a) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$ using the unified model, in logarithmic scale.



(b) Drain current (I_D) vs. drain-source voltage (V_{DS}) for $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$ using the unified model, in linear scale.

Figure D.18: Comparison between measured data and the unified model for $I_D(V_{DS})$ characteristics at $W = 50 \mu\text{m}$ and $L = 5 \mu\text{m}$.

SCALABLE COEFFICIENTS

Figure E.1: Extracted scalable coefficients for V_{on} in both linear and saturation regimes.

APPENDIX E. SCALABLE COEFFICIENTS

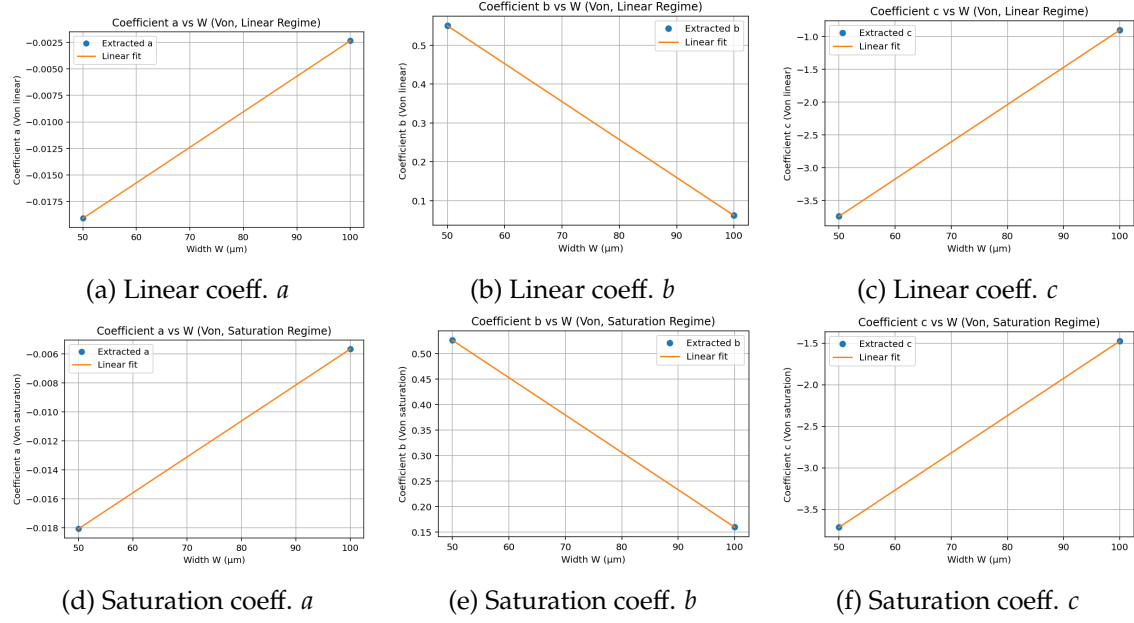


Figure E.2: Polynomial coefficients a , b , and c for V_{on} .

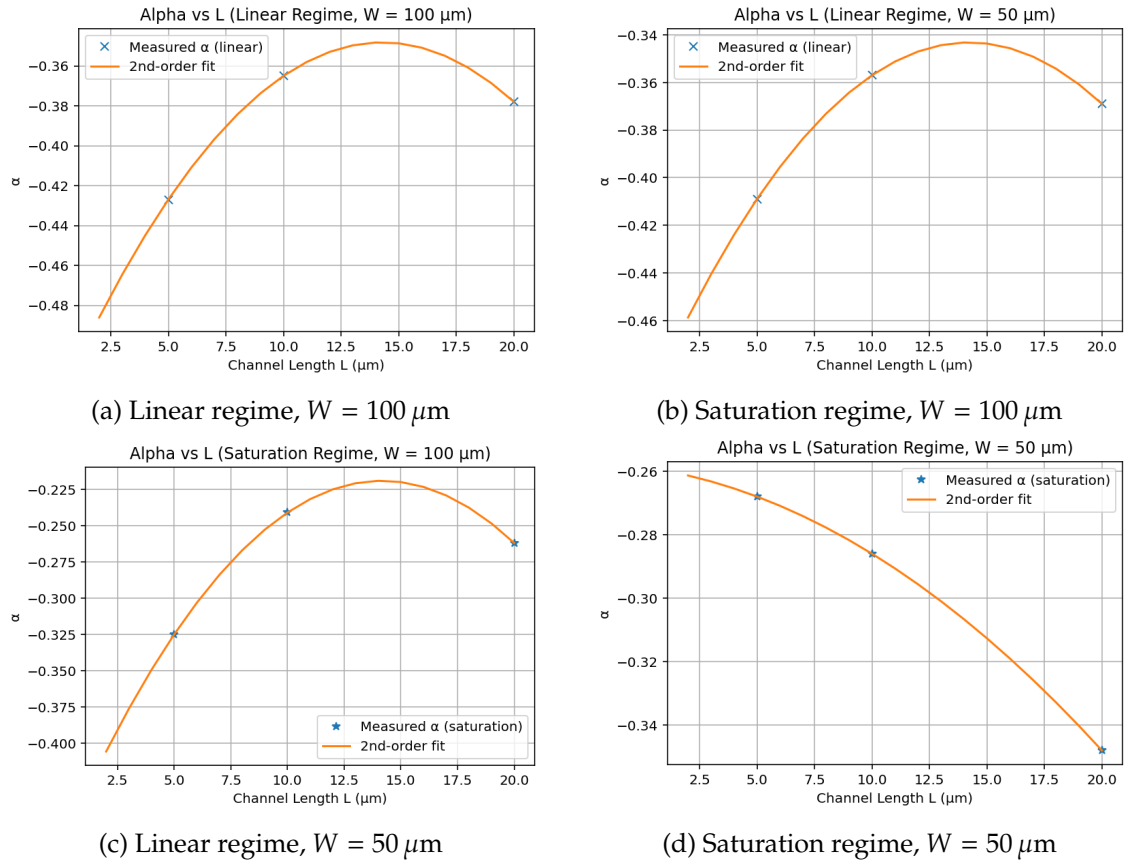
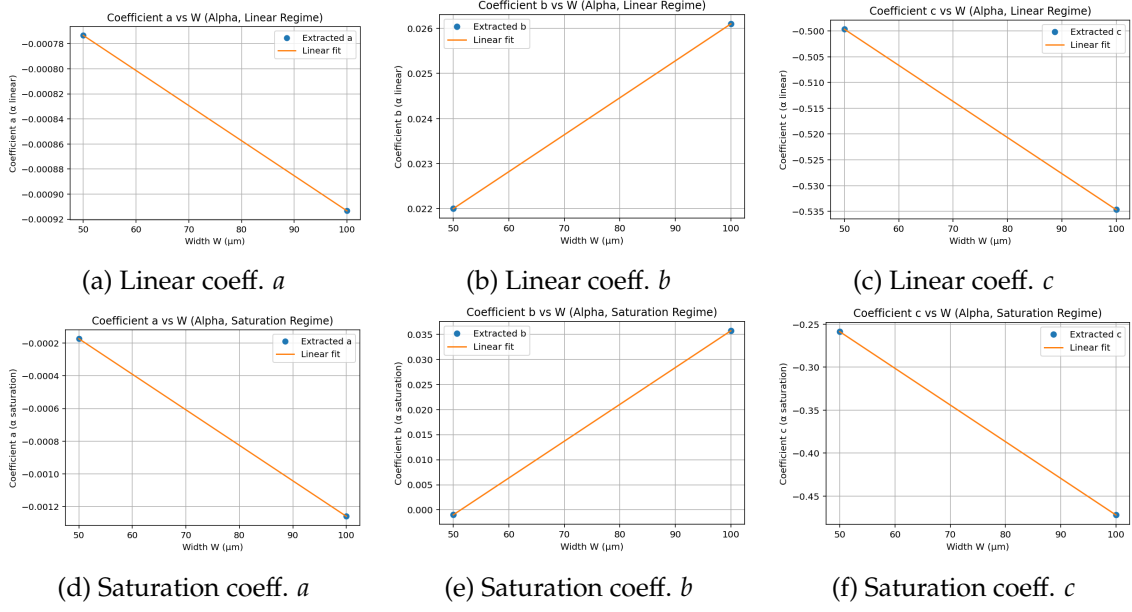
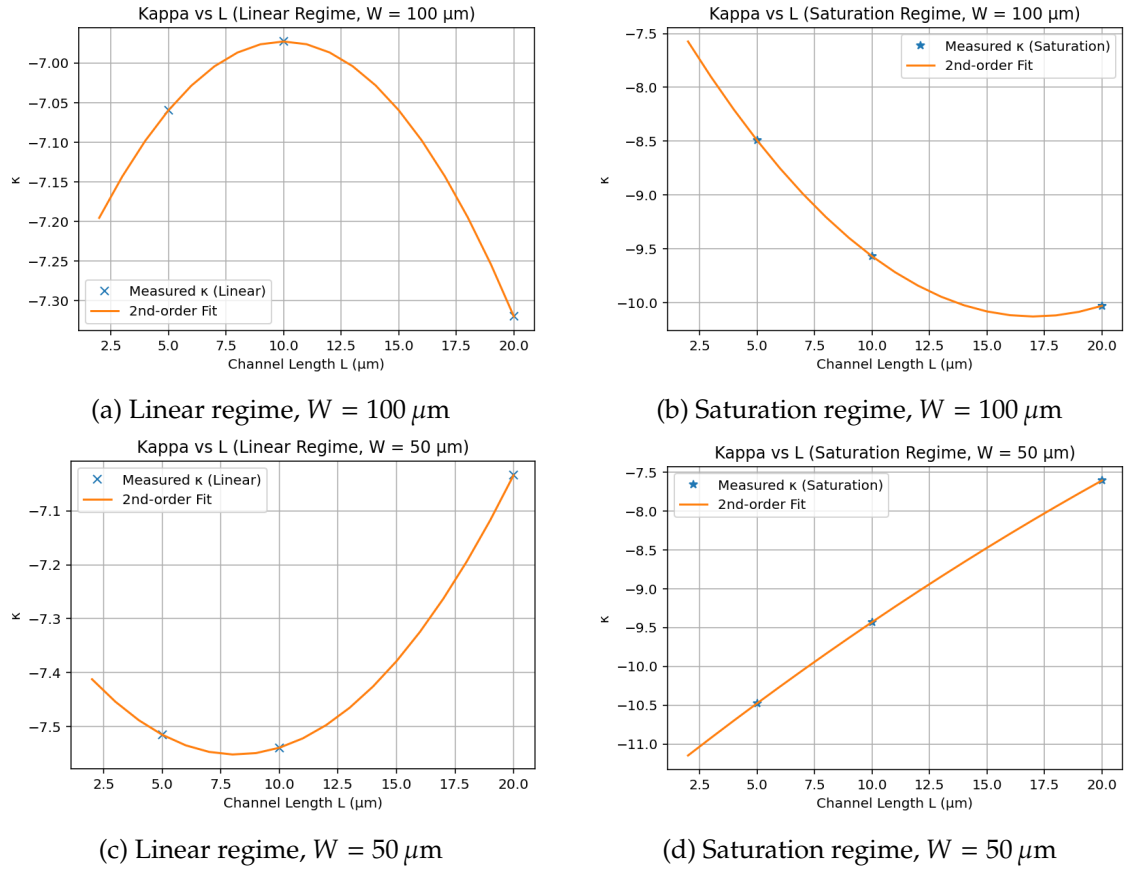


Figure E.3: Extracted scalable coefficients for α in both linear and saturation regimes.


 Figure E.4: Polynomial coefficients a , b , and c for α .

 Figure E.5: Extracted scalable coefficients for κ in both linear and saturation regimes.

APPENDIX E. SCALABLE COEFFICIENTS

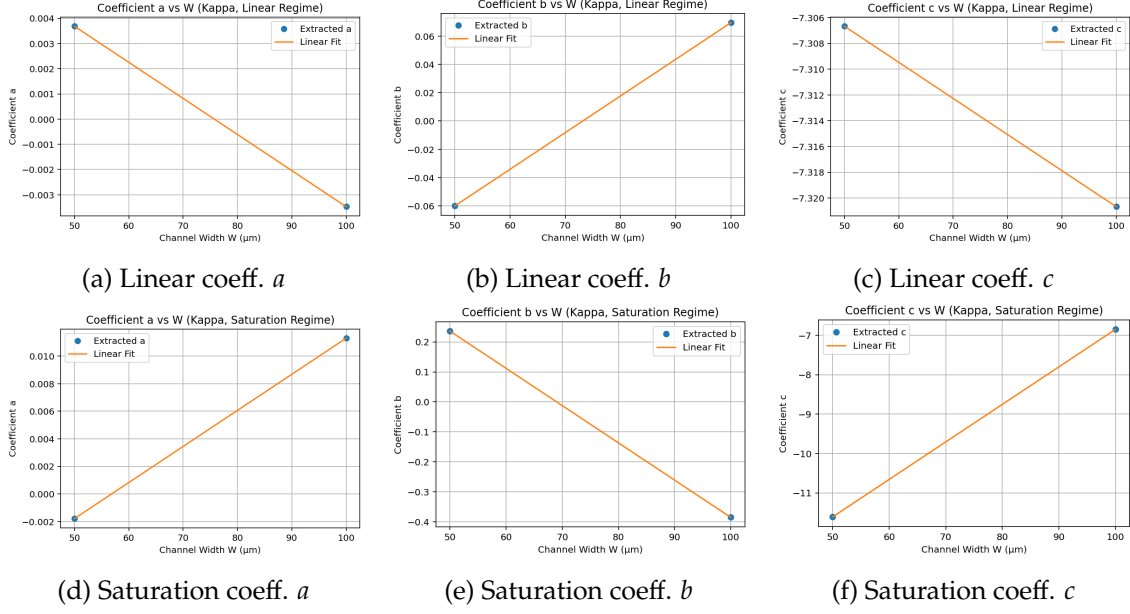


Figure E.6: Polynomial coefficients a , b , and c for κ .

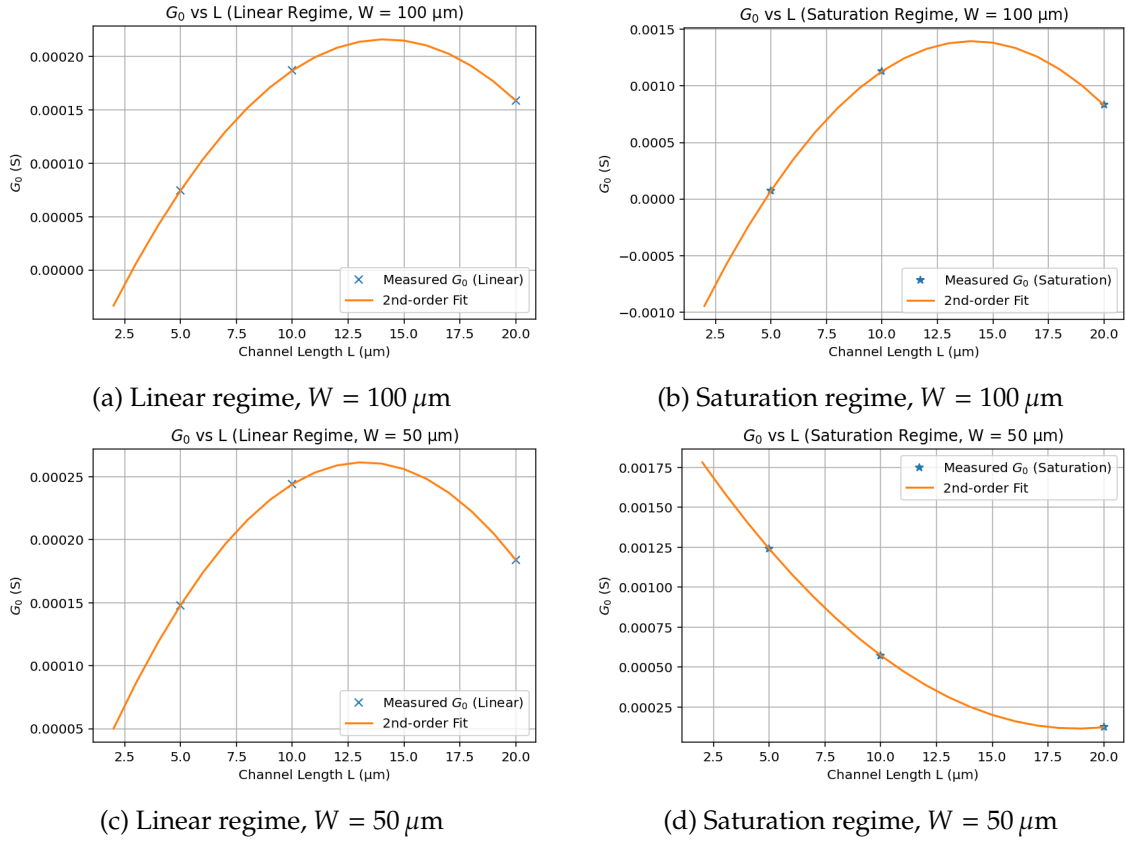
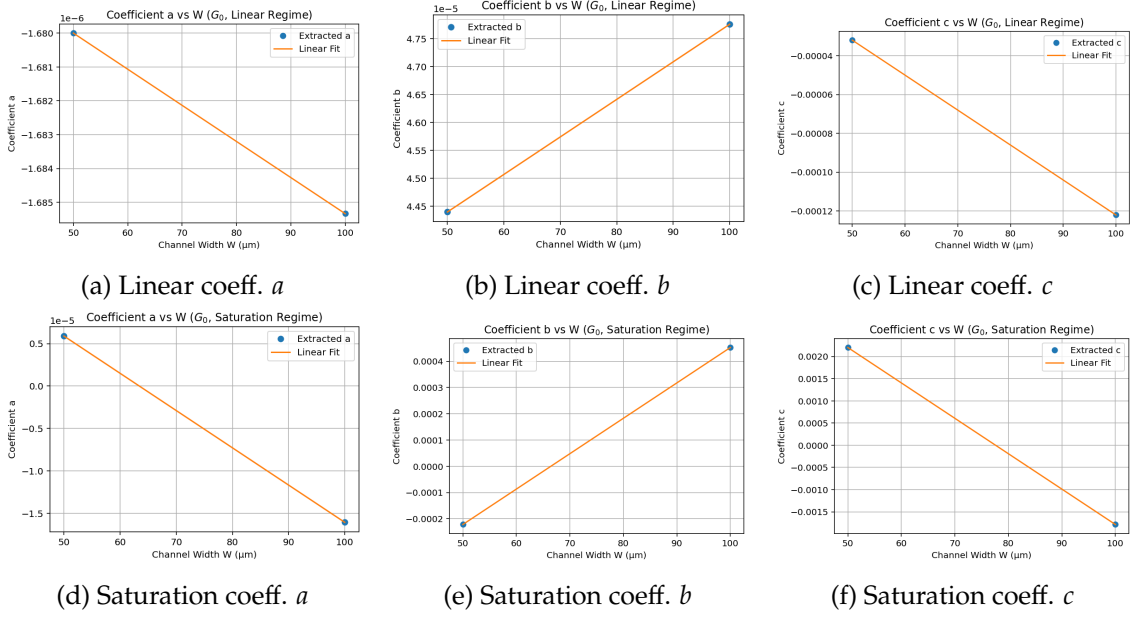
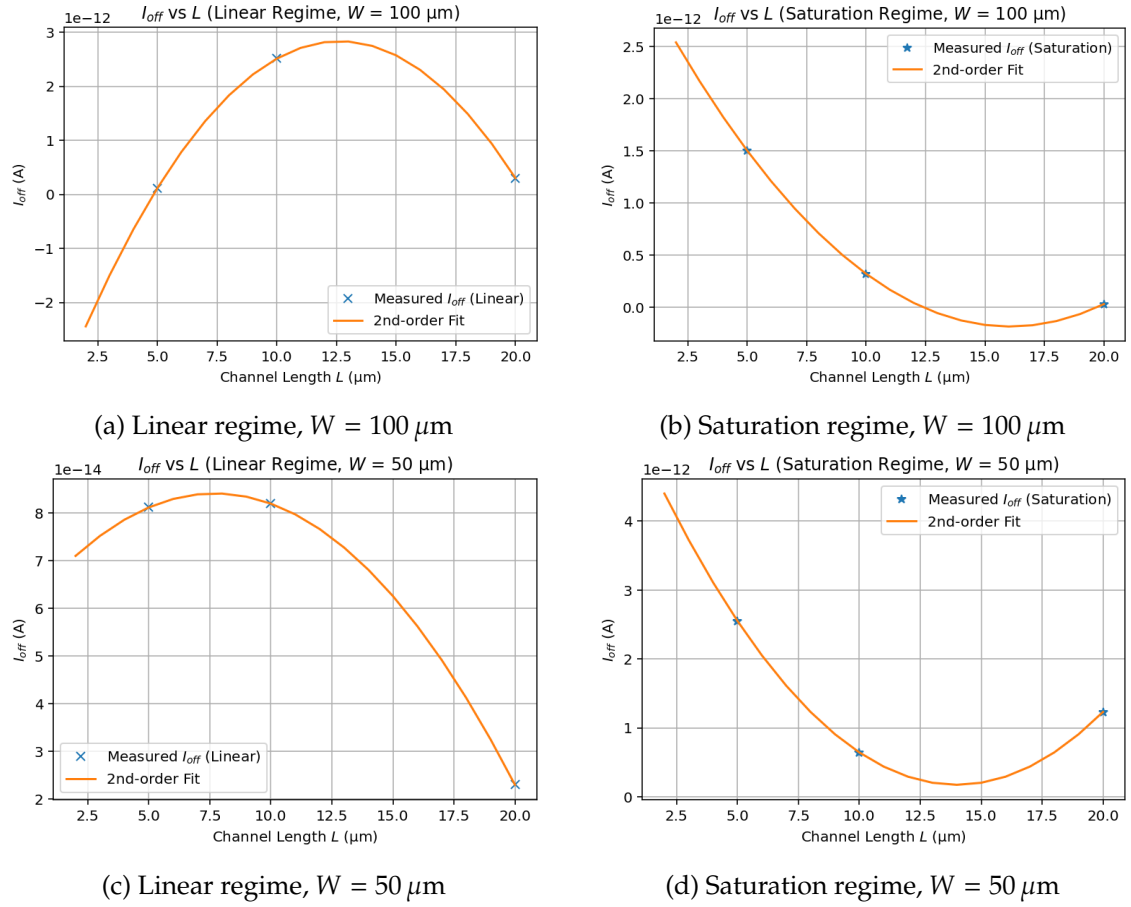


Figure E.7: Extracted scalable coefficients for G_0 in both linear and saturation regimes.


 Figure E.8: Polynomial coefficients a , b , and c for G_0 .

 Figure E.9: Extracted scalable coefficients for I_{off} in both linear and saturation regimes.

APPENDIX E. SCALABLE COEFFICIENTS

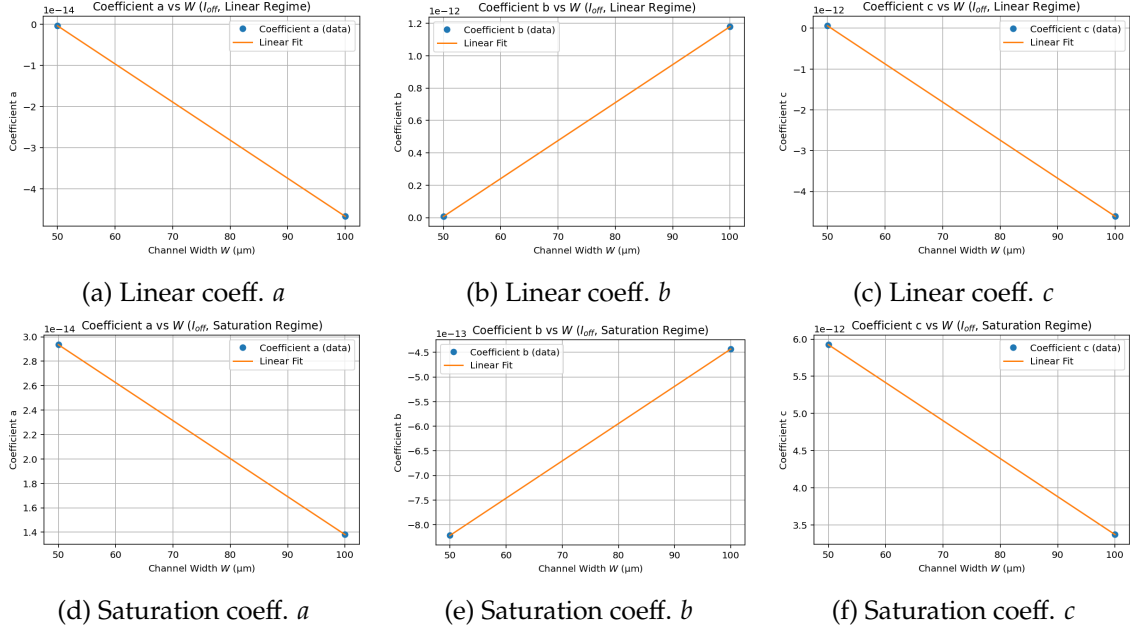


Figure E.10: Polynomial coefficients a , b , and c for I_{off} .

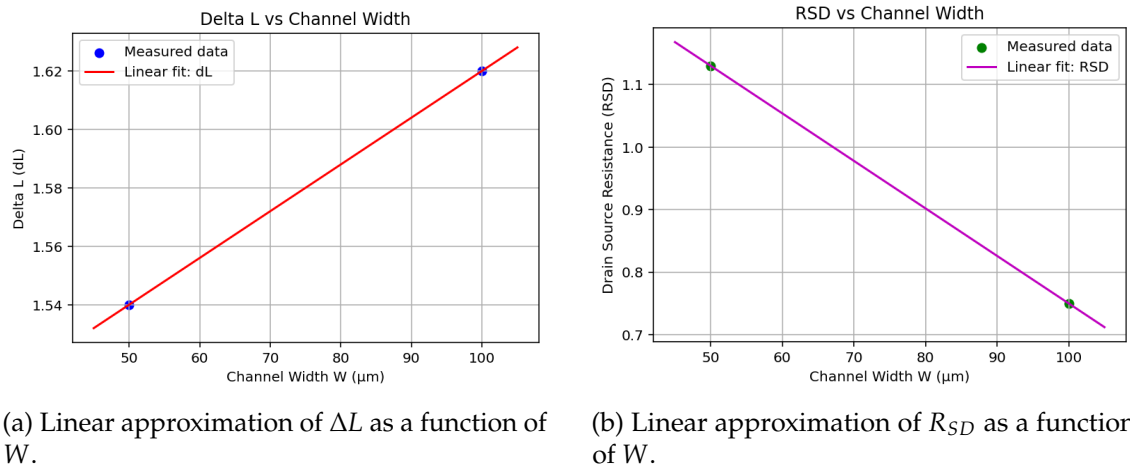


Figure E.11: Extracted linear approximations for ΔL and R_{SD} as functions of channel width W .

VERILOG-A MODEL IMPLEMENTATION

```

1  'include "constants.vams"
2  'include "disciplines.vams"
3
4  module igzo_tft(d, g, s);
5
6  inout d, g, s;
7  electrical d, g, s;s
8
9  parameter real W = 100; //um
10 parameter real L = 20;  //um
11
12 parameter real VH = 7;
13 parameter real VDSref_lin = 0.1;
14 parameter real VDSref_sat = 7;
15
16 parameter real eps_ox = 3.45e-11;
17 parameter real tox = 0.1e-6;
18
19
20
21 parameter real m = 2.2;
22
23 real Vgs, Vds, Vgd, Von_lin, Von_sat, Von_eff;
24 real alpha_lin, alpha_sat;
25 real G0_lin, G0_sat;
26 real Ioff_lin, Ioff_sat;
27 real DeltaL, RSD;
28 real Vgs_eff, Vds_eff;
29 real Iprime; //  $I' = I - I_{off}$ 
30 real Ids_lin_expr, Ids_sat_expr, Ids;
31 real denom_lin, denom_sat;
32 real k_lin, k_sat;
33 real Lp;

```

```

34 real Ids_sat, Ids_lin;
35 real Ids_total;
36 real term_exp;
37 real G;
38 real Covs, Covd, CCH;
39 real Qovs, Qovd, Qch;
40 real Lov, Lovch;
41
42
43 analog function real von_lin_func;
44     input Lm, Wm; // micrometers
45     real Lm, Wm;
46     real L2;
47     begin
48         L2 = Lm*Lm;
49         von_lin_func = ((3.35e-4 * Wm -3.58e-2) * L2) + ((-9.776e
50             -3 * Wm + 1.04) * Lm) +(5.68e-2 * Wm -6.58);
51     end
52 endfunction
53
54 analog function real von_sat_func;
55     input Lm, Wm;
56     real Lm, Wm;
57     real L2;
58     begin
59         L2 = Lm*Lm;
60         von_sat_func = ((2.48e-4 * Wm - 3.05e-2) * L2) +
61             ((-7.332e-3 * Wm + 8.93e-1) * Lm) +
62             (4.48e-2 * Wm - 5.95);
63     end
64 endfunction
65
66 function real alpha_lin_func;
67     input Lm, Wm;
68     real Lm, Wm;
69     real L2;
70     begin
71         L2 = Lm*Lm;
72         alpha_lin_func = ((-2.8e-6 * Wm -6.33e-4) * L2) +
73             ((8.20e-5 * Wm + 1.79e-2) * Lm) +
74             (-7e-4 * Wm - 4.65e-1);
75     end
76 endfunction
77
78 function real alpha_sat_func;
79     input Lm, Wm;

```

```

79  real Lm, Wm;
80  real L2;
81  begin
82      L2 = Lm*Lm;
83      alpha_sat_func = ((-2.17e-5 * Wm + 9.13e-4) * L2) +
84                      ((7.34e-4 * Wm - 3.77e-2) * Lm) +
85                      (-4.27e-3 * Wm - 4.53e-2);
86  end
87  endfunction
88
89  analog function real kappa_lin_func;
90  input Lm, Wm;
91  real Lm, Wm;
92  real L2;
93  begin
94      L2 = Lm*Lm;
95      kappa_lin_func = ((-1.43e-4 * Wm + 1.08e-2) * L2) +
96                      ((2.59e-3 * Wm - 1.9e-1) * Lm) +
97                      (-2.8e-4 * Wm - 7.29);
98  end
99  endfunction
100
101  analog function real kappa_sat_func;
102  input Lm, Wm;
103  real Lm, Wm;
104  real L2;
105  begin
106      L2 = Lm*Lm;
107      kappa_sat_func = ((2.62e-4 * Wm - 1.49e-2) * L2) +
108                      ((-1.24e-2 * Wm + 8.57e-1) * Lm) +
109                      (9.53e-2 * Wm - 1.64e1);
110  end
111  endfunction
112
113  analog function real G0_lin_func;
114  input Lm, Wm;
115  real Lm, Wm;
116  real L2;
117  begin
118      L2 = Lm*Lm;
119      G0_lin_func = ((-1.07e-10 * Wm - 1.67e-6) * L2) +
120                  ((6.72e-8 * Wm + 4.10e-5) * Lm) +
121                  (-1.8e-6 * Wm + 5.81e-5);
122  end
123  endfunction
124

```

```

125 analog function real G0_sat_func;
126     input Lm, Wm;
127     real Lm, Wm;
128     real L2;
129     begin
130         L2 = Lm*Lm;
131         G0_sat_func = ((-4.39e-7 * Wm + 2.79e-5) * L2) +
132                     ((1.35e-5 * Wm - 8.96e-4) * Lm) +
133                     (-7.98e-5 * Wm + 6.19e-3);
134     end
135 endfunction
136
137 analog function real Ioff_lin_func;
138     input Lm, Wm;
139     real Lm, Wm;
140     real L2;
141     begin
142         L2 = Lm*Lm;
143         Ioff_lin_func = ((-9.254e-16* Wm + 5.59e-14) * L2) +
144                     ((2.346e-14 * Wm - 1.17e-12) * Lm) +
145                     (-9.348e-14* Wm + 4.73e-12);
146     end
147 endfunction
148
149 analog function real Ioff_sat_func;
150     input Lm, Wm;
151     real Lm, Wm;
152     real L2;
153     begin
154         L2 = Lm*Lm;
155         Ioff_sat_func = ((-3.11e-16* Wm + 4.49e-14) * L2) +
156                     ((7.57e-15* Wm - 1.2e-12) * Lm) +
157                     (-5.11e-14* Wm + 8.48e-12);
158     end
159 endfunction
160
161 analog function real DeltaL_func;
162     input Wm;
163     real Wm;
164     begin
165         DeltaL_func = 0.0016 * Wm + 1.46; // [um]
166     end
167 endfunction
168
169 analog function real RSD_func;
170     input Wm;

```



```

171     real Wm;
172     begin
173         RSD_func = -0.0076 * Wm + 1.51; // [Kohm] as given
174     end
175 endfunction
176
177 analog begin
178
179     Vgs = V(g, s);
180     Vds = V(d, s);
181     Vgd = V(g, d);
182
183     DeltaL = DeltaL_func(W);
184     RSD = RSD_func(W)/100;
185
186
187     Von_lin = von_lin_func(L, W);
188     Von_sat = von_sat_func(L, W);
189     alpha_lin = alpha_lin_func(L, W);
190     alpha_sat = alpha_sat_func(L, W);
191     k_lin = kappa_lin_func(L, W);
192     k_sat = kappa_sat_func(L, W);
193     G0_lin = G0_lin_func(L, W);
194     G0_sat = G0_sat_func(L, W);
195     Ioff_lin = Ioff_lin_func(L, W);
196     Ioff_sat = Ioff_sat_func(L, W);
197
198     Lp = L - DeltaL;
199
200     Lov = L*10e-5;
201     Lovch = 0.8*L*1e-6;
202
203     Covs = eps_ox * W * 1e-5 * Lov / tox;
204     Covd = eps_ox * W * 1e-5 * Lov / tox;
205     CCH = eps_ox * W * 1e-5 * Lovch / tox;
206
207     Qovs = Covs * V(g, s);
208     Qovd = Covd * V(g, d);
209     Qch = CCH * V(g, s);
210
211     if (Von_lin < Von_sat)
212         Von_eff = Von_sat;
213     else
214         Von_eff = Von_lin;
215
216     if (Vgs <= Von_eff) begin

```

```
217
218   if (Vds < (Vgs - Von_eff)) begin
219       Ids_total = Ioff_lin;
220   end
221   else begin
222       Ids_total = Ioff_sat;
223   end
224
225 end
226 else begin
227
228   term_exp = exp(k_lin * (Vgs - Von_eff)** alpha_lin);
229   G = G0_lin * (W / Lp) * term_exp;
230   Ids_lin = (G * Vds + Ioff_lin) / (1 + RSD * G);
231
232   Ids_sat = G0_sat * (W/Lp)* exp(k_sat*(Vgs - Von_eff)**alpha_sat)* (Vgs
       - Von_eff)+ Ioff_sat;
233
234   Ids_total = (Ids_lin**(-m) + Ids_sat**(-m))**(-1/m);
235 end
236
237 I(d,s) <+ Ids_total;
238 I(g,s) <+ ddt(Qovs + Qch);
239 I(g,d) <+ ddt(Qovd);
240 end
241
242 endmodule
```

Listing F.1: Modelo Verilog-A IGZO TFT



2025 Development of IGZO thin-film transistors (TFTs) compact models Carolina de Almeida