Built-in Self Test of High Speed Analog-to-Digital Converters

Edinei Santin, Luis B. Oliveira, and Joao Goes

Signals found in nature need to be converted to the digital domain through analog-to-digital converters (ADCs) to be processed by digital means [1]. For applications in communication and measurement [2], [3] high conversion rates are required. With advances of the CMOS technology, the conversion rates of CMOS ADCs are now well beyond the gigasamples per second (GS/s) range, but only moderate resolutions are required [4]. These ADCs need to be tested after fabrication and, if possible, during field operation. The test costs are a very significant fraction of their production cost [5]. This is mainly due to lengthy use of very expensive automated test equipment (ATE) to apply specific test stimuli to the devices under test (DUT), and to collect and analyse their responses.

With high conversion rates it is difficult to interface the ADCs to the test instruments due: extra parasitics, line trace mismatches, interferences within the printed circuit board (PCB), and the instrument test probes. This becomes even more challenging in the case of systems-on-a-chip, system-in-a-package, and three-dimensional (3D) chips, where the accessibility of the ADCs for testing purposes is restricted [6].

In this paper we discuss the use of built-in self-test (BIST) techniques for testing high speed ADCs and we present a specific solution, in which the analog input signal and the clock are generated internally.

BIST for High Speed ADCs

Using advanced CMOS technologies, the cost per transistor decreases and integrated solutions become competitive. Thus, more specific functionalities can be fully integrated on-chip. Moreover, the reliability of the manufacturing process maintains high, allowing reliable function to be implemented on-chip as well.

The implementation of test-related functions directly on-chip during the IC design phase, which is called design for testability, evolved firstly for purely digital ICs and then migrated to mixed-signal devices. Using a BIST approach contributes to additional area, increases design time and effort, and may degrade the performance of the DUT due to intrusive test structures. Table 1 summarizes the pros and cons of a BIST solution.

Table 1 - Summary of advantages and disadvantages of BIST.

Advantages	Disadvantages
vertical testability (wafer to system)	area overhead
high diagnosis resolution	performance penalties
full-speed testing	additional design time & effort
reduced need for external test equipment	additional risk to project
reduced test development time & effort	difficulty to reach full accuracy
reduced manufacturing test time & effort	
reduced time-to-market	

As discussed above, as a result of the increase of the conversion rate of ADCs, from the present few GS/s, their testing becomes progressively more time-consuming and costly. Here we present a novel solution, which consists of using two small area synchronized phase-locked loops (PLLs) to generate high frequency sinusoidal and clock signals. We analyse the possibility of using a dedicated BIST approach for testing high speed, moderate resolution ADCs, either embedded into complex systems or as standalone components. This BIST approach is based on two compact and easy-to-integrate oscillators that generate high frequency test stimuli (analog input and clock) to the DUT. Instead of using free-running oscillators for generating the analog input and clock test stimuli, we propose to employ two phase-locked-loops to improve the phase noise of the generated signals and, more importantly, to allow coherent sampling. The use of coherent sampling is beneficial since it simplifies the processing of the output data and a coherent sampled signal leads to a coherent spectrum, which avoids undesirable artefacts due to spectral leakage. This fully integrated in CMOS technology BIST approach, which reduces test costs by avoiding the need of expensive mixed-signal ATEs, improves reliability by avoiding interfacing critical signals between the DUT and ATE, and enhances feasibility by carrying out the test procedure completely on-chip, is the main contribution of this paper. Although the DUT used in this work employs a pipelined ADC topology, the approach can be applied to other converter topologies, since it “sees” the DUT as an almost ideal “black box”. The conceptual overview of the proposed approach is shown in Fig. 1.

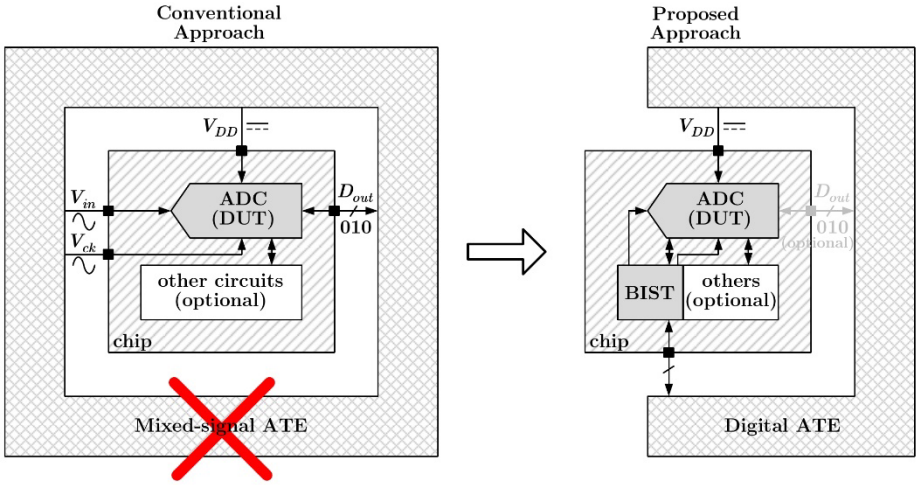


Fig. 1. Overview of the proposed idea.

Using the proposed BIST approach, the only off-chip component required is a low frequency and stable reference signal. Digital signal processing (DSP) techniques for output response analysis are used, which rely primarily on spectral computations using fast Fourier transform (FFT) algorithms. The proposed concept was implemented in an integrated circuit featuring two PLLs for test stimuli generation and an 8-bit 500 MS/s ADC as the DUT and was validated with silicon measurements. In a 0.13 μm CMOS technology, the area overhead introduced by the two PLLs is only 0.052 mm^2.

PROPOSED ADC BIST ARCHITECTURE

The ADC BIST architecture proposed in this work is illustrated in Fig. 2. It is composed of two integer-*N* PLLs (PLLIN and PLLCK) that share the same external reference clock to ensure signal synchronization. This synchronization is necessary to achieve coherent sampling. PLLIN generates low distortion, high frequency, and low jitter sine wave signals, while PLLCK generates high frequency and low jitter square wave clock signals, which are used to drive the ADC during the test procedure. The only off-chip component required is a stable and low frequency reference clock, which may be implemented, for example, by an inexpensive crystal oscillator. The digitized samples are processed by a DSP (e.g. to execute a FFT algorithm), in order to calculate the most important functional performances of the DUT. The results may then be compared, for example, with different effective resolution thresholds (e.g. 6, 7, and 8 bits) up to the maximum resolution allowed by the self-testing system and, for each comparison, a pass or fail indication shown. With this, ADCs having different resolutions are sorted and it becomes possible to check the performance degradation during the ADC life time. A test controller takes care of the test application and sequence.

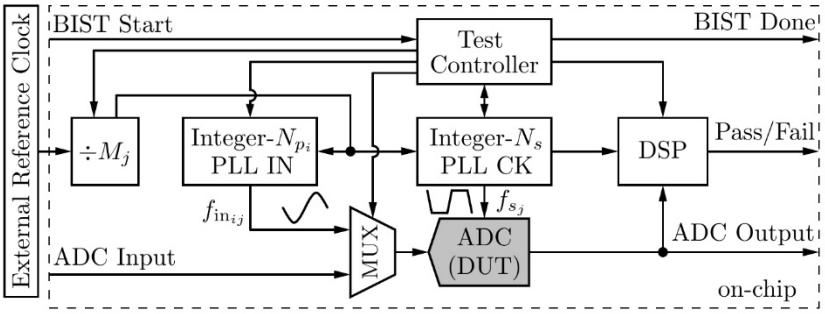


Fig. 2. Proposed BIST architecture for coherent testing of high speed ADCs.

When the two PLLs are locked, the input and sampling frequencies of the ADC are, respectively,

$$f_{\text{in}_{ij}} = N_{p_i} \frac{f_{\text{ref}}}{M_j} \tag{1}$$

$$f_{s_j} = N_s \frac{f_{\text{ref}}}{M_j} \tag{2}$$

where f_{ref} is a stable external reference frequency, N_s is the number of collected samples, and M_j and N_{pi} (i,j = 1,2,...) are integer programmable frequency divider values, which enable different frequencies for the input and sampling signals. From Eqs. (1) and (2) coherent sampling is achieved (i.e. $f_{\text{in}}/f_s = N_p/N_s$).

The architecture parameters N_s, N_{pi}, and M_j are selected according to the resolution of the ADC under test, the external reference frequency, the desired sampling frequencies ($\hat{f}_{sj}$), and the desired normalized input frequencies ($\hat{f}_{\text{in}i}/f_s$). N_s is a power of two ideally given by $N_s > \pi 2^N \approx 2^{N+2}$ [7], where N is the number of bits of the ADC. N_{pi} (i = 1,2,...) is given by

$$N_{p_i} = \left\{ \frac{\hat{f}_{\text{in}_i}}{f_s} N_s \right\} \tag{3}$$

where $\{x\}$ means the nearest odd integer value of x. Note that odd integer values for N_{pi} ensure irreducibility with respect to N_s, since the latter is a power of two (this irreducible ratio is another requisite of coherent sampling). M_j (j = 1,2,...) is given by

$$M_j = \left\langle \frac{f_{\text{ref}} N_s}{\hat{f}_{s_j}} \right\rangle \tag{4}$$

where $\langle x \rangle$ is the nearest integer value of x. As an example, Table 2 gives the architecture parameters and the resulting frequency map for a hypothetical 6-bit ADC with f_{ref} = 4 MHz, $\hat{f}_{sj}$ = 250, 500, and 1000 MS/s,

and f_{ini}/f_s = 1/2, 1/4, and 1/8. We can see that the actual analog input and sampling frequencies are slightly different from the desired ones, but this is required to guarantee coherent sampling.

Table 2 – Programmable parameters and frequency map for a 6-bit ADC.

$f_{\text{ref}} \equiv 4$ MHz		$\hat{f}_{s_1} \equiv 250$	$\hat{f}_{s_2} \equiv 500$	$\hat{f}_{s_3} \equiv 1000$
$N \equiv 6$ bits	$N_s = 256$	$M_1 = 4$	$M_2 = 2$	$M_3 = 1$
		$f_{s_1} = 256$	$f_{s_2} = 512$	$f_{s_3} = 1024$
$\hat{f}_{\text{in}_1}/f_s \equiv 1/2$	$N_{p_1} = 127$	$f_{\text{in}_{11}} = 127$	$f_{\text{in}_{12}} = 254$	$f_{\text{in}_{13}} = 508$
$\hat{f}_{\text{in}_2}/f_s \equiv 1/4$	$N_{p_2} = 63$	$f_{\text{in}_{21}} = 63$	$f_{\text{in}_{22}} = 126$	$f_{\text{in}_{23}} = 252$
$\hat{f}_{\text{in}_3}/f_s \equiv 1/8$	$N_{p_3} = 31$	$f_{\text{in}_{31}} = 31$	$f_{\text{in}_{32}} = 62$	$f_{\text{in}_{33}} = 124$

* All frequencies are in MHz or MS/s.

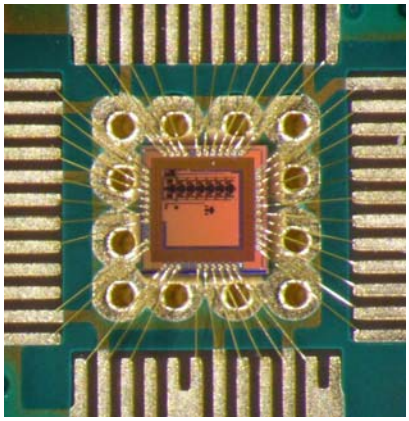
The reconfigurable BIST architecture shown in Fig. 2 can be efficiently integrated (e.g. with small area overhead), as detailed explained in [8]. As a result, it is a very attractive solution for functional testing of high speed ADCs.

EXPERIMENTAL RESULTS

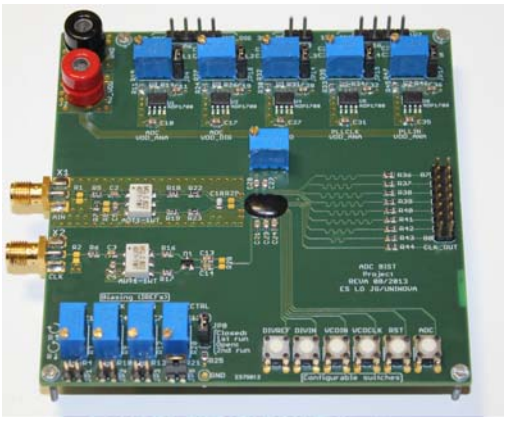
We will consider two extreme evaluation modes:

i) ADC driven by the external analog input and clock (this mode assesses the standalone ADC performance); *ii*) ADC stimulated with the internal analog input and clock (this mode assesses the performance of the whole BIST system, i.e., ADC + PLLCK + PLLIN).

The test modes above are evaluated using the PCB board (with a wire-bonded die) shown in Fig. 3. The evaluation mode where both the analog input and clock are generated externally is the most demanding in terms of test equipment resources.



(a)



(b)

Fig. 3. Photograph of a wire-bonded die before glob top encapsulation (a) and of a completely assembled test board (b). Die dimensions are 1525×1525 μm^2. PLLIN core occupies an area of only 138 μm ×282 μm and PLLCK occupies 92 μm ×138 μm.

The high-quality (i.e., very low phase noise) external analog input is provided by an RF signal generator, Marconi Instruments 2041. In order to remove the harmonics of the generated signal (intrinsic to this kind of generator), the analog input is bandpass or low-pass filtered before being applied to the test board. In this work, the following Mini-Circuits passive filters were used: SBP-10.7, SLP-100+, SLP-250+, SLP-550+, and SLP750+. The external clock signal, both for ADC clocking or for the reference clock of the PLLs, is provided by another RF signal generator, Rohde&Schwarz SMB100A/SMB-B112. This generator also has very low phase noise. For instance, the integrated rms jitter in the bandwidth from 100 Hz to 2 GHz at 1 GHz is merely 210 fs. The ADC output data are captured with a logic analyzer, Agilent 16702B/16715A, and the data are then remotely transferred to a personal computer and processed in MATLAB. A set of on-board push-button switches allows the configuration of the system and the selection of the desired test mode.

The standalone performance of the ADC, when both the analog input and the clock are provided externally, is presented. Following that, the whole ADC BIST performance is presented, when the analog input and the clock are both generated internally by PLLIN and PLLCK, respectively.

The results are presented in terms of the performance parameters: SINAD, SNR, and THD. Since the ADC topology is based on a two-channel time-interleaving (TI) array, it is also interesting to analyse the spurious tones caused by TI. The THD values presented account up to the 13rd harmonic. The even harmonics are insignificant with respect to the odd ones due to the use of differential signalling and very symmetrical and careful layouts. All results presented are derived from 512 collected samples, coherent spectra and no averaging is applied.

DUT with External Analog Input and Clock:

In this case the converter is stimulated with external analog input and clock. This evaluation gives a reference performance which can then be contrasted with the other evaluation case, in which the analog input and clock are generated on-chip.

The measured SINAD, SNR, THD, and TI spurious components versus input frequency for a randomly selected die sample are shown in Fig 4. With a full-scale input tone, all metrics remain approximately flat up to the Nyquist frequency.

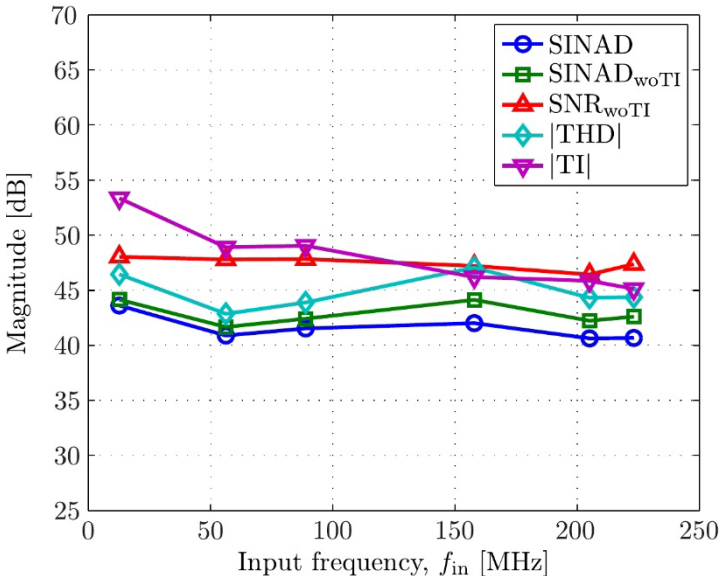


Fig. 4 Measured SINAD, SNR, THD, and TI spur versus f_{in} at $f_s \approx 464$ MS/s and $V_{\text{in}} \approx -0.1$ dBFS (time-interleaving spur is removed, i.e. "woTI").

DUT with Internal Analog Input and Clock

In this case both the analog input signal and the clock signal are provided internally by means of PLLIN and PLLCK, respectively. Thus, the complete BIST system is evaluated.

The amplitude of the sinusoidal signal generated by PLLIN directly influences the THD of the analog input signal to the ADC, because the voltage-controlled oscillator produces more distortion as the oscillation amplitude increases, and also because the linear buffer that follows the VCO and drives the track-and-hold stage of the ADC becomes more nonlinear as the input signal increases.

Since in this work the distortion of the VCO dominates and increases when the output differential amplitude of the VCO becomes larger than $V_{\text{in}} = 600$ mV$_{\text{pp,diff}}$, we set the analog input amplitude to this level. Given that the input full-scale range of the ADC is nominally 800 mV$_{\text{pp,diff}}$, this level of V_{in} corresponds to −2.5 dBFS. If we were not constrained by the distortion of the VCO, we would choose a larger analog input level, e.g., −0.1 dBFS (corresponding to 790 mV$_{\text{pp,diff}}$ in this case), in order to exercise almost all output codes of the ADC.

Table 3 – H3 and TI spur.

Testing case*	H3 [dB]	TI spur [dB]
1) External input and clock	-48.3	-44.4
2) Internal input and clock	-41.4	-42.2

* Obtained from the measured output spectra (512 points) of one of the test samples at $f_s = 464.64$ MS/s ($= 256 \times 3.63/2$ MHz), $f_{\text{in}} = 226.875$ MHz ($= 125 \times 3.63/2$ MHz) with $V_{\text{in}} \approx -2.5$ dBFS for the two cases.

Table 3 summarizes the highest harmonic and TI tone from the measured output spectra for the evaluation cases. For a fair comparison, we use the same frequencies and amplitude for all cases. We note in case 1) that besides the fundamental tone, a set of odd harmonics, dominated by the third harmonic (−48.3 dB), and the TI spurious tone (−44.4 dB), which is the strongest in the spectrum.

In case 2), the third harmonic level is −41.4 dB and the TI spurious tones is −42.2 dB. We have a 6.9 dB difference in the third harmonic and a 2.2 dB difference in the TI spurious components level. The larger discrepancy in the third harmonic level is mainly due to the increased distortion introduced by the VCO of PLLIN (even though we are using a $V_{\text{in}} \approx -2.5$ dBFS).

Similar conclusions can be drawn analysing the output spectra of other two randomly selected die samples.

In summary, we can say that the quality of the analog input and clock signals produced by the PLLs of the BIST scheme proposed in this work allows us to evaluate an ADC with a SFDR as high as about 41.4 dB when sampling an almost-Nyquist-frequency tone at about 500 MS/s.

Discussion

The BIST scheme proposed in this work can be compared with other works in the literature, as shown in Table 4.

One of the key requisites of a BIST circuitry is small area overhead, since the extra silicon area affects both the overall cost and yield of the ICs. As we can see in Table 4, our work has an almost fourfold area improvement compared with the most area-efficient implementation, even ignoring that the other works do not deal with the clock signal generation. This improvement is achieved by a judicious selection of circuit topologies and techniques. For instance, instead of using area-hungry LC oscillators to build up the voltage-controlled oscillators of the phase-locked loops, we use simple RC oscillators. We use a capacitance multiplication scheme to reduce the capacitances, and consequently the silicon area, of the loop filters of the PLLs.

The power dissipation of the BIST circuits is not very important because they are used only during a fraction of the operation time of the remaining (core) circuits, usually during the power-on or during idle time slots. After the self-test procedures, the BIST circuits are turned-off, dropping the power dissipated by these circuits to (almost) zero. Hence, even though the BIST circuits proposed in this work dissipate a relatively high power, 26 mW, this is acceptable for the target application.

We compare the quality of the analog input signal to the DUT using the SFDR metric. Even though the measured SFDR of this work is worse than that of [10]-[12], it is obtained for much higher analog input

frequencies and amplitudes. For example, the SFDR of 74.1 dB reported in [10] is for an analog input frequency as low as 10 MHz and for a low differential amplitude, 228 mV_{pp}. In general, it is unfeasible or very difficult to keep a high SFDR with high analog input frequency and/or amplitude, since the circuits suffer from higher distortions or bandwidth. This is shown in the SFDR of 25.3 dB reported in [9], where the input frequency is 312 MHz.

The main limitations of the generated analog input and clock signals of the proposed BIST scheme are the following:

- Distortion in the analog input signal. The sources of these distortions are the nonlinearity of the VCO of PLLIN, and also the nonlinearity of the buffer that follows this VCO and drives the front-end track-and-hold of the ADC.
- Phase noise (or jitter) in the analog input and clock signals. The source of this noise is mainly the noise in the active devices of the VCOs in PLLIN and PLLCK.
- Deterministic reference spurious tones, which are nonidealities (mainly mismatches) in the charge pumps of both PLLCK and PLLIN.

These limitations can be minimized by improving the sizing of the circuits, by enhancements in the circuit topologies, and by careful layouts. Also, some of these limitations are more severe than others. For example, the deterministic reference spurs are not problematic, since they can be easily separated from the actual performance of the ADC under test. In this work, we achieve a worst-case (for three measured samples) SFDR as high as 41.4 dB for an analog input frequency of about 227 MHz with differential amplitude of 600 mV_{pp}. The SFDR of the generated analog input signal is also dependent on the supply voltage, since reducing this (which is the trend for newer CMOS technologies) equally reduces the voltage headroom available to keep the active devices operating in saturation. In other words, reducing the supply voltage increases the distortion of a given circuit topology, maintaining the same signal swing, unless topology changes (if viable) are made.

The phase noise (or jitter) present in both the output of two PLLs were not measured due to reduced number of I/O pins. By post-layout simulations, we can estimate the integrated rms jitter (above 1 MHz offset) of PLLCK as 1.5 ps, as indicated in Table 4. This result, however, cannot be compared with those of other works, since these works only address the analog input signal generation.

Table 4 – Performance summary and comparison with prior works.

		This Work	[9]*	[10]*	[11]*	[12]
Technology	[μm]	0.13	0.13	0.13	0.8	0.35
Area	[mm^2]	0.052	0.51†	0.186	0.833	0.66
Power	[mW]	26.0	39.5	4.04	36.5	N/A
Supply Voltage	[V]	1.2	1.4	1.2	N/A	3.3
ADC Input Voltage	[mV$_{pp}$]	600	149	228	N/A	-6 dBFS
ADC Input Freq.	[MHz]	227	312	10	40	0.017
SFDR	[dB]	41.4§	25.3	74.1	65.4‡	$>$76
ADC Clock Freq.	[MHz]	465	N/A	N/A	N/A	6.144
ADC Clock Jitter	[ps]	1.5**	N/A	N/A	N/A	N/A

* Do not deal with the clock signal generation.
† Area of the read-only memory not included.
‡ SFDR measured at 1 MHz frequency.
§ Ignoring PLLs reference spurs.
** Jitter rms integrated above 1 MHz and estimated from simulation.

CONCLUSIONS

In this paper we present an overview of challenges in testing ADCs at high frequencies, which will be a hot topic in near future, due to the continuous advances of CMOS technologies. We review the advantages and disadvantages of BIST approaches and show that BIST can be a promising solution for functional and dynamic testing of high speed ADCs.

We present a fully integrated BIST technique, together with experimental results, targeting high-frequency and moderate resolution ADCs. This fully integrated, low cost, and reconfigurable architecture for coherent self-testing of high speed ADCs is based on two synchronized PLLs, one to synthesize the analog input signal and another to synthesize the clock signal for the ADC under test. This synchronization is a key feature of the proposed approach, since it allows coherent sampling. With coherent sampling, the digital output data of the converter are well-behaved and their spectrum is unambiguous, since it is not necessary to worry with spectral leakage, windowing, etc. Hence, with a reduced record length and a relatively low-complexity DSP hardware, it is feasible to do a reliable spectral analysis to assess the dynamic performance of the ADC.

Even though the proof-of-concept is made with a moderate resolution converter, the method proposed can be extended to low- and high-resolution ADCs. The proposed BIST architecture for ADCs is reconfigurable: it is possible to synthesize different analog input and clock frequencies by simply changing

the frequency dividers values related to the PLLs. The frequency ranges depend on the locking ranges of the PLLs. The complete BIST system has been implemented in a 0.13 μm CMOS technology and experimentally evaluated to validate the proposed method.

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Luis B. Oliveira was born in Lisbon, Portugal, in 1979. He graduated with a degree in electrical and computer engineering, and a Ph.D. degree, in 2002 and 2007 respectively, from Instituto Superior Técnico (IST), Technical University of Lisbon. In 2007, he joined the teaching staff of the Department of Electrical Engineering of Faculdade de Ciências e Tecnologia, Universidade Nova de Lisboa, and is currently a researcher at CTS-UNINOVA.
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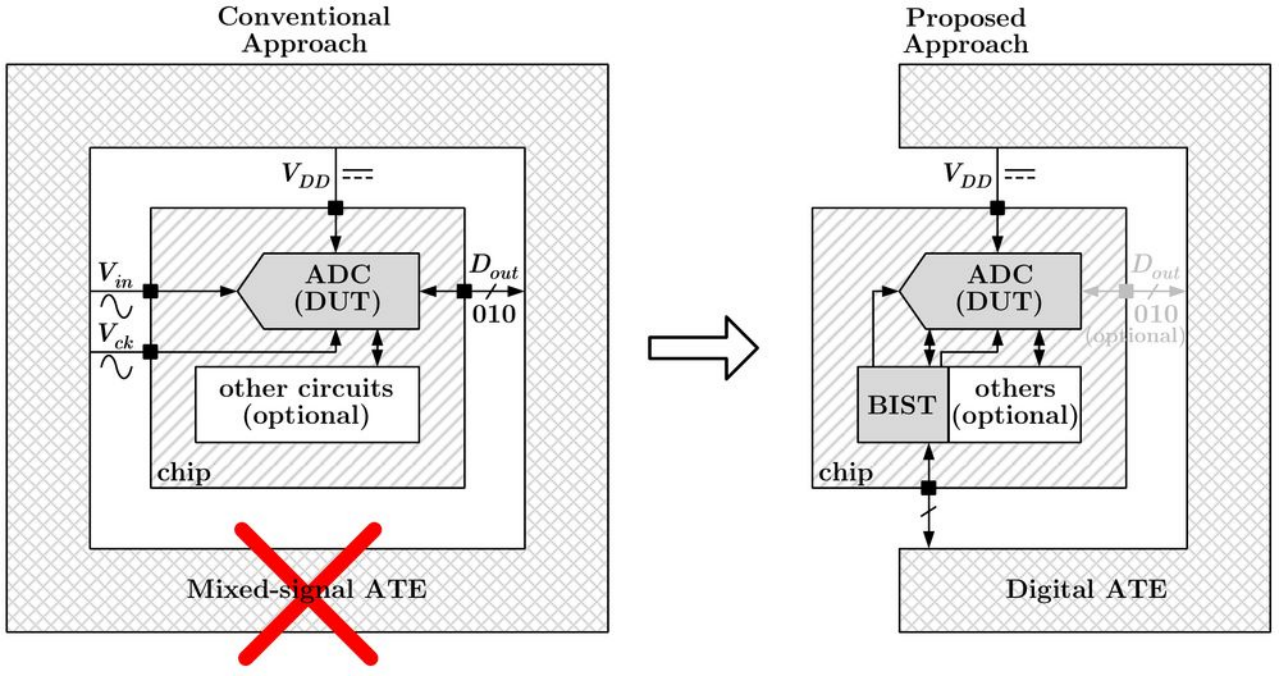
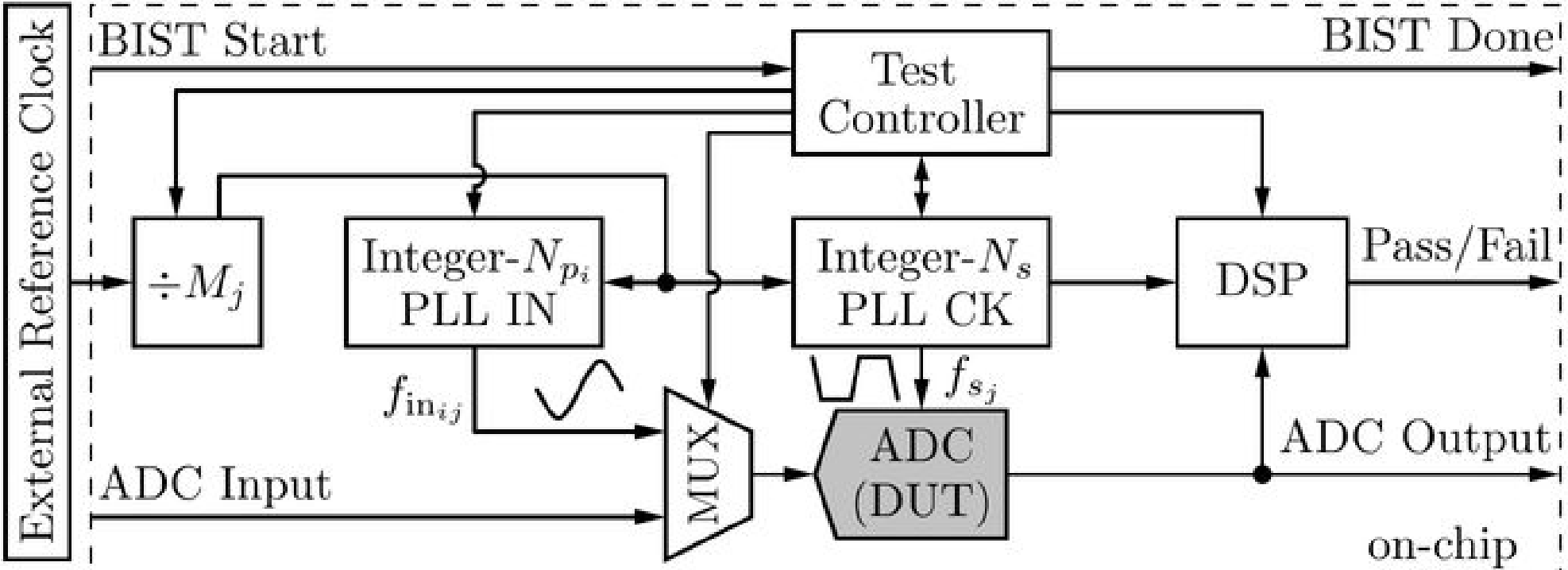
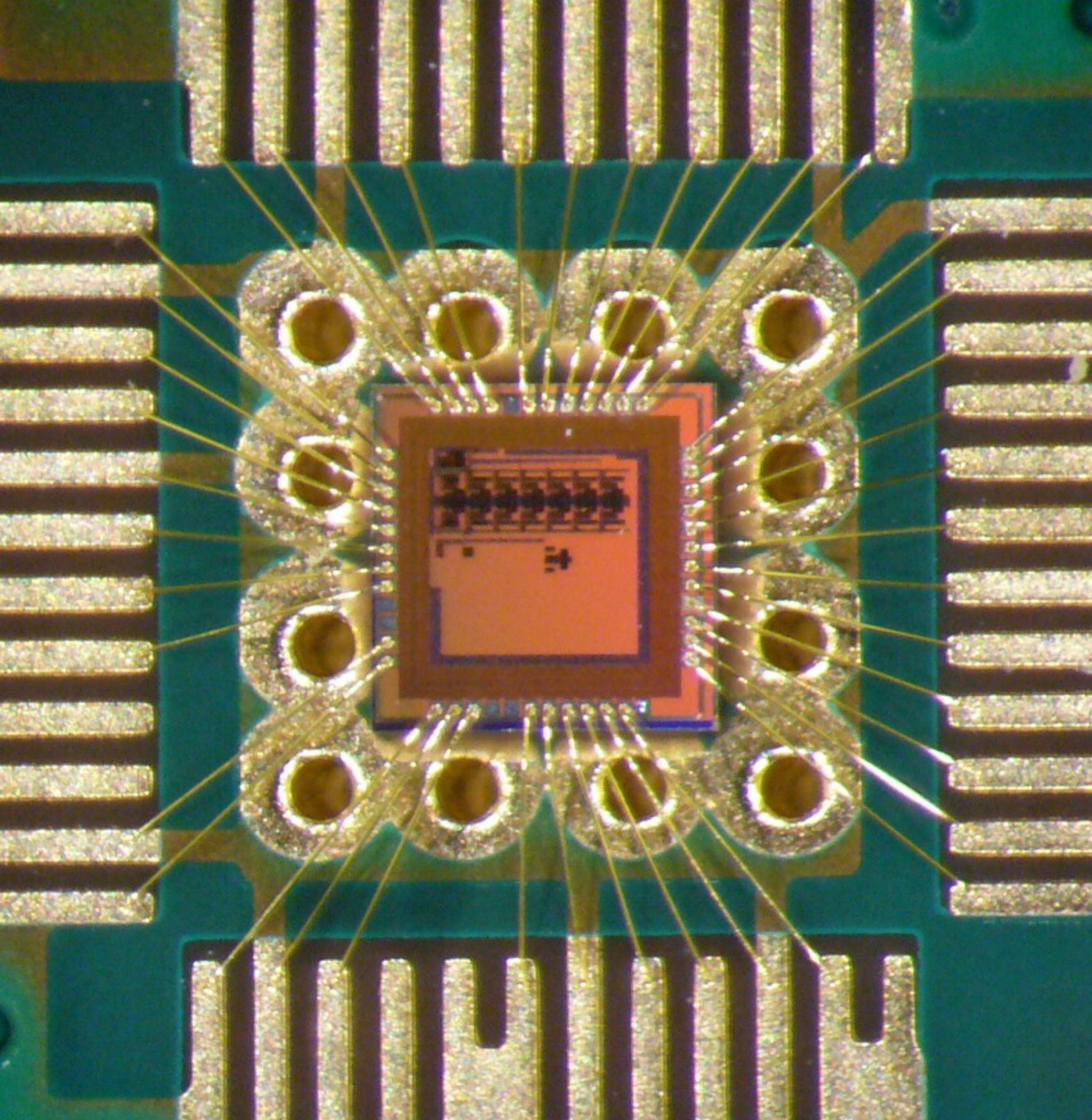

Conventional Approach
V_{DD}
V_{in}
V_{ck}
ADC (DUT)
D_{out}
010
other circuits (optional)
chip
Mixed-signal ATE
Proposed Approach
V_{DD}
ADC (DUT)
D_{out}
010
(optional)
BIST
others (optional)
chip
Digital ATE


External Reference Clock
BIST Start
BIST Done
Test Controller
$\div M_j$
Integer-N_{p_i} PLL IN
Integer-N_s PLL CK
DSP
Pass/Fail
$f_{\text{in}_{ij}}$
f_{s_j}
MUX
ADC (DUT)
ADC Output
ADC Input
on-chip



ADC BIST
Project
REVA 08/2013
ES LO JG/UNINOVA

Biasing (IREFs)

Configurable switches

DIVREF DIVIN VCOIN VCOCLK RST ADC

JP8
Closed:
1st run
Open:
2nd run

ADC
VDD_ANA

ADC
VDD_DIG

PLLCLK
VDD_ANA

PLLIN
VDD_ANA

U1 ADP1708
U2 ADP1708
U4 ADP1708
U5 ADP1708
U6 ADP1708

ADT1-1WT

AIN

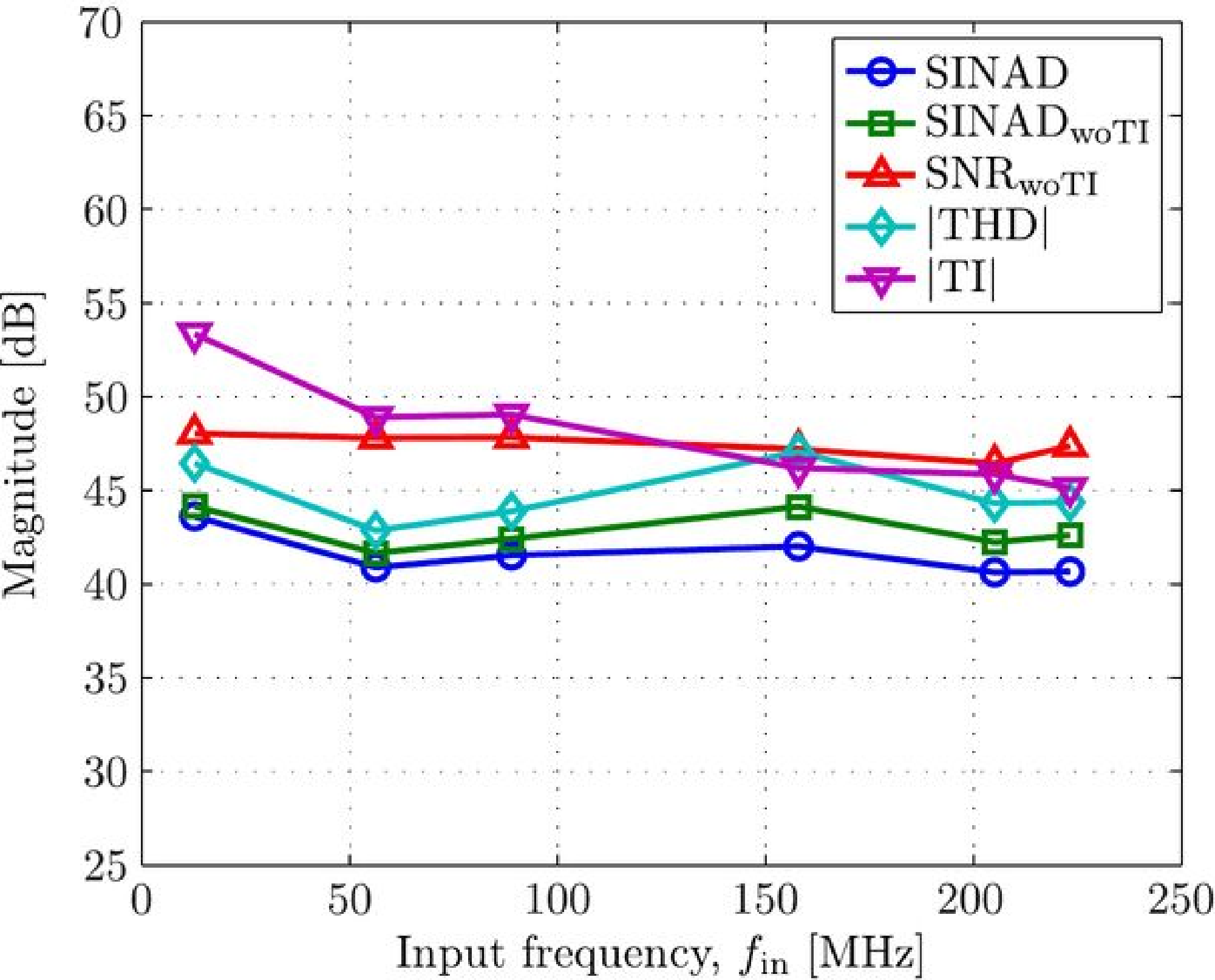
CLK

CLK_OUT

4V_VDD

GND

E575912


70
65
60
55
50
45
40
35
30
25
0
50
100
150
200
250
Magnitude [dB]
Input frequency, f_{in} [MHz]
SINAD
$\text{SINAD}_{\text{woTI}}$
SNR_{woTI}
|THD|
|TI|

Advantages	Disadvantages
vertical testability (wafer to system)	area overhead
high diagnosis resolution	performance penalties
full-speed testing	additional design time & effort
reduced need for external test equipment	additional risk to project
reduced test development time & effort	difficulty to reach full accuracy
reduced manufacturing test time & effort	
reduced time-to-market	

$f_{\text{ref}} \equiv 4$ MHz		$\hat{f}_{s_1} \equiv 250$	$\hat{f}_{s_2} \equiv 500$	$\hat{f}_{s_3} \equiv 1000$
$N \equiv 6$ bits	$N_s = 256$	$M_1 = 4$	$M_2 = 2$	$M_3 = 1$
		$f_{s_1} = 256$	$f_{s_2} = 512$	$f_{s_3} = 1024$
$\hat{f}_{\text{in}_1}/f_s \equiv 1/2$	$N_{p_1} = 127$	$f_{\text{in}_{11}} = 127$	$f_{\text{in}_{12}} = 254$	$f_{\text{in}_{13}} = 508$
$\hat{f}_{\text{in}_2}/f_s \equiv 1/4$	$N_{p_2} = 63$	$f_{\text{in}_{21}} = 63$	$f_{\text{in}_{22}} = 126$	$f_{\text{in}_{23}} = 252$
$\hat{f}_{\text{in}_3}/f_s \equiv 1/8$	$N_{p_3} = 31$	$f_{\text{in}_{31}} = 31$	$f_{\text{in}_{32}} = 62$	$f_{\text{in}_{33}} = 124$

* All frequencies are in MHz or MS/s.

Testing case*	H3 [dB]	TI spur [dB]
1) External input and clock	-48.3	-44.4
2) Internal input and clock	-41.4	-42.2

* Obtained from the measured output spectra (512 points) of one of the test samples at $f_s = 464.64$ MS/s ($= 256 \times 3.63/2$ MHz), $f_{\text{in}} = 226.875$ MHz ($= 125 \times 3.63/2$ MHz) with $V_{\text{in}} \approx -2.5$ dBFS for the two cases.

		This Work	[9]*	[10]*	[11]*	[12]
Technology	[μm]	0.13	0.13	0.13	0.8	0.35
Area	[mm^2]	0.052	0.51†	0.186	0.833	0.66
Power	[mW]	26.0	39.5	4.04	36.5	N/A
Supply Voltage	[V]	1.2	1.4	1.2	N/A	3.3
ADC Input Voltage	[mV$_{pp}$]	600	149	228	N/A	-6 dBFS
ADC Input Freq.	[MHz]	227	312	10	40	0.017
SFDR	[dB]	41.4§	25.3	74.1	65.4‡	$>$76
ADC Clock Freq.	[MHz]	465	N/A	N/A	N/A	6.144
ADC Clock Jitter	[ps]	1.5**	N/A	N/A	N/A	N/A

* Do not deal with the clock signal generation.
† Area of the read-only memory not included.
‡ SFDR measured at 1 MHz frequency.
§ Ignoring PLLs reference spurs.
** Jitter rms integrated above 1 MHz and estimated from simulation.