**Miguel Alexandre Leandro Castilho**

Licenciado em Ciências da Engenharia Eletrotécnica e de Computadores

# Design of a Reference Buffer for a Delta-Sigma ADC with Current DAC

Dissertação para obtenção do Grau de Mestre em
**Engenharia Eletrotécnica e de Computadores**

Orientador: Prof. Dr. Nuno Filipe Silva Veríssimo Paulino, Prof. Auxiliar, Universidade Nova de Lisboa
Co-orientador: Dr. João Luís Alvernaz de Melo, Senior Mixed Signal Design Engineer, Adesto Technologies

Júri

Presidente: Prof. Dr. Luís Filipe Lourenço Bernardo, FCT-UNL
Arguente: Prof. Dr. João Pedro Abreu de Oliveira, FCT-UNL
Vogal: Prof. Dr. Nuno Filipe Silva Veríssimo Paulino, FCT-UNL

FACULDADE DE CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

**Setembro, 2019**

**Design of a Reference Buffer for a Delta-Sigma ADC with Current DAC**

*To my beloved family.*

# Acknowledgements

I would like to thank Professor Nuno Paulino and João Melo for their support, advising and supervising during the development of this thesis. With their help, I was capable of overcoming all the problems that I faced, and I also learn a lot of things while they help me, for they teach me to see the things from a different perspective.

I would also like to thank my friends and colleagues, that support me during this journey, in special to André Toste, Bruno Ambrósio, Carlos Garcia, and José Curva, for all the funny moments, and also for their encouragement and help.

Last but not the least I would like to thank my family, in special to my parents for all of their support during my academic path, because without them this would not be possible.

# ABSTRACT

In analog to digital conversion, it's necessary to provide a reference voltage to the Analog to Digital Converter (ADC), in order to quantify the input signal. However, as the ADC has a switch constantly commuting on its input it will cause perturbations on the reference voltage provided by the Bandgap circuit. Thus, it will interfere with the normal behaviour of the Bandgap circuit, which will longer be capable of provide the desired reference voltage.

Besides, if the reference voltage is not constant in the desired value the output code generated by the ADC will have errors.

In order to avoid conversion errors it will be needed to introduce a buffer between the Bandgap and the ADC. Thus, taking advantage from the characteristics of the buffer (low output impedance, high input impedance and unitary gain) the system will be capable of recover from the perturbations introduced by the ADC in the reference voltage.

Therefore, in this thesis are studied some of the already existing architectures of buffers, in order to see the advantages and disadvantages of each one. This way were chosen the best three architectures from a theoretical point of view, to implement and simulate, to obtain all the needed information in order to better compare them.

**Keywords:** Buffer, ADC, Bandgap, Unitary gain, Low power consumption, Reference voltage.

# Resumo

Em conversão de analógico para digital é necessário fornecer uma tensão de referência ao ADC de forma a quantificar o sinal de entrada. Contudo, como o ADC tem um interruptor a comutar constantemente na sua entrada vão ser introduzidas perturbações na tensão de referência fornecida pelo circuito de Bandgap. Assim, o normal funcionamento do circuito de Bandgap vai ficar em causa, o que vai impossibilitar o fornecimento da tensão de referência desejada.

Alem disso, se a tensão de referência for diferente do desejado então o código na saída do ADC vai apresentar erros.

De forma a evitar erros de conversão será necessário introduzir um buffer entre o Badgap e o ADC. Portanto, ao tirar partido das caracteirísticas do buffer (baixa impedância de saída, alta impedância de entrada, e ganho unitário) o sistema será capaz de recuperar das perturbações introduzidas pelo ADC na tensão de referência.

Portanto, nesta dissertação são estudadas algumas arquiteturas de buffers já existentes, para ver quais são as vantagens e desvantagens de cada uma. Desta forma foram escolhidas as três melhores arquiteturas do ponto de vista teórico, para implementar e simular, para obter toda a informação necessária de forma a compará-las melhor.

**Palavras-chave:** Buffer, ADC, Bandgap, Ganho unitário, Baixo consumo energético, Tensão de referência.

# Contents

# List of Figures

# List of Tables

# Acronyms

AC      Alternating Current
ADC      Analog to Digital Converter

BdFVF    Bulk-driven FVF
BFVF     Buffered FVF

CAFVF    Cascaded FVF
CD       Common Drain
CfLDO    Capacitor free LDO
CMRR     Common mode rejection ratio
CS       common source

DAC      Digital to Analog Converter
DC       Direct Current
DFVF     FVF Differential Structure

FVF      Flipped Voltage Follower

GBW      Gain Bandwidth Product

LDO      Low Drop-out
LSFVF    Level Shifted FVF

OA       Operational Amplifier
OSR      Oversampling Ratio
OTA      Operational Transconductance Amplifier

PSRR     Power Supply Rejection Ratio

QFG        Quasi-Floating Gate


SoC        system-on-chip
SSF        Super Source Follower
SsLDO      Shunt-series LDO                                    *


THD        Total Harmonic Distortion
THD+N      Total Harmonic Distortion Plus Noise


Wbb        Wide bandwidth buffer

1

# Introduction

This Chapter describes the main features of a voltage buffer as well as its importance in integrated circuit. It also explains the purpose of this project and the special importance of a buffer in analog to digital conversion. Finally, a brief resume of the contents present in each Chapter of this thesis is presented.

## 1.1 Context and Motivation

A voltage buffer is a circuit that presents three main features: low output impedance, high input impedance and unitary gain. These characteristics make this kind of circuits very useful for applications where it's necessary to connect two different circuits, for the signal to be transferred without one circuit affecting the behaviour of the other one. This can occur due to the large amount of current required when the delta-sigma ADC start the conversion process, which will cause a perturbation in the reference voltage. In analog to digital conversion, the ADC compares the input voltage to a reference voltage to produce the digital binary output code. So if the reference voltage has perturbations, then the generated code may be wrong, which may cause unwanted behaviours on the system where the ADC is inserted.

Figure 1.1 is a high-level representation of a buffer that can be represented as an amplifier with an unitary gain, or it can also be represented with a voltage follower, and with an ideal opamp.

This project consists in the design of a reference buffer for a delta-sigma ADC with current Digital to Analog Converter (DAC). To do so, it will be necessary to study different approaches and see the benefits and the disadvantages of using each one. After that, it's necessary to choose the approach that gives the best results according to the desired specifications, presented in Table 1.1.

(a) Simple buffer.                    (b) Opamp buffer.

Figure 1.1: High level representation of a buffer.

These specifications are very restricted, since the delta-sigma ADC is already implemented and according to that implementation it will be needed to build a buffer capable of achieve such requirements.

Table 1.1: Buffer design specifications.

| | |
|---|---|
| Bandwidth | $100 - 200 \, MHz$ |
| Technology | UMC $130 \, nm$ |
| Reference Voltage | $1.2 \, V$ |
| Supply Voltage | $2.5 \, V$ |
| Output Impedance (DC) | $< 500 \, \Omega$ |
| Biasing Current | $< 200 \, \mu A$ |
| $\eta$ | $\geq 30 \, \%$ |
| Positive Power Supply Rejection Ratio (PSRR) | $> 40 \, dB$ |
| $V_{Ns}$ | $< \dfrac{1.2}{2^{12}} \sqrt{OSR}$ |
| OSR | 100 |

In Table 1.1 $V_{Ns}$ represents the noise of the system and $\eta$ represents the efficiency of the system. As the supply voltage and the reference voltage of the system have different values it isn't possible to achieve an efficiency of 100%. Thus, in an ideal situation, the maximum efficiency attainable is $\eta = \dfrac{1.2 \times i}{2.5 \times i} \times 100 = 48\%$. Therefore, the results displayed on the last chapters are normalized, which means that 48% is equivalent to 100%.

## 1.2   Main Contributions and Problem Approach

The purpose of this project is to implement a system capable of provide a stable reference voltage to the delta-sigma ADC. To do so it is needed to introduce a buffer between the Bandgap and the ADC. With such a system it's assured that the reference voltage provided by the Bandgap circuit is not affected by the ADC. Since the buffer will be capable of recover from the perturbations that the ADC will cause on its output voltage.

Thus, the first step to do was stablish the conditions in which the circuits will be implemented and simulated. Beforehand, it was noticed that was necessary to use an error amplifier on the feedback of the buffer, in order to the voltage at the output of the buffer be equal to the reference voltage provided to the system. Besides, the error amplifier also

helps to increase the positive PSRR, which means that greater gain of the error amplifier results in a greater PSRR.

In Figure 1.2 is shown an high level representation of the system after adding the amplifier to the feedback of the buffer.
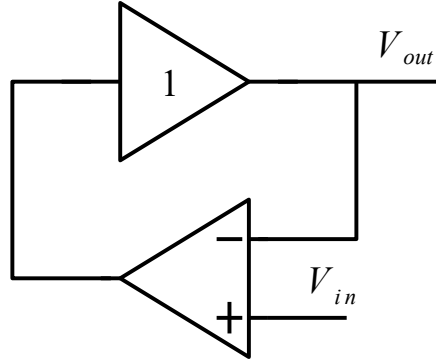


Figure 1.2: Buffer with error amplifier.

Since this buffer is being projected to provide a reference voltage for a delta-sigma ADC with current DAC is also needed to take that into account. Thus, in Figure 1.3, is an high level representation of the system after adding the DAC. As this is a circuit that receives digital signals controlled by a clock, it will introduce perturbations in the reference voltage, which allows to simulate the behaviour of the ADC.
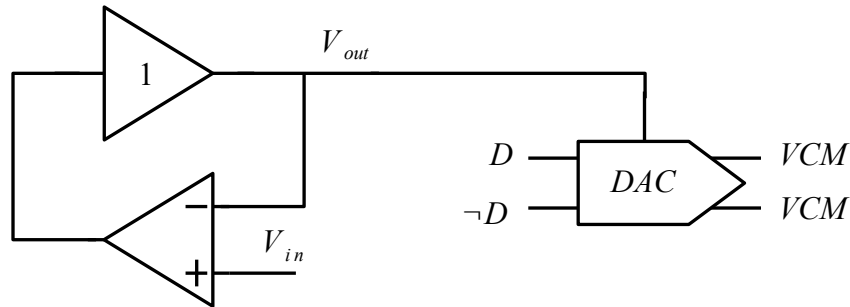


Figure 1.3: Buffer with error amplifier providing a reference voltage to a DAC.

## 1.3 Thesis Structure

This thesis is structured in five chapters, where are presented the most relevant aspects for the development of this project.

In the Chapter 1 are presented the fundamental aspects of a buffer and the main goals to achieve. In Chapter 2 are introduced some of the already existing architectures, as well as a brief theoretical analysis of them. In Chapter 3 are selected the best three architectures from the theoretical point of view, and are explained the methodologies

3

used to implement those architectures. In Chapter 4 are displayed the results obtained form the architectures defined in Chapter 3 and is also done a comparison between those architectures in order to see the advantages and disadvantages of each one. Finally, in Chapter 5 are summarized all the considerations and methodologies used and is also suggested some work to develop as a way to improve this project.

# 2

## STATE OF THE ART

In this chapter some of the already existing topologies of buffers will be studied. In each section a theoretical analysis of the buffer presented will be made, in order to understand its main features such as the gain, output impedance, noise and output swing. After that, a coarse sizing will be made, in order to see the energetic efficiency of each topology for a certain output impedance. Lastly, at the end of this chapter, a comparison between the different topologies will be made in order to see which are the advantages and disadvantages of each topology.

## 2.1 Common Drain (CD) Amplifier

A Common Drain (CD) amplifier (Figure 2.1) is the simplest possible circuit that works as a voltage buffer. However, it has a great disadvantage, because the current through transistor $M_1$ is dependent of the output current [1], and the gain of the circuit can be less than one for resistive loads [2]. Therefore, if it is desired to obtain a small output impedance, is necessary to increase the aspect ratio of $M_1$, resulting in a large power consumption [1]. Another disadvantage of this circuit is the limited sourcing capability by the biasing current, and the absence of linearity in the output [3]. The main advantage of this circuit is its simplicity and the capability of sinking large current from the load [2].

Analysing this circuit, it can be concluded that the output impedance is low and the gain of the circuit is approximately unitary.

$$R_O = \frac{1}{gm_1 + gds_1} \tag{2.1}$$

$$A_V(s = 0) = \frac{gm_1}{gds_1 + gm_1} \tag{2.2}$$
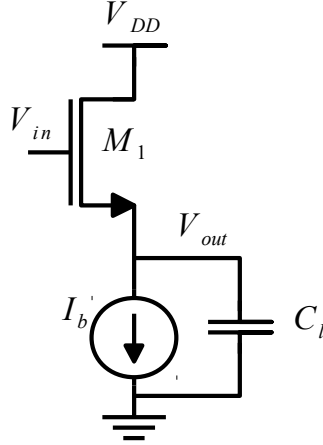
Figure 2.1: Common Drain Amplifier.

Based on: [2].

With the gain expression, it is possible to obtain the follow-up error expression, using the the following method:

$$A_V(s = 0) = \frac{gm_1}{gds_1 + gm_1}$$
$$\iff A_V = \frac{1}{\frac{gds_1}{gm_1} + 1} \tag{2.3}$$
$$\iff A_V = \frac{1}{F_E + 1}$$

$$F_E = \frac{gds_1}{gm_1} \tag{2.4}$$

It's also possible to see by the analysis of the circuit that the CD has one zero and one pole. Doing a stability analysis, it can be observed that the circuit is always stable, because both the pole and the zero are stable (Figure 2.2).
 Using the exact expression of the gain ($A_v(s \neq 0)$) can be calculated the expression of the pole, and that is what will define the bandwidth of the circuit.

$$\omega_p = \frac{gm_1 + gds_1}{C_l + csb_1 + cgs_1} \tag{2.5}$$

Finally, the noise and the output swing of the circuit was calculated.

$$V_{Nin}^2 \approx \frac{\gamma 4 K_B T}{gm_1} \tag{2.6}$$

$$\Delta Vo_{pp} = V_{dd} - 2V_{dsat} \tag{2.7}$$

The following structures are based on the source follower, and some changes are made to the arrangement of the circuit to reduce its disadvantages.
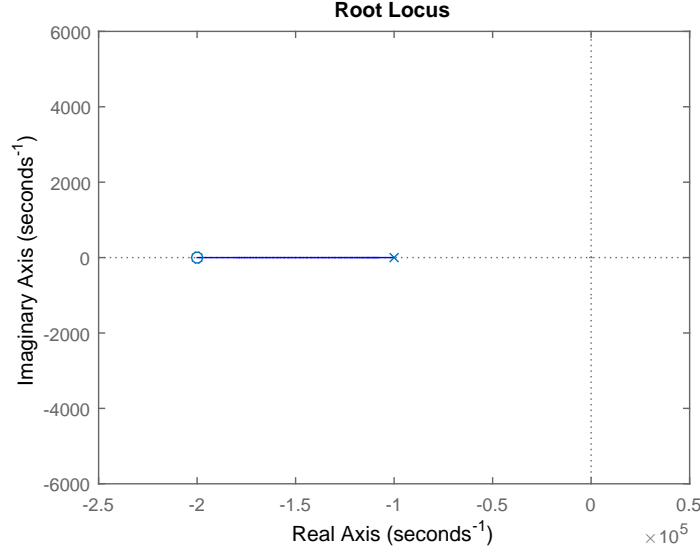
Figure 2.2: Root Locus of the CD.

## 2.2 Flipped Voltage Follower (FVF)

The Flipped Voltage Follower (FVF) (Figure 2.3) allows a constant current through the transistor $M_1$ due to the current source $I_b$, and under this condition, the unitary gain is achieved independently of the output current [1], [2]. By adding transistor $M_2$, there is no longer the previous limitation of sourcing current. However, this change limits the sinking capability of the FVF because of the biasing current [1]-[3]. The big advantage of using a FVF is the aptitude of using a very low voltage supply. Another improvement can be done to this circuit, adding a resistor on the closed loop between the gate of $M_2$ and the drain of $M_1$ [4], resulting in a better bandwidth.

The main application of the FVF is as a voltage buffer with Direct Current (DC) level shifting [5], but it is also used as a current sensing element.

By analysing the circuit, the expressions of the output impedance and the expression of the gain are obtained. Comparing the output impedance of the FVF with the impedance of the CD it can be observed that the FVF impedance is lower. Plus, it's also possible to obtain a unitary gain.

$$R_O \approx \frac{1}{gm_1 gm_2 rds_1} \tag{2.8}$$

$$A_V(s=0) = \frac{gm_1 gm_2}{gm_2 gds_1 + gds_1 gds_2 + gm_1 gm_2} \tag{2.9}$$

By the expression of the gain it's possible to obtain the follow-up error expression.

$$F_E = \frac{gds_1}{gm_1} + \frac{gds_1 gds_2}{gm_1 gm_2} \tag{2.10}$$

It's also possible to see that the FVF has a lower noise than the CD although the FVF has

7
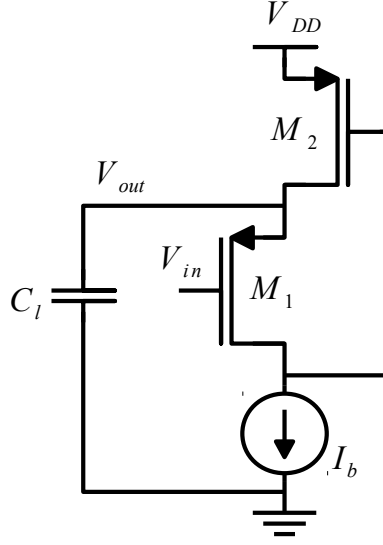
Figure 2.3: Flipped Voltage Follower.

Based on: [2].

two transistors, but as the transistor $M_1$ is cascode its noise is negligible. In the worst case scenario the output swing is lower than the CD output swing.

$$V_{Nin}^2 \approx \frac{\gamma 4 K_B T g m_2}{(g m_1 g m_2 r d s_1)^2} \tag{2.11}$$

$$\Delta V o_{pp} = V_{dd} - 3 V_{dsat} \tag{2.12}$$

With regard to stability, it's also possible to conclude that the system is always stable due to its two stable poles and two stable zeros, which can be visualized in Figure 2.4.
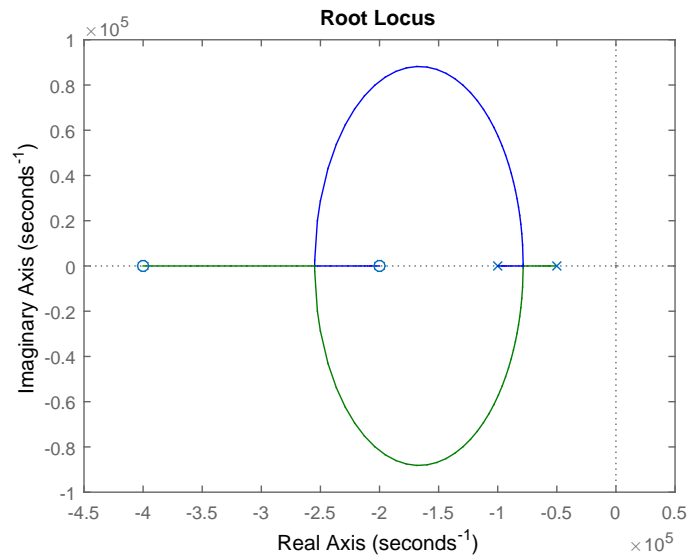


Figure 2.4: Root Locus of the FVF.

Using the exact expression of the gain it's possible to calculate the existing poles and

comparing both expressions it's possible to obtain the dominant pole.

$$\omega_p \approx \frac{gm_2}{cgd_1 + cdb_1 + cgs_2 + cgd_2} \tag{2.13}$$

## 2.3   FVF Differential Structure (DFVF)

The FVF Differential Structure (DFVF) is a FVF based circuit and it presents a Class-AB behaviour. On the DFVF the output is available as either current or voltage, and this characteristic can be very advantageous, since it allows a simplification of the circuit as well as a reduction in noise and in the number of poles and zeros [2].
The DFVF can be used to build low-power low-voltage Class-AB output stages and can be used as a transconductance Operational Amplifier (OA). As a transconductance OA, the DFVF achieves a large Common mode rejection ratio (CMRR) [2], and if two DFVF are used a fully differential behaviour can be obtained.
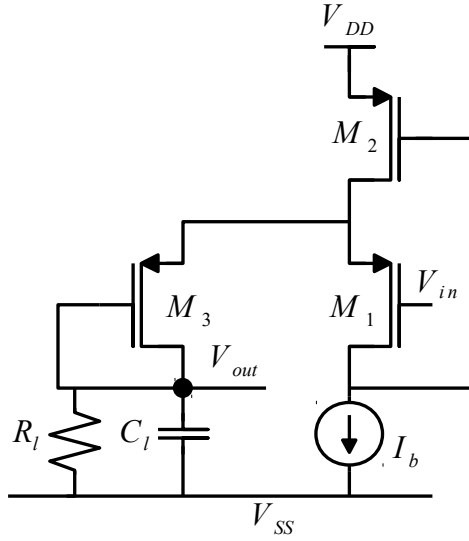


Figure 2.5: FVF Differential Structure.

Based on: [2].

Using the small signal analysis, it's possible to obtain the expressions of the gain and output impedance. Comparatively to the FVF circuit, the gain remains equal but the output impedance is different. However, the output impedance of the circuit remains low.

$$R_O \approx \frac{gm_1gm_2 + gds_1gm_3}{gm_1gm_2gm_3 + gm_2gm_3gds_1} \tag{2.14}$$

$$A_V(s = 0) = \frac{gm_1gm_2}{gm_2gds_1 + gds_1gds_2 + gm_1gm_2} \tag{2.15}$$

9

With the expression of the gain calculated above, it's possible to get the follow-up error expression.

$$F_E = \frac{gds_1}{gm_1} + \frac{gds_1 gds_2}{gm_1 gm_2} \tag{2.16}$$

By observation of Figure 2.5 it's possible to see that this circuit continues to have just one transistor contributing to the overall noise, the transistor $M_2$. The transistors $M_1$ and $M_3$ have a negligible noise, because they are cascode transistors. Also, by observation, it's possible to calculate the output swing.

$$V_{Nin}^2 \approx \gamma 4 K_B T gm_2 \left( \frac{gm_1 gm_2 + gds_1(gm_2 + gm_3)}{gm_1 gm_2 gm_3} \right)^2 \tag{2.17}$$

$$\Delta V o_{pp} = V_{dd} - 2V_{dsat} - V_{C_l} \tag{2.18}$$

By analysing the exact expression of the gain it's possible to see that this circuit has two zeros and three poles. So, the circuit will always be stable, since both poles and zeros are stable. By doing the root locus (Figure 2.6) it's possible to confirm that.
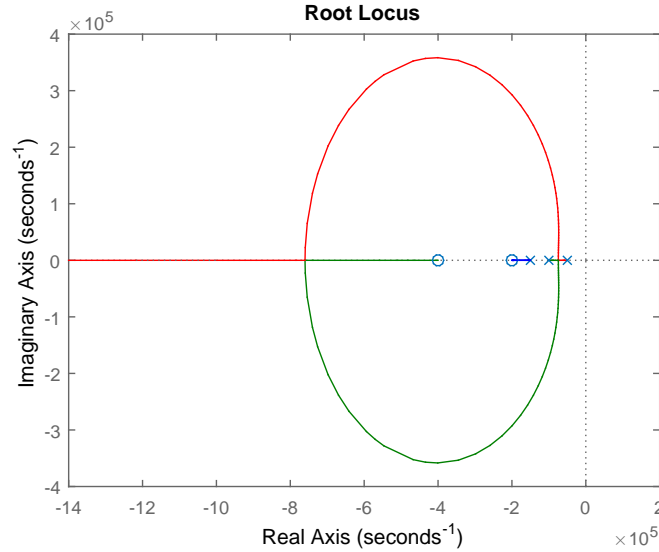


Figure 2.6: Root Locus of the DFVF.

Comparing the three expressions of the poles present in the circuit it's possible to conclude that the dominant pole is given by:

$$\omega_p \approx \frac{gm_2}{cdb_1 + cgd_1 + cgd_2 + cgs_2} \tag{2.19}$$

## 2.4 Bulk-driven FVF (BdFVF)

As a way to improve the FVF a bulk-driven transistor can be used instead of an ideal current source (Figure 2.7). This change will allow the circuit to obtain a Class-AB behaviour

instead of a Class-A behaviour, and consequently obtain a symmetrical slew rate instead of an asymmetrical slew rate [6].

To establish the bias current of the circuit is used a voltage $V_b$ that fixes the $V_{sg}$ voltage of the transistor $M_3$. To guarantee that the bias current is preserved, the node between the drain of the transistors $M_2$ and $M_3$ controls the transistors $M_1$ and $M_3$ [6]. In the case of $V_{in}$ rising too fast the voltage in this node decreases and the transistor $M_3$ starts to provide a larger current. As a consequence of that rise, the transistor $M_1$ will be turned off, and the output voltage will increase with the input voltage until the circuit reaches a balance state [6].
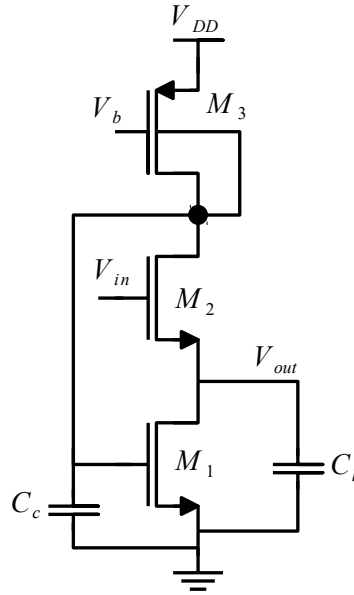


Figure 2.7: Bulk-driven FVF.

Based on: [6].

By analysing the circuit it's possible to obtain the expressions of the gain and output impedance. As expected, it exhibits unitary gain and the output impedance is also very low.

$$R_O \approx \frac{gds_2 + gds_3}{gds_1(gds_2 + gds_3) + gm_2(gds_3 + gm_1)} \tag{2.20}$$

$$A_V(s = 0) \approx \frac{gm_2(gds_3 + gm_1)}{gds_1(gds_2 + gds_3) + gm_2(gds_3 + gm_1)} \tag{2.21}$$

From the gain expression it's possible to get the follow-up error expression.

$$F_E = \frac{gds_1(gds_2 + gds_3)}{gm_2(gds_3 + gm_1)} \tag{2.22}$$

Comparing to the FVF this circuit has one more transistor, so the noise will be slightly higher. In this case, the transistors that will contribute to the noise of the circuit are the transistors $M_1$ and $M_3$, as the transistor $M_2$ is in cascode configuration its noise is

11

negligible. In relation to the output swing peak, to peak it remains equal compared to the original FVF.

$$V_{Nin}^2 \approx \frac{4K_B T (gm_1 + gm_3)}{(gm_1 gm_2 (rds_2 // rds_3))^2} \tag{2.23}$$

$$\Delta V o_{pp} = V_{dd} - 3V_{dsat} \tag{2.24}$$

From the exact expression of the gain, it's also possible to see that this circuit has two poles and two zeros, so the root locus of this circuit will be similar to the root locus of the FVF (Figure 2.4). This way the circuit will be stable, since its poles and zeros remain stable. From the expressions of the two poles that can be obtained from the exact expression of the gain, it's possible to see which is the dominant pole and get its expression.

$$\omega_p \approx \frac{gm_1}{cgd_1 + cgs_1 + cgd_2 + cdb_2 + cgd_3} \tag{2.25}$$

## 2.5   Level Shifted FVF (LSFVF)

This is another circuit that, as the one mentioned in Section 2.4, also uses a bulk-driven transistor as a current source to improve the performance of the circuit from Class-A to Class-AB (Figure 2.8). However, this one has a level shifted feedback that allows increasing the input and output swing of the circuit [7].
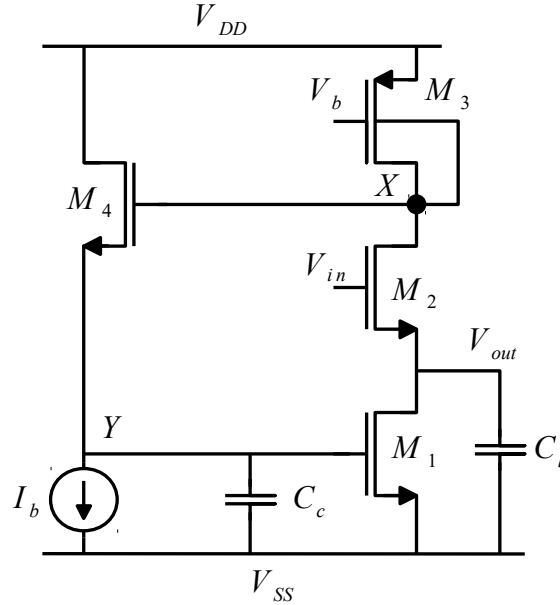


Figure 2.8: Level Shifted FVF.

Based on: [7].

In this case the feedback of the circuit is made by the transistor $M_4$ that is used as a level shifter in order to increase the swing of the circuit as referred previously. As in Section 2.4, the $V_b$ at the gate of transistor $M_3$ is used to set the bias current of transistors

$M_1 - M_3$, and also to establish the $V_{sg}$ voltage of transistor $M_3$. If the input voltage of the circuit suffers a very fast growth, then the voltage at the nodes $X$ and $Y$ will decrease. The opposite situation (fast decreasing of the input voltage) will make the voltage at node $X$ grow and, as a consequence, the transistor $M_3$ will provide a larger source current that also gives a larger current in the output capacitance $C_l$ [7].

Doing the Alternating Current (AC) analysis of the circuit it's possible to obtain the expressions of the gain and output resistance which, as expected presents a unitary gain and a low output impedance, respectively.

$$R_O \approx \frac{gds_2 + gds_3}{gds_1(gds_2 + gds_3) + gm_2(gds_3 + gm_1)} \tag{2.26}$$

$$A_V(s = 0) \approx \frac{gm_2(gds_3 + gm_1)}{gds_1(gds_2 + gds_3) + gm_2(gds_3 + gm_1)} \tag{2.27}$$

Comparing these expressions with the ones of Section 2.4 it's possible to see that they are equal. In other words, these circuits have the same gain and output impedance.

With the gain expression it's possible to obtain the follow-up error expression.

$$F_E = \frac{gds_1(gds_2 + gds_3)}{gm_2(gds_3 + gm_1)} \tag{2.28}$$

In comparison with the circuit of the Section 2.4, this circuit has one more transistor contributing to the total noise. So, the transistors that will affect the overall noise are the transistors $M_1$, $M_3$ and $M_4$. As explained previously, the noise of transistor $M_2$ is negligible, because this is a cascode transistor. Relatively to the output swing, it's expected to obtain something similar to the circuit from Section 2.4.

$$V_{Nin}^2 \approx \frac{4K_B T(gm_1 + gm_3 + gm_4)}{(gm_1 gm_2(rds_2//rds_3))^2} \tag{2.29}$$

$$\Delta V_{o_{pp}} = V_{dd} - 3V_{dsat} \tag{2.30}$$

Comparing the expressions (2.29) and (2.23) it's possible to see that the noise of both circuits is very similar and the only change is that this circuit has one more transistor that contributes to the noise.

Looking to the exact expression of the gain it's possible to see that the circuit will introduce one more zero when compared to the circuit described in Section 2.4. Therefore, this circuit has three poles and three zeros, which will result in a stable system (Figure 2.9).

By the approximated expressions of the poles, it's possible to get the expression of the dominant pole.

$$\omega_p \approx \frac{gm_1}{C_c + cgd_1 + cgs_1 + cgs_4 + csb_4} \tag{2.31}$$
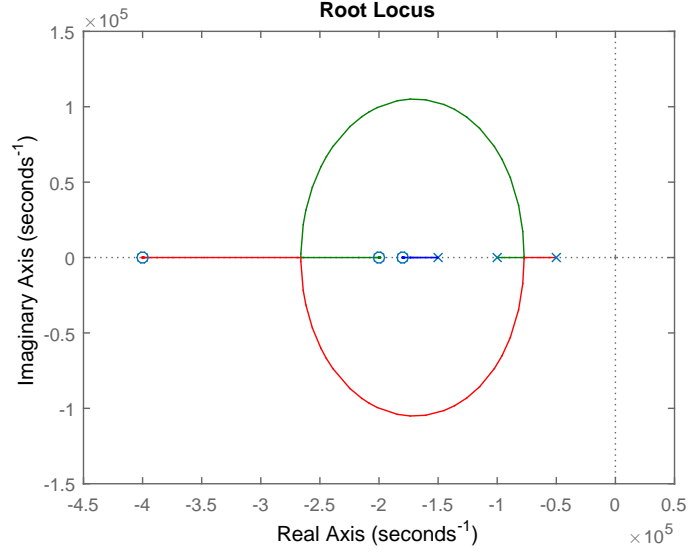
Figure 2.9: Root Locus of the LSFVF.

## 2.6   Wide bandwidth buffer (Wbb)

This buffer is based on the FVF and has the aim of keeping a small load capacitance, while at the same time provides a low power consumption and a large bandwidth, without increasing the the transistors dimensions (Figure 2.10). This is achieved through the improvement of the transconductance of the transistors using a feedback strategy [8].
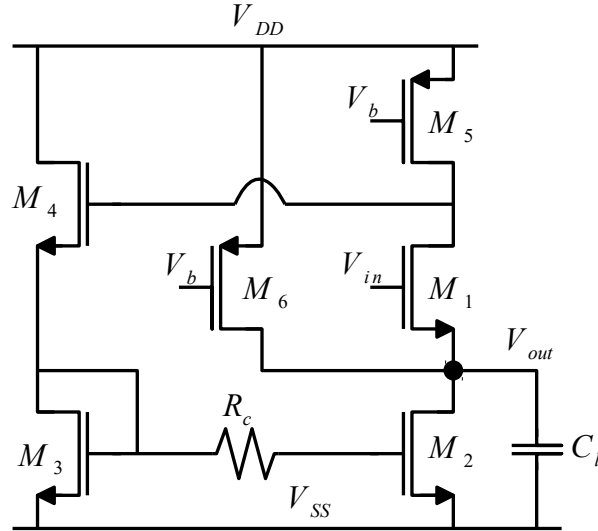


Figure 2.10: Wide bandwidth buffer.

Based on: [8].

To achieve a better bandwidth without increasing the aspect ratio of $M_1$ it's necessary to improve the transconductance of the transistor $M_2$ through the feedback loop constituted by the transistors $M_1$, $M_3$, and $M_4$. In order to obtain a linear circuit, was needed to add

an extra current source represented by the transistor $M_6$, which will provide a larger bias current to the transistor $M_2$. The resistance $R_c$ used between the gates of transistors $M_2$ and $M_3$ was used to face the peck that appears when a small load capacitance is used to obtain a larger bandwidth [8].

Through circuit analysis it's possible to achieve the approximate expressions of the circuit. As expected, an approximately unitary gain was achieved, as well as a low output impedance.

$$R_O \approx \frac{gm_3 gds_1 + gm_4 gds_1 + gm_3 gds_5 + gm_4 gds_5}{gm_1 gm_2 gm_4 + gm_2 gm_4 gds_1 + gm_1 gm_3 gds_5 + gm_1 gm_4 gds_5} \quad (2.32)$$

$$A_V(s=0) \approx \frac{gm_1 gm_2 gm_4 + gm_1 gm_3 gds_5 + gm_1 gm_4 gds_5}{gm_1 gm_2 gm_4 + gm_2 gm_4 gds_1 + gm_1 gm_3 gds_5 + gm_1 gm_4 gds_5} \quad (2.33)$$

Through the gain expression is possible to get the follow-up error expression.

$$F_E = \frac{gm_2 gm_4 gds_1}{gm_1(gm_2 gm_4 + gds_5(gm_3 + gm_4))} \quad (2.34)$$

Observing the circuit, it's possible to see that there are four transistors contributing to the noise ($M_2$, $M_3$, $M_5$ and $M_6$) , as well as the resistance $R_c$. The transistors $M_1$ and $M_4$ have a negligible noise because they are cascode transistors. The output swing will remain equal for the worst case.
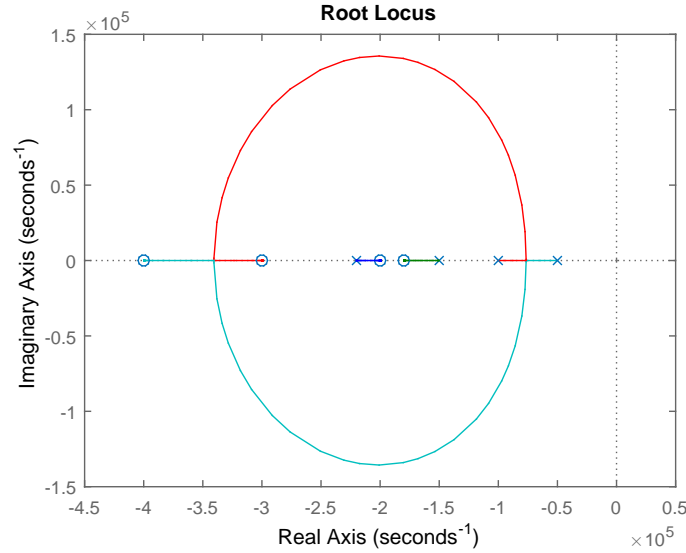


Figure 2.11: Root Locus of the Wbb.

$$V_{Nin}^2 \approx 4K_B T \left( \frac{gm_3 gds_1 + gm_4 gds_1 + gm_3 gds_5 + gm_4 gds_5}{gm_1 gm_2 gm_4 + gm_1 gm_3 gds_5 + gm_1 gm_4 gds_5} \right)^2$$
$$\left( \gamma(gm_2 + gm_3 + gm_5 + gm_6) + \frac{1}{R_c} \right) \quad (2.35)$$

$$\Delta V o_{pp} = V_{dd} - 3V_{dsat} \quad (2.36)$$

15

Analysing the exact expression of the gain, it's possible to conclude that this circuit has four poles and four zeros, resulting in a stable system, as shown in Figure 2.11.

By approximation, all the poles' expressions were calculated allowing to determine the expression of the dominant pole.

$$\omega_p \approx \frac{(1 + gm_1)gm_2gm_4 + gds_5gm_1(gm_3 + gm_4)}{(cdb_3 + cgs_3 + cgs_4 + csb_4)gm_1gm_4} \tag{2.37}$$

## 2.7 Super Source Follower (SSF)

This circuit is an update of the basic Source Follower circuit and it uses negative feedback (through the transistor $M_2$) in order to improve its linearity and its output impedance (Figure 2.12). This feedback is formed by the transistors $M_1$ and $M_2$, and due to it the drain current of $M_1$ is not affected by the output current as in the Source Follower [9]. However, this circuit has a disadvantage regarding large input signal application, since the transistors parameters will change, causing a signal distortion [9].
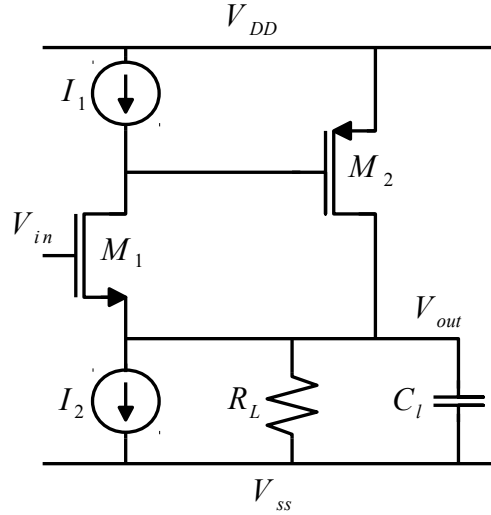


Figure 2.12: Super Source Follower.

Based on: [9].

The circuit analysis allows to obtain the expressions of the gain and of the output impedance.

$$R_O \approx \frac{gds_1}{gm_1gm_2 + gds_1(gds_2 + g_L + gm_2)} \tag{2.38}$$

$$A_V(s = 0) \approx \frac{gm_1gm_2}{gm_1gm_2 + gds_1(gds_2 + g_L + gm_2)} \tag{2.39}$$

As expected, the gain obtained is approximately unitary and the output impedance is very low. By the gain expression it's possible to achieve the follow-up error expression.

$$F_E = \frac{gds_1(gds_2 + g_L + gm_2)}{gm_2gm_1} \tag{2.40}$$

Regarding noise, both transistors and the resistance $R_L$ will affect its overall value. Comparing this circuit with the Source Follower leads to the conclusion of a smaller output swing on the present one.

$$V_{Nin}^2 \approx 4K_B T \left( \frac{gds_1}{gm_1 gm_2} \right)^2 \left( \gamma(gm_1 + gm_2) + \frac{1}{R_L} \right) \quad (2.41)$$

$$\Delta V o_{pp} = V_{dd} - 3V_{dsat} \quad (2.42)$$

By analysing the exact expression of the gain it's possible to see that this circuit has two poles and two zeros, which constitutes a stable system as can be observed in Figure 2.4. With the calculation of the approximated expressions of the poles it's possible to obtain the dominant pole expression.

$$\omega_p \approx \frac{gm_2}{cdb_1 + cgd_1 + cgd_2 + cgs_2} \quad (2.43)$$

## 2.8   Buffer with high linearity and adjustable output impedance

This circuit is an evolution of the Super Source Follower, in two aspects, linearity, and output impedance (Figure 2.13). In this circuit is added another feedback loop, so the circuit stays with two feedback loops. One loop is used to improve the linearity of the circuit while the other one is used to adjust the output impedance. This way, the output impedance depends on a resistor $R_1$ and on the size ratio of $M_2$ and $M_4$. To improve the gain of the circuit was used the resistor $R_{in}$ [9].
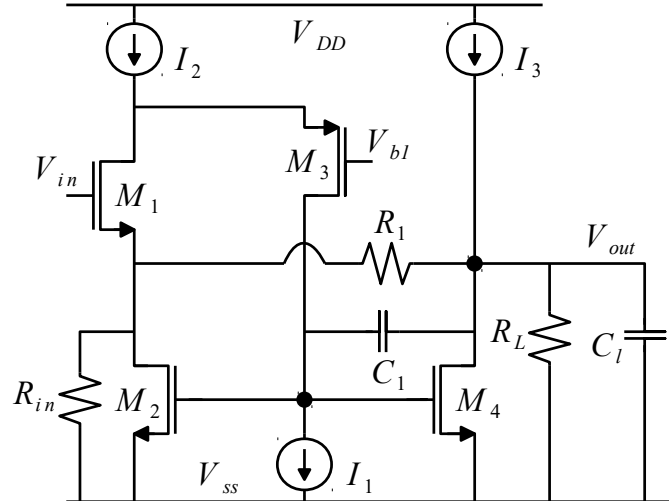


Figure 2.13: Buffer with high linearity and adjustable output impedance.

Based on: [9].

Analysing the circuit is possible to obtain the expressions of the output impedance and

gain. As expected, the gain is approximately unitary and the output impedance is low and dependent of $R_1$.

$$R_O \approx \frac{gm_2}{(g_1 + gds_4 + g_L)gm_2 + (g_1 + gds_3)gm_4} \tag{2.44}$$

$$A_V(s = 0) \approx \frac{g_1 gm_2 + (g_1 + gds_2 + g_{in})gm_4}{(g_1 + gds_4 + g_L)gm_2 + (g_1 + gds_3)gm_4} \tag{2.45}$$

Through the gain expression is possible to get the follow-up error expression.

$$F_E \approx \frac{(gds_4 + g_L)gm_2 + gds_3 gm_4}{g_1(gm_2 + gm_4)} \tag{2.46}$$

By observation of the circuit is possible to see that the transistors $M_1$, $M_2$ and $M_4$ will contribute to the overall noise, as well as the resistors $R_1$, $R_L$ and $R_{in}$. The noise of transistor $M_3$ is negligible because this transistor is folded cascode. Also, by observation, is possible to get the output swing expression.

$$V_{Nin}^2 \approx 4K_B T \left( \frac{gm_2}{g_1 gm_2 + (g_1 + gds_2 + g_{in})gm_4} \right)^2$$
$$\left( \gamma(gm_1 + gm_2 + gm_4) + \frac{1}{R_L} + \frac{1}{R_1} + \frac{1}{R_{in}} \right) \tag{2.47}$$

$$\Delta V o_{pp} = V_{dd} - 2V_{dsat} \tag{2.48}$$

Considering the exact expression of the gain is possible to see that the circuit has five
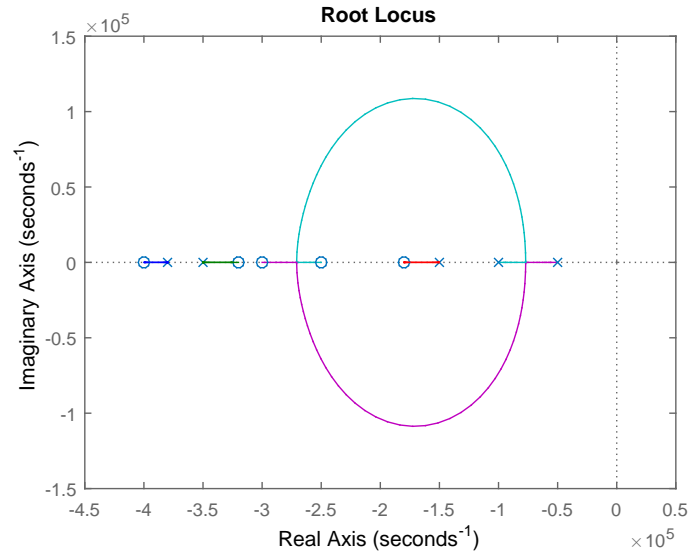


Figure 2.14: Root Locus of the buffer with high linearity and adjustable output impedance.

poles and five zeros. This constitutes a stable system as demonstrated in Figure 2.14. By

the approximated expressions of the poles is possible to achieve the expression of the dominant pole.

$$\omega_p \approx \frac{g_1(gm_2 + gm_4)}{(C_1 + cdb_4 + C_L)gm_2} \tag{2.49}$$

## 2.9  Two stage QFG buffer

This buffer introduces a technique of Quasi-Floating Gate (QFG) (Figure 2.15), without using any DC level shift from the input to the output, in order to avoid problems resulting from it, due to the temperature dependence of the DC level shifting circuits. This circuit also allows to obtain Class-AB behaviour without using any additional supply voltage [10].

The QFG technique consists in stabilize the gate voltage of one transistor from the DC point of view, but from the signal point of view this voltage can be considered a floating voltage. Is it what happens in the gate of transistor $M_2$, and in order to this be possible was added a big resistance, and a capacitor $C_{bat}$ in the gate of $M_2$ [10].
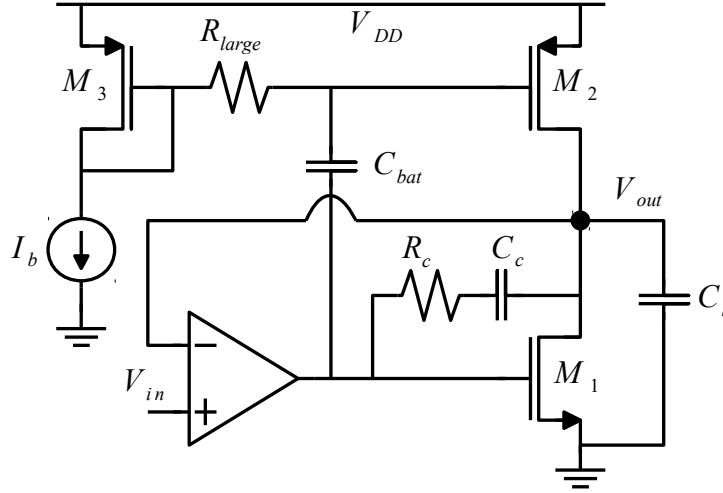


Figure 2.15: Two stage QFG buffer.

Based on: [10].

Another characteristic of this circuit is the capability to work with a small quiescent current in order to save static power, and at the same time exhibit a large slew rate due to the large output current. Case the input voltage rises too fast, the output of this circuit is also capable of follow the variation occurred, providing a large current at the load. Due to the big value of $R_{large}$ the $C_{bat}$ capacitor will act like a DC voltage, because it will not discharge fast, and this will increase the $V_{sg}$ voltage of $M_2$, which will provide the required current at the output. With the increase of the $Vsg$ voltage at $M_2$, its gate voltage decreases, and hence the drain current of $M_1$ will also decrease below $I_b$. Otherwise if the input voltage decreases, then the gate voltage of transistors $M_1$ and $M_2$ will decrease,

19

the drain current of $M_1$ will increase, and the drain current of $M_2$ will decrease, which denote the sinking capability of this circuit at the load [10].

Therefore, this kind of circuit is very useful for applications that require an accurate operation with low quiescent power consumption [10].

Using a transconductance amplifier (Figure 2.17) and doing an AC analysis in the circuit is possible to obtain the expressions of the gain and output impedance. As expected, the gain is unitary and the output impedance is low.

$$R_O \approx \frac{gout_4}{gm_1 gm_4 + (gds_1 + gds_2)gout_4} \tag{2.50}$$

$$A_V(s = 0) \approx \frac{gm_1 gm_4}{gm_1 gm_4 + (gds_1 + gds_2)gout_4} \tag{2.51}$$

In the expressions (2.50) and (2.51) the transconductances $gm_4$ and $gout_4$ represent the components of the transconductance amplifier. By analysing the gain expression calculated above is possible to get the follow-up error expression.

$$F_E \approx \frac{(gds_1 + gds_2)gout_4}{gm_1 gm_4} \tag{2.52}$$

Regarding the noise, is possible to see that this circuit has two transistors ($M_1$ and $M_2$), and two resistors ($R_c$ and $R_{large}$) that will contribute to the overall noise. By observation is also possible to calculate the output swing expression.

$$V_{Nin}^2 \approx \frac{4K_B T}{(gm_1 gm_4 Rout_4)^2}\left(\gamma(gm_1 + gm_2) + \frac{1}{R_c} + \frac{1}{R_{large}}\right) \tag{2.53}$$

$$\Delta V o_{pp} = V_{dd} - 2V_{dsat} \tag{2.54}$$

Using the exact expression of the gain is possible to see that this circuit has four poles and three zeros, which constitute a stable system (Figure 2.18). Based on the gain expression is possible to calculate the approximated expressions of the poles, and consequently achieve the dominant pole, where $C_{p4}$ represents the parasitic capacitances of the transconductance amplifier.

$$\omega_p \approx \frac{gm_1}{C_{bat} + C_c + cgd_1 + cgs_1 + C_{p4}} \tag{2.55}$$

## 2.10  Low Drop-out (LDO) regulators

The Low Drop-out (LDO) regulators are very important components for the system-on-chip (SoC) circuits because there are multiple supply voltages used for the different components that integrate the chip.

The main function of a LDO regulator is to provide the voltage supply that the other circuits need, and at the same time protect them from the disturbances that may happen on the supply voltage [11].

In the next sections, it will be observed some designs of LDO regulators.

### 2.10.1 Shunt-series LDO (SsLDO)

The Shunt-series LDO (SsLDO) regulator allows to obtain a very low output impedance and a gain approximately equal to one (Figure 2.16).

This SsLDO is divided in two control loops, one shunt section and one series section. The shunt section constituted by the amplifier $A_1$ and the transistor $M_1$ deals with fast transients, and the series section composed by the amplifier $A_2$ and transistor $M_2$ handles low frequency load current fluctuations. Besides that, on its output, there is a capacitor $C_d$ that takes care of very fast current changes [12]. After analysing this circuit it was
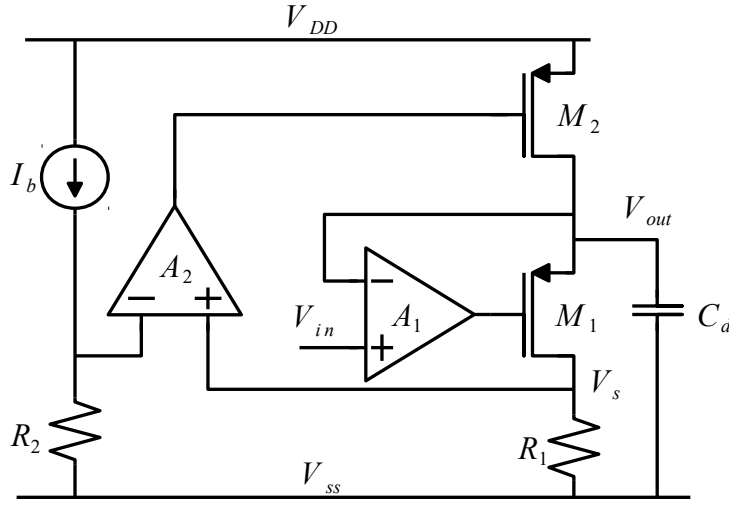


Figure 2.16: Shunt-series LDO.

Based on: [12].

possible to obtain the next expressions of the output impedance and gain, considering $A_1$ and $A_2$ as ideal amplifiers.

$$R_O \approx \frac{g_1 + gds_1}{g_1 gm_1 + A_1 g_1 gm_1 + A_2 gm_1 gm_2 + A_2 gm_2 gds_1 + A_1 A_2 gm_1 gm_2} \quad (2.56)$$

$$A_V(s = 0) \approx \frac{A_1 g_1 gm_1 + A_2 g_1 gm_2 + A_2 gm_2 gds_1 + A_1 A_2 gm_1 gm_2}{g_1 gm_1 + A_1 g_1 gm_1 + A_2 gm_1 gm_2 + A_2 gm_2 gds_1 + A_1 A_2 gm_1 gm_2} \quad (2.57)$$

In the FVF there's only one transistor that contributes to the noise but on this LDO there is also a resistor that contributes to the noise. Lastly it was calculated the output swing.

$$V_{Nin}^2 \approx \frac{4K_B T}{(A_1 A_2 gm_1 gm_2 (rds1 // R1))^2} \left( \gamma gm_2 + \frac{1}{R_1} \right) \quad (2.58)$$

$$\Delta Vo_{pp} = V_{dd} - 2V_{dsat} - V_s \quad (2.59)$$

Replacing the amplifiers $A_1$ and $A_2$ by the circuit of Figure 2.17 the gain and output impedance expressions will be calculated once again. This change is needed in order to be possible to get all the expressions of poles and zeros.
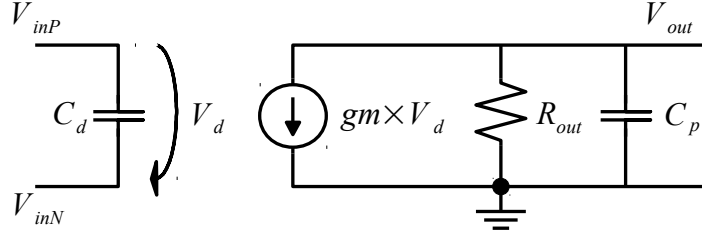
Figure 2.17: Transconductance Amplifier.

$$R_O \approx \frac{(g_1 + gds_1)gout_3gout_4}{gm_1gm_2gm_3gm_4 - gds_1gm_2gm_3gout_4} \tag{2.60}$$

$$A_V(s = 0) \approx \frac{gm_1gm_4}{gm_1gm_4 - gds_1gout_4} \tag{2.61}$$

In the expressions (2.60) and (2.61), the transconductances $gout_3$ and $gm_3$ are related to the components of $A_2$, and the transconductances $gout_4$ and $gm_4$ to the components of $A_1$. By the gain expression calculated after the change of the amplifiers by the transconductance amplifiers is possible to get the follow-up error expression.

$$F_E = \frac{gds_1gout_4}{gm_1gm_4} \tag{2.62}$$

With this change is also possible to obtain another expression of the input noise.

$$V_{Nin}^2 \approx \frac{4K_BT}{(gm_1gm_2gm_3gm_4Rout_3Rout_4(rds_1//R_1))^2}\left(\gamma gm_2 + \frac{1}{R_1}\right) \tag{2.63}$$

This expression meets the expected result, because the gain of the transconductance
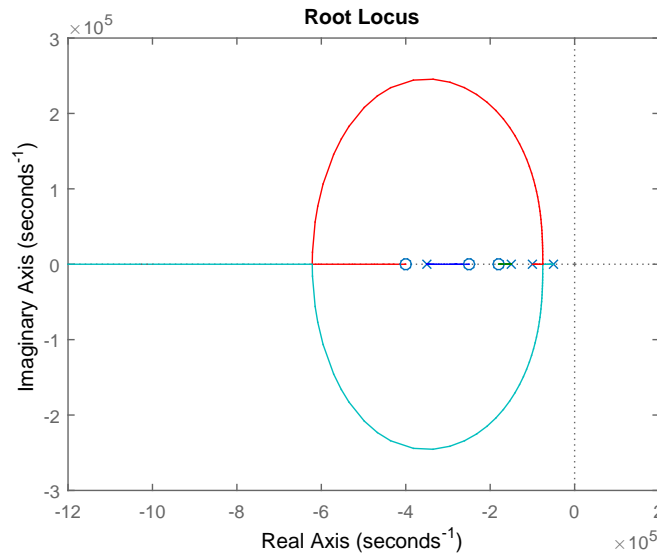


Figure 2.18: Root Locus of the SsLDO.

amplifier is $A_v = gmRout$.

From the analysis of the exact expression of the gain it is possible to conclude that this circuit has five poles and four zeros, but in order to obtain a manageable expression it will be considered that the parasitic capacitance $cgd_1$ of transistor $M_1$ is negligible, and thus simplifying the system to have four poles and three zeros. This results in a stable system as shown in Figure 2.18. Further on, if this circuit reveals itself important, then will be considered the most difficult scenario comprising the parasitic capacitances. Taking into account this simplification is possible to obtain the dominant pole expression, where $C_{p3}$ represents the parasitic capacitances of the transconductance amplifier $A_2$.

$$\omega_p \approx \frac{gm_2}{cgd_2 + cgs_2 + C_{p3}} \tag{2.64}$$

### 2.10.2 Capacitor free LDO (CfLDO)

This is a Capacitor free LDO (CfLDO) that presents an architecture with a fast and a slow loop (Figure 2.19). The circuit can be divided into three different parts: (1) a common source (CS) stage at the output, (2) a fast differential stage that has a feedback from the output stage forming the fast loop of the circuit, and (3) a slow operational amplifier that has a feedback from the output stage forming the slow loop of the circuit.

The fast loop of the circuit has the purpose of deleting the spikes caused by a step in the load, that is felt on the output of the LDO. The slow loop has the purpose of controlling the gate voltage of $M_2$ and $M_3$, that allows to stabilize the DC voltage at the output [11].
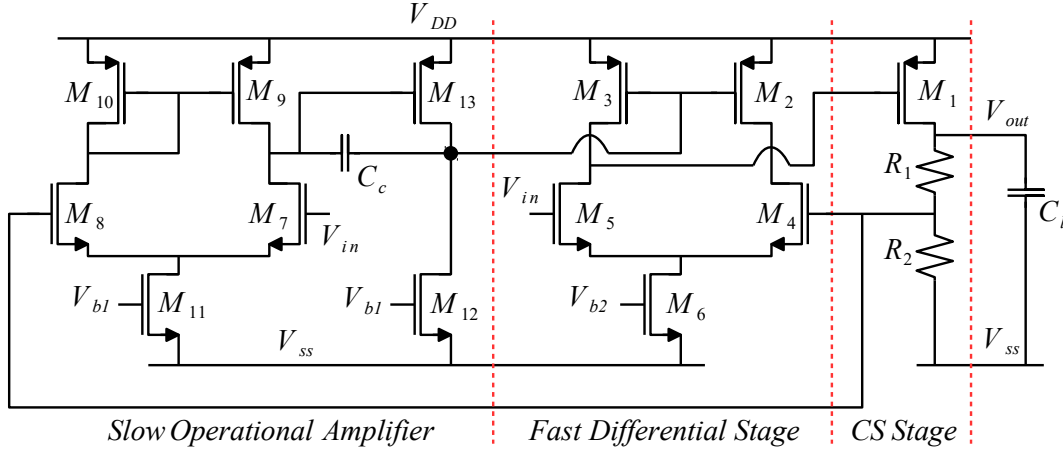


Figure 2.19: Capacitor free LDO.

Based on: [11].

To facilitate the analysis of the CfLDO stage by stage analysis was made, and the resulting expressions were combined to obtain the final expressions for the gain, output impedance and noise.

In order to obtain the gain expression of the circuit the open loop gain of each stage were calculated, and from those expressions, the closed loop gain was obtained using Mason's

rule.

$$A_{OL2}(s = 0) \approx -\frac{(g_1 + g_2)gm_1}{g_2 gds_1 + g_1(g_2 + gds_1)} \tag{2.65}$$

$$A_{OL1}(s = 0) \approx -\frac{gm_5}{gds_3 + gds_5} \tag{2.66}$$

$$A_{OL0}(s = 0) \approx \frac{gm_{13}gm_7}{(gds_1 2 + gds_{13})(gds_7 + gds_9)} \tag{2.67}$$

The above expressions represent the open loop gain of each stage, where $A_{OL2}$ represents the CS stage, $A_{OL1}$ represents the fast differential stage, and $A_{OL0}$ represents the slow operational amplifier. As referenced above, this circuit has two loops so, will be needed to calculate the final expression taking the two loops into account. Therefore, to introduce the fast loop:

$$A_{V21} = \frac{A_{OL2}A_{OL1}}{1 + A_{OL2}A_{OL1}} \tag{2.68}$$

And to introduce the slow loop a similar step was made that allows to obtain the gain expression.

$$A_V = \frac{A_{OL0}A_{V21}}{1 + A_{OL0}A_{V21}} \tag{2.69}$$

$$A_V \approx \frac{(g_1+g_2)gm_1 gm_{13}gm_5 gm_7}{(g_1+g_2)gm_1 gm_{13}gm_5 gm_7+(g_1 g_2+gds_1(g_1+g_2))(gds_{12}+gds_{13})(gds_3+gds_5)(gds_7+gds_9)} \tag{2.70}$$

As expected the expression obtained represents a unitary gain, and with this expression is possible to obtain the follow-up error expression.

$$F_E = \frac{(g_1 g_2 + gds_1(g_1 + g_2))(gds_{12} + gds_{13})(gds_3 + gds_5)(gds_7 + gds_9)}{(g_1 + g_2)gm_1 gm_{13}gm_5 gm_7} \tag{2.71}$$

After with the calculation of the output impedance is possible to verify that this circuit has a low output impedance, as expected.

$$R_O \approx \frac{(g_1 + g_2)(gds_{12} + gds_{13})gds_3 gds_9(gm_7 + gm_8)}{g_1 gm_1 gm_{13}gm_3 gm_7 gm_8} \tag{2.72}$$

Considering all the stages of the circuit, the transistors that will contribute to the overall noise are transistors $M_1 - M_3$, $M_6$, and $M_9 - M_{13}$, the remaining transistors are cascode and as explained previously his noise is negligible. Since this circuit has two resistors they will also contribute to the noise, and, by inspection is possible to get the output swing expression.

$$V_{Nin}^2 \approx 4K_B T \left( \frac{(g_1 + g_2)(gds_{12} + gds_{13})^2 gds_3 gds_9(gds_7 + gds_9)(gm_7 + gm_8)}{g_1 gm_1 gm_{13}gm_3 gm_7 gm_8} \right)^2$$
$$\left( \gamma(gm_1 + gm_2 + gm_3 + gm_6 + gm_9 + gm_{10} + gm_{11} + gm_{12} + gm_{13}) + \frac{1}{R_1} + \frac{1}{R_2} \right) \tag{2.73}$$

$$\Delta Vo_{pp} = V_{dd} - V_{dsat} - V_{R_1} - V_{R_2} \tag{2.74}$$

By observation of the exact expression of the gain is possible to conclude that this circuit has four poles and four zeros, constituting a stable system. In Figure 2.11 can be observed the root locus of an architecture with the same number of poles and zeros. From the gain expression is possible to get the expressions of the poles and observing them, obtain the dominant pole expression.

$$\omega_p \approx \frac{gm_1 R_1}{cdb_3 + cdb_5 + cgd_3 + cgd_5} \tag{2.75}$$

Analysing this expression is possible to see that the pole frequency is also dependent of $R_1$ which means that there is some margin to change the bandwidth of the circuit if needed.

### 2.10.3 Cascaded FVF (CAFVF)

This architecture is another improved circuit driven from the FVF. As in the Level Shifted FVF (LSFVF), this circuit also introduces another transistor in the feedback loop, that is biased by a voltage $V_b$ on its gate, and by a bias current on its drain (Figure 2.20). This way, the transistor $M_3$ can be compared to a common gate amplifier that will provide extra gain in the feedback loop, and also reduce the output impedance [13].
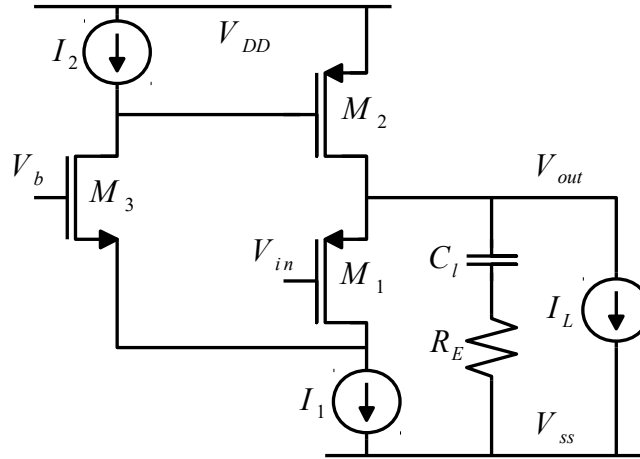


Figure 2.20: Cascaded FVF based LDO.

Based on: [13].

Doing an AC analysis of the circuit is possible to get the expressions of the gain and of the output impedance.

$$R_O \approx \frac{gds_1 gds_3}{gds_1 gm_2 gm_3 + gm_1 gm_2 gm_3} \tag{2.76}$$

$$A_V(s=0) \approx \frac{gm_1}{gds_1 + gm_1} \tag{2.77}$$

Using the gain expression calculated above is possible to obtain the follow-up error expression.

$$F_E = \frac{gds_1}{gm_1} \tag{2.78}$$

By circuit observation is possible to see that the circuit has one transistor that will contribute to the overall noise ($M_2$), and that the transistors $M_1$ and $M_3$ have a negligible noise, because they are cascode transistors. Besides that, the resistor $R_E$ will also contribute to the noise. And analysing the circuit is possible to get the output swing expression.

$$V_{Nin}^2 \approx \frac{4K_B T}{(gm_1 gm_2 gm_3 rds_1 rds_3)^2}\left(\gamma gm_2 + \frac{1}{R_E}\right) \tag{2.79}$$

$$\Delta Vo_{pp} = V_{dd} - 3V_{dsat} \tag{2.80}$$

With the exact expression of the gain is possible to see that this circuit has three poles and three zeros, constituting a stable system. In Figure 2.9 is possible to see an example of a system with the same number of poles and zeros. Calculating the approximated expressions of the poles is possible to get the dominant pole expression.

$$\omega_p \approx \frac{gm_2}{cdb_3 + cgd_2 + cgd_3 + cgs_2} \tag{2.81}$$

### 2.10.4  Buffered FVF (BFVF)

This circuit is based on the LSFVF and on the Cascaded FVF (CAFVF) and its aim is to gather the advantages of both topologies (Figure 2.21). This way the circuit is capable of reduce the loading requirement, increase the loop gain in order to improve the load regulation, improve the stability, and allows to have a larger bandwidth. Therefore, this circuit has a feedback loop with two transistors: one that can be interpreted as a common gate amplifier ($M_4$), and the other which can be interpreted as a source follower. In other words, the feedback loop is a junction of the architectures referred above [13].
In this structure, the drain voltage of $M_1$ is defined by the bias voltage $V_b$ and by the $Vgs$ voltage of $M_4$, which removes the minimum loading constraint present in other topologies. Nevertheless, the bias voltage cannot assume the value we want, because otherwise some transistors may enter the triode region. This way, if the bias voltage is too low, the transistor of $I_1$ enters the triode region. Otherwise if the bias voltage is too high, the transistor $M_4$ enters the triode region[13]. Another function of transistor $M_4$ is to ensure that the transistor $M_1$ will work in the saturation region, no matter which is the bias current of $I_1$ [14].
By analysing the circuit in closed loop is possible to get the expressions of both the output
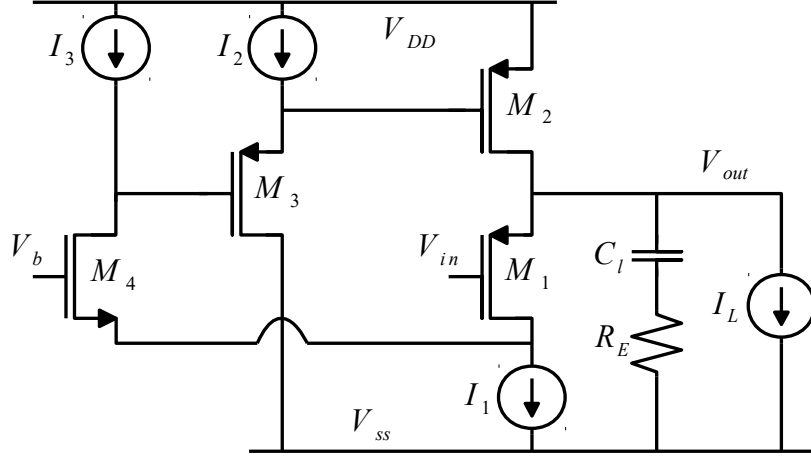
Figure 2.21: Buffered FVF based LDO.

Based on: [13].

impedance and gain.

$$R_O \approx \frac{gds_1 gds_4}{gds_1 gm_2 gm_4 + gm_1 gm_2 gm_4} \tag{2.82}$$

$$A_V(s=0) \approx \frac{gm_1}{gds_1 + gm_1} \tag{2.83}$$

As expected, the output impedance is low, and the gain is unitary. Using this expression is possible to get the follow-up error expression.

$$F_E = \frac{gds_1}{gm_1} \tag{2.84}$$

In relation to the noise, is possible to see that this circuit has two transistors and one resistance that will contribute to the overall noise ($M_2$, $M_3$ and $R_E$). Transistors $M_1$ and $M_4$ have a negligible noise because, as explained previously, they are cascode transistors. Also, by observation of the circuit, is possible to calculate the output swing.

$$V_{Nin}^2 \approx \frac{4K_B T}{(gm_1 gm_2 gm_4 rds_1 rds_4)^2}\left(\gamma(gm_2 + gm_3) + \frac{1}{R_E}\right) \tag{2.85}$$

$$\Delta Vo_{pp} = V_{dd} - 3V_{dsat} \tag{2.86}$$

Using the exact expression of the gain, it can be noticed that this circuit has four poles and four zeros. Since all poles and all zeros remain stable, the circuit will also remain stable. Figure 2.11 constitutes an example of a stable system with the same number of roots. Knowing the approximate expressions of the poles, is possible to get the dominant pole.

$$\omega_p \approx \frac{gm_2}{cgd_2 + cgs_2 + cgs_3 + csb_3} \tag{2.87}$$

## 2.11 Results analysis

On this section a coarse design will be made of the architectures studied in the previous sections. To do so it will be assumed that $\frac{gm_i}{gds_i} \sim 10$ and $gm = \frac{2I_D}{V_{dsat}}$. Therefore, the $V_{dsat}$ voltage established is $50mV$ for all the cases. Then, the necessary supplied current will be calculated, in order to obtain an output impedance of $1\Omega$.

Table 2.1: Coarse design of the different topologies (Part 1/2).

| Characteristics | Circuit/Section | | | | | | |
|---|---|---|---|---|---|---|---|
| | CD | FVF | DFVF | BdFVF | LsFVF | Wbb | SSF |
| Ib (A) | 25 $m$ | 2.5 $m$ | 50 $m$ | 5 $m$ | 5 $m$ | 4.26 $m$ | 6.82 $m$ |
| Ro ($\Omega$) | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 2.2: Coarse design of the different topologies (Part 2/2).

| Characteristics | Circuit/Section | | | | | |
|---|---|---|---|---|---|---|
| | (2.8) | (2.9) | SsLDO | CfLDO | CAFVF | BFVF |
| Ib (A) | - | 2.5 $m$ | 25 $\mu$ | 400 $\mu$ | 250 $\mu$ | 250 $\mu$ |
| Ro ($\Omega$) | 1 | 1 | 1 | 1 | 1 | 1 |

To obtain the results displayed on Table 2.1 and Table 2.2 it was necessary to make several assumptions in each architecture:

- **Common Drain Amplifier:** in this case, it was considered that the current flowing through transistor $M_1$ is only dependent of the current source. In other words, was considered an ideal situation where the output doesn't affect the transistor, $I_{out} = 0A$;

- **FVF Differential Structure:** in this case, a greater approximation was made compared to the one considered in the equation (2.14), $R_O \approx \frac{1}{gm_3}$. Then, it was assumed that the drain current of transistor $M_3$ was half the bias current;

- **Wide bandwidth buffer:** in this case, was considered that the gate current of $M_4$ is zero and that the current flowing in transistors $M_2 - M_4$ is the double of the current flowing in the remaining transistors;

- **Super Source Follower:** in this circuit was considered that the gate current of $M_2$ is zero and that $I_{D1} = 3 * I_{D2}$;

- **Buffer with high linearity and adjustable output impedance:** the crass design made in the previous architectures is not applicable in this situation, because after normalizing the $gm$ of transistors $M_2$ and $M_4$ the output impedance is no longer dependent of $gm$, $R_O \approx \frac{R_1}{2}$;

- **Two stage QFG buffer:** in this circuit was considered that the current flowing in transistors $M_1$ and $M_2$ is equal, and that the current flowing in the amplifier is also the same;

- **Shunt-series LDO:** in this case, was considered that the bias current of the circuit is equal in the two transistors and in the two transconductance amplifiers;

- **Capacitor free LDO:** in this situation was considered that the bias voltages $V_{b1}$ and $V_{b2}$ are equal, the current that flows in $M_{12}$ and $M_{13}$ is equal to $2 \times I_b$, the current that flows in $M_1$ is $0.5 \times I_b$ and that the current in the remaining transistors is equal to $I_b$. It was also considered that the resistors $R_1$ and $R_2$ are sized with $1\Omega$;

- **Cascaded FVF:** in this case, was assumed that the gate current of transistor $M_2$ is zero, the current flowing in $M_1$ and $M_2$ is equal and the drain current of transistor $M_3$ is twice the current observed in the transistors $M_1$ and $M_2$;

- **Buffered FVF:** in this architecture was considered that the gate current of transistors $M_2$ and $M_3$ is zero, the current flowing in $M_1$ is equal in $M_2$ and that transistor $M_4$ presents two times the current when compared to $M_1$ and $M_2$.

The next Tables summarize all the theoretical analysis made in the previous sections, in order to be easier to compare the differences between them. This way joining the results presented in Tables (2.1 to 2.6) will be possible to choose the best architectures to study with more detail in the next Chapter.

Table 2.3: Comparison of the different topologies (Part 1/4).

| Characteristics | Circuit/Section | | | |
|---|---|---|---|---|
| | CD | FVF | DFVF | BdFVF |
| Gain | $\dfrac{gm_1}{gds_1 + gm_1}$ | $\dfrac{gm_1 gm_2}{gm_2 gds_1 + gm_1 gm_2}$ | $\dfrac{gm_1 gm_2}{gm_2 gds_1 + gm_1 gm_2}$ | $\dfrac{gm_1 gm_2}{gds_1(gds_2 + gds_3) + gm_1 gm_2}$ |
| Output impedance | $\dfrac{1}{gm_1}$ | $\dfrac{1}{gm_1 gm_2 rds_1}$ | $\dfrac{1}{gm_3}$ | $\dfrac{gds_2 + gds_3}{gds_1(gds_2 + gds_3) + gm_2 gm_1}$ |
| $\Delta Vo_{pp}$ | $V_{dd} - 2V_{dsat}$ | $V_{dd} - 3V_{dsat}$ | $V_{dd} - 2V_{dsat} - V_{C_l}$ | $V_{dd} - 3V_{dsat}$ |
| $V_{Nin}^2$ | $\dfrac{\gamma 4K_B T}{gm_1}$ | $\dfrac{\gamma 4K_B T gm_2}{(gm_1 gm_2 rds_1)^2}$ | $\dfrac{\gamma 4K_B T gm_2}{(gm_3)^2}$ | $\dfrac{4K_B T(gm_1 + gm_3)}{(gm_1 gm_2(rds_2 // rds_3))^2}$ |
| Bandwidth | $\dfrac{gm_1 + gds_1}{C_l + csb_1 + cgs_1}$ | $\dfrac{gm_2}{cgd_1 + cdb_1 + cgs_2 + cgd_2}$ | $\dfrac{gm_2}{cdb_1 + cgd_1 + cgd_2 + cgs_2}$ | $\dfrac{gm_1}{cgd_1 + cgs_1 + cgd_2 + cdb_2 + cgd_3}$ |
| Follow-up error | $\dfrac{gds_1}{gm_1}$ | $\dfrac{gds_1}{gm_1} + \dfrac{gds_1 gds_2}{gm_1 gm_2}$ | $\dfrac{gds_1}{gm_1} + \dfrac{gds_1 gds_2}{gm_1 gm_2}$ | $\dfrac{gds_1(gds_2 + gds_3)}{gm_2(gds_3 + gm_1)}$ |

Table 2.4: Comparison of the different topologies (Part 2/4).

| | Circuit/Section | | |
|---|---|---|---|
| Characteristics | LSFVF | Wbb | SSF |
| Gain | $\dfrac{gm_1 gm_2}{gds_1(gds_2 + gds_3) + gm_1 gm_2}$ | $\dfrac{gm_1(gm_2 gm_4 + gds_5(gm_3 + gm_4))}{(gds_1 + gm_1)gm_2 gm_4 + gds_5 gm_1(gm_3 + gm_4)}$ | $\dfrac{gm_1 gm_2}{gm_1 gm_2 + gds_1(gds_2 + g_L + gm_2)}$ |
| Output impedance | $\dfrac{gds_2 + gds_3}{gds_1(gds_2 + gds_3) + gm_2 gm_1}$ | $\dfrac{(gds_1 + gds_5)(gm_3 + gm_4)}{(gds_1 + gm_1)gm_2 gm_4 + gds_5 gm_1(gm_3 + gm_4)}$ | $\dfrac{gds_1}{gm_1 gm_2 + gds_1(gds_2 + g_L + gm_2)}$ |
| $\Delta Vo_{pp}$ | $V_{dd} - 3V_{dsat}$ | $V_{dd} - 3V_{dsat}$ | $V_{dd} - 3V_{dsat}$ |
| $V_{Nin}^2$ | $\dfrac{4K_B T(gm_1 + gm_3 + gm_4)}{(gm_1 gm_2(rds_2 // rds_3))^2}$ | $\dfrac{4K_B T((gds_1 + gds_5)(gm_3 + gm_4))^2 X_1}{(gm1(gm2 gm4 + gds5(gm3 + gm4)))^2}$ | $\dfrac{4K_B T X_2}{(gm_1 gm_2 rds_1)^2}$ |
| Bandwidth | $\dfrac{gm_1}{C_c + cgd_1 + cgs_1 + cgs_4 + csb_4}$ | $\dfrac{(1 + gm_1)gm_2 gm_4 + gds_5 gm_1(gm_3 + gm_4)}{(cdb_3 + cgs_3 + cgs_4 + csb_4)gm_1 gm_4}$ | $\dfrac{gm_2}{cdb_1 + cgd_1 + cgd_2 + cgs_2}$ |
| Follow-up error | $\dfrac{gds_1(gds_2 + gds_3)}{gm_2(gds_3 + gm_1)}$ | $\dfrac{gm_2 gm_4 gds_1}{gm_1(gm_2 gm_4 + gds_5(gm_3 + gm_4))}$ | $\dfrac{gds_1(gds_2 + g_L + gm_2)}{gm_2 gm_1}$ |

$$X_1 = \gamma(gm_2 + gm_3 + gm_5 + gm_6) + \frac{1}{R_c}$$

$$X_2 = \gamma(gm_1 + gm_2) + \frac{1}{R_L}$$

Table 2.5: Comparison of the different topologies (Part 3/4).

| Characteristics | Circuit/Section | | |
|---|---|---|---|
| | (2.8) | (2.9) | SsLDO |
| Gain | $\dfrac{g_1 gm_2 + (g_1 + gds_2 + g_{in})gm_4}{(g_1 + gds_4 + g_L)gm_2 + (g_1 + gds_3)gm_4}$ | $\dfrac{gm_1 gm_4}{gm_1 gm_4 + (gds_1 + gds_2)gout_4}$ | $\dfrac{gm_1 gm_4}{gm_1 gm_4 - gds_1 gout_4}$ |
| Output impedance | $\dfrac{gm_2}{(g_1 + gds_4 + g_L)gm_2 + (g_1 + gds_3)gm_4}$ | $\dfrac{gout_4}{gm_1 gm_4 + (gds_1 + gds_2)gout_4}$ | $\dfrac{(g_1 + gds_1)gout_3 gout_4}{gm_1 gm_2 gm_3 gm_4}$ |
| $\Delta Vo_{pp}$ | $V_{dd} - 2V_{dsat}$ | $V_{dd} - 2V_{dsat}$ | $V_{dd} - 2V_{dsat} - V_s$ |
| $V_{Nin}^2$ | $\dfrac{4K_B T (gm_2)^2 X_3}{(g_1 gm_2 + (g_1 + gds_2 + g_{in})gm_4)^2}$ | $\dfrac{4K_B T}{(gm_1 gm_4 Rout_4)^2}\left(\gamma(gm_1 + gm_2) + \dfrac{1}{R_c} + \dfrac{1}{R_{large}}\right)$ | $\dfrac{4K_B T}{(X_4)^2}\left(\gamma gm_2 + \dfrac{1}{R_1}\right)$ |
| Bandwidth | $\dfrac{g_1(gm_2 + gm_4)}{(C_1 + cdb_4 + C_L)gm_2}$ | $\dfrac{gm_1}{C_{bat} + C_c + cgd_1 + cgs_1 + C_{p4}}$ | $\dfrac{gm_2}{cgd_2 + cgs_2 + C_{p3}}$ |
| Follow-up error | $\dfrac{(gds_4 + g_L)gm_2 + gds_3 gm_4}{g_1(gm_2 + gm_4)}$ | $\dfrac{(gds_1 + gds_2)gout_4}{gm_1 gm_4}$ | $\dfrac{gds_1 gout_4}{gm_1 gm_4}$ |

$$X_3 = \gamma(gm_1 + gm_2 + gm_4) + \frac{1}{R_L} + \frac{1}{R_1} + \frac{1}{R_{in}}$$

$$X_4 = gm_1 gm_2 gm_3 gm_4 Rout_3 Rout_4 (rds_1 // R_1)$$

Table 2.6: Comparison of the different topologies (Part 4/4).

| Characteristics | Circuit/Section | | |
| --- | --- | --- | --- |
| | CfLDO | CAFVF | BFVF |
| Gain | $\dfrac{(g_1+g_2)gm_1gm_{13}gm_5gm_7}{(g_1+g_2)gm_1gm_{13}gm_5gm_7+X_5}$ | $\dfrac{gm_1}{gds_1+gm_1}$ | $\dfrac{gm_1}{gds_1+gm_1}$ |
| Output impedance | $\dfrac{(g_1+g_2)(gds_{12}+gds_{13})gds_3gds_9(gm_7+gm_8)}{g_1gm_1gm_{13}gm_3gm_7gm_8}$ | $\dfrac{gds_1gds_3}{gds_1gm_2gm_3+gm_1gm_2gm_3}$ | $\dfrac{gds_1gds_4}{gds_1gm_2gm_4+gm_1gm_2gm_4}$ |
| $\Delta Vo_{pp}$ | $V_{dd}-V_{dsat}-V_{R_1}-V_{R_2}$ | $V_{dd}-3V_{dsat}$ | $V_{dd}-3V_{dsat}$ |
| $V_{Nin}^2$ | $4K_BTX_6$ | $\dfrac{4K_BT}{(gm_1gm_2gm_3rds_1rds_3)^2}\left(\gamma gm_2+\dfrac{1}{R_E}\right)$ | $\dfrac{4K_BT}{(gm_1gm_2gm_4rds_1rds_4)^2}X_7$ |
| Bandwidth | $\dfrac{gm_1R_1}{cdb_3+cdb_5+cgd_3+cgd_5}$ | $\dfrac{gm_2}{cdb_3+cgd_2+cgd_3+cgs_2}$ | $\dfrac{gm_2}{cgd_2+cgs_2+cgs_3+csb_3}$ |
| Follow-up error | $\dfrac{X_5}{(g_1+g_2)gm_1gm_{13}gm_5gm_7}$ | $\dfrac{gds_1}{gm_1}$ | $\dfrac{gds_1}{gm_1}$ |

$$X_5 = (g_1g_2+gds_1(g_1+g_2))(gds_{12}+gds_{13})(gds_3+gds_5)(gds_7+gds_9)$$

$$X_6 = \left(\frac{(g_1+g_2)(gds_{12}+gds_{13})^2gds_3gds_9(gds_7+gds_9)(gm_7+gm_8)}{g_1gm_1gm_{13}gm_3gm_7gm_8}\right)^2\left(\gamma(gm_1+gm_2+gm_3+gm_6+gm_9+gm_{10}+gm_{11}+gm_{12}+gm_{13})+\frac{1}{R_1}+\frac{1}{R_2}\right)$$

$$X_7 = \left(\gamma(gm_2+gm_3)+\frac{1}{R_E}\right)$$

# Buffer Implementation

Considering the work done in the previous Chapter, now the best topologies from a theoretical point of view will be selected and a more careful design will be done.

By observation of the results displayed in the Section 2.11 there are three topologies that clearly show better results than the other ones, and they are the CfLDO, the SsLDO, and the Buffered FVF (BFVF).

The CfLDO is the best architecture from the theoretical point of view because it presents the best output impedance, a very low noise, adjustable bandwidth and also a low follow-up error. Relatively to the coarse design, this architecture appears in third place which is not a surprise, since, in comparison to the other architectures, this is the one that has more transistors working. Therefore, resulting in a large power consumption.

The SsLDO also stands out in the theoretical analysis, since it presents the second best results concerning the output impedance, the noise and the follow-up error. In the coarse design it presents the lowest power consumption.

The other choice was the BFVF, because it presents the second best coarse design, and it also has a good behaviour from the theoretical point of view.

In some cases, the architecture from the Section 2.8 can also be interesting to be studied, since its output impedance and bandwidth are dependent from the resistance $R_1$.

In the next sections, the implementation of these architectures will be made, in order to obtain the desired specifications using the $gm/I_d$ technique.

## 3.1   GM/ID Technique

As referred before, to do this implementation a technique known as $gm/I_d$ was used instead of the traditional technique using the equations to do the calculations. So this technique was chosen because it allows to model the behaviour of the transistors in all

its working regions and this way it's easier to design parameters, such as the transconductance ($gm$), the drain current and the intrinsic gain of the transistor [15], [16]. So, the first step to use this methodology, is to fix the currents in order to satisfy the desired parameters, and then the sizes are chosen, in order to satisfy the parameters that have to be improved for the $gm/I_d$ chosen.

Thus to obtain the graphics that model the behaviours of the NMOS and PMOS transistors, the circuits shown in the Figure 3.1 were used, where is established the supply voltage (1 $V$) of the transistors, then a parametric variation of the gate voltage (from 0 $V$ to 1 $V$) is done and finally are tested different dimensions for the transistors, in order to observe the influence of length and width of the transistor in the different parameters.



(a) NMOS modulation.          (b) PMOS modulation.
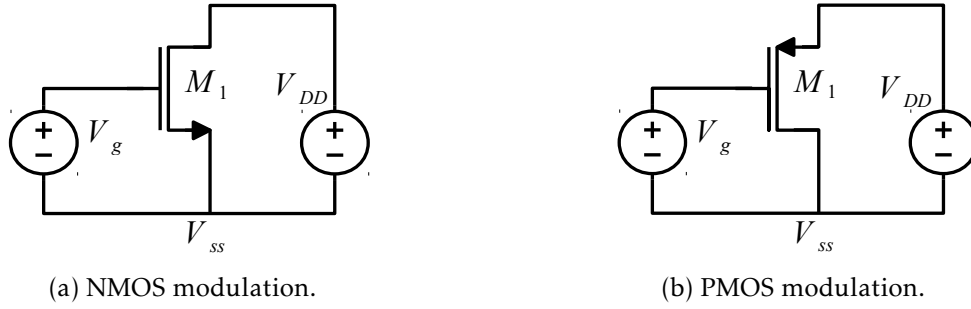
Figure 3.1: Transistors modulation.

This way it was possible to obtain the graphs displayed next (Figures 3.2 to 3.7), where is presented the modulation of a NMOS and a PMOS transistors for different values of length and width. Thus it's possible to see which are the best dimensions for length and width in a given region of $gm/I_d$, taking into account the parameter to optimize (maximize or minimize). After choosing the region of $gm/I_d$ it is necessary to choose the dimensions that better satisfy the desired specifications.



(a) NMOS modulation.          (b) PMOS modulation.
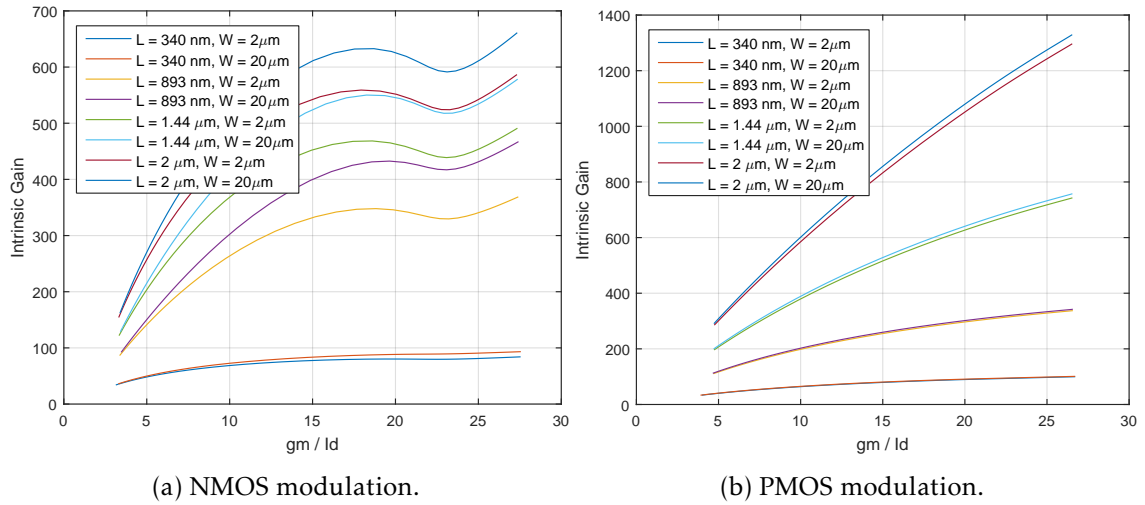
Figure 3.2: Intrinsic gain modulation.

(a) NMOS modulation.

(b) PMOS modulation.

Figure 3.3: GM modulation.
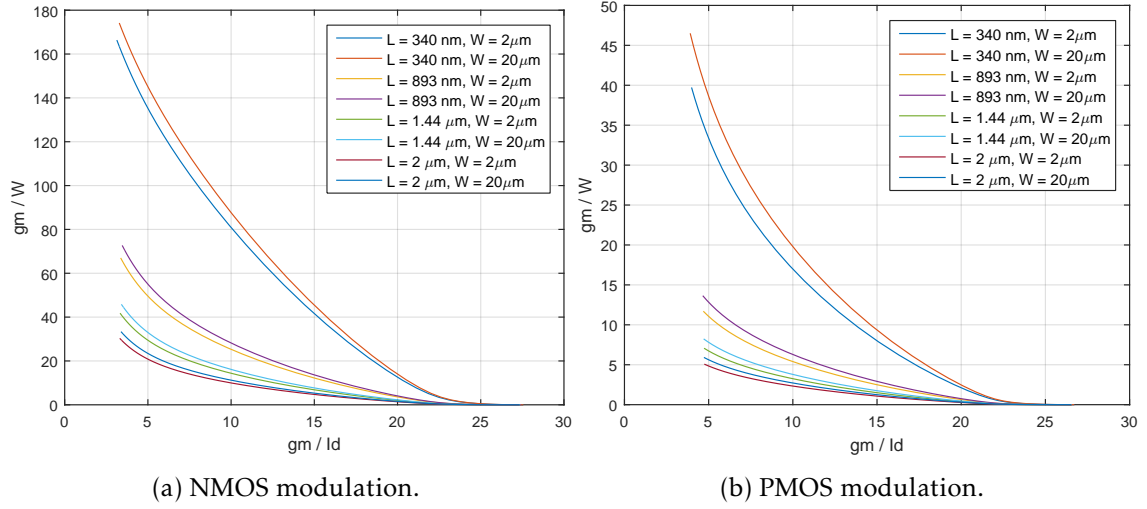


(a) NMOS modulation.
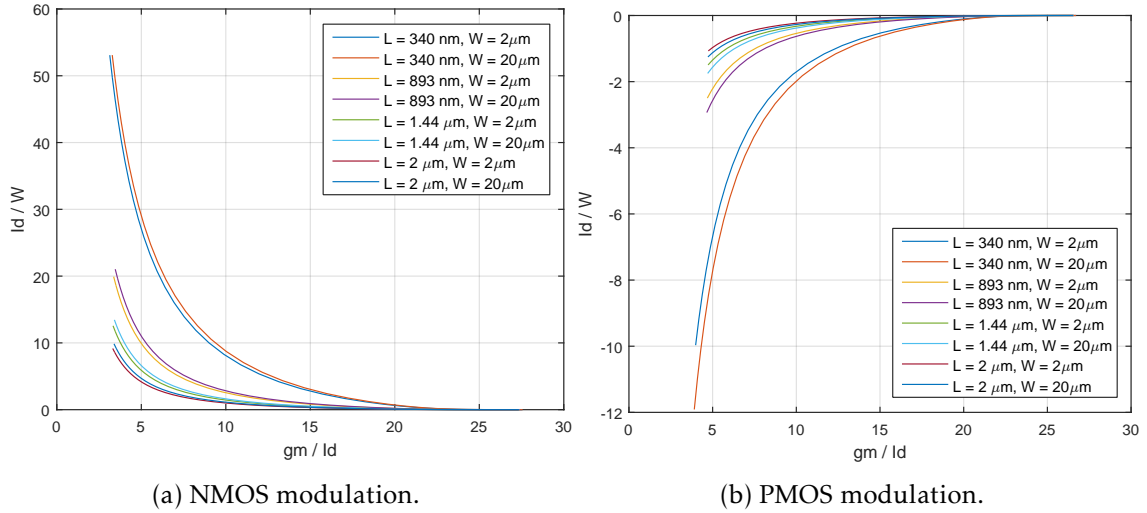
(b) PMOS modulation.

Figure 3.4: Drain current modulation.



(a) NMOS modulation.
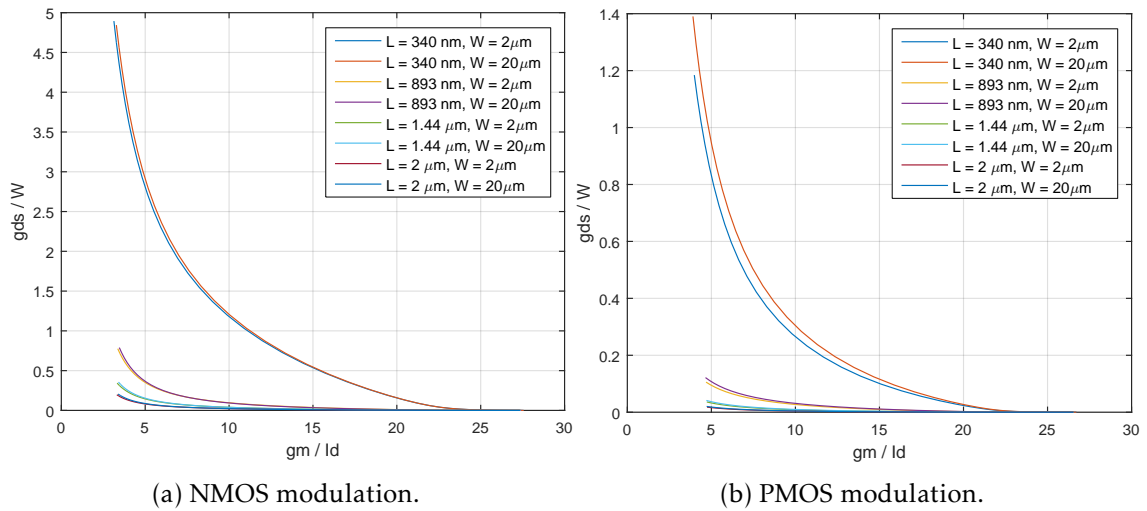
(b) PMOS modulation.

Figure 3.5: GDS modulation.

(a) NMOS modulation.  (b) PMOS modulation.
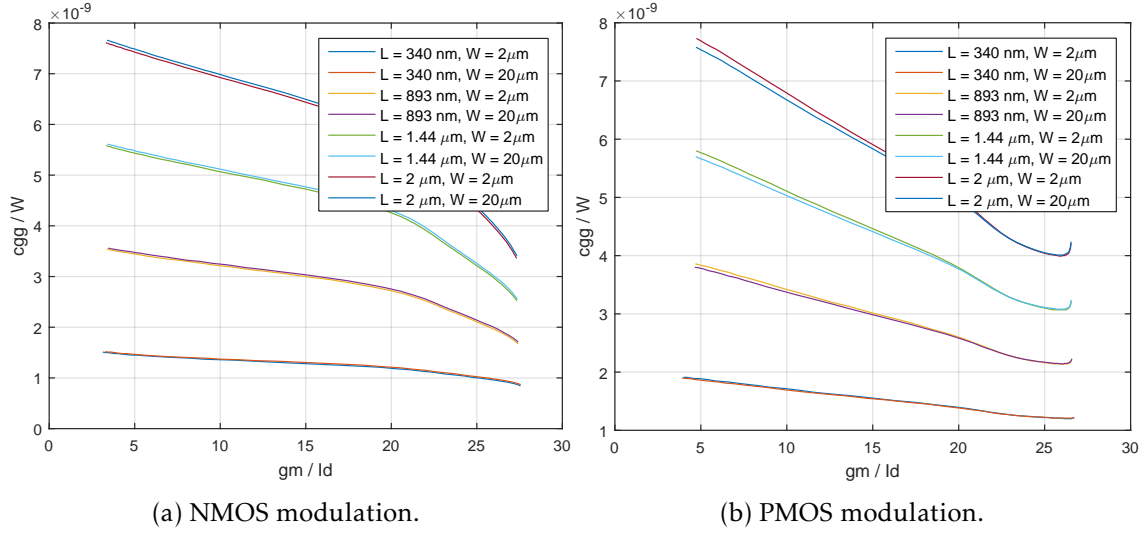
Figure 3.6: CGG modulation.



(a) NMOS modulation.  (b) PMOS modulation.
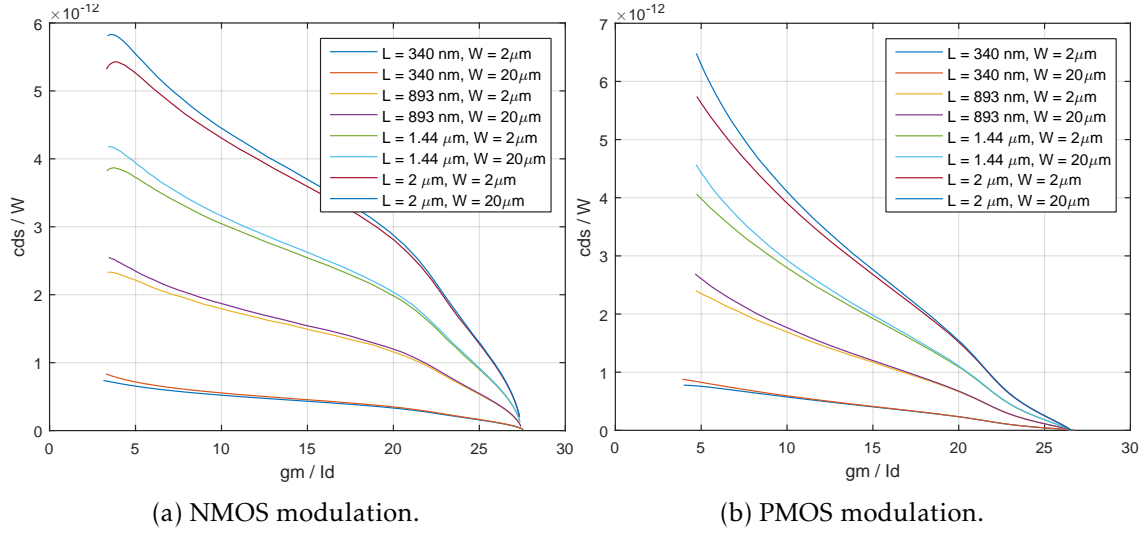
Figure 3.7: CDS modulation.

## 3.2 Sizing Methodology

In addition to using the *gm/Id* technique, other procedures were also used. Figure 3.8 illustrates all the procedures necessary to achieve the desired specifications for the circuit in question. Next, are described with more detail all the Steps referred in Figure 3.8:

- **Step 1:** In the first step are obtained the equations to model the circuit;

- **Step 2:** According to the equations obtained is chosen a *gm/Id* region to size the transistors;

- **Step 3:** Depending on the region chosen the transistors are sized in order to fulfil all the desired specifications of the circuit;
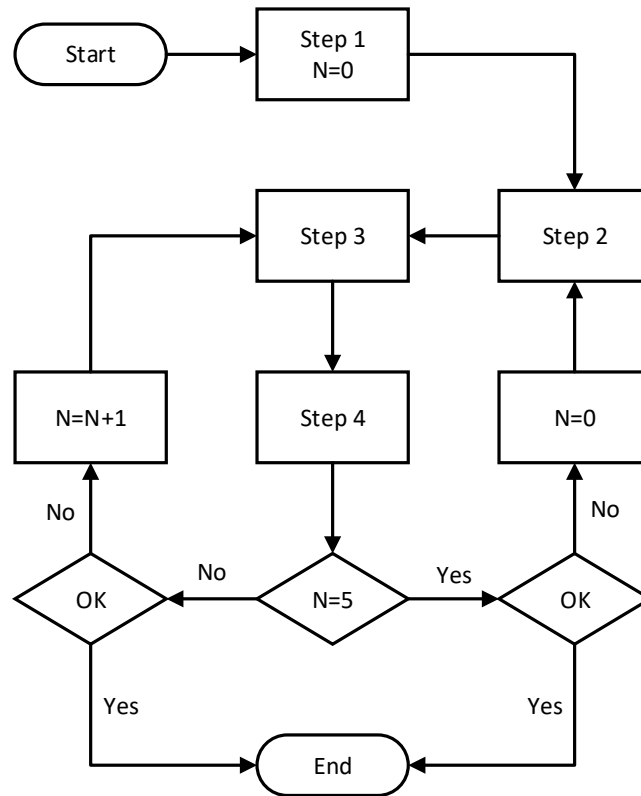
Figure 3.8: Flow chart demonstrating the methodology used to size the transistors of architectures used to implement the buffer.

- **Step 4:** As a way to confirm if the goals are met all the necessary simulations are done;

- **OK:** If "OK" is true the circuit is working as pretended, otherwise it isn't;

- **N:** Is a variable used to count the number of iterations in the process.

Also, in the flow chart is a decision "N=5". It represents the number of iterations to resize the transistors before adjust the $gm/Id$ region, but the number of iterations can be adjusted as desired.

Beyond the steps illustrated in the flow chart, there were made some more considerations. These considerations are relative to transistors working region. Thus all the transistors were sized to work in the saturation region and with strong inversion. Nevertheless, in some cases it was necessary to put some transistors working with moderate inversion to achieve the desired results.

## 3.3   Error amplifiers

The purpose of this section is to study with some detail the architectures of the different amplifiers used. Here is done a brief theoretical analysis of them, in order to obtain some

informations of the circuits, such as the gain and the Gain Bandwidth Product (GBW), and some simulations from these circuits are also shown in this section.

### 3.3.1 Two stage amplifier with Miller compensation

This is a two stage amplifier capable of obtaining an high open loop gain. However, this circuit presents some stability problems, therefore, it was necessary to add a compensation between the two stages [17]. A capacitor and a resistor were used to create such compensation (Figure 3.9), in order to stabilize the circuit and, at the same time, have control to adjust its phase margin and its GBW.
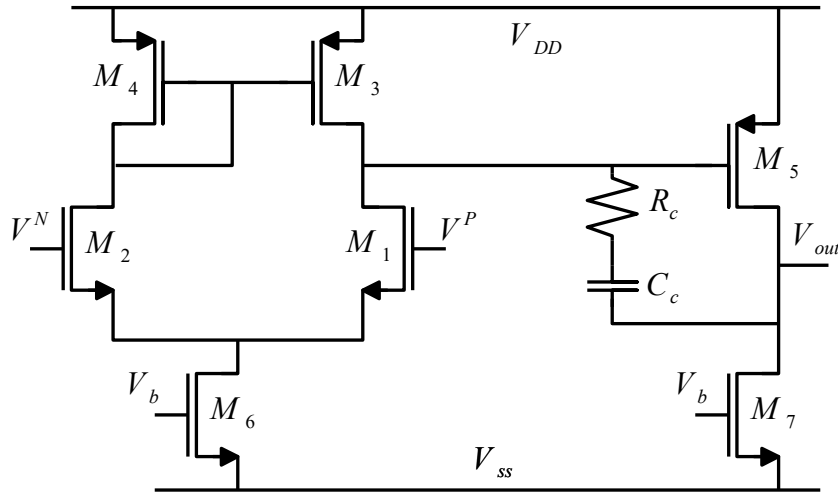


Figure 3.9: Miller compensated amplifier.

Through circuit analysis, is possible to obtain the main equations to design the circuit, the gain, the dominant pole and the GBW expressions.

$$A_V(s = 0) \approx gm_1 gm_5 (rds_1 // rds_3)(rds_5 // rds_7) \tag{3.1}$$

$$\omega_p \approx \frac{1}{gm_5 (rds_1 // rds_3)(rds_5 // rds_7) C_c} \tag{3.2}$$

$$GBW \approx \frac{gm_1}{C_c} \tag{3.3}$$

Considering these equations the circuit was designed to obtain a phase margin greater than 60º and a GBW between 200 to 300 MHz, to make sure that the circuit is stable and fast enough. Alongside this, it was also desirable to obtain the highest possible gain, to increase the performance of the circuit.

According to this specifications, the sizes attributed to the transistors of this amplifier are presented in Table 3.1. Besides that $R_c = 10 \ K\Omega$, $C_c = 200 \ fF$ and the drain current of transistors $M_6$ and $M_7$ is respectively $60.84 \ \mu A$ and $63.60 \ \mu A$.

It was possible to obtain a gain of $73 \ dB$, and fulfil the desired specifications, obtaining a

Table 3.1: Transistors size of the Miller compensated amplifier.

| Device | Width ($\mu m$) | Length ($\mu m$) | Fingers | Multiplier |
|--------|-----------------|------------------|---------|------------|
| $M_1, M_2$ | 20 | 2.04 | 10 | 1 |
| $M_3, M_4$ | 20 | 1.2 | 10 | 1 |
| $M_5$ | 20 | 0.6 | 10 | 1 |
| $M_6, M_7$ | 9 | 2.04 | 3 | 1 |



(a) Magnitude.



(b) Phase.
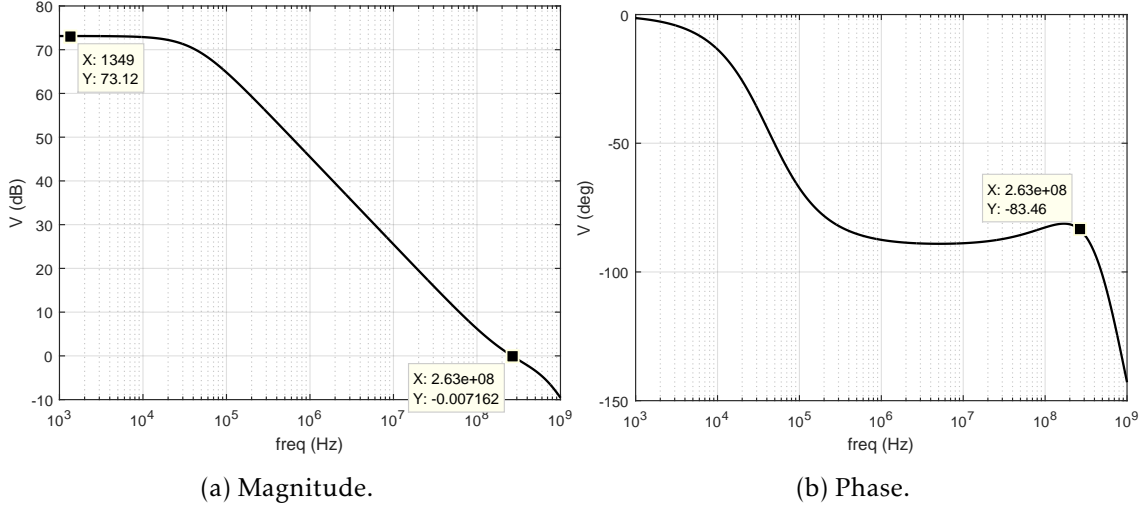
Figure 3.10: Frequency response of the Miller compensated amplifier.

GBW$\approx 263$ $MHz$ and a phase margin equal to 96.5° (Figure 3.10).

In order to achieve these results, it was needed to adjust $R_c$ and $C_c$ to values that allowed to achieve the desired phase margin and the desired GBW. It was also needed to adjust the sizes of transistors in order to obtain a higher gain, and in case of $gm_1$, it was also taken into account that this transistor has direct influence in the GBW. Thus, transistor $M_1$ was set to work with a $gm/I_d \approx 11$. By observation of Figures 3.3a and 3.5a it's clear that the sizes attributed to the transistor $M_1$ produce a small $gm$. Consequently, a smaller compensation capacitance ($C_c$) can be used to adjust GBW. Moreover, the sizes attributed to $M_1$ produce high $gds$, which allows to increase the $rds$ and the gain of the circuit. The same situation occurs in the transistor $M_3$, where is also used a high length to increase the $rds$. Therefore, the transistor $M_5$ (set to work with a $gm/I_d \approx 8$) has a lower length and a higher width to increase the $gm$. This way, the sizes attributed contribute to increase the gain of the amplifier.

### 3.3.2 Current Mirror OTA

The current mirror Operational Transconductance Amplifier (OTA) (Figure 3.11) is a single stage amplifier and consequently its gain is lower than the gain of the amplifier presented in the previous section. However, this circuit presents some advantages due to its architecture, since it allows to reach stability without the use of any compensation,

and also the output swing of this circuit is only dependent of the transistors $M_5$ and $M_7$ [18].

$$A_V(s=0) \approx Bgm_1 gm_5(rds_5 // rds_7) \tag{3.4}$$

$$\omega_p \approx \frac{gds_5 + gds_7}{cgd_5 + cdb_5 + cgd_7 + cdb_7} \tag{3.5}$$

$$GBW \approx \frac{Bgm_1}{cgd_5 + cdb_5 + cgd_7 + cdb_7} \tag{3.6}$$

Analysing the circuit is possible to obtain the expressions needed to design the circuit, such as the gain, the dominant pole and the GBW expressions.
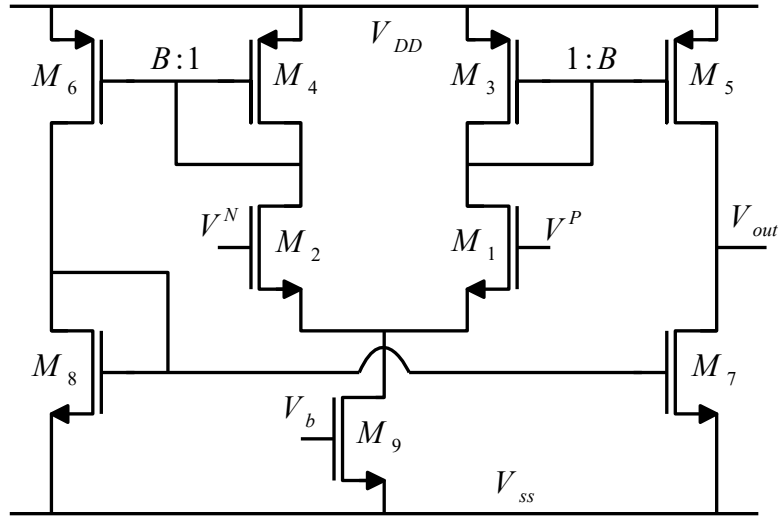

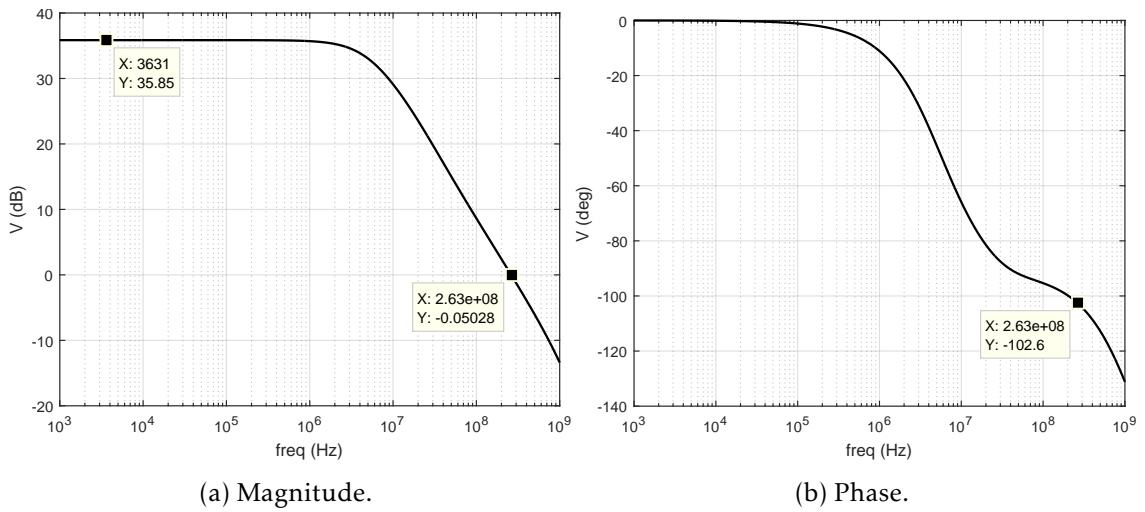
Figure 3.11: Current mirror OTA.



(a) Magnitude.

(b) Phase.

Figure 3.12: Frequency response of the Current Mirror OTA.

42

Table 3.2: Transistors size of the Current Mirror OTA.

| Device | Width ($\mu m$) | Length ($\mu m$) | Fingers | Multiplier |
|---|---|---|---|---|
| $M_1, M_2$ | 4 | 0.68 | 2 | 1 |
| $M_3, M_4, M_5, M_6$ | 4 | 0.30 | 2 | 1 |
| $M_7, M_8$ | 80 | 4.42 | 20 | 1 |
| $M_9$ | 6 | 2.04 | 4 | 1 |

Taking into account the equations of this circuit it was designed to obtain a phase margin greater than 60º and a GBW between 200 to 300 MHz. This way the transistors were sized according to Table 3.2, besides that the drain current of transistor $M_9$ is 38.60 $\mu A$.

Thus it was possible to obtain a gain of almost 36 $dB$, a phase margin of 77.4º and a GBW $\approx 263\ MHz$ (Figure 3.12). In order to achieve the aforementioned was chosen a $\beta = 1$ to have a more stable circuit. After were changed the sizes of transistors in order to achieve the desired specifications, so transistor $M_1$ was set to work with a $gm/I_d \approx 11$. In this situation was impossible to set the sizes that produce the best value for the gain, since this circuit doesn't have compensation, it's necessary to have extra care to stabilize the circuit. So transistors $M_1 - M_5$ were set to have a high $gm$ and transistors $M_7 - M_8$ were set to have higher parasitic capacitances to adjust the GBW and the phase margin.

## 3.4 DAC

The DAC represented in Figure 1.3 was implemented using the architecture present in Figure 3.13, where $R_1 = R_2 = 25K\Omega$. Here are represented three different inverters, all of them have the same architecture. However, they are not equally sized, whence the distinction between them.
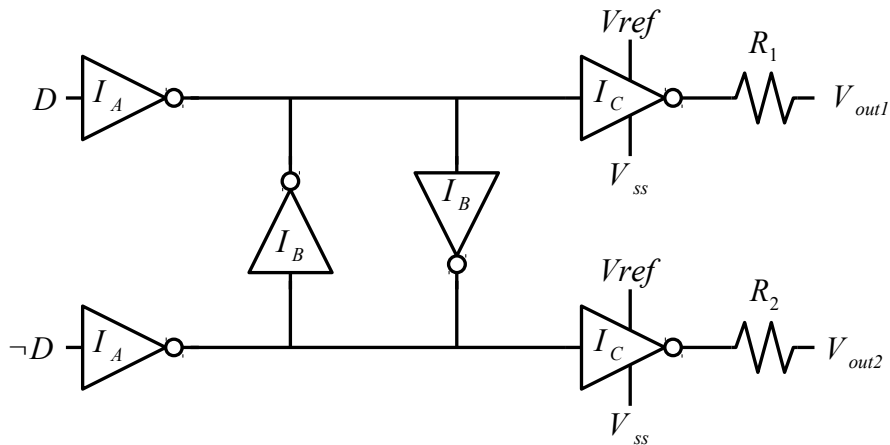


Figure 3.13: DAC architecture.

Figure 3.14 presents the architecture used to implement the inverters and in Table 3.3 is possible to see the dimensions of the transistors used in each inverter.

Besides this, the digital signals applied on the input of the DAC have a period of 10 $ns$,
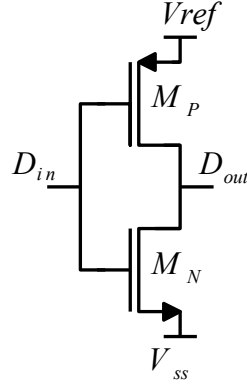
43

Figure 3.14: Inverter architecture.

Table 3.3: Transistors size of the DAC inverters.

| Device | | Width ($\mu m$) | Length ($nm$) | Fingers | Multiplier |
|---|---|---|---|---|---|
| Inv A | $M_P$ | 3 | 120 | 2 | 1 |
| | $M_N$ | 1 | 120 | 2 | 1 |
| Inv B | $M_P$ | 1.5 | 120 | 1 | 1 |
| | $M_N$ | 0.5 | 120 | 1 | 1 |
| Inv C | $M_P$ | 6 | 120 | 4 | 1 |
| | $M_N$ | 2 | 120 | 4 | 1 |

but their pulse width is different in order to always have an active signal. So the pulse width of D is 4.98 $ns$, and the pulse width of ¬D is 5 $ns$.

## 3.5 Delta-Sigma ADC

Considering that the buffer provides a reference voltage to a Delta-Sigma ADC, it is necessary to make some considerations. So the overall architecture used is represented in Figure 1.3, and the function of the DAC represented there is to simulate the behaviour of switches $D_{out}$ and ¬$D_{out}$ present in the first integrator of the Delta-Sigma (Figure 3.15).
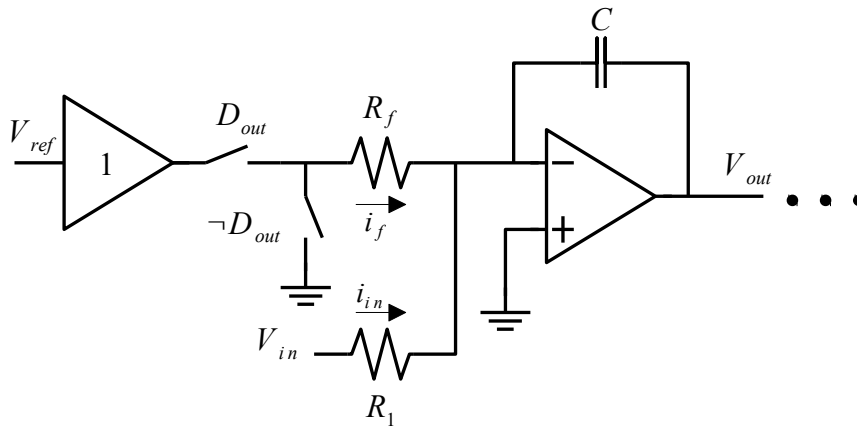


Figure 3.15: First integrator of the Delta-Sigma ADC.

The $D_{out}$ switch is only connected in some periods of time, which will generate some noise at the output transient voltage of the buffer. In order to calculate the aforementioned noise, it was applied the following steps (assuming $R_f \approx R_1$): firstly, is integrated the current $i_f(t)$ when $D_{out}$ is closed ($T_{clk}$) which allows to obtain the charge at capacitor $C$;

$$\Delta Q_N[n] = \int_0^{T_{clk}} i_f \quad dt \tag{3.7}$$

the second step is obtain the current $i_{in}$ through the charge calculated previously;

$$i_{in} = \frac{\Delta Q_N[n]}{T_{clk}} \tag{3.8}$$

lastly, it's only needed to multiply the current $i_{in}$ by the resistor $R_1$ and the voltage obtained is the output transient voltage noise.

$$\Delta V_{in}[n] = i_{in}R_1 \tag{3.9}$$

## 3.6 Common Drain Amplifier

Although this architecture is not in the best ones studied it will also be analysed and implemented in order to have a reference point. As seen in Chapter 2, this circuit has the worse theoretical characteristics, but it helps to see the evolution between this one to the other architectures.

To implement this architecture, it was considered the circuit present in Figure 3.16 instead of the simplified version present in Chapter 2.



(a) Biasing circuit.

(b) Common Drain Amplifier.

Figure 3.16: Common Drain Amplifier with the biasing circuit.
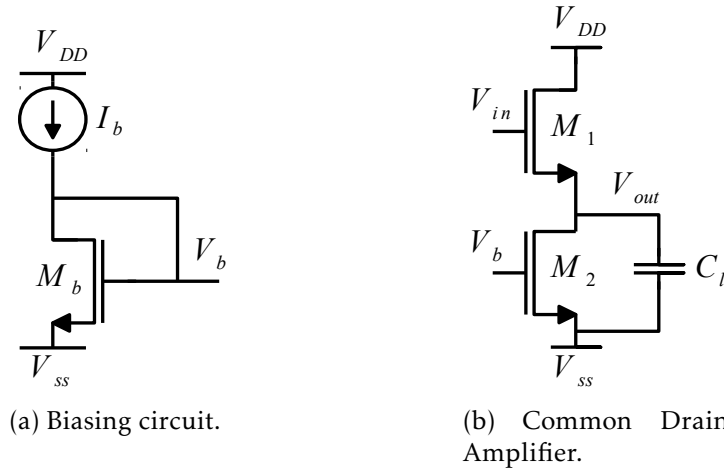
Taking into account the equations of this circuit present in Section 2.1, the size of its transistors was calculated to obtain a stable circuit and, after that, the other characteristics of the circuit were improved. Therefore it's clear that the main objective to increase the performance of the circuit is increase the transconductance ($gm$) of transistor $M_1$. To do

so, it was taken into account the equation $gm = \dfrac{2I_d}{V_{dsat}}$, where is clear that a higher current increases the transconductance. It was also taken into account the $gm/I_d$ technique where is observable that a higher width for the transistor produces a higher gm. Nevertheless, as mentioned before it's necessary to keep the circuit stable, take in consideration the power consumption and the area occupied by the circuit, so the sizes were attributed accordingly.

Thus the circuit was biased with 20 $\mu A$ and the sizes attributed to the transistors are present in Table 3.4. Besides that the load capacitance was sized with 1 $pF$ and the drain current of $M_2$ is 82 $\mu A$. So the sizes of transistors were chosen the following way: in

Table 3.4: Transistors size of the Common Drain amplifier.

| Device | Width ($\mu m$) | Length ($\mu m$) | Fingers | Multiplier |
|--------|-----------------|------------------|---------|------------|
| $M_1$  | 20              | 0.34             | 10      | 1          |
| $M_2$  | 12              | 2.04             | 4       | 1          |
| $M_b$  | 3               | 2.04             | 2       | 1          |

first place it was chosen a higher value for the length of transistors $M_2$ and $M_b$, to obtain a lower $gm$ and a lower $gds$ for those transistors; Then it was set a width of 12 $\mu m$ for transistor $M_2$, to obtain a higher current on that branch; Finally, it was chosen the size of transistor $M_1$, in order to have a bandwidth of at least 100 $MHz$ and to keep satisfying the desired specifications.

By observing Figure 3.3a it's clear that a lower length and a higher width increase the value of $gm_1$, because transistor $M_1$ was set to work with a $gm/I_d \approx 12$.

## 3.7   Shunt-series LDO (SsLDO)

As seen in the Chapter 2, this circuit presents two control loops, and in those loops are present two amplifiers ($A_1$ and $A_2$). Thus to implement them was required to use an amplifier $A_1$ with a higher GBW, and an amplifier $A_2$ with a lower GBW. To implement the amplifier $A_1$ are used error amplifiers. The circuits used to implement it are present in Section 3.3 where its characteristics are explained with more detail. On the other side the amplifier $A_2$ is an amplifier with a lower GBW and lower gain. Therefore, it was used a differential pair to implement it.

Through circuit analysis (Figure 3.17) is possible to obtain the equations to design it, and this way, as shown in Figure 3.18, is possible to obtain a gain of 46 $dB$, a GBW$\approx 6.5\ MHz$ and a phase margin equal to 74.7º. In Table 3.5 are present the sizes of the differential pair transistors, besides that the drain current of $M_5$ is 1 $\mu A$. Two main characteristics are observable: a low biasing current and transistors with high dimensions, due to the need of obtain a small GBW. The transistor $M_1$ was set to work with a $gm/I_d \approx 50$ and, although the graphs of $gm/I_d$ technique don't show the modulation for this region, it's observable that higher values of $gm/I_d$ tend to have lower parasitic capacitances and a
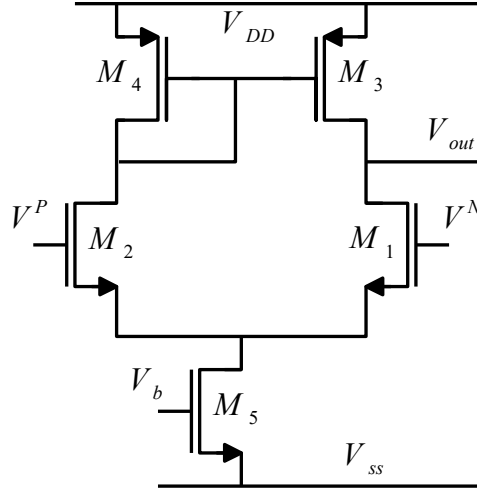
lower transconductance.



Figure 3.17: Differential pair.

$$A_V(s = 0) \approx gm_1(rds_1//rds_3) \tag{3.10}$$

$$\omega_p \approx \frac{1}{(rds_1//rds_3)(cdb_1 + cgd_1 + cdb_3 + cgd_3)} \tag{3.11}$$

$$GBW \approx \frac{gm_1}{cdb_1 + cgd_1 + cdb_3 + cgd_3} \tag{3.12}$$
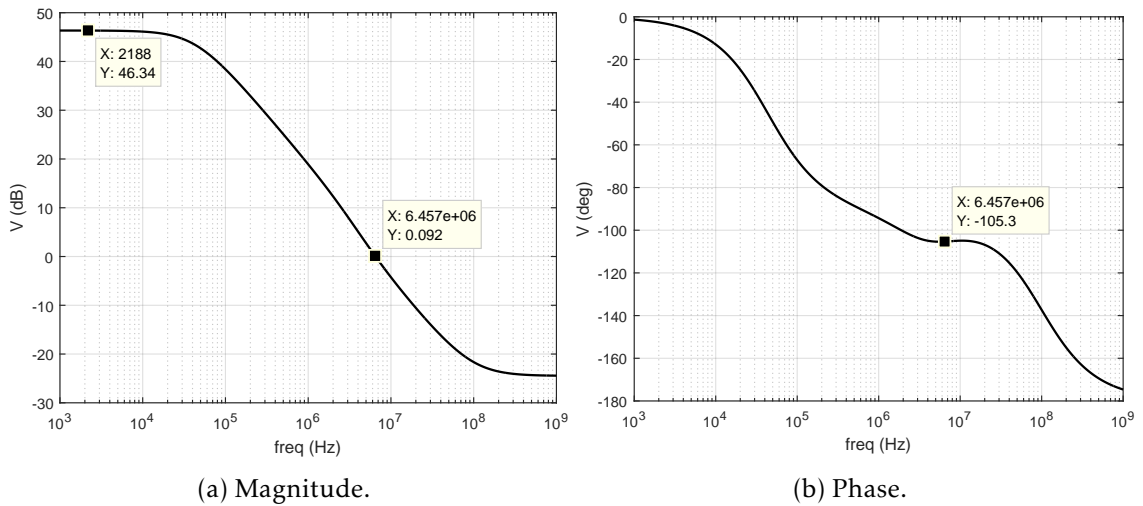


(a) Magnitude.
(b) Phase.

Figure 3.18: Frequency response of the Differential pair.

Since the differential pair doesn't have a load capacitor big enough, it was needed to add the capacitor $C_1$ in the buffer, as shown in Figure 3.19b, in order to do an AC uncoupling. This way, the $Vgs$ voltage of the transistor $M_2$ is held constant and the parasitic capacitances at this node are eliminated, which results in a better positive PSRR and a faster

47

Table 3.5: Transistors size of the Differential pair.

| Device | Width ($\mu m$) | Length ($\mu m$) | Fingers | Multiplier |
|---|---|---|---|---|
| $M_1, M_2$ | 60 | 2.04 | 30 | 2 |
| $M_3, M_4$ | 80 | 0.90 | 40 | 2 |
| $M_5$ | 2 | 2.04 | 10 | 1 |

response to any perturbation at the output of the buffer. To biasing the buffer and the two amplifiers, the circuit in Figure 3.19a was used, where $V_b$ is used in the buffer, $V_{b1}$ is used in the amplifier $A_1$ and $V_{b2}$ is used in the amplifier $A_2$. It was also used a current $I_b = 20\ \mu A$, $C_1 = 500\ fF$, $C_l = 1\ pF$, $R_1 = 20\ K\Omega$, $R_2 = 26\ K\Omega$ and the sizes of both biasing and buffer transistors are present in Table 3.6. This way, the drain current of transistors $M_1$ and $M_3$ is respectively 53.87 $\mu A$ and 41.59 $\mu A$.



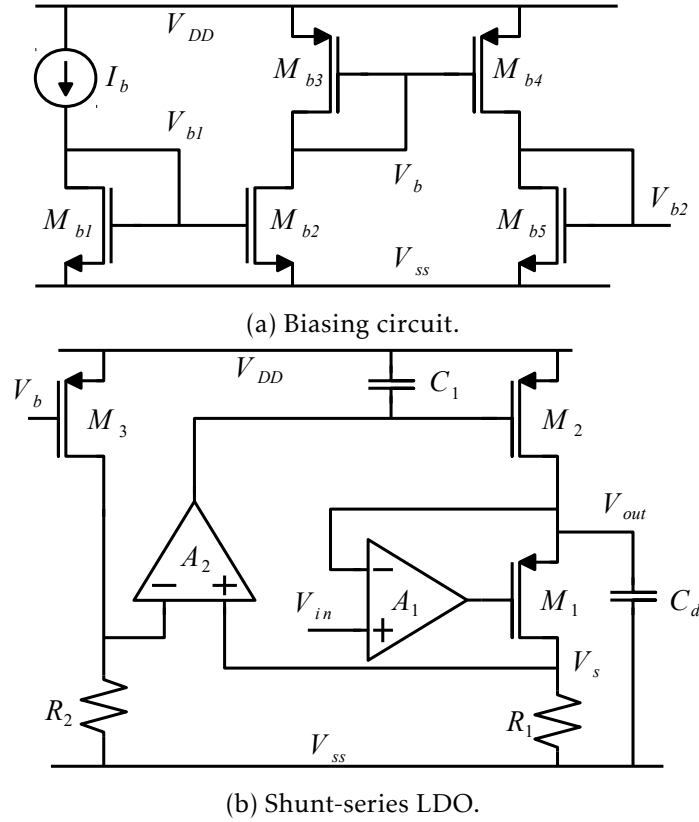(a) Biasing circuit.



(b) Shunt-series LDO.

Figure 3.19: Shunt-series LDO with the biasing circuit.

In order to achieve this results, transistor $M_1$ was set to work with a $gm/I_d \approx 18$. Considering this region, transistor $M_1$ was sized to obtain a high $gm$, which increases the performance of the circuit. On the other side, since the transistor $M_2$ has a high contribute for the noise, it was sized to achieve a lower $gm$. Therefore, it was preferable to improve the noise over the bandwidth of the circuit, because a higher length on this transistor improves the settling time and reduces the noise at the output transient voltage. Besides these two transistors, the resistors $R_1$, $R_2$ and transistor $M_3$ were sized in order to

Table 3.6: Transistors size of the Shunt-series LDO.

| Device | Width ($\mu m$) | Length ($\mu m$) | Fingers | Multiplier |
|--------|-----------------|------------------|---------|------------|
| $M_1$ | 20 | 0.12 | 10 | 1 |
| $M_2$ | 40 | 3.60 | 20 | 1 |
| $M_3$ | 6 | 0.90 | 2 | 1 |
| $M_{b1}, M_{b2}$ | 3 | 2.04 | 2 | 1 |
| $M_{b3}, M_{b4}$ | 3 | 1.80 | 2 | 1 |
| $M_{b5}$ | 40 | 2.04 | 10 | 1 |

regulate the current at transistors $M_1$ and $M_2$, as well as ensuring that those transistors work in the saturation region.

## 3.8 Capacitor free LDO (CfLDO)

Contrary to the architectures studied previously, this one does not require the use of the error amplifiers studied in Section 3.3, because it already has two feedback loops where are used two error amplifiers (Figure 3.20). Thus it was only needed to size all the components in the circuit to achieve the desired specifications and do the biasing circuit for this buffer. But using the original circuit, the output voltage of this buffer would be different from the reference voltage. Therefore, it was made a little modification to the circuit to solve this problem, by removing the resistor $R_1$. Besides that, it was needed to set different speeds for the error amplifiers and, as the names suggest, the fast differential stage was set with a fast speed and the slow operational amplifier with a slow speed. In other words, the speed refers to the GBW of the amplifiers, which means that a fast speed corresponds to a higher GBW and a slow speed corresponds to a lower GBW. To biasing the circuit, it was used a simple current mirror like the one represented in Figure 3.16a.
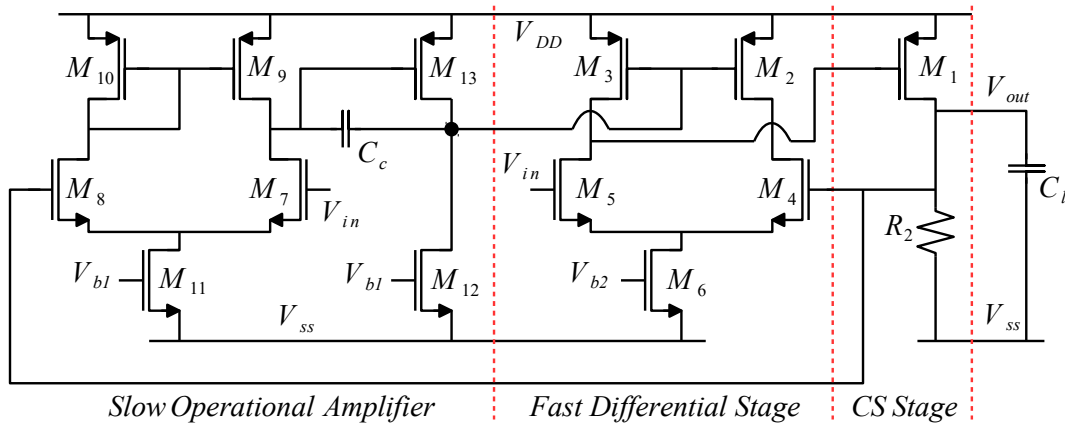


Figure 3.20: Capacitor free LDO.

The transistors of the circuit were sized according to Table 3.7. Besides that, $R_2 = 20\ K\Omega$, $C_c = 500\ fF$, $C_l = 1\ pF$, and $I_b = 2\ \mu A$, which means that the drain current of transistors $M_1$, $M_6$, $M_{11}$ and $M_{12}$ is respectively 83.78 $\mu A$, 7.86 $\mu A$, 2 $\mu A$ and 2 $\mu A$.

Table 3.7: Transistors size of the Capacitor free LDO.

| Device | Width ($\mu m$) | Length ($\mu m$) | Fingers | Multiplier |
|--------|-----------------|------------------|---------|------------|
| $M_1$ | 90 | 0.30 | 40 | 1 |
| $M_2, M_3$ | 4 | 0.90 | 2 | 1 |
| $M_4, M_5$ | 30 | 3.40 | 10 | 1 |
| $M_6$ | 8 | 2.04 | 4 | 1 |
| $M_7, M_8$ | 20 | 2.04 | 10 | 1 |
| $M_9, M_{10}$ | 2 | 1.20 | 2 | 1 |
| $M_{11}, M_{12}$ | 2 | 2.04 | 2 | 1 |
| $M_{13}$ | 40 | 0.90 | 20 | 1 |
| $M_b$ | 2 | 2.04 | 2 | 1 |

In order to achieve this results, transistor $M_1$ was set to work with a $gm/I_d \approx 20$, so it was sized to achieve a high $gm$, and therefore improving the performance of the circuit. For the error amplifiers were chosen other regions to work, in order to obtain the desired GBW as referred before. The transistor $M_4$ was set to work with a $gm/I_d \approx 24$, transistor $M_7$ was set to work with a $gm/I_d \approx 37$ and transistor $M_{13}$ was set to work with a $gm/I_d \approx 35$. Thus the slow operational amplifier was set to have a low GBW and a high gain and the fast differential stage was set to have a high GBW and a high gain. But due to stability problems, it was necessary to reduce the gain in both stages. Nevertheless, as both error amplifiers act together, the circuit still achieves the desired specification for the positive PSRR and is capable of keeping the output voltage equal to the reference voltage.
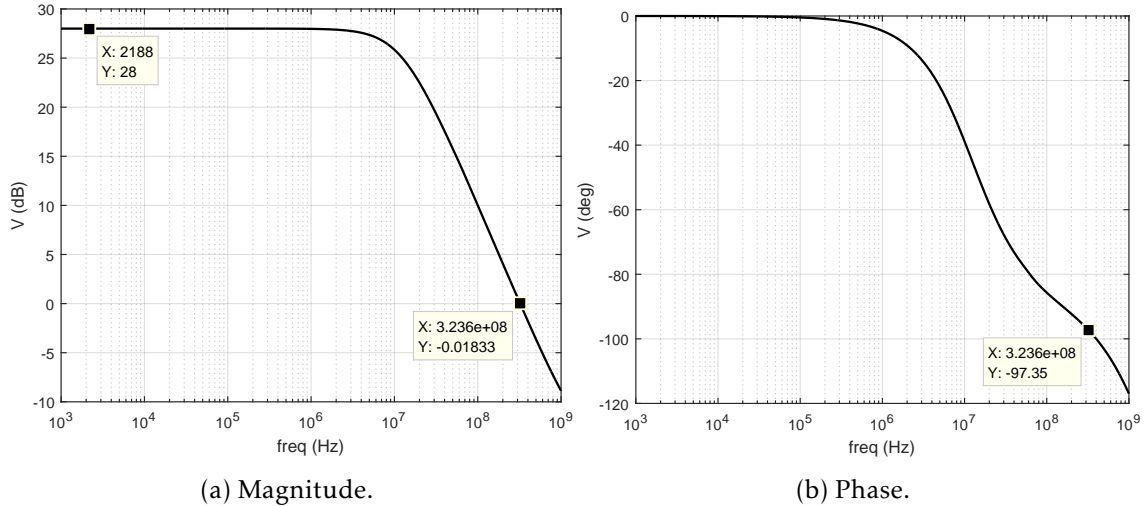


(a) Magnitude.



(b) Phase.

Figure 3.21: Frequency response of the fast differential stage.

Figures 3.21 and 3.22 represent the frequency response of the fast differential stage and of the slow operational amplifier respectively. For the fast differential amplifier was possible to obtain a gain of 28 $dB$, a phase margin of 82.65º and, as desired, a high GBW of approximately 323.6 $MHz$. On the other side, for the slow operational amplifier it was possible to obtain a gain of 20 $dB$, a phase margin of 92.46º and, as desired, a low GBW
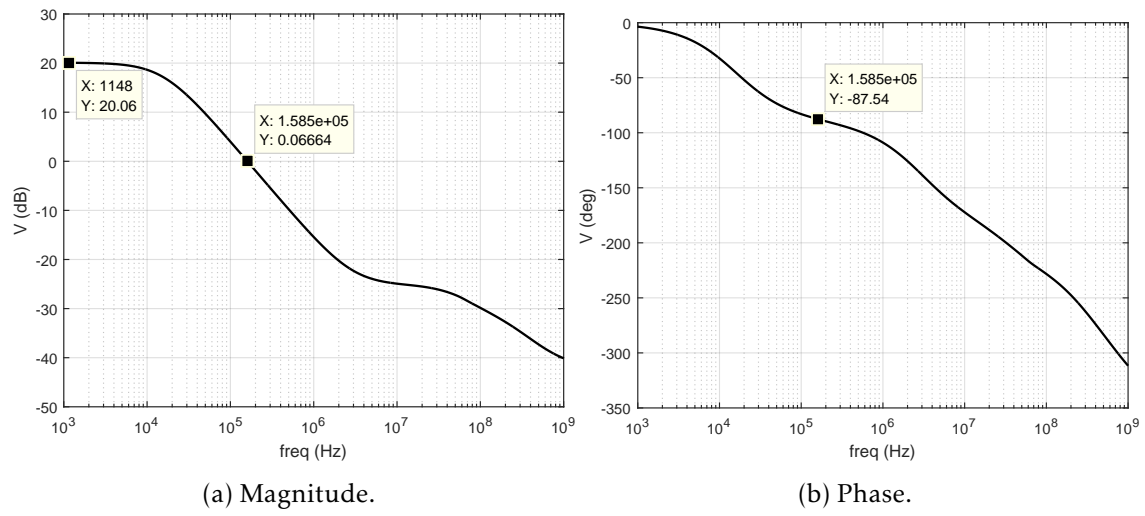
(a) Magnitude.

(b) Phase.

Figure 3.22: Frequency response of the slow operational amplifier.

of $\approx 158.5\ KHz$.

## 3.9 Buffered FVF (BFVF)

Unlike the previous architectures chosen to test, this one doesn't have error amplifiers in its original architecture. However, as seen before, its use is mandatory to regulate the reference voltage as pretended. Thus the error amplifiers studied in Section 3.3 are used in the simulations.
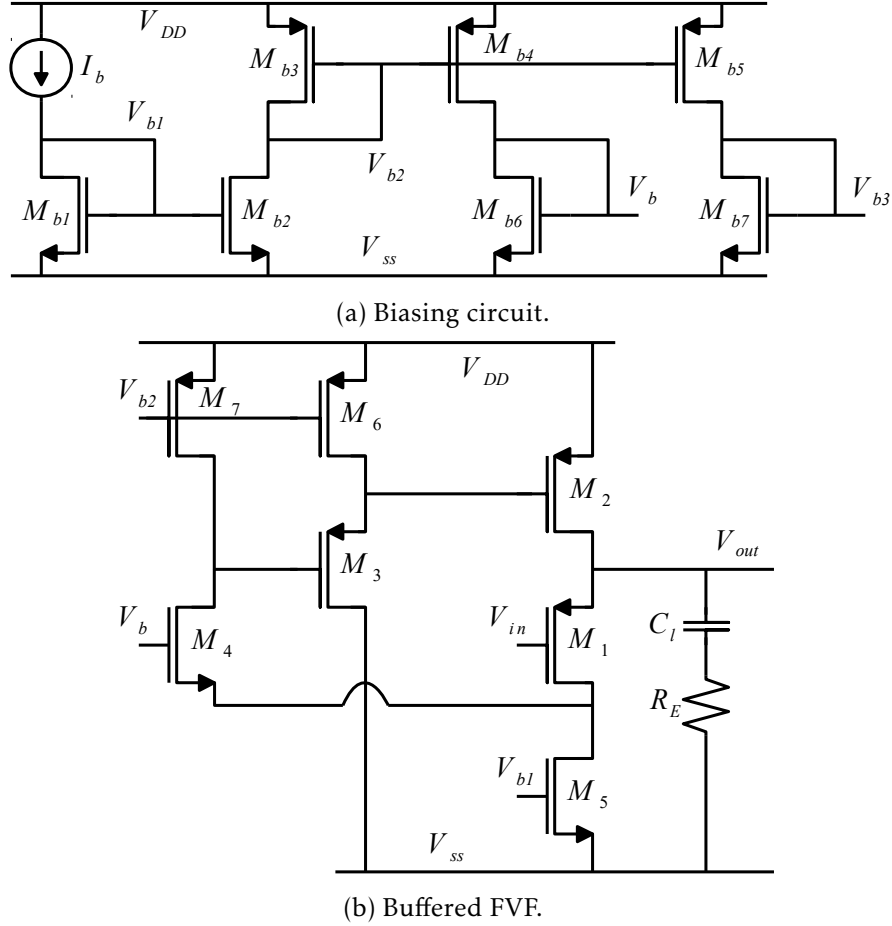


(a) Biasing circuit.



(b) Buffered FVF.

Figure 3.23: Buffered FVF with the biasing circuit.

As in the previous architectures, the simplified version of this circuit is no longer considered, so there were used transistors to substitute the ideal current sources. It was used the circuit present in Figure 3.23a to biasing the buffer and the error amplifier, where $V_b$, $V_{b1}$ and $V_{b2}$ are used as represented in the buffer (Figure 3.23b) and $V_{b3}$ is used to biasing the error amplifier. Taking this into account, the transistors used in both circuits were sized according to Table 3.8. Besides that $I_b = 20~\mu A$, $C_l = 1~pF$, and $R_E = 10~K\Omega$, which means that the drain current of transistors $M_1$, $M_5$, $M_6$ and $M_7$ is respectively 50.39 $\mu A$, 70.95 $\mu A$, 20.18 $\mu A$ and 20.57 $\mu A$.

To achieve this results, transistor $M_1$ was set to work with a $gm/I_d \approx 26$. This way, the transistor was set to have a high $gm$ in order to improve the gain. On the other side in first place, transistors $M_2$ and $M_4$ were also sized to have a high $gm$ and therefore decrease

Table 3.8: Transistors size of the Buffered FVF.

| Device | Width ($\mu m$) | Length ($\mu m$) | Fingers | Multiplier |
|--------|-----------------|------------------|---------|------------|
| $M_1$ | 40 | 0.12 | 20 | 1 |
| $M_2$ | 80 | 0.60 | 40 | 1 |
| $M_3$ | 70 | 2.40 | 40 | 1 |
| $M_4$ | 40 | 1.02 | 20 | 1 |
| $M_5$ | 11 | 2.04 | 4 | 4 |
| $M_6, M_7$ | 12 | 1.80 | 4 | 1 |
| $M_{b1}, M_{b2}$ | 12 | 2.04 | 4 | 1 |
| $M_{b3}, M_{b4}, M_{b5}$ | 12 | 1.80 | 4 | 1 |
| $M_{b6}$ | 4 | 2.04 | 2 | 1 |
| $M_{b7}$ | 3 | 2.04 | 2 | 1 |

the output impedance and increase the bandwidth of the circuit. But due to stability problems, it was crucial to increase the length of this transistors. Although transistor $M_3$ doesn't have a determinant relevance to improve the desired specifications, it was decisive to reach stability.

53

# 4

## Simulation Results

Considering the implementation done in the previous chapter it were obtained the results displayed in next sections. To understand the behaviour of the circuit in extreme situations, a corner simulation was done where some parameters are changed, such as the temperature of the circuit and the speed of the N and P channels. Therefore, all the results have a legend with this information, for example the legend *"FS ,T= - 40°"* means that the circuit was simulated with a temperature of -40 ºC, the N channel is fast and the P channel is slow. Besides that, the nominal simulation was made with a temperature of 27 ºC and with a regular speed for both N and P channels.

So the main objective of this study is to obtain the practical values of the theoretical concepts analysed in Chapter 2. This way, is possible to see if these architectures are good or not, as well as perceiving the advantages and disadvantages inherent to each one. Therefore, there is a section at the end of this chapter that allows to better see the differences of the architectures implemented through direct comparison.

## 4.1 Common Drain Amplifier

### 4.1.1 Miller compensated amplifier

Considering the architecture present in Figure 1.3, the following results were obtained using the DAC presented in Section 3.4 and the Miller compensated amplifier.

From the gain simulation (Figure 4.1) it can be seen that, when the N channel is fast and the temperature of the circuit is -40 ºC, some poles on the circuit become complex. Therefore, the gain magnitude of the circuit increases before the bandwidth frequency . The same situation occurs when the P channel is slow and the temperature is 125 ºC. In other cases is also observable the effects of the complex poles created by those extreme conditions, but nevertheless the cases referred are the worse scenarios.
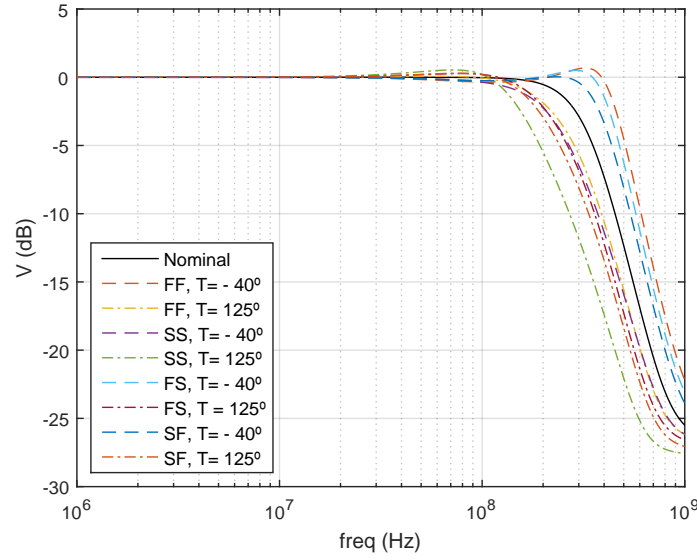
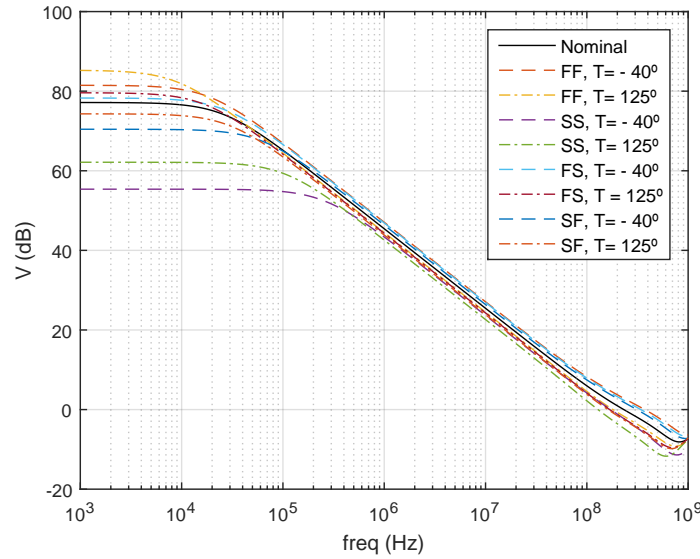Figure 4.1: Gain of the CD amplifier, using the Miller compensated amplifier.



Figure 4.2: Positive power supply rejection ratio of the CD amplifier, using the Miller compensated amplifier.

According to the Table 1.1 is desired to obtain a positive PSRR greater than 40 $dB$ and, even in the worse case, this circuit can fulfil that specification. In Figure 4.2 are presented the results obtained by this circuit. By observation is possible to conclude that when both N and P channels are slow the circuit presents the worse behaviour.

For the output impedance was desired to obtain a DC value smaller that 500 $\Omega$, which means that, in the lowest frequencies, the output impedance has to assume values lower than 500 $\Omega$. In Figure 4.3b is possible to see that even the worse case overcome the specification. Besides this it's also observable a perturbation in higher frequencies, where the value of the output impedance reach its highest value. But, as this only happens in

(a) Without zoom.

(b) With zoom.
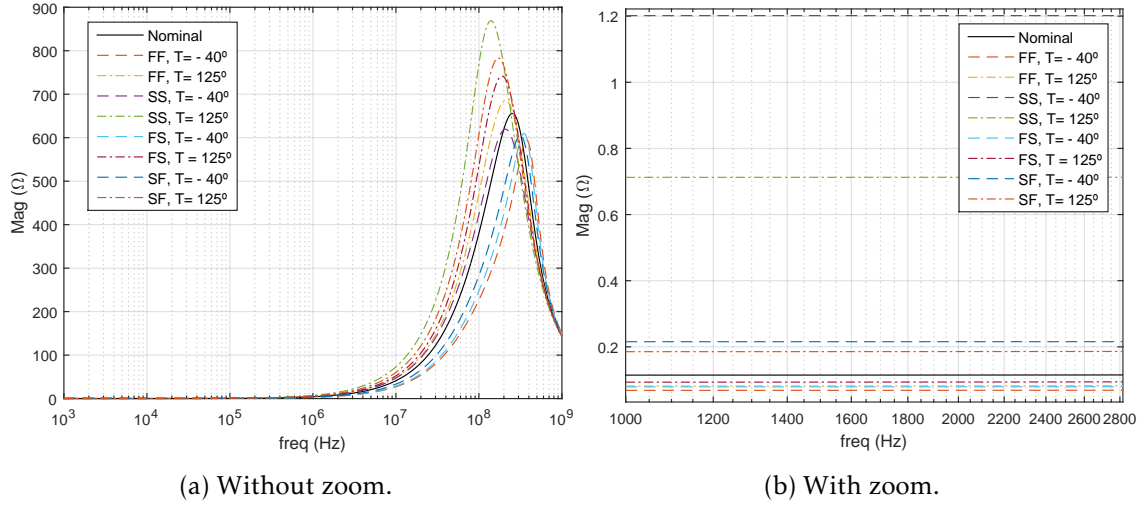
Figure 4.3: Output Impedance of the CD amplifier, using the Miller compensated amplifier.

an little interval of frequency, it doesn't affect the overall proprieties of the buffer.



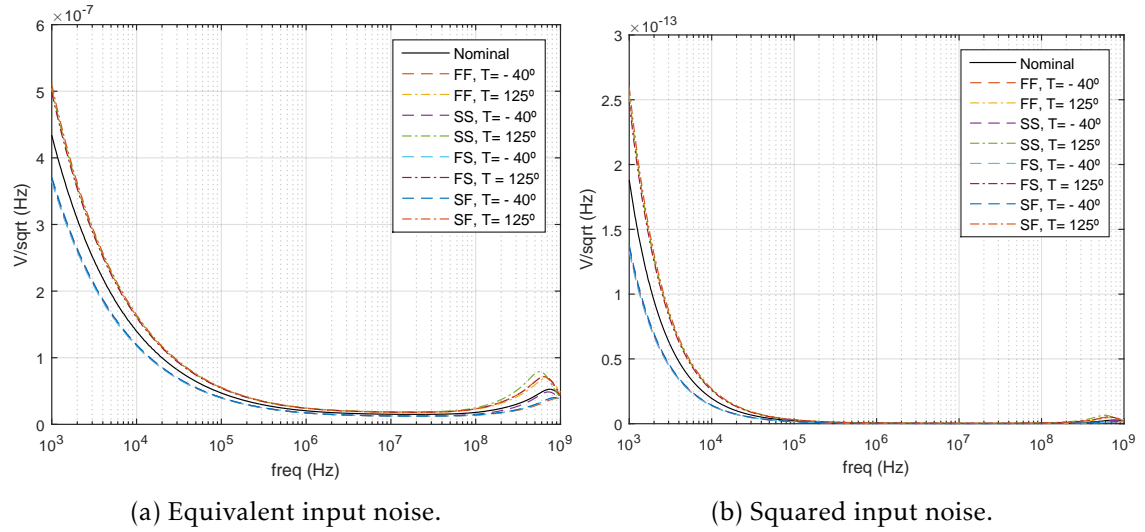(a) Equivalent input noise.

(b) Squared input noise.

Figure 4.4: Input referred noise of the CD amplifier, using the Miller compensated amplifier.

With regard to the noise (Figure 4.4), it's possible to see an higher impact for low frequencies than for higher ones, which means that the flicker noise (with higher impact at low frequencies) is affecting the system, and this happens because there were only taken measures to reduce the thermal noise (with higher impact at high frequencies). Nevertheless, assuming that the ADC to use in the future has at least an Oversampling Ratio (OSR)=100, this buffer fulfil the desired specification of noise.

Once the overall characteristics of the buffer are studied, the next step is to observe its behaviour at the output. In Figure 4.5 is possible to see that the output voltage of the buffer isn't always constant at 1.2 $V$. This happens because the DAC has two digital signals in

57

(a) Without zoom.

(b) With zoom.
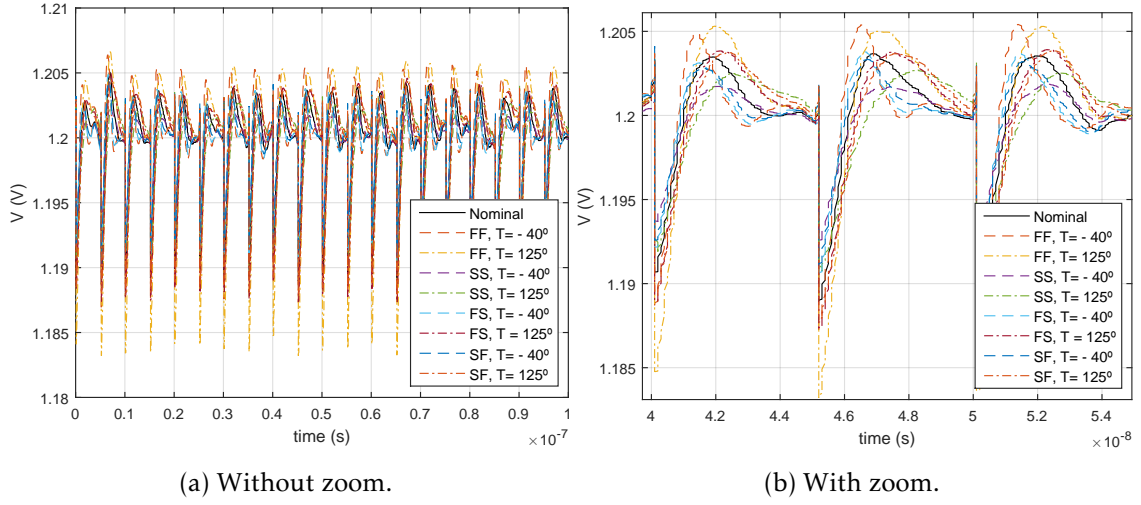
Figure 4.5: Output transient voltage of the CD amplifier, using the Miller compensated amplifier.
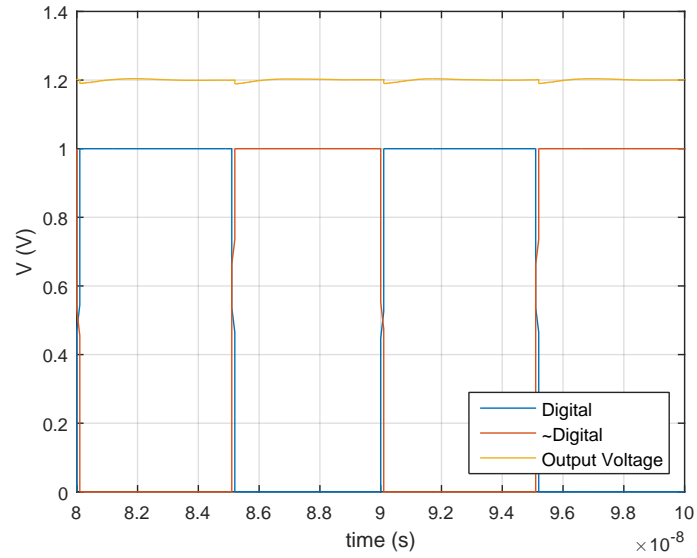


Figure 4.6: Perturbation in the output voltage.

its input, being that these signals are reversed, so the peaks of voltage happen when the signals change from 0 to 1 and from 1 to 0 respectively (Figure 4.6). This generates a cyclic behaviour because the buffer with the error amplifier is fast enough to stabilize the system before the next iteration of the digital signals.

As it happens in the output voltage, the output current also has a cyclic behaviour (Figure 4.7), where the perturbations occur at the same time of the perturbations in the output voltage.

Taking into account that the transient signals represented above have some noise, it's normal that at the end of each period the voltage obtained isn't always the same.

Therefore, the methodology used to measure the output transient voltage noise (also explained in Section 3.5) is through the integration of the transient current. That allows to

(a) Without zoom.

(b) With zoom.
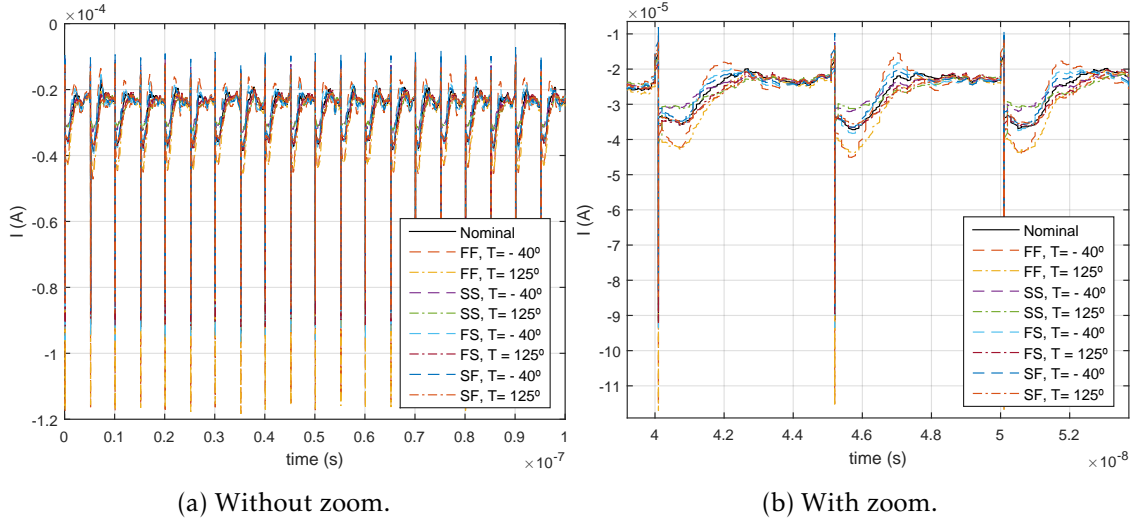
Figure 4.7: Output transient current of the CD amplifier, using the Miller compensated amplifier.

obtain a representative histogram of the charge at the output of the buffer (Figure 4.8) and the value of noise in the transient voltage, by doing the following calculation $\frac{\Delta Q}{T_{clk}} R$, where $R$ is the resistance at the output of the DAC, $T_{clk}$ is the period of the digital signals at the input of the DAC and $\Delta Q$ is the variation of charge at the output (Figure 4.8). This way, the output transient voltage noise is $2\ mV$.
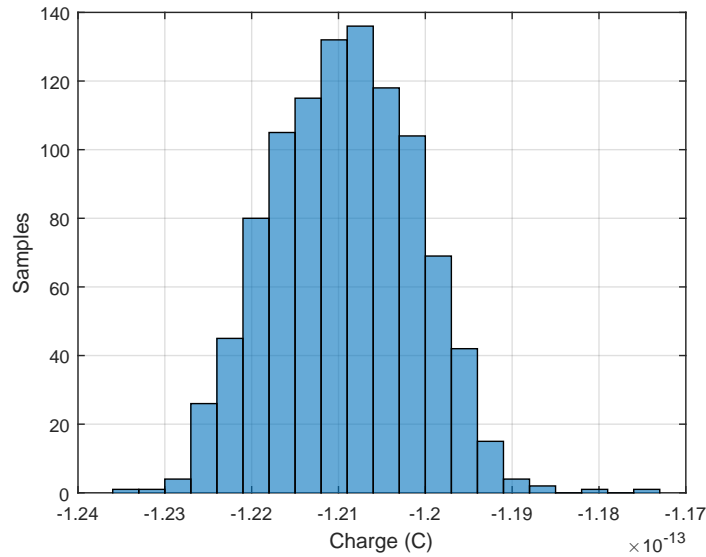


Figure 4.8: Charge at the output of the CD amplifier, using the Miller compensated amplifier.

### 4.1.2 Current Mirror OTA

In order to better understand the influence of the error amplifier in the system, this section presents the same simulations of the previous one, but now using the Current Mirror OTA as an error amplifier.
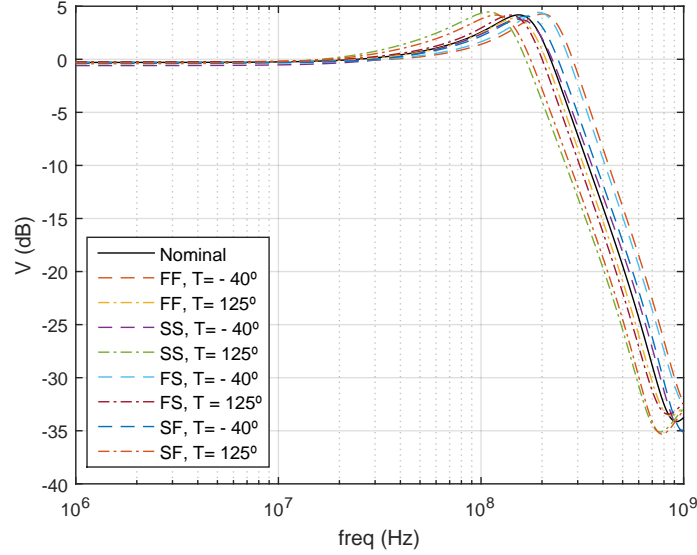


Figure 4.9: Gain of the CD amplifier, using the Current Mirror OTA.

For the gain (Figure 4.9), the circuit is capable of keeping it equal to one, but it's observable that the complex poles in the system have a bigger imaginary part, which causes some perturbation at a frequency of 100 $MHz$.
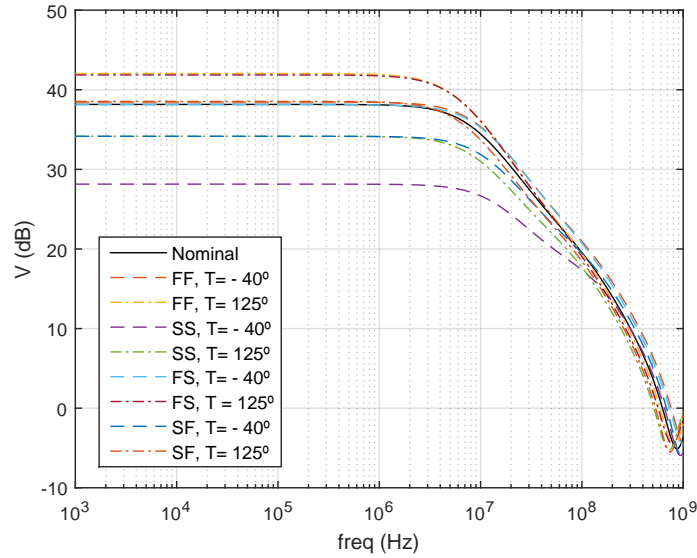


Figure 4.10: Positive power supply rejection ratio of the CD amplifier, using the Current Mirror OTA.

However, since this error amplifier has a lower gain than the previous one, the positive

PSRR decreases drastically (Figure 4.10) and, therefore, the CD amplifier is no longer capable of keeping a positive PSRR greater than 40 $dB$, not even for the nominal simulation.
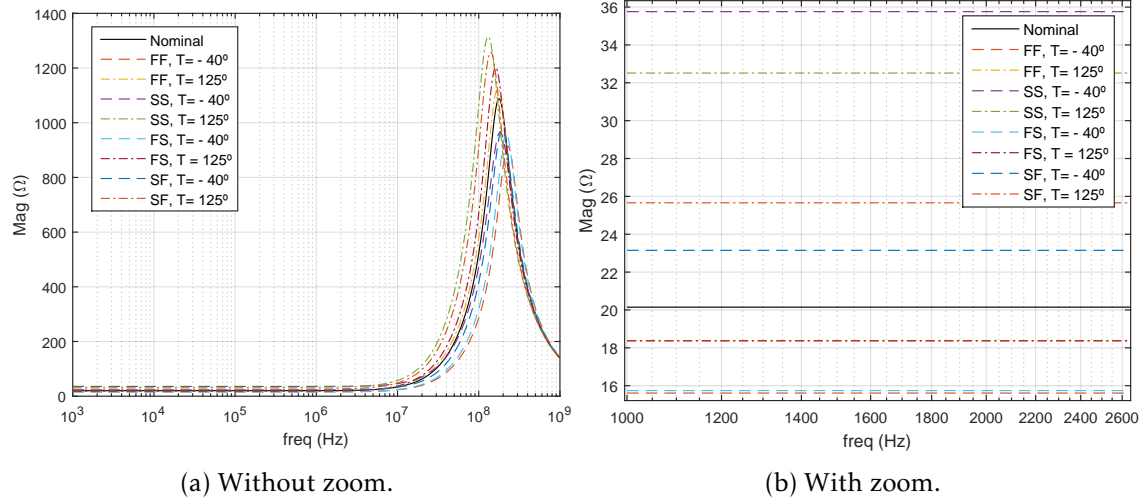


(a) Without zoom.

(b) With zoom.

Figure 4.11: Output Impedance of the CD amplifier, using the Current Mirror OTA.

In the output impedance (Figure 4.11), the circuit is still capable of keeping it lower than 50 Ω at lower frequencies, but there is clearly a growth all along with the frequency, which is due to the lower gain of this error amplifier.



(a) Equivalent input noise.

(b) Squared input noise.
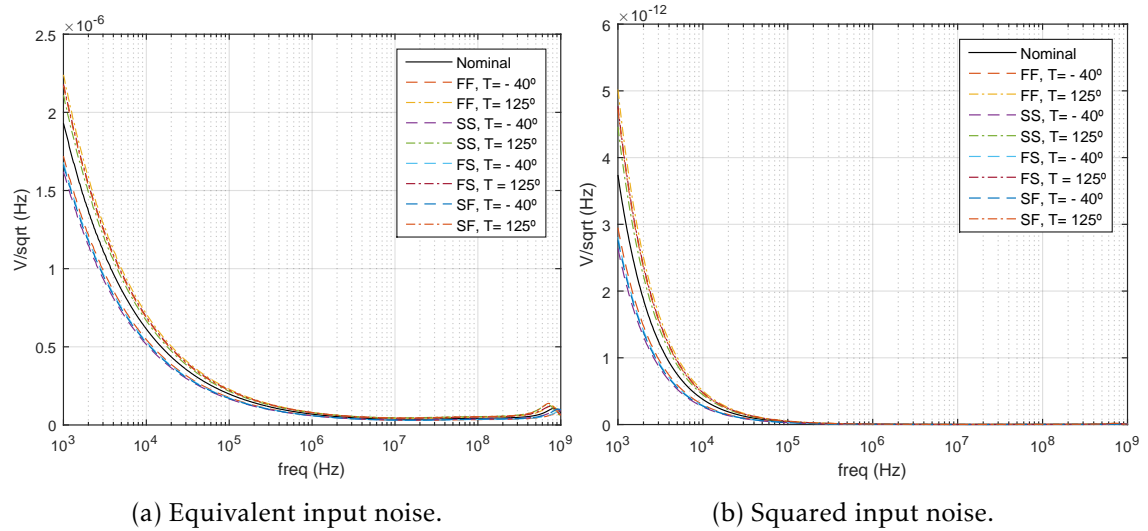
Figure 4.12: Input referred noise of the CD amplifier, using the Current Mirror OTA.

With this error amplifier the level of noise also increases (Figure 4.12), but considering the desired specification, the circuit is still capable of achieving it.

However, this circuit is not capable of keeping the reference voltage provided in its input at its output (Figure 4.13), which isn't desirable and makes this circuit useless.

But even with an unacceptable transient voltage at is output, the output transient current is still very similar to the one obtained with the previous error amplifier (Figure 4.14),
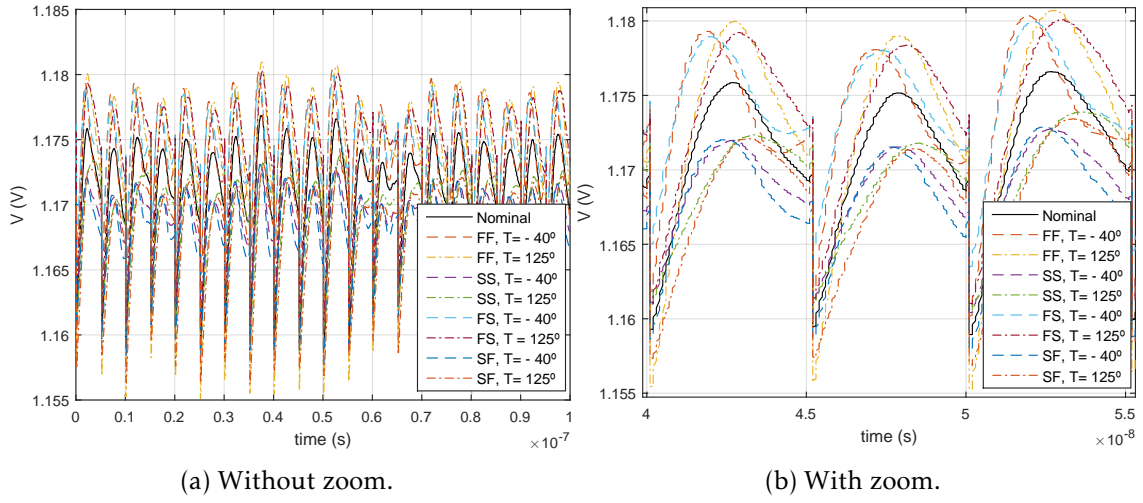
(a) Without zoom.

(b) With zoom.

Figure 4.13: Output transient voltage of the CD amplifier, using the Current Mirror OTA.
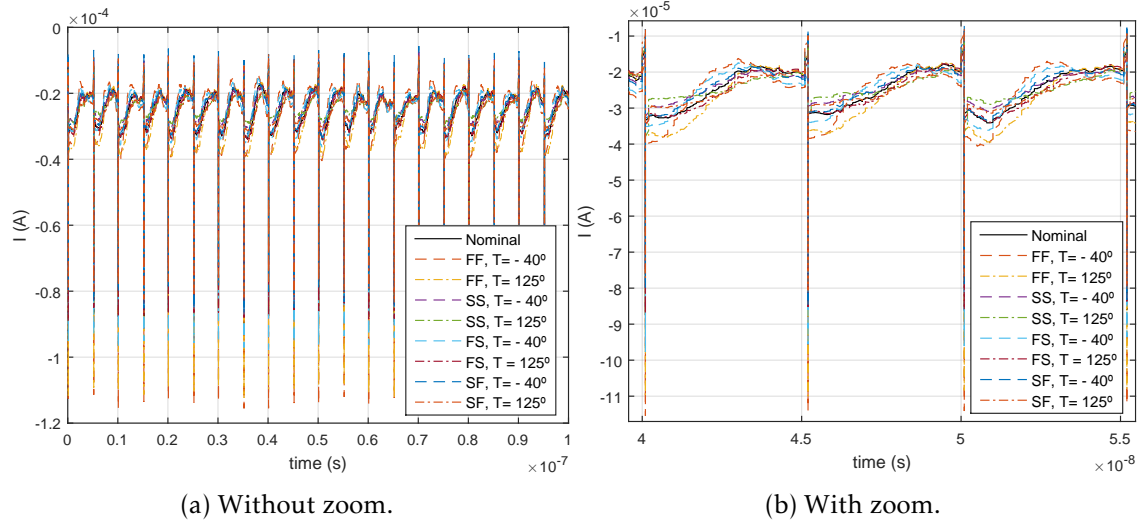


(a) Without zoom.

(b) With zoom.

Figure 4.14: Output transient current of the CD amplifier, using the Current Mirror OTA.

meaning that the error amplifier has no influence in this parameter.

Finally, as the output transient voltage results aren't acceptable, the measurement of the output transient voltage noise isn't reliable. Nevertheless it's displayed the histogram of the charge in Figure 4.15 and the value of the output transient voltage noise is 3.7 $mV$.
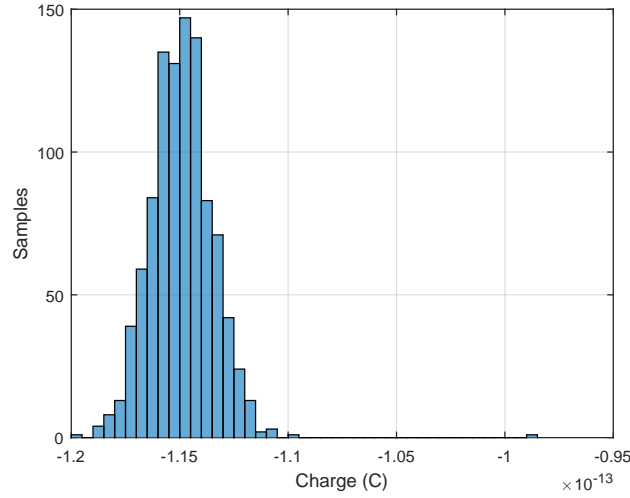
Figure 4.15: Charge at the output of the CD amplifier, using the Current Mirror OTA.

## 4.2 Shunt-series LDO (SsLDO)

### 4.2.1 Miller compensated amplifier

Based on the implementation done in previous chapter, and using the Miller compensated amplifier, was made a corner simulation to see the behaviour of the circuit in extreme conditions. As in the Common Drain amplifier, there are some situations were the circuit poles become complex. However, its imaginary values are lower than in the previous situation, meaning that its impact is less significant (Figure 4.16).
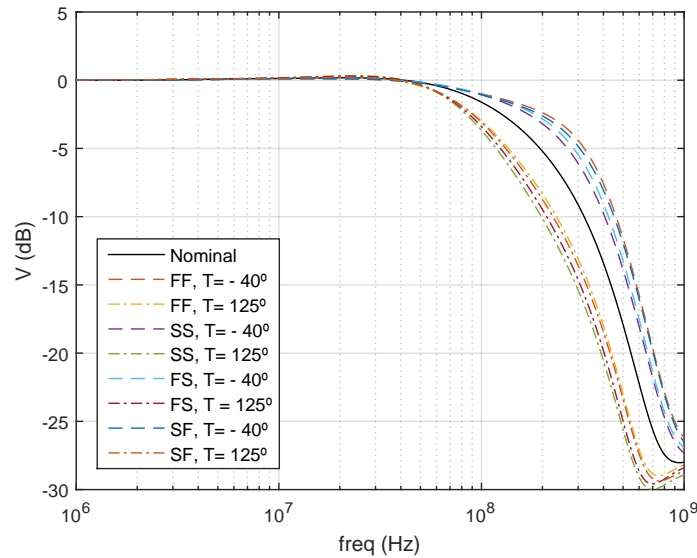


Figure 4.16: Gain of the SsLDO, using the Miller compensated amplifier.

The positive PSRR in this circuit (Figure 4.17) is much higher than in the previous buffer, being always greater than 80 $dB$ for lower frequencies. However, it turns out that its bandwidth decreases as the PSRR increases.
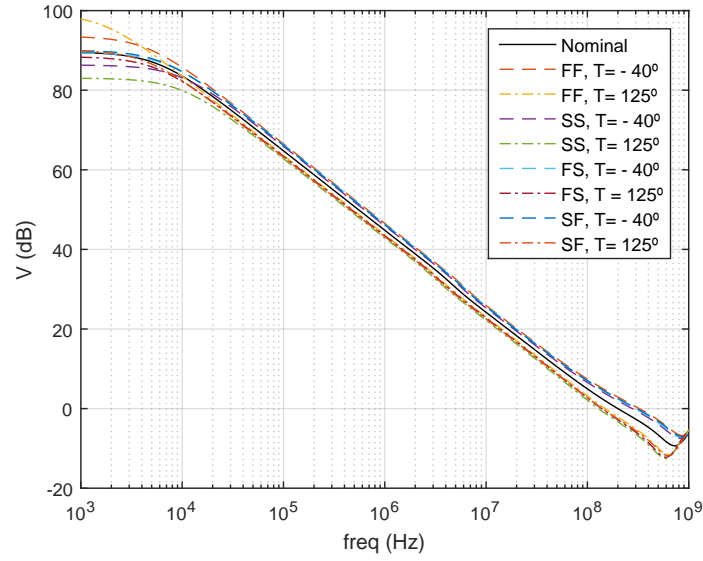
63

Figure 4.17: Positive power supply rejection ratio of the SsLDO, using the Miller compensated amplifier.

In the output impedance (Figure 4.18) of the circuit there is, once again, a perturbation in the highest frequencies, where the impedance even reaches values very close to 1 $K\Omega$. But, as pretended for the lowest frequencies, its value is small and even in the worst case its value is below 2 $m\Omega$.
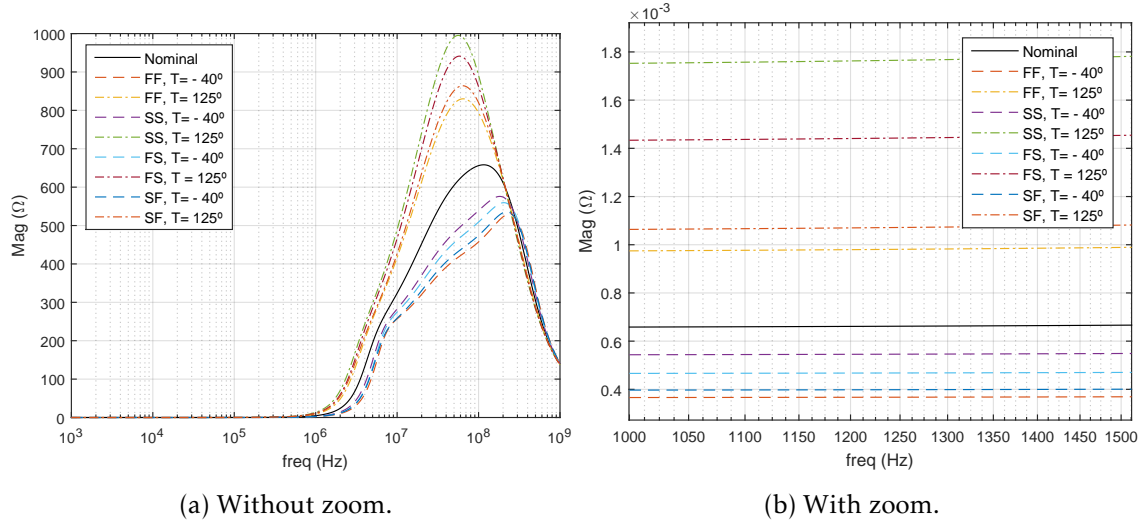


(a) Without zoom.

(b) With zoom.

Figure 4.18: Output Impedance of the SsLDO, using the Miller compensated amplifier.

Regarding the noise (Figure 4.19), this circuit has the same behaviour than the previous one, so there is, once again, a higher impact of the flicker noise.

Given that the main characteristics of the buffer assume results as expected, it's time to observe the transient response of this circuit. In the case of the output transient voltage (Figure 4.20), it's possible to see that it takes some time to stabilize in a value and after it remains constant with a cyclic behaviour. In the Figure 4.20b is represented the

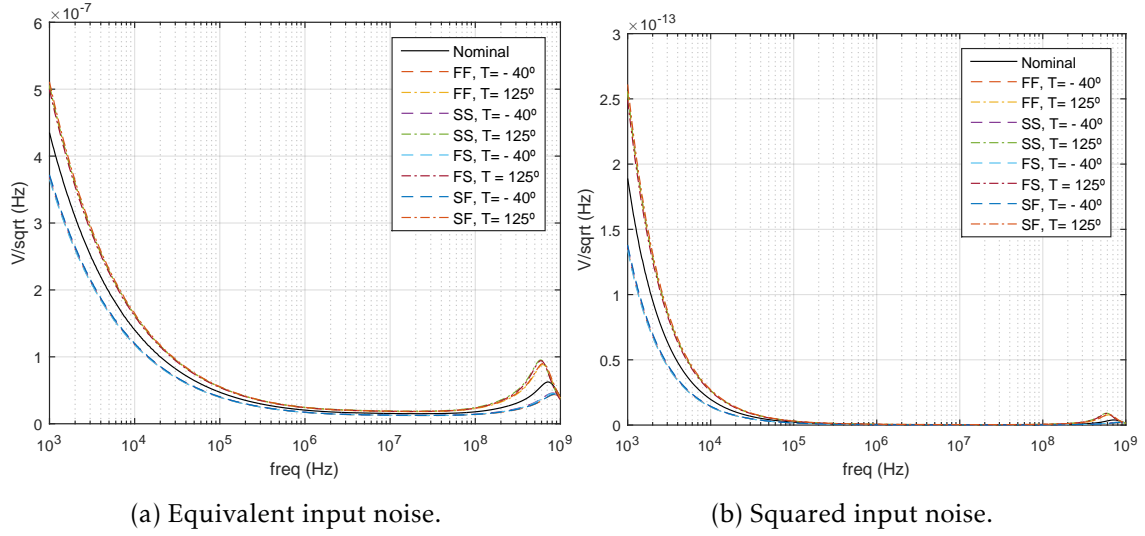(a) Equivalent input noise.

(b) Squared input noise.

Figure 4.19: Input referred noise of the SsLDO, using the Miller compensated amplifier.

aforementioned phenomenon and it's observable the perturbations caused by the DAC. Besides that it's also possible to see a faster response of the circuit when its temperature is -40 ºC, and an higher perturbation in the output voltage when the N channel is fast.
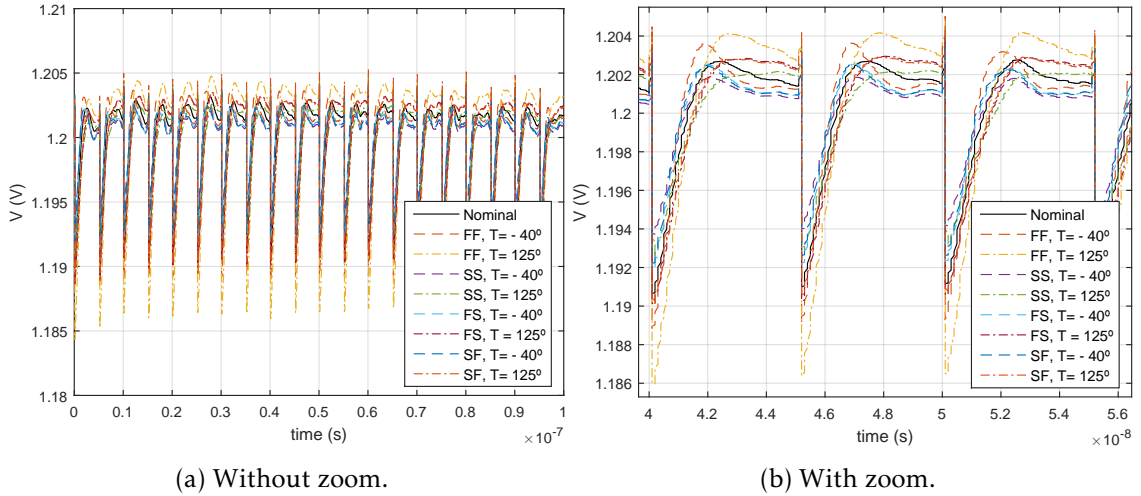


(a) Without zoom.

(b) With zoom.

Figure 4.20: Output transient voltage of the SsLDO, using the Miller compensated amplifier.

For the output transient current (Figure 4.21) it's once again observed a cyclic behaviour where the output current suffers a big perturbation when the digital signals of the DAC change from 0 to 1 and from 1 to 0, respectively. As observed in the output voltage, a lower temperature on the circuit corresponds to a faster response of it, but it also an higher perturbation in the current at the output.

By the output transient current is also possible to obtain the histogram of charge at the output (Figure 4.22) and, this way, obtain an output transient voltage noise of $1.8 \ mV$.

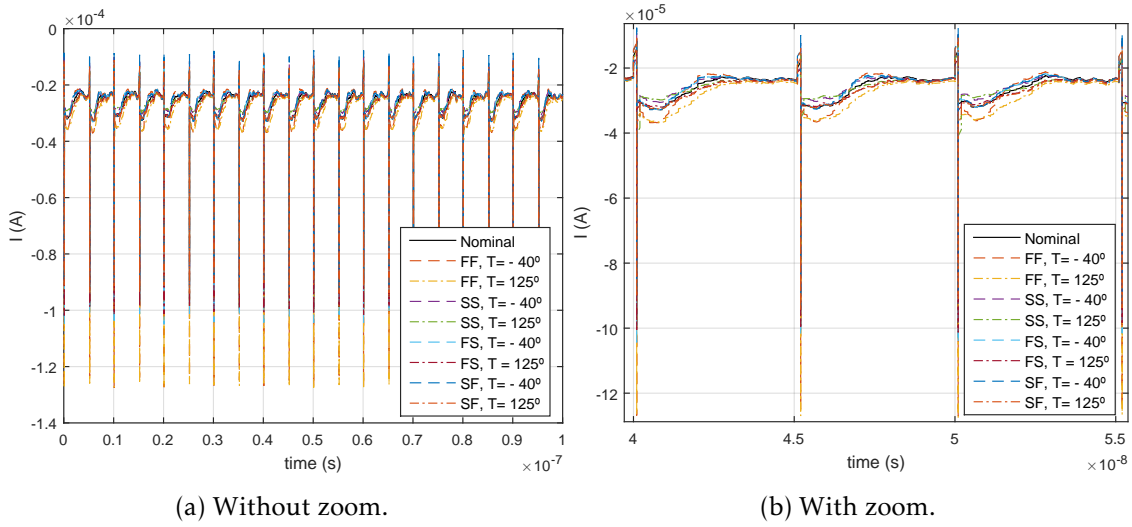(a) Without zoom.

(b) With zoom.

Figure 4.21: Output transient current of the SsLDO, using the Miller compensated amplifier.
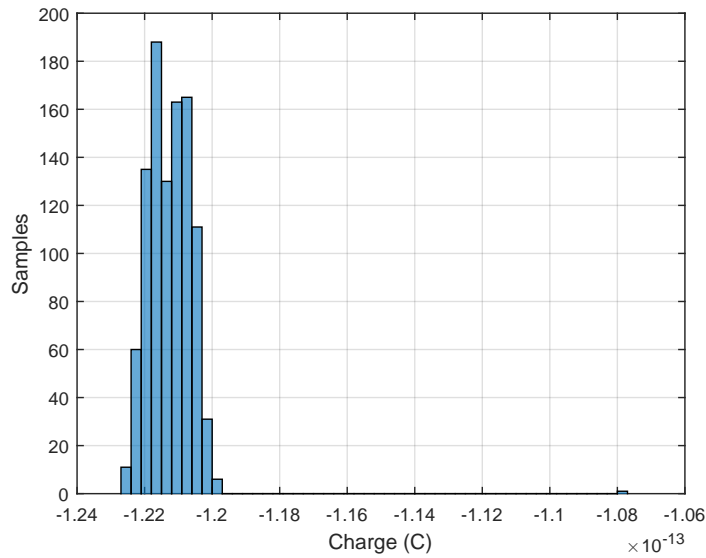


Figure 4.22: Charge at the output of the SsLDO, using the Miller compensated amplifier.

## 4.2.2 Current Mirror OTA

As done in the previous buffer, this one is also tested with two different error amplifiers to see the influence of it in the system.

Regarding the gain (Figure 4.23), it's once again observable that this error amplifier increases the imaginary part of the complex poles, creating a perturbation at higher frequencies. However, it doesn't affect the behaviour of the buffer.

For the positive PSRR it's observable a decrease on its value (Figure 4.24), but nevertheless the circuit is capable of achieving values greater than $40\ dB$, as pretended. One advantage of this error amplifier when compared to the previous one is that it increases the bandwidth and the GBW of the positive PSRR.
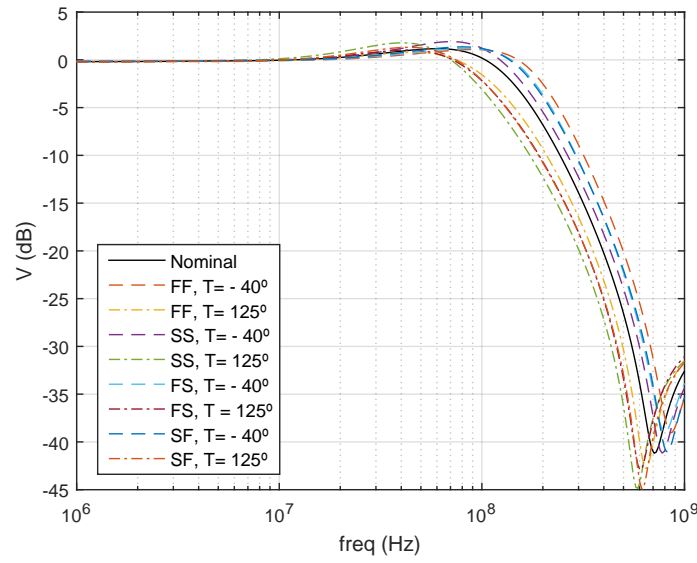
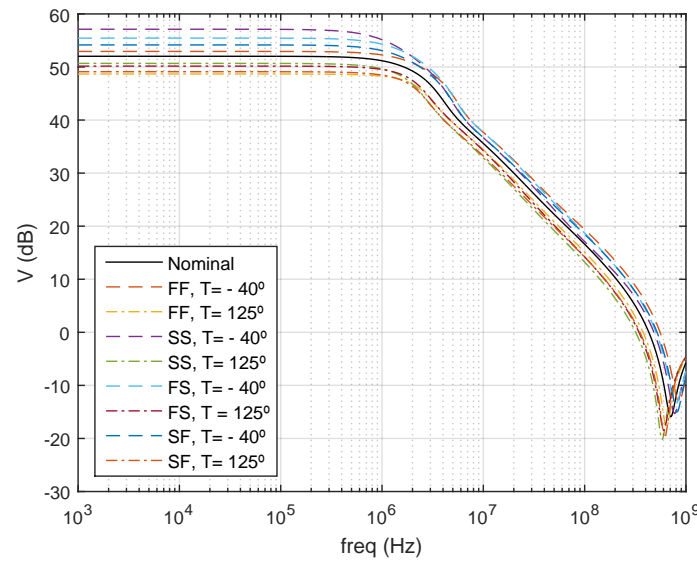Figure 4.23: Gain of the SsLDO, using the Current Mirror OTA.



Figure 4.24: Positive power supply rejection ratio of the SsLDO, using the Current Mirror OTA.

In the output impedance (Figure 4.25), it's observable once again an increase of its value along the frequency, despite its value at lower frequencies still being lower than 200 $m\Omega$.

The levels of noise also increase with this error amplifier for this buffer (Figure 4.26), but considering the desired specification, this growth is not relevant to fulfil it.
For the output transient voltage (Figure 4.27) it's observable a similar behaviour to the previous error amplifier, but it's also observable a slightly slower response to the pertur-bations with this error amplifier. Still the circuit continues to have the expected reference voltage in its output.
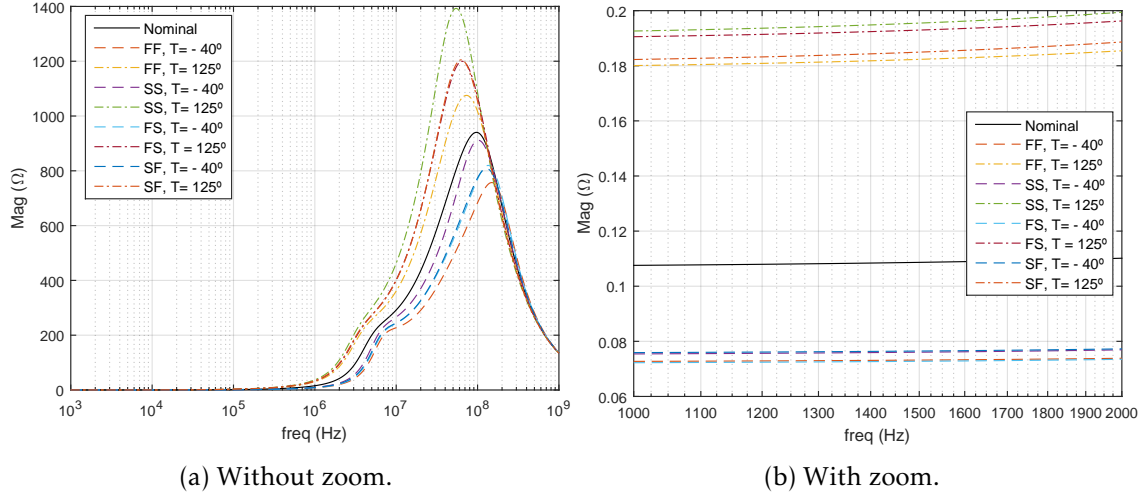
(a) Without zoom.

(b) With zoom.

Figure 4.25: Output Impedance of the SsLDO, using the Current Mirror OTA.



(a) Equivalent input noise.

(b) Squared input noise.
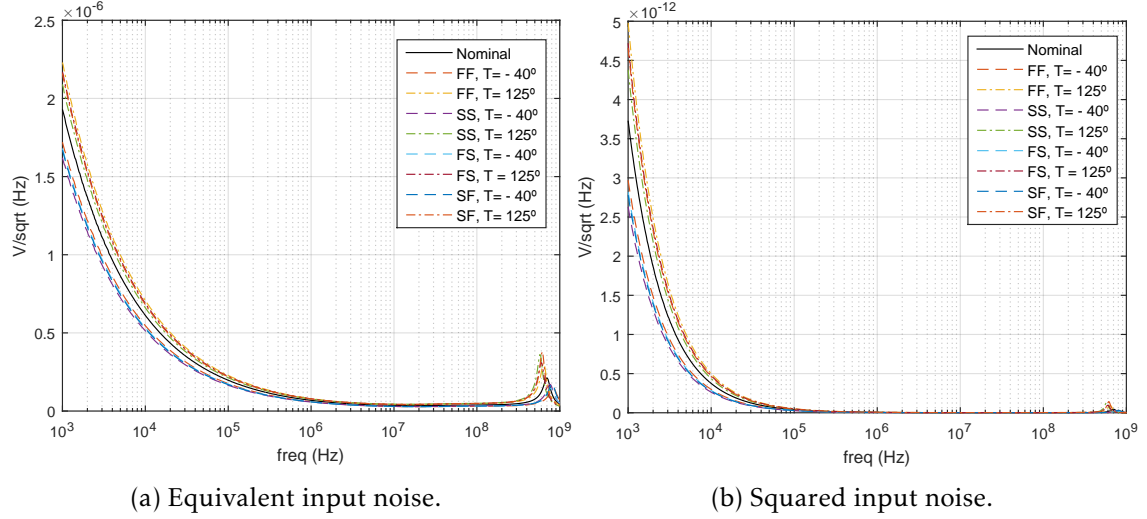
Figure 4.26: Input referred noise of the SsLDO, using the Current Mirror OTA.



(a) Without zoom.

(b) With zoom.
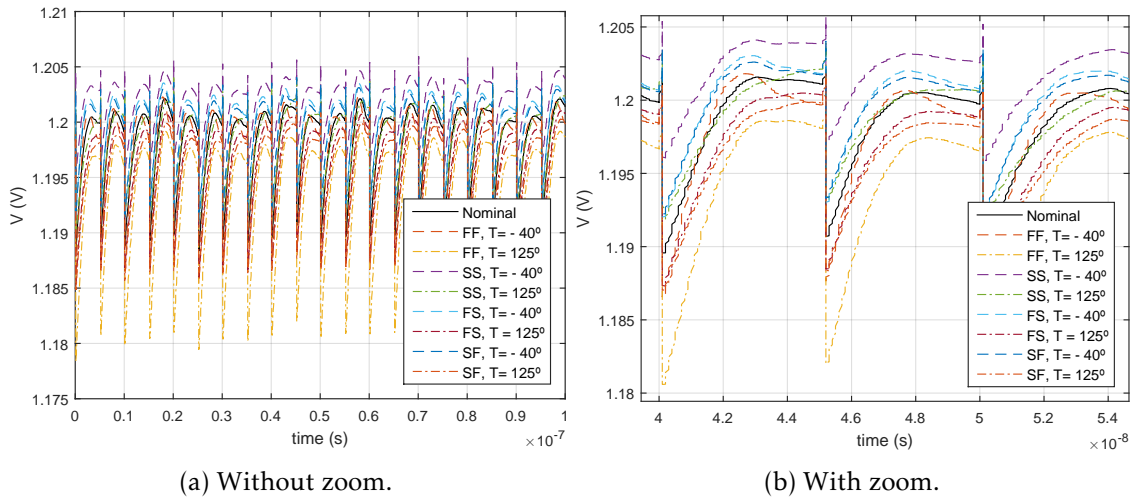
Figure 4.27: Output transient voltage of the SsLDO, using the Current Mirror OTA.
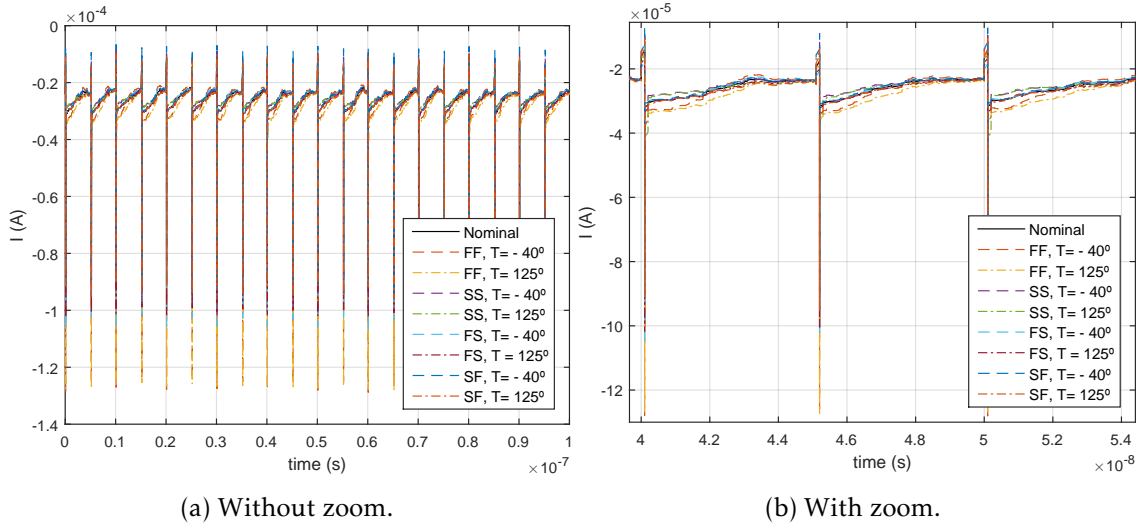
(a) Without zoom.

(b) With zoom.

Figure 4.28: Output transient current of the SsLDO, using the Current Mirror OTA.

In the output transient current (Figure 4.28), there are no significant changes in it's behaviour compared to the previous error amplifier.

Regarding the output transient voltage noise, it's possible to observe once again that this error amplifier has a higher noise, with a measured value of 2.5 $mV$. Figure 4.29 shows the charge at the output.
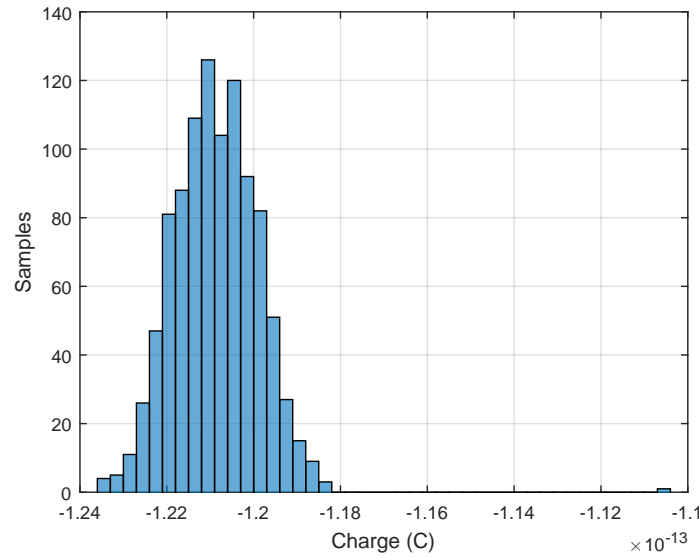


Figure 4.29: Charge at the output of the SsLDO, using the Current Mirror OTA.

## 4.3 Capacitor free LDO (CfLDO)

Considering the implementation done in previous chapter, was made a corner simulation to test the behaviour of the circuit for extreme conditions. It was obtained the gain present in Figure 4.30 where it's observable that the system has complex poles, because
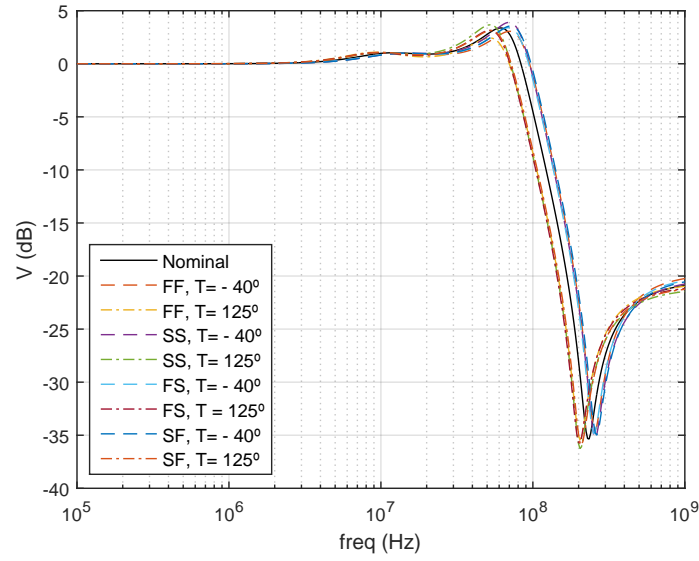
there is a perturbation before 100 $MHz$.



Figure 4.30: Gain of the CfLDO.

For the positive PSRR (Figure 4.31) this buffer can achieve values greater than 80 $dB$ at lower frequencies, and the error amplifiers used in this architecture also allow to have a large bandwidth.
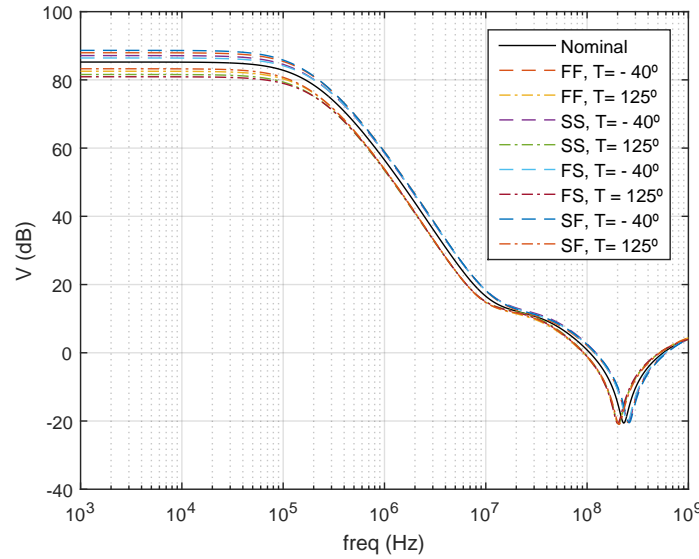


Figure 4.31: Positive power supply rejection ratio of the CfLDO.

In the output impedance (Figure 4.32), this architecture allows to obtain a DC value lower than 1.8 $m\Omega$, but, as in the previous ones, there is a perturbation in higher frequencies, where its value reaches 3 $K\Omega$ in the worst situations.

Regarding the noise (Figure 4.33), it's observable a greater impact of the flicker noise in lower frequencies, but there is also a greater amount of thermal noise for higher frequencies, when compared to the previous buffers. Nevertheless, assuming a OSR=100, the
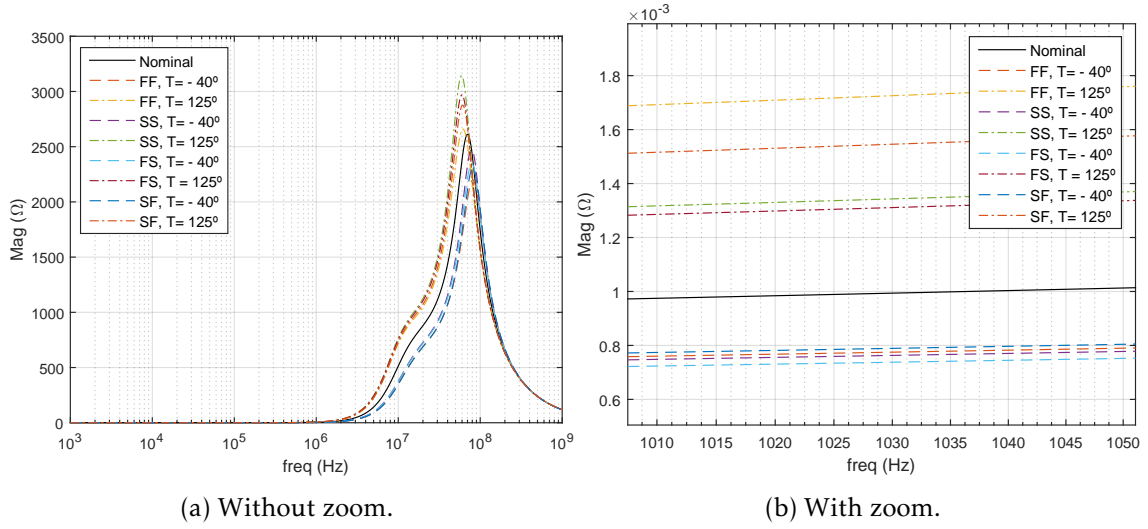
(a) Without zoom.

(b) With zoom.

Figure 4.32: Output Impedance of the CfLDO.

buffer still meets the desired specification.
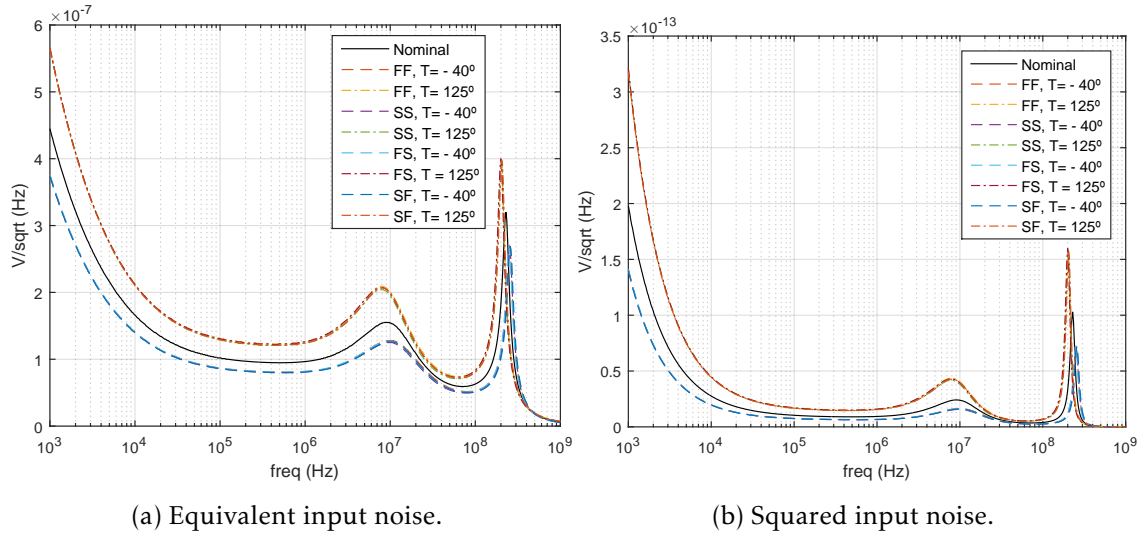


(a) Equivalent input noise.

(b) Squared input noise.

Figure 4.33: Input referred noise of the CfLDO.

Considering Figure 4.34 it's observable that this buffer has a slower response to the perturbations caused by the DAC, therefore, the output transient voltage starts to assume a sinusoidal behaviour around 1.2 $V$.

For the output transient current (Figure 4.35) is observed a behaviour similar to the previous architectures, even with a slower response in the output transient voltage.

By the output transient current is also possible to obtain the histogram of charge at the output (Figure 4.36) and, this way, obtain an output transient voltage noise of 2.7 $mV$.
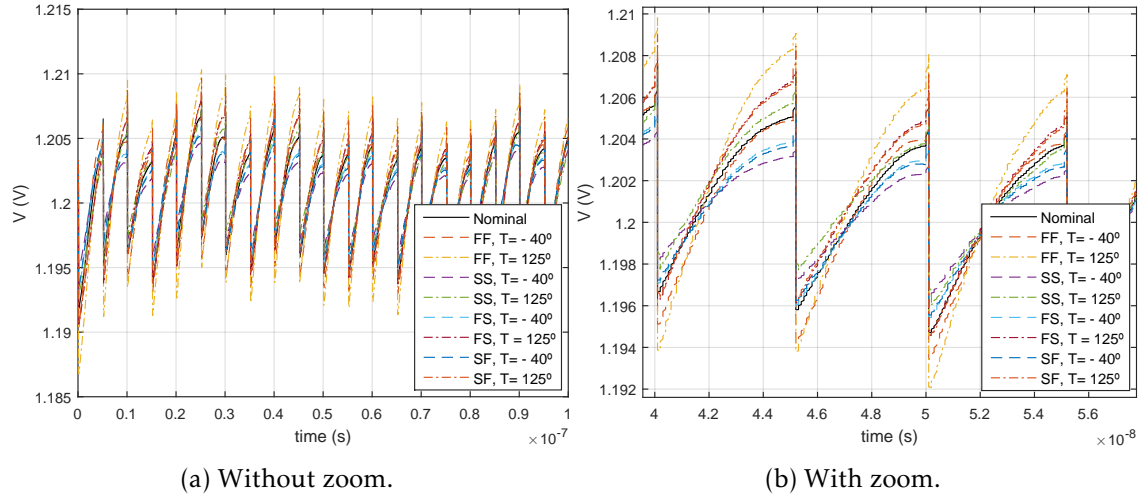
(a) Without zoom.

(b) With zoom.

Figure 4.34: Output transient voltage of the CfLDO.



(a) Without zoom.
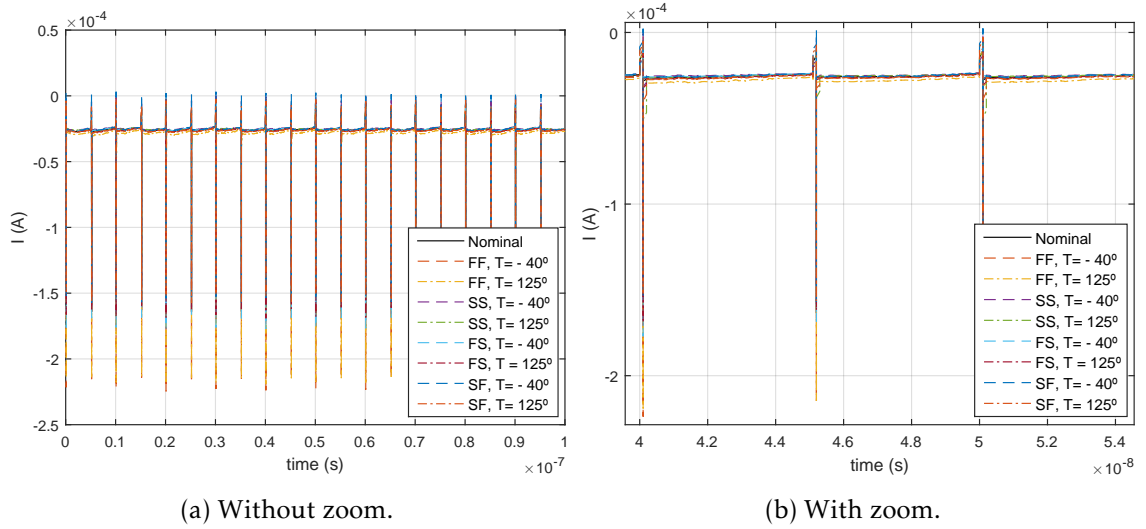
(b) With zoom.

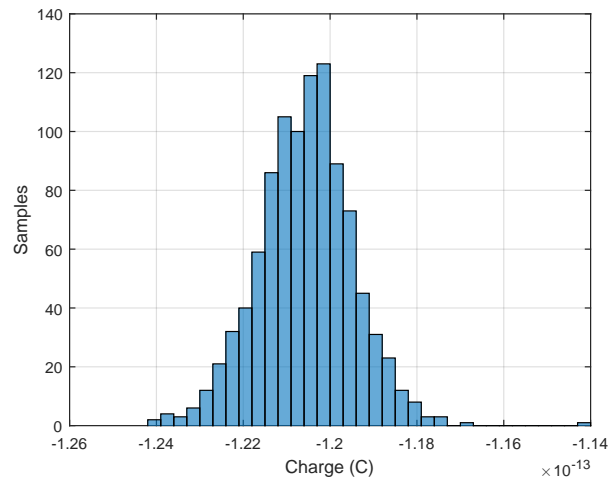Figure 4.35: Output transient current of the CfLDO.



Figure 4.36: Charge at the output of the CfLDO.

## 4.4 Buffered FVF (BFVF)

### 4.4.1 Miller compensated amplifier

Based on the implementation done in previous chapter, was made a corner simulation in order to see the behaviour of the circuit in extreme conditions. It was obtained the gain present in Figure 4.37 where it's observable that the temperature of the circuit has a greater impact in this parameter.
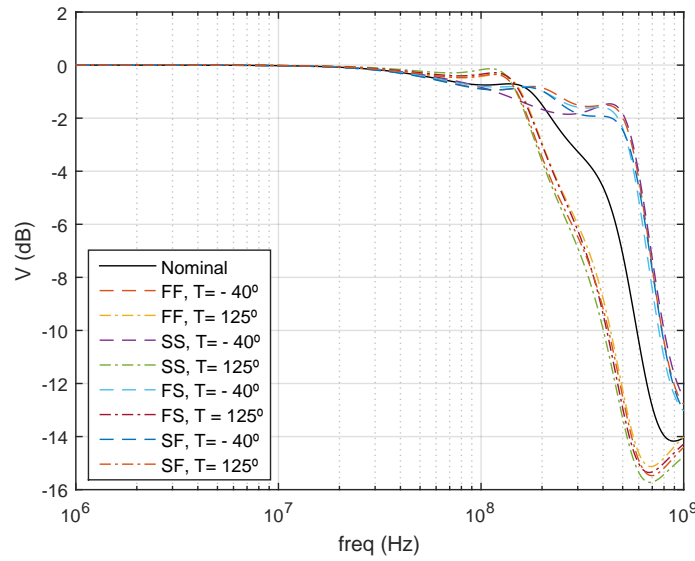


Figure 4.37: Gain of the BFVF, using the Miller compensated amplifier.

For the positive PSRR (Figure 4.38), it's observable a behaviour similar to the SsLDO, where is possible to obtain values greater than 80 $dB$ for lower frequencies and also a GBW between 100 and 300 $MHz$. Both BFVF and SsLDO have a similar behaviour in the positive PSRR, because the error amplifier used in both is the same and, as seen before, the error amplifier has a big influence in this parameter.

In this case, the output impedance (Figure 4.39) has a DC value lower than 400 $\mu\Omega$ in almost all the cases except for the case "SS ,T= - 40º", where its value is greater than 6 $m\Omega$. Nevertheless the buffer still meets the output impedance specification. For higher frequencies it's once again observable a perturbation where the output impedance reaches almost 2 $K\Omega$, but that doesn't affect the behaviour of the buffer.

The input referred noise (Figure 4.40) presents a very similar behaviour to the SsLDO architecture, where it's observable a bigger influence of the flicker noise for lower frequencies and a decrease in the noise value for higher frequencies.

Once the main characteristics of the buffer fulfil the desired specifications, it's time to observe the behaviour at the output of the buffer. This way it's perceivable a very fast response of the buffer for the output transient voltage (Figure 4.41). Taking into account the perturbations caused by the DAC and comparing this results with the previous architectures, it's observable that this buffer reaches the 1.2 $V$ quicker than the other architectures.
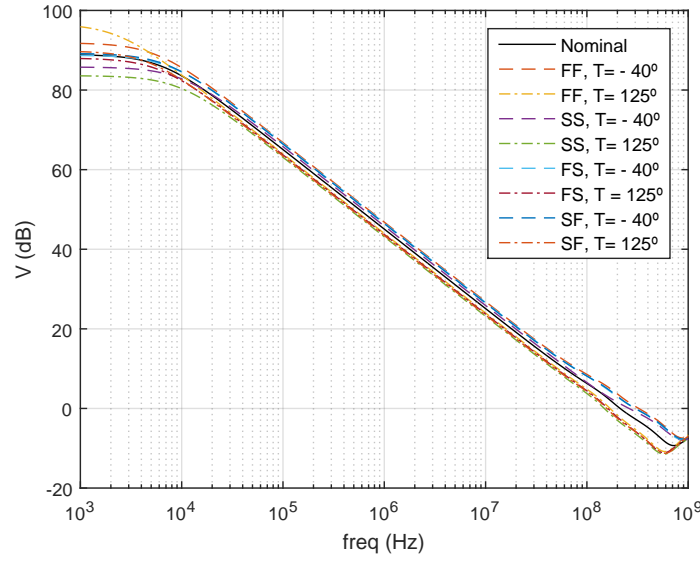
73

Figure 4.38: Positive power supply rejection ratio of the BFVF, using the Miller compensated amplifier.



(a) Without zoom.



(b) With zoom.
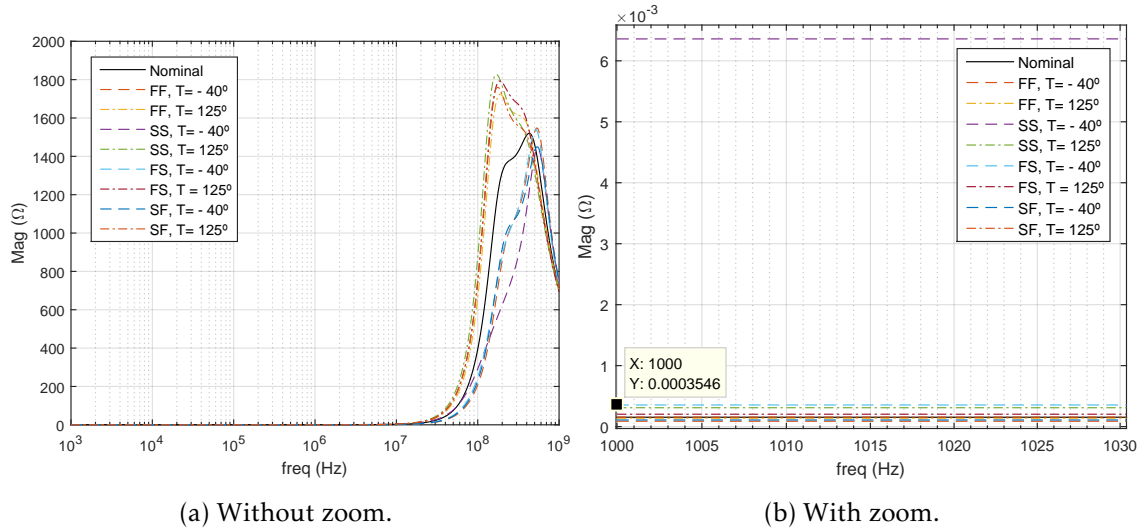
Figure 4.39: Output Impedance of the BFVF, using the Miller compensated amplifier.

As the output transient current is also perturbed by the DAC, and it's behaviour "follows" the output transient voltage it's also observable a faster response of the buffer in this parameter (Figure 4.42).

By obtaining the output transient voltage noise from the output transient current, it's observable that the final value for this parameter is 0.4 $mV$, which is smaller than the values obtained in the previous architectures, and it's due to the faster response of this circuit. Figure 4.43 shows the charge at the output.

(a) Equivalent input noise.

(b) Squared input noise.
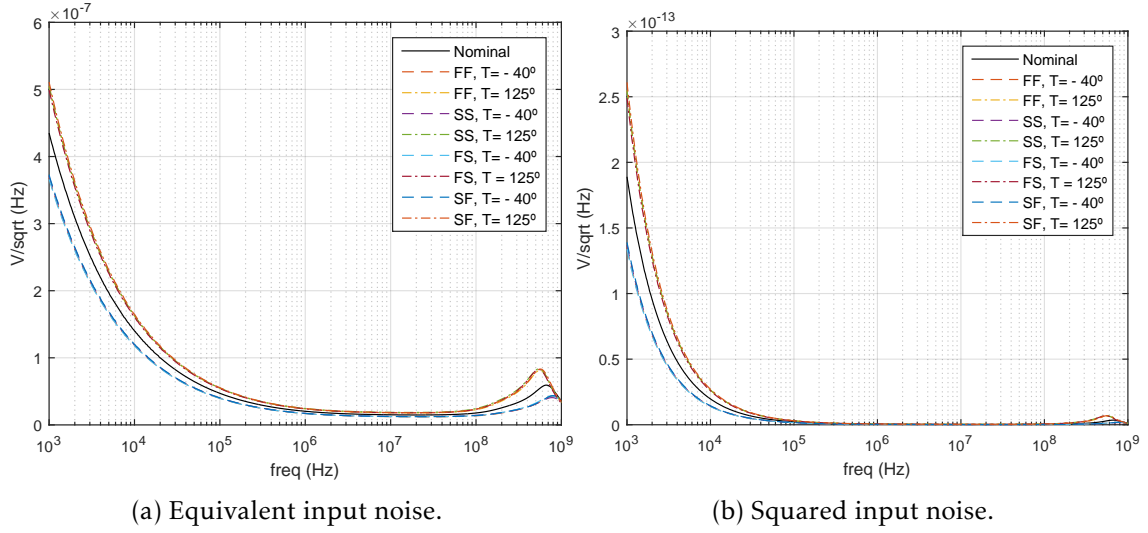
Figure 4.40: Input referred noise of the BFVF, using the Miller compensated amplifier.



(a) Without zoom.

(b) With zoom.
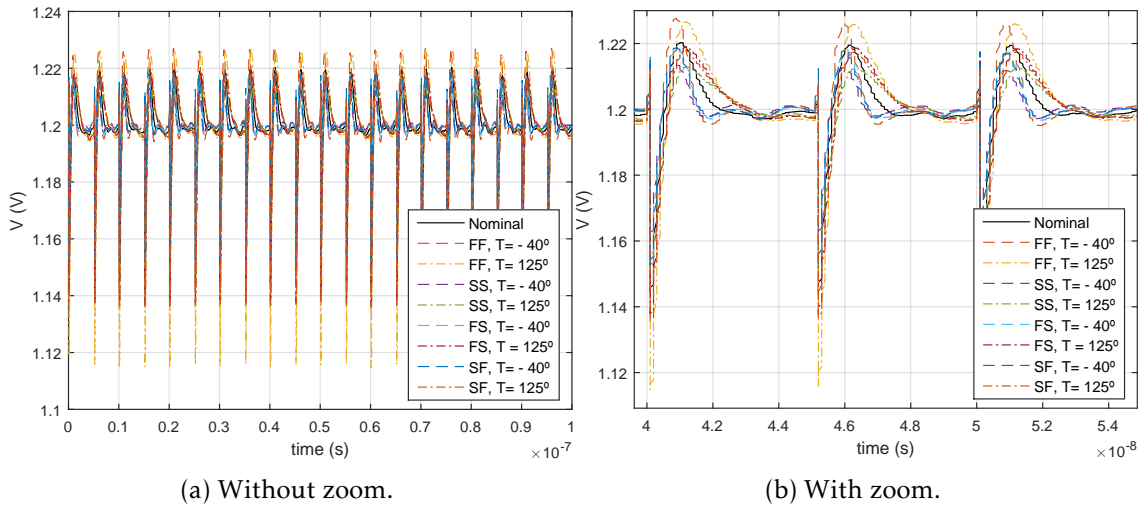
Figure 4.41: Output transient voltage of the BFVF, using the Miller compensated amplifier.

75
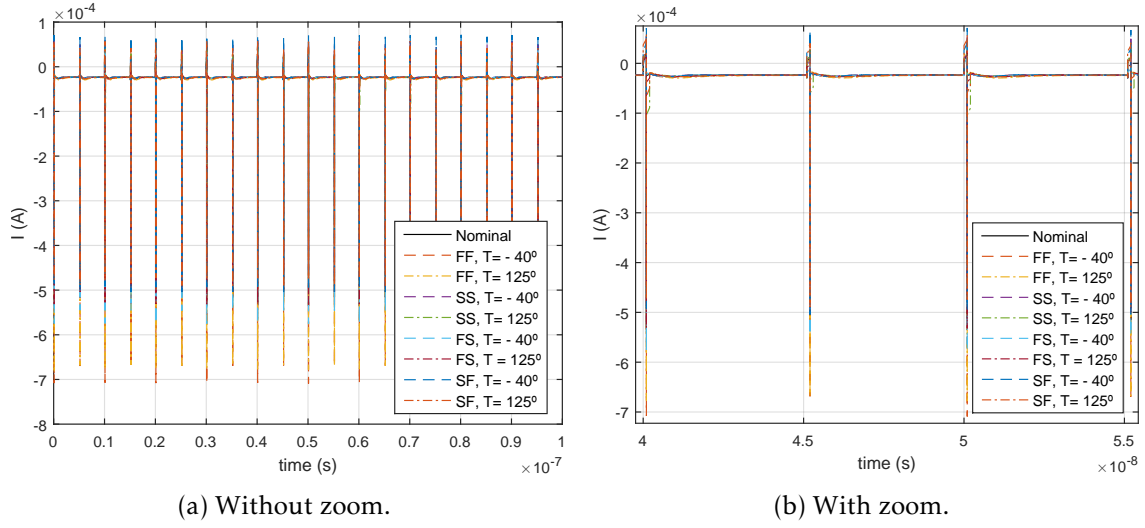
(a) Without zoom.

(b) With zoom.

Figure 4.42: Output transient current of the BFVF, using the Miller compensated amplifier.
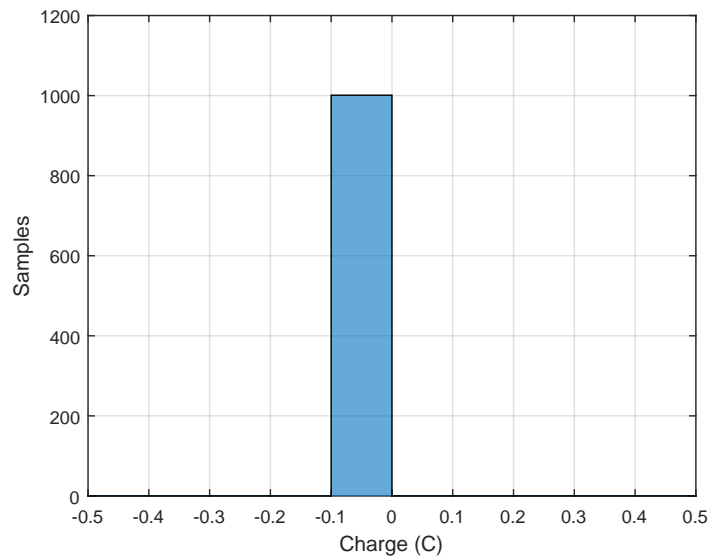


Figure 4.43: Charge at the output of the BFVF, using the Miller compensated amplifier.

### 4.4.2 Current Mirror OTA

As done in the previous buffers, this one is also tested with two error amplifiers in order to better understand its influence in the system and see if it's the buffer that has bad/good characteristics, or if it's the error amplifier.
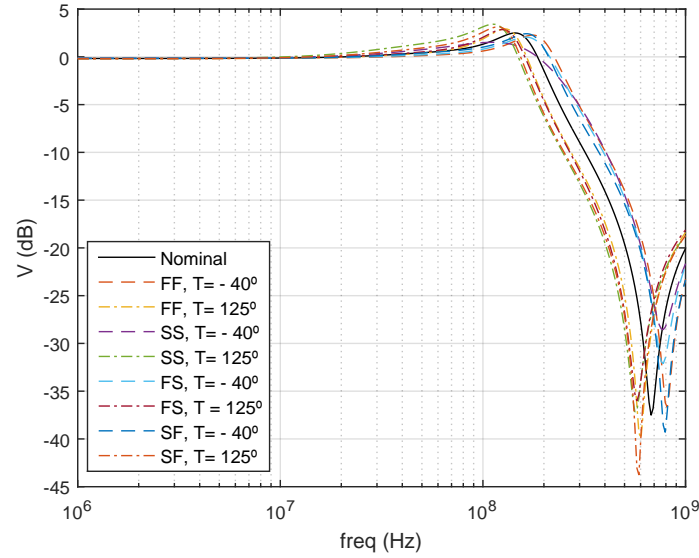


Figure 4.44: Gain of the BFVF, using the Current Mirror OTA.

For the gain (Figure 4.44), with this error amplifier, are observed, once again, perturbations at higher frequencies. But, as in the SsLDO, it doesn't affect the behaviour of the buffer.
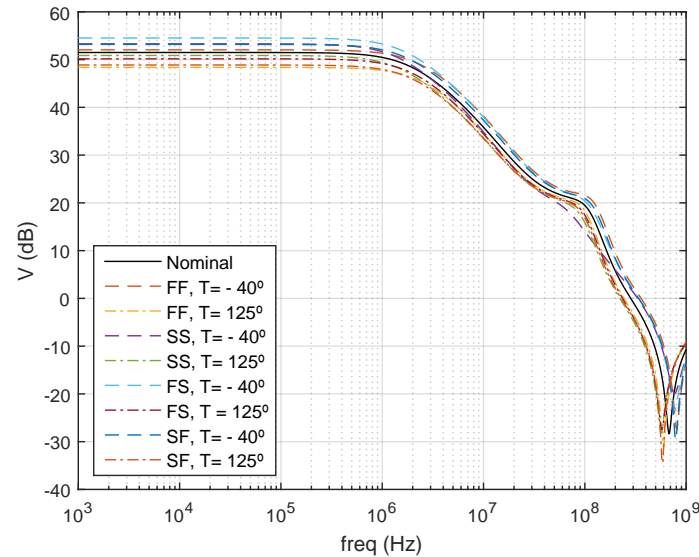


Figure 4.45: Positive power supply rejection ratio of the BFVF, using the Current Mirror OTA.

This way, the positive PSRR (Figure 4.45) suffers a decrease in its value when compared to

the previous error amplifier. At the same time the, the GBW and bandwidth frequencies increase, as happened when the SsLDO was tested with this error amplifier.



(a) Without zoom.



(b) With zoom.
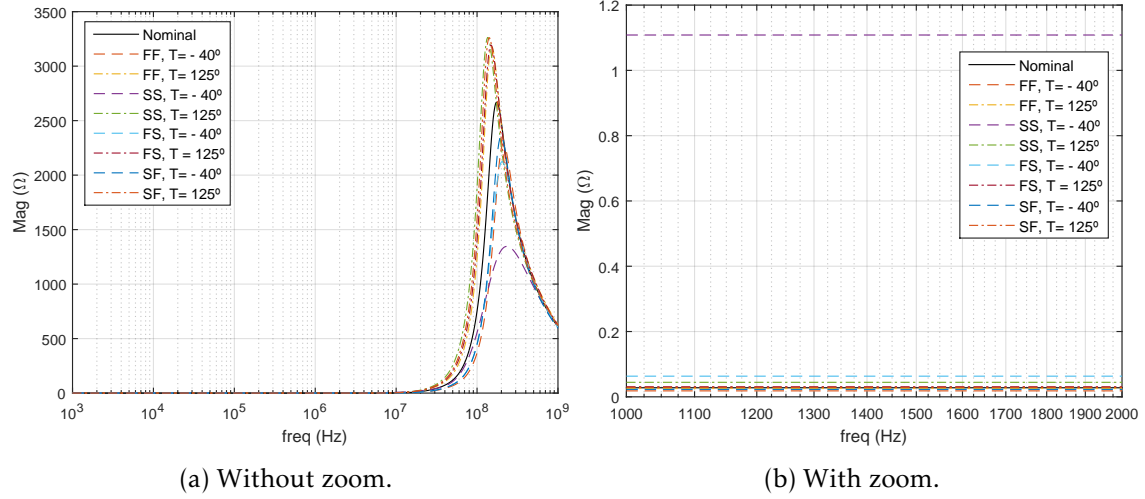
Figure 4.46: Output Impedance of the BFVF, using the Current Mirror OTA.

Similarly, the output impedance (Figure 4.46) also has suffered an increase along the frequency, as in the previous buffers. But for lower frequencies its value doesn't overtake 1.2 $\Omega$.



(a) Equivalent input noise.



(b) Squared input noise.
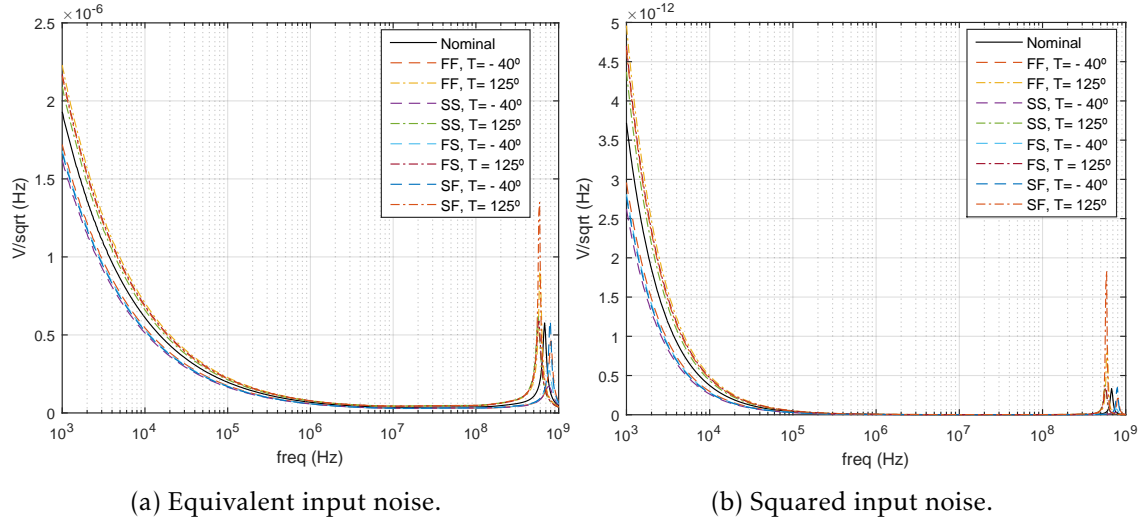
Figure 4.47: Input referred noise of the BFVF, using the Current Mirror OTA.

As expected the levels of noise have increased (Figure 4.47), but as in the previous cases, that rise doesn't affect the desired specification for the noise.

Regarding the output transient voltage (Figure 4.48), it's observable a decrease in the time to recover from the perturbations caused by the DAC, but nevertheless, the circuit is still capable of responding fast enough to keep the reference voltage close to the desired value.

(a) Without zoom.

(b) With zoom.
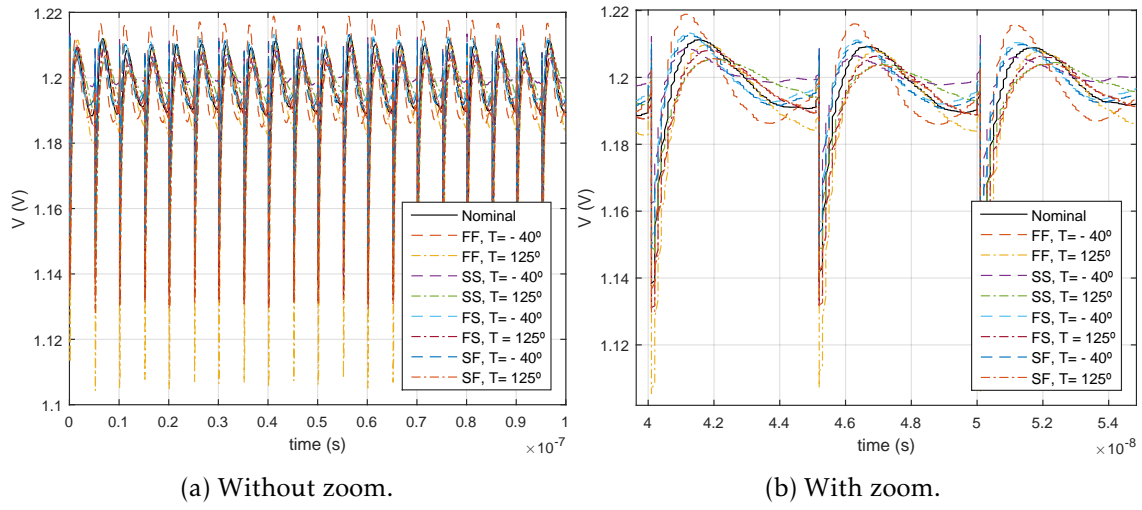
Figure 4.48: Output transient voltage of the BFVF, using the Current Mirror OTA.



(a) Without zoom.

(b) With zoom.
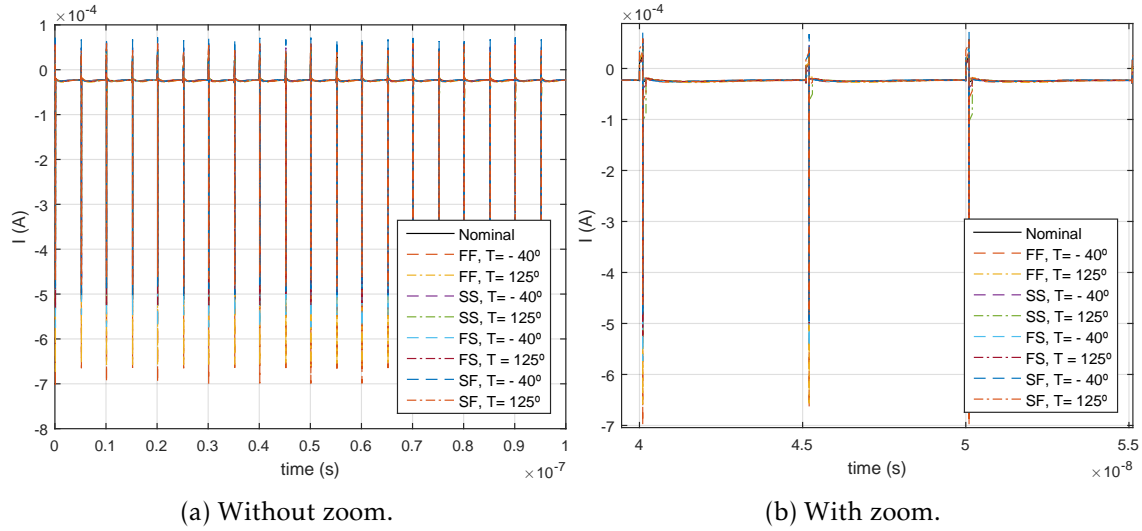
Figure 4.49: Output transient current of the BFVF, using the Current Mirror OTA.

Like in the previous cases, the change in the error amplifier doesn't affect the output transient current (Figure 4.49), so it stays with a similar behaviour comparing to the previous error amplifier.

For the output transient voltage noise it's, once again, obtained a small output transient voltage noise, with a measured value of $0.7\ mV$. Figure 4.50 shows the charge at the output.
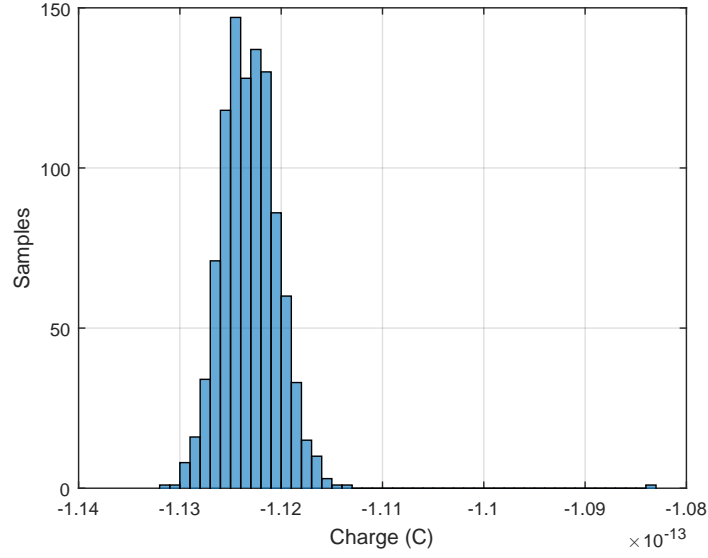
Figure 4.50: Charge at the output of the BFVF, using the Current Mirror OTA.

## 4.5   Comparison between the different topologies

Considering the study done in the previous sections, now it will be done a comparison between each architecture in order to observe the advantages and disadvantages of each architecture. It was selected the nominal case (circuit temperature of 27 ºC and regular speed for both N and P channels) of each architecture to do this comparison.

Taking this into account, it's possible to see that all the architectures have a very similar gain (Figure 4.51) and that the use of the current mirror OTA as error amplifier introduces some perturbations close to 100 $MHz$.
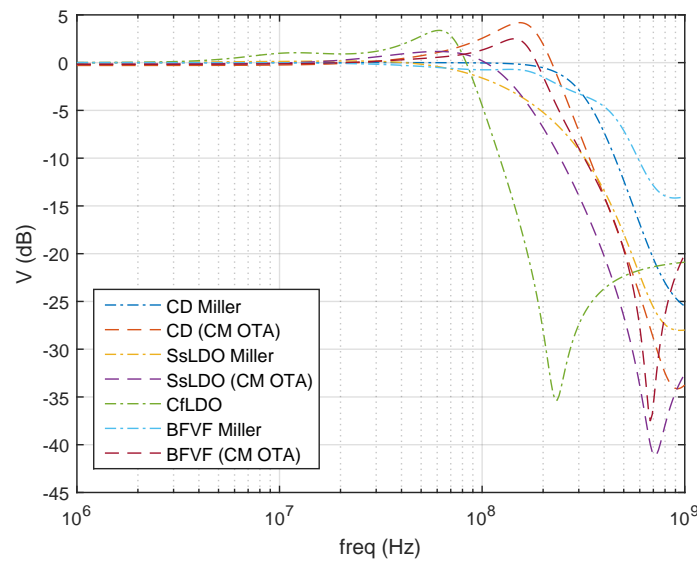


Figure 4.51: Gain comparison.

Regarding the positive PSRR (Figure 4.52), it's possible to see that the BFVF and SsLDO

architectures present very similar results when it's used the same error amplifier. Besides that, it's observable a higher PSRR when it's used the miller compensated amplifier and a larger bandwidth when it's used the current mirror OTA. As a middle term is present the CfLDO architecture, which allows to obtain a positive PSRR greater than 80 $dB$ and, at the same time, a considerable bandwidth.
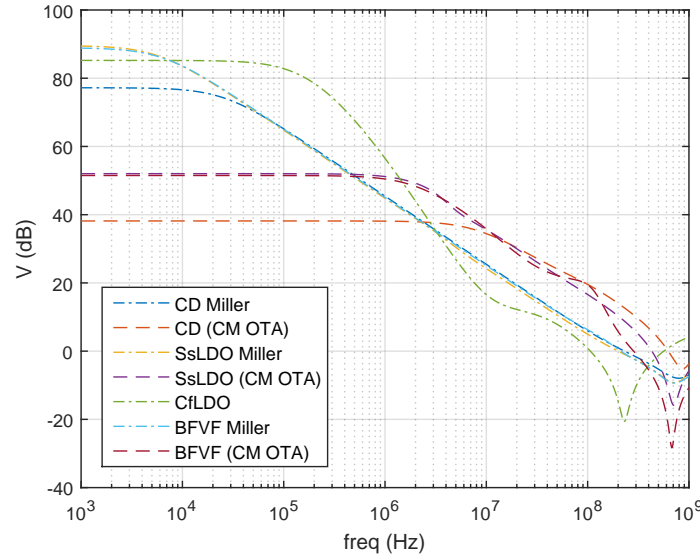


Figure 4.52: Positive power supply rejection ratio comparison.

For the output impedance (Figure 4.53) its observable that all the circuits have a perturbation close to 100 $MHz$, and that with the miller compensated amplifier it's possible to achieve a lower output impedance than with the current mirror OTA for lower frequencies.



(a) Without zoom.

(b) With zoom.
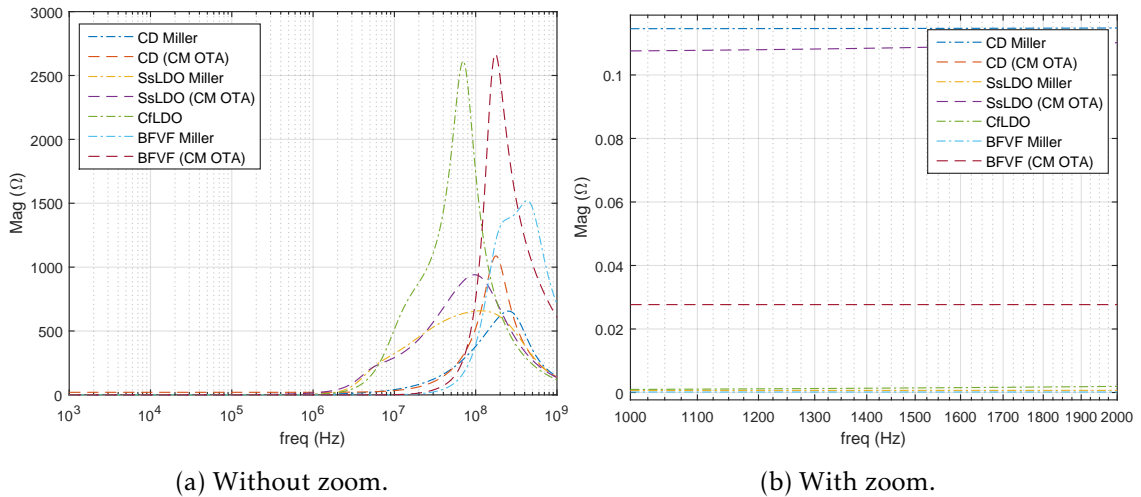
Figure 4.53: Output Impedance comparison.

In the input referred noise (Figure 4.54) it's observable that the error amplifier has a great impact in this parameter, so there are only observed differences between the architectures

81

with the same error amplifier in some points along the frequency. Besides that, it's possible to see that the current mirror OTA produces more noise than the miller compensated amplifier.



(a) Equivalent input noise.

(b) Squared input noise.
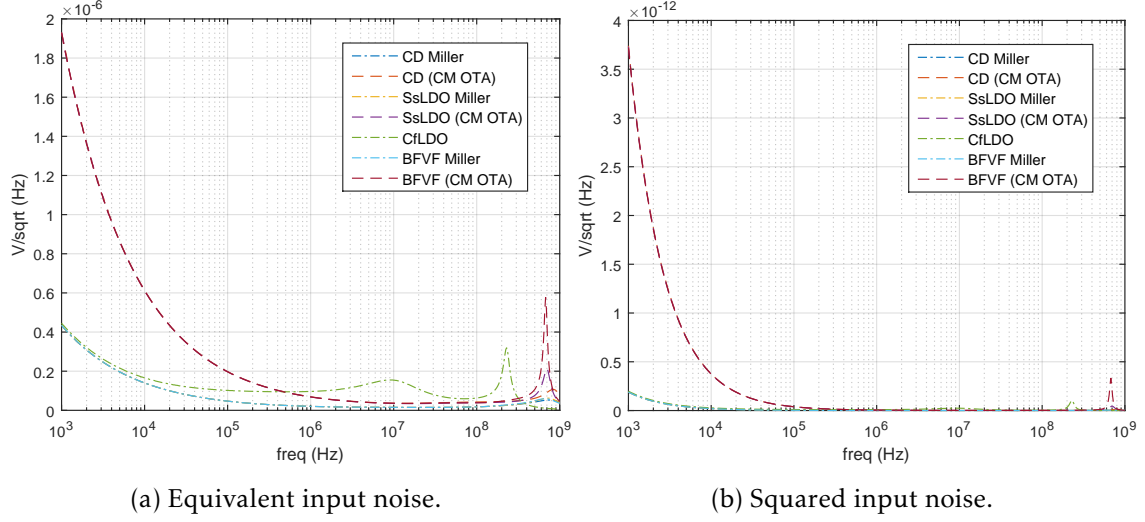
Figure 4.54: Input referred noise comparison.

Regarding the output transient voltage (Figure 4.55), it's observable that a faster recover from the perturbations caused by the DAC means a longer time until the circuit stabilizes at the reference voltage. Taking into account the results obtained, it's also noticeable that, when the CD and BFVF use the current mirror OTA as error amplifier, the reference voltage obtained is more distant from the desired one.



(a) Without zoom.

(b) With zoom.
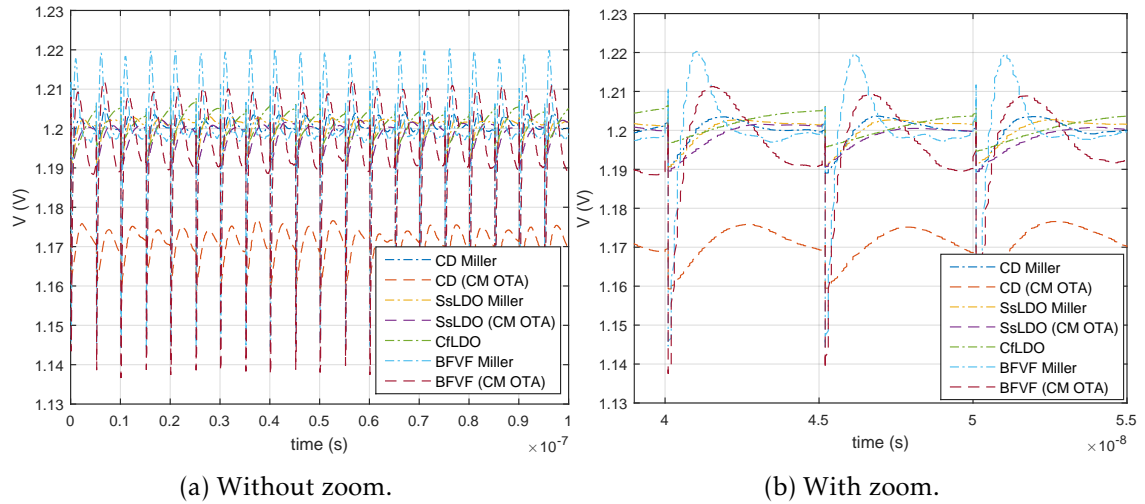
Figure 4.55: Output transient voltage comparison.

For the output transient current (Figure 4.56) it's observed a similar behaviour for all the architectures, and the only thing that changes is the current achieved by the circuit when it is perturbated by the DAC.

As the output transient voltage noise was obtained through histograms, it's not done a

(a) Without zoom.

(b) With zoom.
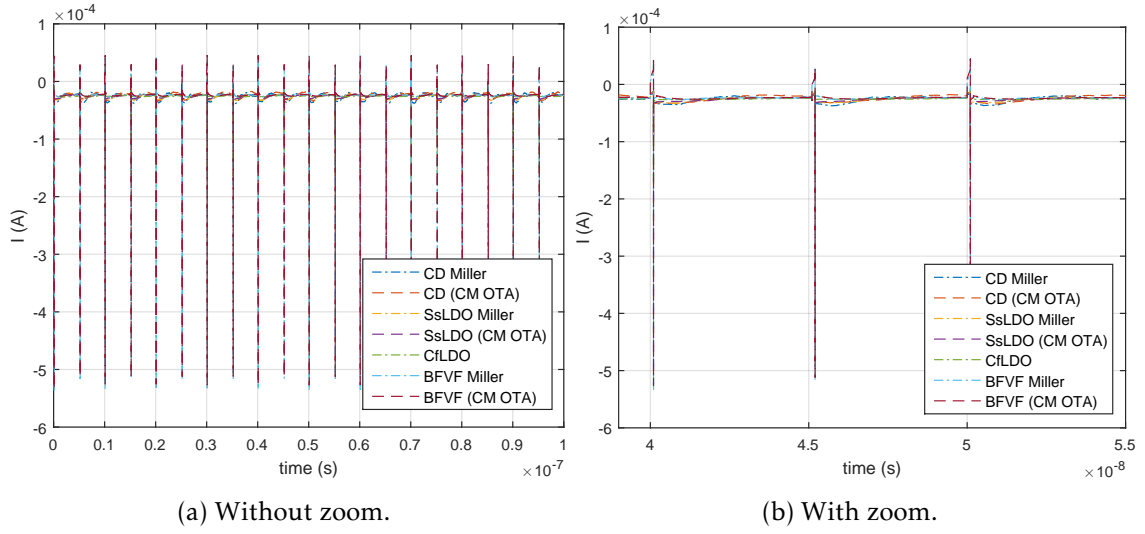
Figure 4.56: Output transient current comparison.

comparison between them in just one figure due to the lack of readability, but the final value obtained is compared in Table 4.1.

Regarding the results displayed, the Table 4.1 is used to better identify the advantages and disadvantages of each architecture, through comparison of the results obtained in the previous sections.

Table 4.1: Comparison of the different topologies.

| Characteristics | Circuit | | | | | | |
|---|---|---|---|---|---|---|---|
| | CD Miller | CD (CM OTA) | SsLDO Miller | SsLDO (CM OTA) | CfLDO | BFVF Miller | BFVF (CM OTA) |
| Gain ($mdB$) | -0.13 | -296.8 | 1.96 | -181.5 | 8.95 | 0.62 | -168.3 |
| Bandwidth ($MHz$) | 138 | 224 | 40 | 100 | 83 | 162 | 186 |
| PSRR$^+$ ($dB$) | 77.2 | 38.16 | 89.44 | 52.02 | 85.22 | 88.82 | 51.48 |
| GBW (PSRR$^+$) ($MHz$) | 234 | 631 | 200 | 437 | 107 | 200 | 282 |
| DC Output Impedance ($\Omega$) | 114.6 $m$ | 20.15 | 658.4 $u$ | 107.6 $m$ | 965.1 $u$ | 153.4 $u$ | 27.68 $m$ |
| $V_{Nin^2}$ ($fV/sqrt(Hz)$) at 10 $MHz$ | 0.23 | 1.35 | 0.24 | 1.25 | 23.8 | 0.23 | 1.3 |
| Overshoot ($V$) | 1.204 | – | 1.203 | 1.201 | 1.204 | 1.22 | 1.209 |
| Rise Time ($ns$) | 0.9 | – | 1.2 | 2 | 2 | 0.4 | 0.5 |
| Settling Time ($ns$) | 3.8 | – | 2.7 | 3.2 | 4.4 | 2.2 | 3.8 |
| Peak Current ($\mu A$) | -91.3 | -88 | -99.5 | -100.4 | -163.5 | -515 | -512 |
| $\eta$ (%) | 7.85 | 7.40 | 6.74 | 6.79 | 10.28 | 6.32 | 6.4 |
| Output transient voltage noise ($mV$) | 2 | – | 1.8 | 2.5 | 2.7 | 0.4 | 0.7 |
| Power Consumption ($\mu W$) | 555 | 455 | 692.5 | 592.5 | 185 | 725 | 625 |

CHAPTER 5

# Conclusions and Future Work

## 5.1 Conclusions

The objective of the work developed in this project was to design a reference buffer for a delta-sigma ADC. To do so, several topologies already implemented were studied, in order to gather enough information for comparison. After such intense research the three theoretically best architectures were chosen, with the intent of implement and simulate them.

Taking into account the results of the first simulations, it was obvious the need of using an error amplifier in the feedback of the buffer, in order to set the output voltage of the buffer equal to the reference voltage. Thus the error amplifier has a great influence in the behaviour of the whole system, because it influences several specifications, such as the positive PSRR, the output transient response (voltage and current), the input referred noise, the bandwidth and the output impedance. Therefore, as the error amplifiers were implemented with approximately the same GBW, it was verified that an error amplifier with a higher gain can improve the gain of the buffer, the positive PSRR, the output impedance, the input referred noise, the response speed to the perturbations caused by the DAC and the output transient voltage noise. On the other hand, an error amplifier with a lower gain can improve the bandwidth of the buffer and the GBW of the positive PSRR. So there are more advantages in using an error amplifier with a higher gain.

Considering the results obtained in previous chapters it's noticeable that each architecture has different pros and cons. Thus taking into account the architecture and the error amplifier used, it was created Table 5.1 that allows to observe which is the best architecture for each characteristic.

85

Table 5.1: Best and worse architectures in each characteristic.

| Characteristics | Best | Worse |
|---|---|---|
| Gain ($mdB$) | BFVF Miller | CD (CM OTA) |
| Bandwidth ($MHz$) | BFVF (CM OTA) | SsLDO Miller |
| PSRR$^+$ ($dB$) | SsLDO Miller | CD (CM OTA) |
| GBW (PSRR$^+$) ($MHz$) | CD (CM OTA) | CfLDO |
| DC Output Impedance ($\Omega$) | BFVF Miller | CD (CM OTA) |
| $V_{Nin^2}$ ($fV/sqrt(Hz)$) at 10 $MHz$ | CD Miller / BFVF Miller | CfLDO |
| Overshoot ($V$) | SsLDO (CM OTA) | BFVF Miller |
| Rise Time ($ns$) | BFVF Miller | SsLDO (CM OTA) / CfLDO |
| Settling Time ($ns$) | BFVF Miller | CfLDO |
| Peak Current ($\mu A$) | CD (CM OTA) | BFVF Miller |
| $\eta$ (%) | CD Miller | BFVF Miller |
| Output transient voltage noise ($mV$) | BFVF Miller | CfLDO |
| Power Consumption ($\mu W$) | CfLDO | BFVF Miller |

## 5.2 Future Work

Regarding the study done in this thesis, it's clear that not all the desired specifications were fulfilled. So, as a possible future work, it would be necessary to do an improvement in the implementation done in this project. In other words, it is necessary to find a way to improve $\eta$ and bandwidth of the system.

Besides that, it can also be made a root design of a new architecture, as a way to overcome the disadvantages of the previous architectures. On the other hand, in order to compare the area used by the architectures studied, it would be necessary to do a layout of them. Finally, to obtain more reliable results, it would be necessary to do the implementation and simulations with the Bandgap and Delta-Sigma ADC circuits.

# Bibliography

[1]  G. P. Banker, A. P. Naik, and N. Devashrayee. "Comparative Analysis of Low Power CMOS Class-A Voltage Followers with Current Mirror as a Load." In: *International Journal of Electronics and Communication Technology (IJECT)* 2.2 (2011).

[2]  R. G. Carvajal, J. Ramírez-Angulo, A. J. López-Martín, A. Torralba, J. A. G. Galán, A. Carlosena, and F. M. Chavero. "The flipped voltage follower: A useful cell for low-voltage low-power circuit design." In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 52.7 (2005), pp. 1276–1291.

[3]  S. Gupta, R. Mehra, and S. Sharma. "Design and Analysis of Flipped Voltage Follower for Different Aspect Ratio." In: *International Journal of Computer Applications* 143.13 (2016).

[4]  J Ramirez-Angulo and M Holmes. "Simple technique using local CMFB to enhance slew rate and bandwidth of one-stage CMOS op-amps." In: *Electronics Letters* 38.23 (2002), pp. 1409–1411.

[5]  S. Rajput and S. S. Jamuar. "Low voltage analog circuit design techniques." In: *IEEE Circuits and Systems Magazine* 2.1 (2002), pp. 24–42.

[6]  J. Molinar-Solis, M. Gurrola-Navarro, I Padilla, J. Ocampo, and C Muñiz. "Free class-AB flipped voltage follower using bulk-driven technique." In: *Electronics Letters* 51.18 (2015), pp. 1411–1413.

[7]  C. Jindal and R. Pandey. "Class-AB level shifted flipped voltage follower cell using bulk-driven technique." In: *IET Circuits, Devices & Systems* 12.3 (2017), pp. 286–294.

[8]  I. L. Abdel-Hafez, Y. A. Khalaf, and F. A. Farag. "CMOS buffer amplifier for wide bandwidth applications." In: *Design & Technology of Integrated Systems in Nanoscale Era, 2007. DTIS. International Conference on.* IEEE. 2007, pp. 56–59.

[9]  M. Koutani, Y. Fujimoto, and M. Miyamoto. "A highly linear CMOS buffer circuit with an adjustable output impedance." In: *Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003.* IEEE. 2003, pp. 685–688.

[10]  A. J. Lopez-Martin, J. M. Algueta, L. Acosta, R. G. Carvajal, and J. Ramirez-Angulo. "200 $\mu$W CMOS class AB unity-gain buffers with accurate quiescent current control." In: *ESSCIRC, 2010 Proceedings of the.* IEEE. 2010, pp. 322–325.

[11]   Y. Yosef-Hay, D. Ø. Larsen, P. L. Muntal, and I. H. Jørgensen. "Fully integrated, low drop-out linear voltage regulator in 180 nm CMOS." In: *Analog Integrated Circuits and Signal Processing* 92.3 (2017), pp. 427–436.

[12]   L. Breems, M. Bolatkale, H. Brekelmans, S. Bajoria, J. Niehof, R. Rutten, B. Oude-Essink, F. Fritschij, J. Singh, and G. Lassche. "A 2.2 GHz Continuous-Time $\Delta\Sigma$ ADC With -102 dBc THD and 25 MHz Bandwidth." In: *IEEE Journal of Solid-State Circuits* 51.12 (2016), pp. 2906–2916.

[13]   H. Chen and K. N. Leung. "A fast-transient LDO based on buffered flipped voltage follower." In: *Electron Devices and Solid-State Circuits (EDSSC), 2010 IEEE International Conference of.* IEEE. 2010, pp. 1–4.

[14]   S. Chong and P. Chan. "A Flipped Voltage Follower based low-dropout regulator with composite power transistor." In: *Integrated Circuits (ISIC), 2011 13th International Symposium on.* IEEE. 2011, pp. 472–475.

[15]   S. L. Pinjare, G Nithya, A Sthuthi, and V. S. Nagaraja. "A Gm/Id Based Methodology for Designing Common Source Amplifier." In: *2018 2nd International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE).* IEEE. 2018, pp. 304–307.

[16]   A. Ayed, H. Ghariani, and M. Samet. "Design and optimization of CMOS OTA with gm/Id methodology using EKV model for RF frequency synthesizer application." In: *2005 12th IEEE International Conference on Electronics, Circuits and Systems.* IEEE. 2005, pp. 1–5.

[17]   M. Ho and K. N. Leung. "Two-stage Miller-compensated amplifier with embedded negative current buffer." In: *2008 IEEE International Conference on Electron Devices and Solid-State Circuits.* IEEE. 2008, pp. 1–4.

[18]   E. D. Manolov. "Design of cascode current mirror OTA in ultra-deep submicron CMOS technology." In: *2017 XXVI International Scientific Conference Electronics (ET).* IEEE. 2017, pp. 1–4.