UNIVERSIDADE NOVA DE LISBOA

Faculdade de Ciências e Tecnologia

Departamento de Engenharia Electrotécnica e de Computadores

SI SC MDAC Switched Current-Capacitor Multiplying Digital-to-Analog Converter

Por

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Abstract

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Mestre em Engenharia Electrotécnica e de Computadores

by João Rafael Caetano Pacheco

This thesis presents a 1.5-bit MDAC circuit to be used in pipeline ADCs which employs a switched-current source to perform the reference shifting of the MDAC (the 1.5-bit digital-to-analog function). In the proposed circuit, the two single-ended reference voltage sources that are traditionally used (V_{Ref}^{+} and V_{Ref}^{-}), are replaced by a switched-current source. To evaluate and compare the performance of the proposed circuit, two 10-bit ADCs operating at 40 and 100MS/s, one using the traditional switched-capacitor (SC) MDAC and the other using the proposed MDAC, are designed.

At 40MS/s the simulation results show that the performance of the ADC with the proposed MDAC is enhanced since the power needed for the current sources is smaller than the power supplied by the reference voltage sources. Moreover, the proposed circuit does not require any reference voltage buffer, which can be difficult to design with relatively low power dissipation.

With the removal of the required reference voltage buffer by means of the proposed circuit the effects of the bonding wire in the normal operation of the circuit at high-frequencies can be avoided. This can be seen in the simulations results of the two designed 10-bit 100MS/s pipeline ADC. They have similar performance, but with high-inductive bonding wires the proposed MDAC is not affected with this problem.

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Resumo

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Mestre em Engenharia Electrotécnica e de Computadores

por João Rafael Caetano Pacheco

Esta tese apresenta um circuito **MDAC** de 1,5-bit a ser usado num **ADC pipeline** que implementa, através da comutação de uma fonte de corrente, o **reference shifting** de um **MDAC** (a função digital-to-analog de 1,5-bit). No circuito proposto, as duas tensões de referência **single-ended** usadas tradicionalmente (V_{Ref}^{+} e V_{Ref}^{-}) são substituídas por uma fonte de corrente comutada. Para avaliar e comparar a performance do circuito proposto, foram desenvolvidos dois **ADCs** de 10-bit operando a 50 e 100**MS/s**, um usando o tradicional **switched-capacitor (SC) MDAC** e outro usando o **MDAC** proposto.

Os resultados das simulações a 40**MS/s** mostram que a performance do **ADC** com o **MDAC** proposto é melhorada, pois a potência necessária às fontes ou que passa pelas fontes pelas fontes de corrente é menor que a potência fornecida pelas fontes das tensões de referência. Mais ainda, o circuito proposto não necessita de qualquer tipo de **buffer** para as tensões de referência, que podem ser difíceis de desenvolver tendo em vista uma baixa potência de consumo.

Com a remoção dos **buffers** das tensões de referência, através do uso do circuito proposto nas condições de uma operação normal, os efeitos dos **bonding wires** a altas frequências podem ser evitados. Isto pode verificado através dos resultados das simulações dos dois **pipeline ADCs** de 10-bit a 100**MS/s**.

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Abbreviations

ADC	Analog-to-Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
ENOB	Effective Number Of Bits
FFT	Fast Fourier Transform
FQ	Flash Quantizer
LSB	Least Significant bit
MDAC	Multiplying Digital-to-Analog Converter
MSB	Most Significant bit
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
SC	Switched-Capacitor
SFDR	Spurious Free Dynamic Range
SNDR	Signal-to-Noise plus Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion

Dedicated to my family

1 – Introduction

1.1 – Motivation and Context

High-resolution analog-to-digital converters (ADCs) with sampling rates in the range of 40 to 160MS/s are required for broad number of applications, ranging from high-resolution and high-speed imaging to the modern digital communication. When designing these ADCs low-voltage, low-power, and low-area are of great importance. One field that reflects the modern digital communication advances are mobile terminals, since they are single battery systems, so low power dissipation is necessary to ensure a reasonable battery lifetime. Another important factor is silicon area since it is directly related with the cost of the integrated circuit.

When very high conversion rates are required, the ADCs usually employ pipelining to relax the speed requirements of the analog components. Such architectures use a cascade of stages

comprising a low resolution flash quantizer and a low resolution multiplying digital-to-analog converter (MDAC), which computes and amplifies the residue to be quantized by the following stages [1]. The flash quantizer typically comprises a bank of comparators and the MDAC uses an operational amplifier (opamp) with a capacitor feedback network to provide linear voltage amplification. The MDACs usually employ a switched capacitor (SC) network to obtain the necessary closed-loop gain to implement the conversion algorithm. The DC offsets in the opamps and comparators do not affect the overall linearity of a pipeline ADC, if redundancy and proper output encoding (digital correction) are adopted [2]. Hence, the accuracy is mainly limited by the gain-error (GE) and static linearity errors (LE) of the MDAC in the first stages, caused by capacitor mismatch errors in the DAC and by finite DC gain of the residue amplifier. The accuracy required for the first MDAC is that of the overall ADC and it is progressively relaxed in subsequent stages.

In current CMOS technologies, component (e.g. capacitor) mismatch accuracy is usually limited to 10-bit resolution. Without using factory trimming [3], self-configuring schemes [4] or self-calibration techniques, the overall resolution of pipeline ADCs is limited to this level. This accuracy is limited by the lithography and subsequent processing steps [5]. The best resolution per stage for pipeline ADCs using digital correction is 1.5 bits per stage [6], this means that the MDAC circuit has three .voltage levels. These levels can be obtained using only one differential reference voltage ΔV_{Ref} (which is generated from 2 single-ended reference voltages, $+V_{Ref}$ and $-V_{Ref}$). The current drawn from the reference voltage buffer is clearly signal dependent and therefore the reference voltage buffer circuits should not have memory of the influence of previous samples processed by the ADC. This can be very challenging to achieve in the case of high sampling frequencies because it requires either a very fast reference voltage buffer or bond wires with very low inductance. It is common, when computing the power dissipation of an ADC, to ignore the power dissipation of the reference voltage circuitry. However this power can be a significant fraction of the overall ADC power dissipation.

1.2 – Comparison between Pipeline Architecture and others architectures

In the planning phases of a system design using an ADC there is a need to choose the correct ADC architecture since this component is the key in digital communications receive channels. And for a better system design optimization the correct choice of ADC is crucial since there are tradeoffs between resolution, power consumption, size, conversion time, and so on.

There are six popular ADC architectures: Flash, Pipeline, Successive-approximation-register (SAR), Sigma-Delta, Two Step, Integrating.

The Flash ADC are the fastest of all the popular architecture, ranging from a few Megasamples per second (MS/s) up to 4GS/s+, with a range of resolutions from 6 to 16 bits. This architecture has the problem of exponential size increase with the resolution increase and consequent power dissipation problems. Because of this the designer only chooses this architecture for high frequency applications.

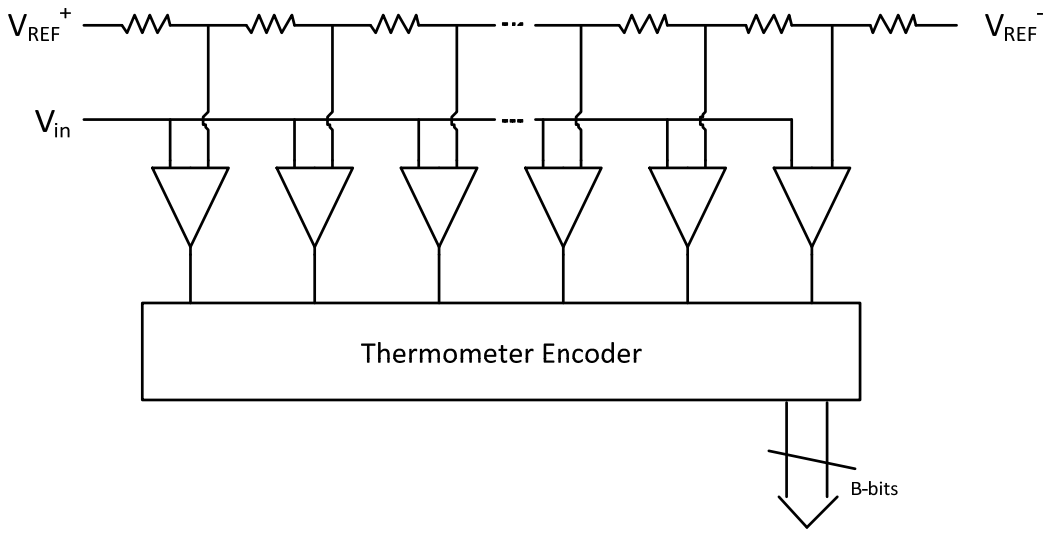


Figure 1.2.1 – Flash ADC Architecture

The Pipeline ADC is a more power efficient than the Flash in high-speed conversion of wide-band input signals (up to 100MHz channel) but cannot achieve the high sampling frequencies of the fastest Flash ADC. This architecture has a resolution ranging from 6 to 16 bits.

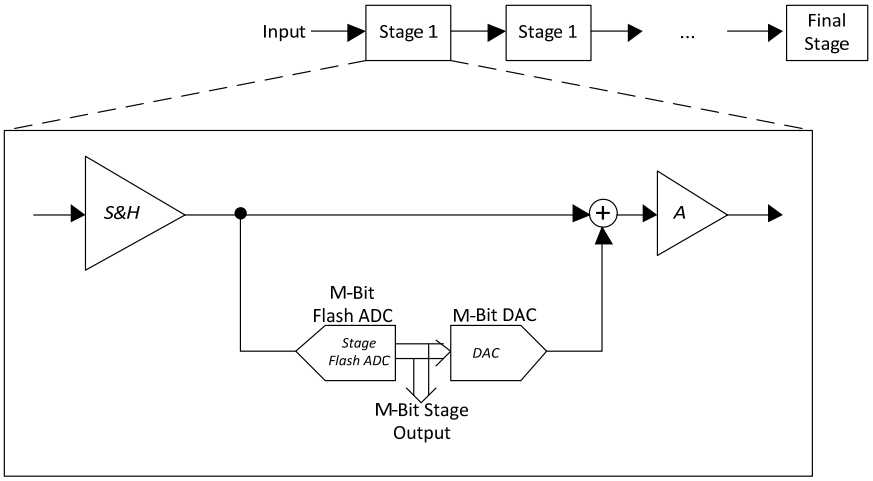


Figure 1.2.2 – Pipeline ADC Architecture

The SAR ADC is a popular architecture for medium-to-high resolution applications, with sampling rates lower than 10 MS/s and the resolution range goes from 8 to 18 bits. In this architecture the resolution is highly dependent of the sampling rate since there are a required number of successive comparisons to achieve a successful conversion. The hardware needed to implement this architecture is simple which leads to low power consumption as well to a small area size.

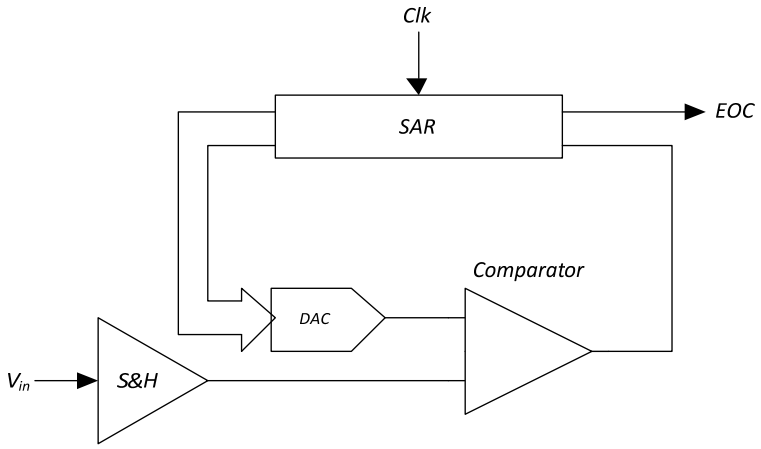


Figure 1.2.3 – SAR ADC Architecture

The Sigma-Delta architecture is commonly used in lower speed applications (low bandwidth input signals) because of requiring a tradeoff between conversion speed and resolution since the principal working concept behind this type of ADC is oversampling the signal. This type of architecture is dominant in audio designs since it can achieve a 24 bit resolution. The typical bandwidth for this type of architecture is 1MHz with a resolution from 12 to 32 bits.

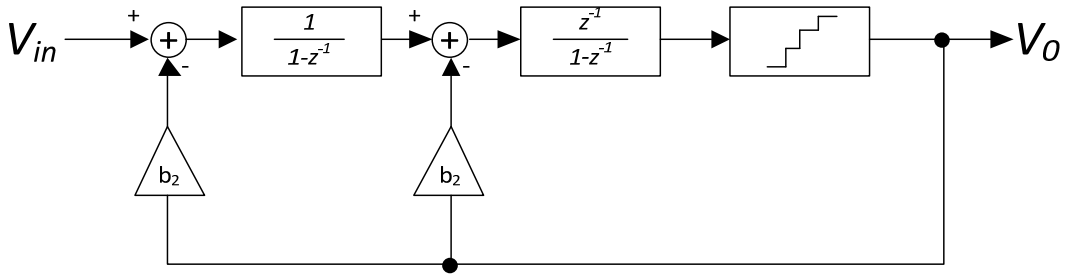


Figure 1.2.4 – Sigma-Delta ADC Architecture

The two step converters also know as sub ranging converter is a cross between the Flash ADC and the stages of a Pipeline ADC. This means that this hybrid architecture can achieve higher conversion rates than the Pipeline ADC and at the same time a smaller area size and power dissipation for a given resolution in comparison with a Flash ADC.

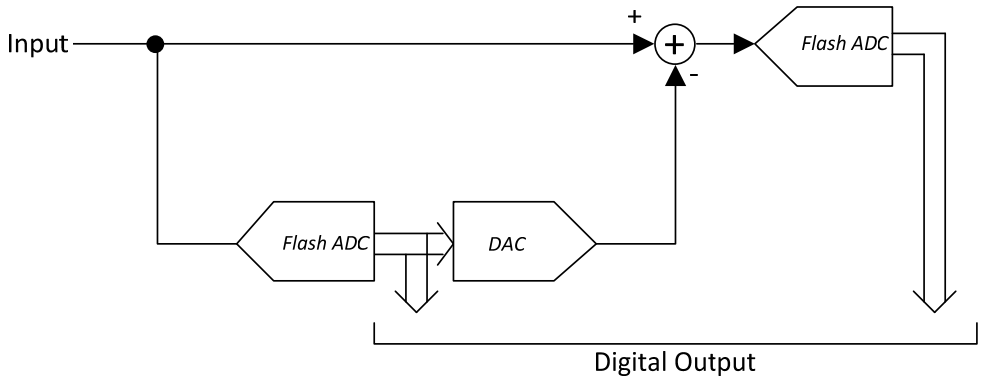


Figure 1.2.5 – Two Step ADC Architecture

The Integrating ADC converts any input voltage into its digital code through the use of an integrator. The converters of this type can achieve high resolutions (28 bits) but do so at the expense of speed.

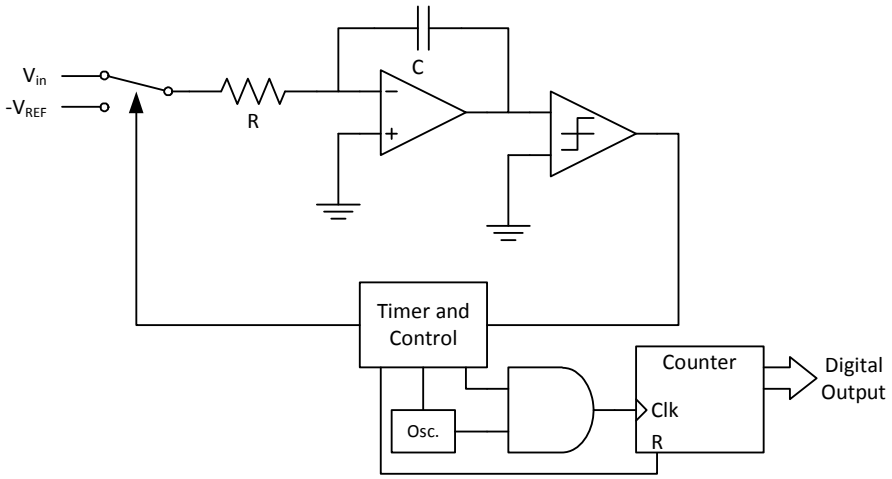


Figure 1.2.6 – Integrating ADC Architecture

For a proper comparison the characteristics of each one of the ADC architectures are placed on the Table 1.2.1.

Table 1.2.1 – Comparison of ADC architectures

Architecture	Output latency	Sampling frequencies	Resolution	Silicon area
Flash	No	High	Low	High
Two-Step	No	Medium-High	Low-Medium	Medium-High
Pipeline	Yes	Medium	Medium-High	Medium
SAR	Yes	Low	Medium-High	Low
Sigma-Delta	Yes	Low	High	Medium

More detailed information about alternative ADC architectures can be found in [10].

1.3 – Thesis Organization

This thesis is organized in seven chapters, most of which with a brief overview discussing the theme described in that chapter. The current chapter gives an introduction to the structure of this thesis, to the context of this work and the challenges for its completion. It is also in this chapter that there is a comparison between the pipeline architecture and others ADC architectures.

In the second chapter there is a brief review of the pipeline architecture and the traditional 1.5-bit MDAC. This chapter also provides some background in the error sources present in this architecture and the digital correction.

The third chapter discusses the implementation of a pipeline ADC using the traditional MDAC approach, some of which are related with sub-chapters from the second chapter. It is also discussed the techniques employed in each of the pipeline stages.

The fourth chapter gives a brief overview of the high-frequency problems in the pipeline ADC and provides detailed information about the proposed architecture and its implementation (the basic principle behind it; changes to the MDAC circuit and its elements; and new sources of error and problems introduced by the new approach).

The fifth chapter introduces the current controller needed to do a proper calibration of the proposed approach. This chapter provides some background over the structures employed in the current controller design.

The sixth chapter discusses the reference voltage generation circuitry, the model used for the electrical simulation, and the problems introduced at high-frequency by the bonding wires.

Finally, the seventh chapter is dedicated to some conclusions and indicate further research suggestions.

2 – Pipeline ADC

This chapter discusses the basic principles of the operation of a pipeline ADC, the building blocks of each pipeline stage, the sources of error presented in each stage of the pipeline ADC, the need to face these errors by means of digital correction.

The digital correction allows to design a 1,5-bit Flash ADC with a lower offset voltage requirement for use inside the pipeline ADC.

2.1 – Introduction

By definition pipelining is a way to increase the productivity of any task. The process of pipelining a task is done by dividing it into sub-tasks and distribute then by a defined number of stages. Every stage has the same completion time for any sub-task, and these stages are done in succession. When

a stage finishes processing a sub-task, it passes the processed output to the next stage, and this happens until the last stage when the task is finished.

But the increase of productivity when processing a task is only achieved when the pipeline is flooded with new tasks to be processed. This means when a stage passes it's processed output to next stage; it receives from the previous stage new input referent to a new task. And by means of this a single stage is never stopped.

One example of pipelining is the auto assembly line, this line doesn't decrease the time of a vehicle assembly, but increases the number of produced vehicles by means of dividing tasks by each manufacturing stage.

The best example of pipelining applied to electronics is the pipeline ADC, because each conversion is divided by a defined number of steps, never greater than the pipeline ADC resolution. The sub-structures responsible for the conversion step are designed stages.

Each stage process a number of bits of the final digital output, and this number is determined by the conversion step resolution. The first stage of the pipeline ADC is responsible for the most significant bits of the digital output, and by logic the last pipeline stage is responsible for the least significant bits.

Because every conversion steps isn't done in the same time, there will be latency in the conversion system. This means that the least significant bits will be converted in a posterior time to the most significant bits. This system latency is related to the number of pipeline stages and is forcibly imposed by the pipeline architecture, and to overcome the latency there it is needed to use buffers to store stages digital output results with the duration of the latency time.

In terms of pipelining applied to ADCs, the introduction of this technique doesn't decrease the time of producing a single conversion it even increases the latency between the start of conversion of the input signal and the end of conversion. But increases the throughput of the system

2.2 – Pipeline ADC Architecture

In an N-bit Pipeline ADC like the one represented by the figure 2.1, we have X stages with the final stage being a low resolution Flash ADC, where X is equal or lower than N because each stage can have an digital output higher than a bit. Also in each stage there are three essential structures: a Digital-to-Analog Converter (DAC), a voltage gain, and an Analog-to-Digital Converter (ADC).

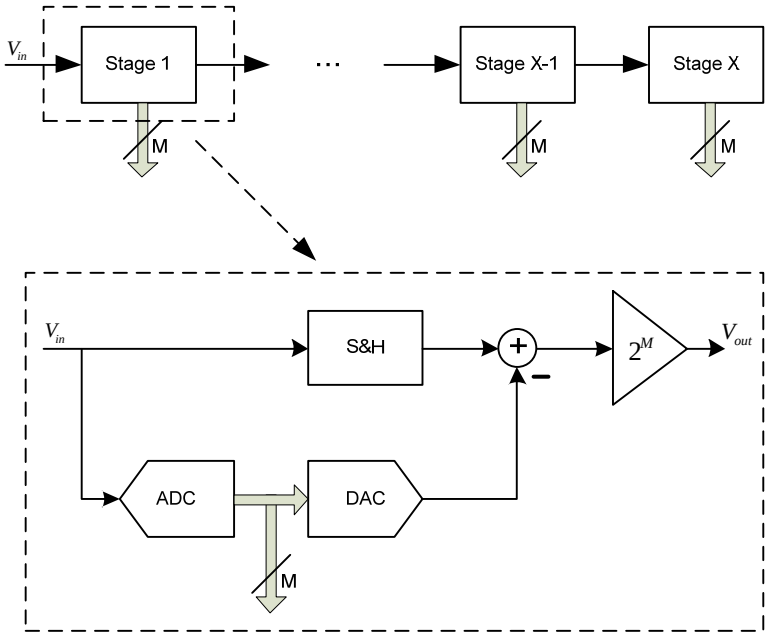


Figure 2.2.1 – Block diagram of the Pipeline ADC architecture

Each stage works in the following way: it starts by performing a low resolution quantization of the stage's input. Converts the result of the quantization to an analog value, and subtracts the analog value to the stage input. The resulting difference is them multiplied by two to the power of stage resolution minus one bit (because of the extra bit for digital correction).

The voltage gain of two to the power of stage resolution minus one is done by a switched capacitor circuit in conjunction with the operational amplifier in the Pipeline stage which results in a Sample-and-Hold Amplifier (SHA).

In a way to further simplify the pipeline stage architecture, the voltage gain and the DAC can be combined to form a structure know as a MDAC (Multiplying Digital to Analog Converter).

2.2.1 – MDAC

In this section it will be discussed a generic MDAC like the one represented in figure 2.2.1.1. The first MDAC structure was initially proposed in [1] and was a 1,5-bit MDAC.

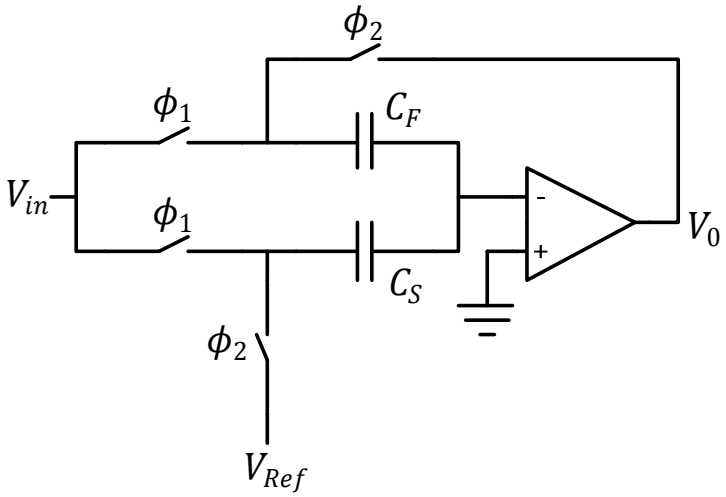
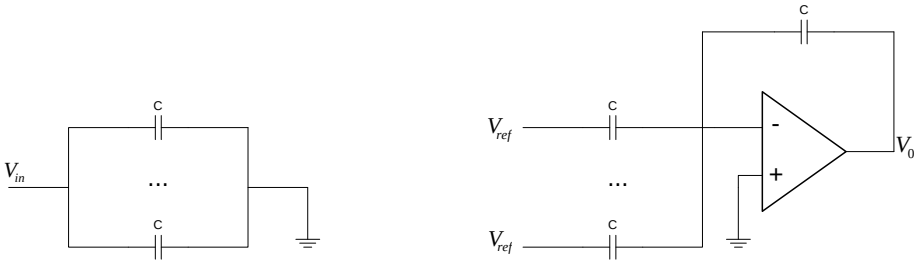


Figure 2.2.1.1 – Generic MDAC structure

The sampling process described in resume in introduction of section 2.2, doesn't tell us that the conversion operation is done in MDAC in two phases: sampling phase and the amplification phase.

There are two options to implement the amplification phase in regards to the reference voltage: based on an R-DAC and another based on a C-DAC.

In figure 2.2.1.2 is represented how the stage circuitry, with a C-DAC approach, adapts to each phase.



(a) Sampling Phase (b) Amplification Phase

Figure 2.2.1.2 – Switched Capacitor Circuit adaptation in a MDAC using C-DAC

In the C-DAC approach, the end of sampling phase determines the sampling of the input signal by a set of 2^B capacitors and the simultaneous quantization of the input with a resolution of B,5 bits by a low resolution Flash ADC.

The DAC function and the multiplication of the residue voltage occurs in the amplification phase. The DAC function is done by charging or discharging a set of capacitors with a reference voltage $\pm V_{Ref}$, this is responsible for the subtraction in the transfer function of the stage. The number of capacitors connected to the reference voltage is equal to $2^B - 1$, while the remaining capacitor connects the input of the OPAMP to its output. This last connection is responsible for the multiplying part of the transfer function.

The charge stored in the capacitors during the sampling phase is given by

$$Q_{sampling} = 2^B . C . V_{in} \tag{2.2.1.1}$$

And the charge in the amplification phase is equal to

$$Q_{amplification} = C . \left(V_0 - \frac{V_0}{A}\right) + (2^B - 1) . C . \left(V_{Ref} - \frac{V_0}{A}\right) \tag{2.2.1.2}$$

By charge conservation between the phases, the output of the stage in the amplification phase is

$$V_0 = 2^B . V_{in} - (2^B - 1) . V_{Ref} + E_{gain} \tag{2.2.1.3}$$

where the value of the error introduced by the OPAMP finite gain, designated by E_{gain}, and considering that there is not mismatch between the capacitors, is given by

$$E_{gain} = 2^B . \frac{V_0}{A} \tag{2.2.1.4}$$

Another important factor needed in future sections is the feedback factor in the amplifying phase, represented by the greek letter β, and its value is given by

$$\beta = \frac{C}{2^B . C + C_{input\ capacitance}} \tag{2.2.1.5}$$

where $C_{input\ capacitance}$ is the OPAMP parasitic input capacitance. In equation (2.2.1.5) capacitors C_s or C_f are not reference because it's admitted that there isn't a mismatch between the capacitors.

2.2.2 – Flash ADC

Each of the pipeline stages contains a Flash ADC with low resolution for producing the digital code output of the stage and to provide support for the implemented function performed by the MDAC. A typical Flash ADC architecture is defined in figure 2.2.2.1.

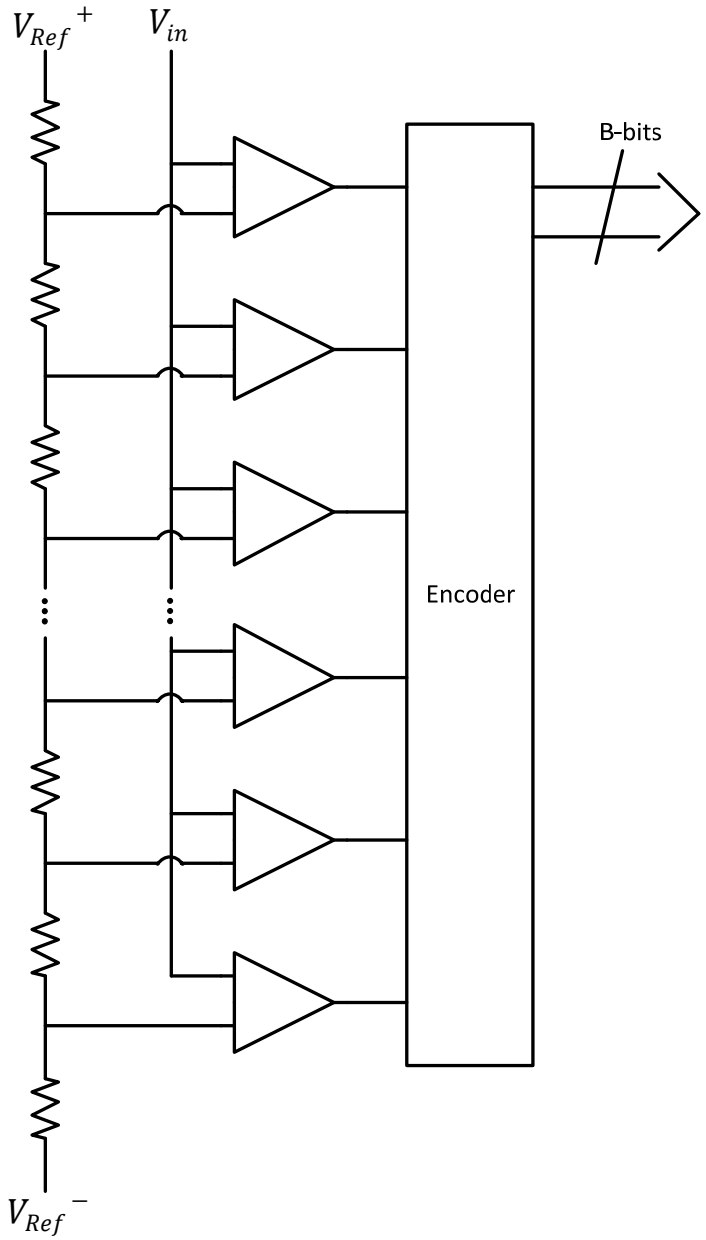


Figure 2.2.2.1 – Flash ADC Architecture

The reference voltages required for the flash can be generated using a resistive ladder or using capacitive division; each of the approaches has advantages and disadvantages, although the capacitive division approach is preferred because it has smaller DC power dissipation.

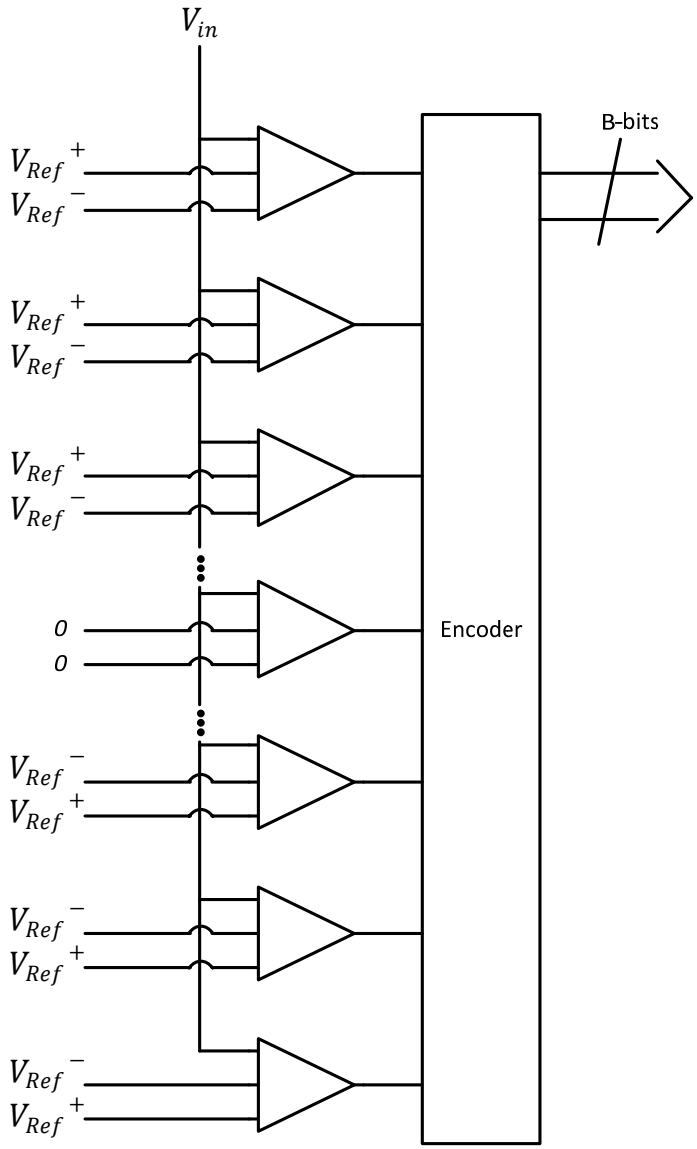


Figure 2.2.2.2 – Switched-capacitor based flash ADC Architecture

Offset error in the comparator of the Flash cause quantization errors in the Flash. These errors result in the wrong code being applied to the DAC of the MDAC circuit, ultimately resulting in the saturation of the analog output of the MDAC and therefore missing code in the ADC.

To reduce the influence of these error sources, digital correction is used, which increases (doubles in the 1,5-bit Flash ADC) the number of comparators in the default flash ADC, which means the pipeline stage flash ADC with digital correction have $2^{M+1} - 2$ comparators. At the same time the gain of the MDAC is divided by two.

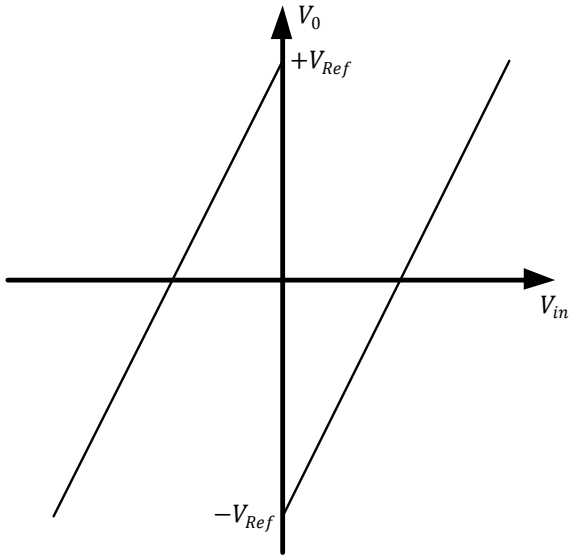


Figure 2.2.2.3 – Pipeline Stage Flash ADC Transfer Function without digital correction

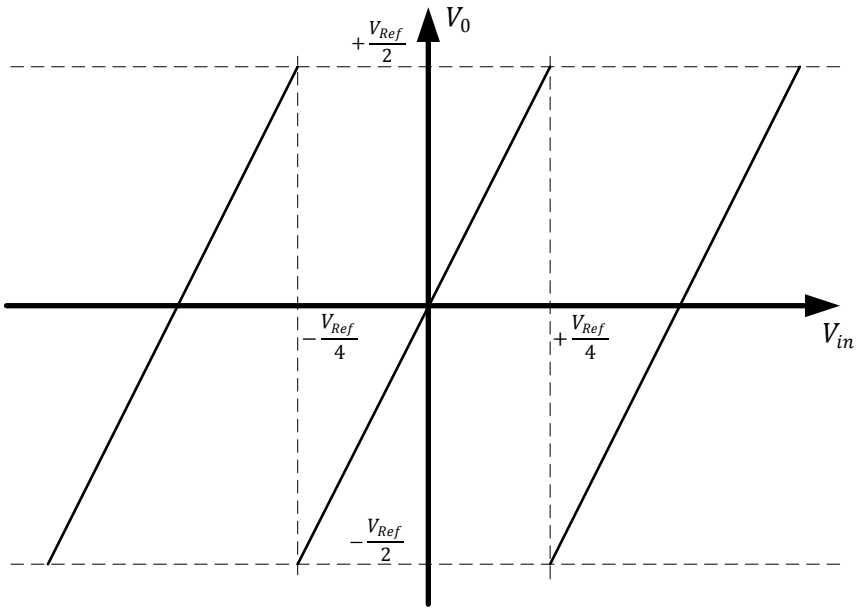


Figure 2.2.2.4 – Pipeline Stage Flash ADC Transfer Function with digital correction

It's important to refer that since the last stage is only a Flash ADC with a higher resolution that the ones used in the other stages, it doesn't need to have the extra comparator incorporated in it, because the major significant bit can be used has the redundant bit in the digital correction.

2.2.3 – Error sources in this Architecture

In this section some of the noises sources in the pipeline ADC architecture are discussed. These error sources are responsible for limitations in the correct operation of the pipeline ADC. In the next error analysis it's assumed that only one error source is affecting the circuit at a time. In order to simplify the analysis, it is assumed that only one error source is affecting the performance of the circuit at the same time.

2.2.3.1 – Thermal Noise

By the laws of physics, all particles at temperatures above absolute zero are in some kind of random motion. In the case of particles with electrical charge this random motion creates electrical noise and is generated by the thermal agitation of the charges carries (usually electrons) inside an electrical conductor.

For the thermal noise applied to a conducting medium, the RMS of the noise voltage is given by

$$v_n = \sqrt{4.k_B.T.R.B} \qquad (2.2.3.1.1)$$

where B is de finite bandwidth where the noise is calculated, T is the room temperature is absolute degrees, k_B is the Boltzmann constant and R is the medium resistance.

The thermal noise that applies in a capacitor is not caused by the capacitor, but by the sampling mechanism. Since a sampling switch is used in the process to sample the input signal to the sampling capacitance, at the same time the sampling is occurring, noise from the sampling switch is sampled onto the capacitor.

The RMS value of the thermal noise on capacitor is

$$v_n = \sqrt{\frac{k_B.T}{C}} \qquad (2.2.3.1.2)$$

where C is the value of the capacitor, k_B the Boltzmann constant and the T is the absolute value of the temperature.

One thing that can be concluded from observing the RMS value of the thermal noise on capacitor is that it doesn't depend of the frequency, which means that the power spectral density is equal throughout the frequency spectrum, and because of this effect, it can be considered as white noise.

2.2.3.2 – Comparator Offset

This is considered to be the most important non linear characteristic of the comparator. The comparator works by determining which input has the larger voltage, an offset voltage causes an error where a small voltage can be considered to be larger.

This type of error is considered crucial when the two inputs have similar values, and because of the added offset the comparator will cause an error in the conversion. And this will propagate to the following stages.

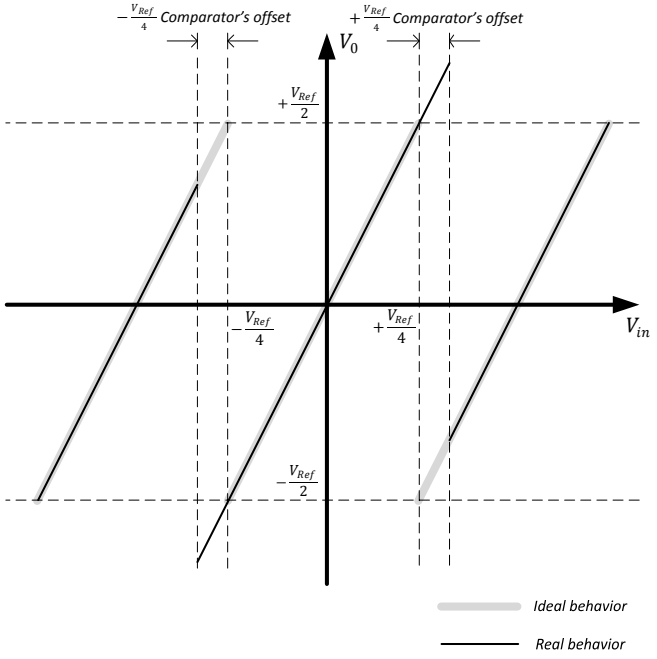


Figure 2.2.3.2.1 – Effect of the Comparator Offset on 1,5-bit Stage Transfer Function

2.2.3.3 – Residue Amplifier Gain Error

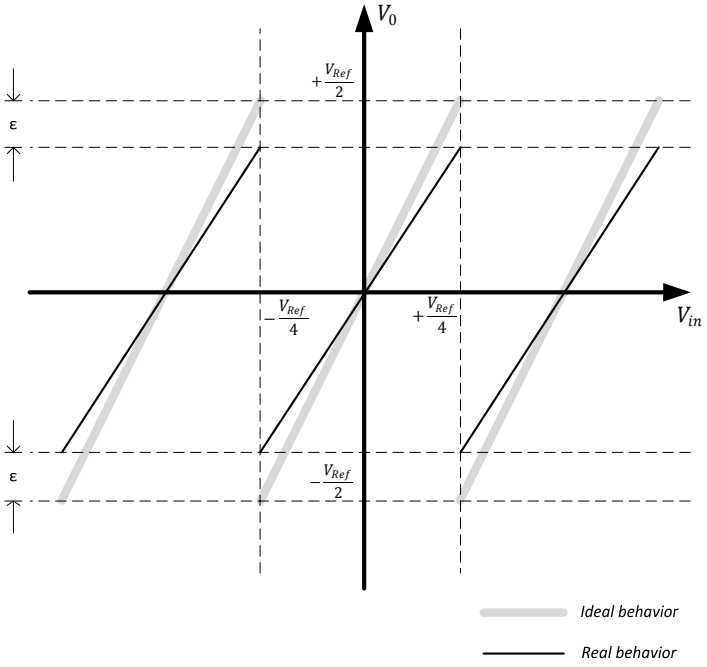


Figure 2.2.3.3.1 – Effect of Residue Amplifier Gain Error on 1,5-bit Stage Transfer Function

In pipeline ADCs the errors in the stage voltage gain are mostly due to by capacitor mismatch and non-infinite OPAMP gain and GBW.

This type of errors will affect the multiplication in the stage transfer function. Affecting the voltage gain will cause the converter to lose converting codes. These lost codes will affect the converters DNL. It's out of the scoop of this thesis a more profound mathematical analysis on the relation between the DNL and the gain error.

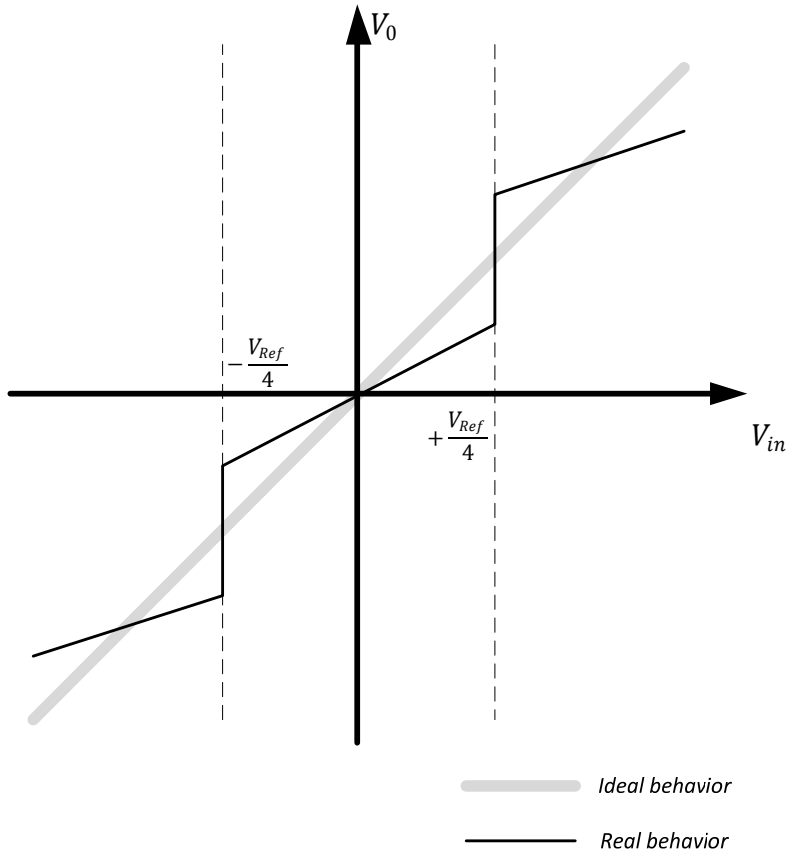


Figure 2.2.3.3.2 – Effect of Residue Amplifier Gain Error on Pipeline ADC Transfer Function

2.2.4 – Digital Correction

The converter accuracy is limited by the matching accuracy of nominal equal-sized analog circuit elements (resistors, capacitors, current sources). Hence, to perform an 10-bit digital-to-analog conversion, the required matching error of components cannot exceed 2^{-11}. This type of accuracy is within reach of CMOS technologies.

Several techniques were employed in the converters for relaxing the accuracy needs in the components. They can be classified into four different categories: analog correction, digital correction, error cancellation, and spectral error shaping.

In analog correction, an analog quantity (voltage, current, capacitance, …) is adjusted under digital control to regain the required accuracy. In digital correction, a digital code is modified so as to rectify the error made due to analog inaccuracies. In error cancellation, the conversion process is performed such that the unknown error enters twice, with opposite polarities, and is hence cancelled. The spectral error shaping (also designed mismatch shaping) the conversion process modifies the spectrum of the conversion error signal (which is unknown to the designer) so as to suppress its energy in the signal band.

The correction algorithms described can be performed at the system startup, or they can be performed continuously during the conversion process. The latter type of algorithm is preferable, since it can also correct time-varying inaccuracies, for example, inaccuracies caused by temperature variations.

In the designed converters the technique used is digital correction (also called digital redundancy) which can recover from code errors caused by nonzero comparator offsets. Another technique in this category is digital calibration, in both of them the analog errors are compensated in the digital domain.

To explain the digital correction it is best to start in understanding the effects of an offset in a normal N-bit pipeline ADC with 1-bit per stage resolution. Each stage provides one bit of the output,

starting with the most significant bit provided by the first stage, and passes on an analog residue voltage to the next stage for processing. In each stage it is included a 1-bit comparator with an input range from 0 to V_{Ref} and with a threshold voltage of $\frac{V_{Ref}}{2}$. The ideal stage operation it is described graphically in the figure 2.2.4.1(a).

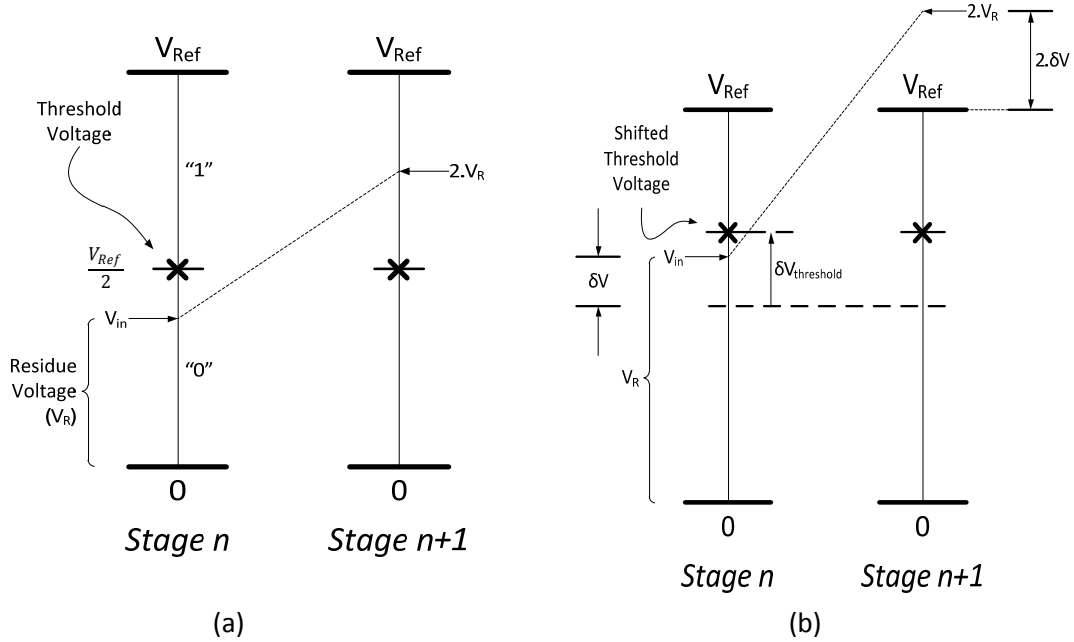


Figure 2.2.4.1 – Pipeline stage operation: (a) ideal; (b) with comparator offset

At the stage digital output will be a bit "1" or "0", depending if the input signal is above or below the threshold voltage (in the figure it is $\frac{V_{Ref}}{2}$). The residue voltage for this system accepting only positive input voltages will be $V_{in} - \frac{V_{Ref}}{2}$ or $V_{in} - 0$. The residue voltage enters the following stage with twice its value. So this means if the input voltage is below $\frac{V_{Ref}}{2}$, the input voltage of the following stage will be $2.V_{in}$; else if the input voltage is higher than $\frac{V_{Ref}}{2}$ the amplified residue voltage will be $2.V_{in} - V_{Ref}$.

If the converter has a input range from $-V_{Ref}$ to $+V_{Ref}$, then the comparator threshold will be located at 0 volt (since $V_{threshold} = \frac{+V_{Ref} - V_{Ref}}{2}$). So the amplified residue voltage will be $2.V_{in} - V_{Ref}$ and $2.V_{in} + V_{Ref}$ for input voltages below and above the comparator threshold, respectively.

The problem with this converter arises when the threshold voltage of the converter is not exactly $\frac{V_{Ref}}{2}$. Considering the case present in the figure 2.2.4.1(b) where the threshold voltage of the comparator is above $+\frac{V_{Ref}}{2}$ by a error value of $\delta V_{threshold}$, and having present an input signal above the $+\frac{V_{Ref}}{2}$ (by δV) but below the threshold voltage with offset. Since the signal is below the threshold voltage the output code of this stage will be zero, so this results at an amplified residue voltage of $2.V_{in} = 2.\left(\frac{V_{Ref}}{2} + \delta V\right) = V_{Ref} + 2.\delta V$, which is out of the input range of the following stage. This will result in input saturation which leads to code errors because of the comparator offsets.

To avoid the problems created by offsets in the comparators a simple architecture modification which can reduce the comparator specifications needed for a specified system. This modification is increasing the converter resolution for each stage (without one of the possible digital output codes) and using a lower resolution for the residue amplification, this way the input saturation of the following stage is avoided.

Using of a higher resolution in each stage leads to redundant bits, which allows up to $\pm 0{,}5$ LSB voltage for comparator offsets. Since the correction is done in the digital domain no more modifications are needed in the analog circuitry of the pipeline.

The most commonly used implementation of the digital correction is the 1,5-bit per stage pipeline architecture, introduced in [1]. The flash ADC present in this stages is composed by two comparators with threshold voltages of $-\frac{V_{Ref}}{4}$ and $+\frac{V_{Ref}}{4}$, resulting in three possible digital output codes.

A more rigorous description of digital correction can be found in [9] [2].

3 – Implementation of the Traditional Pipeline ADC

There are many trade-off when planning a Pipeline ADC. All of them can be related with the ADC resolution (and the related component accuracy); its power dissipation; and the converted number of bits per stage. This can be put into representation like the figure 3.1.1.

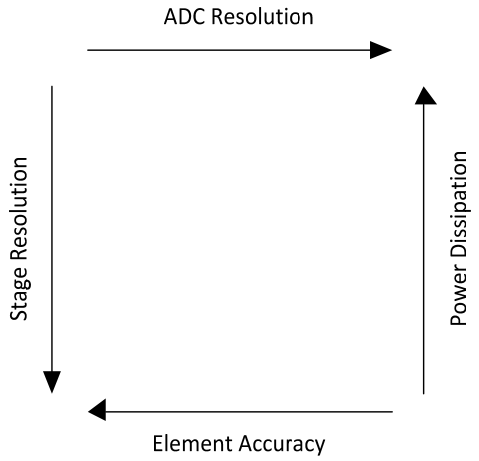


Figure 3.1 – Trade-off in the Pipeline ADC

Since the main question of this thesis is if a current based MDAC can withstand and achieve better results than the traditional pipeline ADCs it will be chosen the simplest design, because the main concern of this thesis is to prove the concept.

In this chapter the design for the implementation of a 10-bit Pipeline ADC with a maximum sampling frequency of 100MHz will be presented. So having in the base of the design the concept showed by the figure 2.1 and the design specifications, the simplest design of a pipeline ADC are 8 stages with a resolution of a 1,5-bit and a final 2-bit Flash ADC.

For the presentation of this traditional design, this chapter is divided in five sections: the MDAC design, the two Flash ADC designs, the Synchronization Logic, and the Digital Correction Logic.

Since there is a partial lock in the Stage resolution because of the need of comparing the traditional architecture and the proposed one while maintaining the same simplistic base design, it is needed for the several proposed designs to possess several techniques to permit the low voltage operation of Pipeline ADC converter architecture, and this way it is possible to reduce the power dissipation of the converter system.

3.1 – MDAC

The transfer function for a 1,5-bit stage is represented in the figure 3.1.1, and the equation system modeling the function is:

$$\Delta V_0 = \begin{cases} 2.\Delta V_{in} + V_{Ref}, & \Delta V_{in} < -\dfrac{V_{Ref}}{4} \\ 2.\Delta V_{in}, & -\dfrac{V_{Ref}}{4} \leq \Delta V_{in} \leq \dfrac{V_{Ref}}{4} \\ 2.\Delta V_{in} - V_{Ref}, & \Delta V_{in} > \dfrac{V_{Ref}}{4} \end{cases} \quad (3.1.1)$$

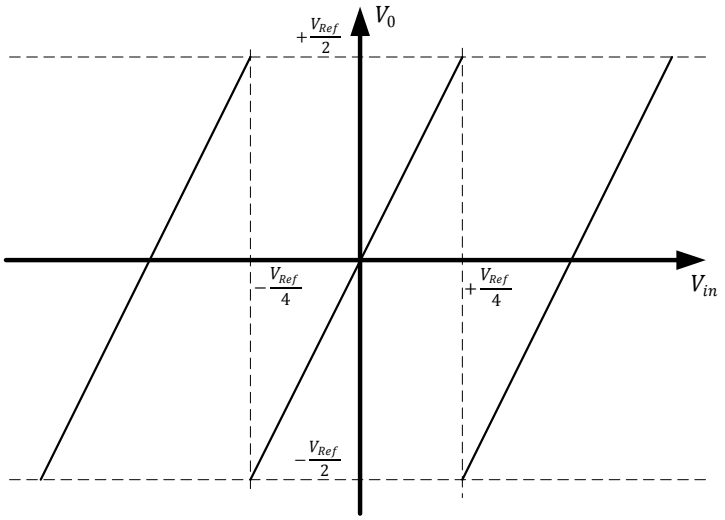


Figure 3.1.1 – Transfer function of a 1,5-bit stage

So observing the model equation and the transfer function plot there is the need for having three functions in the MDAC: a digital-to-analog converter, a adding and a subtraction, a sample-and-hold function, and a amplification.

The digital-to-analog converter is realized by using only two equal capacitors for a 1,5-bit stage, with the adding of a 1,5-bit Flash ADC with some logic to this structure it is possible to implement the adding and the subtraction functions.

The sample-and-hold and the amplification are done by the switched capacitor network.

The proposed 1,5-bit pipeline stage is represented by the figure 3.1.2. In that figure it's represented three structures: the OPAMP, 1,5-bit Flash ADC and switched capacitor network.

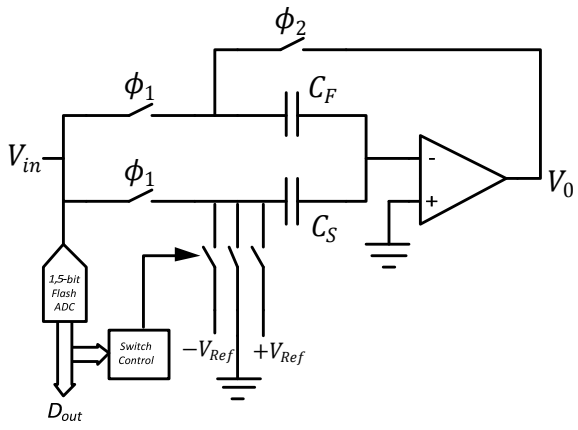


Figure 3.1.2 –1,5-bit pipeline stage structure

The switched capacitor network has a feedback factor associated with the number of capacitors in the circuit. Since the stage resolution is 1,5-bit it is only needed two equal capacitors. So the equation (2.2.1.7) without the input parasitic capacitance of the OPAMP will transform into:

$$\beta = \frac{C}{2.C} = \frac{1}{2} \tag{3.1.2}$$

This feedback factor is going to affect the accuracy requirements needed for the OPAMP, but also has problems with the thermal noise, which is for capacitors:

$$v_n(C) = 2.\sqrt{\frac{K_B.T}{C}} \tag{3.1.3}$$

Where K_B is the Boltzman constant which is:

$$K_B = 1{,}38 \times 10^{-23}\left(\frac{J}{K}\right) \tag{3.1.4}$$

And T is the absolute temperatures where it is assumed the circuit will work. The normal temperature is 28ºC which is:

$$T = 273 + T_{ºCelsius} = 301K \tag{3.1.5}$$

Since the maximum error allowed is:

$$\varepsilon_{max} = \frac{V_{lsb}}{2} = \frac{V_{Ref}}{2^{N+1}} \overset{N=10}{\Longrightarrow} \varepsilon_{max} = \frac{V_{Ref}}{2^{11}} = 0.1953\ mV \tag{3.1.6}$$

Where $V_{Ref} = 400\ mV$.

The capacitor value is determined in order to obtain a thermal noise value bellow the desired value. In terms of representation for respecting the thermal noise accuracy it's all the capacitors value which the noise generated by them in inferior to the maximum error.

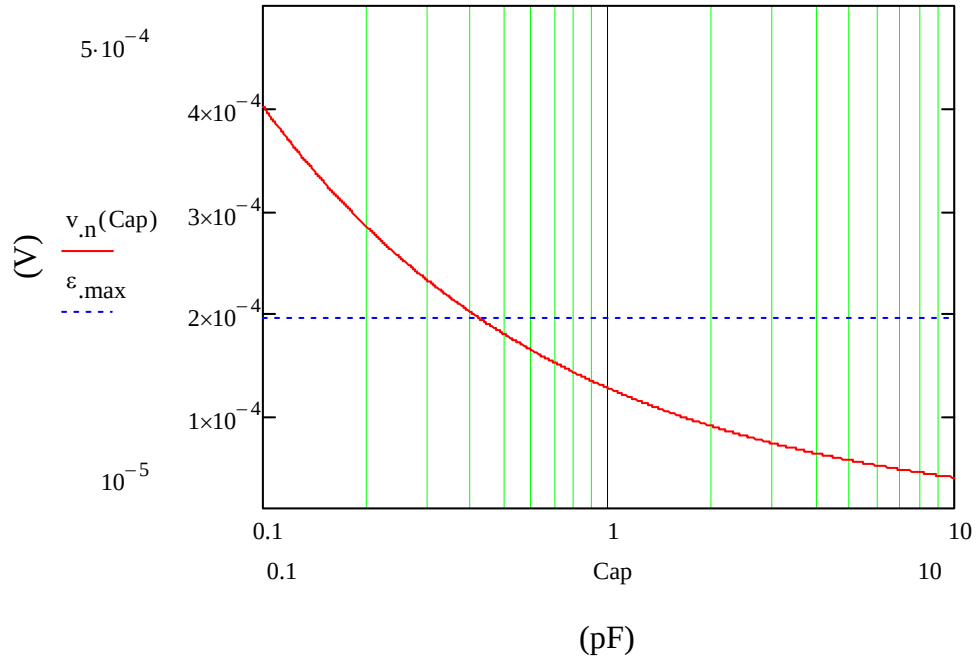


Figure 3.1.3 – Plot of capacitor thermal noise for a 10-bit ADC

The OPAMP presented in the design is considered a single-pole OPAMP, with bode diagram like the one represented in the figure 3.1.4.

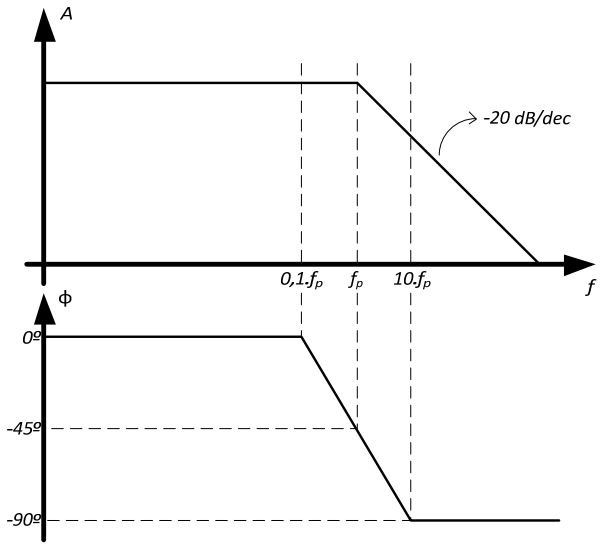


Figure 3.1.4 – Bode diagram of the transfer function of a single-pole OPAMP

The positioning of the pole in the OPAMP will limit the resolution and sampling frequency of the design where the OPAMP is used. So it is necessary to arrange equations for finding the best specifications for the OPAMP. This has the following mathematical expression for its open-loop gain:

$$A_{open-loop}(s) = \frac{A_0}{s + \frac{1}{\omega_p}} \tag{3.1.7}$$

Where A_0 is the finite DC gain. Also the closed-loop gain is:

$$A_{closed-loop}(s) = \frac{A_{open-loop}(s)}{1 + A_{open-loop}(s).\beta} = \frac{A_0}{1 + A_0.\beta} \frac{1}{s + \frac{1}{\omega_p(1 + A_0.\beta)}} \tag{3.1.8}$$

Knowing that the input signal is of the following type:

$$v_{in}(t) = V_x.u(t) \tag{3.1.9}$$

Where $u(t)$ is a unit step function.

Applying the Laplace Transform to the previous equation will result in:

$$V_{in}(s) = \frac{V_x}{s} \tag{3.1.10}$$

The output of the OPAMP is obtained by multiplying the transfer function of the closed-loop gain with the input signal. So the output of the closed-loop gain is:

$$V_0(s) = A_{closed-loop}(s).V_{in}(s) = \frac{A_0}{1 + A_0.\beta} \frac{1}{s + \frac{1}{\omega_p(1 + A_0.\beta)}} \frac{V_x}{s} \tag{3.1.11}$$

Applying the inverse Laplace Transform to equation (3.1.11):

$$v_0(t) = \frac{V_x}{\beta} \frac{A_0}{\frac{1}{\beta} + A_0} (1 - e^{-\omega_p(A_0+1).\beta.t}) \tag{3.1.12}$$

Where:

$$\omega_p(A_0 + 1).\beta = GBW \tag{3.1.13}$$

Rewriting the equation (3.1.12):

$$v_0(t) = \frac{V_x}{\beta} \frac{A_0}{\frac{1}{\beta} + A_0} (1 - e^{-GBW.t}) \tag{3.1.14}$$

So in equation (3.1.14) it is possible to see the non-idealities of the OPAMP present in each of the pipeline stage, which includes the finite OPAMP gain, finite time-settling, but doesn't take into account the mismatch in the switched capacitor network.

So a mismatch in the capacitors changes the feedback factor equation into:

$$\beta = \frac{C_F}{C_S + C_F} \tag{3.1.15}$$

To take the mismatch into account the equation (3.1.14) has to be changed into:

$$v_0(t) = \frac{1}{\frac{C_F}{C_S + C_F}} \frac{A_0}{\frac{1}{\frac{C_F}{C_S + C_F}} + A_0} (1 - e^{-GBW.t}).V_x \tag{3.1.16}$$

Using the zone where $-\frac{V_{Ref}}{4} \leq \Delta V_{in} \leq \frac{V_{Ref}}{4}$, it has the following transfer function:

$$\mathrm{V_0} = \mathrm{Gain}.\Delta V_{in} \tag{3.1.17}$$

Where V_x of equation (3.1.16) is equal to ΔV_{in}, so the Gain is:

$$\begin{aligned} \mathrm{Gain} &= \frac{1}{\frac{C_F}{C_S + C_F}} \frac{A_0}{\frac{1}{\frac{C_F}{C_S + C_F}} + A_0} (1 - e^{-GBW.t}) = \left(1 + \frac{C_S}{C_F}\right)(1 - e^{-GBW.t}) \frac{A_0}{\frac{1}{\frac{C_F}{C_S + C_F}} + A_0} \\ &= \left(1 + \frac{C_S}{C_F}\right) \frac{1}{\frac{1}{A_0 \frac{C_F}{C_S + C_F}} + 1} (1 - e^{-GBW.t}) = \left(1 + \frac{C_S}{C_F}\right) \frac{1}{\frac{1}{A_0.\beta} + 1} \left(1 - e^{-\frac{t}{\tau}}\right) \end{aligned} \tag{3.1.18}$$

Where $\tau = \frac{1}{GBW}$.

There are three terms in the previous equation where two of those are caused by a non-ideal effect. The first one, $\left(1 + \frac{C_S}{C_F}\right)$, is the term responsible for the voltage gain. The second one is related with the finite OPAMP gain. The last term with the exponential function is related with the settling time for a single-pole OPAMP, with its respective time constant τ.

If B is the per-stage resolution the ideal gain per-stage is given by:

$$G_{ideal} = 2^B \tag{3.1.19}$$

The gain error term can be achieved by:

$$\frac{\Delta G}{G} = \frac{G_{ideal} - Gain}{G_{ideal}} = \frac{2^B - \left(1 + \frac{C_S}{C_F}\right)\frac{1}{\frac{1}{A_0.\beta} + 1}\left(1 - e^{-\frac{t}{\tau}}\right)}{2^B} = \frac{1}{2^B}\left(2^B - \left(1 + \frac{C_S}{C_F}\right)\frac{1}{\frac{1}{A_0.\beta} + 1}\left(1 - e^{-\frac{t}{\tau}}\right)\right) \quad (3.1.20)$$

Simplifying the previous equation and normalizing the error:

$$\left|\frac{\Delta G}{G}\right| \approx \left|\left(\frac{(2^B - 1).\Delta C_F}{2^B.C} - \sum_{i=1}^{2^B-1}\frac{\Delta C_{S,i}}{2^B.C} + e^{-\frac{t}{\tau}} + \frac{1}{A_0.\beta}\right)\right| \quad (3.1.21)$$

Where:

$$\begin{cases} C = \frac{\sum_{i=1}^{2^B-1} C_{S,i} + C_F}{2^B} \\ \Delta C_F = C_F - C \\ \Delta C_{S,i} = C_{S,i} - C \end{cases} \quad (3.1.22)$$

In order to follow the N-bit accuracy, the normalized gain error, should be less than $\frac{1}{2^{N-B}}$, where N is the full resolution of the pipeline ADC. The reason for this restriction is to prevent missing codes. [11]

$$\left|\frac{\Delta G}{G}\right| < \frac{1}{2^{N-B}} \quad (3.1.23)$$

From previous equations three design requirements can be extracted: the OPAMP DC gain, the OPAMP bandwidth, the capacitor matching accuracy and thermal noise.

For the OPAMP gain, it's reasonable that $\frac{1}{A_0.\beta} \ll \frac{1}{2^{N-B}}$, because it's the most flexible design requirement. So:

$$\frac{1}{A_0.\beta} \ll \frac{1}{2^{N-B}} \quad \Rightarrow \quad A_0 > \frac{2^{N-B}}{\beta} = 2^{N-B}\frac{2^B.C + C_{input\ capacitance}}{C} \quad (3.1.24)$$

If there isn't no input parasitic capacitance the previous expression reduces to $A_0 > 2^N$. But because of process variations, and to make the ADC more reliable, this value needs to be at least two to three times larger than this theoretical value.

For a regular operation the OPAMP has to have a settling time of half clock period $\left(T_{Settle} = \frac{1}{2f_s}\right)$ in which the OPAMP settles with an error of $\frac{1}{2^N}$. So:

$$e^{-\frac{T_{Settle}}{\tau}} < \frac{1}{2^N} \Leftrightarrow -\frac{T_{Settle}}{\tau} < \log\left(\frac{1}{2^N}\right) \Leftrightarrow -\frac{T_{Settle}}{\tau} < -\log(2^N) \Leftrightarrow T_{Settle} > N.\log(2).\tau \tag{3.1.25}$$

Starting to analyze the capacitor matching the transfer function can be written as:

$$V_0 = \left(1 + \frac{\sum_{i=1}^{2^B-1} C_{S,i}}{C_F}\right).V_{in} + \frac{\sum_{i=1}^{2^B-1} d_i.C_{S,i}}{C_F}V_{Ref} \tag{3.1.26}$$

$$\Leftrightarrow V_0 = G\left(1 + \frac{\Delta G}{G}\right)\left(V_{in} + \frac{\sum_{i=1}^{2^B-1} d_i.C_{S,i}}{G.C_F}V_{Ref}\right) \tag{3.1.27}$$

$$\Leftrightarrow V_0 = G\left(1 + \frac{\Delta G}{G}\right)\left(V_{in} + \frac{1}{G}\left(\sum_{i=1}^{2^B-1} d_i.C_{S,i}\right)V_{Ref} + \Delta V_{Ref}\right) \tag{3.1.28}$$

Where d_i is controlled by the Flash ADC and can have the following value:

$$d_i = \begin{cases} +1, & \Delta V_{in} < -\frac{V_{Ref}}{4} \\ 0, & -\frac{V_{Ref}}{4} \leq \Delta V_{in} \leq \frac{V_{Ref}}{4} \\ -1, & \Delta V_{in} > \frac{V_{Ref}}{4} \end{cases} \tag{3.1.29}$$

The ΔV_{Ref} is the error related with the switched capacitors circuit. And its value is:

$$\Delta V_{Ref} \approx \frac{1}{G}\left(\sum_{i=1}^{2^B-1} d_i.\frac{\Delta C_{S,i}}{\mathrm{C}}\right)V_{Ref} \tag{3.1.30}$$

This is one of the major concerns in the design of the pipeline ADC, because this error takes an immediate action on the output voltage of the pipeline stage. So to take this error in check the maximum error permitted is:

$$\Delta V_{Ref} < \frac{V_{lsb}}{2} = \frac{V_{Ref}}{2^{N+1}} \tag{3.1.31}$$

So:

$$\frac{1}{G}\left(\sum_{i=1}^{2^B-1} d_i.\frac{\Delta C_{S,i}}{\mathrm{C}}\right)V_{Ref} < \frac{V_{Ref}}{2^{N+1}} \Leftrightarrow \frac{1}{2^B}\left(\sum_{i=1}^{2^B-1} d_i.\frac{\Delta C_{S,i}}{\mathrm{C}}\right) < \frac{1}{2^{N+1}} \Rightarrow \frac{\Delta C}{C} < \frac{1}{2^N} \tag{3.1.32}$$

3.1.1 – OPAMP sharing

Like it was previously mentioned the main concern in this thesis was trying to answer if the new MDAC approach can mask the high-frequency bounding wires effects. So in a similar way when the Foundries are testing the new process they use a ring oscillator to test it, in this thesis the simplest design was to have a 1,5-bit per-stage resolution.

This simplification is not the best when tackling the power dissipation problem because it needs eight OPAMPs for each of the eight switched capacitor networks. By sharing an OPAMP between two consecutive stages in the pipeline the power consumption of the Pipeline ADC can be reduce significantly [16], by reducing the number of necessary OPAMP by half. This implementation is represented in the figure 3.1.1.1.

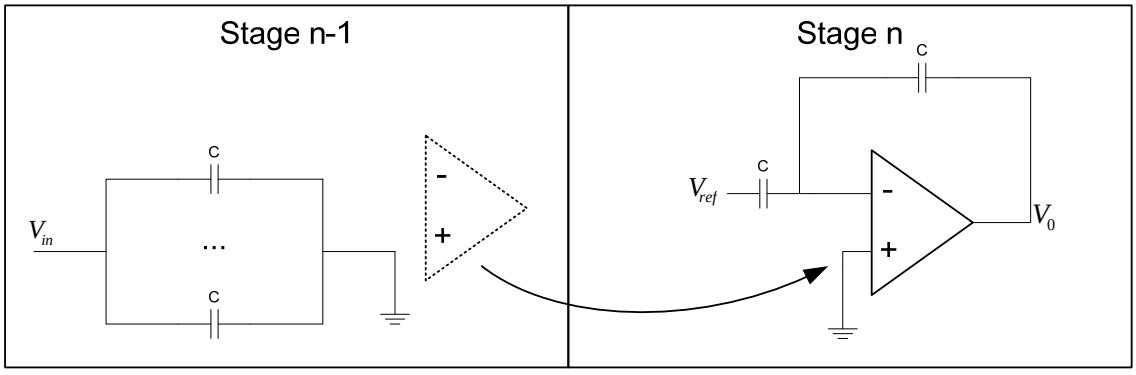


Figure 3.1.1.1 – OPAMP sharing technique

The use of this technique it is only possible because of the temporal way that the switched-capacitor circuit uses the OPAMP. With the classical approach the OPAMP is only being used in half

of a clock cycle, which is during the amplification phase, and it's doing nothing during the sampling phase.

	Not Shared	Shared
ϕ_1		Amplification of stage n-1
ϕ_2	Amplification of stage n	Amplification of stage n

Figure 3.1.1.2 – OPAMP time division

There are some high-precision circuits that use the sampling phase to carry offset cancelation during this phase. Because if a pipeline ADC has interstage offset, this tends to make the ADC non-linear.

The non-linearity on the pipeline ADCs only occurs if there isn't any redundancy, because if there is the interstage offset that are less than the correction range will only cause input-referred ADC offset [12].

The sharing of OPAMP will be made between the adjacent stages [13] [14] because of those two stages have theirs switched-capacitor networks operating at opposite clock phases. Since they are in opposite clock phases it is possible to share the OPAMP between the two stages.

The decision circuits can also be shared between the two stages [15] but since the decision circuits used in this thesis need the two clock phases to produce its output and they only produce a small percentage of dissipated power.

This technique consists in switching the electrical connections of the input and output of the OPAMP depending of the phases of the two adjacent stages. For example, in the figure 3.1.1.1, the stage n-1 is in sampling phase, that means that the OPAMP traditionally is in idle state or offset sampling mode, but the next stage is in amplification phase and in need of an OPAMP. So instead of having the OPAMP doing nothing in sampling phase the designer can have it doing its work where is needed.

The only difference of this technique from the traditional structure is the two additional switches at the two input terminal, like it is represented in the figure 3.1.1.3.

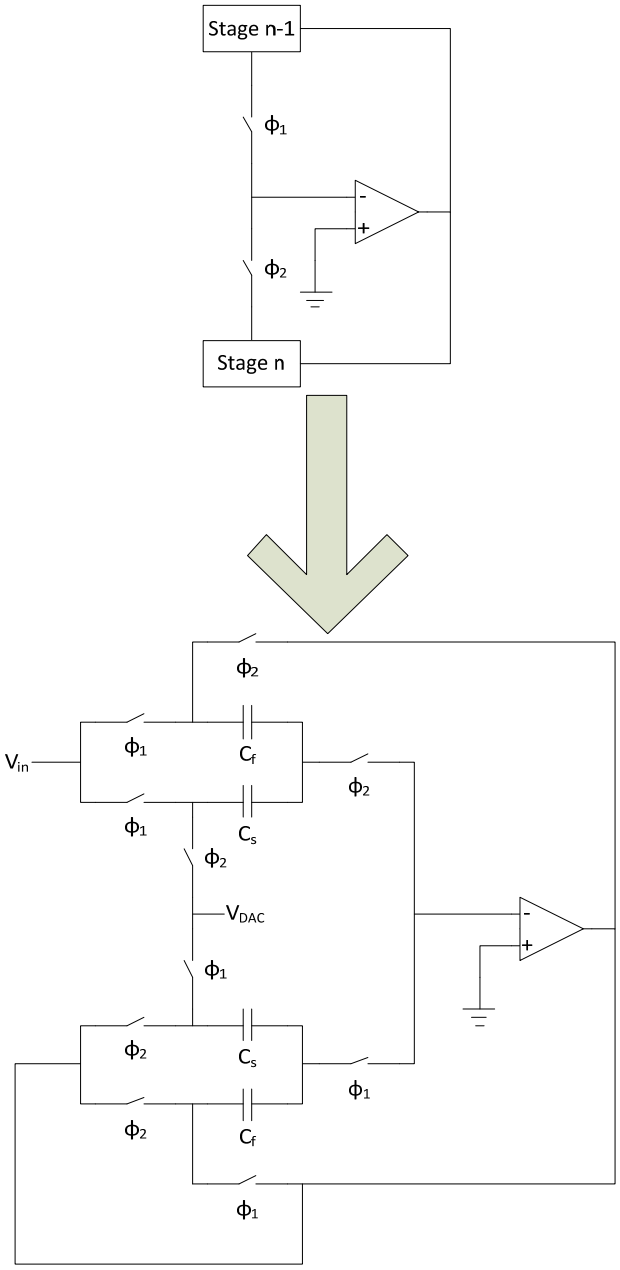


Figure 3.1.1.3 – Block schematic pipeline stage of the shared OPAMP

This technique introduces two side effects. The first effect is the introducing of series resistance by the new switches, which in combination with the OPAMP input capacitance will affect the settling behavior of the stage.

The switch resistance can be reduced if the switches are enlarged but this will also increase the parasitic capacitances in the switch. This has the potential to increase the offsets due to the charge feedthrought.

The second side effect is the memory effect because of the input parasitic capacitances (which are the input parasitic capacitances and the switch parasitic capacitances). This memory effect results of the OPAMP never being able to reset it inputs. This non-reset situation is important because of the nonzero input voltage of the OPAMP since the OPAMP doesn't have an infinite gain.

3.1.2 – Bootstrapping CMOS Switches

One of the more important aspects in the operation of a switch is to maintain the conductance constant during its operation, and to get this condition is that the gate-to-channel voltage should be held with a significant and constant value during the ON switches state.

The value needed for maintaining a constant conductance can be achieved with the bootstrapping technique which consists by the name definition of boosting the gate voltage of the switch to a value superior to the power supply.

This technique uses an extra switched-capacitor circuit to generate the new controlling voltage.

With the use of bootstrapping a reduction of the CMOS switch size can be achieved. And with this reduction of the size there is a reduction of the switch parasitic capacitances.

Since CMOS switch has two transistors, one NMOS and one PMOS, there is the need of two separated bootstrapping circuits. The proposed structure for bootstrapping the CMOS switches is represented in the figure 3.1.2.1.

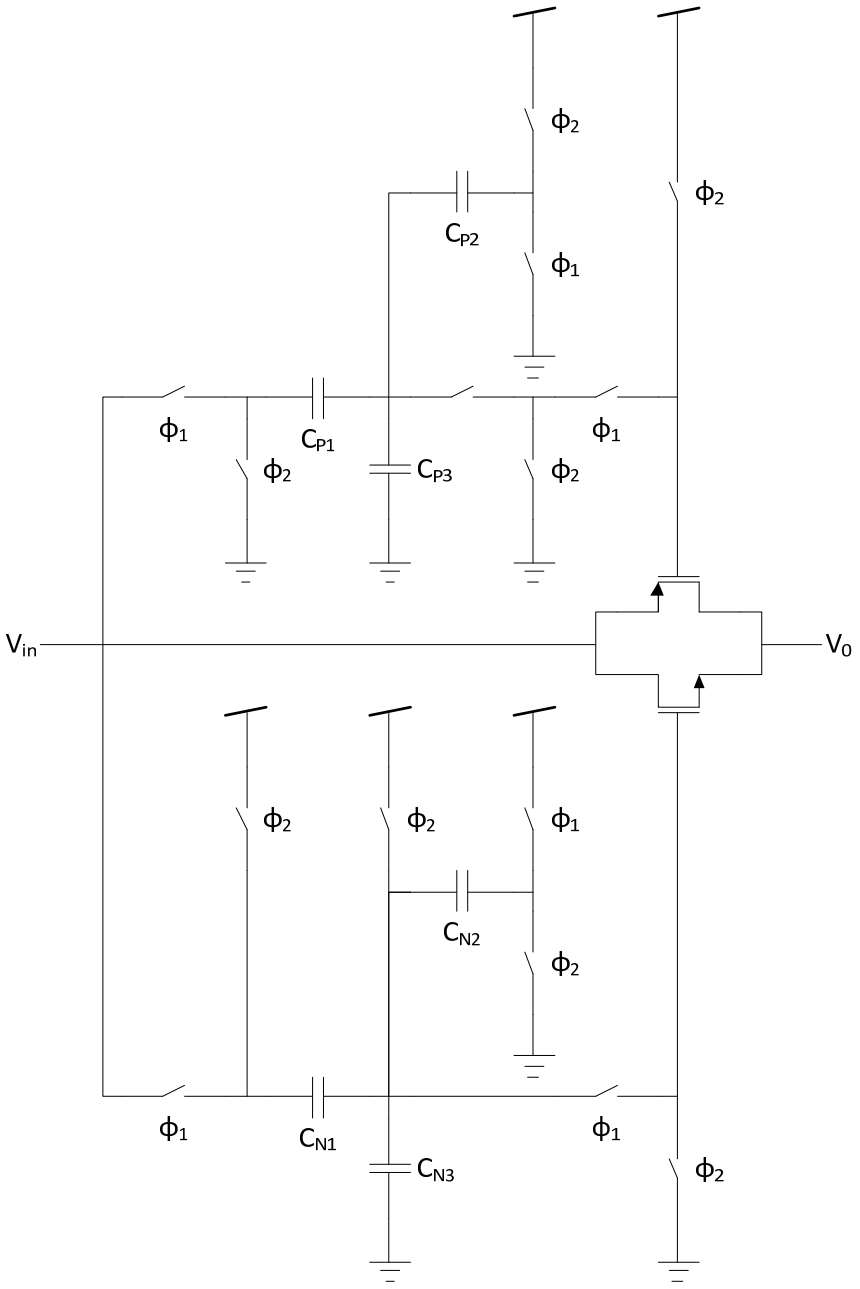


Figure 3.1.2.1 – Proposed bootstrapping for the CMOS switches

The figure above can have two extra representations because of the different clock phases.

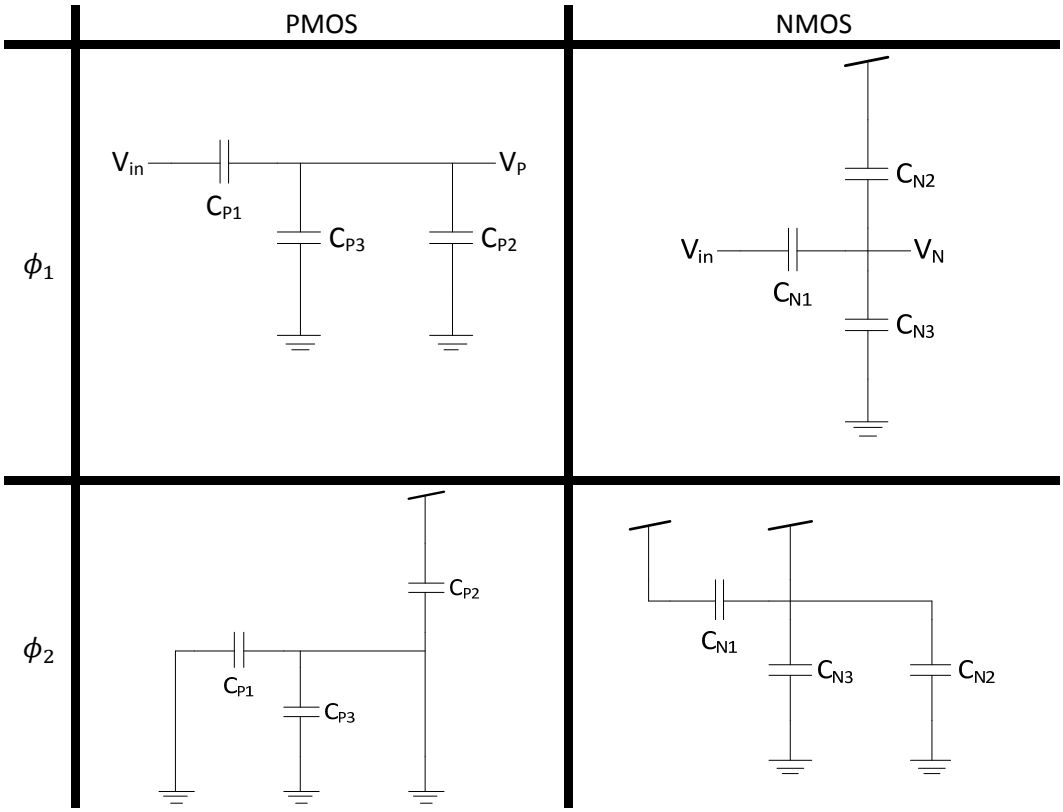


Figure 3.1.2.2 – Bootstrapping structure at different clock phases

From the previous figure it can be extracted the following equations regarding the charge of the capacitors in the different phases:

Table 3.1.2.1 – Charge conservation table

	ϕ_1	ϕ_2
$Q_{C_{N1}}$	$(V_N - V_{in}).C_{N1}$	0
$Q_{C_{N2}}$	$(V_N - V_{DD}).C_{N2}$	$V_{DD}.C_{N2}$
$Q_{C_{N3}}$	$V_N.C_{N3}$	$V_{DD}.C_{N3}$
$Q_{C_{P1}}$	$(V_P - V_{in}).C_{P1}$	0
$Q_{C_{P2}}$	$V_P.C_{P2}$	$-V_{DD}.C_{P2}$
$Q_{C_{P3}}$	$V_P.C_{P3}$	0

From the previous table and by the charge conservation principle:

$$\begin{cases} -V_{DD}.C_{P2} = C_{P1}.(V_P - V_{in}) + C_{P2}.V_P + C_{P3}.V_P \\ V_{DD}.C_{N3} + V_{DD}.C_{N2} = C_{N1}.(V_N - V_{in}) + C_{N2}.(V_N - V_{DD}) + C_{N3}.V_N \end{cases}$$
$$\Leftrightarrow \begin{cases} V_P(C_{P1} + C_{P2} + C_{P3}) = V_{in}.C_{P1} - V_{DD}.C_{P2} \\ V_N(C_{N1} + C_{N2} + C_{N3}) = V_{in}.C_{N1} + V_{DD}.(C_{N3} + 2.C_{N2}) \end{cases} \quad (3.1.2.1)$$

So regarding the final bootstrap voltages of the CMOS switch:

$$\Leftrightarrow \begin{cases} V_P = V_{in}.\dfrac{C_{P1}}{C_{P1} + C_{P2} + C_{P3}} - V_{DD}.\dfrac{C_{P2}}{C_{P1} + C_{P2} + C_{P3}} \\ V_N = V_{in}.\dfrac{C_{N1}}{C_{N1} + C_{N2} + C_{N3}} + V_{DD}.\dfrac{C_{N3} + 2.C_{N2}}{C_{N1} + C_{N2} + C_{N3}} \end{cases} \quad (3.1.2.2)$$

In order to keep the capacitance values of the bootstrap circuits as low as possible, for these capacitors to be implemented in a layout, the effect of the gate capacitance of the main switches, C_{Ng} and C_{Pg}, must be considered in the equation (3.1.2.2).

$$\Leftrightarrow \begin{cases} V_P = V_{in}.\dfrac{C_{P1} + C_{Pg}}{C_{P1} + C_{P2} + C_{P3} + C_{Pg}} - V_{DD}.\dfrac{C_{P2} + \dfrac{C_{Pg}}{2}}{C_{P1} + C_{P2} + C_{P3} + +C_{Pg}} \\ V_N = V_{in}.\dfrac{C_{N1} + C_{Ng}}{C_{N1} + C_{N2} + C_{N3} + C_{Ng}} + V_{DD}.\dfrac{C_{N3} + 2.C_{N2} + \dfrac{C_{Ng}}{2}}{C_{N1} + C_{N2} + C_{N3} + C_{Ng}} \end{cases} \quad (3.1.2.3)$$

The equation system (3.1.2.3) can be re-written with capacitance ratios for simplicity.

$$\Leftrightarrow \begin{cases} V_P = V_{in}.K_{P1} - V_{DD}.K_{P2} \\ V_N = V_{in}.K_{N1} + V_{DD}.K_{N2} \end{cases} \quad (3.1.2.4)$$

Where:

$$\begin{cases} K_{P1} = \dfrac{C_{P1} + C_{Pg}}{C_{P1} + C_{P2} + C_{P3} + C_{Pg}} \\ K_{P2} = \dfrac{C_{P2} + \dfrac{C_{Pg}}{2}}{C_{P1} + C_{P2} + C_{P3} + +C_{Pg}} \\ K_{N1} = \dfrac{C_{N1} + C_{Ng}}{C_{N1} + C_{N2} + C_{N3} + C_{Ng}} \\ K_{N2} = \dfrac{C_{N3} + 2.C_{N2} + \dfrac{C_{Ng}}{2}}{C_{N1} + C_{N2} + C_{N3} + C_{Ng}} \end{cases} \quad (3.1.2.5)$$

Another linearization technique was applied to the PMOS main switch, this technique is explained in [19].

In the Figure 3.1.2.3 it is represented the implementation of the bootstrap circuit for the NMOS and PMOS switches. In the annex chapter where is discussed the application of the different types of switches it is explained why it is used a CMOS switch where the voltage to its terminal vary (because of its fast settling-time), and why when one of the terminal is connected to the ground the designer uses a NMOS transistor as a switch. And when the terminal is connected to a V_{DD} voltage the designer uses the PMOS transistor for that function.

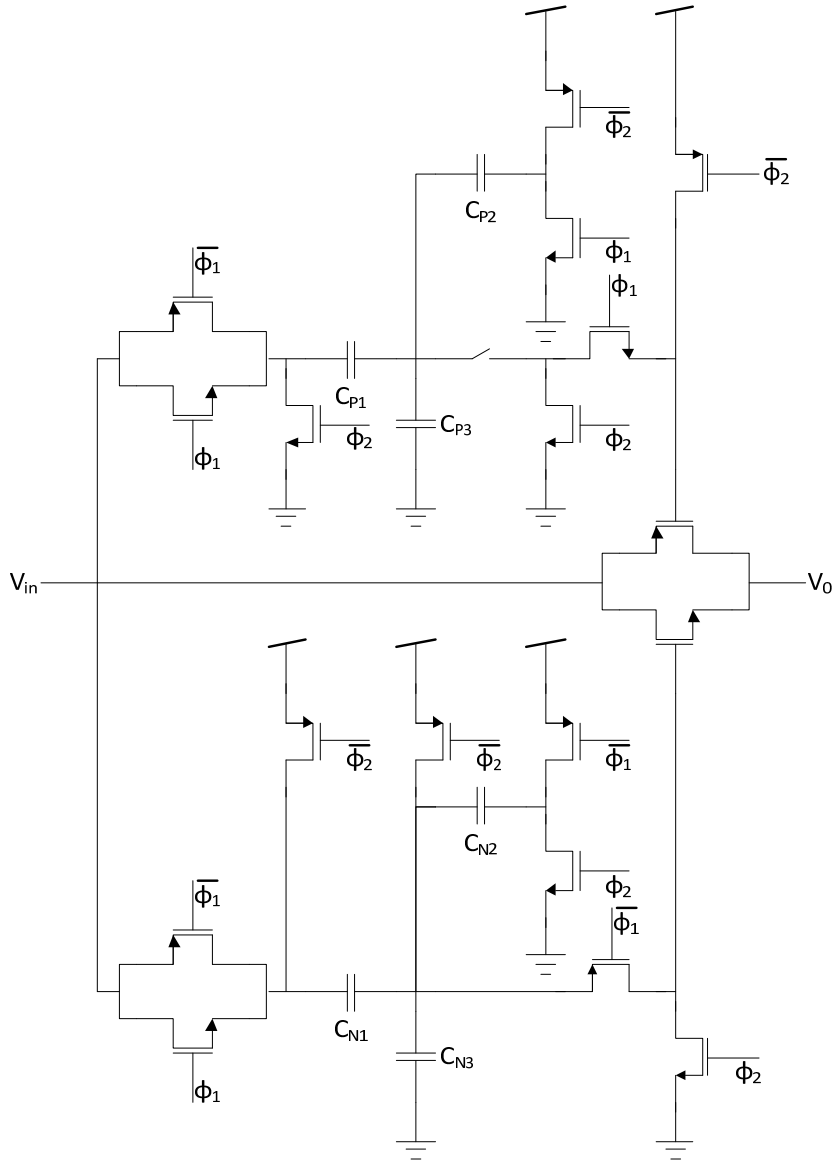


Figure 3.1.2.3 – Proposed bootstrapping structure

To implement the bootstrap circuit, the designer begins to define the capacitance value of C_{N3}. This capacitor value is sized through simulation to be 30fF. This value allows the bootstrap circuit to become more independent of the parasitic effects of the main NMOS switch.

The following step is to define the maximum value allowed for the input voltage. Assuming that V_{in} will have a maximum of ninety percent of V_{DD}. In order to avoid side-effects the NMOS part of the equation system (3.1.2.4) has to be limited to a conservative value of $V_{DD} + V_{T_N}$. Relating all conditions with the NMOS part of the equation system (3.1.2.4):

$$\begin{aligned} 0{,}9.V_{DD}.K_{N1} + V_{DD}.K_{N2} &< V_{DD} + V_{T_N} \\ \Leftrightarrow 0{,}9.K_{N1} + K_{N2} - 1 &< \frac{V_{T_N}}{V_{DD}} \end{aligned} \tag{3.1.2.6}$$

The equation (3.1.2.6) permits to make a relation between K_{N1} and K_{N2}. Plotting V_N in function of V_{in}, the K_{N1} ratio should cause an amplification for low values of V_{in} and an attenuation for high values. Using mathematical auxiliary tools the targeted value for K_{N1} ratio is 0,5. This conditions permits to write the following equation system.

$$\begin{cases} 0{,}9.K_{N1} + K_{N2} - 1 < \dfrac{V_{T_N}}{V_{DD}} \\ \\ K_{N1} = 0{,}5 \end{cases} \tag{3.1.2.7}$$

Developing the equation system, the computed values of C_{N1} and C_{N2} are 100 and 80 fF, respectively. To overcome the effects of the NMOS switch gate capacitance, the sum of C_{N1}, C_{N2} and C_{N3} needs to be higher than the gate parasite. Otherwise, the system needs to be recalculated with a higher value for the bootstrap capacitor C_{N3}.

Since transistors in the CMOS switch are not of the same size because of the electron mobility constant, the CMOS switch is sized asymmetrically, the effective gate voltage absolute value of the NMOS and PMOS switches should be the same in these two conditions.

$$0{,}9.K_{P1} + K_{P2} = 0{,}9 - K_{N2} + \frac{V_{T_N}}{V_{DD}} - \frac{|V_{T_P}|}{V_{DD}} \tag{3.1.2.8}$$

Looking at the traditional slope for the g_{ds_N} as function of V_{in}, it is affected by the body factor γ_N, surface potential $2|\Phi F|$ and input signal. Hence, the slope of V_P will have a lower value than the slope of V_N (in absolute value).

$$K_{P1} = K_{N1} - \frac{\gamma_N}{2.\sqrt{V_{in} + 2|\Phi F|}} \quad (3.1.2.9)$$

For a V_{in} value of $\frac{V_{DD}}{2}$ the capacitor ratio K_{P1} is 0,24. The computed value of the bootstrap capacitors C_{P2} and C_{P3} are 150 and 330 fF, respectively, with the C_{P1} being the defined value of 30 fF. These values aren't affected by the effects of PMOS gate parasite in the simulations at 40 MS/s.

3.2 – 1,5-bit Flash ADC

The 1,5-bit Flash ADC consists of two comparators, followed by a thermometer-to-binary digital encoder. Since this Flash ADC will also control which operation the MDAC will realize, it is needed an X, Y, Z encoder for controlling the switches that perform those functions.

The block diagram of the Flash ADC is represented in the figure 3.2.1.

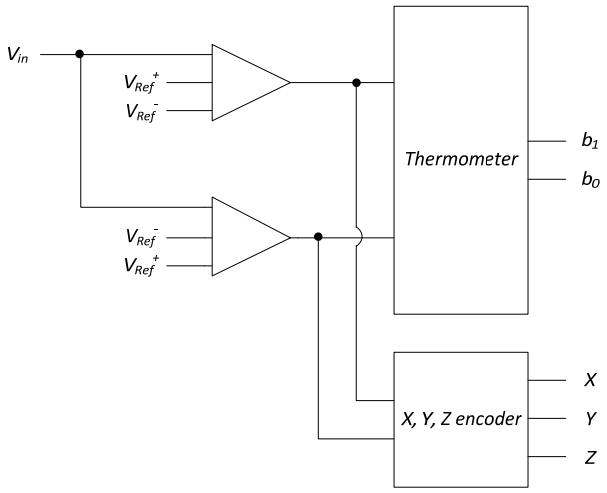


Figure 3.2.1 – Block diagram of a 1,5-bit Flash ADC

The Flash ADC consist of two comparators, thermometer-to-binary encoder and by an x, y and z encoder. The comparators used are based in ones of [17].

3.2.1 – Comparator

Each comparator contains a switched-capacitor circuit (the comparator bank), a pre-amplifier, and a digital latch, as is represented in the figure 3.2.1.1

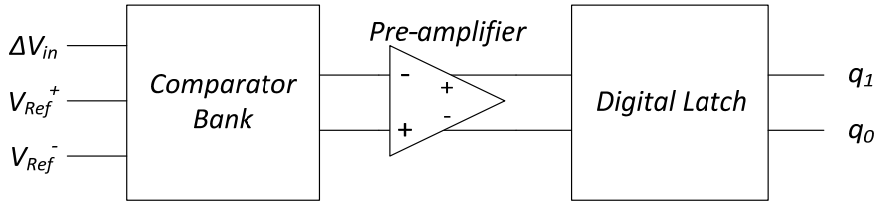


Figure 3.2.1.1 – Block diagram of a comparator

The comparator bank is composed of a switched-capacitor network that does a simple arithmetic operation. And for doing this operation the structure of the switched-capacitor network will have the schematic in figure 3.2.1.2.

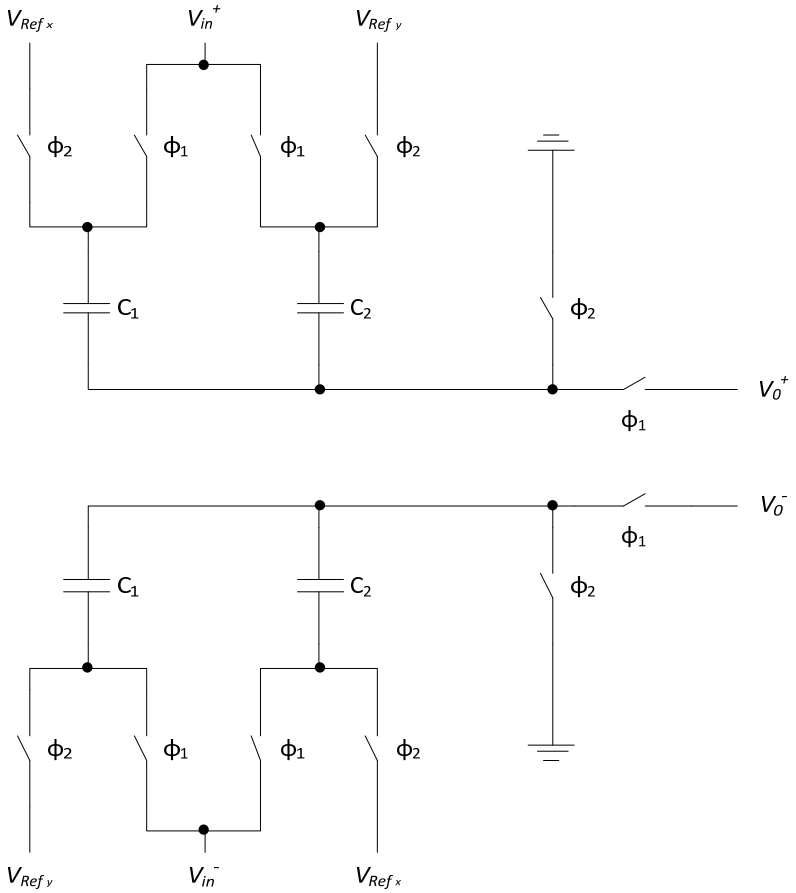


Figure 3.2.1.2 – Schematic of a comparator bank

The pre-amplifier will only look at its inputs during the phase ϕ_1, so the equations that model the behavior of the comparator bank are:

$$\begin{cases} C_1.(V_{in}^{+} - V_0^{+}) + C_2.(V_{in}^{+} - V_0^{+}) = C_1.V_{Ref_x} + C_2.V_{Ref_y} \\ C_1.(V_{in}^{-} - V_0^{-}) + C_2.(V_{in}^{-} - V_0^{-}) = C_1.V_{Ref_y} + C_2.V_{Ref_x} \end{cases} \quad (3.2.1.1)$$

Relating the equations of the system (3.2.1.1), and knowing that $\Delta V_{Ref} = V_{Ref_y} - V_{Ref_x}$ so:

$$\begin{aligned} \Rightarrow C_1.(\Delta V_{in} - \Delta V_0) + C_2.(\Delta V_{in} - \Delta V_0) &= -C_1.\Delta V_{Ref} + C_2.\Delta V_{Ref} \\ \Leftrightarrow (C_1 + C_2).(\Delta V_{in} - \Delta V_0) &= (C_2 - C_1).\Delta V_{Ref} \\ \Leftrightarrow \Delta V_0 = \Delta V_{in} - \frac{C_2 - C_1}{C_1 + C_2}\Delta V_{Ref} & \end{aligned} \quad (3.2.1.2)$$

Because the pipeline stage resolution is of 1,5-bit this means that the 1,5-bit flash ADC only requires two comparators with two threshold voltages:

$$V_{1,5-bit\ Threshold} = \pm\frac{\Delta V_{Ref}}{2^2} = \pm\frac{\Delta V_{Ref}}{4} \quad (3.2.1.3)$$

The different values of capacitors in the switch capacity circuit will define the threshold level. So know the relation between them it will be used the two previous equations. The equivalence between them is:

$$\begin{aligned} \frac{\Delta V_{Ref}}{4} &= \frac{C_2 - C_1}{C_1 + C_2}\Delta V_{Ref} \\ \Leftrightarrow \frac{C_2 - C_1}{C_1 + C_2} &= \frac{1}{4} \\ \Leftrightarrow 4.(C_2 - C_1) &= C_1 + C_2 \\ \Leftrightarrow 3.C_2 &= 5.C_1 \\ \Leftrightarrow C_1 &= \frac{3}{5}C_2 \end{aligned} \quad (3.2.1.4)$$

From the equation (3.2.1.4) the designer knows how much the difference in value of Farads needs to be between the capacitors on the comparator bank for it to respond to the threshold voltage.

The comparators are designed in order to have an offset lower than the value of an ADC's LSB, because if it's larger than that value it can make the comparator to give false results. So to further reduce the possibility of high offset the comparator bank was made with dummy switches to technique to reduce the charge injection provoked by the clock feedthrought.

The output of this circuit will by pre-amplify and then the latch will decide the value of the thermometer. Because these ADC have low resolution the pre-amplifier gain doesn't need to be elevated, so the design of this circuit will be very simple.

The output of the pre-amplifier will connect to a digital latch (regenerative type) that is located at the end of each comparator for storing the result of the quantization. The latch has positive feedback for forcing the output to the logic values zero or one.

3.2.2 – Digital thermometer and X, Y and Z encoder

In the interest of maintaining the power dissipation low both of this structures were assimilated in one. This new structure used to generate the MDAC control inputs, X, Y and Z, and the stage output codes, b_0 and b_1 is represented in the figure 3.2.2.1.

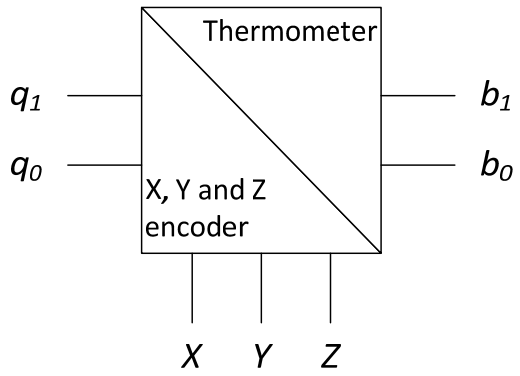


Figure 3.2.2.1 – Digital thermometer and coding generation

The ideal residue amplification characteristics like it was previous discussed will behave like:

$$\begin{cases} \Delta V_0 = 2.\Delta V_{in} + \Delta V_{Ref}, & if\ \Delta V_{in} < -\dfrac{\Delta V_{Ref}}{4} \\ \Delta V_0 = 2.\Delta V_{in}, & if\ -\dfrac{\Delta V_{Ref}}{4} \geq \Delta V_{in} \leq +\dfrac{\Delta V_{Ref}}{4} \\ \Delta V_0 = 2.\Delta V_{in} - \Delta V_{Ref}, & if\ \Delta V_{in} > +\dfrac{\Delta V_{Ref}}{4} \end{cases} \quad (3.2.2.1)$$

The following table is the best way to explain how this sub-circuit works.

Table 3.2.2.1 – Relation between the comparator output and its encoding

Differential input ΔV_{in}	Comparator output		MDAC control input			Output code	
	q_1	q_0	X	Y	Z	b_1	b_0
$\Delta V_{in} < -\frac{\Delta V_{Ref}}{4}$	0	0	0	1	0	0	0
$-\frac{\Delta V_{Ref}}{4} \leq \Delta V_{in} \leq +\frac{\Delta V_{Ref}}{4}$	0	1	0	0	1	0	1
$\Delta V_{in} > +\frac{\Delta V_{Ref}}{4}$	1	1	1	0	0	1	0

From the previous table it's easy to discover the logic needed for the circuit. And the logic is represented in the figure 3.2.2.2.

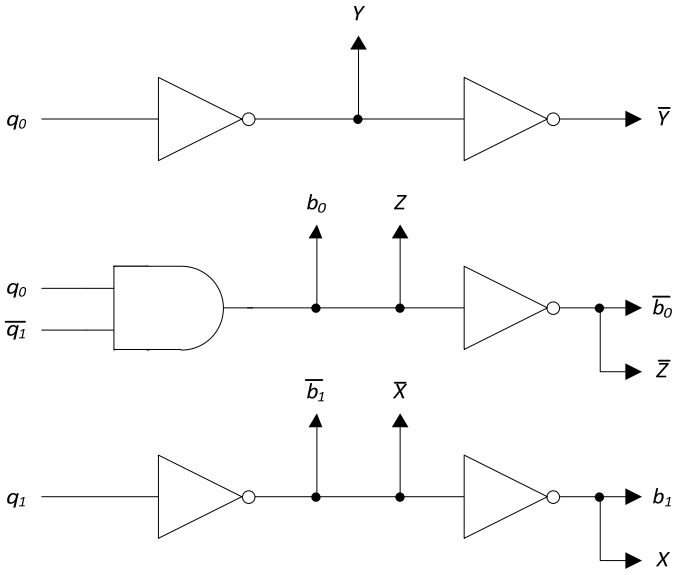


Figure 3.2.2.2 – Logic circuit used for this encoder

3.3 – Final 2-bit Flash ADC Stage

Since the final stage of the pipeline a 2-bit Flash ADC it will need three comparators. And this is the only difference from the 1,5-bit Flash ADC. This and a 3 thermometer encoder without the MDAC controlling input logic.

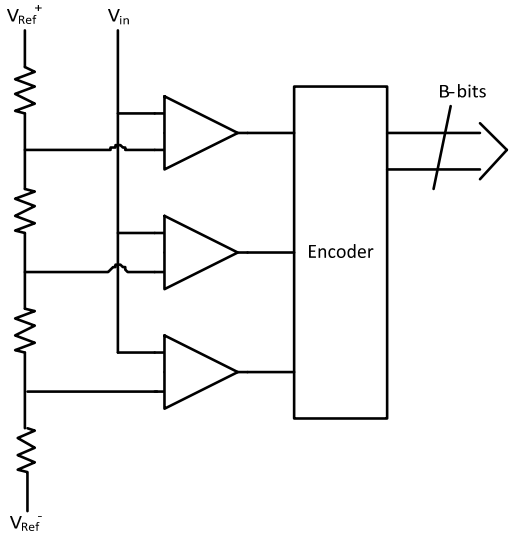


Figure 3.3.1 – 2-bit Flash ADC based in resistances

In the figure 3.3.1 it will be used a comparator bank like it was used in the 1,5-bit Flash ADC. The threshold voltages of the comparators are described in the figure 3.3.2.

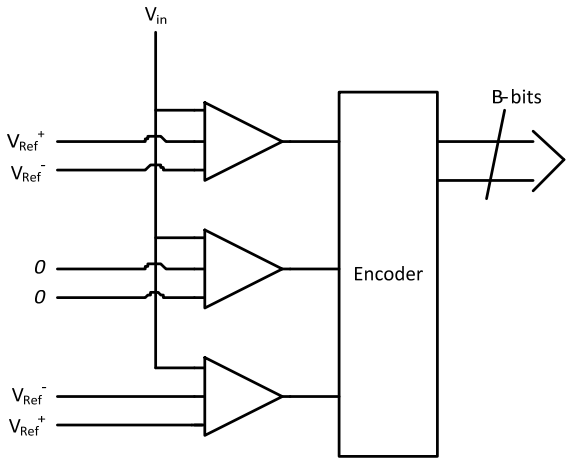


Figure 3.3.2 – Schematic of 2-bit Flash ADC based in capacitors

The following table is the best way to explain how this ADC works.

Table 3.2.1 – Relation between the comparator output and its encoding

Differential input ΔV_{in}	Comparator output			Output code	
	q_2	q_1	q_0	b_1	b_0
$\Delta V_{in} < -\frac{\Delta V_{Ref}}{2}$	0	0	0	0	0
$-\frac{\Delta V_{Ref}}{2} \leq \Delta V_{in} < 0$	0	0	1	0	1
$0 < \Delta V_{in} \leq +\frac{\Delta V_{Ref}}{2}$	0	1	1	1	0
$\Delta V_{in} > +\frac{\Delta V_{Ref}}{2}$	1	1	1	1	1

From the previous table the logic functions can be extracted to obtain a logic circuit that performs the encoding of comparators output. And this logic is shown in the following figure.

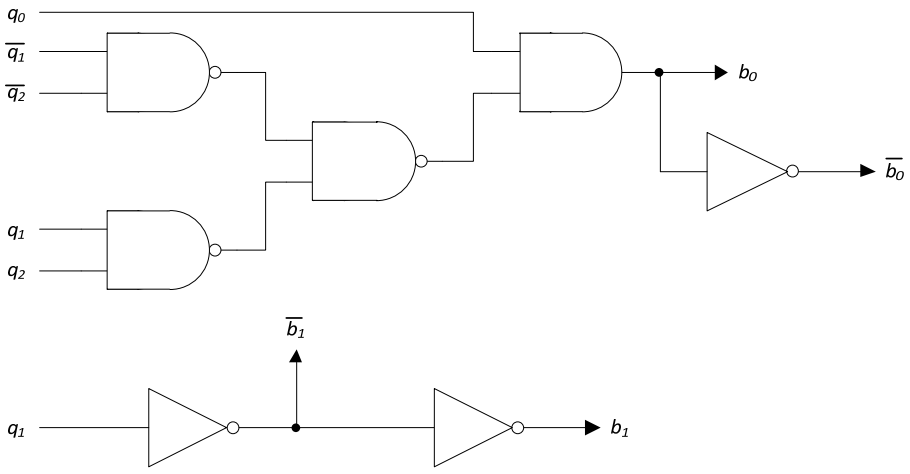


Figure 3.2.2.2 – Logic circuit used for this encoder

3.4 – Synchronization Logic

The synchronization logic is needed because of the pipeline latency. The latency exists because this architecture doesn't make a full conversion at the same instant. The full conversion in this design is done during five clock cycles.

This means that the first stages converted codes need to be stored for more clock cycles than the last stages. This effect is shown in the figure 3.4.1.

ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2
	$B_{9;0}$	…	$B_{9;1}$	…	$B_{9;2}$	…	$B_{9;3}$	…	$B_{9;4}$
		$B_{8;0}$	…	$B_{8;1}$	…	$B_{8;2}$	…	$B_{8;3}$	…
			$B_{7;0}$	…	$B_{7;1}$	…	$B_{7;2}$	…	$B_{7;3}$
				$B_{6;0}$	…	$B_{6;1}$	…	$B_{6;2}$	…
					$B_{5;0}$	…	$B_{5;1}$	…	$B_{5;2}$
						$B_{4;0}$	…	$B_{4;1}$	…
							$B_{3;0}$	…	$B_{3;1}$
								$B_{2;0}$	…
									$B_{1,0;0}$

Figure 3.4.1 – Pipeline output time division

The first clock phase in the previous figure doesn't have any digital output because the first pipeline stage hasn't finished the conversion. Also in the figure above where there is the dot dot dot (or ellipsis) that has one meaning, which is the digital value in the near left column must be stored during this phase.

But the figure above doesn't make an easy way to figure out a synchronization circuit, so rearranging the figure to see the stages output in relation to the clock cycle.

		Stage's output								
		A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	$A_{1,0}$
Clock cycle	ϕ_2	$B_{9;0}$								
	ϕ_1		$B_{8;0}$							
	ϕ_2	$B_{9;1}$		$B_{7;0}$						
	ϕ_1		$B_{8;1}$		$B_{6;0}$					
	ϕ_2	$B_{9;2}$		$B_{7;1}$		$B_{5;0}$				
	ϕ_1		$B_{8;2}$		$B_{6;1}$		$B_{4;0}$			
	ϕ_2	$B_{9;3}$		$B_{7;2}$		$B_{5;1}$		$B_{3;0}$		
	ϕ_1		$B_{8;3}$		$B_{6;2}$		$B_{4;1}$		$B_{2;0}$	
	ϕ_2	$B_{9;4}$		$B_{7;3}$		$B_{5;2}$		$B_{3;1}$		$B_{1,0;0}$
	ϕ_1		$B_{8;4}$		$B_{6;3}$		$B_{4;2}$		$B_{2;1}$	

Figure 3.4.2 – Stage's output in time

In the above figure the clock cycle when the pipeline finishes making a conversion of a sample zero (painted in a light grey) is shown with a black background.

The synchronization circuit is made with the use of D flip-flop. But the question in the design of this circuit is the number of the flip-flops needed by stage. This number is found in the figure 3.4.2 and looking at the stage's sample number at the instant ϕ_2 painted in black.

Table 3.4.1 – Number of flip-flops needed per stage

Stage number	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	$A_{1,0}$
Number of flip-flops	4	3	3	2	2	1	1	0	0

So looking at the table 3.4.1 the number of flip-flops needed for the synchronization logic to fully work is sixteen.

3.5 – Digital Correction Logic

The digital correction can also be called digital redundancy because of the extra bit that each one of the pipeline stage has to convert. The principle behind this block of the system was previously discussed in the chapter 2.

The analog part of this sub-system is included in the 1,5-bit Flash ADC present in each stage. The output of those ADCs will pass thru the synchronization logic to arrive at the same time in the digital domain of this technique.

The basic structure of this technique is the full adder with two one bit inputs and a one bit output with a carry. To fully employ this system it is necessary nine of these basic elements.

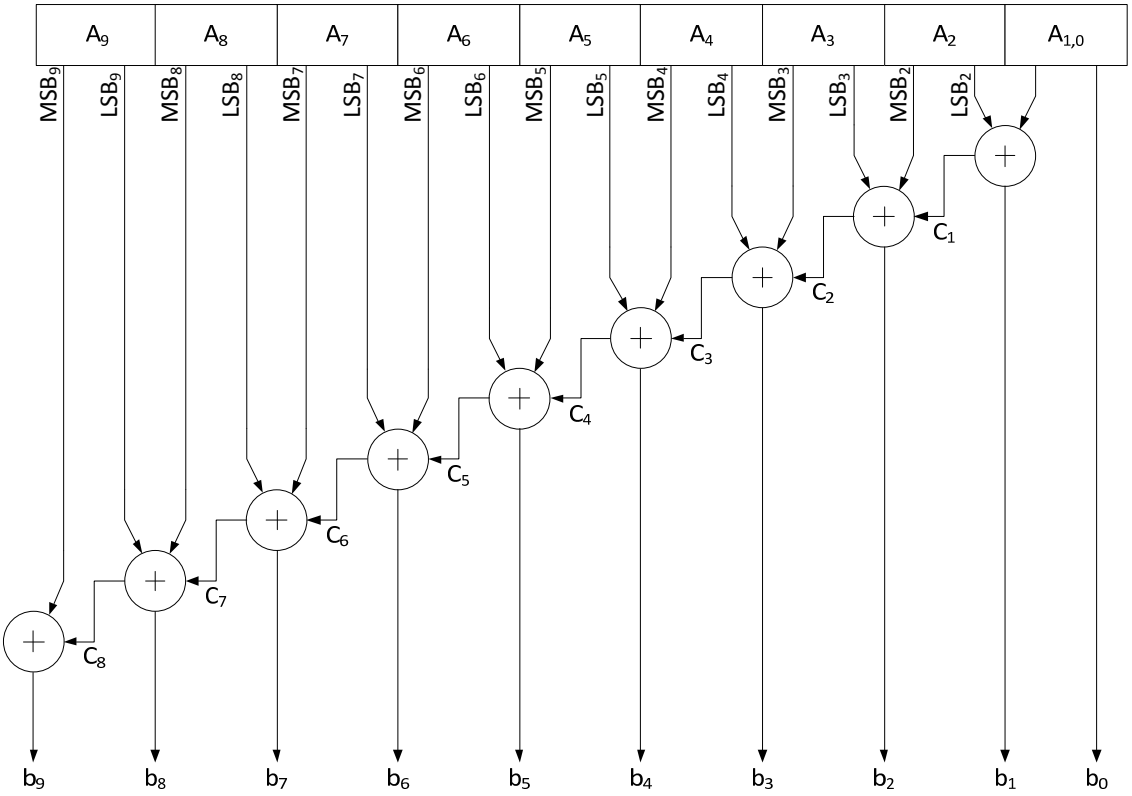


Figure 3.5.1 – Digital Correction Logic digital domain

3.6 – Simulations Results

The simulation presented in this section is related to the implementation of the traditional MDAC approach.

The traditional approach 40MS/s simulation will be used to verify the behavior of the proposed MDAC circuit.

The traditional 10-bit pipeline ADC was implemented using a 0.13 μm CMOS technology from UMC and simulated using Spectre. The ADC was simulated using transient analysis and for an input sine wave signal with amplitude -1 % of the full-scale and a frequency value of 1 MHz.

The implemented MDACs use an electrical model for the amplifiers with a single dominant pole with a DC gain of 65 dB and a gain-bandwidth product (GBW) of 1GHz. All other elements in both pipeline ADCs are made with real devices, including logic circuits, clock-phase generation circuitry and switches. All switches in the signal path employ the previously discussed clock boosting techniques in order to reduce the signal distortion. All capacitors used have a nominal capacitance value of 1 pF. The V_{CM} voltage is set to 0,6 V and the differential reference voltage of the ADC ($\Delta V_{Ref} = V_{Ref}^{+} - V_{Ref}^{-}$) is set to 0,4 V. In the case of the ADC employing the traditional MDAC the differential reference voltage is obtained through two single-ended reference voltages of 0,4 V (V_{Ref}^{-}) and 0,8 V (V_{Ref}^{+}).

The output spectra of the traditional pipeline ADC is depicted in Figure 3.6.1. And from this spectra the performance parameters were calculated, and are summarized in Table 3.6.1.

Table 3.6.1 – Simulated ADCs design performance at $F_S = 40\ MS/s$

	SNR	THD	SFDR	SNDR	ENOB
Traditional MDAC	64,098	-66,056	73,091	61,958	9,9996

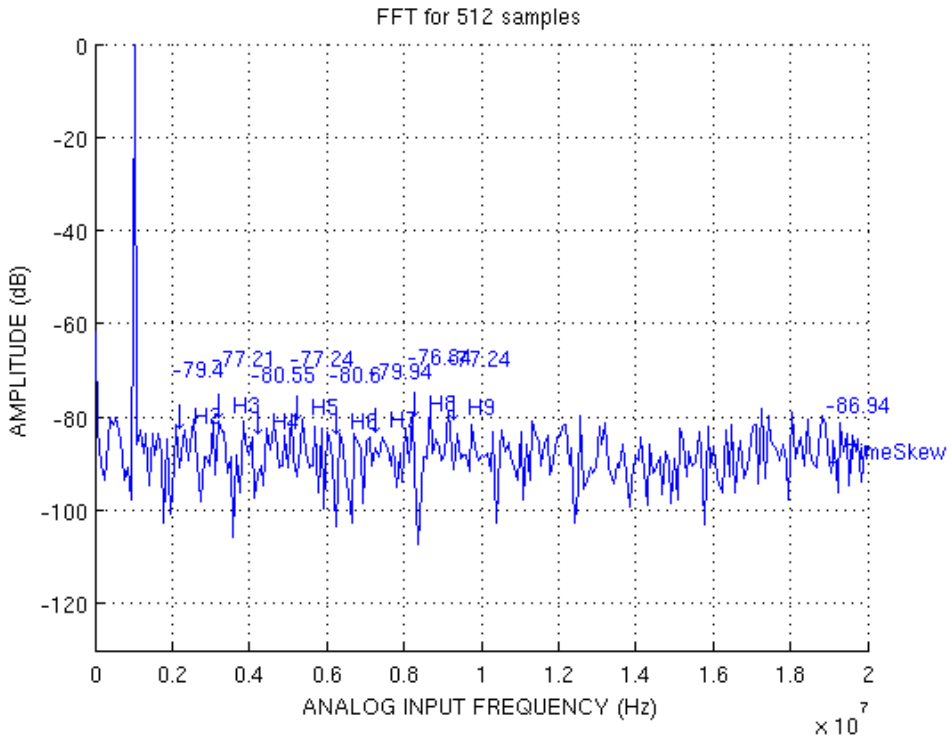


Figure 3.6.1 – Traditional ADC design output spectrum at $F_S = 40MS/s$

Another important aspect is the power dissipation of the reference generation circuit. The results are shown in the Table 3.6.2.

Table 3.6.2 – Power dissipation of the reference circuitry at $F_S = 40MS/s$

	Traditional MDAC		
	V_{Ref}^{+}	V_{Ref}^{-}	Total
Power	383 μW	195,5 μW	578,5 μW

In the case of the ADC using the traditional MDAC circuit, the reference voltage sources (V_{Ref}^{+} and V_{Ref}^{-}) supply a total power of 578,5 μW to the ADC. However, when analyzing these results it is necessary to take into account that the reference voltage sources used in the traditional MDAC are, in fact, built using reference buffer circuits. These circuits are normally difficult to design, since they must have a very high bandwidth (GBW) in order to guarantee that the reference voltage can settle to a value better than $\pm$ 0,25 V_{LSB} @ 10-bit of the ideal value within the available sampling time (which is less than 12,5 ns at $F_S = 40MS/s$) This means that the reference buffers will dissipate more power than the power they supply to the ADC. When the reference voltages are decoupled on-chip, the extra power dissipated by the reference buffers is normally of the order of (up to) 30% of the total power of the ADC.

4 – Proposed Pipeline ADC Architecture

In recent years, high-speed medium resolution analog-to-digital converters (ADC) have reduced their power consumption to enhance their use in portable applications. In these portable applications we have wide range of uses like data communication (mobile phones, 802.11 and 802.16 networks) and image signal processing.

This reduction of the whole system power consumption is achieved by the hardware designer with implementation of a System-On-Chip (SOC), and with this tends to grow the number of bonding wires connected to the chip. A problem with the bonding wires is that they introduce extra noise to the circuit. This noise is related to the working frequency of the circuit.

The approach presented in this thesis tries to overcome the bonding wire effects without making a power consumption compromise.

4.1 – Overview of High-Frequency Problems in Pipeline ADC

In today's systems, bond wires are used to connect the SOC's to the outside world by the way of the interconnect circuitry. There are several side effects while using bond wires: such as high impedance bond wires will provoke inductive discontinuities, which will result in impedance mismatches and unwanted signal reflections.

With the trend of further shrinking the scale of the semiconductors technology, the number of circuits that can be incorporated in a single SOC is rising, because each of these circuits are requiring less area [20].

Since normally each of the SOC's circuits have input and output ports, so increasing the number of these circuits in the SOC will also increase the number of SOC's I/O ports. Because normally the SOC's size does not increase this also means that its perimeter stays the same. And it's at the perimeter that the SOC's I/O ports will be located.

With the increase number to be implemented in the same SOC perimeter, this will cause the pad pitch to be forcibly reduced for the SOC to accumulate all the needed I/O ports.

With the trend of miniaturization there was an advance in the integration density, but there were also technological advances in speed and bandwidth of systems and multi-chip interconnections inside the SOC [21] [22] [23]. One example of this trend is the Moore's law, which describes the long term trend in the history of computing hardware and says that the number of transistors that can be placed inexpensively on an integrated circuit has double approximately every two years. [26] [27]

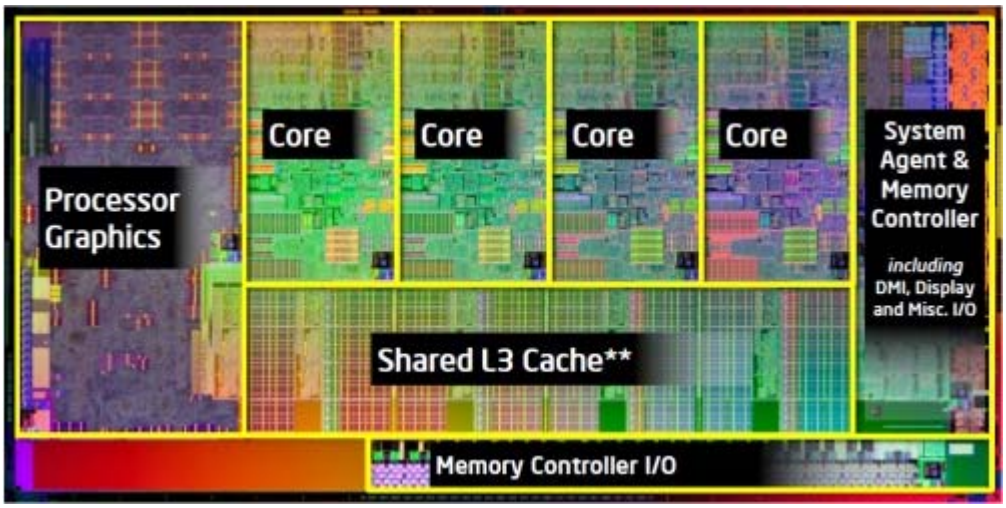


Figure 4.1.2 – Example of a System-On-Chip

Depending on the system in question many approaches can be made to try and solve the bond wire problem, for example, this thesis will try to use a physical effect on the capacitors of the MDAC to avoid the use of reference voltages bond wires in that structure. But for example if the problem is a high speed connection between two chips that cannot be incorporated in the same package there were some advances made in the year 2010 using optoelectronics. [28]

When the working operation of a system falls into the classification of high-frequency, the wire bonding effect is one of the dominant parasitic effects in all of the system and not only on some part of it (like the parasitic elements of CMOS switch). The common approach to this is to take this effect in consideration from the beginning of the circuit design, with the irony of the wire bonding being one of the last processes of the device fabrication [24].

Knowing that the bonding wire is highly inductive in most of the frequency range (from 0 to 100GHz) and its quality factor is determined/limited by the ohmic loss [25] the proposed electrical mode for the wire bond is given by the Figure 4.1.2.

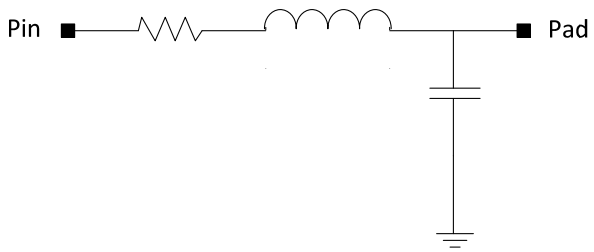


Figure 4.1.2 – Bond wire electrical model

Regarding the pipeline ADC the wire bonding parasitic effects can affect the circuit in two ways: by the reference voltages and by the power supply. Both of this ways can be classified by direct or indirect working effect, regarding the changes to the mathematical model.

Since the output in the MDAC is a class A circuit, its current is DC and therefore it is not affected by the bond wire inductance present in the power supply.

But the same doesn't happen with the wire bonding parasitic effect affecting the reference voltage, because it affects directly the MDAC circuit and by this means the mathematical model expression, so this is a direct effect.

This direct effect is the main concern of this thesis since resonance effect produced in the RLC network of the wire bond will be the major noise source of the circuit. This is true if the OPAMP are extremely well designed to withstand the RLC effects in its power supply.

This new noise source will take the pipeline ADC to its limits regarding the SNDR and consequently the ADC's ENOB. What this thesis proposes is a way to emulate with high precision value the reference voltages in the MDAC using a simple current injection.

4.2 – Principle behind the new architecture

The basics behind this new approach are the injection of a determined value of current in the MDAC's feedback capacitor to emulate the effect of a reference voltage in the charges of the switched-capacitor circuit.

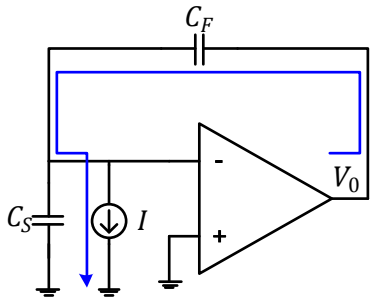


Figure 4.2.1 – Injected current "trajectory"

For obtaining the theoretical value of current needed to proper emulate the reference voltage, the designer has to star from the capacitor current-voltage relation, and from this comes the time dependent and also capacitor dependent current variable:

$$v(t) = \frac{q(t)}{C} = \frac{1}{C}\int_0^t i(\tau)\, d\tau + v(0) \tag{4.2.1}$$

Considering that the capacitor has no initial voltage, and the inject current is always constant, them the equation (4.2.1) transforms to:

$$v(t) = \frac{1}{C}\int_0^t I\, d\tau = \frac{1}{C}[I.\tau]_0^t = \frac{I.t}{C} \tag{4.2.2}$$

Knowing that $v(T)$ has to be equal to V_{Ref}, from equation (4.2.2) the current needed to inject is:

$$I = \frac{C.V_{Ref}}{T} \tag{4.2.3}$$

One of the problems that will be reviewed in following sections is what is the value of C in the equation (.4.2.3). Because like it has a component of the MDAC feedback capacitor but also a component of the parasitic elements associated to the terminals nodes of that capacitor.

4.3 – The Current Switched MDAC

The CSMDAC will be implemented by using the $-\frac{V_{Ref}}{4} < V_{in} < \frac{V_{Ref}}{4}$ electrical configuration of the traditional MDAC and extracting current from one of the input of the AMPOP. This implementation is represented in the figure 4.3.1.

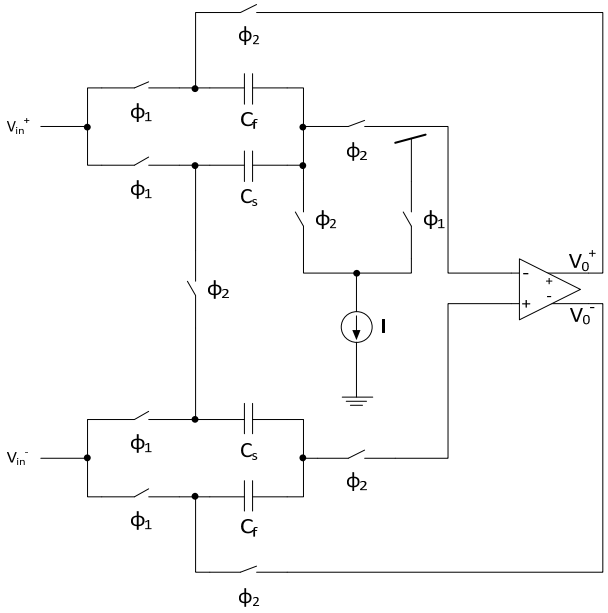


Figure 4.3.1 – Implementation of a CSMDAC's injection zone

Extracting the charge equations of the capacitors of the figure 4.3.1:

$$\begin{cases}(C_1 + C_2).V_{in}^{+} = (V_{SC} - V^{-}).C_1 + (V_0^{+} - V^{-}).C_2 - I.T \\ (C_3 + C_4).V_{in}^{-} = (V_{SC} - V^{+}).C_3 + (V_0^{-} - V^{+}).C_4 \end{cases} \quad (4.3.1)$$

Where V_{SC} is the short circuit node voltage during the phase ϕ_2.

Solving the equation (4.3.1) in terms of ΔV_0 and making $C_1 = C_3$ and $C_2 = C_4$:

$$\begin{cases} V_0^{+} = \frac{C_1 + C_2}{C_2}.V_{in}^{+} - \frac{C_1}{C_2}.V_{SC} + \frac{C_1 + C_2}{C_2}.V^{-} + \frac{I.T}{C_2} \\ V_0^{-} = \frac{C_1 + C_2}{C_2}.V_{in}^{-} - \frac{C_1}{C_2}.V_{SC} + \frac{C_1 + C_2}{C_2}.V^{+} \end{cases} \quad (4.3.2)$$

Transforming the equation (4.3.2) and $V^{+} = \frac{V_0^{-}}{A}$ and $V^{-} = \frac{V_0^{+}}{A}$:

$$\Delta V_0 = \frac{C_1 + C_2}{C_2}.\Delta V_{in} + \frac{C_1 + C_2}{C_2}.\frac{\Delta V_0}{A} + \frac{I.T}{C_2} \quad (4.3.3)$$

Where $\frac{I.T}{C_2} = V_{Ref}$ in equation (4.3.3).

The equation (4.3.3) represent the situation when $\Delta V_{in} < -\frac{V_{Ref}}{4}$. For the system to do the situation $\Delta V_{in} > +\frac{V_{Ref}}{4}$ it is only necessary to inject current in the other feedback capacitor of the MDAC, and then the equation (4.3.3) would change to:

$$\Delta V_0 = \frac{C_1 + C_2}{C_2}.\Delta V_{in} + \frac{C_1 + C_2}{C_2}.\frac{\Delta V_0}{A} - \frac{I.T}{C_2} \qquad (4.3.4)$$

4.3.1 – Circuit

From the equation (4.3.3) and (4.3.4) the designer knows where to inject current for proper emulating the reference voltage effects. The multiply by two zone is done by only short circuiting and by not injecting current of the switched capacitor network.

The proposed 1,5-bit MDAC stage is represented by the figure 4.3.1.1.

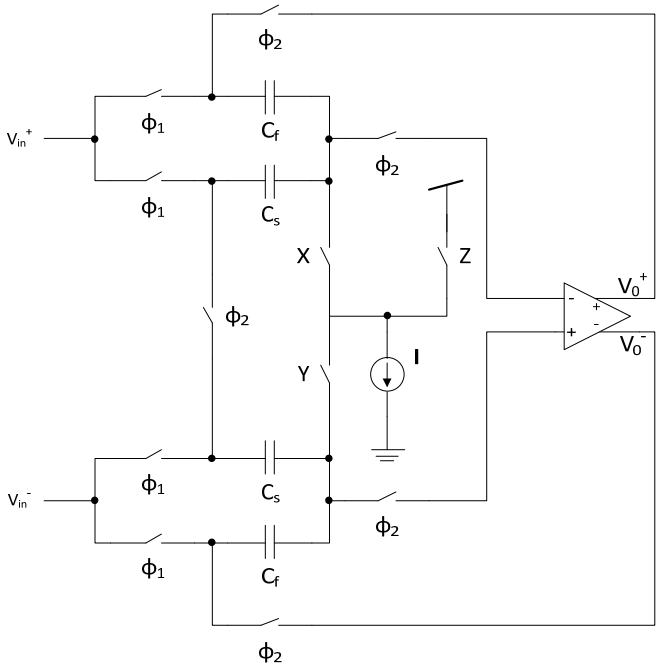


Figure 4.3.1.1 – Proposed 1,5-bit MDAC stage

Like the traditional MDAC the output of the 1,5-bit Flash ADC will tell the circuit which is the node to inject current, or if it is needed to inject current.

4.3.2 – Comparison between the OPAMP requirements in this new MDAC and the standard MDAC

In a previous section it was discussed the OPAMP requirements regarding ADC resolution. The proposed architecture introduces a new requirement: the common gain of the OPAMP.

The OPAMP's output can be written as:

$$V_0 = A_{open-loop}.(V^+ - V^-) + \frac{1}{2}A_{common-mode}.(V^+ + V^-) \quad (4.3.2.1)$$

The effect discussed in here is caused by an irregular value of voltage in one of the OPAMP's input terminal. So rearranging the previous equation:

$$V_0 - \left(\frac{1}{2}A_{common-mode} + A_{open-loop}\right).V^+ = \left(\frac{1}{2}A_{common-mode} - A_{open-loop}\right).V^-$$
$$\Leftrightarrow V^- = \frac{2}{A_{common-mode} - 2.A_{open-loop}}V_0 - \frac{A_{common-mode} + 2.A_{open-loop}}{A_{common-mode} - 2.A_{open-loop}}V^+ \quad (4.3.2.2)$$

Ideally the common mode gain is zero but in a real OPAMP the common mode gain, so some of the other OPAMP's input terminal voltage will be present in the current injector node.

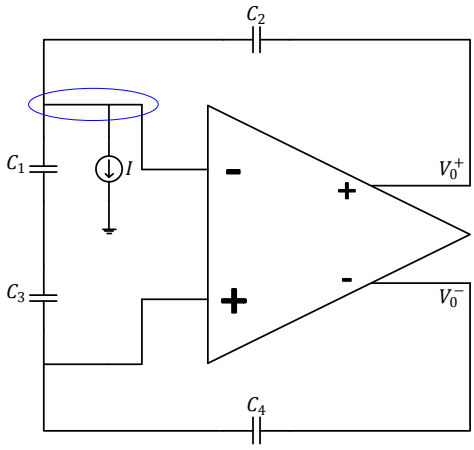


Figure 4.3.2.1 – Proposed 1,5-bit MDAC stage during amplification phase

Since the injector circuit isn't an ideal current source, a variation in the injector node voltage will change the current value being injected.

Although it is impossible to make the injector circuit insensitive to the voltage variations it is necessary to design this circuit to be as insensitive as possible.

Another requirement introduced by this technique can be obtained considering the OPAMP a simple differential pair with propose of a simple analysis of this problem, like the one represented in the figure 4.3.2.2.

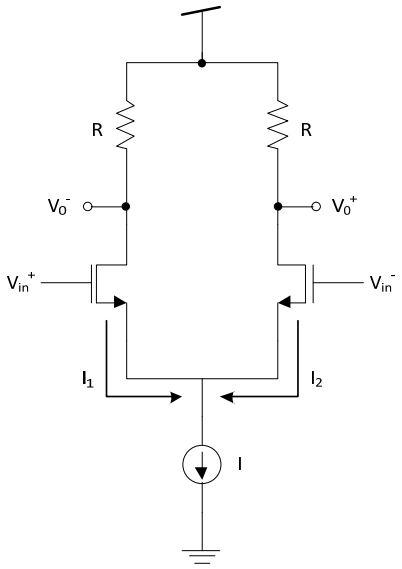


Figure 4.3.2.2 – Simple differential pair

Where:

$$\begin{cases} V_0^+ = V_{DD} - R.I_2 \\ V_0^- = V_{DD} - R.I_1 \end{cases} \quad (4.3.2.3)$$

And:

$$I = I_1 + I_2 \quad (4.3.2.4)$$

If the differential pair inputs are the same, then:

$$I_1 = I_2 = \frac{I}{2} \quad \Rightarrow \quad \begin{cases} V_0^+ = V_{DD} - R\frac{I}{2} \\ V_0^- = V_{DD} - R\frac{I}{2} \end{cases} \quad (4.3.2.5)$$

The problem occurs when the OPAMP inputs do not have the same voltage value and current is being injected in the switched-capacitor circuit. To the OPAMP with a differential pair representation what he senses of the outside world is the figure 4.3.2.3.

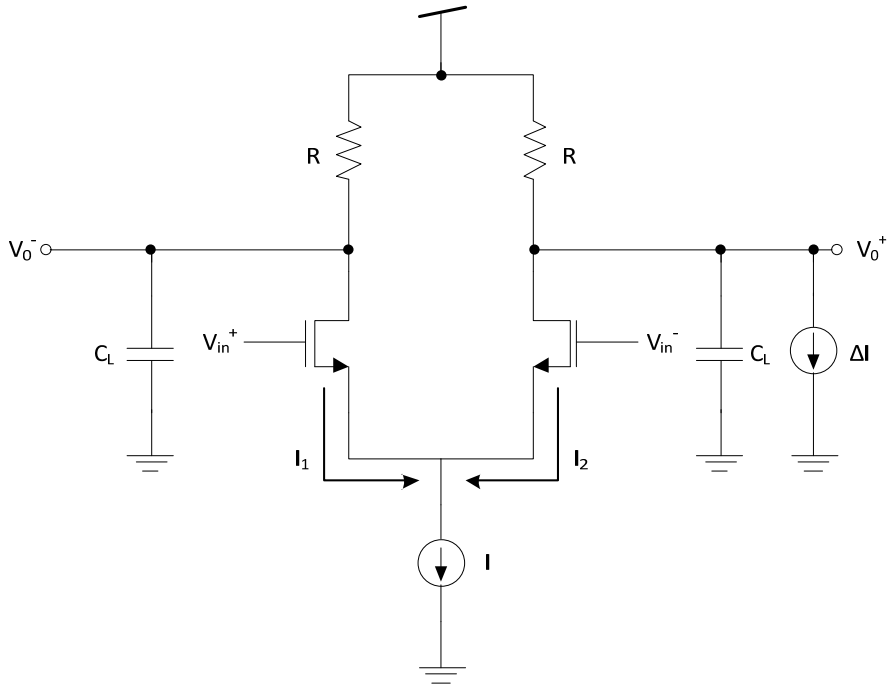


Figure 4.3.2.3 – Simple representation of the problem

Considering that the OPAMP output load is zero to simplify the analysis, when the current is being injected in the circuit the OPAMP outputs with this representation are:

$$\begin{cases} V_0^+ = V_{DD} - R.(I_2 + \Delta I) \\ V_0^- = V_{DD} - R.I_1 \end{cases} \quad (4.3.2.6)$$

In the figure 4.3.2.3 and in the equation (4.3.2.6) the current source ΔI represents the current being injected into the switched capacitor network. The current is being pulled from the OPAMP V_{DD} power supply connection and sinking in the injector circuit, like it is represented on the figure 4.3.2.4 in the single ended form with the current “trajectory” in blue.

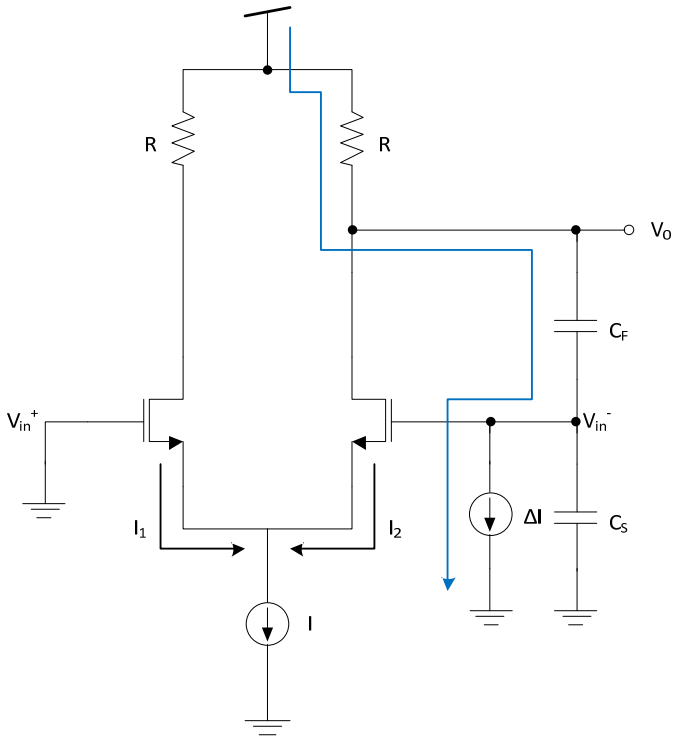


Figure 4.3.2.4 – Single-ended representation

The equation (4.3.2.6) reflects the OPAMP output that is the MDAC output and consequently will be the next stage input. The problem is that one of the output nodes will have a lower voltage than the expected by the next stage (the expected voltage for V_0^+ is $V_{DD} - R.I_2$), this introduces an error that will be propagated by the pipeline and if the current injection occurs again it will introduce more error at the output of that stage.

A solution for this error is reducing the current injection period to allow the OPAMP output nodes to recover to the correct output voltage. The reducing of the current injection period has another benefits discussed later in this thesis. This introduces a new variable in optimizing the OPAMP that is the slew rate, since the slew rate needs to be inferior to the period between the ending of current injection and the amplifying phase.

4.4 – The injected current error effects

Ideally the transfer function of a single stage in a pipeline ADC is:

$$V_0 = \begin{cases} 2.V_{in} + V_{ref}, & V_{in} < -\dfrac{V_{ref}}{4} \\ 2.V_{in}\ , & -\dfrac{V_{ref}}{4} \le V_{in} \le \dfrac{V_{ref}}{4} \\ 2.V_{in} - V_{ref}, & V_{in} > \dfrac{V_{ref}}{4} \end{cases} \tag{4.4.1}$$

The V_{ref} is generated by the current injection and has two components:

$$V_{ref_{generated}} = V_{ref} \pm V_{ref_{error}} \tag{4.4.2}$$

To easy the starting analysis it will be considered the case where $V_{in} > \frac{V_{ref}}{4}$, so has result of the first pipeline stage:

$$\begin{aligned} V_0^{[1]} &= 2.V_{in} - V_{ref_{generated}} = 2.V_{in} - \left(V_{ref} \pm V_{ref_{error}}\right) \\ &= 2.V_{in} - V_{ref} \mp V_{ref_{error}} \end{aligned} \tag{4.4.3}$$

A condition for this analysis to be valid is:

$$2.V_{in} - V_{ref} \mp V_{ref_{error}} > \frac{V_{ref}}{4} \tag{4.4.4}$$

And this means that the result of the second pipeline stage is:

$$\begin{aligned} V_0^{[2]} &= 2.V_0^{[1]} - V_{ref_{generated}} = 2.\left(2.V_{in} - V_{ref} \mp V_{ref_{error}}\right) - V_{ref} \mp V_{ref_{error}} \\ &= 4.V_{in} - 3.V_{ref} \mp 3.V_{ref_{error}} \end{aligned} \tag{4.4.5}$$

Considering that equation (4.4.5) is always superior to $\frac{V_{ref}}{4}$, The output of the third pipeline stage is:

$$\begin{aligned} V_0^{[3]} &= 2.V_0^{[3]} - V_{ref_{generated}} = 2.\left(4.V_{in} - 3.V_{ref} \mp 3.V_{ref_{error}}\right) - V_{ref} \mp V_{ref_{error}} \\ &= 8.V_{in} - 7.V_{ref} \mp 7.V_{ref_{error}} \end{aligned} \tag{4.4.6}$$

Making a prediction for the output of the n pipeline stage using the equations (4.4.3) (4.4.5) (4.4.6):

$$V_0^{[n]} = \begin{cases} 2.V_{in} - V_{ref} \mp V_{ref_{error}}, & if\ n = 1 \\ 2^n.V_0^{[n-1)} + (2^n - 1)\left(V_{ref} \pm V_{ref_{error}}\right), & if\ (n > 1) \wedge \left(V_0^{[n-1]} < -\frac{V_{ref}}{4}\right) \\ 2^n.V_0^{[n-1)}, & if\ (n > 1) \wedge \left(-\frac{V_{ref}}{4} < V_0^{[n-1]} < \frac{V_{ref}}{4}\right) \\ 2^n.V_0^{[n-1)} - (2^n - 1)\left(V_{ref} \pm V_{ref_{error}}\right), & if\ (n > 1) \wedge \left(V_0^{[n-1]} > \frac{V_{ref}}{4}\right) \end{cases} \quad (4.4.7)$$

Since $V_{ref_{error}}$ can be related to V_{ref} in a certain percentage:

$$P_{error} = \frac{V_{ref_{error}}}{V_{ref}} \Longrightarrow V_{ref_{error}} = P_{error}.V_{ref} \quad (4.4.8)$$

Using the equation (4.4.8) to transform the equations (4.4.7):

$$V_0^{[n]} = \begin{cases} 2.V_{in} - (1 \pm P_{error})V_{ref}, & n = 1 \\ 2^n.V_0^{[n-1)} + (2^n - 1)(1 \pm P_{error})V_{ref}, & (n > 1) \wedge \left(V_0^{[n-1]} < -\frac{V_{ref}}{4}\right) \\ 2^n.V_0^{[n-1)}, & (n > 1) \wedge \left(-\frac{V_{ref}}{4} < V_0^{[n-1]} < \frac{V_{ref}}{4}\right) \\ 2^n.V_0^{[n-1)} - (2^n - 1)(1 \pm P_{error})V_{ref}, & (n > 1) \wedge \left(V_0^{[n-1]} > \frac{V_{ref}}{4}\right) \end{cases} \quad (4.4.9)$$

The reference voltage generated by the injected current is given by:

$$V_{ref} = \frac{I.T}{C} \quad (4.4.10)$$

The equation system (4.4.9) can be transformed into:

$$V_0^{[n]} = \begin{cases} 2.V_{in} - (1 \pm P_{error})\frac{I.T}{C}, & n = 1 \\ 2^n.V_0^{[n-1)} + (2^n - 1)(1 \pm P_{error})\frac{I.T}{C}, & (n > 1) \wedge \left(V_0^{[n-1]} < -\frac{V_{ref}}{4}\right) \\ 2^n.V_0^{[n-1)}, & (n > 1) \wedge \left(-\frac{V_{ref}}{4} < V_0^{[n-1]} < \frac{V_{ref}}{4}\right) \\ 2^n.V_0^{[n-1)} - (2^n - 1)(1 \pm P_{error})\frac{I.T}{C}, & (n > 1) \wedge \left(V_0^{[n-1]} > \frac{V_{ref}}{4}\right) \end{cases} \quad (4.4.11)$$

Considering that in the previous equation the only source of error is the current source, meaning that the P_{error} factor is directly related with the injected current value.

A problem will show up if the P_{error} if large enough to cause the value of $V_0^{[n]}$ to have a difference between the wanted value and the obtained value larger than a V_{LSB}, because if this happens, the error will propagate from the initial stage to the last stage of the Pipeline ADC.

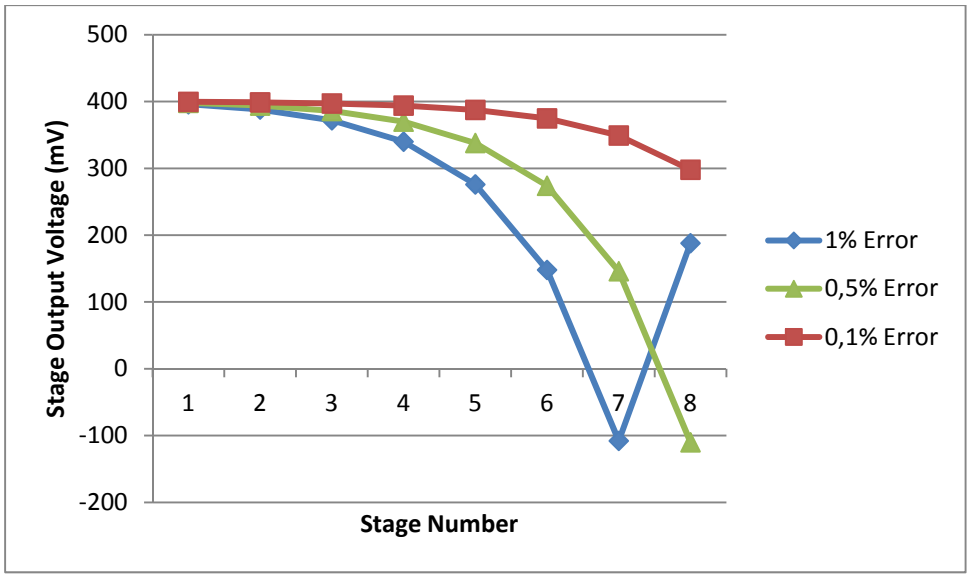


Figure 4.4.1 – CSMDAC Stage Output with an error in the reference

The figure 4.4.1 was obtained using the equation system (4.4.11) that models the output of a current based MDAC with a current error. Looking only at the stage output it is not easy to understand the necessary value of current error value needed for being able to use this technique in a high resolution Pipeline ADC.

To better understand the impact in the performance of the pipeline ADC using the current injection technique, a high level model was developed. This model uses the equation system (4.4.11) to calculate the voltage produced by each MDAC stage in the pipeline ADC. The following two figures use the referred model with the different values for the ADC input signal amplitude.

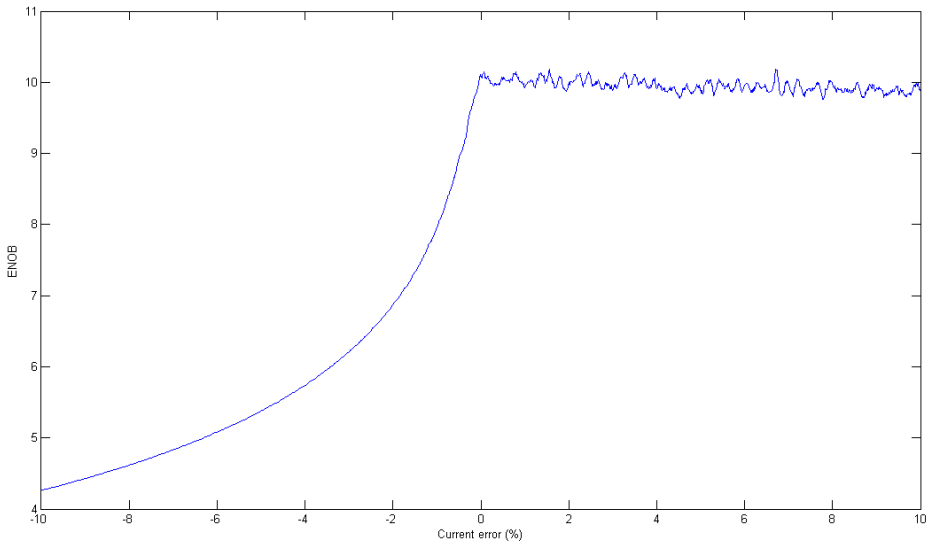


Figure 4.4.2 – ENOB of a current based system with a current error and a full scale input signal

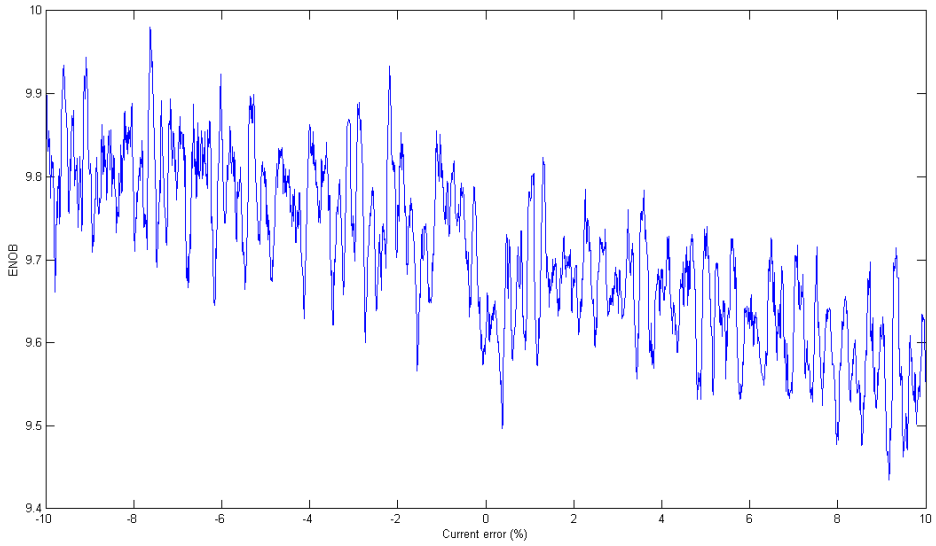


Figure 4.4.3 – ENOB of a current based system with a current error and an 80% full scale input signal

Looking at the simulation of a system with a full-scale signal it expected to see a degradation of the ENOB as an exponential function with an asymptote at an ENOB equal to four. Inserting extra current by this model does not degrade the ENOB of the system, but this is not true because of the charge injection of the feedback switch. The extra current will provoke an extra decrease of the stage output voltage.

Since the ADCs are commonly tested with an input signal close to the full-scale signal, doing a graphical analysis of the figure 4.4.3, it is possible to say that with an eighty percent full-scale signal the current error effects are most imperceptible.

Considering a variable current error using a random number generator based on normal distribution for simulating the ENOB in systems with the type of error previously discussed.

Table 4.4.1 – ENOB of symmetric current errors systems

Amplitude of the input signal	μ	σ
80% of the full-scale	9.641	0.056027
100% of the full-scale	10,034	0.052496

Another problem that might rise in this type of approach is the value of injected current is not the same value in the current based MDAC. The MDAC with this type of error as the following transfer function:

$$V_0 = \begin{cases} 2.V_{in} + \frac{(1+P_{error}).I.T}{C}, & V_{in} < -\frac{V_{ref}}{4} \\ 2.V_{in}\ , & -\frac{V_{ref}}{4} \leq V_{in} \leq \frac{V_{ref}}{4} \\ 2.V_{in} - \frac{I.T}{C}, & V_{in} > \frac{V_{ref}}{4} \end{cases} \quad \text{or} \quad V_0 = \begin{cases} 2.V_{in} + \frac{I.T}{C}, & V_{in} < -\frac{V_{ref}}{4} \\ 2.V_{in}\ , & -\frac{V_{ref}}{4} \leq V_{in} \leq \frac{V_{ref}}{4} \\ 2.V_{in} - \frac{(1+P_{error}).I.T}{C}, & V_{in} > \frac{V_{ref}}{4} \end{cases}$$

(4.4.12)

To see the effects of an asymmetric current error in a current based MDAC present in an ideal 10-bit pipeline ADC, a pipeline ADC model with the same resolution was made having the equation system (4.4.12) as a mathematical representation of the MDAC present in each stage of the pipeline. This model will be useful to find how this type of error affects the ENOB of systems with the proposed technique. The following two figures use the referred model with the difference being two different values for the ADC input signal amplitude.

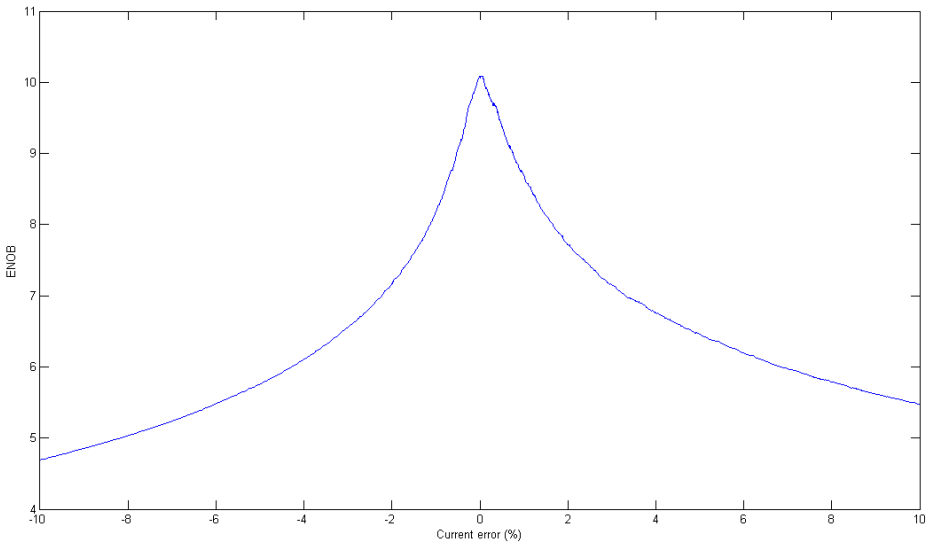


Figure 4.4.4 – ENOB of a current based system with a current error and a full scale input signal

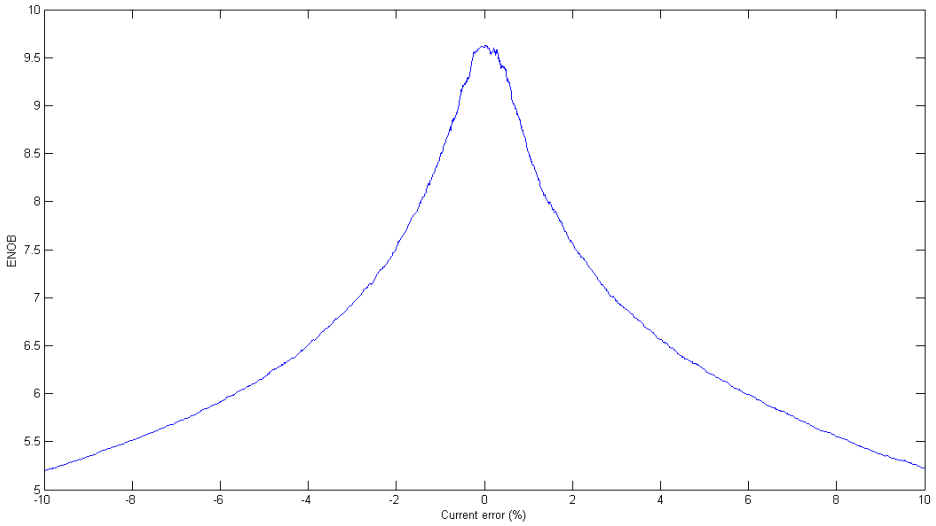


Figure 4.4.5 – ENOB of a current based system with a current error and an 80% full scale input signal

Looking at both simulations of a system it is expected to see a degradation of the ENOB as an exponential function with an asymptote at an ENOB equal to four, this occurs if the system is not injecting sufficient current or injecting extra current.

Looking at both simulations the value of ENOB with a maximum value of current error of one percent is eight. Since the modern manufacturing processes permit an approximated accuracy of ninety nine percent, this means that a system with this type of asymmetric error can achieve a minimum value for ENOB characteristic of eight effective bits.

Considering a variable asymmetric current error using a random number generator based on normal distribution for simulating the ENOB in systems with this type of error.

Table 4.4.2 – ENOB of asymmetric current errors systems

Amplitude of the input signal	μ	σ
80% of the full-scale	9,2249	0,34401
100% of the full-scale	9,3723	0,43684

With this data it is possible to conclude that with an accurate value for current and with digital correction logic it is possible to overcome the asymmetric current error without the need of additional structures or techniques, proving that this approach can be viable for a practical use.

4.5 – Implementation of the new Pipeline ADC

The implementation of this new architecture was only done after the traditional pipeline implementation, and with several more steps. The reason for this is that the traditional MDAC will be the base for the new one, making it possible to do a direct comparison between the traditional and the new implementation.

It is in high frequency that the bond wire effects are seen. So the proposed architecture has to be capable of high frequency and high resolution operation.

4.5.1 – The changes to the traditional MDAC

The basic objective of this architecture is to reduce to the minimum possible the interaction of the MDAC structure with the outside world. To start working on this concept it's better to look at the ideal MDAC's transfer function.

$$\begin{cases} \Delta V_0 = 2.\Delta V_{in} + \Delta V_{Ref}, & if\ \Delta V_{in} < -\dfrac{\Delta V_{Ref}}{4} \\ \Delta V_0 = 2.\Delta V_{in}, & if\ -\dfrac{\Delta V_{Ref}}{4} \geq \Delta V_{in} \leq +\dfrac{\Delta V_{Ref}}{4} \\ \Delta V_0 = 2.\Delta V_{in} - \Delta V_{Ref}, & if\ \Delta V_{in} > +\dfrac{\Delta V_{Ref}}{4} \end{cases} \quad (4.5.1.1)$$

Since ΔV_{Ref} will be emulated by the injection of current in the switched capacitor network. The equation (4.5.1.1) can be re-written has:

$$\begin{cases} \Delta V_0 = 2.\Delta V_{in} + \dfrac{I.T}{C}, & if\ \Delta V_{in} < -\dfrac{\Delta V_{Ref}}{4} \\ \Delta V_0 = 2.\Delta V_{in}, & if\ -\dfrac{\Delta V_{Ref}}{4} \geq \Delta V_{in} \leq +\dfrac{\Delta V_{Ref}}{4} \\ \Delta V_0 = 2.\Delta V_{in} - \dfrac{I.T}{C}, & if\ \Delta V_{in} > +\dfrac{\Delta V_{Ref}}{4} \end{cases} \quad (4.5.1.2)$$

In terms of schematic the equation (4.5.1.2) can be achieve by the represented circuit in the figure 4.5.1.1.

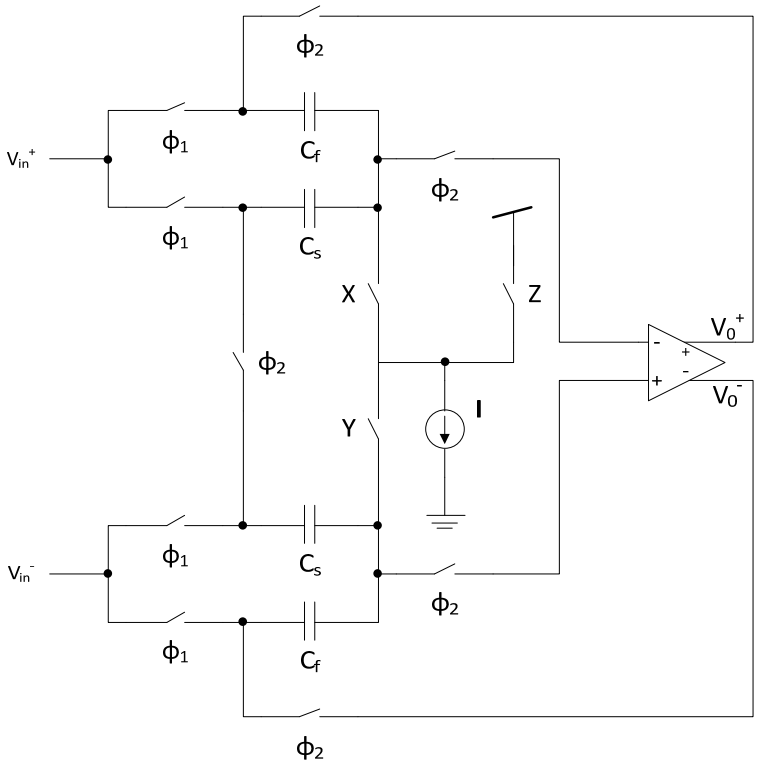


Figure 4.5.1.1 – Proposed 1,5-bit MDAC architecture

So having has a base the traditional MDAC implementation, the only changes to the structure will be introduction of three switches controlling the place where the current will be injected, and the removal of the four switches controlling the reference voltage, maintaining only the switch responsible for short circuiting the switched capacitor network from the traditional structure.

The X, Y, Z switches will control the current injection place. For a proper operation of the injector circuit the Z switch will be on during the sampling phase.

Like in the traditional MDAC's architecture the switch control will respond to the digital output of the 1,5-bit Flash ADC.

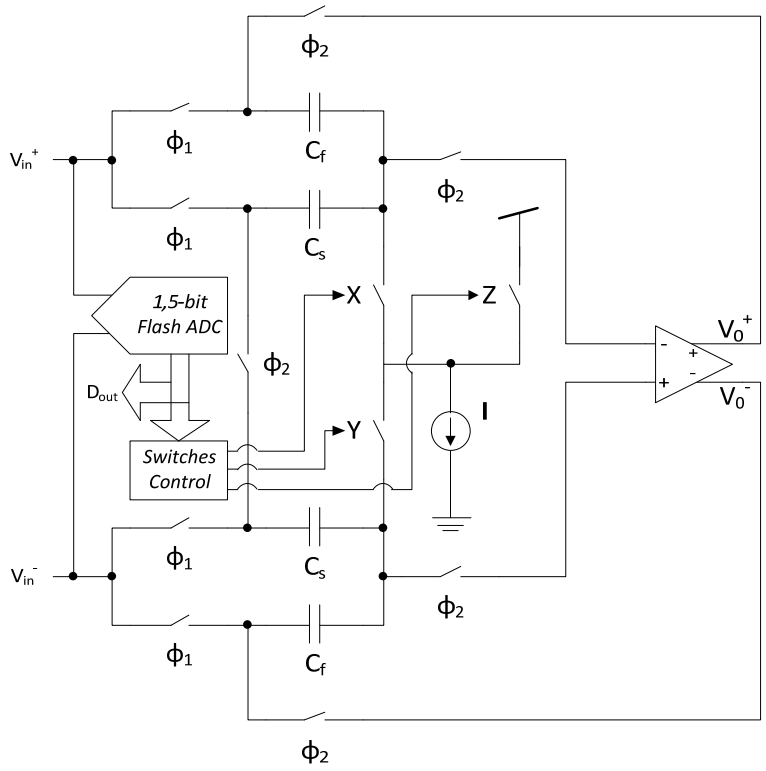


Figure 4.5.1.2 – Proposed 1,5-bit MDAC architecture with the Flash ADC

Like in the implementation of the traditional MDAC the digital thermometer and the X, Y and Z encoder can be assimilated into one structure for simplifying the circuit schematic and because they share the same implicit logic functions.

The best way to explain how the unified ADC with switching works is using the following table.

Table 4.5.1.1 – Relation between the comparator output and its encoding

Differential input ΔV_{in}	Comparator output		MDAC control input			Output code	
	q_1	q_0	X	Y	Z	b_1	b_0
$\Delta V_{in} < -\frac{\Delta V_{Ref}}{4}$	0	0	0	1	0	0	0
$-\frac{\Delta V_{Ref}}{4} \leq \Delta V_{in} \leq +\frac{\Delta V_{Ref}}{4}$	0	1	0	0	1	0	1
$\Delta V_{in} > +\frac{\Delta V_{Ref}}{4}$	1	1	1	0	0	1	0

The X, Y, Z controls are given by the digital logic represented in the figure 4.5.1.3.

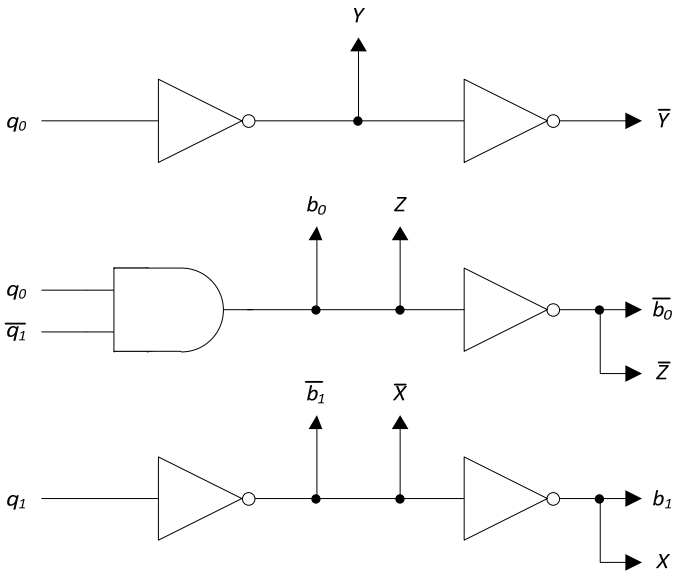


Figure 4.5.1.3 – Unified digital thermometer with switch control

By observing the figure 4.5.1.3 it can be concluded that the switched control for the new approach is the same has the traditional approach. So there isn't needed a redesign of this circuit.

When the current is not being injected in the switched-capacitor circuit the Z switch needs to be in the "on" state. The switch control of figure 4.5.1.3 guarantees that condition only during the amplification phase. For that to be "on" in the sampling phase it is only needed an "Or" logical gate with at its inputs "Z" control signal and the ϕ_1 clock phase.

4.5.2 – The injection of current in the switched capacitor circuit

Like it was previously said the ideal current based MDAC transfer function is:

$$\begin{cases} \Delta V_0 = 2.\Delta V_{in} + \dfrac{I.T}{C}, & if\ \Delta V_{in} < -\dfrac{\Delta V_{Ref}}{4} \\ \Delta V_0 = 2.\Delta V_{in}, & if\ -\dfrac{\Delta V_{Ref}}{4} \geq \Delta V_{in} \leq +\dfrac{\Delta V_{Ref}}{4} \\ \Delta V_0 = 2.\Delta V_{in} - \dfrac{I.T}{C}, & if\ \Delta V_{in} > +\dfrac{\Delta V_{Ref}}{4} \end{cases} \quad (4.5.2.1)$$

But the mathematical expression doesn't tell what happens during the amplification phase. For better explaining what is happening in the circuit, the figure 4.5.2.1 can be used.

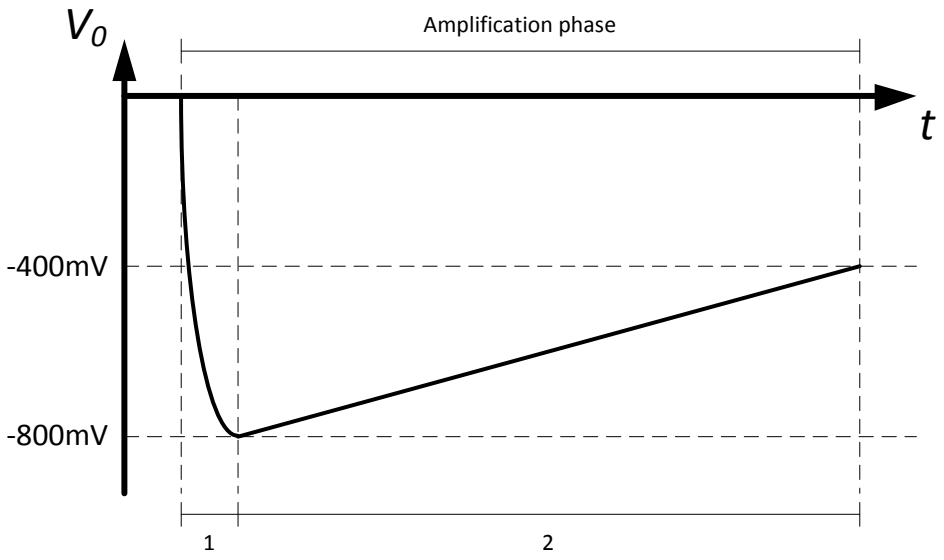


Figure 4.5.2.1 – Ideal time response of current based MDAC

The figure 4.5.2.1 represents the ideal time response of the proposed MDAC architecture. Since the only time when the current is injected in the switched capacitor circuit is during the amplification phase it is only necessary to represent this phase regarding the circuit's time response.

The amplification phase can be divided into two sub-phases by observing the previous figure. The first sub-phase flagged in the figure by the number one represents the normal tendency of the circuit to multiply its inputs by two. This can be explained by only being active the short circuit of the switched capacitor circuit and this means that during this sub-phase the output of the MDAC is:

$$\Delta V_0 = 2.\Delta V_{in} \tag{4.5.2.2}$$

The second sub-phase is the injection of the current in the switched capacitor circuit. Considering that the injected current value stays constant the output of the current based MDAC can be written as:

$$\Delta V_0(t) = 2.\Delta V_{in} \pm \frac{I}{C}t \tag{4.5.2.3}$$

At the end of the amplification phase it is expected that:

$$\Delta V_0 = \Delta V_0(T) = 2.\Delta V_{in} \pm \frac{I.T}{C} \quad (4.5.2.4)$$

Meaning that:

$$\frac{I.T}{C} = \Delta V_{Ref} \quad (4.5.2.5)$$

This is the base of the concept, and model for an ideal world application. But in reality there are two major sources of output error hidden in the operation of the circuit: the channel charge injection and the stability of the OPAMP.

They are hidden because the current is injected along the amplification phase and this mask these two error sources.

The channel charge injection occurs when switches go to off state and/or the current finishes to be injected. This effect is better explained in the annex. The mathematical equation that defines the response of the stage's output with this effect is:

$$\Delta V_0 = 2.\Delta V_{in} \pm \frac{I.T}{C} \pm \frac{Q_{channel}}{C} \quad (4.5.2.6)$$

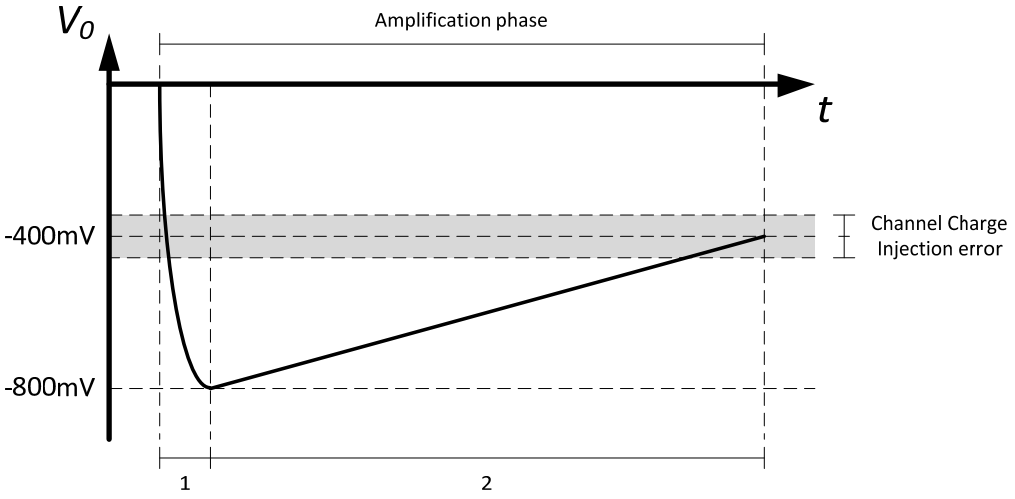


Figure 4.5.2.2 – Channel charge injection

In the figure 4.5.2.2 it is represented the effects of the channel charge injection error in the MDAC's output. The grey area represents the values that the output of the current based MDAC can take because of this effect.

The amplification phase of a MDAC is a negative feedback system, like the one represented in the figure 4.5.2.3. But in the MDAC during this phase there is not a V_{in} since the sampled values are stored in the charges present in the switched-capacitor network.

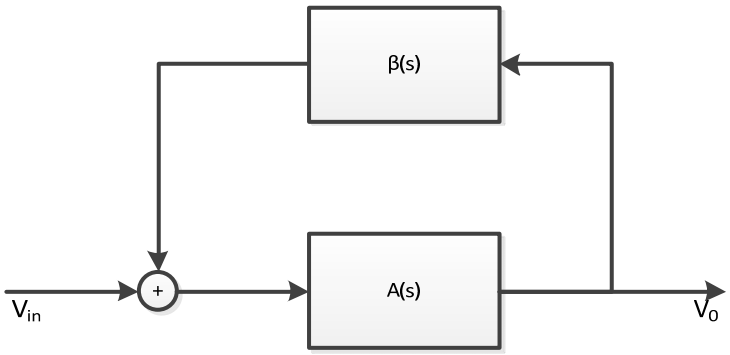


Figure 4.5.2.3 – Negative Feedback System representation

The other error source is the stability of the time response of the switched capacitor circuit. This is represented by the figure 4.5.2.4.

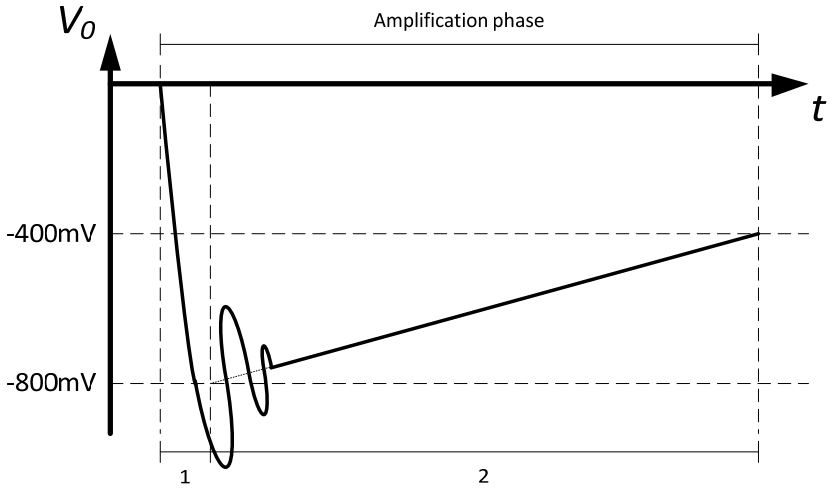


Figure 4.5.2.4 – Circuit's time response stability

An important factor to be referred is that if the oscillations stop before the end of the amplification phase, they can be ignored. But on contrary, if they don't fully attenuate they can be the major source of error in the obtained result.

The oscillation appears in the output of the MDAC because of the increasing value of the feedback switch resistance when the sampling frequency also increases. A model that can explain this phenomenon is represented in the figure 4.5.2.5.

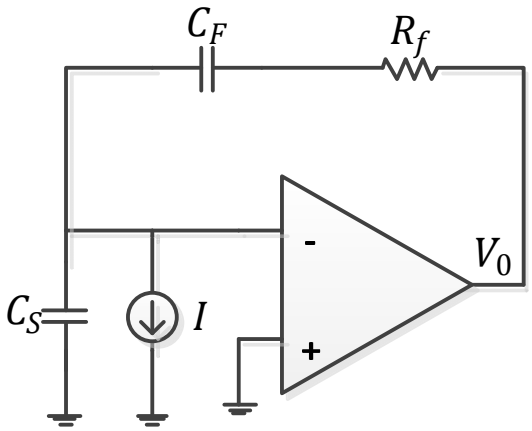


Figure 4.5.2.5 – The resistance presence in the feedback path

The presence of a resistance will change the feedback factor. The new value for this factor will be given by

$$\beta(s) = \frac{V^-}{V_0} = \frac{\frac{1}{sC_s}}{\frac{1}{sC_s} + \left(\frac{1}{sC_F} + R\right)} = \frac{C_F}{C_F + C_S + sR_f C_F C_S} = \frac{1}{1 + sR_f \frac{C_F C_S}{C_F + C_S}} \frac{C_F}{C_F + C_S} \tag{4.5.2.7}$$

For an easy graphical explanation the feedback equation can be written as

$$\beta(s) = \frac{1}{\frac{s}{\omega_\beta} + 1} \beta \tag{4.5.2.8}$$

Where $\omega_\beta = \frac{1}{R_f}\frac{C_F+C_S}{C_F C_S}$ and $\beta = \frac{C_F}{C_F+C_S}$. The transfer function for the single pole amplifier is

$$A(s) = \frac{A_0}{\frac{s}{\omega_p}+1} \tag{4.5.2.9}$$

With a simple graphical representation of the root-locus it is possible to see the reason behind the oscillation introduction on the MDAC output. The simple representation of the root-locus is in the figure 4.5.2.6.

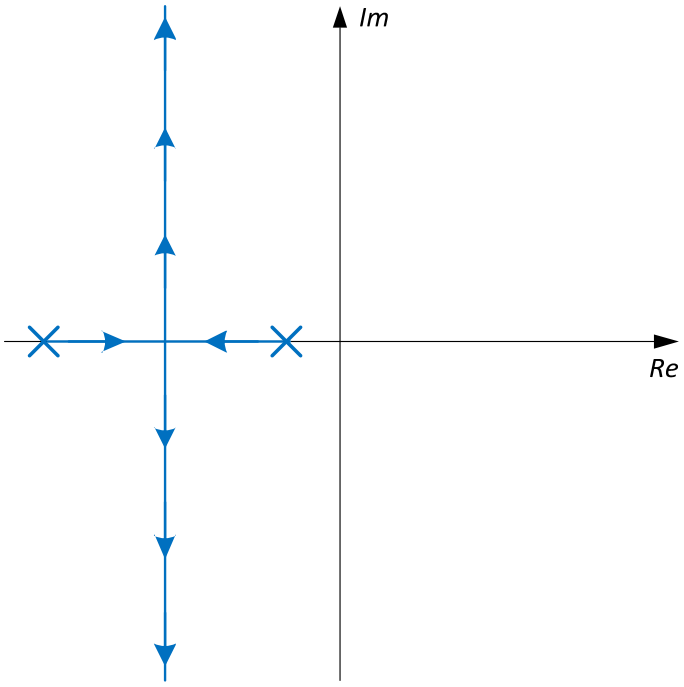


Figure 4.5.2.6 – Root-locus

4.5.2.1 – The current injector circuit

The injector circuit is design as the figure 4.5.2.1.1. It is composed by two NMOS transistors in cascade.

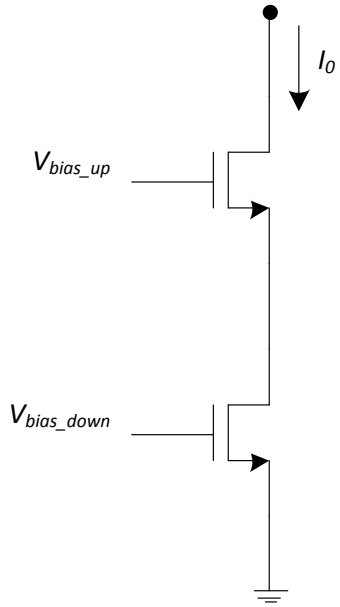


Figure 4.5.2.1.1 – Injector circuit

The reason behind the choosing of this type of transistors is the voltage gap between the expected injection's node voltage.

In the design of this circuit it was taken into account that the intermediary node between the NMOS transistors had to have a constant voltage for the current to be the most constant value possible.

The other thing taken into account it was that the combined $V_{D_{Sat}}$ of the two NMOS transistors had to be smaller than the injection node expected voltage. But at the same time each of the $V_{D_{Sat}}$ should have a value of at least 100mV for a proper operation.

4.5.2.2 – The reason behind the use of CMOS switches

Like the traditional MDAC, switches will be needed to do a proper reference shifting. In the proposed MDAC this shifting will use the switch configuration represented in the figure 4.5.2.2.1.

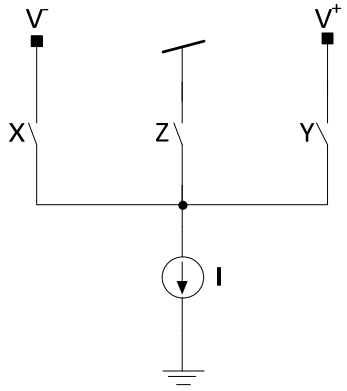


Figure 4.5.2.2.1 – Switches configuration

In the earlier prototypes of the proposed MDAC NMOS switches were employed like it is represented in the figure 4.5.2.2.2.

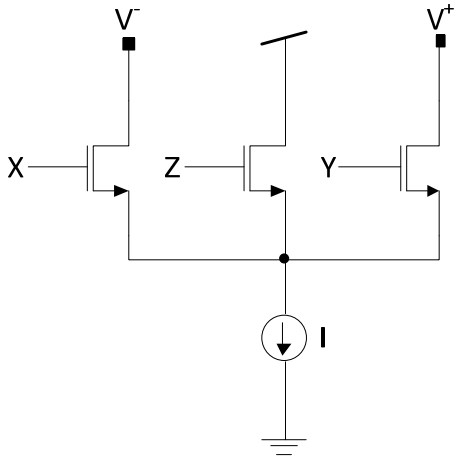


Figure 4.5.2.2.2 – NMOS switching configuration

The NMOS switch technology introduced an extra error that wasn't expected because of their response time going from a voltage close to V_{DD} to a voltage in the middle of the range (this effect is better explained in the annex A). The PMOS technology is not technically viable because of the employment of a NMOS current injector. So this leaves the CMOS switch as the unique viable technology for performing the reference shifting.

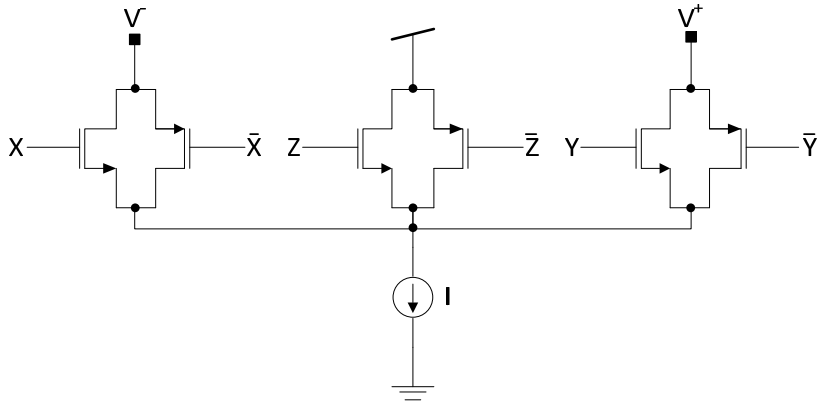


Figure 4.5.2.2.3 – CMOS switching configuration

In the figure 4.5.2.2.3 is represented the way to do the reference shifting employed in the proposed MDAC. It is important for future references that in this proposed approach the switches used for current shifting do not use bootstrapping.

4.5.2.3 – Reducing the injecting period

With the reduction of the current injection period the channel charge injection effects can be reduce in the calculated dynamic parameters. In the figure 4.5.2.3.1 it is pictured these effects in the proposed MDAC output with reduced injecting period.

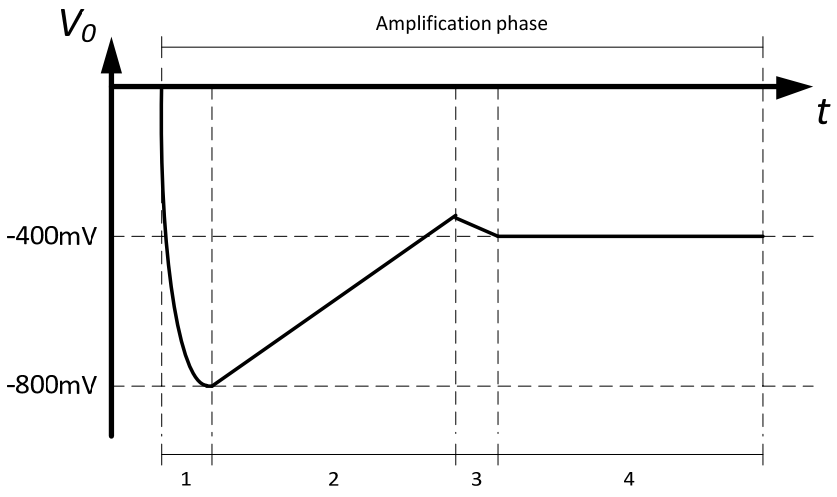


Figure 4.5.2.3.1 – Reducing the current injecting period

By reducing the current injection period the amplification phase will now be divided into four sub-phases by observing the previous figure. Like previously discussed the first sub-phase represents the normal tendency of the circuit to multiply its inputs by two. So the MDAC output during this sub-phase is:

$$\Delta V_0 = 2.\Delta V_{in} \tag{4.5.2.3.1}$$

The second sub-phase has the same previously presented behavior. Considering that the injected current value stays constant the output of the current based MDAC can be written as:

$$\Delta V_0(t) = 2.\Delta V_{in} \pm \frac{I}{C}t \tag{4.5.2.3.2}$$

At the end of the current injection period it is expected that:

$$\Delta V_0 = \Delta V_0(T) = 2.\Delta V_{in} \pm \frac{I_{inj}.T_{inj}}{C} \tag{4.5.2.3.3}$$

Where T_{inj} is the current injection period and I_{inj} is the current needed for the reference shifting (I) plus or minus some current value to attenuate the channel charge injection effects (I_{ext}). So the equation (4.5.2.3.3) can be written has:

$$\Delta V_0 = \Delta V_0(T) = 2.\Delta V_{in} \pm \frac{(I \pm I_{ext}).T_{inj}}{C} \tag{4.5.2.3.3}$$

During the third sub-phase the injection switches go to the off state releasing the charge present in them to the switched-capacitor circuit. Some charge is also released by the feedback switch of the switched-capacitor network since the injected current is not flowing through it.

In the figure 4.5.2.3.1 the third sub-phase period is not a real representation, because this sub-phase is almost instantaneously. At the end of this sub-phase the MDAC output is:

$$\Delta V_0 = 2.\Delta V_{in} \pm \frac{(I \pm I_{ext}).T_{inj}}{C} \pm \frac{Q_{channel}}{C} \tag{4.5.2.3.4}$$

Where:

$$\frac{I_{ext}.T_{inj}}{C} \cong -\frac{Q_{channel}}{C} \tag{4.5.2.3.5}$$

Equation (4.5.2.3.5) needs to be true for a proper attenuation of the channel charge injection. The extra current value is found by using the current controller since this circuit was designed for helping finding the optimal current value.

With the channel charge injection effect attenuated, the MDAC output during the fourth and final sub-phase is:

$$\Delta V_0 = 2.\Delta V_{in} \pm \frac{I.T_{inj}}{C} \qquad (4.5.2.3.6)$$

The circuit responsible for reducing the injection period is represented in the figure 4.5.2.3.2.

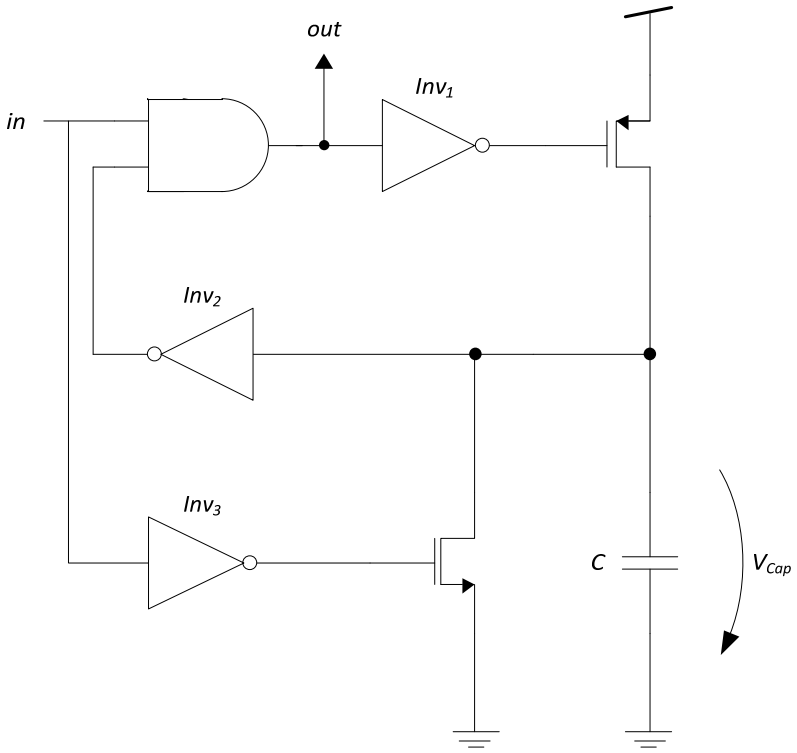


Figure 4.5.2.3.2 – Injection period controller

Since the block input "in" goes from "0" to "1" in digital terms, this means that the starting condition for capacitor voltage is $V_{Cap} = 0\ V$ because if input of this block is "0" the output of inverter Inv_3 is "1" so both of the capacitor plates are connected to ground destroying this way any charge present.

When the block input goes to "1" both the inputs of the logical gate "And" are "1" because V_{Cap} is zero Volts and this means that the inverter Inv_2 output is "1". Hence the output of the "And" logical gate is one which is also the block output.

With "1" at the output of the "And" the PMOS transistors starts letting to flow a current through it. This current will charge the capacitor C, and the voltage to the capacitor terminals will be:

$$V_{Cap}(t) = \frac{1}{C}\int_0^T i(t)\,dt \qquad (4.5.2.3.7)$$

When V_{Cap} is superior to the inverter Inv_2 threshold voltage, the block output goes to "0" and the capacitor C does not receive any more current.

When the block input goes to "0" the NMOS switch will connect the other capacitor plate to the ground preparing this block for the posterior use.

When designing the block the most important factor is the impedance value of the PMOS switch because of the present RC circuit τ constant. The equation (4.5.2.3.7) is a simplification a more real approximation is:

$$V_{Cap}(t) = V_{DD}.\left(1 - e^{-\frac{t}{\tau}}\right) \qquad (4.5.2.3.7)$$

Where $\tau = R_{PMOS}.C$.

4.5.3 – The problem of the OPAMP sharing

In the real world the operational amplifier have parasites in their electrical schemes. The parasite that has the major influence in the obtained results using the OPAMP sharing is the input parasitic capacitance. Its influence is present in either approach. In the proposed MDAC approach the parasitic influence can be represented in the figure 4.5.3.1.

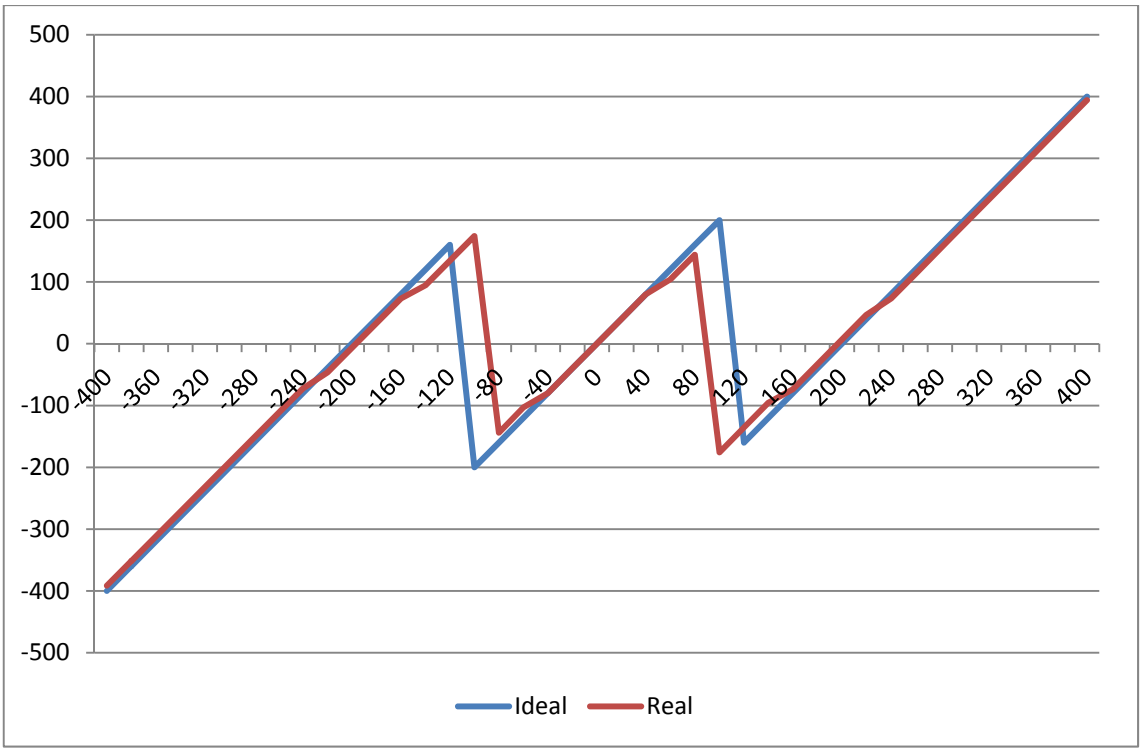


Figure 4.5.3.1 – OPAMP's input capacitance influence

In the current based MDAC the OPAMP parasitic capacitance influence occurs because of the charge build up during the injection of current in the switched-capacitor network. If this problem is not addressed in the design of the circuit, the charge present in the parasite will transit between the operating phases of the OPAMP, causing an error at the output of the stage.

This influence can be seen when previous sample of the n+1 stage obligates the injection of current in the switched-capacitor network and the current sample of the n stage does not make that obligation. So the charge maintained in the parasite will produce what is normally called a memory effect.

4.5.4 – The OPAMP common-mode problem

The proposed MDAC achieves its results by the use of the capacitor physical properties employing currents for reference shifting. The current circuit starts in the OPAMP passes by the feedback capacitor and ends in the injector circuit.

In normal use the OPAMP is a stable circuit in terms of current. This means there is not a great variation in the value of current flowing thru its circuit. But this is not true in the proposed MDAC since the injected current comes from the OPAMP.

The asked current from the OPAMP makes it one of the fundamental keys in this approach because if its common-mode cannot respond swiftly to the circuit it will introduce an unrecoverable error in the design, since it is not possible to know how it will react to different voltage at its input.

4.6 – Simulations Results

The simulation presented in this section is related with the behavior of the proposed MDAC circuit using simulations with a sampling rate of 40MS/s.

Since the proposed approach is based in the traditional structure, the technology behind the implemented ADC is the 0,13 μm UMC CMOS technology and simulated using the Spectre simulator. The ADC was again simulated using transient analysis and for an input sine wave signal with amplitude -1 % of the full-scale and a frequency value of 1 MHz.

The implemented MDACs use an electrical model for the amplifiers with a single dominant pole with a DC gain of 65 dB and a gain-bandwidth product (GBW) of 1GHz. All other elements in both pipeline ADCs are made with real devices, including logic circuits, clock-phase generation circuitry and switches. All switches in the signal path employ the previously discussed clock boosting techniques in order to reduce the signal distortion. All capacitors used have a nominal capacitance

value of 1 pF. The V_{CM} voltage is set to 0,6 V and the differential reference voltage of the ADC ($\Delta V_{Ref} = V_{Ref}^{+} - V_{Ref}^{-}$) is set to 0,4 V. The ADC implemented using the proposed MDAC, the correct ΔV_{Ref} was obtained using two different methods: adjusting the value of the current according to the equation (4.2.3), and using the current controller circuit.

The first current adjusting method previously referred was used in the earlier designs (prototypes) of the proposed MDAC circuit. In these designs the current was injected during the every instant of the amplification phase, so the channel charge injection effect was not seen directly in the transient simulations but in the FFT output spectrum. This non intended effect provokes a ENOB limitation of 8,5-bits.

To overcome this limitation an extra degree of freedom is needed and this new variable is a shorter current injection time, because with this the channel charge injection effect is seeable in the transient analysis. Dimensioning the injection period for half the amplification phase, this leaves enough time for the channel charge injection to cause all the unwanted effects.

To make the system more reliable to exterior effects and almost every non ideal effect present in the circuit the third generation designs use the current controller for achieving the optimum current value for reference shifting. In this new design the distortion introduced by the current error was reduced, which caused the SNDR to increase and consequently the ENOB also increased.

The output spectra of three generation designs of the proposed approach are depicted in the figure 4.6.1, figure 4.6.2 and figure 4.6.3. And from this spectra the performance parameters were calculated, and are summarized in table 4.6.1.

Table 4.6.1 – Simulated ADCs design performance at $F_S = 40\ MS/s$

	SNR	THD	SFDR	SNDR	ENOB
First Generation Proposed MDAC	56,545	-56,129	59,009	53,322	8,5651
Second Generation Proposed MDAC	58,611	-59,462	65,049	56,006	9,0109
Third Generation Proposed MDAC	60,683	-65,273	71,348	59,388	9,5727

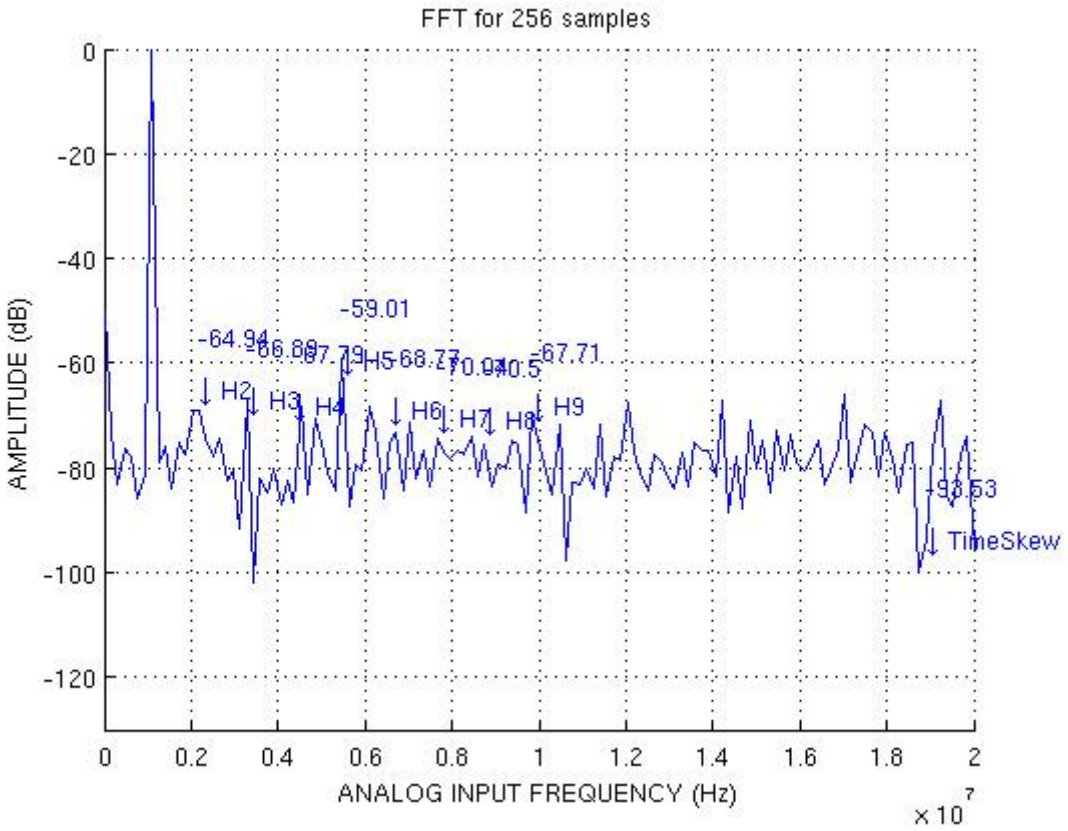


Figure 4.6.1 – First Generation Proposed ADC design output spectrum at $F_S = 40MS/s$

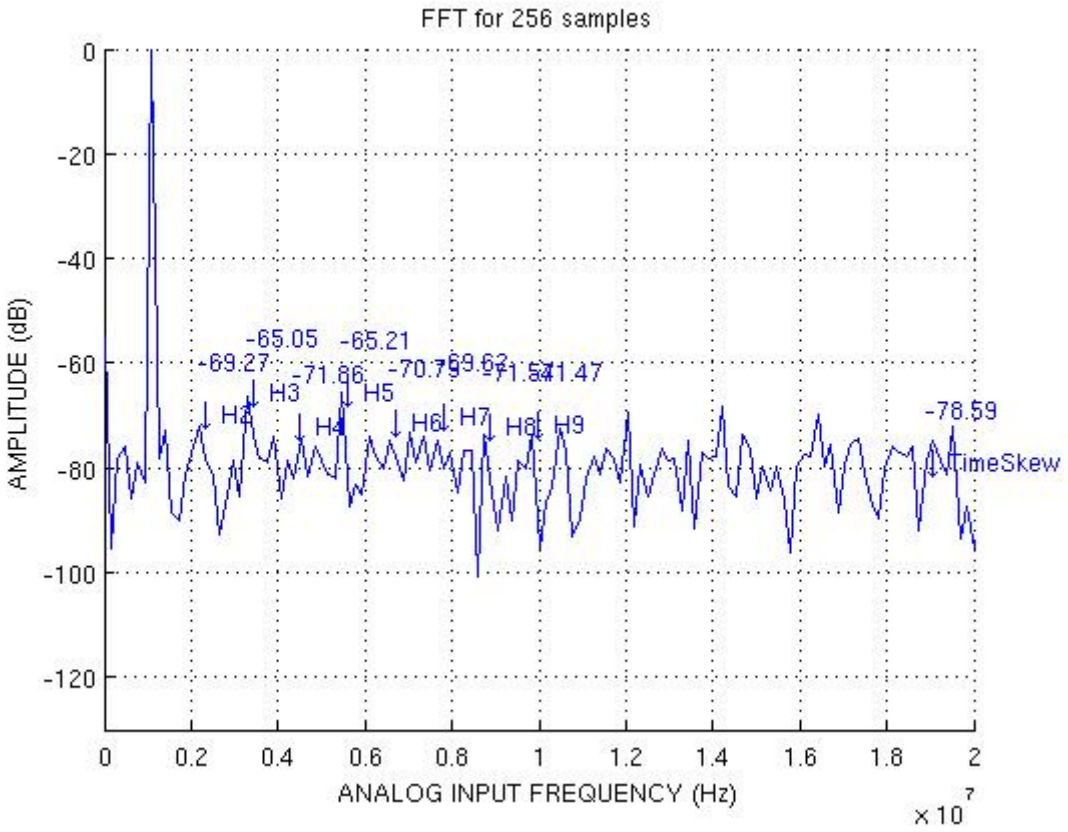


Figure 4.6.2 – Second Generation Proposed ADC design output spectrum at $F_S = 40MS/s$

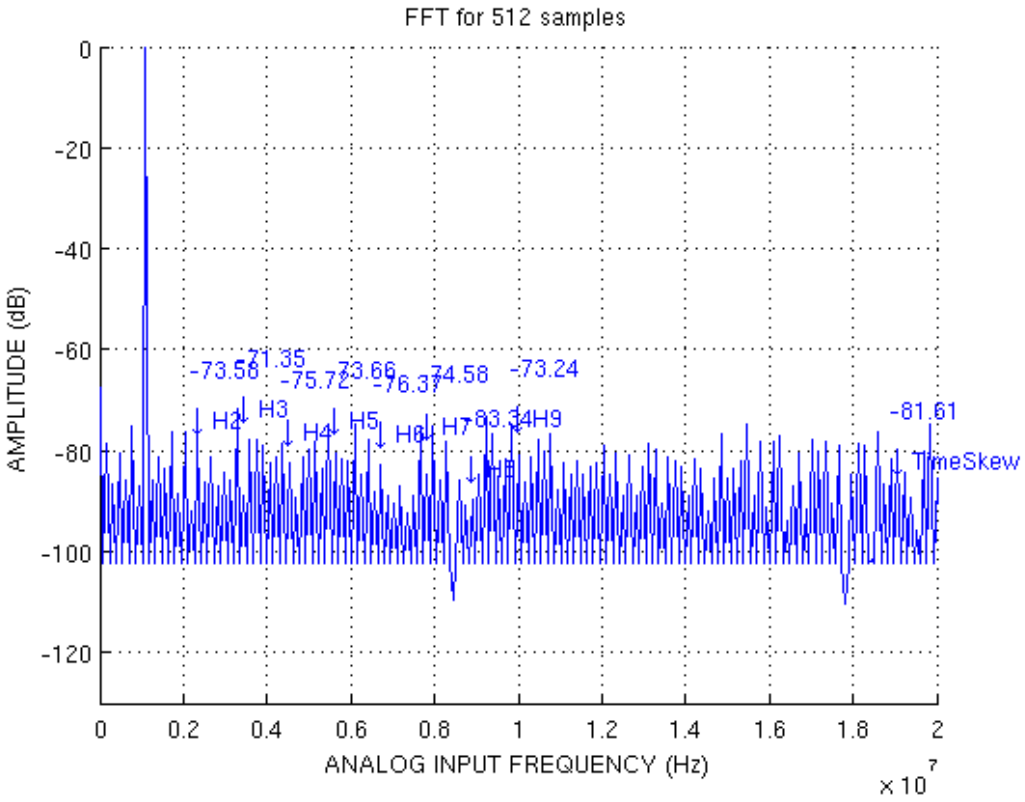


Figure 4.6.3 – Third Generation Proposed ADC design output spectrum at $F_S = 40MS/s$

The simulation results show that the latest generation of the proposed MDAC circuit is capable of achieving a performance similar to the performance of the traditional MDAC circuit.

Another important aspect is the power dissipation of the reference generation circuit. The results are shown in the Table 4.6.2 and only have present the third generation results of the proposed MDAC and the traditional approach.

Table 4.6.2 – Power dissipation of the reference circuitry at $F_S = 40MS/s$

	Third Generation of the Proposed MDAC	
	I_P	Total
Power	55,86 μW	446,88 μW

In case of the ADC using the proposed MDAC circuit with the current controller, the V_{DD} voltage source connected to the current sources inside the MDAC circuits dissipate a total of 447 μW.

5 – Proposed Current Controller Architecture

5.1 – Overview

The linearity of high-resolution architectures of ADCs is commonly limited by the accuracy of the elements present in the analog domain of the ADC. In the previous chapter it was proposed a new approach for the level shifting using current.

A problem with the current value will cause a defective level shifting and causing degradation in the dynamic characteristics of the pipeline ADC, since a lower current value will cause input saturation in the following stages and a higher current value will provoke signal compression in each of the following sub-quantization's.

For simplifying proposes there will be only one current controller in the circuit, like the one represented in the figure 5.1.1. This circuit needs to be aware of all the conditions present in the

analog domain of the MDAC (parasitic elements, phase's duty cycles, and so on), since a small change in one of the present conditions in the pipeline stages can cause a severe degradation of the system SNDR.

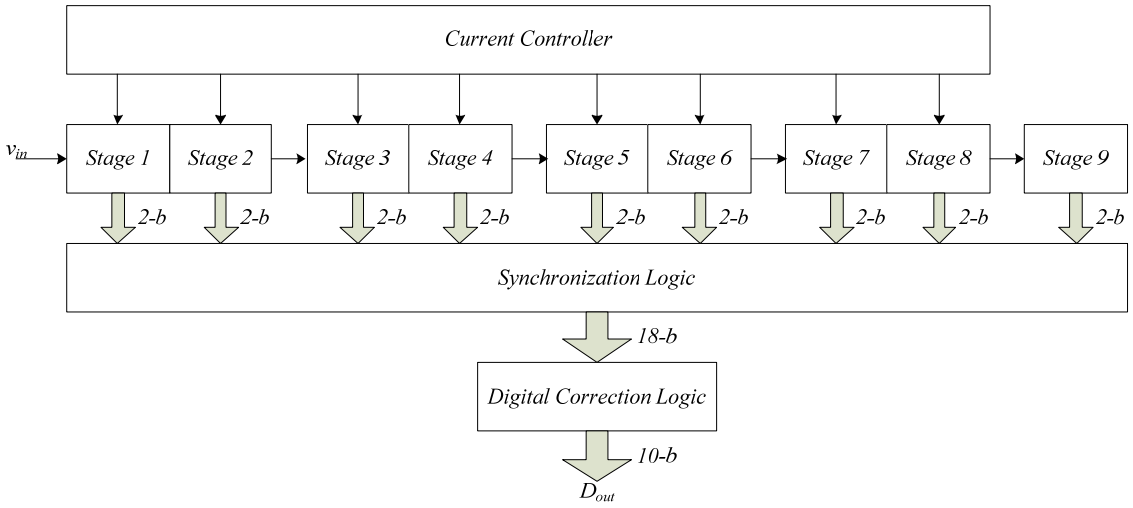


Figure 5.1.1 – Interaction between the current controller and pipeline stages

The proposed circuit will allow the pipeline ADC with the proposed MDAC to do a self-calibration regarding the current value, independent of the initial conditions present in the system.

For simplification the calibration will not be done in the conversion stages, but in a scale replica stage. This was done for reducing the simulation time and for simplifying the earlier prototypes of this circuit.

5.2 – Blocks of the Controller

In the figure 5.2.1 it is represented the three blocks that represent the current controller circuit. These three blocks are: scale replica stage, discrete integrator, bias circuit.

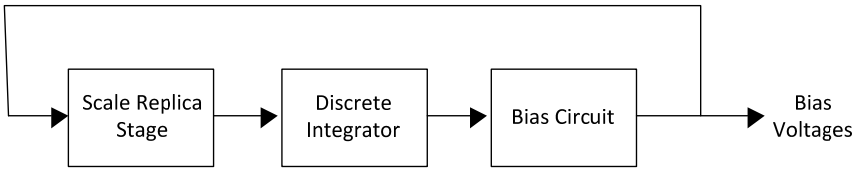


Figure 5.2.1 – Current Controller Blocks

5.2.1 – Scale Replica Stage

This block is an exact replica of a pipeline stage, including the OPAMP sharing technique. The schematic of this block is represented in the figure 5.2.1.1.

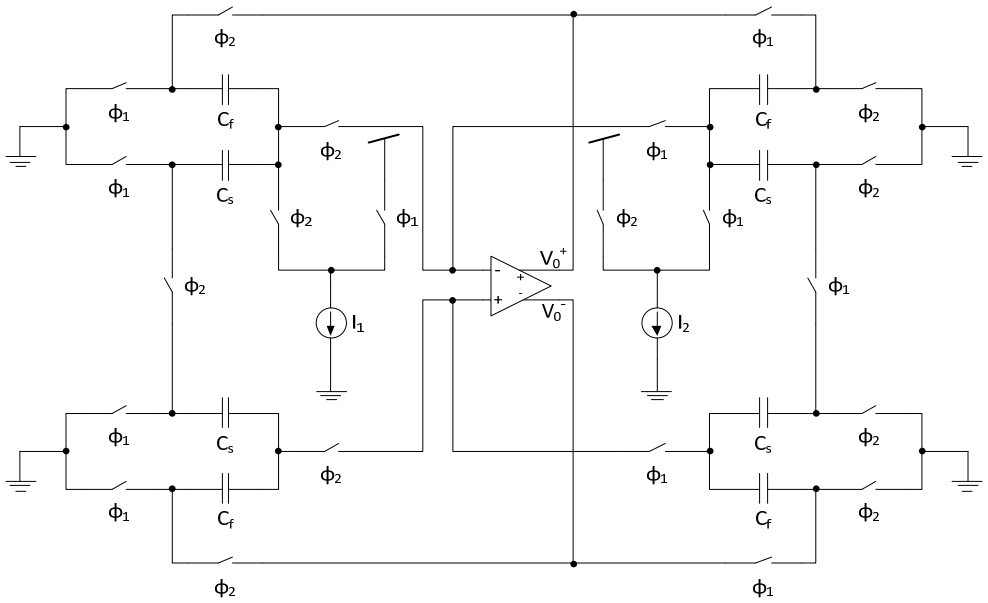


Figure 5.2.1.1 – Pipeline Stage scale replica schematic

The major difference between this replica and the normal conversion pipeline stage is that the inputs of both the stages present in the replica are grounded, and the MDAC will always realize the Y operation. So this means that the transfer function of this block can be written as:

$$\begin{cases} V_0 = \dfrac{I_2.T_{\phi_1}}{C}, during\ \phi_1 \\ V_0 = \dfrac{I_1.T_{\phi_2}}{C}, during\ \phi_2 \end{cases} \quad (5.2.1.1)$$

Where $V_0 = V_0^+ - V_0^-$. This block needs to emulate every function of the normal block, and most importantly, needs to have an equal time response when injecting current in the switched-capacitor network.

During the calibration process the injected current will vary, converging to an optimal result. Since the value of current is directly related with the sampling frequency, this might limit the maximum sampling frequency of the converter.

Every structure present in the normal pipeline stage is present in the scale replica. This is done for achieving the same operating conditions happening in the pipeline stage. With this it is possible to negate the non desired effects discussed in the previous chapter until a certain point.

Depending of the ADC resolution there will be a trade-off between the area size occupied by this structure and the necessary current accuracy. Since a 1:1 scale replica can recreate every one of the parasitic effects, a replica in a 1:2 scale can adapt the system response to the channel charge injection and some of the parasitic capacitances, but cannot anticipate the higher impedance problem in the feedback switch of the switched-capacitor network.

5.2.2 – Discrete Integrator

This is the key block of the current controller circuit, since any unpredicted effects in this block can decrease the converter ENOB to four bits. This problem was first discovered when there was the need of increasing the proposed converter sampling frequency from 40MS/s to 100MS/s. At 40MS/s the discrete integrator used was the one represented in the figure 5.2.2.1.

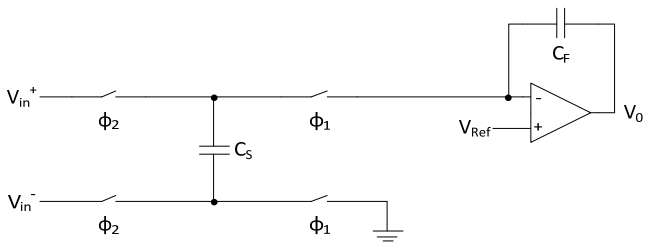


Figure 5.2.2.1 – First version of the discrete integrator

The discrete integrator first used was based on the one employed in [29]. This approach has problems with the parasitic influences in system output, which limits the controlled ADC sampling

frequencies to approximately 60MS/s. Hence, to minimize this system degrading influences the discrete integrator used in the proposed controller is the one represented in the figure 5.2.2.2.

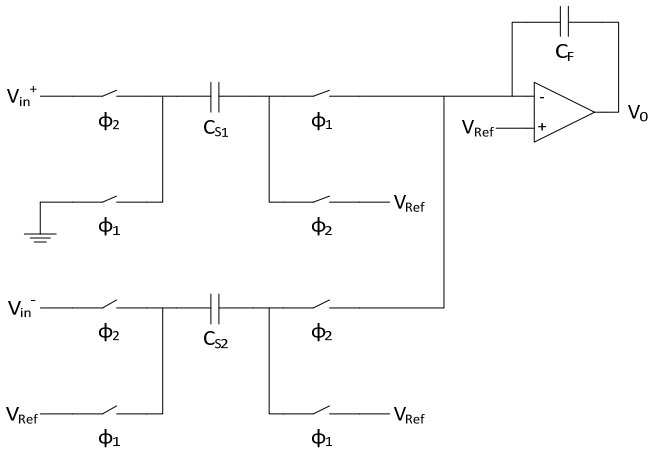


Figure 5.2.2.2 – Discrete Integrator used

The modeling equation for the amplifier present in this circuit can be written as:

$$V_0 = A.\left(V_{Ref} - V_x\right) \Rightarrow V_x = V_{Ref} - \frac{V_0}{A} \qquad (5.2.2.1)$$

Where again A is the finite gain of the amplifier, V_x is the node voltage of the amplifier's minus input, and V_{Ref} is the desired reference voltage.

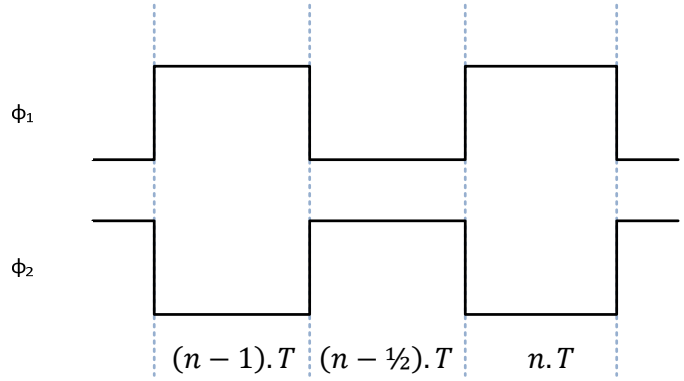


Figure 5.2.2.3 –Phases of this circuit

Using the phase representation in the figure 5.2.2.3 and the circuit representation in figure 5.2.2.2, it is obtained a table with the charges of the capacitors in different time instants.

Table 5.2.2.1 – Charge in the capacitors in different time instants

	C_{S_1}	C_{S_2}	C_F
$(n-1).T$	$C_{S_1}.(0 - V_x[n-1])$	0	$C_F.(V_0[n-1] - V_x[n-1])$
$(n-½).T$	$C_{S_1}.(V_{in}^{+}[n-½] - V_{Ref})$	$C_{S_2}.(V_{in}^{-}[n-½] - V_x[n-½])$	$C_F.(V_0[n-½] - V_x[n-½])$
$n.T$	$C_{S_1}.(0 - V_x[n])$	0	$C_F.(V_0[n] - V_x[n])$

With the principle of charge conservation, from the instant $[n-1]$ to $[n-½]$ the equation that models the charge transfer is:

$$Q_{C_{S_2}}[n-1] + Q_{C_F}[n-1] = Q_{C_{S_2}}[n-½] + Q_{C_F}[n-½] \tag{5.2.2.2}$$

Rewriting the equation (5.2.2.2), using values from the table 5.2.2.1, to obtain the value of $V_0[n-½]$ in this circuit:

$$C_F.(V_0[n-1] - V_x[n-1]) = C_{S_2}.(V_{in}^{-}[n-½] - V_x[n-½]) + C_F.(V_0[n-½] - V_x[n-½])$$

(5.2.2.3)

Knowing that $V_x = V_{Ref} - \frac{V_0}{A}$ from equation (5.2.2.1), the previous equation resolution is:

$$\Leftrightarrow C_F.\left(V_0[n-1] - V_{Ref} + \frac{V_0}{A}[n-1]\right)$$

$$= C_{S_2}.\left(V_{in}^{-}[n-½] - V_{Ref} + \frac{V_0}{A}[n-½]\right) + C_F.\left(V_0[n-½] - V_{Ref} + \frac{V_0}{A}[n-½]\right)$$

$$\Leftrightarrow C_F.\left(1+\frac{1}{A}\right)V_0[n-1] = C_{S_2}.\left(V_{in}^{-}[n-½] - V_{Ref}\right) + V_0[n-½].\left\{C_F.\left(1+\frac{1}{A}\right) + \frac{C_{S_2}}{A}\right\}$$

$$\Leftrightarrow V_0[n-½].\left\{C_F.\left(1+\frac{1}{A}\right) + \frac{C_{S_2}}{A}\right\} = C_F.\left(1+\frac{1}{A}\right)V_0[n-1] - C_{S_2}.\left(V_{in}^{-}[n-½] - V_{Ref}\right)$$

$$\Leftrightarrow V_0[n-½] = \frac{1}{C_F.\left(1+\frac{1}{A}\right) + \frac{C_{S_2}}{A}}\left\{C_F.\left(1+\frac{1}{A}\right)V_0[n-1] - C_{S_2}.\left(V_{in}^{-}[n-½] - V_{Ref}\right)\right\}$$

(5.2.2.4)

Unlike the simple discrete integrator, from the time instant $[n-½)$ to $[n)$, where only the charge in the feedback capacitor is maintained, in this scheme the equation for charge conservation is:

$$Q_{C_{S_1}}[n-½] + Q_{C_F}[n-½] = Q_{C_{S_1}}[n] + Q_{C_F}[n] \tag{5.2.2.5}$$

Equation (5.2.2.5) is true because of the connection between one of the capacitor C_{S_2} connectors and the OPAMP negative input. Finishing the development of the equation (5.2.2.5) to obtain the value of $V_0[n]$ in this circuit:

$$\begin{aligned}
&\Leftrightarrow C_{S_1}.\left(V_{in}^{+}[n-½] - V_{Ref}\right) + C_F.\left(V_0[n-½] - V_x[n-½]\right) \\
&\qquad = C_{S_1}.\left(0 - V_x[n]\right) + C_F.\left(V_0[n] - V_x[n]\right) \\
&\Leftrightarrow C_{S_1}.\left(V_{in}^{+}[n-½] - V_{Ref}\right) + C_F.\left(V_0[n-½] - V_{Ref} + \frac{V_0}{A}[n-½]\right) \\
&\qquad = C_{S_1}.\left(-V_{Ref} + \frac{V_0}{A}[n]\right) + C_F.\left(V_0[n] - V_{Ref} + \frac{V_0}{A}[n]\right) \\
&\Leftrightarrow C_{S_1}.V_{in}^{+}[n-½] + C_F.\left(V_0[n-½] + \frac{V_0}{A}[n-½]\right) = C_{S_1}.\left(+\frac{V_0}{A}[n]\right) + C_F.\left(V_0[n] + \frac{V_0}{A}[n]\right) \\
&\Leftrightarrow C_{S_1}.V_{in}^{+}[n-½] + C_F.V_0[n-½]\left(1+\frac{1}{A}\right) = V_0[n]\left\{C_F.\left(1+\frac{1}{A}\right) + \frac{C_{S_1}}{A}\right\} \\
&\Leftrightarrow V_0[n] = \frac{1}{C_F.\left(1+\frac{1}{A}\right) + \frac{C_{S_1}}{A}}\left\{C_{S_1}.V_{in}^{+}[n-½] + C_F.V_0[n-½]\left(1+\frac{1}{A}\right)\right\} \\
&\Leftrightarrow V_0[n] = \frac{C_{S_1}.V_{in}^{+}[n-½]}{C_F.\left(1+\frac{1}{A}\right) + \frac{C_{S_1}}{A}} + \frac{C_F.\left(1+\frac{1}{A}\right)}{C_F.\left(1+\frac{1}{A}\right) + \frac{C_{S_1}}{A}}\frac{1}{C_F.\left(1+\frac{1}{A}\right) + \frac{C_{S_2}}{A}}C_F.\left(1+\frac{1}{A}\right)V_0[n-1] \\
&\qquad - \frac{C_F.\left(1+\frac{1}{A}\right)}{C_F.\left(1+\frac{1}{A}\right) + \frac{C_{S_1}}{A}}\frac{1}{C_F.\left(1+\frac{1}{A}\right) + \frac{C_{S_2}}{A}}C_{S_2}.\left(V_{in}^{-}[n-½] - V_{Ref}\right)
\end{aligned} \tag{5.2.2.6}$$

Considering that $C_{S_1} = C_{S_2} = C_S$ and that the OPAMP gain is infinite, the previous equation simplifies to:

$$\Leftrightarrow V_0[n] = V_0[n-1] + \frac{C_S}{C_F}V_{in}^{+}[n-½] - \frac{C_S}{C_F}V_{in}^{-}[n-½] - \frac{C_S}{C_F}V_{Ref}$$
$$\Leftrightarrow V_0[n] = V_0[n-1] + \frac{C_S}{C_F}\Delta V_{in}[n-½] - \frac{C_S}{C_F}V_{Ref} \quad (5.2.2.7)$$

Where $\Delta V_{in} = V_{in}^{+} - V_{in}^{-}$. Looking at the equation (5.2.2.7) the integration effect in the discrete domain is present.

5.2.3 – Bias Circuit

The bias circuit implemented is a current sink. In the common operation of this type of circuit the current value flowing thru the transistors in any instant is independent of its terminals voltage. The required condition for the use of this block is that every one of its transistors oblige to:

$$V_{DS} \geq V_{GS} - V_T \quad (5.2.3.1)$$

This condition implies that this block needs to be designed to the required specifications of the ADC. One additional problem of this configuration is the limitation of the available range for the V_0 voltage of this block because for certain of the range values the output transistors (current injector circuit) will leave the saturation region and enter the linear or triode region, in which they cannot function properly has a current source because the current flowing thru them becomes dependent of their terminals voltage.

So for a proper optimization of this circuit the design has to have the minimum possible V_{DSat} in the output transistors (current injector circuit).

The first configuration used in the bias circuit was a High-Swing Cascode, like the one represented in the figure 5.2.3.1.

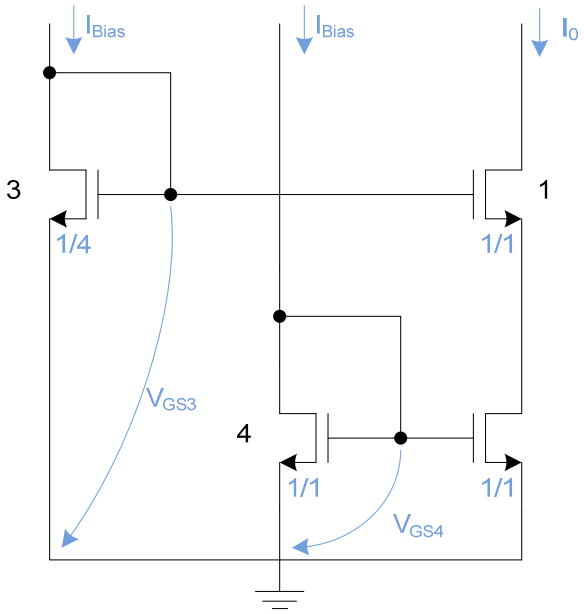


Figure 5.2.3.1 – High-Swing Cascode

Since $\left(\frac{W}{L}\right)_3 = \frac{1}{4}$ developing the large signal equation for the drain current it is possible to conclude that:

$$V_{DSat_3} = 2.V_{DSat_4} \tag{5.2.3.2}$$

Knowing that all other transistors have the same aspect ratio the equation (5.2.3.2) can be rewritten in the following way:

$$V_{DSat_3} = 2.V_{DSat} \tag{5.2.3.3}$$

By guarantying that all the transistors are in the saturation region it is possible to achieve the following equations:

$$V_{GS_3} = V_{DSat_3} + V_{Th} = 2.V_{DSat} + V_{Th} \tag{5.2.3.4}$$

$$V_{GS_4} = V_{DSat_4} + V_{Th} = V_{DSat} + V_{Th} \tag{5.2.3.5}$$

In this case the current of transistor 1 is given by V_{GS_3} so using the equation (5.2.3.4) and knowing that all the transistors are saturated it is possible to know the output voltage, by using the gate voltage of transistor 1.

$$V_{G_1} = V_{GS_3} = 2.V_{DSat} + V_{Th} \tag{5.2.3.6}$$

So the output voltage of the output transistors is:

$$V_0 = V_{D_1} = V_{G_1} - V_{Th} = 2.V_{DSat} \tag{5.2.3.7}$$

It is important to maintain the output voltage in the minimum value possible because it can affect the ADC dynamic parameters since this node will be connected to one of the OPAMP inputs. Hence, it can be seen by a mathematical point of view like introducing a voltage error source in the current based MDAC circuit.

With further research into this configuration for use in future work several problems were detected since $V_{DSat_4} \neq V_{DSat_2}$ and this means that I_0 will not be an exact replica of the bias current because of the channel length modulation [30].

To avoid this error a configuration represented in the figure 5.2.3.2 which is based in the previous but has an extra transistor to force the drain voltage of transistor 2 and 4 to be equal, avoiding this way any type of error.

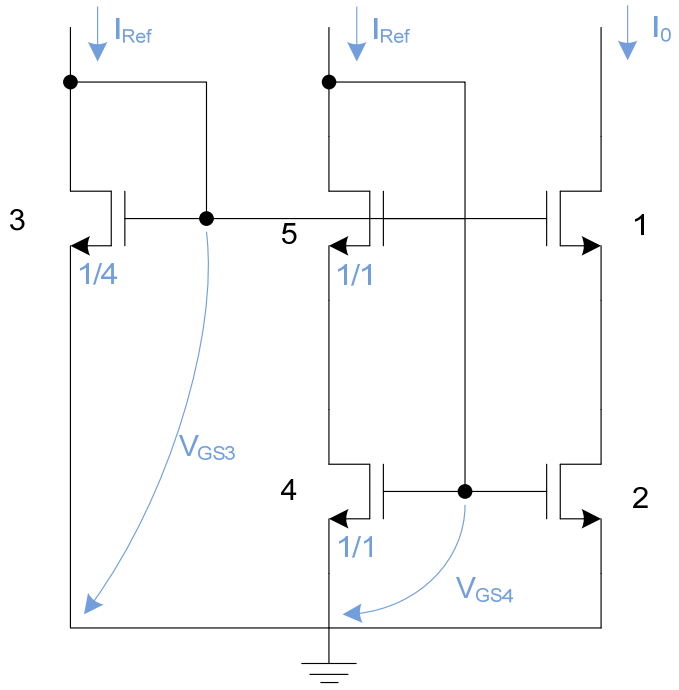


Figure 5.2.3.2 – Improved High-Swing Cascode

All the previous equations found for the High-Swing Cascode are still valid for this improved version. The I_{Ref} current of this circuit is achieved by using PMOS transistors with the output voltage of the discrete integrator present in the gate of these PMOS transistors. The full implementation of the bias circuit is represented in the figure 5.2.3.3.

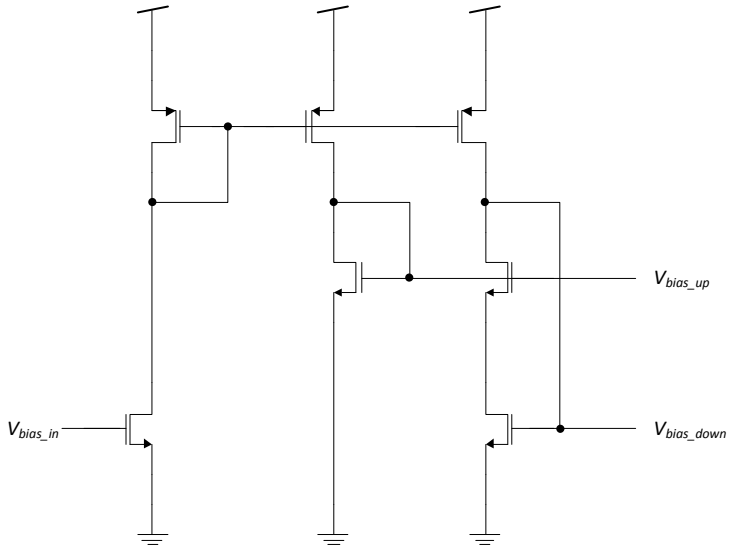


Figure 5.2.3.3 – Full representation of the Bias Circuit

The $V_{bias\ up}$ and $V_{bias\ down}$ are responsible for the biasing of the current injector circuit present in the current controller circuit. The $V_{bias\ in}$ in the input of the biasing circuit and it is responsible for the interface of this block with the discrete integrator.

It is required a current mirror in the PMOS transistors with the current source being a separated NMOS transistors because the $V_{bias\ in}$ voltage can have small values when the current in the MDAC circuit is almost calibrated.

Without taking into account the properties of a current mirror (meaning that the biasing current will be equal to the output current) the design of this circuit is done in three steps, like it is represented in the figure 5.2.3.4.

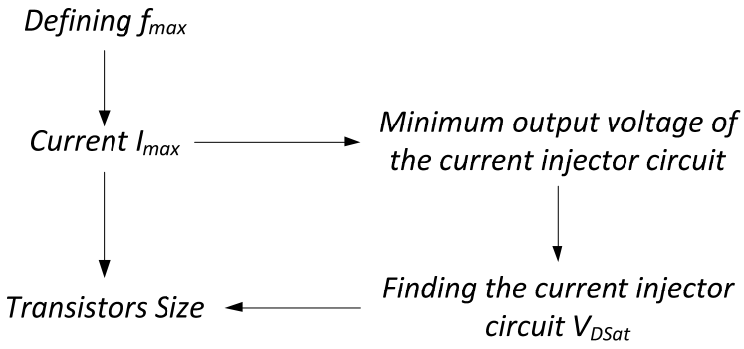


Figure 5.2.3.4 – Bias Circuit Design Steps

The definition of a maximum sampling frequency will give the maximum current produced by the current injector circuit. This current is given by:

$$I_{max} = C.V_{Ref}\frac{f_{max}}{2} \tag{5.2.3.8}$$

The f_{max} is divided by two because the current is only injected during the amplification phase of the current based MDAC.

Since there is 1:1 ratio between the bias current and the injected current it is easily found the minimum output voltage that the current injector circuit will have without its transistors entering into the triode region.

With the use of the current injector circuit transistors size the output voltage needs to be approximately 400 mV for avoiding the presence of distortion on the sampled signal.

The transistors sized for the current injector circuit will be the same in the NMOS transistors present in the bias circuit since there is a 1:1 ratio between the currents.

The remaining transistors sizes where found using the large signal equations for the NMOS and PMOS transistors for the respectively same type transistors.

5.2.4 – Current Controller Transfer Function

The transfer function of the replica stage is defined as:

$$\begin{cases} V_0 = \frac{I_2 . T_{\phi_1}}{C}, during\ \phi_1 \\ V_0 = \frac{I_1 . T_{\phi_2}}{C}, during\ \phi_2 \end{cases} \quad (5.2.4.1)$$

For sake of simplicity it will be considered only one of the phases in the previous equation. So the replica stage transfer function transforms into:

$$V_0 = \frac{I . T_{\phi}}{C} \quad (5.2.4.2)$$

Again to keep the current controller transfer function simple it will be considered that the discrete integrator has an infinite gain and that the C_S capacitors have all the same capacitance value. This means that the discrete integrator transfer function reduces into:

$$V_0[n] = V_0[n-1] + \frac{C_S}{C_F}\Delta V_{in}[n - ½] - \frac{C_S}{C_F}V_{Ref} \quad (5.2.4.3)$$

Since the bias circuit only does the interface between the discrete integrator output and injected current value. This means that the transfer function of this block already considering the injected current circuit is:

$$I_0 = g_m . V_{in} \quad (5.2.4.4)$$

So the current controller transfer function is:

$$V_0[n) = \frac{T_\phi}{C} g_m \cdot \left\{ V_{di}\left[n - {}^3/_2\right] + \frac{C_S}{C_F} \mathrm{V}_0[n-1] - \frac{C_S}{C_F} V_{Ref} \right\} \quad (5.2.4.5)$$

Where V_0 is the output of the replica stage, V_{di} is the discrete integrator output and V_{Ref} is the differential value of the reference voltages used in the MDAC circuit.

5.3 – Simulations Results

The simulation present in this section is related to the current controller behavior.

This circuit behavior was tested for two different sampling rates: 40 MS/s and 100 MS/s. The proposed controller can calibrate the current for higher sampling rates because the flash ADCs present in each of the pipeline stages cannot work at those frequencies.

The current controller was implemented using a 0.13 μm UMC CMOS technology and simulated using the Spectre simulator. Its behavior was simulated using transient analysis and the relation between the scale replica stage and a pipeline stage is 1:1. The inputs of the replica stage are grounded.

The implemented scale replica stage use an electrical model for the amplifier with a single dominant pole with a DC gain of 65 dB and a gain-bandwidth product (GBW) of 1 GHz. All other elements in both pipeline ADCs are made with real devices, including logic circuits, clock-phase generation circuitry and switches. All switches in the signal path employ the previously discussed clock boosting techniques in order to reduce the signal distortion. All capacitors used have a nominal capacitance value of 1 pF. The V_{CM} voltage is set to 0,6 V and the differential reference voltage of the ADC ($\Delta V_{Ref} = V_{Ref}^{+} - V_{Ref}^{-}$) is set to 0,4 V.

The implemented discrete integrator uses the same electrical model for the amplifier with a single dominant pole with different specifications. This model has a DC gain of 60 dB and a GBW of 100 MHz.

Because the system is self-calibrated the current injected in the switched-capacitor circuit will converge in each clock cycle for its optimum value. This value considers every condition applied in the replica stage. Hence, this circuit can make the system more reliable to exterior effects and almost every non ideal effect present in the circuit and reducing the distortion introduced by the current error.

At the 40 MS/s simulations the current controller transient behavior is depicted in the Figures 5.3.1 and figure 5.3.2. And from the transient analysis the mean value for the last 500 ns in each bias voltage is calculated, and are summarized in table 5.3.1.

Table 5.3.1 – Simulated Current Controller design performance at $F_S = 40\ MS/s$

	$V_{bias\ up_1}$	$V_{bias\ up_2}$	$V_{bias\ down_1}$	$V_{bias\ down_2}$
Mean value for the last 500 ns simulation time	56,545	-56,129	59,009	53,322

6 –Reference Voltage Circuitry

High-resolution analog-to-digital converters (ADCs) with high sampling rates need a reference voltage with a high precision and stable value. This is also true in other circuits like voltage regulators, computer memories, flash drives and other communication devices.

When designing these ADCs low-voltage, low-power, and low-area are of great importance. So these new aspects are also required for the circuitry related to the reference voltage. Another important aspects related to these circuit is low sensibility to changes in supply voltage and temperature.

6.1 – Model used

Figure 6.1.1 represents the modeling of the reference voltage circuit.

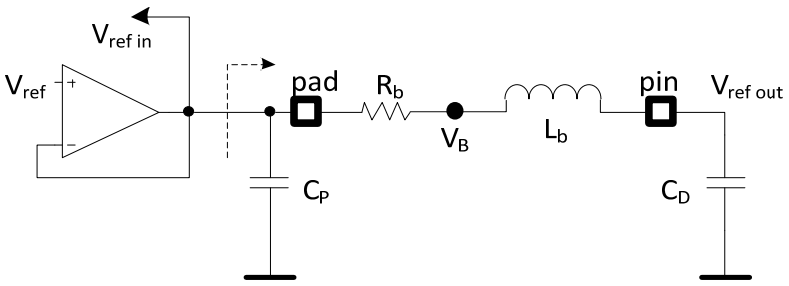


Figure 6.1.1 – Reference voltage circuit model

The model can be split in two different categories related to the structures present in it: inside and outside of the design. Inside of the design circuit are the band-gap circuit and the pad and outside are the bonding wire and the decoupling capacitor.

From the model represented in the figure 6.1.1 can be extracted a three equation system looking at the input impedance of the MDAC circuit.

$$\begin{cases} i_{in} + s.C_P.V_{Ref_{in}} + \dfrac{V_{Ref_{in}} - V_B}{s.L_b} = 0 \\ \dfrac{V_{Ref_{in}} - V_B}{s.L_b} + \dfrac{V_{Ref_{out}} - V_B}{R_b} = 0 \\ \dfrac{V_{Ref_{out}} - V_B}{R_b} + s.C_D.V_{Ref_{out}} = 0 \end{cases} \quad (6.1.1)$$

Where R_b and L_b are respectively the resistance and inductance of the bonding wire. The C_P is the capacitance of the pad. And the C_D is the decoupling capacitor.

So the impedance of the decoupling pin is

$$Z_{decoupling\ pin} = \frac{s^2.L_b.C_D + s.R_b.C_D + 1}{s.(s^2.C_P.L_b.C_D + s.C_P.C_D.R_b + C_D + C_P)} \quad (6.1.2)$$

The pole angular frequency of the system given by the equation (6.1.2) is

$$\omega_p = \sqrt{\frac{C_D + C_P}{C_D.C_P.L_b}} \quad (6.1.3)$$

The equation (6.1.2) pole quality factor is given by

$$Q_p = \frac{\omega_p . C_P . C_D . L_b}{C_P . C_D . R_b} \tag{6.1.4}$$

Simplifying the equation (6.1.4) the obtained result is

$$Q_p = \frac{L_b . \sqrt{\frac{C_D + C_P}{C_D . C_P . L_b}}}{R_b} \tag{6.1.5}$$

The zero angular frequency of the same system is

$$\omega_z = \sqrt{\frac{1}{L_b . C_D}} \tag{6.1.6}$$

The equation (6.1.2) zero's quality factor is given by

$$Q_z = \frac{\omega_z . C_D . L_b}{C_D . R_b} \tag{6.1.7}$$

Simplifying the equation (6.1.7) the obtained result is

$$Q_z = \frac{L_b . \sqrt{\frac{1}{C_D . L_b}}}{R_b} \tag{6.1.8}$$

Plotting the equations (6.1.3) (6.1.5) (6.1.6) (6.1.8) it is possible to see how those parameters change regarding a different value for the inductance present in the bounding wire.

The graphical plots for the pole frequency have the label description has: decoupling capacitance, bounding wire resistance, bounding wire inductance, and pad capacitance.

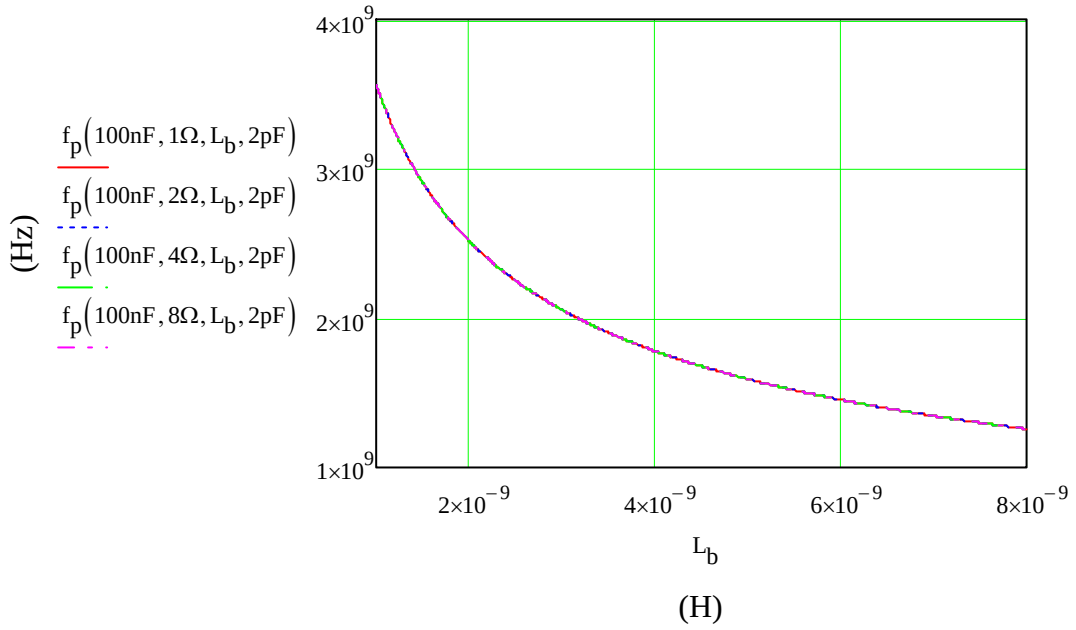


Figure 6.1.2 – Equation (6.1.3) pole with four different resistances and a varying inductance

Looking at the figure 6.1.2 a conclusion can be achieved in regarding to the bonding wire resistance and it is that a variation on this parameter does not change from a mathematical point of view the frequency of the pole given by the equation (6.1.2).

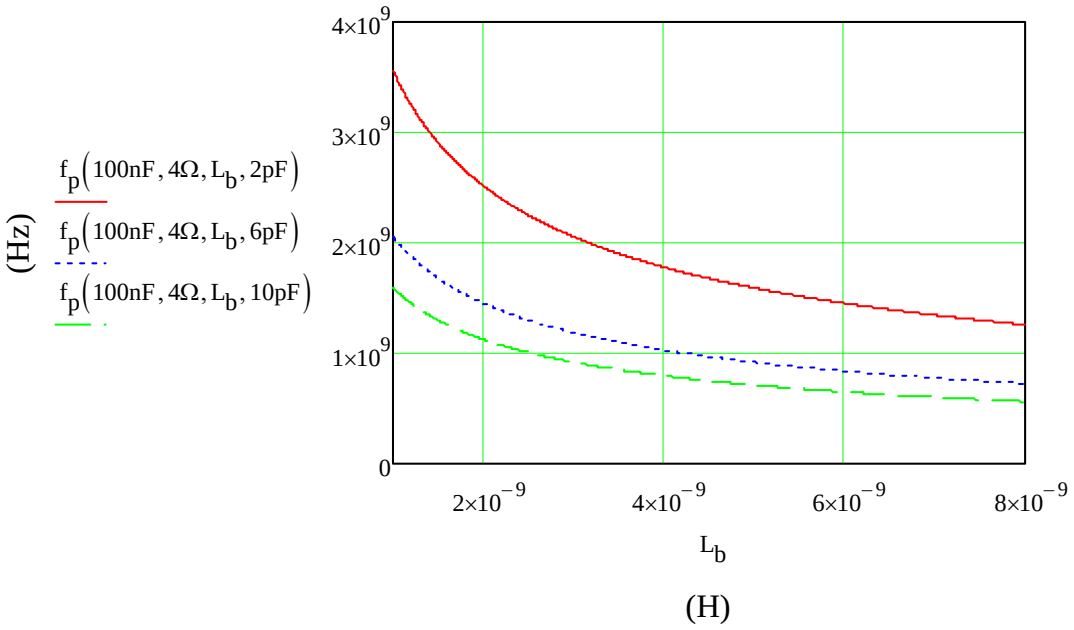


Figure 6.1.3 – Equation (6.1.3) pole with different pad capacitance and a varying inductance

Looking at the figure 6.1.3 it is possible to see that the pad capacitance has a significantly influence over the pole frequency.

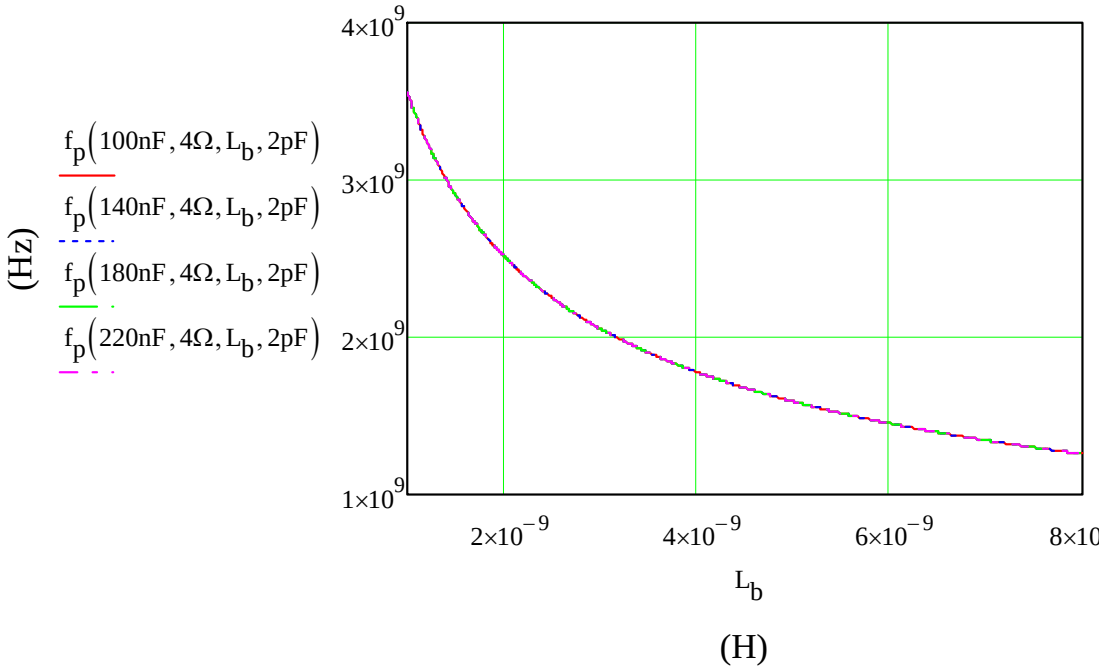


Figure 6.1.4 – Equation (6.1.3) pole with different decoupling capacitor and a varying inductance

In the previous figure it is represented the relation between the system pole frequency and the decoupling capacitor and at the same time a variable inductance. Analyzing the figure 6.1.4 and the equation (6.1.3) it is possible to say that in mathematical terms the effect caused in the system by a different value of the decoupling capacitor can be disregarded because that the pad capacitance has a much smaller value that the referred capacitor.

Another important aspect in the mathematical analysis is the pole quality factor. The graphical plots for the quality factor have the following label description: decoupling capacitance, bounding wire resistance, bounding wire inductance, and pad capacitance.

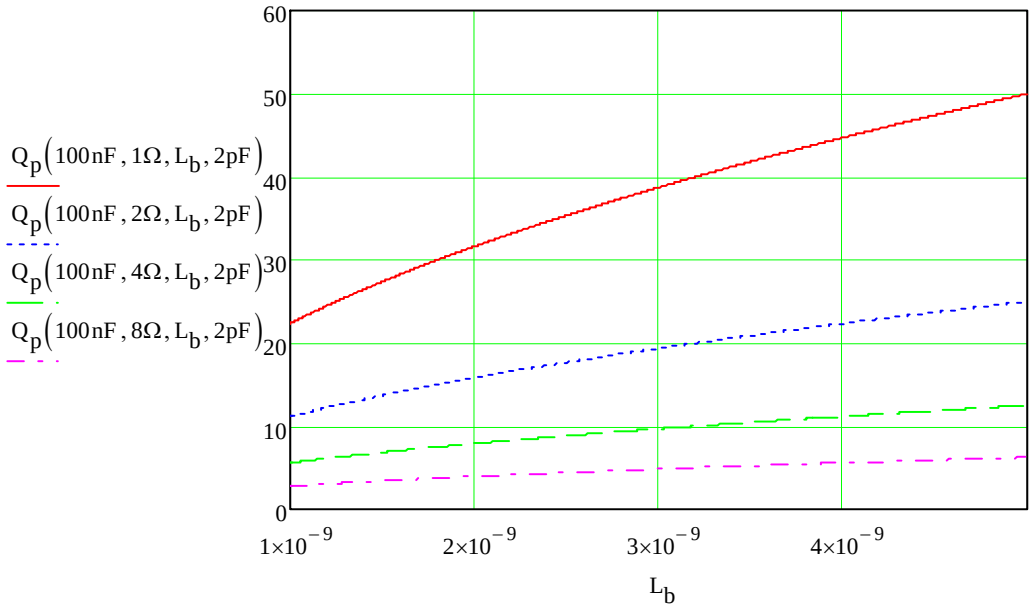


Figure 6.1.6 – Pole quality factor with different resistance and a varying inductance

Since in the mathematical equation for the pole quality factor the bounding wire resistance is the sole divisor, a small variation in this value can change this factor significantly.

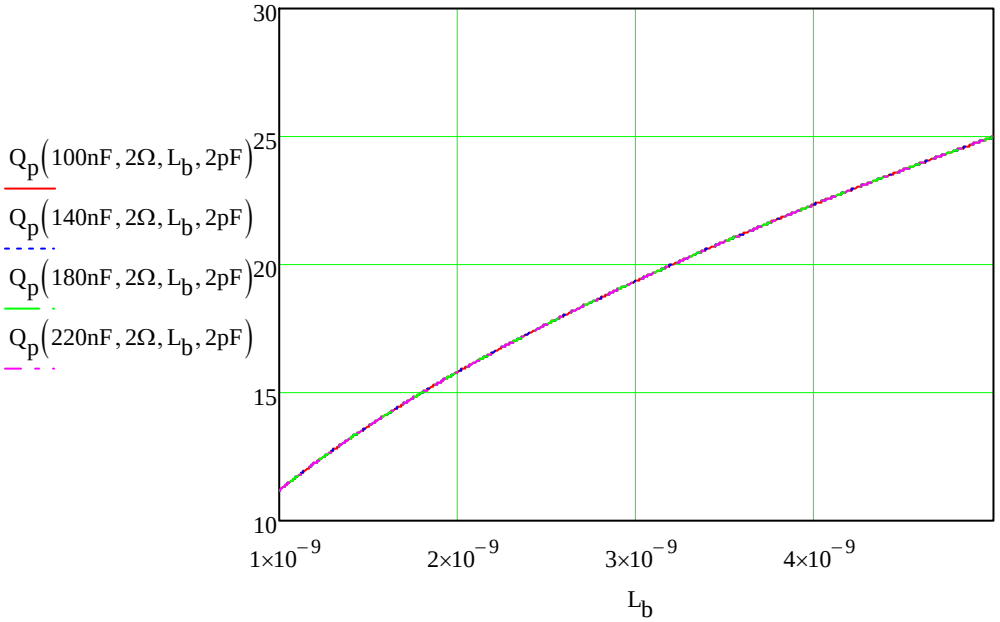


Figure 6.1.5 – Pole quality factor with different decoupling capacitors and a varying inductance

Exactly by the same mathematical reason as for the pole frequency, the pole quality factor will not have a significant change by altering the decoupling capacitance value.

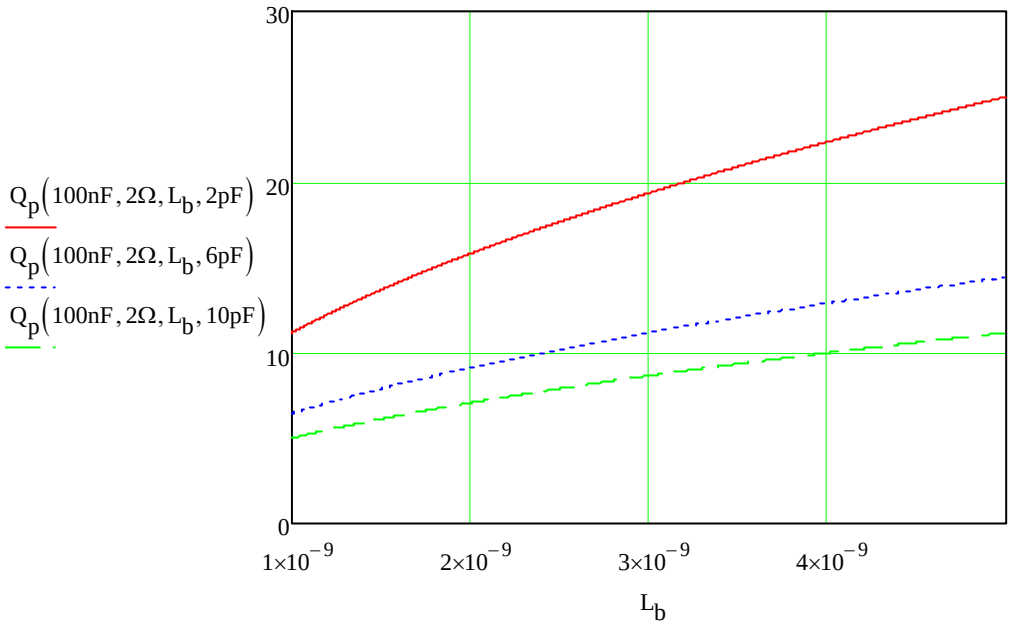


Figure 6.1.6 – The pad capacitance influence in the pole quality factor

Exactly by the same mathematical reason as for the pole frequency the pad capacitance has an important role in the value of the pole quality factor. But comparing the figures 6.1.4 and 6.1.6 it is seeable a more linear gain function (in terms of the quality factor) in the variation of the bounding wire resistance.

It is also important to see the system zero frequency. The graphical plots for this parameter have the label description: decoupling capacitance, bounding wire resistance, bounding wire inductance, and pad capacitance.

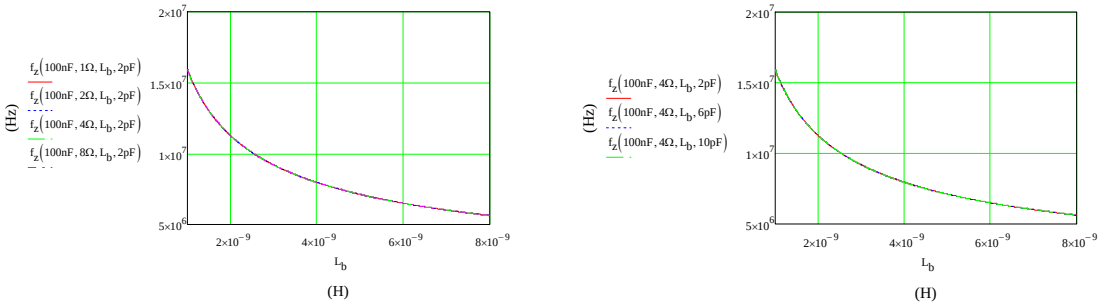


Figure 6.1.7 – The resistance (a) and the pad capacitance (b) influence in the zero frequency

Like it is expected since these parameters aren't reflected in the mathematical equation of the zero frequency they don't change the value of this system component.

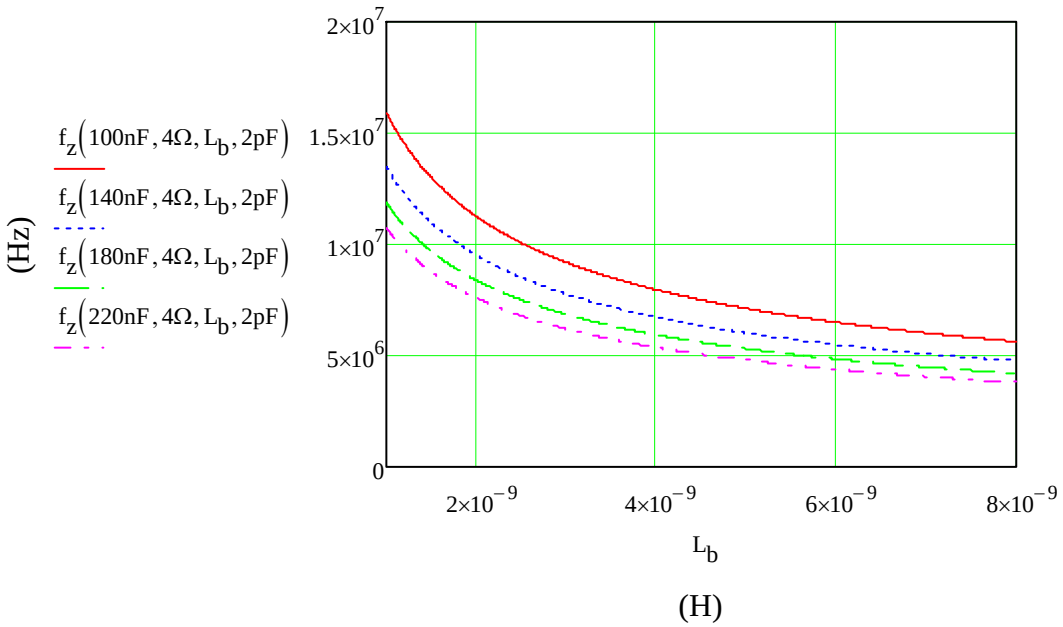
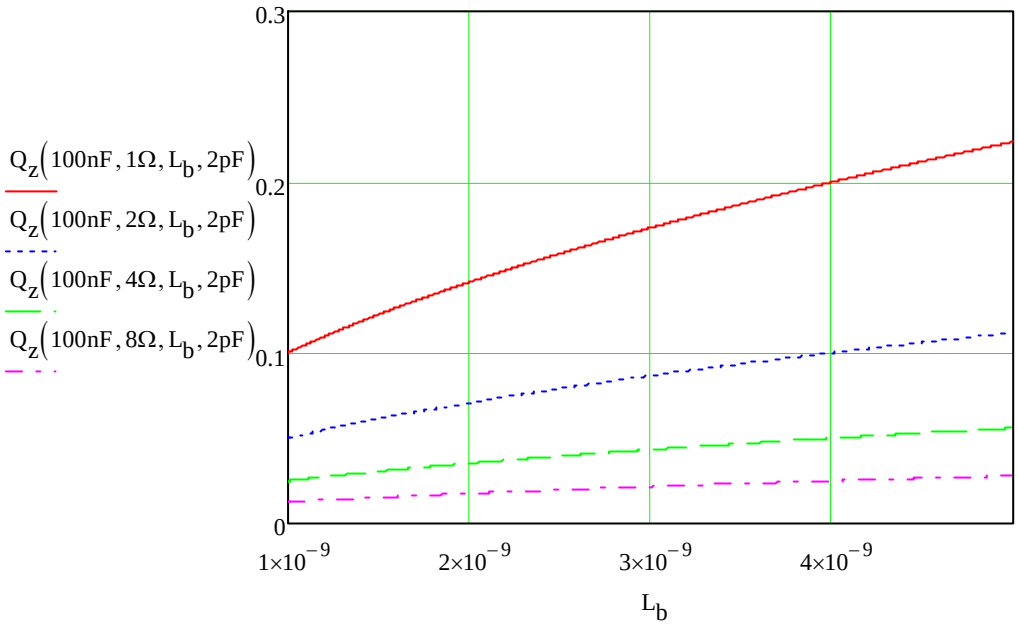


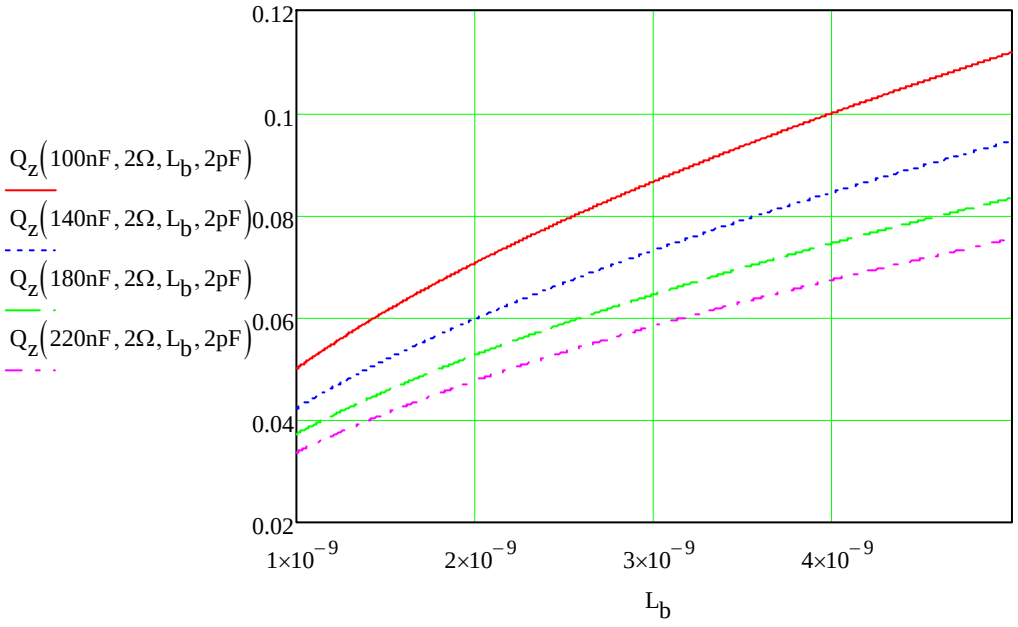
Figure 6.1.8 – The decoupling capacitor influence in the zero frequency

It can be concluded from a mathematical point of view that a smaller decoupling frequency has a benefit for a higher zero frequency.

Analyzing the associated zero quality factor, where the pad capacitance is disregarded because it is not a variable in the equation (6.1.8). The graphical plots for the zero's quality factor have the following label description: decoupling capacitance, bounding wire resistance, bounding wire inductance, and pad capacitance.



(a)



(b)

Figure 6.1.9 – The resistance (a) and the decoupling capacitance (b) influence in the zero's quality factor

Comparing the two previous plots it is seeable that the decoupling capacitor permits the IC designer to do a proper control of the zero's quality factor if the reference voltage system is unstable.

Because of the RLC circuit present in the bonding wire there will be a resonance response in the decoupling pin; this effect can be seen in the figures 6.1.10 6.1.11 obtained using the equation (6.1.2). Like in the traditional RLC circuit different values in the RLC elements will move the resonance frequency.

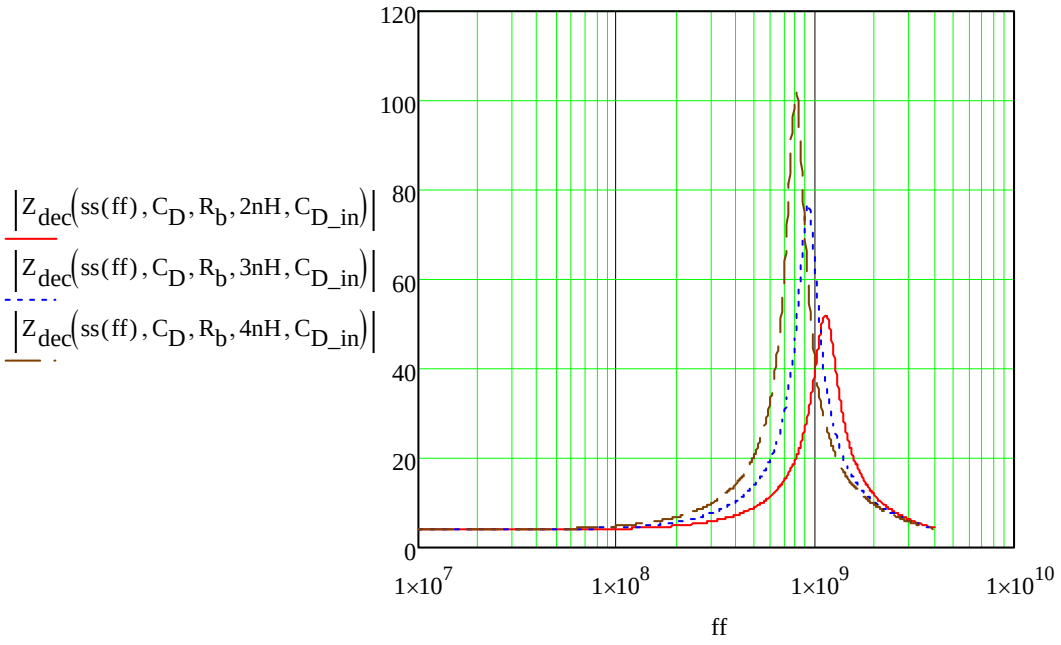


Figure 6.1.10 – RLC resonance effect in the decoupling pin impedance with a variable inductance

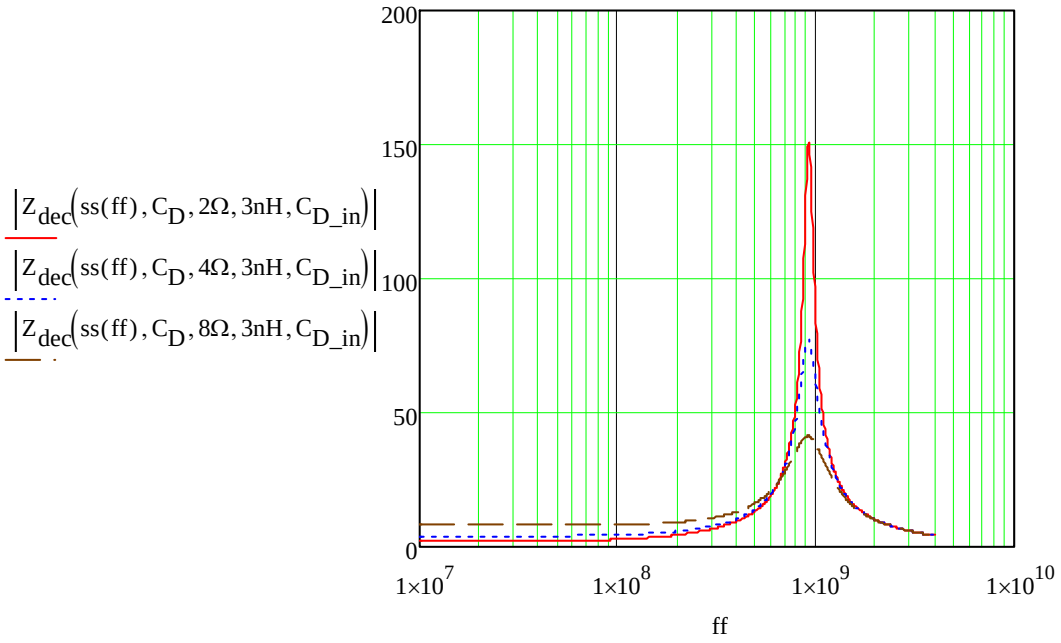


Figure 6.1.11 – RLC resonance effect in the decoupling pin impedance with a variable resistance

Looking at both plots represented in the figures 6.1.10 and 6.1.11 it is possible to arrive at the conclusion that the major unwanted effects of the bonding wires are present in the frequencies above the 500 to 600 MHz, but they are still present in the lower frequencies but do not change dramatically the dynamic parameters of the ADC.

Looking at the decoupling pin impedance does not provide the whole picture of the bonding wire effects, it is necessary to do a time response analysis of this problem and see the error value regarding the difference between the desired reference voltage and the obtained voltage at the decoupling pin.

Since most of the reference voltage power dissipation occurs during the amplification phase and when the MDAC circuit is connect to the reference voltages, it is possible to disregard the power dissipation of the 1,5-bit Flash ADC. So this means that the current flowing thru the reference voltages source is:

$$I_{step} = V_{Ref}.C_T \tag{6.1.9}$$

Where C_T is the total capacitance value that is connected to the reference sources during the amplification phase.

In the frequency domain the decoupling pin response can be written as:

$$V_{Pin}(s) = Z_{decoupling\ pin}.I_{step} \tag{6.1.10}$$

The equation (6.1.10) passage to the time domain only requires the inverse Laplace transform.

$$v_{Pin}(t) = \mathcal{L}^{-1}\{V_{Pin}\} = \mathcal{L}^{-1}\{Z_{decoupling\ pin}.I_{step}\} \tag{6.1.11}$$

The final form of the equation (6.1.11) is:

$$v_{Pin}(t) = \frac{2.C_P.L_B.\lambda + C_D.R_B.\sinh(\lambda.t).e^{-\frac{R_B.t}{2.L_B}} + 2.C_D.L_B.\cosh(\lambda.t).e^{-\frac{R_B.t}{2.L_B}}.\lambda}{2.{C_P}^2.L_B.\lambda + 2.C_D.C_P.\lambda} V_{Ref}.C_T \tag{6.1.12}$$

Where the constant λ in the previous equation is defined by:

$$\lambda = \sqrt{-\frac{4.C_D.L_B - C_D.C_P.{R_B}^2 + 4.C_P.L_B}{4.C_D.C_P.{L_B}^2}} \qquad (6.1.13)$$

The equation (6.1.12) can be used to perform a transient analysis on the error provoked by the bonding wire. This analysis was done using a mathematical tool and is represented in the figures 6.1.12, 6.1.13 and 6.1.14.

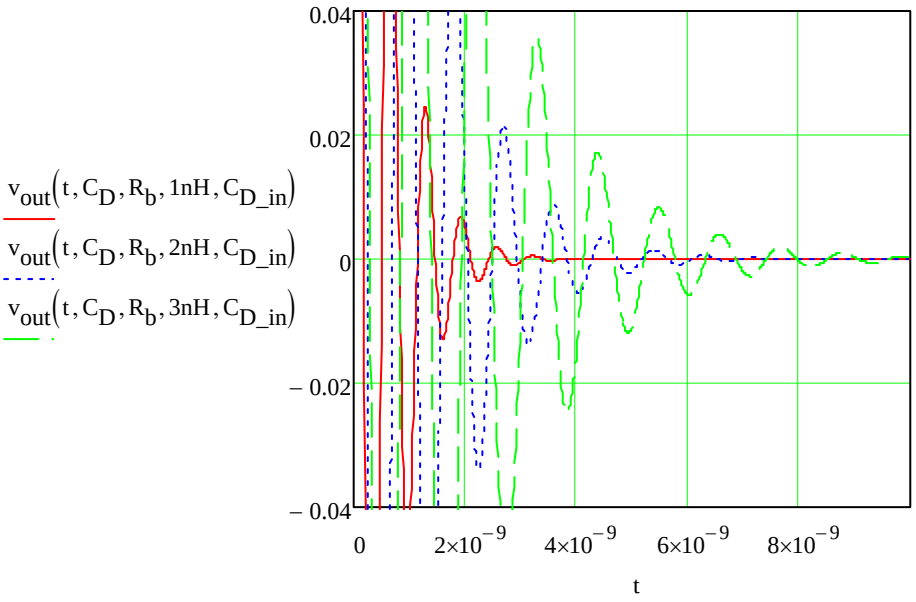


Figure 6.1.12 – The ringing effect provoked by the bonding wire with different inductance values

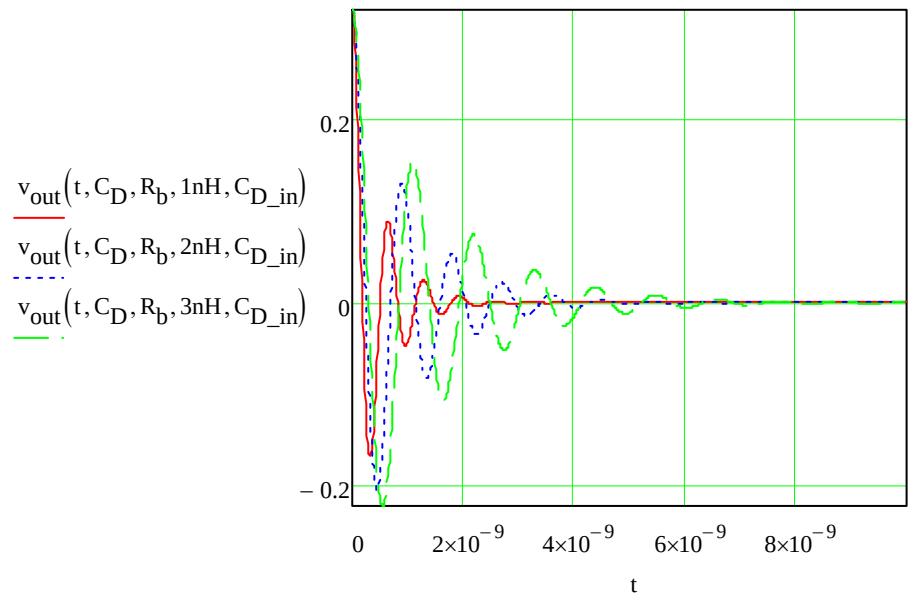


Figure 6.1.13 – The ringing effect provoked by the bonding wire with different inductance values

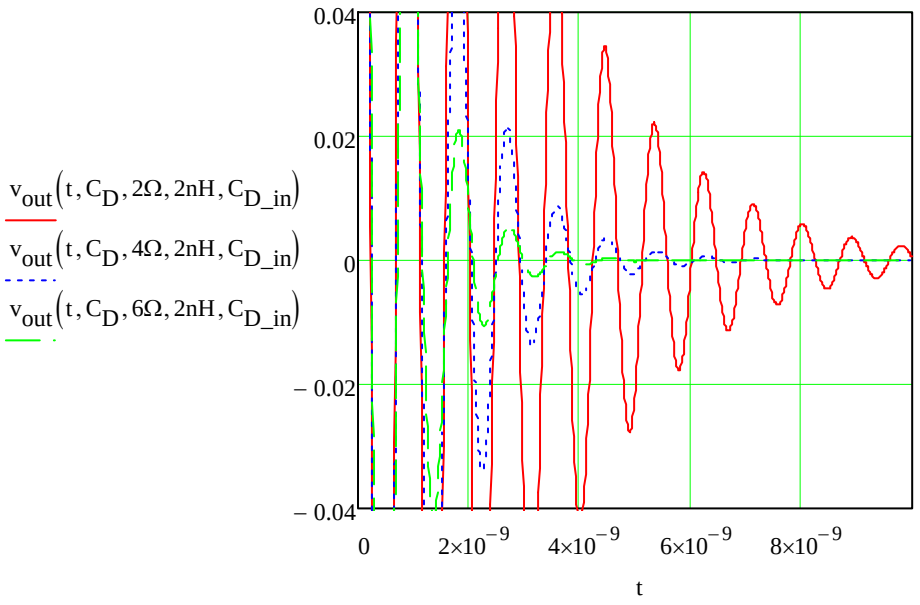


Figure 6.1.14 – The ringing effect provoked by the bonding wire with different resistance values

The figures 6.1.12 and 6.1.13 are the same but using different scales. It is possible to see that the inductance value of the bonding wire affects the amplitude of the ringing effect, the higher the value of this element the higher the maximum amplitude of the ringing effect, which will lead to a longer effect.

The length of the bonding wire not only affects the inductance value of this element but it also affects the resistance value of the wire. Depending of the bonding wire material the resistance and inductance values will change comparing with other material. The resistance value is important since the higher this value the fastest the ringing effect will attenuate this is represented in the figure 6.1.14.

To do a better attenuation of the ringing effect a resistance can be placed in series with the bonding wire to increase the real part of the impedance of that element and this way increasing the attenuation factor of the ringing.

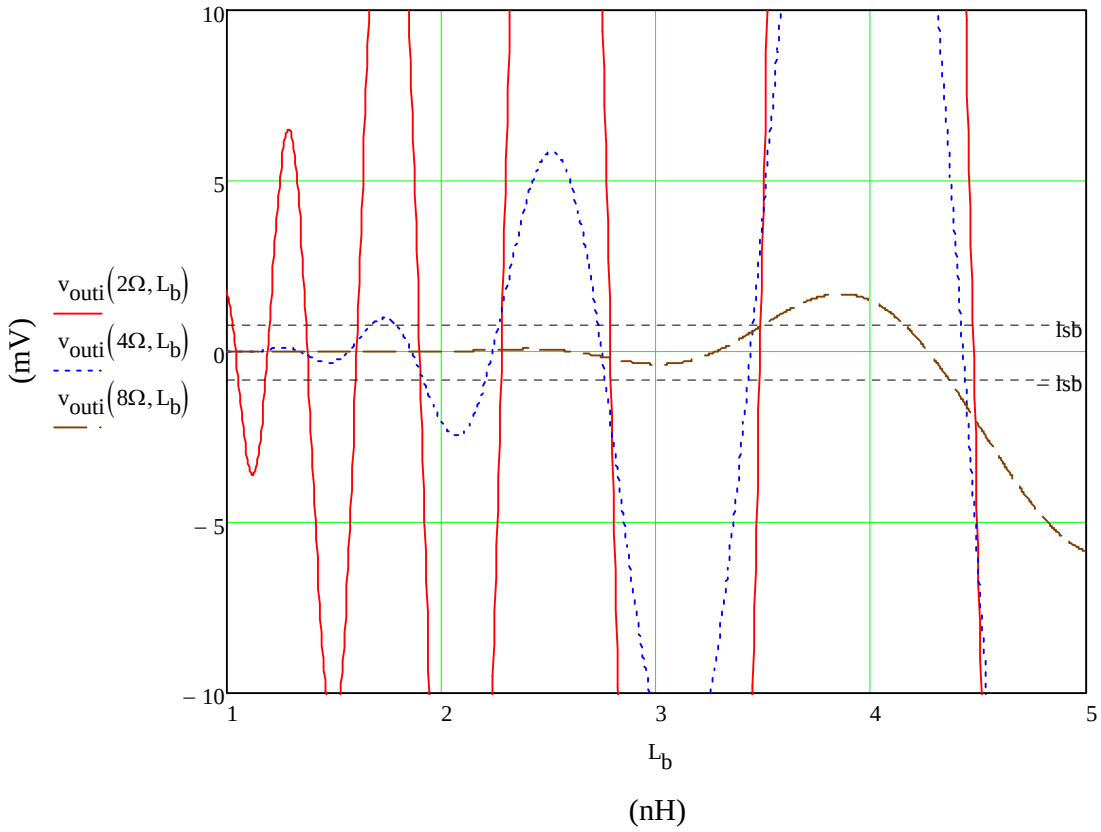


Figure 6.1.15 – The error caused by the bonding wire at 100 MHz

The previous figure makes a relation of the different resistance values and a range of inductance values at the settling time of a sampling frequency of 100MHz. Looking at this figure it can be concluded that a bonding wire with a high resistance to do a fast ringing attenuation and a low inductance value is the best solution but in typical bonding wires the resistance value is highly tied to the inductance value. This is a valid conclusion from the economic point of view where the lesser elements present in the PCB the lower the manufacturing price of that PCB board.

Depending of the error value the digital correction logic can overcome this effect, so it is important to do an analysis of the pipeline ADC dynamic characteristics with a variable reference voltage at the MDAC.

The analysis of the ADC dynamic characteristics variations will be done using a 10-bit pipeline ADC model with the equation system (6.1.14) as the ideal model of the MDAC present in each stage.

$$\Delta V_0 = \begin{cases} 2.\Delta V_{in} + (V_{Ref} \pm V_{Ref_{error}}), & \Delta V_{in} < -\dfrac{V_{Ref}}{4} \\ 2.\Delta V_{in}, & -\dfrac{V_{Ref}}{4} \leq \Delta V_{in} \leq \dfrac{V_{Ref}}{4} \\ 2.\Delta V_{in} - (V_{Ref} \pm V_{Ref_{error}}), & \Delta V_{in} > \dfrac{V_{Ref}}{4} \end{cases} \quad (6.1.14)$$

The reference voltage error analysis were done using two difference amplitudes for the ADC model input signal: one had full-scale amplitude and the other had 80% of the full-scale amplitude. The model produced the two following figures 6.1.16 and 6.1.17.

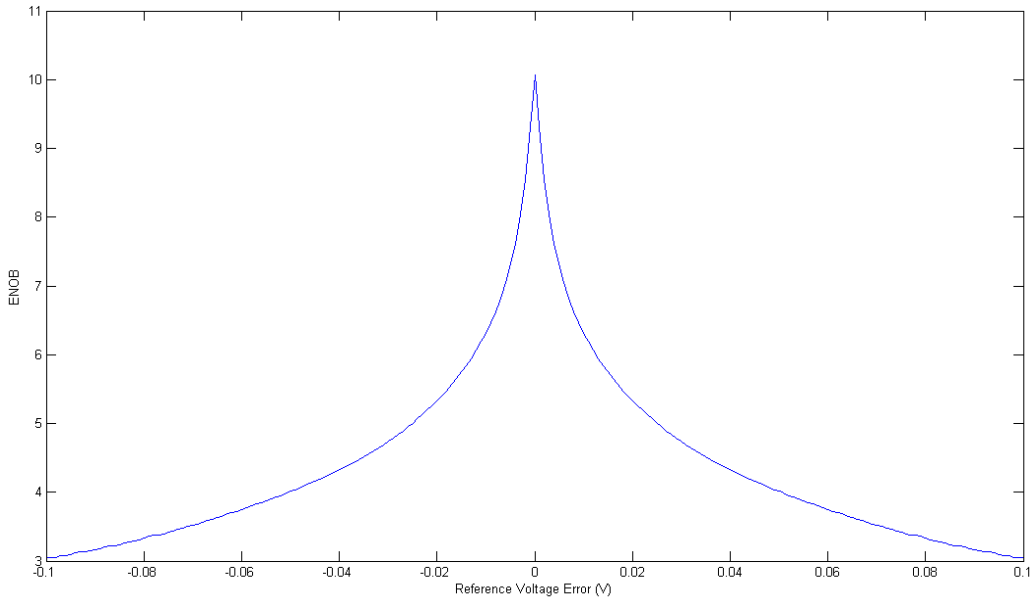


Figure 6.1.16 – ENOB of an ADC with a Reference Error and a full-scale signal

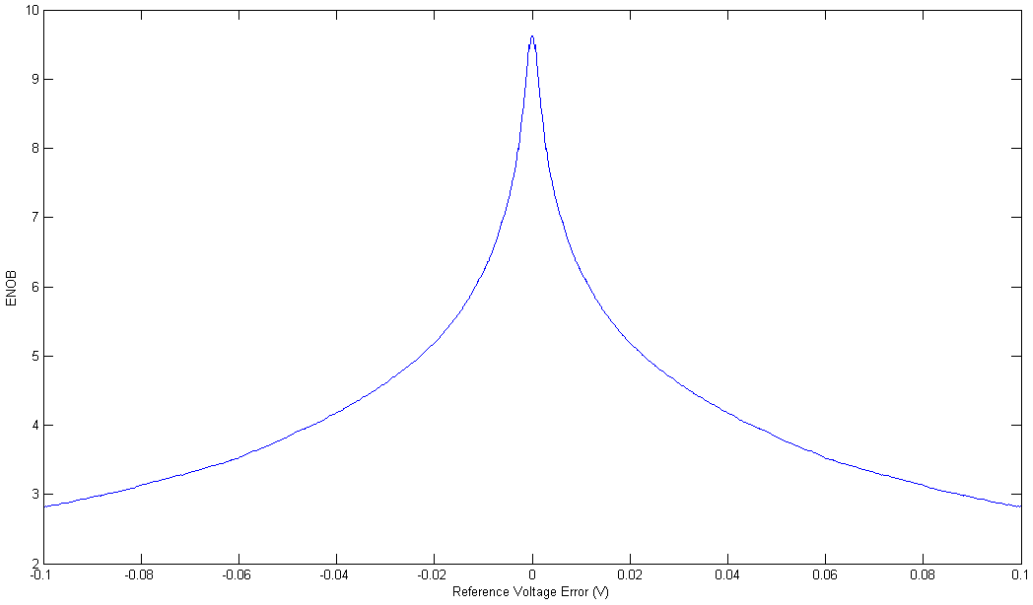


Figure 6.1.17 – ENOB of an ADC with a Reference Error and an 80% full-scale signal

A simple graphical analysis leads to the theoretical conclusion that a signal with a reduced amplitude cannot have the same ENOB has a full-scale input signal. This is not true in the real world because of several errors present in the pipeline which provokes an ADC with a full-scale signal to have a higher distortion than a one with an input signal closer to that value.

What is important to view in the graphical analysis is that an error of 5 mV in the reference voltage will make a drop of one point in the ENOB from a theoretical model point of view. But this was validated with electrical simulations of a bonding wire with an inductance value of 8 nH and a resistance value of 5 Ω.

6.2 – Simulations Results

The simulations presented in this chapter are related with the bonding wire effects in the designed pipelined ADCs.

Because the bonding wire effects have a reduced component in the dynamic parameters in simulations with a sampling rate of 40MS/s. So to see these effects changing the ADC's output spectra a sampling frequency of 100MS/s is the minimum requirement for the reference voltage circuit used.

The two 10-bit ADCs were implemented using a 0,13 μm UMC CMOS technology and simulated using the Spectre simulator. Both ADCs, were simulated using transient analysis and for an input sine wave signal with amplitude -1 % of the full-scale and a frequency value of 1 MHz.

In the 100 MS/s simulations the reference voltage circuitry was introduced in both the ADCs test bench schematics. Since the manual current adjustment proved to be impossible in this sampling frequency due to a several non ideal effects, only the third generation of the proposed design was simulated due to a self-calibration to the conditions around the ADC.

The output spectra of both ADCs with different bonding wire lengths are depicted in the figure 6.2.1 and figure 6.2.2. And from this spectra the performance parameters were calculated, and are summarized in table 6.2.1.

Table 6.2.1 – Simulated ADCs design performance at $F_S = 100\ MS/s$

	Bonding Wire Inductance	SNR	THD	SFDR	SNDR	ENOB
Traditional MDAC	0 nH	60,904	-73,008	76,292	60,645	9,7815
	1 pH	60,339	-64,689	65,45	58,981	9,5051
	1 nH	60,533	-64,693	65,665	59,123	9,5287
	2 nH	60,398	-65,374	66,399	59,199	9,5414
	4 nH	60,916	-64,965	65,805	59,475	9,5872
	6 nH	59,406	-61,268	61,619	57,228	9,2139
	8 nH	54,525	-56,042	56,426	52,208	8,38
Proposed MDAC	0 nH	57,596	-63,766	65,668	56,656	9,119
	1 nH	58,843	-63,035	65,927	57,441	9,2494
	2 nH	58,898	-63,497	66,132	57,605	9,2765
	4 nH	58,999	-63,243	65,925	57,612	9,2777
	6 nH	59,064	-63,523	65,993	57,734	9,298
	8 nH	58,105	-62,858	64,033	56,851	9,1513

The ENOB information summarized in table 6.2.1 comparing the two approaches is represented in the figure 6.2.1.

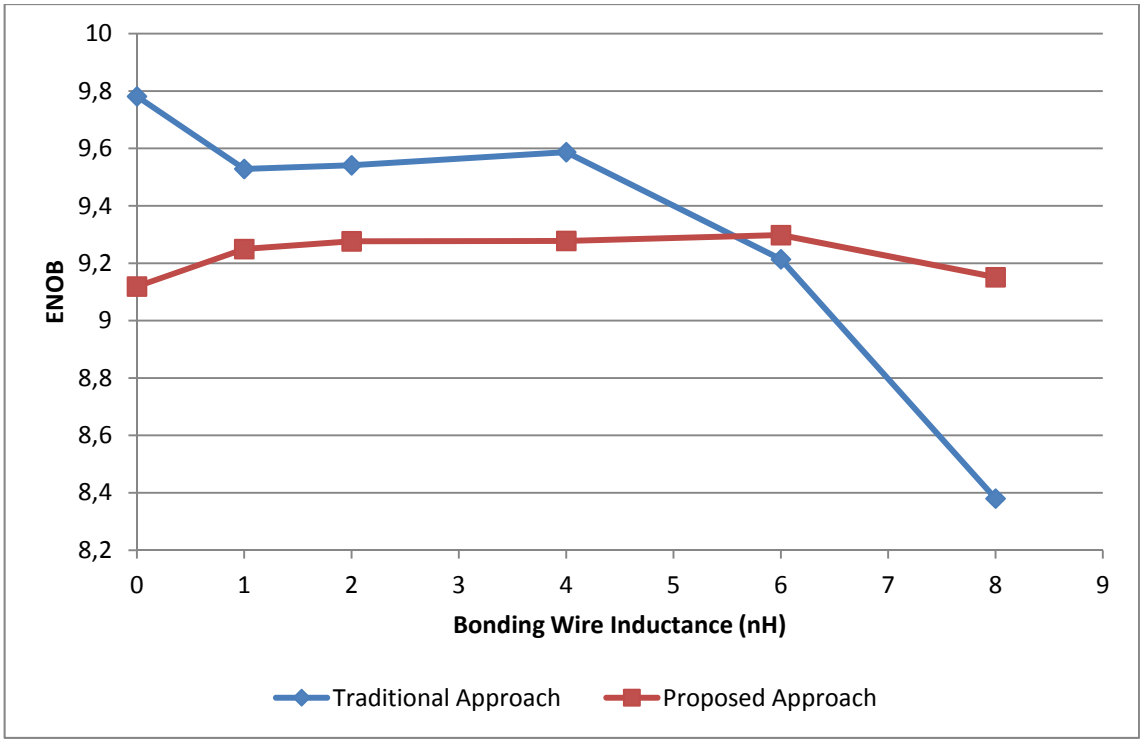
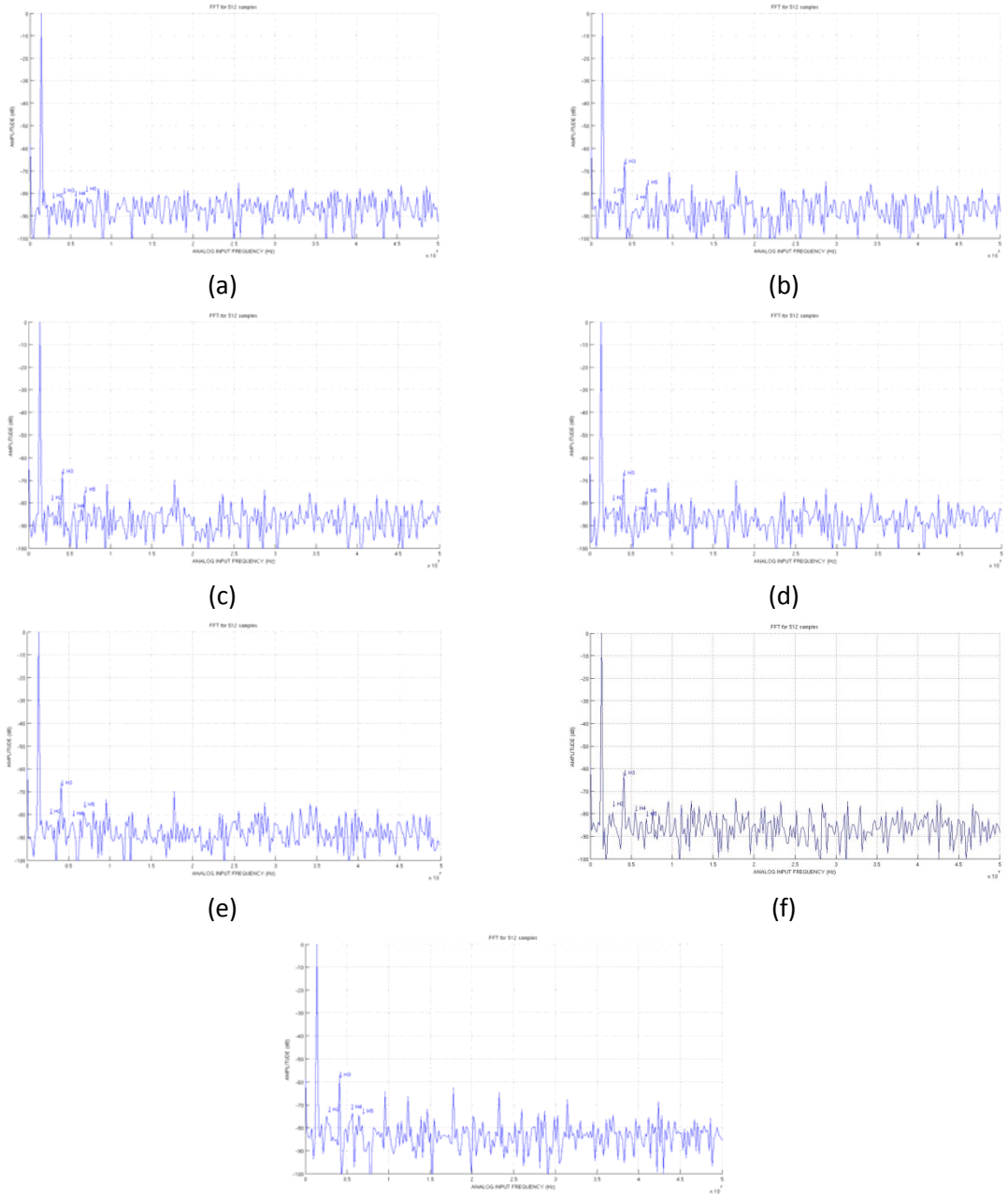


Figure 6.2.1 – Graphical comparison between approaches



(a) (b) (c) (d) (e) (f) (g)

Figure 6.2.2 – Traditional ADC design output spectrum at $F_S = 100MS/s$: (a) 0nH, (b) 1 pH, (c) 1nH, (d) 2nH, (e) 4nH, (f) 6nH, (g) 8nH

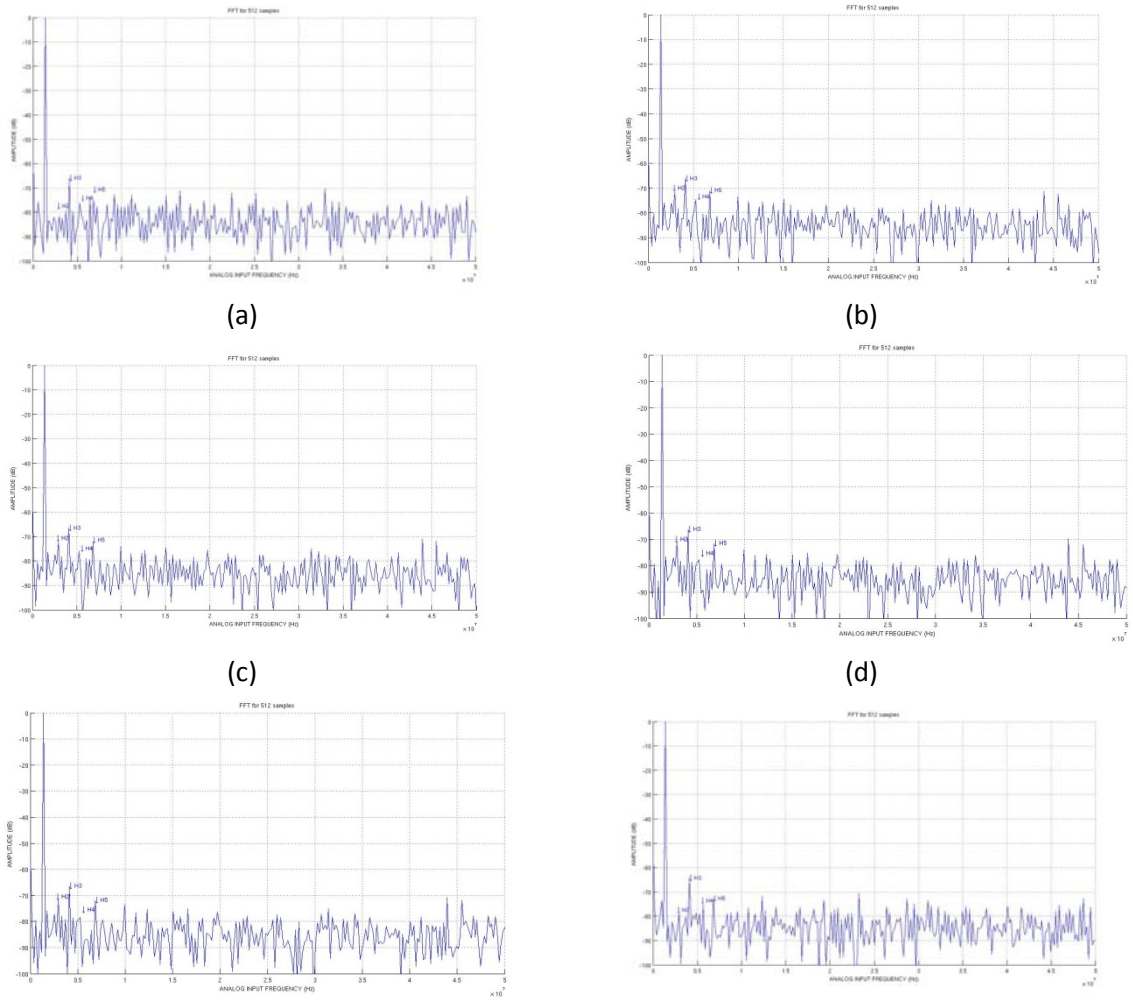


Figure 6.2.3 – Proposed ADC design output spectrum at $F_S = 100MS/s$: (a) 0nH, (b) 1nH, (c) 2nH, (d) 4nH, (e) 6nH, (f) 8nH

7 – Conclusion and Future Work

In this thesis a 1.5-bit MDAC circuit for pipeline ADCs and a current controller were proposed. The MDAC circuit uses a cascaded switched-current source to inject charge into the virtual ground of the amplifier during the amplification phase which allows proper reference level shifting in the MDAC. By using a current source for reference level shifting, with an appropriate current value, it is possible to replace the two single-ended reference voltages traditionally used in conventional MDAC circuits.

The appropriate current value is given by the current controller which uses a 1:1 replica of a pipeline stage, a discrete integrator and a biasing circuit. The 1:1 scale replica is needed for high resolution pipeline ADCs using this technique because of several errors that occur in the signal path, for example, the injector switch channel charge injection and the charge transfer between the injector circuit and the switched-capacitor circuit. The inputs of the scaled replica are grounded and only current is being injected into the switched-capacitor network. The discrete integrator has the function of comparing the replica stage output with the differential reference voltage, they should be equal. The biasing circuit will convert the scaled replica stage output into a current value for the next

calibration cycle. The biasing circuit output is used in the normal pipeline stages and the scaled replica stage.

In order to verify the functionality and performance of the new MDAC circuit, two 10-bit 40 MS/s ADCs, one based on the traditional MDAC circuit and the other based in the proposed MDAC circuit, were extensively simulated. During these simulations the proposed approach could not achieve a similar performance using manual calibration for the current value, so the current controller was implemented and the current injection period was shortened by using a mono-stable circuit to control the injector switches. By employment of these techniques the results show that, both ADCs achieve similar dynamic performance for about the same power dissipation. Hence, the proposed approach allows obtaining lower power dissipation, by eliminating the need for power hungry and design challenging reference voltage circuitry.

The power dissipation is not the only problem that the reference voltage circuitry has; this circuit is dependent to the bonding wires connecting the buffers output to the off-chip decoupling capacitor. Mathematical models show that an error above 5 mV in the differential reference voltage could cause the ADCs ENOB to drop significantly. The error caused by bonding wires is related with the sampling frequency, the wire length and its properties, this relation is not a linear. In theory the replacement of the two single-ended reference voltages traditionally used in conventional MDAC circuits can reduce the effects caused by this type of errors since the only current draw from these sources goes to the Flash quantizers. In order to verify the functionality and performance of the new MDAC circuit regarding this type of error, two 10-bit 100 MS/s ADCs, one based on the traditional MDAC circuit and the other based on the proposed MDAC circuit, were extensively simulated. A simulation of a small inductance values was performed to verify how much the ENOB of the traditional approach is affected in the presence of the bonding wire in the reference voltage circuitry. It war verified that this system's ENOB dropped by 0,3 bits. The remaining results show that while both ADCs achieve similar dynamic performance for bonding wire inductance value up to 6 nH, an 8 nH value for the bonding wire's inductance causes an approximated ENOB degradation of two bits

while the ADC based on the proposed approach maintains a similar dynamic performance for all other inductance values. An important aspect to refer is that while both ADCs have a similar dynamic performance the degradation behavior of this performance is very different between the two approaches. In the traditional approach the ENOB sees an immediate degradation by only having present a bonding wire inductance value, while the dynamic performance of the proposed approach maintains almost constant to the variations of the bonding wire length.

The proposed approach still requires a deeper analysis regarding the extra error sources introduced. Because of the nature of these errors, some of these analyses were performed using approximations. Earlier mathematical models for a 2.5-bit MDAC using the proposed approach show improvements related to the current error that propagates through the pipeline.

For simplifying this thesis the relation between a pipeline stage and the replica stage of the current controller was 1:1, so further study is necessary regarding this point because it is possible to optimize the replica stage area and the current error needed for a specific ADC resolution.

Another important aspect to be studied is a way to do the current value calibration using the pipeline stage by removing the replica stage, thus reducing the total area occupied by the ADC. This concept has a more complex phase generator and has problems with OPAMP memory effects.

Previously discussed was the slew-rate problem caused by a single injector circuit, which introduces an almost unrecoverable error in the OPAMPs output. If this circuit is not design taking into account the extra current necessary for reference shifting, ADC performance degradation is certain. This leaves only two options for a designer that wants to use this technique on a already designed pipeline ADC: a dual injector circuit based on a PMOS and NMOS injector circuit. Even this dual injector circuit can be done following two different approaches: one based on this concept but instead of only having the current being pulled from the OPAMP in the other OPAMP, input node a PMOS injector circuit is injecting current through the switched capacitor circuit in direction of the OPAMP. And the other approach has the PMOS injector circuit connected to the OPAMP output node through where the current is being pulled. With the introduction of dual injector circuits the current

controller also needs to be redesigned to accommodate the new current reference shifting and its calibration.

For future implementations based on this work several improvements are needed. Like previously said it is necessary to improve the OPAMP design so it can handle the single injector circuit more efficiently. Using [31] it is possible to optimize the OPAMP slew-rate behavior to the presence of the single injector circuit. The 1.5-bit Flash ADC needs to be redesigned because it limits the ADC's sampling rate to a maximum of 150 MS/s at a resolution of 10 bits. The injector circuit and the current controller present in this work have a maximum sampling rate of 400 MS/s by design but after 300 MS/s the proposed ADC ENOB will start to degrade.

Appendix

A – Submitted Papers

A.1 – MIXDES 2011

Design of a 10-bit 40 MS/s Pipelined ADC using 1.5-bit with Current-Mode Reference Shifting

Design of a 10-bit 40 MS/s Pipelined ADC Using 1.5-bit with Current-Mode Reference Shifting

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Abstract—**This paper presents a 1.5-bit MDAC circuit to be used in pipeline ADCs which employs a switched-current source to perform the reference shifting of the MDAC (the 1.5-bit digital-to-analog function). In the proposed circuit, the two single-ended reference voltage sources that are traditionally used (V_{REFP} and V_{REFN}), are replaced by a switched-current source. To evaluate and compare the performance of the proposed circuit, two 10-bit 40 MS/s ADCs, one using the traditional switched-capacitor (SC) MDAC and the other using the proposed MDAC, are designed. Simulation results show that the performance of the ADC with the proposed MDAC is enhanced since the power needed for the current sources is smaller than the power supplied by the reference voltage sources. Moreover, the proposed circuit does not require any reference voltage buffer, which can be difficult to design with relatively low power dissipation.**

Index Terms—**pipeline ADC; CMOS Technology; Switched-Capacitor; Current-Mode**

I. Introduction

High-resolution analog-to-digital converters (ADCs) with sampling rates in the range of 40 to 160MS/s are required for broad number of applications, ranging from high-resolution and high-speed imaging systems to the modern digital communication. When designing these ADCs low-voltage, low-power, and low-area are of great importance. One field that reflects the modern digital communication advances are mobile terminals, since they are single battery systems, so low power dissipation is necessary to ensure a reasonable battery lifetime. Another important factor is silicon area since it is directly related with the cost of the integrated circuit.

When very high conversion rates are required, the ADCs usually employ pipelining to relax the speed requirements of the analog components. Such architectures use a cascade of stages comprising a low resolution flash quantizer and a low resolution multiplying digital-to-analog (D/A) converter (MDAC), which computes and amplifies the residue to be quantized by the following stages [1]. The flash quantizer typically comprises a bank of comparators and the MDAC uses an amplifier (opamp) with a capacitor feedback network to provide linear voltage amplification. The MDACs usually employ a switched capacitor (SC) network to obtain the necessary closed-loop gain to implement the conversion algorithm. The DC offsets in the opamps and comparators do not affect the overall linearity of a pipeline ADC, if redundancy and proper output encoding (digital correction) are adopted [2]. Hence, the accuracy is mainly limited by the gain-error (GE) and static linearity errors (LE) of the MDAC in the first stages, caused by capacitor mismatch errors in the DAC and by finite DC gain of the residue amplifier. The accuracy required for the first MDAC is that of the overall ADC and it is progressively relaxed in subsequent stages.

The best resolution per stage for pipeline ADCs using digital correction is 1.5 bit [3], this means that the MDAC circuit has three voltage levels. These levels can be obtained using only one differential reference voltage ΔV_{REF} (which is generated from 2 single-ended reference voltages, $+V_{REF} = V_{REFP}$ and $-V_{REF} = V_{REFN}$). The reference voltage distribution in the design can cause trouble depending of the clock frequency and the ADC resolution. Another problem is the "double settling" caused by the same settling time of the opamp output and of the reference voltage. The approach used in [4] leads to a larger silicon area, but is still dependent of the package inductance and total ADC reference sampling capacitor.

The current drawn from the reference voltage buffer is clearly signal dependent and therefore the reference voltage buffer circuits should not have memory of the influence of previous samples processed by the ADC [5]. This can be very challenging to achieve in the case of high sampling frequencies because it requires either a very fast reference voltage buffer or bond wires with very low inductance. It is common, when computing the power dissipation of an ADC, to ignore the power dissipation of the reference voltage circuitry. However this power can be a significant fraction of the overall ADC power dissipation (up to 30% if the reference voltages are decoupled on-chip).

In this paper, we propose a novel 1.5-bit fully-differential MDAC that uses a switched current source to perform the reference shifting (the embedded 1.5-bit D/A function) of the MDAC. This new approach allows obtaining less overall power dissipation since reference voltage buffers have been avoided.

This paper is organized as follows. In Section II, a brief review of the pipeline architecture and the 1.5-bit MDAC and the proposed approach are discussed. Section III presents the simulation results for the two implemented ADCs, and finally, Section IV draws the main conclusions.

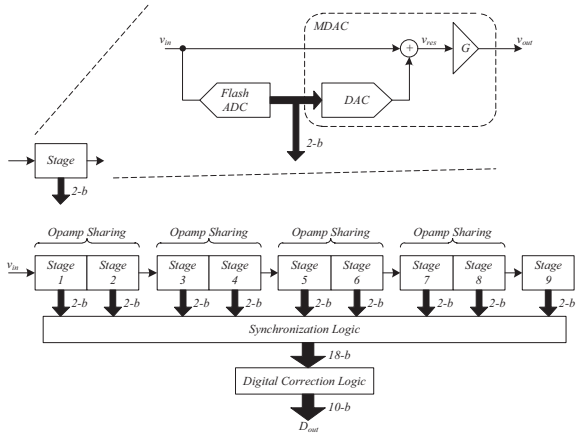

Figure 1. Block diagram of the architecture of the 10-bit 40 MS/s pipeline ADC used as the case-study for this work.

II. Pipeline ADC Architecture and Proposed MDAC Circuit

A. ADC Architecture Review

As stated before, high-speed and high-resolution ADCs usually employ pipelining to relax the speed and accuracy requirements of the analog components. A cascade of stages is used, where each stage comprises a low resolution flash quantizer and a low resolution MDAC, to compute and amplify the residue to be quantized by subsequent stages [2].

Fig. 1 shows the architecture of a 10-bit 40 MS/s pipeline ADC used as the case-study throughout this paper. The 10-bit ADC employs eight 1.5-bit/stages followed by a 2-bit quantizer at the end of the pipelined chain. The 18 output bits are digitally synchronized, and a net resolution of 10 bits is then available after digital correction.

B. Conventional MDAC Circuit

The conventional and well known 1.5-bit MDAC was initially proposed in [1] and it is shown in Fig. 2. This circuit operates in two clock phases. During ϕ_1, the input signal is sampled on capacitors C_{11} and C_{21} for the positive signal path, and on C_{12} and C_{22} for the negative signal path. During the residue amplification phase, ϕ_2, C_{11} and C_{12} are inserted in the feedback loop and the charge stored on C_{21} and C_{22} is redistributed with the former capacitors. For equally sized capacitors, the resulting differential output voltage at the end of ϕ_2, will be two times the differential input voltage sampled in ϕ_1. In addition, the output voltage will be affected by a reference level shifting equal to $+V_{REF}$ (or $-V_{REF}$) if the MDAC operation mode is X (or Z). The X, Y, and Z operation modes are defined by the local 1.5-bit quantizer. In Fig. 1, X*2 (using X = 1 as an example) indicates that the respective switches only close if the MDAC is in X operation mode and the current phase is ϕ_2.

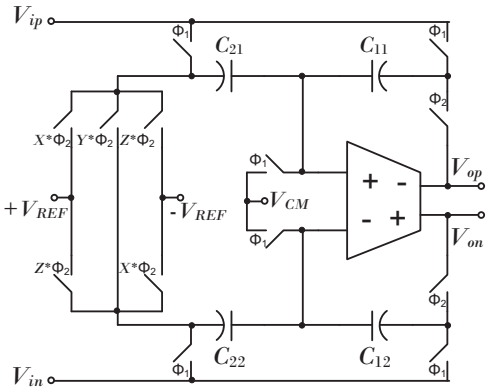

Figure 2. Conventional fully-differential 1.5-bit MDAC.

As a result, the desired 1.5-bit MDAC characteristic is ideally given by

$$\Delta V_{out} = 2 \cdot \Delta V_{in} + B \cdot \Delta V_{REF} \quad (1)$$

where $\Delta V_{out} = V_{op} - V_{on}$, $\Delta V_{in} = V_{ip} - V_{in}$, and B = {+1 (if X = 1), 0 (if Y = 1), -1 (if Z = 1)}. Through this characteristic two sources of error may be found. The first is related with the gain term affecting ΔV_{in}, which should ideally be 2, and the other with the reference level shifting term of ΔV_{REF}, which should be {+1, 0, -1} (this second term implements the local 1.5-bit D/A function for the residue calculations). The error related with ΔV_{REF} is of minor importance, as long as V_{REF} is provided by a reference bandgap circuit (i.e., very stable over time) and digital correction logic (DCL) is employed [2]. In [2] it is shown that DCL can correct both comparator offsets and level shifting errors up to ±1/2 LSB (as long as the MDAC residue characteristic maintains its symmetry).

C. Proposed MDAC

The proposed approach is based on the concept of a current source connected to a capacitor (C) during a certain time interval (T), injects a constant amount of charge into the capacitor. The voltage change, ΔV_C, in the capacitor can be calculated using:

$$\Delta V_C = \frac{1}{C}\int_0^T i(t)dt \quad (2)$$

Assuming that the current is constant and solving equation (2) for obtaining the current needed for emulating a specific reference voltage, yields:

$$I_p = \frac{C}{T}V_{REF} \quad (3)$$

The desired 1.5-bit MDAC characteristic becomes,

$$\Delta V_{out} = 2 \cdot \Delta V_{in} + B\frac{I_p.T}{C} \quad (4)$$

where C is the feedback capacitor (C_{12} or C_{11}), T is the period of the amplification phase, and I_p is the current.

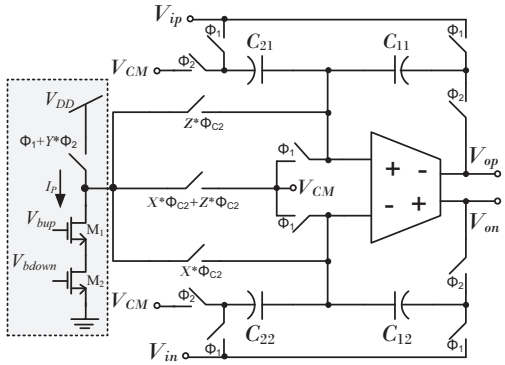

Figure 3. Proposed fully-differential 1.5-bit MDAC using a switched current source composed of transistors M_1 and M_2.

The proposed MDAC is shown in Fig. 3. Basically the two single-ended reference voltage sources ($+V_{REF}$ and $-V_{REF}$) are replaced with a cascoded switched-current source composed of transistors M_1 and M_2. The phenomenon responsible for the level shifting in the proposed MDAC is the injection of current in the switched capacitor circuit as explained above.

The level shifting occurs (during ϕ_2) when current source I_p is turned on. This current source sinks current through the feedback capacitors changing the output voltage by an amount proportional to the respective current, feedback capacitance and duration of ϕ_{C2}. By the end of ϕ_2 the output voltage should have changed by an amount equal to V_{REF} (differentially). Regarding the output waveforms, in Y operation mode the output voltage has an exponential waveform (its operation in Y mode is identical to that of the conventional MDAC), but for X and Z operation modes, the output has a ramped integrating characteristic until the end of ϕ_{C2}. During ϕ_1 the current source is not connected to the circuit, it is connected to V_{DD} in order to guaranty that the current I_p is as close as possible to the desired value obtained using equation 3. The clock phases necessary to the operation of the MDAC circuit are shown in Fig. 4. Phases ϕ_{C1} and ϕ_{C2} are responsible for controlling the current injection.

The cascoded current source only draws current from V_{DD} during the time interval when it is not connected to the SC network (phase ϕ_1), and, simultaneously, when Y is enabled. When it is connected to the virtual ground of the amplifier (phase ϕ_2), it simply draws current from the amplifier. The amount of charge supplied by the amplifier during this time is the same in both MDAC circuits, since the output voltage will be the same. Therefore, the current source does not increase the power dissipation of the ADC during this phase. The only time when the current source dissipates extra power is when it is connected to V_{DD}.

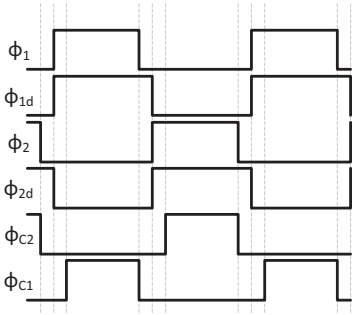

Figure 4. Clock phases necessary to the operation of the proposed MDAC.

III. Simulation Results

In order to verify the behavior of the proposed MDAC circuit and compare it to the behavior of the traditional MDAC circuit, two 10 bit 40 MS/s ADCs were implemented using a 0.13 µm CMOS technology and simulated using Spectre simulator. These implementations use an electrical model for the amplifiers with a single dominant pole with a DC gain of 85 dB and a gain-bandwidth product (GBW) of 350MHz. All other elements in both pipeline ADCs are made with real devices, including logic circuits, clock-phase generation circuitry and switches. All switches in the signal path employ clock boosting techniques in order to reduce the signal distortion. All capacitors have a nominal capacitance value of 1 pF. The V_{CM} voltage is set to 0.6 V and the differential reference voltage of the ADC ($\Delta V_{REF} = V_{REFP} - V_{REFN}$) is set to 0.4 V. In the case of the ADC employing the traditional MDAC ΔV_{REF} is obtained through two single-ended reference voltages of 0.4 V (V_{REFN}) and 0.8 V (V_{REFP}). In the case of the ADC implemented using the proposed MDAC, the correct ΔV_{REF} is obtained by adjusting the value of the current according to equation 3.

Both ADCs, were simulated using transient-noise analysis and for an input sine wave signal with amplitude -1 % of the full-scale and a frequency value of 1 MHz. The output spectra of both ADCs are depicted in Fig. 5 and Fig. 6, for the conventional MDAC and for the proposed MDAC, respectively. From these spectra the performance parameters for both ADCs were calculated, and are summarized in Table I.

TABLE I. Simulated ADCs performance

	SNR	*THD*	*SFDR*	*SNDR*	*ENOB*	*Power*
Traditional MDAC	61.177	-65.826	71.561	59.897	9.6573	18.6 mW
Proposed MDAC	60.154	-64.217	70.114	58.867	9.4929	18.3 mW

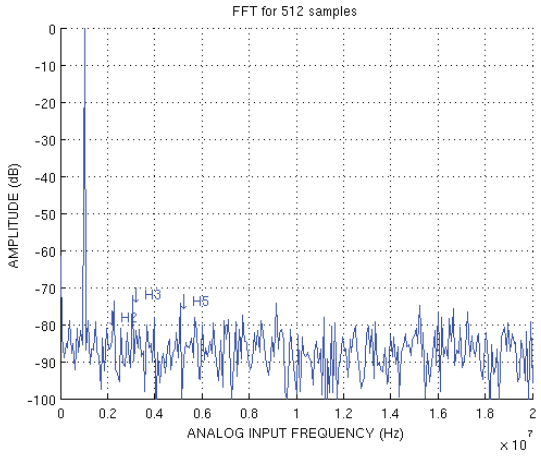

Figure 5. 512-point FFT of the ADC using the conventional MDAC at F_S = 40 MS/s (coherent sampling).

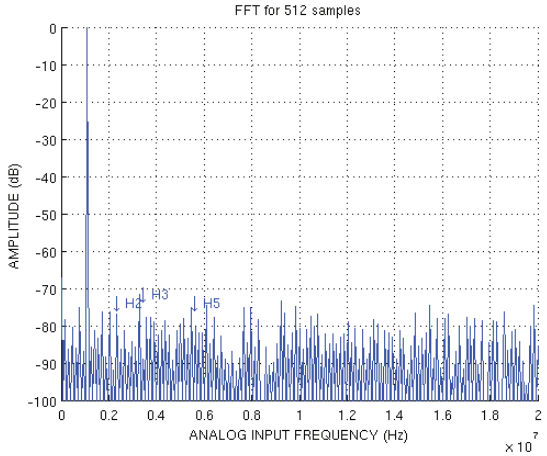

Figure 6. 512-point FFT of the ADC using the proposed MDAC at F_S = 40 MS/s (coherent sampling).

The simulation results show that the proposed MDAC circuit is capable of achieving a performance similar to the performance of the traditional MDAC circuit.

The power dissipation of the reference generation circuitry results are shown in Table II. In the case of the ADC using the traditional MDAC circuit, the reference voltage sources ($+V_{REF}$ and $-V_{REF}$) supply a total power of 578 µW to the ADC. In the case of the ADC using the proposed MDAC circuit, the V_{DD} voltage source connected to the current sources inside the MDAC circuits dissipate a total of 447 µW. However, when analyzing these results it is necessary to take into account that the reference voltage sources used in the traditional MDAC are, in fact, built using reference buffer circuits. These circuits are normally difficult to design, since they must have a very high bandwidth (GBW) in order to guarantee that the reference voltage can settle to a value better than ± 0.25 LSB@10-bit of the ideal value within the available sampling time (< 12.5 ns). This means that the reference buffers will dissipate more power than the power they supply to the ADC. When the reference voltages are decoupled on-chip, the extra power dissipated by the reference buffers is normally of the order of (up to) 30 % of the total power of the ADC.

TABLE II. POWER DISSIPATION OF THE REFERENCE CIRCUITRY (THE POWER FROM THE REFERENCE VOLTAGE BUFFERS REQUIRED FOR THE CONVENTIONAL MDACS ARE NOT INCLUDED)

	Proposed MDAC		**Traditional MDAC**		
	I_p	**Total**	$+V_{REF}$	$-V_{REF}$	**Total**
Power	55.86 µW	446.88 µW	383 µW	195.5 µW	578.5 µW

IV. CONCLUSIONS

In this paper a 1.5-bit MDAC circuit for pipeline ADCs was proposed. This circuit uses a cascoded switched-current source to inject charge into the virtual ground of the amplifier during the amplification phase which allows proper reference level shifting in the MDAC. By using a current source for reference level shifting, with an appropriate current value, it is possible to replace the two single-ended reference voltages traditionally used in conventional MDAC circuits. In order to verify the functionality and performance of the new MDAC circuit, two 10-bit 40 MS/s ADCs, one based on the traditional MDAC circuit and the other based in the proposed MDAC circuit, were extensively simulated. The results show that, both ADCs achieve similar dynamic performance for about the same power dissipation. Hence, the proposed approach allows obtaining lower power dissipation, by eliminating the need for power hungry and design challenging reference voltage circuitry.

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Current-Mode Reference Shifting Solution for MDAC-based Analog-to-Digital Converters

Current-Mode Reference Shifting Solution for MDAC-based Analog-to-Digital Converters

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***Abstract*—This paper presents a current-mode reference shifting solution for MDAC-based ADCs that eliminates the need for external or internal reference voltage buffers, thus improving the energy efficiency of the combined ADC and reference circuitry. The solution consists of using an NMOS current source connected to the opamp's inputs, where reference shifting occurs by pulling a current through the capacitor in the opamp's feedback loop during the amplification phase, thus, emulating a voltage shift, $\mathbf{\Delta V = (I\Delta t)/C}$. The amount of necessary current, i.e., the biasing of the current source is achieved by a replica of a pipeline stage, which is followed by an integrator and the biasing circuit all connected in a negative feedback loop. To illustrate the solution's performance, two 10-bit 100-MS/s pipeline ADCs were implemented: one based on the conventional 1.5-bit MDAC and the other based on the proposed circuit. Simulation results show the functionality of the proposed circuit and results for different wirebond inductances prove the stability and performance of the proposed solution.**

I. Introduction

High resolution pipeline analog-to-digital converters (ADCs) with sampling rates within the tens to hundreds of MS/s are required in a broad area of applications with enhanced performance, ranging from high quality imaging systems to modern digital communication systems (e.g., medical imaging, WiMax, HDTV, mobile devices, etc.) [1], [2]. Low voltage operation, low power dissipation and small silicon area are of great importance in the design of these ADCs. Low power permits longer lasting battery operated devices, while small area directly relates to lower fabrication costs.

A fundamental, but often unreferenced building block of pipeline ADCs are reference voltage (V_{REF}) circuits. These circuits generate, buffer, and decouple reference voltages that need to settle to the linearity of the ADC to avoid distortion and interstage gain errors [3]. Achieving this usually leads to power hungry and large area V_{REF} circuits, which become one of the most power consuming blocks of pipeline ADCs (alongside opamps). This problem becomes particularly exacerbated with increasing sampling frequencies, as the effect of the wirebond's inductance (in conjunction with the pad/pin's parasitic capacitance) severely degrades performance. In the literature many solutions (as will be shown in the following section) can be found, but most of them either increase power, area, or, as in most cases, both. Furthermore, the power and area of V_{REF} circuits are often omitted and unaccounted in the total power and area. Therefore, given today's demands for low power and small area circuits, voltage reference shifting, characterized by power hungry buffers, large capacitors, and instability caused by wirebond inductance, does not fit today's needs.

This paper attempts a shift in paradigm by proposing a current-mode reference shifting multiplying-DAC (MDAC) circuit. We propose a complete integrated solution to substitute reference voltages in the MDACs of pipeline ADCs, where these voltages are more crucial. To evaluate the solution's functionality, and performance, two 10-bit 100-MS/s pipeline ADCs are designed in a standard 0.13 μm CMOS technology. The stages of one ADC are based on the conventional and well known 1.5-bit MDAC [4], while the other ADC employs the proposed MDAC circuit in all its stages.

II. Reference Voltage Circuit Strategies

Reference circuits are essential in analog and data converter systems. They generate reference voltages and currents that are used to bias circuits, signal comparison, addition and subtraction operations, among others. In the specific case of data converters, reference circuits are determinant in defining the input and output full-scale ranges. Therefore it is necessary to guarantee a sufficient level of accuracy so that the overall performance of the data converter is not limited[1]. To achieve this, they need to be independent of external conditions such as, process, supply voltage, temperature, and load disturbances. In the case where a reference voltage needs to drive a large capacitor (or various capacitors amounting to a large capacitance), or be used in a high speed or high accuracy switched capacitor (SC) circuit, an additional block, needs to be added to the output of the reference circuit, a buffer. This block is used to maintain the reference voltage constant and stable, and guarantee that its output settles to within a given error, within a given time slot, which depends on the accuracy and speed of the converter.

It is possible to find many forms of reference voltage circuits and buffering schemes in the literature. The options divide into on- and off-chip buffering with (or without) the use of on- and off-chip damping resistors and decoupling capacitors.

[1]In [9] it is shown that V_{REF} can have 1-bit lower accuracy than the accuracy of the ADC.

TABLE I
DESCRIPTION AND ANALYSIS OF THE ADVANTAGES AND DRAWBACKS OF COMMONLY FOUND VOLTAGE CIRCUIT STRATEGIES.

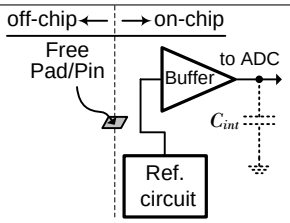
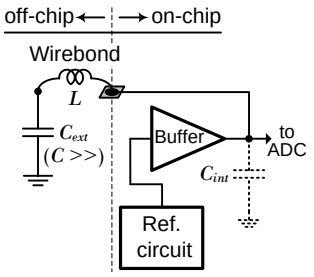
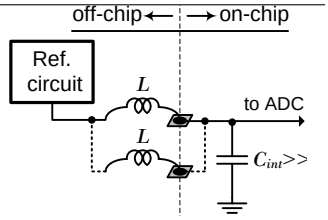
Analysis	Diagram
(a) On-chip buffer with/without internal decoupling [2], [5]	
High speed buffer with wide bandwidth. High power consumption. Noise performance hard to achieve (as frequency rises, output impedance rises). Wirebond inductance too large for off-chip decoupling. Large on-chip capacitors, occupying large area, unavoidable.	
(b) On-chip buffer with external decoupling [1], [3], [6], [7]	
Low bandwidth buffer. Low power consumption. Noise performance and output impedance dependent on quality (ESL and ESR) of decoupling capacitors. Wirebond inductance causes ringing of the internally generated reference voltage. Dampen ringing with large on-chip capacitors and resistors (occupying large area). Reduce inductance with special packaging [1]. Additional pins.	
(c) Off-chip reference with internal decoupling [8]	
Use large on-chip capacitors to dampen the ringing caused by wirebond (occupying large area). For low inductance more pads must be used. Additional pins. Internal decoupling capacitor may be larger than converter itself [8].	

Table I describes and analyses the advantages and drawbacks of the most common forms of V_{REF} circuitry. The conclusions extracted from Table I can be summarized as follows: the reference circuit will occupy a large area, will dissipate a large amount of power, and/or will need at least one extra pin. Most of the currently employed solutions suffer from a combination of these disadvantages, while the solution proposed in this paper solves these limitations by precluding buffers, large on- and off-chip decoupling capacitors, and no extra pins are necessary.

III. PROPOSED SOLUTION

As already mentioned, a current-mode reference shifting technique is employed to substitute reference voltages and associated circuitry. The objective is to emulate the effect of a reference voltage, which can be achieved using a capacitor, a current, and a certain amount of time, i.e., $\Delta V = I\Delta t/C$. In an SC-MDAC circuit, two of the three mentioned items are readily available: the capacitor is the one found in the opamp's feedback loop, the maximum time available is the amplification phase, and only a current source needs be added to the circuit (substituting the reference voltage). To control the amount of current for correct reference shifting, a replica

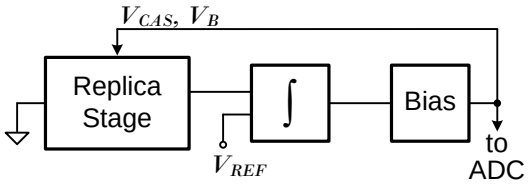


Fig. 1. Block diagram of the global reference shifting current controller.

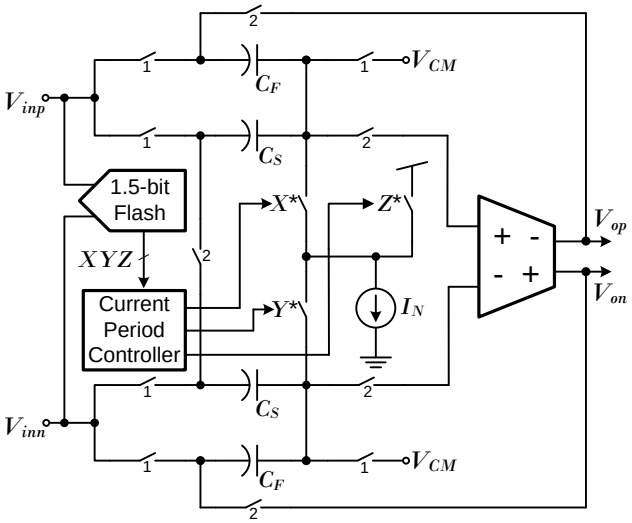


Fig. 2. Proposed current-mode reference shifting MDAC with 1.5-bit flash quantizer and current period controller.

stage followed by an integrator in a negative feedback loop are used, as shown in Fig. 1[2].

The following describes the proposed MDAC and the blocks used to achieve accurate reference shifting in current mode.

A. Current-Mode Reference Shifting MDAC

The differential circuit of the proposed MDAC is shown in Fig. 2. As should be noticed the architecture is similar to the conventional MDAC, except for the addition of three switches for current control and current injection, and the removal of switches responsible for voltage reference shifting. During ϕ_1 the input is sampled on the capacitors. During ϕ_2 three situations may occur: if Z mode is active, only charge redistribution occurs between C_S and C_F (gain of two), and the current flows from V_{dd} directly to V_{ss}[3]; if X is active the current source connects to the noninverting input of the opamp and thus sinks current that flows through the top C_F capacitor; if Y is active, the current source connects to the inverting input of the opamp and sinks current through the bottom C_F capacitor. In both X and Y modes, the current comes from the opamp. The switches used to control the current sinking are transmission gates due to the common-mode value at the opamp's input, and they are controlled by the flash quantizer's outputs (X, Y, or Z). An NMOS cascode current source is

[2]The V_{REF} of Fig. 1 does not need to be buffered.

[3]The current source never turns off to avoid long turn-on times and a floating current source.

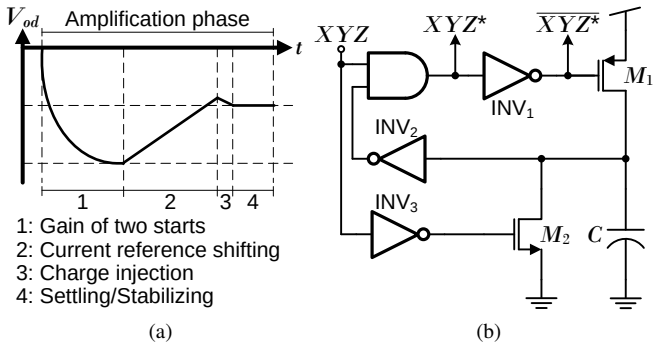


Fig. 3. (a) MDAC timing diagram. (b) Current shifting period controller.

used for reduced sensitivity to variations of the voltage at the opamp's input.

The output waveform, in X and Y modes, has a ramped characteristic, which introduces three limitations: charge injection of the current control switches, opamp's slew-rate and output common-mode (CM) voltage. The slew-rate is solved by proper design of the opamp, while the other two issues are solved by reducing the period the current source is on. By reducing this period, the global reference shifting controller (discussed further on) has time to account for charge injection and adequately control the amount of current sunk, thus minimizing the effect of the switches' charge injection. Moreover, a shorter current shifting period allows the opamp's output voltage to settle, stabilizing its CM voltage, before being sampled by the following pipelined stage. A timing diagram of the MDAC's operations, illustrating the current shifting period and settling/stabilizing period is shown in Fig. 3a.

The circuit responsible for generating a shorter phase within ϕ_2 is described next.

B. Current Shifting Period Controller

The controller, as shown in Fig. 3b, initiates operation with the capacitor, C, discharged. The input, represented by X, Y, or Z, goes from 0 to 1, which causes the output (XYZ^*) to rise, because INV_2's output is also high. This output connects to the MDAC's transmission gates and current sinking is initiated. Simultaneously, M_1 turns on and charges C until INV_2 switches and its output becomes zero. This causes XYZ^* to fall, terminating the current sinking period. When the input falls, at the end of ϕ_2, M_2 turns on, discharging the capacitor.

The capacitor and $M_{1,2}$'s on-resistance (R) determine the charging/discharging time constant, $\tau = RC < 1/2F_S$, where F_S is the ADC's sampling frequency.

C. Replica Stage

To determine the correct amount of current necessary to perform reference shifting, a global reference shifting controller, composed of a replica of a pipeline stage (RS) and a discrete SC-integrator, is used (Fig. 1). These two circuits operate together to generate the biasing voltages for the cascode current mirrors and sources of all the ADC's stages. Here the RS will be discussed.

As the name indicates the RS is an exact copy of a pipeline stage. It is, in fact, a copy of two pipeline stages with shared opamp because the ADC also uses a opamp sharing technique. Any deviations or changes to the circuit's nominal operation will be reflected in this RS, and therefore, corrected. The replica circuit helps minimizing issues caused by charge injection of the MDAC's current control switches, duty-cycle mismatch from 50 %, and undesired parasitic effects (opamp's input, etc.). Scaling of the RS is possible, naturally with corresponding degradation of reference shifting accuracy ($2\times$ scaling is still acceptable at the 10-bit level).

The RS always operates in Y mode, therefore, it always performs reference shifting. The MDAC of the RS has its inputs connected to the analog ground (therefore sampling 0 V), while its outputs are connected to the integrator and compared with the desired reference shifting value (which depends on the full-scale range of the ADC). The flash quantizer of the RS has at its inputs a voltage such that it always produces $Y = 1$, thus, forcing the MDAC to perform reference shifting.

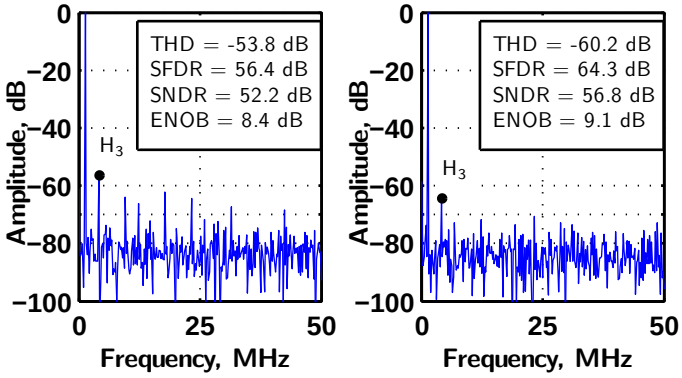
D. Discrete SC-Integrator

The outputs of the RS are connected to the SC-integrator and are compared with the desired reference shifting voltage. The output of the integrator drives a current mirror of the biasing circuit to produce two biasing voltages, V_{CAS} and V_B. These voltages drive the current source of the RS (and all other stages of the ADC) in a negative feedback loop. This calibration scheme allows to continuously adjust the biasing voltages until the desired reference shifting is achieved, taking into account all the nonidealities of a pipeline stage. A conventional parasitic-insensitive SC-integrator is employed.

IV. Simulation Results

As mentioned before, two 10-bit pipeline ADCs were designed in a standard 0.13 μm CMOS technology, one using the conventional MDAC in each stage (and two reference voltages), and the other using the proposed MDAC with global reference shifting controller (no scaling of this circuit was performed). Both converters are composed of eight 1.5-bit stages and a final 2-bit stage, followed by a digital backend of synchronization and correction logic. Opamp sharing between successive stages was used. All building blocks of both ADCs were implemented using real circuits, except for the opamp, where an electrical model with 66 dB DC gain and 1 GHz GBW was employed. For the SC-integrator, a 60 dB DC gain and 100 MHz GBW opamp was used. All main capacitors have 1 pF, the ADC's CM voltage is 0.6 V, and the differential reference shifting is 0.4 V. Regarding the calibration time of the proposed ADC, the worst-case was simulated to be approximately 2 μs.

The circuit used to model the wirebond, pad, and reference circuit is similar to that of Table Ib and is composed of an on-chip V_{REF} with a 2 pF pad parasitic capacitance, a series



(a) (b)

Fig. 4. 512-point FFT at 100 MS/s for 1 MHz input signal and $L = 8$ nH of (a) Conventional ADC, (b) ADC using proposed current-mode reference shifting solution.

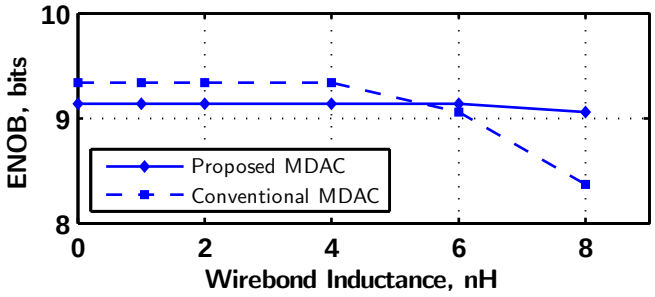


Fig. 5. ENOB vs wirebond inductance at $F_S = 100$ MS/s.

RL for the wirebond ($R = 5\ \Omega$), and an off-chip decoupling capacitance of 5 pF.

The FFTs of Fig. 4 illustrate the degradation caused by an 8 nH wirebond. Distortion and the rise of spurious tones are clearly visible in the conventional ADC's FFT, resulting in an ENOB of 8.4 bits[4], compared to 9.1 bits of the proposed ADC. At this sampling frequency, the reference shifting current was 168 μA per stage. Fig. 5 shows the ENOB of both ADCs for various inductance values, where for $L > 4$ nH the degradation becomes pronounced. The ENOB of the proposed ADC maintains constant for all inductance values. Through simulations, it was verified that for $F_S < 100$ MS/s, the inductance effect is almost irrelevant, at least for the inductance values considered (0-8 nH). A larger degradation in performance is expected for $F_S > 100$ MS/s. Furthermore, as F_S increases, lower inductance values will become more problematic.

To compare the two ADCs in terms of energy efficiency, their power consumption needs to be determined. The simulated power of the conventional and proposed ADC was 18.3 mW and 18.7 mW, respectively (which excludes the opamps as these were ideal). It was estimated that 1 mW opamps would suffice for each opamp of both ADCs. Therefore, the power of the conventional ADC is estimated to be 24.3 mW, which represents its simulated power, 4 opamps (eight stages with opamp sharing), and 2 opamps (to buffer each reference voltage). The proposed ADC's power consumption is 24.7 mW, which can be separated into simulated power, 4 opamps, replica stage opamp, and integrator opamp. Practically the same power consumption is obtained, as the power of the buffers is used for the power of the replica stage and integrator. However, in terms of FoM $= P/(2^{\mathrm{ENOB}} F_S)$, the proposed ADC achieves 450 fJ/conv.-step, as opposed to 720 fJ/conv.-step of the conventional ADC (using the above mentioned ENOB values).

Therefore, the proposed current-mode reference shifting solution will become a good contender to be employed in high-speed medium-to-high resolution pipeline ADCs.

[4]The conventional ADC recovers its ENOB to over 9 bits for a 10× larger decoupling capacitance, 50 pF.

V. Conclusion

This paper presented an overview of common reference voltage circuit techniques and proposed a complete current-mode reference shifting solution for high-speed medium-to-high resolution pipeline ADCs. The solution proposes eliminating voltage reference circuitry, which includes power hungry opamps, large on- and off-chip decoupling capacitors, and the effects of the wirebond inductance. Therefore, this technique allows reducing the total power consumption and, fundamentally, the silicon area (and cost) occupied by the entire ADC (ADC + reference circuitry). Simulation results, of a conventional 10-bit pipeline ADC, show that for $F_S = 100$ MS/s, a wirebond with $L = 8$ nH reduces the ADC's ENOB by 1.5-bits. Using the proposed technique, the ADC's performance maintains constant, for a power consumption similar to the conventional ADC, therefore achieving an a much improved FoM.

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