FACULDADE DE CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

Departamento de Engenharia Electrotécnica e de Computadores

Projecto de um circuito conversor DC-DC para aplicações de "energy harvest"

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Resumo

Faculdade de Ciências e Tecnologia
Departamento de Engenharia Electrotécnica e de Computadores

Mestre em Engenharia Electrotécnica e de Computadores

por José David Lopes Lameiro

Esta tese apresenta um circuito conversor DC-DC ("step-up") para aplicações de *"energy harvest"*. Este circuito utiliza uma arquitectura *"Switched capacitor voltage tripler"*, controlada por um circuito MPPT baseado nos métodos *"Load Voltage Maximization"* e *"Hill Climbing"*. Este circuito foi desenhado usando a tecnologia "*0.13 μm CMOS*" de forma a funcionar com uma célula fotoeléctrica de "*a-silicon*". Este circuito tem uma fonte de alimentação local também controlada pelo mesmo circuito MPPT, que é uma réplica do conversor *"SC voltage tripler"*, redimensionado a 3% da área deste último. Este circuito utiliza a combinação de transístores PMOS e NMOS de forma a reduzir a área ocupada. Um esquema de reutilização de cargas é utilizado para compensar as grandes resistências parasitas associadas aos transístores MOS. Os resultados das simulações mostram que o circuito pode fornecer uma potência de 9636 μW à carga, utilizando uma potência de 1274 μW na célula fotoeléctrica, correspondendo a uma eficiência na ordem dos 75,66%. As simulações mostram também que o circuito é capaz de se iniciar com apenas 19% do nível de iluminação máximo da célula fotoeléctrica.

Palavras-Chave: Energy harvesting, conversor DC/DC, baixa potência, CMOS, Load Voltage Maximization, Hill Climbing.

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Abstract

Faculdade de Ciências e Tecnologia
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Mestre em Engenharia Electrotécnica e de Computadores

by José David Lopes Lameiro

This thesis presents a step-up micro-power converter for solar energy harvesting applications. The circuit uses a SC voltage tripler architecture, controlled by a MPPT circuit based on the Load Voltage Maximization and the Hill Climbing methods. This circuit was designed in a 0.13 μm CMOS technology in order to work with an a-silicon PV cell. The circuit has a local power supply voltage, created using a scaled down SC voltage tripler, controlled by the same MPPT circuit, to make the circuit robust to load and illumination variations. The SC circuits use a combination of PMOS and NMOS transistors to reduce the occupied area. A charge re-use scheme is used to compensate the large parasitic resistors associated to the MOS transistors. The simulation results show that the circuit can deliver a power of 9636 μW to the load using 1274 μW of power from the PV cell, corresponding to an efficiency as high as 75.66%. The simulations also show that the circuit is capable of starting up with only 19% of the maximum illumination level.

Keywords: Energy harvesting, DC/DC converter, low power, CMOS, Load Voltage Maximization, Hill Climbing.

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Abbreviations

AM1	Air Mass 1
ASM	Asynchronous State Machine
CMOS	Complementary Metal-Oxide Semiconductor
COX	Gate-oxide capacitance per unit area
DC	Direct Current
DSP	Digital Signal Processor
ITO	Indium Tin Oxide
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
NMOS	N-Channel Metal Oxide Semiconductor Field Effect Transistor
PMOS	P-Channel Metal Oxide Semiconductor Field Effect Transistor
PECVD	Plasma Enhanced Chemical Vapor Deposition
P&O	Perturb and Observe
PV	Photovoltaic
Rf-PERTE	radio-frequency Plasma Enhanced Reactive Thermal Evaporation
SC	Switched capacitor
VMPPT	Voltage-based Maximum Power Point Tracking
XNOR	Exclusive NOR

Chapter 1

Introduction

1.1 Background and Motivation

Energy harvesting or energy scavenging is the process by which energy is derived from external sources (e.g. solar power, thermal energy, wind energy, salinity gradients, and kinetic energy), captured and stored. Energy harvesting has an advantage over energy derived from fossil fuels or provided by batteries because it is a renewable type of energy, and more environmentally friendly. So, Energy harvesting devices convert ambient energy into electrical energy.

Looking around, there are plenty devices that could be more autonomous, i.e. it may not be practical to plug a device to a power grid, nor to use batteries, as they need to be replaced when their charge is depleted. And all of these devices have the same problem, so the question is how can they be powered without these restraints? The answer is: these applications can be powered by collecting the energy that exists in the surrounding environment (energy harvesting). By employing energy harvesting, circuits can virtually operate permanently. Although there are different ambient energy sources available, ambient light has the highest energy density when compared to other possible ambient energy sources [1] and it can easily be harvested by using photovoltaic (PV) cells.

A photovoltaic cell (which is essentially a diode) converts light energy directly into electrical energy. The output voltage of a single photovoltaic cell (PV) is at the most 0.7 V (under open circuit conditions) and can be as low as 0.4 V under maximum power condition. This means that it is necessary to have a voltage step-up (Figure 1-1) circuit that can increase

the PV voltage to acceptable values, in order to power a Complementary Metal-Oxide Semiconductor (CMOS) circuit (typically larger than 1.0 V).

A small size system will necessarily have a small PV cell which will limit the power available to the step-up converter.

Under low power conditions, it is feasible to use a capacitor based instead of an inductor based voltage step-up converter, allowing the reduction of the system size. Since the power and the voltage produced by a PV cell varies with the connected load and with the amount of incident light, it is necessary for the step-up to compensate for this variation in order to supply the maximum power available to the load. This means that the step-up converter should adjust its behaviour in order to track the maximum power point (MPP) of the PV cell. There are several methods available for determining the MPP of a PV cell (Figure 1-1). Most of these methods are not suitable for low power applications because they require complex implementations that dissipate a lot of power [2].

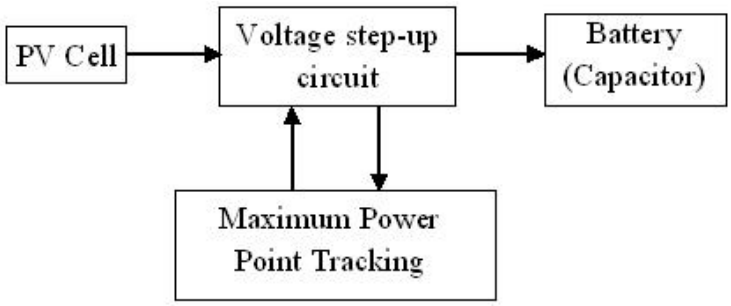

Figure 1-1: Block diagram of PV cell power management system

1.2 Thesis Organization

This thesis has been organized in seven chapters including this introductory one.

A section with the introduction, results and discussion of the Amorphous Silicon Solar Cell will be explained in Chapter 2. Also in Chapter 2, the Switched Capacitor DC-DC Converter will be introduced**.** A section with the circuit's overview of this study is also included.

Chapter 3 gives an in depth analysis about the Maximum Power Point Tracking used in this study. Starting with a theoretical analysis, where some different MPPT techniques will be explained and discussed. Finally, the techniques chosen for this work and the reasons behind it will be explained.

Chapter 4 will focus on the Phase generation and control, where all the relevant sub-modules of Phase Control circuit will be explained. A section with the explanation of Start-Up module is also included.

In Chapter 5, the results of some simulations in 130 nm CMOS technology will be presented.

Chapter 6 is reserved for overall conclusions and further research suggestions.

1.3 Contributions

Most of the existent Solar Harvest Systems are made to deliver medium or large amounts of Power (more than 1W). There is a lack of circuits that are able to work with Power levels smaller than around 1mW. The main contribution of this thesis is that it gives a solution for Solar Harvest Systems with an operating power below 1mW.

The present work has originated a paper (Appendix B) that was accepted for publication at the International Symposium on Circuits and Systems 2011 (ISCAS 2011).

Chapter 2

State of the art

This chapter will introduce an explanation of how the system globally works. The behavior of the amorphous Silicon solar cell will be described. A section with the results and discussion of this study is also included below. Some theory about Switched Capacitor DC-DC Converter will be also introduced.

2.1 Amorphous Silicon Solar Cell

2.1.1 Introduction

In order to reduce the size of the energy harvesting system, an a-Silicon PV cell was chosen, this cell was built by depositing amorphous silicon with a structure p/i/n on a glass previously covered with ITO (Indium Tin Oxide). The ITO was deposited using rf-PERTE (radio-frequency Plasma Enhanced Reactive Thermal Evaporation) and had a sheet resistance of 35 Ω/□. The active p-type, intrinsic and n-type layers were deposited using PECVD (Plasma Enhanced Chemical Vapor Deposition) and had a thickness of 150Å, 4500Å and 500Å respectively. The frontal aluminum electrode was deposited using thermal evaporation [3]. The die containing the step-up converter (and other circuitry) can be glued to the cell and connected to the PV cell terminals. The PV cell was experimentally characterized and an equivalent electrical model, shown in Figure 2-1 , was obtained.

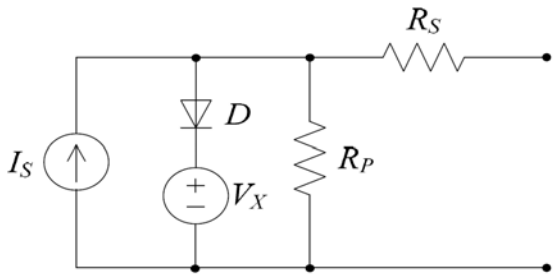

Figure 2-1: Equivalent electrical circuit of the amorphous silicon PV cell

2.1.2 Results and discussion

By simulation on Cadence, the cell has a short circuit current of about 5.9 mA, a maximum power of 1775 µW that occurs for a voltage of 403 mV (maximum power point) and an open circuit voltage of 652 mV. These data refer to a cell having an active area of about 1 cm^2, when irradiated according to AM1 (Air Mass 1) conditions (irradiance by the solar spectrum at the earth surface, having the Sun vertically located). The resulting power and current curves of the cell for AM1 and 20% of AM1 conditions are depicted in Figure 2-2.

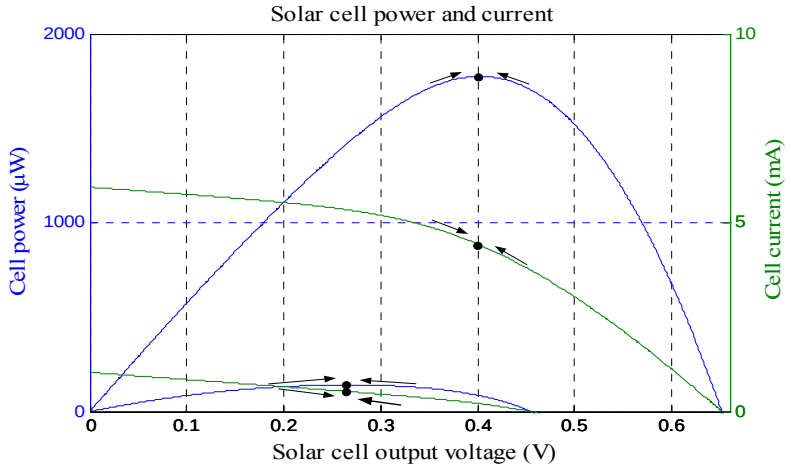

Figure 2-2: Power and current curves of the solar cell equivalent circuit model

2.2 Switched capacitor step-up voltage tripler circuit with charge reusing

2.2.1 Introduction

2.2.1.1 Switched Capacitor DC-DC Converter s

Switched capacitor (SC) DC-DC converters (charge pumps) [4] are widely used in applications where a voltage higher than, or of the opposite polarity to, the input voltage is needed. A switched capacitor converter uses only capacitors and switches to perform the voltage conversion and hence does not need the magnetic storage elements used by inductor-based buck converters.

The Figure 2-3 shows a simplified schematic of the step-up (SC) voltage tripler [5].

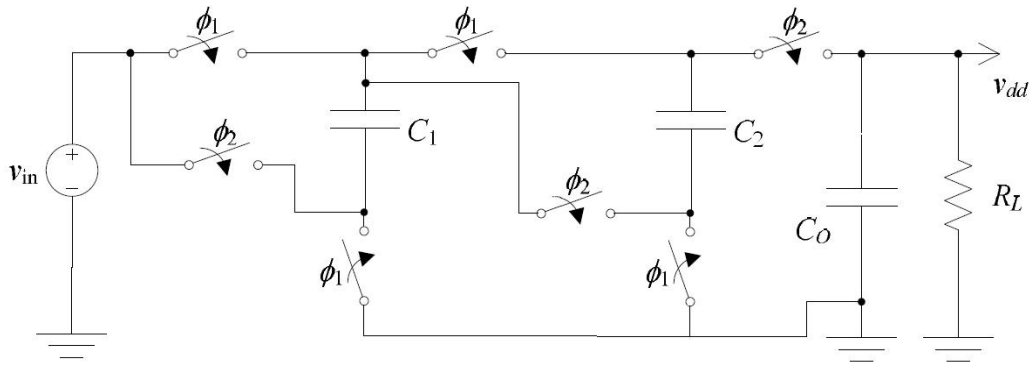

Figure 2-3: Simplified schematic of the step-up voltage converter

During the phase φ_1, the capacitors C_1 and C_2 are charged with the input voltage value (v_{in}). Then, during the phase φ_2, the capacitors C_1 and C_2 are connect in series with the input voltage source (v_{in}), resulting in an output voltage (v_{dd}) that is three times larger than the input voltage value (that's the reason of the name voltage tripler).

Assuming that the output of this circuit is connected to a load resistance (R_L) in parallel with a large external capacitance C_o, the resulting equivalent circuit consists of a voltage source (with a voltage value equal to $3v_{in}$) in series with two resistances. The first one is the equivalent resistance of the switched-capacitor and the second one is the load resistance. The average

output voltage of this circuit is the voltage division of $3v_{in}$ by the resistive divider formed by these two resistors. The output voltage will have a ripple that is inversely proportional to the value of C_o. The value of this capacitance will regulate the upper limit of the output voltage, being inversely proportional to it.

In this type of circuit, the frequency of the clock signal that controls the switches (phases φ_1 and φ_2) changes dynamically the equivalent resistance of the switched capacitors. So the output voltage value (v_{dd}) can be regulated by varying the frequency of the clock. For this reason, the implementation of this type of circuit usually has a Phase Generator or controller module.

Switched capacitor DC-DC converters are a viable option for such systems. One of the main drawbacks of traditional on-chip switched capacitor DC-DC converters is their low efficiency compared to regular switching converters.

2.2.1.2 Loss Mechanisms in a Switched Capacitor

DC-DC Converter Efficiency of a power converter is a key metric for battery operated electronics and energy starved systems. The main contributors to efficiency loss in a switched capacitor DC-DC converter are listed below.

2.2.1.2.1 Conduction loss in transferring charge from the PV cell to the load (battery)

This is the main loss mechanism which arises from charging a capacitor through a switch. When charge flows from the PV Cell to the load, some part of it is dissipated within the switches of the DC-DC converter.

2.2.1.2.2 Loss due to bottom-plate parasitic capacitors

The power lost due to the parasitic bottom-plate capacitors has a significant impact to the total power loss. The next figure illustrates an equivalent model of integrated capacitor with his parasitic elements, where C_{par1} and C_{par2} correspond to the bottom-plate and top-plate parasitic capacitances:

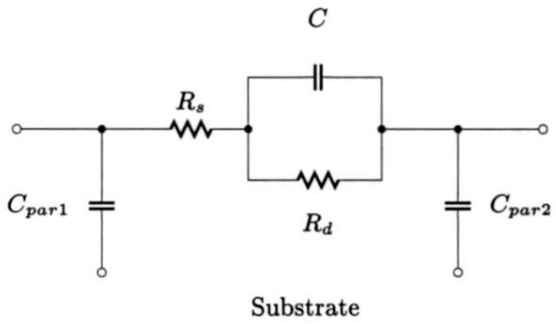

Figure 2-4: Equivalent model of integrated capacitor with its parasitic elements.

In this structure, the top-plate parasitic capacitances is clearly smaller than the bottom-plate parasitic capacitances, for this reason the power lost due to the parasitic elements is almost totally provided by the bottom-plate capacitors.

Therefore, each capacitor of the Figure 2-3 has bottom-plate parasitic capacitance, where C_{parB1} and C_{parB2} correspond to the bottom-plate parasitic capacitances of the capacitances C_1 and C_2. During the phase φ_1, the capacitances C_1 and C_2 are connected in series and the parasitic capacitances C_{parB1} and C_{parB2} are charged up with v_{in}. During the phase φ_2, the capacitances C_1 and C_2 are charged up with v_{in}, and the bottom-plate parasitic capacitances C_{parB1}, C_{parB2} are discharged. So in phase φ_2, the system dissipates the power stored in the phase φ_1 by the parasitic bottom-plate capacitors.

2.2.1.2.3 Gate-drive loss

The power lost due to switching the gate capacitances of the charge-transfer switches is another significant contributor to the total power loss. The energy expended in switching the gate capacitances of the charge-transfer switches every cycle is directly related with *Cox* (the gate-oxide capacitance per unit area), W_{EFF} (the cumulative width of switches that are turned ON / OFF per cycle), L_{min} (the minimum channel length of the technology node in which the switched capacitor converter is implemented) and the output voltage value of the PV cell (v_{in}).

2.2.1.2.4 Power loss in the control circuitry

The power lost in the control circuitry is given by the total power dissipated by all the control circuit of the system. This power is a function of the clock frequency and of the parasitic capacitances in the control circuit. Therefore it is necessary to use minimum size transistors wherever possible in order to reduce the power losses due to the control circuit.

2.2.2 Overview of the circuit

The Figure 2-5 illustrates the schematic of Switched Capacitor Step-up voltage tripler circuit (circuit inside of the square). This circuit is connected in series with the input voltage source v_{in} (provided by the Amorphous Silicon Solar Cell, already explained in chapter 2). If there were no losses, the Step-up SC voltage circuit would provide an output voltage (v_{out}), three times larger than the input voltage value (v_{in}). The output voltage (v_{out}) is typically connected to a large capacitor (C_O), in order to reduce the output ripple and store energy.

The clock phases of the step up converter are generated by a phase controller circuit, and a Start Up circuit guarantees that, during start up, the phase generator is correctly initialized. These two circuits will be described in more detail in chapter 4.

There is a Local Power Supply used to guarantee the voltage supply for the Phase controller module (that will be explained in more detail further ahead in this chapter).

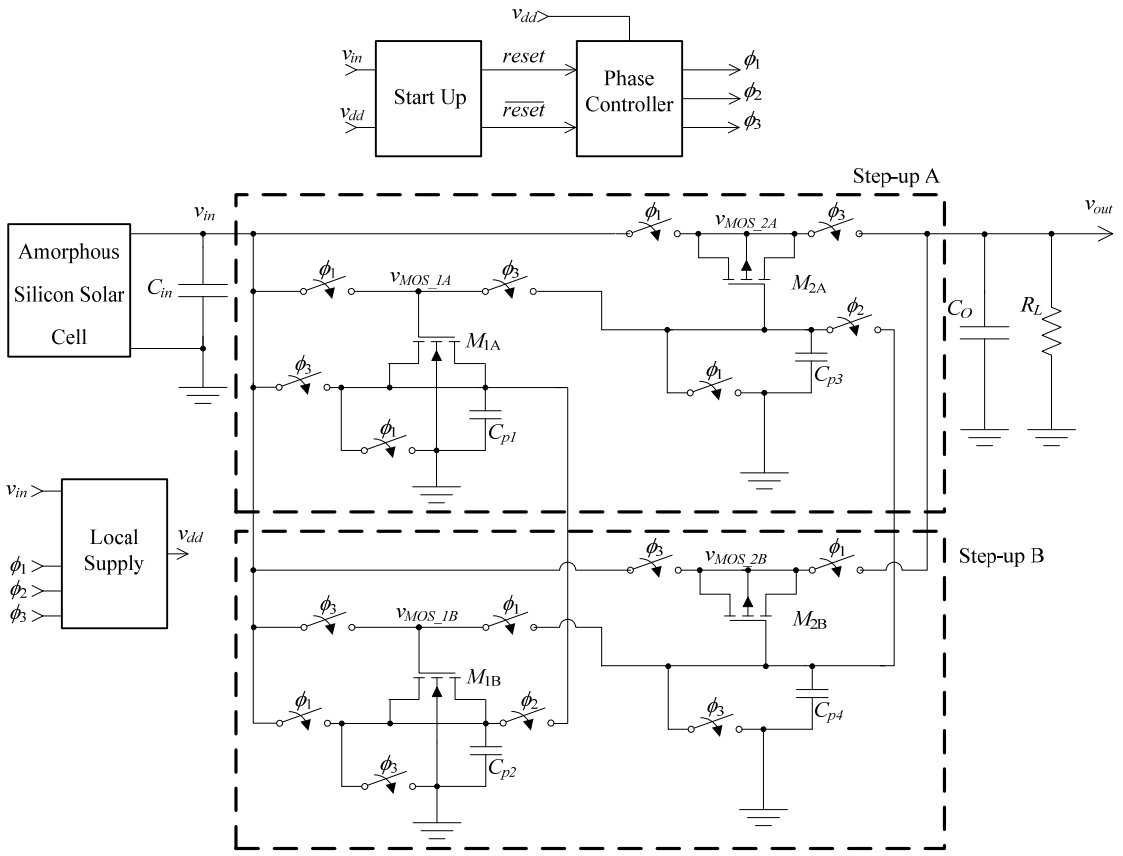

Figure 2-5: Step-up SC voltage tripler circuit

2.2.3 The principle of operation of the step-up converter

The circuit of the SC step-up converter is shown in Figure 2-5. The principle of operation of this circuit is the same as the SC voltage tripler [5, 6]. In order to reduce the area of the circuit, MOS capacitors are used instead of MiM capacitors. During phase φ_1, the MOS capacitors of the upper half circuit (step-up A), M_{1A} and M_{2A}, are charged with the input voltage value (v_{in}) and then, during phase φ_3, they are connect in series with the input voltage source. If there were no losses, this would result in an output voltage (v_{out}) three times larger than the input voltage value.

The clock frequency and the capacitances values are dependent on the amount of power that must be transferred to the load. According to a theoretical analysis [6], the MOS capacitances that would yield the best efficiency were determined to be 4.2 nF. As such, the dimensions of the MOS transistors were set to achieve this capacitance value. For this value, the corresponding operating frequency of the system was determined to be about 1.5 MHz. The efficiency of this circuit (assuming that there are no parasitic losses) depends only on the values of the input and output voltages [5]. Since, during phase φ_3, the drain/source voltage increases, the threshold voltage of a NMOS transistor also increases (due to the body effect), resulting in a decrease of the capacitance of the transistor. This reduction can be significant for transistor M_{2A}, therefore this device is a PMOS instead of an NMOS transistor.

The other issue of using MOS capacitors is the large parasitic capacitance associated to the bottom plate nodes (drain/source nodes). In order to reduce the amount of charge lost in these parasitic capacitances, the circuit is split into two halves. The top half (A) is composed by M_{1A} and M_{2A} and the bottom half (B) is composed by M_{1B} and M_{2B}. The bottom half works in the same way as the top half, with phase φ_1 changed with phase φ_3. During an intermediate phase (φ_2), the bottom nodes of both MOS capacitors of the upper and lower half-circuits are connected together, thus transferring half of the charge in one parasitic capacitance to the other, before the bottom nodes are shorted to ground. This reduces by half the amount of charge that is lost in the parasitic capacitance nodes.

2.2.4 Local power supply

The output voltage of the circuit depends on the value of the load resistance R_L (Figure 2-5). If R_L is very small the output voltage can be very low which would stop the phase generator

circuit from working correctly. This means that the output voltage cannot be used to power the phase generator; therefore a smaller SC voltage step-up circuit, controlled by the same clock, is used to create a local power supply voltage (v_{dd}). This circuit is a replica of the step-up circuits (A + B), scaled to 3% of their area, as this ratio yielded the best results. This local power is decoupled internally with MOS capacitors.

Chapter 3

Maximum power point tracking

Tracking the maximum power point (MPP) of a photovoltaic (PV) cell is usually an essential part of a PV system, because as the name explains, that optimizes the amount of power transferred from the PV cell under a given temperature and irradiance.

PV systems have a single operating point where the values of the current (I) and Voltage (V) result in a maximum power output. These values correspond to a particular load resistance which is equal to:

$$Z_{in} = \frac{V}{I} \tag{3.1}$$

A PV cell has an exponential relationship between current and voltage, and the MPP occurs at the knee of the curve (Fig 3.1), where the resistance is equal to the negative of the differential resistance:

$$\frac{V}{I} = -\frac{\delta V}{\delta I} \tag{3.2}$$

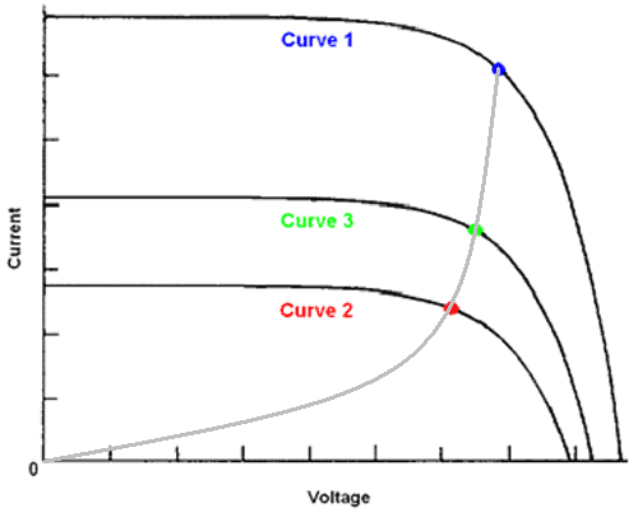

Figure 3-1: Current vs. Voltage for a PV cell

Maximum power point trackers utilize some type of control circuit to search for this point and thus to allow the converter circuit to extract the maximum power available from a cell. This will be explained in more detail in next.

3.4 Photovoltaic Cell Maximum Power Point Tracking Techniques

Many MPP tracking (MPPT) methods have been developed and implemented. The methods vary in complexity, sensors required, convergence speed, cost, range of effectiveness, implementation hardware, popularity, and in other respects. One of the main goals of this work is optimize the efficiency of the circuit composed by the PV cell and the step-up converter, so an implementation with a low consumption of power is an important factor in deciding witch MPPT technique to use. Therefore, an easy implementation, one that would not require the use of software and programming, would be a good option. Following the last criteria, some different MPPT techniques [7] were selected, that will be explained and discussed ahead. Finally, the techniques chosen for this work and the reasons behind it will be explained.

3.1.1 Hill-climbing/Perturb and Observe (P&O)

Hill climbing is a mathematical optimization technique which belongs to the family of local search. It is an iterative algorithm that starts with an arbitrary solution to a problem, then attempts to find a better solution by incrementally changing a single element of the solution.

Talking now about MPPT technique, the hill climbing method [8-15] involves a perturbation in the duty ratio of the step-up converter. The duty ratio of the step-up converter is the control variable of such kind of system. In the case of a PV cell connected to a step-up converter, perturbing the duty ratio of step-up converter perturbs the PV cell current and consequently perturbs the PV cell voltage. A variation of this method is to directly use the duty cycling of switching mode converter or inverter as a MPPT parameter and force dP/dD to zero, where P is the PV cell output power and D is the switching duty cycling of the step-up converter.

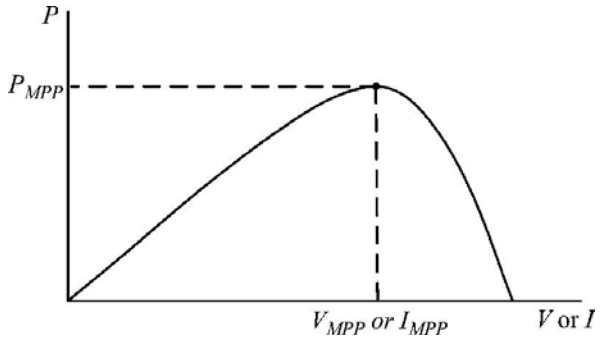

Figure 3-2: Characteristic PV cell power curve

In Fig. 3-2, it can be seen the characteristic of a PV cell power curve: an increase of voltage will lead to an increase of the power when operating on the left of the MPP, and when on the right of the MPP, an increase of the voltage will lead to a decrease of the power. This algorithm is summarized in Table 3-I.

Table 3-I

SUMMARY OF HILL CLIMBING ALGORITHM [8]

Perturbation	**Change in Power**	**Next Perturbation**
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

The P&O method is a method of the Hill Climbing class. By definition, it involves a perturbation in the operating voltage of the PV cell. Therefore, Hill climbing and P&O methods are different ways to envision the same fundamental Method.

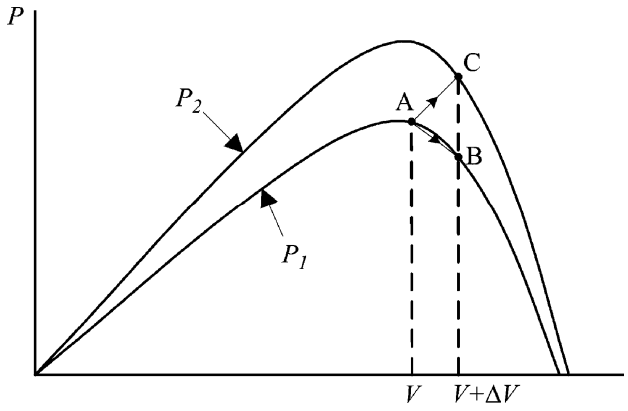

Figure 3-3: Divergence of hill climbing/P&O from MPP

Under rapidly changing atmospheric conditions, it is possible to have multiple local maxima with this method (as illustrated in Fig. 3-3). Starting from an operating point A, if atmospheric conditions stay approximately constant, a perturbation ΔV in the PV voltage V will bring the operating point to B and the perturbation will be reversed due to a decrease in power. On the other hand, if the irradiance increases and shifts the power curve from P_1 to P_2 within one sampling period, the operating point will move from A to C. This represents an increase in power and the perturbation is kept the same. Consequently, the operating point diverges from the MPP and will keep diverging if the irradiance steadily increases. In the present case, this is not a problem because of the high sampling frequency (larger than 100kHz) which will make very unlikely for a significant illumination variation to occur within a sampling period.

3.1.2 Fractional V_{OC}

The fractional V_{OC} method [15] or Voltage-based MPPT (VMPPT) algorithm is based on the near linear relationship between V_{MPP} (output voltage when it operates at MPP) and V_{OC} (open circuit voltage) of the PV cell, under varying irradiance and temperature levels. This relationship can be expressed by:

$$V_{MPP} \approx k_1 V_{OC} \tag{3.3}$$

where k_1 is a constant of proportionality. Since $k1$ is dependent on the characteristics of the PV cell being used, it usually has to be computed beforehand by empirically determining V_{MPP} and V_{OC} for the specific PV cell at different irradiance and temperature levels. For the PV cell, K_1 is normally around 70% (between 0.71 and 0.78), depending on the materials, the surface condition of the cell and also the range of the incident light intensity.

For the circuit implementation of the fractional V_{OC} method, the open circuit voltage (V_{OC}) of the PV cell is firstly measured. It can be done by momentarily shutting down the step-up converter. The MPP voltage can then be calculated according to the equation 4.3. The MPP voltage is used as a reference voltage to adjust the input impedance of the PV cell; consequently the voltage from the PV cell approaches the MPP voltage V_{MPP} and the output power from the PV cell is maximized accordingly.

This method is very easy and cheap to implement as it does not require a DSP or a microcontroller control. However, under changing atmospheric conditions, this method causes multiple local maxima (multiple erroneous maximum power points). In addition to this, the constantly shutting down of the step-up converter incurs some disadvantages, including temporary loss of power.

3.1.3 RCC

Ripple correlation control (RCC) makes use of converter ripple as an alternate source of perturbation. The MPP is usually located by correlating the derivative of the PV cell power (P) with the PV cell voltage (V) or current (I) ripple waveform (Equations 3.4 and 3.5).

$$d(t) = -k_3 \int \frac{dP}{dt}\frac{dI}{dt}dt \tag{3.4}$$

or

$$d(t) = k_3 \int \frac{dP}{dt}\frac{dV}{dt}dt \tag{3.5}$$

Using the Fig. 3-2 to illustrate, if V or I is increasing (PV cell voltage or current derivative is positive) and P is increasing (PV cell power derivative is positive), then the operating point is below the MPP ($V < V_{MPP}$ or $I < I_{MPP}$). However, if V or I is increasing (PV cell voltage or current derivative is positive) and P is decreasing (PV cell power derivative is negative), then the operating point is above the MPP ($V > V_{MPP}$ or $I > I_{MPP}$). Combining these observations, the product of PV cell power and voltage derivatives with respect to time is zero at the MPP, but yields a positive and negative sign when the operating point is to the left or right (respectively) of the MPP.

Simple and inexpensive analog circuits can be used to implement RCC. An example is given in [16], with comparators, amp-ops, a multiplier, a D-type latch, a XOR gate and resistors (Fig 3-4).

In this schematic, the voltage and current are sensed for the PV cell to create two waveforms: the PV cell voltage and the PV cell power (by multiplication of the PV cell voltage and current). After that, the measured power and voltage waveforms are approximately differentiated using high pass filters and then compared with respect to a ground reference. Since each comparator has only binary states, there are four steady-state modes of operation. These modes are evaluated by an exclusive-OR gate and then sampled by a D-type flip-flop clocked at a constant frequency. The flip-flop output provides a suitable signal to drive a DC-DC converter switch.

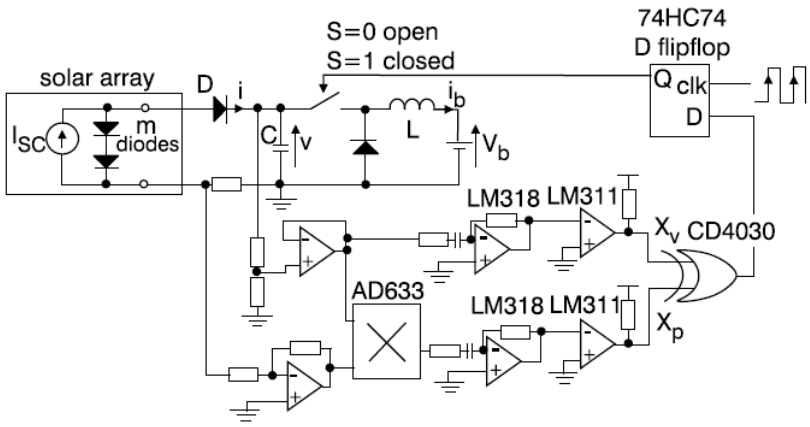

Figure 3-4: Schematic diagram of proposed MPPT using the RCC method [16]

As Midya *et al.* (1996:1710) note, a major benefit of RCC is that it 'keeps [DC–DC] converter operation at the optimum point' while avoiding the 'inconvenient, slow, and fundamentally sub-optimal' perturbation process described in previous sections. But this method can fail due to the phase shift brought about by the intrinsic capacitance of the PV cell at high switching frequencies.

The main disadvantage of this method is that it requires a multiplier block. An analog version of this block is difficult to implement and it can use more power than it is available for the installed application.

3.1.4 Load I or V Maximization

When the PV cell is connected to a step-up converter, maximizing the PV cell power also maximizes the output power at the load of the converter. Assuming a lossless converter, the inverse is also true, i.e., maximizing the output power of the converter should maximize the PV array power.

There are different load types: it can be of voltage-source type, current-source type, resistive type, or a combination of these [7]. As the Fig. 3-5 shows, if you have a voltage-source type load, to obtain the MPP, the load current i_{out} should be maximized. For a current-source type load, the load voltage v_{out} should be maximized. For the other load types, either i_{out} or v_{out} can be used. So, only one sensor is needed (i_{out} or v_{out}).

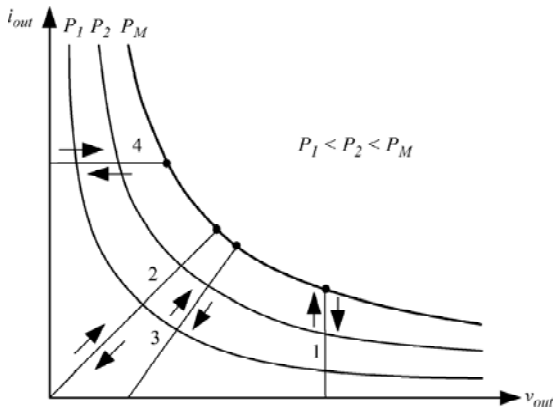

Figure 3-5: Different load types. 1: voltage source, 2: resistive, 3: resistive and voltage source, 4: current source.

In most PV systems, a large capacitor (battery) is used as the main load. In this case, it is very difficult to sense the variation of the load voltage and the load current can be used as the control variable (voltage-source type load) using a current sensor circuit [17].

3.1.5 Analysis and discussion of the different MPPT techniques

The amount of power transferred from the PV cell to the circuit depends on the impedance presented by the step-up converter to the PV cell (Z_{in}). An increase in Z_{in} leads to an increase in the PV cell output voltage and a decrease in the output PV cell output current. The impedance should be adjusted in order to maximize the power of the PV cell. This means that if the PV voltage is lower than the MPP voltage the PV voltage should increase, if it is larger it should decrease (Figure 3-2). Since there is only a small amount of power available for the system, it is difficult to compute the power by performing a multiplication between the voltage and the current (*RCC method*); therefore a different approach should be followed. On the other hand, the fractional V_{OC} method isn't a good alternative, because: under changing atmospheric conditions this method causes multiple local maxima (PV cell technically can operate at multiple MPP); it doesn't control the impedance Z_{in}; and the measurement of V_{OC} includes relevant loss of power. Now, only the Hill Climbing and Load I or V Maximization methods will be analysed and discussed.

In the circuit, the power delivered to the load depends on the output voltage and on the load resistance value. Assuming that the load resistance value is constant (or varies slowly), the variation of the power can be determined by measuring the variation of the output voltage. This means that the MPP can be found by maximizing the output voltage (*Load voltage maximization method*). In reality, this method maximizes the power delivered to the load and not the power from the PV cell [18]. This is preferable because the final objective should always be to maximize the efficiency of the system composed by the PV cell and the step-up converter and not simply to extract the maximum power from the cell at the expense of delivering less power to the load. However, since the output voltage is typically connected to a large capacitor, the amount of voltage variation would be extremely small and very difficult to detect. In order to solve this problem, the local power supply voltage (v_{dd}) is monitored instead (Fig.3-6), because it is a replica of the step-up converter (SC voltage tripler), but without a large capacitor connected on the output voltage (as explained in chapter 3 that power supply provides the v_{dd} voltage to all the local components). Note that if the load resistor decreases, this results in a decrease of the output voltage that in turn leads to a decrease in the voltage of the PV cell, finally resulting in a decrease in v_{dd} that the MPPT circuit can detect.

With this solution, the load current as the control variable of the MPPT method is not necessary and the current sensor circuit is not needed either. So, this solution avoids the complexity of the circuit and the loss of power.

The easy way to adjust the impedance Z_{in} in order to maximize the power of the PV cell is varying the duty cycling of step-up converter. And to do that, the hill climbing method will be added. So, the circuit uses a SC voltage tripler architecture, controlled by a MPPT circuit based on the Load Voltage Maximization and the Hill Climbing methods. In this situation, the hill climbing MPPT circuit (based on the one used in [18]) works by comparing the variation of the output voltage (v_{dd}) between two clock cycles and making an Exclusive-OR with the last variation of the output voltage. The signal resulting of the logical gate XOR (Table 3-I) changes the duty cycling of the step-up converter, and consequently changes the impedance Z_{in}.

The hill climbing MPPT circuit will be better explained in the next chapter, to allow a clearer understanding, before the introduction of some circuits and schematics.

In Summary, a new MPPT circuit will be added to the schematic of the Figure 3-6, which will control the duty cycling of the step-up converter. This circuit will be installed in the module "Phase controller" and it will be sensing the variation of the load voltage of local power supply voltage (v_{dd}).

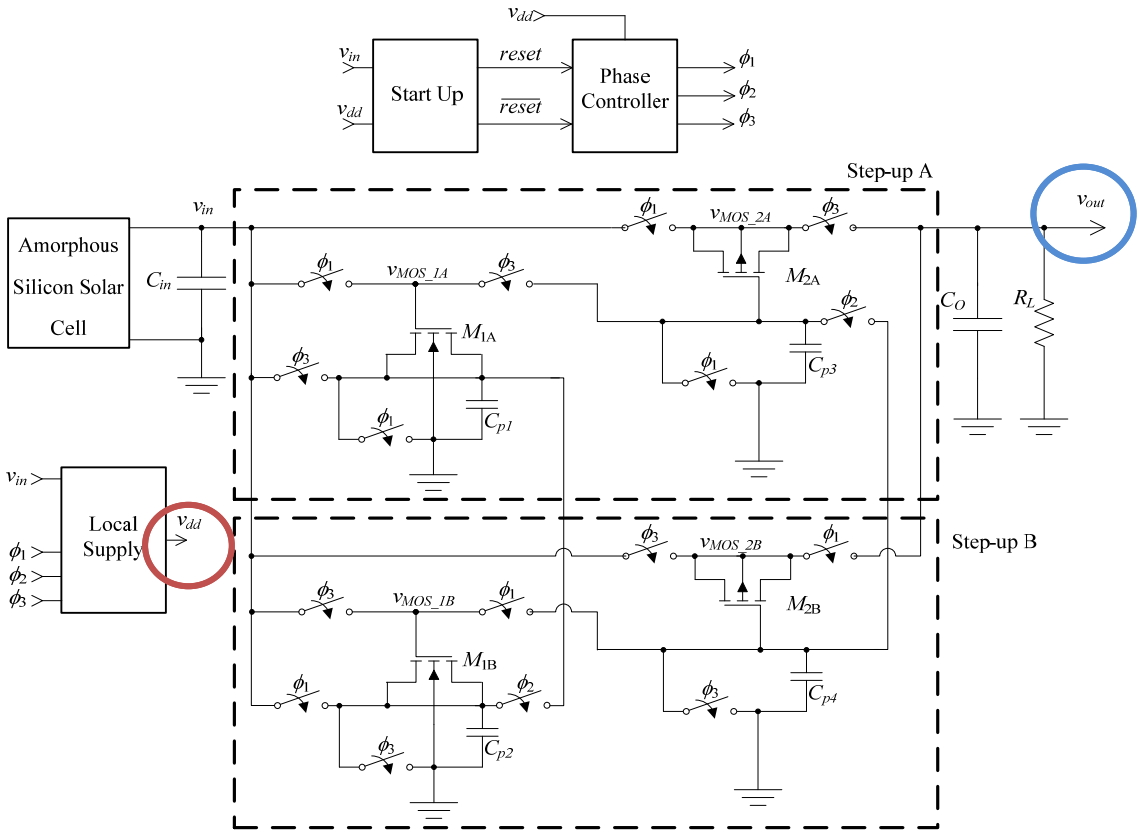

Figure 3-6: Step-up SC voltage tripler circuit

Chapter 4

Phase generation and control

This chapter will focus on the Phase Control and Start-Up modules (Figure 3-6). These two modules are responsible for: the phase generation of the SC step-up circuit; the control of the frequency of these phases, in order to optimize the output power to the load; and the correct reset of the sequence of these phases in some situations.

4.4 Overview

The three clock phases necessary for the operation of the SC step-up circuit are generated by an Asynchronous State Machine (ASM). This circuit is depicted in Figure 4-1.

The operation of this circuit is Similar to the one described in [6]. This circuit has four states that are determined by the output of four latches. These states correspond to the clock phase's φ_1, φ_2, φ_3, and again φ_2 (Figure 4-2). In order to change from one state to the next, the *Set* signal of the latch is activated by changing the output of the latch from 0 to 1. This, in turn, activates the *Reset* signal of the previous latch, causing its output to change from 1 to 0 completing the change.

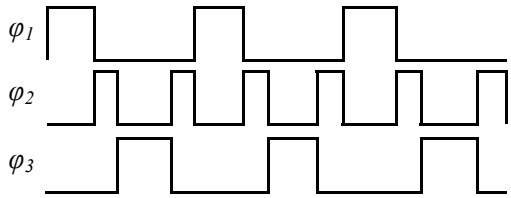

Figure 4-1: Phases generated by the synchronous State Machine (ASM)

The frequency of operation is defined by the delay circuits inserted between the output of each latch and the *Set* input of the next latch (because it defines the duty cycle of the signal). So, controlling these delays, it controls the frequency of operation of the circuit.

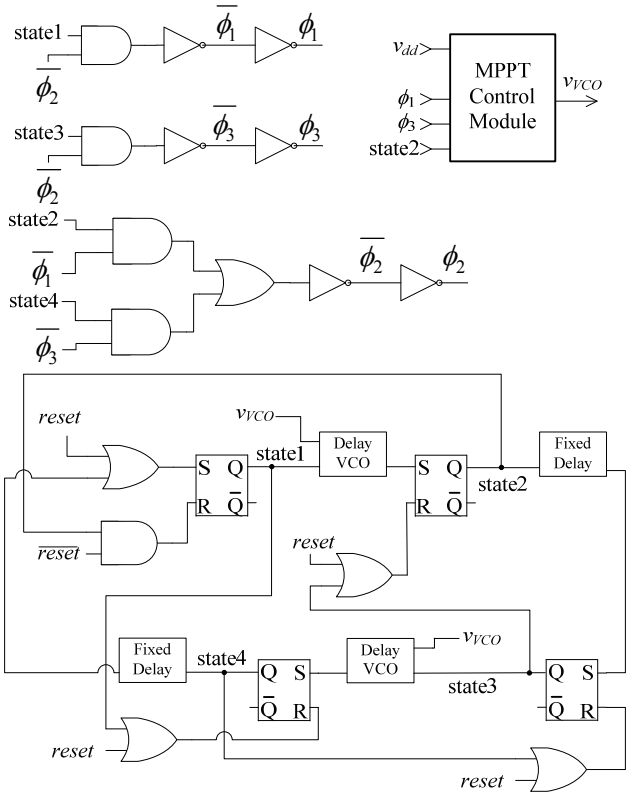

Figure 4-2: Schematic of the Phase Controller

However, as it was mentioned in chapter 3, the phase φ_2 was created to reduce the loss due to bottom-plate parasitic capacitors of the step-up SC circuit, and that's done transferring half of the charge in one parasitic capacitance to the other. This transferring of charge needs a fixed amount of time. So, it is better to define a fixed delay circuit to produce the duty cycle of the phase φ_2, because it will simplify the circuit and it will have less consumption of energy. For

this reason, only the phases φ_1 and φ_3 have variable delay circuit to produce their duty cycle (as shown in Figure 4-2).

The amount of delay of the variable delay circuits is controlled by the voltage v_{VCO} created in the MPP control module (MPPT Control Module in Figure 4-2). The MPPT Control Module will be explained with more detail further.

A start-up circuit (Start Up module in Figure 3-6) generates a *reset* signal that guarantees that the first state is always the state1.

All the logical gates circuits used are described in Appendix A.

4.4 Delay circuit

4.2.1 Introduction

There are two classifications of Variable delay elements [19]:

- Digital Controlled Delay elements
- Voltage Controlled Delay elements

4.2.1.1 Digitally controlled delay elements

In this type of delay, a binary code controls the amount of time delay, and then they provide a fixed and quantized time delay. They are realized as a series of delay elements of variable length, being the different lengths related with the multiplicity of the controller bits. These kinds of delay line elements are suitable for coarse-grain delay variation in a wide range of regulation.

4.2.1.2 Voltage controlled delay element

Voltage controlled delay element, or analog voltage controlled delay element are suitable for fine-grain delay variation. The delay is controlled by a voltage signal. They are efficient in

applications where small, accurate, and precise amounts of delay are necessary to be achieved. Usually, there are two types of Voltage controlled delay elements:

a) Shunt capacitor delay elements

b) Current starved delay elements

a) Shunt capacitor delay elements

Shunt capacitor delay element (see Figure 4-3) is a capacitive loaded inverter. In this case, M_2 acts as a capacitor. Transistor M_1 controls the charging and discharging current to the load capacitor (M_2) from the NOT gate. Indirectly it changes the delay of output pulses. This type of delay element has some disadvantages like: the output capacitor occupies large silicon area; and the amount of a delay and the active range of voltage regulation are small [20].

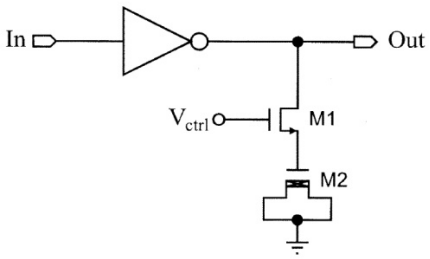

Figure 4-3: Shunt capacitor delay element

b) Current starved delay elements

The Current starved delay element consists of a series of inverters (Fig, 4-4), where the amount of delay is controlled by the time constant formed by a capacitor (C) and a R_{DS} resistance (transistors M_4 and M_3), i.e. R_{DS} are Voltage-controlled resistors that define the charging/discharging current (I_C) of the capacitor (C).

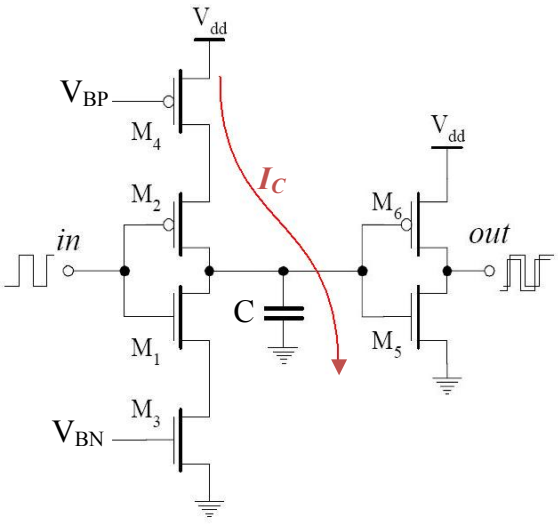

Figure 4-4: Current starved delay element

The time delay is defined by the following Equation (4.1):

$$t_{delay} = \frac{C}{I_{cp}} V_{SW} \tag{4.1}$$

where: C is load output capacitance; I_{cp} corresponds to the charging/discharging current of C, and V_{sw} is a clock buffer (inverter) swing voltage.

4.2.2 Fixed Delay circuit

This delay circuit's purpose is to guarantee a fixed amount of time of waiting between the states 4 to 1 and 2 to 3. But like was explained in the beginning of this chapter, in order to change from one state to the next, the system only looks up to the rising edge of *Set* signal of the latches. So, a fixed delay circuit (Figure 4-5) was implemented with this characteristic in order to limit the power dissipation of the delay circuit (based in [6]). This circuit is a Current starved delay element, so the amount of delay is controlled by the time constant formed by C_{delay} and the resistance of transistor M_5 (which operates in the linear region). When this input clock is low, transistor M_3 charges C_{delay} instantly to v_{dd}, turning off M_6 and turning on M_7. This will result in a low level to appear at the output of the circuit, after the two inverters. When the clock changes to high, transistor M_4 is turned on, allowing the drain current from M_5 to slowly discharge C_{delay}.

After a certain time, the voltage in C_{delay} will be low enough to turn M_7 on, and this will result in a high level to appear at the output of the circuit. During this time, transistor M_7 is turned off to guarantee that there is no current from v_{dd}, through transistors M_6 and M_7. This is necessary to limit the power dissipation of the delay circuit, and it leads the circuit to only delay the rising edge of the input clock. Most of the transistors in this circuit are designed to the minimum size allowed by the technology, in order to reduce the power dissipation of the phase controller circuit and thus improve the efficiency.

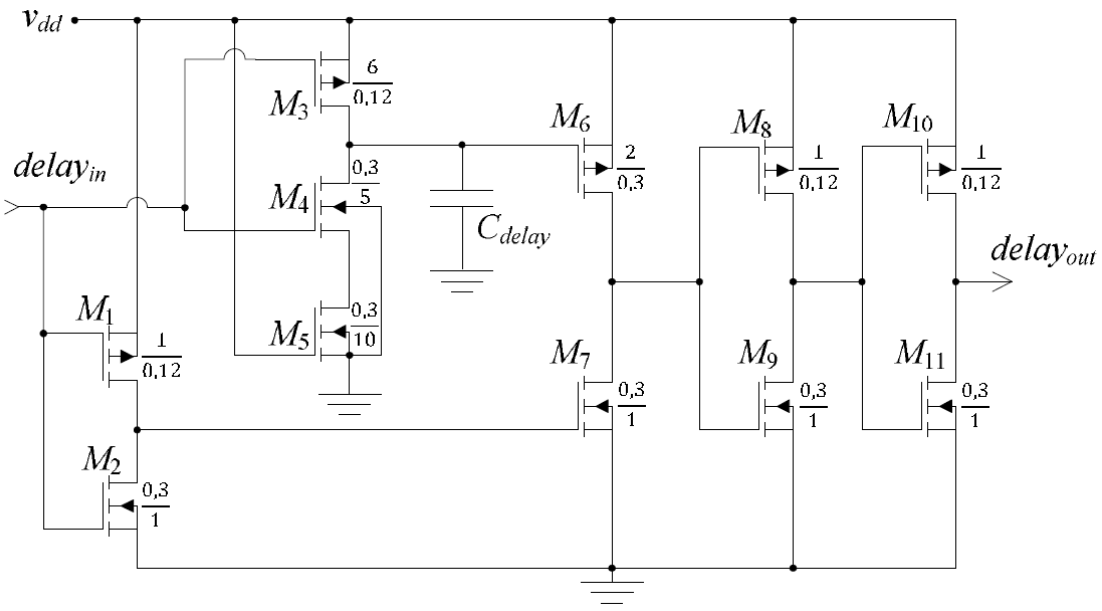

Figure 4-5: Fixed Delay circuit

4.2.2.1 Biasing Process

Like it was mentioned before, the Fixed Delay elements were introduced to guaranty the transfer of half of the charge from one parasitic capacitance to the other. Using some simulation measurements, it is possible to extrapolate that the time needed for the pulse duration of the phase φ_2 is approximately 45ns. Considering that all the MOSFET transistors are biased in the active region, the drain current is calculated with the expression (4.1) and C_{delay}=160fF. The sizes of the transistors are shown in Figure 4-5.

4.2.3 Variable Delay circuit

The Figure 4-6 shows the variable delay circuit implemented.

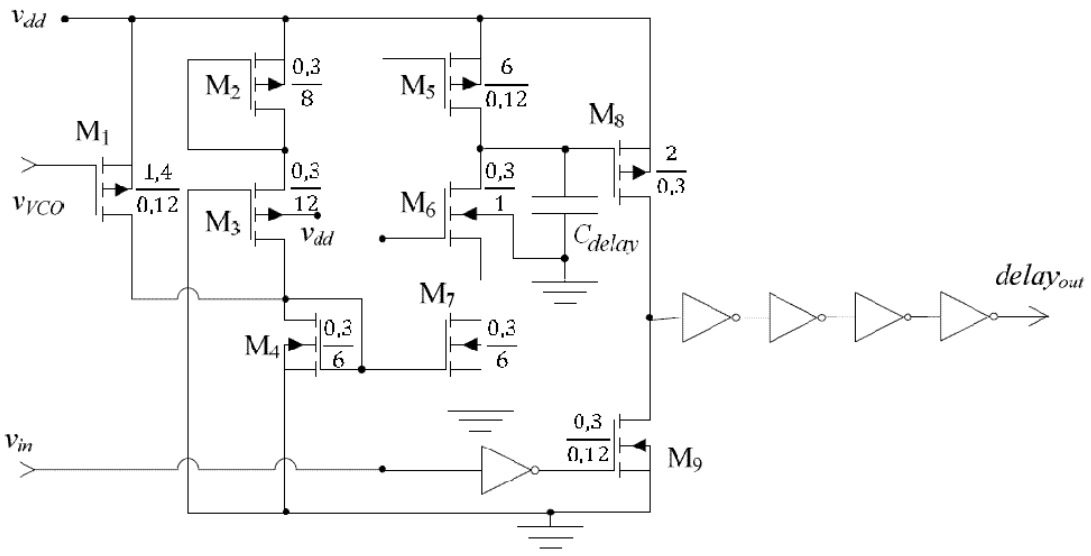

Figure 4-6: Variable Delay circuit

This circuit was based on a Digitally Controller Delay Element proposed in [20] and a Current starved delay element proposed in [6]. The principle of operation of this circuit is the same as the Fixed Delay circuit, i.e. when this input clock is low, transistor M_5 charges C_{delay} instantly to v_{dd}, turning off M_8 and turning on M_9. This will result in a low level to appear at the output of the circuit, after the four inverters. When the clock changes to high, transistor M_6 is turned on, allowing the drain current from M_7 to slowly discharge C_{delay}. After a certain time, the voltage in C_{delay} will be low enough to turn M_9 on, and this will result in a high level to appear at the output of the circuit. During this time, transistor M_9 is turned off to guarantee that there is no current from v_{dd} through transistors M_8 and M_9. This is necessary to limit the power dissipation of the delay circuit. The voltage v_{VCO} controls the drain current of the PMOS transistor M_1. This current is added to the drain current of M_2 and mirrored through M_4 and M_7 (based in [20]). Thus, an increase in v_{VCO} voltage results in a decrease in the mirrored current and, ultimately, in an increase in the delay.

4.2.3.1 Biasing Process

The variation of the frequency of operation is defined by the variable delay circuit presented above. This delay controls the minimum and maximum frequency of operation. Considering 2.6 MHz the maximum and 225 kHz the minimum of frequency of operation, inverting to time's domain (Period) is given by:

$$4.45\mu s > T > 390\ ns$$

Looking at the figure 4-2, the Period is obtained by the addition of the pulse duration of the three phases (φ_1, φ_2 and φ_3):.

$$T = \tau_{\varphi 1} + \tau_{\varphi 2} + \tau_{\varphi 3} \quad (4.2)$$

Considering the pulse duration of phase φ_1 ($\tau_{\varphi 1}$) as equal to the pulse duration of phase φ_3 ($\tau_{\varphi 3}$), because they are controlled by the same signal (V_{VCO}), a new expression is obtained:

$$T = 2\tau_{\varphi 1} + \tau_{\varphi 2} \Leftrightarrow \quad (4.3)$$

$$\Leftrightarrow \tau_{\varphi 1} = \frac{T - \tau_{\varphi 2}}{2}$$

Replacing the values of the T and $\tau_{\varphi 2}$ in expression 4.3, the following expression is obtained:

$$170ns < \tau_{\varphi 1} < 2.2\mu s \quad (4.4)$$

Considering that all the MOSFET transistors are biased in the active region, the drain current is calculated with the expression (4.1) and C_{delay}=2.65pF. The sizes of the transistors are shown in figure 4-6.

4.4 Maximum Power Point Control Module

Until now, the generation of 3 phases (φ_1, φ_2 and φ_3) with 4 states produced by an Asynchronous State Machine (ASM) was explained. Two fixed delay circuits were added, to produce the time's duration of the phase φ_2. Other two variable delay elements were added to produce the time's duration of the phase φ_1 and φ_3. It was also explained that the variables delay elements are controlled by a voltage signal (V_{VCO}). So, this signal (V_{VCO}) is produced by a module called Maximum Power Point Control Module (Figure 4-2). This module is responsible for controlling the work's frequency of the Step-up SC voltage in order to maximize the Load Voltage, only changing the voltage signal V_{VCO}.

The Maximum Power Point control module circuit implemented is based on the one used in [18] and it is depicted in Figure 4-7. This circuit compares the value of v_{dd} at the end of phase φ1 (v_{dd_new}) with the value of v_{dd} at the end of phase φ3 (v_{dd_old}). This way, it is possible to have a comparison between two stable sample voltages in two times (previous and current) that allow a better comparison accuracy. To allow the implementation of the hill climbing algorithm, a gate XNOR and a flip-flop were introduced in the circuit.

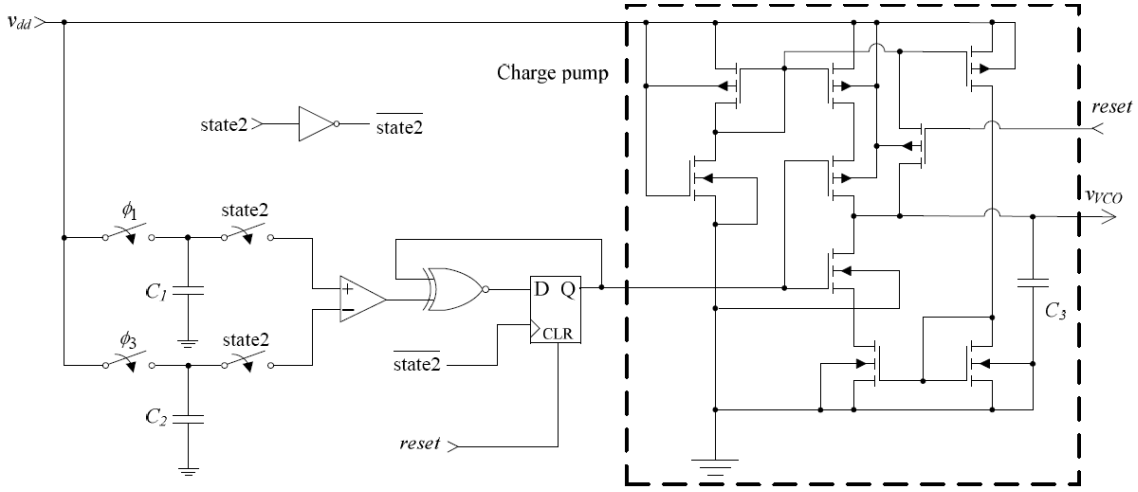

Figure 4-7: Maximum Power Point control module circuit

As a result of this algorithm, if $v_{dd\_new} > v_{dd\_old}$, the charge pump remains in the same state, increasing (or decreasing) the V_{VCO} voltage. This will increase (or decrease) the clock frequency, which in turn will decrease (or increase) Z_{in}. If $v_{dd\_new} < v_{dd\_old}$, the circuit will toggle the way it was, changing Z_{in} (if it was decreasing it should increase it and *vice-versa*). This algorithm is summarized in Table 4-I.

Table 4-I

SUMMARY OF HILL CLIMBING ALGORITHM [8]

	Perturbation	**Change in Power**	**Next Perturbation**
$v_{dd\_new} > v_{dd\_old}$	Positive	Positive	Positive
$v_{dd\_new} > v_{dd\_old}$	Positive	Negative	Negative
$v_{dd\_new} < v_{dd\_old}$	Negative	Positive	Negative
$v_{dd\_new} < v_{dd\_old}$	Negative	Negative	Positive

A charge pump was also introduced to control the rising speed of the Flip-Flop output voltage, by slowing it down. This voltage is then used as an input to the voltage control delay element (V_{VCO}) of the phase generator.

The Figure 4-8 shows all the output signals of the Maximum Power Point control module circuit.

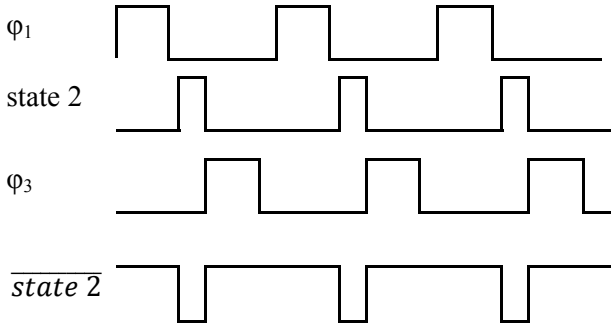

Figure 4-8: Signals of the Maximum Power Point control module unit

4.3.1 Comparator

During the design of the circuit, different types of comparators were tried: two stages, Dynamic Latched, with series of inverters and different combination of three stages. However, the best results were obtained (in terms of efficiency, power dissipation and accuracy) with a three-stage comparator (Figure 4-9). In this section some theory about comparators is presented, specifically about the three-stage comparator, to introduce the comparator used in this work.

A comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on this comparison. A simple comparator is an op-amp without compensation. Comparators are generally used in open-loop mode and so it is not

necessary to compensate the comparator. Since no compensation is needed, it has the largest bandwidth possible which results in a faster response.

The three-stage comparator consists of three stages. The first stage is a Preamplification stage, the second is a decision circuit, and the third and final stage is an output buffer.

Preamplification stage: The preamp stage amplifies the input signal to improve the comparator sensitivity, i.e. it increases the minimum input signal with which the comparator can make a decision, and it isolates the input of the comparator from switching noise coming from the positive feedback stage. Usually, it consists of the differential amplifier with active loads.

Decision stage: The decision stage is the heart of a three-stage comparator and it is used to determine which of the input signals is larger. Hysteresis can be part of the design in the decision circuit.

Output buffer stage: This stage is also called postamplifier stage. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal.

In Figure 4-9 the voltage comparator used in this work is shown [21]. Like explained above, it consists of a Preamplification stage, a decision circuit, and an output buffer. The Preamplification stage (M_1– M_7) is a differential amplifier (diff-amp) with active loads, suitable for high speed since there aren't any high-impedance nodes other than the input and output nodes. The decision circuit (M_8–M_{12}) uses positive feedback from the cross-gate connection between M_9 and M_{10} to increase the gain of the decision element, and it includes a transistor, M_{12}, which acts to shift the output level of the decision circuit upwards and thereby moves it into the common-mode range of the output buffer. Finally, the output buffer or postamplification stage (*M13–M17*) is used to convert the output of the decision circuit into a logic signal, and it consists of a simple self-biased diff-amp that is used to regenerate the signal. The sizes of the transistors are shown in Table 4-II.

Table 4-II

COMPARATOR MOSFET SIZES

	M_1-M_2	M_3	M_4-M_5	M_6-M_7	M_8-M_{11}	M_{12}	M_{13}-M_{14}	M_{15}-M_{16}	M_{17}
W(nm)	2400	2400	600	600	240	240	1200	600	4200
L(nm)	120	240	240	480	240	120	240	240	240

The value of V_{biasn} is 0.178V and I_{biasn} is 182.8nA.

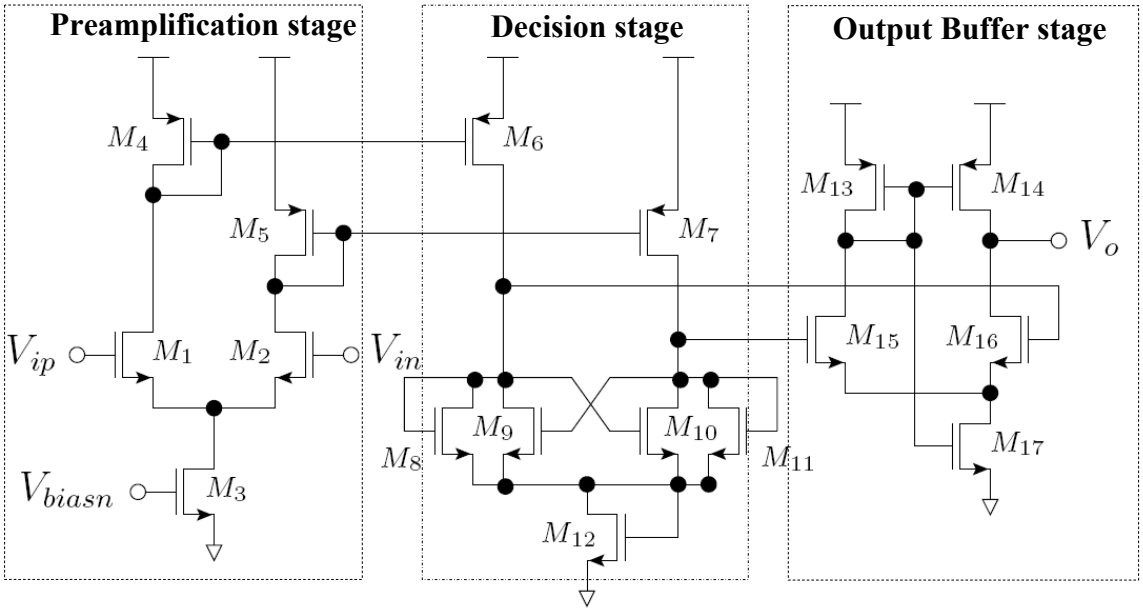

Figure 4-9: Three-stage comparator (bias circuit not shown)

4.3.2 Charge Pump

For the MPPT circuit a Switch in drain Single-Ended Charge Pumps based in [22] was considered. This circuit (Figure 4-10) is the charge pump with the switch at the drain of the current mirror MOS. When the switch is turned off, the current pulls the drain of M_1 to ground. After the switch is turned on, the voltage at the drain of M_1 increases from 0V to v_{dd}. In the mean time, M_1 has to be in the linear region till the voltage at the drain of M_1 is higher than the minimum saturation voltage**.** During this time, high peak current is generated, even though the charge coupling is not considered. It is caused by the voltage difference of two series turn-on resistors from the current mirror, M_1, and the switch. On the PMOS side, the same situation will occur and the matching of this peak current is difficult since the amount of the peak current varies with the output voltage.

In Figure 4-7 the charge pump used in this work is shown and some modifications were made to the circuit above (Figure 4-10): a capacitor was added (C_3) for biasing the rising/falling time of the charge pump. A reset system was introduced, in order to always start the charge pump at 0V in this situation, discharging at this moment the capacitor C_3. Additionally, some connection was added to balance the I_{UP} and I_{DW} (Figure 4-10), i.e. to allow the system to have the same speed time rising and falling.

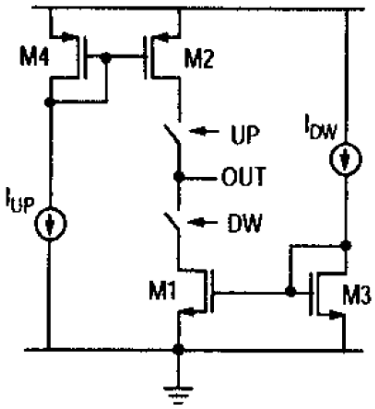

Figure 4-10: Switch in drain single-ended charge pumps

4.4 Start-up circuit

The schematic of the start-up circuit is depicted in Figure 4-11. This circuit is based in [6], it shunts the input and the output nodes during the start-up of the circuit, guaranteeing that the phase controller circuit has a high enough power supply voltage to start working. This circuit also provides the *reset* signal, and its complement, for the ASM, the Charge Pump and some logical gates (XNOR and Flip-Flop type D).

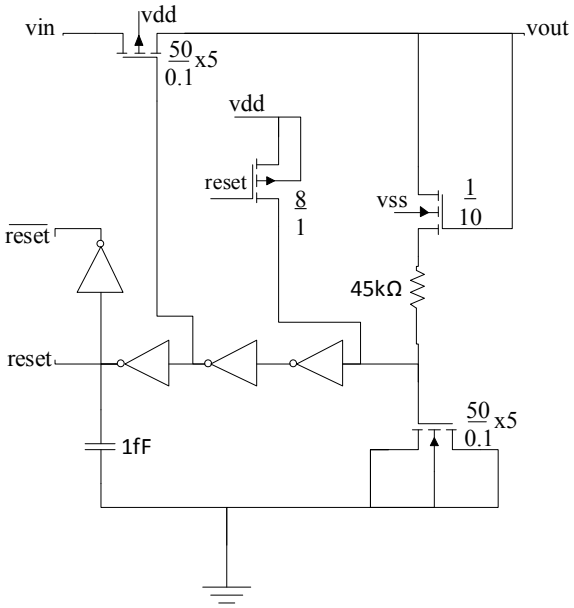

Figure 4-11: Start-up circuit schematic

Chapter 5

Simulation Results

All schematic capture and simulation of the circuits were performed using Cadence's software (Spectre-Virtuoso®). To demonstrate the system operation, we designed the step-up converter using a standard 0.13 μm CMOS technology. All N-channel transistors used in this design have the bulk node connected to the ground (v_{ss}), and all P-channel transistors used in this design have the bulk node connected to the positive potential (v_{dd}).

The step-up converter was designed to work with a single amorphous solar cell, with an area of about 1 cm^2, supplying a maximum power of 1775 μW and a MPP voltage of 403 mV, in a standard 0.13 μm CMOS technology with *VTN* = 0.38 V and *VTP* = -0.33 V. The electrical model of the solar cell is described in chapter 2.

a) The MPPT behavior of the circuit under different light intensities

The first and second simulations of the system were carried out to verify the MPPT behavior of the circuit under different light intensities.

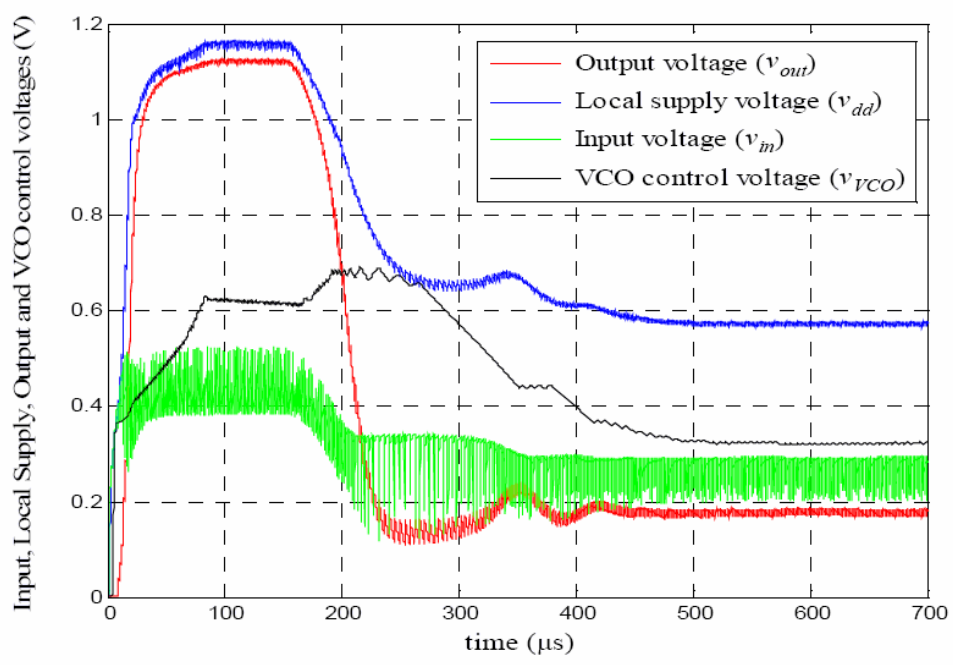

Figure 5-1: Evolution of vin, vdd, vout and vVCO, during start-up and transient operation (Illumination of 100% and 17.5%, changing at 150µs)

In the first simulation, the value of the current I_S in the solar cell model (Figure 2-1) was changed from its maximum value (100%) to a lower value (17.5%) to simulate the change in illumination conditions. The value of the output capacitor of the circuit (*Co*) was limited to 10 nF due to simulation time restriction, this results in a large ripple in the output voltage. The behavior of the circuit, when the illumination changes from 100% to 17.5%, is shown in Figure 5-1.

This simulation shows that under a rapid reduction of the illumination level, the MPPT circuit is still capable of operating: even when the PV voltage is as low as 0.18V, the circuit is resulting in a local power supply voltage of only 0.57 V. This corresponds to the lowest illumination for which the circuit was capable of operating.

The second simulation was carried out for the system operating under different light intensities too, but in this case, the value of the current I_S in the solar cell model (Figure 2-1) was changed from a low value (19% of total illumination) to its maximum value (100%). The behavior of the circuit, when the illumination changes from 19% to 100%, is shown in Figure 5-2.

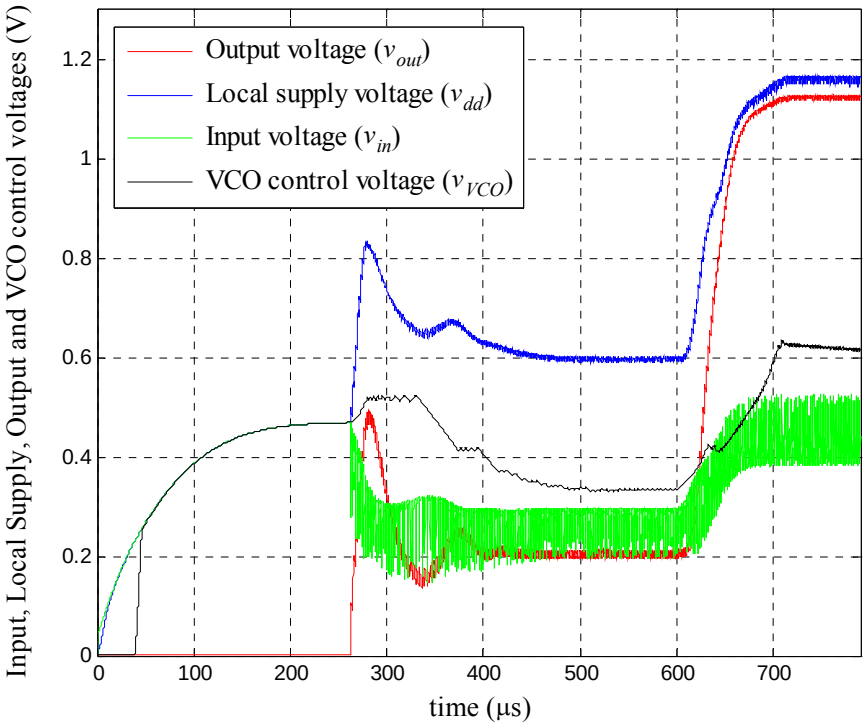

Figure 5-2: Evolution of vin, vdd, vout and vVCO, during start-up and transient operation (Illumination of 19% and 100%, changing at 600µs)

The circuit is capable of starting-up with an illumination condition of 19% of maximum illumination and a load resistance of 1 kΩ, as show in Figure 5-2.

In Fig. 5-1 and 5-2 the relationship between the auto-tracked voltage (V_{VCO}) and the change in light intensity is shown. Under the same light intensity, the auto-tracked voltage (V_{VCO}) oscillates around the optimal value. When the light intensity changes, the MPPT circuit adjusts the V_{VCO} voltage level to the new optimal point.

b) The MPPT behavior of the circuit under different output resistor values

The third simulation was carried out to verify the MPPT behavior of the circuit under different output resistor values.

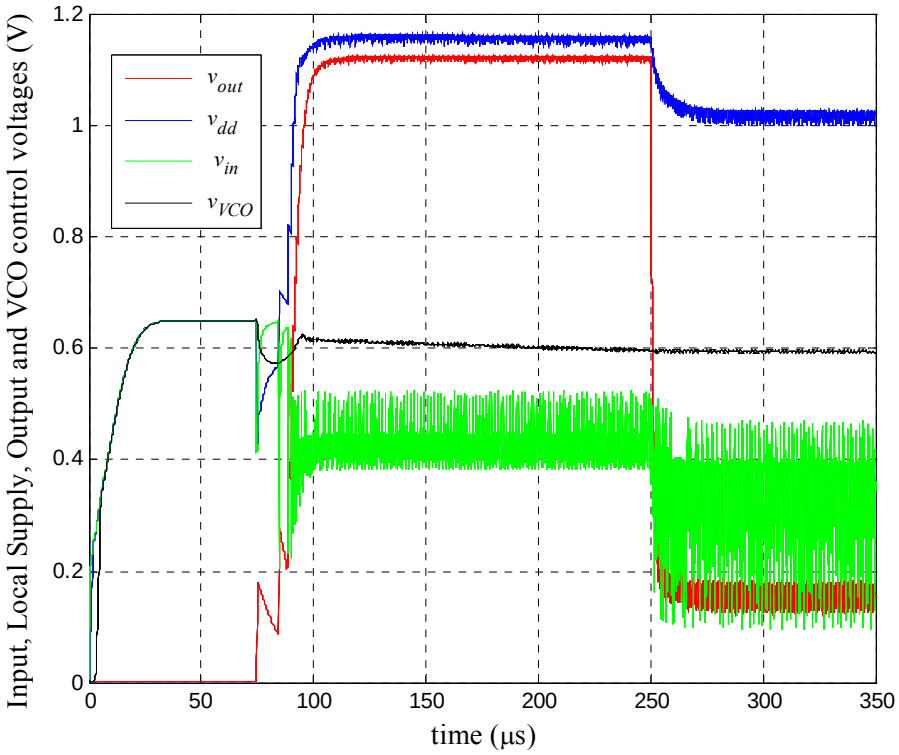

Figure 5-3: Evolution of vin, vdd, vout and vVCO, during start-up and transient operation (Illumination of 100% and load resistance changing at 250µs from 1 kΩ to 100Ω)

Like the Figure 5-3 shows, the circuit is capable of withstanding a change in the output resistor from 1 kΩ to 100 Ω.

To complete the study of the MPPT behavior of the circuit under the different output resistor values, the relevant parameters of the circuit for the different output resistor values were calculated for 100% of the illumination's condition, using the time interval where the system behaviour was stable. These results are presented in Table 5-I.

In Table 5-I it is visible that: v_{out}, v_{in}, v_{dd} and the frequency of the phases of the step-up converter (at MPPT) increase with the increase of the output resistor; the ripple decreases with the increase of the output resistor; and the efficiency, P_{out} and P_{in} have the same curve's shape and they have the maximum points with an output resistor's values between 750Ω and 1kΩ.

Table 5-I

RELEVANT PARAMETERS OF THE CIRCUIT

FOR THE DIFFERENT OUTPUT RESISTOR VALUES

Output Resistor (R_L)	***100% Ligth Intensity (PV power)***							
	P_{out} (µW)	***P_{in} (µW)***	***v_{out} (V)***	***v_{in} (V)***	***v_{dd} (V)***	***fCLK (MHz)***	***η (%)***	***ripple (V)***
100 Ω	282.3	1417	0.167	0.334	1.030	1.154	19.920	0.062
250 Ω	624.2	1521	0.395	0.347	1.044	1.216	41.040	0.054
325 Ω	814.9	1572	0.534	0.356	1.052	1.252	51.820	0.048
500 Ω	1057	1634	0.727	0.369	1.071	1.302	64.670	0.039
625 Ω	1218	1689	0.890	0.384	1.083	1.414	72.110	0.024
750 Ω	1269	1712	0.975	0.401	1.103	1.475	74.130	0.019
1 kΩ	1266	1713	1.126	0.430	1.160	1.780	73.900	0.011
1.5 kΩ	1137	1618	1.305	0.480	1.265	1.927	70.270	0.010
2 kΩ	959.2	1538	1.385	0.493	1.311	2.344	62.350	0.007
5 kΩ	488.3	1258	1.428	0.538	1.428	2.508	38.820	0.008
10 kΩ	260.4	1149	1.613	0.551	1.462	2.604	22.670	0.008

Figure 5-4 shows a graph with the evolution of the efficiency of PV Power at 100% Light Intensity under different output resistor values.

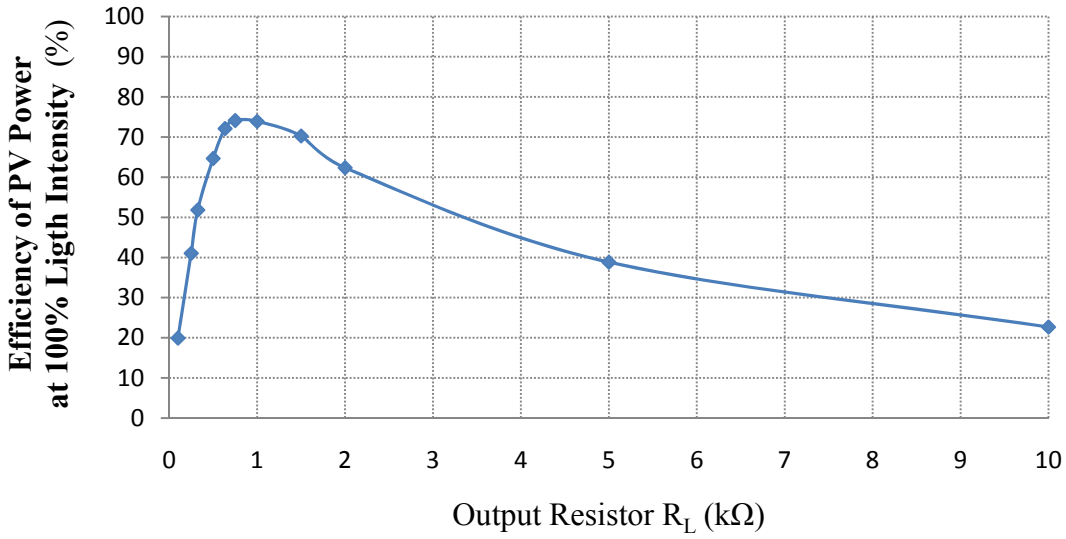

Figure 5-4: Evolution of the efficiency of PV Power at 100% Light Intensity under different output resistor values

Figure 5-4 shows that the efficiency of PV Power at 100% Light Intensity has values upper than 70% with output resistor's values approximately between 600Ω and 1.5kΩ. To reach values of efficiency of PV Power upper than 50%, the range of output resistor value needed are between 300Ω and 3.5kΩ.

c) The MPPT behavior of the circuit under different output resistor values *and light intensities*

The last measurement was carried out to verify the relationship of some relevant parameters under different output resistor values and light intensities. To do that, four levels of light intensities were considered (100%, 75%, 50% and 19%). For each level of light intensities seven different values of output resistor were analyzed. The results of this study are shown in four tables: 5-I, 5-II, 5-III and 5-IV.

Table 5-II
RELEVANT PARAMETERS OF THE CIRCUIT
FOR THE DIFFERENT OUTPUT RESISTOR VALUES AND 19% LIGHT INTENSITY

Output Resistor (R_L)	***19% Light Intensity (PV power)***							
	P_{out} *(μW)*	P_{in} *(μW)*	v_{out} *(V)*	v_{in} *(V)*	v_{dd} *(V)*	f_{CLK} *(MHz)*	*η (%)*	*ripple (V)*
100 Ω	5.552	138.0	0.022	0.276	0.572	0.370	4.024	0.026
250 Ω	7.772	116.1	0.041	0.333	0.670	0.128	6.606	0.058
500 Ω	23.28	142.3	0.108	0.277	0.584	0.396	16.360	0.026
750 Ω	33.39	146.0	0.158	0.277	0.591	0.410	22.830	0.023
1 kΩ	41.97	148.2	0.205	0.278	0.598	0.420	28.330	0.021
2 kΩ	69.04	153.3	0.372	0.281	0.622	0.464	45.050	0.017
10 kΩ	86.01	161.2	0.927	0.333	0.812	0.496	53.350	0.052

Table 5-III

RELEVANT PARAMETERS OF THE CIRCUIT

FOR THE DIFFERENT OUTPUT RESISTOR VALUES AND 50% LIGHT INTENSITY

Output Resistor (R_L)	***50% Light Intensity (PV power)***							
	P_{out} *(µW)*	P_{in} *(µW)*	v_{out} *(V)*	v_{in} *(V)*	v_{dd} *(V)*	f_{CLK} *(MHz)*	*η (%)*	*ripple (V)*
100 Ω	67.06	559	0.080	0.305	0.870	0.660	11.990	0.054
250 Ω	153.3	590.8	0.195	0.307	0.880	0.684	25.950	0.050
500 Ω	282.4	641.2	0.376	0.311	0.873	0.781	44.040	0.044
750 Ω	387.9	672.7	0.539	0.321	0.910	0.794	57.670	0.041
1 kΩ	478.5	705.8	0.692	0.331	0.928	0.823	67.800	0.041
2 kΩ	560.2	792.8	1.058	0.386	1.030	1.374	70.660	0.014
10 kΩ	189.4	708.6	1.376	0.471	1.248	2.266	26.730	0.010

Table 5-IV

RELEVANT PARAMETERS OF THE CIRCUIT

FOR THE DIFFERENT OUTPUT RESISTOR VALUES AND 75% LIGHT INTENSITY

Output Resistor (R_L)	***75% Light Intensity (PV power)***							
	P_{out} *(µW)*	P_{in} *(µW)*	v_{out} *(V)*	v_{in} *(V)*	v_{dd} *(V)*	f_{CLK} *(MHz)*	*η (%)*	*ripple (V)*
100 Ω	162.8	982.4	0.126	0.316	0.964	0.982	16.570	0.058
250 Ω	368.6	1051	0.303	0.326	0.976	0.992	35.080	0.053
500 Ω	6508	1144	0.570	0.343	0.995	1.055	56.900	0.046
750 Ω	866	1218	0.806	0.360	1.018	1.150	71.110	0.036
1 kΩ	9636	1274	0.982	0.388	1.064	1.224	75.660	0.020
2 kΩ	811.4	1240	1.274	0.456	1.212	1.959	65.410	0.010
10 kΩ	232.9	966.5	1.526	0.552	1.383	2.483	24.090	0.010

The results shown in Table 5-I, 5-III and 5-IV show that: v_{out}, v_{in}, v_{dd} and the frequency of the phases of step-up converter (at MPPT) increase with the increase of the output resistor; the

ripple decreases with the increase of the output resistor; and the efficiency, P_{out} and P_{in} have the same curve's shape. In tables 5-I and 5-IV, the maximum points are registered with an output resistor's values between 750Ω and 1kΩ. In table 5-III, however, the maximum points are registered with an output resistor's values between 750Ω and 1kΩ.

Table 5-II shows a different case: i.e. both v_{out}, v_{in}, v_{dd}, and the efficiency, P_{out} and P_{in} (at MPPT) increase with the increase of the output resistor; the ripple has no relation with the output resistor; and the frequency of the phases of the step-up converter (at MPPT) increases with the increase of the output resistor (considering R_L = 100 Ω an exception).

All the tables (5-I to 5-IV) show that v_{dd} has values equivalent to approximately three times of v_{in}, under different output resistor values and light intensities. So, this variation of conditions doesn't affect much the relation of three times between v_{in},and v_{dd} Considering these results, one can conclude that it was a good choice to sense the signal v_{dd} to obtain the MPP.

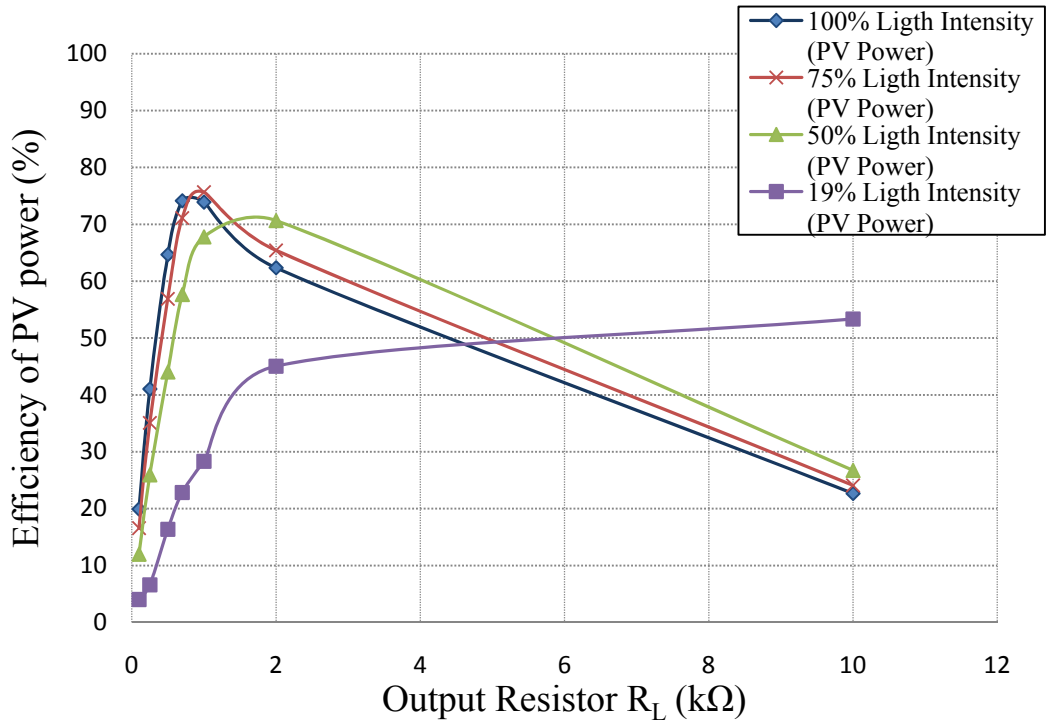

Figure 5-5: Evolution of the efficiency of PV Power under four different Light Intensities and different output resistor values

Figure 5-5 shows the efficiency of PV Power under four different Light Intensities and seven different output resistors. Excluding the result with 19% of Light intensity, all the curves have the same shape. To reach values of efficiency of PV Power upper than 50%, the range of output resistor values needed are between 600Ω and 2kΩ. All those three simulations (50 %, 75 % and 100%) have the maximum value approximately near 1000 Ω.

In the case of the results with 19% of Light intensity, the curve of efficiency is constantly growing, reaching the maximum point with high values of output resistor (upper than 10kΩ). A simple explanation for that is the fact that the system (with output resistors under 10kΩ) doesn't produce power enough to power the control circuit.

Figure 5-6 shows the efficiency of PV Power under four different Light Intensities and different operating frequencies. The MPPT circuit uses the frequency as a control parameter for maximizing the system output voltage (Load Voltage). Therefore, the MPPT circuit tries to find the operating frequency that produces the maximum Load Voltage. However, the step-up voltage converter has different behaviours under different operating frequencies: when the operating frequency is too high, the efficiency will decrease because the system's current loss dominates; when the operating frequency is to low, the efficiency will decrease too, because the step-up voltage converter won't be able to produce power enough to power the control circuit.

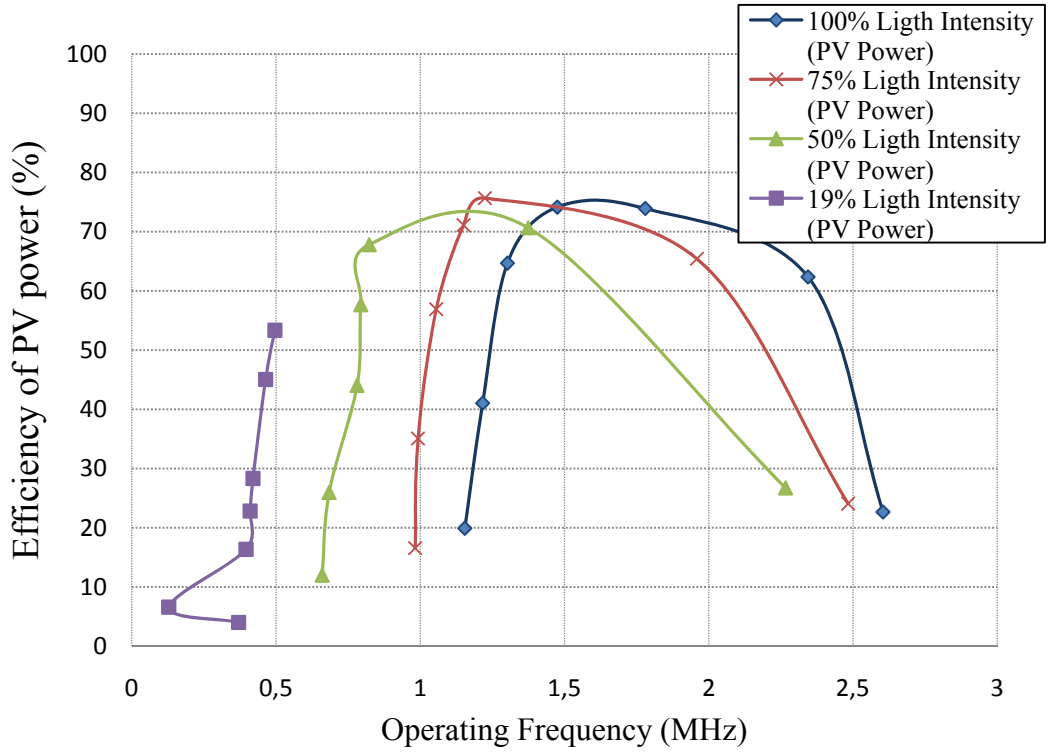

Figure 5-6: Evolution of the efficiency of PV Power under four different Light Intensities and different operating frequencies

The results in Figure 5-6 show that the step-up voltage converter has less power dissipation under operating frequencies between 1MHz and 2MHz. The results show that with 19% of Light intensity, the curve of efficiency is constantly growing, never reaching the maximum point. This confirms that the system's operating frequency is too low (with output

resistors under 10kΩ) and it doesn't produce power enough to power the control circuit, as was also shown in Figure 5-6.

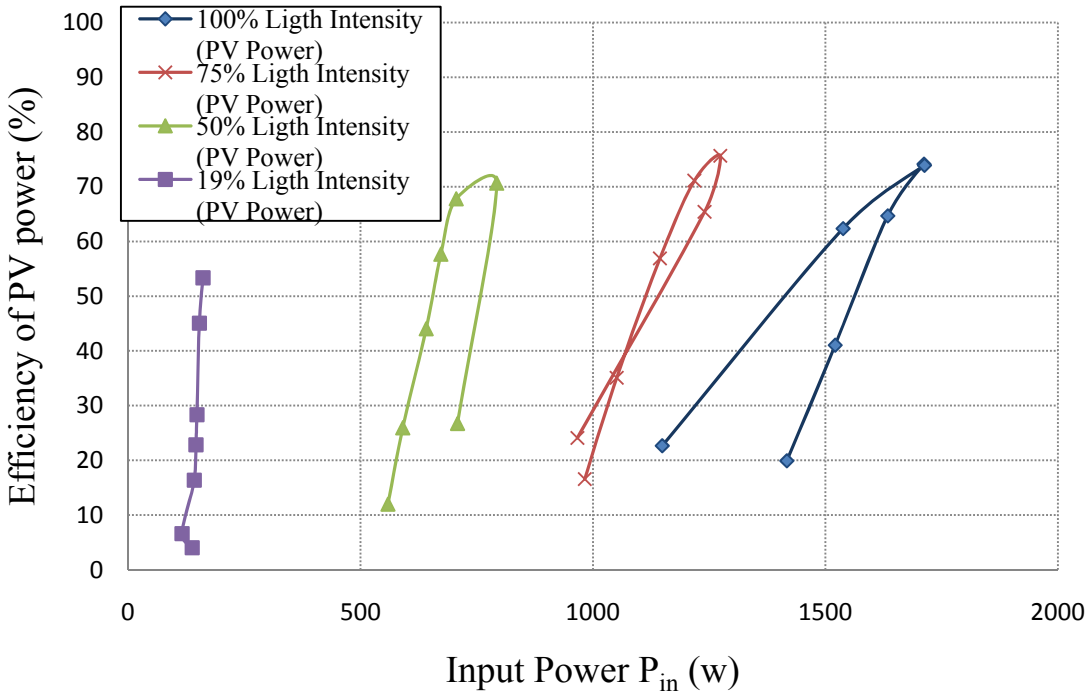

Figure 5-7: Relation of the efficiency of PV Power and the Input Power (P_{in}) under four different Light Intensities and output resistor values.

The results in Figure 5-7 shows that, for each Light Intensity level under different output resistor values, there is a small variation of the Input Power (P_{in}) values. This confirms that the system is trying to track the maximum point of the Input Power under different Light Intensities and output resistors.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

A step-up micro-power converter for solar energy harvesting applications was presented. This circuit was designed in a 0.13 μm CMOS technology in order to work with an a-silicon PV cell.

The circuit uses a SC voltage tripler architecture, controlled by a MPPT circuit. To make the circuit more robust to load, a local power supply voltage was used, which was created using a scaled down SC voltage tripler (controlled by the same MPPT). This local power supply voltage was also used for monitoring the Load Voltage (v_{dd}). This signal (v_{dd}) controls the MPPT circuit based on the Load Voltage Maximization and the Hill Climbing methods. This solution avoids the complexity of the circuit and the loss of power and it makes the circuit more robust to variations of the atmospheric conditions.

The SC circuits use a combination of PMOS and NMOS transistors to reduce the occupied area. A charge re-use scheme is used to compensate the large parasitic resistors associated to the MOS transistors.

Simulation results show that the circuit is capable of starting up with a very low illumination level (around 17, 5% of the maximum). The simulations also show that the circuit can deliver a value around of 1260 μW to the load using 1710 μW of power from the PV cell, corresponding to efficiency as high as 74% (for output resistors between 0.75 kΩ and 1 kΩ and PV Power at 100% Light Intensity).

6.2 Future Work

There is a significant power dissipation of the step-up micro-power converter coming from the variable delays and the comparator elements. During each sampling period, the variable delays and the comparator do not need to operate all the time. There are some moments that they could be disabled. This effort would result in an increase of power delivered to the load, leading to an increase of efficiency.

A suggestion for further investigation was to replicate this study with a fabricated chip, in order to get experimental results.

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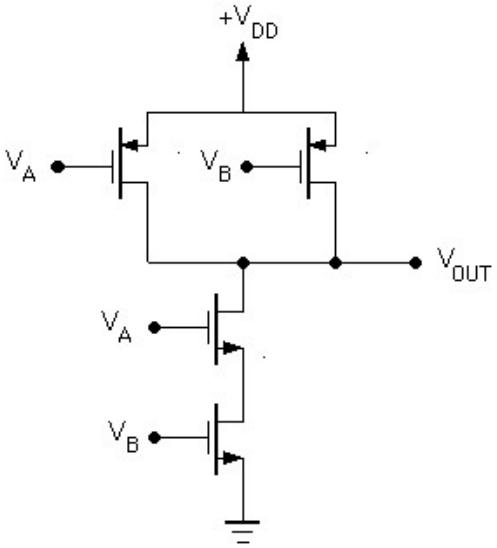
Appendix A

Logical gates – Additional Schematics

All N-channel transistors used in this design have the bulk node connected to the ground (v_{ss}), and all P-channel transistors used in this design have the bulk node connected to the positive potential (v_{dd}).

Most of the transistors in these circuits are designed to the minimum size allowed by technology, in order to reduce the power dissipation of the phase controller circuit and thus improve the efficiency. The circuit only uses transistors with larger sizes, only where the drive capability of the gates is important, such as for the phase buffers. Because of the increased N-channel threshold voltage, the N-to-P channel drive ratio is about 3:1.

A.1 NAND

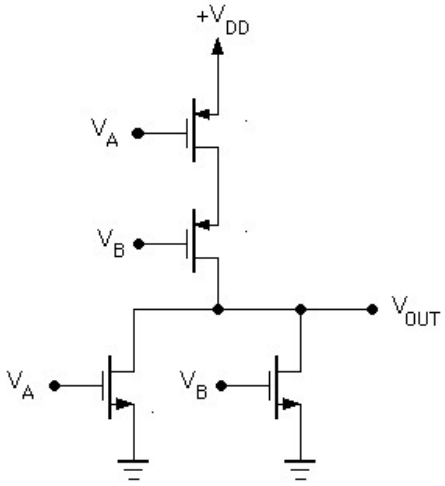


V_A	V_B	V_{OUT}
0	0	1
0	1	1
1	0	1
1	1	0

a) b)

Figure A.1: a) Schematic of NAND. b) TRUTH TABLE of NAND.

A.2 NOR

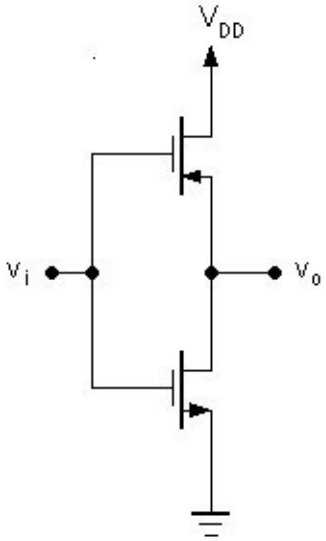


V_A	V_B	V_{OUT}
0	0	0
0	1	1
1	0	1
1	1	1

a) b)

Figure A.2: a) Schematic of NOR. b) TRUTH TABLE of NOR.

A.3 NOT

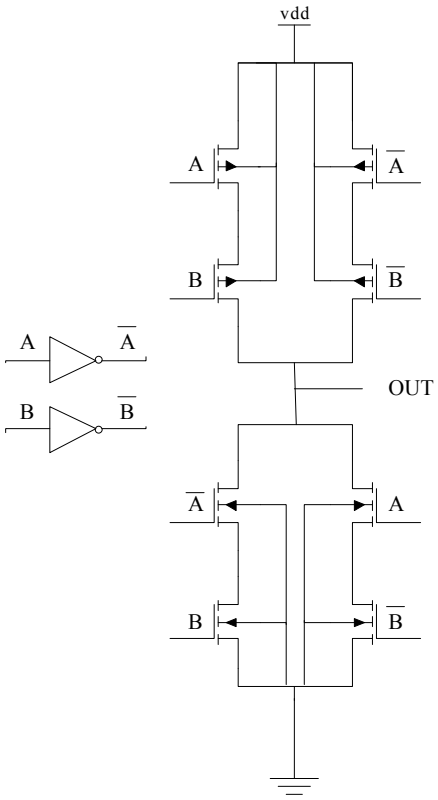


V_i	V_O
0	1
1	0

a) b)

Figure A.3: a) Schematic of NOT. b) TRUTH TABLE of NOT.

A.4 XNOR

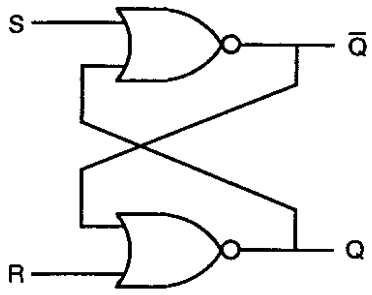


A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	1

a) b)

Figure A.4: a) Schematic of XNOR. b) TRUTH TABLE of XNOR.

A.5 Flip-Flop Type RS



S	R	Q_{n+1}	n+1
0	0	Q_n	n
0	1	0	1
1	0	1	0
1	1	1	1

a) b)

Figure A.5: a) Schematic of Flip-Flop Type RS. b) TRUTH TABLE of Flip-Flop Type RS.

A.6 Flip-Flop Type D

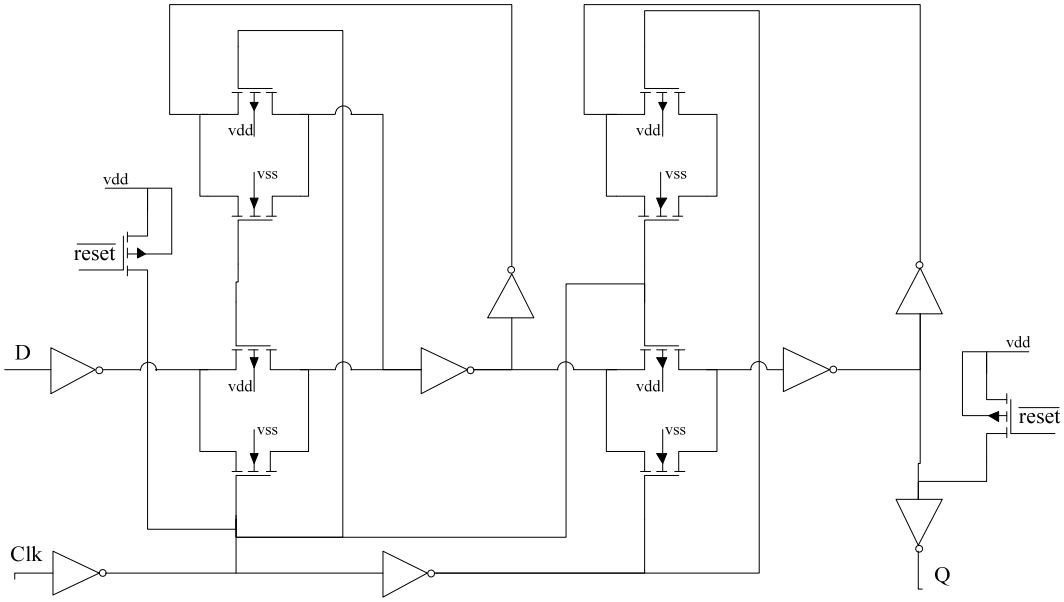


Figure A.6: a) Schematic of Flip-Flop Type D.

D	Clk	Q_{n+1}	$\overline{Q}_{n+1}$
0	0	Q_n	$\overline{Q}_n$
0	1	0	1
1	0	Q_n	$\overline{Q}_n$
1	1	1	1

Table A.1: TRUTH TABLE of Flip-Flop Type RS.

A.7 Switch

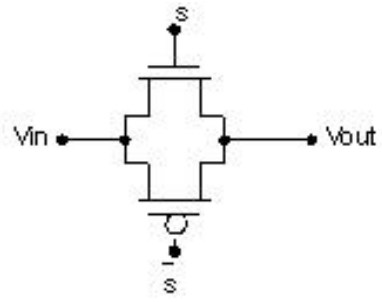


Figure A.8: Schematic of Switch.

Appendix B

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A Step-up μ-Power Converter for Solar Energy Harvesting Applications, using Hill Climbing Maximum Power Point Tracking

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***Abstract* — This paper presents a step-up micro-power converter for solar energy harvesting applications. The circuit uses a SC voltage tripler architecture, controlled by a MPPT circuit based on the Hill Climbing algorithm. This circuit was designed in a 0.13 μm CMOS technology in order to work with an a-Si PV cell. The circuit has a local power supply voltage, created using a scaled down SC voltage tripler, controlled by the same MPPT circuit, to make the circuit robust to load and illumination variations. The SC circuits use a combination of PMOS and NMOS transistors to reduce the occupied area. A charge re-use scheme is used to compensate the large parasitic capacitors associated to the MOS transistors. The simulation results show that the circuit can deliver a power of 1266 μW to the load using 1712 μW of power from the PV cell, corresponding to an efficiency as high as 73.91%. The simulations also show that the circuit is capable of starting up with only 19% of the maximum illumination level.**

I. INTRODUCTION

There is an emerging need to power applications in an autonomous fashion. This need stems from the fact that it may not be practical to plug the device to the power grid, nor to use batteries, as they need to be replaced when their charge is depleted. The applications can be powered by collecting the energy that exists in the surrounding environment. This is known as energy harvesting, or energy scavenging, and has been growing in importance. By employing energy harvesting, circuits can virtually operate permanently. Although there are different ambient energy sources available, ambient light has the highest energy density when compared to other possible ambient energy sources [1].

A photovoltaic cell (which is essentially a diode) converts light energy directly into electrical energy. The output voltage of a single photovoltaic (PV) cell is at the most 0.7 V (under open circuit condition) and can be as low as 0.4 V under maximum power condition. This means that it is necessary to have a voltage step-up circuit that can increase the PV voltage to acceptable values, in order to power a CMOS circuit (typically larger than 1.0 V). A small sized system will necessarily have a small PV cell which will limit the power available to the step-up converter. Under low power conditions, it is feasible to use a capacitor based instead of an inductor based voltage step-up converter, allowing reducing the system size. Since the power and the voltage produced by a PV cell varies with the connected load and with the amount of incident light, it is necessary for the step-up to compensate for these variations in order to supply the maximum available power to the load, i.e. the step-up converter should adjust its behavior in order to track the maximum power point (MPP) of the PV cell. There are several methods available for determining the MPP of a PV cell. Most of these methods are not suitable for low power applications because they require complex implementations that dissipate a lot of power [2]. The Hill Climbing method can be implemented using only analog circuits and it is capable of determining the true MPP of a PV cell [3], therefore this MPP tracking method is selected.

II. AMORPHOUS SILICON SOLAR CELL

In order to reduce the size of the energy harvesting system, an Amorphous-Silicon (a-Si) PV cell was chosen. This cell was built by depositing amorphous silicon with a structure p/i/n on a glass previously covered with ITO (Indium Tin Oxide). The ITO was deposited using rf-PERTE (radio-frequency Plasma Enhanced Reactive Thermal Evaporation) and had a sheet resistance of 35 Ω/□. The active p-type, intrinsic and n-type layers were deposited using PECVD (Plasma Enhanced Chemical Vapor Deposition) and had a thickness of 150Å, 4500Å and 500Å respectively. The frontal aluminum electrode was deposited using thermal evaporation [4]. The die containing the step-up converter (and other circuitry) can be glued to the cell and connected to the PV cell terminals. The PV cell was experimentally characterized and an equivalent electrical model was obtained, as shown in Figure 1.

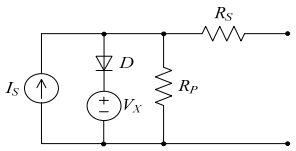

Figure 1. Equivalent electrical circuit of the amorphous silicon PV cell

The cell has a short circuit current of about 5.9 mA, a maximum power of 1775 µW that occurs for a voltage of 403 mV (maximum power point) and an open circuit voltage of 652 mV. These data refer to a cell having an active area of about 1 cm^2, when irradiated according to AM1 (Air Mass 1) conditions (irradiance by the solar spectrum at the earth surface, having the Sun vertically located). The resulting power and current curves of the cell for AM1 and 17.5% of AM1 conditions are depicted in Figure 2.

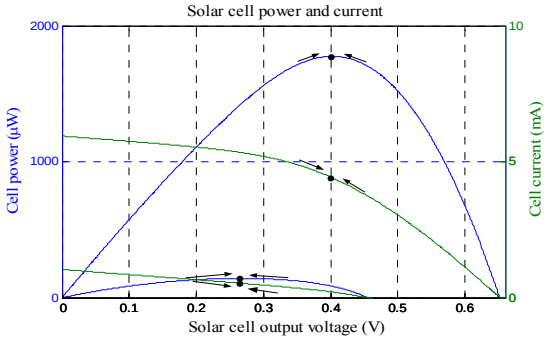

Figure 2. Power and current curves of the solar cell equivalent circuit model for 100% (top) and 17.5% (bottom) illumination

III. SWITCHED CAPACITOR STEP-UP VOLTAGE TRIPLER CIRCUIT WITH CHARGE RE-USE

The circuit of the SC step-up converter is shown in Figure 3. The principle of operation of this circuit is the same as the SC voltage tripler [5]. During phase ϕ_1, the MOS capacitors of the upper half circuit (step-up A), M_{1A} and M_{2A}, are charged with the input voltage value (v_{in}) and after, during phase ϕ_3, they are connect in series with the input voltage source. If there were no losses, this would result in an output voltage (v_{out}) three times larger than the input voltage value. The clock frequency and the capacitances values are dependent on the amount of power that must be transferred to the load. According to a theoretical analysis, the MOS capacitances that would yield the best efficiency were determined to be 4.2 nF. As such, the dimensions of the transistors were set to achieve this MOS capacitance value. With this value, the corresponding operating frequency of the system was determined to be about 1.5 MHz. The efficiency of this circuit (assuming that there are no parasitic losses) depends only on the values of the input and output voltages [5]. In order to reduce the area of the circuit, MOS capacitors are used instead of MiM capacitors. Since, during phase ϕ_3, the drain/source voltage increases, the threshold voltage of a NMOS transistor also increases due to the body effect, resulting in a decrease of the capacitance of the transistor. This reduction can be significant for transistor M_{2A}, therefore this device is a PMOS instead of an NMOS transistor.

The other issue of using MOS capacitors is the large parasitic capacitance associated to the bottom plate nodes (drain/source nodes). In order to reduce the amount of charge lost in these parasitic capacitances, the circuit is split into two halves. The top half (A) is composed by M_{1A} and M_{2A} and the bottom half (B) is composed by M_{1B} and M_{2B}. The bottom half works in the same way as the top half, with phase ϕ_1 changed with phase ϕ_3. During an intermediate phase (ϕ_2), the bottom nodes of both MOS capacitors of the upper and lower half-circuits are connected together, thus transferring half of the charge in one parasitic capacitance to the other, before the bottom nodes are shorted to ground. This reduces by half the amount of charge that is lost in the parasitic capacitance nodes.

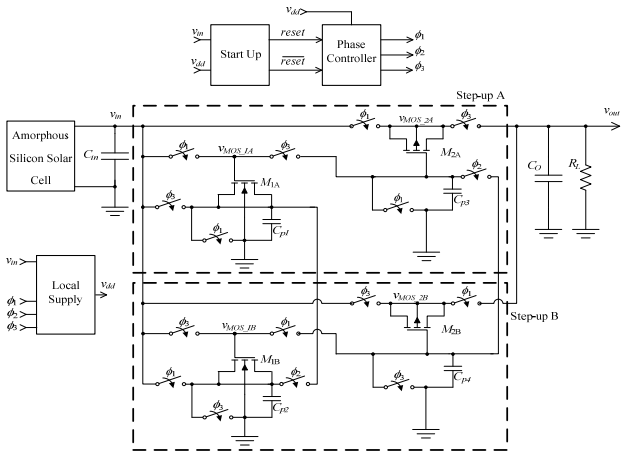

Figure 3. Step-up SC voltage tripler circuit

The clock phases are generated by a phase controller circuit that will be described next. The output voltage of the circuit depends on the value of the load resistance (R_L). During start-up the output voltage will be 0 V because the large output capacitor (C_o) will be discharged. This means that the output voltage cannot be used to power the phase generator; therefore a smaller SC voltage step-up circuit, controlled by the same clock, is used to create a local power supply voltage (v_{dd}). This circuit is a replica of the step-up circuits (A + B), scaled to 3% of their area, as this ratio yielded the best results. This local power is decoupled internally with MOS capacitors.

IV. HILL CLIMBING MAXIMUM POWER POINT TRACKING

The amount of power transferred from the PV cell to the circuit depends on the impedance presented by the step-up converter to the PV cell (Z_{in}). An increase in Z_{in} leads to an increase in the PV cell output voltage and a decrease in the output PV cell output current. The impedance should be adjusted in order to maximize the power of the PV cell. This means that if the PV voltage is lower than the MPP voltage the PV voltage should increase, if it larger it should decrease, as shown by the arrows in Figure 2. Since there is only a small amount of power available for the system, it is difficult to compute the power by performing a multiplication between the voltage and the current; therefore a different approach should be followed. The power delivered to the load depends on the output voltage and on the load resistance value. Assuming that the load resistance value is constant (or varies slowly), the variation of the power can be determined by measuring the variation of the output voltage. This means that the MPP can be

found by maximizing the output voltage. In reality, this method maximizes the power delivered to the load and not the power from the PV cell [3]. However, this is preferable because the final objective should always be to maximize the efficiency of the system composed by the PV cell and the step-up converter and not simply to extract the maximum power from the cell at the expense of delivering less power to the load.

The Hill Climbing MPPT circuit works by comparing the variation of the output voltage between two clock cycles. However since the output voltage is typically connected to a large capacitor, the amount of voltage variation would be extremely small and very difficult to detect. In order to solve this problem, the local power supply voltage (v_{dd}) is monitored instead. Note, that if the load resistor decreases, this results in a decrease of the output voltage that, in turn, leads to a decrease in the voltage of the PV cell, finally resulting in a decrease in v_{dd} that the MPPT circuit can detect.

The MPPT circuit is based on the one used in [3] and it is depicted in Figure 4. This circuit compares the value of v_{dd} at the end of phase ϕ_1 (v_{dd_new}) with the value of v_{dd} at the end of phase ϕ_3 (v_{dd_old}). If $v_{dd\_new} > v_{dd\_old}$ the charge pump remains in the same state, increasing (or decreasing) the v_{VCO} voltage This will increase or decrease the clock frequency, which in turn will decrease (or increase) Z_{in}. If $v_{dd\_new} < v_{dd\_old}$ the circuit will toggle the way it was changing Z_{in} (if it was decreasing it should increase it and *vice-versa*). The comparator circuit is described in [6] (Figure 27.8, p. 914).

V. PHASE GENERATION AND CONTROL

The three clock phases necessary for the operation of the SC step-up circuit are generated by an Asynchronous State Machine (ASM). This circuit is depicted in Figure 5. The operation of this circuit is similar to the one described in [7]. This circuit has four states that are determined by the output of four latches. These states correspond to the clock phases ϕ_1, ϕ_2, ϕ_3, and again ϕ_2, respectively. In order to change from one state to the next, the *Set* signal of the latch is activated, thus changing the output of the latch from 0 to 1. This, in turn, activates the *Reset* signal of the previous latch, causing its output to change from 1 to 0 completing the state change. A start-up circuit (described in [7]) generates a *reset* signal that guarantees that the first state is state1 and that the capacitor at the v_{VCO} voltage is pre-charged to speed-up the MPPT algorithm. The frequency of operation is defined by the delay circuits inserted between the output of each latch and the *Set* input of the next latch. The variable delay circuit is shown in Figure 6. The amount of delay of the variable delay circuits is controlled by the voltage v_{VCO} created in the MPP control module, depicted in Figure 4.

The variable delay circuit only delays the rising edge of the input clock. When this input clock is low, transistor M_5 charges C_{delay} instantly to v_{dd}, turning off M_8 and turning on M_9. This will result in a low level to appear at the output of the circuit, after the four inverters. When the clock changes to high, transistor M_6 is turns on, allowing the drain current from M_7 to slowly discharge C_{delay}. After a certain time, the voltage in C_{delay} will be low enough to turn M_8 on and this will result in a high level to appear at the output of the circuit. During this time, transistor M_9 is turned off to guarantee that there is no current from v_{dd} through transistors M_8 and M_9. This is necessary to limit the power dissipation of the delay circuit. The input voltage v_{VCO} controls the drain current of the PMOS transistor M_1. This current is added to the drain current of M_2 and mirrored through M_4 and M_7 [8]. Thus, an increase in v_{VCO} voltage results in a decrease in the mirrored current and, ultimately, in an increase in the delay.

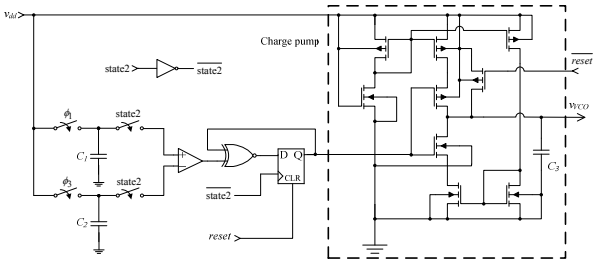

Figure 4. Maximum Power Point control module circuit

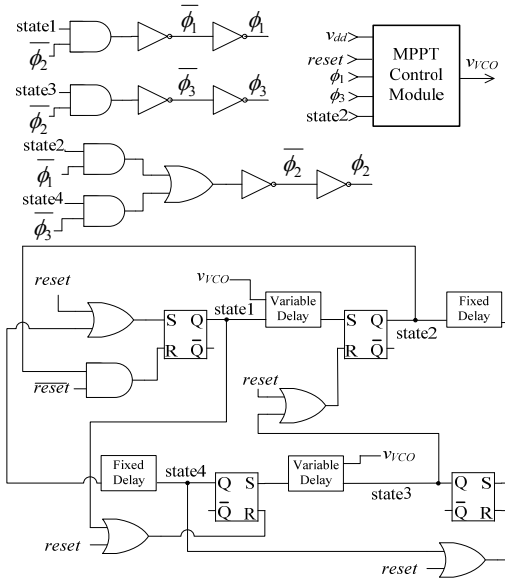

Figure 5. Schematic of the phase generator

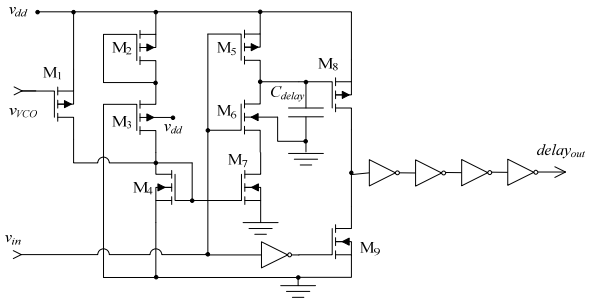

Figure 6. Variable delay circuit

VI. SIMULATION RESULTS

The step-up converter was designed to work with a single amorphous solar cell, with an area of about 1 cm^2, supplying a maximum power of 1775 µW and a MPP voltage of 403 mV, in a standard 0.13 µm CMOS technology with V_{TN} = 0.38 V and V_{TP} = –0.33 V.

In order to verify the MPPT behavior of the circuit, the value of the current I_S in the solar cell model (Figure 1) was changed from its maximum value (100%) to a lower value (17.5% or 19%) to simulate the change of illumination

conditions. The value of the output capacitor of the circuit (C_o) was 10 nF due to simulation time restrictions. This results in a large ripple in the output voltage. The behavior of the circuit, when the illumination changes from 100% to 17.5%, is shown in Figure 7. This simulation shows that, under low illumination, the MPPT circuit is still capable of operating with a PV voltage as low as 0.18V, resulting in a local power supply voltage of only 0.57 V. This corresponds to the lowest illumination for which the circuit was capable of operating. The circuit is capable of starting-up with 19% of maximum illumination and a load resistance of 1 kΩ, as show in Figure 8. The circuit is capable of withstanding a change in the output resistor from 1 kΩ to 100 Ω, under maximum illumination, as shown in Figure 9.

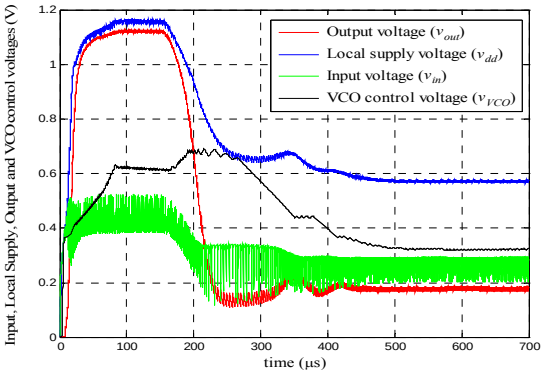

Figure 7. Evolution of v_{in}, v_{dd}, v_{out} and v_{VCO}, during start-up and transient operation (Ilumination of 100% and 17.5%, changing at 150µs)

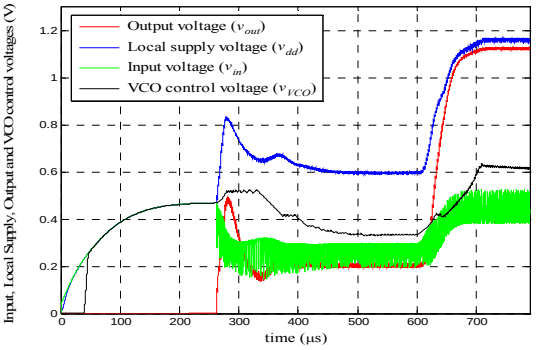

Figure 8. Evolution of v_{in}, v_{dd}, v_{out} and v_{VCO}, during start-up and transient operation (Ilumination of 19% and 100%, changing at 600µs)

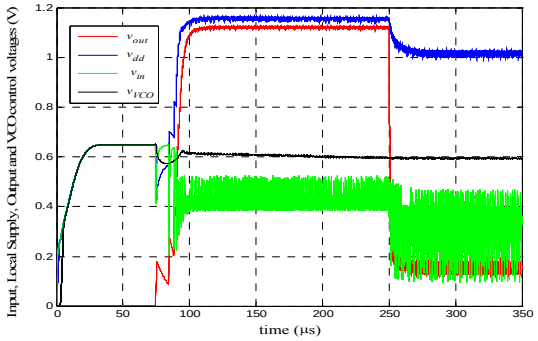

Figure 9. Evolution of v_{in}, v_{dd}, v_{out} and v_{VCO}, during start-up and transient operation (Ilumination of 100% and load resistance changing at 250µs from 1 kΩ to 100 Ω)

The average relevant parameters of the circuit for the different illuminations were calculated from the previous simulations, using the time interval where the system behavior was stable (steady state). These results are presented in TABLE I.

TABLE I. STEADY STATE PERFORMANCE OF THE MPPT CIRCUIT

Light Intensity (PV power)	R_L = 1 kΩ						
	P_{out} *(µW)*	P_{in} *(µW)*	v_{out} *(V)*	v_{in} *(V)*	v_{dd} *(V)*	f_{CLK} *(MHz)*	η *(%)*
100% (1775 µW)	1266	1712	1.13	0.43	1.16	1.756	73.9
19% (167 µW)	42.2	148	0.21	0.28	0.88	0.423	28.6
17.5% (141 µW)	31.6	126	0.18	0.28	0.57	0.380	25.0

VII. CONCLUSIONS

A step-up micro-power converter for solar energy harvesting applications was presented. The circuit uses a SC voltage tripler architecture, controlled by a MPPT circuit with a Hill Climbing algorithm. This circuit was designed in a 0.13 µm CMOS technology in order to work with an a-Si PV cell. The circuit uses a local power supply voltage, created using a scaled down SC voltage tripler (controlled by the same MPPT circuit) to make the circuit more robust to load and illumination variations. The SC circuits use a combination of PMOS and NMOS transistors to reduce the occupied area. A charge re-use scheme is used to compensate the large parasitic capacitors associated to the MOS transistors. Simulation results show that the circuit can deliver a power of 1266 µW to the load using 1712 µW of power from the PV cell, corresponding to an efficiency as high as 73.91%. The simulations also show that the circuit is capable of starting up with only 19% of the maximum illumination level.

ACKNOWLEDGMENT

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