Transparent Oxide Thin-Film Transistors: production, characterization and integration

In partial fulfillment of the requirements for the degree of Doctor of Philosophy in Nanotechnologies and Nanosciences, by Universidade Nova de Lisboa, Faculdade de Ciências e Tecnologia

Lisboa, 2010
Pedro Miguel Cândido Barquinha

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ABSTRACT

This dissertation is devoted to the study of the emerging area of transparent electronics, summarizing research work regarding the development of n-type thin-film transistors (TFTs) based on sputtered oxide semiconductors. All the materials are produced without intentional substrate heating, with annealing temperatures of only 150-200 °C being used to optimize transistor performance. The work is based on the study and optimization of active semiconductors from the gallium-indium-zinc oxide system, including both the binary compounds Ga₂O₃, In₂O₃ and ZnO, as well as ternary and quaternary oxides based on mixtures of those, such as IZO and GIZO with different atomic ratios. Several topics are explored, including the study and optimization of the oxide semiconductor thin films, their application as channel layers on TFTs and finally the implementation of the optimized processes to fabricate active matrix backplanes to be integrated in liquid crystal display (LCD) prototypes. Sputtered amorphous dielectrics with high dielectric constant (high-k) based on mixtures of tantalum-silicon or tantalum-aluminum oxides are also studied and used as the dielectric layers on fully transparent TFTs. These devices also include transparent and highly conducting IZO thin films as source, drain and gate electrodes.

Given the flexibility of the sputtering technique, oxide semiconductors are analyzed regarding several deposition parameters, such as oxygen partial pressure and deposition pressure, as well as target composition. One of the most interesting features of multicomponent oxides such as IZO and GIZO is that, due to their unique electronic configuration and carrier transport mechanism, they allow to obtain amorphous structures with remarkable electrical properties, such as high hall-effect mobility that exceeds 60 cm² V⁻¹ s⁻¹ for IZO. These properties can be easily tuned by changing the processing conditions and the atomic ratios of the multicomponent oxides, allowing to have amorphous oxides suitable to be used either as transparent semiconductors or as highly conducting electrodes. The amorphous structure, which is maintained even if the thin films are annealed at 500 °C, brings great advantages concerning interface quality and uniformity in large areas.

A complete study comprising different deposition conditions of the semiconductor layer is also made regarding TFT electrical performance. Optimized devices present outstanding electrical performance, such as field-effect mobility (µₑₑ) exceeding 20 cm² V⁻¹ s⁻¹, turn-on voltage (Vₒₒ) between -1 and 1 V, subthreshold slope (S) lower than 0.25 V dec⁻¹ and On-Off ratio above 1⁰⁷. Devices employing amorphous multicomponent oxides present largely improved properties when compared with the ones based on polycrystalline ZnO, mostly in terms of µₑₑ. Within the compositional range where IZO and GIZO films are amorphous, TFT performance can be largely adjusted: for instance, high indium
contents favor large $\mu_{\text{FE}}$ but also highly negative $V_{\text{on}}$, which can be compensated by proper amounts of zinc and gallium. Large oxygen concentrations during oxide semiconductor sputtering are found to be deleterious, decreasing $\mu_{\text{FE}}$, shifting $V_{\text{on}}$ towards high values and turning the devices electrically unstable. It is also shown that semiconductor thickness ($d_s$) has a very important role: for instance, by reducing $d_s$ to 10 nm it is possible to produce TFTs with $V_{\text{on}}=0$ V even using deposition conditions and/or target compositions that normally yield highly conducting films. Given the low $d_s$ of the films, this behavior is mostly related with surface states existent at the oxide semiconductor air-exposed back-surface, where depletion layers that can extend towards the dielectric/semiconductor interface are created due to the interaction with atmospheric oxygen. Different passivation layers on top of this air-exposed surface are studied, with SU-8 revealing to be to most effective one. Other important topics are source-drain contact resistance assessment and the effect of different annealing temperatures ($T_a$), being the properties of the TFTs dominated by $T_a$ rather than by the deposition conditions as $T_a$ increases. Fully transparent TFTs employing sputtered amorphous multicomponent dielectrics produced without intentional substrate heating present excellent electrical properties, that approach those exhibited by devices using PECVD SiO$_2$ produced at 400 °C. Gate leakage current can be greatly reduced by using tantalum-silicon or tantalum-aluminum oxides rather than Ta$_2$O$_5$. A section of this dissertation is also devoted to the analysis of current stress stability and aging effects of the TFTs, being found that optimal devices exhibit recoverable threshold voltage shifts lower than 0.50 V after 24 h stress with constant drain current of 10 µA, as well as negligible aging effects during 18 months.

The research work of this dissertation culminates in the fabrication of a backplane employing transparent TFTs and subsequent integration with a LCD frontplane by Hewlett-Packard. The successful operation of this initial 2.8” prototype with 128x128 pixels provides a solid demonstration that oxide semiconductor-based TFTs have the potential to largely contribute to a novel electronics era, where semiconductor materials away from conventional silicon are used to create fascinating applications, such as transparent electronic products.
RESUMO

Esta dissertação é dedicada ao estudo da área emergente da electrónica transparente, resumindo o trabalho de investigação relacionado com o desenvolvimento de transístores de filme fino (TFTs) baseados em óxidos semicondutores depositados por pulverização catódica. Todos os materiais são produzidos sem aquecimento intencional do substrato e os dispositivos são sujeitos a um tratamento térmico final a apenas 150-200 °C para optimização do seu desempenho. O trabalho é baseado no estudo e optimização de semicondutores activos do sistema de óxidos de gálio-índio-zinco, incluindo quer os compostos binários Ga2O3, In2O3 and ZnO, quer óxidos ternários e quaternários baseados em misturas desses, como o IZO ou o GIZO com diferentes razões atómicas. São explorados diversos tópicos, incluindo o estudo e optimização de filmes finos, a sua aplicação como camada activa de TFTs e finalmente a implementação dos processos optimizados para o fabrico de matrizes activas de endereçamento para serem integradas em protótipos de monitores de cristal líquido (LCDs). Dielécticos amorfos com elevada constante dieléctrica (high-κ) depositados por pulverização catódica e baseados em misturas de óxidos de tântalo-silício ou tântalo-alumínio são também estudados e usados como camada dieléctrica em TFTs totalmente transparentes. Estes dispositivos incluem ainda filmes finos transparentes e altamente condutores de IZO desempenhando a função de eléctrodos de fonte, dreno e porta.

Dada a grande flexibilidade da técnica de pulverização catódica, os óxidos semicondutores são analizados relativamente a vários parâmetros de processo, tais como a pressão parcial de oxigénio e a pressão de deposição, para diferentes composições dos alvos cerâmicos. Uma das mais interessantes características destes óxidos semicondutores multicompostos (como o IZO e o GIZO) é o facto de, devido à sua única configuração electrónica e mecanismo de transporte de cargas, estes apresentarem simultaneamente estruturas amorfas e excelentes propriedades eléctricas, destacando-se a mobilidade de hall, que pode superar os 60 cm² V⁻¹ s⁻¹ em filmes finos de IZO. Estas propriedades podem ser modificadas variando as condições de processo e as razões atómicas dos óxidos multicompostos, permitindo obter óxidos amorfos adequados para serem usados como semicondutores transparentes ou como eléctrodos condutores. A estrutura amorfa, que é mantida mesmo recocendo os filmes finos a 500 °C, traz grandes vantagens no que se refere à qualidade das interfaces e à uniformidade em grandes áreas.

Um estudo completo envolvendo diferentes condições de processamento da camada semicondutora é também efectuado relativamente ao desempenho eléctrico dos TFTs. Os dispositivos optimizados apresentam notável performance, destacando-se a mobilidade de efeito de campo ($\mu_{CF}$) superior a 20
cm² V⁻¹ s⁻¹, tensão “turn-on” (Von) entre 1 e 1 V, declive “subthreshold” (S) menor que 0.25 V dec⁻¹ e razão On-Off acima de 10⁷. Os dispositivos com óxidos semicondutores multicompostos amorfos apresentam propriedades consideravelmente superiores aos baseados em ZnO (semicondutor policristalino), principalmente em termos de µFE. Dentro da gama composicional onde os filmes de IZO e GIZO são amorfos, o desempenho dos TFTs pode ser amplamente ajustado: por exemplo, elevadas concentrações de índio favorecem elevadas µFE mas levam também à obtenção de Von muito negativo, o que pode ser compensado por adequadas concentrações de zinco e gálio.

Concentrações elevadas de óxigênio reativo durante o processo de pulverização catódica levam ao decréscimo de µFE e ao deslocamento de Von para valores muito elevados, tornando também os dispositivos electricamente instáveis. É também mostrado o papel preponderante da espessura do semicondutor (dᵣ): por exemplo, reduzindo dᵣ para 10 nm é possível produzir TFTs com Von=0 V mesmo se usando condições de deposição e/ou composições que levam normalmente à obtenção de filmes finos muito condutores. Dada a reduzida dᵣ dos filmes, tal facto está essencialmente relacionado com a existência de estados de superfície nos filmes semicondutores, podendo ser criadas regiões de depleção que se estendem até à interface dieléctrico/semicondutor devido à interacção com o óxigênio. Diferentes camadas de passivação sobre essa superfície são estudadas, com o SU-8 revelando ser o material mais eficaz para essa função. Outros tópicos importantes explorados nesta dissertação são a extracção da resistência de contacto nos eléctrodos fonte-dreno e o efeito de diferentes temperaturas de tratamentos térmicos (Tₐ), sendo observado que para maiores Tₐ as propriedades dos TFTs passam a ser essencialmente controladas por este parâmetro em vez das condições de deposição. TFTs totalmente transparentes usando dielécticos multicompostos amorfos produzidos por pulverização catódica sem aquecimento intencional do substrato apresentam boas propriedades eléctricas, que se aproximam das exibidas por dispositivos que usam SiO₂ produzido por PECVD a 400 °C. A corrente de fuga é significativamente reduzida usando óxidos de tântalo-sílico ou tântalo-alumínio em vez de Ta₂O₅. Esta dissertação inclui ainda uma secção dedicada a testes de stress nos TFTs, verificando-se que os dispositivos optimizados apresentam deslocamentos recuperáveis da tensão de abertura do canal inferiores a 0.50 V durante medições de stress com corrente de dreno contante de 10 µA durante 24 h. Estes dispositivos não apresentam também efeitos significativos de envelhecimento durante 18 meses.

O trabalho de investigação desta dissertação culmina no fabrico de uma matriz de endereçamento usando os TFTs transparentes, que é depois integrada num mostrador LCD pela Hewlett-Packard. O funcionamento deste protótipo inicial com diagonal de 2.8” e 128x128 píxeis constitui uma sólida demonstração que os TFTs de óxidos semicondutores têm o potencial de contribuir significativamente para uma nova era da electrónica, onde materiais semicondutores diferentes do tradicional silício são usados em fascinantes aplicações, como produtos electrónicos transparentes.


SYMBOLS

%O₂ – percentage of oxygen content in the Ar+O₂ mixture

A – optical absorption

\( \vec{B} \) - magnetic field vector

c – speed of light

Cᵣ – gate capacitance per unit area

d – inter-planar spacing

dₛ – oxide semiconductor thickness

D – crystallite size

\( \vec{E} \) – electric field vector

E – energy of electromagnetic wave

\( Eₐ \) – thermal activation energy

\( E_C \) – conduction band

\( E_F \) – Fermi level

\( E₀ \) – bandgap

\( E_{opt} \) – optical bandgap

\( E_{th} \) – threshold energy for potential barriers inhibited transport

\( E_U \) – Urbach energy

\( f_{co} \) – cutoff frequency

F – correction factor for geometrical asymmetry

gᵣ – conductance

gₘ – transconductance

\( h \) – Planck’s constant \((4.135 \times 10^{-15} \text{ eV.s})\)

I – current

\( I_D \) – drain-to-source current

\( I_G \) – gate leakage current
$J$ – current density

$k$ – extinction coefficient

$L$ – channel length

$L_T$ – contact characteristic length

$n$ – refractive index

$N$ – free carrier concentration

$N_s$ – sheet carrier density

$p_{dep}$ – deposition pressure

$P_{rf}$ – rf power density

$q$ – elementary charge of a particle ($1.6 \times 10^{-19}$ C)

$Q$ – symmetry factor

$r$ – scattering factor

$r_{eff}$ – effective contact resistance

$r_{ch}$ – channel resistance per channel length unit

$R$ – reflectivity

$R_H$ – Hall coefficient

$R_{Hs}$ – sheet Hall coefficient

$R_S$ – sheet resistance

$R_{SD}$ – total series resistance

$R_T$ – TFT on-resistance

$S$ – subthreshold slope

$SD$ – standard deviation

$T$ – transmittance

$T_A$ – annealing temperature

$\mathbf{v}$ – velocity vector

$V$ – voltage

$V_{dep}$ – potential difference across the depletion region
Symbols

$V_D$ – drain voltage
$V_G$ – gate voltage
$V_H$ – Hall voltage
$V_{on}$ – turn-on voltage
$V_{pp}$ – peak-to-peak voltage
$V_T$ – threshold voltage
$V_{HH}$ – intrinsic threshold voltage
$W$ – channel width
$X$ – arithmetic mean
$x_d$ – depletion layer width (contact)
$y_d$ – depletion layer width (semiconductor back surface)
$\alpha$ – absorption coefficient
$\Delta$ – differential phase angle
$\Delta_{abs}$ – absolute variation of atomic composition between film and target
$\Delta_{rel}$ – relative variation of atomic composition between film and target
$\varepsilon_0$ – permittivity of free space ($8.854 \times 10^{-12}$ F m$^{-1}$)
$\varepsilon_s$ – dielectric constant of semiconductor
$\theta$ – Bragg angle
$\kappa$ – dielectric constant
$\lambda$ – wavelength of electromagnetic wave
$\mu$ – mobility
$\mu_{avg}$ – average mobility
$\mu_{eff}$ – effective mobility
$\mu_{FE}$ – field-effect mobility
$\mu_H$ – Hall-effect mobility
$\mu_i$ – intrinsic mobility
$\mu_{inc}$ – incremental mobility
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\( \mu_{\text{sat}} \) – saturation mobility

\( v \) – frequency of electromagnetic wave

\( \rho \) – electrical resistivity

\( \rho_F \) – Fresnel coefficient

\( \sigma \) – electrical conductivity

\( \varphi_B \) – barrier height

\( \varphi_G \) – gate electrode work function

\( \varphi_M \) – metal work function

\( \varphi_S \) – semiconductor work function

\( \chi \) – electron affinity

\( \chi^2 \) – error function

\( \psi \) – differential amplitude angle
ABBREVIATIONS

AFM – atomic force microscopy
ALD – atomic layer deposition
AM – active matrix
ATO – antimony-doped tin oxide
AVT – average transmittance in the visible range
AZO – aluminum-doped zinc oxide
BFSTEM – bright-field scanning transmission electron microscopy
CBM – conduction band minimum
CCFL – cold cathode fluorescent light
CEMOP – Center of Excellence in Microelectronics Optoelectronics and Processes
CENIMAT – Centro de Investigação de Materiais
CES – consumer electronics show
CPM – constant photocurrent method
CRT – cathode ray tube
CVD – chemical vapor deposition
d.c. – direct current
DNQ – DiazoNaphtoQuinone
EDS – energy-dispersive X-ray spectroscopy
ELA – excimer laser annealing
FIB – focused ion beam
FPD – flat panel display
FPP – four-point probe
Full-HD – full high definition
GIZO – gallium indium zinc oxide
GZO – gallium-doped zinc oxide
IGO – indium gallium oxide
IPA – isopropyl alcohol
ITO – indium tin oxide
IZO – indium zinc oxide
JFET – junction field-effect transistor
LCD – liquid crystal display
LTPS – low temperature polycrystalline silicon
MESFET – metal-semiconductor field-effect transistor
MIS – metal-insulator-semiconductor
MISFET – metal-insulator-semiconductor field-effect transistor
MOSFET – metal-oxide-semiconductor field-effect transistor
MUSD – millions U.S. dollars
NIR – near infrared
NNH – nearest-neighbor hopping
OLED – organic light emitting device
PDP – plasma display
PECVD – plasma enhanced chemical vapor deposition
PGMEA – propylene-glycol-mono-methyl-ether-acetate
PLD – pulsed laser deposition
PM – passive matrix
PVD – physical vapor deposition
r.f. – radio-frequency
RIE – reactive ion etching
sccm – standard cubic centimeters per minute
SEM – scanning electron microscopy
SIMS – secondary ion mass spectrometry
SMU – source-monitor unit
SPA – semiconductor parameter analyzer
STM – scanning tunneling microscopy
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Abbreviations

TAO – tantalum aluminum oxide
TAO s.t. – tantalum aluminum oxide produced from a single target
TCO – transparent conducting oxide
TEM – transmission electron microscopy
TEOS – tetraethylorthosilicate
TFT – thin-film transistor
TLM – transmission line method
TOF-SIMS – time-of-flight secondary ion mass spectrometry
TSiO – tantalum silicon oxide
TSO – transparent semiconducting oxide
UD – ultra definition
UV – ultra-violet
VBM – valence band maximum
VRH – variable range hopping
WDS – wavelength-dispersive X-ray spectroscopy
XPS – X-ray photoelectron spectroscopy
XRD – X-ray diffraction
XRF – X-ray fluorescence
ZGTO – zinc-gallium-tin oxide
ZTO – zinc-tin oxide
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Chapter 1

Motivation, objective and structure of the dissertation

Transparent electronics is emerging as one of the most promising technologies for future electronic products, away from the traditional silicon technology. The fact that circuits based on conventional semiconductors as silicon and conductors as copper can be turned transparent by using different materials, the so-called transparent semiconducting and conducting oxides (TSOs and TCOs, respectively), is of great importance and allows defining innovative and high added value application fields. The viability of this technology depends to a large extent on the performance, reliability and cost of the transparent transistors. Transistors are the key components in most modern electronic circuits, commonly used to amplify or to switch electronic analog signals and to process digital data. Besides the high-performance silicon transistors used in microprocessors or amplifiers, designated by metal-oxide-semiconductor field-effect transistors (MOSFETs) and requiring processing temperatures exceeding 1000 °C, other types of transistors are available for large area electronics, where lower temperatures and costs are required. Perhaps the most relevant ones are the thin-film transistors (TFTs), which are intimately associated with liquid crystal displays (LCDs), where they allow to independently switch On or Off each pixel of an image. Given this background, the most immediate demonstration of transparent electronics would be the realization of a transparent display, something that has been envisaged already for a long time, at least from the 1930s when H.G. Wells imagined it in his science fiction novel “The shape of things to come” (fig. 1.1a). Nowadays, with the advent of TSOs and TCOs, which besides transparency also allow for low temperature, low processing costs and high performance, transparent displays start becoming truly conceivable and soon the futuristic concepts shown in fig. 1.1b will certainly be real.

Figure 1.1 – Concepts of transparent displays: (a) early vision, in H.G. Wells 1930s novel “The shape of things to come” (www.technovelgy.com); (b) recent concepts from www.microsoft.com and www.engadget.com.

The main objective of this dissertation is to produce, study and optimize transparent TFTs with channel layers comprising sputtered n-type oxide semiconductors based on the gallium-indium-zinc
transparent oxide system. For this purpose, the semiconductor materials are initially studied and then implemented into the TFTs. To prove the viability of this TFT technology, it is also proposed to integrate an active matrix backplane with oxide semiconductor-based TFTs in a 2.8" LCD prototype. Maximum processing temperatures of 150 °C are established in order to allow for future migration to low-cost and flexible substrates, such as polymers or even paper. A secondary objective is to produce sputtered multicomponent amorphous oxide dielectrics with high dielectric constant (high-κ) and smoothness, without intentional substrate heating, to be integrated in the transparent TFTs.

The organization of this dissertation is as follows:

- Chapter 2 provides some fundamental background regarding properties and applications of oxide semiconductors (both binary and multicomponent) and high-κ dielectrics. The chapter also comprises a section devoted to important aspects related with TFTs, such as operation mode, structures and main semiconductor technologies, as well as a brief reference to the display market regarding past, present and future frontplane technologies, with special emphasis on LCDs and organic light emitting devices (OLEDs), which constitute the main application of TFTs;
- Chapter 3 describes the production and characterization techniques used during the research work of this dissertation, mostly highlighting sputtering and electrical characterization of materials and devices;
- Chapter 4 is devoted to the presentation and discussion of the main results obtained in n-type oxide semiconductors and dielectrics thin films. The influence of target composition and of several processing and post-processing parameters on structural, morphological, compositional, electrical and optical properties is analyzed;
- The effect of composition, processing and post-processing parameters is also discussed regarding the TFT electrical properties and stability in chapter 5. The chapter is divided in two main parts, the first dedicated to oxide semiconductor-based TFTs on commercial silicon substrates employing plasma enhanced chemical vapor deposited (PECVD) silicon dioxide as the dielectric layer, the second to entirely sputtered TFTs including electrodes, semiconductor and dielectric layers. Important aspects such as electrical stability, contact resistance and effect of passivation layers are also covered in this chapter;
- Chapter 6 summarizes the initial results obtained regarding integration of amorphous oxide semiconductor-based TFTs with sputtered dielectrics in active matrix backplanes for application in a LCD display prototype, focusing the most significant processing challenges found when moving to large areas with interconnected TFTs;
- Finally, in chapter 7 the main conclusions of this dissertation as well as some future prospects for oxide semiconductor-based TFTs are presented.
Chapter 2

Transparent oxide (semi)conductors, dielectrics, thin-film transistors and displays background

This chapter provides an introductory background to the materials and devices explored in the research work of this dissertation. The main emphasis is given to the properties and applications of binary and multicomponent TCOs and TSOs, mostly the ones based on indium and zinc oxides. Dielectrics for field-effect transistors application are also briefly explored. Since TFTs are extensively studied during this work, essential aspects related with these devices are also covered here, regarding structures, operation mode, a brief historical perspective and main semiconductor technologies. A short reference to the display market and to the main present and future frontplane technologies is also provided in the end of this chapter.

2.1. Transparent oxide (semi)conductors

TCOs and TSOs constitute the key materials of transparent electronics and are the central research topic of the work of this dissertation. This section provides an overview of the most relevant generic properties and applications of these materials, with special emphasis being given to two binary compounds, ZnO and In2O3, and to multicomponent compounds incorporating these oxides.

2.1.1. History, generic properties and applications of transparent oxide (semi)conductors

Materials exhibiting both high optical transparency in the visible range of the electromagnetic spectrum and high electrical conductivity (\(\sigma\)) are not common when considering conventional material categories, such as metals, polymers and ceramics. For instance, metals are generally characterized by having a high \(\sigma\) but being opaque, while ceramics are seen as electrical insulating materials which due to their typically large bandgap \((E_0)\) can be optically transparent. However, certain ceramic materials can simultaneously fulfill the requirements of high \(\sigma\) and optical transparency: these are designated by transparent conducting oxides (TCOs). [1] Physically, this can be achieved if the ceramic material has \(E_0\geq 3\) eV, a free carrier concentration \((N)\) above \(\approx 10^{19-20}\) cm\(^{-3}\) and a mobility \((\mu)\) larger than \(\approx 1\) cm\(^2\) V\(^{-1}\) s\(^{-1}\), which can be verified for metallic oxides such as ZnO, In2O3 and SnO2. [2] Due to the relatively low \(\mu\) of TCOs when compared with classical semiconductors such as single crystalline silicon, which has \(\mu>400\) cm\(^2\) V\(^{-1}\) s\(^{-1}\), TCOs generally need to be degenerately
doped if a high \( \sigma \) is envisaged. Like in silicon, doping can be achieved by the introduction of extrinsic substitutional elements in the host crystal structure, such as elements with different valences that are introduced in the cationic sites. [1, 3, 4] Doping can also be achieved by intrinsic structural defects, such as oxygen vacancies and/or metal interstitials. This structural imperfection, or in other words the deviation from stoichiometry, which always occurs when TCOs are deposited, is the fundamental reason behind electrical conduction on these materials: to maintain charge neutrality, the defects give rise to electrons that depending on the defects’ energy levels within the \( E_G \) of the oxide, can be available for the conduction process, increasing \( N \) and consequently \( \sigma \). [3]

The effect of oxygen defining the final properties of these materials was readily observed at the early stages of this research area. In fact, the first reported TCO, by Badeker in 1907, was obtained after exposing an evaporated cadmium film to an oxidizing atmosphere: the resulting material, CdO, was transparent but maintained a reasonably high \( \sigma \), resembling a metal. [5] In the 1920-1930s’, Cu2O and ZnO were also investigated and researchers experimentally found that a large range of \( \sigma \), exceeding six orders of magnitude, could be obtained by changing the oxygen partial pressure. [6-10] Oxygen concentration can even have more implications than simply changing \( N \) and \( \sigma \). As an example, in tin oxide it is reported that a large oxygen deficiency leads to the change of tin oxidation state from +4 to +2, i.e., SnO2 is transformed into SnO. This can completely change the electrical properties of the resulting material: for instance, as most of the TCOs, SnO2 is an n-type semiconductor, while SnO can present p-type conduction. [1, 11]

Still, even if \( \sigma \) can be significantly modulated by the concentration of intrinsic defects, regarding the objective of obtaining a TCO with a high \( \sigma \), extrinsic doping has to be used, with aluminum-doped zinc oxide (AZO) or tin-doped indium oxide (ITO) constituting some of the most well known examples of these extrinsically doped materials. Even if optimized doped TCOs present \( \sigma \) values \( \approx 10^4 \) S cm\(^{-1}\) [12]) which are almost two orders of magnitude lower than the ones typically obtained in the cooper metal used in integrated circuits, this level of \( \sigma \) signifies that appreciable electrical conduction can be achieved in TCOs, allowing to target a large range of applications, as will be shown in the next paragraphs.

Although works like the one of Badeker were essentially based on pure scientific interest, the continuous advances on solid state physics understanding and on processing and characterization tools that occurred during the first half of the 20\(^{th}\) century allowed for substantial technological progress in TCOs’ research. This resulted in the improvement of material properties and soon a large range of applications for them started to be envisaged. The first large-scale use of TCOs happened during World War II, when antimony-doped tin oxide (SnO2:Sb or ATO) was deposited by spray pyrolysis to be used as a transparent defroster in aircraft windshields. [13] During the last decades,
2. Transparent oxide (semi)conductors, dielectrics, thin-film transistors and displays background

making use of optimized TCO properties such as high $\sigma$, high transparency in the visible range, high reflectivity in the infrared, high mechanical hardness or high sensitivity to gas pressure, these materials have been extensively used as transparent electrodes in solar cells, liquid crystal displays (LCDs) and electrochromic windows, heating stages for optical microscopes, transparent heat reflectors in windows, abrasion and corrosion-resistant coatings, antistatic surface layers on temperature control coatings in orbiting satellites, gas sensors, among many other applications. [1, 2] Some examples of these applications are depicted in fig. 2.1.

![Figure 2.1](image-url)  
*Figure 2.1 – Some applications of TCOs (from left to right: electrochromic windows, [14] displays, [15] solar cells, [16] transparent heaters [17]).*

In all the electrical applications mentioned until now, the TCO is an electrically passive element, i.e., it works as an electrode. Hence, concerning electrical properties, most optimization efforts are focused on achieving the maximum possible $\sigma$, which requires a large $N$. However, a new class of applications requiring TCOs with considerably different electrical properties has recently emerged. In fact, the idea of producing ultra-violet (UV) detectors and diodes or even fully transparent TFTs requires the $N$ of TCOs to be substantially decreased, in order to be able to use them as proper semiconductors, i.e., as active elements in devices. [2, 18] For instance, note that the usage of a TCO with a large $N$ as the active layer of a TFT would result in a useless device, because the semiconductor could not be fully depleted, hence it would not be possible to switch-off the TFT.\(^\text{a}\) To distinguish these transparent oxides from the highly conducting TCOs, the low $\sigma$ and $N$ materials can be designated by transparent semiconducting oxides (TSOs). The properties' tuning of TSOs can be made using the same principles explained above for TCOs, i.e., either by intrinsic or extrinsic doping. For instance, larger oxygen concentrations during deposition should result in less oxygen vacancies, hence less free electrons in an n-type TSO, while extrinsic doping with elements that introduce acceptor-like levels and/or that increase $E_0$ can also lead to similar results. [3, 19]

\(^\text{a}\) TFT operation is explained in section 2.3.1 and in chapter 5 it will be experimentally shown the effect of using an oxide semiconductor with a large $N$ as the active layer of a TFT.
Most of the TCOs and TSOs known until now are n-type. However, p-type oxides are needed to extend the possibilities of transparent electronics, for instance by turning possible the fabrication of complementary logic circuits. Besides the early experiences performed with poor-transparency Cu$_2$O in the early 1930s, the first reported p-type oxide was NiO, in 1993. [20] Although p-type conduction was achieved, poor average visible transmittance (AVT) of 40% and low $\sigma$ ($\approx$ 7 S cm$^{-1}$) were obtained. In 1997 Kawazoe et al. presented a strategy for identifying oxides combining p-type conductivity with good optical transparency. [21] The authors suggested that the candidate materials should have tetrahedral coordination, with cations having a closed shell with comparable energy to those of the 2p levels of oxygen anions, and the dimension of crosslinking of cations should be reduced. They selected CuAlO$_2$ to demonstrate the concept, and p-type conduction and reasonable transparency could in fact be achieved. The article of Kawazoe et al. had a significant impact on the research of p-type oxides, with various works being reported during the following years based on similar theoretical principles, mostly employing delafossite structure materials such as SrCu$_2$O$_2$ or CuGaO$_2$. [22-24] Although the maximum $\sigma$ and $\mu$ achieved with these p-type oxides are for now three to four ($\sigma$) and one to two ($\mu$) orders of magnitude lower than the ones of optimized n-type TCOs, the achieved values start to be suitable for their application as TSOs. Given this, different transparent optoelectronic devices employing p and n-type TSOs have been demonstrated, such as near-UV-emitting diodes composed of heteroepitaxially grown TSOs (p-type SrCu$_2$O$_2$ and n-type ZnO) [25] and UV-detectors composed of single crystalline p-type NiO and n-type ZnO. [26] Still, to achieve reasonable optical and electrical properties, these p-type TSOs generally require very large processing temperatures and significant research is still needed to surpass the temperature and performance limitations of these materials, in order to fabricate transparent p-type materials compatible with the low temperature processed n-type TSOs.

2.1.2. Binary oxide semiconductors: zinc oxide and indium oxide

ZnO and In$_2$O$_3$ are the main binary oxides explored in this work. Hence, some basic properties of these materials are provided here. ZnO is perhaps the metal oxide with a larger field of applications. Some examples are rubber manufacture, concrete industry, medical industry, cigarette filters, food additive, pigment in paints, different types of coatings, among many others. [27, 28] ZnO-based varistors are also well known for a long time [29] and ZnO has a large potential to be used in other applications such as UV light emitters, spin functional devices, gas sensors, surface acoustic wave guides or as a transparent conductor and semiconductor material in the emerging field of transparent electronics. [3]
ZnO crystallizes under the hexagonal wurtzite structure (fig. 2.2a), with lattice constants of a=3.24 Å and c=5.19 Å. [1] ZnO exhibits a direct $E_G$ of 3.2-3.4 eV, which can be tuned by substitutional doping on the cation site, for instance with cadmium or magnesium to decrease or increase $E_G$, respectively. [3] When degenerately doped, the bandgap of ZnO can also be broadened due to Burstein-Moss shift, since the lowest energy states above conduction band minimum (CBM) are already occupied and absorption can only occur for higher energy states as $N$ increases. [1, 30] The intrinsic defects mostly considered on ZnO are oxygen vacancies, interstitial zinc and interstitial hydrogen. From these, oxygen vacancies constituting defect levels lying approximately 0.01-0.05 eV below CBM are the most relevant for n-type conduction, being its concentration quite similar to the $N$ observed in single crystals. [2, 3] Still, neutral oxygen vacancies can also give rise to deep defect levels that can trap electrons and are responsible for phenomena such as persistent photoconductivity. [2, 3, 31] ZnO thin films have been produced using a large number of techniques, such as sputtering, [32-34] pulsed laser deposition (PLD), [35, 36] evaporation, [37] chemical vapor deposition (CVD), [38] spray pyrolysis, [39] sol-gel, [40] ink-jet, [41] among others. Although the obtained properties are highly dependent not only on the technique but also on the processing parameters (see, for instance, ref [33]), thin films suitable for a large range of applications can be prepared even with room temperature processing. Still, even at low processing temperatures and regardless of the deposition technique and parameters, ZnO films tend to always exhibit a polycrystalline structure, which can deteriorate carrier transport and inhibit large area applications due to the lack of uniformity and reproducibility of such structures.

(a)

![Structure Image](image)

(b)

![Structure Image](image)

*Figure 2.2 – Crystalline structure commonly adopted by (a) ZnO, hexagonal (wurtzite) and (b) In$_2$O$_3$, cubic (bixbyite). The small filled spheres represent the metallic cations, while the large unfilled spheres represent the oxygen anions.*

Although several works exist in the literature regarding tentative p-type doping in ZnO, using dopants that introduce deep acceptor levels in ZnO, such as nitrogen or phosphorous, stable and reproducible properties are difficult to achieve. This arises as a consequence of self-compensation mechanisms, i.e., of the redistribution of electronic state occupancy due to self-creation of an intrinsic defect that
counterbalances the effect of the intentionally introduced acceptor level, in order to reduce the overall energy of the system. [31, 42]

Regarding In$_2$O$_3$, it crystallizes according to the cubic structure of the mineral bixbyite (fig. 2.2b), with a lattice parameter of 10.12 Å. [1] Although amorphous thin films can be obtained when deposited at very low temperatures (depending on the processing conditions), they readily crystallize under the cubic system mentioned above when subjected to temperatures around 150 °C. [43-46] In In$_2$O$_3$ light is absorbed by both indirect and direct interband transitions, which correspond to optical bandgaps ($E_{opt}$) around 2.7 and 3.5-3.7 eV, respectively. [1, 32] Bandgap widening due to Burstein-Moss shift is also extremely relevant for degenerately doped In$_2$O$_3$, with shifts larger than 0.6 eV being verified with the increase of $N$ when the Fermi level ($E_F$) is above CBM. [44, 47] As for ZnO, oxygen vacancies are also assumed to be the main sources of the shallow donor levels that yield the characteristic n-type conduction to In$_2$O$_3$. These donor levels are generally very close to CBM, in the range of 0.008-0.03 eV, depending on the donor concentration, with degeneracy beginning at a donor density of 1.48×10$^{18}$ cm$^{-3}$. [1]

Similar techniques to the ones mentioned for ZnO can be used to process In$_2$O$_3$ thin films, some of them even at room temperature. [44, 48-54] Concerning applications, the most relevant one is certainly the usage of tin-doped In$_2$O$_3$ (ITO) as a transparent electrode. This arises as a consequence of the very high σ possible to achieve with sputtered ITO, in some cases above 1×10$^4$ S cm$^{-1}$. Still, the recent developments in aluminum- or gallium-doped zinc oxide (AZO or GZO, respectively) already allow to obtain comparable TCO performance for ZnO-based TCOs, using similar deposition techniques. [12, 55] This is highly important because zinc abundance in the earth’s crust is more than two orders of magnitude larger than indium (132 and 0.1 ppm, respectively [32]), which results in a higher cost of indium-based materials.

As it happens with the other widely studied n-type oxide, SnO$_2$, both ZnO and In$_2$O$_3$ are composed by metallic cations with $ns^0$ and oxide anions with $2s^22p^6$ valence electron configurations, with $n$=4 for ZnO and $n$=5 for In$_2$O$_3$ (and SnO$_2$). The empty metallic s-orbitals constitute the CBM, while the valence band maximum (VBM) is composed by the filled oxygen 2p-orbitals (fig. 2.3). If these materials were stoichiometric, $E_F$ would be in the middle of $E_{o_x}$, but the intrinsic and/or extrinsic defects take $E_F$ near or within the ns conduction band. The nature of the CBM, primarily derived from large radii and spherical s-orbitals, allows having a good pathway for electron transport, since the orbitals of neighboring cations can easily overlap. [56]
Figure 2.3 – Schematic energy-level diagram for n-type oxide semiconductors. The arrows at $E_f$ represent the $E_f$ shift occurring due to intrinsic and/or extrinsic defects. Adapted from [2]

Table 2.1 presents a comparison between the typical electrical and optical properties found on ZnO and In$_2$O$_3$ thin films, with SnO$_2$ being also included for reference.

Table 2.1 – Typical optical and electrical properties found for thin films of ZnO, In$_2$O$_3$, and SnO$_2$, measured at 300 K. $\mu$ values in brackets correspond to the typical $\mu$ obtained in single crystals.

<table>
<thead>
<tr>
<th>Material</th>
<th>$E_{opt}$ (eV)</th>
<th>$\sigma$ (S cm$^{-1}$)</th>
<th>$N$ (cm$^{-3}$)</th>
<th>$\mu$ (cm$^2$ V$^{-1}$ s$^{-1}$)</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZnO</td>
<td>3.2-3.4 (dir)</td>
<td>$&lt;10^4$</td>
<td>$&lt;10^{21}$</td>
<td>5-50 (200-400)</td>
<td>[2, 4, 31, 32, 57, 58]</td>
</tr>
<tr>
<td>In$_2$O$_3$</td>
<td>2.7 (ind), 3.5-3.7 (ind)</td>
<td>$&lt;10^4$</td>
<td>$&lt;10^{21}$</td>
<td>10-50 (160)</td>
<td>[2, 4, 31, 32, 59]</td>
</tr>
<tr>
<td>SnO$_2$</td>
<td>3.6-4.3 (dir)</td>
<td>$&lt;10^3$</td>
<td>$&lt;10^{20}$</td>
<td>5-30 (240)</td>
<td>[4, 31, 32, 60]</td>
</tr>
</tbody>
</table>

For all the materials AVT around 80-90 % and $E_{opt}$ above 3 eV are achieved, in agreement to the requisites of a transparent material. In single crystals, $\mu$ is of the same order of magnitude for all the oxides. Even if In$_2$O$_3$ has larger 5s-orbitals that provide better overlapping than the 4s-orbitals of ZnO, the higher metal-atom number densities and shorter metal-metal distances of the latter tend to equilibrate the overall electrical properties achieved in both single crystalline semiconductors. It is also observed that $\mu$ measured in single crystals is considerably higher than the one obtained in deposited thin films. This would be expected, since thin films of these oxides generally exhibit a polycrystalline structure, regardless of the deposition technique and processing conditions used to fabricate them. As such, grain boundary scattering limits considerably the carrier transport, reducing $\mu$. [32, 62] In addition, note that in deposited thin films $N$ is generally much larger than in undoped

---

$^b$ The highest deviation occurs for single crystalline ZnO, where a large $\mu=400$ cm$^2$ V$^{-1}$ s$^{-1}$ was recently reported by Tsukazaki et al. [58] To achieve this, the authors had to use a Mg$_2$Zn$_{1-x}$O buffer layer to reduce structural defects arising from lattice mismatch and chemical dissimilarity to substrate materials.

$^c$ Even if SnO$_2$ is not explored in this work, note that the analysis of its electrical properties is more complicated than for ZnO and In$_2$O$_3$, because the difference in the thermodynamic stability of the Sn$^{2+}$ and Sn$^{4+}$ is very low and so highly resistive SnO phases may be formed in this material, for instance when too many oxygen vacancies are created. [1, 61]
single crystals, due to intrinsic defects created during deposition that can act as shallow donor levels. As shown by Ellmer, if single crystals of ZnO are intentionally doped to achieve \(N > 10^{20} \text{ cm}^{-3}\), \(\mu\) in single crystals and polycrystalline thin films with the same \(N\) are quite similar, because at this \(N\) range \(\mu\) is essentially controlled by ionized impurity scattering regardless of the material structure. [32] Given this background, it could be plausible to assume that by tuning the deposition conditions of thin films in order to achieve a very low \(N\), a large \(\mu\) could be obtained, which would represent an ideal condition for a TSO to be employed as a channel layer in a TFT. However, this trend is not observed for polycrystalline oxide semiconductors, since for very low \(N\) the energy associated with the grain boundaries is too high, so electrons cannot surmount them, i.e., carrier transport starts to be dominated by the energy barriers at the grain boundaries, which can only be surpassed if a larger \(N\) is used. [2] Hence, even if ZnO and In\(_2\)O\(_3\) have different structural properties, their electrical properties at the \(N\) ranges of interest for TCOs and TSOs are essentially controlled by the same mechanisms, ionized impurity scattering and grain barrier inhibited transport, respectively. This way, the typical electrical properties of both ZnO and In\(_2\)O\(_3\) polycrystalline thin films are quite similar.

2.1.3. Multicomponent amorphous oxide semiconductors: indium-zinc oxide and gallium-indium-zinc oxide

Even if the TCOs and TSOs mentioned until now are quite innovative materials when compared with covalent semiconductors, allowing to explore some unique applications, they always present a polycrystalline structure. In addition, although results in laboratory already show that it is possible to obtain good properties with low processing temperatures, most of the commercial applications of these materials rely on high (post-)deposition temperatures to achieve optimal performance. This is particularly relevant for ITO, which is currently the most widely used TCO, where temperatures above 200-300 °C are typically used for commercial applications. Higher temperatures directly affect the cost and time required to process the materials, besides limiting the type of substrates that are possible to use. Furthermore, due to the polycrystalline structure, carrier transport for oxides with low \(N\) (TSOs) is severely limited by grain boundary effects, as explained before. Besides this, polycrystalline materials are not desirable for large area applications, since it is hard to assure uniform and reproducible grain distribution and size, a problem that is well known in silicon technology. [63] Hydrogenated amorphous silicon (a-Si:H) is perhaps the best example of the successful implementation of an amorphous semiconductor in history, even if the electrical properties are considerably worse than those of polycrystalline silicon (poly-Si). Regarding oxide semiconductors, the first report on an amorphous material dates from the 1950s’, when Denton et al. showed that glasses containing a large amount of V\(_2\)O\(_5\) could present some electrical conductivity.
Several subsequent works followed the same theoretical principles, by employing different variable-valence transition metal oxides, but since carrier transport was dominated by a variable-range hopping mechanism, the resulting $\mu$ was rather low, around $10^{-4}$ cm$^2$ V$^{-1}$ s$^{-1}$. [56]

As stated before, In$_2$O$_3$ thin films can present an amorphous structure, but only when produced at low temperature and under a very narrow range of processing conditions. But contrarily to what happens with silicon, the electrical properties of polycrystalline and amorphous In$_2$O$_3$ films are quite similar. In fact, this was observed by Bellingham et al. in 1990 for films with $N>10^{20}$ cm$^{-3}$. [44] For this $N$ range, the authors found that carrier transport was essentially dominated by ionized impurity scattering both for polycrystalline and amorphous films and the structural disorder of the latter had a negligible effect on the electrical properties.

The material design concept introduced in 1995-96 by Hosono and co-workers revolutionized the field of amorphous oxide semiconductors: the authors proposed that multicomponent oxides composed of post-transition cations with a $(n-1)d^{10}s^0$ electronic configuration are amorphous and present similar $\mu$ to the polycrystalline materials in the degenerated state, with values around 10 cm$^2$ V$^{-1}$ s$^{-1}$. This was experimentally observed with various materials such as Cd$_2$GeO$_4$ implanted with H$^+$ or Li$^+$ ions, AgSbO$_3$ and Cd$_3$PbO$_4$. [65-68] Another striking feature of these materials is that they remain amorphous even when annealed at temperatures of 500 °C. Moreover, it was shown that free carriers could be generated either by ion implantation or by oxygen desorption after annealing (always preserving the amorphous structure), transforming highly resistive films with activation energies above 1 eV into highly conducting films with negligible activation energy, meaning that $E_F$ could be controlled from deep in the bandgap to above CBM.

The primary reason for the excellent properties of these amorphous multicomponent oxide semiconductors can be understood by analyzing the differences in the composition of the CBM between covalent (silicon) and ionic (oxide) semiconductors (fig. 2.4). In crystalline silicon, CBM is primarily composed by strongly directive and anisotropic sp$^3$ orbitals (fig. 2.4a), hence, when moving to an amorphous silicon structure there are significant changes in the bond angles (fig. 2.4b), creating a very large concentration of localized states with energy levels inside the bandgap. This results in severely degraded carrier transport in the amorphous state, which starts to be essentially controlled by hopping between localized tail-states, with band conduction never being achieved. A totally different situation is verified for oxide semiconductors: in this case, CBM is composed by the large spherical isotropic ns orbitals of the metallic cations (fig. 2.4c). If the radii of these orbitals is made larger than the inter-cation distance, which can be achieved for $n>4$, the neighboring orbitals always overlap, despite the degree of disorder of the material (fig. 2.4d). This means that even in the
amorphous state, oxide semiconductors always have a well defined carrier path in the CBM and large $\mu$ can be achieved. [56, 69]

![Diagram](image)

**Figure 2.4** – Schematics proposed by Nomura et al. of the orbitals composing the CBM on covalent semiconductors with $sp^3$ orbitals and ionic semiconductors with $ns$ orbitals (n$24$): (a) covalent crystalline; (b) covalent amorphous; (c) ionic crystalline; (d) ionic amorphous. [69]

Despite the novel and exciting properties exhibited by the initial multicomponent oxide semiconductors, they had somewhat limited capabilities because in some cases good $\sigma$ could only be achieved after ion implantation, while in others the proposed materials were composed by multivalent ions that during the change of their oxidation state (for instance, from Pb$^{4+}$ to Pb$^{2+}$) consumed a large fraction of the electrons generated via the formation of oxygen vacancies. [67] Hopefully, a large range of elements in the periodic table exhibit the $(n-1)d^{10}S^0$ electronic configuration required to obtain an amorphous semiconductor according to this model, including zinc, indium and gallium. These constitute the most widely explored cations for amorphous multicomponent oxide semiconductor fabrication, in the form of indium-zinc oxide (IZO) and gallium-indium-zinc oxide (GIZO). In IZO and GIZO, In$^{3+}$ cations are the main elements of the CBM, like in In$_2$O$_3$, but the incorporation of zinc (and gallium) in significant concentrations prevents the crystallization that easily occurs for In$_2$O$_3$. For room temperature deposited IZO, it is reported that the films are amorphous for a broad range of deposition conditions, at least in the range of 60/40 to 84/16 In/Zn cation % (atomic). [70] For IZO films with 50/50 In/Zn cation % the processing conditions start to be important to define the structure of the thin films and polycrystalline or amorphous structures are observed by different authors. [70-72] Depending on the composition and annealing atmosphere, IZO films are reported to be amorphous up to 600 °C. [72] Even if deposited at room temperature, sputtered IZO thin films already present electrical and optical properties quite similar
to ITO films produced at higher temperatures. [73] However, the application of IZO as a TSO seems to be limited, because $N$ cannot be easily decreased below $10^{17}$ cm$^{-3}$. [56] This can be solved by adding gallium to IZO: as Ga$^{3+}$ has a high ionic potential (+3 valence and smaller ionic radius than In$^{3+}$ and Zn$^{2+}$), this element can establish strong bonds with oxygen, preventing excessive free carrier generation due to oxygen vacancies. [56] Furthermore, given the higher structural disorder achieved with the addition of an extra cation, in GIZO a broader range of amorphous compositions can be explored. In fact, as demonstrated by Orita et al., zinc can even be made the predominant cation in GIZO without losing the amorphous structure. [74] Even if in this case the CBM is mainly derived from zinc 4s-orbitals rather than the larger 5s-orbitals when In$^{3+}$ is the predominant cation, good electrical properties can still be achieved.

Besides indium-containing multicomponent oxide semiconductors, indium-free possibilities are also being studied, such as zinc-tin oxide (ZTO) [75-77] and zinc-gallium-tin oxide (ZGTO). [61, 78] In these materials, where either Zn$^{2+}$ or Sn$^{4+}$ are the predominant metal cations, TSO properties close to the ones achieved with GIZO can be achieved, but this generally requires processing temperatures considerably larger, above 300-400 °C. Still, the exploration of this route is highly important due to the already mentioned scarcity of indium relatively to other post-transition metals.

Given that the study of (gallium-)indium-zinc oxide semiconductors is very recent and since the results obtained from this dissertation pretend to provide a contribute to this emerging area, rather than presenting in this section an exhaustive literature review on this topic, relevant results from literature will be mentioned in more detail in chapters 4 and 5, where the results obtained during this research work are presented and discussed.

### 2.2. High-$\kappa$ dielectrics

In a field-effect transistor the dielectric layer used between the gate electrode and the semiconductor constitutes an important component that defines to a large extent the performance and reliability of the device. Given that multicomponent oxide dielectrics based on high-$\kappa$ materials were preliminary explored and integrated in transparent TFTs during the research work of this dissertation, the importance and requisites of these materials are briefly discussed here.
2.2.1. Moving from low to high-κ dielectrics: material requirements

Since the first microprocessor, the Intel 4004, was introduced in 1971, [79] electronic circuits have been constantly integrating a higher density of increasingly smaller transistors in order to achieve higher performance, increased functionality and lower costs. This evolution was well predicted in 1965 by Gordon Moore, one of the co-founders of Intel, who stated that the number of transistors on a chip would double about every two years. [80] To have an idea of the numbers involved in this evolution, note that the Intel 4004 had a clock speed of 108 kHz, 2300 transistors and a manufacturing technology of 10 μm, while the Intel Penryn from 2007 exhibits a clock speed above 3 GHz and about 820 million transistors fabricated with 45 nm technology. Although semiconductor industry currently faces technological problems for further scale down, such as lithographic tools limitations and severe short-channel and quantum effects when the channel lengths of the transistors are reduced to the dimensions of a few silicon atoms, perhaps the most important issue arising in recent times is related with the dielectric layer. In single crystalline silicon technology, thermally grown SiO₂ is used as the dielectric and the successful Si/SiO₂ combination is probably what mostly contributes to the remarkable properties exhibited by MOSFETs. Si/SiO₂ represents an almost perfect interface, because thermal SiO₂ is not actually deposited but rather grown by the reaction of oxygen with silicon. However, the demand for miniaturization imposed that in the new generation of 45 nm transistors the thickness of the SiO₂ layer would need to be lower than 1 nm, which even for such an excellent insulator as thermal SiO₂ represents a critical issue, because gate leakage current \(I_\text{g}\) dramatically increases due to quantum tunneling effects. [81, 82] This creates a technological limitation that cannot be easily surpassed without looking for new device structures or dielectric materials. [83] One of the best possibilities to overcome this limitation involves the usage of materials with higher-κ than SiO₂, the so-called high-κ dielectrics. This way, thicker insulating films can be used, while maintaining the same capacitance per unit area. High-κ dielectrics started to be intensively studied in the mid-1990s, are currently being used to fabricate the Intel microprocessors with 45 nm feature sizes and will also be employed for the upcoming generation with 32 nm. [82, 84]

Given this background, it is clear the importance of high-κ dielectrics for present and future electronic circuits. However, materials with very large \(\kappa\) present some drawbacks, such as increased parasitic capacitances [85] and lower \(E_\text{g}\), since for most metal oxide dielectrics \(E_\text{g}\) is inversely proportional to \(\kappa\) (fig. 2.5a). [86] Although to assure the same capacitance per unit area of SiO₂ an high-κ dielectric can be thicker, thus preventing direct tunneling across the dielectric layer, if its \(E_\text{g}\) is too low undesirable \(I_\text{g}\) can still remain an issue, due to excitation of electrons or holes by Schottky emission into the dielectric conduction or valence bands, or also due to other defect-assisted transport mechanisms, such Poole-Frenkel effect or hopping conduction. [86, 87] But even if the \(E_\text{g}\)
of the dielectric layer is considerably larger than the one of the semiconductor, another requirement should be fulfilled to achieve good reliability: the offsets of the dielectric’s VBM (for a p-type transistor) and CBM (for a n-type transistor) relatively to the ones of the semiconductor should be at least 1 eV (fig. 2.5b). [81, 86]

Another important aspect to be considered is the structure of the dielectric material: while most of the high-κ dielectrics are polycrystalline even at low temperatures, amorphous structures are preferred because grain boundaries act as preferential paths for impurity diffusion and leakage current, resulting in inferior dielectric reliability. Besides that, amorphous materials present smoother surfaces, resulting in improved interface properties. [2, 83] The quality of the dielectric/semiconductor interface is preponderant determining the performance of the transistors and most high-κ materials exhibit midgap interface state densities one to two orders of magnitude higher than the one of thermal SiO₂. [83] Other considerations regarding the choice of a suitable dielectric involve its thermodynamic stability with the semiconductor and the process compatibility with current or expected tools. [83]

2.2.2. Dielectrics for low temperature processed thin-film transistors

For field-effect transistors processed at considerably lower temperatures than MOSFETs, such as the TFTs explored in this work, thermal SiO₂ is not considered as a possible dielectric. This is attributed to the high temperature required for its growth, not compatible with the glass substrates commonly used for TFT fabrication, and also due to semiconductor material constrains, because a high quality thermal SiO₂ layer requires a high quality single crystalline silicon wafer, but TFTs rather employ

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2. Transparent oxide (semi)conductors, dielectrics, thin-film transistors and displays background

**Figure 2.5 – Some properties of high-κ dielectrics: (a) relation between E₀ and κ; (b) calculated band offsets of oxide dielectrics on silicon. [86]**

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**d** Since a detailed exploration of dielectric materials is out of the scope of this dissertation, interested readers can find valuable information about this topic on a large number of sources, such as ref. [83] and a special edition of the MRS Bulletin, from March 2002 (which includes, for instance, refs. [86] and [87]).
deposited amorphous or polycrystalline semiconductors. Hence, chemical vapor deposited (CVD) SiO$_2$ or silicon nitride (SiN$_x$:H) are generally chosen as the dielectric materials for TFTs, regardless of their semiconductor technology.\footnote{The most relevant semiconductor technologies for TFTs will be discussed in section 2.3.3.} \cite{63} Even if these materials exhibit worse insulating properties than thermal SiO$_2$, higher thicknesses can be used, typically around 100-300 nm, because in TFTs the performance requirements are not as high as in MOSFETs and feature sizes are about two to three orders of magnitude larger in TFTs. While good performance can be obtained with deposited dielectrics when processed above 250–300°C, their properties are degraded when temperatures around 150°C are established as the maximum for transistor fabrication, which is imperative if low cost and/or flexible substrates are required. \cite{88-91} The lower performance is usually a consequence of less compact films and higher density of defects on the dielectric’s bulk and on its interface with the semiconductor when the processing temperature is decreased. Chemically deposited organic dielectrics have been investigated with promising results for TFTs produced at low temperature, but usually their growing and/or curing process is rather slow. \cite{92-94} Physical routes such as radio-frequency (r.f.) magnetron sputtering have also been tested for low temperature dielectric fabrication. This technique, even if perfectly suitable for low temperature fabrication, is theoretically not seen as a potential candidate for good quality dielectrics’ processing, because most of these materials are very hard to sputter, leading to the usage of high power densities ($P_{rd}$) that might damage the growing films and interfaces. Nevertheless, even when considering the recent oxide semiconductor-based TFTs technology, working devices were already obtained using low temperature sputtered SiO$_2$, \cite{95} ferromagnetic materials such as Bi$_{1.5}$Zn$_{1.0}$Nb$_{1.5}$O$_7$ with MgO capping layers, \cite{96} and high-$\kappa$ dielectrics such as Y$_2$O$_3$, \cite{97, 98} Al$_2$O$_3$, \cite{99} HfO$_2$, \cite{100} and Ta$_2$O$_5$. \cite{101} Given that the substrate/film bombardment can be a problem in sputtering, materials with a high-$\kappa$ are desirable because their added capacitance can compensate for the higher density of interface traps and thus improve the transistor performance, namely decrease the subthreshold swing ($S$) and the operating voltage, even if higher thicknesses than for SiO$_2$ have to be used. \cite{2} However, as mentioned before, most of these high-$\kappa$ dielectrics present a polycrystalline structure even when deposited at room temperature, whereas an amorphous structure is preferred to decrease $I_D$ and improve interface properties. Also, higher-$\kappa$ oxide dielectrics have lower $E_g$ (fig. 2.5a), which can bring additional problems regarding band offsets (fig. 2.5b). As a possible solution for this, a similar approach to the one followed for multicomponent oxide semiconductors can be used for the high-$\kappa$ dielectrics: by mixing a high-$\kappa$/low $E_g$ oxide with a low-$\kappa$/high $E_g$ oxide, for instance using a co-sputtering technique (see section 3.1.1), it is expected that the properties of the resulting multicomponent dielectric can be tuned by varying the relative proportions of the composing oxides. Moreover, given the induced structural disorder obtained by mixing the two oxides, an amorphous
structure can be obtained in the multicomponent dielectric thin film, coupled with a moderate-to-high-κ and improved $E_g$ over the binary high-κ oxide.

Sputtered Ta$_2$O$_5$, which has been extensively used as a dielectric in organic TFTs [102, 103] is selected in this work as a starting high-κ material, essentially due to its relatively high sputtering rate even with low $P_{s}$, which results in high throughput and low damage to the growing film and its interfaces. The combination of Ta$_2$O$_5$ with SiO$_2$ or Al$_2$O$_3$ has been found to be useful for applications such as optical filters and corrosion-resistant coatings, [104-106] but in most cases, the materials are grown as multilayer structures rather than as multicomponent layers. However, for a transistor’s dielectric, multicomponent layers (or alternatively multiple layers of multicomponent materials) are preferable due to the tendency of high-κ oxides to crystallize even when processed at low temperatures.

2.3. Thin-Film Transistors (TFTs)

TFTs are important electronic devices which are predominantly used as On-Off switches in active matrix backplanes of flat panel displays (FPDs). As most of the effort of this research work is focused on the production of TFTs, this section provides some relevant background about these devices, regarding their structure, physics and history. A comparison of the different semiconductor technologies currently available is also given, including the emerging oxide semiconductors.

2.3.1. Device structure and operation

A TFT is a device comprising three electrodes, gate, source and drain, one semiconductor placed between the source and drain electrodes and an insulator (or dielectric) inserted between the gate electrode and the semiconductor. The idea behind it is to have a current flowing between drain and source modulated by varying the potential between the gate and the source electrodes. [107] This modulation, known as field-effect, relies on the capacitive injection of carriers close to the dielectric/semiconductor interface, which is turned possible due to the parallel plate capacitor structure formed by the gate electrode, dielectric and semiconductor.

Figure 2.6 shows some of the most common structures employed to produce TFTs. According to the nomenclature initially defined by Weimer in 1960s, these structures are denominated by staggered or coplanar, depending if the source-drain and gate electrodes are on opposite sides or on the same side of the semiconductor. Inside staggered and coplanar structures, two configurations can be distinguished, top-gate (or normal) and bottom-gate (or inverted), depending on whether the gate electrode is on top or bottom of the structure. [63, 108]
Transparent oxide TFTs: production, characterization and integration

Each of these structures presents advantages/disadvantages, largely dictated by the materials used to fabricate the TFTs. For instance, the staggered bottom-gate configuration is widely used for the fabrication of a-Si:H TFTs, due to easier processing and enhanced electrical properties. As a-Si:H is light sensitive, the usage of this configuration is advantageous for the application of these TFTs in LCDs, since the metal gate electrode shields the semiconductor material from the effect of the backlight present on these displays. [108] On the other hand, a coplanar top-gate structure is normally preferred for poly-Si TFTs. This is mostly attributed to the fact that the recrystallization process of the semiconductor material generally requires high temperatures that could degrade the properties of other materials previously deposited, being favored if the semiconductor is a flat and continuous film without any layers beneath it. [108] Furthermore, the fact that in bottom-gate structures (both staggered and coplanar) the semiconductor surface is exposed to air can be explored as a way to easily modify its properties, for instance by the facilitated adsorption of impurities during annealing or plasma treatments in a suitable atmosphere. [107]

The schematics in fig. 2.6 only show the fundamental layers of a TFT, but other layers can also be introduced for several reasons. As an example, in silicon technology is common to use highly doped semiconductor layers at the source-drain regions, in order to form low-resistance contacts. Also, an insulating film is often deposited on top of the semiconductor layer in staggered bottom-gate structures. This can allow for more accurate etching of the source-drain electrodes, without damaging the semiconductor surface, i.e. act as an etch-stopper. [63, 109] This insulating layer can also have interesting effects on semiconductor films that strongly interact with environmental species such as oxygen or moisture, which are reflected in large variations of the electrical properties.
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exhibited by the TFTs. [107] This is particularly relevant for some of the first semiconductors used in TFTs, such as CdSe, and also for oxide semiconductors, as will be shown in chapter 5. Additionally, the insulating layer on top of the TFT structure can work as an effective mechanical and chemical protection of the devices from subsequent processes, such as their integration with liquid crystal cells. [110]

TFTs are quite similar to other field-effect devices in terms of operation and composing layers, such as the well known MOSFETs used in high performance applications as microprocessors or memories. However, important differences exist between these devices, some of them readily seen by inspecting their typical structures (fig. 2.7). First, while TFTs use an insulating substrate, normally glass, in MOSFETs the silicon wafer acts both as the substrate and the semiconductor. Thus, higher performance naturally arises for MOSFETs, given that the electrons flow in a single crystalline semiconductor, rather than in a polycrystalline or amorphous one on TFTs. Also, the temperatures involved in the fabrication of both devices are quite different: while processing temperatures exceeding 1000 °C are common for MOSFETs, for instance to create the dielectric layer, in TFTs they are limited by parameters such as the softening point of the substrate, which for most common glass substrates does not exceed 600-650 °C. [63] In addition, MOSFETs have p-n junctions at the source-drain regions, which are absent in TFTs. This is related with another important difference in device operation: even if both TFTs and MOSFETs rely on the field-effect to modulate the conductance of the semiconductor close to its interface with the dielectric, in TFTs this is achieved by an accumulation layer, while in MOSFETs an inversion region has to be formed close to that interface, i.e., a n-type conductive layer is created in a p-type silicon substrate.

![Figure 2.7 – Comparison between the typical structures of MOSFETs and TFTs.](image)

The ideal operation of a TFT can be described by analyzing the energy band diagram of the capacitor comprised by the gate electrode, dielectric and semiconductor, upon the application of different voltages in the gate electrode \( V_G \), as shown in fig. 2.8.
This analysis assumes an ideal case, considering a n-type semiconductor (given that $E_f$ is shifted from the midgap towards the CBM) and that charge accumulation or depletion does not exist close to the dielectric/semiconductor interface or to the semiconductor back-surface in the unbiased state. [111] Under this situation, an upward band-bending results for $V_G<0$ V, since the negative $V_G$ repels mobile electrons from the dielectric/semiconductor interface, creating a depletion layer near that region that can be extended through the entire semiconductor for $V_G<<0$. In (a) and (b) situations, even if a large drain-to-source voltage ($V_D$) is used, a very low current flows between drain and source ($I_D$), corresponding to the Off-state of the transistor. On the other hand, when $V_G>0$ V (fig. 2.8c), electrons are accumulated close to the dielectric/semiconductor interface, leading to a downward band-bending in that region, which becomes even more pronounced for $V_G>>0$ V. For this condition, a considerable $I_D$ starts flowing upon the application of $V_D$, corresponding to the On-state of the transistor. Based on the description above, a conductive channel is readily formed with a very small increase on $V_G$. However, in a real case, the threshold voltage ($V_T$) corresponding to significant charge accumulation at the dielectric/semiconductor interface deviates from 0 V, being a function of the gate electrode-semiconductor work function difference, the background carrier concentration of the semiconductor, the charge density residing within the dielectric and the trap density at the interface and within the semiconductor. [107, 111] For an n-type TFT, depending on whether $V_T$ is positive or negative, the devices are designated as enhancement or depletion mode, respectively. Both types are useful for circuit fabrication (for instance, NMOS technology requires both enhancement and depletion mode transistors), but for the common function of TFTs as simple electronic switches, enhancement mode is preferable, because no $V_G$ is required to achieve the Off-state, turning easier the circuit design and minimizing power dissipation. [112]

When the transistor is in the On-state, different operation regimes can be distinguished, depending of the value of $V_D$:

\[ V_G, V_D, I_D \text{ and } I_D \text{ are used throughout this dissertation, given that the source electrode is always assumed to be grounded, but these notations have exactly the same meaning as } V_{GG}, V_{DS}, I_{SS} \text{ and } I_{DS}. \]
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- When \( V_D < V_G - V_T \), the TFT is in the pre-pinchoff regime, and \( I_D \) is described by: \([107]\)

\[
I_D = C_i \mu_{FE} \frac{W}{L} \left( V_G - V_T - \frac{1}{2} V_D^2 \right)
\]  

(2.1)

where \( C_i \) is the gate capacitance per unit area, \( \mu_{FE} \) is the field-effect mobility, \( W \) is the channel width and \( L \) is the channel length. For very low \( V_D \), the quadratic term can be neglected, yielding a linear relation between \( I_D \) and \( V_D \). In this situation, the accumulated charges are considered to be uniformly distributed throughout the channel (fig. 2.9a).

- When \( V_D > V_G - V_T \), the accumulation layer close to the drain region becomes depleted, leading to the saturation of \( I_D \). This phenomenon is designated by pinchoff (fig. 2.9b) and starts to occur when \( V_D = V_G - V_T \). At the post-pinchoff or saturation regime, \( I_D \) is described by:

\[
I_D = C_i \mu_{sat} \frac{W}{2L} (V_G - V_T)^2
\]  

(2.2)

where \( \mu_{sat} \) is the saturation mobility.

The equations describing the operation of field-effect transistors are generally based on the assumption that the rate of variation (i.e., gradient) of the lateral field within the channel is much smaller than the rate of variation of the vertical field, i.e., the channel is seen as one-dimensional. [113] This concept was initially proposed by Shockley and is known as “gradual channel approximation”. Even if this approximation is not valid near the drain electrode when the transistor is in saturation regime or for short-channel devices, it describes fairly well most of the operation of TFTs, which generally have \( L \) much larger than the dielectric thickness. [114] Still, it is important to mention that equations 2.1 and 2.2 assume \( \mu_{FE} \) and \( \mu_{sat} \) to be constant. For most of the TFTs, with particular relevance for oxide semiconductor-based ones (as will be shown in chapter 5), this is not valid and \( \mu_{FE}(V_G) \) and \( \mu_{sat}(V_G) \) should be considered instead. [75]

![Schematics of different operation regimes of a TFT in the On-state](image)

*Figure 2.9 – Schematics of different operation regimes of a TFT in the On-state: (a) pre-pinchoff \((V_D < V_G - V_T)\); (b) post-pinchoff \((V_D > V_G - V_T)\).*

The static characteristics of TFTs are accessed by their output and transfer characteristics, shown in figs. 2.10a and 2.10b, respectively.
In output characteristics, $V_D$ is swept for different $V_G$ values, allowing to clearly observe the pre- and post-pinchoff regimes described before. Different qualitative information can be assessed by output characteristics: for instance, a decreasing separation between $I_D$-$V_D$ curves for increasing $V_G$ is indicative of $\mu$ degradation for that $V_G$ range; the flatness of the $I_D$-$V_D$ curves at the post-pinchoff regime permits to evaluate if the channel layer can be fully depleted close to the drain electrode for the range of $V_D$ and $V_G$ used. Good saturation is an important requisite in electronic circuits, specially if the TFT is used as a current limiter; [107] the low $V_D$ region (linear) also provides useful information regarding contact resistance, as demonstrated in section 5.1.3.

On the other hand, transfer characteristics, where $V_G$ is swept for a constant $V_D$, permit to extract a large number of quantitative electrical parameters, which are summarized below:

- **On-Off ratio** – this is simply defined as the ratio of the maximum to the minimum $I_D$. The minimum $I_D$ is generally given by the noise level of the measurement equipment or by $I_O$, while the maximum $I_D$ depends on the semiconductor material itself and on the effectiveness of capacitive injection by the field-effect. On-Off ratios above $10^6$ are typically obtained in TFTs and a large value is required for their successful usage as electronic switches; [108]

- **$V_T$ and turn-on voltage ($V_{on}$)** – as previously defined, $V_T$ corresponds to the $V_G$ for which an accumulation layer or conductive channel is formed close to the dielectric/semiconductor interface. $V_T$ can be determined using different methodologies, such as linear extrapolation of the $I_D$-$V_D$ plot (for low $V_D$) or of the $I_D^{0.5}$-$V_D$ plot (for high $V_D$), $V_G$ corresponding to a specific $I_D$, ratio of conductance and transconductance, among others. [115] Even if considering only one methodology, large ambiguity can arise on the determination of $V_T$ (for instance, by using different fitting parameters on the linear regressions). To avoid this ambiguity, the concept of $V_{on}$ is largely used in literature, simply corresponding to the $V_G$ at which $I_D$ starts to increase as seen

---

*Figure 2.10 – Typical (a) output and (b) transfer characteristics of a n-type oxide semiconductor-based TFT.*
in a $\log I_D-V_G$ plot, or in other words, the $V_G$ necessary to fully turn-off the transistor. [116] In the analysis presented in chapters 5 and 6 of this dissertation $V_{on}$ is mostly employed rather than $V_T$.

- **Subthreshold swing ($S$)** – the inverse of the maximum slope of the transfer characteristic, it indicates the necessary $V_G$ to increase $I_D$ by one decade:

$$S = \left( \frac{d\log(I_D)}{dV_G} \right)_{max}^{-1}$$

Typically, $S<<1$, around 0.10-0.30 V dec$^{-1}$ and small values result in higher speeds and lower power consumption. [108]

Besides the parameters described above, $\mu$ of the free carriers in the channel is also a very important characteristic of TFTs, as it directly affects their maximum $I_D$ and switching speed, thus defining their range of applications. [91] For instance, it has a direct impact on the maximum operating frequency or cutoff frequency ($f_{co}$), which can be defined as: [111]

$$f_{co} = \frac{\mu V_D}{2\pi L^2}$$

Mobility is a measure of the efficiency of carrier transport in a material, depending of several scattering mechanisms, such as lattice vibrations, ionized impurities, grain boundaries and other structural defects. [111, 117] When $\mu$ is measured in a field-effect device, additional scattering arises because the carriers are confined within a narrow region, close to the dielectric/semiconductor interface. Hence, additional mechanisms such as Coulomb scattering from dielectric charges and from interface states or surface roughness scattering contribute to decrease $\mu$. [117] However, it has to be noted that in a TFT $\mu$ is modulated by the bias conditions, since the increase on $V_G$ contributes to decrease the barriers associated with grain boundaries in polycrystalline semiconductors and/or allows $E_F$ to be taken close or above CBM, where $\mu$ is larger. As will be seen throughout this dissertation, this last situation is particularly relevant in oxide semiconductor-based TFTs. Different methodologies can be used to extract $\mu$ in a TFT, with $\mu$ assuming different nomenclatures for each one of them:

- **Effective mobility ($\mu_{eff}$)** – obtained by the conductance ($g_d$) with low $V_D$, according to:

$$\mu_{eff} = \frac{g_d}{W \cdot L \cdot (V_G - V_T)}$$

This is usually considered the most correct estimation of $\mu$, including the effect of $V_G$. [117] However, it requires the previous determination of $V_T$, which as seen before can be associated with some error, and is sensitive to contact resistance, since it is extracted at low $V_G$;

- **Field-effect mobility ($\mu_{fe}$)** – obtained by the transconductance ($g_m$) with low $V_D$, according to:
\[ \mu_{FE} = \frac{g_m}{C_i \frac{W}{L} V_D} \]  

(2.6)

This is the most commonly used mobility estimation used for TFTs. Although it neglects the effect of \( V_G \) and it stills being sensitive to contact resistance effects, it does not require the determination of \( V_T \) and it is easily extracted by the derivative of the transfer characteristics;

- Saturation mobility (\( \mu_{sat} \)) – obtained by the transconductance with high \( V_D \), according to:

\[ \mu_{sat} = \frac{(d \sqrt{I_D})^2}{\frac{1}{2} C_i \frac{W}{L} V_G} \]  

(2.7)

\( \mu_{sat} \) is also very common in TFTs’ literature. It does not require \( V_T \) and as a high \( V_D \) is used is less sensitive to contact resistance. However, it is not physically accurate, as it describes a situation where the channel is pinched-off, i.e., its effective length is smaller than \( L \), which is intrinsically not assumed by the gradual channel approximation used to derive equations 2.1 and 2.2.

Besides these three methodologies, others can be found in literature. From these, particular relevance is assumed by the ones proposed by Hoffman, designated by average and incremental mobility, \( \mu_{avg} \) and \( \mu_{inc} \) respectively. [116] While the former provides an average value of all the carriers induced in the channel, the latter probes the mobility of carriers as they are incrementally added to the channel, thus providing valuable insights into channel carrier transport.

2.3.2. Brief history of TFTs

The first reports on TFTs date from almost 80 years ago and are attributed to Lilienfeld and Heil. [118-121] At that time, little was known about semiconductor materials and vacuum techniques to produce thin films were far from being established. Hence, these first reports are actually concept patents and no evidence exists about the production of working devices. Still, in these patents, the idea of controlling the current flow in a material by the influence of a transversal electrical field was already present. One of Lilienfeld first patents, published in 1930, describes the basic principle of what is known today as the metal-semiconductor field-effect transistor (MESFET, fig. 2.11a), while other, published three years later, already shows the concept of a device where an insulating material (aluminum oxide) is introduced between the semiconductor (cooper sulfide) and the field-effect (or gate) electrode (aluminum), anticipating the so-called metal-insulator-semiconductor field-effect transistor (MISFET, fig. 2.11b). [122] It is also noteworthy that in the MISFET patent, the
2. Transparent oxide (semi)conductors, dielectrics, thin-film transistors and displays background

thickness specified for the insulating layer, 100 nm, is very close to the one used nowadays in TFTs.

[bib][107]

**Figure 2.11 – Initial patents of field-effect devices submitted by Lilienfeld: (a) MESFET; (b) MISFET.** [122]

The first reports of current modulation by field-effect are attributed to Shockley and co-workers at Bell Laboratories in the 1940s, by using a germanium thin film separated from a gate electrode by a thin film of mica. [107] The very small change in the conductivity of germanium, considerably lower than the theoretically expected, was attributed to charge trapping in surface states. Even if the result was disappointing regarding the application of the structure as a practical device, it allowed making great advances on the study of surface defects of semiconductors. During these studies, in late 1947, Bardeen and Brattain discovered the point-contact transistor (fig. 2.12a) [123] and latter on, in 1948, Shockley proposed the p-n junction transistor. [124] But the need for a solid-state amplifier with a higher input impedance than the junction transistor persisted. This was achieved with the junction field-effect transistor (JFET) proposed by Shockley in 1952 (fig. 2.12b). [125] In this case, a reverse biased p-n junction was separating the conductive channel from the gate electrode. This work was extremely important to define the theoretical operation principles of field-effect devices, including the well known “gradual channel approximation”, being most of these principles still used in the analysis of modern TFTs and other field-effect devices. The work of Shockley, Bardeen and Brattain related with semiconductors and transistors allowed them to receive the Noble Prize in physics in 1956.
It took one more decade for the first TFT to be produced. This was achieved by Weimer at the RCA Laboratories in 1962. [126] Weimer used a vacuum technique (evaporation) to deposit gold electrodes, a polycrystalline cadmium sulfide (CdS) n-type semiconductor and a silicon monoxide insulator, using shadow masks to define the patterns of these layers. Another work from Borkan and Weimer also provided an analysis of the characteristics of these devices, based on the models initially proposed by Shockley. [127] During the 1960s' other works on TFTs appeared, such as the ones from Shallcross or Weimer, using semiconductors such as CdSe or tellurium, respectively [128, 129]. However, the emergence of the MOSFETs between 1960 and 1963, employing single crystalline silicon technology, with the works from Kahng/Atalla and Hofstein/Heiman, pushed researchers away from TFT technology, since MOSFETs had remarkable electrical properties, highly promising for fast integrated circuits. [107, 130] Nevertheless, for large area applications, MOSFETs represented a prohibitive cost when compared with TFTs. The turning point that motivated again the research on TFTs was the work presented by Lecnher et al. in 1971, where the authors proposed to use TFTs to control each pixel of a LCD, obtaining considerably less crosstalk, lower response time and higher contrast ratios than the ones achieved when controlling liquid crystals with the more conventional x-y disposed electrodes. [131] A prototype using an array of CdSe TFTs integrated in a LCD was demonstrated by Brody and co-workers in 1973 (fig. 2.13). [132]

Figure 2.12 – Work on transistors in late 1940s’ and early 1950s’: (a) point-contact transistor; (b) JFET. [63]

Figure 2.13 – First LCD employing TFTs as pixel switching elements, by Brody and co-workers. [132]
But the largest innovation in terms of TFT development, that mostly dictated the success of this technology for so many decades, was the introduction of a-Si:H as a semiconductor material in TFTs. This was reported by LeComber, Spear and Ghaith in 1979, as a natural consequence of their work on the analysis of the density of states in disordered structures. [133, 134] In spite of exhibiting considerably lower $\mu$ than polycrystalline materials such as CdSe (about 1 against 150-200 cm$^2$V$^{-1}$s$^{-1}$), a-Si:H was perfectly suitable for the application of TFTs as switching elements in LCDs, since it allowed for low cost, good reproducibility and uniformity in large areas and $On-Off$ ratios exceeding $10^6$.

The study on a-Si:H TFTs continued during the 1980s’, with new improvements being achieved regarding fabrication processes, structures and material combinations. Also, the knowledge of the physics of devices employing this semiconductor material was considerably broadened, for instance with the work of Powell and co-workers. [135, 136] Although CdSe TFTs were still being studied with the main propose of obtaining a viable alternative for a-Si:H TFTs when high $\mu$ was needed, this objective was mostly achieved with the appearance of poly-Si as a semiconductor material in TFTs. A poly-Si-based TFT was initially reported by Depp et al. in 1980 and in the next few years it was already possible to achieve $\mu_{\text{eff}}=400$ cm$^2$V$^{-1}$s$^{-1}$, starting to approach the values typically obtained in MOSFETs. [63] The large $\mu_{\text{eff}}$ of these transistors allowed their application not only as switching elements but also as driver circuitry devices, theoretically decreasing costs and complexity of LCD fabrication. However, poly-Si TFTs had a large cost, mostly because they required high temperature fabrication processes, which were only compatible with quartz substrates, not with normal glass. A considerable decrease on the processing temperature of poly-Si TFTs to around 550 °C was only reported in 1991, by Little et al. from Seiko-Epson. [137] However, these low-temperature poly-Si (LTPS) TFTs could not easily penetrate in the LCD market, which was already widely dominated by a-Si TFTs. Also, the intrinsic limitation of the polycrystalline structure of the semiconductor material imposed several restrictions to large area processing, as previously happened with CdSe TFTs.

The application of organic materials as semiconductors in TFTs was also another interesting technology introduced in 1990s’. At the beginning of that decade, Garnier reported TFTs using evaporated hexathiophene as a semiconductor material, resulting in devices with comparable performance to a-Si:H TFTs. [138] Organic semiconductors have, however, a great advantage over a-Si:H, which is their extremely low processing temperature. This is the reason why organic semiconductor devices in general and organic TFTs in particular are pointed as one of the most promising technologies for flexible electronics (fig. 2.14).
In terms of TFT technologies, the new millennium is marked by the usage of a revolutionary class of transparent semiconductor materials as channel layers: the oxide semiconductors. Although the “big-boom” of this technology is normally associated with reports on ZnO TFTs presented in 2002-2003, there were some tentative applications of oxide semiconductors as channel layers in TFTs forty years before this, almost coincident with the initial CdS TFTs reported by Weimer. In fact, back in 1964, Klasens and Koelmans proposed a TFT comprising an evaporated SnO\textsubscript{2} semiconductor on glass, with aluminum source-drain and gate electrodes and an anodized Al\textsubscript{2}O\textsubscript{3} gate dielectric. [140] Few details regarding electrical performance are provided and the transparent semiconductor is essentially used to demonstrate a new self-aligned lift-off process, where the SnO\textsubscript{2} layer allows to expose the photoresist to UV light penetrating from the bottom of the structure in all the areas expect the one shielded by the aluminum gate electrode, defining this way the pattern of the source-drain electrodes (fig. 2.15a). In 1968, Boesen and Jacobs reported a TFT with a lithium-doped ZnO single crystal semiconductor, with evaporated SiO\textsubscript{x} dielectric and aluminum electrodes, but a very small \(I\text{\textsubscript{D}}\) modulation by \(V\text{\textsubscript{G}}\) and no \(I\text{\textsubscript{D}}\) saturation were observed on these devices. [141] Similar poor performance was obtained in SnO\textsubscript{2} TFTs by Aoki and Sasakura in 1970. [142] In 1996, oxide semiconductors reappeared as channel layers, with two reports on ferroelectric field-effect devices employing SnO\textsubscript{2}:Sb and In\textsubscript{2}O\textsubscript{3}, by Prins et al. and Seager, respectively. [143, 144] Given that the main intent of the authors was to demonstrate hysteresis associated with the ferroelectric behavior, little information is provided on these papers about device performance, but Prins and co-workers, for instance, reports a low \textit{On-Off} ratio of 60. Still, it is noteworthy to observe that full transparency is for the first time persuaded in a TFT and it is only severely affected by the SrRuO\textsubscript{3} gate electrode (fig. 2.15b), although the authors mention that they also fabricated a fully transparent TFT by using a heavily doped SnO\textsubscript{2} gate electrode.
But good performing devices showing that oxide semiconductor-based TFTs could be a viable technology only started to appear in 2002-2003, with the reports on ZnO TFTs by Masuda et al., Hoffman et al. and Carcia et al. [33, 112, 145] The first two authors even report fully transparent devices (comprising TCO-based electrodes), already allowing to obtain respectable performance, comparable and even surpassing in some aspects the one typically exhibited by a-Si:H and organic TFTs, mostly in terms of $\mu_{ce}$, which could be as high as 2.5 cm$^2$V$^{-1}$s$^{-1}$. However, the processing or post-processing temperatures of the semiconductor necessary to obtain good devices were still quite high, between 450-600 °C. But the work from Carcia et al. showed that using r.f. magnetron sputtering to deposit ZnO, similar electrical properties could be achieved with room-temperature processing of the semiconductor layer, even if on this case fully transparent structures were not demonstrated. During 2003-2004 several reports continued to appear on oxide semiconductor-based TFTs, bringing different innovations to this emerging area. Some of the most important achievements were: ZnO TFTs exhibiting improved device performance (mainly regarding $\mu_{ce}$) while keeping low or even room temperature ZnO processing; [34, 146, 147] non-vacuum processes to produce the ZnO layers; [148] first simulations of ZnO TFTs assuming that their properties are largely dictated by the polycrystalline nature of ZnO; [149] new methods for extraction of mobility in ZnO TFTs; [116] application of ZnO TFTs as UV photodetectors; [150, 151] exploration of SnO$_2$ TFTs; [152] use of In$_2$O$_3$ or ZnO nanowires as channel layers. [153-156]

While most of the research work was being devoted to binary compounds such as ZnO, In$_2$O$_3$ or SnO$_2$, Nomura et al. suggested in 2003 to use a complex InGaO$_3$(ZnO)$_5$ (or GIZO) single-crystalline semiconductor layer in a TFT. [157] This layer was epitaxially grown on an yttria-stabilized zirconia substrate and allowed to obtain an impressive $\mu_{eff}=80$ cm$^2$V$^{-1}$s$^{-1}$, $V_{on}=-0.5$ V and $On-Off$ ratio$=10^6$. Even if a very high temperature of 1400 °C was necessary to attain this level of performance, it
showed that oxide semiconductor-based TFTs possessed a large room for improvement. And in fact, in the next year Nomura et al. presented a work that definitely proved the enormous potential of oxide semiconductors (and multicomponent oxides in particular) for TFT applications, by demonstrating a transparent TFT on a flexible substrate using near-room temperature processing (fig. 2.16). [69] For this end, they used a PLD deposited amorphous GIZO layer as the semiconductor. Even if the performance was far away from the single-crystalline TFTs presented by the same authors, $\mu_{sat}=9$ cm$^2$ V$^{-1}$ s$^{-1}$, $V_I=1$-2 V and On-Off ratio$=10^4$ could still be achieved, mostly because the low sensitivity of these multicomponent oxides to structural disorder, as explained in section 2.1.3.

*Figure 2.16 – Flexible substrate with transparent GIZO TFTs presented by Nomura et al. in 2004. [69]*

Nomura’s work opened the door for an impressively growing number of publications in the next years regarding the application of amorphous multicomponent oxides as channel layers in TFTs. Several combinations of cations with $(n-1)d^{10}ns^0$ $(n\geq4)$ electronic configuration started to be used for this end, being ZTO, [75-77, 158] IZO, [71, 159-161] and GIZO [61, 162-166] the most widely explored ones.$^6$ With the continuous improvements verified on these devices, it is now common to obtain remarkable electrical properties, considerably superior to a-Si:H or organic TFTs, such as $\mu_{FE}$ above 10 cm$^2$ V$^{-1}$ s$^{-1}$, close to 0 $V_{on}$, On-Off ratio exceeding $10^7$ and $S=0.20$-0.25 V dec$^{-1}$, with the indium-based semiconductors having the added advantage of allowing for very low or even room temperature processing. In fact, nowadays the processing temperature of these TFTs is dictated not by the semiconductor layer, but rather by the dielectric. Furthermore, it is important to note that if flexible and fully transparent TFTs are envisaged, the optimization of highly conducting TCOs deposited near room temperature for application as source, drain and gate electrodes is also a crucial requirement. [73, 167, 168]

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$^6$ Note that the given references are just a few examples of the large number of reported works, with many more being available, specially for the period comprised between 2007-2009.
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2.3.3. Present and future semiconductor materials for TFTs

During the last section, several properties of the different TFT technologies regarding the respective semiconductor materials were already pointed out. Here, a more comprehensive comparison between the most important TFT technologies available nowadays is made, based on costs, processing and performance of the devices. Table 2.2 gives an overview of these characteristics for a-Si:H, poly-Si, organic and amorphous oxide semiconductor-based TFTs.

Table 2.2 – Comparison between most relevant TFT technologies regarding the semiconductor materials.

<table>
<thead>
<tr>
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<th>Inorganic semiconductors</th>
<th>Organic semiconductors</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>a-Si:H</td>
<td>poly-Si</td>
</tr>
<tr>
<td>Maturity/infrastructures</td>
<td>★★★★</td>
<td>★☆☆☆</td>
</tr>
<tr>
<td>Large area deposition</td>
<td>★★★★</td>
<td>★☆☆☆</td>
</tr>
<tr>
<td>Processing temperature</td>
<td>★☆☆☆</td>
<td>★☆☆☆</td>
</tr>
<tr>
<td>Cost</td>
<td>★☆☆☆</td>
<td>★☆☆☆</td>
</tr>
<tr>
<td>Transparency</td>
<td>★☆☆☆</td>
<td>★☆☆☆</td>
</tr>
<tr>
<td>Electrical performance</td>
<td>★☆☆☆ / ★☆☆☆</td>
<td>★☆☆☆</td>
</tr>
<tr>
<td>Electrical stability</td>
<td>★☆☆☆</td>
<td>★☆☆☆</td>
</tr>
<tr>
<td>Environmental stability</td>
<td>★☆☆☆</td>
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</table>

The maturity of the a-Si:H TFTs technology is unquestionably greater than any of the other technologies. In fact, these devices are studied for almost forty years, and their strengths and limitations are well known. Moreover, there is a huge industrial implementation of a-Si:H TFTs, mostly caused by its successful use as switching elements in LCDs. But even if oxide semiconductor-based TFTs are only now emerging, it can be expected that their industrial implementation will be facilitated, given that they can use the processing and lithographic tools already existent in LCD industry, for instance, the sputtering systems used to fabricate TCO films used as top LCD electrodes (see section 2.4.2 for a brief description of a LCD structure). If physical techniques as sputtering are considered, another advantage arises to oxide semiconductors in comparison with silicon-based technologies, since only argon and oxygen need to be used, rather than explosive gases such as silane, phosphine or diborane.

Poly-Si presents a great disadvantage regarding large area deposition: due to the polycrystalline structure of this semiconductor, the electrical properties are highly dependent of aspects such as grain size and orientation. Thus, the lack of uniformity and reproducibility in large areas are
important drawbacks of this technology. On the contrary, a-Si:H, organic and oxide semiconductors can all exhibit amorphous structures, which are ideal for large area deposition. To obtain larger grain sizes (hence higher performance) in poly-Si, processing temperatures higher than for the other semiconductor technologies are required, but even a-Si:H generally requires temperatures exceeding 250-300 °C to reach its best performance. Oxides and mainly organic semiconductors require the lowest processing temperature, which makes them compatible with inexpensive glass or even plastic substrates, turning possible the concept of flexible electronics. This is also traduced in lower costs for these technologies. Also, the advent of oxide semiconductor processing techniques such as ink-jet or spin-coating, until now mostly devoted to organic materials, permits to foreseen further cost reductions. Still, benefiting from its well established industry, a-Si:H TFTs also present nowadays low production costs. Regarding poly-Si, the fact that it requires high temperature or complex/expensive crystallization methods, such as excimer laser annealing (ELA), results in higher-cost TFTs, even if the base material, silicon, is the second most abundant element in the earth’s crust. [169]

Transparency is naturally a large advantage of oxide semiconductors, although some organic semiconductors also present reasonable transparency in the visible range. This characteristic is important not only for the fabrication of fully transparent electronic circuits but also to increase the aperture ratio in displays, which directly results in improved brightness levels. [108] Furthermore, this means that transparent TFTs can be made with large W/L ratios, allowing them to supply larger currents for a given supply voltage, which is extremely important for applications where the TFT is used as a current driver, as in OLED displays (see section 2.4.2). [170]

Regarding electrical performance, poly-Si TFTs have the advantage of exhibiting the highest $\mu_{FE}$, which even for LTPS TFTs can reach 200 cm² V⁻¹ s⁻¹. [171] As pointed out earlier, this feature allows to use them also for the drivers circuitry in LCDs. a-Si:H and organic semiconductor TFTs have very small $\mu_{FE}$, typically less than 1 cm² V⁻¹ s⁻¹, while oxide semiconductor-based TFTs exhibit intermediate $\mu_{FE}$ values between poly-Si and a-Si:H TFTs, but more than 1 order of magnitude larger than a-Si:H. Still, even if poly-Si TFTs have a clear advantage regarding $\mu_{FE}$, it should be noted that these devices generally exhibit large leakage currents, which are associated with electron-hole generation stimulated by electric fields, via the trap-states on the grain boundaries. [172] This is traduced in reduced On-Off ratios when compared with the other TFT technologies, limiting their application as switching elements, specially for large area and high resolution displays. Even if little is known yet about long term stability of oxide TFTs, the initial results show that $V_T$ shift under constant bias or current stress is the predominant instability effect, but the magnitude of variation can be quite smaller than the exhibited by a-Si:H TFTs, as will be shown in section 5.1.6. Furthermore, given the large $E_g$ of oxide semiconductors, their properties are not significantly changed when exposed to
visible light, contrarily to a-Si:H (and also to poly-Si, although to a considerably less extent), where degradation can arise due to the creation of dangling bonds according to the Staebler-Wronski effect, with the initial properties only being reestablished after an annealing treatment. [173] This imposes the usage of light shields in silicon-based TFTs, increasing the process complexity, cost, and contributing to decrease even more the aperture ratio when these TFTs are used in displays. Even if UV filters have to be used for oxide semiconductor-based TFTs to block wavelengths lower than 400-450 nm, these filters do not compromise the overall appearance of the devices. [174] Organic materials also present a well known sensitivity to environmental species, such as water and oxygen, which can even permanently affect their properties, hence a meticulous passivation step is required for these devices. Even if this passivation step is a requisite for subsequent integration of devices, regardless of their semiconductor technology, it will be shown in chapter 5 that the interaction with oxygen can even be advantageous for oxide semiconductor-based TFTs.

Based on all this, it seems that oxide semiconductors provide a solid and viable alternative for the present and future of TFTs, covering important drawbacks of the existing technologies, ending up being a very attractive technology that allows for transparent, low cost, low temperature and high performance devices.

2.4. Displays

Nowadays, TFTs are mostly used as pixel switching elements in FPDs, particularly in LCDs. Given the relevance of displays for the present and future TFT industry, this section gives a brief overview of the display market and its future trends. The most relevant frontplane FPD technologies, LCDs and OLEDs, are compared regarding their main characteristics and the requisites they impose to the TFTs.

2.4.1. Market overview and future trends

Displays constitute one of the most interesting markets in all the electronics area, both technological and economically. The first practical and durable cathode ray tube (CRT) for a TV was made by Du Mont, in 1931. [175] However, only after World War-II, at the beginning of the 1950 decade, a market for black-&-white displays in general and TVs in particular started to emerge. Some years later, color CRTs started to be commercialized, although at a prohibitive price: for instance, one of the first color TV commercially available, the RCA CT-100, was being sold for 1000 USD in 1954, which was equivalent to the price of an automobile by that time. [176] Color CRTs dominated the display market for more than three decades. However, a new display technology started to emerge in the
1990s': the FPDs, with particular relevance for the LCDs. These offered immediate advantages in terms of power consumption, weight and space, which allowed not only to replace existing TV sets but also to integrate displays in portable applications, such as cell phones and notebooks, something unthinkable with the bulky and heavy CRT technology. Very recently, in 2007-2008, LCD shipments started to supplant CRTs [177] and LCDs are increasingly becoming the dominant FPD technology even for large size screens (more than 40”), a market which until 2006 was dominated by another FPD technology, the plasma displays (PDPs). [178] The continuous development in display’s area does not show any trends to slow down and another technology emerged at the beginning of the millennium, being expected to surpass LCDs in terms of market share during the next decades: the OLED displays (fig. 2.17).

The economical importance of the present and future FPD market is noteworthy: currently, FPD shipments represent more than 90000 millions U.S. dollars (MUSD) and 125000 MUSD are expected for 2015. [179] As mentioned before, LCDs are nowadays the dominant technology, with around 100 million units of LCD TVs shipped in 2008 and more than 200 million being expected to 2013. [180] PDPs, on the other hand, had only about 14 % of the total LCD TV shipments in 2008, or if only screen sizes larger than 40” are considered, about half of LCD TVs. [178, 181]

Regarding OLEDs, for now they only represent a small percentage of the total FPDs shipments and revenues: for instance, in 2008, OLEDs represented revenues of 500 MUSD, but 6200 MUSD are expected by 2016. [182] While in 2008 several small screen size applications such as mobile phones integrating OLED technology started to be commercialized, by 2010 this market will start to expand, including larger screen sizes for notebook and TV applications, such as the 15-30” ones already announced by LG, Sony and Samsung.
Potentiated by the appearance of OLEDs and other technologies such as electrophoretic displays, [183] which can both be fabricated at very low temperatures, a new display market starts now to assume particular relevance: the flexible displays, which are predicted to expand by a factor of 35 from 2007 to 2013. It is foreseen that by that time revenues of 2800 MUSD will be achieved, [184] increasing to 12000 MUSD by 2017. [185]

Another important market area is expected to be created during the next years, by using technologies such as OLEDs integrated with the new oxide semiconductor-based TFTs: the transparent (and flexible) displays.

2.4.2. Liquid crystal displays (LCDs) and organic light emitting devices (OLEDs) technologies

TFTs are key components of two of the most important display technologies, LCDs and OLEDs. To understand the different electrical performance requirements of the TFTs for these two frontplane technologies, they are briefly discussed in this section.

LCDs are an example of a non-emissive display, because liquid crystals do not emit light, but rather work as independent light switches in each pixel. Liquid crystals were discovered more than a century ago, but their useful electro-optic effects and stability were only developed during the 1960-70s. [108] These materials possess physical properties intermediate to those of crystalline solids and isotropic liquids. Regarding their usage in displays they can be seen as light modulators, since their function is to allow or block light transmission. This is achieved by the reorientation of the liquid crystal director by an applied external voltage. [108] For instance, considering the simple case of a twisted nematic liquid crystal inserted between two 90° crossed polarizers, in the unbiased state the liquid crystal reorients light coming from a backlight (located behind the first polarizer), allowing its transmission through the second polarizer; on the other hand, liquid crystal molecules tend to align themselves with the direction of an applied electric field, i.e., the molecules become untwisted. Under this situation, the liquid crystal can no longer reorient the light, making it to be absorbed at the second polarizer. Hence, transparent and opaque states are created, with intermediate states being achieved by using intermediate external voltages. The same principle can be used to obtain color, by using suitable color filters (red, green and blue) at each subpixel. Since liquid crystals are a birefringent medium, its electro-optic effects are dependent on the incident light direction, implying that the viewing angle is a critical issue of LCD technology. However, viewing angles can be improved by using optical phase compensation films. [108]
The most common LCDs used in applications such as TVs or notebooks are called transmissive, because light is provided by a backlight. However, transmissive LCDs present poor performance under intense sunlight. Reflective LCDs, on the contrary, use ambient light as the light source, providing reasonable outdoor performance but are not usable in a dim environment. Transflective LCDs combine both transmissive and reflective features, switching off the backlight in bright ambients. [108] The backlight in LCDs, responsible for most of the power consumption of the display, [170] generally employs cold cathode fluorescent lights (CCFLs), but recently LEDs started to replace CCFLs as backlights due to aspects such as lower power consumption, longer lifetime, smaller size and ruggedness. [108]

Regarding the driving technique, two techniques can be distinguished: passive and active matrices (PM and AM, respectively). PMs consist of simple x-y electrodes in a stripe configuration, with the ones on top of the liquid crystal aligned perpendicularly to the ones on the bottom and each crossed section constituting a pixel. This is a simple addressing scheme and it was used on the first LCDs. However, PMs have severe limitations on the maximum display size and resolution achievable and suffer from large crosstalk (i.e., the electrical signal applied to a line undesirably affects neighboring lines, which is particularly critical in displays with large pixel densities and LCDs in particular due to the capacitor characteristics of the liquid crystal layer). [63, 108] AMs solve these problems, by employing an array of TFTs in a backplane (i.e., below the liquid crystal), with each pixel being controlled independently by a TFT,\(^h\) while an unpatterned transparent electrode is placed on the top of the liquid crystal. AMs are nowadays used in all the high resolution LCDs, both with small and large areas. Figure 2.18 shows a schematic of the structure (fig. 2.18a) and of the electronic circuit (fig. 2.18b) of an AM LCD pixel. Even if simplified, fig. 2.18a already shows that the structure of the pixel can be rather complex, involving a large number of components. The presence of the storage capacitor improves the retention characteristics, allowing to bias the liquid crystal pixel even if the corresponding scan line is not selected (note that only one scan line is selected at a time). [108]

In AM LCDs, the TFTs act as switches, being their main requirements large On-Off ratios and close to 0 \(V_T\), in order to allow for high image contrast, to simplify circuit design and minimize power dissipation. All the TFT technologies discussed in section 2.3.3 can fulfill these requirements, at least for current displays with small-to-moderate sizes and resolutions. However, for future LCDs, which will have even larger sizes, resolutions and frame rates, \(\mu_E\) starts to be an important parameter to consider and can hinder the usage of a-Si:H or organic semiconductor TFTs. In fact, in the case of an ultra definition (UD, or 4K x 2K pixels) AM LCD, a-Si:H TFTs enable operation of a 82” display at only

\(^h\) Actually, in a color LCD, each pixel has 3 subpixels, each one with a TFT, in order to obtain red, green and blue colors and their combinations.
60Hz. To achieve higher frequencies (120 Hz or above) $\mu_{FE} > 3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ is required, because of the need to charge the storage capacitor with shorter pulse time. [186]

Contrarily to LCDs, OLED displays are emissive, because OLEDs emit light. This process is achieved by the recombination of holes and electrons, injected from an anode and a cathode, with the $E_g$ of the organic semiconductors determining the emission wavelength. [108] Electroluminescence in organic materials was initially observed in 1950s by Bernanose and co-workers, but the first OLED was only invented in the late 1980s by Tang and Vanslyke, in Kodak. [187, 188]

Since OLED displays are emissive they do not need any backlight, allowing these displays to exhibit much higher contrast ratios than LCDs, because in the Off-state the pixel is completely dark. Besides this, the structure of the display also results considerably simpler (fig. 2.19a), which will contribute to reduce the production costs by the time this technology is widely implemented. In brief, the main advantages of OLED displays comparatively to LCDs are higher contrast ratios, lower response times, wider viewing angle, lower display thickness and lower power consumption. [189] Also, the low temperature processing techniques of OLED composing materials turn them suitable for future flexible displays, as mentioned before.

![Figure 2.18 – Schematics of the (a) structure and (b) electronic circuit of a pixel in an AM LCD.](image)

![Figure 2.19 – Schematics of the (a) structure and (b) electronic circuit of a pixel in an AM OLED.](image)
As with LCDs, PMs and AMs can be used as driving techniques in OLED displays. PMs suffer from the same typical problems as in LCDs, such as crosstalk and limitations on screen size and resolution. Given this, AMs are also preferred for OLEDs over PMs and the market forecasts reflect this, with AM OLED revenues expected to surpass PM OLED ones already in 2009-2010. [179] However, the electronic circuit of an AM OLED pixel is more complicated than an AM LCD (fig. 2.19b). Here, at least two TFTs need to be used, one as a switching element (address TFT), other as a current driver to switch on the OLED (drive TFT). For the drive TFT a high current density is required. Although some a-Si:H TFT architectures can provide this, very large W/L and high supply voltages would have to be used, which would translate in low aperture ratios and high power consumption. [170, 189] A considerably better solution, followed in most of the current AM OLEDs, is to use poly-Si TFTs: since $\mu_{FE}$ is much higher than in a-Si:H TFTs, the required current densities can be achieved using smaller devices and lower operating voltages. However, the uniformity problems in large areas can be a problem for the success of poly-Si TFTs in future OLED displays. These problems, as well as stability related ones, can be attenuated by using pixel structures with more than two TFTs (compensation circuits), but this increases production costs and decreases the aperture ratio. Due to all this, oxide semiconductor-based TFTs seem to be potential candidates for future AM OLED displays: besides having considerably larger $\mu_{FE}$ than a-Si:H TFTs, oxide TFTs can be made larger without compromising the aperture ratio. Furthermore, the fact that they can be produced at very low temperatures fits, together with the OLED frontplane, the needs for flexible electronics. During this year, Görn et al. already reported a simple 2 TFTs + 1 capacitor pixel circuit using oxide TFTs, with suitable performance for an OLED display with full-HD resolution (full high-definition, 1080 rows), 100 Hz frame rate and brightness levels of 2000 cd m$^{-2}$. [190]

2.5. References


2. Transparent oxide (semi)conductors, dielectrics, thin-film transistors and displays background


[27] "http://www.navbharat.co.in/ Clients.htm."


Transparent oxide TFTs: production, characterization and integration


2. Transparent oxide (semi)conductors, dielectrics, thin-film transistors and displays background


[121] O. Heil, "Improvements in or relating to electrical amplifiers or other control arrangements," U.K., 1935.

[122] "http://chem.ch.huji.ac.il/history/lilienfeld.htm."


Transparent oxide TFTs: production, characterization and integration


2. Transparent oxide (semi)conductors, dielectrics, thin-film transistors and displays background


Chapter 3

Thin films and devices: deposition and characterization techniques

The research work summarized in this dissertation involved the production and characterization of thin films and devices. This chapter summarizes relevant techniques used for that end. Regarding thin film deposition techniques, the main focus is given to sputtering, since it was preponderant to produce all the oxide semiconductors and high-κ dielectrics presented throughout the dissertation. Conventional patterning techniques are also briefly discussed, as they were required for the production of TFTs and active matrix backplanes. Characterization techniques aiming the analysis of a broad range of materials and devices' properties are also covered in this chapter, with special relevance being given to electrical characterization.

3.1. Thin film deposition techniques

A variety of deposition techniques is employed to fabricate the thin films investigated throughout this research work. Sputtering is used as the central technique, being used to deposit the oxide semiconductor and dielectric thin films. Additional techniques, both vacuum and non-vacuum based, such as electron-beam evaporation and spin coating, are used to deposit electrodes and passivation layers, being also briefly described herein.

3.1.1. Sputtering

Sputtering is one of the most well known physical vapor deposition (PVD) techniques. Commonly to other PVD techniques (such as evaporation or PLD), atoms or molecules are physically removed from a source material and transported through vacuum to a substrate, where they form a thin film. In its essence, sputtering consists on ejecting atoms from the surface of a source material as a result of collisions and momentum transfer from incoming highly energetic ions that are created due to ionization of gaseous species. The process is maintained and the sputtered species are directed to a substrate by an electric field. [1, 2] The sputtering phenomenon was first described more than 150 years ago, in the 1850s’, with the works of Grove, Faraday and Plücker. [3] The technique started to be occasionally used in the late 1800s for the deposition of thin films aiming the production of mirrors. [3] Nowadays it is a well established and versatile deposition technique for a wide range of
applications, from simple metallic coatings to the production of all the layers in electronic devices, such as the TFTs produced in this work. Relatively to other thin film deposition techniques, sputtering provides several advantages, such as low substrate temperatures, good adhesive strength, good control of film thickness and composition, highly dense films, possibility to deposit a broad range of materials (either by using different target compositions, a reactive gas or simultaneous sputtering from two or more target sources (co-sputtering)) and good scalability to large areas. [4-6]

The sputtering process is initiated in a vacuum chamber containing two electrodes, cathode and anode, being the source material or target placed on top of the cathode and the substrate on the anode, which is generally grounded. An inert gas is introduced in the chamber, typically argon due to its low cost and high cross section, and an electric field is created between the two electrodes. Under these conditions, electrons are accelerated towards the anode, colliding with gas atoms, giving rise to different reactions depending on the energy transferred in the collision process: [1, 7]

- Electronic excitation, in the form $e^- + Ar \rightarrow Ar^- + e^-$
- Ionization, in the form $e^- + Ar \rightarrow Ar^+ + 2e^-$

After electronic excitation, when electrons fall to their initial shells, the energy can be released in the form of photons, creating the so-called glow discharge. On the other hand, ionization creates additional electrons, which can participate in further excitation and ionization reactions, and positive gas ions that are directed by the electric field to the cathode, sputtering the target. Different phenomena occur at the target when the ions impinge its surface (fig. 3.1). As will be shown in section 3.4.2, some of these phenomena can be explored for powerful characterization techniques. For the sputtering deposition process the most important interactions are: [7]

- Release of atoms or molecular species from the target that are then deposited into the substrate. The incident ions have to possess a kinetic energy larger than a threshold value, typically 10 eV, in order to have a sputter yield (i.e., the number of atoms liberated from the target by each incident ion) higher than unity. The sputter yield depends on the incident particle characteristics (energy, masses and incident angle) as well as on the target material (crystalline structure, binding energy and masses of the constituent atoms). [1, 8] In their way to the substrate, dissociation of the sputtered species can also occur;

- Release of secondary electrons from the target, which sustain the glow discharge by promoting further ionization and excitation reactions. However, these emitted electrons can also reach the substrate and cause resputtering of the growing film.
3. Thin films and devices: deposition and characterization techniques

Figure 3.1 – Some of the main effects arising from the interaction between incident ions and the target surface (adapted from [9]).

The most important processes of the glow discharge occur close to the target surface, in a region designated by Crookes’ dark space, after the initial experimental research of the British chemist and physicist Sir William Crookes on what is known nowadays by plasma. [3, 10] This region mostly consists of a positive space charge because the mass of electrons is much smaller than that of the positive ions, hence electrons are quickly accelerated away from the cathode. This gives rise to a strong electric field in front of the target that provides the ion acceleration required for sputtering.

Thin films can also be deposited by using a reactive gas inside the system, in addition or in substitution of the inert gas. This process is known as reactive sputtering and is widely used to produce different materials, such as oxides or nitrides by using oxygen or nitrogen, respectively. [1] For instance, thin films of TCOs and TSOs based on indium, tin or zinc oxides are often produced by sputtering metallic targets (which are much cheaper than ceramic ones) in an oxidizing atmosphere. [4, 5] Even if starting with ceramic targets already with the desired thin film composition, reactive sputtering is useful to control film’s stoichiometry, as will be seen in this work. Still, high concentrations of reactive gases can also induce resputtering effects on the substrate due to the incidence of negative ions, which is particularly relevant for oxygen, given its high electronegativity. [2, 11]

Two types of electrical excitation can be used in sputtering: direct current (d.c.) or radiofrequency (r.f.). D.c. sputtering systems are the simpler ones, using a d.c. voltage between the cathode and anode. However, these systems are restricted to the usage of conductive targets (mostly metals), because insulating materials are not able to supply the target surface with sufficient secondary electrons to maintain the glow discharge. [1, 5] On the contrary, on r.f. sputtering systems both conducting and insulating target materials can be used. In this case, a high frequency (typically 13.56 MHz) voltage is supplied to the target. This way, even if the target does not supply enough secondary
electrons during the negative portion of the r.f. signal (when the positive ions are attracted to it), electrons from the glow discharge are attracted towards the target during the positive portion of the r.f. signal. Since the target area is much smaller than the grounded anode (constituted both by the substrate area as well as the chamber walls) and given the lower mass of electrons relatively to ions, a self-biased d.c. voltage emerges in the target, creating the conditions for sputtering to occur. [1]

The system configurations mentioned until now are known as diode-configurations. Even if they are able to provide thin films with sufficiently good properties for a large number of applications, there are two major problems with diode-sputtering systems: the deposition rate is slow and the electron bombardment of the substrate is extensive and can cause overheating and structural damage. One way to overcome these limitations is to use magnetron sputtering (fig. 3.2). Magnetron sputtering was first proposed by Penning in 1936 and the first practical magnetron system was developed by Chapin four decades latter. [1, 3] In these systems, a magnetic field is created above the target surface by having strong magnets behind the target. This way, electron movement is confined to the region right above the target surface, within an extensive and circular (or rectangular, depending on the target and magnets arrangement) path. This simultaneously reduces the substrate bombardment by electrons and increases the probability of ionization of neutral gaseous molecules, which results in higher sputtering and growth rates. [1] Since in magnetron sputtering systems the availability of ions for a given pressure is higher than in diode systems, lower deposition pressures can also be used. A disadvantage of magnetron sputtering systems is the poor target utilization, since material is preferentially sputtered from the path defined by the magnetic field.

![Diagram of magnetron sputtering process](image)

*Figure 3.2 – Phenomena occurring during a magnetron sputtering process (adapted from [12]).*

In this work, three r.f. magnetron sputtering systems existent in CEMOP and capable of processing up to 10×10 cm substrates were used. The first two, devoted to oxide semiconductor thin film fabrication, are depicted in fig. 3.3. The Pfeiffer system (fig. 3.3a) is used for all the studies on thin films and for most of the channel layers of TFTs produced on Si/SiO₂ substrates, while the home-
made system (fig. 3.3b) is used for the fabrication of the channel layers and electrodes of TFTs and active matrix backplanes employing sputtered dielectrics. Although not explored in this work, both systems have the capability of co-sputtering and substrate heating. Sputtering is always carried out at room temperature, with a base pressure of 0.4–0.6 mPa and target-to-substrate distance of 15 cm. The effect of composition inside the gallium-indium-zinc oxide system is widely explored by using different ceramic targets\(^a\), both binary and multicomponent (ternary or quaternary) compounds, which are presented in table 3.1 according to their In/(In+Ga) and In/(In+Zn) atomic ratios:

Table 3.1 – Ceramic target compositions of the gallium-indium-zinc oxide system studied in this work.

<table>
<thead>
<tr>
<th>In/(In+Zn) atomic ratio</th>
<th>In/(In+Ga) atomic ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.50</td>
</tr>
<tr>
<td>ZnO, Ga(_2)O(_3)</td>
<td>--</td>
</tr>
<tr>
<td>0.50</td>
<td>GIZO 2:2:2</td>
</tr>
<tr>
<td>0.67</td>
<td>GIZO 2:2:1</td>
</tr>
<tr>
<td>0.80</td>
<td>GIZO 2:4:1</td>
</tr>
<tr>
<td>1</td>
<td>IGO 4:2</td>
</tr>
<tr>
<td></td>
<td>In(_2)O(_3)</td>
</tr>
</tbody>
</table>

For different compositions, processing parameters of the sputtering technique are varied as follows:

- percentage of oxygen content in the Ar+O\(_2\) mixture (\(\%O_2 = 100 \times p_{O_2}/p_{Ar+O_2}\)), between 0 and 10.0 %;
- deposition pressure (\(p_{dep}\)), between 0.4 and 1.0 Pa;
- rf power density (\(P_{rf}\)), between 1.1 and 2.7 W cm\(^{-2}\).

The thin films are produced either on silicon wafers or on Corning 1737 glass substrates, depending on the characterization technique or devices they are aimed for (see figs. 4.1, 5.2 and 5.36),\(^b\) with thicknesses ranging between 5 and 250 nm. A pre-sputtering procedure (i.e., sputtering with the

\(a\) The targets used in this work are mostly from LTS Chemical Inc., except ZnO (from Super Conductor Materials) and GIZO 2:8:2 (from JSI, Slovenia).

\(b\) Note that the process parameters given in this chapter constitute a generic overview of the work developed in terms of both isolated thin films and their application to devices. For easier reference, specific details regarding either thin films or devices processing and post-processing conditions are given at the beginning of chapters 4 to 6.
shutter closed, preventing deposition on the substrate) of 15 or more minutes is performed before all the depositions to assure reproducible properties on the thin films.

A different sputtering system is used to process the dielectric thin films, both isolated and integrated in TFTs and active matrix backplanes. The system is an AJA ATC-1300F (fig. 3.4a) that can be almost entirely computer-controlled. As with the Pfeiffer and home-made systems, this also provides the possibility of heating the substrate (up to 850 °C), although all the deposition are performed without intentional substrate heating. Another important feature is the possibility of biasing the substrate with a r.f. signal, although this is not explored in this research work. The AJA system is equipped with a load-lock chamber for sample loading/removal, so very low base pressures are achieved in the main chamber (about 0.05 mPa or below). Target-to-substrate distance is fixed at 10 cm and during the deposition the substrate is kept rotating to allow for enhanced uniformity on the resulting thin film. As will be show in chapter 6, uniformity can also be adjusted by changing the configuration of the magnetrons (which are con-focally oriented relatively to the substrate), namely their tilting angle. The system has three magnetrons (fig. 3.4b) allowing for co-sputtering and subsequent production of multicomponent materials. In fact, most of the work regarding dielectrics is devoted to the production of multicomponent oxides, using mixtures of high and low-κ materials, either by co-sputtering or by starting with a ceramic target with a pre-defined mixed composition. For the co-sputtering process, $P_r f$ applied to each target is used to control the incorporation of each element in the deposited thin film. The studied dielectric materials are SiO$_2$, Al$_2$O$_3$, HfO$_2$, Ta$_2$O$_5$ and mixtures of Ta$_2$O$_5$ with SiO$_2$ or Al$_2$O$_3$. The thin films are deposited on silicon wafers (and on Corning 1737 glasses when integrated in TFTs) with thickness around 300 nm, with Ar/O$_2$ flow ratio of 14/1 sccm and $P_{dep}$=0.3 Pa.$^d$

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5 The application of bias to the substrate can increase the purity of the deposited thin film by resputtering poorly bonded surface atoms, but can also lead to damaged structures, depending on the materials and bias magnitude. [5, 13]

6 See note b.
3.1.2. Electron-beam evaporation

Physical evaporation is one of the oldest and most widely used methods to deposit thin films of metals. This deposition technique consists essentially on heating a material up to its point of vaporization, allowing the evaporated molecules to be deposited in a substrate placed close to the source material. [6] In order to increase the mean free path of vaporized molecules and to reduce the contamination of the deposited thin films, the heating process is performed under high vacuum. In classical thermal evaporation, the material intended to be evaporated is placed on top of a filament of a refractory metal, such as tungsten or tantalum. The vaporization of the material is achieved by increasing the current that passes through the metal filament. For materials requiring high temperatures to be evaporated, such as oxides, this process can lead to significant cross-contamination from the filament material in the deposited thin film, or in extreme cases, to the physical damage of the filament due to overheating. Electron-beam evaporation provides a good solution for these issues, by using as a heating source a highly energetic electron beam rather than the refractory filament. The source material is placed in a water-cooled crucible and the electron beam generated by thermionic emission from an incandescent filament (located below the crucible to prevent contamination) is deflected towards the surface of the source material by a magnetic field. This way, only the specific region of the material being evaporated is heated, allowing to deposit materials with higher melting points. The deposition rate can be easily controlled by changing the current of the electron beam. Some systems also provide the option of introducing in the chamber a reactive gas such as oxygen during the evaporation process, allowing to obtain oxide thin films from metal sources. [5] One of the drawbacks of electron-beam evaporation is that for very high beam acceleration voltages (above 5-10 keV) substrates may suffer some radiation damage from energetic electrons and X-rays. [2, 6]

Electron-beam evaporation is used in this research work to deposit metal electrodes (Al and Ti/Au) on oxide semiconductor and dielectric samples for electrical characterization, as well as on some of the TFT structures. Additionally, it is also employed for the deposition of SiO₂ and MgF₂ passivation layers on the TFTs. This is accomplished using a home-made system existent in CEMOP (fig. 3.5). For all the depositions, base pressure is around 7×10⁻⁴ Pa, electron-beam acceleration voltage is about 5-6 kV and current is adjusted for each material to achieve deposition rates around 2-3 Å s⁻¹.
3.1.3. Spin-coating

Spin-coating has been used for several decades to produce thin films. Unlike sputtering or electron-beam evaporation, spin-coating is a non-vacuum process and makes use of a very simple apparatus, which is reflected in fast processing times and low equipment costs. The process is typically initiated by dropping an excess amount of a liquid precursor on top of a substrate. The substrate is held in vacuum to a chuck, which is then rotated at high speed (typically above 1000 rpm) in order to spread the liquid precursor over the entire substrate, forming a thin film whose thickness is determined by the properties of the liquid precursor itself (viscosity, drying rate, surface tension...) and also by deposition parameters such as rotation speed and acceleration. [2, 14, 15] After this process, the thin film still includes not only the desired chemical constituents but also some portion of the solvents included in the initial liquid precursor. These solvents are removed by a dehydration process, normally consisting of heating the substrate in a hot-plate or oven. Higher film thickness or multilayer structures with different materials can be obtained by repeating the processes described above. Despite consisting of a fast and low cost process, spin-coating has the disadvantage of generally requiring high annealing temperatures to attain thin films with reasonable electronic properties, and even when optimized, these properties are typically far from the ones attained using vacuum deposition techniques.

Spin-coating is extensively used in this work to deposit positive photoresist layers for photolithographic processes (see section 3.2.1) and also to deposit the SU-8 epoxy based negative resist [16] used as a passivation layer in TFTs. Positive photoresist is deposited with a Headway Research PWM32 system existent in CEMOP, using a rotation speed of 3000 rpm during 10 s and then 4000 rpm during 20 s. To prevent contamination, SU-8 is deposited in a different spinner, a KarlSuss CT62, using a rotation speed of 1340 rpm during 40 s. Typical film thicknesses are 1-3 and 20 µm, for positive photoresist and SU-8, respectively.
3.1.4. Supplementary techniques: thermal oxidation and plasma enhanced chemical vapor deposition (PECVD)

A large amount of this research work relies on silicon substrates coated with SiO₂, either to be used as thermally stable substrates for the analysis of oxide semiconductors annealed at different temperatures or as reliable and reproducible substrate/gate electrode/dielectric structures of TFTs. In these commercially available structures the SiO₂ layer is deposited either by thermal oxidation or by plasma enhanced chemical vapor deposition (PECVD).

Thermal oxidation is not exactly a deposition technique, since the SiO₂ layer is grown by the reaction of oxygen with silicon atoms already existent in a single crystalline silicon wafer. [6] This process is generally accomplished in a tubular furnace at temperatures between 900 and 1200 °C, with an atmosphere containing either water vapor or pure oxygen. The different atmospheres result in the so-called “wet” or “dry” oxides, respectively, being the latter characterized by a lower growth rate but by improved quality, namely in terms of the oxide density, which is reflected in higher breakdown fields. [6, 17, 18] The high temperature of the process allows oxygen to diffuse through the silicon wafer surface and the previously grown oxide, in order to continue the oxidation reaction.

Although the excellent quality of thermal oxide is not obtained with lower temperature processes, PECVD still yields very good quality SiO₂ layers. In a typical CVD process, thin films are deposited on a substrate by thermal decomposition and/or reaction of precursor gaseous compounds. [6] The dissociation of the precursor gases and subsequent deposition on the substrate can be made at lower temperatures if additional energy for these reactions is supplied by a plasma generated with a r.f. signal, which is the fundamental principle behind the PECVD technique. Effects such as $P_{r.f.}$, $P_{dep}$, gas flows, distance between the r.f. electrode and the substrate, temperature and reactor geometry, all affect the properties of the obtained thin film. [19] The most widely used precursors for SiO₂ deposition by PECVD are silane+nitrous oxide (SiH₄+N₂O) and tetraethylorthosilicate (TEOS, Si(OC₂H₅)₄. [20, 21]

3.2. Patternning techniques

A device is generally comprised of structures with several stacked layers of different materials, with each layer having a specific pattern. To fabricate simple structures, such as the small circular electrodes for current-voltage or capacitance-voltage measurements, shadow masks are used between the material source and the substrate during the deposition. However, for the fabrication of
TFTs and backplanes different patterning processes are required, in order to have feature sizes in the range of 2-50 μm and small alignment tolerances for the several layers that constitute these devices. The techniques to achieve this are briefly summarized in the following paragraphs.

3.2.1. Photolithography

In its essence, the term lithography derives from the Greek words “lithos” (stone) and “grapho” (to write). It is one of the important landmarks of the history of printing, invented in 1796 by Alois Senefelder as a low-cost method of reproducing artwork. Photolithography emerges as an adaptation of the lithographic processes to microelectronics fabrication, comprising all the steps involved in transferring a pattern from a mask to the surface of a substrate. [6] The overall process relies essentially on the light sensitivity of a material called photoresist. Since the maximum spectral sensitivity of the photoresist used in this process is in the near ultraviolet (UV) and blue part of the visible spectrum (between 320 and 460 nm) a yellow light ambient is used, in order to block photons with wavelengths smaller than 500 nm (fig. 3.6). [22]

![Figure 3.6 – Equipments used for photolithographic processes, in a yellow room: (a) spinner; (b) mask aligner.](image)

A typical photolithography process flow is represented in fig. 3.7a. After substrate cleaning with acetone, isopropilic alcohol (IPA) and ultra-pure water, the photoresist is spin-coated on top of the previously deposited thin film (fig. 3.6a). According to the principles of the spin-coating process described in section 3.1.3, the thickness of the photoresist depends on its viscosity and is inversely proportional to the square root of the spinning speed. [6, 22] Most of this research work is performed using an AZ6612 photoresist, but a more viscous one, AZ6632, is used to provide extra protection to the dielectric layer of the active matrix backplanes during the etching step (see section 6.2). The spin-coating process generally comprises two stages, one at a lower speed to spread the photoresist through all the substrate surface area, and another at a higher speed to adjust the final
thickness. For AZ6612 and AZ6632, the typical thicknesses obtained with this process are 1.2 and 3.2 µm, respectively. After spin-coating, the coated substrates are placed in a hot-plate at 100-115 °C during 1m15s in order to improve photoresist adhesion to the substrate and to reduce its solvent content, a process designated by softbake. For the AZ resists used herein, the solvent is propylene-glycol-mono-methyl-ether-acetate (PGMEA) and if not properly removed during the softbake step it can lead to undesirable phenomena such as increased dark erosion, reduced thermal stability in subsequent process steps or lack of definition of the resist structures. [22]

The substrate is now ready to the mask alignment and UV exposure processes, which are made in a mask-aligner, in this work a Karl-Suss MA6 (fig. 3.6b). If the substrate already contains previously defined patterns, these are aligned with the ones included in the lithographic mask, by moving and rotating the substrate in a x-y stage. This is generally accomplished by including alignment marks such as squares, boxes or lines in all the masks. When a good alignment is obtained, the photoresist below the transparent areas of the mask is exposed to UV light coming from a mercury light source, which has an emission spectrum matching the photoresist absorption spectrum. The exposure step can be made in proximity or contact modes. Although the former has the advantage of resulting in less mask damage, the latter is mostly used since it allows for better resolution. When the photoresist is exposed to UV-light, its photo active compound, DiazoNaphtoQuinone- (DNQ-) sulfonate, looses a nitrogen molecule, being converted into indene carboxylic acid by incorporating a water molecule. The photoresist regions where this photoreaction happens have a much higher alkaline solubility than the unexposed regions, thus when the substrates are introduced in a suitable developer the desired patterns can be obtained in the photoresist. [22] Depending on the photoresist, several developers can be used. For the AZ6612 and 6632 resists used throughout this work, a metal ion free developer, AZ 726 MIF, primarily composed by tetrametil ammonium hydroxide is selected.

After this sequence of steps, the photoresist is only protecting the areas of the substrate that are intended to remain in the final pattern, hence an etching process can be used to remove the unprotected material. Before the etching step, if further thermal, chemical and physical stability of the photoresist is required, an extra hardbake step is performed in a hot-plate. [6, 22] After etching, a last process designated by resist stripping is required, simply consisting of dipping the substrate in a liquid that dissolves the photoresist or causes it to swell and lose adhesion to the substrate. In this work, this is accomplished using acetone and a subsequent cleaning in IPA to avoid striations on the substrate.

Two important variations can be made to the typical process described above:
Instead of using positive photoresists, such as the AZ6612 or AZ6632 used in this work, negative photoresists can also be used. In this case, the UV exposed areas of the photoresist remain on the surface, i.e., only the non-exposed areas are removed during the development step. Hence, to obtain the same final pattern, masks with opposite polarity (negative) have to be used.

By using a positive resist and a negative mask, a photoresist structure with the negative of the desired final pattern can be defined prior depositing the thin film. After thin film deposition, the substrate goes directly to the resist stripping step, removing both the photoresist and the thin film deposited on top of it. This way, the final pattern of fig. 3.7a can be obtained without the need of an etching process. This process is depicted in fig. 3.7b and is known as lift-off, being preferentially used in this work to pattern the composing layers of the TFTs and active matrix backplanes. Lift-off has the great advantage of allowing to selectively pattern a low-temperature deposited material without affecting others beneath it, but it generally results in poorer definition and/or increased contamination. These issues will be further addressed in section 6.2.

![Process flows showing the main steps of photolithographic processes: (a) conventional; (b) lift-off.](image)
3. Thin films and devices: deposition and characterization techniques

3.2.2. Wet-etching and dry-etching

Even if lift-off is the selected patterning method to fabricate the TFTs and active matrix backplanes in this work, etching is also used in some specific cases. One of the natural requisites of etching is that the etchant is selective regarding photoresist and other materials previously deposited on the substrate. Two main etching techniques can be distinguished, wet and dry-etching.

Wet-etching is accomplished by dipping the substrate in an adequate solution that breaks intermolecular and/or atomic bonds of the solid to be etched, dissolving it. In this work, this process is used to define the semiconductor pattern in samples for Hall effect and four-point-probe measurements, as well as for native SiO₂ etching on silicon wafers used to deposit dielectric thin films. The oxide semiconductors are etched using a highly diluted hydrochloric acid solution (HCl:HO, 1:100), while native SiO₂ is etched with an ammonia fluoride-buffered hydrofluoric acid (NH₄F:HF:H₂O). Wet-etching tends to be an isotropic process, removing material in all directions. Hence, undesirable under-etching below the photoresist with a magnitude similar to the thickness of the etched film can be observed, which is a critical issue when linewidths with dimensions similar to the film’s thickness are required. [6]

Dry-etching methods and reactive ion etching (RIE) in particular rely on a mixture of chemical and physical processes to etch a material. The chemical component results from the reaction of the ions of a gas with the material to etch. This confers a good selectivity to the process but creates an isotropic profile in the etched structured, like in wet-etching. On the other hand, the physical component of the RIE process relies on the momentum transfer from the etching species to the atoms on the surface of the material to etch, similarly to what happens during the sputtering process described in section 3.1.1. Even if this confers a lower selectivity to the etching process, highly anisotropic profiles can be obtained. [6] Whether the chemical or physical component is dominant during the dry-etching process depends on the material to etch, on the reactive gas and on the etching conditions, such as pressure or applied power. RIE is used in this work to etch dielectric thin films based on tantalum-silicon and hafnium-silicon oxides in the active matrix backplanes, using sulfur hexafluoride (SF₆) or tetrafluoromethane (CF₄) as reactive gases. The process is performed using an Alcatel GIR 300 system existent in CEMOP. Typical process parameters are base pressure of 0.05 Pa, gas flow of 10 sccm, etching pressure of 0.85 Pa and r.f. power of 20-50 W.
3.3. Post-deposition annealing

The properties of thin films can be severely modified by different post-deposition processes, such as plasma or thermal treatments. For TCO and TSO thin films the effect of post-deposition treatments is expected to be large, since depending on their deposition conditions these methods affect for instance the concentration of oxygen vacancies in the structures, which is known to largely control the electrical properties exhibited by these materials. An extreme example of this is the first TCO reported by Badeker, which resulted from the thermal oxidation of a previously deposited metallic cadmium thin film. [23] Increased temperatures may also play an important role on other properties of thin films and devices, for instance by promoting the crystallization of initially amorphous structures and/or by modifying interfaces due to annihilation of surface states or inter-diffusion of different elements. These effects are extensively studied throughout this dissertation. Thermal annealing in air atmosphere is selected as the post-deposition technique on this research work, essentially due to its simplicity and efficiency in largely modifying the properties of thin films and devices. Annealing is performed with temperatures ($T_a$) ranging from 150 to 500 °C, with heating ramps of 10 °C min$^{-1}$, maintaining the desired temperature during 1 h and removing the samples only after cooling down below 60 °C. The annealing treatments are preferentially performed using a Barnstead Thermolyne F21130 tubular furnace existent in Centro de Investigação de Materiais (CENIMAT), but for the production of the active matrix backplanes in 10×10 cm substrates a Torrey Pines ECHOTerm digital hot-plate with controllable heating ramp existent in CEMOP is used instead.

3.4. Thin film characterization techniques

The oxide semiconductor and dielectric thin films are characterized using a broad range of tools, aiming to study their structural, morphological, compositional, optical and electrical properties. From these, the structural, morphological and compositional analyses are performed by University of Barcelona, in the framework of the Multiflexioxides European project. Relevant details about all the characterization techniques used throughout the research work of this dissertation are given below.

3.4.1. Structural and morphological characterization

3.4.1.1. X-ray diffraction (XRD)

X-ray radiation was discovered in 1895 by the German physicist Wilhelm Röntgen, an achievement that earned him the first Nobel prize in Physics in 1901. [24, 25] Of particular relevance for the
structural characterization of materials is the phenomenon of X-ray diffraction (XRD), initially studied by Laue, Friedrich, Knipping and Bragg (father and son). [24, 25] XRD constitutes a powerful characterization technique, for instance to know if materials are amorphous or polycrystalline, which phases are present and if there are any preferential crystallographic orientations. [19] The principle can be briefly described as follows: when a monochromatic X-ray beam (which can be considered as an electromagnetic wave travelling through space) is directed to a material it will cause all electrons in its path to oscillate at the same frequency as the incident beam, causing constructive (in phase) and destructive (out of phase) interference of the waves emitted by the atoms. A diffracted beam results from the constructive interferences, requiring that both the waves emitted by all the atoms lying in a single plane and the scattering of waves by successive planes are in phase. For a given X-ray wavelength ($\lambda$) with a value close to the inter-planar spacing ($d$), this only occurs for certain angles relatively to the scattering planes ($\theta$), depending on the structure of the material. This can be described by the well-known Bragg’s law: [25]

$$n\lambda = 2d \cdot \sin \theta$$  \hspace{1cm} (3.1)

where $n$ is an integer. By varying $2\theta$ (the diffraction angle) and measuring the diffracted beam intensity, which depends on the number of atomic planes equally spaced participating in the diffraction phenomena, a diffractogram is obtained, exhibiting peaks with different intensities in the analyzed range of $2\theta$ if the material has crystalline domains. [25] The positions and relative intensities of these peaks can then be compared with a database where several crystalline materials and phases are listed, allowing to identify which are present in the analyzed sample.

XRD is used in this work to analyze oxide semiconductor and dielectric thin films produced on silicon substrates. The measurements are performed using a Siemens D-500 diffractometer existent in the University of Barcelona, using Cu Kα radiation ($\lambda=1.5418$ Å) and varying $2\theta$ between 20 and 80°.

### 3.4.1.2. Scanning electron microscopy (SEM)

When a highly energetic electron beam is directed to a given material a multitude of interactions can occur, such as absorption of electrons by the sample, reflection of primary (backscattered) electrons, emission of secondary electrons and emission of electromagnetic radiation. [26, 27] Scanning electron microscopy (SEM) relies on these interactions to provide high resolution images of the surface of a sample, being possible to analyze features in the nanometer scale. To obtain an image by SEM, an electron beam is generated typically by thermionic emission from a tungsten filament
cathode or in the more recent equipments by a field-emission gun. [26] The electron energy is generally between 1 and 30 keV and before reaching the sample the beam passes through pairs of scanning coils or deflector plates in the electron column that deflect the beam in the x and y axes, in order to scan a rectangular area of the sample surface. The electron beam/material interaction phenomena mentioned above are then analyzed by different detectors. The conventional SEM image is formed by the detection of the secondary electrons emitted by the sample, which was achieved for the first time by Max Knoll in the 1930s’. [28] In this mode, surface topography can be analyzed, because the number of secondary electrons emitted depends on the angle between the incident beam and the sample surface where it collides, hence a contrast is obtained between steep and flat regions of the sample. On the other hand, on images obtained due to backscattered electrons contrast is achieved due to the different atomic numbers of elements, i.e., heavy elements backscatter electrons more strongly than light elements, thus the former appear brighter in the image. Hence, this imaging mode provides useful information about chemical composition of the sample.

In this work, SEM analyzes are performed in oxide semiconductor thin films using either a FEI Quanta 3D FEG or a FEI Helios Nanolab system, both existent in FEI Nanoport, Eindhoven. Cross-sections of TFT structures are also analyzed by using a Zeiss Auriga system, existent in Zeiss, Oberkochen.

3.4.1.3. Transmission electron microscopy (TEM)

The first transmission electron microscopy (TEM) system was built by Max Knoll and Ernst Ruska in 1931. As in SEM, TEM also relies on the interaction of a highly energetic electron beam with a sample. However, the range of accelerating voltages is much higher in TEM, typically between 100 and 400 kV, and the analyzed samples have to be very thin in order to be transparent to electrons. [26, 27] The transmitted and forward scattered electrons form a magnified image with very high resolution, allowing to analyze features at the atomic scale. Additionally, they can also form a diffraction pattern that provides valuable information regarding the structure of the material. Contrast formation is highly dependent on the imaging mode (for instance, bright-field and dark-field modes), but generically is related with mass, thickness, diffraction and phase contrast. [26] In the most widely used imaging mode, bright-field, contrast is essentially formed due to the increased electron scattering as the beam passes by atoms with higher atomic numbers or by thicker regions of the sample. These appear as dark regions in the image, because a less intense beam arrives at the transmitted electron detector. By adjusting the magnetic lenses, image can be acquired by the back focal plane of the lens, resulting in a diffraction pattern. This allows to clearly distinguish between
amorphous and crystalline samples and for the latter, information regarding the space group symmetries and the crystal's orientation to the beam path can be obtained. [26, 27] The largest drawback of this technique is the time consuming sample preparation that can last several hours using the traditional mechanical polishing and ion milling methods. Still, recent techniques such as focused ion beam (FIB) allow to considerably decrease the sample preparation time, although the FIB’s gallium beam can also contaminate the thin film to be analyzed by TEM. [26]

A JEOL J2010F TEM system existent in the University of Barcelona is used in this work to analyze oxide semiconductor and dielectric thin films. The samples are thinned using mechanical polishing and ion milling with argon ions, being placed afterwards on a copper mesh grid for the TEM analysis.

3.4.1.4. Atomic force microscopy (AFM)

Atomic force microscopy (AFM) is a relatively new characterization technique created in 1986 by Binning, Quate and Gerber, which can be seen as a combination of the principles of the scanning tunneling microscopy (STM)* and the stylus profilometry. [30] AFM provides very high resolution three dimensional surface profiles, where atomic scale features can be detected. In addition, it does not require any sample preparation and the measurements can be performed in air ambient, contrarily to SEM or TEM. Given the low sample requirements and large imaging possibilities, AFM is used in several research fields, such as materials science, chemistry, biology and physics. Contact mode AFM is one of the most widely used scanning probe modes, and operates by scanning a sharp tip across the sample, under the action of a piezoelectric actuator. The tip is generally made of silicon or silicon nitride (Si₃N₄) and is attached to a low spring constant cantilever. An extremely low force (around 10⁻⁹ N, similar to interatomic force range) is maintained on the cantilever, thereby pushing the tip against the sample as the sample is scanned. Either the repulsive force between the tip and sample or the actual tip deflection is recorded relatively to spatial variation and then converted into an analogue image of the sample surface. The small cantilever deflection can be measured by using a laser beam reflected from the top surface of the cantilever into a photodiode. Other imaging modes are available, such as the AC (or tapping) mode, which is particularly useful to analyze soft samples (even liquids) that can be damaged when using contact mode. In tapping mode the tip-cantilever assembly is always oscillating while the sample is scanned, with the tip only touching the sample at the bottom part of each oscillation cycle. [31]

* In 1986, Gerd Binning and Heinrich Rohrer were awarded the Nobel prize in Physics for their design of the STM. [29]
Besides acquiring images at a nanoscale, by using special tips and/or software modules, AFM can also be a powerful nanofabrication and electrical measurement tool, allowing for instance to define patterns with feature sizes in the range of a few nm and to measure electrical potential across the channel of operating transistors. [32, 33]

AFM analysis is performed on oxide semiconductor thin films deposited on silicon substrates, using an Asylum MFP3D AFM system existent in CENIMAT (fig. 3.8). The images are acquired in AC mode with a Si$_3$N$_4$ tip and a scan rate of 1 Hz.

![Figure 3.8 – Asylum MFP3D AFM system.](image)

3.4.2. Compositional characterization

3.4.2.1. Energy-dispersive X-ray spectroscopy (EDS), X-ray fluorescence (XRF) and X-ray photoelectron spectroscopy (XPS)

As shown in section 3.4.1.1 X-rays are very useful to infer about elemental identification of materials. The same kind of emitted radiation can be used to provide qualitative and even quantitative detection of elements by different techniques, being the ones used in this work briefly summarized below.

Energy-dispersive X-ray spectroscopy (EDS) is based on the detection of secondary X-rays emitted as a result of the interaction of a highly energetic electron beam with a sample. The incident beam ejects electrons from one of the inner shells of the material under analysis, hence electrons lying in outer, higher-energy shells tend to occupy the vacancies left by the ejected electrons. The energy difference between these shells, which is a signature of a chemical element, can be released in the form of X-rays that can then be collected by a suitable detector. The same apparatus used in a typical
SEM can be used to generate the electron beam and emit the secondary X-rays from the sample (see section 3.4.1.2), hence the EDS analysis capability is generally integrated in SEM systems by equipping them with a X-ray detector. EDS provides a quick analysis of the individual chemical elements in a sample, by comparing the experimental spectra to known X-ray energies. With recent detectors, even elements as light as beryllium can be detected. [34] The technique can also provide some quantitative information by the peak-height ratio relatively to a previously known standard. [35] Still, the obtained spectrum frequently contains overlapping energy peaks, because the energies corresponding to different energy-level shells in different elements can be coincident. Significant higher spectral resolution and enhanced quantitative potential are obtained by using the more expensive Wavelength-Dispersive X-Ray Spectroscopy (WDS) detectors. [26]

X-ray fluorescence (XRF) is based on the same principle, but now the samples are illuminated by an intense X-ray beam typically produced from a rhodium target, although tungsten, molybdenum, chromium and others can also be used. The same kind of detectors (EDS and WDS) can be employed in XRF systems, which are able to analyze elements until beryllium, although most conventional XRF equipments are limited to the detection of elements with higher atomic number than sodium. [26] The main advantage of XRF is the easy and fast acquisition of data, which can be done in air (i.e., not requiring vacuum). Still, due to the difficulty of focusing the incident X-ray beam in a small spot, the resolution is affected. Also, XRF measurements are affected by matrix effects, due to the absorption of secondary X-rays by the sample itself. [26]

While both techniques described above provide compositional analysis in the bulk of thin films, X-ray photoelectron spectroscopy (XPS) can provide information about the surface of the sample, with most of the signal arising from the top 0.5-5 nm. [26] The physical principle behind XPS is the photoelectric effect initially observed by Hertz in 1887. In XPS, soft monochromatic X-rays with E=200-2000 eV emitted by an X-ray source are directed to the sample, ejecting photoelectrons from it. The energy of an ejected electron can be measured by a spectrometer, being related with the binding energy of the atom from which the electron is ejected, i.e., the difference in energy between the ionized and neutral atoms. [27, 36] Since the binding energy is affected by the chemical surroundings, XPS allows both elemental and chemical identification. Detection of elements with atomic number above lithium is possible by XPS. Given the relatively low electron mean free paths, only the electrons ejected from the surface layers are able to escape the sample, and the measurements have to be performed in high vacuum to enable their analysis without interference from gas phase collisions. Depth profile measurements are also possible by using a complementary ion beam sputtering apparatus, but the damage induced by sputtering can modify the oxidation states of the sample under analysis. [26]
EDS, XRF and XPS are used in this work to access the composition of oxide semiconductor and dielectric (XPS only) thin films produced on silicon substrates, being performed with equipments located in the University of Barcelona. For EDS, a FEI Quanta 200 SEM equipped with an EDAX Saphire Si(Li) detector and Genesis microanalysis software is used, for a scan area around 50×50 μm². XRF is performed with a Philips PW2400 spectrometer equipped with a Rh tube. Finally, the XPS analysis is made in a Physical Electronics PHI 5500 Multitechnique System with a monochromatic X-ray source (Al Kα, 1486.6 eV), for an analyzed area of 0.8 mm diameter.

3.4.2.2. Time-of-flight Secondary ion mass spectroscopy (TOF-SIMS)

In most of the previously presented structural, morphological and compositional characterization techniques either electron beams or X-rays are used as the primary radiation source. Ion beams can also be used for this end, in powerful compositional analysis techniques such as secondary ion mass spectroscopy (SIMS), which allows to detect with high sensitivity elements as well as isotopes and molecular species present on a sample. [26, 27] The basic principle of SIMS, developed in the early 1960s, is the detection of the mass/charge ratio of secondary ions emitted from the sample when a primary beam of highly energetic ions (1-30 keV) impinges on it. [37] The primary ion beam, generally originating from ionization of noble gases (argon, xenon), oxygen or cesium, is accelerated and focused through the ion column onto the sample. The interaction of the ion beam with the sample gives rise to a sputtering process, where neutral species but also charged ones (secondary ions) are ejected from the sample. A mass spectrometer separates those ions according to their mass/charge ratios, being their number (intensity) measured by a suitable detector, such as a Faraday cup. The process requires a high vacuum to assure that a sufficient number of secondary electrons reach the spectrometer and that background gas species do not collide with them or are adsorbed at the sample’s surface. If instead of a magnetic/electrostatic or a mass quadrupole spectrometer a time-of-flight spectrometer is used, the mass/charge ratios are measured as a function of the time that ions take to travel to the analyzer. [26] This constitutes the designated time-of-flight SIMS (TOF-SIMS), requiring a pulsed ion beam (typically generated from liquid metal ion sources, using elements as gallium or bismuth) to impinge on the sample rather than a continuous ion beam as in conventional SIMS. Given that the TOF spectrometer does not have any narrow slits, ion collection is increased, allowing to use reduced incident beam energies, useful to analyze surface sensitive materials, such as organic materials. TOF-SIMS also provides a wider mass range and higher mass resolution detection than conventional SIMS. [26] TOF-SIMS measurements can be performed in different modes. The most widely used is depth profiling, where compositional
analysis is made layer by layer, and by scanning the beam across the surface of each layer three-
dimensional images relatively to the distribution of elements and compounds can be obtained.

TOF-SIMS is used in this work to analyze the contact region between source-drain electrodes and
channel layers in TFTs. The measurements are performed in an ION-TOF TOF-SIMS IV system with
Bi3++ ions, at the Parc Científic de Barcelona, University of Barcelona.

3.4.3. Electrical characterization

3.4.3.1. Four-point-probe (FPP) measurements

The resistivity ($\rho$) defines the fundamental class of an electronic material as a conductor,
semiconductor or insulator. Thus, $\rho$ constitutes one of the elementary properties that need to be
measured when exploring new materials for electronic applications. The simplest method to
measure $\rho$ in a thin film is to use a two point-probe setup, where each contact acts as a current ($I$)
and as a voltage ($V$) probe. Despite the simplicity, this method has important drawbacks, because the
measured resistance is severely affected by probe resistance, the spreading resistance under each
probe and the contact resistance between each metal probe and the semiconductor material. The
solution is to employ a four-point probe (FPP) setup, where $I$ is applied between two points and $V$ is
measured with two additional contacts. Even if the parasitic components enunciated above still exist
with the FPP setup, the voltage drops associated with them are negligible because the voltmeter has
a very high input impedance. [26, 38]

The FPP setup was originally proposed by Wenner in 1916 to measure the earth’s $\rho$, [39] being
adapted by Valdes in 1954 to measure the $\rho$ of germanium. [40] There are different FPP methods
that can be used, the most usual ones are: [38]

- the collinear method, where four equally spaced probes are placed on top of the semiconductor
  and the two outer probes are used for sourcing $I$ while the resulting $V$ is measured by the two
  inner probes;
- the van der Pauw method, which consists in having four small electrodes on the periphery of a
  flat, arbitrarily shaped sample of uniform thickness.

This last method is used to analyze the oxide semiconductor films produced during this research
work. A clover-leaf pattern is defined in the semiconductor by photolithography, and four Ti/Au
electrodes are then deposited on the periphery of the sample by e-beam evaporation using shadow
masks (fig. 3.9a). Each sample has approximately 1×1 cm. With this structure, $I$ is applied in two adjacent electrodes and $V$ is measured in the remaining ones, yielding a total of four possible electrode permutations, each with two $I$ directions. For each sample, suitable $I$ is chosen to provide acceptable signal-to-noise ratio ($V$>5 mV) and to avoid sample heating and large potential gradients induced by excessively high $I$.\[41\] For two adjacent electrode permutations (i.e., first applying $I$ between electrodes 1-2 and then between electrodes 1-4) $\rho$ is given by:

$$
\rho = \frac{\pi d_s}{2 \ln(2)} \left( \frac{V_{43} + V_{23}}{I_{12}} \right) \cdot F \cdot Q
$$

(3.2)

where $d_s$ is the semiconductor’s thickness, $F$ is the correction factor for geometrical asymmetry and is a function of the symmetry factor ($Q$), which can be defined by:

$$
Q = \frac{V_{43} \cdot I_{14}}{I_{12} \cdot V_{23}}
$$

(3.3)

or its reciprocal, whichever is greater than 1. [41] For an ideal sample $Q$=1 but values between 1 and 2 are normally obtained in real measurements. Higher values are typically a consequence of badly defined van der Pauw structures, non-Ohmic contacts between the semiconductor and the deposited electrodes and anisotropic samples. $F$ and $Q$ are related according to: [38]

$$
\frac{(Q - 1)}{(Q + 1)} = \frac{F}{0.693} \arccos \left[ \frac{e^{-F}}{2} \right]
$$

(3.4)

If $Q$<10, $F$ can be approximated by:

$$
F = 1 - 0.34657A - 0.09236A^2
$$

(3.5)

with $A$ given by:

$$
A = \left( \frac{Q - 1}{Q + 1} \right)^2
$$

(3.6)

Note that if $d_s$ is not known (in this work it is always determined by using a profilometer) a sheet resistance ($R_s$) can still be measured using the methodology described above, since $R_s = \rho / d_s$.

---

1 In van der Pauw samples, $d_s$ should be less than 1/15 of the peripheral length and the four electrodes should be placed symmetrically to minimize misalignment voltages. [41] Additionally, the ratio of sample thickness to probe spacing should be smaller than 0.3. [38] All these conditions are verified for the samples produced here.
The expressions above are then applied for all the possible electrode permutations, being the final $R_s$ and $\rho$ of the sample the average of those measurements. The system used for $R_s$ and $\rho$ determination is an Agilent 4155C semiconductor parameter analyzer (SPA) attached to a Cascade M150 microprobe station inside a dark box using triaxial cables, existent in CENIMAT (fig. 3.9b). This system is equipped with four source-monitor units (SMUs) that have very high input impedance voltmeters and high output impedance current sources, being suitable for measuring highly resistive samples. To attain all the electrode permutations in each sample, the SMUs are automatically programmed either as current sources or voltage meters by a simple configuration program run from the controlling computer, thus not requiring manually rotating the sample or using switching matrices to accomplish the complete measurement, which would induce additional noise to the measurements.

Even if the methodology described in this section is followed to extract $R_s$ and $\rho$, a modification is made in order to attain meaningful and reproducible measurements in highly resistive samples. For these samples it is noticed that the $V$ resulting from a $I$ stimulus takes some time to stabilize: [38, 41] with some of the more resistive oxide semiconductors analyzed in this work settling times as high as 2 to 3 min are verified. Hence, instead of collecting a single $V$ point for each electrode configuration, the measurements are rather performed as a function of time, typically 3-4 minutes each, considering for the final $R_s$ and $\rho$ calculation an average of the points acquired during the last 30 s, when $V$ is already stable.

The Agilent SPA is also used to make simple $I$-$V$ plots using two probes in metal-insulator-semiconductor (MIS) structures employing the sputtered dielectrics. Aluminum is e-beam evaporated in both sides of the structure, with a shadow mask being used to define circular electrodes with a diameter of 1 mm on top of the dielectric.
3.4.3.2. Hall effect measurements

The Hall effect was discovered in 1879 by Edwin Hall by characterizing a gold sheet and is used for a long time as a powerful tool for semiconductors’ research, allowing to obtain important properties such as $\rho$, majority carrier type (electrons of holes), $N$ and $\mu$. [26, 42] The effect is based on the Lorentz force, which reflects how a charged particle is affected when subjected to magnetic and electric fields:

$$F = q(\vec{v} \times \vec{B})$$  \hspace{1cm} (3.7)

where $q$ is the elementary charge of the particle, $\vec{v}$ is the velocity vector and $\vec{B}$ is the magnetic field vector. In a hall effect measurement with a van der Pauw sample (fig. 3.9a) $I$ is injected at two non-adjacent electrodes while having a magnetic field perpendicular to the sample surface. The Lorentz force deflects carriers to one side of the sample, perpendicularly to $\vec{B}$ and $\vec{I}$, creating an electric field ($\vec{E}$) in the sample between the remaining two non-adjacent electrodes (fig.3.10a). When the system is in equilibrium the magnetic and electrostatic forces are balanced:

$$q(\vec{v} \times \vec{B}) = q\vec{E}$$  \hspace{1cm} (3.8)

Since $\vec{B}$, $\vec{I}$ and $\vec{E}$ are perpendicular, the vectors can be replaced by scalars. In this situation $I$ is given by:

$$I = qNd_sWv$$  \hspace{1cm} (3.9)

where $W$ is the separation between the two electrodes. By substituting eq. 3.9 into eq. 3.8, the Hall voltage ($V_H$) can be defined, since $V_H = EW$:

$$V_H = \frac{BI}{qNd_s}$$  \hspace{1cm} (3.10)

This value is measured by the system, and from $V_H$ another important parameter can be extracted, the Hall coefficient ($R_H$):

$$R_H = \frac{V_Hd_s}{IB}$$  \hspace{1cm} (3.11)

The sign of $R_H$ indicates whether the semiconductor is n- (negative) or p- (positive) type. n-type conduction is observed for all the oxide semiconductors studied in this work. If $d_s$ is not known, one can still define a sheet Hall coefficient ($R_{hs}$):
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\[ R_{HS} = \frac{R_H}{d_s} = \frac{V_H}{IB} \]  

\[ R_{HS} \] is useful to determine the sheet carrier density \( (N_s) \), but if \( d_s \) is known \( N \) can be determined by \( R_{HS} \):

\[ N_s = \frac{1}{qR_{HS}} \]  

Finally, \( R_{HS} \) is employed to calculate the Hall mobility \( (\mu_H) \) without requiring \( d_s \) by:

\[ \mu_H = \frac{R_{HS}}{R_S} \]  

where \( R_S \) is measured using the FPP setup, as described in p. 65. \( \mu_H \) is related with \( \mu \) by the scattering factor \( (r) \), according to:

\[ \mu_H = r \mu \]  

\( r \) assumes a statistical distribution of \( v \) essentially due to scattering effects, and typically has values between 1 and 2. For instance, \( r \) is 1.18 for lattice scattering and 1.93 for impurity scattering. [26, 42]

![Figure 3.10 – Hall-effect measurements: schematic of the experimental setup; (b) Biorad HL-5500PC Hall effect system.](image)

Throughout this research work, oxide semiconductors based on the gallium-indium-zinc oxide system are analyzed by Hall effect using a Biorad HL-5500PC equipment existent in CENIMAT (fig. 3.10b), with a constant magnetic field of 0.5 T. The same Van der Pauw test structures used for \( R_s \) and \( \rho \) measurements in the Agilent 4155C SPA are used here (fig. 3.9a). The system is equipped with a high resistivity buffer amplifier that allows to work in the pA range, in order to measure highly resistive samples. Still, given the low \( \mu_H \) of these materials comparatively to conventional single crystalline semiconductors such as silicon, consistent measurements are only obtained for samples with \( \rho \) lower
than $\approx 10^2 \ \Omega\cdot \text{cm}$. Depending on the films’ $\rho$, delay and integration times up to 10 s are used and $V_H$ is determined for each sample as the average of three hall measurement cycles. Each cycle includes offset measurement, magnet reversal (north-south) and changing the $I$ direction on the two sets of electrode combinations. Samples are measured in the dark, at room temperature.

The Biorad system is also equipped with a vacuum pump, heating stage and a liquid nitrogen pump, allowing to perform hall-effect measurements at different temperatures. This feature is used to analyze oxide semiconductors between 100 and 300 K, which is extremely relevant to access information regarding the conduction mechanisms of these materials. The results are presented and discussed in section 4.1.5.2.

3.4.4. Optical characterization

In a material, a multitude of effects can arise due to its interaction with photons. The incident photons can be emitted, reflected, absorbed or transmitted and each one of these phenomena can be explored by different techniques. [26] Which of the photon-material interactions happens depends on the material itself and on the energy ($E$) of the incident photons, given by:

$$
E = h\nu = \frac{hc}{\lambda}
$$

(3.16)

where $h$ is the Planck’s constant, $\nu$ is the photon frequency, $c$ is the speed of light and $\lambda$ is the photon wavelength. In this work are explored two optical characterization techniques that deal with several of these interactions, because $E$ is changed over a large range in both of them. These techniques are UV-Visible-Near-infrared (NIR) transmittance spectroscopy and spectroscopic ellipsometry.

3.4.4.1. UV-Visible-NIR transmittance spectroscopy

This technique can be used to extract important optical parameters of transparent oxide (semi)conductors, such as the absorption coefficient ($\alpha$), the refractive index ($n$), the optical bandgap ($E_{\text{opt}}$) and transition type, the thin film’s thickness ($d$), and naturally, the degree of transparency for a given $\lambda$. [2, 26, 43] To determine these parameters, the optical transmittance ($T$) and reflectance ($R$) are first measured across the $\lambda$ range of interest, by using a spectrophotometer. From this data $\alpha$ can be determined by:
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\[ \alpha = \frac{1}{d_s} \ln \left( \frac{1}{1 - A} \right) \quad (3.17) \]

where \( A \) is the optical absorption of the thin film. Even if \( A = 1 - T - R \), by neglecting \( R \) slightly inaccurate \( \alpha \) values are obtained, but \( \alpha \) evolution with \( E \) is not severely affected, thus not introducing significant errors in \( E_{\text{opt}} \) determination. [43] \( E_{\text{opt}} \) corresponds to the fundamental absorption process, i.e., to the excitation of a valence electron to a higher energy state. Assuming parabolic bands, \( E_{\text{opt}} \) can be calculated by a linear fit at the onset of \( \alpha^x \) abrupt rise, according to: [2, 43, 44]

\[ \alpha^x \propto (h\nu - E_{\text{opt}}) \quad (3.18) \]

where \( x \) is a value related with the transition type, which can be \( 2, 2/3, 1/2 \) or \( 1/3 \) depending if the transition is allowed direct, forbidden direct, allowed indirect or forbidden indirect, respectively. The dominant transition type is determined by the linearity of the fit, but due to the multiple competing absorption processes, this estimation of \( E_{\text{opt}} \) has some degree of uncertainty. [43]

Valuable information regarding absorption at the band tails, i.e., for lower energies than \( E_{\text{opt}} \), can also be obtained. This involves plotting the \( \alpha \cdot E \) data according to: [2, 45]

\[ \alpha \propto e^{-\frac{E}{E_u}} \quad (3.19) \]

where \( E_u \) is the Urbach energy, often seen as a measure of structural disorder and representative of the width of the band tails.

The transmittance measurements of the oxide semiconductor thin films deposited on glass substrates are accomplished with a Shimadzu UV-3101 system existent in CEMOP (fig. 3.11a), with \( \lambda \) between 250 and 2500 nm. On selected samples, reflectance measurements are also performed in the range between 250 and 800 nm, by using a spectrophotometer accessory, the integrating sphere, whose interior surfaces are coated with barium sulfate (BaSO_4) so that all the scattered light is focused toward the detector plates. \( \alpha \) and \( E_{\text{opt}} \) are the main parameters analyzed in this dissertation, according to the methodology described above, and since the main focus is on transparent materials in the visible region of the wavelength spectrum, transparency is also measured by averaging transmittance data between 400 and 700 nm (average visible transmittance, AVT).
3.4.4.2. Spectroscopic ellipsometry

Ellipsometry is a contactless and non-invasive optical technique permitting to measure changes in the polarization state of light reflected from a surface. [26] Ellipsometry relies on the measurement of amplitude and phase variation of a polarized light beam after being reflected by the sample. [19] The polarized light can be resolved into parallel and perpendicular components relatively to the incident plane, allowing to measure a complex reflection ratio ($\rho_F$), also known as Fresnel coefficient, as a function of the parallel and perpendicular reflection coefficients ($R_p$ and $R_s$, respectively) or of the ellipsometric angles $\psi$ and $\Delta$, that represent the differential changes in amplitude and phase, respectively: [19, 26]

$$\rho_F = \frac{R_p}{R_s} = \tan \psi \cdot e^{i\Delta} \quad (3.20)$$

Single-wavelength ellipsometry employs a monochromatic light source, hence for a given sample the measurements only provide a set of $\psi$ and $\Delta$ angles. Still, this data can be used to analyze various properties of the materials, since $\psi$ and $\Delta$ are sensitive to film thickness, composition, microstructure, surface roughness, among other properties. [19, 26] But spectroscopic ellipsometry can further extend the possibilities of this technique, by using a light source coupled with a photo-elastic modulator that allows to collect data over a broad spectral range (covering IR, visible and UV regions), and by allowing to change the angle of incidence of the light beam. This permits a new field of applications, with special relevance for non-invasive real-time process control. [26]

In this work, spectroscopic ellipsometry is used for the determination of two important optical parameters, extinction coefficient ($k$) and refractive index ($n$), for oxide semiconductor and dielectric thin films deposited on glass and silicon substrates, respectively. This is accomplished over a broad range of $E$, 0.65-6.5 eV for oxide semiconductors and 1.5-6.0 eV for dielectrics, with an incident angle of 70°, by using a Jobin Yvon Uvisel system existent in CENIMAT (fig. 3.11b). The acquired data is modulated using the DELTAPSI software with different models depending on the analyzed materials, always pursuing the minimization of the error function ($\chi^2$). For the dielectric thin films a Tauc-Lorentz dispersion formula is used, while for the oxide semiconductor thin films a Drude model is associated with the Tauc-Lorentz formula to take into account the contribution of free carriers. [5, 19]
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3.5. Thin-film transistor and active matrix backplane characterization

Most of the characterization effort of this research work is devoted to electrical analysis of TFTs produced with different processing conditions. Main emphasis is given to the measurement of typical I-V characteristics, both in TFT test substrates and in the test structures of active matrix backplanes. Stress measurements, including aging effects, constant $I_D$ stress and On-Off switch simulation by using a square wave signal on the gate electrode are also explored.

3.5.1. Static current-voltage characteristics

As mentioned in section 2.3.1, the fundamental characterization of a TFT encompasses the measurement of output and transfer characteristics. The former are essentially used for qualitative evaluation of the devices, allowing for instance to verify if saturation is achieved or if $I_D$ crowding exists at the low $V_D$ region, which is generally indicative of contact resistance issues. However, most of the characterization is focused on transfer characteristics, which allow to extract several parameters such as $\mu FE$, $V_{on}$, $V_T$, $S$ and On-Off ratio.

The same measurement protocol is used to characterize all the devices, regarding the order of obtaining each characteristic curve, the number of successive measurements and the range of $V_G$ and $V_D$ employed. The effect of this measurement procedure is negligible for stable transistors, but erroneous analysis and comparisons can arise for unstable or non-ideal devices if exactly the same protocol is not followed, as verified in initial samples produced during this research work. A typical example is the comparison of two transfer characteristics of two similar but non-ideal devices: if in

Figure 3.11 – Optical characterization tools: (a) UV-Vis-NIR Shimadzu UV-3101 spectrophotometer; (b) Jobin Yvon Uvisel spectroscopic ellipsometer.
one device the transfer characteristic used for comparison is taken as the absolutely first measurement while in the other device the transfer characteristic is only measured after taking several transfer and/or output characteristics, from the comparison it could be concluded that the two transistors present totally different properties, even if processed under the same deposition conditions. But in reality, this would not be a consequence of lack of reproducibility, but rather of a different kind of non-ideality, for instance related with the large $V_{on}$ shift ($\Delta V_{on}$) that unstable devices present after three or four successive transfer characteristics measurements, which can be higher than 6 V (see section 5.1.2). The established protocol to avoid these erroneous comparisons from happening consists of:

- Three consecutive transfer characteristics with $V_G$ ranging from -10 to 30 V, with $V_G$=20 V, performed in single sweep mode. This set allows to have an initial idea of the stability of the TFT, by inspection of $\Delta V_{on}$;
- One transfer characteristic with $V_G$ ranging from -10 to 30 V, with $V_G$=1 V to assure linear mode operation, performed in double sweep mode. This plot is used to extract $\mu_{FE}$;
- One transfer characteristic with $V_G$ ranging from -10 to 30 V, with $V_G$=30 V to assure saturation mode operation, performed in double sweep mode. This plot is used to extract $V_{on}$, $V_T$, $S$ and On-Off ratio;
- One output characteristic with $V_G$ ranging from 0 to 30 V, with 9 steps of $V_G$, from 0 to 30 V.

This setup is valid for the TFTs produced on Si/SiO$_2$ substrates. For the TFTs employing sputtered dielectrics the same procedure is used, with the only difference being the maximum $V_G$ and $V_D$, which are reduced to 15 V to prevent dielectric breakdown.

All these tests are performed using the same Agilent 4155C SPA and Cascade M150 microprobe station used for $R_s$ and $\rho$ measurements in oxide semiconductor thin films. The measurements are made in the dark, at room temperature, with relative humidity being maintained between 35-50 %. The protocol defined above is configured in the controller computer, using the software ICS Lite.

Some electrical measurements are also performed in vacuum (see fig. 5.27) and for this the Agilent SPA is connected to a small cryostat chamber existent in CENIMAT. For this setup the triaxial connectors have to be replaced by BNC connectors, resulting in higher noise level (i.e., higher Off-current). For all the transfer and output characteristics, hold and delay times are fixed at 100 ms.
3.5.2. Stress measurements

Even if oxide semiconductor-based TFTs are still in a very early stage of development, stress measurements are important to study the dominant degradation mechanisms and to see if they are suitable for application in present and future electronic circuits. Besides the early-stage aging inferred by $\Delta V_{on}$ in consecutive transfer characteristics, three other stress methodologies are used in this work and are briefly described below. The same Agilent 4155C SPA and Cascade M150 microprobe station are used for all these stress measurements.

3.5.2.1. Aging effects

This method consists in measuring the TFTs electrical characteristics by using the protocol described in section 3.5.1 in specific time periods, during 18 months. Throughout this period the devices are kept in a room, exposed to air ambient. This is used to evaluate the variation of the electrical properties on TFTs produced on Si/SiO$_2$ substrates with different oxide semiconductor processing conditions.

3.5.2.2. Constant drain current and constant gate bias stress

Constant $I_D$ consists in a severe stressing condition, intended to simulate the behavior of the TFTs in an electronic circuit where they have to supply a constant current to another device. The most immediate example is the usage of these TFTs as the “drive transistors” in OLEDs (see section 2.4.2). A schematic of the electrical connections is presented in fig. 3.12. Drain and gate terminals are shorted in a diode-connected configuration, with the source electrode grounded. [46] A constant $I_D=10$ $\mu$A is applied during 24 h, at room temperature, in the dark. During this period, the electrical configuration automatically adjusts $V_G$ to maintain the constant $I_D$. After 24 h the constant $I_D$ is no longer applied and the devices start recovering their properties. The stress measurement and recovery period are shortly interrupted several times to assess the transfer characteristics of the TFTs. Devices on Si/SiO$_2$ substrates and on glass/sputtered dielectrics are both subjected to constant $I_D$ stress measurements.

Some devices are also analyzed using typical bias stress measurements, where a constant $V_G=20$ V is applied during 8 h, while keeping the source and drain electrodes grounded. As in the constant $I_D$
stress measurements, the stress/recovery periods are shortly interrupted several times to assess the transfer characteristics of the TFTs.

![Schematic of the electrical connections for constant \(I_o\) stress measurements.](image)

### 3.5.2.3. Square wave on gate electrode

The last stress methodology also intends to be a preliminary simulation of the behavior of the TFT in an electronic circuit. By applying a square wave signal to the gate electrode, the objective is to rapidly alternate for a large number of times between the \(\text{On}\) and \(\text{Off}\) states of the transistor. For instance, this is the situation that the TFTs are subjected when they are used as switching elements in LCD or OLED backplanes (see sections 2.4.1 and 2.4.2). These tests are accomplished by characterizing the TFTs in the Agilent 4155C SPA and Cascade M150 microprobe station, but having the gate electrode connected to a Wavetek 395 synthesized arbitrary waveform generator. During the measurement, \(V_o\) is kept at 15 V and \(V_G\) assumes a square wave form, with an offset of 2.5 V and a peak-to-peak voltage \((V_{pp})\) of 15 V, corresponding to \(V_G=-5\) and 10 V, i.e., to the \(\text{Off}\) and \(\text{On}\) states of the TFT, respectively. Two different square wave frequencies are used, 2 Hz and 10 kHz, being the stress duration of 40 and 20 min, respectively. During this period, \(I_o\) data is recorded with the Agilent SPA, which is also used to measure the transfer characteristics before and after the stress measurement. In this dissertation, this methodology is demonstrated on TFTs produced with sputtered dielectrics, since they closely match in terms of structure and materials the devices integrated afterwards in the LCD active matrix backplanes.

### 3.6. References

Chapter 4

Properties of n-type oxide semiconductor and high-κ dielectric thin films produced by sputtering

This chapter discusses the results regarding the characterization of sputtered oxide thin films, both semiconductors and high-κ dielectrics, which are the basis of the TFTs and active matrices presented in the next chapters. The materials are characterized concerning a broad range of properties such as structural, morphological, compositional, electrical and optical. The detailed analysis of these material properties is of great relevance to understand the behavior of the devices where they are integrated. The chapter is divided in two main sections, the first and more detailed one being dedicated to n-type oxide semiconductors, the second to multicomponent amorphous high-κ dielectrics, all processed without intentional substrate heating.

4.1. Oxide semiconductors based on gallium-indium-zinc oxide system

Given that the main focus of this thesis is on the study and optimization of oxide semiconductors for application on TFTs, a more detailed analysis is presented for these materials, primarily concerning their electrical properties, including some insights about conduction mechanisms and long-term stability data. Several ceramic target compositions, including binary and multicomponent compounds (ternary and quaternary, with different atomic ratios), deposition and post-deposition parameters are studied, namely \( %O_2 \), \( p_{\text{depl}} \), \( P_{\text{tot}} \), and \( T_A \), being their effect on the materials’ properties discussed throughout the chapter.

4.1.1. Process flow and deposition parameters

Figure 4.1 shows the process flow used to fabricate the oxide semiconductor thin films suitable for the different characterization techniques. Regarding the sputtering process, it was performed in a Pfeiffer Vacuum 500 system (fig. 3.3a, p. 51) always without intentional substrate heating. Base pressure was maintained at 0.4-0.6 mPa, target-to-substrate distance at 15 cm and substrate size was always 2.5×2.5 cm. In order to assure reliable results for the various characterization techniques, the oxide semiconductor films were produced with a thickness around 200-250 nm, although thinner films (=40 nm) were also deposited for selected samples to study the effect of thickness on the electrical properties.
4.1.1. Dependence of the growth rate on the deposition parameters and target composition

The growth rate of sputtered films is highly dependent not only on the material composition but also on the deposition parameters (and naturally, on the sputtering system itself). Furthermore, the growth rate can affect the properties of a sputtered thin film: as an example, it is known that for a given material certain deposition conditions assuring too high or too low growth rates can negatively affect the film’s properties, since under these extreme conditions the sputtered species can, respectively, damage the growing film due to severe bombardment or reach the substrate without...
4. Properties of n-type oxide semiconductor and high-κ dielectric thin films produced by sputtering

enough energy to create a compact film. Thus, before initiating a detailed discussion about the properties of the oxide semiconductor materials, it is important to see how their growth rates are affected by the deposition parameters and composition. This is depicted in fig. 4.2, regarding %O₂, p_{dep}, P_{rf} and target composition.

The deposition of oxides by sputtering in a pure argon atmosphere, even if starting from ceramic targets, generally results in films with high oxygen deficiency. This is essentially related with the threshold energy required to sputter a particle, which is higher for a metal-oxide than for a metal. [1] Additionally, molecular species sputtered from a target heading towards the substrate, such as a ZnO molecule, can be dissociated inside the plasma, increasing the chances of non-stoichiometric film formation. [2] Hence, a small percentage of oxygen, typically less than 10 %, is usually mixed with the argon atmosphere in order to have a better control of the stoichiometry of the growing film. [3, 4] Figure 4.2a shows the effect of increasing %O₂ on the growth rate, for films produced from targets with different compositions. Regardless of the composition, growth rate decreases as %O₂ increases, which can be attributed to multiple factors:

---

**Figure 4.2 – Dependence of the growth rate on (a) %O₂, (b) p_{dep}, (c) P_{rf} and (d) target composition.**
• Resputtering (i.e., sputter-etch) of the growing film due to bombardment of highly energetic oxygen ions. [3, 5] This is especially relevant for higher %O₂ and as will be seen later, this phenomenon can significantly affect other film’s properties, including its composition;

• Change of the surface conditions of the target. [2, 3] For instance, with a ZnO target, if a pure argon atmosphere is used, target surface will be less oxidized, favoring the sputtering of zinc atoms rather than ZnO aggregates. This results in higher growth rates, since the binding energy of zinc is lower than the one of ZnO, i.e., sputtering a ZnO molecule from the target requires more energy. [3] Additionally, the energy transfer from an Ar⁺ incident ion to the ejected target material is greatest when the mass of the ejected particle is closer to that of the ion, resulting in a greater sputtering rate in the absence of oxygen. [4] Different surface conditions of the target can be readily seen by visual inspection of its surface after being involved in sputtering processes with different %O₂;

• For low %O₂ the oxidation reaction takes place essentially on the substrate, which is reflected in a small or even negligible decrease on the growth rate when compared with sputtering in a pure argon atmosphere. However, for higher %O₂ target oxidation starts to play an important role, decreasing the growth rate due to the arguments given in the previous point. [3, 6]

\( p_{\text{dep}} \) also affects the growth rate of all the analyzed oxide semiconductors. As shown in fig. 4.2b, the growth rate decreases as \( p_{\text{dep}} \) increases. Similar results were obtained before for the indium-zinc oxide system. [7] This is essentially related with the lower mean free path of sputtered species for higher \( p_{\text{dep}} \), due to their more intense scattering by gas atoms and molecules during their path from the target to the substrate. [8] After these collisions, the sputtered particles are thermalized and only contribute to the film growth by diffusive transport, decreasing the growth rate when compared with processes at lower \( p_{\text{dep}} \), where ballistic transport dominates (or contributes) to the film growth. This is in agreement with the Keller-Simmons relation, [1, 9] which is adequate to describe the behavior of most of the oxides studied here. The most significant exception is ZnO that presents similar growth rates for \( p_{\text{dep}}=0.4 \) and 0.7 Pa. This should be attributed to higher sensitivity of this material to resputtering effects by energetic plasma particles, such as O⁺ and neutralized Ar ions, which are more prevalent at lower pressures. Similar results were obtained for ZnO films by other authors. [1, 9]

Since \( P_{rf} \) directly affects the discharge voltage, i.e., the negative dc voltage measured at the target, it is expected that growth rate increases for higher \( P_{rf} \), which can indeed be verified in fig. 4.2c. For GIZO 2:4:2, four different \( P_{rf} \) were tested, yielding a linear relation with the growth rate for \( P_{rf} \) between 1.1 and 2.7 W cm⁻². However, for very low \( P_{rf} \) (0.6 W cm⁻²), growth rate decreases faster than this linear relation would predict, meaning that in this regime the energy of the incident ions is not enough to assure a large number of sputtered species. This is typical in sputtering processes with rf excitation, since for a given power the discharge voltages are considerably lower than with dc
excitation, so a certain threshold \( P_{e/f} \) needs to be applied to have a reasonably high discharge voltage that permits an efficient sputtering process. [2, 10] Additionally, given the low energy of the sputtered species close to this threshold \( P_{e/f} \), they have very low velocities and are more prone to be affected by collisions on their path to the substrate, decreasing the growth rate. This non-ideal growth process for low \( P_{e/f} \) dramatically affects films’ properties, hence this processing condition was avoided during this work.

Figure 4.2d shows a ternary diagram with the growth rates of all the oxide semiconductor compositions studied in the gallium-indium-zinc oxide system, deposited using the same deposition conditions: \( \%O_2=0.4 \% \), \( p_{dep}=0.7 \) Pa and \( P_{e/f}=1.1 \) W cm\(^{-2}\). Comparing the binary oxides, In\(_2\)O\(_3\) exhibits the highest growth rate, more than twice of ZnO, while Ga\(_2\)O\(_3\) is slightly higher than ZnO. The differences should be related with the different mass (atomic number) and binding energy of the elements composing the ceramic targets as well as with the crystal structure of their surfaces, which are known to be the target parameters mostly affecting the sputtering yield. [10, 11] For instance, it was shown by Stuart and Wehner that sputter yields vary periodically with the element’s atomic number, with the yield increasing consistently as the electronic \( d \) shells of the materials are filled. [10] For the multicomponent oxides, it is found that growth rate decreases when compared with In\(_2\)O\(_3\) and gets lower for higher concentrations of zinc and gallium, i.e., it gets closer to the growth rates of isolated ZnO and Ga\(_2\)O\(_3\), respectively.

### 4.1.3. Structural and morphological properties

Oxide semiconductors present a multitude of different structures and morphologies which directly affect other properties and hence dictate to a large extent the possible applications envisaged for a given material. Composition and \( T_s \) dependence were studied for all the produced oxide semiconductors. For the multicomponent oxides, particularly GIZO, a more complete study was performed, comprising the effect of the various deposition parameters (\( \%O_2 \), \( p_{dep} \) and \( P_{e/f} \)) on the structural and morphological properties but no significant or meaningful trends were found for those parameters, at least within the range of deposition conditions studied herein. On the contrary, although not explored here, it is reported that the structure and morphology of ZnO are severely affected by the deposition conditions mentioned above, specially regarding grain size, internal stress and surface roughness. [2, 8, 12-14]

Figure 4.3 shows the X-ray diffraction (XRD) results obtained for (a) In\(_2\)O\(_3\), (b) ZnO and (c) IZO and GIZO thin films annealed at different temperatures but deposited under the same deposition conditions.

---

\( \text{Note that for all the multicomponent compositions studied herein } \text{In/}(\text{In+Zn}) \text{ and In/}(\text{In+Ga}) \text{ atomic ratios are always } \geq 0.50, \text{ i.e., indium has always the same or larger atomic concentration as zinc and gallium.} \)
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conditions (\(\%O_2=0.4\ %, p_{dep}=0.7\ Pa\) and \(P_{nf}=1.1\ W\ cm^{-2}\)), on Si/SiO\(_2\) substrates. For all the XRD analyses presented here, some decoupling for the silicon substrate was applied in order to reduce its large peak close to 70\(^\circ\), resulting in a broad and low intensity peak rather than an intense and sharp peak that would overshadow films’ features. The data is normalized to the maximum peak intensity.

Typically, low-temperature deposited In\(_2\)O\(_3\) films are amorphous but have a very low crystallization temperature, around 150-170 °C. [15-17] Figure 4.3a shows that the In\(_2\)O\(_3\) films annealed at 150 °C are already polycrystalline, but still present some amorphous contribution, as evident from the halo peak around 32° that exist on the background of the diffractogram. Structures comprising amorphous and polycrystalline components are common for In\(_2\)O\(_3\) films annealed (or processed) below 200 °C. [17, 18] Enhanced crystallization and a predominance of (222) reflection occurs for higher \(T_a\), and at 500°C the films exhibit sharp crystalline peaks that clearly correspond to the cubic bixbyite In\(_2\)O\(_3\) structure. For In\(_2\)O\(_3\) films (or ITO, which crystallize in the In\(_2\)O\(_3\) system) deposited at low temperatures, generally the predominant planes are (222) and (400), [3] with (222) being the
preferred orientation for films deposited using an oxygen containing atmosphere, which is the case here. [17, 19]

An estimate of the crystallite sizes (D) can be obtained by the Scherrer formula: [20, 21]

\[ D = \frac{0.9 \lambda}{B \cos \theta} \]  

(4.1)

where \( \lambda \) is the X-ray wavelength (1.54 Å), \( B \) is the full width at half maximum (FWHM) of the Bragg diffraction angle \( 2\theta \). This yields a value of 27 nm for the (222) orientation of In\(_2\)O\(_3\) film annealed at 500 °C, which is close to the values reported in literature extracted by this methodology for In\(_2\)O\(_3\) and ITO films. [6, 22]

ZnO films (fig. 4.3b) are polycrystalline even before any annealing treatment. The films crystallize with a hexagonal wurtzite structure, with a preference for the (002) plane of this structure, i.e., the crystals grow along the c-axis, perpendicularly to the substrate, forming highly textured films. This preferential orientation, observed in most of the low-temperature deposited ZnO films reported in literature, [13, 23-25] is attributed to the fact that in the hexagonal structure the c-plane of the ZnO crystallites corresponds to the densest packed plane with the minimal surface energy. [10, 12] Films annealed at higher temperatures do not reveal any change on this preferred orientation, but the decreased width of the (002) peak suggests an improvement on the crystallinity. In fact, the crystallite size increases from 14.2 to 20.35 nm, as \( T_a \) increases from 150 to 500 °C. Similar grain sizes extracted using the Scherrer formula were obtained for sputtered ZnO films by other authors. [4, 20, 26]

For the other binary oxide used here, Ga\(_2\)O\(_3\), amorphous films are always obtained, even if annealed at 500 °C (not shown). In the literature, Ga\(_2\)O\(_3\) sputtered films were consistently found to crystallize only when annealed at higher temperatures, typically above 800 °C. [27, 28]

Concerning the multicomponent oxides, as-deposited IGO, IZO and GIZO films are found to be amorphous regardless of their composition, exhibiting only a broad peak centered at \( 2\theta \approx 32-34\degree \) (besides the one close to 70°, arising from the silicon substrate), typical of amorphous films. [15, 29-31] By Scherrer analysis on this broad peak, possible crystallite sizes have only around 2 nm, which is consistent with the values typically reported in literature for multicomponent oxides, validating their designation as amorphous materials. [32-36] Even after 500 °C annealing (fig. 4.3c), most of the films remain amorphous, with the only exception being the IZO 4:1 composition, which undergoes crystallization between 400 and 500 °C. This film crystallizes under the same cubic bixbyite structure as the isolated In\(_2\)O\(_3\) films, with the predominant planes and the relative intensities of the peaks being essentially the same in both cases (compare with fig. 4.3a), although the IZO films present smaller crystallite sizes, around 18 nm. The peaks are slightly shifted to higher values of \( 2\theta \) for the
IZO 4:1 composition due to the distortions in the In$_2$O$_3$ crystal lattice caused by zinc. Based on these results, three general rules can be deduced concerning the multicomponent oxides structure:

- Mixing different oxides, such as In$_2$O$_3$ and ZnO, inhibits or at least increases the crystallization temperature, due to the disorder introduced in the structure (compare fig. 4.3a and b with c);
- The crystallization in multicomponent oxides is favored for compositions with higher concentration of one of the composing elements, being the obtained crystal lattice based on the oxide of the predominant element$^b$ (compare IZO 4:1 with IZO 1:1 in fig. 4.3c);
- Multicomponent oxides with a higher number of elements (in this case, GIZO) are harder to crystallize, due to increased disorder in the structure.

The fact that these multicomponent oxides present amorphous structures, which are stable in a broad range of compositions and temperatures, is of major importance for the application of these films on devices. In fact, an amorphous structure is advantageous concerning not only process related issues, like uniformity, reproducibility and low-temperature deposition, but also regarding device performance, since amorphous films are generally much smoother than polycrystalline ones, improving interface properties.

The differences in smoothness and morphology between ZnO and IZO/GIZO films are clearly visible in the SEM and AFM images presented in figs. 4.4 and 4.5, respectively.

![SEM and AFM images](image_url)

*Figure 4.4 – SEM images of (a) ZnO and (b) GIZO 2:2:1 surfaces, for thin films annealed at 500 °C.*

ZnO presents a typical textured surface (fig. 4a), with nanocrystals in the range of 70 nm, measured using simple imaging techniques. Note that when compared with the crystallite size determined by the Scherrer formula, these values are around 3 times higher, revealing that the grain sizes are underestimated by using the Scherrer formula. This effect was already verified for sputtered ZnO films [20, 37] and also for other oxides such as SnO$_2$ [38] and is generally attributed to the different grain size estimation methodology inherent to the techniques. While in SEM the grain size is

$^b$ Although not studied here, IZO films where zinc is the predominant element are reported to crystallize with the wurtzite ZnO structure. [30, 32]
measured by the distances between the visible grain boundaries, in XRD it is determined by the extent of the crystalline regions that diffract the X-rays coherently, which is a more stringent criterion. [37] Other reasons pointed out in literature to justify these differences are instrumental broadening of FWHM, stress-induced and mosaic structure-induced broadening and neglect of strain. [21] The inset in fig. 4.4a shows the columnar growth of the ZnO film, being visible that the first deposited layers are composed of grains with smaller size and during the growth of subsequent layers larger crystallites start to coalesce perpendicularly to the substrate. Under certain deposition conditions, especially when using amorphous substrates, this initial layer may even form a very thin amorphous film, since new coming particles have, in general, higher tendency to relax in the same phase of nearby particles. [39] The GIZO surface reveals a totally different morphology, with very smooth and small feature sizes, less than 10 nm, measured using the same imaging methodology as for ZnO. The fact that these small features are present in these multicomponent oxides makes some authors to designate them by amorphous/nanocrystalline materials, [35, 40] although no distinct peaks are visible in the XRD data.

AFM images confirm the results obtained by XRD and SEM, with features considerably larger being obtained for ZnO (fig. 4.5a) than for GIZO (fig. 4.5b) films. The root-mean-square (RMS) roughness was determined from the AFM images, yielding values close to 3.8 nm for ZnO and 2.0 to GIZO.

![Figure 4.5 – Topography AFM images of (a) ZnO and (b) GIZO 2:4:2 surfaces, for thin films annealed at 500 °C.](image)

TEM analyses were also performed on 500 °C annealed films to confirm the structural results presented above. For GIZO films, the electron diffraction patterns reveal diffuse and broad electron diffraction rings, typical of amorphous films that exhibit some short-range order (fig. 4.6a). [41, 42] However, for IZO 4:1 films annealed at 500 °C, the electron diffraction pattern clearly shows evidence of a crystalline structure, which corresponds to the cubic In₂O₃ phase (fig. 4.6b). It is also interesting to note that the 250 nm thick IZO 4:1 film is not fully crystallized after 1 hour at 500 °C and that the crystallization process is initiated on the IZO/SiO₂ interface, as revealed by the Bright-Field Scanning TEM (BFSTEM) image (fig. 4.6c).
4.1.4. Compositional analysis

The composition of the multicomponent thin films was also analyzed and the obtained results were compared with the actual target compositions, for films produced with different GIZO targets and deposition parameters. Figure 4.7 shows some of the most relevant results, obtained for GIZO films annealed at 300 °C, deposited with %O₂=0.4 %, p_{dep}=0.7 Pa and P_{rf}=1.1 W cm⁻². Different analytical techniques were used, namely XPS, EDS and XRF. However, with the XPS analysis, severe carbon contamination was detected on the surface of the GIZO samples, reaching in some cases around 30 %. Given that XPS is essentially a surface analysis technique, with most of the signal arising from the first layers of the films, this contamination inevitably leads to erroneous results. Hence, a common surface cleaning treatment is generally employed on these cases, consisting of an Ar⁺ bombardment at relatively low energies (about 4 keV). However, this raised another issue, since besides removing the carbon contaminants, the Ar⁺ ions also sputtered indium atoms from the films, changing again their composition (fig. 4.7a). This preferential indium removal can be justified by its high sputtering yield in a typical sputtering process (like was seen in fig. 4.2a, In₂O₃ deposits much faster than ZnO or Ga₂O₃). On the other hand, EDS and XRF allowed to obtain considerably improved results, as these techniques deal with compositional information extracted from a large volume (or depth) of the films. In fact, with the experimental conditions used for both techniques, the silicon substrate was detected, meaning that the films were being analyzed through all their thickness.

Although some more results are needed to make detailed conclusions about the compositional variations, some general trends regarding the influence of the target composition on the composition of the films can already be established based on fig. 4.7 and table 4.1:
4. Properties of n-type oxide semiconductor and high-κ dielectric thin films produced by sputtering

**Figure 4.7** – Atomic concentrations of gallium, indium and zinc on GIZO thin films produced from targets with different compositions: (a) GIZO 2:2:1; (b) GIZO 2:2:2; (c) GIZO 2:4:1 and (d) GIZO 2:4:2. The results were obtained by EDS and XRF for all the compositions and also by XPS for (a), before and after Ar⁺ cleaning.

**Table 4.1** – Relative (Δ₉ₑ) and absolute (Δₐₛ) variations on the atomic concentration of gallium, indium and zinc, compared with the target concentrations. The values were calculated based on the results depicted in fig. 4.7, with EDS and XRF averaged values yielding the atomic concentrations on the thin films.

<table>
<thead>
<tr>
<th>Atomic GIZO composition</th>
<th>In/(In+Zn) (target at%)</th>
<th>Ga/(Ga+Zn) (target at%)</th>
<th>Ga</th>
<th>In</th>
<th>Zn</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Δᵣₑ (%)</td>
<td>Δᵢₛ (%)</td>
<td>Δᵣₑ (%)</td>
</tr>
<tr>
<td>2:2:2</td>
<td>0.50</td>
<td>0.50</td>
<td>+26.1</td>
<td>+8.6</td>
<td>+7.2</td>
</tr>
<tr>
<td>2:4:2</td>
<td>0.67</td>
<td>0.50</td>
<td>+16.4</td>
<td>+4.1</td>
<td>+6.2</td>
</tr>
<tr>
<td>2:2:1</td>
<td>0.67</td>
<td>0.67</td>
<td>+5.5</td>
<td>+2.2</td>
<td>+10.8</td>
</tr>
<tr>
<td>2:4:1</td>
<td>0.80</td>
<td>0.67</td>
<td>+4.5</td>
<td>+1.3</td>
<td>+5.3</td>
</tr>
</tbody>
</table>

- All the target compositions lead to films with a high deficiency on zinc, around 30% relatively to the atomic concentration of this element in the target, being this relative value similar in all the
analyzed compositions. The zinc deficiency on sputtered GIZO films was already reported (although not explained) by different authors to be as high as 40%; [29, 43-46]

- The films having higher absolute deficiency on zinc are the ones richer on this element (2:4:1, 2:2:1, 2:4:2 and 2:2:2, by increasing order, from 4 to 10 % deficiency). This kind of behavior was also observed for indium-doped ZnO films, where the indium deficiency in the films increased for higher indium concentration in the target; [47, 48]

- The loss of zinc is compensated by an increase of indium and gallium, but the definition of a rule that dictates the amount of compensation of each cation is not straightforward, or at least needs some more results to be confirmed;

- For a fixed Ga/(Ga+Zn) ratio (0.50 or 0.67), the relative variations of gallium and indium decrease (i.e., the films’ compositions get closer to the target ones) as the In/(In+Zn) ratio increases. However, while for Ga/(Ga+Zn)=0.50 these relative variations are higher for gallium than for indium, meaning that the zinc deficiency is preferentially compensated by gallium, the opposite happens when Ga/(Ga+Zn)=0.67;

- Finally, for a fixed In/(In+Zn) ratio, smaller variations are obtained for larger Ga/(Ga+Zn) ratios.

Based on the trends given above, the target composition that allows depositing films with the smallest compositional variation is GIZO 2:4:1, for which maximum absolute variations of ≈5 % are obtained.

The reasons for these trends to occur are not completely clear to date, but should mostly be related with target aspects rather than the deposition conditions, since low-to-moderate $P_{rf}$, $p_{dep}$ and $%O_2$ were used to produce the films analyzed above (more details about the effect of deposition conditions on films’ composition are given below). In order to briefly explore this hypothesis, it is important to consider the morphology of a GIZO sputtering target, presented in fig. 4.8 for the 2:2:1 composition.

![Figure 4.8 – SEM image of the surface of a GIZO 2:2:1 ceramic target.](image-url)
The target presents a multitude of phases, such as In$_2$O$_3$, InGaZnO$_4$, In$_2$Ga$_2$ZnO$_7$ and ZnGa$_2$O$_4$, that when summed through the entire target volume yield the target composition. The number and composition of the phases existent on a target depends on multiple factors, such as the target composition and its fabrication process, and for each one of these phases different sputtering yields are expected, not only due to their different compositions, but also due to their diverse crystal structures and variety of binding energies between their composing elements, which have different masses. [10, 11] Then, a complex interdependence between a large number of variables should play a determinant role to define which atoms or aggregates of atoms are preferentially sputtered from the target surface. Additionally, note that single In$_2$O$_3$ phases were detected in all the GIZO target compositions analyzed. Based on the growth rates presented in fig. 4.2a, it is expected that this phase presents a considerably higher sputtering yield than multicomponent phases, which would result in GIZO films with a high excess of indium. However, and even if most of the films are indeed richer in indium than what would be predicted by the target composition, preferential sputtering of this phase will cause a depletion of the target surface region in In$_2$O$_3$, counteracting its high sputtering yield. Nevertheless, this balance doesn’t necessarily imply that a stationary state where the film is sputtered stoichiometrically is achieved, given the intricate interdependence mentioned above. [11]

Still, it seems that a relation exists between the growth rate of indium, gallium and zinc oxides and the effective incorporation of these elements in a GIZO thin film:

- ZnO is the material having the lowest growth rate, hence zinc is the cation always presenting higher deficiency on GIZO films;
- On the other hand, as indium and gallium oxides have higher growth rates, those cations compensate the loss of zinc, but as the gallium concentration on the target increases the zinc substitution is strongly assured by indium, because multicomponent oxides (or alternatively, target phases) with higher gallium contents have lower growth rates.

Figure 4.9 shows that deposition parameters, namely %O$_2$ and $P_{rf}$, can also have some influence on the composition of GIZO films, deposited from GIZO 2:4:1 targets. For $p_{dep}$ and $T_A$, no significant effects were found. Nevertheless, although not studied here, it is noteworthy to mention that considerable desorption/adsorption processes related with H$_2$O, H$_2$ and O$_2$ species may occur depending on the annealing temperature and atmosphere, as observed by Nomura et al. in GIZO films. [49] Regarding fig. 4.9, two extreme cases are presented for %O$_2$ and $P_{rf}$. For %O$_2$, it can be noticed that the larger effect is a decrease on indium, compensated by an increase on gallium and zinc, as %O$_2$ is changed from 0.4 to 10.0 %. Since at higher %O$_2$ highly energetic oxygen ions can severely affect the surface of the growing film, it is possible that indium atoms are preferentially resputtered from the substrate, given their higher sputtering yield. Smaller indium to gallium ratios
with increased $\%O_2$ were also obtained for GIZO films by Suresh et al. [34] Regarding the effect of $P_r$, for films deposited with low $\%O_2$ (0.4 %), the opposite behavior is observed, i.e., for higher $P_r$ the films get richer on indium. In this higher $P_r$ regime and since the variations on this parameter directly affect the sputtering phenomena at the target surface, it is possible that the higher increase on the growth rate of $In_2O_3$ as $P_r$ is increased from 1.1 to 2.7 W cm$^{-2}$ (fig. 4.2c) plays a dominant role, contributing to a higher incorporation of this element in the films. Being the element with the lowest sputtering yield, zinc is the most affected cation by this increase on indium, with its concentration decreasing more than 25 %.

![Figure 4.9](image)

*Figure 4.9 – Atomic concentrations obtained by EDS of gallium, indium and zinc on GIZO thin films produced from a GIZO 2:4:1 target under different $\%O_2$ and $P_r$, annealed at 500 °C.*

From fig. 4.9 it can also be inferred that low $\%O_2$ and low $P_r$ lead to films with compositions closer to the target composition, which can be an indicative that a more ideal sputtering process occurs under these conditions. In fact, as will be seen in the next section, these are the conditions generally leading to the best electrical performance and stability.

Even if in this section it was shown that the composition of the oxide semiconductor films can deviate from the ones of the targets, for simplicity in the following sections and chapters these films will be designated by the composition of the ceramic targets used to deposit them.

### 4.1.5. Electrical properties

Since the main focus of this work was on the integration of oxide semiconductors as active layers of TFTs, the study of the electrical properties of these materials, including their dependence on the (post-)processing conditions and composition as well as their stability, is naturally one of the most important topics to be addressed. Data is presented and discussed both for polycrystalline and amorphous oxides, with the latter assuming particular relevance, as they constitute the most innovative area explored during this work.
4. Properties of n-type oxide semiconductor and high-κ dielectric thin films produced by sputtering

4.1. Dependence of the electrical properties on the deposition and post-deposition parameters

4.1.5. Percentage of oxygen content in the Ar+O2 mixture (%O2)

Besides doping, oxygen vacancies derived from stoichiometry deviations on the deposited films are the main contributors for electrical conduction in oxides. These oxygen vacancies form shallow electron donor levels close to the conduction band and are readily ionized near room temperature, with each doubly charged oxygen vacancy contributing two free electrons, preserving charge neutrality. [16, 50-52] Hence, the variation of %O2 is one of the most effective ways to control the electrical properties of oxide semiconductors. Figure 4.10 shows the ρ dependence on %O2 for a polycrystalline and an amorphous material, ZnO (fig. 4.10a) and GIZO 2:4:1 (fig. 4.10b), respectively.

Figure 4.10 – Effect of %O2 on ρ for different oxide semiconductors: (a) ZnO; (b) GIZO 2:4:1. Samples annealed with Tₐ ranging from 150 to 500 °C.

For both cases, the main trend is for ρ to increase with %O2, which is consistent with the introductory idea given above, since the additional oxygen atoms supplied using a higher %O2 can be incorporated in the film, filling the high number of oxygen vacancies that are created on films sputtered in a pure argon atmosphere. This is clearly visible for films annealed at lower temperatures, such as 150 °C (fig. 4.10b), for which ρ increases more than 6 orders of magnitude by changing %O2 from 0 to 10.0 %. The highest ρ variation occurs for %O2 between 0 and 1.8 %, and although some oxygen vacancies may still be compensated above this %O2 value, the increase on ρ between 1.8 and 10.0 %O2 can also be attributed to a different mechanism: for high %O2 the intense substrate bombardment by highly energetic oxygen ions can cause considerable resputtering of the deposited film, inducing structural defects on its growing surface, raising the film’s ρ. The bombardment effect was found to be of extreme relevance on sputtered films by different authors. [1, 9, 22, 53, 54] Additionally, since the growth rate decreases so drastically for %O2=10.0 %, regardless of the target/film composition (fig.

Note that for ZnO these values are not presented, as it was not possible to measure them using the 4 point probe setup, due to their high ρ. Based on the specifications of the semiconductor parameter analyzer and on the sample geometry, a ρ value higher than 10⁸ Ω cm is expected for these highly-resistive samples.
4.2a), it is also proposed that for this value of %O₂ the films’ compactness is affected, which may also contribute to the increase of ρ. Experimental evidence of this will be shown in section 4.1.6, using spectroscopic ellipsometry data. Another factor that can contribute to the increased ρ with %O₂ in GIZO films is the reduction of the indium content of the films when high %O₂ is used, in agreement with fig. 4.9. As will be shown in this chapter, (G)IZO films with lower indium content have higher ρ. Another important aspect shown in fig. 4.10 is that the increase of TA tends to decrease the films’ ρ and also the influence that %O₂ has on it, although the main ρ-%O₂ trend described above is still verified (a dedicated section about the effect of TA can be found in p. 103). For instance, with GIZO 2:4:1 annealed at 300 °C, ρ increases less than 2 orders of magnitude within the studied %O₂ range, against more than 6 orders at 150 °C, and at 500 °C the ρ variation is even smaller. However, for ZnO films annealed at 300 °C the increase of ρ with %O₂ is still quite significant, even if in this case %O₂ is only increased up to 1.0 %. This should primarily be related with the polycrystalline structure of the material and the consequent existence of grain boundaries, which act like preferential paths for absorption/desorption of elements to/from the film, such as oxygen atoms. Another important factor that could justify the high ρ of ZnO films with %O₂=1.0 %, even when annealed at 300 °C, is the higher sensitivity of this oxide to the bombardment by highly energetic particles, such as oxygen ions. This effect can lead to the creation of defects on the films, like crystallographic damage and internal stress, raising ρ. [1, 2, 53] Nevertheless, after annealing at 500 °C, grain size gets larger and the additional energy supplied by the increased TA should allow to attenuate the effect of the oxygen bombardment damage, which is reflected in a considerably lower influence of %O₂ on ρ.

It is also important to analyze the effect of %O₂ on other electrical parameters directly related with ρ, namely carrier concentration (N) and mobility (μ). Although the films whose results are discussed in fig. 4.10 were not measurable with the hall effect system for all the range of %O₂, due to their high ρ, low N and μ (at least the ones annealed at 150 °C, where the %O₂ effect dominates the films’ properties), by using films produced under similar processing conditions but with a different target composition, such as IZO 2:1, consistent hall effect measurements were obtained. The results achieved for this multicomponent amorphous oxide are presented in fig. 4.11. First, as already seen in fig. 4.10, ρ increases with %O₂, although here both the absolute ρ values and their modulation with %O₂ are considerably smaller than for GIZO 2:4:1. This is expectable since GIZO has one more cation than IZO and so, assuming similar conduction mechanisms for both materials, GIZO is able to incorporate more oxygen in its structure. Furthermore, gallium creates stronger bonds with oxygen than indium or zinc due to its high ionic potential (+3 valence and small ionic radius), which greatly contributes to a higher ρ of GIZO. [55] More details about the effects of composition on the electrical properties of oxide semiconductors are given in p. 101. The increase of ρ with %O₂ is accompanied by a decrease of N, reinforcing the idea that free electrons originate essentially from oxygen vacancies.
Other important aspect of fig. 4.11 is that \( \mu \) decreases as \( N \) decreases (\%O\(_2\) increases), at least for \( N>10^{18} \) cm\(^{-3}\). This trend, which is opposite to the verified for conventional crystalline semiconductors where carrier scattering with dopant ions controls \( \mu \), is attributed to the different conduction mechanisms of oxides. On these oxides, there is a random distribution of metallic cations around the conduction band edge, so charge transport gets more efficient (i.e., \( \mu \) increases) for higher \( N \), because the extra carriers allow the Fermi level \( (E_F) \) to surpass the potential barriers derived from the structural randomness. This \( \mu-N \) tendency and its magnitude are naturally dependent on the considered \( N \) range, and consequently on the processing parameters and target composition, but a clear inversion is only observed for very high \( N \), above \( 10^{20} \) cm\(^{-3}\), where ionized impurity scattering becomes relevant (conduction mechanisms and their dependence on \( N \) are discussed on section 4.1.5.2).

![Graph](image-url)

Figure 4.11 – Effect of \%O\(_2\) on \( \rho \), \( N \) and \( \mu \) for IZO 2:1 thin films annealed at 150 °C.

Note that the IZO films presented in fig. 4.11 are theoretically not ideal for the application as channel layers on TFTs, because they invariably result in high \( N \) and low \( \rho \) films, which compromise the Off-state of the devices. Nevertheless, it will be shown that these materials can be tuned for TFT application by adjusting other parameters, such as their thickness and/or their annealing temperature. Furthermore, the effect of \%O\(_2\) was tested for other target compositions and other fixed processing parameters \( (p_{\text{sep}} \text{ and } P_{\text{rf}}) \), and the trends described above were verified for most of the cases, with only the magnitudes and absolute values presenting significant changes. So, the analysis of these IZO films can provide a valid tool to understand the effect of \%O\(_2\) on multicomponent oxide semiconductors.

Given this, for the application as channel layer of TFTs, optimal \%O\(_2\) is generally found to be between 0.4 and 1.0 %: this way, the high oxygen deficiency of films sputtered without oxygen can be compensated, which would otherwise result in “always-on” devices, hard to switch-off with reasonable \( V_{\text{th}} \) values; on the other hand, this moderate \%O\(_2\) prevents the severe substrate
bombardment effects that occur for high %O_2, which could result in a highly defective semiconductor material and unstable/poorly performing transistors.

4.1.5.1.2. Deposition pressure ($p_{\text{dep}}$) and rf power density ($P_{\text{rf}}$)

The effect of $p_{\text{dep}}$ and $P_{\text{rf}}$ on the electrical properties of the sputtered films is somehow related, given that both directly affect the energy of sputtered and plasma species arriving the substrate. Low $p_{\text{dep}}$ and moderate-to-high $P_{\text{rf}}$ contribute to the ballistic plasma transport regime, [40] which is generally employed to process TCOs. [8, 56] Under this regime, it is reported that doped ZnO and doped In_2O_3 films exhibit denser structures, higher N and improved crystallinity, which favors their electrical properties for application as transparent electrodes. However, the optimization work developed here pursued a different objective, which was to obtain oxide semiconductors with moderate-to-high $\rho$.

To achieve this, $p_{\text{dep}}$ and $P_{\text{rf}}$ effects were studied.

Figure 4.12 shows how $p_{\text{dep}}$ and $P_{\text{rf}}$ affect $\rho$ on ZnO films, annealed at 300 and 500 °C.\(^d\)

![Figure 4.12](image)

*Figure 4.12 – Effect of (a) $p_{\text{dep}}$ and (b) $P_{\text{rf}}$ on $\rho$ for ZnO thin films annealed at 300 and 500 °C.*

Concerning $p_{\text{dep}}$ (fig. 4.12a), the 300 °C films are a clear example of the high sensitivity of ZnO’s growing surface to the substrate bombardment effects. For low $p_{\text{dep}}$ (0.4 Pa) the films should be severely affected by the ion bombardment effects due to the high energy of the species arriving to the substrate, such as high-energy argon neutrals recoiled from the target or high-energy negative oxygen ions accelerated in the cathode sheath toward the growing film surface. [57] The high energetic bombardment can be reflected in several structural and even compositional changes, due to phenomena such as resputtering of atoms from previously grown layers, creation of defects and internal stress, all possibly contributing to raise $\rho$. For instance, it is well known that structural defects in ZnO films, such as oxygen vacancies, which generally introduce shallow donor levels, may

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\(^d\) Films annealed at lower $T_a$ are highly resistive, see note c.
also introduce deep energy levels within the bandgap, trapping electrons and degrading $\rho$. [58, 59] On the other hand, for $\rho_{\text{dep}}=1.0$ Pa, the bombardment effects should be suppressed, as all the species suffer more collisions inside the plasma before reaching the substrate. However, given the low energy of those species when arriving at the substrate, less compact films with lower crystalline quality are created, which contributes to an increase of $\rho$. An equilibrium between these two extreme situations is found for $\rho_{\text{dep}}=0.7$ Pa, which is close to the $\rho_{\text{dep}}$ value reported by Meng et al. for sputtered ZnO films with enhanced homogeneity and crystallinity. [60] The same trend is seen for the 500 °C annealed films, but the magnitude of $\rho$ variation is much smaller at this temperature (like was verified for %O$_2$), specially for films deposited below $\rho_{\text{dep}}=0.7$ Pa. Reduction of compressive stress might be a plausible reason for this, as verified by other authors for ZnO films annealed between 400-500 °C. [61, 62]

Substrate bombardment should also be the main factor determining the $\rho$ differences found on 300 °C annealed ZnO films deposited with different $P_{\text{rf}}$ (fig. 4.12b): as $P_{\text{rf}}$ increases, O` ions get more energetic, increasing resputtering [1] and other bombardment related effects, leading to higher $\rho$. Again, after annealing at 500 °C, these effects are attenuated, resulting in lower $\rho$ and negligible dependence of it on $P_{\text{rf}}$.

The electrical properties of multicomponent oxides present different dependences on $\rho_{\text{dep}}$ and $P_{\text{rf}}$ than the ones exhibited by ZnO. Typical examples are presented in fig. 4.13a and 4.13b for GIZO 2:4:1 and IZO 2:1 films, respectively.

![Figure 4.13](image)

**Figure 4.13** – Effect of (a) $\rho_{\text{dep}}$ and (b) $P_{\text{rf}}$ on $\rho$ for GIZO 2:4:1 and IZO 2:1 thin films annealed at $T_A$ ranging from 150 to 500 °C.

For GIZO, contrarily to ZnO, $\rho_{\text{dep}}=0.4$ Pa leads to the most conductive films. This is tentatively attributed to a considerable lower effect of sputtering induced damage on GIZO than on ZnO. In fact, Sasabayashi et al. showed that amorphous IZO films present considerably less internal stress than polycrystalline oxides such as ITO, processed under similar conditions. [57] Hence, for low $\rho_{\text{dep}}$ it is
believed that the higher energy of the sputtered species arriving at the substrate allows them to increase the mobility of other particles present on the substrate by momentum transfer, allowing them to reach equilibrium sites within the film structure, forming a more dense and defect free film with low $\rho$. [12, 43, 63] The fact that $\rho$ is maintained almost unchanged between 0.7 and 1.0 Pa might be explained by a combination of two factors: first, as noted above, it is expected that films deposited with higher $p_{\text{dep}}$ have a less compact structure, which would contribute to increase $\rho$; on the other hand, as $p_{\text{dep}}$ increases, the surface mobility of the species that reach the substrate is lower, due to the higher number of collisions that they suffer inside the chamber. The lack of surface mobility reduces the chances of species being oxidized close to the substrate with previously adsorbed oxygen atoms, [2] which would contribute to a decrease of $\rho$. As happens with ZnO, the increase of $T_A$ decreases the discrepancies among the properties of the films deposited at different $p_{\text{dep}}$, essentially due to oxidation (see next paragraph) and densification of the low $p_{\text{dep}}$ and high $p_{\text{dep}}$ films, respectively.

Similar effects to the ones verified for low $p_{\text{dep}}$ are expected for films deposited with higher $P_{\text{rf}}$. Furthermore, in agreement with fig. 4.9 regarding compositional analysis of GIZO films, it is expected that higher $P_{\text{rf}}$ leads to films with increased indium content, which may also contribute to a reduced $\rho$ (see also section 4.1.5.1.3). Still, an additional mechanism responsible for the considerable decrease of $\rho$ between $P_{\text{rf}}$=1.1 and 2.7 W cm$^{-2}$ and $p_{\text{dep}}$=0.7 and 0.4 Pa is proposed: as more species are sputtered from the target (higher $P_{\text{rf}}$) and/or move in the plasma subjected to less scattering (lower $p_{\text{dep}}$), more oxygen is needed to oxidize them when reaching the substrate and also to reoxidize the target surface, which easily gets reduced during the sputtering process. Given that low $\%$O$_2$ is used on this study, the overall oxygen concentration may not be enough to accomplish all the required oxidation processes, resulting in a higher number of oxygen vacancies in the film, thus higher $N$ and lower $\rho$. For sputtering processes using metallic targets different authors observed that as $P_{\text{rf}}$ increases and $p_{\text{dep}}$ decreases, more oxygen was required to completely oxidize the sputtered films. [3, 12, 37] These results can also be extended to ceramic targets, since both metal-oxide and metal atoms or aggregates are sputtered from the targets’ surface and these species can suffer further dissociation inside the plasma. Chiang et al. also observed higher $N$ for GIZO films deposited with higher $P_{\text{rf}}$. [64] The high oxygen deficiency of the (G)IZO films deposited with high $P_{\text{rf}}$/low $p_{\text{dep}}$ would justify the increase on $\rho$ (decrease on $N$) verified as $T_A$ increases to 300 °C. Further considerations about annealing are done in a dedicated section on p. 103.

Even if low $p_{\text{dep}}$ and moderate-to-high $P_{\text{rf}}$ generally lead to highly conducting films, very high $\rho$ can also be achieved under these conditions, but using a high $\%$O$_2$. For instance, for films annealed at 150 °C, sputtered from GIZO 2:4:2 targets with $p_{\text{dep}}$=0.4 Pa, $P_{\text{rf}}$=2.7 W cm$^{-2}$ and $\%$O$_2$=10.0 %, $\rho>$10$^8$ Ω cm is achieved, which is at least 11 orders of magnitude higher than the value obtained for films produced
with $p_{\text{dep}}=0.4$ Pa, $P_{\text{rf}}=1.1$ W cm$^{-2}$ and $\%O_2=0.4\%$. Besides showing that the final properties of a thin-film can be modulated by changing deposition parameters in different ways, this result turns clear that, for the range of $\%O_2$, $p_{\text{dep}}$ and $P_{\text{rf}}$ studied here, $\%O_2$ is the parameter having the most significant effect on the definition of the final properties of the sputtered films. Based on this, for the $\%O_2$ adopted as optimal for this work (between 0.4 and 1.0%), $p_{\text{dep}}=0.7$ Pa and $P_{\text{rf}}=1.1$ W cm$^{-2}$ are the conditions leading to the best equilibrium between good compactness and controllable $\rho$. In addition, these are also the conditions leading to less variation of electrical properties with annealing temperatures up to 300 °C.

4.1.5.1.3. Composition (binary and multicomponent oxides)

During the analysis presented in this chapter several aspects were already mentioned regarding the effect that the different compositions have on the electrical properties of the resulting films. This section comprises a more detailed overview regarding compositional-electrical dependences, namely the effect of the different cationic concentrations on the electrical performance of multicomponent oxide films. Figure 4.14a shows the dependence of $\rho$ on composition for films with different $\text{In/(In+Zn)}$ and $\text{In/(In+Ga)}$ atomic ratios, annealed at 300 and 500 °C and deposited under the same conditions ($\%O_2=0.4\%$, $p_{\text{dep}}=0.7$ Pa and $P_{\text{rf}}=1.1$ W cm$^{-2}$). For the films annealed at 500 °C, the trends of $\mu$ and $N$ on the gallium-indium-zinc oxide system can be seen in fig. 4.14b.

![Figure 4.14](image.png)

**Figure 4.14** – Effect of target composition on the electrical properties of oxide semiconductor thin films produced under the same deposition conditions: (a) Effect of $\text{In/(In+Zn)}$ and $\text{In/(In+Ga)}$ atomic ratios on $\rho$, for $T_a=300$ and 500 °C; (b) Ternary diagram for gallium-indium-zinc oxide system, showing $\mu$ and $N$ of films annealed at 500 °C. The red and yellow symbols denote amorphous and polycrystalline films, respectively.

*Although it was already shown that larger dependence of the electrical properties on the processing parameters is verified for films annealed at lower $T_a$, 300 and 500 °C films are presented on these figures as they allow to have a larger number of measurable films, hence a clearer relation between composition and electrical properties. Despite this, note that for the films measurable with lower $T_a$, the trends described for 300 and 500 °C are also verified, but with even larger magnitudes.*
Several conclusions can be drawn from these figures:

- Comparing the binary oxides, ZnO and In$_2$O$_3$, the latter presents considerably lower $\rho$, which should be ascribed with the larger orbitals of indium (5s) than zinc (4s) and also with the larger grain sizes of In$_2$O$_3$. Still, these advantages of In$_2$O$_3$ should be attenuated by the higher metal number density and shorter metal-metal distances of ZnO. [40] For Ga$_2$O$_3$ (not shown) produced under these deposition conditions highly resistive films are always obtained (>10$^8$ $\Omega$ cm), even after a 500 °C annealing. This should be related with the already mentioned higher ionic potential of gallium when compared with indium or zinc, which is responsible for strong bonds between gallium and oxygen, thus Ga$_2$O$_3$ films should always be nearly stoichiometric, without considerable concentration of oxygen vacancies;

- For the multicomponent oxides, the general trend is for $\rho$ to decrease as the In/(In+Zn) atomic ratio is increased. This is in agreement with the fact that the In$_2$O$_3$ films present a considerably lower $\rho$ (higher $N$ and $\mu$) than ZnO films, with the multicomponent oxides reflecting this to an extent dependent on the relative concentrations of indium and zinc. Additionally, when comparing films without gallium with In/(In+Zn)=0.80 and 1.00 (i.e. IZO and pure In$_2$O$_3$ films), $\rho$ is higher for the latter, which is attributed to the polycrystalline structure of In$_2$O$_3$, where grain boundaries trap the free carriers, increasing the potential barriers between the grains and degrading carrier transport; [2]

- The dependence of multicomponent oxide films on the gallium content follows a similar trend to the one described above for zinc, i.e., higher gallium contents (lower In/(In+Ga)) result in films with higher $\rho$. However, as Ga$_2$O$_3$ has an even higher $\rho$ than ZnO, the effect of adding gallium to multicomponent films based on In$_2$O$_3$ is even higher than the effect of adding zinc, i.e., $\rho$ is more affected by In/(In+Ga) than by In/(In+Zn) atomic ratio. This is also clearly visible on the ternary diagram of fig. 4.14b, where for amorphous (G)IZO films $\mu$ and $N$ are more affected (decreased) by gallium than by zinc addition. The increase of $\rho$ with the added gallium content is even more significant for the indium-poorer films (GIZO 2:2:2), since for this composition the zinc deficiency in the films is mainly compensated by gallium (see p. 91). Furthermore, contrarily to what happens for films without gallium, when In/(In+Ga)=0.67 $\rho$ decreases for all the range of In/(In+Zn), since the films always remain amorphous, even when no zinc exists in the structure (i.e., In/(In+Zn)=1.00);

- The trends described in the last points for multicomponent oxides only fail for the 500 °C IZO 4:1 (In/(In+Zn)=0.80) film, because crystallization occurs for this composition at this $T$ (fig 4.3c). As stated above, crystallization leads to trapping of free carriers at the grain boundaries, decreasing $N$ and $\mu$ and increasing $\rho$. In fact, for films annealed at 500 °C, it can be seen in fig. 4.14a that IZO
4.1.5.1.4. Annealing temperature \( (T_a) \)

The effect of \( T_a \) on the electrical properties of oxide semiconductors was already mentioned in different sections of this chapter. What was verified until now was essentially that, depending on the deposition conditions and target compositions, increasing \( T_a \) increases or decreases \( \rho \) with different magnitudes and attenuates the differences between the electrical properties of films produced under different conditions and/or compositions. Since all the annealing treatments were done in air,
increased adsorption or desorption of oxygen is expected to happen as \( T_A \) gets higher. Whether incorporation or removal of oxygen on the films’ structure happens, mostly depends on the relation between the oxygen concentration in the annealing atmosphere and in the films: for instance, for polycrystalline materials, it is reported that the concentration of oxygen states at the grain boundaries (the preferential paths for impurities diffusion) relatively to the ambient oxygen pressure over the film determines whether adsorption or desorption takes place to reach an equilibrium state. [3] Although no grain boundaries exist in amorphous multicomponent oxides, their surfaces also strongly interact with the surrounding atmosphere even at room temperature, either by physisorption, chemisorption or desorption processes. [65, 66] Given that the properties of oxide semiconductors strongly depend on their oxygen deficiency/excess, it is not strange that they are significantly affected by these annealing treatments. Besides the oxygen concentration changes, annealing can also promote structural rearrangement and reduce the internal stress effects of the films. [57, 67, 68] Furthermore, as presented before, annealing can also lead to the crystallization of as-deposited amorphous structures or to the improvement of the crystalline quality of as-deposited polycrystalline materials, which naturally also affects the electrical properties.

Figure 4.15 illustrates the different effects that \( T_A \) between 150 and 500 °C has on IZO 2:1 films produced with different \( \%O_2 \) (fig. 4.15a) and \( p_{\text{dep}} \) (fig. 4.15b). \( N \) variation is chosen for these plots, as it should be the electrical parameter more directly related with the oxygen content of the films, since in undoped oxide semiconductors the free carriers mostly derive from oxygen vacancies. Note that these films remain amorphous for all the range of analyzed temperatures.

Concerning the \( \%O_2 \) dependence, three different behaviors can be clearly seen as \( T_A \) increases from 150 to 300 °C:

- \( N \) decreases for films deposited in pure argon atmosphere (\( \%O_2=0 \% \)), since oxygen adsorption should take place to compensate the high deficiency of this element on the films;
• $N$ increases for films deposited with $\%O_2 \geq 1.0 \%$, which could be attributed not only to oxygen desorption due to the high oxygen concentration in the film relatively to the annealing atmosphere, but also to structural relaxation, as films deposited with higher $\%O_2$ should be more prone to bombardment effects, specially when produced with $\%O_2=10.0 \%$;

• $N$ doesn’t present a significant variation for $\%O_2=0.4 \%$, meaning that a better equilibrium between oxygen concentration in the films and in the atmosphere should exist right from $150 \, ^\circ\text{C}$ and also that the films should be structurally more stable.

If $T_a$ is increased to $500 \, ^\circ\text{C}$, $N$ increases for all the films. For this temperature, the oxygen content of the films should be in equilibrium with the annealing atmosphere and a better structural arrangement between indium, zinc and oxygen atoms should be obtained for all the range of $\%O_2$, but still preserving for all the cases an amorphous structure. Hence, all the films present very similar electrical properties at $500 \, ^\circ\text{C}$.

The same kind of $N$ evolution with $T_a$ is verified for films deposited with different $p_{\text{dep}}$ (fig. 4.15b): for films initially with high oxygen deficiency ($p_{\text{dep}}=0.4 \, \text{Pa}$) and consequently high $N$, $N$ decreases until $300 \, ^\circ\text{C}$, while the opposite happens for films deposited at high $p_{\text{dep}}$ (1.0 Pa), which can also be attributed to a better densification of these films. Intermediate $p_{\text{dep}}$ (0.7 Pa) allows to obtain the most stable films. Again, when annealed at $500 \, ^\circ\text{C}$, $N$ increases for all the analyzed $p_{\text{dep}}$. Similar trends with $T_a$ are also observed for films produced with different $P_{\text{rf}}$ (see, for instance, the evolution of $\rho$ for IZO 2:1 films, presented in fig. 4.13b). These effects were observed for all the studied multicomponent oxides, to an extent essentially dependent on the intrinsic $\rho$ and $N$ provided by the target compositions, being the compositions with higher $\rho$ and lower $N$ the ones presenting the larger variations with $T_a$. This should be expected, as for materials with lower $N \, E_f$ moves away from the conduction band towards the midgap. Thus, the electronic properties start to be more dependent on the defect levels contained into the bandgap, namely tail states, which arise from heavily distorted indium-oxygen-metal bonds and random distribution of the cations, or oxygen vacancies that can trap electrons to form fully occupied deep states. [46, 67, 69]

It is also interesting to note that the deposition conditions generally providing the best compromise in terms of electrical performance, i.e. $\%O_2$ between 0.4 and 1.0 $\%$, $p_{\text{dep}}=0.7 \, \text{Pa}$ and $P_{\text{rf}}=1.1 \, \text{W cm}^{-2}$, are also the ones leading to smaller $T_a$ effects. However, for the production of oxide semiconductors intended to be used as highly conducting electrodes (TCOs), which are also vital components of a transparent TFT, different processing conditions need typically to be employed, to assure the lowest possible $\rho$ without severely compromising the transparency. To achieve this sort of properties, films are usually grown under a ballistic transport plasma regime, i.e., with high $P_{\text{rf}}$ and low $p_{\text{dep}}$. [40] Figure 4.16 shows the effect of $T_a$ on such films, produced from an IZO 5:1 target.
As-deposited films exhibit the lowest $\rho$ and the highest $N$ and $\mu$ presented so far on this dissertation, clearly showing that these deposition conditions and target composition are optimized to obtain films to be used as electrodes. Note also that the achievement of these properties corroborates well with the results previously presented on this chapter, as it was seen that low $\rho_{\text{dep}}$, high $P_r$, and high indium concentration are key factors to obtain the lowest $\rho$ and higher $N$ in multicomponent oxides. Given the high oxygen deficiency of the films, as $T_A$ increases oxidation takes place and less oxygen vacancies are available, which increases $\rho$ and decreases $N$. Concerning $\mu$, it assumes a different relation with $N$ than the one previously verified for the multicomponent oxides, i.e. $\mu$ increases as $N$ decreases. This is attributed to the different $N$ range of these films: for IZO, it is reported that ionized impurity scattering starts to dominate carrier transport when $N$ is above $10^{20} \text{ cm}^{-3}$. [70] Hence, for the $N$ range of the IZO films presented in fig. 4.16, $E_r$ is well above the CBM and enhanced carrier transport (higher $\mu$) starts to be achieved for lower $N$, since less scattering centers derived from the ionization of native point defects affect the movement of carriers. [24, 71] Additionally, $\mu$ can also be increased due to the better structural rearrangement of the amorphous structure as $T_A$ increases. This is even more plausible considering the low $\rho_{\text{dep}}$ and high $P_r$ used here, which can lead to more significant film bombardment effects, although it was already shown that multicomponent oxides seem to be considerably less sensitive to these effects than ZnO (see p. 99). For the highest $T_A$ analyzed here (500 °C), all the electrical properties are deteriorated ($\mu$ and $N$ decrease, $\rho$ increases) regarding the application of this material as a transparent electrode, similarly to what was reported by other authors for IZO 5:1 films. [15, 68, 72] Several phenomena can justify this result:

- The crystallization of the film. When this happens, potential barriers associated with charge trapping and scattering effects at the grain boundaries start to be relevant, resulting in lower $\mu$.

[3] This is even more critical for materials with low crystallite size, which is the case of IZO.
annealed at this temperature, since the created depletion regions can easily overlap in adjacent grains, degrading charge transport. Nevertheless, as the material has still a relatively high $N$, above $10^{19}$ cm$^{-3}$, the grain boundary regions should only be partially depleted, so their negative effect on charge transport may be less severe; [73]

- The grain boundaries constitute preferential paths for oxygen to penetrate in the film, increasing the oxygen concentration in the film, which is reflected in higher $\rho$ and lower $N$. Furthermore, this oxygen diffusion process modulates the inter-grain boundary barrier height, affecting $\mu$; [74]
- As $N$ is now smaller than for the films annealed at lower temperatures, the degenerated ionized impurity scattering mechanism, dominant for higher $N$, may now be replaced by a mechanism where the electronic transport is affected by the random distribution of zinc cations around the more ordered indium cations that primarily compose the CBM (note that IZO crystallizes according to the In$_2$O$_3$ system), which together with the grain boundaries create potential barriers around the conduction band edge. [75] This leads to a lower $\mu$ than for films annealed at 300 °C, where higher $N$ and amorphous structures are obtained.

Although amorphous oxides have a large number of advantages when compared with polycrystalline oxides regarding their application as channel layers on TFTs, it is also interesting to investigate how the electrical properties of as-grown polycrystalline materials (or at least crystallized at very low temperature) are affected when subjected to different $T_A$. Figure 4.17 shows the hall-effect data obtained for In$_2$O$_3$ films annealed up to 500 °C.

![Figure 4.17 – Effect of $T_A$ on $\rho$, $\mu$ and $N$ for In$_2$O$_3$ thin films produced using the same deposition conditions.](image)

For the non-annealed films, which present an amorphous structure and high oxygen deficiency, large $\mu$ and $N$ and small $\rho$ are obtained. However, as the films are annealed at 150 °C, crystallization starts to occur and the existence of grain boundaries facilitates film’s oxidation. Due to this, $\mu$ and $N$ sharply decrease and $\rho$ increases. Above this $T_A$, the films cannot achieve the initial electrical properties anymore, as the charge transport starts to be limited by the existence of grain boundaries. When
compared with the crystalline IZO films discussed in fig. 4.16, the effect of grain boundaries should in principle be more relevant here, as $N$ is considerably lower, so wider depletion regions may be expected. However, this effect is counterbalanced by the increased grain sizes of In$_2$O$_3$ when compared with IZO films, which favors intra-grain dominated charge transport. [76] Hence, for the higher $T_A$, when the films are polycrystalline, a combination of two factors should be considered: the increase of the grain size and overall crystalline quality and the adsorption/desorption of oxygen from the grain boundaries, which change the potential barrier height at the grain boundaries, governing the electrical performance of the films. [3] For the crystallized films, $\mu$ varies inversely with $N$, meaning that a non-degenerate ionized impurity scattering mechanism, derived from the ionization of oxygen vacancies or interstitial indium atoms, should also have particular relevance. This will be further explored in the next section.

Regarding fig. 4.17, it’s also inevitable its comparison with the results obtained for ZnO and Ga$_2$O$_3$, the other binary compounds studied herein. Although hall-effect measurements were not possible on ZnO films, $\rho$ variation with $T_A$ was opposite to the verified for In$_2$O$_3$ and of much larger magnitude, even if the as-deposited films are already polycrystalline: for ZnO, $\rho$ decreases from $>10^8$ $\Omega$ cm (as-deposited) down to $10^3$ $\Omega$ cm (500 °C), for films produced under the same deposition conditions as the In$_2$O$_3$ films discussed in fig. 4.17. For Ga$_2$O$_3$ films, even after annealed at 500 °C, $\rho$ was still non-measurable. This result, together with the compositional dependence on the electrical properties of the oxide semiconductors presented in p. 101, makes understandable that the multicomponent oxides based on In$_2$O$_3$ present different variations with $T_A$ depending on their composition, with films with larger zinc and mainly gallium contents being more sensitive to $T_A$ (fig. 4.18). In addition, even if the (G)IZO films are amorphous at $T_A=500$ °C, it should be plausible to assume that some In$_2$O$_3$-rich agglomerates start to be formed at this $T_A$ (given that In$_2$O$_3$ is always the first phase to crystallize for the films analyzed here), contributing to the large reduction of $\rho$ at $T_A=500$ °C verified not only in fig. 4.18 but also in previously presented data, such as in figs. 4.10b, 4.13b and 4.14a.

![Figure 4.18 – Effect of $T_A$ on $\rho$ for In$_2$O$_3$ IZO 4:1 and GIZO 2:4:1 thin films produced using the same deposition conditions.](image)

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4.1.5.2. Additional considerations about the conduction mechanisms in oxide semiconductors

The composition and the conditions under which the oxide semiconductor films are prepared have a significant effect on their electrical properties, as shown before. In addition, some brief discussions were already made regarding the mechanisms possibly affecting charge transport in oxide semiconductors, both in amorphous and polycrystalline films. In this section a larger quantity of experimental data is compiled to discuss the relevant conduction mechanisms in more detail.

4.1.5.2.1. Dependence of ρ and µ on N

As $E_F$ is shifted inside the bandgap depending on the value of $N$ (or even above the conduction band edge if degeneracy is obtained), it is not strange that other electrical parameters such as $\rho$ or $\mu$ show a marked dependence on $N$. Figure 4.19 shows these relations, for binary and multicomponent oxide films deposited with different conditions and target compositions, with $T_A=150$ and 500 °C.

![Graphs showing the dependence of $\rho$ and $\mu$ on $N$ for oxide semiconductor thin films](image)

*Figure 4.19 – Dependence of $\rho$ and $\mu$ on $N$ for oxide semiconductor thin films produced under different deposition conditions, using different target compositions and annealed at 150 and 500 °C. Each symbol represents a specific target composition. (a) $\rho(N)$, $T_A=150$ °C; (b) $\rho(N)$, $T_A=500$ °C; (c) $\mu(N)$, $T_A=150$ °C; (d) $\mu(N)$, $T_A=500$ °C.*
As seen in fig. 4.19a and 4.19b, \( \rho \) sharply decreases with \( N \), following a linear relationship in a double logarithmic plot. This trend is not surprising, since \( \rho \) in oxide semiconductors directly decreases with the concentration of intrinsic donors originated from lattice defects – such as oxygen vacancies or metal atoms on interstitial lattice sites – or with the introduction of extrinsic dopants with different oxidation numbers than the atoms of the host lattice. [77] Hence, the \( \rho-N \) relation found for the analyzed oxide semiconductors reinforces the idea that these materials behave as impurity semiconductors, where the intrinsic or extrinsic impurities create donor or acceptor levels that control the obtainable electrical properties. Similar trends can be found on the literature for intentionally doped and undoped oxides, based on ZnO and In\(_2\)O\(_3\), for different ranges of \( N \). [19, 51, 77] Although this is the main idea instantaneously given by these plots, some considerations regarding the actual data deviations from the ideal \( \rho-N \) linear relation are important to consider:

- For very high \( N \), close to \( 10^{21} \, \text{cm}^{-3} \), \( \rho \) doesn’t decrease anymore with \( N \), since a degenerated ionized impurity scattering mechanism starts to dominate the transport properties. This is turned even clearer by inspecting fig. 4.19c and 4.19d, where it can be seen that \( \mu \) is significantly decreased for films with such a high \( N \). As pointed out earlier, ionized impurity scattering should be dominant for this \( N \) range, since the large number of scattering centers generate an electrostatic field that remains effective for large distances, deflecting the charge carriers; [3]

- The as-deposited polycrystalline material data presented on these plots, relative to gallium-doped ZnO (5 wt% of gallium, denoted GZO) films, deviates from the linear \( \rho-N \) relation followed by the amorphous multicomponent oxides, following instead a parallel shifted \( \rho-N \) line, both for 150 and 500 °C annealed films. Similar splits are found on literature for single-crystalline and polycrystalline ZnO films, for \( N=10^{18} \, \text{cm}^{-3} \), with the latter exhibiting larger \( \rho \) due to the effect of grain boundaries. [77] However, when \( N>10^{20} \, \text{cm}^{-3} \), which is the \( N \) range where most of the oxide semiconductors are optimized for the application as transparent electrodes, even the data of polycrystalline and single-crystalline structures merge into one single line, since the depletion regions associated with the grain boundaries at this \( N \) range are so narrow that the electrons are able to tunnel through the barriers, so charge transport is mostly dominated by scattering at ionized impurities. [8, 77] On the other hand, when comparing \( \rho \) values for polycrystalline and amorphous In\(_2\)O\(_3\) films, both with \( N>10^{20} \, \text{cm}^{-3} \), Nakazawa et al. obtained two parallel \( \rho-N \) lines, with amorphous films exhibiting higher \( \rho \) for a given \( N \). [19] The authors attributed this to the different states of structural defects of both types of films. Given this background, the higher \( \rho \) values obtained here for polycrystalline ZGO films when compared with amorphous (G)IZO ones having the same \( N \) are justified essentially by the combined effect of grain boundary (small) and ionized impurity scattering (high) effects typical of polycrystalline oxides with this \( N \) range. [3] Contrarily, electron movement is relatively insensitive to structural disorder in an amorphous
structure primarily composed by large indium cations, typical of (G)IZO films. In addition, even when comparing polycrystalline oxide semiconductors based on In\textsubscript{2}O\textsubscript{3} and ZnO structures, the latter are generally slightly more resistive for a given $N$, which agrees with the experimental data obtained here. [2] Nevertheless, note that when produced under optimal conditions, GZO films can present very low $\rho$, around $3\times10^{-4}$ $\Omega$ cm, which is achieved with $N=10^{21}$ cm$^{-3}$, when the films are deposited under a ballistic transport plasma regime; [8]

- Even considering only the amorphous multicomponent oxides, there is considerably more dispersion on the $\rho$-$N$ data for 150 than for 500 °C annealed films, especially when $N<10^{18}$ cm$^{-3}$. This result suggests a model where carriers are relatively insensitive to structural disorder above this $N$ but are more prone to be affected by higher densities of defects for lower $N$, when $E_F$ starts to move out of the conduction band, being these defects dependent on the processing conditions and composition. When $T_A$ is increased, a large part of these defect levels are annihilated, allowing for a more linear $\rho$-$N$ relation. This is in agreement with the results presented in previous sections, where it was seen that the electrical properties start to depend less on the deposition conditions as $T_A$ increases.

A confirmation and more insights about the dispersion phenomena mentioned above are obtained analyzing the $\mu$-$N$ plots (fig. 4.19c and 4.19d). For the 150 °C annealed films, the two different regimes occurring below and above $N=10^{18}$ cm$^{-3}$ are very clear, with the films below this threshold $N$ value presenting reduced $\mu$, which remains almost unchanged down to $N=10^{16}$ cm$^{-3}$, consistent with the higher defect level density below the conduction band: as it will be seen below, GIZO films, even if annealed at 500 °C, have thermally activated (non-degenerated) conduction for $N=10^{16}$ cm$^{-3}$, meaning that $E_F$ is below the mobility edge for this $N$ range. [29] Above $N=10^{18}$-$10^{19}$ cm$^{-3}$, $\mu$ sharply increases with $N$, which is consistent with the existence of potential barriers associated with the random distribution of gallium and zinc atoms. These barriers should have a relatively small height, as the conduction is essentially dominated by the large indium 5s spherical orbitals, which easily overlap even in a disordered structure, while the zinc and gallium cations assure that this structure does not crystallize and prevent excessive free carrier generation. [55] As $N$ increases above $10^{20}$ cm$^{-3}$, ionized impurity scattering dominates charge transport, which is translated in lower $\mu$, as discussed before. For (G)IZO films annealed at 500°C, a continuous increase of $\mu$ with $N$ is verified right from $N=10^{16}$ cm$^{-3}$, meaning that most of the defects affecting the films with low $N$ are extinguished after the annealing treatment and $E_F$ can reach the conduction band edge for considerably lower $N$ than films annealed at lower temperatures. Another interesting feature of fig. 4.19c and 4.19d is that $\mu$ is increased to a much lower extent by the annealing treatment for the $N$ region comprised around $10^{19}$-$10^{20}$ cm$^{-3}$. Assuming that on this range of $N$ the most important scattering effects on these amorphous oxides are related with the structural randomness, it is expectable that the annealing
treatment leads to some structural relaxation, improving \( \mu \). Still, as this improvement on \( \mu \) is relatively small (around 10-20 \%) when compared to the \( \mu \) increase occurring for lower \( N \), it can be concluded that structural disorder does not affect significantly the electrical properties of (G)IZO films.

Data is also depicted for In\(_2\)O\(_3\) films which are already polycrystalline at 150 °C. Given the \( N \) values of these low-temperature annealed In\(_2\)O\(_3\) films (between \( 10^{18} \) and \( 10^{19} \) cm\(^{-3}\)), carrier transport is not significantly affected either by grain boundaries or by degenerated ionized impurities, hence similar \( \mu-N \) trends are verified for In\(_2\)O\(_3\) and (G)IZO films, reinforcing the idea that indium is the main element contributing to electronic transport. However, as \( T_a \) is increased to 500 °C \( N \) decreases below \( N=10^{18} \) cm\(^{-3}\), leading to grain boundary inhibited transport, as explained before. Concerning the GZO films, as they have higher \( N \) than crystalline In\(_2\)O\(_3\) films, carriers are more prone to be scattered at the higher number of ionized impurities, such as oxygen vacancies and gallium ions, decreasing their \( \mu \) as \( N \) increases, [77, 78] with this trend being valid both for low and high \( T_a \). Nevertheless, note that a combined effect of ionized impurity scattering and grain boundary scattering is also plausible for the lower \( N \) films, with \( N \approx 10^{19} \) cm\(^{-3}\) or below. [3]

To finish the analysis of fig. 4.19, it is also interesting to notice that after annealing at higher temperature, when the properties are less affected by the deposition conditions, the data in fig. 4.19b and 4.19d can be divided into well defined groups (different colors and symbols), with each one of these groups corresponding to a specific target composition, a range of \( \mu \) and \( N \). This constitutes valuable information about the flexibility of the (G)IZO system, being useful to select the necessary target composition to achieve the required electrical properties for each application.

4.1.5.2.2. Temperature dependence for binary polycrystalline oxides

Important details about the conduction mechanisms of semiconductors can be extracted by measuring their electrical properties for different temperatures. [79] This was accomplished for some of the oxide semiconductors produced in this work, in a range of temperatures between 100 and 300 K, namely for polycrystalline ZnO and In\(_2\)O\(_3\) and amorphous IZO and GIZO films, with special relevance being given to GIZO films, as they constitute the main semiconductors envisaged for the application as channel layers in TFTs.

The results obtained for a ZnO film annealed at 500 °C are presented in fig. 4.20. The film presents a thermally activated behavior with at least two regimes (fig. 4.20a), one with a thermal activation energy \( (E_a) \) of 0.02 eV (low temperature), other with \( E_a=0.15 \) eV (high temperature). Although no \( \mu-T \) data is available for the analyzed ZnO films, given their high \( \rho \), a \( N<10^{15} \) cm\(^{-3}\) is expected (assuming \( \mu \approx 1 \) cm\(^2\) V\(^{-1}\) s\(^{-1}\)). Hence, due to the non-degeneracy and to the polycrystalline structure, \( \mu \) should be 112
mainly governed by thermionic emission over the grain boundaries, as initially proposed by Seto, [80] at least for the higher range of $T$ (fig. 4.20b), rather than by thermal field emission of carriers through the barrier, as typically happens for higher doping levels or low $T$. [3] Still, other conduction mechanisms should be superimposed to this and assume more relevance specially for lower $T$, such as nearest-neighbor hopping (NNH) or variable range hopping (VRH) by localized electrons at impurity levels (for constant and non-constant hopping distances, respectively), as proposed in literature for ZnO films. [81] A more detailed analysis extended to a higher $T$ range, which is out of the scope of this research work, will be required to define which conduction mechanisms are prevalent on the present ZnO films.

![Figure 4.20](image)

*Figure 4.20 – Temperature dependence of the electrical properties for ZnO thin films annealed at 500 °C: (a) Arrhenius plot, showing activation energies for the two suggested regimes; (b) Relation between $\sigma$ and $T$ for thermionic emission and VRH conduction mechanisms.*

Given the considerably lower $\rho$ of In$_2$O$_3$ films, hall-effect measurements are possible for this material, allowing to extract not only $\sigma$ but also $\mu$ and $N$ evolution with temperature. This permits to have some more insights about relevant conduction mechanisms on this oxide semiconductor. The results obtained for an In$_2$O$_3$ film annealed at 500 °C are presented in fig. 4.21. $\sigma$ shows some thermal activation but considerably lower than for ZnO films ($E_a=0.014$ eV). Additionally, $N$ is not significantly changed with temperature, which is consistent with a close to degenerate state. On the contrary, $\mu$ shows a considerable dependence on $T$, meaning that complete degeneracy is not obtained. To help analyzing the $\mu$-$T$ trend and identifying the relevant conduction mechanisms, table 4.2 presents some of the most important scattering mechanisms for polycrystalline oxide semiconductors.
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Figure 4.21 – Temperature dependence of the electrical properties for In$_2$O$_3$ thin films annealed at 500 °C: (a) Arrhenius plot for $\sigma$, $\mu$ and $N$; (b) Relation between $\mu$ and $T$ using the grain boundary scattering model for degenerated and non-degenerated cases; (c) Relation between $\mu$ and $T$ using the ionized impurity and lattice vibration scattering models.

Table 4.2 – Different scattering centers and their $\mu$-$T$ relation for polycrystalline oxide semiconductors. [76, 78]

<table>
<thead>
<tr>
<th>Scattering center</th>
<th>$\mu$-$T$ relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grain boundary (degenerated)</td>
<td>$\ln(\mu T)\sim T^{-2}$</td>
</tr>
<tr>
<td>Grain boundary (non-degenerated)</td>
<td>$\ln(\mu T^{1/2})\sim T^{-1}$</td>
</tr>
<tr>
<td>Lattice vibration</td>
<td>$\mu \sim T^{-2}$</td>
</tr>
<tr>
<td>Ionized impurity (degenerated)</td>
<td>$\mu$ independent of $T$</td>
</tr>
<tr>
<td>Ionized impurity (non-degenerated)</td>
<td>$\mu \sim T^{3/2}$</td>
</tr>
</tbody>
</table>

The $\mu$ data was fitted for all the possible mechanisms listed on this table (fig. 4.21b and 4.21c).

Starting by grain boundaries effect, reasonably linear fits ($R^2\approx0.975$) are achieved for both degenerate and non-degenerate relations. The fact that both models yield the same fitting results may be explained by the $N$ value of the film, $\approx8\times10^{17}$ cm$^{-3}$ at room temperature, which is close to the
threshold for degeneracy on this material (around 1.48×10^{18} \text{ cm}^{-3}). Based on this, it can be predicted that the analyzed film has a donor level slightly below the CBM, but without overlapping it. [3, 82] Still, some deviations from an ideal fit are obtained in both cases, which could be indicative that grain boundaries are not the main scattering centers involved, or that another scattering mechanism plays simultaneously an important role. In fact, in polycrystalline oxide semiconductors with this range of \( N \), \( \mu \) is typically governed by the contribution of different mechanisms, namely bulk properties and grain boundary effects. [3] In addition, as pointed out before, grain boundaries are expected to have some contribution to the conduction mechanism for low \( N \) (comparatively to the \( N \) values typically obtained in TCOs, above 10^{20} \text{ cm}^{-3}), specially in materials with small grain size, due to their large depletion regions that directly affect the grain boundaries potential barriers height. [73, 76] To test the possibility that electronic conduction has simultaneous contributions, \( \mu \) data is fitted for the ionized impurity and lattice vibration models in fig. 4.21c, which were seen to affect non-degenerated single crystalline In_{2}O_{3} by other authors. [82] Clearly, linear relations are not obtained for all the temperature ranges, but each scattering mechanisms seems to be dominant for different temperatures. Based on this, it is proposed that ionized impurities are the main scattering centers for low temperatures, while lattice vibrations dominate for higher temperatures. Similar mechanisms are found in literature for GZO films. [78] Hence, it seems that at least three different scattering centers affect charge transport for the analyzed In_{2}O_{3} films, namely the ones associated with ionized impurities (low \( T \)), lattice vibrations (high \( T \)) and grain boundaries. Nevertheless, for a valid and accurate attribution of these different mechanisms to the different temperature ranges, a more detailed analysis is required, including more data points and the analysis of films with different \( N \).

**4.1.5.2.3. Temperature dependence for multicomponent amorphous oxides**

Given that multicomponent oxides are the main topic of this dissertation, their conduction mechanisms are analyzed in more detail than the binary oxides presented above. Figure 4.22 shows the temperature dependence of the electrical properties of IZO 5:1 thin films annealed at 150 °C, which are intended to be used as the electrodes of the TFTs. Given the temperature independency of the large \( N \), above 10^{20} \text{ cm}^{-3}, E_{F} \) should already be above \( E_{C} \), hence the conduction is essentially degenerated, as typically happens in TCOs. Still, \( \mu \) decreases for higher temperatures, which can be due to a lattice scattering mechanism, perhaps phonon or alloy related, as proposed by Leenheer \textit{et al.} for IZO films with similar \( N \). [70] For IZO films with higher \( N \), ≈6×10^{20} \text{ cm}^{-3}, which can be obtained by using \%O_{2}=0 \%, this \( \mu-T \) dependency is not verified but \( \mu \) is considerably decreased (see fig. 4.19c)
when compared with the one of the film presented in fig. 4.22. Thus, complete degeneracy associated with an ionized impurity scattering mechanism is only achieved for very high \( N \) values. These results are consistent with the ones obtained by Leenheer et al., where complete \( \mu-T \) independency only occurred for \( N \approx 5 \times 10^{20} \) cm\(^{-3}\). [70]

\[
\sigma (S \text{ cm})
\]

\[
1000/T (K^{-1})
\]

\[
IZO 5:1 (\text{for source-drain})
T_a=150 \degree C
\]

\[
\mu (cm^2 V^{-1} s^{-1})
N (\times 10^{20} \text{ cm}^{-3})
\]

Figure 4.22 – Temperature dependence of the electrical properties (Arrhenius plot for \( \sigma, \mu \) and \( N \)) for IZO 5:1 thin films annealed at 150 \degree C, intended to be used as electrodes in TFTs.

Concerning the GIZO analysis, films produced in pure argon atmosphere or with very small \( \%O_2 \) (\( \leq 0.4 \% \)) were prepared using different target compositions, namely GIZO 2:4:1, 2:2:1 and 2:2:2, and different \( T_a \), 300 and 500 \degree C. This set of films provided reasonably low \( \rho \) and high \( \mu \) to be measurable by hall-effect and a large range of \( N \) that allows understanding the effects of \( E_F \) shifting. Figure 4.23 shows the obtained results for these GIZO films (In\(_2\)O\(_3\) results are also plotted for comparison). It can be seen that fully thermal activated behavior (i.e., \( \rho, \mu \) and \( N \) changing significantly with \( T \), having \( E_a=0.05 \) eV) is only obvious for \( N<10^{17} \) cm\(^{-3}\), suggesting that above this \( N \) value \( E_F \) exceeds the mobility edge. However, \( \mu \) is thermally activated even for \( N=10^{19} \) cm\(^{-3}\), which suggests that some potential barriers exist above this mobility edge, in the vicinity of the conduction band. These potential barriers are associated with the structural randomness, mainly due to the random distribution of Ga\(^{3+} \) and Zn\(^{2+} \) ions, which form non-localized tail states around the conduction band edge. Thus, when \( E_F \) is located at energies corresponding to these potential barriers, carrier transport (i.e., \( \mu \)) is enhanced when the temperature is increased.

\footnote{IZO films processed under these conditions (\( \%O_2=0 \% \)) are not suitable to be used as transparent electrodes, given that their AVT is severely degraded (>50 \%).}
To clearly explain the proposed model, different regimes can be considered:

- For $N=10^{20}$ cm$^{-3}$, $E_F>E_C$ and $\mu$ shows little dependence on temperature. This suggests that $E_F$ is above a certain threshold energy ($E_{\text{th}}$) where carrier transport is not affected by the potential.
barriers associated with structural randomness. Thus, conduction is essentially degenerated, with the small \( \mu-T \) dependence for higher \( T \) being possibly ascribed to lattice scattering effects, as mentioned before for highly conducting IZO films;

- As \( N \) is decreased, first to \( 10^{19} \text{ cm}^{-3} \) and then to \( 10^{18} \text{ cm}^{-3} \), \( \mu \) changes with \( T \) and decreases when compared with the values obtained for \( N=10^{20} \text{ cm}^{-3} \). Hence, even if \( E_F>E_C \) can still be verified, carrier transport is limited because \( E_F<E_{th} \), i.e., the electrons are affected by the potential barriers. This type of conduction resembles a percolation mechanism, where the carriers move through a distribution of potential barriers, being the effect more pronounced as \( E_F \) moves to lower energies, towards the conduction band bottom.

- For the GIZO film with \( N=10^{17} \text{ cm}^{-3} \) an interesting effect is seen which, at first sight, could contradict the model exposed above, since \( \mu \) for this film is higher than for the films with \( N=10^{18} \) and \( 10^{19} \text{ cm}^{-3} \), even if \( E_F \) should be now located very close to \( E_C \) or even slightly below it, since \( N \) starts to present some dependence on \( T \). The reason for this behavior is related with the annealing treatment: since the as-grown film is highly deficient in oxygen (a \( \% O_2=0 \% \) was used), the annealing treatment promotes film’s oxidation, resulting in lower \( N \). But as suggested before, annealing can also result in structural rearrangement and annihilation of defects arising from the growth process, which is reflected in lower potential barriers and decreased trap states density. [83] Hence, despite having lower \( N \) and consequently being more prone to the effects of structural disorder and/or defects (\( E_F \) located at lower energies), a considerable decrease of the density of those scattering centers occurs with annealing, improving the quality of the film and the transport properties. The fact that \( \mu \) presents some more thermal activation than for the higher \( N \) films is consistent with this, since \( E_F \) is located at lower energy levels. This result is in agreement to the data presented in fig. 4.19c and 4.19d, where it can be seen that annealed films with \( N=10^{17} \text{ cm}^{-3} \) can present higher \( \mu \) than non-annealed films with \( N=10^{19} \text{ cm}^{-3} \);

- Finally, for films with \( N=10^{16} \text{ cm}^{-3} \), even if annealed at 500 °C, both \( N \) and \( \mu \) are thermally activated and \( \mu \) is the lowest among all the analyzed GIZO films. For this \( N \) range, \( E_F \) should be located below \( E_C \), on energies corresponding to high trap densities, related with structural randomness, heavy distortion of indium-oxygen-metal bonding angles and defects which are not totally annihilated by the annealing treatment. [67, 69, 84] Still, definite Hall voltage signals are obtained, which is an indication that the tail states created just below the conduction band are not localized and carrier mean free path is much larger than the chemical bond distances, which is opposite to what happens on a-Si:H, where the Hall sign double anomaly is verified. [29, 75, 85]

Since percolation between the potential barriers formed by the random distribution of cations seems to be the dominant conduction mechanism for GIZO, the \( \sigma \) data was also represented as a function of
$T^{1/4}$, which describes the percolation model if the potential barrier height has Gaussian-type distributions. [75] Linear fits for $\sigma-T^{1/4}$ and $\sigma$-$1000/T$ are presented in fig. 4.23d for the films with the lowest $\sigma$, where thermal activation is more evident. The results show that considerably improved fits are obtained for $\sigma-T^{1/4}$, reinforcing that a percolation conduction model is valid for GIZO. Note that a $\sigma$-$T^{1/4}$ relation may also be in accordance with a VRH mechanism, typical of disordered or highly doped semiconductors. [75] In the VRH mechanism the transport is limited by localized states and the charge carriers hop from a neutral atom to another neutral atom situated at the same energy level, even if located very interatomic distances away. [3] VRH shouldn’t be a relevant mechanism here, since the measured $N$ gives consistent Hall voltage signals, i.e., the carriers shouldn’t be localized [86] as predicted by the VRH model.

Similar results were reported for amorphous, polycrystalline and single-crystalline GIZO films, although with some differences on the threshold $N$ where the transition between the different regimes takes place, which can be attributed to the different growing methods and resulting quality of the films. [29, 75] Also, even if not defining whether hopping or percolation is the dominant conduction mechanism, Leenheer et al. obtained analogous $\mu$-$T$ relations in the IZO system. [70]

Additionally, note that even if the IZO and GIZO films with high $N$ presented in figs. 4.22 and 4.23 have similar $N$ values, $\mu$ is considerably higher for IZO. This clearly reinforces one of the main ideas exposed throughout this chapter, i.e., that (post-)deposition conditions (for instance, the low $\rho_{dep}$ used for IZO and the fact that GIZO films are not annealed) and composition play a very important role defining the electrical properties of oxide semiconductors when high $T_A$ is not used.

Nevertheless, even if exhibiting lower $\mu$ than IZO films, the GIZO films of fig 4.23 still present a large $\mu$, considerably higher (=60 %) than polycrystalline In$_2$O$_3$ films (also represented in fig. 4.23) having similar $N$. This is even more striking considering that the GIZO films were not annealed and the In$_2$O$_3$ films had an annealing treatment at 500 ºC that enhanced its crystallinity. This result clearly shows the advantage in terms of electrical performance of using multicomponent amorphous materials, at least for this range of $N$, where In$_2$O$_3$ transport is limited by grain boundaries, lattice scattering and ionized impurities, as discussed before.

### 4.1.5.3 Effect of thickness ($d_f$) on the electrical properties

Figure 4.23 also shows another interesting feature of amorphous oxide semiconductors that was not discussed yet: the electrical properties are essentially the same for GIZO 2:4:1 films with different thicknesses, around 230 and 40 nm. This situation is contrary to what happens in most polycrystalline materials, where $\rho$ variation with thickness only saturates for thicknesses above 200-300 nm. [3] Below these values, $\rho$ typically shows a large dependence on thickness: for instance, in GZO films $\rho$
can be increased more than one order of magnitude when thickness is decreased from 200 to 100 nm. [3] This $\rho$ improvement for higher thickness in polycrystalline materials is mostly attributed to improved crystallinity, lower number of defects and less surface scattering effects for thicker films. [3] Even when considering amorphous covalent materials, such as a-Si:H, where the grain boundary problems are absent, electronic quality of the films is reported to improve (in terms of density-of-states) as the thickness increases, [87] which is related with the fact that dangling bonds created during the growth process are mostly distributed around 100 nm from the top-surface. [88] The insensitivity of GIZO electrical properties to thickness should result from its amorphous structure composed of large overlapping cationic orbitals and strong ionic bonds, as opposed to the amorphous structure with large density of dangling bonds of covalent amorphous semiconductors. Hence, despite the thickness of GIZO, an overall structure with low density of defects is always created, much lower than the one typically found on a-Si:H, for which the tail states density is reported to be two to three orders higher than for GIZO. [69] Nevertheless, when GIZO thickness is decreased to a few nm surface effects such as the interaction with atmospheric oxygen should naturally start to be relevant and can dominate the overall properties of the thin films. This effect is explored with advantage for the application of oxide semiconductors with high $N$ as the channel layers of TFTs, as will be shown in chapter 5.

4.1.5.4. Electrical stability measurements

Selected films (=200 nm thick) deposited with different %$O_2$, target compositions and $T_a$ were electrically characterized during 18 months. During this period, the films were kept under normal room conditions, i.e., exposed to room temperature and atmospheric pressure, but stored in the dark to avoid possible light induced effects. Figure 4.24 shows the most relevant results obtained.

Figure 4.24 – $\rho$ measurements in an 18 months time-scale after the fabrication of the oxide semiconductor thin films: (a) Effect of %$O_2$ for GIZO 2:4:1 thin films annealed at 150 °C; (b) Effect of composition for thin films annealed at 500 °C.
The results are correlated with what was observed in previous sections of this chapter:

- Concerning the GIZO films produced with different \%O₂ and annealed at a low \( T_a \) 150 °C (fig. 4.24a), it is verified that the most stable films are the ones produced using low \%O₂ (0.4 \%). For films produced without oxygen \( \rho \) increases with time, while for films produced with higher \%O₂ the contrary happens. Furthermore, the most significant variation occurs for the films deposited with very high \%O₂, for which \( \rho \) decreases more than 3 orders of magnitude during the 18 months test. These results resemble the ones presented for instance in fig. 4.15a, where the variation of \( N \) as a function of \( T_a \) was analyzed for IZO films processed with different \%O₂. The effect here should be essentially the same, i.e., the materials always tend to an equilibrium point, where the discrepancies between their electrical properties, arising from the different processing conditions, are reduced. Here, this evolution occurs in a much larger time scale, due to the totally different amounts of energy supplied in each case: while here the films were annealed only at 150 °C and kept at room temperature during 18 months, which is consistent with low energy exchange processes, in the case of fig. 4.15a the properties of the films where changed almost instantaneously for higher \( T_a \), because the involved energy, thermally supplied to the materials, was much higher;

- The idea of the previous point is in agreement with the data depicted in fig. 4.24b. On this case, it can be seen that films produced with different target compositions and annealed at 500 °C do not show significant variations on \( \rho \) during the 18 months test. This is true for the multicomponent oxides, which are amorphous or at most crystallize close to this temperature, with very small grain sizes (IZO 4:1). For the binary oxides In₂O₃ and ZnO, which are both polycrystalline even at 150-170 °C, notorious variations are still observed after annealing at 500 °C, which should mostly be related with the presence of grain boundaries where several oxygen adsorption/desorption processes occur. The instability of these binary oxides is reinforced by the different variations observed for In₂O₃ films processed with \%O₂=0.4 and 1.0 \%, which do not happen for the multicomponent amorphous oxides when annealed at high temperature (as an example, compare in fig. 4.24b the properties of GIZO 2:4:1 films produced with \%O₂=0.4 and 10.0 \%, where even for the latter good stability is obtained).

However, note that considering an even larger time scale for low temperature annealed (or non-annealed) films does not necessarily lead to exactly the same properties as the ones instantaneously obtained after an high \( T_a \) treatment. Processes involving severe structural changes, such as significant atomic rearrangement and amorphous-crystalline transition, or desorption of strongly bonded oxygen atoms, generally require that certain threshold energy values are surpassed, and these cannot be supplied by simply leaving the film at room temperature for a long period of time.
Itagaki et al. also analyzed the shelf life stability on non-annealed IZO films with different compositions during 3 months. [89] The results presented by the author show that during this period $\rho$ can decrease around 4 orders of magnitude for large zinc contents ($\text{In}/(\text{In}+\text{Zn})$ atomic ratio $\approx$0.20), but only around 1 order of magnitude for large indium contents ($\text{In}/(\text{In}+\text{Zn})$ atomic ratio $\approx$0.80). Most of these changes occur during the first month, which is in agreement with the data presented above, at least for the less resistive samples.

Based on the data collected for IZO and GIZO films during the 18 months study and on Itagaki's results, it is proposed that for low temperature annealed (or non-annealed) multicomponent amorphous oxide films stability is enhanced when deposited under ideal conditions, specially regarding $\%O_2$ that should be low ($\approx$0.4 %), and for indium-richer compositions, but increased $T_A$ brings improved stability even for deposition conditions/compositions that deviate from these. However, note that even fulfilling the requirements for good stability listed above, it is expected that for very thin films, adsorption/desorption processes at the films' surface can play a very significant role and considerably changes on the electrical properties can happen through time. This is particularly important for the application of these materials on TFTs, as it will be seen on the next chapter.

Naturally, these are only preliminary conclusions about the stability of these materials. The described trends must be confirmed and the mechanisms responsible for them must be clearly understood before any definitive conclusions are taken.

### 4.1.6. Optical properties

Given that optical effects deal with transitions between bands and/or energy levels inside the bandgap, optical measurements are of great interest to analyze semiconductors. [90] In addition, high optical transmittance is generally desirable for oxide semiconductors, as one of the main applications of these materials is on the emerging area of transparent electronics. This section presents a brief analysis of the optical properties achieved for the produced oxide semiconductors, obtained by transmittance measurements and spectroscopic ellipsometry. The dependence of these properties on $\%O_2$, composition and $T_A$ is discussed.

#### 4.1.6.1. General considerations about the optical measurements

For most of the amorphous semiconductors, non-direct optical transitions are allowed and the exponent $x$ in Tauc's relation $\alpha^x \approx (E-E_{opt})$ (see chapter 3, p. 73) assumes the value 0.5. [91] However, for $\text{In}_2\text{O}_3$ it was reported that electron momentum is conserved and the shapes of the absorption
edges are similar when considering amorphous and crystalline structures. [51] Therefore, the direct bandgap model with x=2, which is typically applied for polycrystalline In$_2$O$_3$ films, also provides a good description of the optical absorption band edge for amorphous In$_2$O$_3$ films. Given that IZO, IGO and GIZO are amorphous materials primarily composed of In$_2$O$_3$, this model is also extended to their analysis. This methodology was followed by different authors to extract $E_{\text{opt}}$ on multicomponent oxides based on In$_2$O$_3$, [15, 31, 70, 92] although some others adopt the typical $\alpha^{1/2}$-E plot of covalent amorphous materials for the determination of $E_{\text{opt}}$. [46, 93, 94] Since the $E_{\text{opt}}$ determination by $\alpha^{2}$-E yielded results closer to the ones obtained by spectroscopic ellipsometry, this was the methodology followed here, but both x=0.5 and x=2 yielded reasonably good linear fits to the experimental data at the onset of absorption rise. Differences in $E_{\text{opt}}$ as large as 0.5-0.6 eV were found when using x=0.5 or x=2 (higher $E_{\text{opt}}$ for x=2), although the trends described in the following pages are essentially the same for both methodologies.

Optical analysis can also provide valuable information about defect states of a given material. In particular, oxide semiconductors have important subgap absorptions related with deep and shallow levels that considerably affect electrical properties, hence are important to be analyzed. [59, 83] However, to fit different models to the experimental data obtained by transmittance and reflectance measurements, one has to be aware of the limitations of the spectrometer and of the sample itself. Figure 4.25 shows an example of an $\alpha$-E plot for a GIZO film, where Tauc and Urbach models are fitted to the experimental data, according to the equations 3.18 and 3.19.

![Figure 4.25 – $\alpha$-E plot for a non-annealed GIZO thin film, showing Tauc and Urbach models fittings to the experimental data.](image)

Although the Tauc plot provides a good fit to the experimental results above the bandgap (in the strong absorption region), $\alpha$ data fitted with the Urbach law is close to the reliability limit of the experimental setup. It is clear that some subgap absorption is present, but detailed comparisons between different films or the correctness of fitting the Urbach law to the tail-like absorption reveal a large degree of inaccuracy. Hence, to correctly evaluate the subgap optical properties some other
techniques should be used, such as constant photocurrent method (CPM) or modeling by spectroscopic ellipsometry. Although the last technique was also used here, it served essentially to confirm results and a detailed modulation of subgap states was for now out of the scope of the work.

4.1.6.2. Dependence of the optical properties on the (post-)deposition parameters and composition

4.1.6.2.1. Percentage of oxygen content in the Ar+O₂ mixture (%O₂)

From the three deposition parameters studied, %O₂, \( P_{\text{dep}} \) and \( P_{\text{rf}} \), the former is the one mostly affecting the optical properties. Figure 4.26 shows the effect of %O₂ on the \( \alpha^2 - E \) plots for films produced using a GIZO 2:4:2 target, annealed at 150 (fig. 4.26a) and 300 °C (fig. 4.26b).

![Figure 4.26 – \( \alpha^2 - E \) plots as a function of %O₂ for GIZO 2:4:2 thin films annealed at (a) 150 and (b) 300 °C.](image)

Two effects are immediately observable: \( E_{\text{opt}} \) increases with %O₂ (see also table 4.3) and although the same trend is verified for both \( T_A \), at 300 °C the effect is less pronounced, which agrees with the results regarding the electrical properties, where fewer discrepancies are also found for higher \( T_A \). The increase of \( E_{\text{opt}} \) with %O₂ is tentatively attributed to different factors:

- As seen in section 4.1.4, higher %O₂ leads to an increase of gallium at the cost of indium concentration. Given that Ga₂O₃ has a considerably higher \( E_{\text{opt}} \) than In₂O₃ or ZnO, this can be reflected in a higher \( E_{\text{opt}} \) on the final GIZO structure (see also the discussion on composition below);
- Higher %O₂ allows to fill a higher number of absorptive defect states, associated with oxygen deficiency. This way, the levels available for optical absorption are located at higher energies as %O₂ increases, raising \( E_{\text{opt}} \). A similar mechanism is proposed by Suresh et al. for GIZO films. [34]

Based on the results presented in the last section, films produced with higher %O₂ are expected to have lower \( N \). For TCO films, this typically leads to lower \( E_{\text{opt}} \), in agreement to the well known Burstein-Moss shift. [95] However, an opposite trend is verified for the results discussed here,
because the GIZO 2:4:2 films presented in fig. 4.26 are not degenerate. Hence, $E_{\text{opt}}$ variation should rather be governed by mechanisms such as the ones proposed above. Similar $E_{\text{opt}}$-%$O_2$ trends are verified for other compositions and/or $p_{\text{dep}}$ and $P_{\text{rf}}$ conditions that yield films with low $N$, usable as active layers on TFTs. IZO films with higher $N$, used for electrodes, will be analyzed on p. 129. In fig. 4.26 it is also noticeable that for all the films $\alpha^2$ does not increase abruptly, which is consistent with subgap absorption due to the band-tails, typical on amorphous materials. [90]

The trends observed with %$O_2$ on GIZO 2:4:2 were confirmed by spectroscopic ellipsometry analysis, as presented in fig. 4.27 for non-annealed films. The extinction coefficient ($k$) does not have an abrupt increase with $E$, confirming the amorphous structure of the material (fig. 4.27a). Also, the shift of the absorption edge with %$O_2$ agrees with the results presented in fig. 4.26. Concerning fig. 4.27b, the contribution of the Drude model is visible in the low energy part of the $n$-$E$ spectrum: for the film produced without oxygen a large $N$ is obtained, affecting the relative permittivity at this energy range and consequently the value of $n$. [3] For higher %$O_2$ the contribution of the Drude model is negligible, due to a considerably lower $N$ of the films. As suggested by the previous electrical characterization results, the degree of compactness also seems to be affected by %$O_2$, which is verified by the peak value of $n$, that reaches a maximum for %$O_2$=0.4 %. The minimum $n$ value is obtained for %$O_2$=10.0 %, suggesting lower compactness for films produced under these conditions, presumably due to the deleterious substrate bombardment effects described before. The $E_{\text{opt}}$ calculated from figs. 4.26 and 4.27 data are presented in table 4.3, showing that spectroscopic ellipsometry yields lower values. This is related with the fact that the simulation model used here takes into account the absorption due to tail-states to calculate $E_{\text{opt}}$.

Figure 4.27 – Spectroscopic ellipsometry data, showing (a) $k$-$E$ and (b) $n$-$E$ plots as a function of %$O_2$ for non-annealed GIZO 2:4:2 thin films.
Table 4.3 – $E_{opt}$ values extracted from $\alpha^2$-$E$ plots and from spectroscopic ellipsometry data (identified by SE), for GIZO 2:4:2 thin films produced with different %O2, annealed at 150 and 300 °C.

<table>
<thead>
<tr>
<th>%O2 (%)</th>
<th>$E_{opt}$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>150 °C</td>
</tr>
<tr>
<td>0</td>
<td>3.47</td>
</tr>
<tr>
<td>1.0</td>
<td>3.51 (SE)</td>
</tr>
<tr>
<td>10.0</td>
<td>3.60 (SE)</td>
</tr>
</tbody>
</table>

4.1.6.2.2. Composition (binary and multicomponent oxides)

In materials composed by two or more compounds, $E_{opt}$ is expected to assume a value intermediate to the ones of the composing compounds, varying in proportion to their concentration on the final material. However, the variation is rarely linear, mainly because of the formation of band tails due to the random perturbation introduced in the host lattice by the minority atoms. This is the typical case of germanium-silicon alloys. [90] To see if the same applies for multicomponent oxides, $E_{opt}$ evolution is analyzed for different In/(In+Zn) (fig. 4.28a) and In/(In+Ga) (fig. 4.28b) atomic ratios. The extracted $E_{opt}$ values are presented in table 4.4.

Figure 4.28 – $\alpha^2$-$E$ as a function of (a) In/(In+Zn) and (b) In/(In+Ga) atomic ratios for oxide semiconductor thin films annealed at 150 °C. Data for the binary oxides (In$_2$O$_3$, ZnO and Ga$_2$O$_3$) is also included for reference.

Table 4.4 – $E_{opt}$ values extracted from $\alpha^2$-$E$ plots for different binary and multicomponent compositions, for thin films annealed at 150 °C.

<table>
<thead>
<tr>
<th>Composition</th>
<th>In$_2$O$_3$</th>
<th>ZnO</th>
<th>Ga$_2$O$_3$</th>
<th>IZO 2:1, $(\text{In}/(\text{In}+\text{Ga}))=1$</th>
<th>GIZO 2:4:2, $(\text{In}/(\text{In}+\text{Ga}))=0.67$</th>
<th>GIZO 2:2:1, $(\text{In}/(\text{In}+\text{Ga}))=0.50$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{opt}$ (eV)</td>
<td>3.52</td>
<td>3.24</td>
<td>4.16</td>
<td>3.33</td>
<td>3.64</td>
<td>3.81</td>
</tr>
</tbody>
</table>
It can be seen that within the range of In/(In+Zn) ratios analyzed here $E_{opt}$ does not present significant changes, being the values located between 3.29 and 3.33 eV. These values are similar to the ones reported in literature for IZO films with moderate-to-high $\rho$. For films with $N>10^{20}$ cm$^{-3}$ $E_{opt}$ can increase above 3.5 eV due to Burstein-Moss shift. [15, 70] The fact that a systematic trend for $E_{opt}$ is not verified with the In/(In+Zn) atomic ratio should be ascribed to the insensitivity of the electronic structure to the metal composition, as proposed by Leenheer et al. [70] Additionally, a very large $E_{opt}$ variation would not be expected, given the proximity of In$_2$O$_3$ and ZnO bandgaps. [96] As expected, even if gallium is incorporated in the structure (i.e., for GIZO), $E_{opt}$ is still relatively unaffected by the In/(In+Zn) atomic ratio. However, In/(In+Ga) atomic ratio has an important effect on $E_{opt}$, with a shift of $\approx 0.5$ eV being verified when ln/(ln+Ga) is decreased from 1 to 0.50. Since Ga$_2$O$_3$ has a considerably larger $E_{opt}$ than In$_2$O$_3$ and ZnO, the increase in Ga$_2$O$_3$ content widens the bandgap in the amorphous GIZO films. [93] Similar dependences for GIZO films were found by Kang et al. [96]

Spectroscopic ellipsometry analysis reinforces the trends discussed above. In fact, the $k$-$E$ plots represented in fig. 4.29 for non-annealed films with different compositions are in agreement with fig. 4.28b, being verified that the addition of gallium to the IZO structure significantly shifts the absorption edge toward higher $E$. Furthermore, given that all the films analyzed in fig. 4.29 are amorphous except ZnO (note that these are non-annealed films), it is noticeable a sharper increase of $k$ with $E$ for ZnO films, consistent with the fact that in polycrystalline materials band transitions occur for a well defined $E$, while in amorphous materials they occur for a broader $E$ range.

![Figure 4.29 - Spectroscopic ellipsometry data, showing k-E plots for oxide semiconductor films with different compositions. Non-annealed films.](image-url)
4.1.6.2.3. Annealing temperature ($T_A$)

Besides reducing the discrepancy between the obtainable properties using different deposition conditions, such as $%O_2$ (fig. 4.26), increased $T_A$ may also promote important structural and chemical modifications that are reflected in the optical properties. Figure 4.30 shows the effect of $T_A$ on In$_2$O$_3$ and ZnO thin films.

For In$_2$O$_3$ (fig. 4.30a) a considerably sharper $\alpha^2$ rise can be seen when moving from 150 to 200 °C, which is coincident with the crystallographic changes occurring on the material: if at 150 °C the structure is essentially polycrystalline but still has a significant amorphous contribution, the amorphous phase tends to disappear for higher $T_A$, being this evolution also accompanied by changes on the preferential orientations of the crystals, as seen in the XRD analysis (fig. 4.3). Still, $E_{opt}$ is only slightly affected, changing from 3.52 to 3.63 eV, reinforcing the idea that the properties of ionic semiconductors based on large cations are considerably less sensitive to structural disorder than covalent semiconductors. Concerning ZnO (fig. 4.30b), which always presents a polycrystalline structure with the same preferential orientation, a slightly sharper rise is verified for higher $T_A$, being consistent with the improvement of the crystalline quality (larger grain size). Both materials present average transmittance in the visible range (AVT) of 80-85 % and the obtained $E_{opt}$ are in agreement to what is typically found in literature.

For the multicomponent oxides, different behaviors are observed as $T_A$ increases, depending on the $N$ range. Two illustrative cases are shown in fig. 4.31:

- For materials with low $N$, such as GIZO 2:4:2, transmittance spectra and consequently $\alpha^2$-$E$ plots and $E_{opt}$ are not significantly changed with $T_A$ (fig. 4.31a). The only visible change occurs for films annealed at 500 °C, for which $N$ increases from $<10^{14}$ (estimated from $\rho$ measurements) to $10^{17}$ cm$^{-3}$ (actually measured). These results are consistent with the trend presented for $%O_2$, since
these materials are not degenerated (although at 500 °C they should be close to the onset of degeneracy), turning the Burstein-Moss rule non-applicable. For the 500°C annealed films, structural relaxation and annihilation of trap states close to the conduction band edge, associated with random ionic distribution and heavy distortion of indium-oxygen-metal bonds, can also contribute to the slight decrease of $E_{\text{opt}}$. For this high $T_a$, even if In$_2$O$_3$ phases are not yet visible in XRD data, some In$_2$O$_3$–rich agglomerates may start to form, contributing to a decrease of $E_{\text{opt}}$ ($E_{\text{opt,In2O3}}<E_{\text{opt,GZO}}$). AVT is maintained around 84% for all the analyzed $T_a$.

- On the other hand, significant changes are verified for materials with high $N$, such as the IZO films produced for electrode application (fig. 4.31b). As seen before (fig. 4.16), $N$ decreases from $\approx 2\times10^{20}$ to $\approx 1\times10^{19}$ cm$^{-3}$ with $T_a$, but even the lowest $N$ value assures degeneracy. Given the high $N$ involved, a considerable decrease is verified on the transmittance in the near infrared region, i.e., the infrared absorption edge is shifted towards the visible region as $N$ increases. This effect is well predicted by Drude’s theory for free electrons in metals and is associated with the plasma oscillation of the free carriers that screen the incident electromagnetic wave via transitions within the conduction band. [3, 71] AVT values are also affected by annealing (and consequently by $N$), being consistently changed between 76 and 79% as $N$ is decreased from $1.9\times10^{20}$ (150 °C) to $2.0\times10^{19}$ (300 °C). Another different effect from the previously analyzed oxides is that the absorption edge is blue shifted for higher $N$, in accordance with the Burstein-Moss effect, since in degenerated semiconductors the lowest states in the conduction band are blocked as $N$ increases, turning optical absorption only possible for higher energies. [29, 92]

![Graphs showing the effect of $T_a$ on the optical transmittance in the UV-Visible-NIR regions for multicomponent oxide semiconductor thin films produced under different processing conditions and compositions, in order to achieve different $N$ ranges: (a) GIZO 2:4:2 thin films; (b) IZO 5:1 thin films. The insets show the $\alpha^2$ vs $E$ plots obtained from the transmittance data.](image)

Note that for the IZO and GIZO compositions analyzed in this work In$_2$O$_3$ is always the first phase to crystallize.
Typical Burstein-Moss shifts require that $E_{\text{opt}}$ varies linearly with $N^{2/3}$, considering a threedimensional parabolic band material. [70] Figure 4.32 shows that the IZO films from fig. 4.31 obey this relation until a $T_A$ of 300 °C, with the same being verified for GIZO 2:8:2 films, which always have $N>10^{18}$ cm$^{-3}$. The deviations from linearity can be due to the error in fitting the $\alpha^2$-$E$ plot, electron–ion and electron–electron scattering effects which can narrow $E_{\text{opt}}$ even when $N$ increases in a degenerate semiconductor. [3, 51, 97] Also, structural changes arising due to the increase of $T_A$ may also affect the optical properties. In fact, when these structural changes are extreme, leading to crystallization (which happens for the IZO films), $E_{\text{opt}}$ can deviate significantly from the linear $E_{\text{opt}}$-$N^{2/3}$ relation, as shown by the isolated points in the plot below. A similar effect on $E_{\text{opt}}$ was also found by Gonçalves et al. in IZO films annealed at 500 °C. [31] For GIZO 2:8:2 films, even if crystallization does not occur for $T_A=500$ °C, the formation of In$_2$O$_3$-rich agglomerates contributes to decrease $E_{\text{opt}}$, as suggested above.

![Figure 4.32 – $E_{\text{opt}}$-$N^{2/3}$ plots for IZO 5:1 and GIZO 2:8:2 thin films, with different $N$ values obtained by varying $T_A$. The linear fit shows good agreement of the data with the Burstein-Moss rule for degenerate semiconductors.](image)

A last graph is show on this section to reinforce the interrelation between optical, electrical and structural properties on oxide semiconductors (fig. 4.33). GIZO 2:8:2 films are chosen since the as-deposited films present a high $N$, above $10^{19}$ cm$^{-3}$, allowing to have clearer optical effects than the films analyzed in fig. 4.27b. It can be seen that as $T_A$ increases the variation on $N$ is clearly monitored in the low energy part of the spectrum down to $N<10^{18}$ cm$^{-3}$, due to the Drude component introduced in the simulation model. Also, the films’ compactness seems to be improved for higher temperatures, as suggested by the continuous increase of the maximum $n$ as $T_A$ increases. Although the calculation of the $N$ and $\mu$ values by applying the Drude model to the optical data was out of the scope of this work, the fact that the qualitative information extracted from fig. 4.33 totally corroborates the trends observed by the electrical analysis performed on the same materials is an excellent indicative regarding the validity of the simulation model, showing also that spectroscopic ellipsometry is a valuable complementary technique for the present and future analysis of oxide semiconductors.
4. Properties of n-type oxide semiconductor and high-κ dielectric thin films produced by sputtering

![Graph showing n-E plots as a function of Ta for GIZO 2:8:2 thin films processed using the same deposition conditions.]

4.2. Amorphous high-κ dielectrics based on tantalum-silicon and tantalum-aluminum oxide systems

In this section are presented relevant results regarding the amorphous high-κ dielectrics studied during this dissertation. The detail of analysis intended here is far from the one previously presented for oxide semiconductors. The main emphasis is given on the concept of multicomponent amorphous dielectric oxides, based on mixtures of low and high-κ materials.

4.2.1. Process flow and deposition parameters

The process flow used to deposit the dielectric thin films is shown in fig. 4.34. At this stage of the work, only silicon wafers (2.5×2.5 cm squares) were used as substrates and semiconductors (important regarding electrical measurements, see p. 137). The films were produced in an AJA ATC-1300F sputtering system, with a base pressure below 0.05 mPa, target-to-substrate distance of 10 cm and no intentional substrate heating. Too assure reasonable insulating properties, all the dielectric films were produced with a thickness around 300 nm. Although Ar/O₂ flow ratios and p_{dep} effects were studied for some of the dielectrics during this work, high Ar/O₂ ratio and low p_{dep} (14/1 sccm and 0.3 Pa, respectively) were used for all the study presented herein, since only under these conditions the growth rates could be reasonably high (at least above 2 nm min⁻¹), thus of interest for device fabrication. Most of the work was devoted to the production of multicomponent oxides, using mixtures of high- and low-κ materials, either by co-sputtering or by starting with a ceramic target with a pre-defined mixed composition. For the co-sputtering process, P_r applied to each target was used to control the incorporation of each element in the deposited film.
Like for oxide semiconductors, selected dielectric samples were subjected to annealing treatments, performed in air using a tubular furnace, with a heating ramp of 10 °C min⁻¹ and maintaining the desired temperature (300 °C) for 1 hour.

### 4.2.2. Growth rate of the sputtered dielectrics

Figure 4.35 shows the growth rates obtained for the tested materials.

The data shows that even if low %O₂ and pₐₕₑₜ were used, which favor higher growth rates, considerably higher Pₚf had to be employed to achieve growth rates comparable to the ones of oxide semiconductors analyzed at the beginning of this chapter. This is expected since insulators are generally very hard materials to sputter. Reinforcing this, fig. 4.35 shows that SiO₂ and Al₂O₃, which have the largest E₀ and intrinsic ρ, have the smallest growth rates. Concerning the high-κ dielectrics, Ta₂O₅ provides the highest growth rate, even using the lowest Pₚf. This is theoretically advantageous over the high Pₚf process of HfO₂, as less substrate damage should be obtained. [2] As expected, for the co-sputtered materials (Ta₂O₅-SiO₂ and Ta₂O₅-Al₂O₃, denoted TSiO and TAO, respectively), higher growth rates are achieved than for the single targets, as two material sources were sputtered.
simultaneously. Finally, for the TAO multicomponent target (denoted TAO s.t.), intermediate values to the ones of the constituting binary compounds are obtained, as observed before for the GIZO semiconductor system (fig. 4.2d).

Given the higher growth rate and less sputtering damage arising from the Ta2O5 based processes, tantalum-silicon and tantalum-aluminum oxides were the multicomponent systems elected for this study. Still, multicomponent dielectrics based on hafnium-silicon oxides (denoted HSO) were studied simultaneously in the same laboratory by Pereira et al. [98] As these HSO based insulators were also used in the last stage of the dissertation to successfully produce good performance TFTs and active matrices, relevant comparisons with the results achieved for this system are made in the analysis that follows.

4.2.3. Structural, compositional, optical and electrical properties

A tight relation is found between structural, compositional, optical and electrical properties on the analyzed materials. Before starting the discussion of the results, some clarifications should be made regarding the characterization presented herein:

- The data for the structural properties refers to films intentionally annealed at a relatively high temperature (300 °C), in order to investigate the stability of their properties at the maximum temperature for which most of the TFTs presented in the next chapter were subjected. Films annealed at lower temperatures were also analyzed, being found that their structure is not affected for this T
t range. All the remaining properties were analyzed in non-annealed films;
- XPS technique was used to obtain compositional data and contrarily to what was verified for GIZO films (see fig. 4.7a), it did not lead to large discrepancies when compared with other techniques, such as XRF and EDS. This is in agreement with the small sputtering yield obtained for the dielectric materials. Still, for the Ta2O5 films some compositional variations were verified if an argon cleaning process was used to remove carbon from the surface, although to a much lower extent than for the GIZO films;
- Electrical properties, critical for the application of these films on TFTs, were only briefly analyzed at this stage, as most of the electrical performance evaluations were done directly in TFT structures, produced simultaneously with the thin films.

Figures 4.36 and 4.37 show the structural and compositional data obtained for the TSiO and TAO dielectrics. SiO2 and Al2O3 films present an amorphous structure, as expected for these large bandgap materials. [99] For the Ta2O5-based compositions a broad diffraction peak appears close to 2θ=30°, suggesting that some short-range order exists in the thin films, but crystallization (i.e., long-
range ordering) is not achieved (fig. 4.36a). XPS and spectroscopic ellipsometry analysis suggest that this short-range order can be affected by composition, namely by the amount of tantalum present in the films. According to the XPS data (fig. 4.37), tantalum content is decreased from 30.4 % in pure Ta₂O₅ to 16.3 % in TAO s.t., while the co-sputtered dielectrics exhibit intermediate percentages. In addition, spectroscopic ellipsometry analysis reveals that the broadening parameter is higher for the multicomponent oxides (1.86-1.96) than for the Ta₂O₅ (1.73) films, suggesting higher degree of short-range ordering for Ta₂O₅ than for multicomponent thin-films. [96, 100] This supports the hypothesis that Ta₂O₅ is the responsible element for the enhancement of such short-range ordering and that its mixture with lower-κ materials is effective to increase the disorder and so inhibit crystallization.

**Figure 4.36** – Structural analysis obtained for Ta₂O₅-based dielectrics annealed at 300 °C: (a) XRD analysis, where the bars show the peak positions and relative intensities for β crystalline orthorhombic Ta₂O₅ (ASTM, card 25-0922); (b) TEM analysis, showing an electron micrograph of a TAO s.t. film cross section. The inset shows the corresponding electron diffraction pattern.

Furthermore, note that these structures, even when considering only the pure Ta₂O₅ films, show a considerably lower tendency to crystallize than other high-κ materials, such as HfO₂ or Y₂O₃, which can bring benefits in terms of electrical performance, reliability and integration. [101] Figure 4.36b
shows an example of the results obtained by TEM analysis of a TAO s.t. film, confirming that even after the annealing treatment at 300 °C, the structure remains amorphous.

For the HfO$_2$ based dielectrics, the effect of adding SiO$_2$ or Al$_2$O$_3$ is much more pronounced: HfO$_2$ films, even if sputtered without intentional substrate heating, generally present a polycrystalline structure, but the addition of SiO$_2$ or Al$_2$O$_3$ turns the structure amorphous. [98]

Concerning the compositional analysis of the Ta$_2$O$_5$-based thin films, the results also show that good correlation between nominal (i.e., target composition) and experimental values is found for the different binary compositions. The largest discrepancy is obtained for the pure Ta$_2$O$_5$ films, with 28.6 % Ta/71.4 % O and 30.4 % Ta/69.6 % O, for the nominal and experimental values, respectively. This is in agreement with the variations observed after the argon cleaning process, given that among all the tested binary oxides, Ta$_2$O$_5$ is the most sensitive to it. Variations of the same order of magnitude between the target and film composition are also achieved for the multicomponent target (TAO s.t.).

The spectroscopic ellipsometry data are presented in figs. 4.38 a-d and provide good support to the structural and compositional data discussed above.

**Figure 4.38** – Spectroscopic ellipsometry data obtained for the dielectric thin films of (a and b) TSiO and (c and d) TAO systems. Dependences of \( n \) and \( k \) on \( E \) are presented, for films deposited on c-Si substrates.
Starting by the $n$ evolution of $\text{Ta}_2\text{O}_5$ and $\text{SiO}_2$ related dielectrics (fig. 4.38a), it is evident that $\text{SiO}_2$ is incorporated in the co-sputtered $\text{TSiO}$ film, since its $n$-$E$ plot is located between those of pure $\text{Ta}_2\text{O}_5$ and $\text{SiO}_2$ films. In addition, the co-sputtered film’s $n$-$E$ plot is closer to the $\text{Ta}_2\text{O}_5$ one, both in absolute values and shape, suggesting a higher concentration of tantalum than silicon, in agreement with the XPS data depicted in fig. 4.37. Valuable information concerning the absorption rise at the onset of conduction band is given by the $k$-$E$ plot in fig. 4.38b. An increase on $E_{\text{opt}}$ from 4.08 to 4.27 eV is achieved when comparing pure $\text{Ta}_2\text{O}_5$ and co-sputtered $\text{TSiO}$ films, suggesting $\text{SiO}_2$ incorporation in the latter. Note that the $E_{\text{opt}}$ values presented herein are lower than the ones usually reported in the literature for $\text{Ta}_2\text{O}_5$ (around 4.5 eV), even if the analyzed films are close to the ideal stoichiometry, according to XPS data. This is attributed to two factors: first, the simulation model used here takes into account the absorption due to tail-states (located inside the bandgap, close to the bands) to calculate $E_{\text{opt}}$; second, the sputtering process may induce some damage to the structure, reflected in the broadening of the band-tails. For the TAO system similar conclusions can be drawn: both TAO films (co-sputtered and s.t.) present $n$-$E$ plots located between the $\text{Ta}_2\text{O}_5$ and $\text{Al}_2\text{O}_3$ ones (fig. 4.38c). Once again, in agreement to XPS data, the s.t. film should have higher $\text{Al}_2\text{O}_3$ incorporation than the co-sputtered TAO film, since its $n$-$E$ plot is closer to the $\text{Al}_2\text{O}_3$ reference and the onset of absorption starts for higher energy than the co-sputtered film (fig. 4.38d). The $E_{\text{opt}}$ determined for the TAO films are 4.14 (co-sputtered) and 4.35 eV (s.t.). When comparing the co-sputtered $\text{TSiO}$ and TAO $E_{\text{opt}}$ values, note that the higher value of the former can be a consequence of two factors: its slightly smaller amount of $\text{Ta}_2\text{O}_5$ and the higher bandgap of $\text{SiO}_2$ when compared with $\text{Al}_2\text{O}_3$; the higher damage induced during the co-sputtering process when using $\text{Al}_2\text{O}_3$, since a higher $P_n$ is needed for this material to attain reasonable incorporation rates (fig. 4.35). A damaged structure and poor compactness might be the main reasons behind the poor device performance obtained with $\text{Al}_2\text{O}_3$ and co-sputtered TAO, as will be shown in the next chapter.

The $\kappa$ values of the dielectric films were determined from MIS capacitors and are presented in table 4.5.

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>$\text{SiO}_2$</th>
<th>$\text{Al}_2\text{O}_3$</th>
<th>$\text{HfO}_2$</th>
<th>$\text{Ta}_2\text{O}_5$</th>
<th>$\text{TSiO}$</th>
<th>TAO</th>
<th>TAO s.t.</th>
<th>PECVD $\text{SiO}_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\kappa$</td>
<td>5.0</td>
<td>8.4</td>
<td>24.7</td>
<td>24.6</td>
<td>17.3</td>
<td>21.7</td>
<td>14.2</td>
<td>3.9</td>
</tr>
</tbody>
</table>

The obtained values are in agreement with the XPS data, showing a trend to increase with the $\text{Ta}_2\text{O}_5$ content in the thin films. The binary compounds, specially $\text{Ta}_2\text{O}_5$, present $\kappa$ values close to the ones expected for the nominal compositions, [99] reinforcing the idea already demonstrated with XPS that
their composition should be close to the theoretical stoichiometry. For the SiO₂ and Al₂O₃ films higher variations of κ from the nominal values were found, which might be explained by the above mentioned structural damage occurred during sputtering with higher Peff. As expected, the multicomponent dielectrics present κ values between those of their constituent binary oxides. Measurements of the current density as a function of voltage (J-V) were also performed in MIS structures, to evaluate the electrical reliability of these dielectrics. Low J values are a fundamental requisite, as these materials have to provide electrical insulation between the gate electrode and the semiconductor in TFT structures. Figure 4.39 shows the results obtained for some of the analyzed materials. Due to its lower bandgap, Ta₂O₅ presents larger J, around 2 orders of magnitude higher than SiO₂, even if the SiO₂ sputtering process is not entirely optimized. However, when SiO₂ and Ta₂O₅ are co-sputtered, a significant improvement is verified, with TSiO exhibiting J values similar to the ones of SiO₂. Additionally, as presented in table 4.5, TSiO presents a κ more than 3 times larger when compared with SiO₂, which can be reflected in enhanced capacitive injection and better overall transistor performance, as will be shown in the next chapter.

![Figure 4.39 – J-V characteristics for MIS structures comprising dielectric thin films based on tantalum-silicon oxide system.](image)

In brief, it is verified that multicomponent dielectrics provide enhanced insulating properties together with moderate-to-large values of κ, important to assure good transistor performance when large densities of defects need to be compensated. Furthermore, multicomponent dielectrics present a more disordered structure, remaining amorphous for a broad range of processing/annealing temperatures, which is translated not only in lower leakage currents but also in smoother surfaces and improved interface properties, highly important for the integration of these materials in devices.

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Note that these MIS structures comprise crystalline silicon as the semiconductor, instead of the oxide semiconductors that will be used to fabricate TFTs. This can naturally affect the overall J-V characteristics, as the semiconductor-dielectric band alignments are different. Hence, the results presented in fig. 4.39 are only intended for comparison purposes between different dielectrics, while a more “real-world” test will be presented in the next chapter, where the application of these dielectrics to TFT structures will be shown.
4.3. Conclusions

The characterization and discussion presented in this chapter allows to conclude some important aspects regarding the properties of multicomponent semiconductors based on gallium-indium-zinc oxide system and multicomponent dielectrics based on tantalum-silicon and tantalum-aluminum oxide systems. Starting by the oxide semiconductors, the most significant points are:

- Comparing the binary oxides, In$_2$O$_3$, Ga$_2$O$_3$ and ZnO, the former presents the highest growth rate, while the latter presents the lowest, being less than half of the one obtained for In$_2$O$_3$, for the same deposition conditions. The growth rate of the multicomponent oxides reflects these differences, depending on the relative concentration of each metallic cation. Also, the growth rate is severely affected by the deposition conditions, decreasing for higher \%O$_2$, higher $p_{\text{dep}}$ and lower $P_{\text{rf}}$. For $P_{\text{rf}}$, a threshold value higher than 0.6 W cm$^{-2}$ is required to start having a linear growth rate-$P_{\text{rf}}$ relation;

- Structurally, there are significant differences between binary and multicomponent oxides. Concerning binary oxides, as-deposited ZnO films are polycrystalline, with hexagonal wurtzite structure and (002) preferential orientation, while In$_2$O$_3$ films only start to crystallize in the bixbyite cubic system after annealing at 150 °C. For both materials, increased $T_a$ is reflected in improved crystalline quality. Ga$_2$O$_3$ films are amorphous even after being annealed at 500 °C. Multicomponent oxides, whether ternary (IZO, IGO) or quaternary (GIZO) remain amorphous at least until 500 °C, with the only exception being the indium-richer IZO (4:1), that crystallizes around this temperature. This crystallization occurs according to the In$_2$O$_3$ cubic system, although with smaller grain sizes and slight shifts of the peak positions due to distortions in the In$_2$O$_3$ crystal lattice caused by zinc. The effect of \%O$_2$, $p_{\text{dep}}$ and $P_{\text{rf}}$ on GIZO films is also examined, but their structure is not significantly affected by the variation of these deposition parameters, at least within the ranges studied here. Comparing ZnO and GIZO, it is verified that the former presents a considerably higher surface roughness than the amorphous GIZO films (around 4 and 2 nm, respectively), which can be seen as an advantage for the integration of GIZO in electronic devices, where interface control is critical;

- Regarding compositional analysis, it is verified that GIZO films are always deficient in zinc with respect to the target composition, being the largest differences (around 10 % in absolute values) observed for zinc-richer targets (GIZO 2:2:2). The zinc deficiency is compensated by an increase of the indium and gallium concentrations. The reasons dictating these variations in composition are not totally clear, but seem to be related with the multiple phases present in the ceramic targets, which have sputtering yields dependent on a large number of factors, including their gallium-indium-zinc contents. Additionally, it is concluded that larger \%O$_2$ and larger $P_{\text{rf}}$
contribute, respectively, to a decrease and an increase of the indium content in the films relatively to the target composition;

- The (post-)deposition conditions and composition remarkably affect the electrical properties of the oxide semiconductors. \(\%O_2\) is one of the most important studied parameters, since it directly deals with the concentration of oxygen vacancies in the films, hence with the films’ \(N\). As expected, \(\rho\) increases for higher \(\%O_2\), being the magnitude of the variation higher for ZnO than for (G)IZO films, given the polycrystalline structure of the former, where grain boundaries act as preferential paths for oxygen incorporation. Still, for GIZO films annealed at low temperature, \(\rho\) changes around 7 orders of magnitude when \(\%O_2\) is increased from 0 to 10.0 \%. For the higher \(\%O_2\), besides the indium deficiency that contributes to increase \(\rho\), it is suggested that severe bombardment effects by highly energetic oxygen ions may also occur, degrading the electrical performance. ZnO seems to be more sensitive to the bombardment phenomena, with \(\rho\) being raised when low \(p_{dep}\) and high \(P_{rf}\) are used. For (G)IZO the contrary happens, and films deposited under those conditions (low \(p_{dep}\) and high \(P_{rf}\)) yield materials suitable for electrode application, with high \(N\) and low \(\rho\). For the multicomponent oxides, higher \(\text{In}/(\text{In}+\text{Zn})\) atomic ratios favor lower \(\rho\), higher \(N\) and \(\mu\), in agreement to what is verified for the binary oxides that compose them. The same applies for the \(\text{In}/(\text{In}+\text{Ga})\) atomic ratios, but here the effect is even larger, meaning that in GIZO gallium should be the main responsible for suppressing free carrier generation, while zinc has a role more related with the stabilization of the amorphous structure.

\(T_A\) can completely change the electrical properties of a given material. In fact, despite of the deposition conditions, higher \(T_A\) tend to dominate those properties, reducing the discrepancies between films produced under different \(\%O_2\), \(p_{dep}\) and \(P_{rf}\) conditions. The effects of \(T_A\) are different and of various magnitudes, depending on the deposition parameters (for instance, \(\rho\) can increase or decrease with \(T_A\) depending if the films are produced without oxygen or with large \(\%O_2\) and composition, but generally involve oxygen adsorption/desorption processes and structural rearrangement. In extreme cases (IZO 4:1), annealing can also lead to crystallization, negatively affecting the electrical properties due to charge trapping at the grain boundaries and/or increased oxygen adsorption. Additionally, annealing can also reduce the stress effects on films processed under non-ideal conditions. The deposition conditions leading to less variations of the electrical properties with annealing are \(\%O_2=0.4\ \%\), \(p_{dep}=0.7\ \text{Pa}\) and \(P_{rf}=1.1\ \text{W cm}^{-2}\), which interestingly are also the ones allowing to obtain the most stable properties during the 18 months shelf-life tests. Some insights about the conduction mechanisms in binary polycrystalline and multicomponent amorphous oxides are also given, revealing important differences between these materials. For polycrystalline ZnO films thermionic emission over grain boundary barriers seems to be relevant, at least for higher \(T\). Regarding polycrystalline In\(_2\)O\(_3\) films it seems that
three scattering mechanisms are relevant: ionized impurities, lattice vibrations and grain boundaries. Concerning (G)IZO, a percolation conduction mechanism seems to be dominant, where free carriers have to surpass potential barriers around the conduction band edge. These are essentially derived from the random distribution of gallium and zinc cations around the large and overlapping indium 5s orbitals and from some heavily distorted indium-oxygen-metal bonding angles. Thus, in (G)IZO carrier transport (µ) is enhanced with higher N, even reaching a degenerate state, since Er moves away from the conduction band edge, where transport is less affected by those potential barriers. This way, large µ (above 60 cm² V⁻¹ s⁻¹) can be achieved for N comprised between 10¹⁵-10²⁰ cm⁻³. Above this N, typical ionized impurity scattering dominates conduction, reducing µ.

- Optical properties are also briefly explored, revealing that these oxide semiconductors have good transparency in the visible range, with AVT exceeding 80 % and Eopt between 3.2 and 3.8 eV, depending on the deposition conditions, composition and TA. For non-degenerate films, Eopt slightly increases with %O₂, but differences are attenuated for higher TA. On the other hand, Eopt is significantly affected by composition, with the multicomponent oxides exhibiting values intermediate to the composing binary oxides. Still, Eopt maintains similar values for the range of ln/(ln+Zn) ratio studied here, due to the proximity of the In₂O₃ and ZnO bandgaps, but the introduction of gallium increases remarkably Eopt because of the large bandgap of Ga₂O₃. The annealing treatment has a small effect on the optical properties of ZnO, but In₂O₃ shows distinct absorption rise when films annealed at 150 and 200 °C are compared, which is consistent with the structural changes occurring at this temperature range. For resistive (G)IZO films TA only has some effect on the optical properties at 500 °C, but highly conducting (G)IZO films show a gradual enhancement of the transmittance in the near-infrared region as TA increases, due to the decrease of N. Given the degeneracy of those highly conducting films, typical Burstein-Moss shift is verified on them, raising Eopt as N increases. Spectroscopic ellipsometry analysis, even if not explored in detail, reveals to be a powerful technique to analyze oxide semiconductors, with the simulation results showing good agreement with the N values determined by hall-effect and also suggesting improved compactness for higher TA and low %O₂.

Concerning the multicomponent oxide dielectrics, the main aspects to retain are:

- Binary oxides such as SiO₂, Al₂O₃ and HfO₂ have very small growth rates when compared with Ta₂O₅, which grows twice as fast as Al₂O₃, even if using half of the Pₚ. When TSiO or TAO are co-sputtered larger growth rates are obtained, since two sputtering sources are used simultaneously. For TAO s.t., growth rate is intermediate to the ones of the composing binary oxides, similarly to what is verified for the multicomponent oxide semiconductors;
4. Properties of n-type oxide semiconductor and high-k dielectric thin films produced by sputtering

- Although all the tested dielectrics from the tantalum-silicon and tantalum-aluminum oxide systems remain amorphous at least until 300 °C, spectroscopic ellipsometry analysis reveals that the broadening parameter is higher for the multicomponent oxides than for the Ta2O5 films, suggesting higher degree of short-range ordering for Ta2O5 than for multicomponent dielectrics. For dielectrics, it is highly desirable to have amorphous structures, not only due to the better interface related aspects already pointed out for the oxide semiconductors, but also because the grain boundaries in polycrystalline insulators potentiate higher leakage currents.

- Spectroscopic ellipsometry data agrees with the XPS data regarding the composition of multicomponent dielectrics. Adding SiO2 or Al2O3 to Ta2O5 shifts its n-E plot to lower values, toward the ones corresponding to SiO2 or Al2O3, being the shift dependent on the relative concentration of the composing binary oxides, as clearly revealed by the TAO and TAO s.t. compositions. Same trends are verified for Ecpl evolution;

- As expected, TAO and TSiO exhibit κ values intermediate to the composing binary oxides, but always closer to Ta2O5 (24.6), which is the predominant element. TAO s.t. is the multicomponent dielectric having the lowest κ, since it is the one with lowest tantalum concentration. The J-V plots reveal considerable improvements for TSiO, with J being decreased around 2 orders of magnitude when compared with pure Ta2O5, down to values close to the ones obtained for SiO2.

Based on all this and within the range of composition and (post-)processing parameters studied, the best compromise in terms of performance and stability envisaging the application of oxide semiconductors as active layers in TFTs seems to be obtained for GIZO with compositions around 2:4:1 or 2:4:2, %O2=0.4-1.0 %, Pdep=0.7 Pa, Pif=1.1 W cm⁻2 and Ta=200 °C. Regarding the dielectrics, both TSiO and TAO s.t. provide considerable improvements over binary compounds such as Ta2O5, Al2O3 or SiO2, hence they are selected as the preferred dielectrics for integration in devices. All these considerations are important in order to choose the optimal (post-)deposition conditions and target compositions to fabricate TFTs, as will be shown in the next chapter.

4.4. References


4. Properties of n-type oxide semiconductor and high-κ dielectric thin films produced by sputtering


4. Properties of n-type oxide semiconductor and high-κ dielectric thin films produced by sputtering


Chapter 5

Properties of n-type oxide semiconductor-based thin-film transistors

This chapter constitutes the central point of this dissertation, presenting the results regarding the application of oxide semiconductors and high-κ dielectrics to TFTs. Electrical characterization of the devices is discussed in detail concerning the effects of processing and post-processing parameters, semiconductor composition and device structure. The effects of different source-drain materials and passivation layers are also addressed. Stability measurements are another important point focused here, serving to evaluate the reliability of the processed TFTs. The analysis presented in Chapter 4 about materials' properties constitutes the fundamental basis to understand the results obtained in the devices and, as in that chapter, there are two main sections, the first comprising the optimization of oxide semiconductor-based TFTs using a commercial dielectric, the second the application of optimized semiconductor processes to devices employing sputtered high-κ dielectrics.

5.1 – TFTs with PECVD silicon dioxide dielectric

It is well known that the properties of devices are dependent not only on the characteristics of the composing materials themselves but also, and very significantly, on their interfaces. Hence, even if valuable information can be extracted from the analysis of materials' properties presented in chapter 4, a detailed study of oxide semiconductor (post-)processing conditions and composition aiming their optimization for TFT application would not be complete without fabricating and analyzing actual transistors. However, to assure a correct and trustful study, a well known, reliable and reproducible base structure is required, otherwise the effects of the different processing conditions of the material under study can be overshadowed. For a TFT produced at low temperature, the dielectric is probably the most critical layer regarding reliability and reproducibility issues. [1] Thus, to analyze the effect of different (post-)processing parameters and compositions of oxide semiconductors on the electrical properties of TFTs, a 100 nm thick SiO$_2$ dielectric deposited by a well established PECVD process at 400 °C on heavily doped silicon wafers is used. Unless otherwise stated, this is the dielectric used for all the TFTs presented in this section, being preferred over thermally grown SiO$_2$ due to its lower processing temperature, allowing for a more truthful comparison between the oxide semiconductor-based devices produced here and “real-world” TFTs. The effect of different source-drain materials (including contact resistance assessment) and passivation layers are also analyzed using similar device structures. Finally, the stability of TFTs fabricated using different oxide semiconductor processes is evaluated, using constant current stress tests and by measuring their electrical properties during 18 months.
5.1.1. Process flow and device structure

Figure 5.1 shows the 3 superimposed lithographic masks necessary to produce the TFTs. In this structure, gate electrode (silicon) and dielectric layer ($\text{SiO}_2$) are common to all the devices contained in a substrate. Thus, semiconductor, source-drain electrodes and passivation material are the only layers requiring a patterning process. Each 2.5×2.5 cm substrate includes isolated TFTs with different $W/L$, with $W$ and $L$ varying between 15 to 50 and 2 to 50 $\mu$m, respectively. The device structure corresponds to the “staggered bottom-gate” configuration, as initially proposed by Weimer (see p. 17). [2, 3]

![Figure 5.1 - Mask layout used to fabricate the TFTs on commercial Si/SiO2 substrates.](image)

The process flow to produce such devices is depicted in fig. 5.2. Most emphasis was given to the oxide semiconductor sputtering process, which was performed using the same deposition system, conditions and target compositions as the thin films presented in the previous chapter. In fact, given the possibility of mounting substrates in three independent positions of the sputtering system and depositing a film on each one of them separately, the semiconductor layer of the TFTs was produced in the same run as the respective thin films, minimizing eventual process variations. For each deposition, $d$, was decreased relatively to the thin films previously analyzed (by decreasing deposition time) to assure proper TFT operation, being its effect on the electrical properties studied in the range between 5 and 75 nm. Given the enhanced and more stable properties evidenced by multicomponent amorphous oxides in the last chapter, most of the analysis presented in the next sections is devoted to devices employing these oxide semiconductor materials, rather than binary oxides.

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This is accomplished by rotating the substrates where deposition is not desired to a position where they are protected by a shutter, leaving exposed only one of the substrate positions at a time.
For the oxide semiconductor study, TFTs were produced using source-drain electrodes of Ti/Au (around 5 and 70 nm thick, respectively), but the effect of replacing this material by IZO was also studied on optimized GIZO TFTs. The IZO conductive layers were produced in a home-made sputtering system where this process was previously optimized. [4] Since a passivation layer would be required for subsequent integration of TFTs on the active matrix backplanes presented in chapter 6, different materials produced using various deposition techniques were tested for this purpose on selected samples. For these last two sets of experiences (effect of source-drain material and passivation layer) the semiconductor layer was deposited in the same home-made sputtering system used for the conductive IZO electrodes, rather than on the Pfeiffer system.\(^b\)

Annealing treatments on devices, performed before and after passivation layer processing, were also carried out using exactly the same conditions as for the oxide semiconductor films previously analyzed, i.e., using a tubular furnace, in air atmosphere, a 10 °C min\(^{-1}\) heating ramp and maintaining temperatures ranging from 150 to 500 °C for 1 hour. Nevertheless, TFTs were more intensively tested

\(^b\) When compared with the oxide semiconductor films produced in the Pfeiffer system, the ones obtained in the home-made sputtering system present slightly higher \(N\) and \(\mu\) for the same deposition conditions. Hence, to assure the validity of the analysis presented herein, for each study only devices produced in the same sputtering system are compared.
for $T_A \leq 200$ °C, as this corresponds to the range of low-to-moderate temperatures defined as one of the main motivations for this work.

Regarding electrical characterization, the devices were analyzed using the procedures explained in section 3.5. Special relevance is given to transfer characteristics, as they allow extracting a large number of electrical parameters. Transfer characteristics obtained at low $V_D$ are used to extract $\mu_{FE}$, while $V_{on}$, $V_T$, $S$ and On-Off ratio are calculated using transfer characteristics taken at high $V_D$. Output characteristics are used for qualitative evaluation of devices as well as for contact resistance assessment. All the devices were characterized using exactly the same protocol, regarding the order of obtaining each characteristic curve, the number of successive measurements and the range of gate and drain voltages employed. Although this is not particularly relevant for stable transistors, erroneous analysis and comparisons can arise for unstable or non-ideal devices if this is not taken into account.

5.1.2. Influence of semiconductor (post-)processing parameters and composition on the electrical properties of TFTs

In chapter 4 it was shown that the processing and post-processing parameters and the composition play a crucial role defining the properties of oxide semiconductor thin films. This section shows the effect of those parameters and compositions on the electrical properties of oxide semiconductor-based TFTs, fabricated on Si/SiO$_2$ substrates.

5.1.2.1. Percentage of oxygen content in the Ar+O$_2$ mixture (%O$_2$)

As shown in the previous chapter, %O$_2$ is one of the key factors dictating the properties of oxide semiconductors thin films. Thus, the electrical performance of TFTs is also expected to be significantly affected by the %O$_2$ used to produce its oxide semiconductor layer. Figure 5.3a shows the effect of %O$_2$ on the transfer characteristics of oxide TFTs. The semiconductor layer is based on GZO 2:4:2, produced with $p_{dep}=0.7$ Pa and $P_{inj}=1.1$ W cm$^{-2}$, with $d=40$ nm. A low $T_A=150$ °C is used here in order to have large but reproducible variations on the electrical properties arising from changing %O$_2$ (higher $T_A$ would lead to less variations, see also fig. 5.18).
Figure 5.3 – Effect of %O₂ on the electrical properties of GIZO 2:4:2 TFTs annealed at 150 °C: (a) transfer characteristics; (b) \( V_{on} \) and On-Off ratio; (c) \( \mu FE \) and \( S \).

Figure 5.3a shows that as %O₂ increases \( V_{on} \) is shifted toward more positive values. This effect is easily understandable having in mind the field-effect theory and the way the \( E_f \) is shifted with %O₂ on oxide semiconductors. As \( V_G \) increases, the first induced charges need to compensate unfilled traps, including the ones from the bulk semiconductor and the ones arising from its interface with the dielectric. As seen in the previous chapter, higher %O₂ translates in lower \( N \), since oxygen vacancies are the main source of free electrons in oxide semiconductors. A lower \( N \) means that, with zero-gate bias, \( E_f \) is deeper inside the bandgap, away from the CBM. The \( E_f \) location in energy levels deeper in the bandgap is plausible for all the data presented in fig. 5.3a, since for all these thin films \( N<10^{16} \) cm\(^{-3} \) (not measurable in the hall effect system). Hence, for lower \( N \) a larger number of traps have to be filled by the induced charges supplied by \( V_G \) before \( E_f \) reaches tail and extended states, where the induced carriers start to be free to increase \( I_D \). This results in larger \( V_{on} \) for devices having GIZO films with lower \( N \) (higher %O₂). Superimposed to the “natural” free carrier suppression by increased %O₂ mentioned above, the more severe bombardment phenomena by energetic ions for higher %O₂ can also yield a less compact film and generate more defects, both in GIZO’s bulk and at its interface with SiO₂, contributing also to the increase of \( V_{on} \). The fact that GIZO films sputtered with high %O₂ have
lower indium concentration than GIZO films sputtered with low \%O₂ can also affect negatively the performance of the devices, as will be shown in section 5.1.2.3.

The electrical parameters most affected by \%O₂ are \( V_{on} \) and \( \mu_{FE} \), whose trends seem to be related, with lower \( V_{on} \) devices exhibiting larger \( \mu_{FE} \) (figs. 5.3b and 5.3c). This is not strange considering the background given above: for films with higher \( N \) (lower \( V_{on} \)), as \( V_G \) is increased a larger fraction of induced charges is available to drift between source and drain. Since carrier transport on oxide semiconductors is strongly enhanced by a larger concentration of available free charges, \( \mu_{FE} \) is increased. Similar relations were found by other authors. [5-7] Regarding On-Off ratios, all the devices present values between 10⁵ and 10⁷, which are comparable or even superior to the best performing a-Si:H TFTs. This is of great importance regarding their application as switching elements. [3] The \( S \) value is slightly increased for \( \%O₂=10.0 \% \), which is consistent with a larger defect density on GIZO bulk and/or on its interface with SiO₂. [8] The obtained results agree quite well with a model where \( V_{on} \) control is attributed to deep gap states while subthreshold, threshold and On-state current behaviors are attributed to tail states, as proposed by Hsieh et al. In this model, the effect of trap states at the gate-insulator interface is implicitly included in bulk subgap states. [9]

A more clear insight about the \( \mu_{FE} \) evolution with \%O₂ is given in fig. 5.4a, where \( \mu_{FE}-V_G \) plots are presented for the different \%O₂ used to deposit the GIZO layers. Regardless of \%O₂, a remarkable enhancement of \( \mu_{FE} \) (i.e., of transconductance) is verified as \( V_G \) increases. This is a characteristic of these multicomponent oxide semiconductors and is only possible due to the relatively low tail state density of these materials, which allows \( V_G \) to lift \( E_f \) above CBM. [10] In fact, recent studies show that tail state density is reduced by more than two orders of magnitude on GIZO when compared with a-Si:H. [11] Thus, in a-Si:H few electrons exist in the conduction band extended states and even those few are soon annihilated by the creation of dangling bonds, because they are seen as occupying anti-bonding states. [12] All this results in the pinning of \( E_f \) below CBM, which is the fundamental cause of low \( \mu_{FE} \) on a-Si:H TFTs. Getting back to the discussion of fig. 5.4a, it can also be seen that as \( V_G \) increases \( \mu_{FE} \) tends to a constant value and for the higher \%O₂ it even starts to decrease at high \( V_G \). This is related with the fact that for higher gate fields the carriers are more sensitive to the GIZO/SiO₂ interface defects, because they are constrained to move closer to that interface. [13, 14] This reinforces the idea that a higher trap density should exist at this interface for the devices having GIZO films produced with higher \%O₂. Moreover, the fact that \( \mu_{FE} \) changes with increasing \( V_G \) by other means than its direct relation with \( N \) is in total agreement with the model suggested by Haering in 1964 for TFT operation, where it is proposed that a modulation of the mobility occurs by several mechanisms when carriers are injected by increasing \( V_G \). [13, 15]
The properties' degradation for higher %O₂ is also verified by measuring the V_on shift in consecutive transfer characteristics (ΔV_on). This simple procedure is useful to analyze early-stage aging of devices and also to infer about the instability mechanisms that might be present. For instance, it is reported that V_f is shifted using this procedure on In₂O₃ based TFTs, which is attributed to the existence of interface defects. [16] The results obtained using this procedure for the GIZO TFTs analyzed in fig. 5.3 are presented in fig. 5.4b. For devices where GIZO is produced with low %O₂ (0 and 0.4 %) ΔV_on=0 V, which might indicate that a low density of traps exists or that the background N obtained in these films is enough to permit that a low density of unfilled traps exists at zero-gate bias. However, as %O₂ is increased ΔV_on starts to deviate from 0 V toward positive values, reaching 6 V for %O₂=10.0 % (see inset in fig. 5.4b). In this case, a higher trap density could be expected and because the background N is lower a large number of unfilled traps would be present in the unbiased device. Note that this positive ΔV_on shift is consistent with electron trapping at or near the GIZO/SiO₂ interface rather than with more severe instabilities, such as positive or negative ion migration in the insulator, which would lead to a negative ΔV_on. [1] Hysteresis analyses are also performed, and although the verified hysteresis is always clockwise, consistent with trap filling by accumulated electrons (rather than counterclockwise, which might indicate ionic drift), [17] this hysteresis is almost negligible for %O₂=0 and 0.4 % (see inset in fig. 5.4b), but increased to around 6–7 V for %O₂=10.0%. However, even for the high-%O₂ devices, hysteresis almost disappears (or at least is considerably reduced) after the four successive transfer characteristics measurements described above, because after that the accumulated electrons supplied during the previous V_g sweeps are filling most of the existent traps. 

Further evidence that electron trapping at or near the GIZO/SiO₂ interface should be critical for GIZO...
produced with high %O₂ is the recovery of the initial V_on and large hysteresis after a long period of rest time, typically more than one day. This should be related to the slow release of electrons by deep traps and not with some sort of ionic drift because a large amount of energy (only attainable, for instance, by a thermal annealing treatment) would need to be supplied to the device in order for ions to diffuse back to their original positions. [1]

Output characteristics for TFTs where GIZO is deposited with %O₂=0.4 and 10.0 % are presented in fig. 5.5. As already seen in fig. 5.3a, the I_D achieved with lower %O₂ is considerably higher, as a result of the enhanced μFE. Both plots show no evidence of current crowding for the low V_D region, indicative of low series resistance at the source-drain Ti/Au contacts with GIZO. [2, 18] Further considerations about contact reliability will be made in section 5.1.3. Also, good saturation is achieved for both cases, although a slight positive slope is observed for %O₂=0.4 % due to the higher conductance of the bulk semiconductor. Still, both devices exhibit relatively flat saturation regimes, meaning that the entire thickness of GIZO can be depleted close to the drain electrode, leading to the so-called pinch-off effect. Although not evident in fig. 5.5, small negative slopes in the saturation regime are sometimes observed for higher %O₂. This was also reported for oxide semiconductor TFTs in the past and attributed to slow traps near the dielectric/semiconductor interface. [19] The nature of these traps is not known for now, but the fact is that the negative slopes tend to be attenuated and even disappear in some cases, typically after some weeks to months. The annihilation of this effect is probably related with the achievement of equilibrium between the occupancy of the slow traps and the bulk material itself after that time. [13]

![Figure 5.5 - Output characteristics of GIZO 2:4:2 TFTs annealed at 150 °C, for GIZO layers deposited with different %O₂: (a) 0.4 %; (b) 10.0 %.

Based on the results and analysis presented above, the %O₂ conditions yielding best and more stable performance are %O₂=0 and 0.4 %. Nevertheless, during the work of this dissertation, it was found that a better control of semiconductor’s N is achieved with %O₂ ranging between 0.4 and 1.0 %, even
if for %O₂=1.0 % \( \mu T \) and \( \Delta V_{on} \) start to be slightly affected. This is specially relevant for non-annealed devices or for \( T_A<150 \) °C: for these situations, GIZO films produced without oxygen tend to become highly conductive, leading to always-on devices without appreciable channel conductivity modulation (this will be further addressed on p. 175). For the other multicomponent amorphous oxides where a complete %O₂ study was made, IZO 2:1 and GlIZO 2:4:1, similar dependences of %O₂ are observed, but the effects mentioned above regarding films produced without oxygen are even more severe, since these compositions yield films with higher \( N \) than GlIZO 2:4:2. The effect of %O₂ was also studied for polycrystalline ZnO TFTs. For this binary oxide similar effects are verified, although the properties are even more dependent of %O₂ content, i.e., the processing window to obtain good performance devices is considerably narrower than for IZO or GlIZO. For ZnO, with \( p_{dep}=0.7 \) Pa, \( P_{rf}=1.1 \) W cm² and \( T_A=150 \) °C, devices only show significant field-effect for %O₂=0 and 0.4 %. This is in agreement to what was verified in Chapter 4, where ZnO was seen to be highly sensitive to %O₂, much more than (G)IZO, which arises mainly due to the existence of grain boundaries in ZnO, which act as additional paths for oxygen absorption/desorption processes. The deleterious effects of increased substrate bombardment verified for ZnO should also play an important role for this result. In fact, other authors also found ZnO TFT performance to be highly dependent of substrate bombardment: Yao et al. showed that by putting a grounded mesh between the substrate and the target, the On-Off ratio was increased by one order of magnitude, due to less severe substrate bombardment. [20]

The overall control of properties and large process window regarding %O₂ variation achieved for TFTs based on (G)IZO constitutes a great advantage for multicomponent amorphous oxide systems over binary polycrystalline ones.

5.1.2.2. Deposition pressure \( (p_{dep}) \) and rf power density \( (P_{rf}) \)

As seen in chapter 4, the effects of \( p_{dep} \) and \( P_{rf} \) on the electrical properties of oxide semiconductor thin films are somehow similar, since both affect the energy of sputtered and plasma species arriving to the substrate. Figure 5.6a shows the transfer characteristics for TFTs employing a semiconductor layer based on GlIZO 2:4:2, deposited with %O₂=0.4 %, \( P_{rf}=1.1 \) W cm², \( d_s=40 \) nm and different \( p_{dep} \). Final devices were annealed at 150 °C. Extracted electrical parameters are presented in table 5.1.
Figure 5.6 – Effect of (a) $p_{\text{dep}}$ and (b) $P_{\text{rf}}$ on the transfer characteristics exhibited by GIZO 2:4:2 TFTs annealed at 150 °C. Unless otherwise stated, %O$_2$=0.4 % is used for all the semiconductor layers. The inset in fig. 5.6b shows the $P_{\text{rf}}$ effect for non-annealed devices.

Table 5.1 – Electrical properties obtained for the devices depicted in fig. 5.6.

<table>
<thead>
<tr>
<th>$p_{\text{dep}}$ (Pa), $P_{\text{rf}}$ (W cm$^{-2}$)</th>
<th>$\mu_{\text{eff}}$ (cm$^2$ V$^{-1}$ s$^{-1}$)</th>
<th>On-Off ratio</th>
<th>$V_{\text{on}}$ (V)</th>
<th>$V_T$ (V)</th>
<th>$S$ (V dec$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4, 1.1</td>
<td>56.6</td>
<td>--</td>
<td>--</td>
<td>1.0</td>
<td>0.25</td>
</tr>
<tr>
<td>0.7, 1.1</td>
<td>51.7</td>
<td>1.9×10$^8$</td>
<td>-1.0</td>
<td>1.0</td>
<td>0.37</td>
</tr>
<tr>
<td>1.0, 1.1</td>
<td>50.2</td>
<td>3.3×10$^8$</td>
<td>-3.0</td>
<td>0.1</td>
<td>0.26</td>
</tr>
<tr>
<td>0.7, 2.7</td>
<td>52.4</td>
<td>3.3×10$^8$</td>
<td>-1.5</td>
<td>0.3</td>
<td>0.63</td>
</tr>
<tr>
<td>0.4, 2.7 (%O$_2$=10.0 %)</td>
<td>0.02</td>
<td>5.5×10$^3$</td>
<td>6.0</td>
<td>9.3</td>
<td>0.63</td>
</tr>
</tbody>
</table>

The data show that for $p_{\text{dep}}$=0.4 Pa, although a non-negligible field effect and a high $\mu_{\text{eff}}$=56.6 cm$^2$ V$^{-1}$ s$^{-1}$ are obtained, the channel conductivity modulation is rather poor, being the transistor always in the On-state, even for negative $V_G$. This behavior is a direct consequence of a very conductive GIZO film ($\rho$=10$^3$ Ω cm), hence of a large $N$ that cannot be entirely depleted within the $V_G$ range used here. For devices where GIZO is produced at higher $p_{\text{dep}}$, between 0.7 and 1.0 Pa, typical transistor behavior is obtained, but properties are slightly improved for the 0.7 Pa deposited GIZO, being possible to achieve higher $\mu_{\text{eff}}$, closer to 0 $V_{\text{on}}$ and smaller $S$. This should be the consequence of a more compact film structure with a lower number of defects, related to the enhanced sputtered energy and higher diffusion length of species when lower $p_{\text{dep}}$ is used. In fact, spectroscopic ellipsometry analysis confirms that short-range order and density are improved when decreasing $p_{\text{dep}}$ from 1.0 to 0.7 and to 0.4 Pa. The evolution of electrical properties verified from 0.7 to 0.4 Pa is somewhat contradictory compared to what is reported by Jeong et al. for GIZO TFTs, where a large improvement on $S$ was verified for films deposited at lower $p_{\text{dep}}$ without comprising the device’s Off-current and $V_{\text{on}}$. [8] To understand the differences between the two works we must take into account that different processing conditions were used, namely, %O$_2$, which is much higher in ref. [8], and...
5. Properties of n-type oxide semiconductor-based TFTs

target composition, which is 2:2:1 in ref. [8] and 2:4:2 in the present work. As shown in chapter 4, these two parameters have a strong effect on the electrical properties of oxide semiconductor thin films, being expected that the ones produced in this work have considerably lower \( \rho \) (higher \( N \)) than the ones reported by Jeong et al. Thus, even if an improvement on \( S \) is plausible for lower \( p_{\text{dep}} \), given the higher compactness and lower defect density of the GIZO thin films obtained under these conditions, the effect is overshadowed here by a high \( N \), which does not allow for ideal channel conductivity modulation, with the devices always remaining in the \( \text{On} \)-state. This clearly shows that to tailor the oxide semiconductor properties towards a specific application, one needs to have in mind that these properties are affected simultaneously by a large number of (post-)deposition parameters. To reinforce this idea, TFTs were also fabricated using a different GIZO process, with \( p_{\text{dep}}=0.4 \) Pa, \( P_f=2.7 \) W cm\(^2\) and \( \%O_2=10.0 \% \) (fig. 5.6a and table 5.1). The results show that although a low \( p_{\text{dep}} \) and high \( P_f \) are used, both favoring a high \( N \) in the GIZO films, the electrical properties of the devices are rather poor, evidencing a highly resistive semiconductor, with a low \( N \) and a large trap density. In fact, a GIZO thin film produced under these conditions exhibits \( \rho>10^8 \) \( \Omega \) cm. This means that for these deposition conditions, the deleterious effect of using a large \( \%O_2 \) cannot be compensated by using higher \( P_f \) and lower \( p_{\text{dep}} \), which for low \( \%O_2 \) would result in a decrease of \( \rho \) (increase of \( N \)). Actually, for high \( \%O_2 \), given the larger density of oxygen ions in the plasma, an increase of the substrate bombardment by highly energetic oxygen ions can even be expected by using a large \( P_f \) and low \( p_{\text{dep}} \), resulting in degraded film’s properties. This can justify why TFTs with GIZO layers produced under these conditions present considerably worse performance than devices where GIZO is deposited with the same \( \%O_2=10.0 \% \) but with \( p_{\text{dep}}=0.7 \) Pa and \( P_f=1.1 \) W cm\(^2\) (compare with fig. 5.3a).

The effect of \( P_f \) on the electrical properties of GIZO-based TFTs is shown in fig. 5.6b and table 5.1, for GIZO 2:4:2 films deposited with \( \%O_2=0.4 \% \), \( p_{\text{dep}}=0.7 \) Pa and \( d_s=40 \) nm. A low \( \%O_2 \) is chosen to prevent the effects mentioned in the previous paragraph. For non-annealed devices (inset in fig. 5.6b), large differences are verified, with \( P_f=2.7 \) W cm\(^2\) resulting in always-on characteristics due to a low \( \rho \) and large \( N \) (=10\(^{-2}\) \( \Omega \) cm and 10\(^{19}\) cm\(^{-3}\), respectively). On the other hand, GIZO films produced with \( P_f=1.1 \) W cm\(^2\) have \( \rho=10^5 \) \( \Omega \) cm, yielding devices with well defined \( \text{On} \)- and \( \text{Off} \)-states but poor overall performance. The properties of both transistors are impressively improved after a low temperature annealing (150 °C) and interestingly they converge to the same values, despite the \( \rho \) values still exhibit a significant difference (=10\(^{1}\) and 10\(^{5}\) \( \Omega \) cm, for \( P_f=2.7 \) and 1.1 W cm\(^2\), respectively). The different effects of the annealing treatment depending on the as-grown properties of the films are in agreement to what was discussed in the previous chapter regarding material properties and will be further addressed concerning TFT behavior in section 5.1.2.5 of this chapter.
5.1.2.3. Composition (binary and multicomponent oxides)

The composition of the oxide semiconductors has a fundamental role defining their electrical properties, as demonstrated in chapter 4. In this section, the performance of TFTs is discussed regarding the composition of their active layers, both for binary and multicomponent oxide semiconductors. All the films are produced using %O₂=0.4 %, P_{dep}=0.7 Pa, P_{e}=1.1 W cm⁻² and d_e=40 nm, being the final devices annealed at T_a=150 °C. Transfer characteristics are presented in fig. 5.7 and 5.8 for binary/ternary and ternary/quaternary oxides, respectively, being the μFE and V_{on} values presented in the ternary diagram of fig. 5.9.

The analysis of the data allows observing significant differences and trends. Starting by the TFTs comprising binary oxides, large differences are obtained for In₂O₃, ZnO and Ga₂O₃ based devices. This is naturally related with the different electrical properties of the respective thin films. For these deposition conditions, N=10¹⁸ cm⁻³ for In₂O₃, which renders E_F to be very close to CBM, turning impossible to deplete the semiconductor with reasonable V_G values. Hence, even if a very large μ_FE is achieved for the In₂O₃ TFTs, due to the E_F pinning above CBM as V_G is increased, the devices are not usable as transistors, since they cannot be switched off. On the other hand, Ga₂O₃ films have non-measurable ρ (i.e., >10⁶ Ω cm), presumably due to a very low N and large density of empty traps, in addition to the large bandgap, above 4 eV. This results in very poor device performance, with V_{on}>20 V, μ_FE=0.02 cm² V⁻¹ s⁻¹ and large ΔV_{on}, above 6 V, which is not improved even for T_a=500 °C. Chiang et al. also reported similar characteristics for Ga₂O₃ TFTs, with μ_{inc}=0.05 cm² V⁻¹ s⁻¹ and V_{on}>10 V for T_a=800 °C. [6] ZnO seems to be the best binary oxide for TFT application considering the range of deposition conditions used herein. In fact, close to 0 V_{on}, On-Off ratio exceeding 10⁶ and ΔV_{on}=1 V are achieved on these ZnO TFTs. Still, the small slope of the transfer characteristics is synonym of a relatively high S (0.90 V dec⁻¹) and the low maximum I_D is indicative of a low μ_FE (1.6 cm² V⁻¹ s⁻¹) comparatively with the other devices depicted in fig. 5.7. Two reasons can be pointed as the main justification for the moderate performance of the ZnO TFTs: first, ρ=10⁷ Ω cm, which is indicative of low N and/or large unfilled trap densities; second, the existence of grain boundaries, which are associated with depletion regions with high potential barriers that greatly affect the movement of free carriers.

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*[d] In fact, it was verified that the properties of ZnO TFTs are improved by growing the ZnO films under a pure argon atmosphere and keeping all the other deposition parameters unchanged. Although this seems to contradict what is generally found in literature for ZnO TFTs, where most authors have to use arg+O₂ atmospheres to control N to proper levels, one has to have in mind that the overall deposition conditions (and not only %O₂) dictate the final properties exhibited by films and devices and ZnO is particularly sensitive to small changes on the processing conditions.
Multicomponent oxides, in general, allow for considerably better TFT performance than binary oxides. The amorphous structure of these materials turns grain boundaries unimportant and the carrier transport is mostly limited by potential barriers located around the CBM, associated with the structural randomness, which can easily be surpassed in properly processed films (i.e., with adequate %O₂, \( p_{\text{dep}} \) and \( P_{\text{fr}} \), as seen in the previous sections) by increasing \( V_G \). Furthermore, the background \( N \) can be adjusted within a broad range simply by changing the relative proportions of the cations, which is of great relevance since this parameter is perhaps the most important one to control in order to obtain good transistor performance. For IZO based TFTs with \( \text{In}/(\text{In+Zn}) \) atomic ratios between 0.50 and 0.80 it is verified that the properties tend to get closer to the predominant binary oxide, i.e., for \( \text{In}/(\text{In+Zn})=0.80 \) both \( I_D \) and \( \mu_{\text{FE}} \) are similar to \( \text{In}_2\text{O}_3 \) TFTs, while for \( \text{In}/(\text{In+Zn})=0.50 \) the properties start to move away from those of \( \text{In}_2\text{O}_3 \) TFTs toward the ones of ZnO TFTs. Intermediate properties are obtained for \( \text{In}/(\text{In+Zn})=0.67 \). This means that \( N \) and \( \mu_{\text{FE}} \) get higher for increased indium content: for instance, \( \mu_{\text{FE}} \) increases almost three times when moving from IZO 1:1 to 4:1. In agreement with this, only the IZO 1:1 TFTs are able to present clear On- and Off-states within the \( V_G \) range used here. Considerably better device performance is achieved using IGO instead of IZO. When comparing IGO 4:2 with IZO 2:1 (which have similar indium contents relatively to the other composing cation), although \( \mu_{\text{FE}} \) is smaller for IGO, it still exhibits a remarkably high value, around 50 cm² V⁻¹ s⁻¹. In addition, the IGO TFTs present, for these deposition conditions, very good switching performance, such as On-Off ratio\(>10^6 \), \( S=0.25 \) V dec⁻¹ and \( V_{\text{on}}=-1.0 \) V, contrarily to IZO TFTs, that cannot be switched off even with \( V_G=-10 \) V. These differences arise as a direct consequence of the strong bonds that gallium forms with oxygen, [21] suppressing the generation of free carriers and raising \( \rho \), that reaches \( 10^3 \) Ω cm for the IGO 4:2 used here, against \( 10^1 \) Ω cm of the IZO 2:1 film.

\[ \text{Note that even if the In}_2\text{O}_3 \text{ thin films deposited under the conditions used to produce these TFTs are polycrystalline, their high } N \text{ makes them almost unaffected by grain boundary scattering effects, so they can exhibit similar } \mu_{\text{FE}} \text{ to indium-rich multicomponent amorphous oxides.} \]
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Figure

– Effect of oxide semiconductor target composition on the transfer characteristics of TFTs annealed

at 150 °C, with %O₂=0.4 %: ternary and quaternary oxides.

The transfer characteristics of TFTs based on ternary (IZO) and quaternary (GIZO) multicomponent

oxides are presented in fig. 5.8. Regardless of the selected In/(In+Zn) atomic ratio, the addition of

more gallium (i.e., reduction of In/(In+Ga)) considerably shifts V_{on} toward more positive values and

decreases \( \mu_{FE} \), due to the already mentioned decrease of the background \( N \). This is naturally

advantageous for large In/(In+Zn), since it permits to produce TFTs that clearly switch between Off-

and On-states. However, for smaller In/(In+Zn), a careful choice of In/(In+Ga) has to be made: for

In/(In+Ga)=0.50, corresponding to GIZO 2:2:1 and GIZO 2:2:2 compositions, it is verified that the

devices not only exhibit considerably lower \( \mu_{FE} \) and higher \( V_{on} \), but also larger \( \Delta V_{on} \) around 4 and 5 V,

respectively, against \( \Delta V_{on}=0 \) V for the remaining GIZO compositions. These trends are justified by two

factors: first \( N \) is lower, making \( E_F \) to be shifted towards the midgap, thus a larger fraction of the

charges induced by \( V_G \) have to fill empty traps before \( E_F \) reaches CBM or above it, where \( \mu_{FE} \) is

maximized; second, since the ratio of In/(In+Zn+Ga) starts to decrease, the higher structural disorder

close to CBM increases the potential barriers that constrain the movement of free carriers, turning

harder the \( E_F \) shifting above CBM mentioned in the previous point. Naturally, even if this describes

the results obtained here, all this depends on the remaining processing parameters and should not

be taken as an entirely strict rule: in fact, a large number of reports regarding stable TFTs with close

to 0 \( V_{on} \) exist in the literature, for compositions around 2:2:2 and 2:2:1. [8, 22, 23] The trends verified

for In/(In+Zn) in fig. 5.7 can also be observed in fig. 5.8, for fixed In/(In+Ga) atomic ratios, although to

a smaller extend than in gallium-free materials, since the properties start to be essentially dominated

by the gallium content when this element is present. The effect of zinc, besides being a stabilizer of

the amorphous structure, is not totally clear regarding TFT performance. Still, it was consistently

observed that for In/(In+Zn)=0.67, provided that some gallium is included in the structure to inhibit

excessive free carrier generation, improved subthreshold properties were obtained over TFTs with

GIZO films having In/(In+Zn)=0.80. Although a clear explanation for this is not conceivable at this
time, it seems that zinc can somehow contribute to the modulation of the shallow states below CBM and/or to the reduction of interfacial states between GIZO and the dielectric layer, as initially proposed by Iwasaki et al. [24]

Even if in different compositional ranges, recent papers also show similar results regarding the trends on the properties of TFTs depending on oxide semiconductor composition, both for IZO [25] and GIZO-based devices. [24, 26-29] Note that the gallium-indium-zinc oxide region of the ternary diagram explored during this dissertation aims to obtain large $\mu FE$ but controllable $V_{on}$ and $S$, hence the work was more focused on the indium-rich region, with smaller amounts of gallium and zinc.

Despite the increase of $V_G$ above $V_{on}$ leads invariably to the enhancement of $\mu FE$, as predicted by conventional field-effect theory, the transconductance (hence $\mu FE$) is changed in different ways, depending on the composition and structure of the oxide semiconductor material. Figure 5.10 illustrates this for GZO 2:4:2 (amorphous) and ZnO (polycrystalline) TFTs, both having semiconductor layers deposited with $%O_2=0.4 \%$, $p_{dep}=0.7 \text{ Pa}$, $P_{rf}=1.1 \text{ W cm}^{-2}$ and $d_s=40 \text{ nm}$, being the final devices annealed at 150 °C. Given that the PECVD SiO$_2$ has a high breakdown voltage, the $V_G$ range is extended for both cases in order to see all the $\mu FE$-$V_G$ regimes.

Figure 5.9 – $\mu FE$ and $V_{on}$ obtained for TFTs with different oxide semiconductor compositions, in the gallium-indium-zinc oxide system. Devices annealed at 150 °C, with $%O_2=0.4 \%$. The red and yellow symbols denote amorphous and polycrystalline semiconductor films, respectively.
For the GIZO TFT (fig. 5.10a) an almost abrupt increase of $\mu_{FE}$ is verified after $V_{cnt}$, given the small $S$. Physically, $E_F$ is raised very quickly above CBM by $V_{G}$, since the trap density is very low and very large $\mu_{g}$ can be achieved when the small potential barriers associated with structural disorder are surmounted, which happens for $V_g$=20-30 V, where $\mu_{FE}$ is maximum. As $V_G$ gets higher than these values, the conductive channel is drawn closer to the GIZO/SiO₂ interface, which contributes to increased scattering effects of the large density of induced charges, resulting in a decrease of $\mu_{FE}$. [13] An electron injection barrier at the source electrode may also contribute for this drop in $\mu_{FE}$, as proposed by Dehuff et al. [5] A considerably different $\mu_{FE}$-$V_G$ trend is observed for the ZnO TFT (fig. 5.10b). For this case the increase of $\mu_{FE}$ with $V_G$ is much more gradual, essentially due to the polycrystalline structure of ZnO with small grain sizes, hence large density of grain boundaries. Some models describe quite well the behavior of polycrystalline TFTs, namely the one proposed by Levinson in 1982 [30] and more recently the one of Hossain, specifically oriented for ZnO TFTs. [31] From these models it can be seen that the barrier height associated with the depletion regions at the grain boundaries is modulated by the total $N$, which has contributions both of the background $N$ and of the charges induced by $V_G$. Furthermore, for smaller grain sizes the width of the depletion regions can extend deep inside the crystallites and even overlap with adjacent depletion regions, resulting in very high $\rho$. For the ZnO TFTs presented in fig. 5.10b the modulation of these effects by $V_G$ should be dominant and overshadow ZnO/SiO₂ interface scattering, even if $V_G$ is increased up to 100 V. Although measured in a smaller $V_G$ range, Nishii et al. also obtained a similar $\mu_{FE}$-$V_G$ trend in ZnO TFTs. [32] For a large $V_G$ range, saturation (and even decrease) of mobility is observed by Hoffman for $V_G$>70 V, on ZnO TFTs produced on thermal SiO₂. [33] Still, note that mobility is extracted by Hoffman using a different methodology, designated by incremental mobility ($\mu_{inc}$), which probes the mobility of carriers as they are incrementally added to the channel, rather than averaging the mobility of all the carriers present in the channel for a given $V_G$. [33] In fact, by using the more conventional
“average mobility” ($\mu_{\text{avg}}$), physically similar to $\mu_{N}$, mobility saturation is not achieved in Hoffman’s paper. By plotting $\mu_{\text{inc}}$-$V_G$ for the data depicted in fig. 5.10b, saturation is still not obtained, which can be due to different ZnO processing conditions (plausible given the considerably higher $\mu_{FE}$ achieved by Hoffman) and also to the effect of $I_O$ that for the present PECVD SiO$_2$ starts to increase considerably for $V_G$>70 V.

Some comments should also be made regarding the other polycrystalline binary oxide, In$_2$O$_3$. If the devices employing this semiconductor are annealed at a higher $T_A$ to allow for complete crystallization, such as $T_A$=300 °C, intermediate properties to those observed in figs. 5.10a and 5.10b are observed. Although grain boundaries can still affect the movement of the free carriers, their effect should be considerably smaller, given the larger grain size and larger $N$ of this material. Hence, in the unbiased state, most of the traps associated with grain boundaries can be compensated by the background $N$, leaving more of the $V_G$ induced charges available to increase the transconductance.

5.1.2.4. Thickness ($d_l$)

As seen in the previous sections, some oxide semiconductor layers yield “always-on” transistors that cannot be switched off even using a large negative $V_G$. This situation arises as a natural consequence of the high $N$ of those layers, rendering the channel conductivity modulation achieved with $V_G$ ineffective to deplete all those free carriers to attain the Off-state. For these cases, besides changing the composition and/or deposition conditions of the oxide semiconductor, there are two other solutions that can render good performing devices, with well defined On- and Off-states within a reasonable $V_G$ range:

- To use a dielectric layer with a very large $\kappa$, capable of inducing or withdrawing much larger charge densities than conventional dielectrics. For instance, Tokumitsu et al. showed that even a highly conducting ITO film may be used as a channel layer if a ferroelectric film of Bi$_4$La$_{1-x}$Ti$_x$O$_{12}$ (BLT) is used as the dielectric layer. [34] Even if reasonable switching performance can be achieved, with On-Off $\text{ratio}=10^3$, the Off-current is still relatively high, in the range of 100 nA, and large hysteresis arises due to the ferroelectric nature of the dielectric layer. This can be used as an advantage for memory applications, but is undesirable considering other applications, such as the more usual integration in backplanes for displays. The other disadvantage is the fact that generally these very high-$\kappa$ dielectrics require very high (post-)processing temperatures, in the case of reference [34] around 700 °C, rendering them unpractical for low temperature electronics;
• To use very thin oxide semiconductor layers, maintaining all the remaining device structure unchanged.

This last solution was used extensively in this work. To clearly understand the principle, the surface effects of oxide semiconductors have to be briefly reviewed. The TFTs analyzed here have the staggered bottom-gate structure, so a surface of the semiconductor film (from now on designated by “back surface”) is always exposed to the environment. For very thin films, as the ones used here, the control of this back surface has a dramatic effect on the properties exhibited by the oxide semiconductor-based TFTs, because these oxides strongly interact with environmental species such as O₂ and H₂O. [35, 36] Considering that the back surface has a large density of defects such as oxygen vacancies, plausible given that surfaces or interfaces represent discontinuities on the material and oxygen vacancies are the most abundant defect on oxide semiconductors, such defects can work as adsorption sites. [13, 37] The oxygen adsorption at these sites is reported to happen as a two-step process: initially, oxygen is physisorbed, leading to weakly bounded molecules; then, the physisorbed molecules capture electrons from the semiconductor and are converted into chemisorbed and strongly bonded species. [38] This results in the creation of a depletion layer close to the back surface of air exposed oxide semiconductors. This effect is experimentally shown in fig. 5.11 for two non-annealed GIZO TFTs, intentionally produced with a more conductive GIZO film (2:4:1 composition and %O₂=0 %) than the ideal. The transfer characteristics of the devices were measured during two months, but during this period one of them was left in vacuum (only brought to atmospheric pressure to perform the measurements), while the other was left exposed to ambient conditions.

![Image](image_url)

Figure 5.11 – Evolution of transfer characteristics of non-annealed GIZO 2:4:1 TFTs, with %O₂=0 %. Devices stored (a) in vacuum; (b) exposed to air.

The results show that a highly conductive path is always present in the TFTs left in vacuum, because oxygen adsorption was only possible during the time the devices were removed from vacuum (fig. 5.11).
5. Properties of n-type oxide semiconductor-based TFTs

5.11a). Clear On- and Off-states are only achieved after annealing the device in air at 200 °C. On the other hand, the back surface of GIZO in air exposed devices is free to adsorb oxygen. This way, after only 3 days of air exposure the devices already can be switched off applying $V_{\text{on}} = -10$ V and their properties continue to shift until an ideal close to 0 $V_{\text{on}}$ is achieved (fig. 5.11b). Due to this evolution, there is not a great difference on the characteristics after the annealing treatment. Although the exact rate of oxygen adsorption is not determined in the present experience, it is evident that it is a rather slow process, in line with the results obtained by Lagowski et al. and Kang et al., for ZnO and GIZO films, respectively. [35, 38]

The creation of these depletion regions close to the back surface and their interaction with the bulk and front surface (dielectric/semiconductor interface) of the oxide semiconductor layer are the effects dictating the extent of the variations on the electrical properties exhibited by TFTs having different $d_s$. Figure 5.12 shows two extreme cases of $d_s$ variation, one for a high $N (>10^{19}$ cm$^{-3}$) semiconductor (fig. 5.12a), other for a more ideal case, for a semiconductor with $N < 10^{16}$ cm$^{-3}$ (fig. 5.12b). To achieve this, the only process variation is the target composition, which is GIZO 2:8:2 in fig. 5.12a and GIZO 2:4:2 in fig. 5.12b. The other GIZO process parameters are $\%O_2 = 0.4 \%$, $p_{\text{dep}} = 0.7$ Pa and $P_{\text{rf}} = 1.1$ W cm$^{-2}$, being the final devices annealed at 150 °C. Table 5.2 summarizes relevant electrical parameters extracted from the transfer characteristics.

![Figure 5.12](image)

*Figure 5.12 – Effect of $d_s$ on the transfer characteristics exhibited by (a) GIZO 2:8:2 TFTs; (b) GIZO 2:4:2 TFTs. Devices annealed at 150 °C, with $\%O_2 = 0.4 \%$.**
It is readily visible that the transfer characteristics of the $N>10^{19}$ cm$^{-3}$ device are completely changed when $d_s$ is decreased from 40 to 10 nm: properly working devices are obtained using the thinner GIZO layers, with $\mu_{FE}$ not being largely affected. This can be explained by the analysis of band and carrier density diagrams for different values of $d_s$, considering a highly doped semiconductor (fig. 5.13). On this analysis, some modifications are introduced when comparing with the ideal band diagrams presented in fig. 2.8 (p. 20), where work function differences between the gate electrode and the semiconductor ($\Phi_G-\Phi_s$) and interface states were neglected. The situation presented here, without accounting for the effect of the back surface, represents the worst-case scenario for the depletion of the semiconductor bulk, by considering the existence of an accumulation layer at the dielectric/semiconductor interface even at zero-gate bias, created by negative $\Phi_G-\Phi_s$, donor-like interface states and positive charges contained in the dielectric. [13] The semiconductor region close to the back surface is depleted of free carriers due to the interaction of that surface with oxygen, as explained before. The potential difference across the depletion region ($V_{dep}$) is given by: [13]

$$V_{dep} = \frac{qN_y^2}{2\varepsilon_0\varepsilon_s} \quad (5.1)$$

where $q$ is the electronic charge, $y_d$ the width of the depletion layer, $\varepsilon_0$ the permittivity of free space and $\varepsilon_s$ the dielectric constant of the semiconductor.

Considering a high $d_s$ (fig. 5.13a), a region of the semiconductor’s bulk always presents a large $N$, equal to the background $N$, turning the Off-state of the transistor impossible to achieve. To deplete this region, it would be necessary that the dielectric field could penetrate the accumulation layer at the semiconductor/dielectric interface, which involves removing first all the free and trapped electrons from that interface. This could be achieved using a large negative $V_G$. However, such a large $V_G$ is unlikely to be possible, given that it would lead to the breakdown of the dielectric layer.

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1 Note that most of the traps at the dielectric/semiconductor interface should already be filled even if the assumptions of $\Phi_G-\Phi_s<0$ and positive charges contained in the dielectric are not valid, because electrons from the high $N$ semiconductor can be captured by the lower energy trap states at that interface.
The strategy of increasing the dielectric thickness to increase the breakdown voltage is not viable, given that it would also reduce the capacitance, hence the charge density possible to induce/withdraw. Also, using a dielectric with a higher \( k \) would not be a solution to withdraw larger charge densities from the semiconductor, since dielectrics with very large \( k \) fail to present large breakdown fields. [39]

By reducing \( d_s \), the thickness of the semiconductor’s bulk unperturbed by the accumulation and depletion layers at the interface and back surface, respectively, also decreases, and in a limit situation the accumulation and depletion regions almost touch (fig. 5.13b). Eventually, by decreasing \( d_s \) even more, to a value smaller than \( y_d \), the semiconductor region with the background \( N \) is suppressed. By making \( d_s << y_d \), \( V_{dep} \) will be significantly reduced, as it scales with \( y_d^2 \). This allows for unfilled traps and remaining physisorbed oxygen on the back surface to capture electrons from the channel, leading to the full depletion of the entire semiconductor thickness (fig. 5.13c), hence to the Off-state of the transistor. Naturally, for a high \( N \), the magnitude of these effects depends on \( d_s \) itself, on the back surface state density and on the dielectric/semiconductor interface condition. These parameters have a direct effect on the obtained \( V_{on} \) values.

![Figure 5.13 – N and band diagrams for different \( d_s \): (a) high; (b) medium; (c) small.](image)

Note that in the discussion above, it is assumed that the high background \( N \) allows for filling most of the trap levels present at the semiconductor’s bulk at zero-gate bias, since \( E_F \) is already around the CBM in the unbiased state. However, if a lower \( N \) semiconductor is used, \( E_F \) is moved well below CBM and the band diagram of the resulting structure is inevitably changed. Figure 5.12b shows the
evolution of the transfer characteristics with $d_s$ when using a lower $N$ GIZO layer. On this case, a region with large conductance inside the semiconductor’s bulk does not exist, due to the low background $N$. Regarding the dielectric/semiconductor interface, it is unlikely that an accumulation layer is present (or at most it should be considerably less evident than for higher $N$ semiconductors) even if $\Phi_G-\Phi_d<0$ and positive charges exist in the dielectric, because a large number of unfilled traps would exist at this interface, counterbalancing the downward band bending that can exist for the case of a high $N$ semiconductor. Traps would be unfilled at zero-gate-bias because the $E_F$ at the semiconductor would be too low in energy to permit charges to move to those trap states.

Concerning the back surface and the associated depletion region, its trend with $d_s$ would be the same as above, i.e., getting closer and eventually reaching the dielectric/semiconductor interface as $d_s$ is decreased. Still, this movement would be enhanced since larger $y_d$ is expected here, given the lower $N$ ($y_d^{-N^{1/2}}$). Hence, the depletion layer could even reach the dielectric/semiconductor interface in the unbiased state for a relatively large $d_s$, depending on $N$ and on the total surface state density.

Given this background, considering a high $d_s$, the unbiased state results in a low $I_D$ current. Whether this would correspond or not to the Off-state of the TFT (i.e., if $V_{on}$ is 0 or slightly negative) depends essentially on the balance between unfilled trap states at the interface and at semiconductor’s bulk, $\Phi_G-\Phi_d$ and charges lying in the dielectric layer. For this high $d_s$, positive $V_{on}$ can also be obtained if the semiconductor and/or its interface with the dielectric layer possess a large defect density that require a positive $V_G$ to be compensated. This is not the case for the largest $d_s$ presented in fig. 5.12b (80 nm), where a slightly negative $V_{on}$ is obtained.

As $d_s$ is decreased, the depletion layer associated with the back surface reaches the semiconductor/dielectric interface. Hence, before any free charges can be induced by $V_G$, the depletion layer has to be replaced by an accumulation layer at the interface, resulting in a shift of $V_{on}$ towards positive values. This requires an increasingly higher $V_G$ (higher $V_{on}$) as $d_s$ is further reduced, because the dielectric/semiconductor interface is now even more depleted.

When $d_s$ is reduced to very small values (5 nm in fig. 5.12b), the unbiased device is essentially dominated by the properties of both surfaces of the semiconductor film (back surface and interface). Given that $V_{dep}$ is decreased ($y_d$ decreases), a considerable density of the charges induced by $V_G$ can be captured by the back surface traps. Note that a large amount of these traps should be empty in the unbiased state, because there are not enough electrons available at the semiconductor to fill them. Moreover, there is no accumulation channel at the unbiased state to shield the effect of the back surface traps, because the entire semiconductor is depleted, since $d_s<<y_d$. All this results in a large increase of $V_{on}$. Moreover, significant instability also arises for very small $d_s$, as evidenced by the large $\Delta V_{on}$ obtained for the $d_s=5$ nm devices. This can be attributed to the fact that the interface and back surface traps are largely being filled by the charges induced by $V_G$ and not by the semiconductor
itself at the unbiased state. Hence, given that these defect states can behave both as slow and fast traps, [13] various rates of trapping/detrapping processes might occur while $V_{g}$ is being swept. Note that a large $\Delta V_{on}$ is not observed for TFTs employing thin GIZO layers with high $N$ (table 5.2), since on that case most of the traps would already be filled before applying any $V_{g}$.

A considerable decrease of $\mu_{ic}$ is also observed for the TFTs based on GIZO 2:4:2 when $d_s=5$ nm. This should be ascribed to the fact that $d_s$ starts to be comparable to the mean free path of electrons within the channel and their movement starts to be confined essentially to a very narrow region close to the dielectric/semiconductor interface, turning the electrons more sensitive to those interface defects. [13] For such a small $d_s$, another problem can arise, which is the fact that the films may start to become non-continuous or inhomogeneous, degrading the transport properties. [13]

The increased Off-current obtained for higher $d_s$ obscures the effect of the $V_{g}$-induced current, resulting in an increase of $S$ with $d_s$. [40, 41] However, the differences in $I_{on}-$Off observed in TFTs produced on Si/SiO$_2$ substrates are to some extent artificial, arising due to the 100 ms delay times used for the electrical measurements. If lower delay times are used the devices depicted in fig. 5.12b present essentially the same Off-current values, resulting in less discrepancy among the $S$ values. The residual differences can be attributed to the movement of the charge centroid of the induced accumulation layer away from the dielectric/semiconductor interface, increase in the sheet trap density and an increase in the series resistance for higher $d_s$, as proposed by Chiang. [40]

The results discussed above show that within a large $d_s$ range, thickness variation can be a very effective way to control the $V_{on}$ of an oxide semiconductor TFT without considerably affecting the remaining electrical properties, being the extent of $V_{on}$ variation dependent on the background $N$. In fact, this practice was successfully used by Park et al. to control $V_{g}$ on GIZO TFTs between -15 and 0 V. [42] Note that although %O$_2$ also has a significant effect on $V_{on}$ (or $V_{t}$), the variation of this processing parameter also changes considerably other electrical properties, as seen in fig. 5.3.

Even if a $d_s$ study was not done for ZnO TFTs, it is not likely that it would result in an effective $V_{on}$ control. There are at least two reasons for this: first, the crystalline quality is reduced as $d_s$ decreases, which affects the overall device performance, as reported by Remashan et al. and Redinger et al. [43, 44] Still, for very thin ZnO layers (10 nm), it is reported that good properties are achieved on TFTs, due to the amorphous structure possible to achieve with such a low $d_s$. [45] However, a very narrow process window exists for further $d_s$ reduction, because the films would start to become electrically discontinuous close to these $d_s$ values, as mentioned before; second, for the ZnO films obtained on the work of this dissertation very low $N$ is generally obtained, which renders devices with moderately thin ZnO layers to be essentially controlled by unfilled trap states, turning their properties highly unstable.
This shows, once again, that multicomponent amorphous oxides are advantageous for TFTs, not only in the point of view of pure performance, but also due to the larger process flexibility.

### 5.1.2.5. Annealing temperature ($T_A$)

Until now, only TFTs annealed at 150 °C were analyzed. This $T_A$ is ideal for flexible and low-cost electronics, where the maximum processing temperature has to be kept as low as possible. Even without accounting for pure device performance, the low $T_A$ treatment at the end of device production is useful to remove any residual contaminations due to the involved processing steps, namely the lithographic processes, being crucial to enhance the reproducibility and reliability of the transistors. Still, depending on the properties of the as-deposited semiconductor materials, imposed by the target composition, $\%O_2$, $p_{dep}$ and $P_{rf}$ used to produce them, device performance can be greatly affected by $T_A$. Figures 5.14 and 5.15 show this for TFTs employing different oxide semiconductors, all deposited with $p_{dep}=0.7$ Pa, $P_{rf}=1.1$ W cm$^{-2}$ and $d_s=40$ nm, being the final devices annealed until 300 °C.

**Figure 5.14 – Effect of $T_A$ on the transfer characteristics exhibited by TFTs with different semiconductor layers:**

(a) GIZO 2:2:1, $\%O_2=0.4 \%$; (b) GIZO 2:4:2, $\%O_2=10.0 \%$; GIZO 2:8:2, $\%O_2=0.4 \%$; ZnO, $\%O_2=0.4 \%$. 

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Figure 5.15 – Electrical properties obtained for the devices depicted in fig. 5.14, having different oxide semiconductor processes: (a) GIZO 2:2:1, %O₂=0.4 %; (b) GIZO 2:4:2, %O₂=10.0 %; GIZO 2:8:2, %O₂=0.4 %; ZnO, %O₂=0.4 %.

For TFTs employing GIZO 2:2:1 channel layers deposited with %O₂=0.4 % (fig. 5.14a and 5.15a), a significant improvement from non-annealed to Tₘₐₜ=150 °C is verified. The most interesting feature between the two transfer characteristics is that the non-ideality observed for the non-annealed device, in the form of a kink starting at Vₜₐₜ=9 V, disappears after Tₘₐₜ=150 °C. This suggests the existence of trap levels on the non-annealed TFT that are holding back the smooth progress of Eₜ towards (and above) CBM, although the nature of these traps is not clearly understood for now. As the energy range corresponding to these trap levels is surpassed by increasing V_G, all the traps are filled and the newly induced charges become available to raise I_D. This is consistent with the discrete acceptor-trap model proposed by Hong et al. and Wager et al., [1, 46] where kinks are more evident as the trap density increases. The association of these kinks to dielectric/semiconductor trap levels that need to be filled by electrons seems to be plausible because devices produced in parallel but using a high-κ dielectric such as aluminum-titanium-oxide instead of the low-κ SiO₂ generally do not present any kinks and have a more abrupt increase of I_D in the subthreshold region (i.e., lower S). This should be a consequence of different dielectric/semiconductor interface properties and of a
larger capacitance, thus of higher density of charges induced by the high-$\kappa$ dielectric, which allows for easier trap filling. Non-idealities in the form of large kinks in the transfer characteristics were also obtained by Hoffman in zinc-tin oxide TFTs [47] and were also found using some sputtered dielectrics during the work of this dissertation, as will be shown in section 5.2.5. Returning to the discussion regarding the effect of $T_A$ on the GIZO TFTs presented in fig. 5.14a, for $T_A>150 \degree C$ the properties are further improved, suggesting that the density of defect states on the semiconductor and/or at the GIZO/SiO$_2$ interface continues to be reduced and that short-range order is improved. Indeed, this local atomic rearrangement was confirmed by spectroscopic ellipsometry, by the decrease of the broadening parameter [28, 48] for higher $T_A$. Nevertheless, with $T_A=300 \degree C$ the $\rho$ of the GIZO 2:2:1 film continues to be high, around $10^6$, due to its high gallium concentration, resulting in $V_{on}=3 \: V$.

Even if enhanced properties with higher $T_A$ are observed for the previously discussed GIZO TFTs, the magnitude of the improvements is not very large, because the GIZO films are produced with the $%O_2$, $\rho_{dep}$ and $P_{Ar}$ conditions yielding the most stable films, in agreement with what was seen in chapter 4. A different situation is verified for devices employing GIZO films produced under non-ideal conditions, such as $%O_2=10.0 \%$. Figures 5.14b and 5.15b illustrate this for a TFT based on GIZO 2:4:2. The trends with $T_A$ verified in figs. 5.14a and 5.14a are also observed here, but the effects are now much more pronounced, because the as-grown semiconductor is highly resistive, having a large defect density and poor compactness, due to the already mentioned oxygen ion bombardment that occurs when such a high $%O_2$ is used: note, for instance, the large increase of $\mu_{FE}$ between the non-annealed and the $T_A=150 \degree C$ condition, from 0.25 to 30.5 cm$^2$ V$^{-1}$ s$^{-1}$. The predominant causes for this improvement are ascribed not only to weakly bonded oxygen desorption but also to enhanced local atomic rearrangement and overall reduction of the trap state densities, both at semiconductor’s bulk and at its interface with SiO$_2$. In response to these effects, at $T_A=300 \degree C$, GIZO’s $\rho$ decreases around five orders of magnitude relatively to the as-grown value, being obtained $\rho=10^3 \: \Omega \: cm$. Recently, a reduction of trap density near CBM was experimentally verified using C-V measurements in GIZO films after annealing at 300 °C, by Kimura et al. [11]

A distinct behavior with $T_A$ is verified for TFTs having initially highly conductive semiconductor layers. This is evident by using an indium-rich GIZO composition, such as 2:8:2 (figs. 5.14c and 5.14c). Here, only for $T_A=200 \degree C$ it is possible to start observing reasonable channel conductivity modulation, although the devices still remain in the On-state for the range of $V_{gs}$ used here. After annealing at 300 °C, the devices start operating properly, although in depletion mode, with $V_{on}=-7.5 \: V$. For this composition, because the as-deposited films have a very high oxygen deficiency, resulting in $N=10^{20}$ cm$^{-3}$, the evolution of properties with increasing $T_A$ is being controlled essentially by the $N$ variation, that only decreases to $10^{17}$ cm$^{-3}$ range at $T_A=300 \degree C$. Hence, the improvement of
semiconductor/dielectric interface and decrease of the trap states density as \( T_A \) increases are less relevant for this case.

Finally, ZnO TFTs are also analyzed regarding \( T_A \) dependence in figs. 5.14d and 5.15d. The results show that the electrical properties are significantly modified with \( T_A \). The non-annealed devices exhibit rather poor performance, concomitant with a large defect density and low \( N \) of the ZnO films (non-measurable \( \rho \), above \( 10^8 \) \( \Omega \) cm). This is specially important given the polycrystalline nature of this semiconductor, turning the transport mechanism essentially controlled by the depletion layers of the grain boundaries. [1] But given that grain boundaries should behave as preferential paths for interdiffusion processes, the effects of \( T_A \) are enhanced in this material. Hence, \( \rho \) is significantly decreased for \( T_A=300 \) °C, resulting in a large enhancement of \( \mu_{FE} \). However, this is accompanied by a severe decrease of \( V_{on} \), rendering the device to be in the \( On\)-state even for \( V_G=-10 \) V. These results show, once again, the very narrow process window to obtain good performance devices based on ZnO. This process window is highly amplified when using amorphous multicomponent oxides.

Although \( T_A \) above 200-300 °C are of no interest for low-temperature electronics, for an exploratory study selected devices were also annealed at 500 °C, but they generally exhibit degraded properties for this \( T_A \). Figure 5.16a presents typical output characteristics obtained for TFTs annealed at 500 °C, where the semiconductor is GIZO 2:4:1, produced with \%O\(_2\)=10.0 % and \( d_s=40 \) nm.

![Figure 5.16](image)

*Figure 5.16 – Effect of \( T_A=500 \) °C on the electrical properties of TFTs: (a) output characteristics of devices based on GIZO 2:4:1 with \%\( O_2 \)=10.0 %; (b) transfer characteristics and \( \mu_{FE}-V_G \) plots for GIZO 2:4:2 TFTs, with \%\( O_2 \)=0.4 % and annealing treatments performed before or after source-drain deposition. Characteristics of similar TFTs produced on thermal SiO\(_2\) are also shown in (b).*

Three features are immediately apparent from this plot: first, even for \( V_G=0 \) V a large \( I_D \) is obtained (=5 \( \mu A \)), suggesting a very large \( N \) on the semiconductor layer and consequent depletion mode behavior of the transistor; second, severe current crowding exists for low \( V_D \), revealing possible problems at the source-drain contacts; [18] third, the maximum \( I_D \) for large \( V_D \) and \( V_G \) is very small,
around 1 order of magnitude lower than similar devices annealed at 150 °C (compare with fig. 5.5b), which can also be symptomatic of eventual source-drain contacts issues or degradation of the semiconductor/dielectric interface. Regarding the first feature, it was already seen in chapter 4 that \( N \) increases remarkably for IZO/GIZO films annealed at 500 °C (fig. 4.15, p. 104). For the specific deposition conditions used for the GIZO of fig. 5.16a, \( N=10^{18} \) cm\(^{-3} \) is obtained by Hall effect measurements. Although this is already a high \( N \) to render a usable device with \( d_s=40 \) nm, it would still be small enough to allow for complete depletion of a 10nm GIZO film within a reasonable \( V_g \) range, in agreement with the discussion presented in the previous section. To have a more clear evidence of the causes behind the current crowding and lower \( I_d \) after \( T_A=500 \) °C, further characterization was performed on devices produced on top of different dielectrics (PECVD and thermal SiO\(_2\)) and with the annealing treatment executed at different stages, i.e., before and after source-drain deposition. Transfer characteristics of these devices, obtained at low \( V_{ds} \), are shown in fig. 5.16b, for a GIZO 2:4:2 semiconductor, 40 nm thick. For the TFTs where the annealing is performed before source-drain deposition, it can be seen that there is no degradation of \( \mu_{FE} \) even if \( V_{d}=1 \) V, meaning that the performance is not severely affected by the source-drain contact properties. Naturally, given the high \( N \) of GIZO annealed at 500 °C, the device presents always-on characteristics. On the other hand, if the annealing step is made after source-drain deposition, severe \( I_d \) and \( \mu_{FE} \) degradation is observed. This result is a clear evidence that source-drain contact properties degradation is the main mechanism justifying the poor TFT performance after \( T_A=500 \) °C. Current crowding and lower \( I_d \) after annealing GIZO TFTs with molybdenum source-drain electrodes at \( T_A=400 \) °C were also observed by Son et al. and attributed to the formation of a metal oxide layer between the semiconductor and the metal layer. [49] Returning to the results presented in fig. 5.16b, it is also observed that the degradation effect is much more pronounced when PECVD SiO\(_2\) is used as a dielectric.\(^6\) Hence, despite the largest degradation mechanism being attributed to contact related issues (discussed in more detail in section 5.1.3), the dielectric layer and its interface with the semiconductor also seem to play an important role when high \( T_A \) is used, with thermal SiO\(_2\), due to its high thermal stability, allowing for better performance at this \( T_A \) range.

Besides overall properties optimization, a \( T_A \) below 300 °C is also useful to improve the reproducibility of devices (i.e., for semiconductors deposited under intentionally equal conditions) and also to decrease the discrepancies among devices where the semiconductor is intentionally produced under different processing conditions.

To illustrate the first point, 5 TFTs were produced using GIZO 2:4:1 with \( \%O_2=0 \) %. Short pre-sputtering times (less than 5 minutes) were intentionally used to allow for large process variation. [50] The electrical properties of the non-annealed devices are in fact quite different, with some of

\(^{6}\) Note that for low \( T_A \), such as 150 °C, devices produced on PECVD or thermal SiO\(_2\) exhibit similar performance.
them being always-on through all the $V_g$ range, while others reveal good On-Off switching but different $V_{on}$ values (fig. 5.17a). This effect arises mainly due to low pre-sputtering times, which do not allow to establish an equal target surface condition for all the deposited films, and also due to other non-intentional process variations, such as residual water or other residual products arising from lithographic processes that may be stuck at GIZO surface or at its interface with the dielectric. After annealing at 200 °C, the properties of the 5 TFTs become remarkably similar, with $V_{on}$ varying less than 0.5 V and $\mu_{FE}$, $S$ and On-Off ratio presenting negligible variations among all the devices (fig. 5.17b). For less extreme variations on as-deposited devices than the presented in fig. 5.17a, this uniformization is possible to achieve with even lower $T_A$, such as 150 °C.

![Figure 5.17 – Transfer characteristics of 5 similarly processed GIZO 2:4:1 TFTs, with %O2=0 %: (a) non-annealed; (b) annealed at 200 °C.](image)

Regarding devices produced with intentionally different GIZO processes, a good example of properties uniformization is seen in fig. 5.18. Here, for each TFT a GIZO 2:4:1 layer with $d_f=40$ nm was deposited using different %O$_2$, on top of thermal SiO$_2$. As expected, the transfer characteristics present large variations among the devices (fig. 5.18a), being the trend in agreement with what was previously presented in fig. 5.3. The differences are even larger here than in fig. 5.3a because on this case no low-temperature annealing treatment was performed. By using a moderate $T_A=300$ °C, although the same trend with %O$_2$ is still verified, the variations among the different devices are now much smaller, with all the TFTs presenting good performance. As discussed in Chapter 4, the annealing treatment can have different effects, contributing to an increase or decrease of $N$, depending on the as-grown properties of the thin films. A similar effect was also observed by Nomura et al. in GIZO TFTs. [22] Note that the temperatures involved in the uniformization process depicted in fig. 5.18 have to be higher than the ones involved in the phenomena presented in fig. 5.17, since on this case the properties of the thin films are completely different, i.e., the variations observed in non-annealed devices are not attributed only to minor differences on the films or residual contaminations.
Figure 5.18 – Transfer characteristics of GIZO 2:4:1 TFTs produced with different %O₂ on thermal SiO₂: (a) non-annealed; (b) annealed at 300 °C.

The two uniformization processes presented in figs. 5.17 and 5.18 constitute a great advantage regarding the industrialization of amorphous oxide semiconductors technology, since process variations can be significantly attenuated by using a final low temperature treatment, which has the advantage of simultaneously improving device performance and reliability.

5.1.3. Influence of source-drain electrodes material on the electrical properties of TFTs

In order to fabricate TFTs with good electrical properties and to apply them to electronic circuits such as active matrix backplanes, one of the essential requirements is to form good electrical contacts between the semiconductor and the source-drain regions. [51] In fact, several reports in literature concerning oxide semiconductor-based TFTs show important non-idealities on devices attributed to contact effects, such as current crowding in the output characteristics for low V_D, [50, 52-54] μFE degradation and increase of pinch-off voltage. [46]

For most of the oxide semiconductor TFTs demonstrated in literature, a dual layer comprising titanium and gold is used for the source-drain electrodes (for instance [22, 50, 55]). This combination generally allows to obtain reliable Ohmic contacts with low specific contact resistance to ZnO related materials, at least for annealing temperatures up to 300 °C. [56] But naturally, Ti/Au cannot be used for the realization of a fully transparent device, hence IZO electrodes were also explored in this work. Figure 5.19 compares the electrical performance of GIZO TFTs produced with Ti/Au and IZO source-drain electrodes. The GIZO layer was produced with a 2:4:2 target composition, %O₂=0.4 %, p_{dep}=0.7 Pa, P_{rf}=1.1 W cm⁻² and d_s=40 nm. Final devices were annealed at 150 and 300 °C.
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Figure 5.19 – Electrical properties of GIZO 2:4:2 TFTs (%O2=0.4 %) produced with Ti/Au and IZO source-drain electrodes: (a) Transfer characteristics for TA=150 °C; (b) μFE-Vg plots for TA=150 and 300 °C; (c) Output characteristics of TFTs with Ti/Au electrodes, annealed at 300 °C; (d) Output characteristics of TFTs with IZO electrodes, annealed at 300 °C.

The properties at TA=150 °C are quite similar for both source-drain materials, as illustrated by the transfer characteristics in fig. 5.19a and by the μFE-Vg plots in fig. 5.19b. As pointed out before, the low TA helps to improve reliability and reproducibility on the devices and in some cases it allows to reduce current crowding effects typical of some non-annealed devices, as was also observed by Liu et al. [53] The largest dissimilarities are the V_on values (~0.5 and 0.5 V for IZO and Ti/Au, respectively) and the μFE degradation occurring at high Vg for IZO electrodes. When annealed at 300 °C, both devices show a decrease on μFE, but the effect is much more pronounced for IZO, which starts presenting noisy characteristics, specially for large Vg. This is further evidenced by the output characteristics of the TA=300 °C TFTs, presented in figs. 5.19c and 5.19d for Ti/Au and IZO electrodes, respectively. The insets in these figures show that for low Vd (i.e., linear region) Ti/Au electrodes allow for larger Id and less current crowding effects than IZO.

Some contradiction seems to exist comparing the results presented in the previous section and the ones in fig. 5.19. It was seen before that increasing TA up to 300 °C improves μFE, but here μFE is
slightly decreased at this temperature, even considering Ti/Au source-drain electrodes. However, note that the semiconductor layer is different in the two situations: even if optimal\(^b\) \(\%O_2\), \(\rho_{\text{dop}}\) and \(P_{\text{rf}}\) were used, for instance, on the devices of fig. 5.14a, the fact that the films are based on a GIZO composition with high gallium content results in very large \(\rho\). Hence, improvements on the GIZO layer and on its interface with SiO\(_2\) are expected to be predominant with increasing \(T_A\), as discussed before. On the other hand, for the devices presented in this section, the same deposition conditions were used for the GIZO layer but its composition is different (GIZO 2:4:2). For this case, by analysis of the thin films, very small \(\rho\) changes are observed for \(T_A\) between 150 and 300 °C. Hence, other factors such as source-drain/semiconductor contact properties are expected to be dominant to explain the variation of device properties with increasing \(T_A\).

Non-idealities at the source-drain/semiconductor contact region on TFTs can generally arise due to the creation of Schottky barriers and due to large contact resistance, although sometimes both are simply defined as “contact effects”. [57] Also, given that the GIZO TFTs proposed here do not have a highly doped layer between the source-drain electrode material and GIZO (contrarily to what generally happens in a-Si:H TFTs [58, 59]), the properties at the contact region are dominated by the bulk characteristics of the involved materials and most importantly by their interface. To understand this and correlate the theory with the results obtained on this section, some fundamental properties of metal-semiconductor junctions are briefly introduced in the following paragraph.

When a metal and a semiconductor are joined there is charge transfer between both materials until their \(E_f\) are aligned.\(^1\) The direction of charge flow is dictated by the work function differences of the metal \((\Phi_m)\) and semiconductor \((\Phi_s)\). Figure 5.20 illustrates the three possible situations, for \(\Phi_m<\Phi_s\), \(\Phi_m=\Phi_s\) and \(\Phi_m>\Phi_s\). [60]

![Figure 5.20 – Band diagrams of different metal-semiconductor contacts, before (upper) and after (lower) contact: (a) accumulation; (b) neutral; (c) depletion. [60]](image)

\(^b\) In this context, optimal means that these conditions allow for the smaller variations on electrical properties with increasing \(T_A\), as shown for thin films analyzed in Chapter 4.
\(^1\) For simplicity, no interfacial layers are considered in this exposition.
The barrier height ($\Phi_b$) formed after contact is given by $\Phi_b=\Phi_{he}-\chi$, where $\chi$ is the electron affinity of the semiconductor. [60, 61] Following the nomenclature of Schroder, the three contacts presented in fig. 5.20 are designated by accumulation, neutral and depletion contacts, respectively. Although accumulation-type contacts would naturally be preferred to achieve good ohmic behavior, in practice, with most of the materials depletion-type contacts are obtained. Hence, to have an ohmic contact, most work is focused on decreasing $\Phi_b$ as well as the depletion layer width (defined here as $x_d$, to distinguish it from the depletion layer at the semiconductor back surface, $y_d$), which depends on $N^{1/2}$. In fact, for very thin depletion regions, even if $\Phi_b$ is relatively high, carriers can tunnel trough instead of going over the potential barrier (field emission rather than thermionic emission). [60, 61]

Considering the same $\chi$ for both devices in fig. 5.19, $\Phi_b$ is higher when IZO is used for source-drain electrodes, because $\Phi_{IZO}=4.8$ eV and $\Phi_{Ti}=4.3$ eV ($\Phi_{IZO}$ and $\Phi_{Ti}$ were measured by Kelvin probe). In addition, Shimura et al. suggest that the GIZO layer can be slightly oxidized during the IZO electrodes sputtering process, decreasing $N$. [62] If this is the case, it results in the widening of the depletion layer, but given the linear I-V characteristics obtained for IZO electrodes at $T_a=150$ °C, it seems that this effect is not particularly relevant here, at least to the extent of significantly inhibiting tunneling of electrons through the potential barrier of the contact. Interface quality between IZO and GIZO is expected to be good, with low density of defects, given the similar amorphous structures and smooth surfaces of both materials. On the other hand, it is reported that very thin TiO$_x$ layers are created when Ti is deposited on top of oxide semiconductors, such as ZnO, even before any annealing treatment. This is attributed to the very high affinity of titanium with oxygen. [63, 64]

Although the formation of this TiO$_x$ interfacial layer could be seen as disadvantageous for good contact properties, the fact is that it increases $N$ near the semiconductor surface (via oxygen vacancies creation), resulting in easy tunneling of carriers through the thin oxide barrier. The Au film on top of the very thin Ti layers prevents oxidation of the bulk electrode when exposed to air. Due to the combination of these phenomena, the properties of GIZO TFTs employing whether IZO or Ti/Au source-drain electrodes are similar when $T_a=150$ °C.

When $T_a$ is increased to 300 °C, several effects are observed at the contacts that might justify the large differences obtained in terms of device performance. Regarding IZO, its $\Phi_M$ is increased due to the shifting of $E_F$ towards the midgap, in response to the decreased $N$. This results in a significant increase of IZO's $\rho$ by almost one order of magnitude relatively to $T_a=150$ °C and in a larger $\Phi_b$, degrading contact properties (again, note that the GIZO films used herein do not present significant electrical performance variation between $T_a=150$ and 300 °C). For Ti/Au electrodes, important chemical modifications occur, which are illustrated by TOF-SIMS results for Si/SiO$_2$/GIZO/Ti/Au structures, non-annealed and after $T_a=250$ °C (fig. 5.21). It can be seen that the relatively sharp

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$^1$IZO is considered here as a metal, given its high degeneracy.
interfaces of non-annealed structures are replaced by broad interfaces, suggesting interdiffusion of elements. Similar effects were verified in Ti/Al/Pt/Au contacts on ZnO. [56] Besides the increased oxidation of Ti that could arise as a consequence of a higher $T_a$, (this could not be confirmed by the current TOF-SIMS setup, given the low signal obtained for oxygen) the interdiffusion effects should even allow some Au to reach the Ti/GIZO contact layers, changing significantly the overall contact properties. For Au-richer interfaces, a higher $\Phi_M$ (thus $\Phi_B$) is expected, given that $\Phi_{Au} > \Phi_{Ti}$. In agreement with this, note that pure Au source-drain electrodes (i.e., without the thin Ti layer) are reported to result in worse performing GIZO TFTs, namely in terms of $\mu_{FE}$ and $V_T$. [62]

\[ R_T = \frac{V_D}{I_D} = r_{ch} L + 2R_{SD} \]  

(5.2)

where $r_{ch}$ is the channel resistance per channel length unit and $2R_{SD}$ is the total (source+drain) series resistance. $R_{SD}$ includes the contributions both of the contact itself as well as the semiconductor regions between the contact and the channel. $R_T$ can also be related with $\mu_{FE}$ and $V_T$ by:

\[ R_T = \frac{L}{\mu_{FE} C_t W (V_G - V_T)} \]  

(5.3)

But since $R_T$ includes the contribution of $R_{SD}$, equation 5.3 can also be written considering the intrinsic semiconductor mobility and threshold voltage, $\mu_t$ and $V_{Tt}$ by:

\[ r_{ch} = \frac{1}{\mu_t C_t W (V_G - V_{Tt})} \]  

(5.4)
The determination of these parameters involves plotting $R_T$ for different $V_G$ and $L$ and fitting the experimental data with linear curves for each $V_G$ (fig. 5.22a). The intercept with the $R_T$ axis yields $2R_{SD}$, whereas $r_{ch}$ is given by the slope, according to equation 5.2. Plotting the reciprocal of $r_{ch}$ as a function of $V_G$ (fig. 5.22b) and fitting the results with equation 5.4 gives $\mu_i$ (slope) and $V_{Ti}$ ($V_G$ axis interception).

![Graphical examples of the main steps involved in the determination of contact resistance and intrinsic semiconductor parameters by TLM](image)

Table 5.3 shows the $\mu$ and $V_{Ti}$ values obtained according to this methodology for the $T_A=150$ and 300 °C TFTs with IZO and Ti/Au source-drain electrodes depicted in fig. 5.19.²

<table>
<thead>
<tr>
<th>Source-drain material, $T_A$ (°C)</th>
<th>$\mu_{FE}$ (cm² V⁻¹ s⁻¹)</th>
<th>$\mu_i$ (cm² V⁻¹ s⁻¹)</th>
<th>$V_{Ti}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IZO, 150</td>
<td>52.7</td>
<td>55.4</td>
<td>5.44</td>
</tr>
<tr>
<td>Ti/Au, 150</td>
<td>54.9</td>
<td>57.1</td>
<td>5.89</td>
</tr>
<tr>
<td>IZO, 300</td>
<td>=40</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Ti/Au, 300</td>
<td>50.5</td>
<td>60.2</td>
<td>5.17</td>
</tr>
</tbody>
</table>

The results are in agreement with the considerations made above regarding device performance degradation for higher $T_A$. In effect, while $\mu$ is only marginally larger than $\mu_{FE}$ for $T_A=150$ °C devices, a considerable difference is observed for $T_A=300$ °C. Still, by comparing $\mu_i$ and $V_{Ti}$ for 150 and 300 °C annealed TFTs with Ti/Au electrodes, it can be seen that they are enhanced for the higher $T_A$, meaning that the intrinsic properties of the semiconductor and/or its interface with the SiO₂ layer.

² The results are not presented for TFTs employing IZO source-drain electrodes with $T_A=300$ °C, since for this case it is not possible to have reliable and reproducible measurements of device characteristics, resulting in large deviation of the linear fittings from the experimental data.
are improved but the extrinsic properties are degraded due to contact effects. Besides experimental errors arising from the multiple fitting procedures, the slightly lower $\mu$, for $T_A=150$ °C devices having IZO electrodes may be related with the possible oxidation of GIZO during IZO deposition, decreasing its $N_e$ as proposed by Shimura et al. [62]

The width-normalized $2R_{SD}$ and $r_{ch} \times L$ values can also be plotted against $V_G$ to infer about their relative contributions to $R_T$. This is shown in fig. 5.23a for $T_A=150$ °C IZO and Ti/Au devices, neglecting the small differences of $r_{ch}$ for both TFTs.

As expected, the series resistance contribution using either IZO or Ti/Au is essentially the same, only marginally larger for the former. This figure also shows other important aspects:

- Both $r_{ch}$ and $2R_{SD}$ decrease with increasing $V_G$. The large $r_{ch}$ dependence on $V_G$ would be expected at the light of field-effect theory, since more carriers are being induced in the channel as $V_G$ increases. Regarding the $2R_{SD}$ dependence, one should account for the fact that source-drain to gate overlap is full for the present devices, since the silicon wafer works as the gate electrode. Hence, carriers are also induced in the GIZO regions outside the channel length defined by $L$, reducing the overall series resistance as $V_G$ increases. In a-Si:H TFTs similar relations were found, being the $R_{SD} \cdot V_G$ dependence considerably lower for reduced source-drain to gate overlaps; [67]
- For $L$ between 15 and 5 μm $R_{SD}$ starts to be similar or even higher to $r_{ch}$. This is extremely relevant for designing TFTs based on the current processes and materials, since it indicates that for this $L$ range the device properties start to be dominated by contact effects rather than intrinsic semiconductor and dielectric/semiconductor interface characteristics.
The same principle can be used to compare devices annealed at different temperatures, as presented in fig. 5.23b for TFTs employing Ti/Au source-drain electrodes. As expected by the previous analysis, $R_{SD}$ increases after $T_a=300 \, ^\circ\text{C}$, revealing degraded contact properties. Additionally, $r_{ch}$ slightly decreases for $T_a=300 \, ^\circ\text{C}$, confirming the small $\rho$ variation verified on thin films produced under the same conditions. Furthermore, while TFTs annealed at 150 °C only show $R_{SD}>r_{ch}$ for $L=5-10 \, \mu\text{m}$, the $R_{SD}$ of TFTs annealed at 300 °C is already comparable to $r_{ch}$ for $L=15 \, \mu\text{m}$, meaning that contact resistance starts to be critical for larger $L$ devices as $T_a$ increases.

In recent reports related with GIZO TFTs using MoW source-drain electrodes, authors found the devices to be contact limited at considerably larger $L$, around 30 \, \mu\text{m}. [23, 68] Although the source-drain material selection seems to be able to justify the difference by itself, the question remains if the GIZO deposition conditions and composition can also affect this. To clarify this, the width normalized $2R_{SD}$ and $r_{ch}\times L$ plots are presented in fig. 5.24 for TFTs having non-ideal GIZO layers, produced with 2:2:1 composition, %O$_2=10.0 \%$, $\rho_{dep}=0.7 \, \text{Pa}$, $P_r=1.6 \, \text{W cm}^{-2}$ and $d_e=40 \, \text{nm}$, being the final devices annealed at 150 °C.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{figure5_24.png}
\caption{Width-normalized $2R_{SD}$-$V_g$ and $r_{ch}$-$L$-$V_g$ plots for TFTs employing a non-ideal GIZO process (2:2:1, %O$_2=10.0 \%$), with Ti/Au source-drain electrodes and $T_a=150 \, ^\circ\text{C}$.
}
\end{figure}

The results show that, in fact, the semiconductor layer can greatly affect both $2R_{SD}$ and $r_{ch}$ and devices start to be contact limited for $L$ above 15 \, \mu\text{m}, even if the TFTs were only annealed at 150 °C. A large increase of $r_{ch}$ when compared with the values presented in fig. 5.23 would be expected, since both composition and processing parameters greatly affect intrinsic semiconductor properties, as seen before. Regarding the increase of $2R_{SD}$, it should be ascribed not only to the higher $\rho$ of the access regions inside the GIZO layer but also to degraded metal/semiconductor contact properties. In fact, both $\Phi_B$ and $x_d$ are expected to be larger for the present case: regarding $\Phi_B$, it should be increased due to the higher gallium content of GIZO, which makes its $\chi$ become lower, since Ga$_2$O$_3$
Transparent oxide TFTs: production, characterization and integration

has lower $\chi$ than any of the other binary oxides present in GIZO (ZnO and In$_2$O$_3$). [28] Given the lower $N$ of GIZO, $x_d$ is also increased, as $x_d$ scales with $N^{-1/2}$, as mentioned before.

By using the TLM analysis it is also possible to calculate the effective contact resistance ($r_{c eff}$), defined as the sum of the source (or drain) contact resistivity and the bulk resistivity associated with the access region between the contact and the channel. This can be calculated from the source-drain contact characteristic length ($L_T$), i.e., the dimension of the effective contact area, according to: [65]

$$r_{c eff} = W L_T^2 r_{ch}$$ (5.5)

For source-drain to gate overlaps much higher than $L_T$, which is the case here since the overlap is full (non-patterned gate electrode), $L_T$ can be determined by:

$$L_T = \frac{R_{SD}}{r_{ch}}$$ (5.6)

$L_T$ is a critical design parameter for TFTs to be integrated in circuits, as it defines the minimum source-drain to gate overlap for which the contact dimension does not affect $R_{SD}$. Although for the devices presented in this chapter this overlap is the highest possible, it should be reduced for circuit applications, as large overlaps induce large parasitic capacitances that degrade device performance. [69]

The $r_{c eff}$ values obtained for TFTs with Ti/Au electrodes produced in similar conditions as the ones discussed in fig. 5.19, annealed at different temperatures and with different GIZO thickness are depicted in fig. 5.25.

![Figure 5.25 – $r_{c eff}$–$V_G$ plots for GIZO 2:4:2 TFTs (%O$_2$=0.4 %) having Ti/Au electrodes, with different $d_s$ and $T_A$.](image)

A clear dependence of $V_G$ is verified, which should mostly be related with the $p$ modulation of overlapping regions close to the channel by $V_G$, assuming that contact resistivity is essentially $V_G$ independent. [2] $r_{c eff}$ increases with $T_A$, given the contact resistivity degradation mentioned before. A helpful feature to improve device performance is also shown in this figure: by reducing $d_s$ to a level
where \(\mu_{\text{te}}\) and \(V_T\) are still not significantly affected \(r_{\text{eff}}\) can be decreased, since the distance of the access region in GIZO's bulk is reduced. These \(r_{\text{eff}}\) values are around one to two orders of magnitude lower than the ones generally obtained for α-Si:H TFTs. [65, 67]

Regarding \(L_T\), it does not show a significant trend with \(V_G\), but their absolute values change with \(T_{\text{Ar}}\) from 4 to 7 \(\mu\)m as \(T_{\text{Ar}}\) increases from 150 to 300 °C.

Contact properties can generally be improved by surface cleaning or modification processes of the semiconductor surface. [64] For the specific case of oxide semiconductor TFTs, different approaches have been tested, such as the usage of a highly conductive buffer layer between the semiconductor and source-drain electrodes, either created by plasma treatments of the semiconductor surfaces or by the deposition of a highly conductive semiconductor layer (e.g., without introducing oxygen) on those surfaces. [68, 70-72] Other approaches involve producing coplanar homojunction structures, where \(\rho\) of the semiconductor layer is modified at the source-drain regions by depositing passivation layers (this effect will be explored in section 5.1.4). [51] Even if none of these procedures were used in the current work, comparable or even lower width-normalized \(R_{\text{SO}}\) values are achieved for optimized TFTs, revealing that the overall (post-)processing parameters and material choices are critical to minimize contact effects.

### 5.1.4. Influence of passivation layer on the electrical properties of the TFTs

Passivation is a crucial step to protect the devices from subsequent processes, such as the integration with liquid crystal cells or OLEDs. [51] Passivation also has an important role in isolating the devices from the environment, a concern specially relevant not only for organic semiconductors but also for oxide semiconductors: for instance, the electrical properties of GIZO TFTs are reported to significantly change when the devices are exposed to a high humidity environment. [36] Also, passivation layers are useful to protect the surface of oxide semiconductors from ionic damage due to source-drain reactive ion etching (RIE) processes in staggered bottom gate structures. [23, 73] Additionally, it was also reported by Lee et al. that variation of TFT performance across large area substrates is greatly decreased after passivating devices with \(\text{SiO}_x\). [74]

Even if passivation seems to bring several advantages, it is imperative to study how it affects the electrical properties of oxide semiconductor-based TFTs. For this, similar TFTs employing a GIZO layer with a 2:4:2 composition, \(%\text{O}_2=0.4\ \%\), \(p_{\text{ar}}=0.7\ \text{Pa}\), \(P_{\text{ir}}=1.1\ \text{W cm}^{-2}\) and \(d_s=40\ \text{nm}\) were produced and passivated with different materials, deposited with various techniques: SU-8 by spin-coating, MgF\(_2\) and \(\text{SiO}_2\) by e-beam evaporation and \(\text{SiO}_2\) by sputtering. All the passivation layers were \(\approx200\ \text{nm}\) thick, except for the SU-8, which was considerably thicker, \(\approx10-20\ \mu\text{m}\), due to the available SU-8
formulation at the laboratory. Annealing treatments at 200 °C were performed before and after the passivation layer deposition.

Figure 5.26 shows the transfer characteristics obtained before (fig. 5.26a) and after (fig. 5.26b) the second annealing step, being relevant electrical parameters presented in table 5.4.

![Figure 5.26](image)

Table 5.4 – Electrical properties obtained for the devices depicted in fig. 5.26b.

<table>
<thead>
<tr>
<th>Passivation layer</th>
<th>( \mu_F ) (cm² V⁻¹ s⁻¹)</th>
<th>( V_{on} ) (V)</th>
<th>On-Off ratio</th>
<th>S (V dec⁻¹)</th>
<th>( \Delta V_{on} ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-passivated</td>
<td>59.6</td>
<td>-1.0</td>
<td>9.2×10⁷</td>
<td>0.30</td>
<td>0.1</td>
</tr>
<tr>
<td>SiO₂ (e-beam)</td>
<td>60.9</td>
<td>&lt;&lt;-10.0</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>SiO₂ (sputtering)</td>
<td>83.5</td>
<td>&lt;&lt;-10.0</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>MgF₂ (e-beam)</td>
<td>61.8</td>
<td>&lt;&lt;-10.0</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>MgF₂ (e-beam) @ 300 °C</td>
<td>57.8</td>
<td>-7.5</td>
<td>4.9×10⁷</td>
<td>0.68</td>
<td>-0.5</td>
</tr>
<tr>
<td>SU-8 (spin-coating)</td>
<td>61.2</td>
<td>-3.0</td>
<td>9.4×10⁹</td>
<td>0.28</td>
<td>0.2</td>
</tr>
</tbody>
</table>

It is clear that the passivation layer severely affects the electrical properties of the devices, being the most striking effect a shift of \( V_{on} \) towards highly negative values. In fact, for non-annealed TFTs only SU-8 allows to obtain clear channel conductivity modulation, although with a \( V_{on} \) slightly lower than -10 V. After annealing, the performance of the passivated devices is improved, with SU-8 allowing to obtain almost similar performance as non-passivated devices. Still, all the other passivants continue to render always-on transistors. A transfer characteristic is also shown for a 300 °C annealed TFT with MgF₂ passivation layer deposited by e-beam evaporation. For this case it already starts to be possible
to deplete the GIZO layer with \( V_{\text{on}} = -7.5 \) V, but the devices present some instability, with \( \Delta V_{\text{on}} = -0.5 \) V and a shift of the characteristics to lower \( V_{\text{on}} \) after some time of device production.

The results can be understood by investigating the effects occurring at the air-exposed surface of GIZO. As mentioned in p. 164, in a non-passivated oxide semiconductor oxygen is physisorbed at the back surface, creating acceptor-like surface states that attract electrons from the semiconductor. This gives rise to a depletion region in the semiconductor close to that surface and allows obtaining good performing devices, with well defined \textit{Off} and \textit{On}-states, even for large \( N \). Consider now the deposition of a passivation layer on top of the back surface: when this happens, oxygen can no longer be adsorbed and the depletion layer is not formed anymore. Indeed, an accumulation layer can even appear at this surface if oxygen vacancies are created during the passivation layer deposition (for instance, by breaking of metal cation-oxygen bonds [49, 75]) and/or if the passivation layer has a large density of positive charges. Moreover, this effect is even magnified if the semiconductor has a relatively large \( N \), because on that case the depletion layer in the non-passivated material is thinner (\( \nu_c \sim N^{-1/2} \)) and \( E_l \) in the unperturbed region of the semiconductor is very close to CBM, so a minor accumulation layer of electrons can lead to a dramatic increase of \( N \) and consequently to non-desirable \( I_D \) flowing in the zero-gate bias state. This naturally results in the degradation of the electrical properties of the TFTs, leading in extreme cases to devices that cannot be switched off even with a large negative \( V_G \).

Given this background, the different results depicted in fig. 5.26 and table 5.4 can be understood based on the passivation material and on its deposition technique. For vacuum deposition techniques (e-beam and sputtering), some of the oxygen lying at GIZO’s back surface can be removed during pump down time. This way, the semiconductor region close to the back surface is no longer depleted. Furthermore, during sputtering deposition, the intense substrate bombardment can break weak metal cation-oxygen bonds, generating oxygen vacancies that increase \( N \). This was in fact observed by different authors when exposing a GIZO surface to RIE or to \( \text{N}_2 \) and \( \text{NH}_3 \) plasma treatments.\(^1\) [23, 49, 73] If superimposed to this the deposited passivation layer has a large density of positive charges at its bulk and/or close to its interface with the semiconductor, a significant electrons accumulation layer is created close to its back surface, turning the channel conductivity modulation hard to achieve, even for a large negative \( V_G \). Considering this, the most dramatic effect is observed for sputtered \( \text{SiO}_2 \), then for e-beamed \( \text{SiO}_2 \) and \( \text{MgF}_2 \). For these materials, after \( T_A = 200 \) °C, some improvements are observed, mainly for the e-beamed materials, possible due to the decrease of the density of charges on (or close to) their interface with GIZO. Since the annealing

\(^1\) Note that in the case of plasma species containing \( \text{H}^+ \), the incorporation of this element in oxide semiconductors can also form shallow donor states that contribute to the increase of \( N \), as confirmed by first-principles calculations for GIZO. [76] On the other hand, for oxygen containing plasmas, the incorporation of this element can lead to acceptor-like surface states that reestablish the depletion layer close to the oxide semiconductor’s back surface. [43, 49, 75]
treatments were performed in air and due to the relatively large density of pinholes of these passivation layers, it is also plausible to assume that during annealing some oxygen could easily diffuse through these pinholes and reach the GIZO/passivation layer interface. A second annealing step was also used in other works in literature to turn the properties of passivated devices similar to the ones obtained before passivation. [77, 78] Still, in the present work, all these passivation layers continue to result in always-on devices. The effect of $T_a=300$ °C is also shown for MgF$_2$, being visible that the Off-state can be achieved, although with a highly negative $V_{dd}$ ($V_{on}=-7.5$ V). Moreover, these transistors exhibit a negative $\Delta V_{on}$ and counterclockwise hysteresis, which can mean that ionic drift mechanisms can be present at the device. [1, 79, 80] Mobile ions are generally responsible for large instabilities and failures in transistors, and their presence should be minimized for most of the applications. [79]

The results obtained for SU-8 show that this material is considerably more effective regarding device passivation. SU-8 is an epoxy-based negative chemically amplified resist that is commonly used for the fabrication of high aspect ratio features. [81] It is sensitive to near UV-region (365 nm), but it is also compatible with X-ray and electron beam lithography. [82, 83] It finds applications in numerous fields, such as sensors, micro-fluidic components and inkjet print head nozzles. SU-8 was already used in fully transparent electronic devices: for instance, Gorrn et al. have shown the integration of an OLED with an oxide semiconductor-based TFT, where SU-8 is used to define the OLED pixel area. [84] Regarding its application as a passivation material in GIZO TFTs, it can be seen that even without using a second step annealing a $V_{on}$ close to -10 V can be achieved (fig. 5.26a and table 5.4). When compared with the other transfer characteristics in fig. 5.26a, the improved results with SU-8 can be justified to a great extent by a totally different fabrication process than the one used for the other passivation materials. SU-8 film production involves only a non-vacuum technique (spin-coating), multiple baking steps to evaporate solvents, UV exposure to initiate chemical amplification, post-exposure baking to promote cross-linking reaction and development. A subsequent baking process can promote further cross-linking of the polymeric network. Given that a non-vacuum deposition technique is used and due to the absence of back surface bombardment during the fabrication of the passivation layer, oxygen can remain at the GIZO back surface. However, the large depletion layer close to the back surface of the non-passivated material is not maintained. In fact, some of the weakly bonded oxygen might lose its bonding with GIZO, for instance during the baking steps, UV exposure or due to the rearrangements that take place in the SU-8 film during cross-linking. All this can be superimposed to the existence of positive charges lying in the SU-8 layer, for instance H$^+$ that arises due to the decomposition of the photoacid generator present in SU-8, which catalyzes the cross-linking reaction. Thus, an accumulation layer can even replace the previous depletion layer close to the back surface of GIZO. However, this should be considerably less significant than for the
other analyzed passivation layers, since as shown in fig. 5.26a the GIZO layer in TFTs passivated with SU-8 can be almost entirely depleted by using a $V_0$ close to -10 V. After a second annealing step at 200 °C, electrical properties close to the ones of non-passivated devices are obtained. At this stage, cross-linking of the SU-8 layer is fully achieved (confirmed by FTIR analysis, article in press) and remaining H$^+$ ions available at the passivation layer, close to its interface with GIZO, can probably capture some electrons from GIZO, re-establishing a depletion layer close to the back surface of GIZO. An interesting effect visible in fig. 5.26b and consistently reproduced in SU-8 passivated devices is the significant decrease of the Off-current when compared with non-passivated devices. Although full details regarding the reason for this are not clearly understood for now, it is suggested that SbF$_6^-$ ions in the SU-8 layer act as negative charges, contributing to a strong depletion of the back surface region of the semiconductor. Negative charges in passivation layers of nanocrystalline and a-Si:H TFTs were also found to decrease the Off-current. [85, 86] Improved Off-currents after annealing passivated GIZO TFTs were also observed by Lee et al. [74]

In the latter stages of the work of this dissertation, higher %O$_2$ (1.0 %) started to be used to produce the GIZO layer in order to have lower background $N$ and obtain non-passivated devices with closer to 0 or positive $V_{on}$. For these GIZO deposition conditions it was found that the effect of the second annealing step after SU-8 passivation was considerably lower. Based on the discussion above, this would be expected, given that even without a depletion layer at the back surface, a lower $N$ semiconductor would naturally have a larger energetic difference between CBM and $E_F$. So, even if a small accumulation layer is formed at the back surface due to the passivation process, the depletion of the entire semiconductor by using a slightly negative $V_0$ is facilitated, given its lower $N$. These assumptions were in fact somehow observed by Chiang: in his work he shows that the variation of $V_{on}$ between non-passivated and passivated oxide semiconductor TFTs is dramatically increased when the non-passivated device possesses a large negative $V_{on}$ (i.e., high $N$). [40]

To infer about the effectiveness of the SU-8 passivation layer, the non-passivated and SU-8 devices presented in fig. 5.26b were measured in high vacuum. As evident from fig. 5.27a, the non-passivated TFT presents a very large negative shift of $V_{on}$ when measured under vacuum, consistent with the strong interaction of the back surface with oxygen explained before. [37] For thin films or nanowires, this surface interaction extends to a point where it dominates the overall material properties. [35, 37, 78, 87, 88] Note that the most significant differences on the transfer characteristics are found only after the devices remain in vacuum for 30-60 minutes. This confirms the fact that oxygen adsorption/desorption in oxide semiconductor surfaces can be rather slow processes and both slow and fast surface states can play an important role in these phenomena. [13, 40]
In fact, even if some positive shift of $V_{on}$ is verified right after bringing the device again to atmospheric pressure, the initial properties are only recovered after 1 week of air exposure. These results are consistent with the ones obtained by Kang et al. in non-passivated GIZO TFTs, where $V_{on}$ shifts as large as -50 V were observed under vacuum. The change in GIZO’s $N$ due to oxygen adsorption/desorption was measured to be of the order of $10^{20}$ cm$^{-3}$. [35] On the other hand, SU-8 passivated TFTs do not present significant changes on their electrical properties when measured under vacuum and the small changes are almost instantaneously recovered after bringing the devices to atmospheric pressure (fig. 5.27b).

![Figure 5.27 - Transfer characteristics of (a) non-passivated and (b) SU-8 passivated GIZO 2:4:2 TFTs, with $\%O_2=0.4 \%$ and $T_x=200 \, ^\circ C$. Measurements performed in air, under high-vacuum and after recovering in air.](image)

A large variety of organic layers present poor diffusion barriers to oxygen and water vapor. [89] This can have severe implications in the properties of oxide semiconductor devices: as shown above, oxygen considerably shifts the transfer characteristics of GIZO TFTs; also, it was shown by Jeong et al. and Park et al. that H$_2$O molecules can act as electron trap centers as well as electron donors on the GIZO surface, resulting in considerable shifts of the electrical properties and severe instability. [36, 90] Although an exhaustive study was not carried out in the present devices, moisture does not seem to affect the properties of SU-8 passivated devices, at least in a relative humidity range between 30-70%. Further considerations on stability will be made in section 5.1.6.

### 5.1.5. Considerations about $\mu_{fe}$ and limitations of short-channel devices

Throughout this chapter devices with very large $\mu_{fe}$ were presented. In fact, $\mu_{fe}$ generally surpasses $\mu$ measured for an oxide semiconductor thin film produced using the same composition and deposition conditions. At first sight, this is physically impossible, since the carrier transport in a device is severely limited by the existence of interfaces with other materials, such as the dielectric/semiconductor interface in the specific case of a field-effect transistor. Nevertheless, similar effects were already...
observed in TFTs, with \( \mu_{FE} \) of devices employing polycrystalline semiconductor materials (which besides the interface scattering effects are also affected by grain boundaries) being comparable even to the \( \mu \) of single crystals. [13] Several theories tried to explain such phenomena, being proposed that the dominant factor was not the mobility of the material itself but rather the modulation of that mobility that could be possible to achieve when carriers were injected by field effect. [91, 92]

For the specific case of an oxide semiconductor-based TFT, even considering a semiconductor with a low-to-moderate \( N \), \( E_F \) can be raised well above CBM just by increasing \( V_G \), because the tail state density is low. [10] This is totally different from what happens, for instance, in a-Si:H, where the large density of tail states pins \( E_F \) well below CBM. [12] This characteristic of oxide semiconductors allows them to present a very large modulation of mobility when integrated in a TFT. This is even enhanced if the semiconductor is made amorphous, because on that case the charges injected by \( V_G \) do not have to be used to lower the intercrystalline barrier height and can be readily available to increase the transconductance (this difference between amorphous and polycrystalline oxide semiconductors is evident by analysis of fig. 5.10). So, a larger \( \mu_{FE} \) than the corresponding \( \mu \) of the films used to produce the TFTs can be expected on these devices. In fact, this behavior is reported in the literature of oxide semiconductor-based TFTs. [93, 94]

However, even considering that \( E_F \) is raised above CBM when \( V_G \) is increased (thus, a large variation of \( N \) exists relatively to the background \( N \) of the semiconductor in the TFT), the \( \mu_{FE} \) values reported here are even higher than the \( \mu \) obtained for films with very large \( N =10^{20} \text{ cm}^{-3} \), where \( \mu \) is maximum (see fig. 4.19, p. 109). This can be attributed to the fact that the increase of \( N \) by changing the deposition conditions and by capacitive injection are two different mechanisms. Achieving a high \( N \) by changing the deposition conditions, such as %O\(_2\) or the target composition, can lead to the creation of a large number of trap states, affecting the movement of charges. On the other hand, when \( V_G \) is increased in a TFT, mechanisms such as neutralization of scattering centers or electric field excitation of electrons from shallow traps can significant raise \( N \) without introducing additional scattering or trapping centers in the semiconductor, contributing to a very large \( \mu_{FE} \). [13]

Still, the effect of fringing currents as a source of error of the extracted \( \mu_{FE} \) values should also be considered. Even if all the analyzed devices have patterned semiconductor layers, the width of the source-drain electrodes is actually smaller than the width of the active layer. This potentiates the flow of peripheral currents outside the channel drawn by the source-drain electrodes, leading to an overestimation of \( \mu_{FE} \). For such cases, a more reliable \( \mu_{FE} \) value is obtained for large \( W/L \), in order to neglect the effect of the fringing electric field. [46, 95] Figure 5.28a shows the evolution of \( \mu_{FE} \) with \( W/L \) for TFTs based on GIZO 2:4:2, with W fixed at 50 \( \mu \)m. Although the variation of \( \mu_{FE} \) with \( W/L \) is not as large as the one reported in [96] for unpatterned semiconductor layers, the plot confirms that \( \mu_{FE} \) is in fact overestimated for small \( W/L \). For larger \( W/L \), when fringing current effects can be
neglected, $\mu_{FE}$ is decreased to approximately half of the values obtained for small $W/L$, but a high $\mu_{FE}=20-30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is still obtained, which is significantly larger than the typical $\mu_{FE}$ values of a-Si:H or organic TFT technologies.

![Graph](image)

**Figure 5.28** – (a) $\mu_{FE}$-$W/L$ plot for GIZO 2:4:2 TFTs (%O$_2$=0.4 %) annealed at 150 °C, having $W$ fixed at 50 $\mu$m; (b) transfer characteristics of the same devices, with $L$ ranging from 50 to 2 $\mu$m.

Although the $\mu_{FE}$-$W/L$ trend of fig. 5.28a is mostly justified by the fringing current effects, contact resistance may also have an important effect for smaller $L$. As shown in section 5.1.3, for $L<15$ $\mu$m ($W/L$=3.33 in fig. 5.28a) $R_{SD}$ starts to be comparable or even larger than $r_{ch}xL$, so the electrical properties of short channel devices can be affected not only by the intrinsic properties of the semiconductor and its interface with the dielectric layer but also by contact effects. This can also contribute to a limitation on the increase of $I_D$ for lower $L$ devices (fig. 5.28b), i.e., the increase of $I_D$ with $W/L$ is less than what would be predictable by equation 2.1. The effect of contact resistance was also found to be preponderant on small $L$ oxide semiconductor-based TFTs by other authors. [23, 52, 97]

### 5.1.6. Stress and aging effects

Stress measurements constitute an important starting point to study the instability mechanisms on transistors. Although a detailed study of these mechanisms is out of the scope of the present dissertation, given the novelty of oxide semiconductor-based TFTs research area it is relevant to show and briefly analyze the results achieved until now, regarding stress measurements under constant $I_D$ or $V_G$ and aging effects, for devices measured during 18 months.
5.1.6.1. Constant drain current and constant gate bias stress

It is well known, for more than 30 years, that the electrical properties of TFTs are degraded when they are subjected to a constant \( V_G \) for long periods of time. [2] A large number of reports regarding gate bias stress measurements exists in the literature of TFTs, for the different semiconductor technologies. [98-100] The most frequent instability mechanism is found to be charge trapping at or close to the dielectric/semiconductor interface, which results in a shift of \( V_T \) (\( \Delta V_T \)). The same mechanism has been found to be predominant for oxide semiconductor-based TFTs stressed under constant gate bias, as shown by recent reports. [77, 101-105] However, even if constant gate bias stress constitutes the most used methodology to infer about the electrical stability of TFTs, from an application point of view it is also relevant to study how the devices behave under a constant \( I_D \). A good stability under constant \( I_D \) is critical, for instance, when the devices are intended to be used as the “drive TFTs” in an OLED display, since for this application the transistor has to supply a high and stable current to the OLED when the pixel is turned on, otherwise significant variation in the pixel brightness can arise. [3, 105] Essentially, constant \( I_D \) stress measurements accurately simulate the stress conditions that a TFT may be subjected to when integrated into an analog circuit environment. [106]

These tests were carried out for 24 h at room temperature, keeping the drain and gate terminals shorted in a diode-connected configuration,\(^n\) with the source electrode grounded. [107] This configuration permits an automatic \( V_G \) (thus, \( V_{on} \)) adjustment to maintain the constant \( I_D \). During the 24 h period, the stress condition was shortly interrupted several times to access the devices’ transfer characteristics at different stress times. A constant \( I_D = 10 \mu A \) was used, which can be considered a severe test condition, given that lower currents (\( = 1 \) to 5 \( \mu A \)), are generally required to properly drive an OLED in a display. [44, 90] The timescale of these measurements is also significantly larger than the one usually found in the literature for bias or current stress in GIZO TFTs. [7, 73, 77, 90, 103, 105, 108] To prevent ambiguous determination of \( V_{on} \) (or \( V_T \)) shifts in devices presenting non-abrupt rises of \( I_D \) after some stress time, for these stress measurements \( V_T \) is taken as the \( V_G \) corresponding to a specific \( I_D \) (10 \( \mu A \)). Similar procedures to estimate \( V_T \) were already used in the past by different authors. [60, 109] After the 24 h stress, the devices were left in the dark and the recovery dynamics were analyzed by measuring the transfer characteristics at specific recovery times.

Figure 5.29 shows two extreme examples of the evolution of transfer characteristics with stress and recovery time, for TFTs with a GIZO 2:4:2 semiconductor deposited with \( P_{dep} = 0.7 \) Pa, \( P_{Prf} = 1.1 \) W cm\(^{-2}\)

\(^n\) Even if some mixed effects of gate and drain bias can arise from this setup, it is expected that drain bias is not particularly relevant in oxide semiconductor-based TFTs, as reported by Gorrn et al. [104]
and $d_o = 40$ nm, but different $\%O_2$ (0.4 and 10.0 $\%$ for figs. 5.29a and 5.29b, respectively). Final devices were annealed at 150 °C.

![Graphs showing transfer characteristics and stability](image)

**Figure 5.29** – Results obtained from constant $I_D$ stress measurements on GIZO 2:4:2 TFTs annealed at 150 °C, for different $\%O_2$: transfer characteristics evolution for (a) $\%O_2=0.4\%$ and (b) $\%O_2=10.0\%$; $\Delta V_T$ and $\Delta S$ evolution for (c) $\%O_2=0.4\%$ and (d) $\%O_2=10.0\%$. The insets in (c) and (d) show the $V_G$ (to assure $I_D=10\mu A$) measured during stress.

It can be seen that $\%O_2=10.0\%$ leads to highly unstable devices, with the transfer characteristics being significantly shifted towards higher $V_G$ values. This result is consistent with a large density of defects on the semiconductor and on its interface with the dielectric, which can trap the induced electrons, resulting in a large $\Delta V_T$. [77, 103, 105] Note that this effect coincides with the early-stage aging evaluation obtained by measuring $\Delta V_{on}$ in consecutive transfer characteristics measurements (fig. 5.4), where it was seen that oxide semiconductor layers produced with very large $\%O_2$ resulted in large $\Delta V_{on}$. This is not surprising, since the instability mechanism involved in both kinds of measurements is essentially the same (charge trapping) although here the testing conditions are more severe and extended throughout a longer time scale. Based on this, it would also be expected that TFTs with semiconductor layers produced with lower $\%O_2$ would present improved stability, which is indeed verified.
Figs. 5.29c and 5.29d give more detailed insights regarding the dynamics of the most affected parameters during the stress test, $\Delta V_T$ and $\Delta S$. An increase on $S$ is generally associated with defect state creation in the semiconductor material. [90, 104, 110] $\Delta S$ is quite similar and low for both devices, around 0.2 V dec$^{-1}$, and is completely reversible, meaning that the creation of these new states should not be much relevant in GIZO, or at least can be quickly annihilated. The insets in figs. 5.29c and 5.29d show the evolution of the $V_G$ needed to assure $I_D=10 \, \mu\text{A}$ during the stress time. In agreement with the corresponding transfer characteristics, the shift is much lower for $\%O_2=0.4 \,$%. An interesting feature is also observable in these insets: $V_G$ quickly drops in selected times, corresponding to the short interruptions of the stress measurements to access the transfer characteristics. This means that a considerable fraction of the trapped charges can be quickly detrapped, presumably because they are associated with fast surface states lying close to the dielectric/semiconductor interface. [13, 79]

Note that these stress measurements were performed around 18 months after device fabrication. As will be seen in p. 199, aging can lead to considerable improvements on initially unstable devices, such as the ones where the oxide semiconductor is produced with high $\%O_2$. Nevertheless, the constant $I_D$ stress measurements show that significant differences still exist on the devices depending on the $\%O_2$ used to fabricate the oxide semiconductor layer, being smaller $\%O_2$ preferable to obtain more stable devices. Different oxide semiconductor compositions were also analyzed regarding their stability under constant $I_D$ stress. For this set of experiments, semiconductors produced with $\%O_2=0.4 \,$% were selected. By far, ZnO is the most unstable composition, which is in agreement with a large density of defects on this material (fig. 5.30). In addition, the creation/annihilation of new defect states should be easily achieved on the sputtered ZnO films, judging by their high sensitivity to the processing conditions. In fact, defect creation/removal process is suggested by Cross et al. to justify the initial degradation and subsequent recover of $S$ during gate bias stress, superimposed to charge trapping at the dielectric/semiconductor interface. [110] Although the processing conditions of ZnO are different in both works, a somewhat similar behavior under stress is observed here: at the initial stage of the test, charge trapping is the dominant mechanism, concomitant with a high increase on $\Delta V_T$. However, after prolonged stress time, this effect looses relevance and a complex defect creation/removal seems to be dominant, resulting in large fluctuations of $S$. Furthermore, note that ZnO is well known to exhibit a significant degradation in electrical characteristics when stressed continuously by an electric field due to electron trapping, dipole orientation and ion migration. [111] Additionally, adsorption or migration of molecules on ZnO can be enhanced by an electric-field, which can also contribute to the large variations on the electrical properties during stress. [90, 111, 112]
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Figure 5.30 – Results obtained from constant $I_0$ stress measurements on ZnO TFTs with %O$_2$=0.4 % and annealed at 150 °C: (a) transfer characteristics evolution; (b) $\Delta V_T$ and $\Delta S$ evolution.

Considering now the evolution of properties on IZO-based TFTs, stability is improved as zinc content is decreased (fig. 5.31a). However, for IZO 4:1 a negative and non-recoverable $\Delta V_T$ is obtained. This is not verified for TFTs with In$_2$O$_3$, but the In$_2$O$_3$ data refers to 300 °C annealed devices, since on 150 °C ones channel depletion (i.e., Off-state) could not be achieved. Annealing can have a significant effect on stability, as will be shown below. With the introduction of gallium it is verified that even if the magnitudes of $\Delta V_T$ and $\Delta S$ are not improved, the recovery of the initial properties is entirely achieved, contrarily to what typically happens with IZO (fig. 5.31b).

Figure 5.31 – Summary of the $\Delta V_T$ and $\Delta S$ variations obtained in constant $I_0$ stress measurements for TFTs with %O$_2$=0.4 % and annealed at 150 °C (except In$_2$O$_3$, having $T_a$=300 °C), where different target compositions are used for processing the semiconductor layer: (a) ZnO, In$_2$O$_3$ and IZO; (b) IZO and GIZO.

Optimized GIZO 2:4:2 devices annealed at different temperatures and with a SU-8 passivation layer were also subjected to constant $I_0$ stress measurements. The results show that for $T_a$=200 °C $\Delta V_T$ and
 Properties of n-type oxide semiconductor-based TFTs

$\Delta S$ are reduced (fig. 5.32). The improved stability can be related with enhanced dielectric/semiconductor interface properties and a reduction in the subgap states of GIZO. [22] A lower $\Delta V_T$ on annealed GIZO TFTs exposed to gate bias stress was also observed by Suresh et al. [103]

$\Delta S$ are reduced (fig. 5.32). The improved stability can be related with enhanced dielectric/semiconductor interface properties and a reduction in the subgap states of GIZO. [22] A lower $\Delta V_T$ on annealed GIZO TFTs exposed to gate bias stress was also observed by Suresh et al. [103]

![Graph showing $\Delta V_T$ and $\Delta S$ variations](image)

**Figure 5.32 – Summary of the $\Delta V_T$ and $\Delta S$ variations obtained in constant $I_D$ stress measurements for GIZO 2:4:2 TFTs, with $%O_2=0.4\%$, different $T_A$ (non-passivated) and passivated with SU-8.**

However, the most impressive optimization arises after device passivation, where $\Delta V_T$ as small as 0.46 V and negligible $\Delta S$ could be obtained. This gives new insights about the instability mechanisms that might be occurring in GIZO TFTs. Given that the dielectric/semiconductor interface should have the same properties for both passivated and non-passivated devices, GIZO’s back surface should also have an important contribution to the shifts observed during stress. As stated above for ZnO, oxygen adsorption/desorption processes might be enhanced when the material is subjected to an electric field. Given that the electronegativities of indium, gallium and zinc are quite similar, it is plausible to assume that the same processes can happen at the surface of a GIZO film. As oxygen is adsorbed in the non-passivated device, the depletion layer close to the back surface assumes more relevance, raising $V_T$. On the other hand, when GIZO is passivated additional oxygen cannot be provided to the back surface, hence this source of instability is eliminated. Naturally, this assumption is only correct if the passivation material is dense and/or does not have a large concentration of mobile ions that could affect the stability of the transistor. The SU-8 passivation layer used here seems to fulfill these requirements. Jeong et al. observed that GIZO TFTs passivated with organic photoacryl and non-dense SiO$_2$ films result in larger $\Delta V_T$ under gate bias stress measurements than dense SiO$_2$ films. [90] Improvements on the stability of passivated oxide semiconductor-based TFTs are also reported by Levy et al. and Cho et al. [77, 113]
The results obtained here compare quite favorably with the recent reports in literature regarding GIZO TFTs tested under constant \( I_D \) stress. In 2007, Jeong \textit{et al.} reported a \( \Delta V_T = 3.4 \) V after 60 h with \( I_D = 3 \) \( \mu A \) for a non-passivated device, while in 2008 the same research group obtained a \( \Delta V_T = 2.3 \) V after 10 h with \( I_D = 10 \) \( \mu A \) for a \( \text{SiO}_x \) passivated device. [29, 108] Concerning other TFT technologies, a-\( \text{Si:H} \) TFTs were also analyzed by Jahinuzzaman \textit{et al.}, revealing considerably worse stability than GIZO TFTs: for \( I_D = 10 \) \( \mu A \) a \( \Delta V_T \approx 10 \) V is obtained after 24 h stress, increasing to \( \Delta V_T \approx 15 \) after more 24 h. [106]

At a later stage of this work, typical bias stress measurements were also performed on SU-8 passivated TFTs, by applying a constant \( V_G = 20 \) V during 8 h, while keeping the source and drain electrodes grounded. The results are presented in fig. 5.33, reinforcing the good stability of the passivated devices: in fact, a small and recoverable \( \Delta V_T \approx 0.10 \) V was the only shift observed.

![Figure 5.33 - Transfer characteristics evolution obtained from constant bias stress measurements on GIZO TFTs with \%O\textsubscript{2}=0.4 % and annealed at 150 °C, passivated with SU-8.](image)

5.1.6.2. Electrical performance evolution during 18 months

The electrical properties of oxide semiconductor-based TFTs produced on Si/SiO\textsubscript{2} substrates were monitored during 18 months. During this period the devices were stored in a room, exposed to air ambient. Depending on the oxide semiconductor layer, significant differences on the stability of the TFTs were verified during this period of time. Even if processing parameters have some effect on this, \( N \) seems to be the dominant factor defining the degree of stability on these devices. Figure 5.34 tries to elucidate this, presenting the transfer characteristics shifts during time for non-passivated TFTs with different oxide semiconductors.
In fig. 5.34a it can be seen that TFTs having a GIZO 2:4:2 semiconductor produced with low \( %O_2 \) (0.4 \%) and \( d_1=40 \) nm present remarkable stability over time, with a shift of \( V_{on} \) as small as -1 V, an increase on \( \mu_{eff} \) of around 6 \% and negligible effect on the remaining electrical parameters, even if the devices were only annealed at 150 °C. On the other hand, despite the same (optimal) \%O_2 is used for an IZO 2:1 layer with \( d_1=20 \) nm, the resulting TFTs present a very large positive shift of \( V_{on} \) of more than 6 V, but a small decrease on \( \mu_{eff} \) (≈ 7 \%), for the same \( T_A=150 \) °C (fig. 5.34b). These results clearly show that good stability do not depend solely on optimized processing parameters, but also on a target composition that allows obtaining a moderate \( N \). Large \( N \) materials have more oxygen vacancies, hence larger chances to physisorb oxygen at the empty surface states over time. After oxygen is physisorbed, given that a large amount of conduction band electrons are available, these can be captured by the physisorbed oxygen promoting its change to a chemisorbed state. This process can be repeated during a large period of time until the oxygen concentrations inside the film and in the environment reach an equilibrium state (or alternatively, until the surface barrier height to complete the chemisorption process reaches a value where it starts not being energetically
favorable). [38, 114] As discussed before, this process leads to the formation of a depletion region close to the semiconductor’s back surface. The predominance of this depletion region relatively to the bulk semiconductor over time is particularly relevant for such thin films, whose properties are essentially surface-controlled, resulting in an increase of $V_{on}$ over time, justifying the results depicted in fig. 5.34b. For materials with lower $N$ but also produced under optimal %O$_2$ conditions (fig. 5.34a), the variations on the back surface during time would be less relevant, since the depletion region is already further extended through the bulk of the semiconductor (and eventually reaches the dielectric/semiconductor interface) at the initial times and the lower $E_F$ at the bulk region of these materials would prevent the continuous supply of electrons to feed the chemisorption process, hence the widening of the depletion region and consequent changes on the electrical properties over time. This behavior is reinforced by the fact that devices with lower $N$ (i.e., GIZO 2:4:2 and %O$_2$=0.4 %, like the ones presented in fig. 5.34a) but with smaller $d_s$ (20 nm) also exhibit good stability over time, contrarily to what happens with IZO-based devices (higher $N$) with the same $d_s$ (fig. 5.34b).

For both cases (figs. 5.34a and 5.34b), the small variations on $\mu_{IZO}$ can be related with the $V_{on}$ evolutions, because a lower $V_{on}$ corresponds to a larger number of free electrons available at the semiconductor to increase the transconductance, thus in fig. 5.34a $\mu_{IZO}$ increases, but decreases in fig. 5.34b. Some material relaxation at the semiconductor layer and/or rearrangements at the dielectric/semiconductor region could also happen during time for these cases, but this would not be particularly relevant here, given the optimized processed conditions of the IZO and GIZO layers. Still, small improvements could justify the fact that $\mu_{IZO}$ is not severely affected in fig. 5.34b, even if $V_{on}$ is largely shifted.

A different situation is verified in fig. 5.34c, being a clear example that processing conditions also have a large effect on the aging of these TFTs. For this case, the 40 nm thick GIZO layer was grown with %O$_2$=10.0 %, which was already shown to result in devices severely affected by large instability, mostly associated with structural defects created due to intense bombardment effects. These cannot be compensated by the background $N$, because it is too low. For these semiconductor layers a large decrease of $\rho$ with time is verified, even for thicker films (fig. 4.24, p. 120), which is tentatively associated with significant structural relaxation that can lead to the annihilation of some empty trapping sites, including those located close to the dielectric/semiconductor interface. In fact, a very large improvement of the electrical properties is verified throughout time, including the elimination of the kinks of the transfer characteristics and an overall shift of $V_{on}$ towards the ideal 0 V value. For this TFT, $\mu_{IZO}$ is increased more than 35 %, $V_{on}$ is shifted around 7 V and most interestingly $\Delta V_{on}$ in consecutive transfer characteristics measurements is decreased from 7 to only 1.5 V. However, note that a large density of traps should still persist for these deposition conditions after 18 months, as evidenced by the constant $I_0$ stress measurements shown in fig. 5.29b for similar devices. This would
be expectable, since threshold energies required for more severe structural changes are not achievable at room temperature. However, if these TFTs having a non-favorable %O₂ processing condition are annealed at a higher temperature (300 °C), the variation of properties during time becomes almost inexistent and their electrical properties are significantly improved over the 150 °C annealed ones – slightly higher μ_{FE}, closer to 0 V_{on} and negligible ΔV_{on} in consecutive measurements (fig. 5.34d).

Little information exists in literature regarding the variation on the properties of oxide semiconductor-based TFTs when analyzed during long periods of time. Still, interesting observations are reported by McDowell et al. for IZO TFTs, with μ_{FE} and V_{f} decreasing around 10 % and -10 V, respectively, after seven months of storage in air. [25] On the other hand, Chiang reported that for GIZO TFTs only very thin channel layers present some increase on V_{on} (5-6 V) after 18 weeks of production time. [7] Although stability dependence on d_s was not studied here in detail, the results obtained by Chiang et al. are consistent with a higher dominance of back surface properties as d_s decreases, which is plausible in the context of the discussion presented above regarding the formation of a depletion layer close to this back surface.

5.2 – TFTs with sputtered dielectrics based on tantalum-silicon and tantalum-aluminum oxide systems

After the optimization study concerning the oxide semiconductor, source-drain and passivation layers presented in the last sections, the dielectric is the only material missing for the production of fully patterned devices, ready to integrate in active matrix backplanes. This was accomplished by using the sputtered dielectric materials previously explored in Chapter 4. In this section, the results obtained on TFTs employing these dielectrics are presented and analyzed, not only concerning typical static characterization, but also regarding different types of stability measurements.

5.2.1. Process flow and device structure

To produce these devices, a 4 mask process was used, including the one required for the passivation layer, which was only grown on selected devices to confirm the results obtained on TFTs produced on Si/SiO₂ substrates. The same lithographic mask was used for the dielectric and semiconductor layers, allowing for less processing steps and time consumption. Also, it is expected that enhanced dielectric/semiconductor interface properties are obtained with this process, due to the fact that the dielectric surface is not subjected to any lithographic process prior depositing the semiconductor
layer. Figure 5.35 shows the 4 mask layout used to fabricate the TFTs, consisting of exactly the same masks used for the Si/SiO₂ TFTs (fig. 5.1), adding only the mask for the gate electrode patterning.

![Mask layout](image)

**Figure 5.35 – Mask layout used to fabricate the TFTs on glass substrates with sputtered dielectrics.**

The process flow (fig. 5.36) is also very similar to the one used for Si/SiO₂ TFTs, with the only differences being the requirement of glass substrate cleaning, mainly to have good adhesion of photoresist, [115] the patterning, deposition and lift-off of gate electrode and the sputtering of the dielectric layer. Regarding the semiconductor used for these devices, a GIZO 2:4:2 composition was selected, with the deposition conditions being %O₂=1.0 %, pₜₚₚ=0.7 Pa, P₀=1.1 W cm⁻² and dₛ=20 nm. The oxide semiconductor films obtained under these conditions represent a good compromise between stability, large μₑₑ and low background N, important to assure good overall performance of the devices. For these TFTs, all the sputtering processes were carried out using the home-made sputtering system (fig. 3.3b, p. 51).

In order to study the effect of different device structures, TFTs with staggered bottom-gate and staggered top-gate configurations were processed. The latter structure was achieved by using the same lithographic masks and simply by changing the order of the process flow (starting with the source-drain and ending with the gate electrodes).

Concerning electrical characterization, the same considerations made for TFTs on PECVD SiO₂ were taken into account here (see p. 150). The only difference regarding the devices employing sputtered dielectrics was the range of V₆ and V₇ used to perform the measurements, which was lower than for TFTs on PECVD SiO₂. The reason behind this is the lower breakdown field of sputtered dielectrics, but it will be shown that higher V₆ and V₇ values are not necessary to clearly observe linear and saturation regimes on these devices, since the higher-κ dielectrics require lower operating voltages.
5. Properties of n-type oxide semiconductor-based TFTs

Figure 5.36 – Process flow used to produce TFTs on glass substrates employing sputtered dielectrics. In the bottom is shown a photograph of a final substrate containing 16 TFTs.

5.2.2. Electrical properties of TFTs using binary oxide dielectrics

Figure 5.37 and table 5.5 show the transfer characteristics and extracted electrical parameters for some of the binary oxide dielectrics studied during the work of this dissertation. A detailed study was not carried out for each one of these dielectrics in terms of (post-)deposition conditions, serving this initial analysis solely to verify the level of device performance that could be expected for binary oxide dielectrics with different intrinsic properties (κ, E\textsubscript{g}, amorphous or polycrystalline structure), sputtered with the same deposition conditions.\(^\text{○}\) Characteristics for TFTs using a PECVD SiO\textsubscript{2} dielectric are also given for comparison. Given that one of the largest motivations of this work is to fabricate devices at low temperatures, a T\textsubscript{d}=150 °C was used at the end of device production.

\(^\text{○}\) Except for P\textsubscript{in}, which was different for each dielectric in order to assure reasonable growth rates, as described in chapter 4 (p. 132).
Transparent oxide TFTs: production, characterization and integration

Figure 5.37 – Transfer characteristics obtained for GIZO TFTs using different binary oxide dielectrics, annealed at 150 °C.

Table 5.5 – Electrical properties obtained for the devices depicted in fig. 5.37.

<table>
<thead>
<tr>
<th>Dielectric material</th>
<th>$\mu_{FE}$ (cm$^2$ V$^{-1}$ s$^{-1}$)</th>
<th>$V_{on}$ (V)</th>
<th>On-Off ratio</th>
<th>$S$ (V dec$^{-1}$)</th>
<th>$I_g$ @ $V_g$=15 V (A) Before stress</th>
<th>$I_g$@ $V_g$=15 V (A) After stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>1.3</td>
<td>-0.25</td>
<td>2.8×10$^4$</td>
<td>1.08</td>
<td>9.7×10$^{-12}$</td>
<td>--</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>5.1</td>
<td>3.00</td>
<td>2.0×10$^4$</td>
<td>0.58</td>
<td>2.2×10$^{-6}$</td>
<td>--</td>
</tr>
<tr>
<td>Ta$_2$O$_5$</td>
<td>36.1</td>
<td>0.50</td>
<td>2.9×10$^3$</td>
<td>0.31</td>
<td>6.2×10$^{-9}$</td>
<td>5.3×10$^{-7}$</td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>7.3</td>
<td>8.50</td>
<td>8.4×10$^{2}$</td>
<td>1.47</td>
<td>8.1×10$^{-10}$</td>
<td>--</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>16.8</td>
<td>3.50</td>
<td>9.3×10$^{6}$</td>
<td>0.42</td>
<td>1.5×10$^{-11}$</td>
<td>--</td>
</tr>
<tr>
<td>PECVD SiO$_2$</td>
<td>43.0</td>
<td>0</td>
<td>3.8×10$^{7}$</td>
<td>0.27</td>
<td>2.8×10$^{-11}$</td>
<td>2.2×10$^{-11}$</td>
</tr>
</tbody>
</table>

As expected, device performance greatly depends on the dielectric layer, as already shown by different authors for oxide semiconductor-based TFT. [93, 116, 117] Starting by the low-κ dielectric, sputtered SiO$_2$, although the requisites of low Off-current and close to 0 V $V_{on}$ are fulfilled, $S$ is very high and the maximum $I_D$ is around 2 orders of magnitude lower than that of the TFTs fabricated with PECVD SiO$_2$. This results in devices with the lowest $\mu_{FE}$, around 1 cm$^2$ V$^{-1}$ s$^{-1}$. Still, note that in literature, sputtered SiO$_2$ allows to obtain better performing GIZO TFTs, mainly in terms of $S$ and $\mu_{FE}$, as demonstrated by Ofuji et al. [69] The poor characteristics reported herein should be attributed to a non-optimized SiO$_2$ processing, resulting in a degradation of the film’s compactness and increased dielectric/semiconductor interface trap density. Hence, even if the amorphous structure and the high-$E_g$ of SiO$_2$ allow to obtain good insulating properties, the poor compactness and the large trap state densities, together with the low κ of SiO$_2$, significantly affect the density of charges that can be

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As mentioned before, the study presented here does not intend to find optimal deposition conditions for each dielectric, which will naturally be different depending on the material system.
induced and, from these, the ones that can actually act as free carriers to modulate the channel conductivity of the TFT.

Al₂O₃ is generally considered a high-κ dielectric, even if its κ is less than half of other high-κ dielectrics such as ZrO₂, HfO₂ or Ta₂O₅. Still, the Al₂O₃ films produced in this work exhibit a κ which is almost twice the one of SiO₂, allowing the corresponding TFTs to present considerably improved μₑₑ over TFTs employing SiO₂ as the dielectric layer, due to easier filling of interface traps by the higher density of charges induced by the capacitive effect. However, even if Al₂O₃ also presents an amorphous structure and a large $E_0$, with band offsets to GIZO similar to the ones presented by SiO₂, the Off-current is increased to more than 1 nA and $V_{on}$ is significantly shifted towards positive values, accompanied by an increased $ΔV_{on}$. Although the increase of the Off-current is not totally understood for now, most of these deleterious effects should be related with the high $P_{rf}$ required to sputter Al₂O₃, which can induce structural defects that trap charges and degrade the films’ compactness, as well as with the natural trap charging properties of Al₂O₃ surfaces, which are verified even for films produced by high-temperature deposition techniques, such as atomic layer deposition (ALD). [118]

TFTs using ZrO₂ present the poorest properties, with the lowest On-Off ratio and highest $S$. A large density of pinholes, arising from a deposition process where a large $P_{rf}$ (similar to Al₂O₃) has to be used to achieve reasonable growth rates could justify the high Off-current of these transistors. Additionally, the decreased $E_0$ relatively to Al₂O₃ (or SiO₂) turns the band-offsets with GIZO less favorable, which can contribute to the increased Off-current comparatively to Al₂O₃. Superimposed to this, the fact that as-deposited ZrO₂ films are polycrystalline should also contribute to degraded insulating properties, since the grain boundaries typically act as preferential paths for impurity diffusion and leakage current, as well as to poor interface properties resulting from the high roughness of the films. Hence, despite the high-κ of ZrO₂ ($κ=24$), the corresponding TFTs present the lowest μₑₑ among all the high-κ dielectrics analyzed here. Besides this, ZrO₂ always results in devices with large $ΔV_{on}$ and counterclockwise hysteresis, which could be an indication that multiple instability mechanisms, such as charge trapping at the dielectric/semiconductor interface and ion drift inside the dielectric layer, should play an important role. [1, 80]

Even if ZrO₂ and HfO₂ have similar intrinsic properties, the performance of TFTs employing the latter are considerably improved. Although as-deposited HfO₂ films have a polycrystalline structure, most of the problems mentioned for TFTs with ZrO₂ are not verified. This could be related with the slightly lower $P_{rf}$ used to deposit HfO₂ and/or to a lower sensitivity to substrate bombardment effects of this material. Additionally, note that HfO₂ intrinsically presents a slightly higher $E_0$ than ZrO₂, and this can even be accentuated by the higher bombardment effects on ZrO₂, which can broaden its band-tails, resulting in higher band-offsets relatively to GIZO for HfO₂ than for ZrO₂ films. This way, a low Off-current is achieved for TFTs employing HfO₂, starting to be comparable with the typically obtained
when PECVD SiO₂ is used. Still, a moderate $\Delta V_{on}$ ($\approx 2$ V) and $\mu_{FE}$ are obtained (although considerably better than ZrO₂), which should be ascribed with poor interface properties: in fact, Pereira et al. found that for HfO₂ films produced under similar deposition conditions and in the same sputtering system rough surfaces are obtained, associated with the dominance of the orthorhombic crystalline phase on these HfO₂ films. [119]

The best electrical performance is verified when Ta₂O₅ is used as the dielectric layer, with devices exhibiting a large $\mu_{FE}$ and low $S$, in parallel with close to 0 V $V_{on}$. This clearly shows the advantage of using a low $P_{tr}$, which does not induce appreciable structural damage to the growing film, and an amorphous high-$\kappa$ dielectric: even if it can be expected that the interface quality of the low-temperature Ta₂O₅/GIZO is far from the one of the high temperature thermal or PECVD SiO₂/GIZO, the extra capacitance provided by the high-κ dielectric allows easier interface trap filling due to the large density of induced charges that it can provide. [1] Moreover, the fact that Ta₂O₅ films present an amorphous structure and a smooth surface greatly contribute to the good interface properties: for instance, note that $\mu_{FE}$ obtained on these TFTs approaches the one obtained with PECVD SiO₂ ones, even if the dielectric films are processed under totally different temperature ranges.

Nevertheless, although the On-Off ratio is one order of magnitude higher than that of the sputtered SiO₂ TFTs, its value is limited by the high Off-current (0.5 nA), which arises as a consequence of the low $E_G$ of Ta₂O₅ and of its poor band offset relatively to GIZO. Also related with this, table 5.5 shows that $I_0$ of Ta₂O₅ devices increases almost two orders of magnitude after an $I_D$ stress test performed during 24 h, meaning that degradation of the dielectric occurs during stress (the stress measurements will be presented in section 5.2.5).

Given these results, several approaches could be followed. One of them would naturally be the improvement of surface properties of HfO₂, since this dielectric provides good insulating properties, allowing to obtain low Off-current. Another possibility would be to tune the properties of Ta₂O₅ in order to decrease its Off-current without degrading the remaining electrical properties, which are quite similar to the remarkable ones obtained using high temperature PECVD SiO₂. In this dissertation work the second route was explored, by mixing Ta₂O₅ with high-$E_G$ dielectrics (SiO₂ and Al₂O₃).

5.2.3. Electrical properties of TFTs using multicomponent amorphous oxide dielectrics

The properties exhibited by TFTs employing co-sputtered Ta₂O₅-SiO₂ (denoted TSiO) are presented in fig. 5.38 and table 5.6. The transfer characteristics of the composing binary oxides are also shown for reference.
Figure 5.38 – Electrical properties obtained for GIZO TFTs using co-sputtered multicomponent oxide dielectrics based on Ta$_2$O$_5$ and SiO$_2$, annealed at 150 °C: (a) transfer characteristics; (b) output characteristics for a device employing a TSiO dielectric.

It can be seen that a remarkable improvement is achieved when TSiO is used instead of Ta$_2$O$_5$. A high \( \mu_{FE} \) is maintained, only slightly smaller than with Ta$_2$O$_5$, which should mostly be related with the lower \( \kappa \), that allows capacitive injection of a lower density of charges. But the striking feature is the large decrease on the Off-current by more than one order of magnitude, due to the decrease of \( I_G \).

This allows an On-Off ratio increase, which now surpasses 3×10^6. Furthermore, because \( S \) essentially depends on the GIZO’s bulk and interface trap densities, [8] and given that all the devices were produced with the same GIZO process, \( S \) variations in different dielectrics can provide a valid indicator on the quality of these dielectrics and their interfaces with GIZO. For TSiO, \( S \) is improved when compared to Ta$_2$O$_5$, suggesting better interface properties. However, as previously discussed in p. 169, the \( S \) improvement may also be a consequence of the lower Off-current, which permits a more notorious channel conductivity modulation as the first free charges are induced close to the interface, leading to a more abrupt increase of \( I_D \) in the subthreshold region. [40] Nevertheless, since the transfer characteristics are slightly left-shifted towards \( V_{GS} = 0 \) V for TSiO when compared with Ta$_2$O$_5$, this can suggest that a lower trap density at the interface and/or improved bulk properties are achieved when this multicomponent dielectric is used. The TFTs using TSiO allow for quite comparable performance to the ones using PECVD SiO$_2$, even if totally different processing temperatures are used for producing these dielectric layers (less than 100 °C and 400 °C for TSiO and PECVD SiO$_2$, respectively). The largest differences are verified on \( I_D \), which is around one order of magnitude lower for PECVD SiO$_2$. The other major difference between TFTs employing TSiO and PECVD SiO$_2$ is on the \( \mu_{FE} \) value, which is higher when PECVD SiO$_2$ is used. However, note that the \( \mu_{FE} \) presented in tables 5.5 and 5.6 correspond to peak values obtained at large \( V_{GS} \) (15 V), when the conductive channel is located closer to the dielectric/semiconductor interface. In this situation, the
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Improved interface provided by the PECVD SiO₂ is expected to play an important role, even if TSiO can provide a larger density of induced charges due to its increased capacitance (higher-κ).

Figure 5.38b shows an example of typical output characteristics obtained from TFTs with the TSiO dielectric. No evidence of current crowding appears for the low V_D, confirming the results presented in section 5.1.3, where IZO source-drain electrodes were seen to provide good contact properties on devices annealed at low temperatures. In addition, a hard saturation is achieved for large V_D, meaning that a full pinch-off condition is attained, i.e., the entire thickness of GIZO can be depleted of free carriers close to the drain electrode. [17] Also, μ_FE degradation is not evident for high V_G, given the non-decreasing spacing of the output curves as V_G increases, reinforcing the idea that good interface properties can be achieved between GIZO and TSiO.

The other multicomponent oxide system explored for dielectric fabrication was Ta₂O₅-Al₂O₃ (denoted TAO). Transfer characteristics and the extracted electrical properties are shown in fig. 5.39 and table 5.6 for co-sputtered and single target (s.t.) TAO. Transfer characteristics for Ta₂O₅ and Al₂O₃ are also shown in fig. 5.39 for comparison purposes.

Figure 5.39 – Electrical properties obtained for GIZO TFTs using co-sputtered and single target multicomponent oxide dielectrics based on Ta₂O₅ and Al₂O₃ annealed at 150 °C: (a) transfer characteristics; (b) output characteristics for a device employing a TAO s.t. dielectric.

Table 5.6 – Electrical properties obtained for the GIZO TFT based on TSiO, TAO and TAO s.t. dielectrics, depicted in figs. 5.38 and 5.39.

<table>
<thead>
<tr>
<th>Dielectric material</th>
<th>μ_FE (cm² V⁻¹ s⁻¹)</th>
<th>V_on (V)</th>
<th>On-Off ratio</th>
<th>S (V dec⁻¹)</th>
<th>I_G @ V_G=15 V (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Before stress</td>
<td>After stress</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSiO</td>
<td>35.5</td>
<td>0</td>
<td>3.3×10⁶</td>
<td>0.24</td>
<td>4.2×10⁻¹⁰</td>
</tr>
<tr>
<td>TAO</td>
<td>32.1</td>
<td>0.50</td>
<td>3.7×10⁴</td>
<td>0.63</td>
<td>7.4×10⁻¹⁰</td>
</tr>
<tr>
<td>TAO s.t.</td>
<td>31.4</td>
<td>1.00</td>
<td>1.4×10⁷</td>
<td>0.23</td>
<td>1.7×10⁻¹²</td>
</tr>
</tbody>
</table>
As mentioned before, a high \( P_{\text{off}} \) was required to deposit Al\(_2\)O\(_3\) films with reasonable growth rates, but this processing condition may result in films with poor compactness and high density of pinholes that may deteriorate their insulating properties. These assumptions are verified for the TFTs employing Al\(_2\)O\(_3\) as the dielectric layer and the poor insulating properties are also transposed for the co-sputtered TAO films, resulting in TFTs with large Off-current. Nevertheless, due to the high tantalum content of co-sputtered TAO (see fig. 4.37, p. 134), a high \( \mu_{\text{FE}} \) can still be obtained. However, \( \mu_{\text{FE}} \) is lower than the one achieved using TSiO (even if TSiO has a lower \( \kappa \)), which should be ascribed to degraded interface properties when using TAO.

A significant improvement in the TFT characteristics is obtained when using TAO s.t.. In this case, the dielectric films grow at a reasonably fast rate (=3 nm min\(^{-1}\)) even using a considerably lower \( P_{\text{off}} \) than Al\(_2\)O\(_3\), which contributes to decrease film’s bombardment. The advantages of these transistors are obvious: first, the \( I_0 \) and Off-current are comparable to the ones typically obtained with high temperature PECVD SiO\(_2\). This represents a decrease in these parameters of two to three orders of magnitude over Ta\(_2\)O\(_5\)-based devices. Due to the low Off-current and the improved interface properties with GIZO, the transistors present a high On-Off ratio exceeding \( 10^7 \), a low \( S \) approaching 0.2 V dec\(^{-1}\) and a high \( \mu_{\text{FE}} \), similar to the one presented by the co-sputtered TAO devices, even if \( \kappa \) is significantly reduced from 21.7 to 14.2, reflecting a lower tantalum concentration in TAO s.t. films. The \( V_{\text{on}} \) value also reflects the different composition of TAO s.t., with the transfer characteristics being shifted towards the Al\(_2\)O\(_3\) TFT plot, but still presenting a low value (1 V). Regarding \( I_0 \) degradation arising due to the \( I_0 \) stress test, table 5.7 shows that even if \( I_0 \) increases, it is maintained in the pA range. The output characteristics of TFTs with TAO s.t. (fig. 5.39b) show good saturation, no current crowding and no \( \mu_{\text{FE}} \) degradation at high \( V_{\text{GS}} \), although the maximum \( I_0 \) is lower than for devices having TSiO as the dielectric layer (compare with fig. 5.38b).

Although not mentioned in the discussion above, electrical measurements were also performed in double sweep mode to access the hysteresis magnitude obtained with the different dielectrics. The verified hysteresis is always clockwise (except for the ZrO\(_2\) case mentioned before), consistent with trap filling by the accumulated electrons at (or close to) the dielectric/semiconductor interface. [1]

Concerning the hysteresis’ magnitude, it is, in most cases, smaller than 0.5 V, with TSiO exhibiting the smaller value, around 0.1 V. The larger values are registered for the dielectrics containing Al\(_2\)O\(_3\), with the magnitude increasing as aluminum content is increased: 0.4 V for TAO, 0.5 V for TAO s.t. and around 2.5 V for pure Al\(_2\)O\(_3\). Besides the damage induced during the Al\(_2\)O\(_3\) films’ growth, it is expected that the dielectrics containing this binary compound should intrinsically present some defect states at or close to their surface, which might induce phenomena of charge trapping and instability. [118]
5.2.4. Staggered bottom-gate and top-gate TFT structures

Besides the staggered bottom-gate structures previously analyzed, the performance of TFTs using a TSiO dielectric was also evaluated using a staggered top-gate configuration. For this batch of TFTs different lithographic masks for the dielectric and semiconductor layers were used for both device configurations, contrarily to what happened for all the remaining TFTs presented in section 5.2. A comparison between both device structures annealed at 200 °C is presented in fig. 5.40 and table 5.7.

![Comparison of the transfer characteristics obtained for GIZO TFTs using TSiO as the dielectric layer, for staggered bottom-gate and top-gate structures. Devices annealed at 200 °C.](image)

**Figure 5.40 – Comparison of the transfer characteristics obtained for GIZO TFTs using TSiO as the dielectric layer, for staggered bottom-gate and top-gate structures. Devices annealed at 200 °C.**

**Table 5.7 – Electrical properties obtained for the TFTs depicted in fig. 5.40.**

<table>
<thead>
<tr>
<th></th>
<th>( \mu_F ) (cm² V⁻¹ s⁻¹)</th>
<th>On-Off ratio</th>
<th>( V_{on} ) (V)</th>
<th>( S ) (V dec⁻¹)</th>
<th>( \Delta V_{on} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top-gate</td>
<td>15.0</td>
<td>1.3×10⁴</td>
<td>2.75</td>
<td>0.45</td>
<td>-1.8</td>
</tr>
<tr>
<td>Bottom-gate</td>
<td>31.6</td>
<td>8.7×10⁵</td>
<td>-0.75</td>
<td>0.36</td>
<td>0.8</td>
</tr>
</tbody>
</table>

First, note that the properties of bottom-gate TFTs are generally degraded in comparison to the ones presented in fig. 5.38 and table 5.6, even if a higher \( T_A \) is used here,⁹ which should be a consequence of the extra lithographic steps introduced between the TSiO and the GIZO deposition processes.

The electrical properties are negatively affected when using the top-gate configuration. Even if TSiO deposition constitutes a relatively low-damage process when compared with the other tested dielectrics, the results suggest that the interface with GIZO is significantly affected by the bombardment effects inherent to the sputtering process. For lower \( T_A \) and for other tested dielectric materials, such as TAO s.t., the differences between both device configurations are even larger, reinforcing the idea that defect creation at or close to the interface with GIZO due to intense

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⁹ For similarly processed devices, \( T_A=200 \) °C leads to slightly improved performance over \( T_A=150 \) °C.

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bombardment should be the dominant mechanism dictating the poor performance of top-gate structures employing sputtered dielectrics.

Even if these differences can be attenuated in the future, for instance by using buffer layers deposited at low $P_{fj}$ between the semiconductor and the bulk dielectric in top-gate structures, for GIZO TFTs it seems that there are no great advantages of using a top-gate structure. One could think about instantaneous passivation of GIZO back surface using this kind of structure, but for subsequent integration of the devices in electronic circuits a dedicated passivation layer step would still be required. However, for other oxide semiconductor-based TFTs there seem to be good advantages in using top-gate structures: for instance, on ZnO TFTs it is suggested that improved performance could be achieved using this configuration because the ZnO seed layer (see fig. 4.4a) would not be at the dielectric/semiconductor interface, which would be rather composed by the larger grains that exist in the top of the ZnO layer. [44]

5.2.5. Electrical stability measurements

Different electrically stability measurements were performed on staggered bottom-gate TFTs using different dielectrics. The most relevant results are presented and discussed in this section.

5.2.5.1. Constant drain current stress

It was already shown in tables 5.5 and 5.6 that some differences in $I_D$ values arise when the TFTs employing sputtered dielectrics are subjected to constant $I_D$ stress measurements, specially for pure Ta$_2$O$_5$-based devices. However, even for cases where low $I_D$ variations are observed, it is well known that instability mechanisms derived from non-ideal dielectric layers can result in effects such as large shifts of the transfer characteristics, preventing a circuit where these transistors are used from operating properly. [13] Thus, it is imperative to analyze the behavior of these structures when subjected to $I_D$ stress measurements. The experimental conditions were exactly the same as the ones used to analyze the Si/SiO$_2$ TFTs presented in section 5.1.6.1, except the $I_D$ value considered for $V_T$ determination: in this case, due to the higher $I_D$ of sputtered dielectrics, $V_T$ was extracted at $I_D=1$ nA. For all the devices the GIZO back surface was exposed to the air, i.e., no passivation layer was used. Starting with the TFTs with Ta$_2$O$_5$ (fig. 5.41), the evolution of their properties follows the expected trend when charge trapping at the dielectric or at its interface with GIZO is the dominant instability mechanism. [105] The transfer curves shift in a parallel way, hence without an appreciable change in
μ_{FE}’ or S. Only V_T shifts significantly during stress, about 5 V, but the initial properties are almost recovered 4–5 h after the stress test. After 1 week, the initial device properties are fully recovered. This is consistent with predominant electron trapping at the dielectric/semiconductor interface and the creation of extra trapping sites is not likely to occur, because the properties are recovered without any annealing treatment. [1, 77, 105] Still, even after 1 week recovery time, I_G at V_G=15 V is more than two orders of magnitude higher than in the initial state, suggesting an irreversible creation of defects on Ta_2O_5, possibly facilitated by the low band offset of this material with GIZO.

Figure 5.41 – Results obtained from constant I_G stress measurements on GIZO TFTs annealed at 150 °C with a Ta_2O_5 dielectric: (a) transfer characteristics evolution; (b) ΔV_T and ΔS evolution.

The transistors with TSIO show a different stress behavior when compared with the Ta_2O_5 ones (fig. 5.42). As with Ta_2O_5, appreciable μ_{FE} variations are also not detected for these devices. ΔV_T reaches a maximum of 1.75 V after 24 h (only 0.3 V after 10 h), recovering after 3–4 h. In addition, only a small and recoverable increase in I_G is verified after a 24 h stress. However, TFTs with a TSIO dielectric generally exhibit an increase in the Off-current with stress time, affecting the subthreshold region, thus the S value, which increases to around 0.55 V after the 24 h stress.\(^1\) The reason behind this phenomenon is still under study but should be related to non-idealities also found in output characteristics measured with a very small V_{GS}, where an abrupt increase in I_G happens for a high V_{DS} when the device should supposedly be in the saturation regime. As a positive remark, the devices can sustain repeated stress/recovery cycles similar to the ones presented herein, without a permanent degradation of their electrical properties.

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\(^1\) Given that the maximum μ_{FE} is obtained at the higher V_G used in these measurements, the absolute μ_{FE} value is naturally affected by a V_{Sn} (V_I) shift. However, the important feature to consider is if μ_{FE}(V_G-V_I) trends are compared, they are essentially unchanged during the stress measurements.

\(^1\) Given that these stress measurements and analysis are time consuming, only three TSIO devices from different substrates could be analyzed to clarify the nature of this feature, which was found to be valid in two of them. Hence, it is possible that this increase in the Off-current and S during stress is also related with some non-controllable processing parameter, although it should be pointed out that TSIO was the only dielectric exhibiting this feature.
The most unstable properties are verified in the TFTs based on the TAO s.t. dielectric (fig. 5.43), in accordance with the higher hysteresis of the Ta₂O₅-Al₂O₃ dielectric system. In spite of no appreciable or permanent degradation is verified in 𝐼₀ and the Off-current, the curves shift significantly toward a positive 𝑉ₒ (Δ𝑉ₒ=12 V), which is accompanied by the appearance of noticeable kinks and by an increase of Δ𝑆 after the 24 h stress. Given this, it seems that two concurrent factors play an important role in the instability of the transistors with TAO s.t. dielectric: charge trapping at or close to the dielectric/semiconductor interface and creation of defect states or ion migration on the Al₂O₃-containing dielectric after some stress time, which can only be removed by a subsequent annealing treatment. This is reinforced by the recovery dynamics of these devices, where it can be seen that the initial 𝑉ᵣ is almost fully recovered after 1 week (𝑉ₒ is actually fully recovered), but the kink still persists. After the annealing treatment, the initial properties are re-established, which can also indicate that charge injection in the dielectric can occur during stress. [90, 110] Defect creation in oxides is known for a long time [120] and for instance, in the particular case of Al₂O₃, is believed to be responsible not only for instability [118] but also for interesting effects such as resistive switching in memories, [121] but the exact dynamics of all these defect creation processes are not clear to date.

The shifts observed on the electrical properties for TFTs with sputtered dielectric layers are, as expected, larger than the ones verified for TFTs on Si/PECVD SiO₂ (fig. 5.30). Still, note that the processing temperatures involved on the fabrication of both types of dielectric layers are totally different and much higher for PECVD SiO₂. Additionally, when considering TSiO, Δ𝑉ᵣ is minor and the moderate Δ𝑆 is fully reversible without any subsequent annealing treatment, which is highly promising regarding future efforts to improve the reliability of TFTs employing low temperature dielectrics when subjected to aggressive electrical stress conditions, as the ones presented herein.
5.2.5.2. Square wave on gate electrode stress

Besides functioning as current drivers for the next generation of OLED displays, TFTs should also be able to work as simple On-Off switches, for instance, to turn On and Off the pixels of an LCD or OLED display. [3] A preliminary test was made to TFTs with TSiO and TAO s.t. dielectrics regarding their application as switches. For that, the TFTs were subjected to a gate stimulus consisting of a square wave with frequencies of 2 Hz and 10 kHz, ranging between $V_G=-5$ and 10 V (which corresponds to the Off- and On-states of the transistors), superimposed to a continuous $V_D=15$ V. The 2 Hz and 10 kHz tests were run during 40 and 20 min, respectively, being the resulting $I_D$ continuously monitored (fig. 5.44).

![Figure 5.43](image)

Figure 5.43 – Results obtained from constant $I_D$ stress measurements on GIZO TFTs annealed at 150 °C with a TAO s.t. dielectric: (a) transfer characteristics evolution; (b) $\Delta V_T$ and $\Delta S$ evolution.

![Figure 5.44](image)

Figure 5.44 – Results obtained from stress measurements consisting on applying a square wave signal as $V_G$ on GIZO TFTs annealed at 150 °C employing TSiO and TAO s.t. dielectrics: (a) evolution of On- and Off-currents during stress measurements at 2 Hz, during 40 min; (b) transfer characteristics before and after stress measurements at 10 kHz, during 20 min.
As verified in figs. 5.44a and 5.44b, the TSiO devices do not present any degradation for both frequencies. The Off-current and S increase during $I_D$ stress mentioned in the previous section for these TFTs should not be relevant here, since they are only visible when the devices are subjected to a constant $I_D$ (or $V_G$) signal during a long period of time, typically more than 1 hour. In fact, by measuring the same TFTs repeatedly using the square wave methodology during a larger time scale (around 3 hours), significant variations were still not observed.

A different situation is verified for the TFTs using TAO s.t. dielectrics. For these devices, a large shift on the transfer characteristics is observed as the stress measurement progresses, resulting in a decrease of the On-current with time for both tested frequencies. This behavior is in agreement with the results of the previous section, where it was observed that charge trapping at the dielectric/semiconductor interface was significant right from the beginning of the $I_D$ stress test (fig. 5.43). Although non-idealities such as kinks in the transfer characteristics were not observed at the end of the square wave stress tests, which should be consistent with the absence of defect state creation during these short tests, the decrease of On-current means that trapped charges are not released during the negative part of the square wave cycle. In fact, the initial characteristics are only re-established after 1-2 hours of recovery time, but an annealing treatment is not necessary for recovery because there should be no creation of new defect states.

Naturally, these are only preliminary results and more detailed tests at higher frequencies should be performed in the near future.

5.3. Conclusions

Throughout this chapter it was shown that semiconductor composition, processing and post-processing conditions, source-drain electrodes, passivation layer and dielectric materials all have a significant effect on the electrical properties achieved on oxide semiconductor-based TFTs. The results obtained on devices, which are in agreement with the conclusions from chapter 4 regarding isolated oxide semiconductor and dielectric thin films, are summarized as follows:

- Concerning the processing of the oxide semiconductor layer, it is clear that for best overall performance deposition conditions assuring a moderate $N$ should be used. Materials with a very low $N$ typically have a large number of unfilled traps at zero-gate bias state, resulting in devices with high $V_{on}$ and $\Delta V_{on}$ and low $\mu_{FE}$. On the other hand, free carriers on large $N$ materials (above $\approx 10^{18}$ cm$^{-3}$) are difficult to deplete even using negative $V_G$, resulting in useless field-effect devices. Hence, for the range of deposition conditions studied here, the best compromise to achieve a moderate $N$, low trap state density and good performing TFTs is selecting a low (but non-zero)
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%O₂, between 0.4 and 1.0 %, 〈pₚₑDeveloper=0.7 Pa and 〈Pᵣₜ=1.1 W cm⁻². As expected, composition has a major role defining the final properties of the devices, being the properties of TFTs employing multicomponent amorphous oxides based on the gallium-indium-zinc oxide system considerably improved when compared with the binary polycrystalline oxides of this system. When compared with ZnO, GIZO TFTs allow for much better performance, namely higher 〈μₑₑ and lower S, mostly attributed to the grain barrier inhibited transport on ZnO, absent in GIZO. Indium-richer compositions allow for higher 〈μₑₑ but also higher N, resulting in always-on TFTs. To solve this, higher concentrations of zinc and/or gallium should be used, but small ln/(ln+Zn+Ga) atomic ratios lead to large 〈V_on and 〈ΔV_on and low 〈μₑₑ. For optimized GIZO compositions, around 2:4:1 and 2:4:2, using the %O₂, 〈pₚₑDeveloper and 〈Pᵣₜ mentioned above, excellent TFT performance can be achieved, with 〈μₑₑ=50 cm² V⁻¹ s⁻¹, 〈V_on=1 to 0 V, negligible 〈ΔV_on, S=0.25 V dec⁻¹ and On-Off ratio exceeding 10⁸. However, even for devices employing semiconductor layers with N=10¹⁸ cm⁻³, remarkable field-effect and close to 0 V 〈V_on are possible to achieve, provided that 〈d is reduced to very small values, typically 10 nm or even less. This is possible due to the interaction of the back surface of the semiconductor layer with environmental oxygen, forming a depletion region that for low 〈d can reach the dielectric/semiconductor interface. For lower N oxide semiconductors, the effect of 〈d can be used to modulate 〈V_on, without significantly affecting the remaining electrical properties. The effect of 〈Tₐ on the performance of the TFTs assumes different magnitudes depending on the as-deposited properties of the oxide semiconductors. For as-deposited thin films with large N (not possible to deplete with 〈V_on), as 〈Tₐ increases 〈ρ can be substantially decreased, rendering the materials usable as channel layers in transistors. On the other hand, for initially low N materials possessing large unfilled trap state densities, increased 〈Tₐ can bring enhanced properties via annihilation of some of the defect levels – both at the bulk of the semiconductor and at its interface with the dielectric – and structural relaxation. The properties of TFTs comprising oxide semiconductors processed under ideal conditions (composition, %O₂, 〈pₚₑDeveloper, 〈Pᵣₜ and 〈d) present considerably less dependence on 〈Tₐ. Still, when 〈Tₐ=500 °C is used, these TFTs present a significant degradation of their properties, mostly attributed to issues arising at the source-drain contact regions, because the annealing treatment is performed at the final stage of device production (and not before source-drain deposition). The effectiveness of a low 〈Tₐ treatment to improve the uniformity of properties between devices intentionally or non-intentionally produced with different processing conditions is also shown:

- If a low 〈Tₐ (150-200 °C) is used on optimized GIZO devices, similar properties are obtained whether Ti/Au or IZO source-drain electrodes are employed. For higher 〈Tₐ (300 °C), a degradation of the electrical properties occurs for both electrodes, but is more evident for IZO, since the 〈ρ of this material increases around one order of magnitude due to significant oxidation as 〈Tₐ
increases. The extraction of intrinsic electrical parameters and series resistance using the TLM procedure allows to conclude that TFTs with small $l$ can start to be limited by contact resistance effects. This is specially relevant for devices where the semiconductor is produced under non-ideal conditions (for instance, with high $\%O_2$) and/or the final structures are annealed at temperatures above 200 °C;

- The effect of different passivation layers on the performance of GIZO TFTs was also briefly analyzed. From all the tested materials, only spin-coated SU-8 can provide adequate device protection while maintaining similar electrical properties when compared with unpassivated devices. For sputtered or e-beam passivation schemes (SiO$_2$ and MgF$_2$), always-on (or at most largely negative and unstable $V_{on}$) devices are obtained, presumably because the depletion layer at the GIZO back surface can no longer be maintained and can even be replaced by an accumulation layer. The effectiveness of the SU-8 passivation layer is also proved by the stability of electrical properties when the devices are measured under vacuum, which does not happen for non-passivated transistors;

- Regarding the integration of sputtered dielectrics on GIZO TFTs, it was shown that for binary compounds, within the range of deposition and post-deposition conditions studied in this work, only Ta$_2$O$_5$ and HfO$_2$ provide good electrical performance. The mixture of Ta$_2$O$_5$ with SiO$_2$ (TSIO) or Al$_2$O$_3$ (TAO) allows to obtain devices with considerably lower $I_{on}$, specially for TAO when sputtered from a single target (s.t.). However, the TAO system always results in devices with larger $\Delta V_{on}$ than TSIO, anticipating charge trapping effects at the dielectric/semiconductor interface (see next paragraph). For TFTs with these multicomponent amorphous dielectrics, properties as $\mu_{fe}=30$ cm$^2$ V$^{-1}$ s$^{-1}$, $V_{on}=-1$ to 1 V, S$<0.25$ V dec$^{-1}$ and On-Off ratios between $10^6$ and $10^7$ are obtained, comparing quite favorably with devices fabricated on top of PECVD SiO$_2$, which involve considerably higher maximum processing temperatures (150 against 400 °C). Staggered top-gate TFTs were also fabricated using a TSIO dielectric, but the properties are considerably degraded when compared against the staggered bottom-gate structure because of the deleterious effects of GIZO surface’s bombardment during the sputtering of the dielectric layer.

Besides the points summarized above, several stress measurements were also presented and briefly discussed, in order to access the main instability mechanisms present on these TFTs and also to evaluate their usefulness in electronic circuits. For devices produced on Si/SiO$_2$ substrates, it was found by constant $I_{on}$ stress measurements that GIZO layers produced with low $\%O_2$ lead to the most stable devices, with small and fully recoverable $\Delta V_{T}$ and $\Delta S$, contrarily to devices having GIZO layers processed with large $\%O_2$, where a high $\Delta V_{T}=10$ V is attributed to significant charge trapping effects. ZnO TFTs present large instability even if processed under optimized conditions, due to charge trapping and defect state creation/removal. Increased $T_A$ leads to enhanced stability and for SU-8
passivated devices the best results are found, which is ascribed to the suppression of field-enhanced oxygen adsorption/desorption processes occurring at the back surface of GIZO in non-passivated devices. Constant \( I_D \) stress measurements were also performed in some TFTs employing sputtered dielectrics. The transfer characteristics of devices with a Ta₂O₅ dielectric are shifted towards positive \( V_G \) values but the initial properties are reestablished, however, \( I_D \) permanently increases after stress. TFTs with TSiO present negligible \( \Delta V_T \) but \( \Delta S \) increases during stress, although the initial properties are fully recoverable. The most unstable properties are obtained for TFTs with TAO s.t., which present both large \( \Delta V_T \) and \( \Delta S \) that are only recoverable after a subsequent annealing treatment, consistent with severe defect state creation during stress and/or charge injection in the dielectric. The stress measurements performed using a square wave with different frequencies as an input \( V_G \) signal confirm the instability of TFTs with TAO s.t., but reveal that devices having TSiO can be switched On and Off a large number of times without affecting their electrical properties.

Aging effects were also analyzed regarding different oxide semiconductor processing and post-processing conditions, for non-passivated TFTs produced on Si/SiO₂ substrates. Devices employing an optimized semiconductor process that allows obtaining close to 0 V \( V_{on} \) as an initial characteristic (month 0), using for instance GIZO 2:4:2, \%O₂=0.4 %, \( p_{dep}=0.7 \) Pa and \( P_{in}=1.1 \) W.cm⁻², do not present significant changes on their electrical properties during 18 months, even for a low \( T_A=150 \) °C. However, devices maintaining either a favorable composition but a large \%O₂ or the same deposition conditions but an indium-rich composition present very large deviations on their electrical properties during the 18 months test. Interestingly, after the 18 months, the transfer characteristics converge in both cases for a close to 0 V \( V_{on} \). Higher \( T_A \) (300 °C) is demonstrated to be effective in turning the unstable and large \%O₂ device into a stable TFT over time.

Finally, it is plausible to assume that the TFTs analyzed in this chapter are affected by fringing currents which sum to the current flowing between the area delimited by the width of source and drain electrodes, because the active layer is slightly wider than the width of the source-drain contacts. Still, even assuming a reduction to half of the \( \mu FE \) values reported herein (see fig. 5.28a), these continue to be considerably larger than the ones obtained with competing technologies, such as organic and a-Si:H TFTs. This renders the oxide semiconductor-based TFTs highly promising for the next generation of fast, low-cost and transparent electronic circuits.

5.4. References


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5. Properties of n-type oxide semiconductor-based TFTs


Chapter 6

Active matrix backplanes with n-type oxide semiconductor-based thin-film transistors and their integration with a liquid crystal display frontplane

The optimization work presented in the last two chapters culminates in the fabrication of active matrix backplanes composed by TFTs based on multicomponent amorphous oxide semiconductors and high-κ dielectrics. These backplanes are then integrated with a LCD frontplane by Hewlett-Packard (in the framework of the Multiflexioxes European project), to show the viability of the TFT technology developed during this work for display applications. This chapter, more oriented to technological aspects than the previous ones, which were essentially focused on scientific research of materials and devices' properties, shows the initial results achieved with these integration tests, presenting also the most relevant processing challenges found when moving from the fabrication of isolated devices in 2.5×2.5 cm substrates to the fabrication of arrays of interconnected TFTs in 10×10 cm substrates.

6.1 – Process flow and backplane structure

The backplanes were fabricated on 10×10 cm Corning 1737 glass substrates, using the mask layout depicted in fig. 6.1.

![Figure 6.1](image_url)

*Figure 6.1 – Mask layout used to fabricate the active matrix backplanes.*

This layout, built using a total of 5 lithographic masks, comprises several parts:
• A 5×5 cm active area consisting of an array of 128×128 pixels, each pixel having an approximate area of 350×350 µm. The architecture followed here is the simplest possible, with a single TFT per pixel, with W/L=35/10 µm;

• 8 sets of pads (2 on each side) to connect the external driver circuitry to control the 128 rows and 128 columns;

• 16 TFTs (4 on each side) located on the periphery of the active area, to evaluate the electrical performance of the devices composing the active matrix. Each side includes a set of 4 TFTs with different W/L ratios, namely 35/10, 35/20, 25/10 and 25/20 µm;

• 8 capacitors (2 on each corner), to measure the capacitance of the dielectric layer;

• 4 sets of profilometer structures (1 on each corner), to measure the thickness of the different layers composing the active matrix.

**Figure 6.2** – Process flow used to produce the active matrix backplanes. The figure in the bottom shows the final backplane structures, both transparent (left) and non-transparent (right). A glass (center) is shown for comparison.
The process flow to fabricate the backplanes is presented in fig. 6.2. It consists essentially on the same processes used for the production of the TFTs using sputtered high-κ dielectrics (fig. 5.36, p. 203), with the main exception being the dielectric processing and patterning. Here, excluding the passivation layer, a 4 mask process had to be used, rather than the 3 mask process used for the isolated TFTs, since the dielectric layer also has to provide electrical insulation at the intersection of the lines and columns of the active matrix. Also, due to the lack of reliability associated with lift-off processes, the dielectric layer had to be patterned using RIE. Additionally, a passivation layer had to be deposited in all the backplanes (contrarily to what happened for isolated devices, where only selected samples were passivated), since the active area had to be protected before integration with the frontplane.

6.2 – Moving to larger areas and to TFT arrays: processing challenges

Even if the backplane’s process flow is very similar to the one used to successfully produce the TFTs presented in the last chapter, there are several points which are extremely important to consider when moving to a process where larger areas and larger yields are required. Below is a description of the most usual problems found during this work that significantly affected the performance of the produced backplanes:

- **Substrate cleaning** – a large number of particles or residuals (such as water or acetone stain) in the surface of the substrate or of the deposited films can considerably deteriorate the properties of the devices. In the most extreme situation, these contaminants can be trapped at the interface of thin films, can turn the photoresist coating less effective or can result in bad adhesion of subsequent deposited layers. An example of this effect is shown in fig. 6.3 for a Ti gate electrode, being visible that several features are irreversibly damaged. For the isolated devices presented in the previous chapter, this is a considerably minor problem, resulting only in some non-working transistors, but when considering an array of TFTs the damage shown in fig. 6.3 automatically results in the failure of two lines of the active matrix. The existence of a large number of particles can also be problematic for the SU-8 passivation layer: given that SU-8 is very viscous to assure a thickness of a few μm, its spinning process is more sensitive to particles lying on the substrate, creating some areas where the layer is clearly not uniformly distributed. Naturally, this results in additional problems for the subsequent integration with the frontplane, for which a very smooth and uniform surface is required. Even if no special cleaning protocols were established for this work, careful cleaning of substrates with acetone and isopropilic alcohol (IPA) were performed prior any processing. Oxygen plasma treatments, generally used to remove organic contaminants from surfaces, [1] were also tested, but no significant advantages were detected;
Annealing furnace – since the substrates are now 10×10 cm, a new furnace was required to perform the annealing steps, before and after SU-8 spin-coating. In order to replicate the same annealing conditions as for the test devices described in chapter 5, a large tubular furnace normally used for crystalline silicon processes was used. However, the devices reveal considerably worse properties and reliability, presumably due to some sort of contamination of the furnace tube. To solve this, the annealing process started to be performed with a different setup, using a hot-plate with controllable heating ramp. Since the heat transfer to the substrate and deposited films is significantly different when using a tubular furnace or an hot-plate, annealing time and (mainly) $T_a$ had to be adjusted to obtain similar properties for both setups, using for that study TFTs produced on 2.5×2.5 cm substrates;

Layers’ uniformity – it is well known that depending on the deposition conditions and on the sputtering system itself, the properties of thin films exhibit a considerable spatial distribution over the substrate area. For instance, Minami et al. showed that $\rho$ and $N$ of IGO films can present variations of about one order of magnitude in a 10×10 cm substrate. [2] Furthermore, thickness variations are naturally higher for larger substrates, and as seen in chapter 5, thickness of oxide semiconductors plays an important role defining the properties of TFTs. The thickness uniformity-electrical properties relation was observed to be of major importance for the fabrication of GIZO TFTs in large area (30×40 cm) glass substrates by Lee et al. [3] Wet-etching processes can also be problematic if large thickness variations exist, leading to severe under-etching on thinner film regions. This effect is shown in fig. 6.4a for a non-uniform IZO film ($\approx$25% thickness variation), where longer etching times were required to wet-etch all the film, resulting in under-etched features on thinner film regions. On the other hand, for anisotropic etching processes such as RIE, large thickness variations can lead to undesired removal of other materials if the reactive gas is not selective between the different materials of the structure, as shown in fig.6.4b for a thin titanium layer beneath a non-uniform $\text{Ta}_2\text{O}_5$ layer etched using $\text{SF}_6$. The oxide
semiconductor and the dielectric were the layers where uniformity was found to be more relevant and for their production different configurations and processing conditions were studied in order to maximize uniformity. These results will be shown in section 6.3;

![Figure 6.4](image)

**Figure 6.4** – (a) Non-uniform IZO layer exhibiting severe under-etching; (b) Undesired removal of titanium due to long RIE process to etch a non-uniform Ta$_2$O$_5$ layer.

- **Patterning and etching processes** – For the isolated TFTs produced in 2.5×2.5 cm substrates discussed in chapter 5, all the layers were defined using lift-off processes. Although lift-off generally results in patterns with lower resolution than the obtained with conventional lithography, this does not constitute a critical issue for the dimensions used on the present devices. Lift-off has the advantage of turning possible the selective patterning of virtually any material deposited at low temperature (higher temperatures would damage the photoresist), without affecting other materials previously deposited. However, some aspects can limit the applicability of lift-off: photoresist can be damaged during a physical deposition process such as sputtering, even if performed without intentional substrate heating, due to the high kinetic energy of the species arriving to the substrate, exposure to UV radiation and increased substrate temperature. Under these conditions, the resist can reach temperatures above its softening point (110-130 °C), which rounds the resist profile, making the deposited material to cover also the resist sidewalls, turning harder subsequent lift-off processes. [4] This photoresist degradation is specially important for a ballistic plasma transport regime (low $p_{dep}$ and high $P_{RI}$). [5] which was used to produce the dielectric and transparent electrode thin films in this work. Even using a more thermally stable photoresist such as AZ TI 35ES, instead of the typically used AZ 6612 or AZ 6632, no significant improvements were observed. Additionally, based on the inherent aspects to the sputtering process mentioned above, thicker films such as the dielectrics ($\approx$300-400 nm) are naturally harder to lift-off than thin films such as the oxide semiconductors ($\approx$10-40 nm). All this creates important issues when trying to define the patterns of the layers, mainly the dielectric. In fact, for this layer, severe photoresist degradation was always verified after deposition (fig. 6.5a), turning inevitable the usage of ultrasonic bath to perform the lift-off process. But even if the
substrate is subjected to an ultrasonic bath for a long time (more than 30 minutes), a considerable amount of photoresist (and the film deposited on top of it) can remain in the substrate. This was not improved even by using aggressive lift-off solutions such as NH₄OH:H₂O₂ (RCA). [6] This residual photoresist may eventually be removed during subsequent lift-off processes of other layers and besides that, due to the violence inherent to the ultrasonic bath, the final film patterns can get damaged, even if no residual photoresist remains in the substrate. Figure 6.5b shows an example of how these effects can result in the irreversible failure of a TFT. The cross section image clearly shows a discontinuity in the composing layers, most probably caused during the lift-off process. Alternatively, this sort of failure may also permit that subsequent conductive layers infiltrate through the crack, causing a short-circuit between gate and source-drain electrodes. Again, in substrates where TFTs are grown isolated (chapter 5), this can lead to a few non-working devices but in active matrices, where TFTs are interconnected, it can ruin several (or even all) lines or columns. Thus, different etching processes are required to produce the backplanes, at least for the most critical layer, the dielectric. This was achieved using RIE, as will be shown in section 6.4.

![Figure 6.5](image)

*Figure 6.5 – (a) Photograph of a backplane after dielectric deposition on top of photoresist, for subsequent lift-off process; (b) Cross section of a TFT structure obtained by SEM, showing a catastrophic discontinuity in all the layers, possibly caused during a lift-off process.*

These last two points, layers’ uniformity and patterning/etching processes, were the ones requiring more effort and optimization, being described in some detail in the next sections.

### 6.3 – Uniformity optimization and its effect on the electrical properties

#### 6.3.1 – Dielectric layer

The uniformity of the dielectric layer had to be optimized mainly due to two factors: first, to assure that similar electrical properties could be obtained across all the substrate area (for instance, regions with lower thickness or subjected to more severe bombardment could present higher leakage
current); second, to allow for complete etching of the film by RIE in all the substrate area without affecting the layers beneath it. The AJA sputtering system used to produce the dielectric films is equipped with a magnetron tilting feature, which allows to adjust the con-focal orientation of the magnetrons relatively to the substrate. This feature was successfully used to optimize the uniformity of co-sputtered TSiO films, as shown in fig. 6.6 and table 6.1. The difference between the “with chimney” and “with chimney, magnetron tilt” configurations is that in the latter the magnetrons were tilted outward relatively to the former, pointing to a position between the points 5 and 6 of fig. 6.6b.

![Figure 6.6](image.png)

Figure 6.6 – Photograph of silicon wafers coated with TSiO deposited using three different magnetron configurations, clearly showing large thickness variation for the “with chimney” setup; (b) Schematic of the substrate regions where the thickness was measured for each magnetron configuration.

Table 6.1 – Thickness measured by spectroscopic ellipsometry in the substrate regions represented in fig. 6.6b, for the different magnetron configurations. X and SD represent the mean and standard deviation, respectively.

<table>
<thead>
<tr>
<th>Position</th>
<th>With chimney (nm)</th>
<th>With chimney, magnetron tilt (nm)</th>
<th>Without chimney (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>103.0</td>
<td>97.0</td>
<td>118.0</td>
</tr>
<tr>
<td>2</td>
<td>91.5</td>
<td>98.0</td>
<td>116.0</td>
</tr>
<tr>
<td>3</td>
<td>90.5</td>
<td>97.5</td>
<td>115.5</td>
</tr>
<tr>
<td>4</td>
<td>90.5</td>
<td>98.5</td>
<td>115.0</td>
</tr>
<tr>
<td>5</td>
<td>95.0</td>
<td>100.5</td>
<td>115.0</td>
</tr>
<tr>
<td>6</td>
<td>101.0</td>
<td>104.0</td>
<td>117.0</td>
</tr>
<tr>
<td>X; SD</td>
<td>95.3; 5.5</td>
<td>99.3; 2.6</td>
<td>116.1; 1.2</td>
</tr>
</tbody>
</table>

To show the significant effect that different magnetron configurations can have on the electrical properties of devices, results for another configuration (“without chimney”) are also presented here, consisting of simply removing the chimneys from the top of the targets (fig. 3.4b, p. 52), in order to disperse the sputtered species through a larger area of the substrate region. Even if the thickness
uniformity of TSiO films is improved using this configuration, it is crucial to know what is the effect on the electrical properties of devices. To access this information, TFTs were produced in 2.5×2.5 cm substrates placed close to position 3 (fig. 6.6b). Although \( I_G \) is not significantly affected by the magnetron configuration, the results show an overall deterioration of device performance for the “without chimney” configuration (fig. 6.7a), with the larger hysteresis and higher \( V_{on} \) suggesting worse dielectric and dielectric/semiconductor interface properties for these TFTs. To reinforce this, \( \mu_E \) is also considerably lower (fig. 6.7b) and for the lowest \( T_A \) (150 °C) it is noticeable the decrease of \( \mu_E \) for higher \( V_G \), consistent with increased interface scattering effects. [7, 8] This phenomenon disappears after annealing at 200 °C, proving once again the advantageous effect of the thermal treatment on device performance, as explained in chapter 5, but \( \mu_E \) still remains considerably lower than the obtained for the “with chimney” configuration. A possible cause for these differences is the lower compactness of the films produced with the “without chimney” setup, as suggested by the spectroscopic ellipsometry analysis of the films.

![Graphs showing electrical properties of GIZO TFTs with TSiO dielectric produced using two different magnetron configurations](image)

**Figure 6.7** – Electrical properties of GIZO TFTs with a TSiO dielectric produced using two different magnetron configurations: (a) transfer characteristics obtained in double sweep mode \((T_A=200 °C)\); (b) \( \mu_E-V_G \) plots for \( T_A=150 \) and 200 °C.

Given this, the “with chimney, magnetron tilt” configuration was chosen to fabricate the dielectric layer of the active matrix backplanes, consisting on the best compromise between thickness uniformity and electrical properties.

### 6.3.2 – Oxide semiconductor layer

Regarding the oxide semiconductor layer, the requirement of good uniformity was solely based on its effect on the electrical properties. Uniformity was not a major concern with respect to the patterning/etching processes for this layer, because it had to be patterned by lift-off in order to have selectivity relatively to the transparent IZO gate electrode beneath it. The home-made sputtering
system used to fabricate the oxide semiconductors didn’t have the tilting angle feature of the AJA system. Instead, the magnetron surface is always parallel to the substrate, with the magnetron and substrate central regions being coincident. Hence, to study and optimize the uniformity of this layer, three different setups were tested, always using the same %O, \( P_{dep} \) and target composition (0.4 %, 0.7 Pa and GIZO 2:4:2, respectively):

- **Setup 1** – Target-to-substrate distance of 15 cm, with \( P_{rf} = 1.1 \, \text{W cm}^{-2} \). This was the typical setup used to produce the films and devices presented in chapters 4 and 5;
- **Setup 2** – Target-to-substrate distance of 20 cm, maintaining the same \( P_{rf} \) but increasing deposition time to obtain the same thickness as in “setup 1” (growth rate varies approximately with the inverse of the target-to-substrate distance);
- **Setup 3** – Target-to-substrate distance of 20 cm, raising \( P_{rf} \) to achieve the same growth rate as in “setup 1” (as seen in chapter 4, fig. 4.2d, growth rate is proportional to \( P_{rf} \)).

For each setup, 3 TFTs on Si/SiO\(_2\) substrates were produced, distributed in an area of 10x10 cm according to the schematic in fig. 6.8.

![Figure 6.8 – Schematic of the setup used to study the uniformity of the oxide semiconductor layer, comprising 3 2.5x2.5 cm Si/SiO\(_2\) substrates distributed in the diagonal of a 10x10 cm substrate.](image)

Thickness is found not to change appreciably in the 10x10 cm area for the different setups, as shown in table 6.2. The variations are always lower than 5 %, which for this range of thicknesses is close to the error associated with the profilometry measurement.

*Table 6.2 – Thickness measured by profilometry on the 3 TFTs produced for each setup. X and SD represent the mean and standard deviation, respectively.*

<table>
<thead>
<tr>
<th>Position</th>
<th>Setup 1 (nm)</th>
<th>Setup 2 (nm)</th>
<th>Setup 3 (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TFT A</td>
<td>49.8</td>
<td>49.5</td>
<td>48.8</td>
</tr>
<tr>
<td>TFT B</td>
<td>52.4</td>
<td>48.0</td>
<td>46.3</td>
</tr>
<tr>
<td>TFT C</td>
<td>50.5</td>
<td>47.9</td>
<td>47.5</td>
</tr>
<tr>
<td>( X ; SD )</td>
<td>50.9 ; 1.3</td>
<td>48.5 ; 0.9</td>
<td>47.5 ; 1.3</td>
</tr>
</tbody>
</table>
The electrical properties of the devices were evaluated by the transfer characteristics and by the parameters $\mu_{FE}$, $V_{on}$ and $\Delta V_{on}$ in 3 consecutive measurements, before and after annealing at 200 °C. The results for non-annealed devices (fig. 6.9 and table 6.3) show that for the different setups the TFT B is the one exhibiting worse properties, while TFT A and C have similar performance. This would be expected given the geometry of the sputtering system (center of the magnetron facing the center of the substrate), suggesting that TFT B is subjected to more intense bombardment, which affects the GIZO film and its interface with SiO$_2$ by the creation of a larger density of defects where the electrons capacitively injected by the gate potential are trapped, resulting in lower $\mu_{FE}$ and larger $V_{on}$ and $\Delta V_{on}$. Based on this, it makes sense that the configuration more affected by this effect is “setup 1”, where the target-to-substrate distance is lower, followed by “setup 3”, where although the target-to-substrate distance is increased, higher $P_{rf}$ is used.

![Figure 6.9 – Transfer characteristics obtained for non-annealed GIZO TFTs produced with setup 1, 2 and 3.](image)

![Table 6.3 – Electrical properties obtained for the non-annealed devices depicted in fig. 6.9. X and SD represent the mean and standard deviation, respectively.](table)

<table>
<thead>
<tr>
<th></th>
<th>Setup 1</th>
<th></th>
<th>Setup 2</th>
<th></th>
<th>Setup 3</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$H_{FE}$ (cm$^2$ V$^{-1}$s$^{-1}$)</td>
<td>$V_{on}$ (V)</td>
<td>$\Delta V_{on}$ (V)</td>
<td>$H_{FE}$ (cm$^2$ V$^{-1}$s$^{-1}$)</td>
<td>$V_{on}$ (V)</td>
<td>$\Delta V_{on}$ (V)</td>
</tr>
<tr>
<td>TFT A</td>
<td>55.4</td>
<td>0.5</td>
<td>2.0</td>
<td>48.1</td>
<td>2.5</td>
<td>3.0</td>
</tr>
<tr>
<td>TFT B</td>
<td>32.0</td>
<td>8.5</td>
<td>9.0</td>
<td>46.2</td>
<td>4.5</td>
<td>5.0</td>
</tr>
<tr>
<td>TFT C</td>
<td>55.3</td>
<td>2.0</td>
<td>2.5</td>
<td>50.0</td>
<td>3.0</td>
<td>2.5</td>
</tr>
<tr>
<td>$X$ ; SD</td>
<td>47.5 ; 13.5</td>
<td>3.7 ; 4.3</td>
<td>4.5 ; 3.9</td>
<td>48.1 ; 1.9</td>
<td>3.3 ; 1.0</td>
<td>3.5 ; 1.3</td>
</tr>
</tbody>
</table>

After annealing at 200 °C, besides the improvement of all the electrical parameters, the very large differences between TFTs A, B and C disappear for all the setups, in accordance with the results presented in chapters 4 and 5, where it was seen that the discrepancies between films and devices...
tend to be attenuated after an annealing treatment. Nonetheless, the devices produced using “setup 3” still present variations on $\mu_{FE}$ and $V_{on}$ as large as 10 cm$^2$ V$^{-1}$ s$^{-1}$ and 1.5 V, respectively (fig. 6.10 and table 6.4). Due to the smaller variations and enhanced performance exhibited by the TFTs fabricated using “setup 1”, this configuration was selected for the production of the oxide semiconductor layer in the active matrix backplanes.

![Transfer characteristics obtained for 200 °C annealed GIZO TFTs produced with setup 1, 2 and 3.](image)

Table 6.4 – Electrical properties obtained for the 200 °C annealed devices depicted in fig. 6.10. X and SD represent the mean and standard deviation, respectively.

<table>
<thead>
<tr>
<th>Setup 1</th>
<th>Setup 2</th>
<th>Setup 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\mu_{FE}$ (cm$^2$ V$^{-1}$ s$^{-1}$)</td>
<td>$V_{on}$ (V)</td>
<td>$\Delta V_{on}$ (V)</td>
</tr>
<tr>
<td>TFT A</td>
<td>65.9</td>
<td>-1.5</td>
</tr>
<tr>
<td>TFT B</td>
<td>61.0</td>
<td>-1.5</td>
</tr>
<tr>
<td>TFT C</td>
<td>63.1</td>
<td>-1.5</td>
</tr>
<tr>
<td>$X$; SD</td>
<td>63.3; 2.5</td>
<td>-1.5; 0</td>
</tr>
</tbody>
</table>

### 6.4 – Patterning of the dielectric layer

As already stated in section 6.2, the dielectric layer was the most problematic to etch and lift-off was not a viable option for its patterning in the backplanes, due to the severe reliability problems and/or residual photoresist that stays on the substrates after that process. Wet-etching couldn’t be used because for all the tested etchants selectively with the IZO gate electrode of the transparent backplanes was not achieved. Hopefully, RIE provided a good solution to etch Ta$_2$O$_5$, SiO$_2$ and TSiO without affecting IZO, using SF$_6$ as the reactive gas, with a discharge pressure around 0.8 Pa. Using the same protocol, other dielectrics such as TAO could only be etched by significantly increasing $P_{rf}$.
on the RIE system, which makes the etching process to be essentially dominated by a physical component rather than a chemical one. This is not desirable, since selectively is lost and the photoresist mask is etched at a faster rate, resulting in lack of protection for the dielectric regions intended to remain on the substrate.

Even if a low $P_{rf}$ etching process was used for TSiO, a thicker photoresist than the one used for all the other layers (AZ6632 against AZ6612) was employed as the RIE mask, to prevent damage to the protected TSiO regions. Also, like pointed out before, contrarily to the TFTs analyzed in chapter 5, the backplanes had to be fabricated using a 4 mask process (excluding the passivation layer). Figure 6.11 and table 6.5 show a comparison of the electrical properties between TFTs fabricated on 2.5×2.5 cm substrates using 3 and 4 masks lift-off processes and other where a 4 mask process is employed, but RIE is used to etch the TSiO layer, with an etching rate around 25 nm min$^{-1}$.

![Transfer characteristics](image)

**Figure 6.11 – Transfer characteristics obtained for GIZO TFTs produced using different process flows, regarding the total number of masks and pattern definition techniques for the dielectric (TSiO) layer. Devices annealed at 150 °C.**

**Table 6.5 – Electrical properties obtained for the devices depicted in fig. 6.12.**

<table>
<thead>
<tr>
<th>TFT process</th>
<th>$\mu_F$ (cm$^2$ V$^{-1}$ s$^{-1}$)</th>
<th>On-Off ratio</th>
<th>$V_{on}$ (V)</th>
<th>$S$ (V dec$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 mask, lift-off</td>
<td>37.8</td>
<td>3.3×10$^6$</td>
<td>-1.0</td>
<td>0.27</td>
</tr>
<tr>
<td>4 mask, lift-off</td>
<td>18.1</td>
<td>6.2×10$^5$</td>
<td>-0.5</td>
<td>0.48</td>
</tr>
<tr>
<td>4 mask, RIE</td>
<td>26.7</td>
<td>1.3×10$^5$</td>
<td>-0.75</td>
<td>0.36</td>
</tr>
</tbody>
</table>

As expected, comparing the lift-off processed devices, the one produced with the 3 mask process exhibits enhanced properties, because the surface of TSiO is not subjected to any lithographic processes prior depositing the GIZO layer, hence the TSiO/GIZO interface is free from residuals that can degrade interface quality. Concerning the devices fabricated using 4 mask processes, the ones where RIE was used to etch TSiO reveal better performance, probably due to the more clean and less
damaging process that RIE constitutes when compared with the lift-off using the ultrasonic cleaner. Also, the maximum $I_g$ values reinforce this idea, being almost one order of magnitude higher for the TFTs exposed to more lift-off processes (4 mask, lift-off).

Note that the RIE process used in this work is far from being optimized for the specific case of TSiO etching. In fact, it is a protocol already established in our laboratory for silicon technology, where the process time was adapted for TSiO etching. Even so, the present RIE process is already capable of working as a viable solution for Ta$_2$O$_5$, SiO$_2$ and TSiO etching.

6.5 – Characterization of optimized active matrix backplanes

6.5.1 – Materials and processes used for the production of the final backplanes

Based on the optimization processes described in chapters 4 and 5 and on the points previously discussed in the present chapter, two different kinds of backplanes were produced, transparent and non-transparent, being the only difference the material used for the electrodes. Table 6.6 summarizes the materials, deposition techniques and patterning/etching processes used for each layer.

Table 6.6 – Materials, processing and pattern definition techniques used for the fabrication of each layer of non-transparent and transparent active matrix backplanes.

<table>
<thead>
<tr>
<th></th>
<th>Non-Transparent</th>
<th>Transparent</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gate</strong></td>
<td>Ti/Au/Ti by e-beam, lift-off</td>
<td>IZO by sputtering, lift-off</td>
</tr>
<tr>
<td><strong>Dielectric</strong></td>
<td>Ta$_2$O$_5$:SiO$_2$ (TSiO) by co-sputtering, RIE</td>
<td></td>
</tr>
<tr>
<td><strong>Semiconductor</strong></td>
<td>GIZO 1:2:2 by sputtering, lift-off</td>
<td></td>
</tr>
<tr>
<td><strong>Source-Drain</strong></td>
<td>Ti/Au/Ti by e-beam, lift-off</td>
<td>IZO by sputtering, lift-off</td>
</tr>
<tr>
<td><strong>Passivation</strong></td>
<td>SU-8 by spin-coating</td>
<td></td>
</tr>
</tbody>
</table>

To assure good properties and enhanced uniformity, two annealing steps were performed, before and after the SU-8 spin-coating. These were made in a hot-plate at 200 °C during 1h30m each, using a heating ramp of 7.5 °C min$^{-1}$. Photographs of the final backplane structures and micrographs obtained by optical microscopy of the pixel architecture are shown in fig. 6.12 for both kinds of backplanes.
Figure 6.12 – Final (a and c) non-transparent and (b and d) transparent backplanes. (a) and (b) show photographs of the structures, while (c) and (d) show optical micrographs of the pixel area.

At the final stage of this work, a new dielectric structure started to be used in backplanes, showing considerable improvements specially regarding leakage current, which for the same thickness of TSiO can be around two orders of magnitude lower. This new dielectric structure comprises also a multicomponent oxide, hafnium-silicon oxide (HSO, ≈240 nm thick), capped by two thin (≈30 nm) SiO₂ layers. The good insulating properties of this structure arise essentially from two factors:

- Due to the multilayer structure and even if the sputtered SiO₂ produced in this work is not the ideal dielectric regarding TFT electrical performance (see chapter 5, section 5.2.2), the discontinuities created in the interfaces between SiO₂ and the bulk dielectric (HSO) inhibit electrons to flow between the gate electrode and the semiconductor, reducing remarkably the leakage current;
- Also, HSO has a higher bandgap than TSiO (around 5.7 against 4.3 eV), allowing for a more favorable conduction band offset with GIZO, which helps to increase the breakdown voltage and suppress leakage current. The band offset should be even more favorable since a thin layer of SiO₂ (which has an even larger bandgap) is introduced before the GIZO film. [5, 9, 10]

The RIE process used for TSiO was not effective for this new multilayer, but a working recipe was found by using CF₄ and slightly higher Pᵣ in the RIE system: even with the higher Pᵣ, the photoresist still worked as an effective mask, since its etching rate with CF₄ is considerably lower than with SF₆.
The electrical properties obtained on TFTs using this dielectric multilayer structure will be presented in the next section.

6.5.2 – Characterization of backplanes: thickness uniformity and active matrix test structures (TFTs)

Table 6.7 shows the thicknesses measured in the profilometer structures embedded in the substrate of a transparent backplane. The data is complemented by the measurement of the thicknesses of the layers composing a TFT located in the center of the active matrix (denoted “center” in table 6.7). It can be seen that good thickness uniformity is obtained, with similar results being achieved for the non-transparent backplanes.

<table>
<thead>
<tr>
<th>Position</th>
<th>Gate (nm)</th>
<th>Dielectric (nm)</th>
<th>Semiconductor (nm)</th>
<th>Source-Drain (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Left</td>
<td>268.0</td>
<td>286.7</td>
<td>19.7</td>
<td>255.7</td>
</tr>
<tr>
<td>Top Right</td>
<td>254.8</td>
<td>266.0</td>
<td>20.2</td>
<td>254.4</td>
</tr>
<tr>
<td>Bottom Left</td>
<td>250.4</td>
<td>260.5</td>
<td>19.5</td>
<td>241.9</td>
</tr>
<tr>
<td>Bottom Right</td>
<td>267.0</td>
<td>266.2</td>
<td>20.4</td>
<td>247.2</td>
</tr>
<tr>
<td>Center</td>
<td>269.0</td>
<td>275.4</td>
<td>21.1</td>
<td>258.5</td>
</tr>
<tr>
<td>X, SD</td>
<td>261.8 ; 8.6</td>
<td>271.0 ; 10.3</td>
<td>20.2 ; 0.6</td>
<td>251.5 ; 6.8</td>
</tr>
</tbody>
</table>

Concerning the electrical properties of the TFTs located in the periphery of the active matrices, they were not significantly affected by the different electrode materials, in agreement to what was verified in the isolated devices produced in 2.5×2.5 cm substrates discussed is chapter 5. The only negative effect observed when using IZO electrodes was the difficulty in obtaining a relatively noise-free measurement, which could only be achieved after some successive measurements and/or by forcing the probe tips deeper inside the IZO layer (fig. 6.13). This should be related not only with the increased ρ of the material potentiated by the two annealing steps it was subjected (prior and after SU-8 processing), which reduces its efficiency as an highly conducting electrode, but also with the formation of a contamination surface layer on top of the air-exposed IZO film, which needs to be surpassed before good tip/electrode contact is obtained. Similar effects on air-exposed ITO and IZO films were already reported by other authors and are consistently observed in our laboratory. To inhibit the formation of this layer at IZO interfaces, a plasma or RCA cleaning process is generally used right before depositing subsequent films on top of IZO. [1, 11]
Even with this drawback, the electrical properties are quite remarkable and similar to the ones obtained in the isolated TFTs fabricated on 2.5×2.5 cm substrates, using the same processing steps: close to 0 V_{on}, On-Off ratio between 10^6 and 10^7, S=0.25-0.30 V dec^{-1} and \mu_{SE} in the range of 15-25 cm^2 V^{-1} s^{-1} are generally achieved both for transparent and non-transparent backplanes.

Although good performance backplanes were fabricated using TSiO as the dielectric layer, the process yield\(^a\) was frequently lower than 75 %, and even the working-devices presented significant discrepancies on their I_D values in the same substrate, from \approx 10 pA to \approx 1 nA. This is mainly attributed to the relatively low bandgap of TSiO, compromising the successful integration of those backplanes in a display prototype. The process yield was in some cases very close to 100 % (for instance, by growing thicker dielectric layers, around 400 nm thick), but TSiO could still lead to unfruitful integration tests due to failures in insulating the row/columns intersections. For this last issue, one possible solution would be to use a larger bandgap material such as SiO_2 for the electrical insulation of the row/columns intersections, while maintaining the TSiO as the dielectric of the TFTs. However, this would result inevitably in more lithographic and deposition steps. At this stage of development, the best solution found to increase the yield and maintain the same number of process steps was to use the SiO_2/HSO/SiO_2 dielectric stack. Figure 6.14 shows the transfer characteristics obtained for transparent TFTs located in different regions of the backplane, with the same W/L ratio. The small variations observed, mainly regarding the maximum I_D, are essentially attributed to possible \rho variation or surface contamination of the IZO electrode layers in the different regions of the substrate. Similar results were obtained for the other W/L ratios, and for the backplanes employing this multilayer dielectric process yields very close to 100 % were consistently achieved, with I_D being always lower than 10 pA. The lower I_D obtained on these devices results in higher On-Off ratios that

\(^a\) Process yield values are based on the measurements performed on the 16 TFTs located at the periphery of the active area.
can exceed $10^8$. However, the higher $S$ values obtained for these TFTs (around 0.4-0.5 V dec$^{-1}$) suggest that their dielectric/semiconductor interface could have worse properties than the one presented for devices using TSiO. This is reinforced by the lower $\mu_{FE}$ for SiO$_2$/HSO/SiO$_2$ transistors, around 10 cm$^2$ V$^{-1}$ s$^{-1}$. Still, given the higher yield and less dissimilarity between devices in the same substrate, these TFTs seem to be good candidates to be used as switching devices in active matrix backplanes.

Figure 6.14 – Transfer characteristics of different TFTs located in the periphery of the backplane’s active area, with IZO electrodes and SiO$_2$/HSO/SiO$_2$ dielectric.

6.6 – Integration with liquid crystal display frontplane technology

The transmissive-LCD frontplane technology is not the ideal to fabricate a fully transparent display, since it requires several non-transparent components, such as a backlight and polarizers. [12] In this work, a simple reflective LCD frontplane is used, which does not require any of those components. Although frontplane technologies such as OLEDs will probably be the most appropriate for the high-performance “transparent displays” to appear in the near future (see chapter 7), a reflective LCD frontplane was chosen at this initial stage due to its simplicity and due to the established know-how of Hewlett-Packard on this technology. The liquid crystal used for integration has negative dielectric anisotropy so it rotates perpendicularly to the applied field direction. Figure 6.15 shows a single pixel switching obtained with a non-transparent backplane, using TSiO as the dielectric layer, proving the effectiveness of these TFTs as switching devices. When the TFT is in the Off-state, the liquid crystal is homeotropically aligned, resulting in low optical absorption (fig. 6.15a). When the TFT is switched-on, the liquid crystal molecules are tilted planar and form a twisted structure, resulting in high optical absorption (fig. 6.15b). Alternating between these two states provides a clear-to-black switch.
Figure 6.15 – Optical micrograph of a non-transparent backplane integrated with a LCD frontplane, showing the (a) Off-state (bright) and (b) On-state (dark) of a single pixel.

Besides the already described reliability problems related with the usage of TSiO in large area and interconnected devices, the biggest issue to achieve successful integration with the LCD frontplane was particle contamination on SU-8 layer. These particles had heights as high as 30 µm, which are incompatible with the 5-10 µm cell gaps used for frontplane integration. Higher cell gaps would require more liquid crystal, reducing the electro-optic effect on the pixel. To circumvent this problem, when the particle contamination was not extremely severe, a chemical-mechanical polish of the SU-8 surface was performed prior to the frontplane integration. An example of a successful integration using a non-transparent backplane is shown in fig. 6.16, on a 32x32 pixel area. Although a bright line and some bright spots are present, due to shorted gates, a good contrast ratio between On and Off pixels is achieved, revealing that the performance of the TFTs is adequate for display application. The integration tests with the fabricated transparent backplanes, using either TSiO or SiO₂/HSO/SiO₂ dielectric stacks are currently underway.

Figure 6.16 – Optical micrograph of a non-transparent backplane integrated with a LCD frontplane, showing an image in a 32×32 pixel area.
6.7 – Conclusions

The main conclusion taken from this chapter is that TFTs based on multicomponent amorphous oxide semiconductors and dielectrics can be successfully used as switching elements on displays, even if produced at temperatures not exceeding 200 °C. When compared with a-Si:H TFT technology, even if a clear advantage in terms of performance is not visible for the low resolution and LCD frontplane of these prototypes, the fact that considerably lower processing temperatures are used here constitutes a major benefit of oxide TFTs backplanes. Moreover, the feasibility of a fully transparent active matrix backplane proves that fully transparent displays will be possible in the near future.

To accomplish successful integration of the backplanes, several processing challenges were found and discussed in this chapter. The most critical ones were substrate cleaning during the various processing steps, layers’ uniformity (in terms of thickness and electrical properties), specially for the dielectric and oxide semiconductor, and patterning/etching processes. Since severe reliability problems were verified when using lift-off for the definition of the dielectric pattern, a RIE recipe from silicon technology had to be adapted for the etching of this layer. A RIE process for TSiO was achieved and TFTs produced with exactly the same process flow but using RIE instead of lift-off for the TSiO layer revealed improved electrical properties and higher yield. However, given the low bandgap of TSiO, some reliability issues remained in the backplanes, such as short-circuits in the row/columns intersections. This was considerably enhanced by using a multilayer dielectric structure, composed by SiO₂/HSO/SiO₂, which was also possible to etch selectively using RIE and allowed to obtain yields on the TFTs distributed by the periphery of the active matrix very close to 100 %.

The results presented in this chapter can be seen as an initial proof of concept of the oxide TFT technology for display applications and also as a first step towards the transition from laboratorial to industrial implementation of the technology, where aspects related with cleaning, uniformity, reliability and fine optimization have to be addressed.

6.8 – References

Transparent oxide TFTs: production, characterization and integration

Chapter 7

Final conclusions and future perspectives

The research work presented in this dissertation was divided into three main areas: study and optimization of sputtered oxide semiconductors and high-κ dielectrics, mostly focusing on materials with amorphous structures, effect of the different compositions, processing and post-processing conditions of those materials on the performance of TFTs and finally, implementation of optimized processes to fabricate active matrix backplanes to be integrated in a prototype with LCD frontplane technology. In this chapter are presented general conclusions about these topics, as well as some future perspectives for further development of this research area, based on the results of this dissertation and on recent reports in literature.

7.1. Final conclusions

The main conclusion to take from this work is that \textit{n-type amorphous multicomponent oxide semiconductors} and \textit{amorphous multicomponent high-κ dielectrics} can be used to fabricate transparent and high performance TFTs at temperatures that do not exceed 150 °C. This is achieved by using the same deposition technique – sputtering – to deposit all the composing materials: conductors, semiconductors and dielectrics. The viability to integrate these devices as electronic switches is shown by using them to fabricate the backplane of a 128x128 pixels LCD display.

Several trends and relations were systematically found for different combinations of compositions, processing and post-processing conditions of the different layers needed to fabricate the TFTs. Although all these variables are related and are naturally studied only within a limited range, some optimal values can be established for them, aiming the pursuit of high performance and stable transparent TFTs. This information is summarized in table 7.1, together with the most relevant trends and findings obtained for each variable. Since this constitutes an important base not only regarding fundamental knowledge but also to define optimized processes when transporting these materials and devices into real-world applications, the following pages present a more detailed overview of the most significant results obtained during this work, based on the information provided in table 7.1.
Table 7.1 – Summary of the most important findings arising from this research work, including optimal values for each studied variable and layer.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Optimal composition or value</th>
<th>Key comments (regarding material and device performance)</th>
</tr>
</thead>
</table>
| Composition | GIZO 2:4:2 | - Most important parameter to define the final properties of films and devices. 
- Multicomponent amorphous preferable to binary polycrystalline (enhanced performance and stability). 
- Indium-richer – higher \( \mu \) but also \( N \), thus highly negative \( V_{on} \). 
- Gallium inhibits excessive free carrier generation. 
- Zinc stabilizes the amorphous structure. |
| \( %O_2 \) | 0.4 – 1.0 % | - Direct control of oxygen vacancies concentration, thus \( N \). 
- Low \( %O_2 \) results in conductive films (highly negative \( V_{on} \)). 
- High \( %O_2 \) leads to resistive films and increases substrate bombardment effects (lower \( \mu_{fg} \), higher \( V_{on} \) and \( \Delta V_{on} \)). |
| Active layer \( p_{dep} \), \( P_{rf} \) | 0.7 Pa, 1.1 W cm\(^{-2} \) | - Associated with the energy of sputtered and plasma species. 
- Higher \( P_{rf} \) and lower \( p_{dep} \) are favorable to obtain compact and very low-\( p \) multicomponent oxide films, but can also lead to severe substrate bombardment effects, specially for ZnO films. |
| \( d_s \) | 20 nm | - Controls the predominance of surface effects and surface depletion regions relatively to bulk properties. 
- For high-\( N \) semiconductors reduced \( d_s \) permits to turn always-on TFTs into usable devices. 
- For low-to-moderate-\( N \) semiconductors, \( d_s \) variation allows for \( V_{on} \) adjustment without compromising the remaining properties. |
| \( T_A \) | 200 °C | - Complex effects, depending on the as-deposited properties. 
- Generally, higher \( T_A \) leads to improved performance and stability, as well as to less dissimilarity among different films. 
- \( \rho \) increases/decreases with \( T_A \) for initially low-\( p \)/high-\( p \) films. 
- \( T_A=500 \) °C leads to the crystallization of indium-richer IZO films, degrading electrical performance. |
| Passivation layer material and deposition process | SU-8 by spin-coating | - Vacuum/physical deposited materials – poor TFT performance 
- Spin-coated SU-8 allows for similar properties to non-passivated devices and improved stability under stress and vacuum measurements. |
| Source-drain electrodes material | IZO 5:1, \( %O_2=0.7 \% \), \( p_{dep}=0.2 \) Pa, \( P_{rf}=1.6 \) W cm\(^{-2} \) | - Transparent IZO and opaque Ti/Au electrodes result in similar performance, provided that \( T_A\leq 200 \) °C is used (or if higher \( T_A \) is needed, it should be performed prior source-drain deposition). |
| Dielectric layer material | TSiO (or SiO\(_2\)/HSiO/SiO\(_2\)) | - Multicomponent dielectrics exhibit improved properties over binary dielectrics (amorphous structure, smoother surface, better compromise between \( E_\parallel \) and \( k \)). 
- TAO s.t. leads to worse stability than TSiO (larger hysteresis, \( \Delta V_{on} \) and non-recoverable \( \Delta S \) under constant current stress). 
- Multilayer structures comprising multicomponent oxides permit a significant reduction of \( I_\parallel \). |
7.1.1. n-type oxide semiconductors

Concerning oxide semiconductor materials, all the work focused on the gallium-indium-zinc oxide system, including the Ga2O3, In2O3 and ZnO binary oxides and most importantly, multicomponent oxides based on mixtures of those binary compounds. Indium richer compositions constitute a good starting point to obtain good semiconductor performance, given that In2O3 allows to obtain much higher $\mu$ than ZnO or Ga2O3. Still, the addition of zinc and/or gallium to the In2O3 matrix is of vital importance: first, they inhibit excessive free carrier generation, resulting in adequate $N$ values to render the materials usable as channel layers on TFTs. This is mainly achieved by gallium incorporation, since this element has a high ionic potential (+3 valence and small ionic radius) when compared with the other cations, allowing it to create strong bonds with oxygen. Second, the incorporation of larger concentrations of zinc and/or gallium inhibit the crystallization of In2O3, with an amorphous structure being preserved for a broad (G)IZO compositional range for $T_a=500 \, ^{\circ}\mathrm{C}$ and even higher. This allows having much smoother surfaces in multicomponent oxide semiconductors than for instance in ZnO, as seen by AFM analysis. The films with amorphous structure still have a conduction band primarily composed by large and overlapping indium cations, like in In2O3, but the carrier transport is no longer limited by the existence of grain boundaries inherent to polycrystalline materials. In fact, carrier transport in GIZO is seen to be limited essentially by the random distribution of zinc and gallium cations around CBM, but the potential barriers arising from this structural perturbation are much smaller than the ones created by grain boundaries and can be easily surpassed by larger $N$. For this reason, these oxide semiconductors present larger $\mu$ as $N$ is increased, at least until $N=10^{20-24} \, \text{cm}^3$, where large $\mu>60 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$ can be achieved (for larger $N$, typical ionized impurity scattering mechanisms decrease $\mu$). The fact that the tail state density is much lower than in a-Si:H allows $E_t$ to easily surpass CBM, explaining why these amorphous oxides have much larger $\mu$ than amorphous covalent materials. For active layer application, and considering the range of deposition conditions explored in this work, GIZO 2:4:2 and 2:4:1 are selected as the most adequate compositions, since they provide amorphous structures and smooth surfaces combined with moderate $N$ (below $10^{16} \, \text{cm}^{-3}$), that allow to obtain $\rho=10^{-1}-10^{-3} \, \Omega \, \text{cm}$. Even if a detailed study is not performed envisaging the optimization of oxides for electrode application (i.e., as TCOs), it can be concluded that indium-richer compositions without gallium, such as IZO 5:1, allow to achieve the best results, corresponding to the higher $N$/lower $\rho$ films.

Besides composition, $\%O_2$, $p_{\text{deo}}$, $P_{\text{rf}}$ and $T_a$ are found to significantly affect the overall properties of the materials. $\%O_2$ directly controls the oxygen vacancy concentration, hence $N$, but large $\%O_2$ (10.0 \%) can also result in indium deficiency of GIZO films and deleterious bombardment effects, which increase the defect density and $\rho$ of the sputtered thin films. For these reasons, low $\%O_2$ between 0.4
and 1.0 % are chosen as ideal to obtain materials with moderate $N (\approx 10^{14} - 10^{17} \text{ cm}^{-3})$ and small trap state densities, to render them usable as active layers in transistors. Both $p_{\text{dep}}$ and $P_{\text{rf}}$ affect the energy of the species arriving at the substrate, and for the range of %O$_2$ defined above, moderate $p_{\text{dep}}$ (0.7 Pa) and low $P_{\text{rf}}$ (1.1 W cm$^{-2}$) are preferable to achieve good control of $N$ and defect density. These %O$_2$, $p_{\text{dep}}$ and $P_{\text{rf}}$ conditions also lead to the most electrically stable thin films, regarding aging tests during 18 months of air exposure. Increased $T_A$ promotes structural rearrangements that in the limit lead to crystallization, but as stated before, this severe structural change does not occur until $T_A$=500 °C for most of the (G)IZO compositions studied herein. Still, annealing treatments help to improve electrical properties, specially for thin films produced using non-ideal deposition conditions, meaning that structural rearrangements and annihilation of defect states might play an important role. The evolution of properties with $T_A$ follows different trends depending on the as-deposited properties of the thin films, with oxygen adsorption or desorption being favored for initially low and high $p$ materials, respectively, until equilibrium between oxygen concentration in the film and in the annealing atmosphere is achieved. As $T_A$ increases, the properties of all the materials converge to the same point, i.e., they start to be essentially dominated by $T_A$ rather than by the deposition conditions. The effects of processing and post-processing conditions on the electrical properties are seen to be much more critical for ZnO than for (G)IZO, i.e., the process window to obtain good performing thin films is considerably broadened when multicomponent oxides are used. Also, both ZnO and In$_2$O$_3$ thin films exhibit considerably worse electrical stability than (G)IZO thin films regarding aging tests during 18 months of air exposure, even if annealed at $T_A$=500 °C, which is ascribed to effects related with grain boundaries. Another advantage of the multicomponent amorphous oxide semiconductors over binary polycrystalline ones is that their electrical properties are relatively insensitive to the thickness of the films, at least in a range between 40 and 230 nm, as opposed to ZnO and In$_2$O$_3$. Still, surface effects associated with depletion regions created due to the surface interaction with atmospheric oxygen should play a fundamental role determining the electrical properties even of amorphous oxides, when their thicknesses are decreased to a few nm, as shown later when the materials were used as channel layers in TFTs.

The optical properties of oxide semiconductors are also briefly analyzed. Burstein-Moss shifts are only observed for $N>10^{18} \text{ cm}^{-3}$, since only above this $N$ range $E_F$ can surpass CBM. For thin films having lower $N$, larger %O$_2$ is seen to slightly increase $E_{\text{opt}}$, but the most significant $E_{\text{opt}}$ variations are found for different compositions of the multicomponent oxides. The $E_{\text{opt}}$ values in these materials reflect the different concentrations of the composing binary oxides, being larger $E_{\text{opt}}$ obtained for gallium-richer GIZO compositions, since Ga$_2$O$_3$ presents the largest $E_{\text{opt}}$ (>4 eV) among all the binary oxides studied here. All the oxide semiconductors present $E_{\text{opt}}>3$ eV and AVT around 80 % or even higher, turning them suitable for transparent electronics applications.
7.1.2. High-κ dielectrics

A multicomponent approach is also followed for the production of dielectric thin films. The strategy is to have a high-κ material, such as HfO₂ or Ta₂O₅, and mix it with a high-\( E_g \) material, such as SiO₂ or Al₂O₃, either using co-sputtering or targets with specific multicomponent compositions. This permits to obtain more disordered structures than in the high-κ binary compounds, as confirmed by spectroscopic ellipsometry for TSiO and TAO relatively to Ta₂O₅. For HfO₂ the structural change is even more evident, since the multicomponent dielectrics result in amorphous structures while HfO₂ is polycrystalline even when deposited at room temperature. The multicomponent approach also allows to increase the \( E_g \) of high-κ dielectrics, preserving relatively high \( \kappa \) values. Furthermore, this approach is highly flexible, since the best compromise between \( E_g \) and \( \kappa \) for a specific application can be achieved simply by changing the relative concentrations of the composing elements. For the more widely explored dielectric system in this work, tantalum-silicon oxide, considerably lower current density is obtained for TSiO when compared with Ta₂O₅ (around \( 10^{-9} \cdot 10^{-8} \) against \( 10^{-7} \cdot 10^{-6} \) A cm⁻²) while preserving a high \( \kappa \) (17.3), revealing the effectiveness of the multicomponent approach to fabricate good performance dielectrics without intentional substrate heating.

7.1.3. n-type oxide semiconductor-based thin-film transistors

All the trends described above are also verified when moving from isolated thin films to TFT structures. Regarding the oxide semiconductor, best properties are achieved for \%O₂=0.4-1.0 \%, \( p_{\text{dep}}\approx0.7 \) Pa and \( P_{\text{c}}\approx1.1 \) W cm⁻². Using these deposition conditions, multicomponent oxide compositions based on In₂O₃ but having enough zinc and/or gallium content (in order to suppress high \( N \) and assure that an amorphous structure is obtained) exhibit considerably improved performance over ZnO TFTs, where carrier transport is inhibited by depletion layers at grain boundaries. When the processing conditions deviate from this, several non-ideal effects such as large \( V_{\text{on}} \) and \( \Delta V_{\text{on}} \) (due to very high \%O₂ or gallium content) or highly conductive channel layers and consequently always-on devices (due to low \( p_{\text{dep}} \) or high indium content) are obtained. Still, high-\( N \) oxide semiconductors (\( \approx10^{19} \) cm⁻³) can yield good performing transistors, with close to 0 \( V_{\text{on}} \), provided that \( d_i \) is reduced to very small values (\( \approx10 \) nm). For lower \( N \) semiconductors that even with high \( d_i \) can be fully depleted by \( V_{\text{bi}} \), \( d_i \) variation is an effective way to control \( V_{\text{on}} \) without significantly affecting other electrical properties. Regarding the effect of \( T_A \), as stated before, it depends on the as-deposited properties of the oxide semiconductor materials. The largest improvements as \( T_A \) increases are verified for initially low \( N \)/high defect density and high-\( N \) materials: the former tend to present higher \( \mu_{\text{FE}} \), lower \( V_{\text{on}} \) and \( \Delta V_{\text{on}} \) as \( T_A \) increases, while the evolution in the latter is essentially
verified in the $V_{on}$ values, which tend to approach 0 V. Annealing treatments are also found to be relevant to decrease differences arising from uncontrolled process variations in supposedly similar devices. In addition, as verified for the isolated thin films, as $T_A$ increases above 300 °C the deposition conditions have a less predominant role defining the properties of the devices, which start to be mostly dictated by $T_A$. When considering the optimized oxide semiconductor processes mentioned above, it is possible to achieve remarkable electrical properties in GIZO TFTs, such as $\mu_{fe}=50$ cm$^2$ V$^{-1}$ s$^{-1}$, $V_{on}=-1$ to 0 V, negligible $\Delta V_{on}$ and hysteresis, $S=0.25$ V dec$^{-1}$ and On-Off ratio exceeding $10^6$, all with a low $T_A$ of 150 °C. These properties clearly surpass the typical performance achieved with a-Si:H TFTs.

Similar performance can be achieved by using Ti/Au or IZO source-drain electrodes, provided that low $T_A$ (150-200 °C) is used. For these conditions, with optimized GIZO TFTs, width-normalized series resistance below 50 Ω cm is achieved for both electrode materials. This value is increased both by using non-optimized oxide semiconductor processing conditions and by using higher $T_A$ (300 °C or above). For this last case, IZO contact properties are considerably degraded because the bulk electrode ρ significantly increases due to oxidation. Regarding the effect of passivation layers, all the tested materials and processes except spin-coated SU-8 lead to always-on devices, due to the modification of the semiconductor back surface during the deposition of the passivation layer. If a subsequent annealing treatment is performed in SU-8 passivated TFTs, similar electrical properties to the ones achieved in non-passivated TFTs are obtained.

Measurements under constant $I_D$ stress in devices using Si/SiO$_2$ substrates reveal that improved stability is achieved for low %O$_2$ (0.4-1.0 %), GIZO 2:4:2 and 2:4:1 compositions, $T_A=200$ °C and SU-8 passivated devices. Under these conditions, after 24 h stress at $I_D=10$ μA, $\Delta V_I=0.46$ V and negligible $\Delta S$ are obtained, which is quite promising regarding the integration of these devices in demanding circuits, such as current drivers in OLED active matrices. In addition, even when considering non-passivated devices, no aging effects are observed after 18 months of device processing, provided that optimized deposition conditions and a composition yielding a moderate $N$ (such as GIZO 2:4:2) are used for the production of the active layer. For non-ideal oxide semiconductors, which have initially high or low $V_{on}$, the main trend with time is for $V_{on}$ to approach 0 V.

To obtain fully transparent TFTs produced at low temperatures, devices employing sputtered dielectrics were also fabricated. Good electrical properties, in some cases comparable with devices on Si/SiO$_2$ substrates could be achieved. This is mostly verified for TFTs with multicomponent amorphous dielectrics based on Ta$_2$O$_x$, such as TSiO or TAO s.t., which exhibit $\mu_{fe}=30-35$ cm$^2$ V$^{-1}$ s$^{-1}$, $V_{on}=-1$ to 1 V, $S<0.25$ V dec$^{-1}$ and On-Off ratios between $10^6$ and $10^7$. However, the TAO system results in devices with larger $\Delta V_{on}$ and hysteresis than TSiO, which is also reflected in the poor
stability of TAO TFTs when subjected to stress tests, such as a constant $I_D$ stress or $V_G$ signals consisting of square waves with different frequencies.

### 7.1.4. Active matrix backplanes and integration with liquid crystal display frontplane

The optimized processes for the production of TFTs were then transposed to larger areas, for the fabrication of active matrix backplanes with an active area of 2.8”, a resolution of 128x128 pixels and a single TFT per pixel. Both non-transparent and fully-transparent backplanes were fabricated, using Ti/Au and IZO electrodes, respectively. When moving to larger areas and interconnected devices (rather than the isolated ones in the TFT test structures studied before) several processing challenges had to be surpassed, because initial backplanes presented very small yields. The main optimizations had to be made regarding layers’ uniformity (in terms of thickness and electrical properties) for the dielectric and oxide semiconductor and patterning/etching processes. The most striking difference relatively to isolated devices is the usage of RIE to etch the dielectric layer rather than lift-off, since significant reliability problems were arising due to this process step. At the end of the research work of this dissertation, a multilayer and multicomponent dielectric structure comprising SiO$_2$/HSO/SiO$_2$ (also etched by RIE) started to be used, turning possible to obtain yields very close to 100 % in the test structures distributed around the backplane active area. The backplanes were then successfully integrated in a prototype using a LCD frontplane technology, demonstrating that multicomponent amorphous oxides, both semiconductors and dielectrics, are a viable technology to fabricate TFTs with high performance and processing temperatures below 200 °C. In addition, the fact that these devices can be fully transparent permits not only to conceive but also to fabricate new and exciting products, integrated in the recent and fascinating concept of transparent and flexible electronics.

### 7.2. Future perspectives

As with any kind of research work, a large number of questions and paths remain unanswered and unexplored after this dissertation. Based on the results presented here and in recent literature regarding transparent electronics, some recommendations for future work are given in this section:

- **Characterization of oxide semiconductors**: although binary oxides such as ZnO and In$_2$O$_3$ have been studied for a long time, multicomponent oxides are only now starting to be widely explored. Important characteristics such as the nature of defects and a complete mapping of their energy levels, or the exact dynamics and phenomena involved on the evolution of their properties during time or with increasing $T_A$ should be addressed. Besides the large range of
electrical characterization techniques available to study this, it is proposed that constant
photocurrent method (CPM) and spectroscopic ellipsometry (SE) can be explored as important
tools to study subgap states on these materials;

- **n-type oxide semiconductors**: as seen in this work, a large modulation of properties can be
  achieved in multicomponent oxides simply by changing the relative concentrations of the
  composing cations. Even if currently indium-based materials are the most widely studied
  multicomponent oxides, improvements on tin or zinc-based materials should also be persuaded
  envisaging the application of these materials as high-performance semiconductors at low
  temperatures. Due to the scarcity and high demand of indium, this would result in lower costs;

- **p-type oxide semiconductors**: even if a large number of reports exist in the literature about p-
  type ZnO, good performance, stability and low temperature processing remain critical issues for
  this material. On the other hand, materials such as SrCu2O2, AlCuO2, Cu2O [3] or SnO [4]
  present stable p-type characteristics, but high temperature processing and poor electrical
  performance are generally observed when compared with n-type oxide semiconductors.

Nevertheless, recent developments in our laboratory already allowed integrating p-type SnO and
Cu2O in TFTs with μeff=1-4 cmV⁻¹s⁻¹ and On-Off ratio=10⁴, with (post-)processing temperatures
not exceeding 200 °C. The continuous research on p-type oxides is of vital importance in order to
fabricate transparent CMOS circuits;

- **Improvement of sputtered dielectrics**: the multicomponent approach explored in this work
  should be studied in more detail, possibly with other material systems. Note that deposition
  conditions are far from being optimized and extensive work is needed in this area. Furthermore,
  the integration of the multicomponent dielectrics in multilayer structures, as shown in the last
  stage of this dissertation work, seems to be a viable option to achieve both high-κ and low 1p0,
  with the added advantage that different materials, either with good interface or bulk properties,
  can be used simultaneously;

- **Other techniques for material deposition**: sputtering was used to effectively produce transparent
  conductors, semiconductors and insulators without intentional substrate heating. However, this
does not invalidate that other techniques are explored for the production of these materials. Ink-
jet assumes particular relevance as a powerful and low cost technique for the future of
transparent electronics, as it provides a method to easily print materials with predefined
patterns, provided that ink chemistry is continuously improved in order to have stable and good
performing base materials to work with. Other simple and non-vacuum techniques, such as spin-
coating, should also be explored, as they provide a low cost and fast method for thin film
fabrication. In fact, spin-coating can be particularly useful for the fabrication of low temperature
organic dielectrics, also compatible with transparent electronics, as shown in recent works; [5]
Final conclusions and future perspectives

- **Improvement of passivation layers**: although SU-8 already provides a good protection for subsequent integration of oxide semiconductor-based TFTs while maintaining the electrical properties of non-passivated devices, lower cost, easier/faster-to-process materials should also be explored;

- **Device characterization**: stability measurements should be continued, extended to larger time scales and performed under different environmental conditions, changing temperature, humidity and pressure. In order to investigate in detail the physical mechanisms responsible for non-idealities and instability, this should be complemented by thermally stimulated current techniques. Photoconductivity measurements on these TFTs should also be investigated.

Even if the physics behind multicomponent oxide semiconductors is far from being totally explored, given the remarkable properties of these materials when integrated in TFTs several applications start already to appear and will certainly gain more relevance in the near future:

- **OLED displays**: OLEDs will probably be the dominant frontplane technology in displays’ market in some years from now. The demanding performance and stability requirements of OLEDs seem to be a good opportunity to show the viability of oxide semiconductor-based TFTs technology. In fact, this OLED/oxide TFT combination is already gaining strength, as evidenced by the prototypes recently unveiled by consumer electronics giants as Samsung and LG;

- **Transparent displays**: this is probably the most fascinating and immediate demonstration of the concept of “transparent electronics”. Surprisingly, and demonstrating the enormous interest on this application even if the oxide semiconductor-based TFTs are still very recent, both Samsung and LG already presented during 2009 prototypes of transparent displays, based on OLED technology (fig. 7.1). This will certainly be one of the largest applications for these TFTs, turning possible to discover completely new ways of interacting with visual information, which until now were typical of science fiction movies;

*Figure 7.1 – Transparent display prototypes using oxide semiconductor-based TFTs and OLEDs: (a) Samsung, 4.3”, presented at CES2009; (b) LG, 15”, presented at FPD2009.*
- **Ultra-low cost, recyclable and flexible electronics:** given the low processing temperatures possible to achieve with oxide semiconductors, migration of these materials to flexible substrates is naturally foreseen. In fact, some reports recently appeared regarding oxide semiconductor-based TFTs on plastic substrates. [6-8] But flexibility can be taken one step further, by using cellulose paper, not only as a substrate but also as the dielectric layer of transistors. This was recently demonstrated by our laboratory, by fabricating transistors and simple memories on paper (fig. 7.2), [9, 10] and is believed to be an important area to further explore in the future;

![Figure 7.2](image)

*Figure 7.2 – Application of oxide semiconductors to fabricate transistors and memories on paper, being the paper used as the substrate and the dielectric layer: (a) photograph of paper transistors; (b) transfer characteristics of paper transistors employing two different types of paper.*

- **Other applications:** countless examples of new applications will certainly arise for oxide semiconductors in the near future. For instance, a large interest exists in using them for memory applications [11, 12] and concepts of transparent memory circuits already circulate in the internet. [13] Other examples could be the production of bio-sensors from oxide semiconductor-based TFTs, which is being explored now at our laboratory for pH, DNA and enzyme detection. The subsequent integration of all these sensing possibilities in arrays of different TFTs contained in a single substrate potentiates the concept of a versatile lab-on-chip with low production costs.

The migration of new technologies from laboratorial prototypes to industrial products is never straightforward or fast and depends on multiple factors, such as market demands and associated costs. Even if a huge industry is nowadays established around the fabrication of a-Si:H TFTs, the advantages brought by oxide semiconductor-based TFTs will certainly allow for a facilitated penetration of this new technology in the market. First, because the range of applications is by far larger than the one achieved with a-Si:H TFTs, due to the high performance, low processing temperatures and transparency turned possible with oxide TFTs. Second, because the processes and tools involved in their fabrication are similar and even simpler than the ones already implemented to
fabricate a-Si:H TFTs and displays. Third, because multicomponent oxide semiconductors can easily be produced in large areas without the typical reproducibility and uniformity problems of polycrystalline materials such as poly-Si, since they are amorphous. Hence, a very promising future is foreseen for this amazing and transparent technology.

7.3. References