UNIVERSIDADE NOVA DE LISBOA
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A MOSFET-Only Wideband LNA Exploiting Thermal Noise Canceling and Gain Optimization

por

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"Engineers have no life and can prove it mathematically!"

Unknown

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Abstract

Faculdade de Ciências e Tecnologia
Departamento de Engenharia Electrotécnica e de Computadores

Mestre em Engenharia Electrotécnica e de Computadores

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In this thesis a MOSFET-only implementation of a balun LNA is presended. This LNA is based on the combination of a common-gate and a common-source stage with canceling of the noise of the common-gate stage. In this circuit, resistors are replaced by transistors, to reduce area and cost, and minimize the effect of process and supply variations and mismatches. In addition we obtain a higher gain for the same voltage drop. Thus, the LNA gain is optimized, and the noise figure(NF) is reduced. We derive equations for the gain, input matching, and NF. The performance of this new topology is compared with that of a conventional LNA with resistors. Simulation results with a 130 nm CMOS technology show that we obtain a balun LNA with a peak 20.2 dB gain (about 2 dB improvement), and a spot NF lower than 2.4 dB. The total power consumption is only 4.8 mW for a bandwidth wide than 5 GHz.

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Abbreviations

AC	**A**lternating **C**urrent
BER	**B**it **E**rror **R**ate
BiCMOS	**B**ipolar **C**omplementary **M**etal-**O**xide **S**emiconductor
CG	**C**ommon **G**ate
CMOS	**C**omplementary **M**etal-**O**xide **S**emiconductor
CS	**C**ommon **S**ource
DC	**D**irect **C**urrent
GaAs	**Ga**llium **As**senide
GSM	**G**lobal **S**ystem **M**obile
IC	**I**ntegrated **C**ircuits
KCL	**K**irchhoff's **C**urrent **L**aw
KVL	**K**irchhoff's **V**oltage **L**aw
LNA	**L**ow **N**oise **A**mplifier
LO	**L**ocal **O**scillator
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
NEF	**N**oise **E**xcess **F**actor
PCB	**P**rinted **C**ircuit **B**oard
QPSK	**Q**uadrature **P**hase-**S**hift **K**eying
RF	**R**adio **F**requency
SiGe HBT	**Si**licon-**Ge**rmanium **H**eterojunction **B**ipolar **T**ransistor
SoC	**S**ystem **o**n **C**hip
UMTS	**U**niversal **M**obile **T**elecommunication **S**ystem
VCCS	**V**oltage **C**ontrolled **C**urrent **S**ource

Chapter 1

Introduction

1.1 Background and Motivation

Nowadays, a rapid growth of mobile communication systems has increased the use of wireless devices in applications in the license free ISM (industrial, scientific and medical) bands . The need to build devices that at the same time reduce cost and power consumption is the main challenge in the IC (integrated circuits) design.

The CMOS technology, given its current position in market and technological evolution, allows the development of low cost integrated circuits, with high performance and low supply voltage (allowing low power consumption). Thus, there is a strong motivation to implement circuits in this technology [1].

Until very recently, high and low frequency ICs were treated separately. The high frequency ICs could only be realized with large areas in more expensive technologies than CMOS, like GaAs, SiGe HBT, Bipolar, and BiCMOS [2]. This limitation gives rise to problems in circuit design, namely, the need to match the inputs and outputs of the various circuits in order to maximize the power transfer between them. The electrical connection between them through wires on printed circuit board (PCB), which at high frequencies, have undesired capacitive and inductive parasitics. In order to minimize these effects and avoid off chip connections, we should design all the system circuits in the same die (SoC - System on Chip). This is possible in modern CMOS technologies.

LNAs (low noise amplifiers) are key blocks in modern receivers, and they can be divided into two main groups: narrowband and wideband. Narrowband LNAs use inductors and

have very low noise figure, but they occupy a large area and require a technology with RF options to have inductors with high Q. Wideband LNAs with multiple narrowband inputs have low noise, but their design is complicated and the area and cost are high [1, 3]. RC LNAs are very simple and inherently wideband, but conventional topologies have large noise figures. Recently, wideband LNAs with noise and distortion canceling [4] have been proposed, which can have noise figures below 3 dB. Inductorless circuits have reduced die area and cost [5]. However, they are usually realized with MiM capacitors, which require an additional insulator/metal layer, and they use poly or/and diffusion resistors, which have large process (typically 25%) and mismatch variations.

In this work, our main goal is to design a very low area and low-cost LNA, and at the same time obtain less circuit variability, by implementing the resistors using transistors (MOSFET-only design) [6]. As it will be shown, this approach adds a new degree of freedom, which can be used to maximize the LNA gain, and, therefore, minimize the circuit noise figure.

1.2 Thesis Organization

This thesis has been organized in six chapters, including this introduction.

In Chapter 2, an overview of receiver architectures is presented, emphasizing the RF front-end, in which the LNA is included. We briefly describe the existing LNA topologies, making a distinction between inductor and inductorless LNAs. We introduce the basic concepts, definitions, and figures of merit, which are widely employed in LNAs (e.g., impedance matching, noise, and intermodulation products).

Chapter 3 gives an in depth analysis of the common gate (CG) stage used as an LNA. We start with a theoretical analysis, in which we review the equations for input impedance, gain, and noise figure. For each parameter we derive three equations with different degrees of approximation. The theoretical analysis is validated with simulation results in 130 nm CMOS technology. In Chapter 4, with the same structure as Chapter 3, a common source (CS) amplifier is analyzed.

Chapter 5 presents the LNA structure proposed in this thesis, which combines the two amplifier stages. The principle of noise canceling is explained. A theoretical analysis is made combining the results obtained in the previous chapters. Validation is made through

simulation results, and then different approaches will be taken to optimize the proposed circuit. The substitution of the load resistors by transistors is proposed, leading to a MOSFET-only circuit. Comparison with state-of-the-art wideband LNAs is made. The circuit layout is produced, and post-layout simulations are performed.

Chapter 6 gives overall conclusions and further research suggestions.

1.3 Contributions

The main contributions of this thesis are as follows.

We derive equations to describe the basic amplifier stages (CG and CS), with different levels of approximation, for the gain, input impedance, and noise figure. The equations are validated by simulation for the frequency range of interest.

For the complete LNA (combined CG and CS balun topology), we compare the conventional design (with resistors) with the new MOSFET-only implementation optimized for gain and noise figure (NF). Equations for optimization of key parameters, such as gain and NF, are also presented. Simulation results of an example circuit designed in a standard 130 nm CMOS technology validate the proposed methodology.

This work has originated a paper at the Mixed Design of Integrated Circuits Systems International Conference (MIXDES)[7], and an extended version was submitted to the International Journal of Microelectronics and Computer Science.

Chapter 2

Receiver Architectures and RF Blocks

In the following sections an overview is made of receiver architectures and the main RF (radio frequency) front-end blocks.

2.1 Receiver Architectures

A communication system is composed of a transmitter, a receiver, and a communication channel (in which the signal is propagated). In a wireless system, on the transmitter side, the information is included in a radio frequency signal through the variation of, at least, one of its characteristics, amplitude, frequency, or phase, a process that is called modulation. The main function of the receiver is to recover the information contained in the original RF signal through a demodulation process. The communication medium (air, in the case of wireless communications) is far from ideal, and the signal received is usually very weak (of the order of microvolts), which is also susceptible to interferences from other signals (that can be stronger). So, it is necessary to eliminate unwanted signals and detect the information contained in the signal of interest. After selecting the desired signal, by filtering, it must be amplified and converted to baseband to be demodulated, to retrieve the information contained in the signal.

The reason why the signals are converted to high frequency for transmission and then converted back for the baseband for reception is that the signals can carry more information

at high frequencies (higher bandwidth); furthermore, small size antennas are required, (the size is typically proportional to the wavelength of the signal). However, the influence of parasitics is higher at high frequency. In the following, the main receivers architectures that are commonly used today are shortly described [1, 8].

2.1.1 Heterodyne Receiver

The super-heterodyne receiver topology, represented in fig. 2.1, was proposed by Armstrong in 1918 [9] and is one of the most used architectures in wireless communication systems. The RF signal received by the antenna is filtered by a bandpass filter, then it is amplified by a low noise amplifier(LNA) and down-converted to a lower, intermediate frequency (IF), through a signal multiplier(mixer), to which the output of a local oscillator (LO) is applied. At the mixer output there is a bandpass filter at the IF, called the channel selection filter, which isolates the desired signal from signals in adjacent channels. The great advantage of this architecture is that the IF is fixed, the desired RF frequency being selected by tunning the LO; this makes it easier to design the filter, which should be very selective, with a high quality factor (Q). The signal demodulation is usually done in the digital domain and, therefore, it is necessary to include an analog to digital converter (ADC), followed by a digital signal processor to perform the demodulation process.

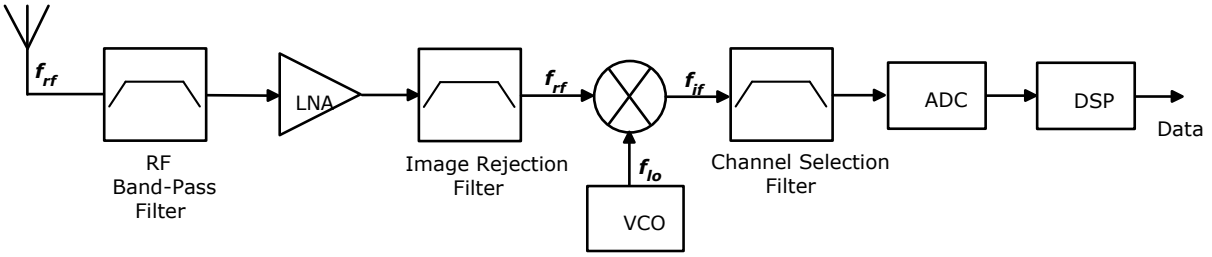


FIGURE 2.1: Super-Heterodyne Receiver.

To better understand the operation principle of this receiver, particularly with regard to mixing, consider that at the mixer inputs there are the RF and LO signals,

$$v_{rf}(t) = V_{rf}cos(\omega_{rf}t) \tag{2.1}$$

$$v_{lo}(t) = V_{lo}cos(\omega_{lo}t) \tag{2.2}$$

At the mixer output, we have

$$v_{if}(t) = v_{rf}(t)v_{lo}(t) = \frac{1}{2}V_{rf}V_{lo}\left[cos((\omega_{rf} - \omega_{lo})t) + cos((\omega_{rf} + \omega_{lo})t)\right] \tag{2.3}$$

From (2.3), the wanted signal is that with the lower frequency,

$$\omega_{if} = \omega_{rf} - \omega_{lo} \tag{2.4}$$

A bandpass filter is used for channel selection, centered on the IF (f_{if}), which eliminates all other unwanted signals that may be present in the spectrum. A major problem can occur if at the mixer input also exists a signal with frequency $f_{im} = 2f_{lo} - f_{rf}$ (fig. 2.2), called image signal. This signal, after the multiplication, originates at the mixer output two signals at frequencies $f_1 = f_{lo} - f_{rf}$ and $f_2 = 3f_{lo} - f_{rf}$: since f_1 coincides with the intermediate frequency, it overlaps the signal of interest, and it is impossible to separate the two signals. A filter is necessary before the mixer to reject the image signal (called image rejection filter).

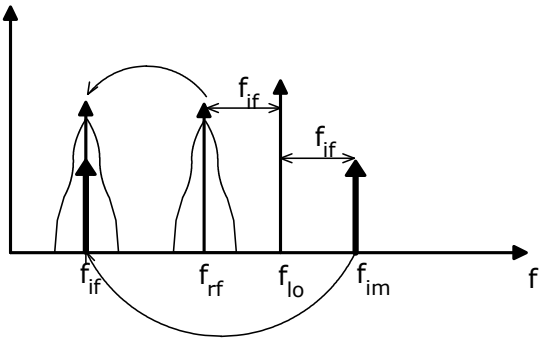


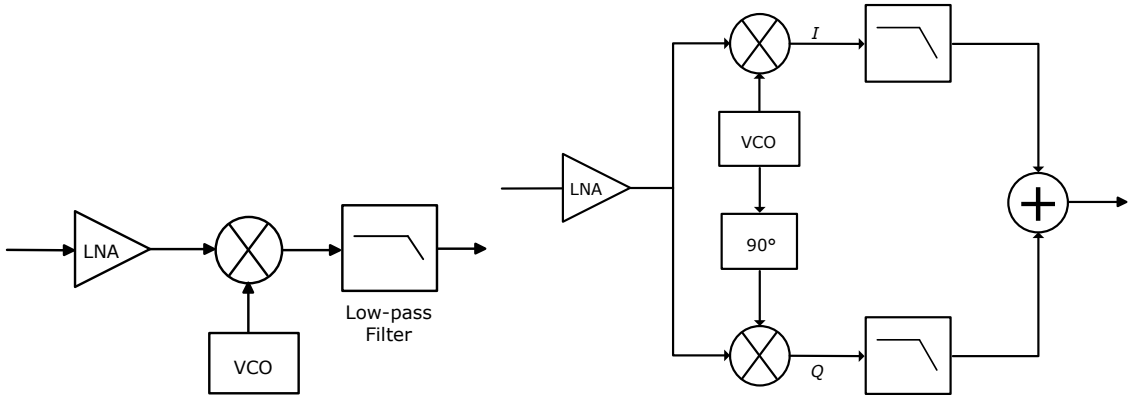
FIGURE 2.2: Frequency spectrum showing the image signal.

The frequency difference between RF and image signals is $2f_{if}$; hence, increasing f_{if} relaxes the image rejection filter specifications. However, as f_{if} increases, the channel selection filter must have tighter specifications for the same bandwidth, because the quality factor $Q = \frac{f_0}{\Delta f}$ increases. Filters with a high Q are difficult to realize with CMOS technology, and so there is a compromise between intermediate frequency and quality factor. In practice, high performance filters must be realized externally, which makes on chip full integration impractical.

2.1.2 Homodyne Receiver

Since the heterodyne receiver is difficult to integrate, another receiver topology is employed, commonly referred to as homodyne, direct conversion, or "Zero-IF". In the direct conversion receiver (fig. 2.3(a)), the RF signal is converted directly to baseband by using an LO with the same frequency as the RF signal. With the signal of interest in baseband, the channel selection filter is a low-pass filter which is simpler to design and integrate. The image rejection filter is no longer required.

In most cases, the received signals are modulated in phase or frequency, and for this type of modulations the information contained in the signal sidebands is different. These modulation schemes differs from amplitude modulation (AM) where the sidebands have the same information. Hence, receivers with quadrature down conversion are used (fig. 2.3(b)) to preserve the information contained in the sidebands.

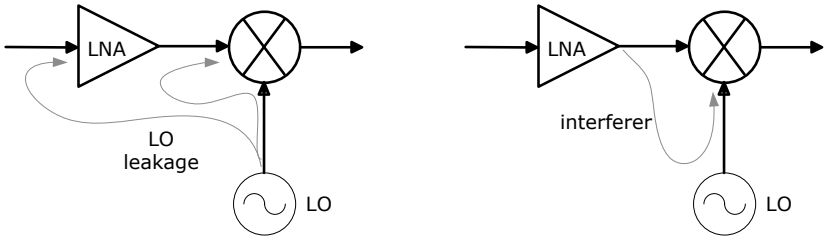


(a) (b)

FIGURE 2.3: Homodyne receiver: (a) single (b) in quadrature.

Despite its simplicity, this architecture presents some drawbacks that prevent it from being applied in some cases.

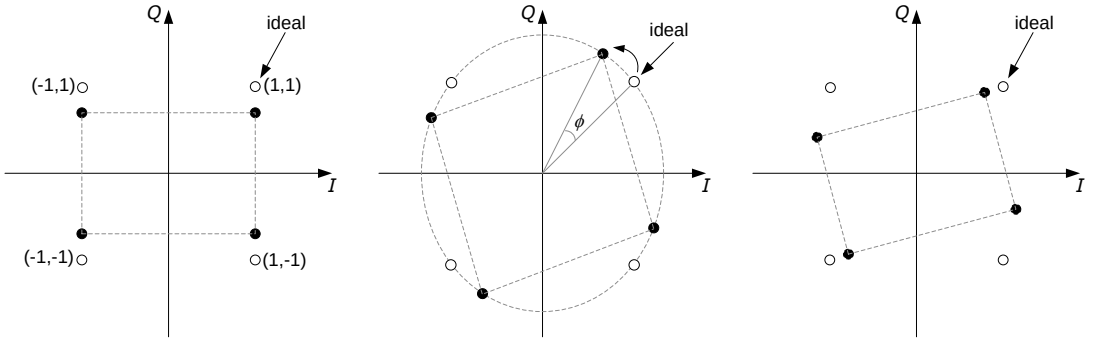
DC offsets One problem is related to leakages between the LO port and the LNA and mixer inputs when the ports are inadequately isolated, due to substrate and capacitive coupling. In fig. 2.4(a), a leakage signal "LO leakage" appears at the inputs of LNA and mixer resulting in a "self-mixing" that origins a DC component at the mixer output, which can lead to saturation of the following blocks. A similar effect occur if there is a leakage from the LNA or mixer input to the LO port of the mixer(fig. 2.4(b)).



(a) (b)

FIGURE 2.4: DC offsets caused by self-mixing (a) "LO leakage" (b) interferer.

I/Q Mismatch As referred previously, with frequency or phase modulation, quadrature signals are required, and ideally they should have the same amplitude and a phase difference of 90°. However, the circuits are not ideal and imbalances between I and Q are expressed as gain and phase errors. The result of "I/Q mismatch" is a corruption of the received signal constellation, and consequently an increase of the bit error rate (BER). As example, fig. 2.5(a) shows the effect of "I/Q Mismatch" on a QPSK(Quadrature Phase-Shift Keying) constellation, when the mixer at th Q path haves less conversion gain than the one at the I path, and therefore, the Q signal has less amplitude than expected, resulting in a gain error.



(a) (b) (c)

FIGURE 2.5: Effect of I/Q mismatch in QPSK: (a) gain error (b) phase error (c) gain and phase error.

Now, assuming that there is no gain error, but there is a phase error ϕ between the signals fed by the LO and the splitter,

$$x_{LO,I}(t) = 2\ cos(\omega_0 t) \tag{2.5}$$

$$x_{LO,Q}(t) = 2\ sin(\omega_0 t + \phi) \tag{2.6}$$

(the factor 2 is used to simplify the equations). If the RF signal provided by the LNA is $x(t) = a\ cos(\omega_0 t) + b\ sin(\omega_0 t)$, where a and b can take the values 1 or -1 to produce the four constellation symbols, we have at the mixers output the following signals,

$$y_I(t) = a + a\ cos(2\omega_0 t) + b\ sin(2\omega_0 t) \tag{2.7}$$

$$y_Q(t) = a\ sin(\phi) + b\ cos(\phi) + a\ sin(2\omega_0 t + \phi) - b\ cos(2\omega_0 t) \tag{2.8}$$

Adding the two signals and applying a low pass filter, the resulting signal at baseband is

$$y(t) = y_I(t) + y_Q(t) = a + a\ sin(\phi) + b\ cos(\phi) \tag{2.9}$$

which is direct related with phase error, illustrated on fig. 2.5(b). The fig. 2.5(c) shows the correspondent constellation when both, gain and phase errors exists.

Even order distortion If the LNA has a second order nonlinearity such as $y(t) = a\ x(t) + b\ x^2(t)$, and if near the channel of interest there exist two interferers, $x(t) = A_1\ cos(\omega_1 t) + A_2\ cos(\omega_2 t)$, one of the resulting output terms is $b\ A_1\ A_2\ cos((\omega_1 - \omega_2)t)$. This indicates that one of the interferers component is near the baseband $(\omega_1 - \omega_2)$ and in the case of an ideal mixer there is no problem because, after multiplication by the LO signal, this component is shifted to high-frequencies. However, the mixers are not ideal and exhibit some feedthrough directly to the output, so part of the interferer appears at the output at baseband together with the down converted signal, which leads to signal distortion(fig. 2.6).

To avoid this problem, differential LNAs and mixers should be employed in order to eliminate even order harmonics, but this implies more power consumption and larger circuit area.

Flicker noise Another drawback is the existence of "flicker noise" that is more significant for low frequencies, specially for MOSFETS. This noise causes signal degradation

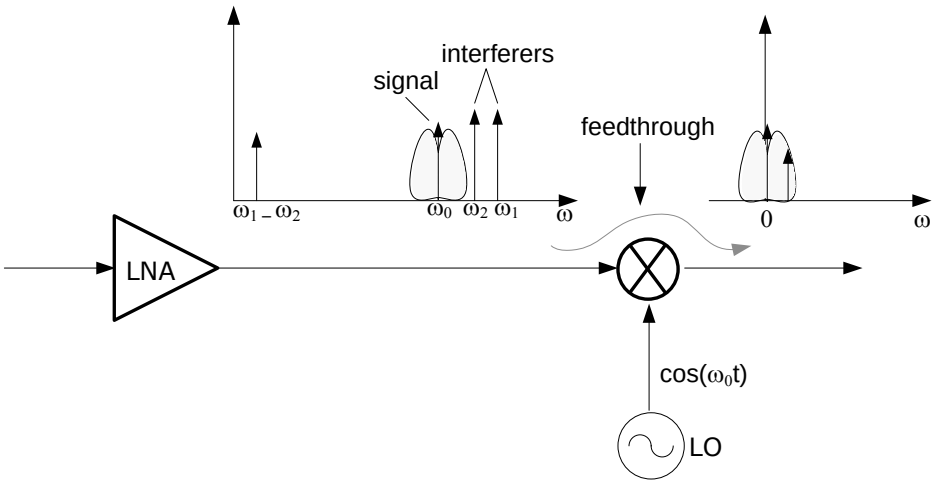


FIGURE 2.6: Effect of even order distortion.

if it appears in the baseband, at the mixer output. The flicker noise subject is further discussed in section 2.4.

In spite of its simplicity, this topology becomes impractical for some applications, although there are techniques to solve some of the above drawbacks by adding additional complexity to the circuit.

2.1.3 Low-IF Receiver

The low-IF topology combines the advantages of both types of receivers, heterodyne and homodyne, by using a mixed approach, i.e, by selecting a low intermediate frequency. This relaxes the channel selection filter specifications and simultaneously avoids the problems related to direct conversion, in particular the flicker noise that strongly affects the baseband signal. To overcome the image problem associated with the heterodyne receiver, a technique to cancel the image signal is employed in order to avoid the image rejection filter. The image cancelation is achieved by using quadrature architectures, in which is supressed after generating a negative replica.

The Hartley[10] architecture (fig. 2.7(a)) is one of the alternatives to cancel the image signal. If at input there is the signal and the corresponding image $x(t) = V_{RF}\ cos(\omega_{RF}t) + V_{Im}\ cos(\omega_{Im}t)$, after down conversion and filtering the resulting signals at X and Y are,

respectively:

$$y(t) = \frac{V_{RF}}{2} cos((\omega_{RF} - \omega_{LO})t) + \frac{V_{Im}}{2} cos((\omega_{LO} - \omega_{Im})t) \tag{2.10}$$

$$y(t) = -\frac{V_{RF}}{2} sin((\omega_{RF} - \omega_{LO})t) + \frac{V_{Im}}{2} sin((\omega_{LO} - \omega_{Im})t) \tag{2.11}$$

Since $sin(\theta - \frac{\pi}{2}) = -cos(\theta)$, after a $-90°$ shift, the signal at Z is,

$$y(t) = \frac{V_{RF}}{2} cos((\omega_{RF} - \omega_{LO})t) - \frac{V_{Im}}{2} cos((\omega_{LO} - \omega_{Im})t) \tag{2.12}$$

Finally, by adding the signals at X and Z, the wanted signal is recovered and the image is suppressed. The Weaver[11] architecture (fig. 2.7(b)) produces a similar result, and the second LO frequency can be chosen to achieve a direct conversion to the baseband. However, both circuits are susceptible to "I/Q mismatch", as referred above, leading to incomplete image rejection.

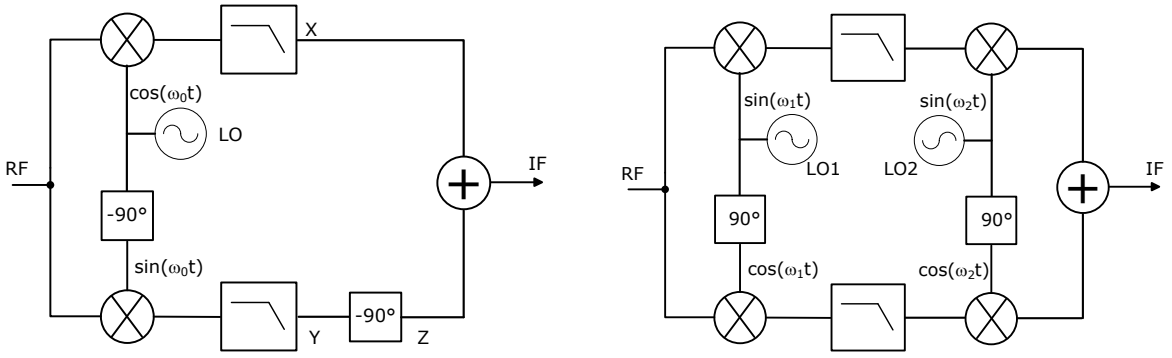


FIGURE 2.7: Image rejection architectures: (a)Hartley (b)Weaver .

The low-IF topology allows a flexible compromise between the Zero-IF and Heterodyne topologies.

2.2 Impedance Matching

Lumped circuit analysis assumes that the physical network's dimensions are much smaller than the electromagnetic wavelength, and therefore, the signal propagation over the network is practically instantaneous. However, for high frequencies the wavelength tends to

be of the same order of the circuit dimensions, and consequently the circuit paths behaves like transmission lines, which require distributed parameters analysis. A segment of a transmission line can be represented by an equivalent lumped circuit, as shown in fig. 2.8, where R,G,L and C, are defined per unit length [12].

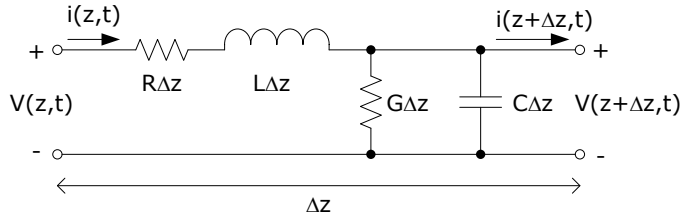


FIGURE 2.8: Transmission line equivalent circuit.

The resistance R represents the conductor loss and the conductance G is due to dielectric loss between the two conductors. Since this is a lumped elements circuit, the Kirchhoff's voltage and current laws (KVL and KCL) can be applied to give,

$$v(z,t) - R\Delta z\, i(z,t) - L\Delta z \frac{\partial i(z,t)}{\partial t} - v(z+\Delta z,t) = 0 \tag{2.13}$$

$$i(z,t) - G\Delta z\, v(z+\Delta z,t) - C\Delta z \frac{\partial v(z+\Delta z,t)}{\partial t} - i(z+\Delta z,t) = 0 \tag{2.14}$$

Dividing (2.13) and (2.14) by Δz and taking the limit for $\Delta z \to 0$, and noting that the derivative of a function by definition is $f^{'}(a) = \lim_{\Delta z \to 0} \dfrac{f(a+\Delta x) - f(a)}{\Delta x}$, results in:

$$\frac{\partial v(z,t)}{\partial z} = -R\, i(z,t) - L\frac{\partial i(z,t)}{\partial t} \tag{2.15}$$

$$\frac{\partial i(z,t)}{\partial z} = -G\, v(a,t) - C\frac{\partial v(z,t)}{\partial t} \tag{2.16}$$

For the sinusoidal steady-state condition, (2.15) and (2.16) can be simplified into,

$$\frac{d\,V(z)}{dz} = -(R + j\omega L)\, I(z) \tag{2.17}$$

$$\frac{d\,I(z)}{dz} = -(G + j\omega C)\, V(z) \tag{2.18}$$

Applying the derivative in both terms of (2.15) and (2.16) a second order differential equations are given as follows

$$\frac{d^2\,V(z)}{dz^2} - \gamma^2\,V(z) = 0 \tag{2.19}$$

$$\frac{d^2\,I(z)}{dz^2} - \gamma^2\,I(z) = 0 \tag{2.20}$$

where,

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.21}$$

is the propagation constant, which is frequency dependent. The solutions of these differential equations gives the expressions for currents and voltages of the traveling waves across the transmission line at a specific point, namely,

$$V(z) = V_o^+\,e^{-\gamma z} + V_o^-\,e^{\gamma z} \tag{2.22}$$

$$I(z) = I_o^+\,e^{-\gamma z} + I_o^-\,e^{\gamma z} \tag{2.23}$$

where the term $e^{-\gamma z}$ represents the wave propagation in the $+z$ direction and $e^{\gamma z}$ in the $-z$ direction. Applying (2.17) on (2.22) is obtained the following expression for the current over the line,

$$I(z) = (V_o^+\,e^{-\gamma z} - V_o^-\,e^{\gamma z})\frac{\gamma}{R + j\omega L} \tag{2.24}$$

For (2.24) and (2.23) to be equivalent, implies that $I_o^+ = V_o^+\frac{\gamma}{R+j\omega L}$ and $I_o^- = V_o^-\frac{\gamma}{R+j\omega L}$, where

$$Z_0 = \frac{V_o^+}{I_o^+} = \frac{V_o^-}{I_o^-} = \frac{R + j\omega L}{\gamma} \tag{2.25}$$

is the transmission line characteristic impedance. When the line is terminated by a load Z_L at $z = 0$ (fig. 2.9), assuming that the wave source is located at a positions $z < 0$, the following condition must be verified,

$$Z_L = \frac{V(0)}{I(0)} = \frac{V_o^+ + V_o^-}{V_o^+ - V_o^-}Z_0 \tag{2.26}$$

where V_o^+ and V_o^- are the amplitude voltages of the incident and reflected waves, respectively. From this relation is derived the voltage reflection coefficient, Γ:

$$\Gamma = \frac{V_o^-}{V_o^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.27}$$

that is the amplitude of the reflected wave normalized to the incident wave amplitude.

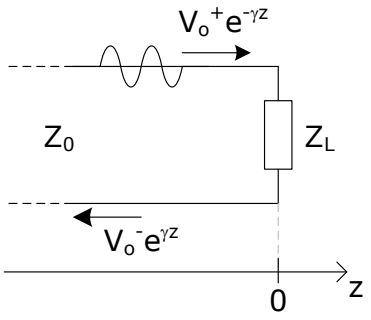


FIGURE 2.9: Transmission line terminated by an arbitrary load.

To achieve the maximum power transfer to the load, there should not exist reflection, i.e, $\Gamma = 0$, which only occurs when $Z_L = Z_0$, and then the load is matched to the line characteristic impedance. Usually in RF systems the antenna has a characteristic impedance of 50 Ω, so the first block of a receiver must have the input impedance matched to 50 Ω.

2.3 Scattering Parameters

At high-frequencies, the traditional system characterization used in low-frequencies trough open and short-circuit measurements is no longer possible, because currents and voltages measurements involve the magnitude and phase of the traveling waves[13]. For that reason, at high-frequencies (when the device length is not negligible with respects to the wavelength) different parameters are required for network characterization. The scattering parameters (S-parameters) relate the voltages of incident and reflected waves, at n-ports, trough the scattering matrix,

$$\begin{bmatrix} V_1^- \\ \vdots \\ V_n^- \end{bmatrix} = \begin{bmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & & \vdots \\ S_{n1} & \cdots & S_{nn} \end{bmatrix} \cdot \begin{bmatrix} V_1^+ \\ \vdots \\ V_n^+ \end{bmatrix} \tag{2.28}$$

where, V_n^+ is the voltage amplitude of the incident wave on port n and V_n^- corresponds to the reflected wave. A specific s-parameter is determined as follows,

$$S_{ij} = \left.\frac{V_i^-}{V_j^+}\right|_{V_k^+=0,\ k\neq j} \tag{2.29}$$

which physically means that an s-parameter gives the voltage ratio between the reflected wave at port i and the incident wave at port j when the other ports are terminated with a matched load to avoid reflections. The s-parameters are measured directly with a network analyzer, and allow an accurate network characterization without knowing in detail the circuit inside the network.

For the particular case of a two-port network (fig.2.10) the s-parameters are designated according to their physical meaning[12]:

- S_{11} - Input reflection coefficient
- S_{21} - Forward voltage gain
- S_{12} - Reverse voltage gain
- S_{22} - Output reflection coefficient

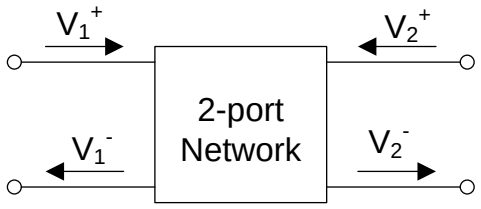


FIGURE 2.10: Two-Port Network with the incident and reflected waves.

In receiver front-ends, the s-parameters are particularly useful in LNA design due the need of input matching, and are associated with the concept of return loss. The return loss is a figure of merit for signal reflection and indicates the fraction of the incident power that is reflected back to the source. LNAs technical specifications usually include the input return loss, defined as,

$$RL = -20log(|s_{11}|) \tag{2.30}$$

It is desirable to minimize the reflected power, so more power is transferred to the load. Typically, designers aim for at least 10 dB return loss, which means that only a maximum of 10% of the total power is reflected back.

2.4 Noise

Noise arises in electronic circuits as a random variable, caused by physical phenomena due to the nature of the materials or by external interferences. Noise is non deterministic and its instantaneous value can not be foreseen. The presence of noise in circuits is inevitable, and therefore, is important to analyze its impact on the degradation of signals of interest and develop methods to minimize the its effect. In this section the main noise sources present in CMOS transistors [3, 14] are described.

2.4.1 Thermal Noise

The thermal noise in circuits is due to the random motion of electrons causing a variation of current. The thermal noise power can be quantified by

$$P = kT\Delta f \tag{2.31}$$

that is proportional to the material temperature T (Kelvin), where k is Boltzmann's constant and Δf is the bandwidth of the system. In a resistor, the average noise power generated

$$\overline{V_{th}^2} = 4kTR\Delta f \tag{2.32}$$

can be modeled by a voltage source in series with the resistor or by a current source in parallel with it, as shown in fig. 2.11.

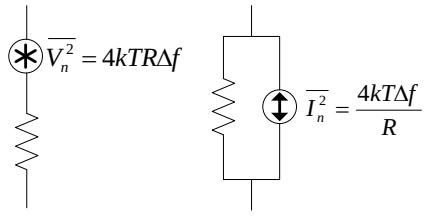


FIGURE 2.11: Resistor thermal noise models.

MOS transistors also exhibit thermal noise due to carrier motion through the channel, and this noise can be represented by a current source in parallel with the conducting channel (fig. 2.12). The noise generated when the device is operating in triode region is given by [15]:

$$\overline{I_n^2} = 4kT\gamma g_{d0}\Delta f \tag{2.33}$$

where g_{d0} is the drain-source conductance for $V_{DS} = 0$ and γ is the noise excess factor(NEF) and has a value of unity for this bias condition. However, this result can be extended to long-channel MOSFET devices operating in saturation [16],

$$\overline{I_n^2} = 4kT\gamma g_m\Delta f \tag{2.34}$$

by matching $\gamma = 2/3$. For short-channel and submicron MOSFETS, the value of γ has higher values [17].

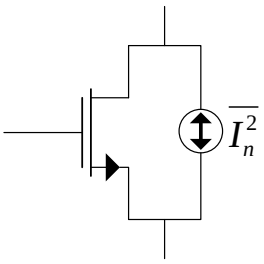


FIGURE 2.12: Mosfet thermal noise representation.

For further analysis and notation simplicity let we assume that $\Delta f = 1$ Hz, which means that the noise is expressed per unit bandwidth (A^2/Hz).

2.4.2 Shot Noise

Shot noise is caused by fluctuation of the current that crosses a potential barrier, such as in a pn-junction. The diffusion of charge carriers, which leads the current is random, because the carriers do not all have the same speed, causing the fluctuation of current around an average value. The equivalent noise source is given by

$$\overline{I_{ns}^2} = 2qI_{DC}\Delta f \tag{2.35}$$

where q is the electron charge and I_{DC} is the DC current. Shot noise is more significant in bipolar transistors, because both emmiter and collector currents are sources of shot noise,

since they cross pn-junctions. In MOSFETs, the DC gate leakage current contributes with shot noise, but it is usually very small and in most cases it can be neglected.

2.4.3 Flicker Noise

The flicker noise in FETs has origin in a physical phenomenon, somewhat unpredictable, that is related with the interface between the gate oxide (SiO_2) and silicon substrate (Si). The random fluctuation of the number of carriers in the channel is caused by trapping and release of carriers in the $Si - SiO_2$ interface. Flicker noise is proportional to $1/f$, so it is dominant at low frequencies. It is represented by a voltage source in series with the gate

$$\overline{V_{nf}^2} = \frac{k_f}{c_{ox}\, W\, L\, f^{\alpha_f}} \tag{2.36}$$

where k_f is a process dependent constant, which is bias independent, and c_{ox},W and L, are the gate oxide capacitance per unit area, width, and length of the MOSFET, respectively. A cleaner fabrication process results in lower values for k_f. For p-channel devices k_f is lower than for n-channel, and thus, have less flicker noise. The exponent α_f is close to unity, and can have values between 0.7 and 1.2[16]. In this thesis, the values $k_f = 4 \times 10^{-}23$ V^2F and $\alpha_f = 1.2$ are considered for the 130 nm technology [18]. This type of noise is still subject of study with respect to its origins and modeling.

2.4.4 Noise Figure

The noise factor, F, or noise figure, NF, when expressed in dB, is the most common measure of the noise generated by a circuit (characterized by a 2-port network). The noise factor is defined as the ratio between the total noise power at the 2-port output and the 2-port output noise power due to the input noise source only:

$$F = \frac{Total\ output\ noise\ power}{Output\ noise\ due\ to\ the\ source} \tag{2.37}$$

In fig. 2.13 is represented a noisy 2-port with gain A. The noise factor is

$$F = \frac{N_2}{A^2 N_1} \tag{2.38}$$

where N_2 is the total noise power available at the output and N_1 is the noise power available at the 2-port input.

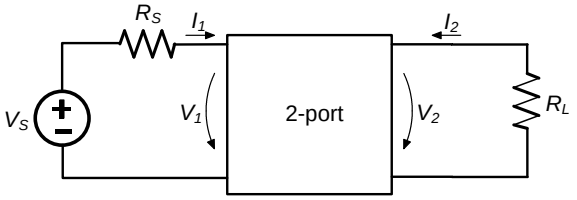


FIGURE 2.13: Noisy 2-port with gain A

If the ports are adapted and a power signal S_1 is applied from generator, then by the maximum power transfer theorem, the signal power is transferred entirely to the 2-port, and so is the signal power S_2 from the 2-port output to the load resistor R_L. The power gain is

$$A^2 = \frac{S_2}{S_1} \tag{2.39}$$

so,

$$F = \frac{N_2}{A^2 N_1} = \frac{\frac{S_1}{N_1}}{\frac{S_2}{N_2}} = \frac{(S/N)_i}{(S/N)_o} \tag{2.40}$$

The last equation relates the noise factor with the signal to noise ratios at the input and output of the 2-port, which shows the degradation of the signal to noise ratio due to the noise introduced by the 2-port. When no additional noise is introduced by the 2-port, $F = 1$.

2.5 Nonlinear Distortion

The performance related to linearity can be characterized by the 1 dB compression point and the 3rd-order intermodulation product. These parameters appear in the systems specification.

A linear system when excited by an input signal generates an output signal proportional to the input. Most devices have non-linear characteristic, and if they are memoryless and time invariant, then their operation may be represented by a Taylor series, i.e,

$$y = a_0 + a_1 x + \ldots + a_n x^n \tag{2.41}$$

The terms used to represent these devices depend the type of non-linearity, its representation being more accurate if more terms are used.

2.5.1 Harmonics

Nonlinear devices generate harmonics. A nonlinear device characterized by a third-order polynomial is usually a good approximation, that simplifies the calculations. If the input signal is sinusoidal,

$$v_i(t) = V_m cos(\omega_f t) \tag{2.42}$$

the output is

$$y(t) = a_0 + a_1 V_m cos(\omega_f t) + a_2 V_m^2 cos^2(\omega_f t) + a_3 V_m^3 cos^3(\omega_f t) \tag{2.43}$$

or

$$y(t) = \underbrace{a_0 + \frac{a_2 V_m^2}{2}}_{DC\ component} + \underbrace{\left(a_1 V_m + \frac{3a_3 V_m^3}{4}\right) cos(\omega_f t)}_{1^{st} Harmonic(fundamental)} + \underbrace{\frac{a_2 V_m^2}{2} cos(2\omega_f t)}_{2^{nd} Harmonic} + \underbrace{\frac{a_3 V_m^3}{4} cos(3\omega_f t)}_{3^{rd} Harmonic} \tag{2.44}$$

A nonlinearity of order n generates n harmonics with multiples of the fundamental frequency ($n\,\omega_f$). The even order coefficients affect the DC component, whereas the odd order coefficients have impact on the fundamental frequency amplitude.

2.5.2 Intermodulation Product

If, instead of applying a single sinusoidal signal at the non-linear device input, two signals are applied with different frequencies:

$$v_i(t) = V_1 cos(\omega_1 t) + V_2 cos(\omega_2 t) \tag{2.45}$$

intermodulation products are generated at the output, given by:

$$\begin{aligned} y(t) =& a_0 + a_1(V_1 cos(\omega_1 t) + V_2 cos(\omega_2 t)) + \\ & a_2 \left[\begin{array}{c} \frac{V_1^2}{2}(1 + cos(2\omega_1 t)) + \frac{V_2^2}{2}(1 + cos(2\omega_2 t)) + \\ V_1 V_2 (cos((\omega_1 + \omega_2)t) + cos((\omega_1 - \omega_2)t)) \end{array} \right] + \\ & a_3 \left[\begin{array}{c} \left(\frac{3}{4}V_1^3 + \frac{3}{2}V_1 V_2^2\right) cos(\omega_1 t) + \left(\frac{3}{4}V_2^3 + \frac{3}{2}V_2 V_1^2\right) cos(\omega_2 t) + \\ \frac{3}{4}V_1^2 V_2 (cos((2\omega_1 + \omega_2)t) + cos((2\omega_1 - \omega_2)t)) + \\ \frac{3}{4}V_2^2 V_1 (cos((2\omega_2 + \omega_1)t) + cos((2\omega_2 - \omega_1)t)) + \\ \frac{3}{4}V_1^3 cos(3\omega_1 t) + \frac{3}{4}V_2^3 cos(3\omega_2 t) \end{array} \right] \end{aligned} \tag{2.46}$$

In addiction to harmonics, intermodulation products appear at frequencies $n\,\omega_1 \pm m\,\omega_2$. Fig. 2.14 illustrates the intermodulation products for a particular case of a nonlinearity of order 3 (IM3).

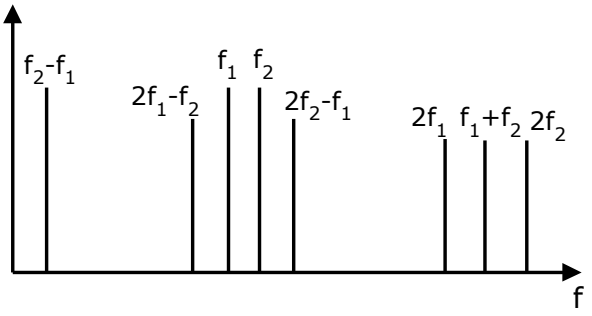


FIGURE 2.14: Frequency spectrum showing the intermodulation products of a nonlinear device of order 3.

2.5.3 1 dB Compression Point

The 1 dB compression point is a linearity measure of a circuit and is defined as the output signal power that corresponds to a difference of 1 dB from the ideal (linear) circuit, as shown in fig. 2.15. In that point, the saturation is reached and consequently degrades the signal.

2.5.4 Third-order Intercept Point

The third-order intercept point (IP3) is defined as the point at which the curves of power output of the fundamental frequency and of the third-order intermodulation product

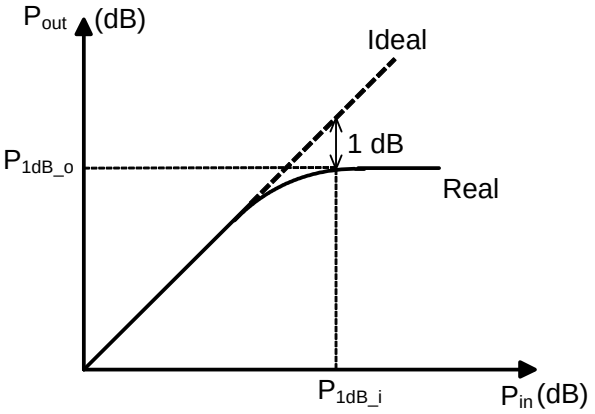


FIGURE 2.15: Definition of 1 dB compression point.

would intercept if they were linear, i.e, when the amplitude of the fundamental frequency would be equal to the amplitude of the third-order intermodulation product. A practical rule that is employed in most radio frequency amplifiers is that the 1 dB compression point falls approximately 10 dB below the intercept point. The specification of IP3 is usually input-referred (IIP3), but can also output-referred (OIP3), as illustrated in fig. 2.16.

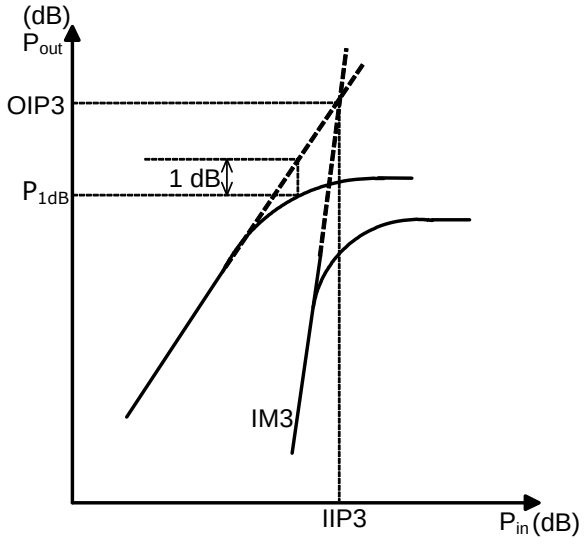


FIGURE 2.16: Definition of IP3.

2.6 Low Noise Amplifiers

In this section, typical requirements and LNA topologies are discussed. The LNA, is typically the first amplifying stage. The LNA input impedance should match the antenna characteristic impedance to maximize the power transfer. The LNA should provide enough gain for the required SNR, and at the same time the noise factor should be low to introduce a minimum noise in the system. The fulfillment of these specifications, when several blocks are connected in cascade, require additional considerations. For example, the overall noise factor of a cascade stages is given by Friis formula [19]:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \times \cdots \times G_{n-1}} \tag{2.47}$$

where F_n and G_n are the noise factor and the available power gain of the n^{th} stage. From (2.47) it is seen that the noise factor of the first stage (LNA) is dominant, and that its gain should be large enough to reduce the noise contributions of the subsequent stages.

The overall performance of cascaded stages in terms of linearity can be characterized by equation[1]:

$$\frac{1}{IIP_3} = \frac{1}{IIP_{3,1}} + \frac{G_1}{IIP_{3,2}} + \frac{G_1 G_2}{IIP_{3,3}} + \cdots \tag{2.48}$$

where $IIP_{3,i}$ and G_i, are the input referred third-order intercept point, expressed in power, and the power gain of the i^{th} stage, respectively. The stage with the worst IIP_3 limits the the overall system linearity. The gain of preceding stages affects directly the IIP_3 of the last stage, but a low noise figure demands a high gain for the first stage. So, there is a trade off between noise and linearity.

Concerning the bandwidth LNAs can be either narrowband, multi-band or wideband. An overview of the main existing LNA topologies for CMOS technology are presented next [20, 21, 22].

2.6.1 Narrowband LNAs

Common-Source LNA with Degeneration

The common-source (CS) LNA with inductive degeneration is one of the most used topologies to design a narrowband LNA, because it allows low noise figure, high gain, and easy

input matching. The input impedance of the CS LNA (fig. 2.17) is:

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L_s \tag{2.49}$$

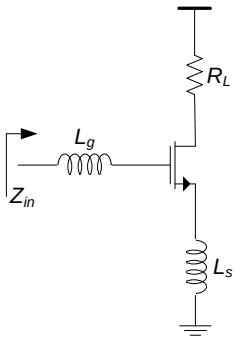


FIGURE 2.17: Common-Source LNA with inductive degeneration.

where the inductances L_s and L_g are chosen to resonate with the device capacitance C_{gs} at the frequency operation

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{2.50}$$

This eliminates the imaginary part of Z_{in} and the term $\frac{g_m}{C_{gs}}L_s$ is set to match 50 Ω. The inductance L_g gives degree of freedom in the LNA design, since the gain is proportional to g_m. The use of inductors, which are ideally noiseless, improves the noise factor, but it increases significantly the die area of the LNA. RF options (thick metal layer for high Q inductors), and the large die area, increase the production cost.

2.6.2 Wideband LNAs

2.6.2.1 Common-Source with Resistive Input Matching

The simplest way to get a stable input impedance is to use resistive input matching. The CS stage, shown in fig. 2.18, employs this technique, in which a resistor is in parallel with the amplifier input. However, this resistor introduces a significant amount of noise.

Assuming that the amplifier has an available power gain A_p and a noise power at output P_n, due to internal sources only, if the source has an impedance R_S, the noise factor can

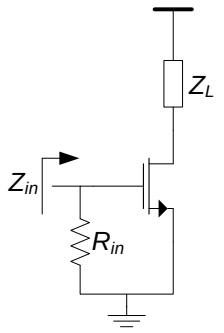


FIGURE 2.18: Common-Source stage with resistive input matching.

be expressed by:

$$F = \frac{Total\ output\ noise}{Total\ output\ noise\ due\ to\ source\ only}$$

$$= \frac{4kTR_SA_p + 4kTR_{in}A_p + P_n}{4KTR_SA_p} = 2 + \frac{P_n}{4KTR_SA_p} \tag{2.51}$$

which gives a noise figure of at least 3 dB.

2.6.2.2 Common-Gate

The common-gate topology (fig. 2.19) has an intrinsic wideband response, which is one of the reasons why it is widely used to implement LNAs. In a first order analysis, its input impedance is approximately $\frac{1}{g_m}$, and g_m can be easily dimensioned to achieve the input impedance matching.

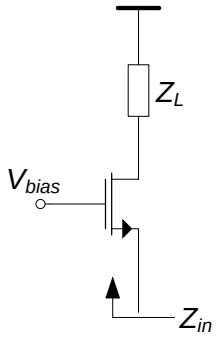


FIGURE 2.19: Common-Gate LNA.

To estimate the lower bound of the noise factor, only the transistor thermal noise is considered. If it is referred to the input, we obtain:

$$F = 1 + \gamma g_{d0} R_S = 1 + \frac{\gamma}{\alpha} g_m R_S \tag{2.52}$$

where $\alpha \approx \frac{g_m}{g_{d0}}$. For long channel devices, the noise excess factor γ is $\frac{2}{3}$ and the short-channel effects can be neglected ($\alpha = 1$) [17]. With matching $g_m R_S = 1$. Thus, the minimum noise factor is about $F = \frac{5}{3}$, which corresponds a noise figure of 2.2 dB. However, the CG-LNA has a disadvantage, since g_m is imposed by the matching condition, the gain being only dependent on the load Z_L. Increasing Z_L increases the gain, but also increases the noise, which will limit the gain possible to achieve. In practice, the CG-LNA has typical noise figures values above 3 dB. A detailed analysis of the CG is performed in the next chapter.

2.6.2.3 LNA with resistive shunt feedback

The wideband LNA represented in fig. 2.20(a) uses the feedback resistor R_F for matching. Accordingly to the incremental model (fig. 2.20(b)), the input impedance is:

$$Z_{in} = \frac{R_F + Z_L}{sC_{gs}(R_F + Z_L) + 1 + g_m Z_L} = \left(\frac{1}{sC_{gs}} // \frac{R_F + Z_L}{1 + g_m Z_L} \right) \tag{2.53}$$

which depends of many parameters, so, some assumptions will be made. For frequencies such that C_{gs} is negligible, the gate is seen like a high impedance, and assuming that $Z_L >> R_F$ the input impedance simplifies to $1/g_m$.

Using a similar analysis, for low frequencies the gain is

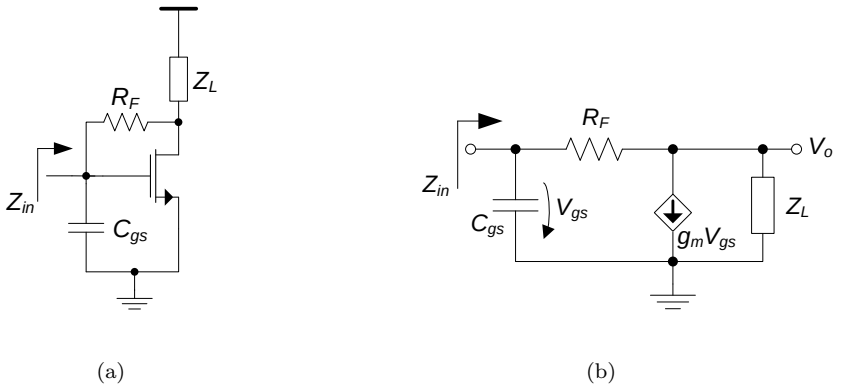
$$A_v = \frac{(1 - g_m R_F) Z_L}{R_F + Z_L} \tag{2.54}$$

and if the load Z_L is high, $g_m R_F >> 1$, the gain is simplified into:

$$A_v \approx -g_m R_F \tag{2.55}$$

This approximation is useful when considering the noise factor, that is found to be [23]:

$$F = 1 + \frac{R_F}{R_S} \left(\frac{1 + g_m R_S}{1 - g_m R_F} \right)^2 + \frac{1}{R_S Z_L} \left(\frac{R_F + R_S}{1 - g_m R_F} \right)^2 + \frac{\gamma g_m}{\alpha R_S} \left(\frac{R_F + R_S}{1 - g_m R_F} \right)^2 \tag{2.56}$$



(a) (b)

FIGURE 2.20: LNA with resistive shunt feedback: (a) schematic (b) low and medium frequencies small signals model.

and at a first sight, by increasing the term $g_m R_F$ the noise factor is reduced and the gain is enhanced, as intended. g_m is set by the input matching condition, and R_F is increased, the previous assumption of having a high load Z_L compared to R_F is no longer valid. So, g_m and R_F have to be carefully dimensioned to achieve an optimal performance.

2.6.3 Discussion

The basic LNA architectures were presented above in the single-ended form, but a differential structure could be used instead. To transform the signal from the antenna into a differential signal, a balun would be required which introduces extra loss and additional noise.

The narrowband LNAs present good noise figure, high gain, and accurate matching due to the LC tunning for the frequency of interest, but inductors occupy a large area and increase significantly the chip cost. Wideband LNAs are typically inductorless, suitable for systems with low area and with specifications that are not critical. With the scaling of CMOS technology it is possible to achieve low power, low cost, and an acceptable noise figure, and inductorless wideband LNAs became a competitive choice to implement multi-band LNAs. These can be implemented by using narrowband LNAs in a multiple input stage, or by wideband LNA with a band-pass filter for each band.

Chapter 3

Common Gate Stage

The common gate stage (fig. 3.1) is a widely known amplifier topology, which will be used as one of the stages in the proposed LNA architecture. In this chapter, a theoretical analysis to obtain the key parameters of the LNA (input matching, gain, NF) is done, and different levels of approximation are performed. Equations are validated by circuit simulation with in a 130 nm CMOS technology.

3.1 Theoretical Analysis

In this section we review some known expressions for input impedance, gain, and noise figure. For each parameter we derive three equations that depends on the model used to

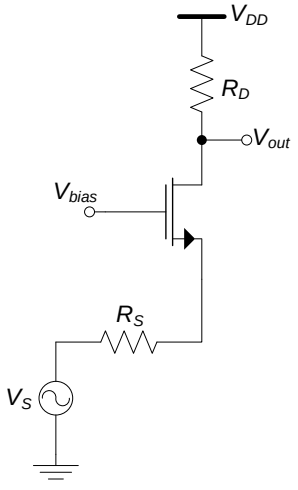


FIGURE 3.1: Common Gate Stage.

represent the transistor, starting with the most simplified model till a more complex one including the parasitic capacitances.

3.1.1 Low frequency model neglecting r_o

The small signal model for low frequencies of the CG stage is represented in fig.3.2, where transistor's output impedance is neglected for simplicity. Since the signal(V_{in}) is applied in transistor's source terminal, the bulk effect has to be considered, represented in the model by a voltage controlled current source(VCCS) that depends on source-bulk voltage (V_{sb}).

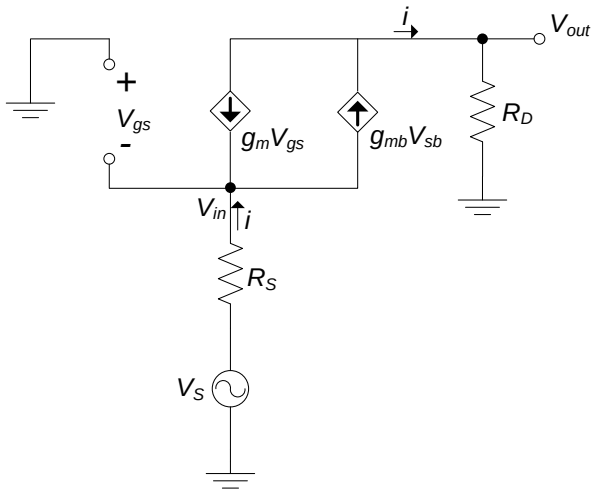


FIGURE 3.2: Simplified CG small signal model for low frequencies.

Gain

The signal present at output is given by

$$V_{out} = R_D i \tag{3.1}$$

Noting that $V_{sb} = -V_{gs} = V_{in}$, the current i can be expressed as

$$i = g_{mb}V_{sb} - g_m V_{gs} = (g_m + g_{mb})V_{in} \tag{3.2}$$

and then substituting on (3.1), we obtain the CG gain

$$A_{vCG\_0} = \frac{V_{out}}{V_{in}} = (g_m + g_{mb})R_D \tag{3.3}$$

Input Impedance

The input impedance is viewed from the source, as shown in fig. 3.3.

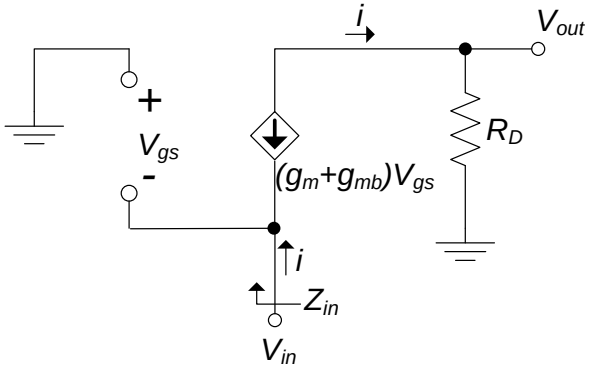


FIGURE 3.3: Input impedance.

The current i that flows into the transistor source is

$$i = -(g_m + g_{mb})V_{gs} = (g_m + g_{mb})V_{in} \tag{3.4}$$

and the input impedance is

$$Z_{inCG\_0} = \frac{1}{g_m + g_{mb}} \tag{3.5}$$

Noise

The three major noise sources in the circuit are considered: thermal noise generated by the resistors and transistor, and flicker noise. These noise sources are represented in fig. 3.4(a).

To obtain the total noise power at the output, $\overline{V_{n,out}^2}$, we have to sum (assuming independent noise sources) all the noise contributions at output using the superposition theorem.

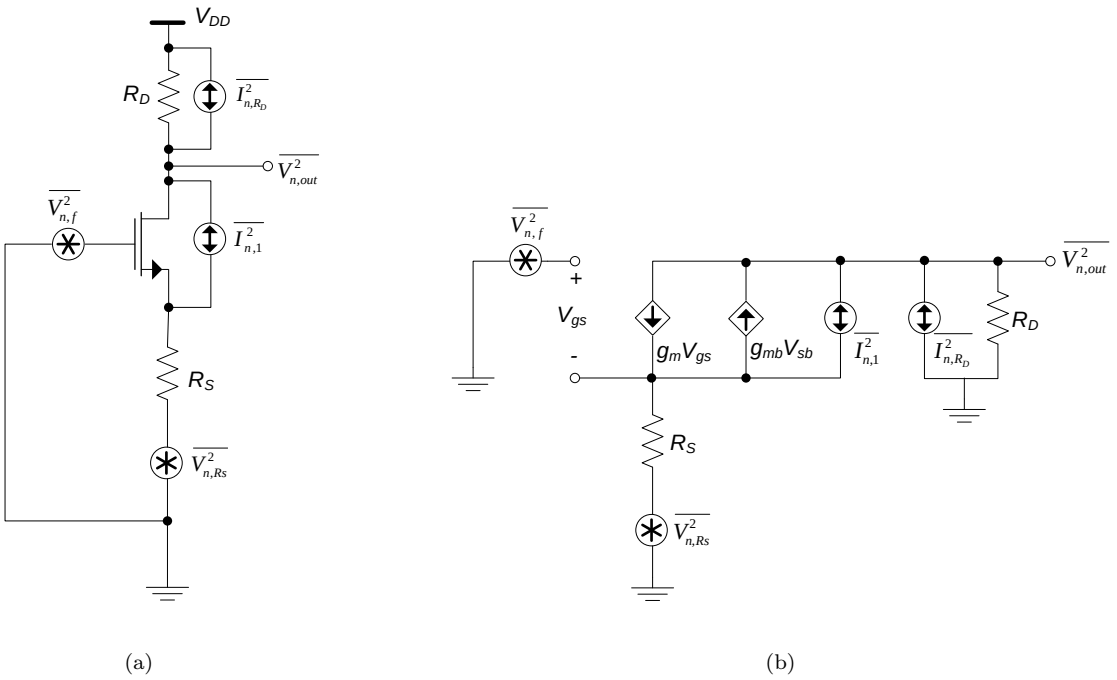


FIGURE 3.4: CG noise model: (a)circuit, (b)small signal equivalent circuit.

Thermal noise due to source resistor R_S

Let us consider now only the thermal noise source V_{n,R_S} due to R_S, as shown in fig. 3.5

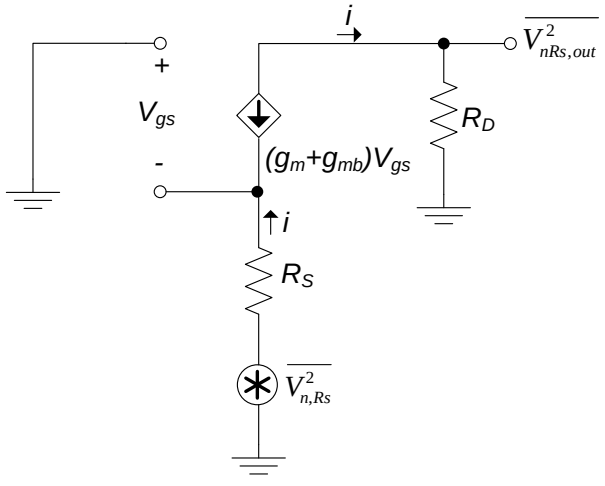


FIGURE 3.5: Thermal noise representation from the source resistor.

At output we have the noise generated by R_S, resulting from the current i, which passes trough R_D,

$$V_{nR_S,out} = iR_D = -(g_m + g_{mb})V_{gs}R_D \tag{3.6}$$

Applying the KVL from the gate to ground, we verify that $V_{gs} - iR_S + V_{n,R_S} = 0$ and, therefore:

$$V_{gs} = iR_S - V_{n,R_S} \Leftrightarrow V_{gs} = \frac{V_{nR_S,out}}{R_D}R_S - V_{n,R_S} \tag{3.7}$$

Then substituting (3.7) on (3.6) and solving,

$$V_{nR_S,out} = \frac{V_{n,R_S}(g_m + g_{mb})R_D}{1 + (g_m + g_{mb})R_S} \tag{3.8}$$

Turning (3.8) in terms of power, the output noise power due to R_S is:

$$\overline{V^2_{nR_S,out}} = \frac{\overline{V^2_{n,R_S}}(g_m + g_{mb})^2 R_D^2}{(1 + (g_m + g_{mb})R_S)^2} = 4kTR_S\left[\frac{(g_m + g_{mb})R_D}{1 + (g_m + g_{mb})R_S}\right]^2 \tag{3.9}$$

Flicker noise

The flicker noise is modeled as a voltage noise source($V_{n,f}$) in series with the transistor gate (fig. 3.6).

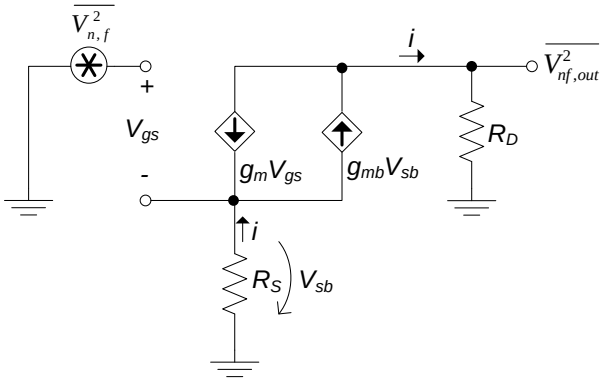


FIGURE 3.6: Flicker noise representation.

From the gate to ground we have $V_{n,f} = V_{gs} + V_{sb}$, where

$$V_{sb} = -iR_S \tag{3.10}$$

and consequently:

$$V_{gs} = iR_S + V_{n,f} \tag{3.11}$$

where the current i is given by

$$i = g_{mb}V_{sb} - g_m V_{gs} \tag{3.12}$$

Replacing (3.10) and (3.11) on (3.12), and solving in order to i,

$$i = -\frac{V_{n,f} g_m}{1 + R_S(g_m + g_{mb})} \tag{3.13}$$

Now, we can compute the voltage noise at output($V_{nf,out}$) due to flicker noise,

$$V_{nf,out} = iR_D = -\frac{V_{n,f} g_m R_D}{1 + R_S(g_m + g_{mb})} \tag{3.14}$$

and in terms of power, we have

$$\overline{V_{nf,out}^2} = \frac{\overline{V_{n,f}^2}(g_m R_D)^2}{(1 + R_S(g_m + g_{mb})^2} = \frac{k_f}{C_{ox} W L f^{\alpha_f}} \left(\frac{g_m R_D}{1 + R_S(g_m + g_{mb})} \right)^2 \tag{3.15}$$

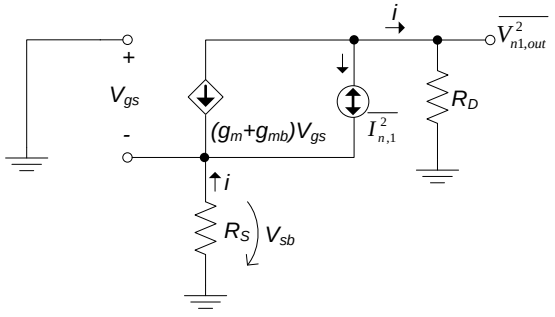


FIGURE 3.7: Transistor thermal noise.

Transistor thermal noise

The thermal noise of the transistor is represented by a current source($I_{n,1}$) between the drain and source(fig. 3.7), so the current that flows into resistor R_D is

$$i = -\left((g_m + g_{mb})V_{gs} + I_{n,1}\right) = -\left((g_m + g_{mb})iR_S + I_{n,1}\right) \Leftrightarrow$$
$$i = \frac{I_{n,1}}{1 + (g_m + g_{mb})R_S} \tag{3.16}$$

and, the noise power due to $I_{n,1}$ present at output is

$$\overline{V_{n1,out}^2} = (iR_D)^2 = \overline{I_{n,1}^2}\left(\frac{R_D}{1 + (g_m + g_{mb})R_S}\right)^2 \Leftrightarrow$$
$$\overline{V_{n1,out}^2} = 4kT\gamma g_m \left(\frac{R_D}{1 + (g_m + g_{mb})R_S}\right)^2 \tag{3.17}$$

Thermal noise due to load resistor (R_D)

The noise due to load resistor R_D, is represented in the small signal model in fig. 3.8. For simplicity, the noise power will be computed referred to the input $V_{nR_D,in}$ without considering R_S.

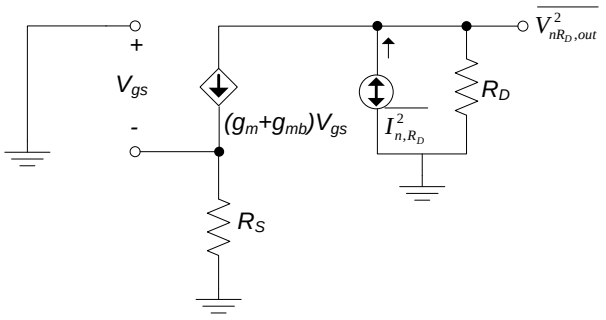


FIGURE 3.8: CG Load resistor thermal noise

The noise present at output ($V_{nR_D,out}$) is only due to the noise current (I_{n,R_D}) that passes through R_D, which is

$$V_{nR_D,out} = I_{n,R_D}R_D \tag{3.18}$$

The noise at input is the output noise divided by the gain of the CG stage A_v, given in (3.3),

$$V_{nR_D,in} = \frac{V_{nR_D,out}}{A_v} = \frac{I_{n,R_D} R_D}{A_v} \tag{3.19}$$

In order to take into account the effect of R_S in the circuit's transfer function, let us consider the Thevenin's equivalent circuit of the CG stage (fig. 3.9), where Z_{in} is the input impedance given in (3.5) [24].

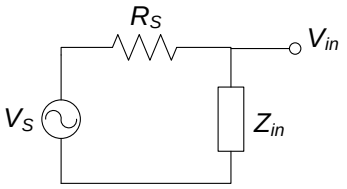


FIGURE 3.9: CG equivalent circuit.

The signal present at input is the source signal multiplied by a resistive divider term (α),

$$V_{in} = \frac{Z_{in}}{R_S + Z_{in}} = \frac{1}{1 + (g_m + g_{mb})R_S} V_S = \alpha V_S \tag{3.20}$$

where

$$\alpha = \frac{1}{1 + (g_m + g_{mb})R_S} \tag{3.21}$$

So, the noise power at output caused by R_D (considering R_S) is

$$\overline{V^2_{nR_D,out}} = \alpha^2 \overline{V^2_{nR_D,in}} A_v^2 = \frac{4kTR_D}{(1 + (g_m + g_{mb})R_S)^2} \tag{3.22}$$

Noise Factor

Since all the noise sources are independent, and consequently the total output noise power ($\overline{V^2_{n,out}}$), shown in fig. 3.4(b), is given by the sum of all noise power contributions at the output,

$$\overline{V^2_{n,out}} = \overline{V^2_{nR_S,out}} + \overline{V^2_{nf,out}} + \overline{V^2_{n1,out}} + \overline{V^2_{nR_D,out}} \tag{3.23}$$

So, by the definition of noise factor (2.37), we have

$$F = \frac{\overline{V_{n,out}^2}}{\overline{V_{n,R_S}^2}(\alpha A_v)^2}$$
$$= 1 + \frac{k_f}{4kTR_SC_{ox}WLf}\left(\frac{g_m}{g_m + g_{mb}}\right)^2 + \frac{\gamma g_m}{R_S(g_m + g_{mb})^2} + \frac{1}{R_SR_D(g_m + g_{mb})^2} \quad (3.24)$$

3.1.2 Low frequency model considering r_o

In the previous section, it was assumed that the transistor output impedance(r_o) was infinite. Here, we derive the expressions for the same parameters considering the effect of r_o, which is modeled with a resistor between the transistor's source and drain (fig. 3.10).

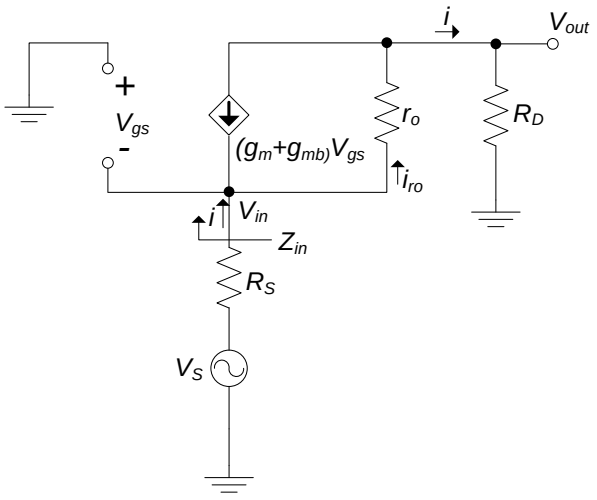


FIGURE 3.10: CG small signal model for low frequencies.

Gain

Analyzing the circuit, it can be seen the current that flows through R_S is the same that goes into R_D, thus,

$$i = \frac{V_{out}}{R_D} \quad (3.25)$$

Using a nodal analysis on the drain, the current i_{ro} is

$$i_{ro} = \frac{V_{out}}{R_D} + (g_m + g_{mb})V_{gs} \tag{3.26}$$

where,

$$V_{gs} = iR_S - V_S = \frac{V_{out}}{R_D}R_S - V_S \tag{3.27}$$

In the terms of KVL, the output voltage (V_{out}) can be expressed as,

$$V_{out} = V_S - iR_S - i_{ro}r_o \tag{3.28}$$

and solving we obtain the transfer function:

$$A_v = \frac{V_{out}}{V_S} = \frac{R_D(1 + r_o(g_m + g_{mb}))}{R_D + r_o + R_S(1 + r_o(g_m + g_{mb})} \tag{3.29}$$

and turning $R_S = 0$, the CG stage gain is

$$A_{vCG\_1} = \frac{V_{out}}{V_{in}} = \frac{R_D(1 + r_o(g_m + g_{mb}))}{R_D + r_o} \tag{3.30}$$

Input Impedance

According to fig. 3.10, the input voltage V_{in} is the sum of drop voltages trough r_o and R_D,

$$V_{in} = r_o i_{ro} + R_D i \tag{3.31}$$

where,

$$i_{ro} = i + (g_m + g_{mb})V_{gs} \tag{3.32}$$

and substituting (3.32) on (3.31), where $V_{gs} = -V_{in}$, the input impedance is

$$Z_{inCG\_1} = \frac{v_{in}}{i} = \frac{r_o + R_D}{r_o(g_m + g_{mb}) + 1} \tag{3.33}$$

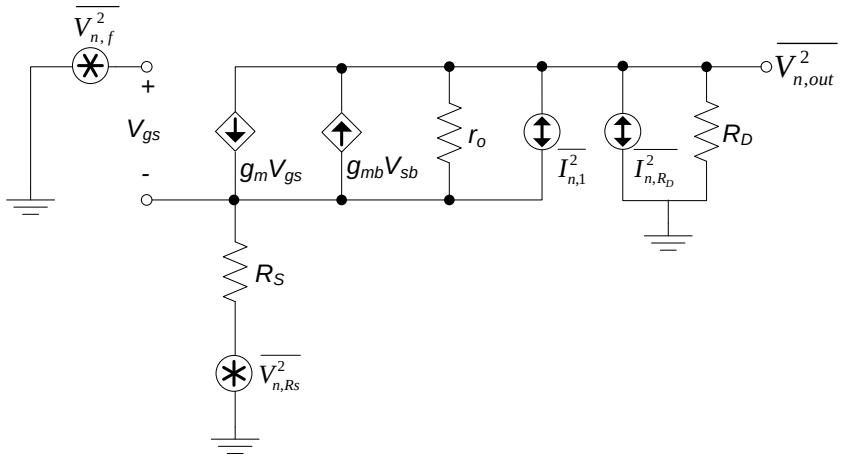


FIGURE 3.11: CG small signal noise model for low frequencies.

Noise

The small signal noise model for low frequencies is represented in fig. 3.11.

Thermal noise due to source resistor R_S

Considering only, the noise source from R_S, at the output we have

$$\overline{V_{nR_S,out}^2} = \overline{V_{n,R_S}^2} A_v^2 \tag{3.34}$$

where the term A_v is the global transfer function obtained in (3.29), leading to

$$\overline{V_{nR_S,out}^2} = 4kTR_S \left[\frac{r_o(g_m + g_{mb})R_D + 1}{r_o + R_S(r_o(g_m + g_{mb}) + 1) + R_D} \right]^2 \tag{3.35}$$

Flicker noise

The noise voltage at the output $V_{nf,out}$ is generated by the current i that passes trough R_D d(fig. 3.12).

According to the currents flow, the current i is

$$i = -g_m V_{gs} + g_{mb} V_{sb} + \underbrace{\frac{(V_{sb} - V_{nf,out})}{r_o}}_{i_{ro}} \tag{3.36}$$

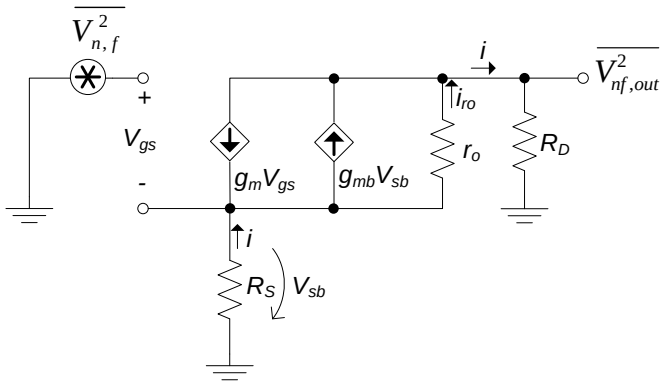


FIGURE 3.12: Flicker noise representation.

where $V_{sb} = -iR_S$ and consequently $V_{gs} = V_{n,f} + iR_S$, and then i can be expressed as

$$i = -\frac{(g_m V_{n,f} + \frac{V_{nf,out}}{r_o})}{1 + R_S(g_m + g_{mb} + \frac{1}{r_o})} \tag{3.37}$$

and the output flicker noise due to flicker is

$$V_{nf,out} = iR_D = -\frac{g_m r_o R_D}{r_o + R_D + R_S(r_o(g_m + g_{mb}) + 1)} V_{n,f} \tag{3.38}$$

which in terms of power is

$$\overline{V_{nf,out}^2} = \left(\frac{g_m R_D r_o}{r_o + R_D + R_S(r_o(g_m + g_{mb}) + 1)}\right)^2 \frac{k_f}{c_{ox} W L f^{\alpha_f}} \tag{3.39}$$

Thermal noise of the transistor

Similarly to the previous case, to determine the output noise voltage $V_{n1,out}$ originated by the transistor thermal noise, we must obtain the output current i expression, which analyzing the circuit output node (fig. 3.13) is

$$i = -(g_m + g_{mb})V_{gs} + I_{n,1} + \frac{V_{sb} - V_{n1,out}}{r_o} \tag{3.40}$$

Since the gate of the transistor is connected to ground, we have $V_{gs} = -V_{sb} = iR_S$, and solving equation (3.40) the current i is

$$i = \frac{I_{n,1} - \frac{V_{n1,out}}{r_o}}{1 + R_S(g_m + g_{mb} + \frac{1}{r_o})} \tag{3.41}$$

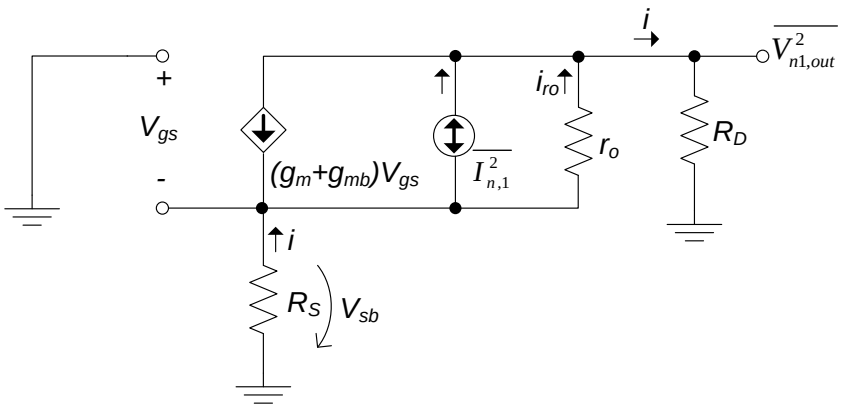


FIGURE 3.13: Transistor thermal noise representation.

The noise voltage generated at output is,

$$V_{n1,out} = iR_D = I_{n,1}\frac{r_o R_D}{r_o + R_D + R_S(r_o(g_m + g_{mb} + 1))} \tag{3.42}$$

and the noise power is,

$$\overline{V^2_{n1,out}} = 4kT\gamma g_m \left(\frac{r_o R_D}{r_o + R_D + R_S(r_o(g_m + g_{mb} + 1))}\right)^2 \tag{3.43}$$

Thermal noise of load resistor

The small signals model representing the thermal noise of R_D, is shown in fig. 3.14.

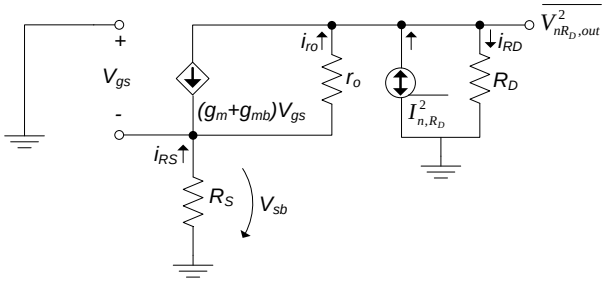


FIGURE 3.14: CG Load resistor thermal noise.

To simplify the circuit analysis, the output noise is computed without considering the effect of R_S, and it is referred to input. The output noise power is,

$$\overline{V^2_{nR_D,out}}' = \overline{I^2_{n,R_D}}\left(\frac{r_o R_D}{r_o + R_D}\right)^2 = \frac{4kT}{R_D}\left(\frac{r_o R_D}{r_o + R_D}\right)^2 \tag{3.44}$$

To refer this noise power at the input, we must divide it by CG square gain obtained in (3.30),

$$\overline{V_{nR_D,in}^2} = \frac{\overline{V_{nR_D,out}^2}'}{A_{vCG}^2} = \frac{4kT}{R_D}\left(\frac{r_o R_D}{(r_o(g_m+g_{mb})+1)R_D}\right)^2 \tag{3.45}$$

The output noise power of the original circuit (including R_S), is calculated by multiplying the noise power at input by the transfer function obtained in (3.29). The noise power at output is,

$$\overline{V_{nR_D,out}^2} = \overline{V_{nR_D,in}^2}A_v^2 = 4kTR_D\left(\frac{r_o}{r_o + R_D + R_S(r_o(g_m+g_{mb})+1)}\right)^2 \tag{3.46}$$

Noise Factor

The total output noise power $\overline{V_{n,out}^2}$ is given by the sum of all individual contributions of noise at the output,

$$\overline{V_{n,out}^2} = \overline{V_{nR_S,out}^2} + \overline{V_{nf,out}^2} + \overline{V_{n1,out}^2} + \overline{V_{nR_D,out}^2} \tag{3.47}$$

and the noise factor is,

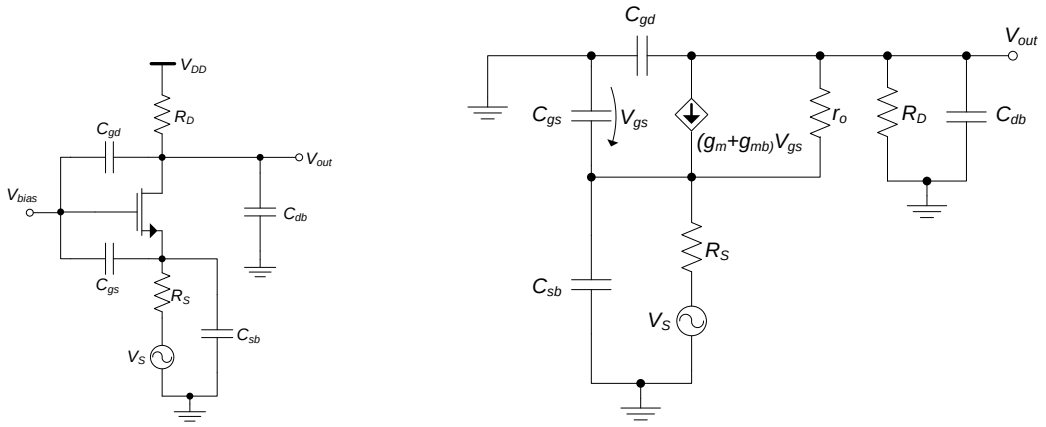
$$F = 1 + \frac{1}{R_S(g_m + g_{mb} + \frac{1}{r_o})^2}\left(\gamma g_m + \frac{1}{R_D} + \frac{k_f g_m^2}{4kTc_{ox}WLf^{\alpha f}}\right) \tag{3.48}$$

3.1.3 Model with parasitic capacitances

In the most complete model of the CG stage, the parasitic capacitances are taken into account, as shown in fig. 3.15(a), where c_{gs}, c_{gd}, c_{db} and c_{sb} are the gate-source, gate-drain, drain-bulk, and source-bulk capacitances, respectively.

From (fig. 3.15(b)), C_{gs} and C_{sb} are connected to the same nodes, and they will be referred as $C_S = C_{gs} + C_{sb}$. The same observation is made for C_{gd} and C_{db}, that will be referred as $C_L = C_{gd} + C_{db}$. At this point, we can simplify the circuit of fig. 3.15(b) into the one represented in fig. 3.16, where the impedance Z_L is the parallel between C_L and R_D.

$$Z_L = (R_D//C_L) = \frac{R_D}{sR_DC_L + 1} \tag{3.49}$$



(a) (b)

FIGURE 3.15: CG stage with parasitic capacitances: (a)circuit, (b)equivalent small signals model.

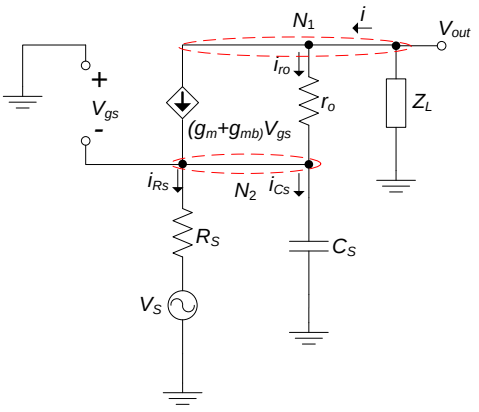


FIGURE 3.16: CG simplified small signals model.

Gain

To obtain the circuit transfer function of fig. 3.16, a nodal analysis is performed at nodes N_1 and N_2. From N_2 we derive an equation for the current i_{R_S}, which passes trough R_S,

$$i_{R_S} = i - i_{C_S} = -\frac{V_{out}}{Z_L} + sC_S V_{gs} \tag{3.50}$$

Performing now the KVL across the source to ground and using (3.50) we have,

$$V_{gs} + i_{R_S} R_S + V_S = 0 \Leftrightarrow V_{gs} = \frac{-\frac{V_{out} R_S}{Z_L} - V_S}{1 + sC_S R_S} \tag{3.51}$$

By inspection of node N_1, we derive the current i_{ro} as,

$$i_{ro} = i - (g_m + g_{mb})V_{gs} = -\frac{V_{out}}{Z_L} - (g_m + g_{mb})V_{gs} \tag{3.52}$$

V_{out} is defined by,

$$v_{out} = i_{ro} r_o - V_{gs} \tag{3.53}$$

and replacing (3.51) and (3.52) in (3.53), we obtain,

$$A_v(s) = \frac{V_{out}(s)}{V_S(s)} = \frac{R_D(r_o(g_m + g_{mb}) + 1)}{as^2 + bs + c} \tag{3.54}$$

where,

$$\begin{aligned} a &= C_S C_L R_S R_D r_o \\ b &= C_L(r_o R_D + R_S R_D r_o(g_m + g_{mb}) + R_S R_D) + C_S R_S(r_o + R_D) \\ c &= r_o + R_D + R_S(ro(g_m + g_{mb}) + 1) \end{aligned}$$

and if $R_S = 0$, we get the CG gain,

$$A_{vCG}(s) = \frac{R_D(r_o(g_m + g_{mb}) + 1)}{sC_L r_o R_D + r_o + R_D} \tag{3.55}$$

Input Impedance

To derive the input impedance, let us consider the currents directions defined on fig. 3.17. At the input node, the current that flows into the circuit is,

$$i = sC_S V_{in} + (g_m + g_{mb})V_{in} - i_{ro} \tag{3.56}$$

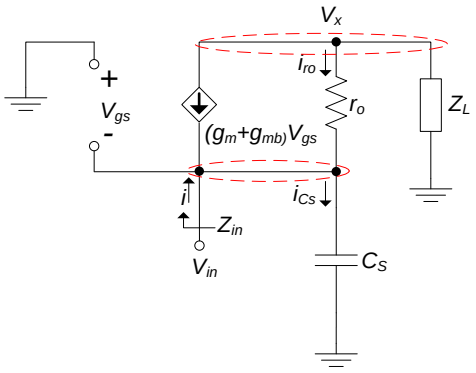


FIGURE 3.17: CG input impedance.

The current i_{ro} can be obtained in terms of V_{in} by solving the following equations system:

$$\begin{cases} i_{ro} = \frac{V_x - V_{in}}{r_o} \\ V_x = -(i_{ro} + (g_m + g_{mb})V_{in})Z_L \end{cases} \Rightarrow i_{ro} = \frac{(g_m + g_{mb})V_{in}Z_L - V_{in}}{r_o + Z_L} \tag{3.57}$$

Substituting (3.57) on (3.56), we obtain,

$$\frac{V_{in}}{i} = \frac{r_o + Z_L}{sC_S(r_o + Z_L) + r_o(g_m + g_{mb}) + 1} \tag{3.58}$$

Regarding that Z_L is given by (3.49), we obtain

$$Z_{inCG}(s) = \frac{sr_oR_DC_L + r_o + R_D}{s^2C_SC_Lr_oR_D + s(C_S(r_o + R_D) + C_L(R_D + r_oR_D(g_m + g_{mb}))) + ro(g_m + g_{mb}) + 1} \tag{3.59}$$

3.2 Circuit Implementation and Biasing

The CG stage, is used for input matching with the antenna (50 Ω). The circuit biasing (fig. 3.18) is made by using a current source I_D. The capacitor at the input decouples the AC signal source from the DC component.

As a starting point to biasing the transistor, the following considerations are taken into account:

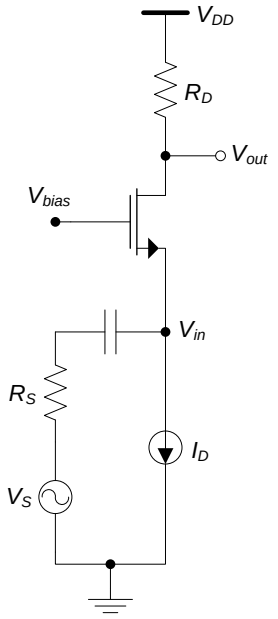


FIGURE 3.18: CG stage biasing circuit.

- The input impedance, is close to $\frac{1}{g_m}$, so it is necessary a $g_m \approx 20$ mS.
- A value of 100 Ω is chosen for the load resistor R_D, to obtain some gain.
- The bias current I_{DC} should be low to reduce the power consumption and large enough to get an adequate voltage drop across the load resistor to provide a suitable output signal range. For these reasons, a bias current of 2 mA is chosen.
- The bias voltage V_{bias} is used to adjust the gate-source voltage V_{GS} in order to maintain the transistor's operating point in the active region($V_{DS} \geq V_{GS} - V_{tn}$). Besides that, the source voltage V_S should allow some margin for the case when the ideal current source I_D is substituted by a transistor operating like a current source.

3.2.1 Biasing Process

The MOSFET drain current for a transistor biased in the active region is,

$$I_D = k_n \frac{W}{2L} V_{dsat}^2 \tag{3.60}$$

where $V_{dsat} = V_{GS} - V_{tn}$. For specific values of I_D and g_m, V_{dsat} is obtained

$$V_{dsat} = \frac{2I_D}{g_m} \tag{3.61}$$

and the value of V_{GS} is imposed. We use the minimum L (120 nm), and from (3.60) the channel width (W) is calculated. Considering the design values above, the CG stage operation point is fully characterized. The drain and source node voltages are

$$V_D = V_{dd} - R_D I_D \tag{3.62}$$

$$V_S = V_{bias} - V_{GS} \tag{3.63}$$

The values used in the first dimensioning are listed on table 3.1, and the simulation results for the DC operation point are compared in table 3.2 with the theoretical values.

R_S (Ω)	R_D (Ω)	W (µm)	L (µm)	V_{DD} (V)	V_{bias} (V)	I_D (mA)
50	100	22.86	0.12	1.2	1	2

TABLE 3.1: Simulation Parameters.

Parameter	Theoretical	Simulated
g_m (mS)	20	14.72
V_{DS} (mV)	581	577.1
V_{dsat} (mV)	200	151
V_{GS} (mV)	581	577.1

TABLE 3.2: Common-Gate DC Operating Point.

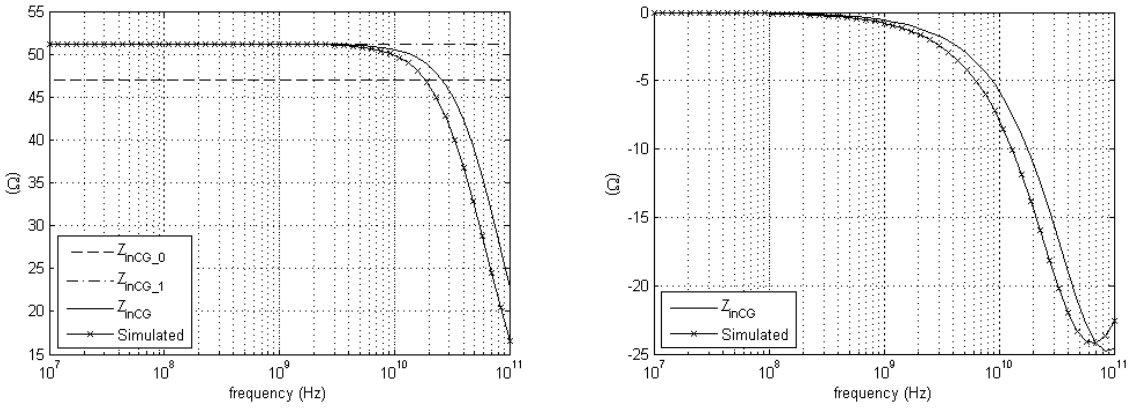
The values of g_m and V_{dsat} are lower than the theoretical ones, so W must be increased to 36.5 µm (for the same bias current) to achieve the desired value. Table 3.3 shows the final values.

Parameter	Value
g_m (mS)	20
V_{DS} (mV)	528.7
V_{dsat} (mV)	125.1
V_{GS} (mV)	528.7

TABLE 3.3: Final DC Operating Point.

3.3 Simulation Results

This section shows the simulation results for the biasing in table 3.3 and the comparison with the theoretical expressions. The real part of the input impedance is shown in fig. 3.19(a). Equation (3.5) for Z_{inCG_0}, used to obtain 50 Ω, is a reasonable starting point,



(a) (b)

FIGURE 3.19: CG Input Impedance: (a)Real part, (b)Imaginary part.

but the input impedance depends also on r_o and R_D, and equation (3.33) for Z_{inCG_1} is accurate for the required frequency range (up to 10 GHz). The plot of Z_{incg} from (3.59) is close to the simulated one, which confirms the theory. This is a complex equation used to verify the limits of the application, since for frequencies higher than 10 GHz, the imaginary part (fig. 3.19(b)) starts to be significant due to parasitic capacitances.

The gain (fig. 3.20) is constant for a wide band, which gives some margin to gain optimization. There is as slight divergence between the simulated and theoretical curve from (3.55). The frequency where A_{vCG} starts to decrease, is higher than in the simulation because the complete model considered does not takes into account all the parasitics effects.

The results for the noise figure are shown in fig. 3.21 where, NF_0 and NF correspond to equations (3.24) and (3.48), respectively. We assume a value for noise excess factor of γ=1 for simplicity. Note that the CG configuration presents a considerable noise figure due to the resistive input matching, which adds at least 3 dB to the noise figure, which is a major drawback.

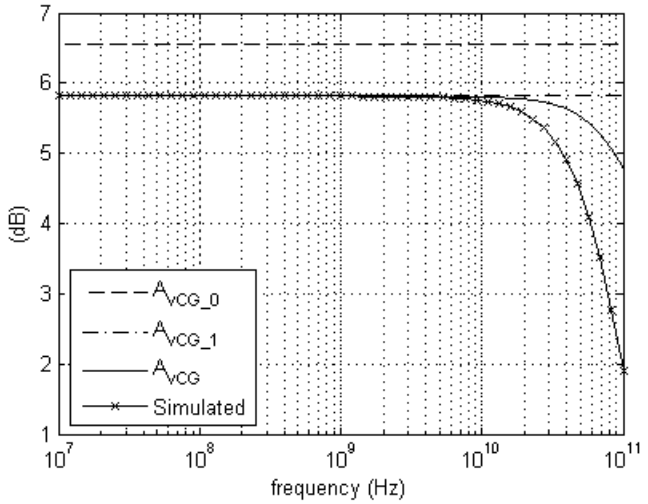


FIGURE 3.20: CG Gain.

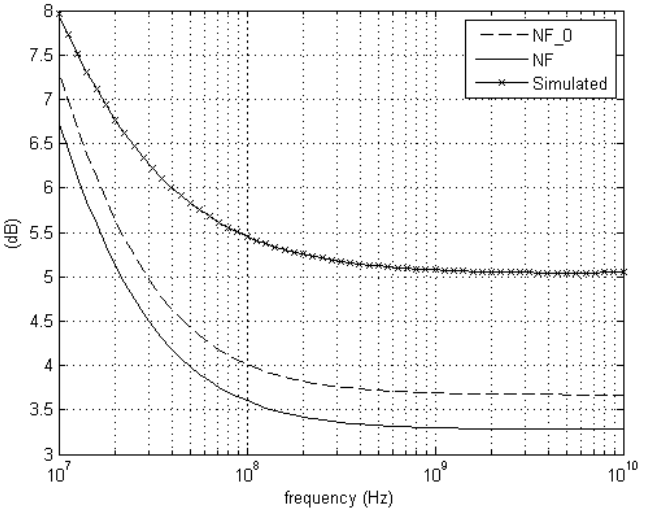


FIGURE 3.21: CG Noise Figure.

Chapter 4

Common Source Stage

The common-source stage (CS) is one of the most used single-stage amplifier topologies, typically used as a voltage or transconductance amplifier. The principal features of this stage are the high input and output impedances and a potential high voltage gain. Since the input impedance cannot be matched to 50 Ω, this circuit is not suitable for a single stage wideband LNA [25].

The CS is used for narrowband LNAs by inserting a source-degeneration inductor between the source of the MOSFET and ground. This provides an effective resistive input without contributing additional noise, and gate inductors can be used to optimize the noise figure. A CS stage connected with the CG stage leads to a balun LNA, which will be studied in next chapter.

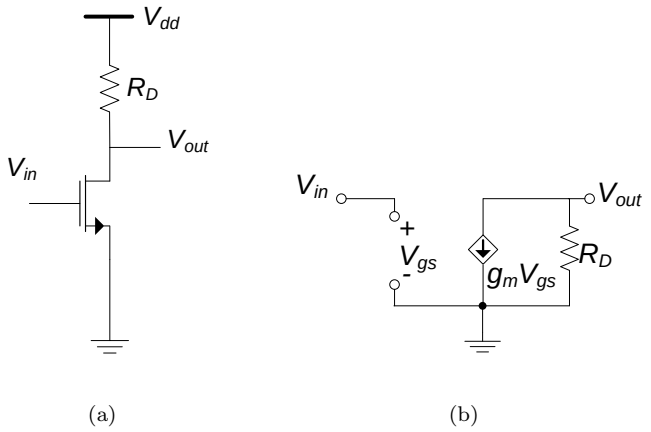
4.1 Theoretical Analysis

As for the CG stage, we derive equations for: input impedance, gain, and noise factor, starting by the simplest transistor model and progressing towards a more complex one including the parasitic capacitances.

4.1.1 Low frequency model neglecting r_o

In the common-source stage (fig. 4.1(a)), the input signal is applied to the gate, which is, physically isolated from the transistor channel, and therefore, for low frequencies the input

impedance is assumed to be infinite. Since the source and the bulk are both connected to the ground, there is no body effect (fig. 4.1(b)).



(a) (b)

FIGURE 4.1: Common-source stage: (a)circuit, (b)small signal model.

Gain

Analyzing the circuit of fig. 4.1(b) we obtain

$$\begin{aligned} V_{out} &= -g_m V_{in} R_D \Leftrightarrow \\ A_{vCS\_0} &= \frac{V_{out}}{V_{in}} = -g_m R_D \end{aligned} \tag{4.1}$$

Noise

The major noise sources are represented in fig. 4.2(a): R_S and R_D thermal noise, V_{n,R_S} and V_{n,R_D}; flicker noise source $V_{n,f}$ and the transistor thermal noise $I_{n,1}$. Fig. 4.2(b) shows the small signal model.

The analysis is performed considering each noise source at once, assuming that all noise sources are uncorrelated, and applying the superposition theorem.

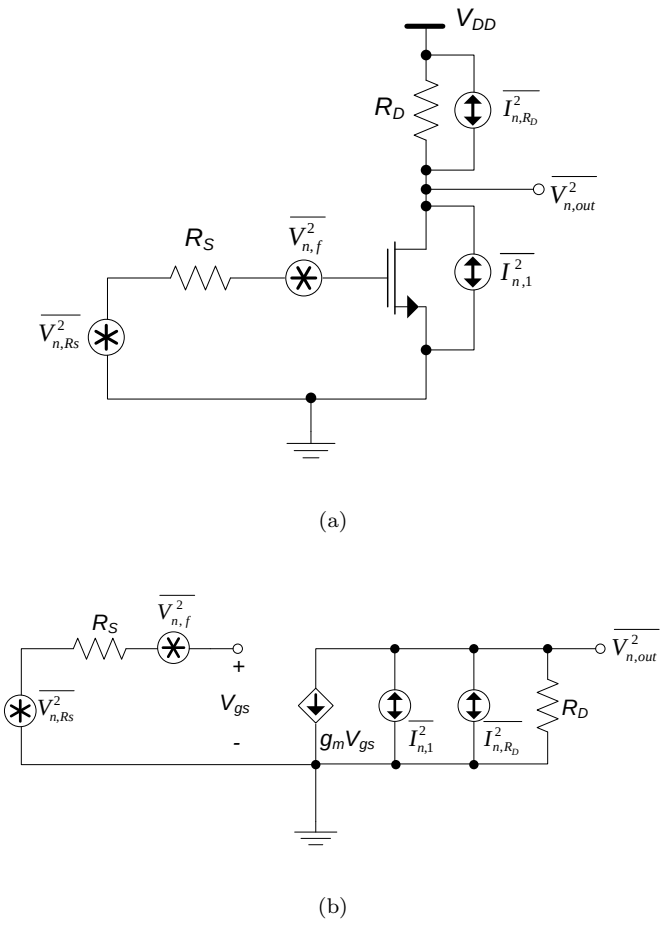


FIGURE 4.2: CS noise sources: (a)circuit, (b)small signal model.

Thermal noise of R_S

The noise due to the source resistor V_{n,R_S} (fig. 4.3) is present at the input. At the output this noise appears multiplied by the CS gain.

In terms of power, the noise at output is,

$$\overline{V^2_{nR_S,out}} = \overline{V^2_{n,R_S}} A^2_{vCS\_0} = 4kTR_S g_m^2 R_D^2 \tag{4.2}$$

Flicker noise

The circuit with the flicker noise source is represented in fig. 4.4. This noise is represented by a voltage source $V_{n,f}$ in series with the gate of the transistor, so the result is the same

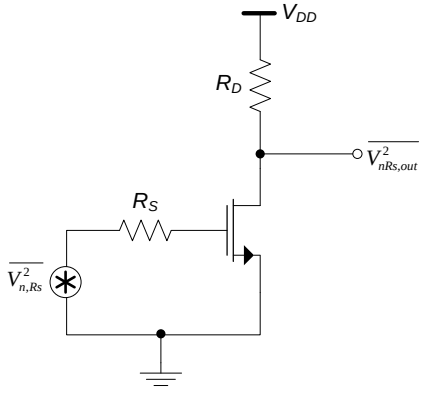


FIGURE 4.3: Source resistor thermal noise.

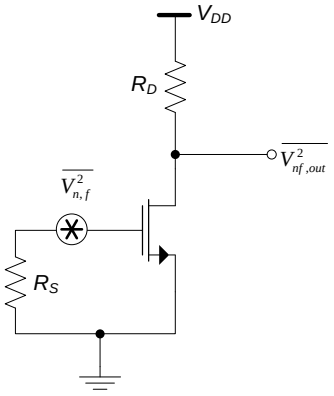


FIGURE 4.4: Flicker noise.

as for the source resistor thermal noise,

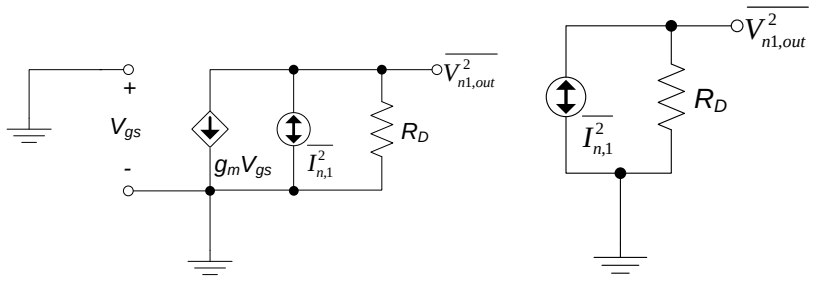
$$\overline{V^2_{nf,out}} = \overline{V^2_{n,f}} A^2_{vCS\_0} = \frac{k_f}{WLc_{ox}f^{\alpha_f}} g_m^2 R_D^2 \tag{4.3}$$

Thermal noise of the transistor

The thermal noise of the transistor is modeled by the current source $I_{n,1}$. We eliminate all other independent sources (fig. 4.5(a)), reducing the equivalent circuit as shown in fig. 4.5(b).

Then the output noise power due to thermal noise is,

$$\overline{V^2_{n1,out}} = \overline{I^2_{n,1}} R_D^2 = 4kT\gamma g_m R_D^2 \tag{4.4}$$



(a) (b)

FIGURE 4.5: CS transistor thermal noise: (a)equivalent circuit, (b)simplified circuit.

Thermal noise of the load resistor R_D

The thermal noise source of the load resistor I_{n,R_D}, which is in parallel with the output, is shown in fig. 4.6.

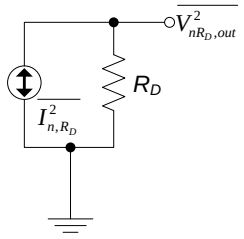


FIGURE 4.6: CS thermal noise of load resistor.

The output noise power is then

$$\overline{V_{nR_D,out}^2} = \overline{I_{n,R_D}^2} R_D^2 = \frac{4kT}{R_D} R_D^2 = 4kTR_D \tag{4.5}$$

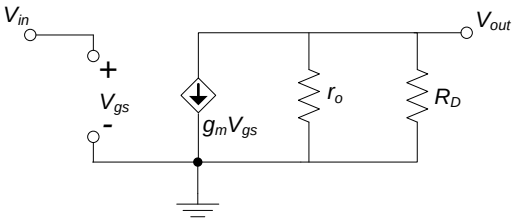
Noise Factor

The noise factor is

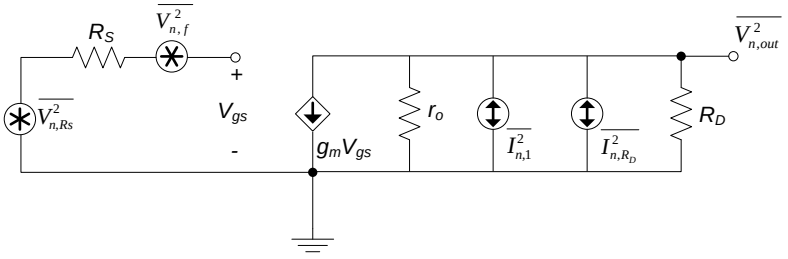
$$\begin{aligned} F &= \frac{\overline{V_{n,out}^2}}{\overline{V_{n,R_S}^2} A_{vCS\_0}^2} = \frac{\overline{V_{nR_S,out}^2} + \overline{V_{nf,out}^2} + \overline{V_{n1,out}^2} + \overline{V_{nR_D,out}^2}}{\overline{V_{n,R_S}^2} A_{vCS\_0}^2} \\ &= 1 + \frac{k_f}{4kTR_S WLc_{ox} f^{\alpha f}} + \frac{\gamma}{R_S g_m} + \frac{1}{R_S R_D g_m^2} \end{aligned} \tag{4.6}$$

4.1.2 Low frequency model with r_o

If the output impedance r_o is included we have the circuit in fig. 4.7(a).



(a)



(b)

FIGURE 4.7: CS model for low frequencies: (a)equivalent circuit, (b) noise model.

Gain

Since r_o is in parallel with the load resistor R_D, the gain is

$$A_{vCS\_1} = -g_m \frac{r_o R_D}{r_o + R_D} \tag{4.7}$$

Noise

The noise model with r_o included is represented in fig. 4.7(b). Since the inclusion of r_o does not introduce any additional noise source because the thermal noise of the transistor is only defined by $I_{n,1}$, the only change, as for the gain, is the replacement of R_D by the parallel of r_o and R_D in the equations of noise from (4.2) to (4.5),

$$\overline{V^2_{nR_S,out}} = 4kTR_S g_m^2 \left(\frac{r_o R_D}{r_o + R_D} \right)^2 \tag{4.8}$$

$$\overline{V_{nf,out}^2} = \frac{k_f}{WLc_{ox}f^{\alpha_f}} g_m^2 \left(\frac{r_o R_D}{r_o + R_D} \right)^2 \tag{4.9}$$

$$\overline{V_{n1,out}^2} = 4kT\gamma g_m \left(\frac{r_o R_D}{r_o + R_D} \right)^2 \tag{4.10}$$

$$\overline{V_{nR_D,out}^2} = \frac{4kT}{R_D} \left(\frac{r_o R_D}{r_o + R_D} \right)^2 \tag{4.11}$$

Thus, the noise factor is,

$$F = 1 + \frac{k_f}{4kTR_S WLc_{ox}f^{\alpha f}} + \frac{\gamma}{R_S g_m} + \frac{1}{R_S R_D g_m^2} \tag{4.12}$$

Regarding the equation obtained, we observe that it is the same result as given in (4.6); hence we can conclude here that the inclusion of r_o in the model does not affect the noise factor.

4.1.3 Model with parasitic capacitances

In the complete model (fig. 4.8), there are the parasitic capacitances at the gate-source, gate-drain, and drain-bulk junctions, C_{gs}, C_{gd}, and C_{db}, respectively. The capacitance between source and bulk does not appear because these nodes are both connected to ground.

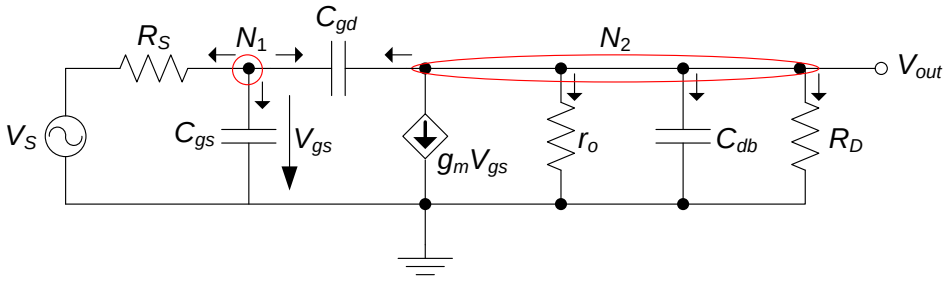


FIGURE 4.8: CS equivalent circuit with parasitic capacitances.

Gain

Analyzing we derive the following equations,

- At node N_1:
$$\frac{V_{gs} - V_S}{R_S} + V_{gs}sC_{gs} + (V_{gs} - V_{out})sC_{gd} = 0 \tag{4.13}$$
- At node N_2:
$$g_m V_{gs} + \frac{V_{out}}{r_o} + V_{out}sC_{db} + \frac{V_{out}}{R_D} + (V_{out} - V_{gs})sC_{gd} = 0 \tag{4.14}$$

Solving (4.14) in order to V_{gs} we obtain,

$$V_{gs} = -\frac{V_{out}(\frac{1}{r_o} + sC_{db} + \frac{1}{R_D} + sC_{gd})}{g_m - sC_{gd}} \tag{4.15}$$

Substituting (4.15) on (4.13),

$$A_v(s) = \frac{V_{out}}{V_S}(s) = \frac{(sC_{gd} - g_m)r_o R_D}{as^2 + bs^2 + c} \tag{4.16}$$

where,

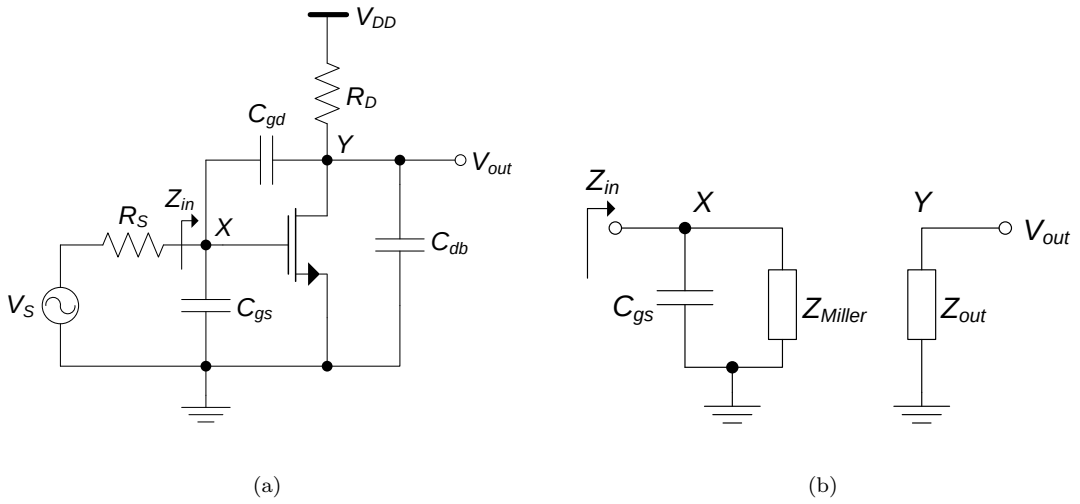
$$\begin{aligned} a &= r_o R_S R_D(C_{db}C_{gs} + C_{db}C_{gd} + C_{gd}C_{gs}) \\ b &= R_S R_D(C_{gs} + C_{gd}) + r_o R_D(C_{db} + C_{gd}(1 + g_m R_S)) + r_o R_S(C_{gs} + C_{gd}) \\ c &= r_o + R_D \end{aligned}$$

From (4.16) we obtain the CS gain,

$$A_{vCS}(s) = \frac{(sC_{gd} - g_m)r_o R_D}{sr_o R_D(C_{db} + C_{gd}) + r_o + R_D} \tag{4.17}$$

Input impedance

In the previous sections, it was assumed that the input impedance was infinite, but now there are the parasitic capacitances, as represented in fig. 4.9(a).



(a) (b)

FIGURE 4.9: Application of Millers theorem: (a)CS with parasitic capacitances, (b)Miller's equivalent circuit.

By using the Miller's theorem the circuit in fig. 4.9(b) is obtained (see Appendix A). With

$$Z_{Miller} = \frac{\frac{1}{sC_{gd}}}{1 - A} \tag{4.18}$$

where A is the circuit gain ($\frac{V_Y}{V_X}$). The CS gain is frequency dependent, but as an approximation the low frequencies gain (4.7) is considered. Substituting (4.7) on (4.18) we have,

$$Z_{Miller} = \frac{r_o + R_D}{sC_{gd}(r_o + R_D + g_m r_o R_D)} \tag{4.19}$$

The input impedance is

$$Z_{inCS} = (\frac{1}{sC_{gs}} // Z_{miller}) = \frac{r_o + R_D}{s(C_{gs}(r_o + R_D) + C_{gd}(r_o + R_D + g_m r_o R_D))} \tag{4.20}$$

4.2 Circuit Implementation and Biasing

The CS amplifier is analyzed in this chapter as a single stage, but it is aimed to be used combined with the CG to realize a balun configuration, so the dimensions and biasing

take into account the CG stage analyzed in the previous chapter. Based on the CG, there are some guidelines to be followed to biasing the CS stage, which are:

- The DC output voltage must be the same to avoid common mode mismatch; therefore, for the same value of load resistor (100 Ω) the drain current should be equal, i.e, $I_D = 2\ mA$
- The gain must be the same as that of the CG stage, so using (4.1) as approximation we set $g_{m\_CS} \approx g_{m\_CG} + g_{mb\_CG}$

To fulfill these requirements, W and V_{GS} parameters must be adjusted. Here, V_{GS} is imposed in the signal source by a DC offset , but later this voltage will be provided by the source terminal of CG and can be properly tuned by adjusting V_{bias} voltage. Hence, the DC parameters used for biasing the CS stage are listed on table 4.1.

W (µm)	L (µm)	g_m (mS)	V_{DS} (V)	V_{dsat} (mV)	V_{GS} (mV)
36	120	20.88	1	116	460

TABLE 4.1: Common-Source DC operating point parameters.

4.3 Simulations and Validation

Considering the DC operating point specified on table 4.1, we can validate the results for input impedance, gain, and NF. For the input impedance, only the complete model is considered since in the low frequencies approach it is assumed to be a high impedance, which is confirmed by simulation, as shown in fig. 4.10. For frequencies above 10 GHz the input impedance in module tends fastly to 0. By inspection we see that the real part is close to 0, as expected. Looking at the reactance, the theoretical equation is accurate to define the input impedance, which means that miller's approximation is adequate in this case.

The CS stage gain A_{vCS} (fig. 4.11) is well characterized by the equation (4.17); it is constant for a wide frequency range (more than 10 GHz). Thus, the low frequencies approximation of (4.7) can be used instead of (4.1) as good starting point in the design.

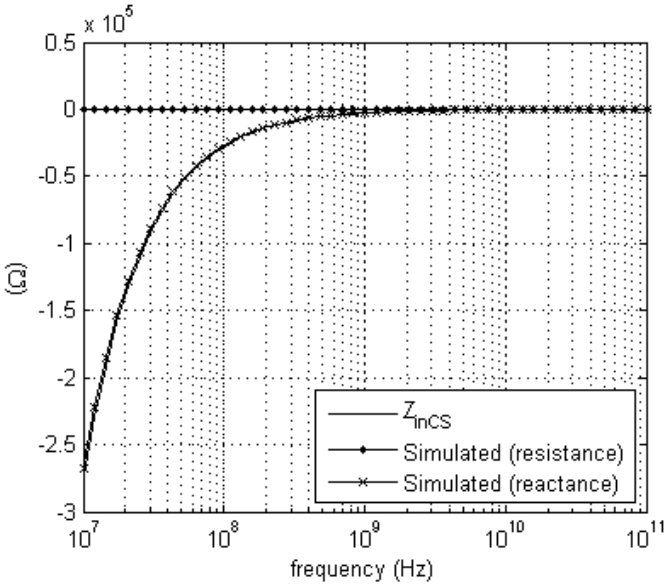


FIGURE 4.10: CS input impedance.

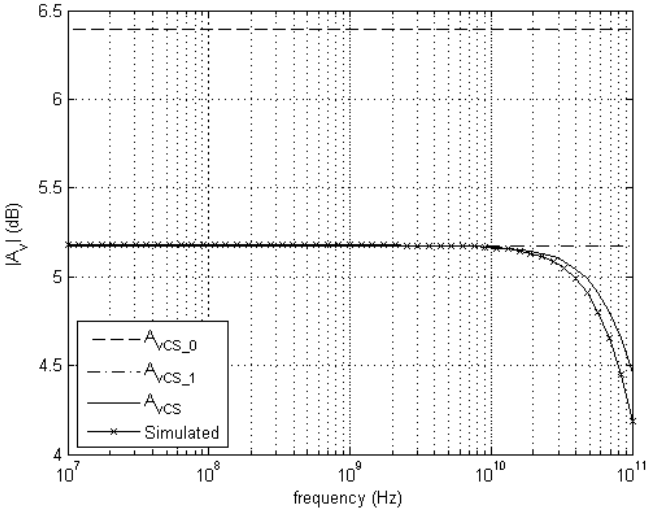


FIGURE 4.11: CS stage gain.

Fig. 4.12 presents the theoretical noise figure with $\gamma = 1$, and the simulated one.

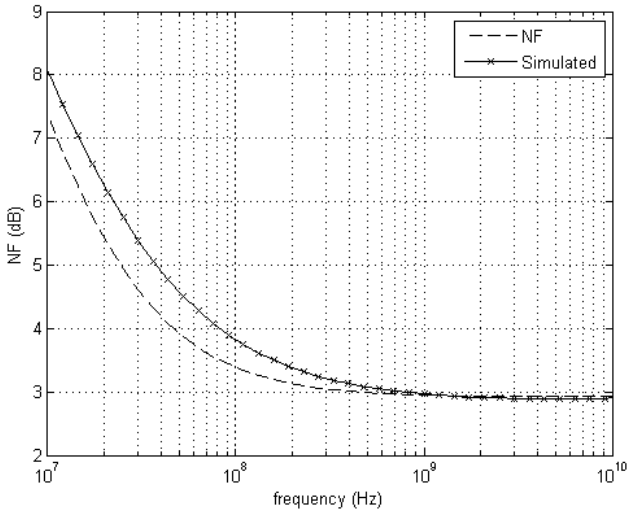


FIGURE 4.12: CS Noise Figure.

Chapter 5

Low Noise Amplifier

A single input to differential output (balun) wideband LNA has been proposed, based on a common source and common gate amplifiers[24]. This topology is chosen to integrate a compact RF receiver in which the LNA is coupled directly to a differential mixer without the need for a separate balun or impedance matching networks. The differential LNA is suitable to achieve a higher gain, reducing the noise effect of the subsequent stages, and also improves the linearity, because it is less sensitive to even-order harmonic distortion. This topology includes noise cancelation, which is a major advantage with respect to other LNA architectures.

This chapter is organized as follows: a theoretical analysis is made and the principal equations for LNA characterization are derived, based on the previous study of CG and CS stages, and are then validated trough simulation. A MOSFET-only LNA with gain optimization is also presented, and its performance is compared with other types of existing LNAs.

5.1 Theoretical Analysis

The proposed LNA is represented in fig. 5.1, with illustration of its operation principle. The output signal of the CG stage has the same sign as the input signal, whereas the CS output signal is in opposition, leading to balun operation for the signal. The thermal noise produced by the CG stage (M_1), represented by the current source I_{n1}, originates a noise voltage at the input $V_{n,in}$ since it flows into R_S. This noise voltage appears in

opposition at the CG output $V_{n,out1}$, and also appears in phase at the CS output $V_{n,out2}$: thus, the CG thermal noise is canceled. The gain matching of the two stages is critical since the same gain is needed for full noise cancelation.

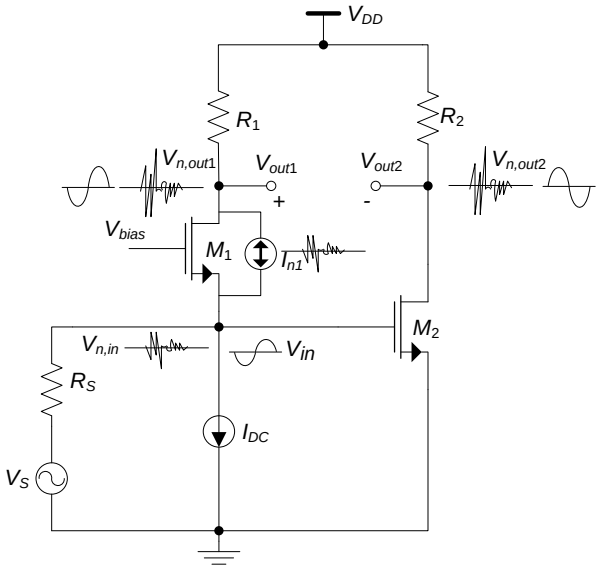


FIGURE 5.1: Balun LNA with noise canceling [24].

In the following sections, the circuit equations are derived for different levels of approximation.

5.1.1 Input Impedance

The LNA input impedance is the parallel of those of the CG and CS stages,

$$Z_{inLNA} = (Z_{inCG}//Z_{inCS}) \tag{5.1}$$

If it is assumed that the CS input impedance is very high,

$$Z_{inLNA\_a} = Z_{inCG} = \frac{sC_L r_{o1} R_1 + r_{o1} + R_1}{as^2 + bs + c} \tag{5.2}$$

where,

$$a = C_S C_L r_{o1} R_1$$
$$b = C_S(r_{o1} + R_1) + C_L R_1(r_{o1}(g_{m1} + g_{mb1}) + 1)$$
$$c = r_{o1}(g_{m1} + g_{mb1}) + 1$$

and if the low frequency approximation is considered(3.33),

$$Z_{inLNA\_b} = Z_{inCG\_1} = \frac{r_{o1} + R_1}{r_{o1}(g_{m1} + g_{mb1}) + 1} \tag{5.3}$$

5.1.2 Gain

Since the output signal is differential, and V_{out1} and V_{out2} are the CG and CS outputs, from (3.55) and (4.17), the differential gain is given by

$$A_{vLNA\_a} = \frac{R_1(r_{o1}(g_{m1} + g_{mb1}) + 1)}{sC_L r_{o1} R_1 + r_{o1} + R_1} - \frac{(sc_{gd2} - g_{m2}) r_{o2} R_2}{s r_{o2} R_2(c_{db2} + c_{gd2}) + r_{o2} + R_2} \tag{5.4}$$

and if the low frequencies approximation is used (3.30 and 4.7),

$$A_{vLNA\_b} = \frac{R_1(1 + r_{o1}(g_{m1} + g_{mb1}))}{R_1 + r_{o1}} + g_{m2}\frac{r_{o2} R_2}{r_{o2} + R_2} \tag{5.5}$$

Assuming an infinite transistors output resistance r_o, we can simplify (5.5) into,

$$A_{vLNA\_c} = (g_{m1} + g_{mb1}) R_1 + g_{m2} R_2 \tag{5.6}$$

To achieve noise cancelation and balun operation (converting a single-ended input to a differential output) the CG and CS stages gain should be equal. Considering $r_{o1}(g_{mb1} + g_{m1}) >> 1$ and for the same current and length (L) of M_1 and M_2, $r_{o1} \approx r_{o2}$, and chosing $g_{m1} + g_{mb1} = g_{m2} = g_m$ and $R_1 = R_2 = R_D$, we obtain from (5.5),

$$A_{vLNA\_d} = \frac{2 r_o R_D g_m}{r_o + R_D} \tag{5.7}$$

5.1.3 Noise Factor

The total noise power at LNA output will be given by the sum of the noise power at each output stage. For simplicity, the noise generated by the source resistor(R_S) is neglected first, but its effect is added in the final equation. This noise at the LNA input according to fig. 5.2, is given by:

$$V_{nR_S,in} = \alpha V_{n,R_S} \tag{5.8}$$

where,

$$\alpha = \frac{Z_{in}}{Z_{in} + R_S} = \frac{r_{o1} + R_1}{r_{o1} + R_1 + R_S(r_{o1}(g_m + g_{mb1}) + 1)} \tag{5.9}$$

assuming that the input impedance(Z_{in}) is approximately that of the CG stage as in (5.3).

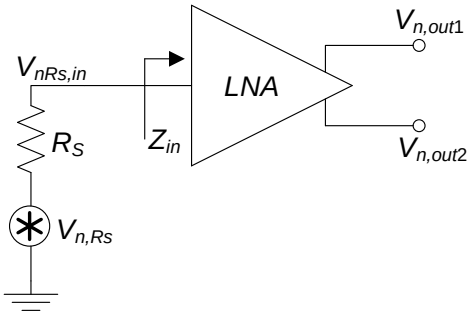


FIGURE 5.2: LNA input noise due to source resistor.

The noise analysis starts by the determination of the noise at each stage individually, due to flicker and thermal noise of the transistors and load resistor. At the CG output, the noise power originated by M_1 and R_1 can be found as:

$$\overline{V^2_{nf,outCG}} = \frac{(g_{m1} r_{o1} R_1)^2}{(r_{o1} + R_1)^2} \frac{k_f}{c_{ox} W_1 L_1 f^{\alpha_f}} \tag{5.10}$$

$$\overline{V^2_{n1,outCG}} = 4kT\gamma g_{m1} \left(\frac{r_{o1} R_1}{r_{o1} + R_1} \right)^2 \tag{5.11}$$

$$\overline{V^2_{nR_1,outCG}} = \frac{4kT R_1 r^2_{o1}}{(r_{o1} + R_1)^2} \tag{5.12}$$

and at the CS output the noise power generated by M_2 and R_2 is:

$$\overline{V^2_{nf,outCS}} = \frac{(g_{m2}r_{o2}R_2)^2}{(r_{o2}+R_2)^2}\frac{k_f}{c_{ox}W_2L_2f^{\alpha_f}} \tag{5.13}$$

$$\overline{V^2_{n2,outCS}} = 4kT\gamma g_{m2}\left(\frac{r_{o2}R_2}{r_{o2}+R_2}\right)^2 \tag{5.14}$$

$$\overline{V^2_{nR_2,outCS}} = \frac{4kTR_2r^2_{o2}}{(r_{o2}+R_2)^2} \tag{5.15}$$

Additionally, the noise contributions by the CG stage will appear at the CS output and vice-versa. To evaluate this effect, the noise generated by the CG can be input referred, divided by the CG gain (3.30), and then be amplified by the CS stage (4.7):

$$\overline{V^2_{nfCG,outCS}} = \frac{\overline{V^2_{nf,outCG}}}{A^2_{vCG}}A^2_{vCS} = \frac{(g_{m1}r_{o1}R_1)^2(g_{m2}r_{o2}R_2)^2}{\left[r_{o1}(g_{m1}+g_{mb1})+1\right]^2R_1^2(r_{o2}+R_2)^2}\frac{k_f}{c_{ox}W_1L_1f^{\alpha_f}} \tag{5.16}$$

$$\overline{V^2_{n1,outCS}} = \frac{\overline{V^2_{n1,outCG}}}{A^2_{vCG}}A^2_{vCS} = 4kT\gamma g_{m1}\left(\frac{r_{o1}R_1}{(r_{o1}(g_{m1}+g_{mb1})+1)R_1}\right)^2\left(\frac{g_{m2}r_{o2}R_2}{r_{o2}+R_2}\right)^2 \tag{5.17}$$

$$\overline{V^2_{nR_1,outCS}} = \frac{\overline{V^2_{nR_1,outCG}}}{A^2_{vCG}}A^2_{vCS} = \frac{4kTR_1r^2_{o1}}{((r_{o1}(g_{m1}+g_{mb1})+1)R_1)^2}\left(\frac{g_{m2}r_{o2}R_2}{r_{o2}+R_2}\right)^2 \tag{5.18}$$

The same situation occurs for the noise generated by the CS, which appears at the CG output as:

$$\overline{V^2_{nfCS,outCG}} = \frac{\overline{V^2_{nf,outCS}}}{A^2_{vCS}}A^2_{vCG} = \left(\frac{(r_{o1}(g_{m1}+g_{mb1})+1)R_1}{r_{o1}+R_1}\right)^2\frac{k_f}{c_{ox}W_2L_2f^{\alpha_f}} \tag{5.19}$$

$$\overline{V^2_{n2,outCG}} = \frac{\overline{V^2_{n2,outCS}}}{A^2_{vCS}}A^2_{vCG} = 4kT\gamma\frac{1}{g_{m2}}\left(\frac{(r_{o1}(g_{m1}+g_{mb1})+1)R_1}{r_{o1}+R_1}\right)^2 \tag{5.20}$$

$$\overline{V_{nR_2,outCG}^2} = \frac{\overline{V_{nR_2,outCS}^2}}{A_{vCS}^2} A_{vCG}^2 = \frac{4kT}{R_2 g_{m2}^2} \left(\frac{(r_{o1}(g_{m1} + g_{mb1}) + 1)R_1}{r_{o1} + R_1} \right)^2 \tag{5.21}$$

The total noise power at the differential output is given by the sum of all the noise power contribution available at the output, assuming that the noise sources are uncorrelated:

$$\overline{V_{n,outCG}^2} = \overline{V_{nf,outCG}^2} + \overline{V_{nfCS,outCG}^2} + \overline{V_{n2,outCG}^2} + \overline{V_{nR_1,outCG}^2} + \overline{V_{nR_2,outCG}^2} \tag{5.22}$$

$$\overline{V_{n,outCS}^2} = \overline{V_{nf,outCS}^2} + \overline{V_{nfCG,outCS}^2} + \overline{V_{n2,outCS}^2} + \overline{V_{nR_2,outCS}^2} + \overline{V_{nR_1,outCS}^2} \tag{5.23}$$

The thermal noise voltage produced by M_1 appears in phase at the two outputs, consequently this term is full canceled according to properly cancelation conditions. To determine the LNA noise factor, the effect of R_S is now introduced, resulting in:

$$F = \frac{\alpha^2(\overline{V_{n,R_S}^2} A_{v,LNA}^2 + \overline{V_{n,outCG}^2} + \overline{V_{n,outCS}^2})}{\alpha^2 \overline{V_{n,R_S}^2} A_{v,LNA}^2} = 1 + \frac{\overline{V_{n,outCG}^2} + \overline{V_{n,outCS}^2}}{\overline{V_{n,R_S}^2} A_{v,LNA}^2} \tag{5.24}$$

and if is assumed the same approach applied for noise cancellation in (5.7), the simplified noise factor is given by,

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S g_m^2 c_{ox} f^{\alpha_f}} \left(\frac{g_{m1}^2}{W_1 L_1} + \frac{g_m^2}{W_2 L_2} \right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S R_D g_m^2} \tag{5.25}$$

5.2 Circuit Implementation and Validation

The LNA is designed for 50 Ω input impedance using equation (3.5) as a first approximation, fixing the transconductance of M_1, which is biased with 2 mA. The load resistances (R_1,R_2) are about 200 Ω, to give a DC output level that avoids signal limitation and gives enough voltage headroom to keep M_1 and M_2 in saturation. Then, g_{m1} is adjusted to fulfill the matching requirements by increasing the transistor width (W_1) using (5.3), while the length (L) is the minimum value allowed by the technology. The DC voltage V_{bias} is used to adjust the DC current of M_2 to the same value as that of M_1 and then g_{m2} is chosen so that the gain of the two stages given by (3.30) and (4.7) have the same value.

This first design already produces noise cancelation and provides reasonable gain for the LNA, but there is little freedom to maximize the gain. Moreover, the noise factor can be

reduced more effectively by increasing the transconductance g_m than the load resistor R_D [24]. Since the thermal noise of M_1 is canceled and its transconductance must to be fixed to maintain the input matching, an alternative design procedure is to increase g_{m2} and reduce the value of R_2 in the same proportion to maintain the gain (assuming the simple equation $g_m R$ for the gain).

Design		I_D(mA)	$R(\Omega)$	g_m(mS)	W(µm)	L(µm)	V_{DSAT}(mV)
$R_1 = R_2$	M_1	2	200	24.5	72	0.12	120.1
	M_2	2	200	27.2	90	0.12	109.3
$R_1 \neq R_2$	M_1	2	200	24.5	72	0.12	120.1
	M_2	4	100	53.3	172.8	0.12	110.7

TABLE 5.1: LNA parameters.

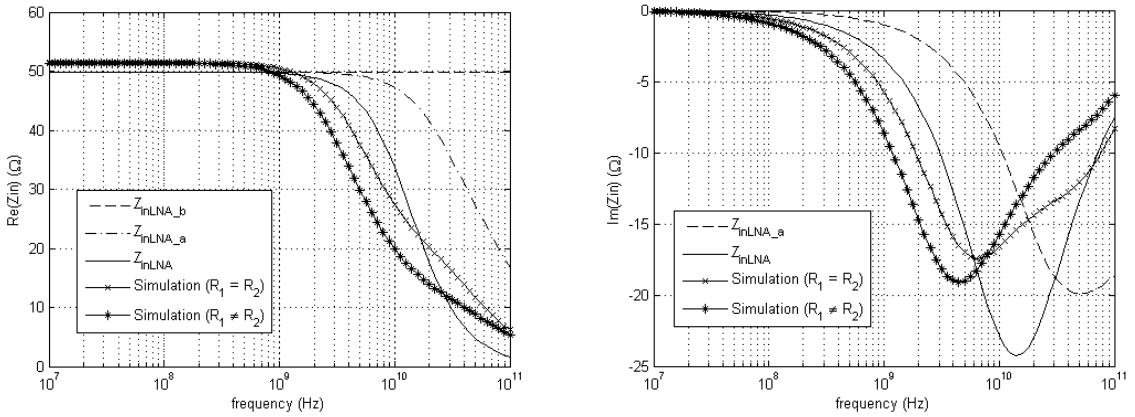
Using this alternative leads to a new circuit design, g_{m2} is increased by a factor of 2 and R_2 is reduced to 100 Ω, to improve of the noise factor. The final dimensions and parameters for the two cases are shown in table 5.1, with a bias voltage (V_{bias}) of 940 mV. The results for both designs are further compared and discussed.

Simulation Results

To validate the equations obtained previously for the LNA performance parameters, and to find out the required level of approximation, a comparison is made with simulation results. The values used to obtain the theoretical equations correspond to the first design where $R_1 = R_2$, but, they are still applicable for the case where the load resistors are different with the proper adjustment.

The real part of the input impedance is constant up to 2.5 GHz, and the imaginary part starts to be significant above 1 GHz as shown in figs. 5.3(a) and 5.3(b), so the input matching must be designed carefully for wideband applications, which needs higher operating frequencies. Equation (5.3) can be used for this purpose, after assure that the required bandwidth is achieved.

The voltage gain with both designs achieves 18 dB (fig. 5.4) almost constant up to 3 GHz. With the first design the gain loss is less than 3 dB at 10 Ghz, where as for the second design the bandwidth decreases considerably, by about 4 GHz of difference at the -3 dB limit.



(a) (b)

FIGURE 5.3: LNA Input Impedance: (a)Real part, (b)Imaginary part.

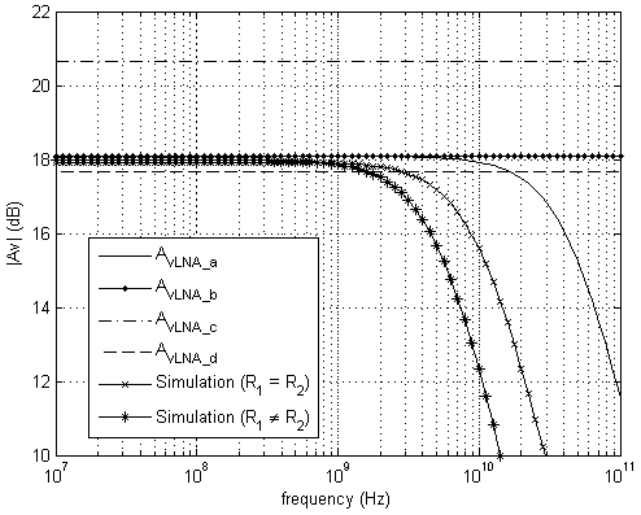


FIGURE 5.4: LNA Gain.

This is justified considering that the CS has a dominant pole that can be found from (4.17) as:

$$|\omega_p| = \frac{r_{o2} + R_2}{r_{o2} R_2 (c_{db2} + c_{gd2})} = \frac{1}{R_2 (c_{db2} + c_{gd2})} + \frac{1}{r_{o2} (c_{db2} + c_{gd2})} \tag{5.26}$$

The parasitic capacitances are proportional to the transistor width, which in the second design is practically doubled. The first term of (5.26) remains constant because R_2 is reduced to a half, but the second term is increased.

According to fig. 5.5, the LNA has a noise figure less than 2.5 dB from 100 MHz to 10

GHz. The simulations show that the noise excess factor (γ) is between 1 and 2 to take into account short channel characteristics. By simulation, we confirm that the second design has lower noise figure, but the improvement is less than 0.5 dB in the band of interest. So, we confirm by simulations that equations (5.2),(5.5) and (5.25) are valid and accurate for the LNA design.

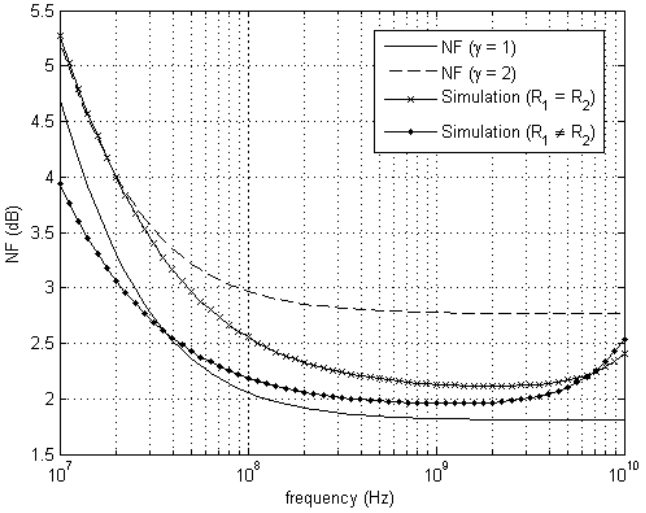


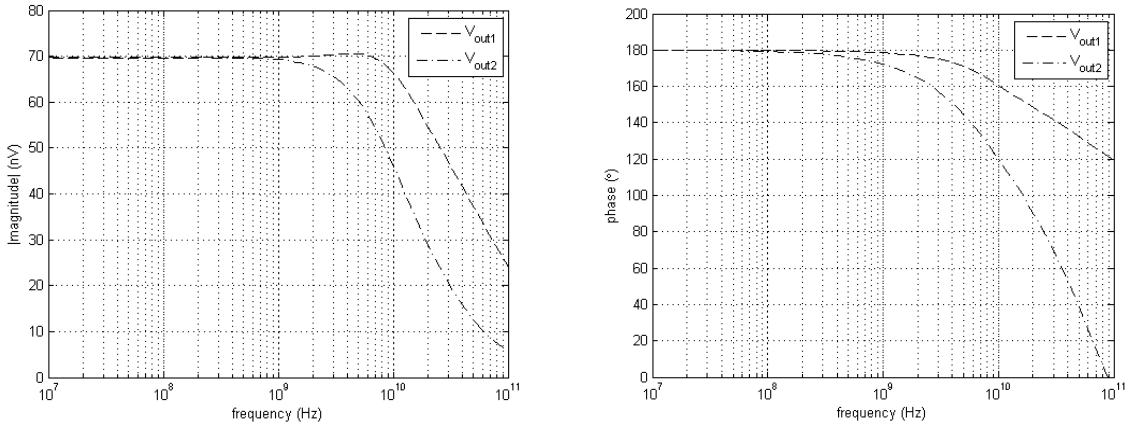
FIGURE 5.5: LNA Noise Figure.

To figure out if the thermal noise of M_1 is properly canceled, a current source is placed in parallel with M_1 to simulate the thermal noise. The noise voltage is effectively canceled if the outputs have the same amplitude and phase: as shown in figs. 5.6(a) and 5.6(b) the noise is fully canceled until 1 GHz; above that frequency the gain and phase start to be unbalanced and the noise is only partially canceled.

In summary, two different designs were presented for the same input matching and gain. The first design has higher bandwidth and less area and power. The second design has lower noise figure but the improvement is not very significant. For applications that demand low area and low power, which is one of the motivations for this work, the first design is the best choice.

5.3 MOSFET-Only Low Noise Amplifier

In the MOSFET-only LNA (fig. 5.7) the load resistors are replaced by PMOS transistors (M_3,M_4) operating in the triode region, which are modeled ideally by a resistor between



(a) (b)

FIGURE 5.6: Frequency response from M_1 noise source to the outputs: (a)magnitude , (b)phase.

the drain and source, $r_{ds} = 1/g_{ds}$ where g_{ds} is the channel conductance. To make a comparison with the LNA with load resistors, r_{ds} is dimensioned to have the same resistance value of 200 Ω. The circuit is biased with a V_{bias} of 935 mV, and the dimensions and parameters are shown in table 5.2.

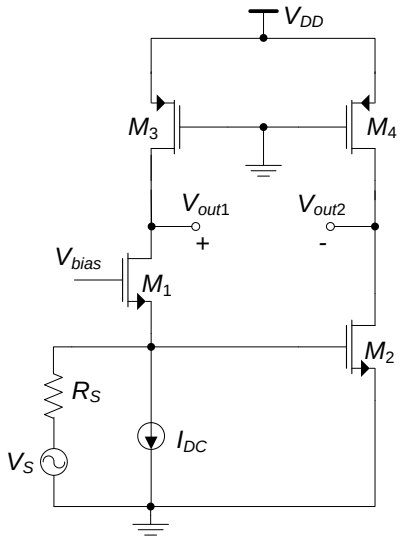


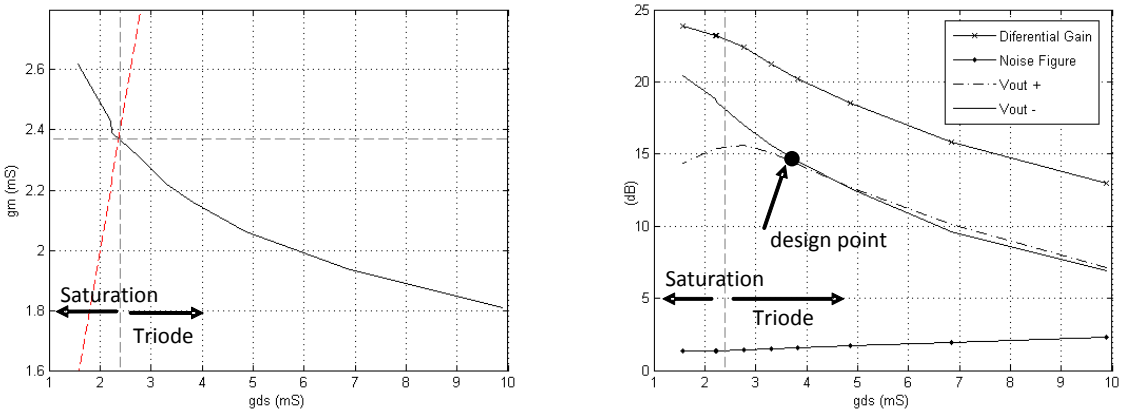
FIGURE 5.7: MOSFET-Only LNA.

Once the resistors are replaced by MOSFETs it becomes possible to optimize the initial design, as explained in the following.

	I_D(mA)	$r_{ds}(\Omega)$	g_m(mS)	W(µm)	L(µm)	V_{DSAT}(mV)
M_1	2	467.3	25.38	75.6	0.12	117.6
M_2	2	581.4	26.73	82.8	0.12	112.8
M_3	2	206.2	2.06	15.3	0.12	−748.7
M_4	2	208.3	2.09	15.3	0.12	−748.9

TABLE 5.2: MOSFET parameters (initial design).

The saturation region is reached when g_m is of about the same magnitude as g_{ds}. A MOS transistor operating in the triode region can be modeled by a resistor if $g_{ds}/g_m > 10$, otherwise the transistor should be modeled by a resistor in parallel with a current source. In this case we can increase the incremental load resistance without increasing the DC voltage drop. This allows the gain to be increased with respect to the circuit with true resistors. By simulations we find the boundary between triode and saturation (fig. 5.8(a)) and we obtain the gains and noise figure as a function of g_{ds} (fig.5.8(b)).



(a) (b)

FIGURE 5.8: LNA gain optimization: (a)Transistor g_m VS g_{ds} characteristic , (b)LNA design point.

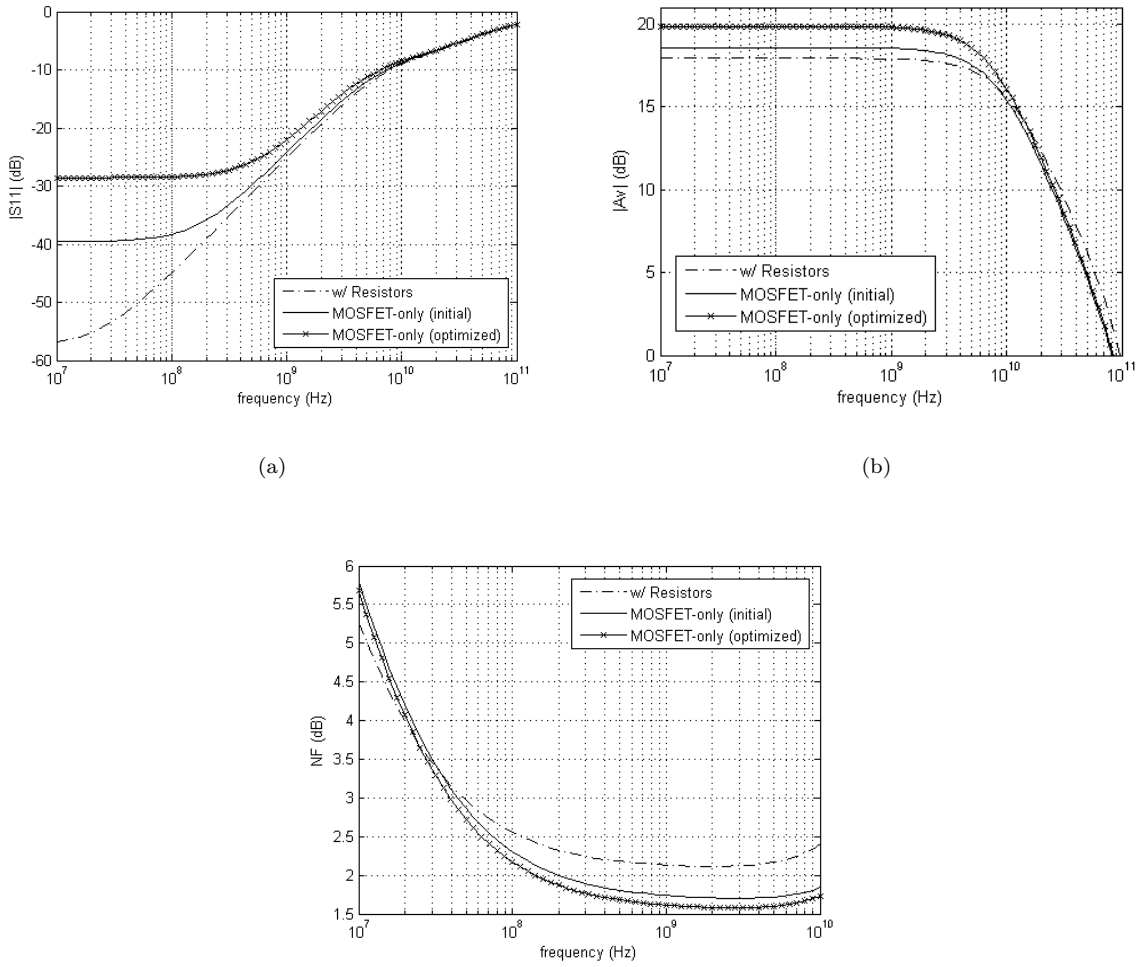
By inspection of fig. 5.8(b) we find that the better operation point is before the single stages gain becomes unbalanced ($g_{ds} \approx 3.8$ mS), which occurs before the load transistors reach saturation. The circuit parameters are given in table 5.3.

	I_D(mA)	$r_{ds}(\Omega)$	g_m(mS)	W(µm)	L(µm)	V_{DSAT}(mV)
M_1	2	448.4	25.23	75.6	0.12	118.1
M_2	2	574.7	26.74	82.8	0.12	113.1
M_3	2	261.8	2.16	13.5	0.12	−750.9
M_4	2	266	2.2	13.5	0.12	−751.2

TABLE 5.3: MOSFET parameters (optimized).

5.3.1 Pre-Layout Simulations

In fig. 5.9, the simulation results for MOSFET-only design (initial and optimized) are presented and are compared with the LNA with resistors.



(a)

(b)

(c)

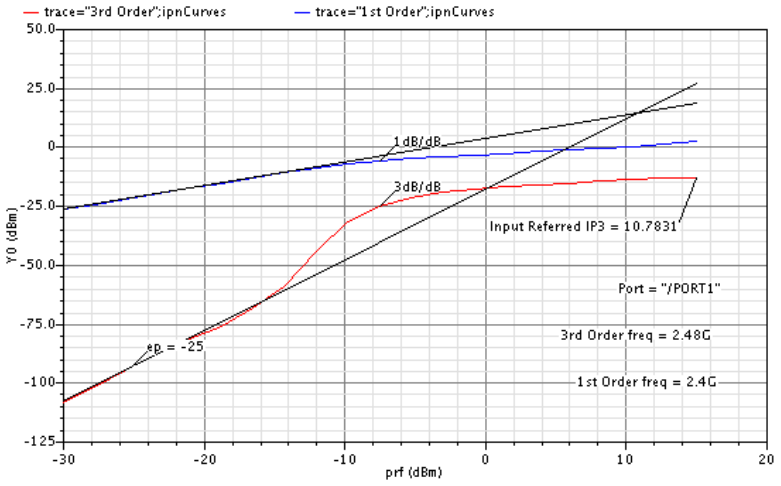
FIGURE 5.9: LNA results comparison: (a)Input impedance , (b)Gain, (c)Noise Figure.

In the MOSFET-only design it is difficult to fix a specific value for the load, since for equal transistors size the r_{ds} has slightly different values (as shown in table 5.3).

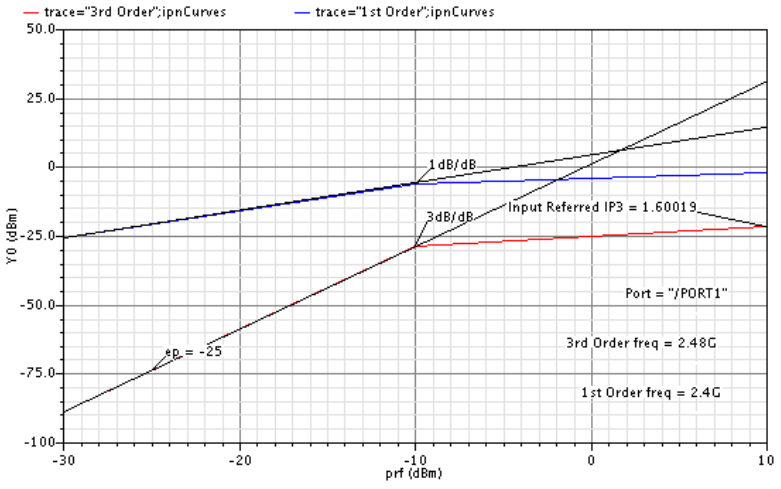
To evaluate the LNA input matching a S-parameter analysis is performed(fig 5.9(a)). In practice the LNA is considered input matched if $|S_{11}| < -10$ dB, which means a bandwidth of 8 GHz for these designs. The MOSFET-only LNA with optimized gain has a gain improvement of 2 dB over the traditional design, as expected, but has less bandwidth due to parasitics of the load transistors. Considering the NF, we obtain less than 2 dB, from 200 MHz up to 10 GHz (0.5 dB reduction), for the MOSFET-only implementation.

If we only consider the MOSFET dominant noise source(thermal) and compare with a resistor thermal noise it is desirable that $4KTg_m < 4KT/R$, assuming $\gamma = 1$ for simplicity. In this particular case, a MOSFET operating in triode region with an equivalent resistance of 200 Ω has a g_m about 2 mS contrasting to the 5 mS for the load resistor, which confirms that for this design the noise introduced by the MOSFETs is lower. This associated with the higher gain of the MOSFET design and the lower flicker noise of PMOS transistors, results in lower noise figure.

Concerning linearity, figs. 5.10(a) and 5.10(b) show the simulated IIP3 for traditional and MOSFET-only optimized design, respectively. Both designs have an IIP3 above 0 dB, but the MOSFET-only approach has poorer linearity, justified by the LNA higher gain and the intrinsic nonlinearities of MOSFET devices.



(a)



(b)

FIGURE 5.10: LNA IIP3: (a)Resistor load , (b)MOSFET-only.

5.3.2 Layout Design and Post-Layout Simulations

In this section we present a circuit layout for the proposed MOSFET-only LNA, and perform a more realistic simulation including the RC parasitics. The results are compared with the schematic simulation results.

The MOSFET-only LNA layout, shown in fig. 5.11, has a die area of 31 x 30.5 µm^2. The technology used has constraints relative to the size, and the maximum number of gate fingers for RF MOSFETs (more gate fingers leads to less gate resistance, thus minimizing the effect of the parasitics). The MOSFET sizes are adjusted to minimize the poly gate resistance, and V_{bias} is tuned to set the same current for M_2 and M_4. The final layout design parameters are listed in table 5.4.

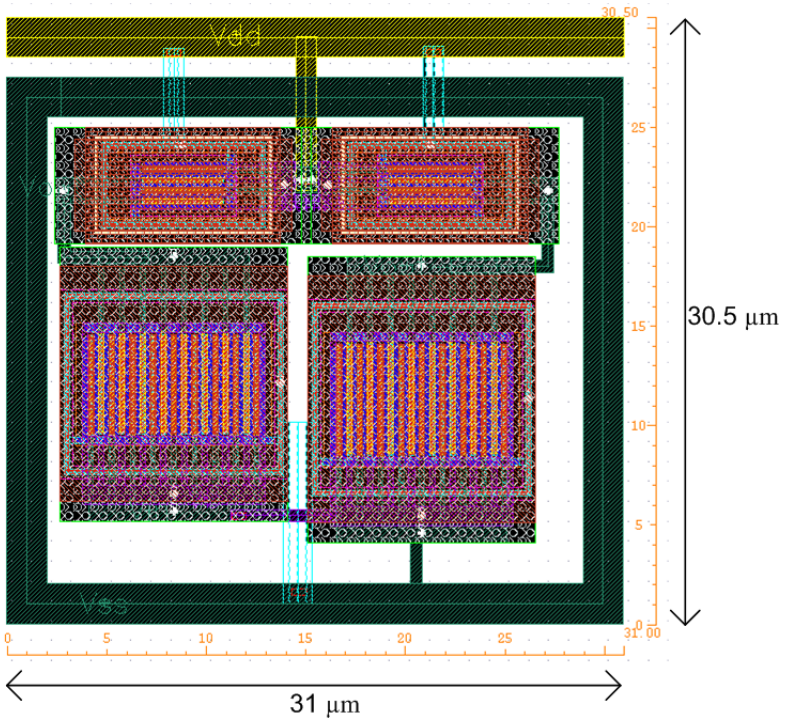


FIGURE 5.11: MOSFET-only LNA layout.

	I_D(mA)	$r_{ds}(\Omega)$	g_m(mS)	W(µm)	L(µm)	V_{DSAT}(mV)
M_1	2	454.5	25.5	80	0.12	115.4
M_2	2	569.8	27.1	89.6	0.12	109.5
M_3	2	252.4	2.1	12.3	0.12	−718
M_4	2	252.2	2.1	12.3	0.12	−718

TABLE 5.4: Post-Layout parameters.

The post-layout simulation results for the main LNA parameters are shown in in figs. 5.12(a)-(c).

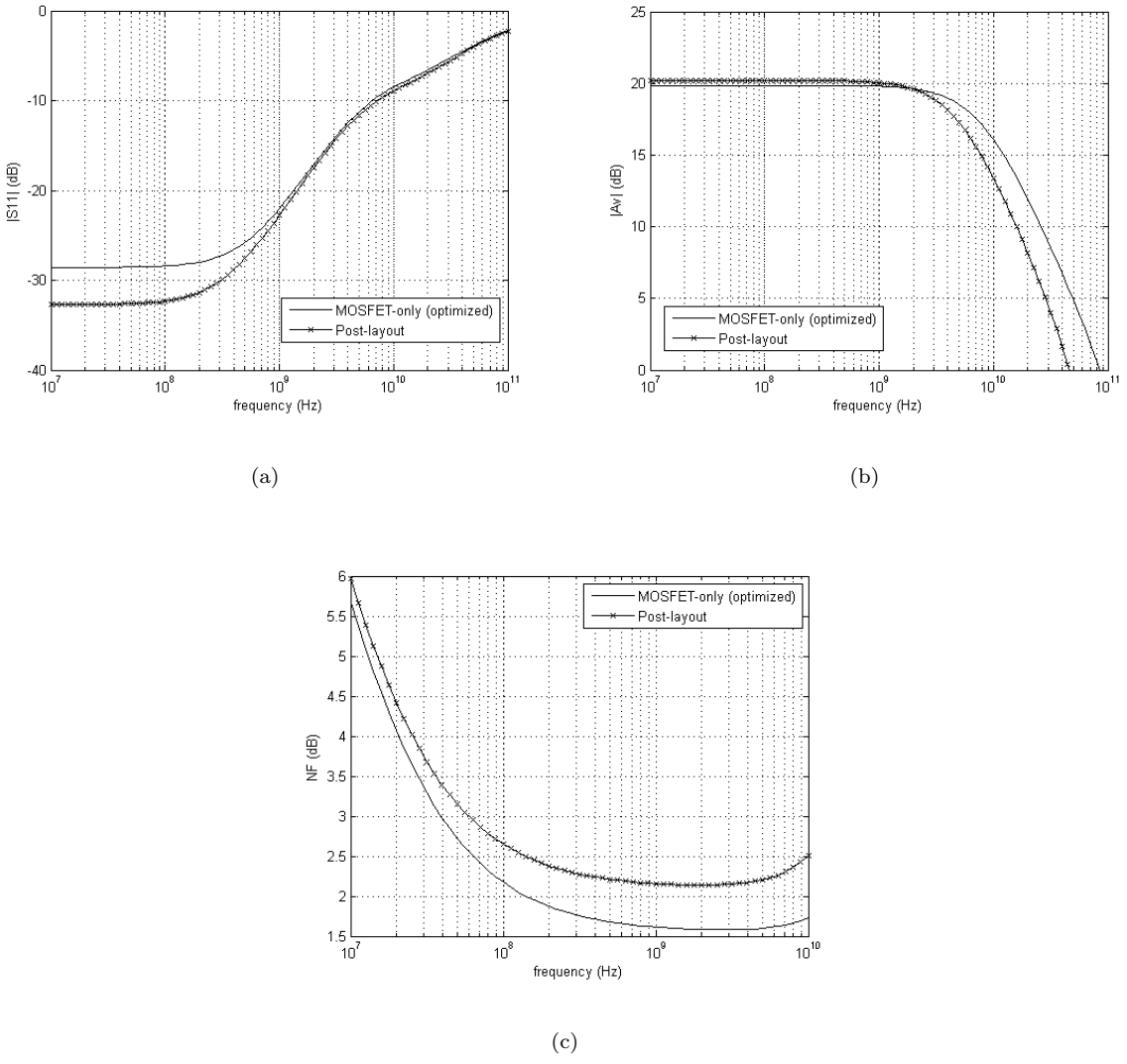
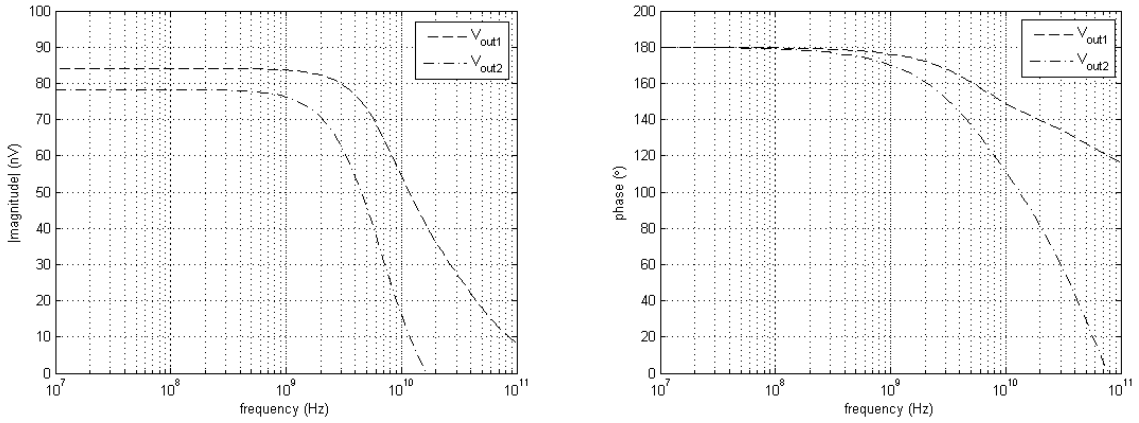


FIGURE 5.12: MOSFET-only LNA post-layout simulation results: (a)Input impedance , (b)Gain, (c)Noise Figure.

The post-layout simulations show that the input matching is not affected: in fact there is a slight improvement, since the equivalent resistance of load transistors is closer to the initial design (fig. 5.12(a)). The gain increases slightly, since the tranconductances of M_1 and M_2 increase, and, consequently, the bandwidth decreases (fig. 5.12(b)), also slightly. The main difference relatively to the pre-layout results is in the NF, which increases by approximately 0.5 dB. This is due to the thermal noise of M_1 being not fully canceled

beyond 1 GHz. This is shown by the frequency response from the M_1 noise source to the outputs of the two stages, shown in figs. 5.13(a) and 5.13(b).



(a) (b)

FIGURE 5.13: Post-layout frequency response from M_1 noise source to the two outputs: (a)magnitude , (b)phase.

If we adjust the layout to obtain full cancelation, there will be mismatches in the gain and DC offsets and, thus, the LNA becomes unbalanced.

5.4 Discussion

Comparing the results of our optimized MOSFET-only design with those for state-of-the-art inductorless LNAs (table 5.5), we can conclude it has the advantages of higher gain and lower noise figure. The drawbacks are a reduction of available bandwidth and the increase of the circuit non-linearity (reduction of IIP3), when compared to the LNA with resistors.

Ref.	Technology (nm)	Bandwith (Ghz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Balun
[24]JSSC 2008[m]	65	$0.2 - 5.2$	$13 - 15.6$	< 3.5	> 0	14	Yes
[26] ISSCC 2006[m]	90	$0.5 - 8.2$	$22 - 25$	< 2.6	$-4/-16$	42	No
[27] JSSC 2006[m]	90	$0.8 - 6$	$18 - 20$	< 3.5	> -3.5	12.5	Yes
[28] TCAS-I 2009[s]	90	$0.1 - 1.9$	20.6	< 2.7	10.8	9.6	Yes
[29] TCAS-II 2007[s]	130	$0.2 - 3.8$	11.2	< 2.8	-2.7	1.9	Yes
This work MOS	130	$0.2 - 5.1$	20.2	< 2.4	3.1	4.8	Yes

Table 5.5: LNA Comparison.

[m] Measurement results
[s] Simulation results

Chapter 6

Conclusions and Future Work

6.1 Conclusions

Nowadays, the demand for mobile and portable equipment has led to a large increase in wireless communication applications. In order to achieve full integration and low cost, modern receivers, require inductorless circuits. The LNA, which is a key block in the design of such receivers, was investigated in this thesis.

In this work a MOSFET-only implementation of a balun LNA was presented, based on the combination of a common-gate and a common-source stage. We have derived equations for gain, input matching, and noise figure, which were validated through simulation for a wide frequency range. In the MOSFET-only LNA, the replacement of resistors by transistors, reduces the area and cost, and minimizes the effect of process and supply variations and of mismatches [6].

This new approach adds a new degree of freedom, which can be used to optimize the LNA gain and minimize the noise figure, since we can obtain a higher gain than with resistors for the same DC voltage drop. As a drawback, the distortion increases, which can be seen by the decrease of the IIP3 value.

Simulation results of a circuit implemented in a 130 nm CMOS technology are presented. For comparison, we also show the performance of a conventional LNA with resistors. Both circuits have the same power consumption of 4.8 mW. For the MOSFET-only LNA we obtain a gain improvement of 2 dB, and the NF is below 2.4 dB.

6.2 Future Work

Through the realization of this work, some space for further improvement was found. The following topics are left for future work, since they fall outside the scope of this thesis.

In chapter 5, the MOSFET-only gain was found to be dependent on the equivalent resistance of the load PMOS transistors in triode region, which can be varied by changing the gate bias voltage, resulting in a variable gain LNA.

In a low-voltage fully integrated CMOS receiver, which uses a co-design strategy for LNA, mixer, and oscillator, a narrowband single-ended LNA is used [30]. This LNA has 15 dB of gain, 2.7 dB of noise figure at 900 MHz and a power consumption of 9 mW. As future work, it is proposed to replace of the narrowband LNA by the MOSFET-only implementation in a co-design perspective. This solution will introduce wideband and fully differential features, with direct coupling to the mixer input, avoiding the need of a balun. It is expected that a significant improvement in gain, noise figure, power, and cost, may be obtained.

Since the work in this thesis is only theoretical and by simulation, future work should validate the results by measurements on a test-circuit.

Appendix A

Miller's Theorem

Consider an arbitrary network where two nodes are interconnected by an impedance Z (fig. A.1(a)). Miller's theorem states that impedance Z can be replaced by two impedances, Z_1 connected between node X and ground and Z_2 between node Y and ground, as shown in fig. A.1(b) [31].

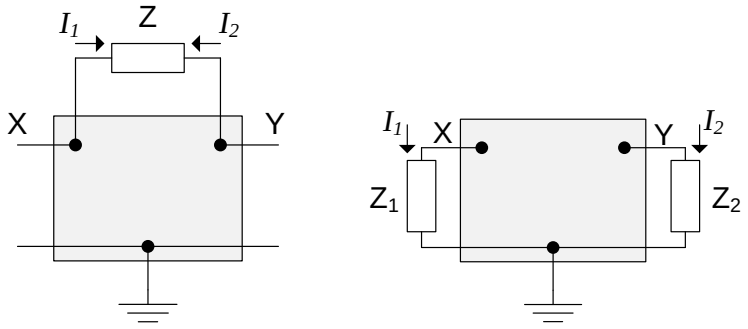


FIGURE A.1: Miller's theorem application

In Miller's theorem is assumed that the ratio $\frac{V_Y}{V_X}$ is known and denoted here by A. For the two circuits to be equivalent, the current that flows into Z from X to Y must be the same that flows trough Z_1. Thus,

$$\frac{V_X - V_Y}{Z} = \frac{V_X}{Z_1} \tag{A.1}$$

and solving to obtain Z_1 we have,

$$Z_1 = \frac{A}{1 - A} \tag{A.2}$$

Making the same analysis for Z_2, it follows that

$$Z_2 = \frac{Z}{1 - A^{-1}} \tag{A.3}$$

It must be emphasized that the application of this theorem is only useful if A can be determined by some independent means.

Appendix B

Published Papers

Co-Design Strategy Approach of LNA, Oscillator, and Mixer

Electronics and Telecommunications Quartely
(Invited paper of MIXDES 2009)

Co-Design Strategy Approach of LNA, Oscillator, and Mixer

J. FERREIRA, I. BASTOS, L. OLIVEIRA, J. P. OLIVEIRA

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A co-design strategy for the implementation of a low-voltage fully integrated CMOS receiver is presented. This co-design approach allows the design of a compact direct-conversion receiver by avoiding 50 Ω matching buffers and networks, and AC coupling capacitors between mixer inputs and LNA and oscillator outputs. Moreover, the proposed circuit does not require DC choke inductors for mixer biasing. Since a 1.2 V power supply is used, a current bleeding technique is applied in the LNA and in the mixer. To avoid inductors and obtain differential quadrature outputs, an RC two-integrator oscillator is employed, in which, a filtering technique is applied to reduce phase noise and distortion. The proposed receiver is designed and simulated in a 130 nm standard CMOS technology. The overall conversion voltage gain has a maximum of 35.8 dB and a noise figure below 6.2 dB.

Keywords: LNA, RC Oscillator, mixer, direct-conversion receiver, low–IF receiver, fully integrated CMOS receiver

1. INTRODUCTION

The direct conversion architecture, shown in Fig. 1, and low-IF architecture, shown in Fig. 2 are approaches to enable full integration of RF receivers in pure standard digital CMOS technology which is reaching higher transistor's cutoff frequencies ω_T. The success of these approaches is supported by its dissemination from high demanding 2G and 3G handsets to low data rate and low-power wireless sensors (WSN) and ISM applications.

Both, the direct conversion receiver (DCR) and the low-IF receiver techniques, allow significant reduction on the number of off-chip components, which means that all the major building blocks will interconnect to each other inside the chip [1-3]. Therefore, the match between these internal interconnects at 50 Ω level is no longer required. This simple approach opens the design of highly integrated RF front-end with low area, low power, and low-cost implementation.

DCR and low-IF receivers require linear low noise amplifier (LNA) followed by a mixer that needs a high frequency local oscillator (LO) with precise quadrature outputs. Within these types of receivers, the conventional approach of designing independently these blocks is not longer suitable. Alternatively, a co-design methodology for adapting the mixer to the LNA and to the oscillator is required. All these requirements are difficult to fulfill simultaneously, and therefore, an optimized trade-off process should be followed.

This paper proposes a co-design strategy applied jointly to the LNA, mixer and to the local oscillator for applications in the sub-gigahertz band and with low to moderate data rate, which can be applied to direct or low-IF receivers.

The main objective of this co-design is to avoid matching buffers (in LNA and oscillator outputs), and directly connect to the mixer without using AC coupling capacitors and choke inductors. This co-design also allows the minimization of power consumption, which is an ongoing research work.

.

2. RF FRONT-END CONSIDERATIONS

In the homodyne receiver shown in Fig. 1, the RF spectrum is directly translated to the baseband by the complementary operation of the LNA, mixer and LO. The sub-gigahertz RF signal is first amplified by the LNA and then down-converted to zero-IF in-phase and quadrature (I/Q) signals by the composite mixer driven by quadrature LO signals. For DCR operation the LO has the same

frequency of the input radio and I/Q signals are needed to separate the wanted channel from its mirror, which is accomplished by means of a Hilbert transform. As a consequence, this downconversion requires accurate quadrature signals generated by the LO [1, 2].

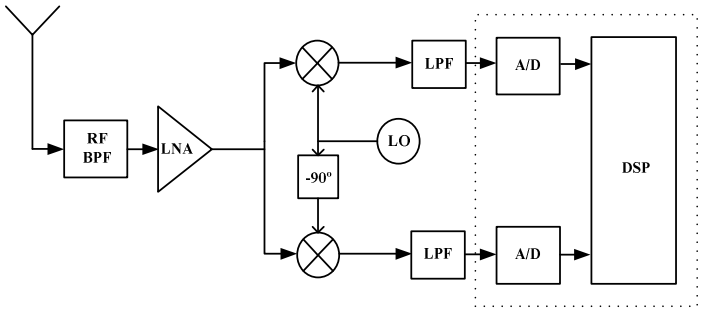

Fig. 1. Direct Conversion Receiver.

Besides the previous requirements, the DCR architecture has several design issues to be addressed:

a) Flicker noise – the low frequency 1/f corner associated with standard MOS technology degrades the Signal-to-Noise ratio (SNR) at low frequency baseband signals. The major contribution at the output comes from the current commutating switching transistors of the mixer.

b) LO leakage – LO signal coupled to the antenna will be radiated again and re-injected to the mixer through the main signal path, originating unwanted baseband DC components.

c) Quadrature error – Quadrature error and amplitudes mismatches between the I and Q signals corrupt the downconverted signal constellation.

d) DC offsets – Since the downconverted band extends down to zero frequency, any offset voltage can corrupt the signal and saturate the receiver's baseband output stages. Hence, DC offset removal or cancellation is required in DCR.

The DCR approach removes the need for IF high-Q filters (reducing the receiver area and/or avoiding external components) which means that the LNA can be directly connected to the mixer. Moreover, since the input mixer impedance is essentially capacitive, the LNA output does not have to be matched

to 50 Ω. Additionally, if a gate input type mixer is considered (meaning that it is driven by a voltage), it is the LNA voltage gain that should be considered.

It has been implicitly demonstrated that heterodyne receivers have important limitations due to the use of external image reject filters. But, DCR receivers have also some drawbacks which degrades the signal translated directly to the baseband. Thus, there is interest in the development of new techniques to reject the image without using filters. An architecture, which combines the advantages of both the IF and the zero-IF receivers, is the low-IF architecture.

The low-IF receiver is a heterodyne receiver that uses special mixing circuits that cancel the image frequency, as shown in Fig. 2. A high quality image reject filter is not necessary anymore, while the disadvantages of the zero-IF receiver are avoided [3, 4].

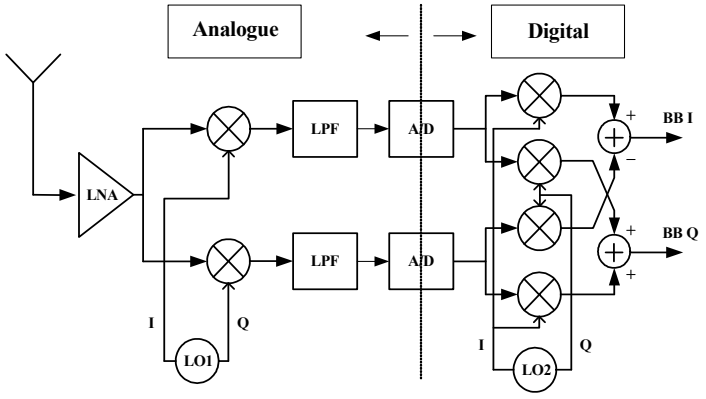

Fig. 2. Low-IF receiver (simplified block diagram).

The co-design strategy, proposed by this work, can be applied both for DCR or low-IF receivers.

3. RF FRONT-END KEY BLOCKS

3.1. LOW NOISE AMPLIFIER

The LNA topology, shown in Fig. 3, account for a source-degenerated effect around the input transconductance transistor M_1. This architecture is very common among narrowband LNA's as it is very close to achieving the goal of providing the input match and best noise performance simultaneously [1-4]. The cascode transistor (M_2) is used to reduce the effect of the gate-drain capacitance C_{gd} of the input transistor (M_1) and to increase the reverse isolation of the LNA.

This improves the stability and makes the LNA's input impedance less sensitive to its load impedance. The number of integrated inductors is reduced to one, since L_S is implemented with the bonding wire and the output inductance L_D is replaced by a resistance. In order to avoid significant voltage drop at the output resistor a bleeding current is injected at the drain of M_1 preserving the value of the g_m of M_1, needed to maintain the input matching to 50 Ω.

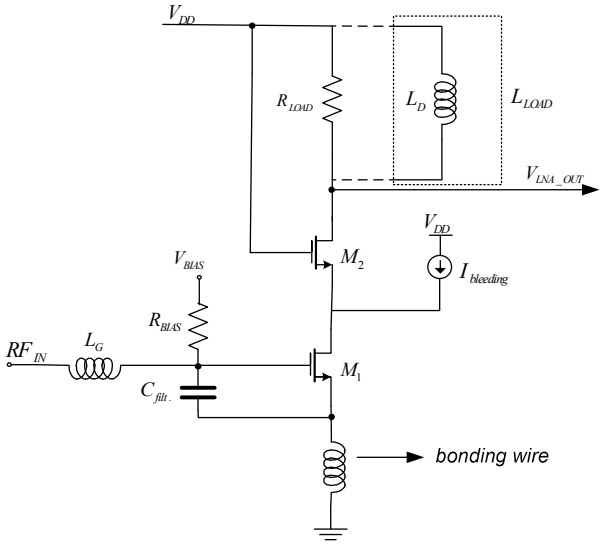

Fig. 3. LNA circuit schematic.

It is clear from the input impedance, which is approximately given by (1), that at resonance and for a given L_S the 50 Ω input match sets the value of the transconductance gain.

$$Z_{in} = j\omega L_g + j\omega L_s + \frac{1}{j\omega(C_{filt} + C_{gs1})} + \frac{g_{m1} L_s}{C_{filt} + C_{gs1}} \tag{1}$$

On the other hand, due to capacitive nature of the mixer input, an optimized value for the LNA voltage gain can be found by selecting an appropriate value of the output LNA load resistance.

Entering into account the effective transconductance gain at the resonance frequency, set by the input matching requirement, the LNA voltage gain in case of resistive load R_L is given approximately by:

$$\left|A_v\right| = G_{m,LNA}.R_{out,LNA} \approx gm_{1,eff} \cdot R_L \tag{2}$$

The total LNA transconductance $G_{m,LNA}$ is approximately given by the effective transconducantce of M_1 if $1/g_{m2} << r_{out,M1}$. This effective transconductance also includes the degeneration effect due to L_s. The output LNA impedance is approximately given by R_L due the cascode configuration of M_1 and

M_2 he value of R_L is the result of co-designing the LNA together with the mixer. The value of the 700 Ω guaranteed the best performance, from which a gain of 28 dB is achievable.

3.2. QUADRATURE LOCAL OSCILLATOR

The schematic of the two-integrator oscillator [5] is presented in Fig. 4. Each integrator is realized by a differential pair (transistors M) and a capacitor (C). The oscillator frequency is controlled by I_{tune}. There is an additional differential pair (transistors M_L), with the output cross-coupled to the inputs, which performs two related functions: a) compensation of the losses due to R to make the oscillation possible (a negative resistance is created in parallel with C); b) amplitude stabilization, due to the non-linearity (the current source I_{level} controls the amplitude). To start the oscillations the condition $g_m > 1/R$ must be met. Moreover, the I_{level} is used to control the output signals amplitude.

In order to obtain low distortion output, a filtering technique is used. To achieve this goal the extra capacitor C_{filter} is introduced to the terminals of the tuning current source I_{tune}. The introduction of this element reduced cancels the harmonics at this point and reduced the oscillator phase-noise.

The circuit of Fig. 4 can be represented by the linear model in Fig. 5, where the negative resistance is realized by the cross-coupled differential pair (M_L), and R represents the integrator losses due to the pairs of resistances R / 2.

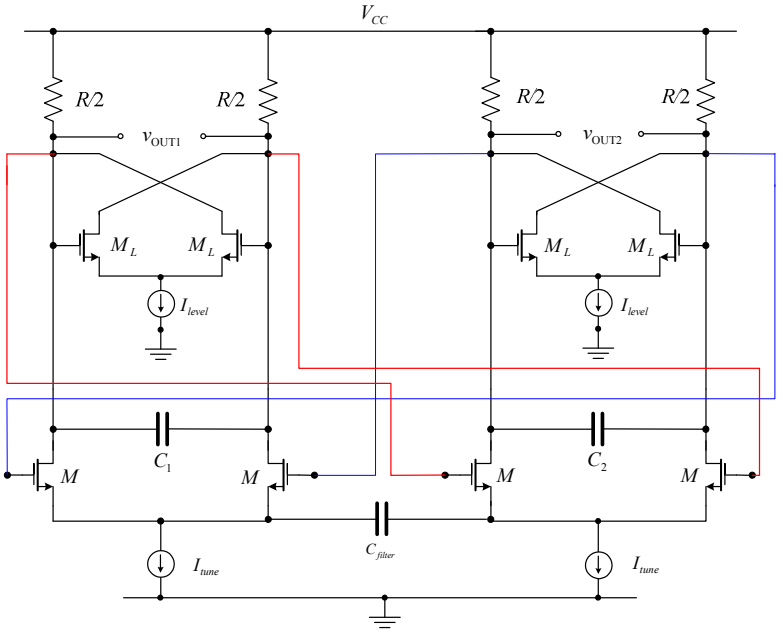

Fig. 4. Two-integrator schematic.

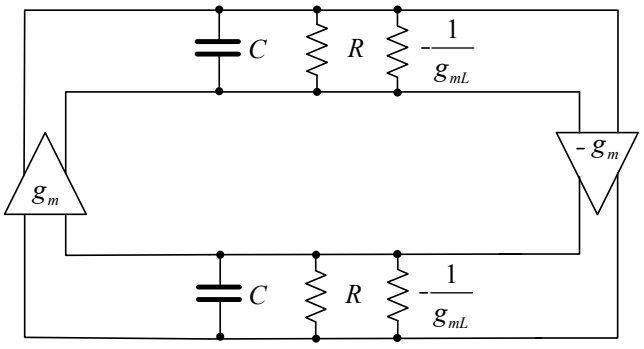

Fig. 5. Two-integrator linear model.

The oscillator frequency varies by changing either the capacitance or the transconductance. In a practical circuit we can use varactors to change the capacitance or, most commonly, we can change the tuning current, and therefore, the transconductance.

These oscillators have wide tuning range with very precise inherent differential quadrature outputs (less than one degree quadrature error), which are required for very compact DCR and low-IF receivers [5].

3.3. MIXER

The I/Q mixer topology, shown in Fig. 6, is constructed around a double balanced Gilbert cell which needs accurate I/Q differential inputs from the LO. This differential mixer structure has higher conversion gain, lower noise figure, improved linearity, higher port-to-port isolation, higher spurious rejection, and lower even-order distortion, with respect to the single-balanced mixer. The main disadvantage is the increased area (due to complexity) and power consumption but in order to save area and since the LNA output is single ended it has not been used a balun transformer to provide the RF differential at the mixer input [1-4].

Considering the high impedance mixer input, the LNA output can be directly AC connected to the mixer. Nevertheless, the LNA output DC component is important to bias the transconductance mixer stage, which controls the mixer conversion gain. Inside this transconductance mixer block, a minimum L is used, to maximize gain and speed, and the W is adjusted according to the DC voltage at the LNA output node. An additional current is injected into the mixer transconductance (formed by M_3 and M_4) to improve linearity and to set the

conversion gain and noise figure. By adjusting this current, the DC output level from the LNA will have less impact on the mixer output voltage.

The mixing switching current commutating stage is formed by a couple of NMOS transistors pair, which are connected directly to the oscillator I/Q outputs. As in the previous stage, the oscillator AC output is connected directly to the mixer. The oscillator amplitude needs to be maximized to properly drive the mixer switching transistors and reduce the mixer output 1/*f* noise. Moreover, the oscillator output DC component is important to bias these switching pairs, and it will define their widths (since the *L* is kept at minimum value).

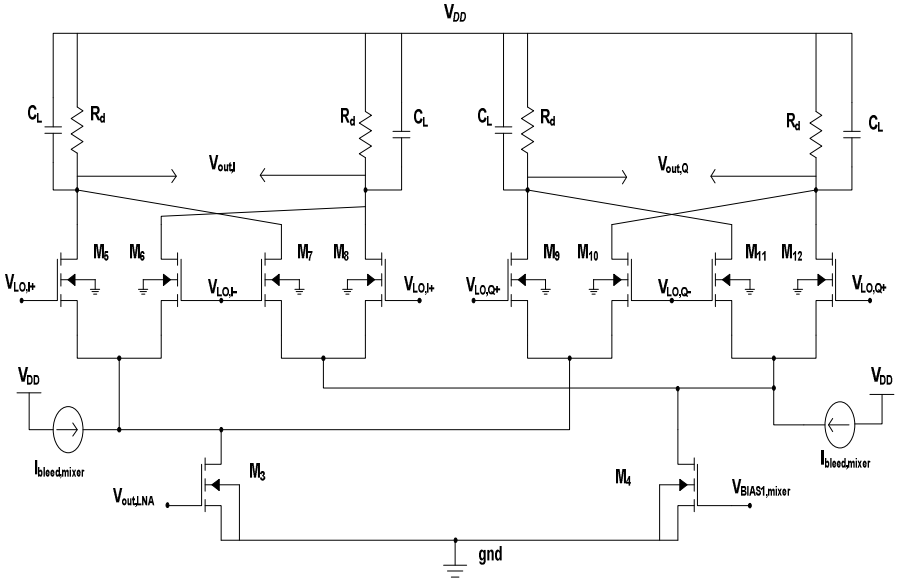

Fig. 6. Mixer circuit.

3.4. CO-DESIGN STRATEGY

The co-design of the LNA, oscillator and mixer facilitates the optimization process to reach better tradeoff between conversion gain and noise figure. Another objective of this co-design is to avoid 50 Ω matching buffers and AC coupling capacitors. LNA and mixer merged topologies has been proposed in literature [6], but in our design a cascaded structure was chosen. This topology can achieve higher gain and better noise figure since the noise contribution of the mixer can be substantially suppressed by the high voltage gain of the LNA. In this work we propose that the mixer should be co-designed with both the LNA and LO.

The design process begins by maximizing the LNA voltage gain for a given input match criteria (50 Ω in this case). By its turn the oscillator is designed

to maximize the signal output swing voltage and improve the I/Q signals accuracy for a given power. With the obtained DC components at the output of these blocks, the mixer is then optimized to reach a reasonable conversion gain and noise figure. In order to reduce the total area, the design must remove as much as possible the use of inductors and AC coupling capacitors.

The co-design example presented in this work will reduce the total circuit area allowing the design of a low cost compact receiver.

The main objective of this work is the co-design between the LNA, LO and mixer in order to avoid 50 Ω matching buffers and AC coupling capacitors.

4. SIMULATION RESULTS

To validate the proposed design strategy, a LNA, mixer, and quadrature oscillator have been co-designed and simulated in a 130 nm CMOS technology with 1.2 V power supply. Two cases have been considered by varying the LNA gain from a high value, for improved sensitivity, to a reduced one, for improved receiver linearity under strong received signals.

4.1. RECEIVER WITH HIGH LNA GAIN

Beginning with a traditional inductive load of 27 nH inductor (one of the maximum available values for the chosen technology), a gain of 15 dB and a noise figure of 2.7 dB at 900 MHz are achieved. Replacing this inductor by a 700 Ω resistor (this can not be higher due to power supply headroom), the voltage gain and noise figure change, respectively, to 28 dB and 2.24 dB while maintaining the power consumption below 9 mW.

Concerning the RC two-integrator oscillator, Tab. 1 shows the effect of the capacitive filtering technique to reduce phase noise and distortion.

Table 1

RC Oscillator Simulation Results

Case	*Phase-noise @ 10MHz offset* [dBc/Hz]	*THD* [dB]	P_D [mw]
I : without C_{filter}	-111.0	-31.3	4.8
II : with C_{filter}	-112.6	-30.8	5.2
III: with C_{filter} optimized for THD	-120.0	-43.5	8.6

In comparison to case I, the simulations results from case II show that the introduction of a filtering capacitor C_{filter} generates a phase noise improvement of 1.6 dB but with a drop in output signal magnitude. Therefore, to achieve the desired amplitude and frequency, the current values have to be increased, and, the power consumption rises slightly. In case III, I_{tune} and I_{level} currents were further increased leading to better phase-noise and lower THD but followed by the corresponding increase of the circuit consumption.

The final values in the designed oscillator are: R = 314 Ω, (W/L) = 15 µm / 0.255 µm for M transistors, W/L = 10.8 µm / 0.255 µm for M_L transistors, C_{filter} =217 fF (for cases I and II) and C_{filter} =430 fF (for case III). The oscillator differential output amplitude is 290 mV @ 900 MHz.

The final values in the designed mixer are: R_{L}=800 Ω, C_{L}=2.5 pF, (W/L)= 100 µm/ 0.13 µm for the switching stage transistors, (W/L)= 30 µm / 0.13 µm for the RF stage transistors, and $I_{\text{bled,mixer}}$=4.15 mA.

In Figs. 7 to 11 simulations results are presented for the completed front-end obtained from SpectreRF simulator, using BSIM3V3 models, including noise and linearity performance.

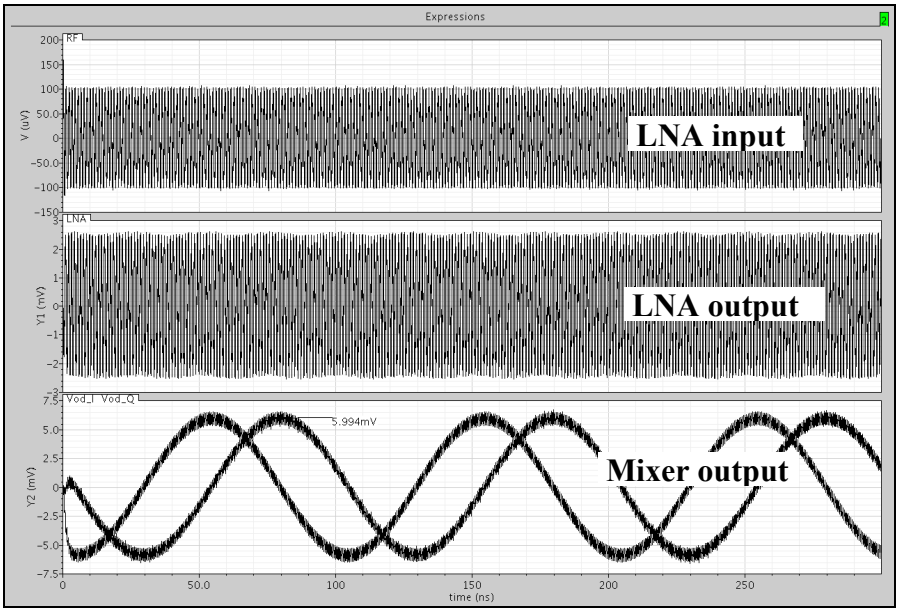

Fig. 7 – LNA and Mixer simulated waveforms.

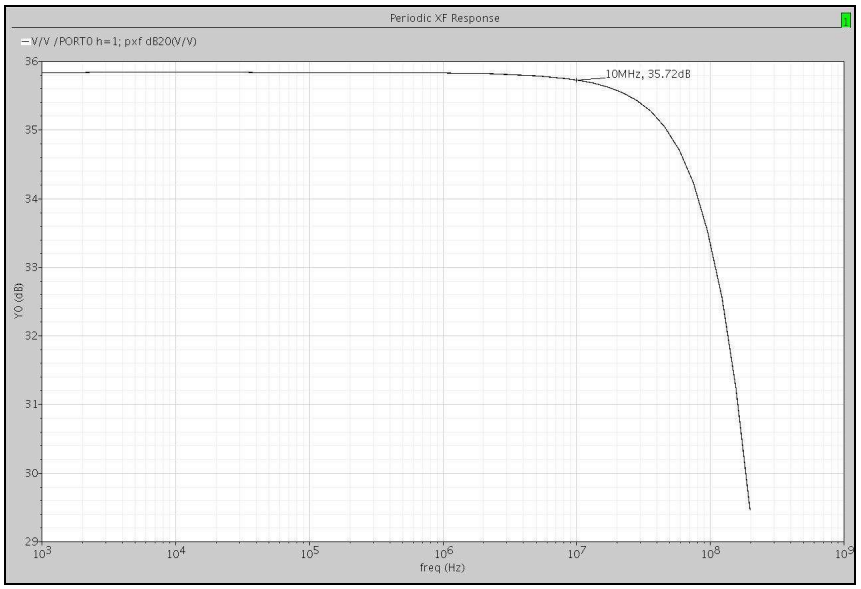

Fig. 8 - Total conversion gain.

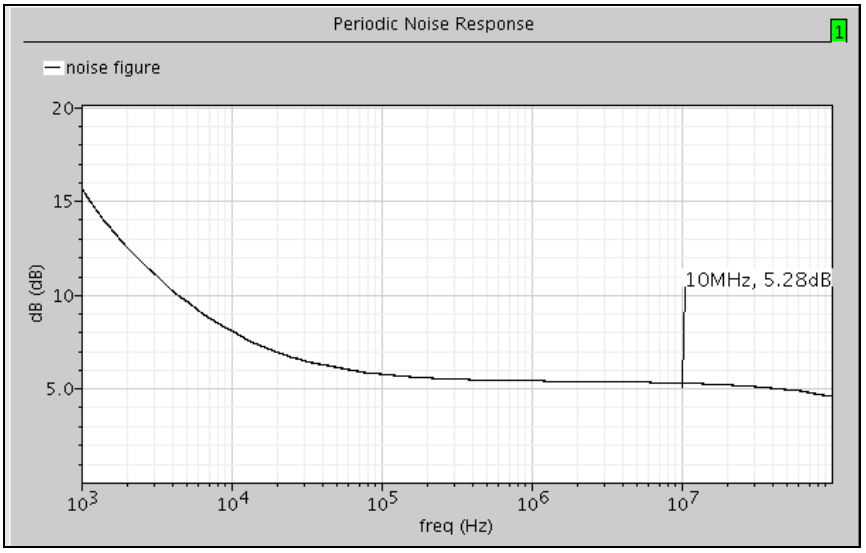

Fig. 9 – Noise figure for the RF front-end.

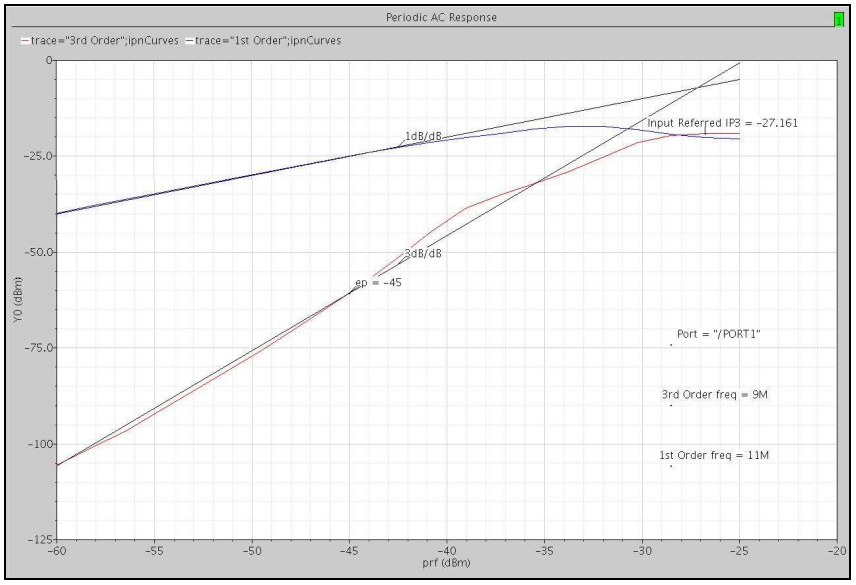

Fig. 10 - IIP3.

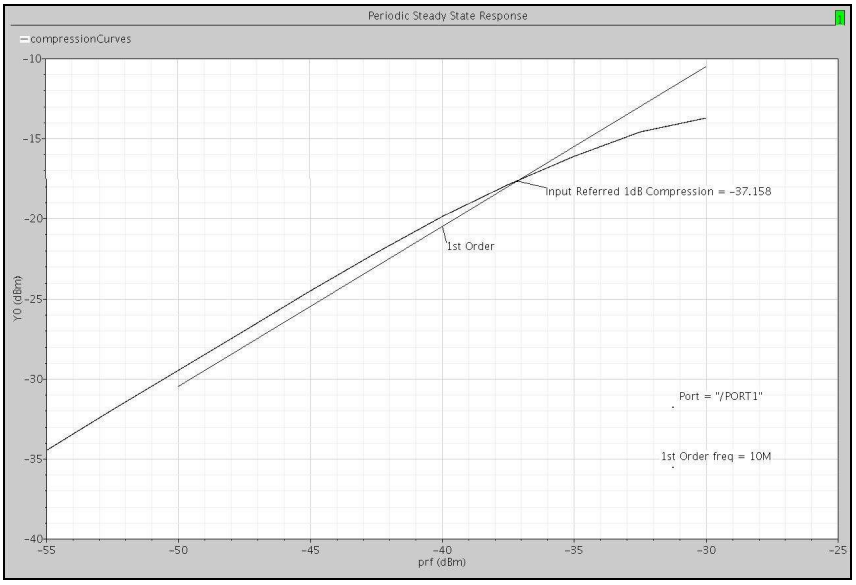

Fig. 11 - 1dB Compression Point.

4.2. RECEIVER WITH LOW LNA GAIN

In order to improve linearity, the LNA gain is reduced by removing the bleeding current and adjusting the resistive load R_L (from 700 Ω to 72 Ω) to meet the same DC output (thus, keeping the Mixer and LO unchanged). Table 2 shows the simulation results obtained for this low LNA gain design, and a comparison with the previous design.

The objective of these two designs is the following: in a complete receiver an RSSI block checks the amplitude at the output of the mixer and adjust the LNA

gain in order to avoid the saturation of the amplifiers blocks. Thus, the gain of the LNA has at least two possible gains: a high value if we have a very low input signal; and a low value in the presence of a strong input signal (e.g., close to the transmitter antenna). In both cases, the noise figure (NF) and conversion gain (CG) results were obtained from SpectreRF simulator, using BSIM3V3 with the complete front-end, models, including noise.

Table 2

Front-end results (@ 10 MHz)

Parameter	High LNA Gain (#1)	Low LNA Gain (#2)
NF	5.28 dB	6.16 dB
CG	35.7 dB	25.5 dB
IIP3	-27.16 dBm	-17.33 dBm
1dB Compression Point	-37.16 dBm	-28.95 dBm

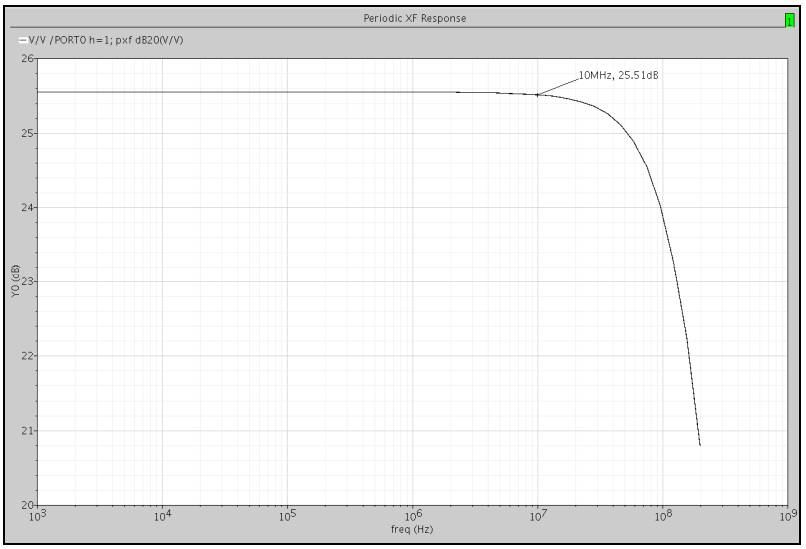

Fig. 12 - Total conversion gain.

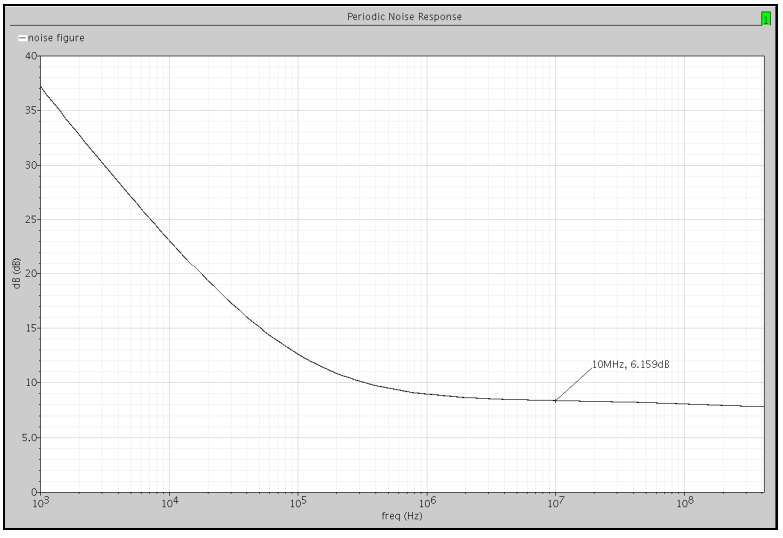

Fig. 13 - Noise figure for the RF front-end.

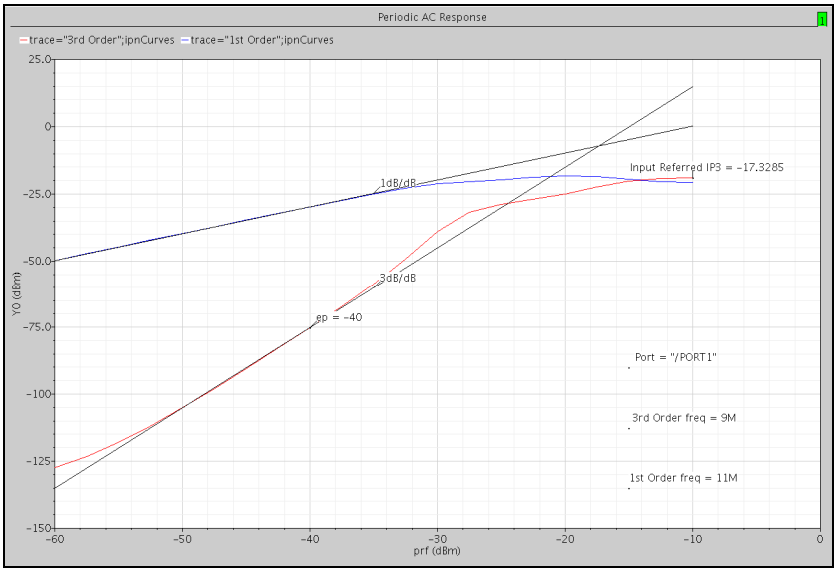

Fig. 14 - IIP3.

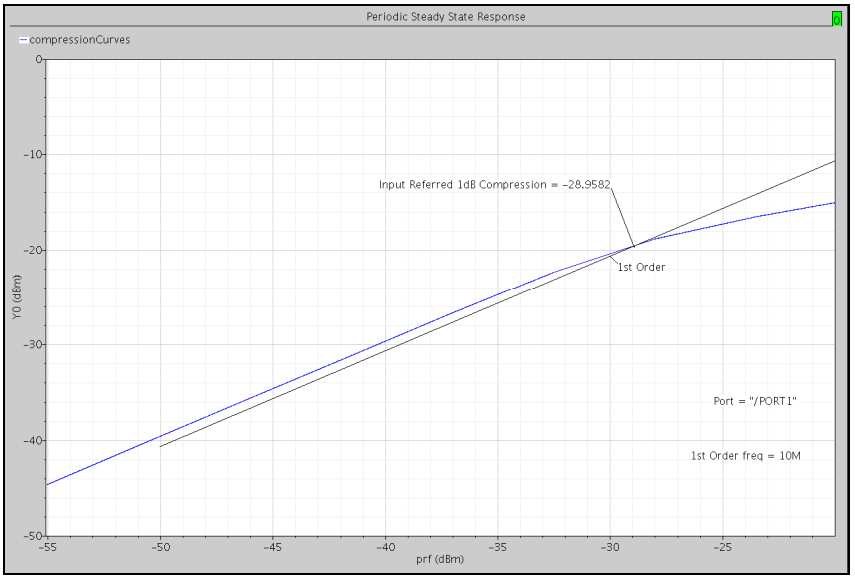

Fig. 15 - 1dB Compression Point.

5. DISCUSSION AND CONCLUSIONS

In this paper, a co-design strategy for the implementation of a low-voltage, low-area, and low-cost, fully integrated CMOS receiver was presented. This approach avoids 50 Ω matching buffers and networks, AC coupling capacitors, and DC choke inductors.

We present a resistive load LNA, with 700 Ω load, and an inductorless differential RC quadrature oscillator, which are combined with a mixer in a co-design strategy. A current bleeding technique is applied to the LNA and mixer,

due to the low power supply voltage. The low area quadrature two-integrator oscillator uses a capacitive filtering technique, which reduces the oscillator phase-noise and the harmonic distortion.

The circuit in this paper has only one inductor, allowing the design of a very compact and low-cost receiver (DCR or low-IF), suitable for low data rates ISM applications.

The proposed receiver was designed and simulated with UMC 130 nm CMOS technology. The total conversion voltage gain has a maximum of 35.8 dB and the cascade noise factor has a minimum of 5.3 dB for the band of interest.

ACKNOWLEDGMENT

This work was supported by the Portuguese Foundation for Science and Technology (FCT) through funding of CTS-UNINOVA and project LEADER (PTDC/EEA-ELC/69791/2006).

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Analysis and Design of a MOSFET-Only Wideband Balun LNA

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Analysis and Design of a MOSFET-Only Wideband Balun LNA

Ivan Bastos, Luis B. Oliveira, João Goes, and Manuel Silva

***Abstract*—In this paper we present a MOSFET-only implementation of a balun LNA. This LNA is based on the combination of a common-gate and a common-source stage with cancellation of the noise of the common-gate stage. In this circuit, we replace resistors by transistors, to reduce area and cost, and to minimize the effect of process and supply variations and mismatches. In addition, we obtain a higher gain for the same voltage drop. Thus, the LNA gain is optimized and the noise figure (NF) is reduced. We derive equations for the gain, input matching and NF. The performance of this new topology with that of a conventional LNA with resistors is compared. Simulation results with a 130 nm CMOS technology show that we obtain a balun LNA with a peak gain of 20.2 dB (about 2 dB improvement), a spot NF lower than 2.4 dB. The total power consumption is only 4.8 mW for a bandwidth higher than 6 GHz.**

***Index Terms*— CMOS LNAs, MOSFET-only circuits, Noise cancelling, Wideband LNA.**

I. Introduction

Nowadays, the demand for mobile and portable equipment has led to a large increase in wireless communication applications. In order to achieve full integration and low cost, modern receiver architectures (Low-IF and Zero-IF receivers), require inductorless circuits [1 - 4]. The LNA, which is a key block in the design of such receivers, is investigated in this paper.

LNAs can be either narrowband or wideband [1, 2]. Narrowband LNAs use inductors and have very low noise figure, but they occupy a large area and require a technology with RF options to have inductors with high Q. Wideband LNAs with multiple narrowband inputs have low noise, but their designs are complicated and the area and cost are high [1, 2]. RC LNAs are very simple and inherently wideband, but conventional topologies have large noise figures (NFs). Recently, wideband LNAs with noise and distortion cancelling [5] have been proposed, which can have NFs below 3 dB.

Inductorless circuits have reduced die area and cost [4]. However, they are usually realized with MiM capacitors, which require an additional insulator/metal layer, and they use poly or/and diffusion resistors, which have large process variations and mismatch.

In this paper our main goal is to design a very low area and low-cost LNA, and at the same time obtain less circuit variability, by implementing the resistors using MOS transistors (MOSFET-only design) [6]. As it will be shown, this approach adds a new degree of freedom, which can be used to maximize the LNA gain, and, therefore, minimize the circuit NF.

We start by reviewing the basic amplification stages, common-gate (CG) and common-source (CS). For each circuit we derive equations, with different levels of approximation, for the gain, input matching and noise figure. By comparing the results obtained with the different equations with those obtained by simulation, we select the level of approximation required for the frequency range in which we are interested.

For the complete LNA (combined CG and CS balun topology), we compare the conventional design with resistors, and the new MOSFET-only implementation optimized for gain and NF. Simulation results of a circuit example designed in a standard 130 nm CMOS technology validate the proposed methodology.

This paper is organized as follows. In section II we derive the equations for the basic CG and CS stages. In section III we present simulation results for the conventional LNA with resistors, which confirm the theory. In Section IV we present the MOSFET-only LNA and we describe the optimization of gain and NF. We compare performance of this LNA with others in the literature. Finally, a discussion and some conclusions are given in Section V.

II. Common-Gate and Common-Source Stages

Figs. 1 and 2 show, respectively, the CG and CS stages, normally employed in RC LNAs. We derive equations using three different levels of approximation, denoted by *a*, *b*, and *c*: *a* - transistors' complete model including the parasitic capacitances; *b* - low frequency approximation; *c* - low-frequency approximation neglecting the transistors' output resistance.

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A. *Common-Gate Stage*

In the equations below g_{m1} and g_{mb1} are the transistor's transconductance and body effect transconductance, respectively, and r_{o1} is the transistor's output resistance. The capacitance C_S represents the source-bulk and source-gate capacitances and C_L the drain-bulk and drain-gate capacitance. R_s is the signal source resistance and R_1 is the load resistance.

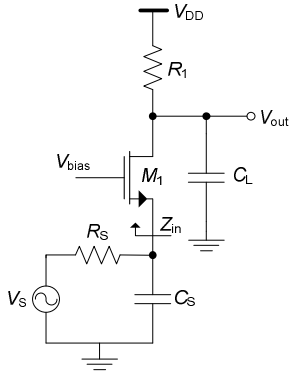

Figure 1. Common-Gate Stage.

1) Gain

$$A_{vCG\_a} = \frac{[(g_{m1}+g_{mb1})r_{o1}+1]R_1}{sC_Lr_{o1}R_1+r_{o1}+R_1} \quad (1a)$$

$$A_{vCG\_b} = \frac{[(g_{m1}+g_{mb1})r_{o1}+1]R_1}{r_{o1}+R_1} \quad (1b)$$

$$A_{vCG\_c} = (g_{m1} + g_{mb1})R_1 \quad (1c)$$

2) Input Impedance

$$Z_{inCG\_a} = \frac{sC_Lr_{o1}R_1+r_{o1}+R_1}{as^2+bs+c} \quad (2a)$$

where,

$$a = C_SC_Lr_{o1}R_1,$$

$$b = C_S(r_{o1} + R_1) + C_LR_1(r_{o1}(g_{m1} + g_{mb1}) + 1),$$

$$c = r_{o1}(g_{m1} + g_{mb1}) + 1,$$

$$Z_{inCG\_b} = \frac{r_{o1}+R_1}{r_{o1}(g_{m1}+g_{mb1})+1} \quad (2b)$$

$$Z_{inCG\_c} = \frac{1}{g_{m1}+g_{mb1}} \quad (2c)$$

3) Noise Figure

$$F_{CG} = 1 + \frac{\gamma g_{m1}}{R_S\left(g_{m1}+g_{mb1}+\frac{1}{r_{o1}}\right)^2} + \frac{1}{R_SR_1\left(g_{m1}+g_{mb1}+\frac{1}{r_{o1}}\right)^2} + \frac{k_f}{4kTR_Sc_{ox}W_1L_1f^{\alpha f}}\left(\frac{g_{m1}}{g_{m1}+g_{mb1}+\frac{1}{r_{o1}}}\right)^2 \quad (3)$$

where k is the Boltzmann constant c_{ox} is the oxide gate capacitance *per* unit area, W_1 and L_1 are the transistor channel's width and length, respectively, T is the absolute temperature in Kelvin, γ is the excess noise factor, k_f and α_f are intrinsic process parameters, which depends on the size of the MOSFET transistors [7, 8].

B. *Common Source Stage*

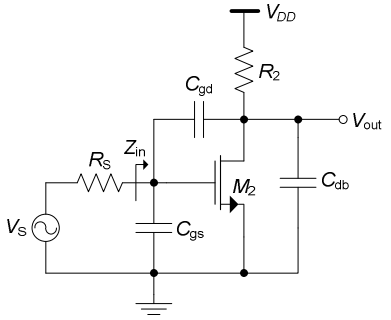

Figure 2. Common-Source Stage.

In the following equations g_{m2} and r_{o2} are the transistor's transconductance and output impedance. The capacitances C_{gs2}, C_{gd2}, and C_{db2} are the gate-source, gate-drain and drain-bulk capacitances, respectively. R_2 is the load resistor.

1) Gain

$$A_{vCS\_a} = \frac{(sC_{gd2}-g_{m2})r_{o2}R_2}{sr_{o2}R_2(C_{db2}+C_{gd2})+r_{o2}+R_2} \quad (4a)$$

$$A_{vCS\_b} = -g_{m2}\left(\frac{r_{o2}R_2}{r_{o2}+R_2}\right) \quad (4b)$$

$$A_{vCS\_c} = -g_{m2}R_2 \quad (4c)$$

2) Input Impedance

$$Z_{inCS} = \frac{r_{o2}+R_2}{s\left(C_{gs2}(r_{o2}+R_2)+C_{gd2}(r_{o2}+R_2+g_{m2}r_{o2}R_2)\right)} \quad (5)$$

3) Noise Figure

$$F_{CS} = 1 + \frac{\gamma g_{m2}}{R_Sg_{m2}^2} + \frac{1}{R_SR_2g_{m2}^2} + \frac{k_f}{4kTR_Sc_{ox}W_2L_2f^{\alpha f}} \quad (6)$$

III. LNA

In the design of a wideband LNA there is an important choice to be made. A single-ended input simplifies the connection to the antenna and RF filters (they are usually single-ended) and avoids the need of a balun for the single to differential conversion (the balun usually has high loss and degrades the NF significantly). A differential input leads to reduced harmonic distortion and to better power supply and substrate noise rejection.

In this paper we study a single-ended input LNA (Fig. 3), which combines the balun and LNA functionalities in order to obtain a simple and low cost LNA (trying to get the best of the two above described approaches).

We obtain a low noise figure LNA (NF < 3 dB), since the thermal noise of M_1 is cancelled out. The noise produced by M_1 appears in phase at the two outputs, while the signals are in opposition. Thus, we double the gain and cancel the noise. The gain matching of the two stages is critical: we need the same gain to maximize the circuit performance.

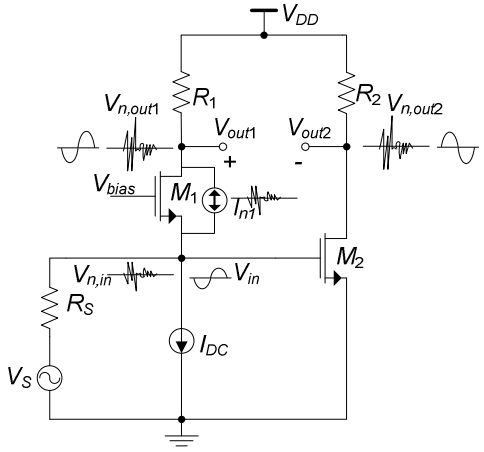

Figure 3. Balun LNA with noise canceling [9].

1) Input Impedance

The LNA input impedance is the parallel of those of the CG and CS stages,

$$Z_{inLNA} = (Z_{inCG\_a} \,//\, Z_{inCS}) \tag{7}$$

if it is assumed that the CS input impedance is very high,

$$Z_{inLNA\_a} = Z_{inCG\_a} \tag{8}$$

and if the low frequency approximation is considered (2b),

$$Z_{inLNA\_b} = Z_{inCG\_b} \tag{9}$$

2) Gain

Since the output signal is differential, and v_{out1} and v_{out2} are the CG and CS outputs, the differential gain is given by

$$A_{vLNA\_a} = A_{vCG\_a} - A_{vCS\_a} \tag{10}$$

and if the low frequencies approximations are used (1b) and (4b),

$$A_{vLNA\_b} = A_{vCG\_b} - A_{vCS\_b} \tag{11}$$

Assuming a infinite transistor's output impedance we can simplify (11) into,

$$A_{vLNA\_c} = (g_{m1} + g_{mb1})R_1 + g_{m2}R_2 \tag{12}$$

To achieve noise cancellation and balun operation (conversion of a single-ended input to a differential output) the CG and CS's stages gain should be equal. Considering $r_{o1}(g_{mb1}+g_{m1}) >> 1$ and for the same current and length (L) on M_1 and M_2, their output resistance (r_o) are approximately equal, and making $(g_{m1}+g_{mb1}) = g_{m2} = g_m$ and $R_1=R_2=R_D$, we obtain from (11), a fourth approximation denoted by subscript d

$$A_{vLNA\_d} = \frac{2r_o R_D g_m}{r_o + R_D} \tag{13}$$

3) Noise Figure

Considering the same approach for noise cancellation, the simplified noise figure is given by,

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S g_m^2 c_{ox} f^{\alpha f}}\left(\frac{g_{m1}^2}{W_1 L_1} + \frac{g_m^2}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S R_D g_m^2} \tag{14}$$

4) Dimensions and Biasing

The LNA is designed for 50 Ω input impedance using equation (2c) as a first approximation and imposing the transconductance of M_1. M_1 is biased with 2 mA. The load resistors values are about 200 Ω to give a DC output level that avoids signal limitation and to keep M_1 and M_2 in the saturation region. The DC voltage V_{BIAS} is used to adjust the DC current of M_2 to the same value as that of M_1. The dimensions are shown on table I.

TABLE I. LNA DESIGN VALUES

	I_D (mA)	R (Ω)	g_m (mS)	W (µm)	L (µm)	V_{BIAS} (mv)	V_{GS} (mV)
M_1	2	200	24.5	72	0.12	940	515
M_2	2	200	27.2	90	0.12	-	425

5) Simulation Results

To validate the equations obtained previously for the LNA's performance parameters, and to find out the required level of approximation, a comparison is made with the simulation results.

The real part of the input impedance (Figs. 4 and 5) remains almost constant up to 10 GHz, and the imaginary part starts to be significant above 1 GHz, so the input matching must be designed carefully for wideband applications. Equation (9) can be used for this purpose.

We confirm by simulations that equations (9) and (11) are accurate for our design, as shown in Figs. 4 to 6.

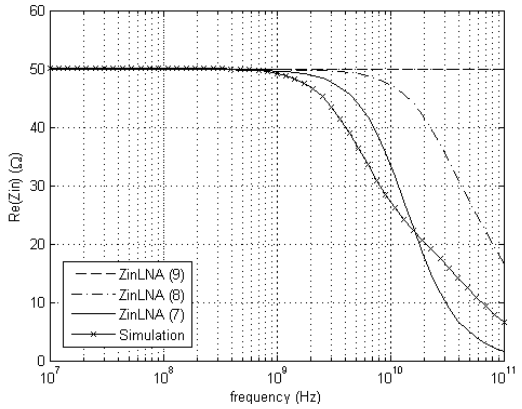

Figure 4. LNA input impedance (real part).

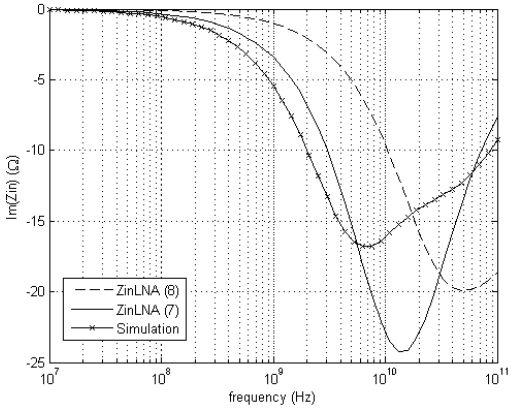

Figure 5. LNA input impedance (imaginary part).

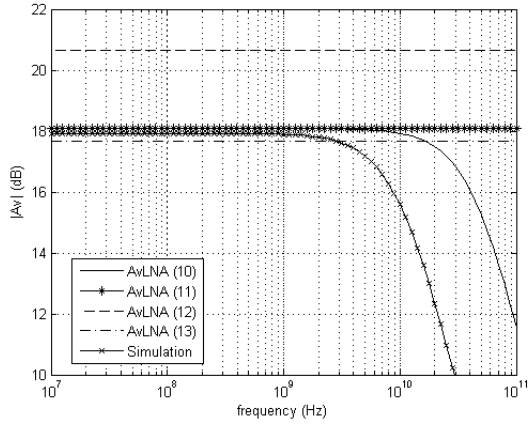

Figure 6. LNA Gain.

For the noise figure simulation we have considered $k_f = 4\text{x}10^{-23}$ V^2Hz and $\alpha_f = 1.2$ for the 130 nm technology [7,8]. We observe in Fig. 7 that the simulations are in accordance with equation (14).

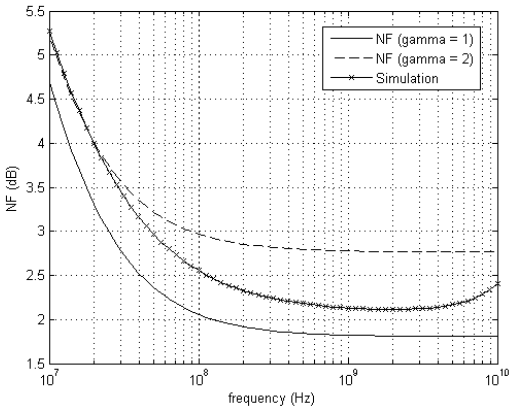

Figure 7. LNA noise figure.

IV. MOSFET-ONLY LNA

A. *Initial Design*

In the MOSFET-only LNA (Fig. 8) the load resistors are replaced by PMOS transistors (M_3, M_4) operating in the triode region, which are modeled ideally by a resistor between the drain and source,

$$(r_{ds} = 1/g_{ds}) \tag{15}$$

where g_{ds} is the channel conductance. To make a comparison with the LNA with load resistors in the initial design, r_{ds} is dimensioned to have the same resistance value of 200 Ω. The biasing parameters are shown in table II.

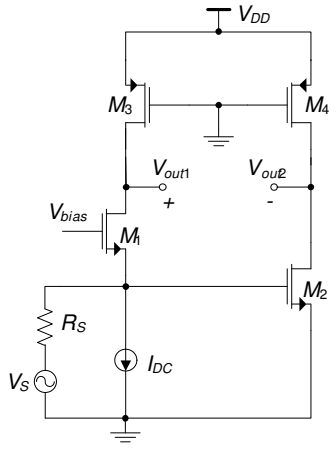

Figure 8. MOSFET-Only LNA

TABLE II. MOSFET-ONLY DESIGN VALUES

	I_D (mA)	r_{ds} (Ω)	g_m (mS)	W (µm)	L (µm)	V_{BIAS} (mv)	V_{GS} (mV)
M_1	2	-	25.38	75.6	0.12	935	507
M_2	2	-	26.73	82.8	0.12	-	427
M_3	2	206.2	2.06	15.3	0.12	-	-
M_4	2	208.3	2.09	15.3	0.12	-	-

However, once the resistors are replaced by MOSFETs it becomes possible to optimize the initial design, as explained in the following.

B. *Optimization Results*

The saturation region is reached when g_m is of about the same magnitude as g_{ds}. A MOS transistor operating in triode region can be modeled by a resistor if $g_{ds} / g_m >> 10$, otherwise the transistor should be modeled by a resistance in parallel with a current source. In this case we can increase the incremental load resistance without increasing the DC voltage drop. This allows the gain to be increased with respect to the circuit with true resistors. By simulations we find the boundary between triode and saturation (Fig. 9) and we obtain the gains and the NF as a function of g_{ds} (Fig. 10).

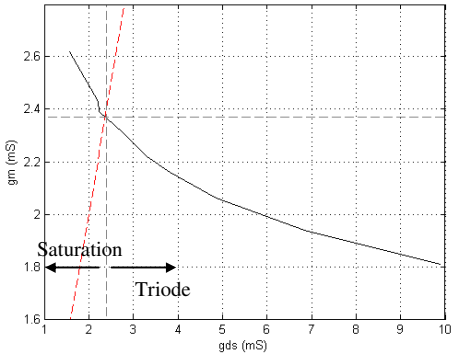

Figure 9. Transistor g_m (g_{ds}) curve.

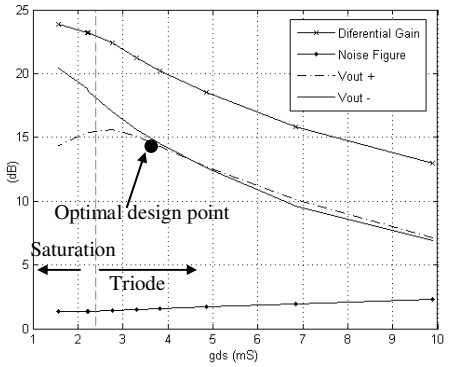

Figure 10. LNA gain optimization.

By inspection of Fig. 10 we find that the optimum operation is just before the gain of the two stages becomes unbalanced ($g_{ds} \approx 3.8$ mS), which occurs before the load transistors reach saturation. The circuit parameters are given in table III.

TABLE III. MOSFET-ONLY DESIGN VALUES (OPTIMIZED)

	I_D (mA)	r_{ds} (Ω)	g_m (mS)	W (µm)	L (µm)	V_{bias} (mv)	V_{GS} (mV)
M_1	2	-	25.23	75.6	0.12	945	513
M_2	2	-	26.74	82.8	0.12	-	432
M_3	2	261.8	2.16	13.5	0.12	-	-
M_4	2	266	2.2	13.5	0.12	-	-

C. *Simulation Results*

1) *Pre-Layout Simulation*

In Figs. 11-13, we present the simulation results for our MOSFET-only design (initial and optimized) and we compare it with the traditional LNA with resistors.

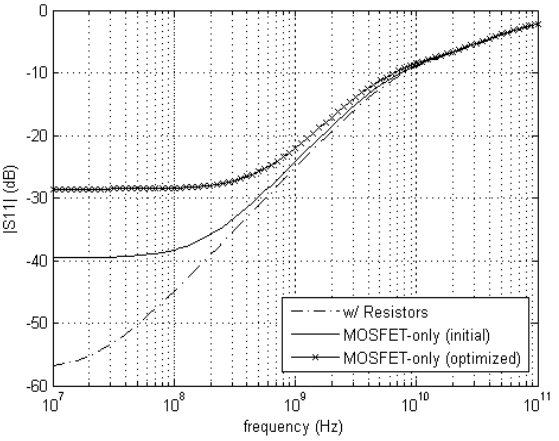

Figure 11. LNA input impedance.

The LNA is considered input matched for values below -10 dB for $|S_{11}|$, which is about 8 GHz for these designs (Fig. 11)

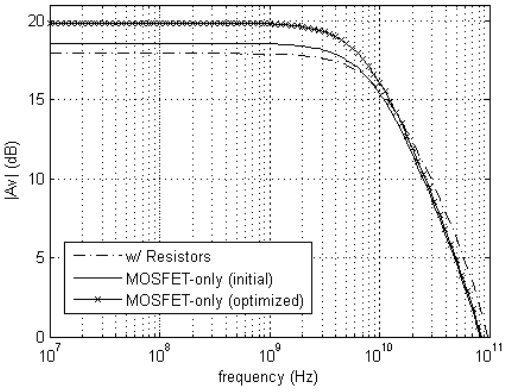

Figure 12. LNA Gain.

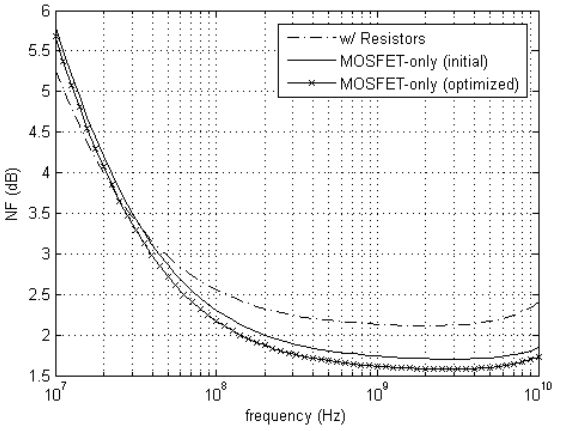

Figure 13. LNA Noise Figure.

In the MOSFET-Only design it is difficult to fix a specific value for the load, since for equal transistors size the r_{ds} has slightly different values (as shown in Table III). The MOSFET-Only LNA with optimized gain has an improvement of 2 dB over the traditional design, but has less bandwidth. Considering the NF, we obtain less than 2 dB, from 200 MHz up to 10 GHz (0.5 dB reduction), for the MOSFET-Only implementation.

2) *Layout design and Post-Layout Simulations*

The proposed MOSFET-only LNA layout is shown in Fig. 14, which has a die area of 31 x 30.5 μm^2. For the layout implementation, the MOSFET sizes are adjusted to minimize the poly gate resistance, and V_{bias} is tuned to set the same current for M_2 and M_4.

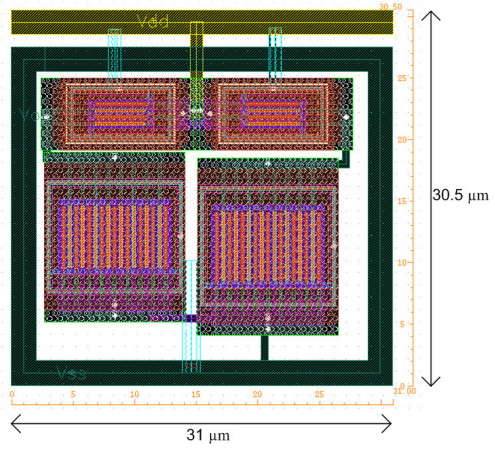

Figure 14. MOSFET-Only LNA layout.

The final layout design parameters are listed in table IV.

TABLE IV. POST-LAYOUT VALUES

	I_D (mA)	r_{ds} (Ω)	g_m (mS)	W (μm)	L (μm)	V_{bias} (mv)	V_{GS} (mV)
M_1	2	-	25.5	80	0.12	925	503
M_2	2	-	27.1	89.6	0.12	-	422
M_3	2	252.4	2.1	12.3	0.12	-	-
M_4	2	252.2	2.1	12.3	0.12	-	-

The post-layout simulation results for the main LNA parameters are shown in Figs. 15-17.

The post-layout simulations show that the input matching is not affected (Fig. 15): in fact there is a slight improvement since the equivalent resistance of load transistors is closer to the initial design.

The gain increases, since the tranconductances of M_1 and M_2 increase, and, consequently, the bandwidth decreases (Fig. 16).

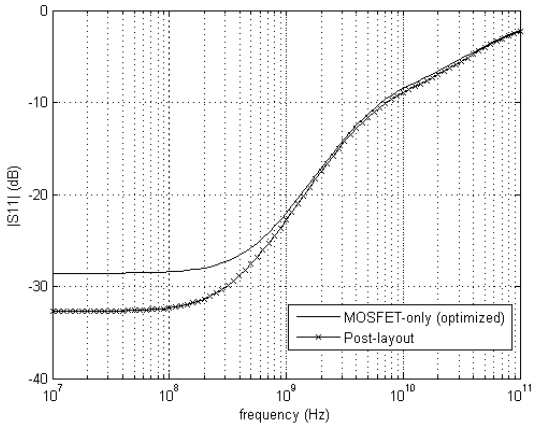

Figure 15. Input impedance.

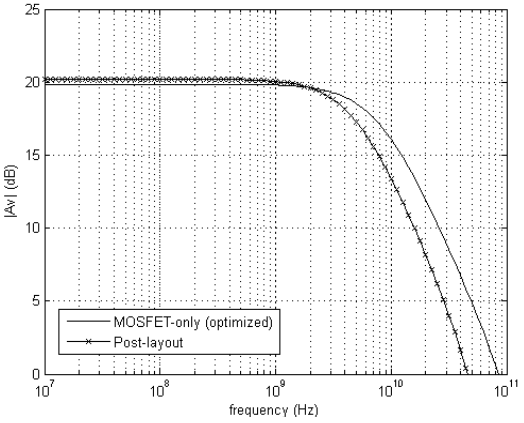

Figure 16. Gain.

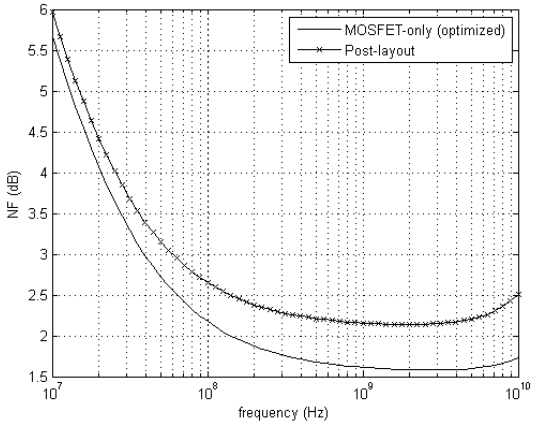

Figure 17. Noise Figure.

The main difference relatively to the pre-layout results is in the NF, which increases by approximately 0.5 dB. This is due to the thermal noise of M_1 being not fully cancelled out, beyond 1 GHz. This is shown by the frequency response from the M_1 noise source to the outputs of the two stages, shown in Figs. 18 and 19.

If we adjust the layout to obtain full cancellation, there will be mismatches in the gain and DC offsets and, thus, the LNA becomes unbalanced.

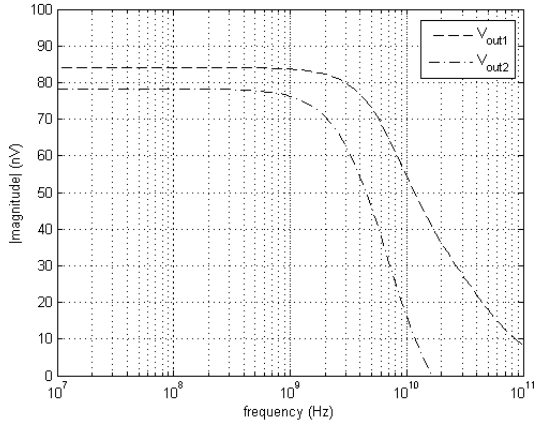

Figure 18. Thermal noise due to M_1 at the outputs of the two stages (magnitude).

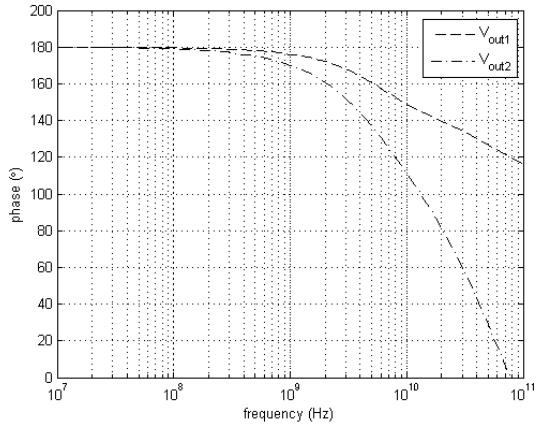

Figure 19. Thermal noise due to M_1 at the outputs of the two stages (phase).

Comparing the results of our optimized MOSFET-only design with those for alternative state-of-the-art inductorless LNAs (Table V), we can conclude it has the advantages of higher gain and lower NF; the drawbacks are a reduction of bandwidth and the increase of the circuit non-linearity (reduction of IIP3).

TABLE V. LNA COMPARISON

	Tech (nm)	**Band (GHz)**	**Gain (dB)**	**NF (dB)**	**IIP3 (dBm)**	**Power (mW)**	**Balun**
[9]	65	0.2-5.2	13.15.6	< 3.5	>0	14	YES
[10]	90	0.5-8.2	22-25	< 2.6	-4/-16	42	NO
[11]	90	0.8-6	18-20	< 3.5	>-3.5	12.5	YES
[12] (sim)	90	0.1-1.9	20.6	< 2.7	10.8	9.6	YES
[13] (sim)	130	0.2-3.8	11.2	< 2.8	-2.7	1.9	YES
This work MOS	**130**	**0.2-5.1**	**20.2**	**<2.4**	**3.1**	**4.8**	**YES**

V. DISCUSSION AND CONCLUSIONS

In this paper we present a MOSFET-only implementation of an LNA based on the combination of a common-gate and a common-source stage. We derive simple equations for gain, input matching and noise figure, which are validated by simulation.

In MOSFET-only LNAs, the replacement of resistors by transistors reduces the area and cost and minimizes the effect of process and supply variation and of mismatches [6]. Moreover, the LNA gain can be controlled by changing the bias of the PMOS transistors that replace the resistors.

The new approach proposed here adds a new degree of freedom, which can be used to optimize the LNA gain and minimize the noise figure: we can obtain a higher gain than with resistors for the same DC voltage drop. As a drawback, this approach increases the distortion (decrease of IIP3).

Simulation results of a circuit implemented in a 130 nm CMOS technology are presented. For comparison, we also show the performance of a conventional LNA with resistors. Both circuits have the same power consumption of 4.8 mW. For the MOSFET-only LNA we obtain a gain improvement of 2 dB, and a NF below 2.4 dB.

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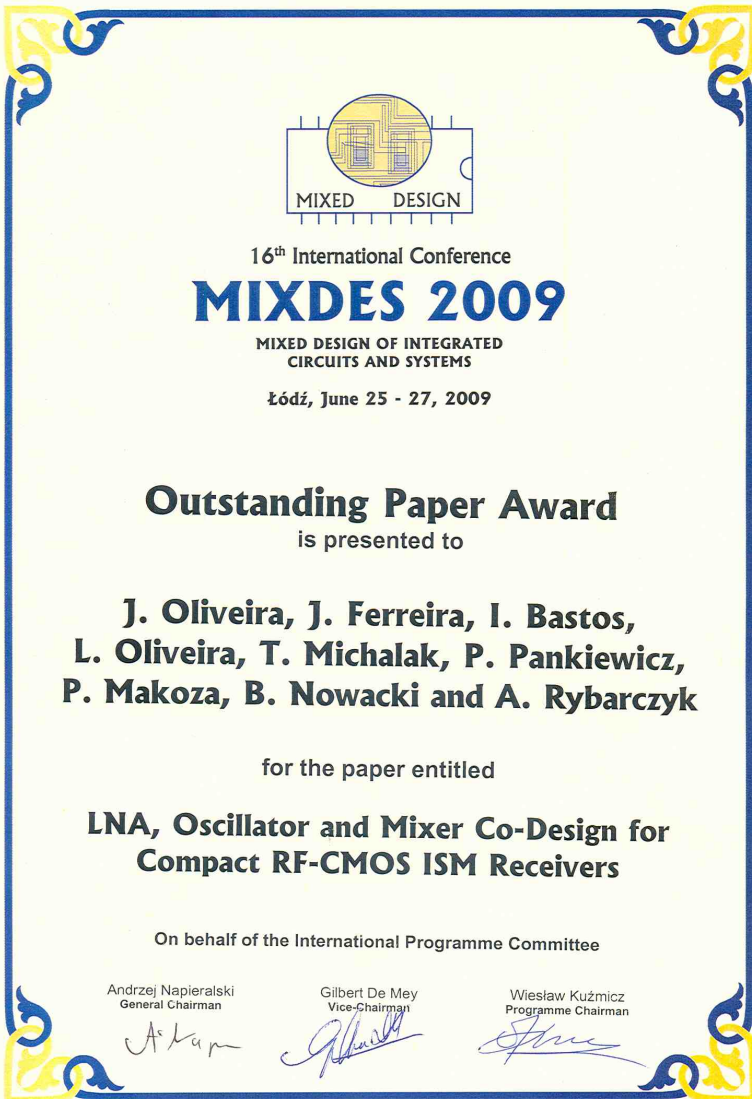
Appendix C

Award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