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Bachelor in Micro and Nanotechnology Engineering

# Influence of uniaxial bending on IGZO TFTs: A study of materials and device

Master of Science in

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Influence of uniaxial bending on IGZO TFTs: A study of materials and device

*“The best way out is always through”*

- *Robert Frost*

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# Abstract

In recent years flexible electronics have gained relevance with applications such as displays, sensors and wearables. In that regard, studying how flexible transistors behave under bending has become of major importance. This work aims to fabricate indium gallium zinc oxide (IGZO) Thin Film Transistors (TFT) with the best bendability possible, without any major changes in the production techniques already used in the industry.

To understand the influence of the substrate on flexible devices, TFTs were fabricated on polyimide substrates using different thicknesses, down to 25 μm, with and without parylene encapsulation layers on top of the device stack. To determine the position of the neutral strain plane, nanoindentation measurements were performed on different device layers at IKTS-Fraunhofer, within BET-EU project.

The delamination of the substrates is a critical step, especially for thinner substrates. The concept of "paper blade" was used in this project to improve the yield of the delamination process.

Initial bending measurements, using a 75 μm thick substrate, showed that bending radii of 45, 25 and 15 mm do not permanently change the performance of the TFTs. Tensile bending measurements with a radius of 1.25 mm were also performed, revealing that the 75 μm thick substrate achieves critical failure in <500 cycles, while the thinner substrate (25 μm) could withstand almost 1000 cycles.

The most common failure mechanism observed under tensile bending was the appearance of cracks in the oxide dielectric when in direct contact with the polyimide substrate. These cracks do not appear in regions where molybdenum gates were in contact with the substrate, hence the mismatch between the coefficient of thermal expansion of the substrate and the dielectric thin film were identified as the reason for failure.

This work shows that, even with intrinsically rigid materials as oxides and metals, it is possible to obtain reliable flexible TFTs, provided that proper stack engineering is considered for their fabrication.

**Keywords:** flexible electronics, IGZO TFTs, bending, mechanical characterisation, neutral strain plane

# Resumo

Atualmente, a eletrónica flexível tem ganho maior relevância com aplicações como mostradores, sensores e *wearables*. Devido a isso, os estudos do comportamento de transístores flexíveis quando estão dobrados é extremamente importante. Este trabalho tem como objetivo fabricar transístores de filme finos (TFT) de óxido de índio-gálio-zinco (IGZO) com a melhor flexibilidade possível, sem alterar significativamente as técnicas de produção utilizadas atualmente pela indústria.

Para compreender a influência do substrato em dispositivos flexíveis, foram fabricados TFTs em substratos de poliamida com espessuras até 25 μm, com e sem uma camada de encapsulamento de parileno. Para a determinação do plano de deformação neutra, foram efetuados testes de nanoidentação em diferentes camadas constituintes dos dispositivos pelo IKTS-Fraunhofer, incluído no projecto BET-EU.

A delaminação dos substratos mostrou-se uma etapa crítica, especialmente para substratos mais finos. O conceito de "lâmina de papel" foi utilizado neste trabalho para aumentar o rendimento do processo.

Medições iniciais dos dispositivos fabricados num substrato com 75 μm, a sofrer deformação mecânica em tensão e compressão, mostram que raios de curvatura de 45, 25 e 15 mm não afetam permanentemente o desempenho dos TFTs. Testes de deformação tênsil com um raio de curvatura de 1.25 mm também foram realizados, mostrando que os dispositivos fabricados no substrato de 75 μm de espessura atingem falha crítica em <500 ciclos, enquanto que o substrato mais fino (25 μm) consegue alcançar quase 1000 ciclos.

O mecanismo de falha ocorrido durante a deformação mecânica em tensão dos dispositivos foi o aparecimento de fendas, onde o dielétrico se encontrava em contacto com o substrato de poliamida. Estas fendas não ocorrem em regiões onde os elétrodos de portas de molibdénio estão em contacto com o substrato, concluindo-se então que a principal razão para a ocorrência desta falha deve-se à diferença entre coeficientes de expansão térmica do substrato e do filme dielétrico.

Este trabalho mostra que é possível obter TFTs flexíveis e fiáveis, mesmo utilizando materiais intrinsecamente rígidos como óxidos e metais, desde que se tenha em conta uma boa engenharia e estudo de multicamadas para a fabricação.

**Palavras chave**: eletrónica flexível, IGZO TFTs, curvatura, caracterização mecânica, plano de deformação neutro

# Abbreviations

| | |
|---|---|
| AMLCD | Active Matrix Liquid Crystal Display |
| AMOLED | Active Matrix Organic Light Emission Diode |
| CEMOP | *Centro de Excelência em Microeletrónica, Optoelectrónica e Processos* |
| CENIMAT | *Centro de Investigação de Materiais* |
| CTE | Constant of Thermal Expansion |
| EDS | Energy-dispersive X-ray spectroscopy |
| e-skin | Electronic skin |
| IGZO | Indium Galium Zinc Oxide |
| IKTS Fraunhofer | *Institut für Keramische Technologien und Systeme Fraunhofer* |
| K25 | Kapton with thickness 25 μm |
| K50 | Kapton with thickness 50 μm |
| K75 | Kapton with thickness 75 μm |
| NSP | Neutral Strain Plane/Point |
| PEN | Polyethylene Naphthalate |
| PET | Polyethylene Terephthalate |
| PI | Polyimide |
| PVD | Physical Vapour Deposition |
| RF | Radio Frequency |
| RIE | Reactive Ion Etching |
| SE | Secondary Electrons |
| SEM | Scanning Electron Microscope |
| SEM-FIB | Scanning Electron Microscope – Focused Ion Beam |
| TEM | Transmission Electron Microscope |
| TFT | Thin Film Transistor |
| XRD | X-Ray diffraction |

# Symbols

| | |
|---|---|
| b | position of NSP |
| $C_i$ | Intrinsic capacitance |
| d | crystal lattice distance |
| $d_f$ | film thickness |
| $d_s$ | substrate thickness |
| $I_D$ | Drain Current |
| $I_G$ | Gate Current |
| $I_{on}/I_{off}$ | Ratio between On Current and Off Current |
| L | Channel Length |
| n | number of layers |
| R | Bending Radius |
| $R_0$ | Radius at unstressed state |
| Tg | Vitreous Transition Temperature |
| ti | thickness of individual layer |
| tj | sum of thickness of all layers before individual layer |
| $V_{DS}$ | Voltage between drain and source |
| $V_{GS}$ | Voltage between gate and source |
| $V_{on}$ | Turn-on Voltage |
| $V_T$ | Threshold voltage |
| W | Channel width |
| Y | Young Modulus |
| $Y_f$ | film Young Modulus |
| $Y_i$ | individual layer's Young Modulus |
| $Y_s$ | substrate Young Modulus |
| z | distance from the neutral plane |
| α | coefficient of thermal expansion |
| ε | strain |
| $\eta_1$ | ration between thickness of substrate and film on top layer |
| $\eta_2$ | ration between thickness of substrate and film on bottom layer |
| $\mu_{FE}$ | Field effect mobility |
| $\mu_{sat}$ | saturation mobility |
| ν | poisson ratio |
| σ | mechanical stress |

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# 1 Motivation and Objectives

The flexible electronics sector is now starting to gain momentum, particularly with the investment, by the consumer electronics industry, in flexible and curved phones and wearables. The benefits offered by this type of electronics with respect to weight, cost, ruggedness and portability make it a desirable area to invest [1, 2]. According to Grand View Research [3], it is forecasted that by 2024 the global flexible market will reach USD 87.21 billion globally. The growing trend in the Asia Pacific is shown in Figure 1-1, as an example.

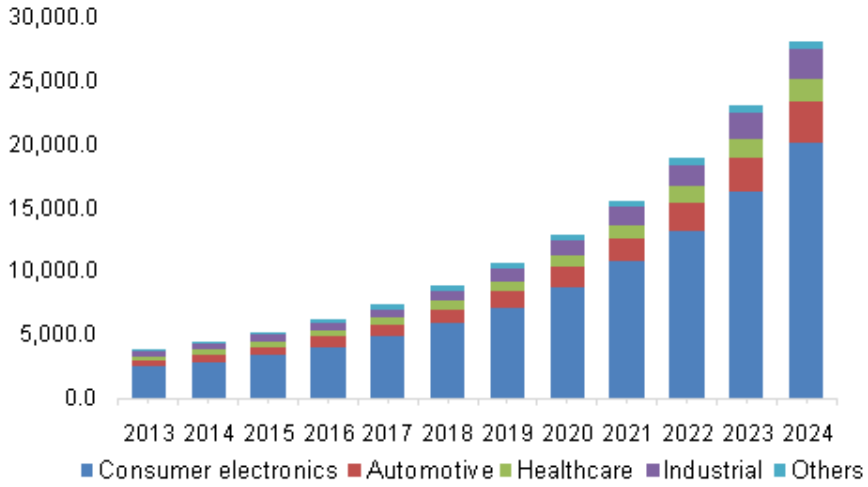


Figure 1-1: Market Forecast for Asia Pacific Flexible Electronics Market by Application (Consumer Electronics, Automotive, Healthcare, Industrial) (USD Million) until 2024 [3].

This work seeks to explore some of the characteristics of inorganic metal-oxide semiconductor thin film transistors (TFT) in flexible polymers under mechanical uniaxial strain, and it is inserted in the BET-EU European Project (http://www.bet-eu.eu) [4].

The main goal of this thesis is to fabricate TFTs with the best bendability possible, studying its layers mechanically and identifying critical ones. This is important because of the many advantages obtained with flexible electronics, with applications such as flexible TFTs [5, 6], bendable and rollable displays, flexible sensors [7, 8], RF tags [9, 10], electronic skin (e-skin) [11], and flexible solar cells [12].

To reach the already defined goals, several fabrication and characterisation techniques were employed, such as,

- Fabrication: sputtering, lithography, reactive ion etching (RIE), and lift off;
- Characterisation: electrical, mechanical (nanoindentation), and by microscopy (optical and SEM)

Throughout the work, fundamental choices were done regarding the fabrication of TFTs in substrates with different thicknesses, their characterisation using different bendability radii, and the nanoindentation to measure the mechanical properties of the TFTs' layers.

# 2 Flexible Electronics

Flexible electronics have gained more interest in the last years, with applications such as paper-like displays [13, 14], sensors/actuators [15], medical devices [16, 17], and radio frequency (RF) tags [9]. In the future, many electronic assemblies on rigid substrates will be replaced by mechanically flexible or even stretchable alternatives. The reason for this replacement is the qualities that flexibility can offer, such as bendability, conformability and elasticity, making flexible electronics generally lightweight, non-breakable, roll-to-roll and large area manufacturable [12, 16].

In the display industry, this trend is now starting, with LG creating a rollable television [18], and with curved displays already on the market. To achieve device flexibility, it is required the use of flexible components. In microelectronics, one of the most important building blocks is transistors. In this field, TFTs are gaining increasing interest due to ease of manufacture and low-temperature deposition compatible with polymer substrates [19]. These devices allow the drive of active matrix liquid crystals displays (AMLCDs) [20], and active matrix organic light emission diode (AMOLED) [14, 21]. However, they are also being used in applications such as X-ray [22, 23], temperature [24] and pH sensors [25, 26], wearable electronics, e-skin and memories [27].

## 2.1 Thin Film Transistors

A TFT is a field-effect transistor fabricated by depositing thin films of the constituent layers over a non-conducting substrate. These layers consist of an active semiconductor layer, the dielectric layer and metallic contacts. The semiconductor layer can be amorphous silicon, more conventionally used and well established, or an amorphous metal oxide semiconductor, which, although not as well established, can have good uniformity over large areas, is low temperature manufacturable, transparent, and can achieve mobilities much higher than amorphous silicon [28]. For the metal-oxide semiconductors, the indium gallium zinc oxide (IGZO) stands out as the most favourable material for oxide TFT applications, since it presents several advantages, such as high mobility, wide process window, and superior stability [29, 30].

Thin film transistors have different configurations regarding the position of the channel with respect to the metal contacts, staggered or coplanar, and regarding the position of the gate, being top or bottom gate. This creates four different configurations, each with its own set of advantages and disadvantages [31]. Complying with the most widely used configuration in display industry, this work will study staggered bottom-gate TFTs.

### 2.1.1 Operation of a TFT

A transistor operates in the on and off state and produces two main characteristic curves, called transfer characteristic curve and output characteristic curve, represented in Figure 2-1. If a sweep voltage is applied to the gate, the transfer characteristic curve is obtained. On the other hand, if the sweep voltage is applied to the drain, the output characteristic curve is attained.[32]

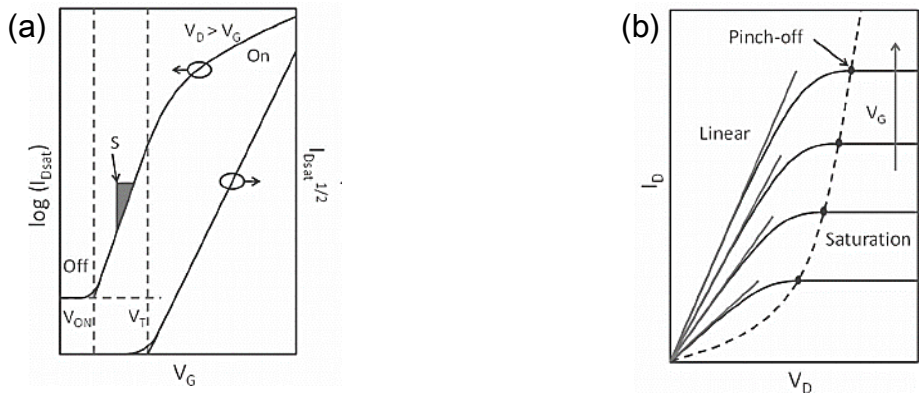


Figure 2-1: Characteristic curves of transistors: (a) transfer curves; (b) output characteristics [33].

When the transistor is in the off-state, the obtained current $I_D$ is very small, since the low or negative $V_{GS}$ (considering a n-type transistor) is unable to induce significant free charge accumulation close to the dielectric/semiconductor interface. The off state is then characterised as being the current before $V_{on}$ [32].

When the transistor is in the on-state, different operation regimes can be distinguished depending on the value of $V_{DS}$. When $V_{DS}<V_{GS}-V_T$, the TFT is in the pre-pinch-off regime (or linear regime for $V_{DS} \ll V_{GS}-V_T$). When $V_{DS}> V_{GS}-V_T$, the accumulation layer close to the drain region becomes depleted, leading to the saturation of $I_D$, known as saturation regime [32].

$$\begin{cases} I_D = C_i \mu_{FE} \frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] & if\ V_{DS} < V_{GS} - V_T \quad (1) \\ I_D = C_i \mu_{sat} \frac{W}{L}(V_{GS}-V_T)^2 & if\ V_{DS} > V_{GS} - V_T \quad (2) \end{cases}$$

In equations 1 and 2, $I_D$ is the drain current, Ci is the intrinsic capacitance, $\mu_{FE}$ is the field effect mobility, $\mu_{sat}$ is the saturation mobility, $V_{GS}$ is the gate voltage, $V_T$ is the threshold voltage, $V_{DS}$ is the drain voltage, and W and L are the width and length of the channel, respectively.

## 2.2 Mechanical Properties

When an external force is applied to an object made of elastic materials, it changes the shape and size of the object, making it is possible to measure the strain and the stress associated. The strain is the relative change in shape or size of an object due to externally applied forces (dimensionless), and stress is the internal force (per unit area) associated with strain (Force per unit length) [34].

For flexible electronics, where the mechanical bending is a required function, the mechanical properties of the constituent layers are very important to consider when projecting a device. In this case, the most important mechanical properties are the ones that define the elastic region, such as the Young modulus, since the device needs to be restored to its original position after mechanical stress. However, for plastics, it is also necessary to consider viscosity, creep rate and damping. Mechanical properties, such as hardness, fracture strength, fatigue resistance and wear, define the plastic region and are important to understand the failure of the device [34]. Figure 2-2 shows the relationship between strain and stress where the plastic and elastic regions are evidenced.

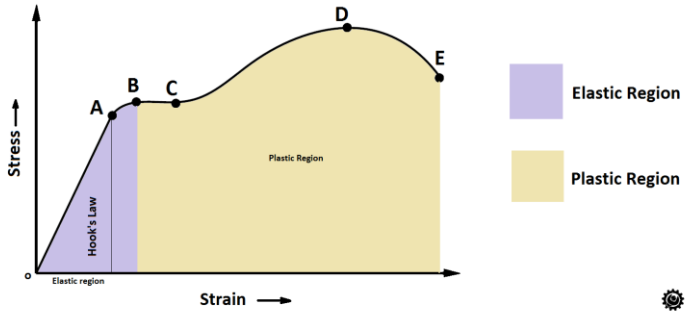


Figure 2-2: Stress vs Strain graph of a material: A defines the elastic limit, B defines the upper yield stress point, C is the lower yield stress point, D is the ultimate stress point, and E is the breaking or rupture point [35].

Within the elastic region, Hooke's law (in Figure 2-2, from 0 to A) relates the behaviour between the strain and the stress, as shown in equation 3, where σ is the stress, ε is the strain, and Y is the Young Modulus [34]. This way, it is possible to obtain the Young modulus by its slope.

$$\sigma = Y\varepsilon \quad (3)$$

Following the growth of the film material, changes in its physical environment induce extrinsic stress. The most common ways of inducing extrinsic stress are the mismatch between the **coefficients of**

**thermal expansion between bonded elements when temperature changes,** piezoelectric response to an electric field, electrostatic forces, gravitational or inertial forces, compositional segregation by bulk diffusion, electromigration, chemical reactions, stress-induced phase transformations, and **plastic or creep deformation** [36]**.**

### 2.2.1 Substrates of Choice for Flexible Electronics

Plastic or thin metal foils are the most widely chosen substrates for flexible electronics, having the thickness and conformability necessary for these applications [37]. However, it is possible to obtain flexible devices, like curved displays, from a very thin glass [38].

Polymeric foils are extremely attractive, since they can be made lightweight and low cost. The most used ones are polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polyimide (PI) [19, 37]. In the last years, PI has been the polymer of choice for the substrate in ultra-flexible devices. Its properties, such as a very low (CTE) coefficient of thermal expansion, a high glass transition temperature (Tg), as high as 300 °C, and the possibility of fabricating this layer by spin coating, makes it the best choice for the basis of these devices [39].

### 2.2.2 Compression and Tension

Bendability and conformability are important requirements for flexible electronic systems. As such, it is imperative to study the mechanical behaviour of the samples composing these systems. Bending can be uniaxial or biaxial. In the former, the sample is bent in one direction and the sample suffers tension or compression, while for the latter, the sample is subjected to strain in two directions [40].

For this work, only the uniaxial bending is considered. The uniaxial strain can be compressive or tensile, depending on the position of the sample in the bending environment, as shown in Figure 2-3 (a) and Figure 2-3 (b), respectively.

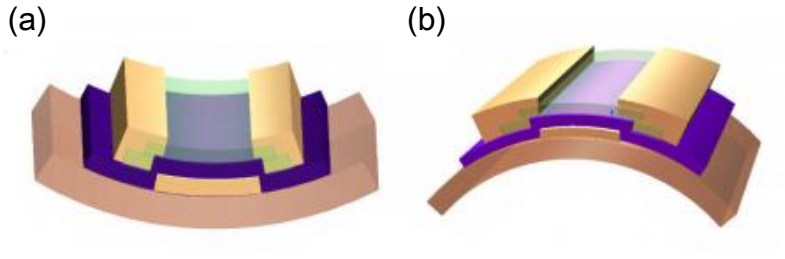


Figure 2-3: Graphical representation of TFTs under uniaxial strain, (a) under compression, (b) under tension [19].

These two different bending conditions give rise to different problems in the devices. Commonly, thin films subjected to **compression** fail due to debonding and delamination, Figure 2-4 (a), caused by poor adhesion between the constituent layers of the device. When subjected to **tension**, the main failure is due to cracking, Figure 2-4 (b), which appears parallel to the bending direction.


Figure 2-4: General failure mechanisms (a) under tension; (b) under compression [41].

Due to these different failure mechanisms in the different bending conditions, the strain at which the failure of the TFT occurs is different for each one. Regarding a-Si TFTs on polyamide substrates, the

strain necessary for definitive mechanical failure is much higher in compression than tension, around 0.3 % for tension [41].

### 2.2.3 Improving Mechanical Properties

Since TFTs have a critical strain, attempts have been done to reach the critical strain at increasingly smaller radii. Some simple methods to achieve ultra-flexibility are the use of thinner substrates, the choice for the constituent layers with smaller Young modulus and passivation layers.

State of the art methods includes double gate TFT structures [42], nanowires[43], mesh and strip patterning layers [44], seen in Figure 2-5, and locating the TFTs close to the neutral bending plane [45].

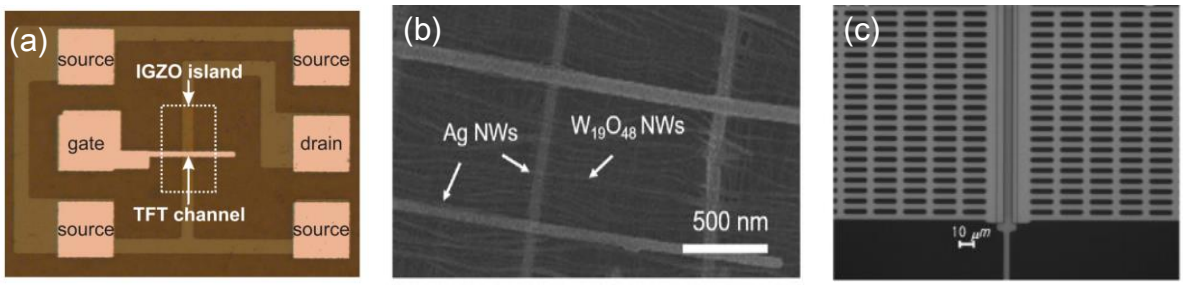


Figure 2-5: Examples of state of the art methods for better TFT flexibility: (a) double gate TFT structures [42]; (b) nanowires [43]; (c) mesh and strip pattering layers [44].

#### 2.2.3.1 Substrate Thickness

In microelectronic and nanoelectronic devices, the substrate's thickness is generally a lot higher than the one of the film or device, meaning it is the most important characteristic for achieving lower bending radius, as shown in equation 4.

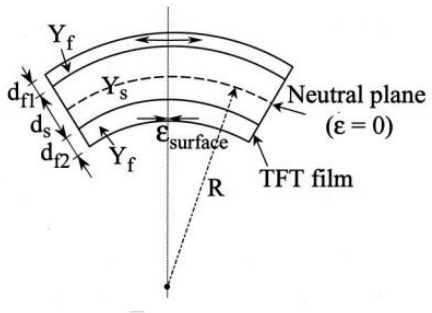


Figure 2-6: Schematic of a bended system used to understand the equation 4, the top layer is under tensile strain and the bottom layer is under compressive strain [40].

Young modulus (Y) can be used to determine the strain (ε) experienced by any TFT device as a function of bending radius and film thickness, shown below, where the position of the top and bottom layer is schematised in Figure 2-6,

$$\varepsilon_{surface} = \left(\frac{1}{R} \pm \frac{1}{R_0}\right) \cdot \frac{d_s + d_{f1} + d_{f2}}{2} \cdot \frac{\chi(\eta_1^2 + \eta_2^2) + 2(\chi\eta_1 + \chi\eta_1\eta_2 + \eta_2) + 1}{\chi(\eta_1 + \eta_2)^2 + (\eta_1 + \eta_2)(1 + 1\chi) + 1} \quad (4)$$

where R is the radius of curvature, $R_0$ is the radius of curvature of the structure before applying any external bending moment, and $\chi = Y_f / Y_s$ $\eta_1 = d_{f1}/d_s$ and $\eta_2 = d_{f2}/d_s$, characterize the top or bottom surface of the substrate, respectively. Likewise, $d_s$, $d_{f1}$, and $d_{f2}$ are, respectively, the thicknesses of substrate, stiff film on top, and stiff film on bottom. When decreasing $d_s$, keeping all the other parameters constant, $\epsilon_{surface}$ also decreases.

In conclusion, with decreasing R and increasing $d_s$, the strain $\varepsilon_{surface}$ increases.

### 2.2.3.2 Neutral Strain Plane

A common method for improving the mechanical performance of TFTs is by introducing a passivation layer to achieve the neutral strain plane. In theory, if one sandwiches the TFTs between two equal layers of thin films, the tension and compression forces exerted on the bottom substrate will be annulled by the top substrate. This means that the tension and/or compression forces exerted during the bending will not have any influence on the devices they are protecting.

The position b of the neutral mechanical plane (NMP), zero strain position of a multilayer stack with the $n^{th}$ layer on top of the substrate at the bottom, is given by [45],

$$b = \frac{\sum_{i=1}^{n} Y_i t_i \left[\sum_{j=1}^{i} t_j - \frac{t_i}{2}\right]}{\sum_{i=1}^{n} Y_i t_i} \tag{5}$$

where n is the number of layers, $Y_i$ is the Young modulus, $t_i$ is the thickness of each individual layer and $t_j$ is the sum of thickness of all layers before individual layer.

Even if the neutral strain point can be determined, it is generally known that if one puts a passivation layer of the same thickness on top of the stack, the NMP is much closer to the stack and the strain is reduced. However, to get the smallest bending possible, it is essential to know the weakest layer, and ideally put the neutral mechanical plane in that layer.

For the calculation of the engineering strain $\varepsilon_{eng}$ using the NSP position the equation 6 can be used,

$$\varepsilon_{eng} = \frac{z}{R} \tag{6}$$

where R varies linearly with the distance z from the neutral plane, where z is the distance between the position where we want to calculate the strain, generally the last layer of the device, and the NMP position,b.

### 2.2.3.3 Bending radius obtained for TFTs

In the last years, studies have been performed to analyse the smaller bending radius obtained for IGZO - TFTs. Table 2-1 summarizes some of the results obtained in other works for TFTs.

Table 2-1: Comparison between results obtained from different works considering substrate thickness and bending radius obtained before critical failure

| substrate | Bending mode | Bending radius (mm) | reference |
|---|---|---|---|
| 50 μm PI | tensile | 5 | Petti et al, 2015 [46] |
| 20 μm PI | tensile | 100 | Zhang et al, 2017 [47] |
| 17 μm PI | tensile | 1.5 | Park et al, 2016 [48] |
| 10 μm PI | tensile | 2.6 | Honda et al, 2015 [49] |
| 1.5 μm PI | Tensile/compression | 0.25 | Yong-Hwan et al, 2016 [45] |
| 1 μm parylene | tensile | 0.05 | Salvatore et al, 2016 [50] |

Considering the Table 2-1, it is necessary lower thicknesses to achieve smaller bending radius. However, the fabrication of IGZO TFTs using less than 10 μm thick substrates is very difficult. Because of this, the study of an IGZO TFT stack to achieve bending radius of 1.25 mm with thicker substrates (≥25 μm) is important to consider.

# 3 Materials and Methods

## 3.1 Fabrication Process

To accomplish the established goals, two different types of samples were fabricated: firstly, samples of unpatterned layers of Mo, IGZO, parylene and the TFT multilayer, deposited on glass and polymeric substrates; secondly, samples of working TFTs, deposited on polyimide and glass substrates, as term of comparison, analysing polymer's effect on the TFT.

### 3.1.1 Materials

The used substrates were *Corning Eagle XG glass* (1 mm thick), PEN Q51 (125 μm thick), and *Kapton* HN with three different thicknesses (75, 50 and 25 μm), the last two being from *Dupont*. The molybdenum layer was deposited in a RF Magnetron Sputtering *PVD AJA ATC 1800S*, with a molybdenum target from *AJA International*. The IGZO, from *AJA International* with composition 1:1:1 ($In_2O_3$:$Ga_2O_3$:ZnO molar ratio), and the dielectric multilayers were deposited in a deposition system RF magnetron sputtering *PVD AJA ATC 1300F*. The multilayer dielectric was deposited using $Ta_2O_5$ and $SiO_2$ targets from *AJA International*. The parylene C was deposited from a *Specialty Coating System Model PDS 2010 Labcoter 2* [51].

### 3.1.2 Thin Film Transistors

The first step for fabricating the TFTs is annealing, at 180 °C during 1 hour, of the polymeric substrate while free standing. The primary reason for this thermal treatment is the removal of residual stresses, strains and shrinkage of the polymer foils before processing to mitigate the layer-to-layer misalignment [52, 53].

After the annealing, the polymer substrate is glued to a carrier glass. The glue is a resin that is spin coated on to the glass, and after it has the substrate on top is cured. This step is necessary because it allows an easier handling of the sample during processing, and for a better uniformity of the deposited layers.

After the substrate is glued to the carrier glass, the substrate is once again annealed at 180 °C for 1 hour, and cleaned in ultrasounds for 15 minutes, with acetone and isopropyl alcohol. After this step, the substrate is once again heated at 120 °C for 20 minutes, to ensure that any cleaning agent is evaporated from the substrate.

The Mo is deposited for 13 minutes in an Ar atmosphere, with a power of 175 W and pressure 1.7 mTorr. Photolithography is then used to do the patterning of the gate electrode. The positive photoresist (AZ6632) is spin coated on top of the substrate, at 2000 rpm for 90 s. After it is cured at 115 °C for 1 min 15 s, the exposition of the photoresist with the desired pattern is done. The photoresist is developed with a metal ion free developer (AZ 726 MIF) and washed twice using water, to ensure that the unwanted resist is no longer on the substrate. The Mo layer is etched, using a Reactive Ion Etching (RIE) system, *TRION PHANTOM III RIE*, and a $SF_6$ gas, during 210 s [54].

The dielectric multilayer is then deposited, having seven layers made of $SiO_2$ and $Ta_2O_5$:$SiO_2$ repeated consecutively in an Ar+O (14:1) atmosphere, power of 150 W and 100 W for $SiO_2$ and $Ta_2O_5$, respectively with a chamber pressure of 2.3 mTorr. All layers are patterned by photolithography and RIE etched, using $SF_6$ gas for 660 s [54].

After the dielectric, the IGZO is the next patterned layer. Since the IGZO pattern is done by lift-off, the photoresist is spin coated, exposed and developed before the deposition of the IGZO. After the deposition, with a duration of 13.5 minutes in an Ar+O (14:2) atmosphere, power of 100 W and pressure of 2.3 mTorr, and for the lift-off of the unnecessary photoresist, acetone is used [54].

To pattern the last contacts, source and drain, a Mo layer was used. The deposition and etching are done similarly to the gate electrodes [54].

For the passivation of the K75 and K25 samples, 1.8 g, 9 g and 40 g parylene layers are deposited on the parylene system, to achieve thicknesses of 1 μm and 5 μm and 22 μm, respectively.

A schematic of the fabrication steps of these devices can be seen in Figure A-0-1and Figure A-0-2

## 3.2 Characterisation Methods

This work includes the study of TFT's mechanical behaviour and influence on bending conditions and electrical and mechanical characteristics of the devices.

For samples characterisation, a broad range of tools were used, aiming to study their structural, morphological, compositional, optical, electrical and mechanical properties. Among these, the compositional, structural and mechanical analyses of the individual layers, as well as the multilayer system, were performed at *IKTS-Fraunhofer*, in the framework of the BET-EU European project.

The samples' mechanical characterisation was done by nanoindentation, using system *Hysitron TI 950 Triboindenter®*. For the simple nanoindentation experiment, where simple mechanical properties of the layers, such as Young Modulus and Hardness, can be acquired, individual samples of 2.5 × 2.5 cm of glass with Mo (400 nm), IGZO (400 nm), Parylene (500 nm and 1 μm) were used and indented with a *Berkovitch* tip. These samples were also annealed at 140 ºC and 180 ºC, to understand how the temperature influences the mechanical properties of the individual layers. Delamination experiments were also performed on the multilayer samples on the glass with a wedge indent. Cross sections of the indents were performed in a *Carl Zeiss SEM/FIB NVision 40*.

A *Carl Zeiss Libra 200 TEM* with *EDS* was used to understand the structure of the multilayers and the influence of temperature on the multilayer structure. Regarding TEM characterisation, lamellas of the samples with a very small thickness were produced, using an *FEI Helios NanoLabTM 660 SEM*.

The calculation of the coefficient of thermal expansion of the polybdenum was deposited on silicon with 400 nm thickness.

The roughness of the polyimide substrates was calculated from the 3D scanning of the surface of the substrates with a profilometer, *Ambios XP-Plus 200 Stylus*, where the scanning of the sample was achieved on an area of 0.5 mm × 0.5 mm with a space of 0.3 μm between lines. The samples were on a glass support with Kapton tape.

The electrical characteristics of the TFTs were obtained using a semiconductor parameters analyser (*Agilent 4155C*), linked to a microprobe station (*Cascade Microtech M150*).

The electrical characterisation of the TFTs in bending and compression was also obtained, using shapes with bending radii of 45 mm, 25 mm and 15 mm.

To see the propagation of the cracks, cross-section was performed on the multilayer system, using *SEM Zeiss Auriga CrossBeam System*. Also, an optical microscope Olympus BX51 from Zeiss was used to obtain images of the studied system.

For the mechanical characterisation of the TFTs under tensile strain with radii from 10 mm to 1.25 mm, bending cycles were done with a 3-point-bending system, fabricated in *CEMOP*. To achieve very small radii, some parts were designed to adapt to the system, shown in appendix B.

# 4 Results and Discussion

In this chapter, the results obtained from the individual layers, multilayer system and the transistors' characterisation are shown and discussed, as well as the theoretical approach for achieving lower bending radius, used as a guide work.

## 4.1 Multilayer Properties

The developed work focuses on the properties of a TFT, meaning the understanding of the multilayer's composition is of major importance. Also, the interface between the surface can be an indicator of the adhesion between the different layers. A bad adhesion between the layers can diminish the reliability of the system. However, as seen in the TEM Figure 4-1, the layers appear to have a good interface, with overall uniformity.

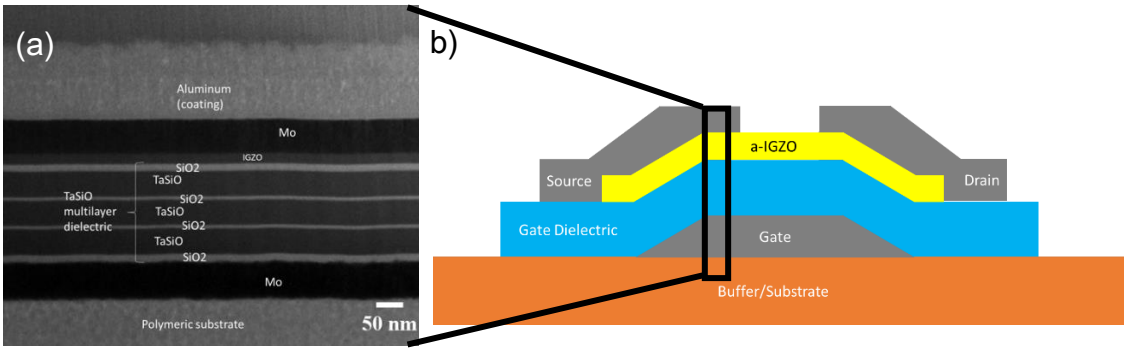


Figure 4-1: Multilayer System of the TFT: (a) TEM image; (b) schematic of the cross-section of the TFT.

The compositional characterisation of each layer was done using TEM EDS, also obtaining the graphs of Figure C-1, from Appendix C. The graphs show all the layers that compose the TFT and were necessary for the label of each layer, on Figure 4-1. However, a peak of copper is aparent in all the deposited layers, due to the support used for handling the sample.

Since the TFTs are annealed 180 °C for 1 hour, to achieve a better performance, the influence of the temperature on the multilayer system was studied.

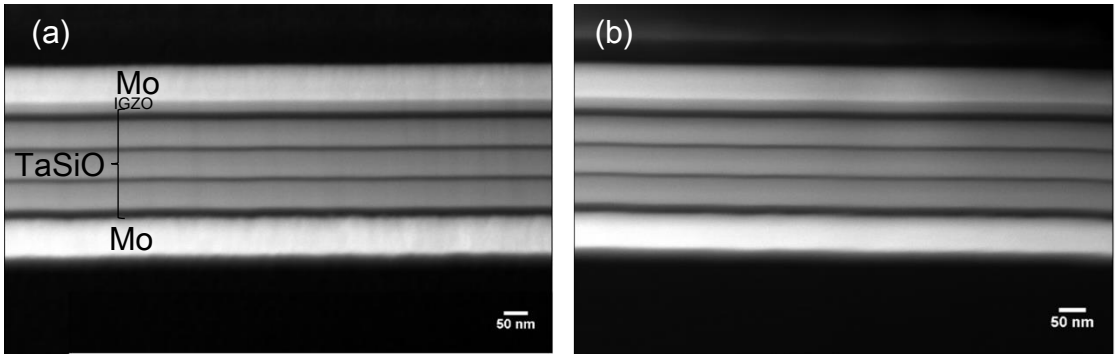


Figure 4-2: TEM image of the multilayer system: (a) without annealing; (b) with annealing at 180 °C for 1 hour.

From analysing Figure 4-2, it is possible to infer that temperature does not influence the multilayer in a major way. Scenarios like diffusion of metal atoms, debonding or cracking, due to the mismatch in the layers' coefficient of thermal expansion before bending, are not evident. This multilayer system is then a good starting point in the investigation of this stacked layers under mechanical stress. Analogous to the multilayer without the passivation layer, the parylene passivation layer does not influence the TFTs, as seen in Figure D-1, from appendix D.

### 4.1.1 Coefficient of Thermal Expansion (CTE)

Since TEM images do not show any cracks due to thermal annealing of the sample, the stress due to the mismatch between the different CTEs gathered in the layers was not relieved [55]. The molybdenum studied is a pure polycrystalline material when sputtered, and so an in-situ X-ray diffraction at different temperatures was performed on the Mo layer.

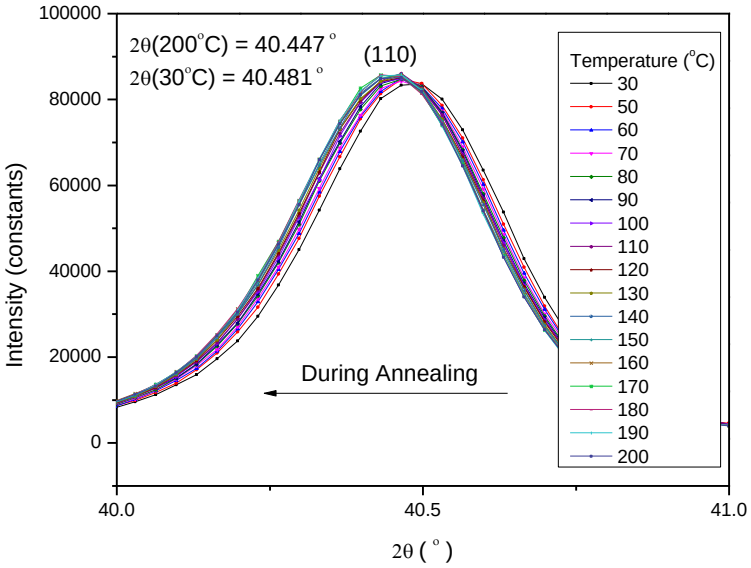


Figure 4-3: In-situ XRD of molybdenum under heating from 30 °C to 200 °C.

The Mo layer during the annealing dilates as expected. Because of the dilation of the crystal lattice, it is possible to determine the CTE of the molybdenum, according to Equation 7.

$$strain = \frac{\Delta d}{d} = \alpha \Delta T \tag{7}$$

Considering the 2θ values shown in the graph from Figure 4-3, that ΔT = 170 °C, $\lambda_{Cu}$=1.516 Å, and that the crystallographic plane is (110), the determined CTE of the Molybdenum is α = 4.7 ppm/°C, as predicted by the literature [56]. The in-situ DRX was made using only molybdenum, since it is a polycrystalline material, with a very defined peak. Table 4-1 shows the different CTE values for each layer.

Table 4-1: Coefficient of thermal expansion of the different layers in the TFT multilayer structure.

| Material | CTE ($10^{-6}$/°C) | material | CTE (ppm/°C) |
|---|---|---|---|
| PEN [57] | 20.0 | $SiO_2$ [58] | 0.7 |
| PDMS [59] | 301.0 | $Ta_2O_5$ [60] | 3.0 |
| Kapton [61] | 20.0 | IGZO [62] | 5.2 |
| molybdenum | 4.7 | Parylene [63] | 35.0 |

Although mechanical properties, such as hardness and Young modulus, change for thin films, the intrinsic characteristic of this layer behaves as expected. The obtained value of CTE for the

molybdenum is one of the most important factors in choosing this material as an electrode in transistors [64].

## 4.2 Mechanical Properties of Individual Layers

For a better understanding of mechanical properties of thin films layers of Mo and IGZO, nanoindentation was performed. These measurements were not done on the dielectric layers, given the very high deposition time needed to reach the necessary 400 nm. However, $SiO_2$ layers have been thoroughly studied in other works.

### 4.2.1 Molybdenum and IGZO Layers

For a better mechanical reliability of the system, it is important to determine mechanical properties of the individual layers of IGZO and Molybdenum, like Young modulus and hardness. Figure 4-4 shows the graphs obtained from the nanoindentation done on the IGZO and molybdenum layers. Since the layers in this study where 400 nm, various indentations where performed in the layer, until a penetration depth of 40 nm, correpondent to 10 % of the thickness of the layer, was achieved.

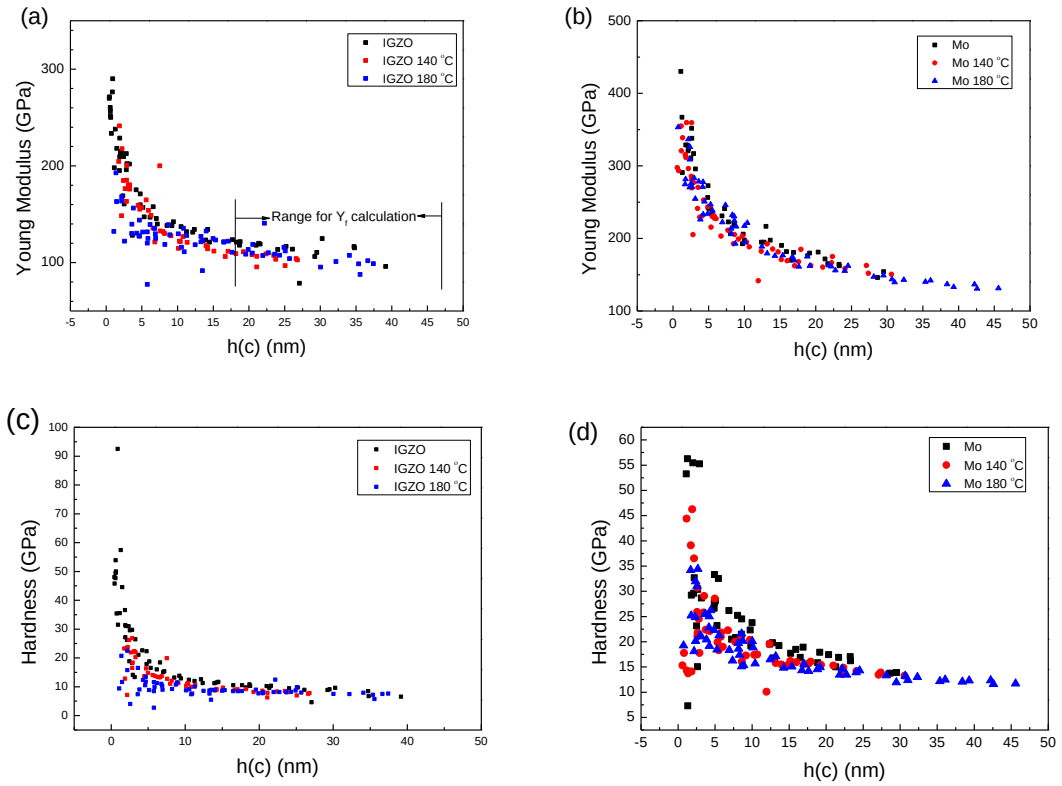


Figure 4-4: Nanoindentation measurements for Young Modulus and hardness: (a) Young modulus of IGZO as deposited, annealed at 140 °C and annealed at 180 °C; (b) Young modulus of molybdenum as deposited, annealed at 140 °C and annealed at 180 °C; (c) hardness of IGZO at the same temperatures; (d) hardness of Mo at the same temperatures.

From the anaylsis of the graphs, the values for Young modulus and hardness reach a *plateu*, starting at around 15 nm of penetration depth. The average values,obtained from the interval hc = [15,40] on Table 4-2, were then obtained.

Table 4-2: Young Modulus and Hardness obtained with nanoindentation in 400 nm thick IGZO and Molybdenum Layers, as deposited, annealed 1 hour at 140 °C and annealed 1 hour at 180 °C.

| | | Young Modulus (GPa) | Hardness (GPa) |
|---|---|---|---|
| IGZO | As deposited | 116.5 ± 6.9 | 9.5 ±1.3 |
| | 140 °C | 112.6 ± 23.2 | 9.0 ± 2.9 |
| | 180 °C | 111.3 ± 11.8 | 8.3 ± 1.2 |
| Molybdenum | As deposited | 171.0 ± 12.4 | 16.6 ± 1.6 |
| | 140 °C | 167.1 ± 10.4 | 15.2 ± 1.6 |
| | 180 °C | 159.8 ± 14.7 | 13.3 ± 1.2 |

The values for the layers' mechanical properties, before and after annealing, are slightly different, as observed in Table 4-2, showing a decrease in both Young modulus and hardness, with a bigger difference in the Molybdenum layer. Nevertheless, the values obtained for before and after annealing are in the interval obtained from the standard. The measured value obtained through nanoindentation of the Mo layer shows a considerable difference from the bulk value of 329 GPa [64], observed in literature, which is explained by the very low thickness of the studied layer. For very thin layers, the mechanical properties are dependent on surface factors, unlike what happens in bulk specimens. Nonetheless, since a lower Young modulus is preferred for better bendability of a system, this difference in values is desired.

However, after performing an XRD-diffraction from the same sample as deposited and after annealing at 180 °C for 1 hour, as shown in Figure 4-5, the crystal lattice does not return to the original state, which can also explain the decrease in Young modulus and hardness values after annealing. From the XRD-diffraction it is possible to obtain the crystallites' size, for each sample, before and after annealing, through the Scherrer equation [65]. The obtained values were 27.39 nm and 28.36 nm for the as-deposited and annealed sample, respectively. The increase in crystallites' size in the annealed samples explains the decrease in Hardness of the films. According to the Hall-Petch relationship, the decrease in particle size increases the Hardness, as obtained by the nanoindentation measurements [66].

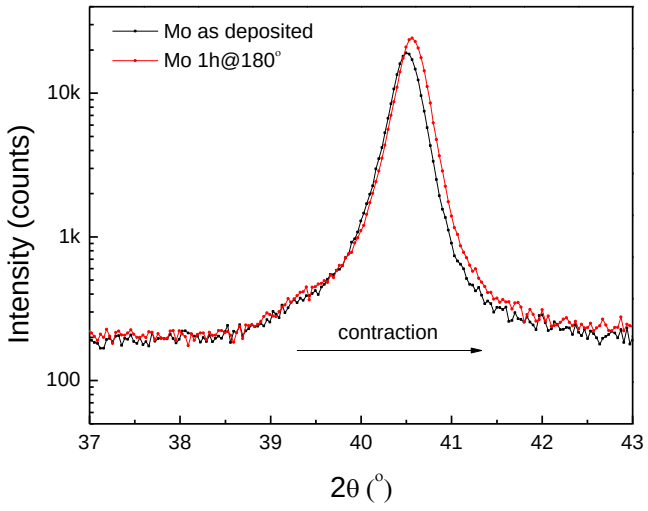


Figure 4-5: XRD of molybdenum sample as deposited (black) and after annealing (red).

### 4.2.2 Parylene Layer

Annealing of the parylene layer dramatically changes the mechanical behaviour, which is expected, since it is a semicrystalline material. During the wedge indentation, the indent is scanned, as seen by the change in indent in Figure 4-6. In the non-annealed sample, the layer is very conformal, while in the annealed one the parylene becomes more rigid. According to Equation 4, it may be possible to work with this property to have a more reliable device.

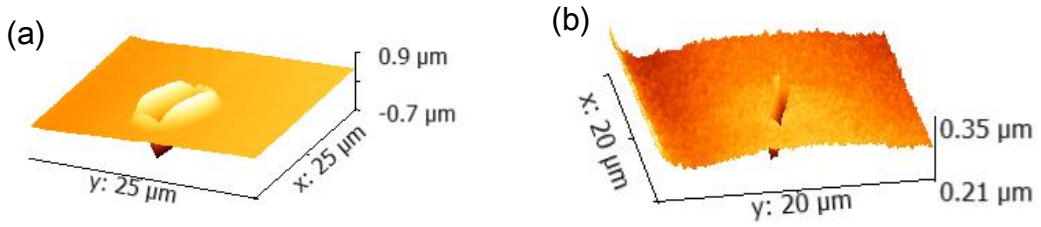


Figure 4-6: Wedge indent on multilayer with 1 µm parylene passivation (a) as deposited; (b) annealed at 180 ºC.

## 4.3 Flexible Transistors

The thickness of the substrate is one of the main properties that influences the bending of the samples. In the beginning of this work a PEN foil was used, with a thickness of 125 µm. PEN is a transparent polymer, has a very uniform surface, and a transition temperature of 155 ºC [67]. However, because of the high thickness, the substrate is not able to support bending radius of less than 2.5 mm, as seen in Figure 4-7.

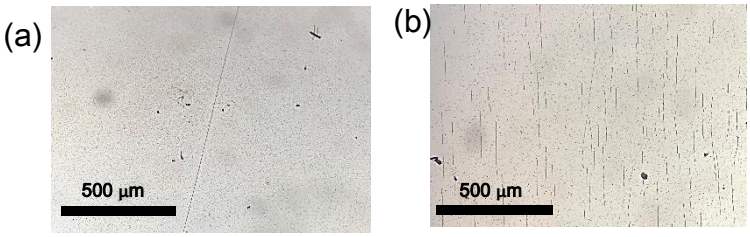


Figure 4-7: Optical microscope Images of Mo on PEN: (a) 10 cycles with bending radius of 2.5 mm; (b) 1 cycles with bending radius of 1.25 mm.

The substrate with a bending radius of 1.25 mm has plastic deformation (1 cycle), fracturing the top Mo layer. Since one of the goals is to be able to get the smallest bending radius possible, smaller thickness substrates were used. Kapton (polyimide) is a very thermally stable substrate (Tg > 300 °C), has lower CTE than other polymers, and can be purchased in smaller thicknesses, down to 25 µm. From here on, the 75 µm thick Kapton is referred as K75, 50 µm thick as K50, and 25 µm thick as K25.

Using Equation 4 and considering the datasheet values Y(PEN) = 5 GPa and Y(Kapton) = 2.5 GPa, the graph in Figure 4-8 can be obtained.

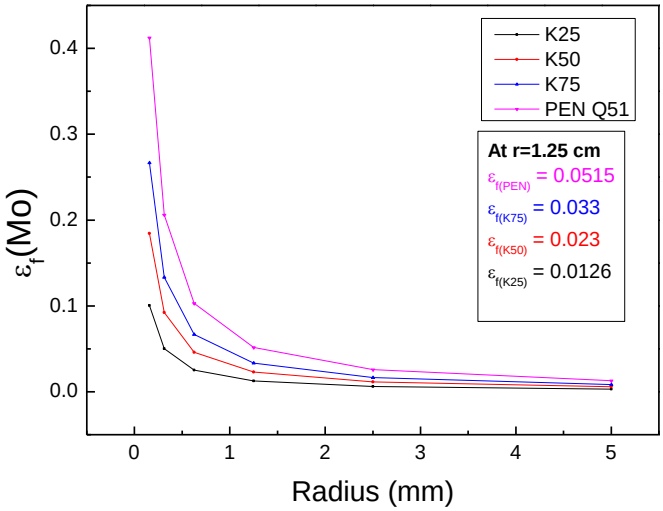


Figure 4-8: Strain on top of Mo depending on the bending radii: in black is K25, in red is K50, in blue is K75, and in pink is PEN with 125 µm.

PEN could not bend for the smaller radius, since the high values of thickness and Young modulus make it so that the strain on the top Mo layer is much higher than on the Kapton substrates, resulting in plastic deformation of the PEN substrate and, subsequently, causing the molybdenum to crack.

### 4.3.1 Kapton as a Substrate

The Kapton used as substrate is a commercially available polymer. The calculations requiring its properties relied on the datasheet [61]. However, characteristics like the roughness of the Kapton were measured using the profilometer, since its surface, shown on the optical microscope in Figure 4-9, was not smooth.

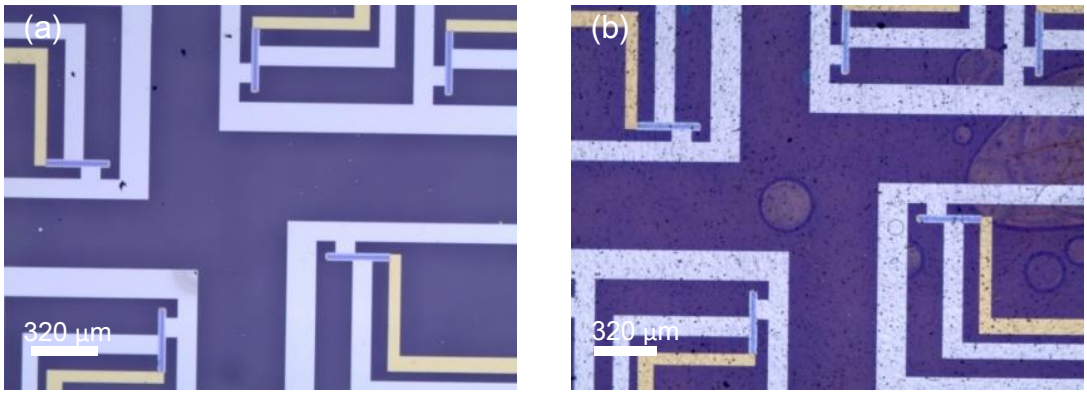


Figure 4-9: Optical microscope image of the TFTs fabricated on (a) glass substrate; (b) Kapton substrate.

As seen in the 3D measurements from Figure E-1, Figure E-2 and Figure E-3 (representative of the sample K75, K50 and K25, respectively), the surface is not totally flat, presenting peaks throughout the surface. From these 3D maps, it was possible to determine the average roughness of the substrate, which is presented in Table 4-3, for the several thicknesses.

Table 4-3: Roughness values for samples K75, K50 and K25.

| | K75 | K50 | K25 |
|---|---|---|---|
| Average Roughnes (nm) | 58 | 67 | 105 |
| RMS Roughnes (nm) | 95 | 94 | 128 |
| Peak to Valley Heigh (nm) | 2379 | 1388 | 1810 |

The obtained root mean squase (RMS) roughness is not the most ideal, especially on the thinnest substrate. However, this value is probably higher than the real one, due to the substrates' flexible nature. During the measurement, the substrates were not totally flat, meaning this could increase the measured roughness. For example, the 3D map of the K25 substrate, Figure E-3,in appendix E, shows with high probability the previous situation, since one of the corners is purple. Also, since transistors' dimensions of width and length are in the order of magnitude of micrometers, substrate's roughness creates pinholes that could possibly affect TFTs properties.

### 4.3.2 IGZO TFTs

To study the electrical properties of TFTs on the different substrates, and to characterise the influence of bending on the transistors, the characteristic curves of TFTs were determined. From them, the parameters of TFTs, such as the $I_{on}/I_{off}$ ratio, $V_{on}$, leakage current ($I_G$), hysteresis, mobilitiy ($\mu_{sat}$) and threshold voltage ($V_T$) were obtained.

The fabricated transistors have dimensions L = 20 μm and W = 320 μm (W/L = 16), a dielectric constant k = 17.3 [68], and are disposed in perpendicular orientations, as shown in Figure 4-10.

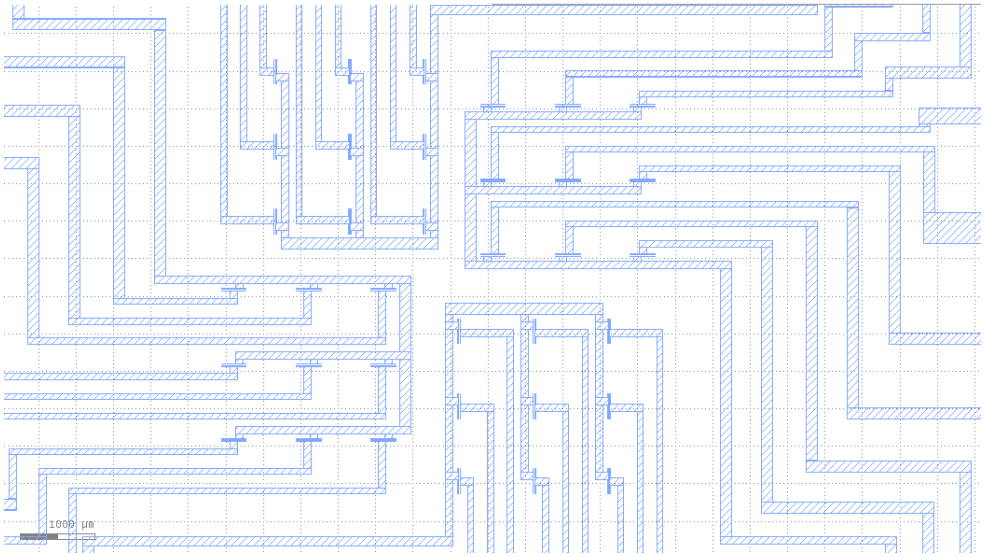


Figure 4-10: Disposition of transistors configuration on the substrate

The graphs (a) and (b) of Figure 4-11 present, respectively, the transfer curve in the saturation mode, $V_{DS}$ = 5 V, and the output of the transistors. The transistors in the different substrates present some differences, but are mostly similar, with overlaying curves.

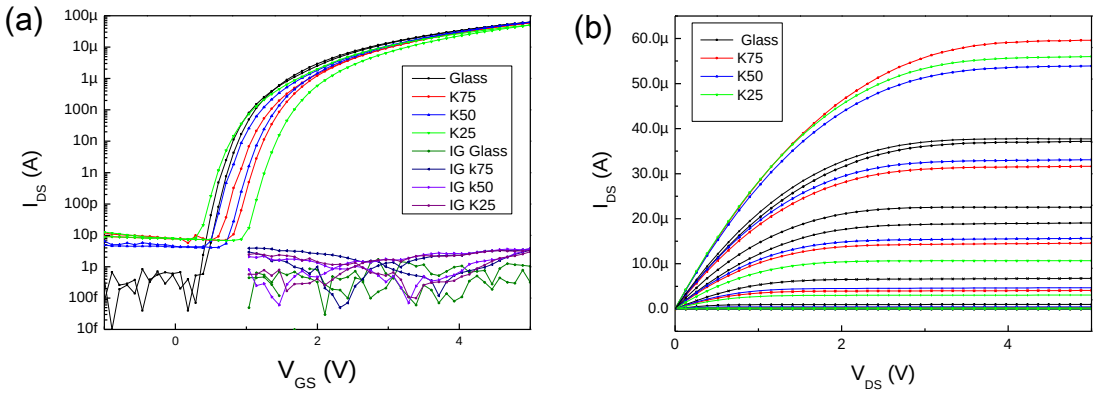


Figure 4-11: Characteristic curves of TFTs fabricated in Glass substrate (black), K75 (red), K50 (blue), and K25 (green): (a) Transfer characteristic curve, where the $I_G$ starts at 1 V for ease of comprehension of the graph, and (b) Output characteristic curve.

Table 4-4 summarizes the results for the parameters of the transistors in the different substrates. Comparing the results, it is possible to see that the $I_{on}/I_{off}$ of the glass substrate transistors is more than an order of magnitude higher than the Kapton ones, due to the higher surface roughness of the Kapton substrates. The $I_{on}/I_{off}$ is very similar between the Kapton substrate transistors. The leakage current increases with the decrease in thickness of the substrate. Nonetheless, it is still a very low value. The mobility of the transistors is around 6 $cm^2V^{-1}s^{-1}$, which is a lower value than the usually published ones in the literature, due to the IGZO used. The IGZO has the composition of 1:1:1 molar ratio, presenting less concentration of indium than other IGZO compositions, which is known to decrease the mobility [69].

Table 4-4: Summary of IGZO TFTs parameters, in glass and polymer substrates.

| | Glass | K75 | K50 | K25 |
|---|---|---|---|---|
| $I_{on}/I_{off}$ | $(2.3 \pm 4.3) \times 10^8$ | $(7.7 \pm 3.2) \times 10^6$ | $(11 \pm 5.9) \times 10^6$ | $(7.4 \pm 5.2) \times 10^6$ |
| $V_{on}$ (V) | 0.30 ± 0.15 | 0.51 ± 0.08 | 0.27 ± 0.23 | 0.26 ± 0.19 |
| $I_G$ (pA) | 2.1 ± 1.3 | 5.6 ± 3.9 | 35.0 ± 70.0 | 57.0 ± 120.0 |
| Hysteresis (V) | 0.12 ± 0.06 | 0.15 ± 0.06 | 0.46 ± 0.15 | 0.33 ± 0.00 |
| $\mu_{sat}$ ($cm^2V^{-1}s^{-1}$) | 5.9 ± 1.7 | 6.6 ± 0.3 | 6.3 ± 0.5 | 5.5 ± 0.6 |
| $V_T$ (V) | 2.95 ± 0.10 | 3.12 ± 0.06 | 2.97 ± 0.15 | 2.97 ± 0.10 |

Nonetheless, the transistors on Kapton substrates still have very good performances and are suitable for bending tests.

### 4.3.3 Iddle shelf Time

Since TFTs were fabricated in thick rigid glass substrates, and in flexible thinner substrates, the influence of time on their performance was studied, to understand if the different substrates yield different results with the aging of the devices.

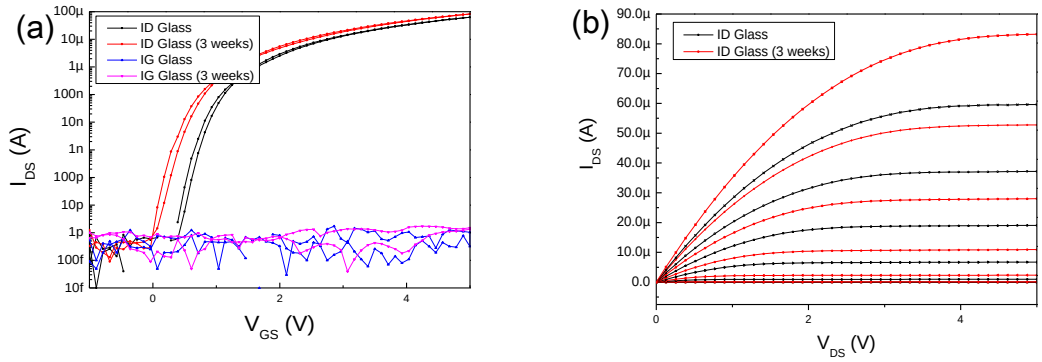


Figure 4-12: Characteristic curves of IGZO TFTs fabricated on corning glass right after production (black), and three weeks after production (red): (a) Transfer characteristic curve, and (b) output characteristic curve.

As seen in Figure 4-12, the transistors fabricated on glass shift to more negative values after three weeks. However, the performance of TFTs regarding $I_{on}/I_{off}$, $I_G$ and mobility, presented in Table 4-5, achieve better values since TFTs were aged in an air-based atmosphere. The IGZO semiconductor becomes more conductive with time, because of the desorption of the oxygen atoms in the metal-oxide-metal lattice [32].

Table 4-5: Summary of IGZO TFTs parameters fabricated on Corning glass after production and after three weeks, in an oxygen rich environment.

| | $I_{on}/I_{off}$ ($10^8$) | $V_{on}$ (V) | $I_G$ (pA) | Hysteresis (V) | $\mu_{sat}$ ($cm^2V^{-1}s^{-1}$) | $V_T$ (V) |
|---|---|---|---|---|---|---|
| Glass | 2.3 ± 4.3 | 0.30 ± 0.15 | 2.1 ± 1.3 | 0.12 ± 0.06 | 5.9 ± 1.7 | 2.95 ± 0.10 |
| Glass (3 weeks) | 6.3 ± 9.4 | -0.08 ± 0.18 | 1.6 ± 0.8 | 0.11 ± 0.00 | 6.6 ± 0.3 | 2.93 ± 0.09 |

However, unlike what happens with TFTs on a glass substrate, TFTs fabricated on a thin polyimide substrate have an increase in leakage current, that translated in a decrease of $I_{on}/I_{off}$, visually represented in Figure 4-13. This happens due to the higher gas permeability of the polyimide substrate, and because of the thinner nature of the flexible substrate regarding the glass substrate [12]. Nonetheless, when comparing the transistors regarding $V_{on}$, hysteresis, mobility and $V_T$, they present the same behaviour as TFTs on *corning* glass.

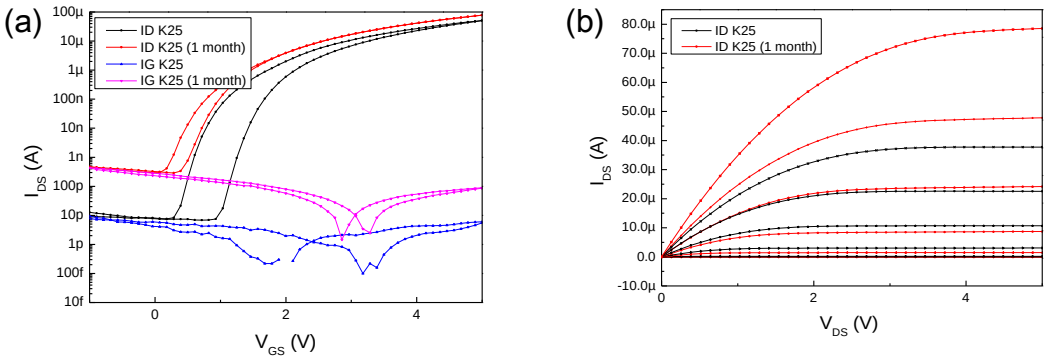


Figure 4-13: Characteristic curves of TFTs fabricated on a kapton substrate (25 µm) after fabrication (black) and after one-month (red): (a) Transfer characteristic curve, and (b) output characteristic curve.

Table 4-6: Summary of IGZO TFTs parameters fabricated on Kapton substrate (25 um), after production and after one month in an oxygenated atmosphere.

| | $I_{on}/I_{off}$ ($10^6$) | Von (V) | $I_G$ (nA) | Hysteresis (V) | $\mu_{sat}$ ($cm^2V^{-1}s^{-1}$) | $V_T$ (V) |
|---|---|---|---|---|---|---|
| K25 | 7.4 ± 5.2 | 0.26 ± 0.186 | 574 ± 12.3 | 0.33 ± 0.00 | 5.52 ± 0.56 | 2.97 ± 0.10 |
| K25 (after 1 month) | 0.8 ± 0.3 | 0.01 ± 0.06 | 4.2 ± 12.3 | 0.29 ± 0.09 | 6.26 ± 0.80 | 2.98 ± 0.08 |

### 4.3.4 Peel-Off (Metal Blade)

Since during the fabrication of the transistors, the substrate is glued to the glass, a peel-off process in necessary to have free-standing samples. In this substrate, the peel-off is done mechanically with a metal blade, since the resin used to glue the substrate to the carrier glass does not dissolve without compromising the layers of this samples.

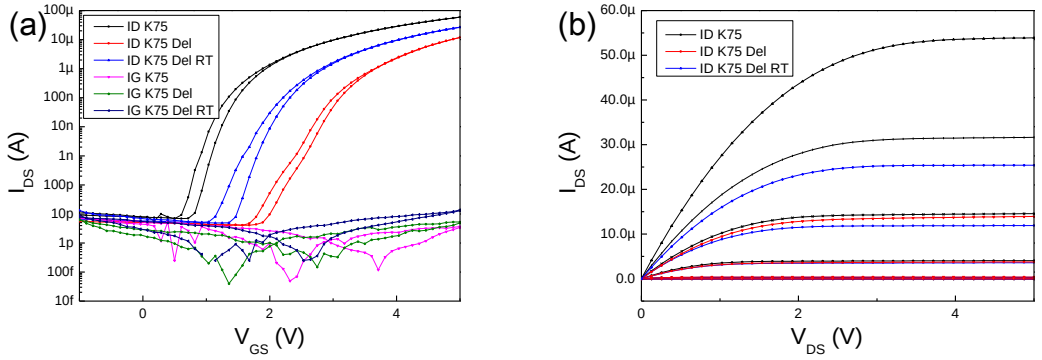


Figure 4-14: Characteristic curves of TFTs fabricated on a K75 glued to carrier substrate (black), after delamination (red) and after delamination and annealing (blue): (a) Transfer characteristic curve, and (b) output characteristic curve.

After the delamination, $V_{on}$ shifted to more positive values and the $I_{on}/I_{off}$ ratio diminished, as seen in Figure 4-14. However, the transistors, with the increase in time and thermal treatment, somewhat recuperated, achieving a better $I_{on}/I_{off}$ and shifting $V_{on}$ to less positive values. After analysing Table 4-7, it is seen that $I_G$ increased significantly after the delamination, and that both $I_G$ and hysteresis did not recover

Table 4-7: Summary of IGZO TFTs parameters, in the K75 substrate, before delamination, after delamination, and delamination and annealing.

| | K75 | K75 Delaminated | K75 Delaminated RT |
|---|---|---|---|
| Ion/Ioff | $(7.7 \pm 3.2) \times 10^6$ | $(3.7 \pm 3.4) \times 10^6$ | $(4.3 \pm 2.1) \times 10^6$ |
| Von (V) | 0.51 ± 0.08 | 1.39 ± 0.40 | 0.92 ± 0.22 |
| $I_G$ (pA) | 5.6 ± 4.0 | 73.7e ± 170 | 97.4 ± 234.9 |
| Hysteresis (V) | 0.15 ± 0.05 | 0.20 ± 0.04 | 0.27 ± 0.06 |
| $\mu_{sat}$ ($cm^2V^{-1}s^{-1}$) | 6.6 ± 0.3 | 5.3 ± 1.5 | 5.2 ± 0.4 |
| $V_T$ (V) | 3.12 ± 0.06 | 3.94 ± 0.33 | 3.62 ± 0.10 |

Although the peel-off process is not the most ideal, for 75 μm thick substrates it yields good results.

### 4.3.5 Bending

The transfer curves presented until now were determined while transistors were in a flat condition. Since this work focuses on the mechanical reliability of transistors under mechanical uniaxial stress, transfer curves of the transistors while under bending were made. The system uses moulds with radii 45, 25 and 15 mm. Given the location of the pads and the system in use, smaller radii were not possible to measure. In Appendix F, there are several pictures of the TFT matrix under a bending measurement with radius of 25 mm.

The bending tests were performed in sequence, starting from the highest radius to the lowest one. Measurements of the transistors characteristic curves while flat, between the different bending radius, were also done. The used sequence of measurements was: Flat 1, tension with radius of 45 mm (T45), compression with radius of 45 mm (C45), flat 2, T25, C25, flat 3, flat after 3 days (flat 3.1) and T15. For the measurements of the transistors when under bending, the direction of the channel regarding the bending direction was considered. In Figure 4-15, it is represented the position of the channel, while taking into consideration the bending direction.

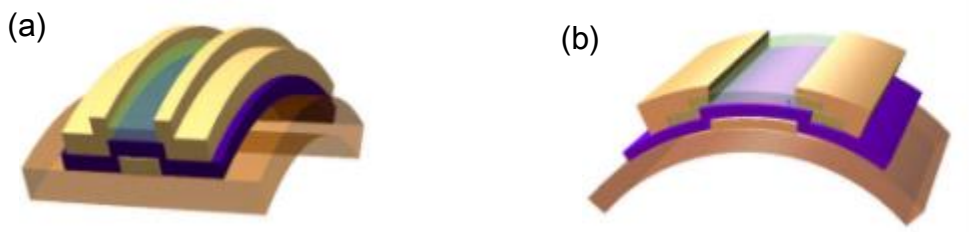


Figure 4-15: Position of channel regarding the bending direction: (a) channel length perpendicular to bending direction; (b) channel length parallel to bending direction [70].

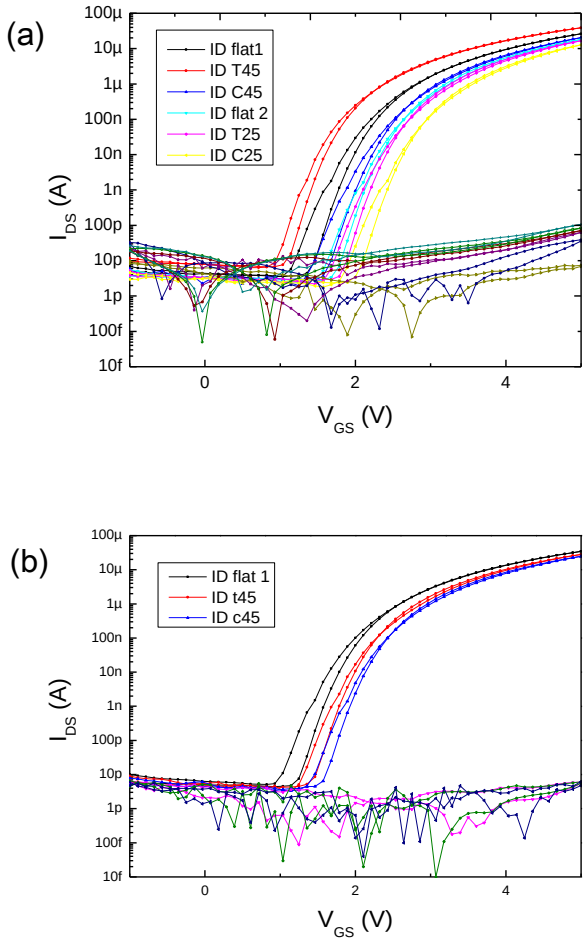


Figure 4-16: Characteristic curves of TFTs under bending with radii of 45, 25 and 15 mm: (a) transfer curve for TFTs with channel perpendicular to bending direction; (b) transfer curve for TFTs with channel parallel to bending direction

As it is possible to observe in the graphs of Figure 4-16, the transistors shift positively after each consequent measurement, both for when the channel is perpendicular, Table G-1, or parallel to the bending direction, Table G-2 in Appendix G, having no apparent pattern when the channel is under compression or tension. However, as the radius decreases, the performance of TFTs appears to degrade.

Measurements were made on the TFTs after three days, while flat (flat 3.1 on Table G-1 and G- 2), to see if the TFTs recover. In both occasions, this occurred with an increase in mobility and a negative $V_{on}$ shift, showing that the bending stress is reversible.

However, considering the measurements' sequence regarding the gradual diminish of bending radius and given the necessity of doing various measurements on the same transistors, TFT' operation changes could also be explained due to the bias stress, and not because of the decrease in bending radius. To test this hypothesis, measurements of TFTs were done randomly from which the Table 4-8 was obtained and the graphs from Figure H-1 in Appendix H were obtained The positive $V_{on}$ shift does not depend on the bending radius. When diminishing or increasing the radius the positive $V_{on}$ shift always occurs for consequent measurements. So, although the bending radii of 45, 25 and 15 mm does not affect the TFTs behaviour, it is important to consider the inflicted electrical stress. This effect on the transistors can also be observed on the transistors when doing three consecutive measurements when the transistors did not have any mechanical force applied, represented in Figure H-2 from Appendix H.

Table 4-8:Summary of IGZO TFTs, fabricated on the K75 substrate in bending and flat conditions, with radii 45, 25 and 15 mm

| | $I_{on}/I_{off}$ ($\times 10^{6}$) | $V_{on}$ (V) | $I_G$ (pA) | Hysteresis (V) | $\mu_{sat}$ ($cm^2V^{-1}s^{-1}$) | $V_T$ (V) |
|---|---|---|---|---|---|---|
| Before peel-off | 18.6 ± 10.8 | 0.55 ± 0.06 | 14.7 ± 19.2 | 0.40 ± 0.08 | 6.26 ± 1.82 | 3.14 ± 0.04 |
| After peel-off | 11.0±5.41 | 1.4 ± 1.1 | 64.0±90.8 | 0.425±0.05 | 7.94 ± 3.22 | 5.05±2.34 |
| T25 | 6.2±3.89 | 0.8±0.14 | 617±867 | 0.4±0.0 | 7.17 ± 3.87 | 3.84±0.104 |
| flat2 | 7.13±2.57 | 1.1±0.57 | 896±200 | 0.55±0.07 | 7.81±2.56 | 4.85±1.05 |
| T15 | 16.9±17.6 | 1.6±0.7 | 1730±2420 | 0.5±0.14 | 8.16±2.22 | 5.71±1.27 |
| Flat 3 | 15.1±12.9 | 1.85±0.49 | 1450±1990 | 0.6±0.14 | 8.53±2.79 | 6.43±1.22 |
| C25 | 19.3±17.6 | 2.15±0.21 | 1730±2390 | 0.6±0.1 | 9.34±2.45 | 6.72±1.09 |
| Flat 4 | 47.4±49.5 | 2.25±0.35 | 3190±4430 | 0.75±0.07 | 10.6±0.7 | 7.61±1.04 |
| C45 | 58.4±69.7 | 2.75±0.21 | 3080±4280 | 0.9±0.28 | 11.3±1.79 | 8.45±0.28 |

### 4.3.6 Substrate Peel-off

The peel-off process is very dependent on the user. Although the K75 sample could still yield functioning transistors, some part of the sample cracked, which made the measurements on the pads of some transistors not possible, as seen in Figure I-1, from Appendix I.

Although the K75 delaminated without cracking most of the sample, the same did not happen with the K50 and K25 samples. The peel-off is done with a metal blade, and, even if this type of delamination works well for thicker substrates, the thinner substrates could not withstand this process and cracked, which is represented in Figure I-2, from Appendix I.

From the analysis of the optical microscope images in Figure I-1 and Figure I-2 from Appendix I, it appears the gate rarely cracks, and that cracks only appear on the top Mo layer. So, to understand which layer is the most critical for this process, SEM images and cross sections were done on the K25 sample.

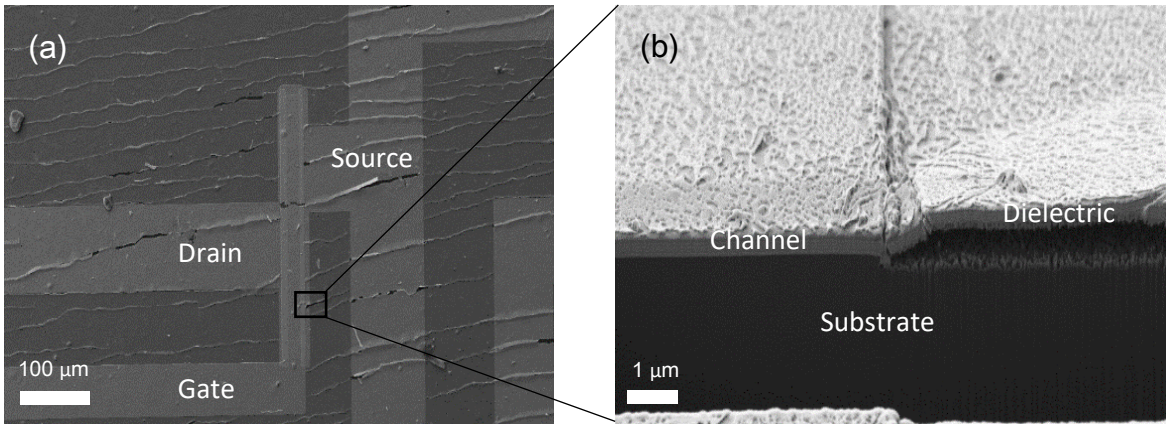


Figure 4-17: SEM images of the K25 delaminated sample: (a) surface with the $SE_2$ detector, (b) cross-section of crack in TFT.

Analysing the SEM images, it is possible to see that the substrate cracks where the dielectric is in contact with the substrate. However, the bottom molybdenum (gate contact) can withstand the process. This means that, although the substrate cracks, these cracks do not propagate through the bottom contact, which results on the multilayer to remain reliable. To test this, measurements were done of the transfer curves of the transistors, with the microprobe on the transistors (and not on the pads), as schemed in Figure I-3, from appendix I.

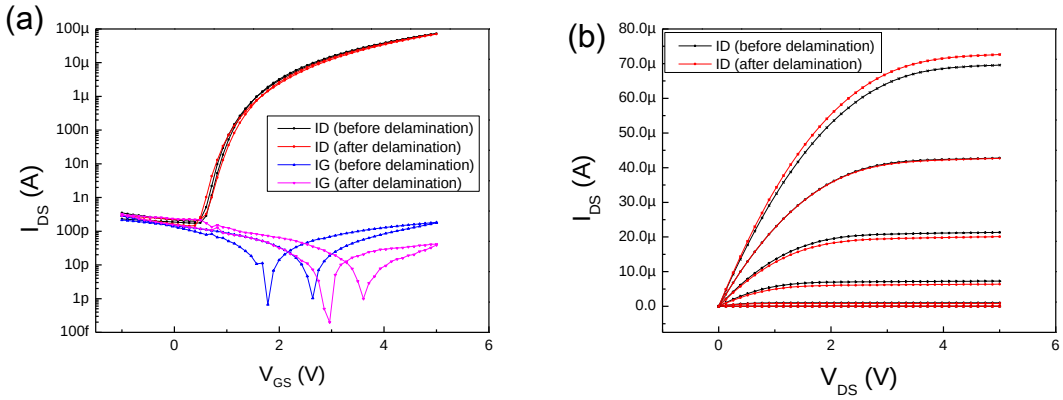


Figure 4-18: Characteristic curves of a TFT in the K25 sample before and after delamination, with probes on TFTs: (a) Transfer curve; (b) Output characteristic curve.

It is then possible to affirm that, although the peel-off process cracks the dielectric multilayer and substrate, it is generally not enough for the transistor (on top of the gate electrode) to stop working. The main consequence of this would be that, although the transistors would still be intact, the circuit would not be able to propagate the signal and no current would be possible to obtain from the drain to the source ($I_{DS}$).

#### 4.3.6.1 Paper Blade Delamination

To achieve better yield of the peel-off process, two simple delamination methods are analysed. The hypotheses are:

- The parylene on top could act as a stress inhibitor and allow for an easier delamination, without cracking the multilayers;
- The blade used is changed to a soft material.

These solutions just present a way to better control the process, Figure 4-19. The delamination is still very dependent on the user.

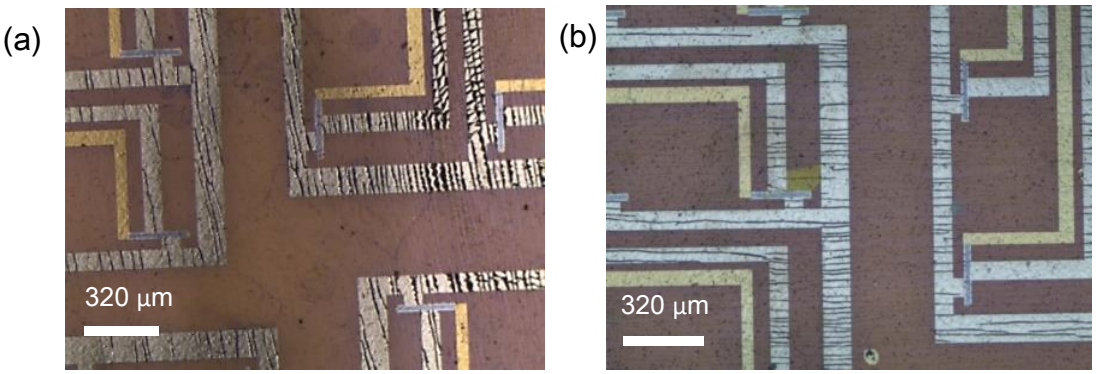


Figure 4-19: Optical microscope images of the K25 sample after delamination: (a) without parylene layer; (b) with 5 µm parylene layer.

It is seen from Figure 4-19 that the 5 µm parylene layer on top does not change the outcome of the delamination. The neutral strain plane does not shift high enough for the neutralization of the stress occurring during the delamination using the metal blade. The metal blade is very efficient at cutting the resin used to glue the substrate to the glass, making the delamination process faster and therefore less controlled. Furthermore, the thickness of the metal blade and the rigidity of this blade can be important factors to crack the devices.

Since the blade is shown as one of the major problems of the delamination, another material is tried as a blade. The paper blade is a soft material, thinner and more flexible. Because of these advantages, it does not cut the glue as easily, making the process slower and doesn't interact as forcibly as the metal with the polymer substrate. The peel-off becomes more controlled and therefore more reliable. Even so, the process is still very dependent on the user and probably does not scale for very thin substrates.

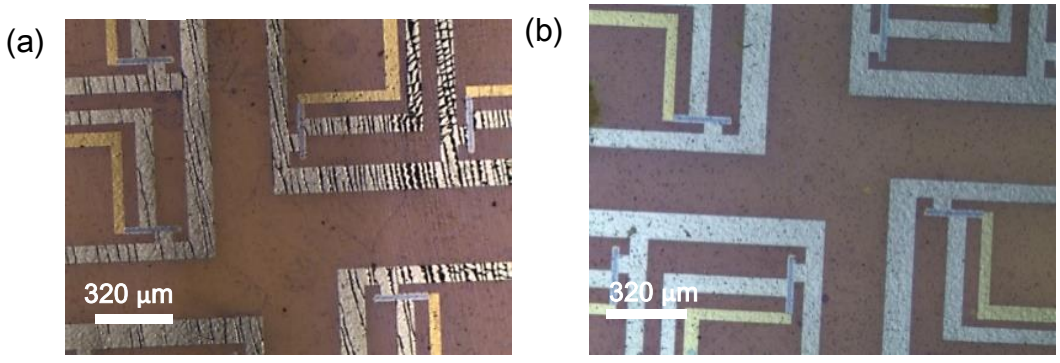


Figure 4-20: Optical microscope images of the K25 sample after delamination: (a) with a metal blade; (b) with a paper blade.

### 4.3.7 Cycles of Bending

Paper-blade delamination was used in K25 substrates which were then subjected to bending cycles test. After achieving free standing substrates with intact IGZOs channels, it is possible to study the critical failure of the multilayers under repeated bending. Since the multilayer is shown as very cohesive and with very good interfaces, the tension bending mode is theoretically more critical than the compression bending mode [40]. A three-point bending test was performed with a one-time bending test. In this test, TFTs were bent at different radii and kept under mechanical strain for 10 s to understand any failure mechanism and the maximum strain and bendability radius possible. The bending radius used were 10, 5, 2.5 and 1.25 mm.

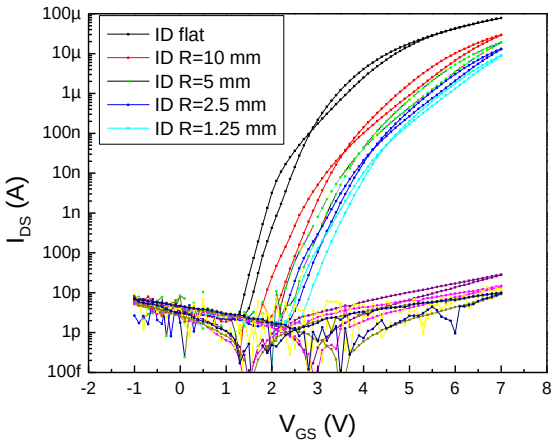


Figure 4-21: Transfer characteristic curve of a TFT on a K25 substrate in a flat position, after bending for 10 s with a radius of 10 mm, 5mm, 2.5 mm and 1.25mm

From the graph of Figure 4-21 it is possible to see that even after bending to a radius of 1.25 mm the curves the TFT still have good performances and that $I_G$ does not increase significantly. From this test it is possible to affirm that this TFT stack has a good performance even for radius smaller than 1.25 mm. However, in some TFTs, $I_{DS}$ decreased significantly, showing that some failure mechanisms occurred. Nevertheless, in no TFT has the $I_G$ raised significantly, demonstrating that the TFT stack is very reliable. From equations 5 and 6 it is possible to affirm that the TFT stack analysed in this study can perform well under a strain of 0.6 %. Since TFTs have several patterned layers, strain within the TFT stack will vary locally. To have more precise numbers, a numerical calculation, including the TFT geometry, is necessary.[71]

A three-point bending test was then performed, with a radius of approximately 1.25 mm, on K25 and K75 samples. As expected, the thicker substrate K75 failed much quicker than the K25 sample and could not withstand as many cycles as the thinner substrate. At 500 cycles, the top molybdenum layer was completely cracked, with presence of interlinked mudcracks, Figure 4-22.

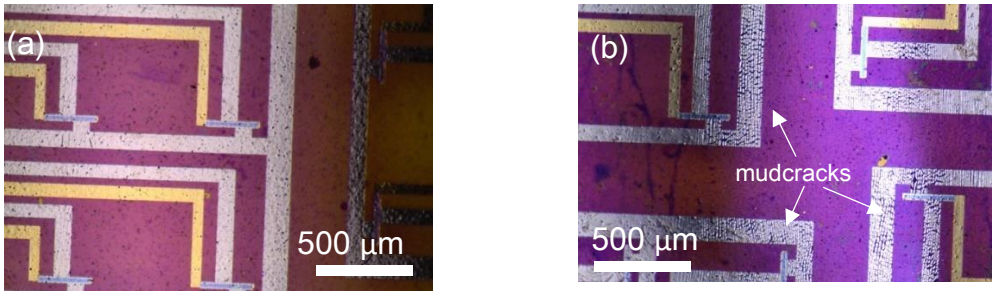


Figure 4-22: Optical microscope image of: (a) K25 sample with 500 cycles of 1.25 mm radius tensile bending, and (b) K75 sample with 500 cycles of 1.25 mm radius tensile bending.

The K25 sample was bended in growing steps, from 0 to 2000 cycles, and optical microscope images were taken to understand the propagation of the cracks, seen in Figure 4-23.

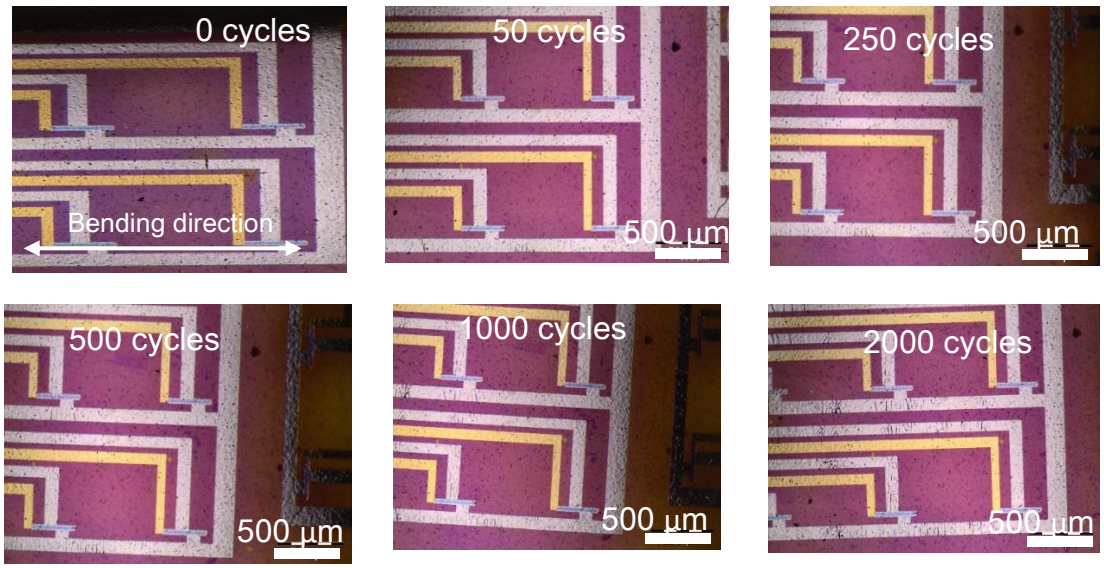


Figure 4-23: Optical microscope images of K25 sample under tensile bending with 1.25 mm from 0 to 2000 cycles.

In Figure 4-23, it is possible to see the cracks propagating through the top Mo layer. Since these cycles were done in tension, cracks appear in parallel to the bending direction. However, the cracks only appear to negatively influence the transistors at around 1000 cycles. To understand if the behaviour of cracking follows the same behaviour during peel-off, SEM images of K25 sample after 2000 bending cycles were obtained, presented in Figure 4-24.

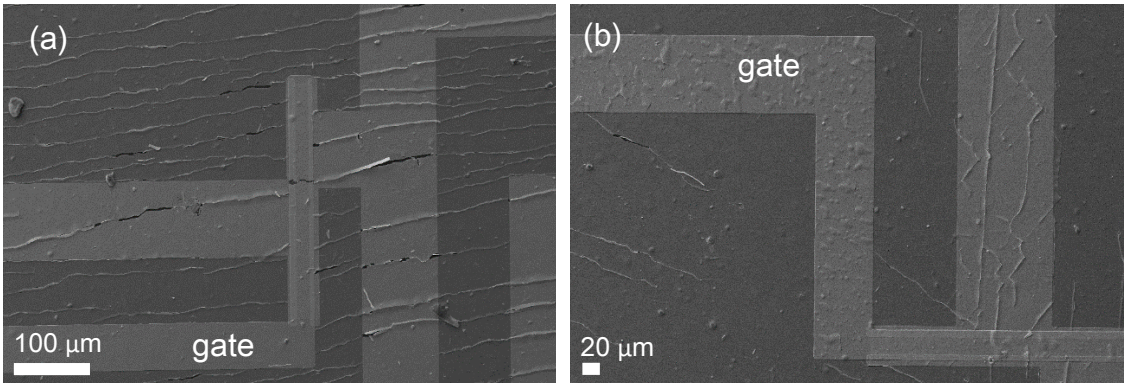


Figure 4-24: SEM images of two different K25 patterned sample: (a) after delamination with metal blade; (b) after delamination with paper blade and 2000 cycles of 1.25 mm radius of curvature.

The cracks kept appearing where the substrate is in direct contact with the dielectric. The dielectric is multi-layered, having sputtered $SiO_2$ as the first layer, which is in contact with the substrate. The cracking phenomenon is probably due to the mismatch in the coefficients of thermal expansion. In Table 4-1, the CTE of the different layers is shown. It is observed that the difference between the Kapton substrate, $\alpha(\text{Kapton}) = 20 \times 10^{-6}/\,°C$, and $SiO_2$, $\alpha(SiO_2) = 0.7 \times 10^{-6}/\,°C$, is much higher than the different between Kapton and molybdenum, $\alpha(\text{Mo}) = 4.7 \times 10^{-6}/\,°C$.

According to Equation 8, the difference between the CTE of the layers gives the strain of the layer,

$$\varepsilon_{f,mismatch} = (\alpha_{Tf} - \alpha_{Ts})\Delta T \quad (8)$$

where, $\varepsilon_{f,\,mismatch}$ is the strain in the film, that results from the difference between CTE of the film $\alpha_{Tf}$ and the substrate $\alpha_{Ts}$. It also depends on the difference in temperature $\Delta T = 180\text{-}25 = 155$ °C, giving the strain for $SiO_2$ ( $\varepsilon_{SiO_2}$=0.00253) and for Mo ($\varepsilon_{Mo}$ = 0.0019). Considering that the stress is given by,

$$\sigma = \varepsilon \times \frac{Y}{1-\upsilon} \quad (9)$$

Where ν is the *poisson ratio*. Considering that for $SiO_2$, Y($SiO_2$) = 70 GPa and ν = 0.25 [58], and for Mo, Y(Mo) = 152 GPa and ν=0.29 [72], the stress associated with the mismatch in CTE is σ($SiO_2$) = 235 MPa and σ(Mo) = 429 MPa. The stress from the mismatch is higher in the Molybdenum than in the $SiO_2$ layer. However, the fracture strength of the $SiO_2$ is 364 MPa [73], which is higher than the calculated stress. Nevertheless, since when bending the stress also increases, this stress together with the stress from the mismatch in CTE results in cracks in this layer. In the case of the molybdenum, the Mo layer is a tough layer with a very high modulus of rupture which makes it a more reliable material. Also, when in bending a continuous film will crack sooner than a layer with a smaller width. In this case, the dielectric is a more continuous film, while the molybdenum has a smaller width. The dimensions of the dielectric layer, together with the stress gathered in this thin film, originate cracks much earlier in the dielectric than on the molybdenum, making the dielectric the critical layer, more specifically the interface between the substrate and the dielectric.

Furthermore, the surface of the molybdenum gate changes after bending, with the appearance of protuberances, Figure 4-24.

#### 4.3.7.1.1 Performance of TFT after bending cycles

The characterisation of TFTs on the substrate K25 was studied after bending cycles with a radius of 5 mm. The 5 mm radius was chosen because it was the only bending radius available that could influence all the TFTs of the matrix at the same time. As done before, the relation between the bending direction and the position of the channel was analysed. The measurements obtained can be observed in Figure 4-25.

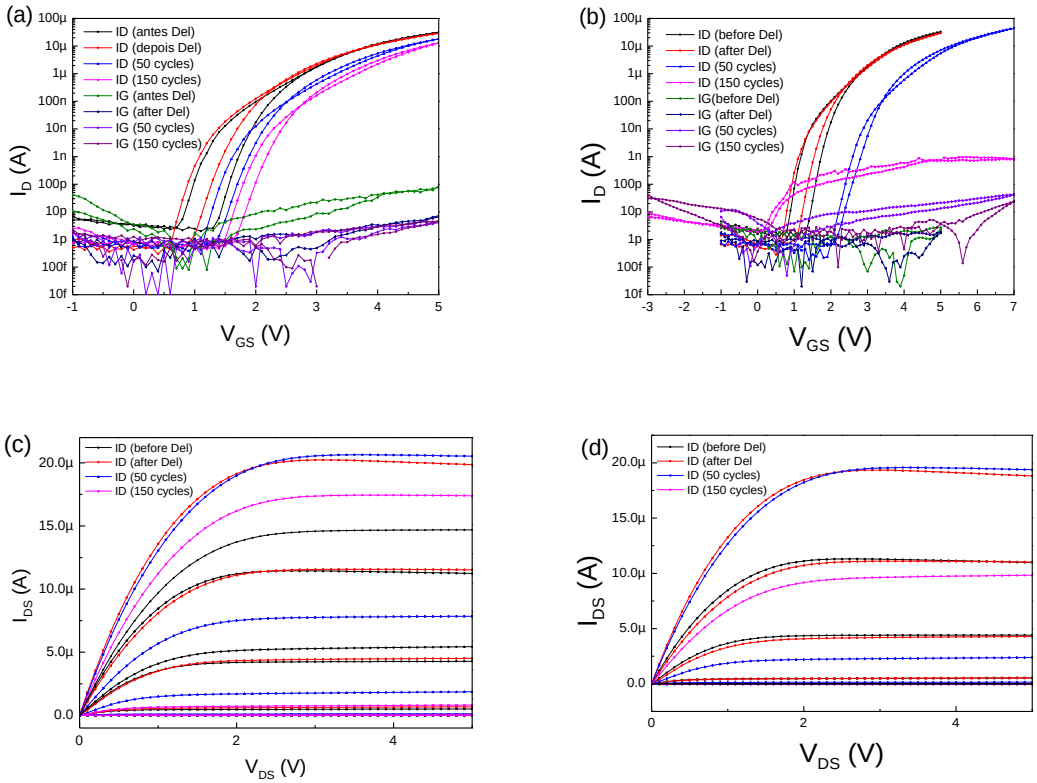


Figure 4-25:Characteristic curves of a TFT in the K25 sample before (black) , after delamination (red) with 50 cycles of tensile bending with r= 5mm (blue) and 150 cycles of tensile bending (pink) (a) Transfer curve of TFT with channel parallel to bending direction; (b) Transfer curve of TFT with channel perpendicular to bending direction; (c) Output characteristic curve of TFT with channel parallel to bending direction¸ (d) Output characteristic curve of TFT with channel perpendicular to bending direction

The K25 sample analysed was peeled-off using the paper blade. After peel-off the TFTs maintained the very good performance observed while glued to the carrier glass. Regarding the bending cycles, when the channel was parallel to the bending direction the performance of the TFTs was maintained until 150 cycles. However, this was not the case for TFTs with channel perpendicular to bending direction. In this case when the 150 cycles were performed, the $I_{on}/I_{off}$ ratio and the mobility decreased significantly. Nonetheless, the $I_G$ maintained a reasonable low value. If the failure was due to the cracking of the dielectric on the channel, the $I_G$ value would increase significantly. However, as it is possible to see in the graph a smaller $I_{DS}$ is obtained which could mean that some part of the signal is not propagating to the drain and source, nevertheless, no cracks appear in the optical microscope images after the 150 cycles bending. This could mean that some microcracks are appearing in the source and drain.

Table 4-9: Summary of IGZO TFTs with channel parallel to bending direction, fabricated on the K25 substrate, in the carrier, after delamination and with 50 and 150 cycles of bending with a radius of 5 mm.

| K25 | $I_{on}/I_{off}$ ($10^6$) | $V_{on}$ (V) | $I_G$ (pA) | Hysteresis (V) | $\mu_{sat}$ ($cm^2V^{-1}s^{-1}$) | $V_T$ (V) |
|---|---|---|---|---|---|---|
| On carrier | 9.59 ± 4.38 | 0.88 ± 0.31 | 17.2 ± 32.9 | 0.48 ± 0.16 | 5.24 ± 0.81 | 3.59 ± 0.15 |
| delaminated | 10.00±1.21 | 0.53±0.05 | 5.54 ±2.96 | 0.4 ± 0.1 | 5.25 ± 1.32 | 3.49 ± 0.01 |
| 50 cycles | 28.6 ± 15.6 | 1.03 ± 1.02 | 3.91 ± 1.58 | 0.33±0.05 | 7.04±2.39 | 4.51 ± 1.03 |
| 150 cycles | 17.5 ± 1.23 | 0.98 ± 1.56 | 6.72 ± 4.94 | 0.30±0.18 | 5.27 ± 0.92 | 4.55 ± 0.97 |

Table 4-10: Summary of IGZO TFTs with channel perpendicular to bending direction, fabricated on the K25 substrate, in the carrier, after delamination and with 50 and 150 cycles of bending with a radius of 5 mm.

| K25 | $I_{on}/I_{off}$ ($10^6$) | $V_{on}$ (V) | $I_G$ (pA) | Hysteresis (V) | $\mu_{sat}$ ($cm^2V^{-1}s^{-1}$) | $V_T$ (V) |
|---|---|---|---|---|---|---|
| On carrier | 19.2 ± 17.4 | 0.96 ± 0.15 | 7.42 ± 9.94 | 0.4 ± 0.1 | 6.38 ± 0.58 | 3.46 ± 0.04 |
| delaminated | 63.5 ± 51.4 | 0.64 ± 0.21 | 10.5 ± 37.5 | 0.46 ± 0.05 | 5.73 ± 1.22 | 3.57 ± 0.15 |
| 50 cycles | 74.2 ±66.7 | 1.44 ±0.48 | 16.8 ± 13.9 | 0.28 ± 0.15 | 6.36 ± 0.82 | 4.59 ± 0.37 |
| 150 cycles | 0.0 ± 0.0 | 0.5 ± 0.57 | 14.5 ± 13.0 | 0.3 ± 0.14 | 0.00±0.00 | 1.97±1.96 |

#### 4.3.7.2 Neutral strain plane

Since the interface between the dielectric multilayer and the substrate is shown as the critical part in this system, it would be ideal for the neutral strain plane to be positioned either in the dielectric layer, or on the surface of the substrate. According to the Equation 5, it is possible to determine the position of the plane using the Young modulus and thickness of the different layers of the system, shown in Table 4-11.

Table 4-11:Thickness and Young modulus of each layer of the TFT.

| Material | Thickness (nm) | Young Modulus (GPa) | Material | Thickness (μm) | Young Modulus (GPa) |
|---|---|---|---|---|---|
| IGZO | 20 | 111.3 | Kapton HN | 25 | 2.3 |
| Mo | 60 | 152 | Parylene | variable | 2.5 |
| TaSiO | 140 | 133 | | | |

From the values of the previous table, the position of the neutral strain plane was calculated for a parylene layer of 1 μm, 5 μm, 10 μm, 20 μm and 25 μm. From which the values of the position of the NSP were obtained and represented in Table 4-12.

Table 4-12: Position of the NSP according to parylene thickness, for K25 substrate.

| Parylene Thickness (μm) | NSP (μm) | Location on stack |
|---|---|---|
| 1 | 17.5 | In the substrate |
| 5 | 18.5 | In the substrate |
| 10 | 20 | In the substrate |
| 20 | 23.7 | In the substrate (close to the surface) |
| 25 | 25.7 | In the encapsulation layer |

As it is expected, the closer the thickness of the parylene is to the thickness of the substrate, the higher the placement of the NSP. Taking this calculation into account, the TFTs were deposited with a parylene monomer weight of 40 g, from which it was obtained a 22.1 μm layer of parylene, achieving a calculated engineering strain of 0.08 % on the surface of substrate with a bending radius of 1.25 mm. However, since it was not used an adhesion promotion the layer peeled off before bending cycles were performed.

However, even without the passivation layer, the TFTs still show a good electrical performance even with a bending radius of 1.25 mm. This means the TFT stack has a very good mechanical reliability and it can be used in future flexible electronics.

# 5 Conclusions and Future Perspectives

The present work was focused on the production and characterisation of TFTs with the best bendability possible using production techniques already used in the industry. Nowadays, the study of TFTs behaviour under mechanical bending is of major importance, and techniques to produce roll-to-roll manufacturable and extreme bendable devices are very important.

The IGZO and Mo layer where characterised mechanically using nanoindentation from which the values for Young modulus and hardness were obtained, Y(Mo)=159.8 GPa and H(Mo)=13.3 GPa, and Y(IGZO)=111.3 GPa and H(IGZO) = 8.3 GPa. For the Mo, the difference in values of the young modulus in literature, Y(Mo) = 329 GPa, and obtained in this study is due to the thickness of the layer studied. The parylene layer is a semycristalline layer that changes the surface conformability after annealing, however, because of the viscoelastic nature of the material an accurate measurement of Young modulus and Hardness were not possible to achieve.

To achieve small bending radius, it is necessary low substrate thickness, so the choice of changing the substrate from PEN (125 μm) to Kapton with 75, 50 and 25 μm was made. The TFTs produced on the Kapton substrate achieved good electrical performances with very similar values to TFTs produced on Corning glass, despite the Kapton substrate surface roughness of 100 nm, much higher than 1.49 nm of the glass [74].

However, the idle shelf life time of the TFTs on the Kapton substrate is much lower than on the glass, with a lower $I_{on}/I_{off}$ and an increase in IG, this is due to the permeability of the Kapton substrate. Furthermore, when in bending, the TFTs do not show any difference in behaviour due to the mechanical stress until 15 mm of bending radius. The occurring Von shift was provoked by the bias stress originated from the continuous use of the TFTs.

For a better reliability of the peel-off process the concept of “paper blade” was used to improve the yield of the delamination process and it is proven that the TFTs do not shift considerably after this method.

To understand the critical strain for the devices, TFTs on 25 μm thick substrates were bended for 10 s with a radius from 10 mm to 1.25 mm with a representative strain from 0.08% to 0.62 %, respectively. Only a slight increase in IG occurs and the measured TFTs retain a good electrical performance. With no increase in $I_G$ it is possible to affirm that the TFT stacks are very reliable until 1.25 mm radius.

Tensile bending measurements with a radius of 1.25 mm revealed that the 75 μm thick substrate achieves critical failure in <500 cycles, while the thinner substrate (25 μm) could withstand almost 1000 cycles before the cracking of the dielectric. The most common failure mechanism observed under tensile bending was the appearance of cracks in the oxide dielectric when in direct contact with the polyimide substrate. These cracks do not appear in regions where molybdenum gates were in contact with the substrate, hence the mismatch between the coefficient of thermal expansion of the substrate and the dielectric thin film were identified as the reason for failure.

When tensile bending cycles were done with a radius of 5 mm, to ensure all the TFTs were under the same bending radius, the performance of the TFTs is shown to be dependent on the channel length direction, regarding the bending direction, with the channel perpendicular to bending direction roughly maintaining the electrical performance for more than 150 cycles. However, when the channel was parallel to bending direction. the IG does not significantly increase which means that in this condition possible microcracks appeared, which deteriorated the source and drain paths.

In conclusion, even with intrinsically rigid materials as oxides and metals, it is possible to obtain reliable flexible TFTs. The main failure mode of this TFTs is a major problem in a circuit and not on the device, because although the TFTs would still work correctly the drain and source paths would crack not obtaining the voltage necessary to modulate the channel.

Regarding further perspectives, an adhesion promotion should be used to achieve better adhesion between the Kapton substrate and the parylene in order to achieve a NSP in the surface of the substrate.

Further studies should be made to measure the mechanical properties of $SiO_2$, TaSiO and parylene. In the latter, it should be taken into consideration the viscoelastic properties of this material. Furthermore, bending cycles of the TFT under compression would be interesting to study to understand the effect of the repetition of mechanical compressive bending in this multilayer system.

Also, stress tests should be performed to better understand the stability of the devices, before and after passivation with parylene and a passivation layer on the substrate should be implemented. This passivation layer would have two main focuses, to guarantee a better roughness of the surface of the substrate and should have a CTE higher than $SiO_2$ so that the circuit is more reliable.

Also, measurements of the TFTs while bending under smaller radii would be interesting to understand the mechanical strain dependance of mobility

In this work it is concluded that the TFT stack used is not the major influence when bending. So, it would be interesting to fabricate this TFTs in a substrate thinner than 10 μm to achieve folding.

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# Appendix A

The Fabrication and Processes needed to obtain the devices in free-standing substrates can be divided in 3 main steps:

1. Put substrate on carrier
2. Fabrication of TFTs
3. Peel-off

These 3 steps are schemetised on the following figures.

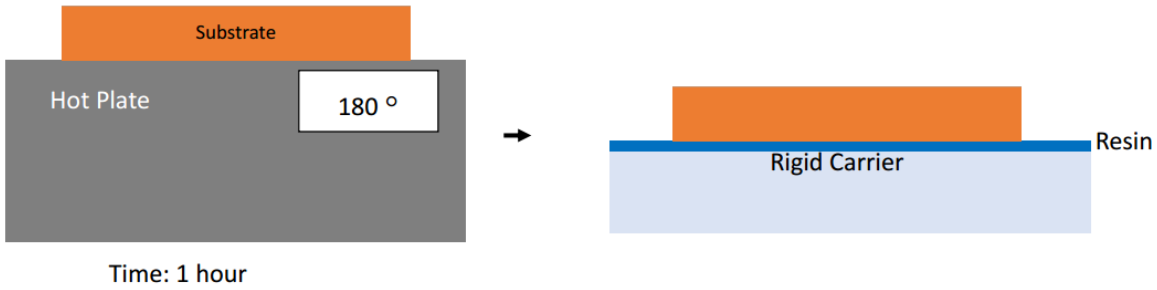


Figure A-0-1:Glueing substrate on a rigid carrier (glass) with a resin

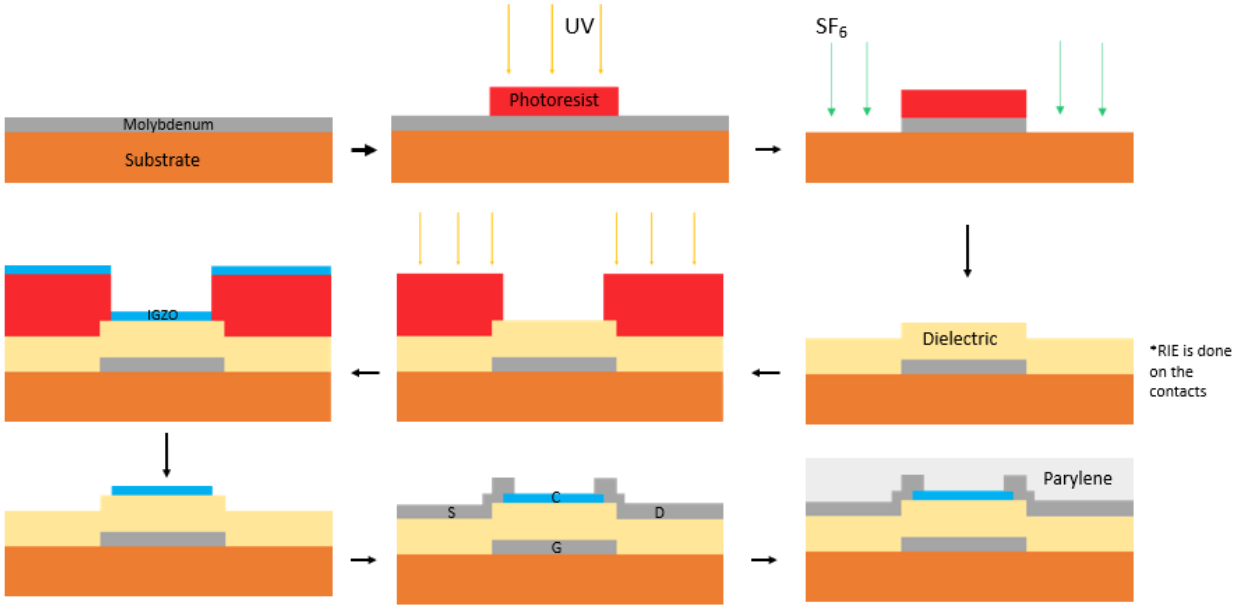


Figure A-0-2: Schematic of the fabrication of the IGZO-TFTs used in this work

# Appendix B

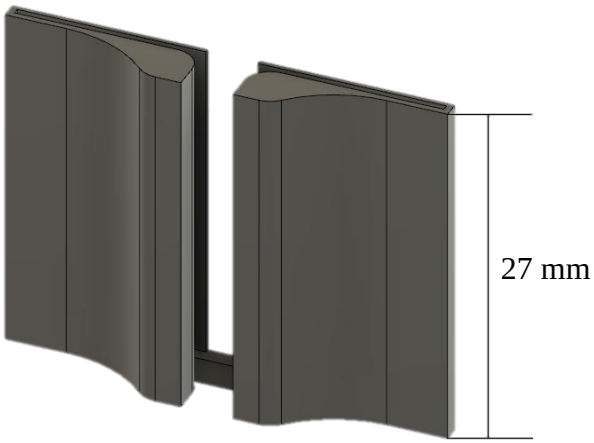


Figure B-1: Design of part to adapt to bending machine to achieve bending radius of r=1.25 mm

(a) (b)

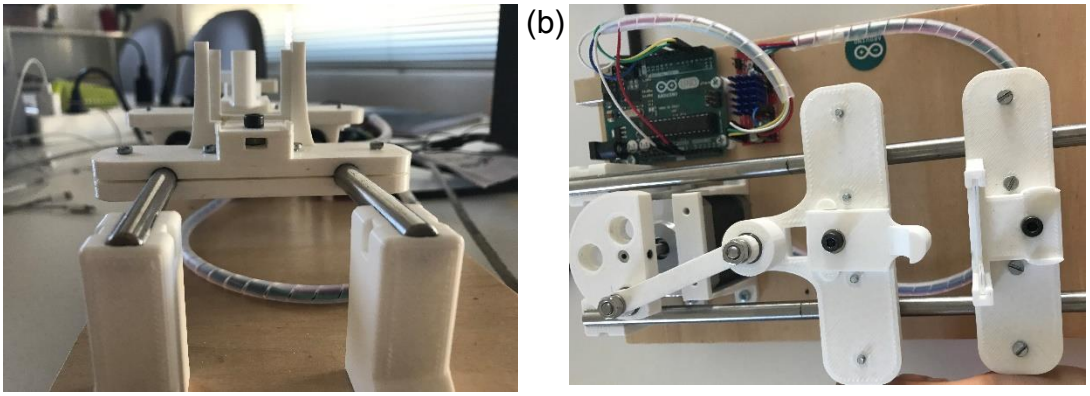

Figure B-2: 3 point bending system (a) picture from the front of the system (a) picture from top of the system

# Appendix C

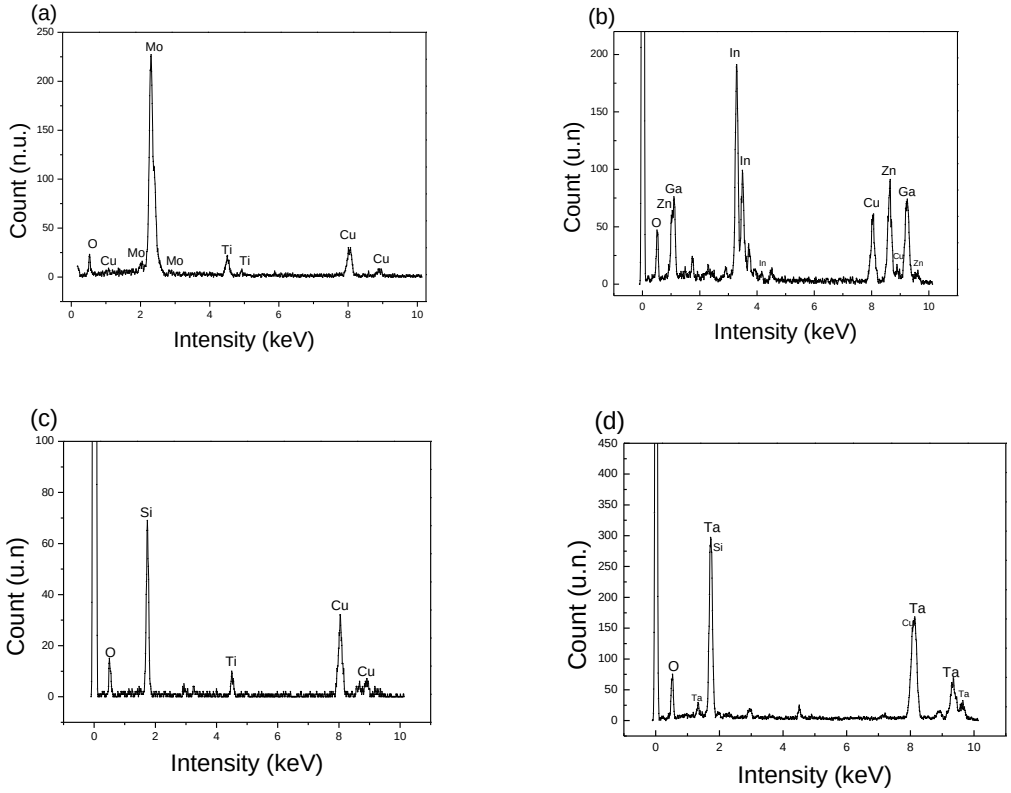


Figure C-1: TEM EDS of the individual layers on the multilayer system of the TFTs studied; (a) Mo; (b) IGZO; (c) $SiO_2$ (part of multilayer); (d) TaSiO (part of multilayer).

# Appendix D

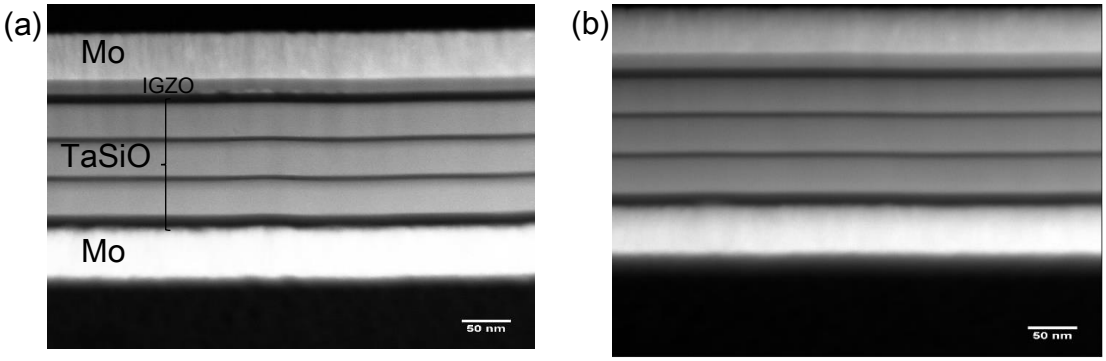


Figure D-1: TEM image of the multilayer system with a parylene passivation layer, (a) without annealing; (b) with annealing at 180ºC for 1 hour

In Figure D-1, the parylene is on top of the TFT stack,. However, since the study of the temperature influence is on the TFT stack, the parylene was cut when doing the TEM images.

# Appendix E

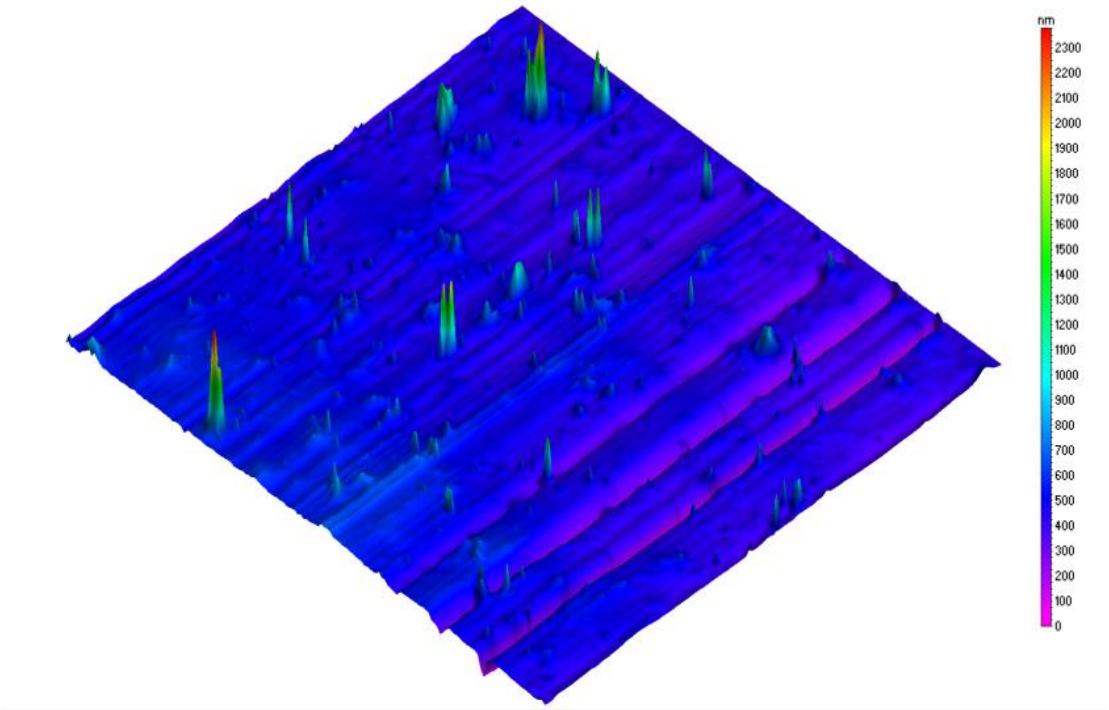


Figure E-1:3D surface measurements of the Kapton substrate with 75 µm.

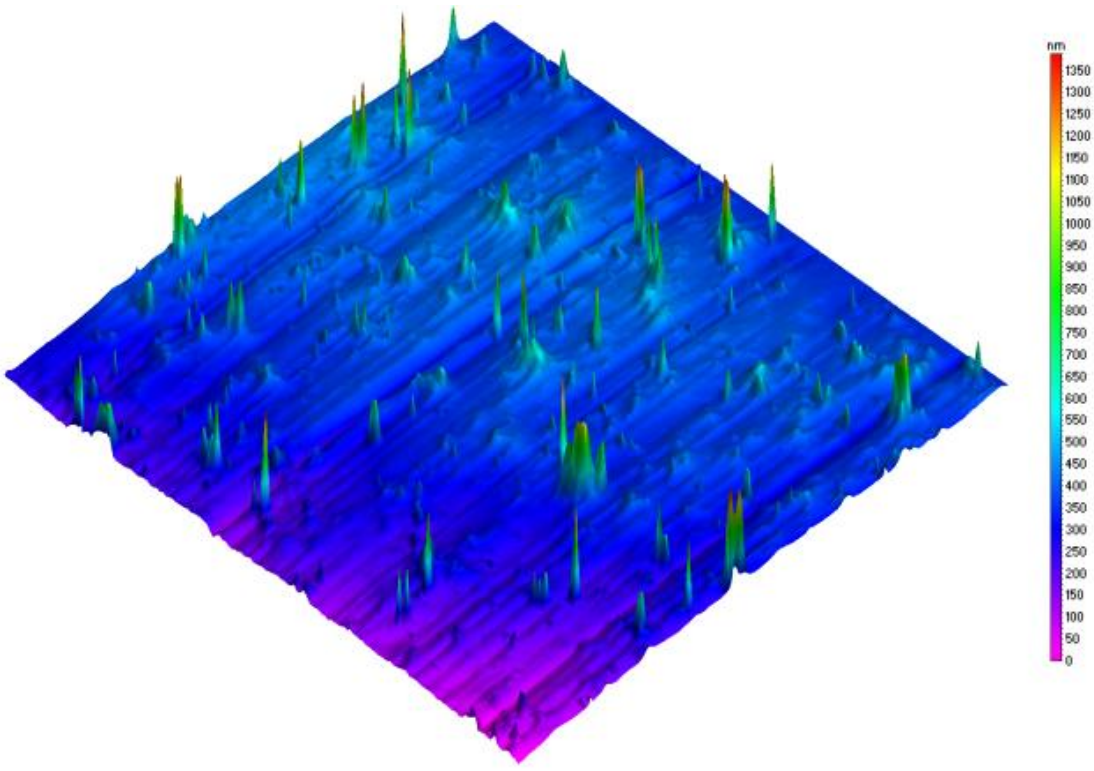


Figure E-2:3D surface measurements of the Kapton substrate (a) with 50 µm.

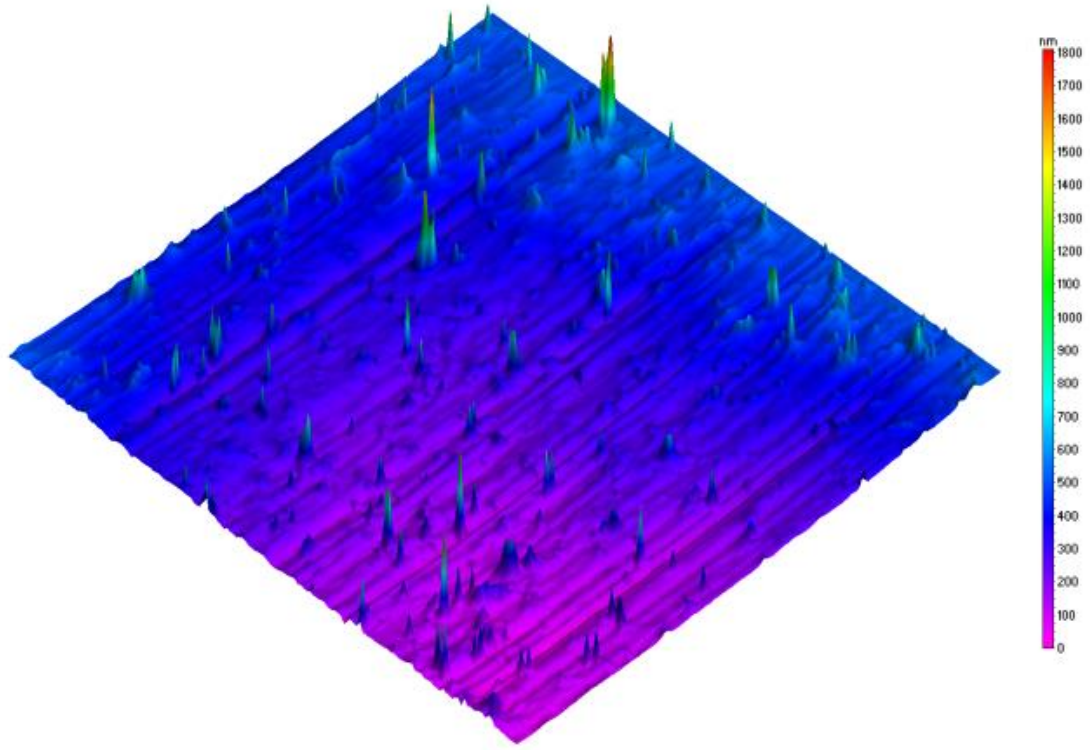


Figure E-3:3D surface measurements of the Kapton substrate with 25 μm.

# Appendix F

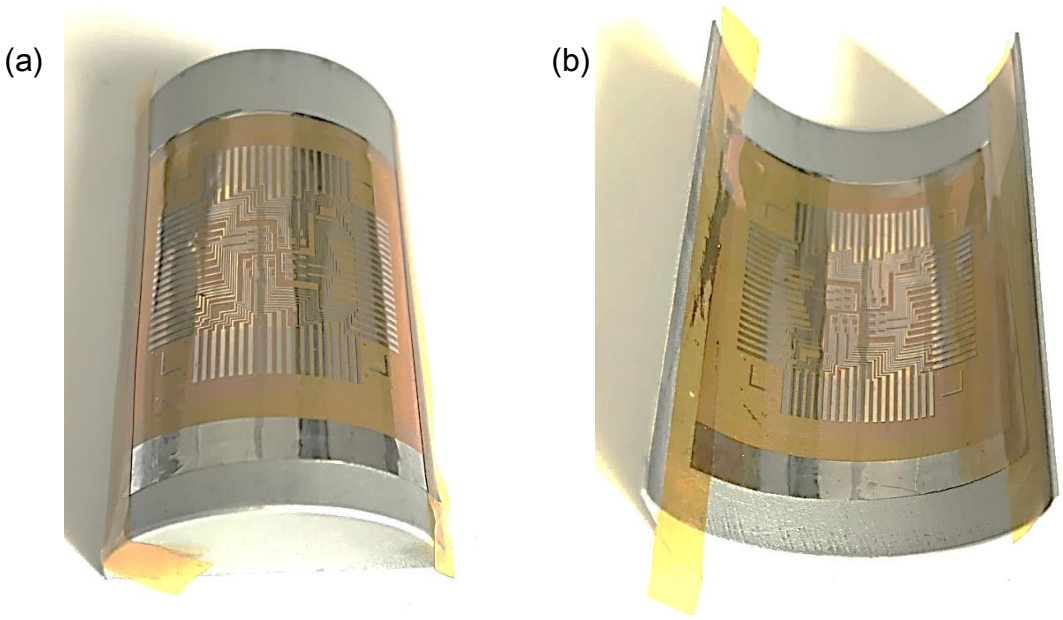


Figure F-1: Fabricated TFTs during bending (a) Tension; (b) Compression with a bending 25 mm bending radius

# Appendix G

Table G-1: Summary of IGZO TFTs with channel perpendicular to bending direction, fabricated on the K75 substrate in bending and flat conditions, with radii 45, 25 and 15 cm.

| | $I_{on}/I_{off}$ ($\times 10^{6}$) | $V_{on}$ (V) | $I_G$ (pA) | Hysteresis (V) | $\mu_{sat}$ ($cm^2V^{-1}s^{-1}$) | $V_T$ (V) |
|---|---|---|---|---|---|---|
| Flat 1 | 5.8 ± 1.7 | 0.93 ± 0 | 20.5 ± 15.0 | 0.21 ± 0.00 | 5.12 ± 0.04 | 3.64 ± 0.04 |
| T45 | 5.5 ± 0.3 | 0.98 ± 0.16 | 6.6 ± 0.8 | 0.22 ± 0.11 | 5.17 ± 0.29 | 3.58 ± 0.21 |
| C45 | 7.4 ± 2.9 | 1.14 ± 0.11 | 33.2 ± 28.9 | 0.22 ± 0.01 | 5.12 ± 0.04 | 3.8 ± 0.02 |
| flat2 | 6.1 ± 1.5 | 1.30 ± 0.05 | 38.9 ± 31.7 | 0.11 ± 0.02 | 5.13 ± 0.05 | 3.85 ± 0.01 |
| T25 | 6.2 ± 1.5 | 1.41 ± 0.05 | 49.5 ± 34.7 | 0.11 ± 0.01 | 5.06 ± 0.07 | 3.89 ± 0.02 |
| C25 | 5.3 ± 0.8 | 1.57 ± 0.11 | 34.6 ± 27.4 | 0.11 ± 0.03 | 4.88 ± 0.14 | 3.97 ± 0.02 |
| Flat 3 | 4.5 ± 2.4 | 1.79 ± 0.15 | 63.8 ± 70 | 0.22 ± 0.01 | 4.26 ± 0.71 | 4.06 ± 0.13 |
| Flat 3.1 | 8.2 ± 4.4 | 1.14 ± 0.15 | 13.0 ± 20.0 | 0.215 ± 0.00 | 4.90 ± 0.13 | 3.81 ± 0.07 |
| T15 | 3.0 ± 1.9 | 1.78 ± 0.54 | 14.2 ± 7.7 | 0.16 ± 0.05 | 4.03 ± 1.02 | 4.13 ± 0.20 |

Table G-2: Summary of IGZO TFTs with channel parallel to bending direction, fabricated on the K75 substrate in bending and flat conditions, with radii 45, 25 and 15 cm.

| | $I_{on}/I_{off}$ ($\times 10^{6}$) | $V_{on}$ (V) | $I_G$ (pA) | Hysteresis (V) | $\mu_{sat}$ ($cm^2V^{-1}s^{-1}$) | $V_T$ (V) |
|---|---|---|---|---|---|---|
| Flat 1 | 6.1 ± 0.9 | 0.88 ± 0.08 | 7.4 ± 1.9 | 2.68 ± 0.08 | 5.71 ± 0.14 | 3.57 ± 0.07 |
| T45 | 6.6 ± 2.5 | 1.14 ± 0.01 | 7.1 ± 1.4 | 0.16 ± 0.08 | 5.75 ± 0.42 | 3.73 ± 0.05 |
| C45 | 7.4 ±0.0 | 1.14 ±0.03 | 6.1±0.6 | 0.11±0.01 | 5.92±0.09 | 3.75±0.01 |
| flat2 | 5.4 ± 1.4 | 1.30 ± 0.23 | 5.6 ± 1.8 | 0.22 ± 0.01 | 5.51 ± 0.38 | 3.86 ± 0.09 |
| T25 | 4.3 ± 3.6 | 1.73 ± 0.53 | 6.3 ± 0.0 | 0.12 ± 0.02 | 4.88 ± 1.56 | |
| C25 | 2.4±0.9 | 1.89±0.06 | 7.4±0.0 | 0.21±0.01 | 4.1±0.0 | 4.18±0.01 |
| Flat 3 | 3.9 ± 2.6 | 1.73 ± 0.53 | 5.7 ± 2.0 | 0.21 ± 0.03 | 4.86 ± 1.14 | 4.07 ± 0.24 |
| Flat 3.1 | 6.6 ± 2.9 | 1.14 ± 0.30 | 5.4± 1.6 | 0.21 ± 0.01 | 5.42 ± 0.51 | 3.78 ± 0.19 |
| T15 | 4.5 ± 5.3 | 1.73 ± 0.83 | 6.6 ± 0.3 | 0.12 ± 0.01 | 4.4 ± 2.20 | 4.05 ± 0.41 |

In Table G-1 and Table G-2 the meaning of bending conditions is as it follows:

- Flat: the measurement was done while the TFT was flat
- T: the measurement was done while the TFT was in tension
- C: the measurement was done while the TFT was in compression

The numbers in front of T and C are the bending radius in mm used in the measurement, 45 is r=45 mm, 25 is r=25 mm and 15 is r=15 mm.

The numbers in front of the Flat tell if the flat was the first, second or third flat to be measures. The flat 3.1 shows that another flat was done after the third flat without bending measurements in between. In this case after a week,

# Appendix H

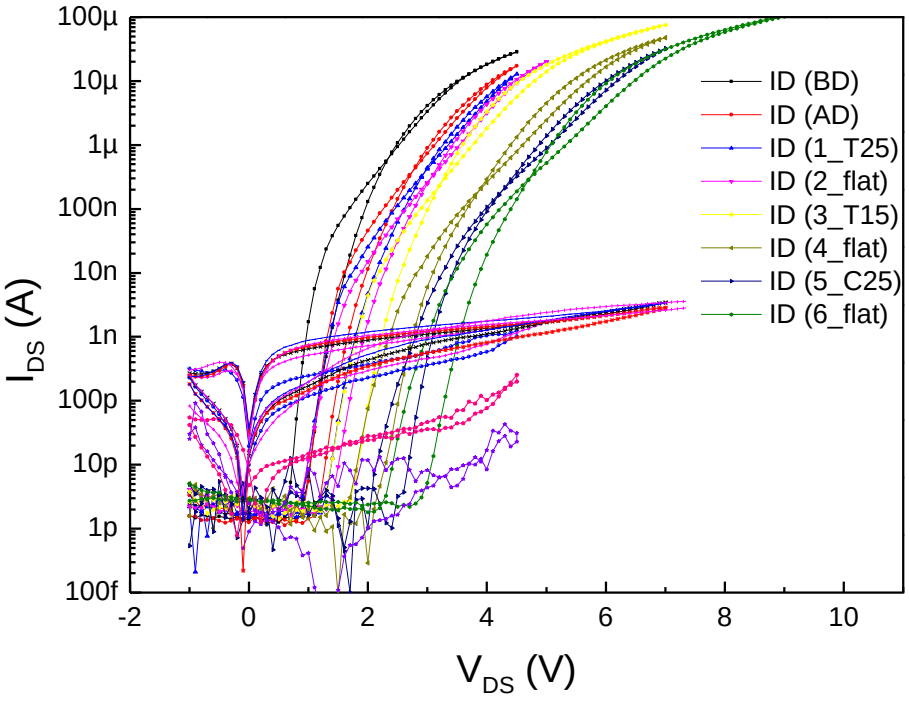


Figure H-1: Characteristic Curves of TFTs under bending with radii 25 mm and 15 mm and in tension and compression, in a random ordering of the conditions

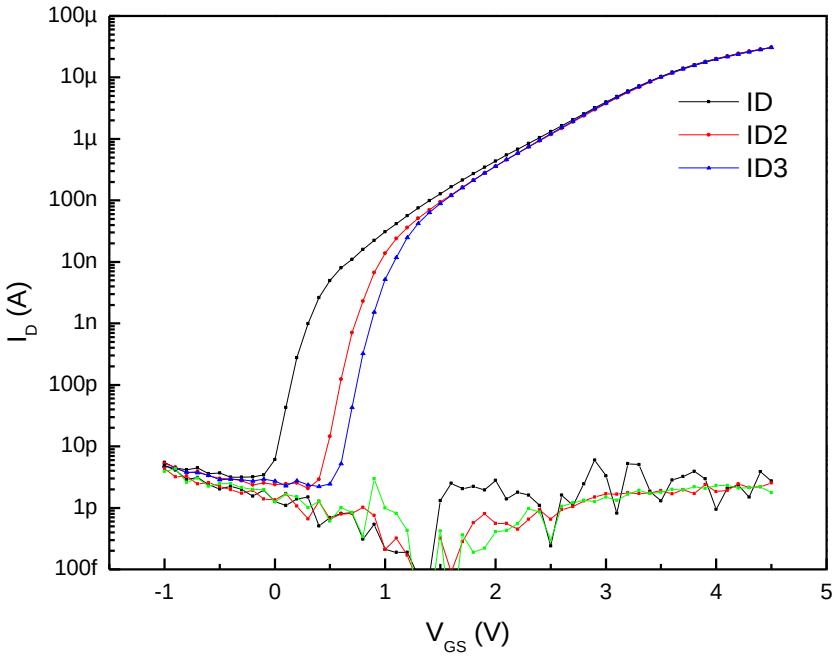


Figure H-2: Transfer characteristic curves of TFTs done consecutively in flat condition

# Appendix I

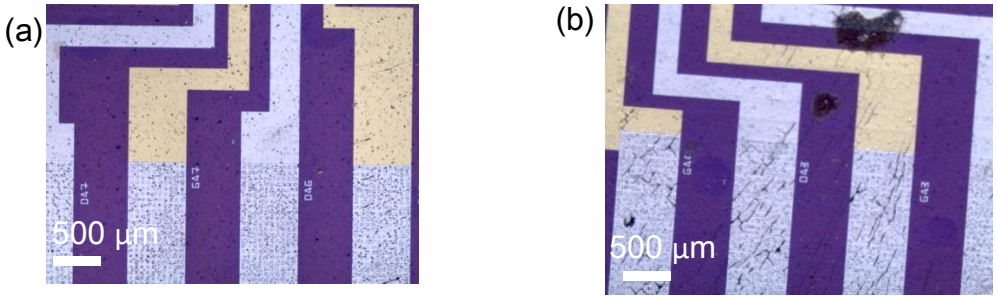


Figure I-1: Optical microscope images of the K75 sample after delamination (a) pads; (b) pads with cracks.

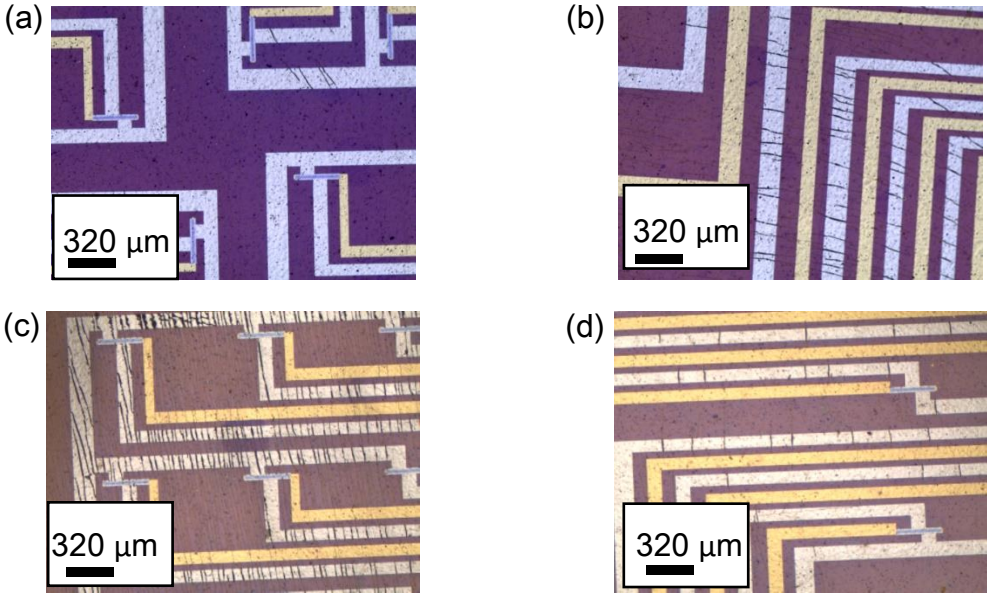


Figure I-2: Optical microscope images of K50 and K25 samples after delamination; (a) K50 sample transistors; (b) K50 vias; (c) K25 sample transistors; (d) K25 sample vias

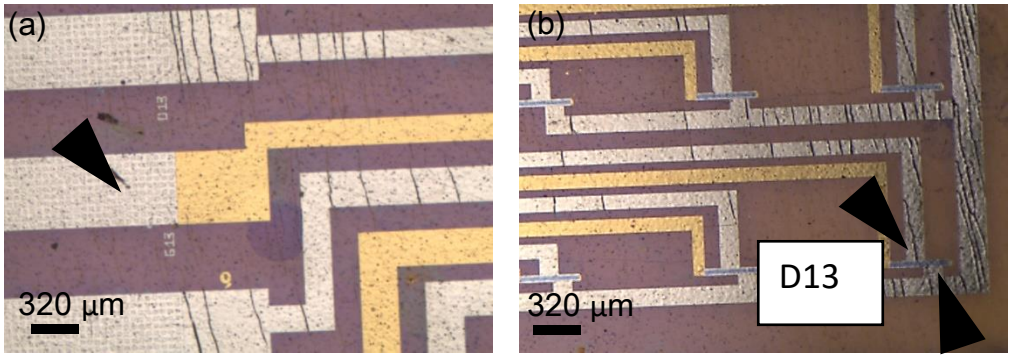


Figure I-3: Optical microscope images of the K25 sample with the representation of the location of probes when measuring TFT characteristic curves; (a) in pads, for gate probe; (b) Transistor, for drain and source pads.