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Fabrication and optimization of hybrid field-effect transistors on fibres

Dissertação para obtenção do Grau de Mestre em
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"When something is important enough,
you do it even if the odds aren't in your favor."

— Elon Musk

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Abstract

Flexible fibre-based devices promise to have a significant impact on future wearable technology. This work, integrated in the 1D-NEON EU project, documents the fabrication and optimization of field-effect transistors (FETs) on conductive wires for further implementation on fibres, promoting the development of smart textiles.

Fibre-transistors were fabricated following a gate-all-around structure, using Ag wire with diameter of 200 and 500 μm as core (gate electrode), parylene deposited by chemical vapor deposition as insulator, sputtered oxide semiconductor (indium-gallium-zinc-oxide or zinc-tin-oxide) and shadow mask evaporated Al or screen-printed Ag as source-drain electrodes. A detailed analysis of the parylene thickness required for proper operation of metal-insulator-metal (MIM) structures and transistors was performed in planar and fibre configurations. While good insulating properties were verified for 500 nm thick films on planar structures, wires required ≈ 1 μm thick films due to the initial wire's roughness. Three different generations of structures were developed, optimizing not only the material stack and deposition processes but also the measurement setups, which were found to be critical to access reliably the electrical properties of fibre-based structures.

Despite their large operating voltage, attributed to the thick insulator layer, fibre-transistors prepared below 150 °C exhibit mobilities over 10^{-2} $cm^2/V.s$, $I_{on}/I_{off} > 10^2$ and no performance degradation after bending with a radius of 45 mm.

Keywords: field-effect transistor, smart textiles, fibre-transistor, chemical vapour deposition, screen-printing

Resumo

Os dispositivos flexíveis à base de fibras prometem ter um impacto significativo na futura tecnologia *wearable*. Este trabalho, integrado no projeto 1D-NEON EU, documenta a fabricação e otimização de transístores de efeito de campo (FETs) em fios condutores para posterior implementação em fibras, promovendo o desenvolvimento dos *smart textiles*.

Os transístores-fibra foram fabricados seguindo uma estrutura *gate-all-around*, usando fio de prata com diâmetro de 200 e 500 μm como núcleo (elétrodo de porta), parileno depositado por deposição química de vapor como isolante, óxido semicondutor pulverizado (óxido de índio-gálio-zinco ou óxido de zinco-estanho) e, como elétrodos de fonte-dreno, Al evaporado com máscara de sombra ou Ag por *screen-printing*. Realizou-se uma análise detalhada da espessura de parileno necessária para o bom funcionamento de estruturas metal-isolante-metal (MIM) e transístores, em configurações planares e em fibra. Enquanto que, em estruturas planares, se verificou uma boa qualidade das propriedades isolantes com filmes de 500 nm de espessura, os fios requerem filmes de ≈ 1 μm, devido à rugosidade inicial do fio. Foram desenvolvidas três diferentes gerações de estruturas, otimizando não só o empilhamento de materiais e os processos de deposição, mas também as configurações para medição, que foram consideradas críticas para aceder de forma confiável às propriedades elétricas das estruturas à base de fibras.

Apesar da elevada tensão de operação, devido à espessa camada isolante, os transístores-fibra preparados abaixo de 150 °C apresentam mobilidades superiores a 10^{-2} $cm^2/V.s$, $I_{on}/I_{off} > 10^2$, sem degradação do desempenho após dobramento num raio de 45 mm.

Palavras-chave: transístor de efeito de campo, *smart textiles*, transístor-fibra, deposição química de vapor, *screen-printing*

Abbreviations

1D	One-dimensional
a.u.	Arbitrary units
AC	Alternating current
CEMOP	Center of Excellence in Microelectronics Optoelectronics and Processes
CENIMAT | i3N	Centro de Investigação de Materiais | Instituto de Nanoestruturas, Nanomodelação e Nanofabricação
CVD	Chemical vapour deposition
DC	Direct current
e-fibres	Electronic fibres
e-textiles	Electronic textiles
EDS	Energy Dispersive Spectroscopy
FET	Field-effect transistor
FIB	Focused ion beam
IGZO	Indium-gallium-zin-oxide
IoT	Internet of things
IPA	Isopropyl alcohol
LCD	Liquid crystal display
LED	Light-emitting diode
MIM	Metal-insulator-metal
MISFET	Metal-insulator-semiconductor field-effect transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
NWFET	Nanowire field-effect transistor
OECT	Organic electrochemical transistors
PEN	Polyethylene naphtalate
PVP	Polyvinylpyrrolidone
RF	Radio-frequency
sccm	Standard cubic centimetres per minute
SEM	Scanning electron microscopy
TFT	Thin-film transistor
ZTO	Zin-tin-oxide

Symbols

A	Area
C	Capacitance
C_i	Dielectric capacitance per unit area
d	Thickness
E_C	Conduction band
E_F	Fermi level
f	Frequency
g_m	Transconductance
I	Current
I_{DS}	Current between source and drain
I_{GS}	Leakage current between gate and source
J	Current density
L	Channel length
L	Contact length
m	Mass
N	Carrier concentration
q	Charge
R	Radius
R	Resistance
R_S	Sheet resistance
S	Subthreshold slope
V	Voltage
V_{DS}	Drain-to-source voltage
V_{GS}	Gate-to-source voltage
V_{on}	Turn-on voltage
V_T	Threshold voltage
W	Channel width
$Ø_{wire}$	Wire diameter
δ	Loss angle
ε	Dielectric constant of semiconductor
ε_0	Permittivity of free space (8.854×10^{-12} F/m)

μ_{FE}	Field-effect mobility in linear regime
μ_{sat}	Field-effect mobility in saturation regime
π	Ratio of a circle's circumference to its diameter
ρ	Electrical resistivity
σ	Electrical conductivity

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1. Motivation and Objectives

The smart textiles sector has taken off in recent years, driven by the intense interest in internet-of-things (IoT) [1]. In 2015, the global smart textiles market size was valued at USD 544.7 million with Europe exhibiting a considerable market share of more than 30%. The growing popularity of sophisticated devices with varied technologically advanced functions such as sensing and reacting to the surrounding is anticipated to drive the demand [2]. *Grand View Research* predicts a European market value growth mainly driven by application in military, fitness and architecture sectors, reaching USD 3 billion by 2024 (see Figure 1.1).

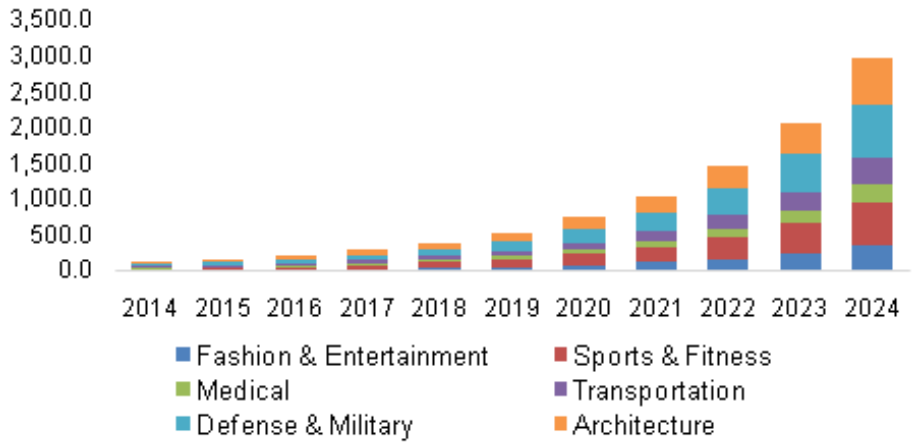

Figure 1.1. European smart textiles market in 2014 and 2015 and the forecast for 2016-2024, in USD million [2].

This work seeks to explore some of the functionalities to be integrated into the next generation fibre-transistors and is part of the European project 1D-NEON (http://1d-neon.eu/).

"The vision of the 1D-NEON project is to create outstanding added value for the textile manufacturing industry. This will be accomplished by developing fibre-based smart materials along with an integrated technology platform for the manufacturing in Europe of new products enabling applications in sensing, lighting, energy and electronics" [3].

The main goal of this master thesis is to produce hybrid transistors, involving the integration of insulating, semiconductive and conductive materials on conductive wires. An organic insulating layer confers good mechanical properties, such as flexibility and an oxide semiconductor layer ensures good electrical properties [4, 5]. Fibre-transistors allow, above all, flexible and cheap technology that could prove useful in building low-cost logic and switching circuits, due to the compatibility of these devices with large-scale/large-area low-cost deposition techniques [5–8].

In order to achieve the main objective, this work consisted in three sub-objectives:

- Optimization of the insulating layer, using metal-insulator-metal (MIM) structures;
- Fibre-transistor stack optimization;
- Establishment of measurement setups for fibre-based devices (MIM and transistors).

2. Introduction

Over the last years, the integration of electronic functionalities in clothing has been a huge target of interest in research, since it promises a variety of new technologies, namely smart clothing and wearable technology [9]. These smart textiles belong to the category of intelligent materials that sense and respond to an environmental stimulus [10].

In addition, technological advancements already made in this new field of studies point to the need for smart materials and electronic components to be integrated directly into fibres, giving rise to electronic fibres (e-fibres), which can be used to build functional circuits [11]. Electronic textiles (e-textiles) result from that integration at the fibre level.

2.1. Electronic textiles: applications in wearable technology

The possibility to integrate electronic functions within the production methods of the textile industry is currently of interest in order to enhance and to add new functionalities to textiles. Among the existing approaches to combine fabrics and electronic functionality, the fabrication of electronic fibres results in the ideal compatibility between textile manufacturing equipment and electronics [12]. The focus on fibre-based devices, such as transistors [4, 13–17], light-emitting diodes (LEDs), solar cells and electrochromic pixels, has been increasing due to their alternative non-planar device architectures, which facilitates their application in wearable technology.

Compared to thin-film devices, fibres have a higher area to volume ratio, enabling not only an increase in the switching speed when applied in transistors, but also being of relevance for other applications such as textile-based sensors and batteries [18, 19].

With the emergence of the wearable technology, an approach oriented to applications is required to take advantage of product opportunities. The integration of technology into fabrics enables a natural and intimate interaction between these two, and the range of applicability is quite large, from smart clothing applied in health care, sports and support of high-risk professionals, to firefighters, with simple soft sensors (temperature or pressure) and actuators that interact with environment, increasing the operator's safety, and also to intelligent furniture in colour-changing curtains and wallpapers [4, 20, 21]. Also noteworthy are commercial applications where electronics including displays and keyboards are integrated into every day clothing [10, 22].

At the same time, the combination of electronic or electromechanical systems and textiles which are not only foldable, but conformable to the human body, represents a breakthrough in various areas of application and opens a new class of human-machine interface technology [16, 17]. Systems based on this type of flexible and smart technology can help to improve radically people's quality of life [16]. In our current modern society, possibly the most captivating application is even the provision of quality health care, delivered through easy-to-use wearable interfaces, to be applied in the field of prevention, monitorization, diagnosis, therapy and even in rehabilitation. In a near future, smart textiles or e-textiles

will be capable of monitoring vital signs for medical patients and hazmat workers, of assisting emergency first-responders and of guiding training for athletes [4, 9, 10, 23, 24]. In addition, biocompatibility of materials is intended in order to promote the application of electronic devices in a biological environment [18, 25].

The vision of an e-textile consists in a fabric that preserves all the properties of its fibres, such as softness, conformability, stretchability and washability, and combines them with electronic functionalities and, for that reason, the choice of fibre materials and functional layers for application in e-textiles plays a main role [12, 26].

In mechanical terms, factors such as bending, stretching and shear must be taken into account in order to prevent degradation and malfunction. In fact, bending and stretching forces during wear can significantly affect the electrical performance of e-fibre devices [11, 26]. As for shear, it can result in two consequences, one of which is the making and unmaking of non-fixed electrical interconnects. The second consequence is abrasive wear associated with shear friction. The weaving process itself can exert significant stress on the material, damaging the e-fibres when the fibres are compacted into a dense textile by the weaving machine [10, 11]. E-textiles, therefore, demand mechanical strength in order to ensure more robust woven [11, 18].

Furthermore, since the subject of this work is a textile, it should also withstand long-term exposure to water and chemicals when washing clothing, without any noticeable degradation, not only of the material itself, but also of the device's performance. To be able to withstand washing, a strong bond between layers and a good environmental stability of the devices is needed [10, 18].

2.2. From planar field-effect transistors to fibre-transistors

Transistors are the key element of most electronic circuits. These electronic devices are normally used as switches, for example, to turn on/off pixels of an active matrix backplane in liquid crystal displays (LCDs) and constitute the basic building block in logic circuits [27, 28].

The metal-insulator-semiconductor field-effect transistor (MISFET) is a field-effect transistor (FET) that, as the name implies, is constituted by a metal, an insulator and a semiconductor layer and uses the electric field to modulate and control the behaviour of the device. Within the MISFET class, we can distinguish three main types of transistors, namely, the metal-oxide-semiconductor field-effect transistor (MOSFET), the thin-film transistor (TFT), and the nanowire field-effect transistors (NWFET), which are slightly similar in terms of operation and composing layers.

For high performance applications, such as microprocessors or memories, MOSFETs are used. In these devices, a silicon wafer acts as the semiconductor and the substrate, and for the modulation of the semiconductor conductance, an inversion region has to be formed close to the dielectric/semiconductor interface [27].

The TFT is a field-effect transistor that depends on an accumulation layer to modulate the conductance of the semiconductor close to the interface with the dielectric. The structure of this device

(Figure 2.1) consists of three electrodes, gate, source and drain, the semiconductor layer placed between the source and drain electrodes, where the channel is formed, and the dielectric layer, used to insulate the semiconductor from the gate electrode. TFT operates as an electrical valve, with the flow of current between the source and drain electrodes controlled by the voltage applied in the gate electrode (V_{GS}). Increasing V_{GS}, charges are capacitively injected near the dielectric/semiconductor interface, creating a conduction channel, through which the current flows from source to drain [9, 15, 27–29]. The magnitude of the V_{GS} applied controls the size of the conduction channel [9, 27].

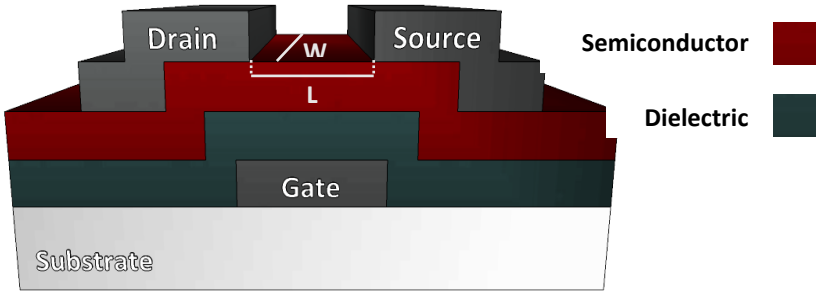

Figure 2.1. Schematic of a staggered bottom-gate TFT with the channel dimensions, width (W) and length (L).

Considering an ideal operation of a n-type TFT, whose Fermi energy (E_F) has a shift towards the conduction band (E_C) relative to the midgap, when V_{GS} is lower than 0 V, a depletion layer near the dielectric/semiconductor interface is created, by repelling mobile electrons, leading to an upward band-bending of the semiconductor close to the dielectric interface. This case, regardless of the drain-to-source voltage (V_{DS}), corresponds to the off-state and a very low current flows between drain and source (I_{DS}) [27, 29].

On the other hand, electron accumulation is reached for $V_{GS} > 0$ V, resulting in a downward band-bending of the semiconductor close to dielectric interface, which becomes more distinct for higher V_{GS} values [27]. Upon the application of V_{DS}, a considerable I_{DS} starts flowing corresponding to the on-state, and depending of the value of V_{DS} and the threshold voltage (V_T), which is the minimum V_{GS} needed to create a conducting path between the source and drain electrodes, different operating regimes can be considered [27, 29]:

- When $V_{DS} < V_{GS} - V_T$ the TFT is in linear mode and I_{DS} is described by:

$$I_{DS} = \frac{W}{L} C_i \mu_{FE} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right] \qquad \textit{Eq. 2.1}$$

where W and L are the channel width and the channel length, respectively, C_i is the gate capacitance per unit area and μ_{FE} is the field-effect mobility, obtained from the transconductance (g_m) with low V_{DS} and described by:

$$\mu_{FE} = \frac{g_m}{\frac{W}{L} C_i V_{DS}} \qquad \textit{Eq. 2.2}$$

The quadratic term can be neglected for very low V_{DS} values, providing a linear relation between I_{DS} and V_{DS}, where the accumulated charges are considered to be uniformly distributed throughout the

channel [27, 29, 30];

- When $V_{DS} > V_{GS} - V_T$ the TFT is in saturation mode and I_{DS} is described by:

$$I_{DS} = \frac{W}{2L} C_i \mu_{sat} (V_{GS} - V_T)^2 \qquad \textit{Eq. 2.3}$$

where μ_{sat} is the saturation mobility, obtained from the g_m with high V_{DS} and described by:

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_{DS}}}{d\,V_{GS}}\right)^2}{\frac{W}{2L} C_i} \qquad \textit{Eq. 2.4}$$

From $V_{DS} = V_{GS} - V_T$, the accumulation layer close to the drain electrode becomes depleted, resulting in the saturation of I_{DS}, phenomenon also known by pinch-off [27, 29].

Output and transfer characteristics, represented in Figure 2.2 (a) and (b), respectively, allow to know the static characteristics of TFTs.

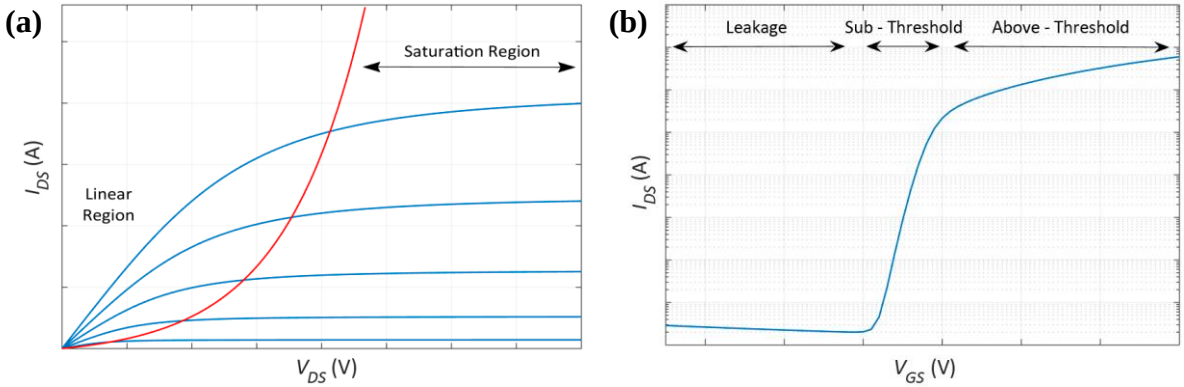

Figure 2.2. Typical characteristics of a n-type TFT, (a) output characteristic; (b) transfer characteristic.

Relating to the output characteristic, where V_{DS} is scanned for different values of V_{GS}, the linear and saturation regimes are clearly noticeable. Through the transfer characteristic, where V_{GS} is swept under a constant V_{DS}, it is possible to extract quantitative electrical parameters such as I_{on}/I_{off} (ratio of the maximum to the minimum I_{DS}), V_T, turn-on voltage (V_{on}, a concept largely used in literature which correspond to the V_{GS} at which I_{DS} starts to increase) and subthreshold slope (S, which indicates the necessary V_{GS} to increase I_{DS} by one decade) that is described by:

$$S = \left(\frac{d \log I_{DS}}{d\,V_{GS}}\bigg|_{max}\right)^{-1} \qquad \textit{Eq. 2.5}$$

The nanowire field-effect transistor typically consists of a semiconductor nanowire surrounded by an insulator and gate electrode, with source and drain electrodes at the ends of the nanowire length [6, 28, 31]. A major advantage of using nanowires is the possibility of having excellent crystalline quality without grain boundaries and one-dimensional (1D) electronic transport, improving transistor performance [5, 32–37]. 1D semiconductor nanostructures have received an increasing interest due to their peculiar and fascinating properties, being attractive building blocks for the future nanoelectronics, since they allow for applications superior to their bulk counterparts [6, 28, 38–40].

Mixing the concept of TFT with NWFET comes the idea of the fibre-transistor, which combines the operation mode of a TFT with the cylindrical structure of NWFET.

Bonderover & Wagner [17] and *Cherenack et al.* [10] described electronic circuits made by weaving together specialized component fibres (spacer fibres, conductor fibres and transistor fibres), and various circuits could be formed by weaving these fibres in different patterns. The transistor fibres have on them amorphous silicon TFTs whose terminals are then connected to the conductor fibres.

Hamedi et al. [13, 14] and *Müller et al.* [18] presented the fabrication of organic electrochemical transistors (OECTs) with low operating voltages, using a simple cross-junction of textile fibres coated with a conjugated polyelectrolyte, in which the gap between the two fibres was bridged with a drop of an electrolyte mixture. The main disadvantages of this type of devices are the low speed of operation and the mode of operation, being restricted to only depletion mode, which complicates the design of logic circuits [9, 13, 14, 18].

Another approach, which was the basis for this work, involves the planar-FET in a coaxial architecture, as presented in Figure 2.3. In this case, the fibre-transistor consists of a conductive fibre, playing the role of gate electrode, coated with a dielectric material, which is covered by a semiconductive layer on which, in turn, the source and drain contacts are placed [4, 9, 15, 41]. The processing of transistors manufactured directly on fibre is very complex, due to the cylindrical topology, which introduces surface curvature and torsion effects and this is the biggest reason for not having been extensively investigated and fully optimized [4, 9, 30].

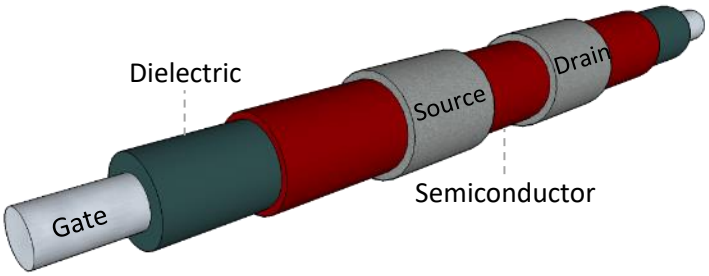

Figure 2.3. Schematic of a gate-all-around fibre-transistor structure.

In 2003, for the first time, *Lee & Subramanian* [4, 41] demonstrated a flexible transistor fabricated with a very similar structure, using aluminium fibre coated with an oxide gate dielectric and, as semiconductor, pentacene. The source and drain contacts were made by gold evaporation and a channel length of 50 µm was defined using a shadowing technique. Also *Maccioni et al.* [15] developed a transistor using polyimide as dielectric and pentacene as semiconductor. In both cases, mobility presented values around 10^{-2} $cm^2/V.s$ and considerable high operation voltages [4, 15, 41].

Similar to this work, *Münzenrieder et al.* [12] reported fibre-transistors, using nylon and glass fibres coated with chromium, parylene as dielectric layer, InGaZnO (IGZO) as semiconductor and titanium/gold for the contacts. The fact that it is a hybrid device allows to take advantage of the constituting layers' properties. The oxides ensure good electrical proprieties of the device and the organic ones are responsible for the good mechanical properties, such as flexibility [4, 5, 42]. Their results show that this fabrication of TFTs seems possible, but the problems associated with the surface roughness and the high operation voltages exclude any useful application [12].

3. Materials and Methods

Since the device's architecture plays a main role in the transistor's performance, this work was dedicated to the fabrication and optimization of the fibre-transistors. The main challenge during this work was to use fabrication processes suitable for e-textile integration.

The generic structure of the produced transistors, as presented in section 2.2, Figure 2.3, is composed of a conductive fibre, coated with an insulating layer, which in turn is covered by a semiconductor layer, on which the source and drain contacts were defined, and several approaches have been tested during this work, including different materials and techniques.

3.1. Fabrication of MIM and FET structures on fibres

This section is divided into sub-sections explaining the different approaches followed to build three distinct generations of devices. Throughout the different generations MIM and FET structures were produced in parallel.

The devices were obtained starting from silver wires (Ag), acting as gate electrodes. Two different diameters ($Ø_{wire}$), namely of 200 and 500 µm, and ≈ 8 cm of wire length were used for each test.

3.1.1. Generation 1 (Gen1)

The first generation produced involves the test of different dielectrics as well as some electrical contact tests to characterize the gate dielectrics. The Ag wires were coated with 2 and 1.5 g of parylene C, deposited by chemical vapor deposition (CVD) in specialty coating system PDS 2010 [43, 44], with a pressure between 11 to 15 mTorr. To ensure a good adhesion of parylene C, the wires were vertically placed in the parylene chamber system (Appendix A.1) and exposed to a silquest A-174 silane, the adhesion promotor, following the procedure of *Fernandes* [45]. Because of the conformability of the deposition, which permits the coating of the wire along its entire perimeter, kapton tape was used to protect the edges of the wires so as to allow subsequent access to the gate electrode. In each parylene deposition, a silicon wafer was also coated allowing to measure the insulating thickness deposited.

At the same time, polyvinylpyrrolidone (PVP), an organic polymer deposited by dip coating, was tested as insulating layer, using an established procedure in CENIMAT|i3N.

To characterize the gate dielectrics, MIM capacitors were made using different techniques to form top electrodes, including another Ag wire perpendicularly placed on top of the gate wire; a drop of silver glue over the wire; a piece of indium sheet wrapped around the wire perimeter, and also a piece of an indium sheet placed below the wire with a drop of silver glue to cover the wire.

3.1.2. Generation 2 (Gen2)

In this device generation, based on the outcomes of Gen1, Ag wires with 500 µm of diameter were used and parylene C was applied as dielectric following the same procedure described in section 3.1.1, only changing the arrangement of the wires during deposition from horizontal to vertical direction

(Appendix A.2). To study the effect of the dielectric layer and its uniformity along the wires' surface, devices were produced with different parylene thicknesses, between 0.2 and 1.5 μm.

The main change of this generation involves aluminium thermal evaporation to create the top electrical contacts on MIM fibre structures. To pattern the contacts, a shadow mask with lines of 4 mm separated by 10 mm (Appendix B.1) was designed in Adobe Illustrator and laser cut on polyethylene naphtalate substrate (PEN). The aluminium deposition was performed using a carrier fibre-rotation system developed in-house to promote the deposition of conductive material along the wire perimeter, providing mechanical support at the same time (Appendix C). The aluminium thickness measured using a quartz crystal during the deposition was 100 nm.

For the characterization of the gate dielectric, a new test setup was necessary. With a thickness of 80 nm, aluminium conductive lines of 7 mm separated by 7 mm (Appendix B.2) were deposited on a 10×10 cm glass and connected to the electrodes in the wires with a drop of silver glue, following the procedure presented in Figure 3.1. Previous to deposition, all glass substrates were cleaned in an ultrasonic bath in acetone, then in isopropyl alcohol (IPA), both for 15 min at 60 °C, cleaned in Millipore water and dried under N_2. To increase the setup mechanical stability, one drop of epoxy resin was placed on each side of the wire and copper tape was used to connect with the core electrode.

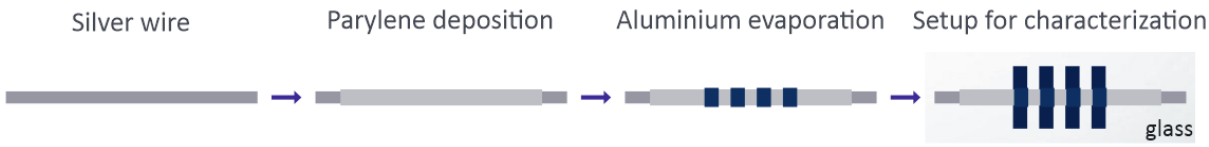

Figure 3.1. Steps for the fibre-MIM capacitor fabrication and its setup assembly.

Concerning the fibre-transistors, a previously established process to sputter indium-gallium-zinc oxide (IGZO) at CENIMAT|i3N was used [46], in an AJA ATC-1300-F system. IGZO films were sputtered using radio-frequency (RF) power, an Ar:O_2 atmosphere and a ceramic target with 2:1:1 (In:Ga:Zn atomic ratio), for 18 min. The same fibre-rotation system used for Al evaporation was also used for IGZO to promote the material deposition throughout the wire perimeter. The transistors were hot plate annealed at 150 °C for 1h in ambient conditions. Instead of aluminium evaporation, the source and drain contacts were made with 2 mm wide copper tape, with a separation (i.e., channel length) of 1 mm, fixed on the glass and connected to the wire with silver glue.

In parallel, MIM and TFT planar structures were fabricated in 2.5×2.5 cm corning glass (Appendix D.1 and 2), using the same insulating and semiconductor layers and aluminium for electrodes (80 nm thickness), enabling the comparison between planar and fibre-based devices.

3.1.3. Generation 3 (Gen3)

The characteristic that define this generation was the usage of the screen-printing technique of commercial silver ink (PE-AG530-Flexible Silver Conductive ink) [47] to create the electrical contacts on wire. Similar to Gen2, the parylene layer was deposited following the procedure in section 3.1.2. In this generation, both Ag wires were used to produce devices (200 and 500 μm of diameter).

Capacitor contacts with a length of 2 mm separated by 500 μm (consult Appendix E. 1) were screen-printed on a 10×2.5 cm glass and, without moving the mask or the glass, the wire was carefully placed on top of the ink. After fixing the wire to the glass, with kapton tape, another printing of silver ink was performed in the exact same place. Only after this last printing, the silver ink was dried at 120 °C for 5 minutes.

By adding the semiconductor deposition (without fibre-rotation system, more details in results and discussion section), transistors were formed on wire using identical fabrication steps, except for the mask for top contacts, that includes channel lengths between 500 to 100 μm, with a step of 50 μm (Appendix E. 2). The IGZO was also used in these devices but, due to a system problem, zinc-tin oxide (ZTO) started to be deposited, in an AJA ATC 1800. This was accomplished using RF power, $Ar:O_2:H_2$ atmosphere and a target with 1:1 Zn:Sn atomic ratio, for 8 min 45 s. An annealing at 150 °C for 1h was performed in ambient conditions.

As in section 3.1.2, a drop of epoxy resin was placed on each side of the printed pattern to increase the mechanical stability of the devices.

For final experiments, to promote a bending test characterization, the silver ink was just printed on one side of the wire, without the glass carrier.

3.2. Characterization techniques

The wires' resistivity was measured with BS407 Precision Milli/Micro Ohmmeter and the ink's resistivity was obtained with four-point probe technique in Jandel Engineering Ltd.

All parylene film thicknesses were measured on a silicon wafer using a profilometer Ambious Technology XP-200.

The electrical characterization of MIM capacitors was performed by capacitance-voltage (*C*-*V*) measurements (-2 to 2 V direct current (DC), superimposing an alternating current (AC) signal of 100 mV and 100 kHz), and by capacitance-frequency (*C*-*f*) measurements, in the range of 1 kHz to 1 MHz using a Keysight B1500A and a Cascade EPS150 Triax probe station. To measure the capacitance at low frequencies, a lock-in amplifier, Stanford research systems, model SR830, was also used. Current-voltage (*I*-*V*) characteristics were obtained in continuous mode, between -2 to 2 V, using a semiconductor parameter analyzer Agilent 4155C and an Agilent 16442A Test Fixture. To measure dielectric breakdown field current-voltage measurements were expanded up to 200 V.

Relating to fibre-transistors, transfer and output characteristics were obtained in ambient conditions inside a Cascade M150 probe station using a semiconductor parameter analyzer Agilent 4155C. Bending tests were performed in some fibre-transistors, which were characterized before and during the bending. For that, an half-round cylinder, with a radius of 45 mm, was used to apply a constant tensile strain during the electrical measurement [30].

The wires surface morphology, and the different layers required for the fibre-transistors were analysed by scanning electron microscopy (SEM), Zeiss Auriga Crossbeam electron microscope.

4. Results and Discussion

In this chapter, all the steps and trials that led to the stacked layers' optimization and the establishment of the final measuring setup are described and studied.

Since the Ag wires play a central role in this type of devices and their surface roughness can perturb the formation of a smooth gate dielectric layer and decrease its electrical strength by increasing the effective electric field [4, 12, 30], a surface analysis was performed (Figure 4.1). As shown in the SEM image, Figure 4.1 (b), the wire presents some disturbances on the surface and, through the profilometer, a surface roughness of about 1 μm was measured.

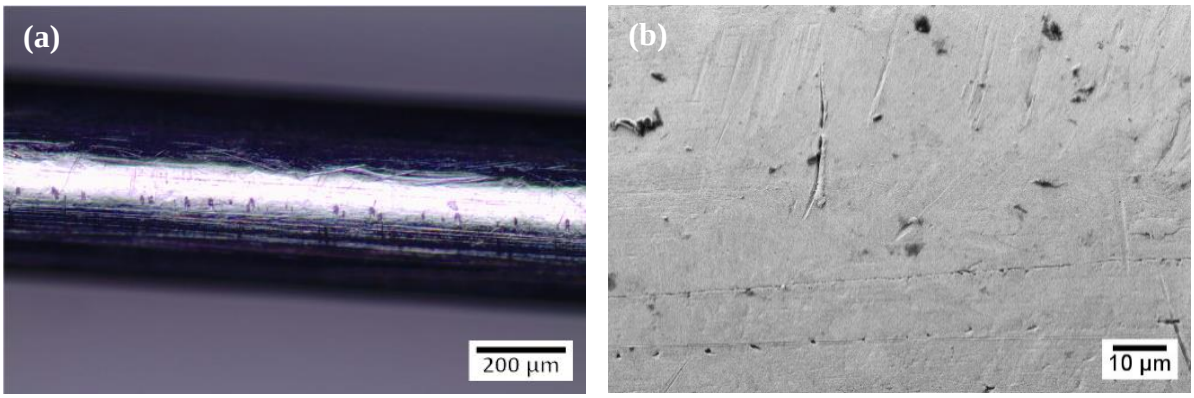

Figure 4.1. Ag wire's surface, (a) by optical microscope; (b) by SEM, with a secondary electron detector.

The electrical resistivity (ρ) of the Ag wire was calculated by measuring its resistance (R) at a known wire length. The calculated silver resistivities, presented in Table 4.1 for the wires with approximately 200 μm and 500 μm diameter but considering the measured diameters (Appendix F), are very close to the values reported in literature, 1.59×10^{-6} Ω.cm [48].

Table 4.1. Resistivity of Ag wires with a diameter of 500 and 200 μm, and the respective standard deviation.

$Ø_{wire}$ (μm)	ρ (Ω.cm)	Standard deviation (Ω.cm)
200	1.84×10^{-6}	0.06×10^{-6}
500	1.69×10^{-6}	0.01×10^{-6}

4.1. Generation 1 (Gen1)

During this generation, two different parylene thicknesses were studied as the insulating layer. Considering the mass of parylene C's dimer used in the deposition, theoretically, the thickness of the deposited parylene should follow the equation:

$$d = 0.62\times m^{0.97} \qquad \textit{Eq. 4.1}$$

where d is the film thickness (nm) and the m is the dimer mass (mg) [44]. Table 4.2 presents the comparison between the expected thickness, based on the equation above, and the experimental average thickness, measured with the profilometer on a silicon wafer. For each sample, at least 5 measurements were made to ensure the most reliable value. The average thickness was about 300 nm higher than expected, which, as verified in parallel works, is related to the cleanliness of the parylene deposition system itself.

Table 4.2. Comparison between the expected thickness, following the Eq. 4.1, and the experimental average thickness measured on a silicon wafer, with the respective standard deviation.

m_{dimer} (g)	Expected thickness (µm)	Experimental thickness (µm)
2.00	1.01	1.43 ± 0.06
1.50	0.76	1.02 ± 0.05

The morphology of the parylene coating with a thickness ($d_{dielectric}$) of 1.43 µm, was also analysed in optical microscope and in SEM. In Figure 4.2 (a) is possible to observe that parylene provides a conformal coating of the wire. Still, it is not enough to planarize all the features observed in the wires, as some are deeper/higher than the parylene thickness itself (Figure 4.2 (b)).

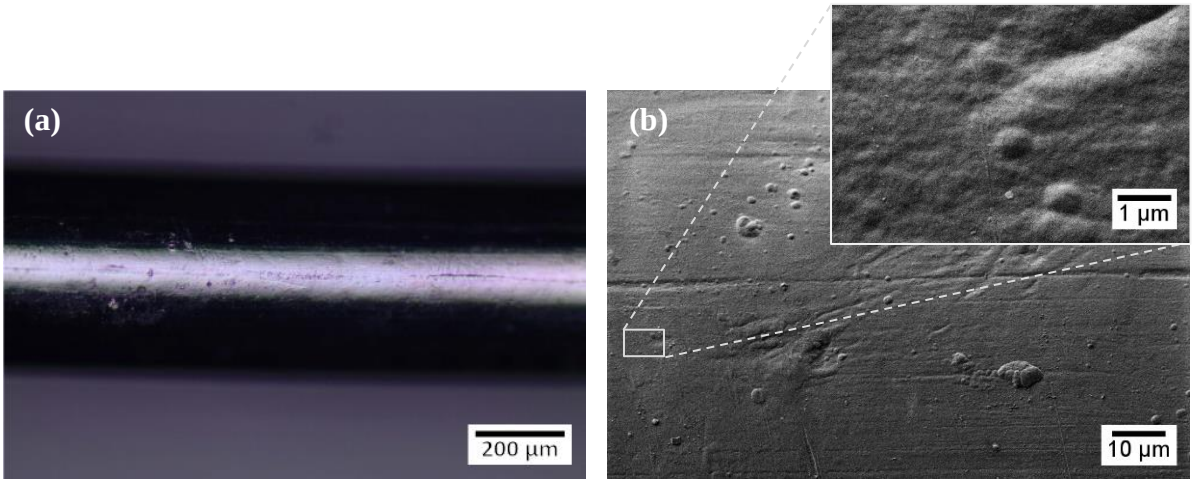

Figure 4.2. Surface of 1.43 µm of parylene coating on an Ag wire, (a) by optical microscope; (b) by SEM, with a secondary electron detector.

The electrical characterization of the insulating layer was made by using metal-insulator-metal fibre structures. As schematized in Appendix G, these surrounding MIM capacitors are composed of a conductive core (one of the electrodes), a dielectric layer around the core, and a second electrode, over the dielectric. The capacitance (C) of cylindrical MIM capacitors is given by the charge (q) over the potential difference between the contacts (V), according to the equation:

$$C \equiv \frac{q}{V} = \frac{2\pi\varepsilon_0\varepsilon L}{\ln\left(\frac{R_2}{R_1}\right)} \qquad \textit{Eq. 4.2}$$

where ε_0 is the permittivity of free space, ε the dielectric constant of the semiconductor, L the contact length, and R_1 and R_2 the radius of the centre to the insulating layer and to the top electrode, respectively.

On the other hand, the current density is given by the current (I) over the contact area (A), that in the case of cylindrical capacitors is described by:

$$J = \frac{I}{A} = \frac{I}{2\pi R_2 L} \qquad \textit{Eq. 4.3}$$

As presented in Figure 4.3, various approaches were attempted for the top electrodes of capacitors, starting from conductive wires with different diameters parallelly placed over the insulated wire, a drop of silver glue over the wire, a piece of indium sheet placed wrapped around the wire perimeter, to a piece of indium sheet placed under the wire with a drop of silver glue to cover the wire. The electrical characterization was made between the Ag wire (the core of the structure), which, during the parylene

deposition was protected with kapton tape, and one of these top electrodes.

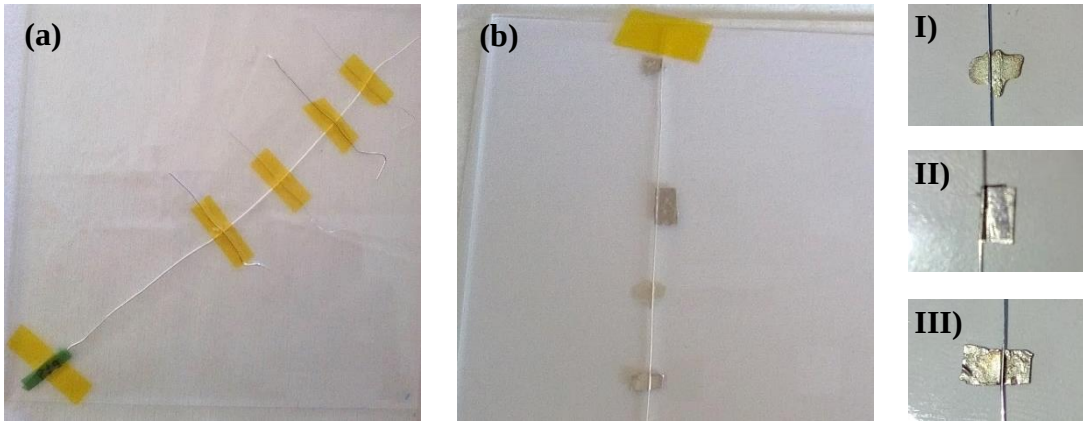

Figure 4.3. MIM capacitors with different top electrodes, (a) using Ag wires with different diameters; (b) I) using a drop of silver glue; II) using an indium sheet wrapped around the wire perimeter; III) using an indium sheet below the wire and a drop of silver glue.

Using conductive wires on top of the insulated wire, Figure 4.3 (a), and by applying voltage between the conductive core and this top electrode wire, the tendency was to reach the current compliance, which means that a lot of current passed through the dielectric, superior to 1 μA. Despite the high field due to the point contact, since this assembly included the pressure of the wires against each other, the parylene layer broke in some regions, which explains the high leakage current. Moreover, the fact that the wires covered with lower dielectric thickness (1.02 μm) had higher failure rate shows already the need to work with thick coatings to guarantee the mechanical integrity of these layers.

Regarding the drop of silver glue Figure 4.3 (b) I), this electrode was also not very efficient, since its spreading could not be controlled, not guaranteeing the covering of the whole wire perimeter. In addition, the silver glue does not have enough mechanical strength to keep the wire attached to the glass, which is necessary to allow for an easy access to the contact, without applying mechanical stress to the wire.

With 0.5 cm of length of indium sheet wrapped around the wire perimeter as well as with 0.2 cm of length of indium sheet placed under the wire with a drop of silver glue to cover the wire (Figure 4.3 (b) II) and III)) the breaking of the insulating layer occurred less frequently and a current in the order of pA was measured. Regarding capacitance, no significant variation was detected with the voltage in *C*-*V* curves (at 100 kHz). In capacitance per area as a function of frequency (*C*/*A*-*f*), using an indium sheet wrapped around the wire perimeter, Figure 4.4 (a), and using an indium sheet placed under the wire with a drop of silver glue, Figure 4.4 (b), both cases show the influence of the dielectric layer's thickness on the structure, where lower thickness leads to a higher capacitance per area value, as expected. It is readily noticeable that, although there is not a very large dependence of the capacitance on the frequency, the values obtained using the two approaches for top electrodes are significantly different (more than one order of magnitude), which indicates that the measurement setup using the indium sheet and silver glue allowed a better coverage of the wires' surface.

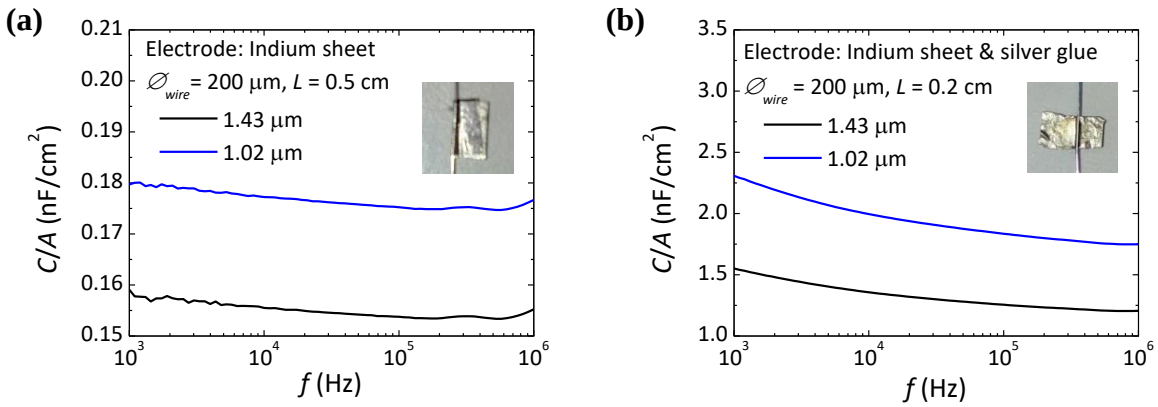

Figure 4.4. C/A-f curves of fibre-MIM capacitors, with different parylene thickness, (a) using indium sheet wrapped around the insulated wire as top electrode; (b) using indium sheet under the insulated wire and silver glue as top electrode.

In Table 4.3, a comparison between the expected and experimental capacitance is presented, using the previous two approaches, as well as the calculated dielectric constant. Looking at the capacitance, the experimental values are much lower than the expected, reaching a difference of one order of magnitude using just the indium sheet, which may be related to the fact that the sheet does not completely contact with the entire perimeter of the wire, decreasing the contact area. The indium sheet with silver glue showed better results, with higher dielectric constant values, nevertheless, still far from the expected, which is approximately 3.0 at 100 kHz for parylene [44, 49].

Table 4.3. Comparison between the expected and measured capacitances using, as electrodes, an indium sheet wrapped around the insulated wire, and an indium sheet over the wire with silver glue to involve the wire.

L (cm)	$\varnothing_{wire}$ (µm)	$d_{dielectric}$ (µm)	$C_{expected}$ (pF)	$C_{measured}$ (pF)	ε
0.50 (Indium sheet)	500	1.43	155.15	5.32	0.11
		1.02	218.63	10.01	0.15
	200	1.43	60.94	4.77	0.25
		1.02	85.77	5.39	0.20
0.20 (Indium sheet and silver glue)	500	1.43	62.06	N/A	N/A
		1.02	87.45	36.90	1.35
	200	1.43	24.38	15.58	2.03
		1.02	34.31	22.68	2.10

From these first tests, the need of a good support and setup for measurements became evident, so that the wire did not have to be subjected to much mechanical stress.

Similar measurements' setups were tested for PVP coated wires, but without success. The silver glue, for instance, because it is composed by acetone, diluted the PVP layer, resulting in high leakage current measured between the electrodes.

4.2. Generation 2 (Gen2)

To guarantee a high capacitance and to work at low operating voltages, fibre-FETs require a very thin and uniform insulating layer between the gate and the semiconductor. However, a detailed investigation on the minimum required thickness to ensure good insulation between gate and semiconductor had to be made, particularly for a rough structure as the wire.

During this generation, five different thicknesses of insulating layer were studied. In Table 4.4 are presented the dimer masses used and the expected and experimental thicknesses of insulating layer, according Eq. 4.1 and measured on a silicon wafer, respectively.

Table 4.4. Comparison between the expected thickness, following the Eq. 4.1, and the experimental average thickness measured on a silicon wafer, with the respective standard deviation.

m_{dimer} (g)	Expected thickness (µm)	Experimental thickness (µm)
2.50	1.25	1.45 ± 0.01
2.00	1.01	1.14 ± 0.03
1.50	0.76	0.96 ± 0.02
0.75	0.39	0.46 ± 0.02
0.30	0.16	0.24 ± 0.02

In Figure 4.5 is plotted the expected and the experimental parylene thicknesses and their respective fittings.

Relatively close to the literature (Eq. 4.1), the non-linear fit of the experimental average thickness is described by:

$$d = 1.31 \times m^{0.90} \qquad \textit{Eq. 4.4}$$

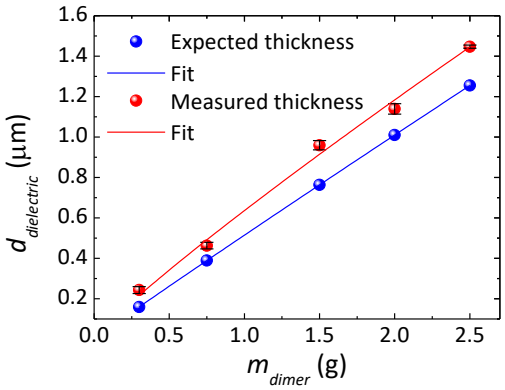

Figure 4.5. Fitting of the expected and measured parylene thickness with the dimer mass.

4.2.1. Characterization of MIM capacitors

4.2.1.1. Planar structures

In Appendix D.1 are presented the capacitors in planar structures fabricated to compare with the capacitors in fibre structures. Each planar sample is composed of six MIM capacitors with different area dimensions, as presented in Table 4.5, and all of them were characterized, without annealing, using *C-V*, *C-f* and *I-V* measurements.

Table 4.5. Designed and experimental area dimensions of the MIM capacitors, in planar structures.

$A_{designed}$ (mm^2)	4.00	2.25	1.00	0.56	0.25	0.06
$A_{experimental}$ (mm^2)	4.14	2.44	1.21	0.77	0.41	0.17

Related to *C-V* and *C-f* characterization, in neither curves occurred any significant variation of capacitance. The values of capacitance with the different contact areas, for the five different dielectric

thicknesses, at 100 kHz (Appendix H.1), are summarized in Figure 4.6 (a). For each dielectric thickness, the capacitance behaviour as a function of area follows a linear distribution, increasing the capacitance with an increase of capacitors' area and registering a slope increase with the dielectric thickness decrease, as expected according the capacitance equation of planar capacitors:

$$C = \frac{\varepsilon_0 \varepsilon A}{d_{dielectric}} \qquad \textit{Eq. 4.5}$$

Through the contact area, the capacitance per unit area was calculated (Appendix H.2). In Figure 4.6 (b) is presented the dependence of the capacitance per unit area on dielectric thickness for the different contact area, being observed the capacitance scaling with thickness and area, as expected. With an increase of dielectric thickness, the specific capacitance decreases. In addition, it is possible to observe that, for the different areas, the graphs are very coincident, however, they present a dispersion for thinner films, since for smaller parylene thicknesses there is greater variation of the same along the substrate.

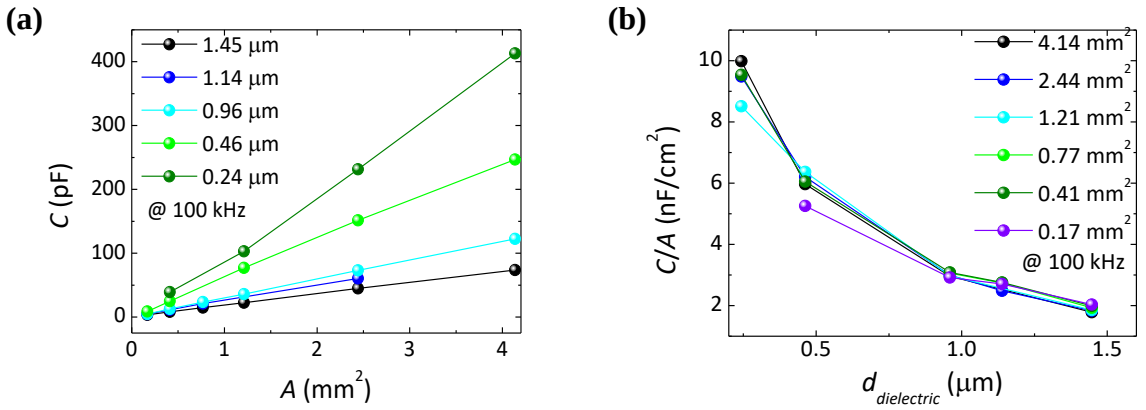

Figure 4.6. (a) Variation of the capacitance values with the MIM area, for different parylene thicknesses; (b) variation of capacitance per unit area with dielectric thickness, for different contact area.

To understand how much the discrepancy of these values was related to the literature, the dielectric constant was also calculated. Considering the five thicknesses and the six areas, the average dielectric constant value, 3.1 ± 0.3, at 100 kHz, is very close to the theoretical dielectric constant of parylene, approximately 3.0 at the same frequency [44, 49], so no electrical problem was detected in this layer. Table 4.6 summarizes the results of four different area capacitors. Only the thinner parylene film shows a greater discrepancy from the expected dielectric value, due to such non-uniformity of the parylene with these thicknesses.

Table 4.6. Calculated dielectric constant of four MIM devices' area with different dielectric thicknesses. The data for certain devices is not available due to high leakage current.

$d_{dielectric}$ (µm)	ε			
	$A_{theoretical}$ (mm²)			
	4.14	2.44	1.21	0.41
1.45	2.91	3.00	3.03	3.25
1.14	N/A	3.19	N/A	3.55
0.96	3.21	3.25	3.22	3.34
0.46	3.12	3.24	3.33	3.16
0.24	2.74	2.60	2.34	2.62

To confirm that the capacitance values were correct, the capacitor with 2.44 mm^2 of contact area, in the sample with 0.96 µm of parylene thickness, was measured with an LCR analyser, from 100 Hz to 10 MHz. Additional data was collected with a lock-in amplifier from 0.1 Hz to 1 kHz, to verify if, at low frequencies, the capacitance value, and consequently the dielectric constant, would remain similar across a broad range of frequencies, not compromising a correct extraction of parameters from the DC analysis. The values obtained in both equipments are in agreement, and no high capacitance variation was observed at low frequencies, presenting a dielectric constant of 3.48 at 100 kHz, calculated based on LCR measurements, and a dielectric constant of 4.10 at 1 Hz was calculated based on lock-in measurements. Relative to the Figure 4.7 (b), both graphs match, being the loss tangent smaller than 10% at 0.1 Hz.

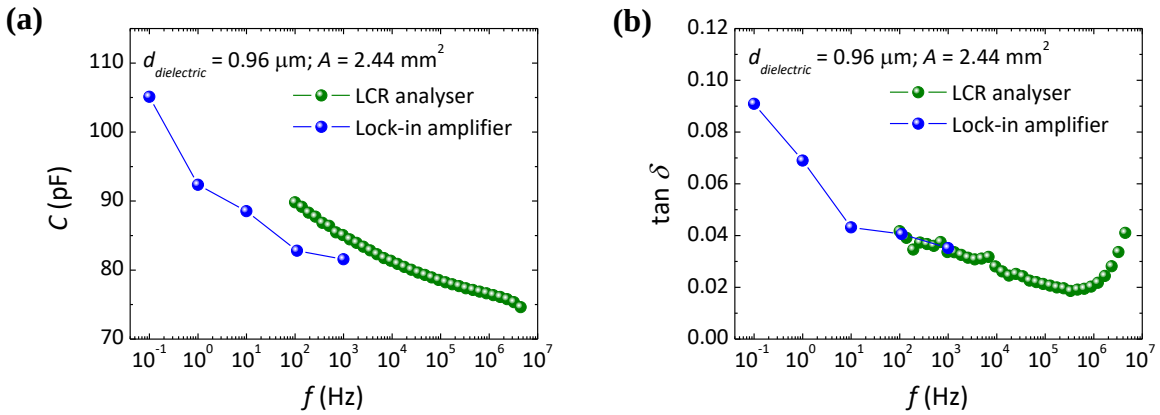

Figure 4.7. LCR and lock-in measurements as a function of frequency of the capacitor with 2.44 mm^2 of contact area, in the sample with 0.96 µm of parylene thickness, (a) in capacitance; (b) in loss tangent.

Through the *I-V* curves, the resistivity was extracted considering the inverse of the *I-V* curves' slope. With an average of $(7 \pm 3)\times10^{12}$ Ω.m, the resistivity values obtained (summarized in Table 4.7), are good for an insulating layer, and relatively close to the parylene surface resistivity in literature, 1×10^{13} Ω.m [44, 49].

Table 4.7. Calculated resistivity of each MIM devices area with different dielectric thicknesses. The data for certain devices is not available due to high leakage current.

$d_{dielectric}$ (µm)	ρ (Ω.m)			
	$A_{theoretical}$ (mm^2)			
	4.14	2.44	1.21	0.41
1.45	1.13×10^{13}	6.65×10^{12}	4.61×10^{12}	5.84×10^{12}
1.14	N/A	1.27×10^{13}	N/A	8.04×10^{12}
0.96	4.56×10^{12}	4.21×10^{12}	2.94×10^{12}	4.23×10^{12}
0.46	1.46×10^{13}	9.02×10^{12}	1.00×10^{13}	3.77×10^{12}
0.24	7.14×10^{12}	8.72×10^{12}	7.75×10^{12}	N/A

Theoretically, the DC breakdown voltage of parylene C is higher than 700 V for 1 µm thickness [50], which corresponds to a breakdown field up to 7 MV/cm. The MIM capacitors were subjected to a sweep of 0 to 100 V and the dielectric breakdown was not reached in any device. By calculating the electric field at 100 V for each thickness (Appendix H.3), it is possible to verify that, under that voltage, the electric field is still below the breakdown field in the literature.

The current density of each device was obtained at the voltage necessary to generate an electric field of 0.1 MV/cm. As summarized in Table 4.8, the low current density obtained, between 10^{-12} to 10^{-8} A/cm^2, presented acceptable range for an insulant layer.

Table 4.8. Calculated current density when an electric field of 0.1 MV/cm was applied, of each MIM devices area with different dielectric thicknesses. The data for certain devices is not available due to high leakage current.

$d_{dielectric}$ (μm)	J @ E = 0.1 MV/cm (A/cm^2)			
	$A_{theoretical}$ (mm^2)			
	4.14	2.44	1.21	0.41
1.45	4.35×10^{-10}	5.90×10^{-10}	7.08×10^{-10}	1.27×10^{-10}
1.14	N/A	5.16×10^{-10}	N/A	8.95×10^{-10}
0.96	7.98×10^{-10}	7.25×10^{-10}	7.33×10^{-10}	2.23×10^{-9}
0.46	9.00×10^{-10}	4.54×10^{-9}	1.59×10^{-9}	1.18×10^{-8}
0.24	3.26×10^{-12}	4.86×10^{-10}	5.39×10^{-11}	N/A

4.2.1.2. Fibre structures

For Gen2, to simplify the study and because they were easier to work with, only the thicker wires were used ($Ø_{wire}$ of 500 μm). Regarding the placement of the wires inside the parylene system's chamber, in Gen1 they were vertically arranged, however, once a thickness variation was observed in different shelves, the wires began to be placed horizontally to minimize process variations (Appendix A.2). Comparing with a parylene coating of 1.43 μm previously presented (Figure 4.2), for a parylene coating of 0.24 μm a greater non-uniformity of the surface layer was detected in SEM (Figure 4.8 (b)).

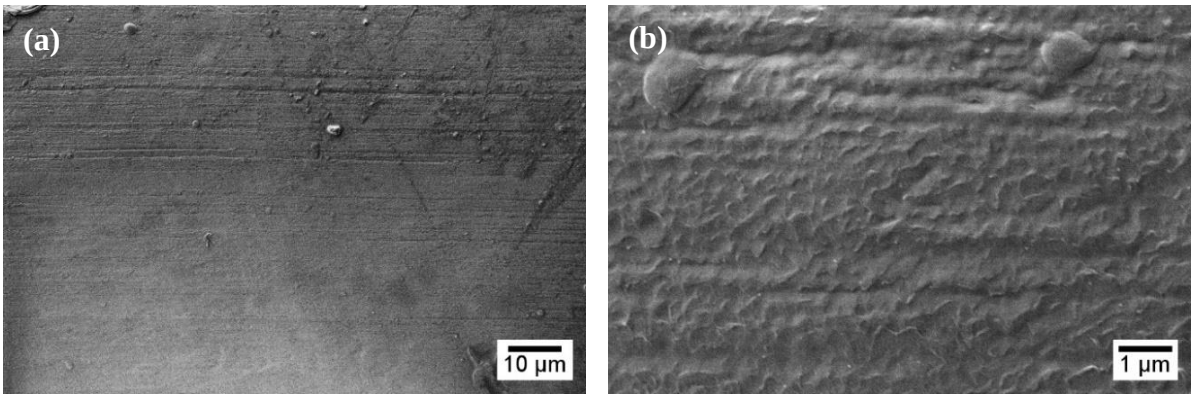

Figure 4.8. (a) and (b): Surface of a 0.24 μm parylene coating on an Ag wire, by SEM, with a secondary electron detector.

Relating to the evaporation of aluminium, a damaged part of the insulating layer was observed (Figure 4.9 (a)), being noticeable a peeling of parylene in the region used to fix the wire to the fibre-rotation system. Moreover, due to the distance between the wires and the PEN shadow mask, placed over the fibre-rotation machine to define the top electrode area, a significant shadow effect was observed. Also, given that the fibre-rotation machine was used to deposit Al, so the entire perimeter of the wire could be coated, the thickness of the deposited layer was significantly reduced when compared to planar structures. Non-uniformities on the wires' surface after coating could be seen (Figure 4.9 (b)), which can be related not only to the low aluminium adhesion but also to the roughness of the wire prior to the coating.

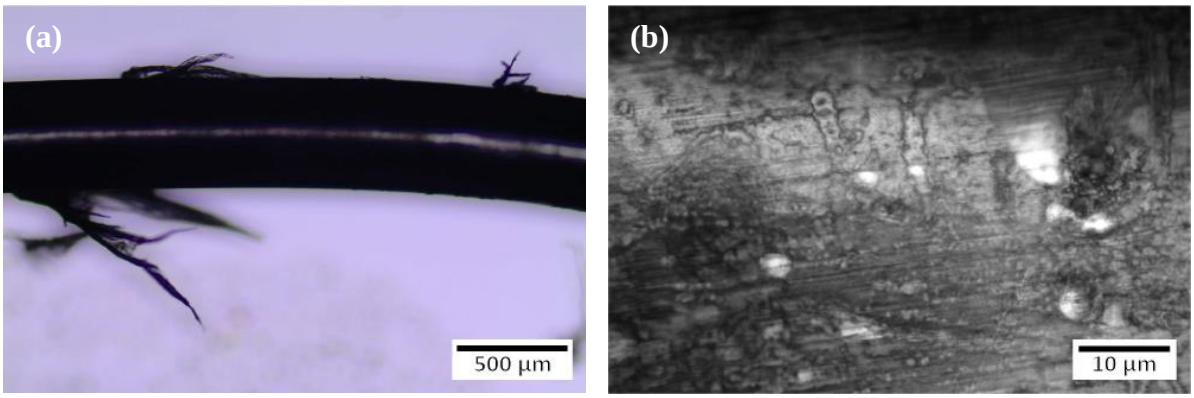

Figure 4.9. Images of an Ag wire coated with parylene after the deposition of aluminium using the fibre-rotation system, (a) peeling of parylene layer on wires, by optical microscope; (b) non-uniformity of aluminium layer, by confocal microscope.

In the same wire, four MIM capacitors were characterized using *C-V*, *C-f* and *I-V* measurements, and the electrical parameters were extracted assuming the aluminium contact length of 4 mm, as defined in the designed mask. The curves were obtained using crocodile clamps for the access, one in conductive tape wrapped in the silver core, to avoid the direct contact with the wire, reducing the mechanical stress, and the other in an aluminium line patterned in glass connected with silver glue to the aluminium contact in wire, as showed in Figure 4.10.

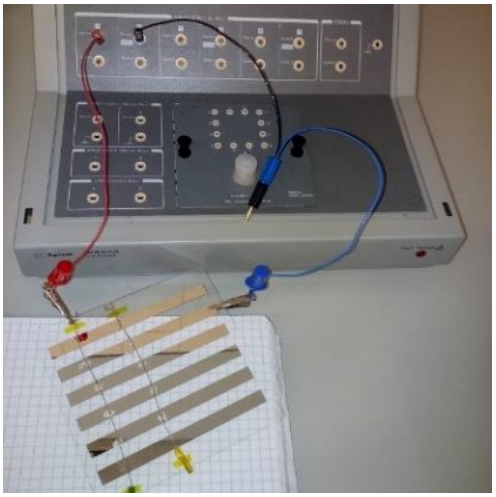

Figure 4.10. Setup for the MIMs characterization that consists in the access to both electrodes, a conductive tape wrapped in the conductive core and an aluminium line patterned in glass, connected with silver glue to the aluminium contact on a wire.

Regarding the capacitance measurements, there was no significant capacitance variation with DC voltage or frequency. The capacitance values, at 100 kHz, for each parylene thickness, are present in Table 4.9, as well as their capacitance per unit area and the dielectric constant. However, from the dielectric constant values, only the data for the thicker parylene layer seems to be reliable, related to an increased sturdiness of the sample. Also, the considerable roughness observed on the wire surface, before any of the depositions, strongly limits the implementation of thinner parylene layers on the surface.

Table 4.9. Capacitance, capacitance per unit area and dielectric constant of fibre-MIM capacitors, using different dielectric thicknesses, from C-V curves at 100 kHz. The data for certain devices is not available due to high leakage current.

$d_{dielectric}$ (µm)	C (F)	C/A (F/cm^2)	ε
1.45	7.30×10^{-11}	1.16×10^{-9}	1.90
1.14	6.22×10^{-12}	9.91×10^{-11}	0.13
0.96	1.08×10^{-12}	1.72×10^{-11}	0.02
0.46	5.16×10^{-12}	8.24×10^{-11}	0.04
0.24	N/A	N/A	N/A

Regarding the *I-V* curves, the current density and the resistivity were extracted. Effectively, a much higher current density was obtained with the thinner insulant layer. Since parylene films in planar structures presented values very close to those expected, the existence of problems with the measurements setup is recognized.

Table 4.10. Calculated current density, from the measured current when 2 V were applied, and resistivity of fibre-MIM capacitors, using different dielectric thicknesses.

$d_{dielectric}$ (μm)	J @ 2 V (A/cm^2)	R (Ω)	ρ (Ω.m)
1.45	1.30×10^{-10}	5.27×10^{11}	2.29×10^{12}
1.14	3.05×10^{-10}	1.09×10^{11}	5.99×10^{11}
0.96	1.01×10^{-10}	3.41×10^{11}	2.23×10^{12}
0.46	5.85×10^{-11}	9.71×10^{11}	1.31×10^{13}
0.24	3.59×10^{-6}	7.99×10^{7}	2.06×10^{9}

The results of fibre-capacitors shown are not conclusive, and many problems were found in the test setup. The main problem was in the access to the deposited aluminium contacts in order to ensure physical stability of the setup. Sometimes, the silver glue, which established the contact between the aluminium electrode on the wire and the aluminium contact on the glass, when a physical pressure was exerted on the wire, damaged the aluminium that was deposited in the glass. Also, the silver glue is not a good option, since its lateral spreading could not be properly controlled.

4.2.2. Characterization of field-effect transistors

4.2.2.1. Planar structures

In this section, and based on the results of capacitors in wires, only the three thicker insulating layers were studied. In Appendix D.2 the fabricated common gate TFTs in planar structures with *W/L* of 1000/100 (measured of 8.93 ± 0.26) are presented. Transfer and output curves were performed in some devices with each different dielectric thickness, 1.45, 1.14 and 0.96 μm, and their transfer curves in saturation mode are presented in Figure 4.11 (a), (b) and (c), respectively, being already noticed the I_{on}/I_{off} of more than 4 orders of magnitude with low gate leakage (10^{-11} A) and a small device-to-device variation within the same substrate. See in Appendix I one output characteristic for each thickness.

The comparison between devices produced with these three different thicknesses is presented in Figure 4.11 (d). Using 1.45 μm of dielectric layer, the I_{on}/I_{off} is visibly lower and the V_{on} more negative than the others. The best case is using the smallest dielectric thickness, 0.96 μm, in which the V_{on} is small, reaching higher I_{on}/I_{off}. These results are in agreement with the I_{DS} formula (Eq. 2.3), since the decrease of the dielectric thickness results in an increase in the capacitance and, as such, in an increase of the source-drain current. Furthermore, a larger gate capacitance enables a closer-to-0 V V_{on} (i.e., less negative), given that the background electrons present in the semiconductor when V_{GS} = 0 V can be more effectively depleted by capacitive effect. In addition, it could be related to the number of defects, which is lower in a smaller volume, i.e., using a finer dielectric thickness.

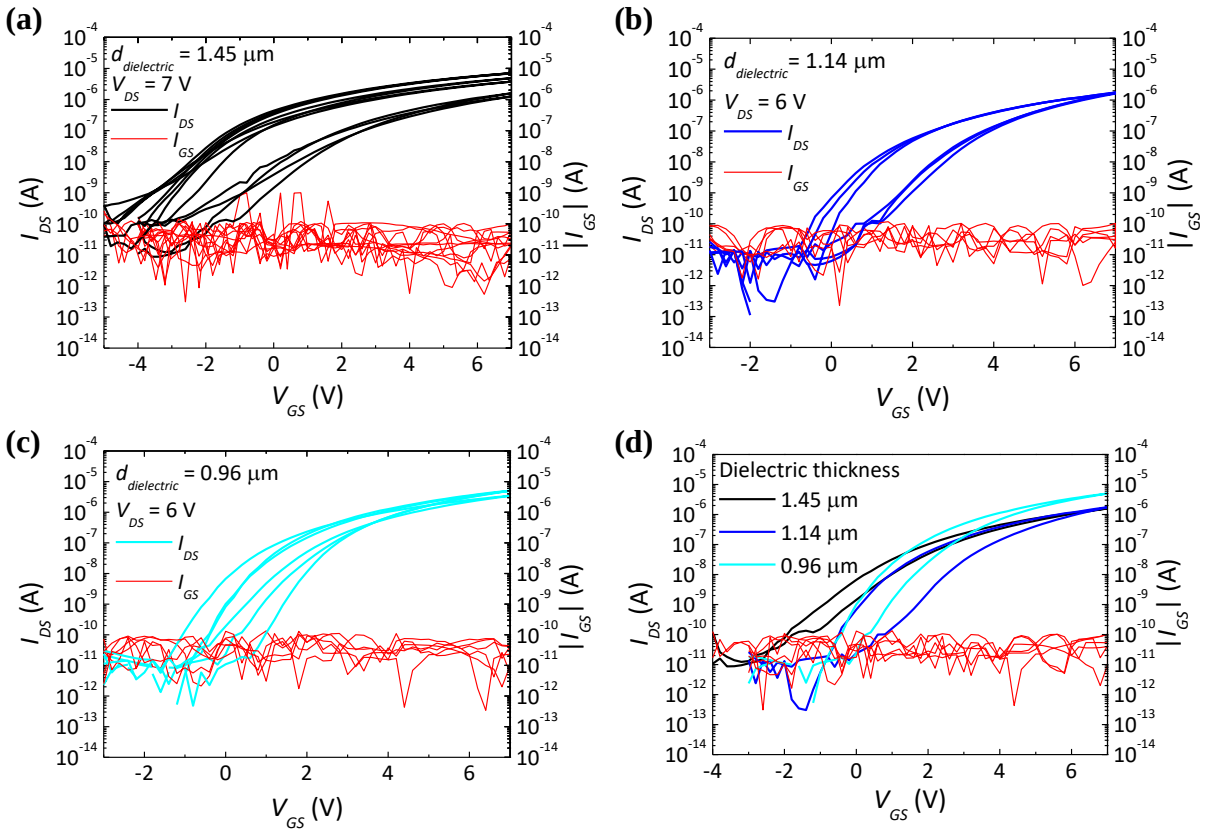

Figure 4.11. Transfer curves, in saturation regime, of long-gate planar TFTs with different dielectric thicknesses, (a) 1.45 µm; (b) 1.14 µm; (c) 0.96 µm; (d) comparison between the three thicknesses.

Table 4.11 contains the TFT parameters extracted from the devices studied with the different parylene thickness. The hysteresis value was obtained at a current value of 10^{-9} A, being always clockwise, consistent with charge trapping close to the dielectric-semiconductor interface [51].

Considering the dielectric constant obtained in planar structures, 3.1, the μ_{sat} was also extracted (consult Appendix I.4). The highest mobility was achieved with 0.96 µm of insulating layer, since a thinner layer results in a larger capacitance, and therefore in a higher number of charge carriers induced in the channel by each V_{GS} step. Moreover, upon application of the same V_{GS}, the vertical electric field increases with a lower dielectric thickness, resulting in the injection of more electrons from the source electrode [52]. This can explain also the V_{on} close to 0 V and the low S, allowing for a low operating voltage and low power consumption. Note that the increased mobility with smaller dielectric thickness is enabled by the peculiar transport mechanism of amorphous multicomponent oxide semiconductors, for which the mobility increases with carrier concentration (N) up to $\approx 10^{20}$ m^{-3} [53].

Table 4.11. Summary of long gate planar TFT parameters extracted from six devices of each dielectric thickness.

$d_{dielectric}$ (µm)	1.45	1.14	0.96
I_{on}/I_{off}	(9.84 ± 9.90) ×10^{4}	(1.37±1.97) ×10^{6}	(2.63±3.20) ×10^{6}
$I_{GS,\,max}$ (V)	(2.57 ± 3.21) ×10^{-10}	(8.58 ± 0.69) ×10^{-11}	(1.30 ± 0.26) ×10^{-10}
V_{on} (V)	-4.00 ± 0.70	-0.63 ± 1.02	-0.90 ± 0.57
Hysteresis (V)	0.37 ± 0.31	1.20 ± 0.55	1.23 ± 0.67
V_T (V)	2.21 ± 0.79	3.48 ± 1.24	4.16 ± 0.86
μ_{sat} (cm^2/V.s)	7.19 ± 2.66	7.74 ± 2.34	10.14 ± 3.88
S (V/dec)	0.82 ± 0.20	0.37 ± 0.07	0.36 ± 0.08

4.2.2.2. Fibre structures

Transistors in wires were also fabricated with the same thicknesses of insulating layer as in section 4.2, covered with sputtered IGZO using the fibre-rotation system and, since the aluminium deposition showed shadow effect being impossible to deposit source and drain electrodes with a small channel length, another setup was tried for the top contacts. Copper tape, conductive in both sides, with a length of 2 mm and spaced by 1 mm, was glued to the glass, in which the wire was placed over, and silver glue was used to connect with the wire, as seen in Figure 4.12.

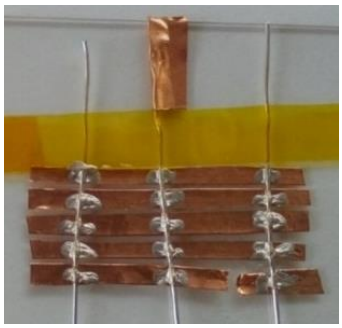

Figure 4.12. Setup for fibre-FETs, consisted of an Ag wire, parylene as the insulator, IGZO as the semiconductor and cooper tape and silver glue as the source and drain electrodes, respectively.

Related to the channel dimensions, since it is a coaxial structure and the semiconductor is deposited over all the wire perimeter, the length is given by the distance between the source/drain electrodes, and the width by the perimeter of the wire covered by the insulating layer, as shown in Appendix J. Considering the wire diameter of 500 µm and the channel length of 1 mm, the *W/L* was about 1.5, which in itself is a limitation for the operation of the device.

About the electrical characterization, the results reveal that no I_{DS} modulation with V_{GS} occur for any thicknesses, presenting a behaviour shown in Figure 4.13. The leakage current (I_{GS}) is always higher than the I_{DS}, indicating that the preferred current flows is between source and gate rather than source and drain, i.e., the resistance of the source-gate path is smaller than the one between source-drain. After analysis of several devices leading to the same behaviour, two possible reasons can be given for this result: either the drain and/or source contacts were not effective (i.e., no electrical contact between electrodes and IGZO) or the IGZO layer was very thin owing to the use of fibre-rotation system. Solutions for these issues were implemented in Gen3.

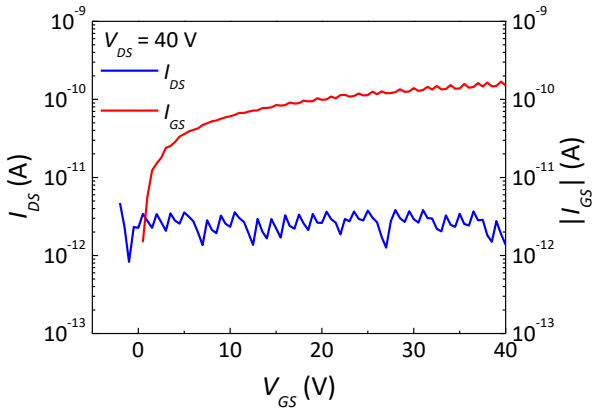

Figure 4.13. I_{DS} and I_{GS} measured as a function of V_{GS} of a fibre-FET, with 1.14 µm of parylene thickness and IGZO as semiconductor layer deposited using a fibre-rotation system.

4.3. Generation 3 (Gen3)

During this generation, the top contacts were made with silver ink by screen-printing. Compared with sputtering, this technique gives an economic solution for high conductive thickness layers.

The silver ink was analysed in SEM and no component was detected in Energy Dispersive Spectroscopy (EDS) besides silver, oxygen and carbon (Appendix K.1). The sheet resistance (R_s) of a film of the commercial silver ink, annealed at 150 ºC during 5 min, was obtained by four-point probe technique (Jandel Engineering Ltd). Applying a voltage between 1 to 10 mV, with a step of 1 mV, the *I-V* curve was obtained, being verified a linear behaviour (see Appendix K.2). The R_s was calculated, which corresponds to 0.04 Ω/square/mil*, and by knowing the thickness of the film (measured with profilometer Ambios), the resistivity was determined (Table 4.12). The reported surface resistivity of the ink is of about 0.2 Ω/square/mil [54], so the lower measured value is related to the solvent evaporation from the container over the years, which caused the ink to become more concentrated and, as such, more conductive.

Table 4.12. Silver ink characterization: the film thickness measured in a profilometer, the sheet resistance obtained from a four-point probe and the respective resistivity.

d_{ink} (μm)	R_s (Ω/□)	ρ (mΩ.cm)
4.92 ± 0.39	0.21 ± 0.01	0.10

4.3.1. Characterization of fibre-MIM capacitors

MIM capacitors were also produced using the same parylene thicknesses as in Gen2 and, because the thinner wires may have advantages for printing contacts in, both Ag wires (500 and 200 μm diameter) were used as core.

For the top contacts, conductive lines were patterned on glass, the wire was placed and fixed over the glass with kapton tape and, without moving the substrate, a new printing was made to deposit ink on top of the wire (Figure 4.14). In this process, the ink was just dried at the final of this process since the viscosity and conformability of the ink itself help to cover all of the perimeter, adapting to the wire's shape and ensuring a good contact.

Figure 4.14. MIM capacitors on Ag wires, with parylene as the dielectric, and top electrodes of silver ink deposited through the screen-printing technique.

Similar to Gen2, the characterization was made by applying the probes, one in the copper tape and the other over a conductive ink line.

Table 4.13 and Table 4.14 summarize the parameters obtained through capacitance characterization (*C-V* and *C-f*) and *I-V* curves, using Ag wires with 200 and 500 μm diameters, respectively, and considering the length contact of 2046 ± 52 μm. In both cases, with a thin thickness of the dielectric layer, less than 1 μm, the capacitor results show that the insulating layer was not working properly, presenting high leakage current and dielectric constant values very distant from the planar results. Looking to dielectric constant, using wires with 200 μm of diameter as core electrodes, the values

* R (Ω/square/mil) = R_s (Ω/□) × d (mil), 1 mil = 0.00254 cm

obtained were very close to the parylene dielectric constant. These MIM capacitors presented reliable results, even with very wide contact area (0.01 cm^2), which is defined by the contact length (2046.48 μm) and the perimeter of the conductive wire with an insulating layer deposited (618.38 μm).

Table 4.13. Parameters obtained through capacitance and current measurements of fibre-MIM capacitors, using Ag conductive core with 200 μm of diameter. The data for certain devices is not available due to high leakage current.

$d_{dielectric}$ (μm)	C/A (F/cm^2)	ε	J @ 2 V (A/cm^2)	R (Ω)	ρ (Ω.m)
1.45	1.00×10^{-9}	1.64	4.00×10^{-9}	6.88×10^{10}	6.03×10^{10}
1.14	2.42×10^{-9}	3.11	7.56×10^{-9}	3.21×10^{10}	3.57×10^{10}
0.96	2.99×10^{-9}	3.24	1.04×10^{-9}	2.56×10^{11}	3.37×10^{11}
0.46	N/A	N/A	N/A	N/A	N/A
0.24	N/A	N/A	N/A	N/A	N/A

Related to the wires with 500 μm of diameter, the determined values of the dielectric constant were much lower. To calculate the dielectric constant, all the perimeter was considered in the capacitor's area (0.03 cm^2), however, since the core is a thicker wire, during the screen-printing process, the silver ink may not completely cover the wire's perimeter, resulting in a smaller contact area.

Table 4.14. Parameters obtained through capacitance and current measurements of fibre-MIM capacitors, using an Ag conductive core with 500 μm of diameter.

$d_{dielectric}$ (μm)	C/A (F/cm^2)	ε	J @ 2 V (A/cm^2)	R (Ω)	ρ (Ω.m)
1.45	5.76×10^{-10}	0.94	1.62×10^{-9}	4.39×10^{10}	9.77×10^{10}
1.14	1.19×10^{-9}	1.53	4.89×10^{-9}	1.69×10^{10}	4.76×10^{10}
0.96	4.23×10^{-10}	0.46	4.53×10^{-9}	1.80×10^{10}	6.04×10^{10}
0.46	1.85×10^{-10}	0.10	6.38×10^{-9}	1.04×10^{10}	7.20×10^{10}
0.24	3.72×10^{-11}	0.01	1.48×10^{-8}	4.39×10^{9}	5.78×10^{10}

Regarding the Ag wire with 200 μm of diameter and 1.45 μm of insulating layer, the capacitance and the loss tangent were also analysed with a lock-in amplifier (Figure 4.15 (a) and (b), respectively) and, comparing with Keysight measurements, both graphs are coherent at 1 kHz. Relating to the capacitance and loss tangent measured with lock-in, a considerable increase was detected at low frequencies (below 1 Hz). Moreover, during the measurements at this frequency range, the loss tangent did not present stable or reproducible values, suggesting a change in the dielectric layer's properties, which can be related with spatial charges or a conductivity increase, however, a more detailed study is required.

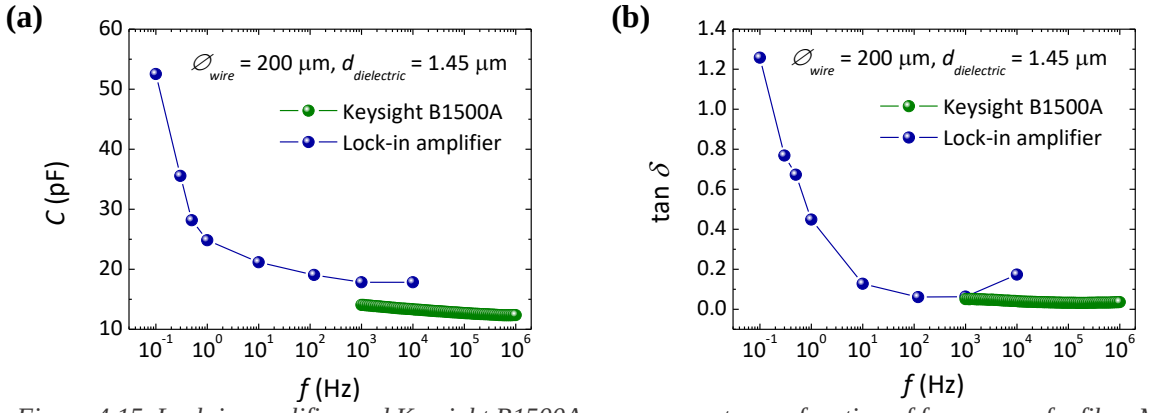

Figure 4.15. Lock-in amplifier and Keysight B1500A measurements as a function of frequency of a fibre-MIM capacitor, (a) in capacitance; (b) in loss tangent.

DC voltage measurements were also performed in fibre-MIM capacitors up to 200 V, and an apparent dielectric breakdown was detected at lower voltages for thinner thicknesses. As discussed in section 4.2.1.1, parylene is reported to withstand an electric field higher than 7 MV/cm, and since it was possible to make measurements in the same contacts of structures suffering this apparent dielectric breakdown, it was found that this was not a dielectric breakdown but rather a local heating of the ink due to the high voltage applied.

Table 4.15. DC breakdown voltage of fibre-MIM capacitors, using different dielectric thicknesses. The data for certain devices is not available due to high leakage current.

$Ø_{wire}$	200 μm		500 μm	
$d_{dielectric}$ (μm)	$V_{breakdown}$ (V)	E (MV/cm)	$V_{breakdown}$ (V)	E (MV/cm)
1.45	> 200	> 1.38	> 200	> 1.38
1.14	152	1.33	> 200	> 1.76
0.96	87	0.91	159	1.66
0.46	N/A	N/A	71	1.53
0.24	N/A	N/A	N/A	N/A

4.3.2. Characterization of fibre-FETs

Using the screen-printing technique to print the source and drain contacts, transistors were fabricated over wires with 200 and 500 μm of diameter. Based on the results obtained in wire MIM capacitors, only the thickness of the parylene layer, which guarantees better properties (1.14 μm), was used for the fabrication of wire FETs. Since the ink printed thickness is at the μm scale, the source and drain could be contacted by W probe tips directly on top of wire without risk of reaching the insulating layer.

During this section, the choice of semiconductor to apply in transistors had to undergo a change due to problems in AJA ATC-1300-F system. As such, the sputtered IGZO was replaced in the middle of this study by sputtered ZTO, so as not to delay the fibre-transistors study.

4.3.2.1. Fibre-transistors with IGZO as semiconductor layer

The first fibre-transistors fabricated in this generation used the same pattern and ink of fibre-MIM capacitors in section 4.3.1 to produce source and drain contacts. In this lot, the semiconductor layer was deposited during 18 min using fibre-rotation system and annealed at 150 °C during 1h.

The *W/L* of these transistors is given by the perimeter of the wire covered with the insulating layer (*W* of 1570 μm considering the wire with 500 μm diameter and 1.14 μm of insulating layer) over the gap between conductive ink lines (*L* of 484 ± 13 μm) which gives a ratio of 3.25. In Figure 4.16 (a) and (b) are presented the transfer curve in saturation regime, using 20 V of V_{DS}, and the output curve of the best transistor obtained. Regarding the transfer curve, the I_{on}/I_{off} is just one order of magnitude (1.20×10^{1} A) and gate leakage current is also increasing with V_{GS}, but a clear I_{DS} modulation with V_{GS} is verified, as expected in a FET. The mobility, calculated using the dielectric constant obtained in planar structures (3.1), was 0.02 cm^2/Vs and the subthreshold slope, 4.62 V/dec. Such values result from the defects or disorder on the interfaces caused by roughness [55]. In addition, the mobility value is affected by the value of the capacitance in the wires, which, as seen in the previous section, is not as consistent

as in the planar structures.

About the output characteristics, the cross-over at low V_{DS} occurs due to the high gate leakage, higher or very close to the I_{DS} [4]. As the potential between source and drain increases, the channel resistance gets lower than the source-gate path's resistance, enabling proper transistor behaviour.

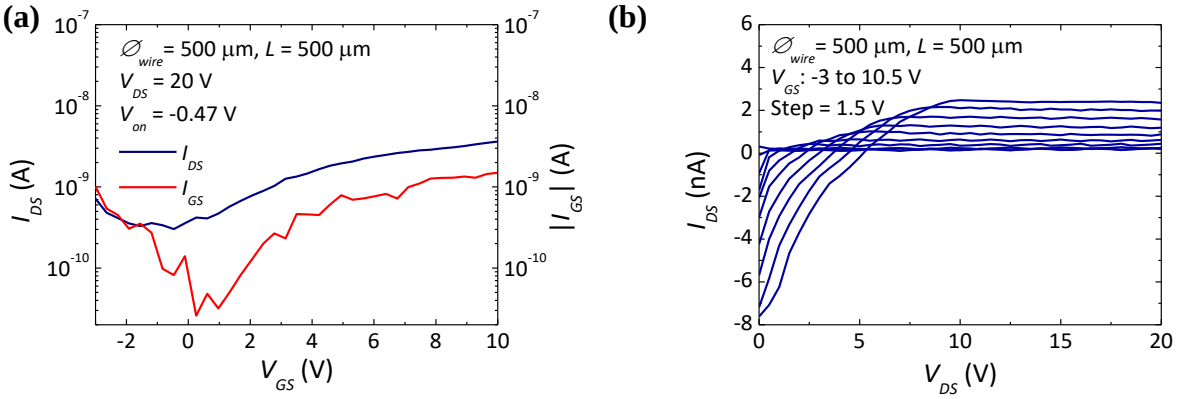

Figure 4.16. Characterization of a fibre-FET with 500 µm of Ag wire diameter, 1.14 µm of insulating thickness, IGZO as semiconductor, (a) transfer curve in saturation regime; (b) output curve.

One wire, with 1.14 µm of parylene thickness and IGZO layer deposited using the fibre-rotation system, was cut and analysed in SEM (see Figure 4.17). The semiconductor layer seems to be covering the insulating layer, however, not uniformly, due to the low IGZO thickness. Also, an EDS analysis was performed (Appendix L.1), but the IGZO constituents (In, Ga and Zn) were very hard to detect due to the very low thickness of this layer (< 10 nm). A cross-section was made in a fibre-transistor with FIB, not being possible to observe all the different constituent layers (Appendix L.2).

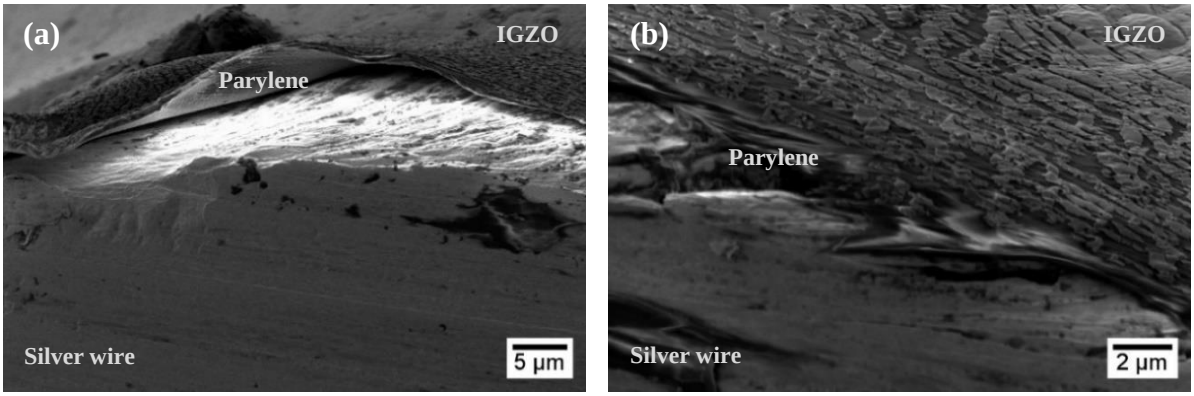

Figure 4.17. (a) and (b): SEM images of a cut wire covered with 1.14 µm of parylene thickness and an IGZO layer deposited using the fibre-rotation system, obtained with a secondary electron detector.

Since the use of the fibre-rotation system during the deposition gives a very thin and non-uniform layer (thickness < 10 nm, based on mathematical calculations), in the next devices, the semiconductor was sputtered in wires fixed on a glass substrate, being considered as channel width half of the wire's perimeter.

4.3.2.2. Fibre-transistors with ZTO as semiconductor layer

Transistors with 1.17 ± 0.04 µm of parylene thickness and 50 nm of ZTO were annealed at 150 °C during 1h. ZTO typically requires a higher annealing temperature than IGZO, however the proprieties of the silver ink would be altered and could cause the diffusion of its constituents to the semiconductor

layer. The surface morphology of the ZTO layer was also analysed in SEM (Figure 4.18 and Appendix M) and, like IGZO, the semiconductor layer presented the same non-uniformity.

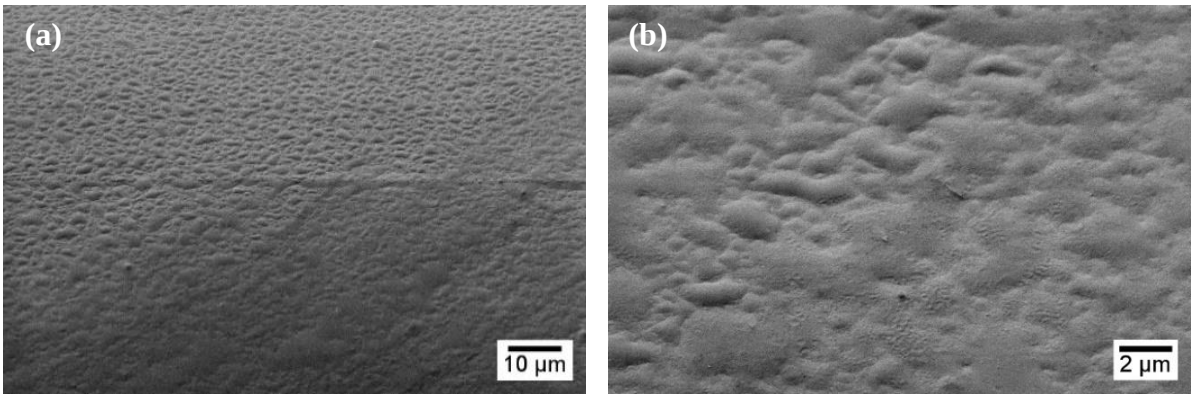

Figure 4.18. (a) and (b) SEM surface image of a ZTO layer deposited on an insulated wire, with a secondary electron detector.

Another mesh that already existed in the laboratory, with channel variations between 100 to 500 µm was used to define the source and drain contacts (see Figure 4.19 (a)), to increase the I_{DS} by increasing the *W/L*. Each set of different spacings consists of three lines, which means that in each set there are two pairs of source and drain contacts, in other words, two transistors.

Analysing the quality of the deposited contacts in the optical microscope, the minimum channel that could be defined was 200 µm, due to the silver ink spreading during the process. In Appendix N are presented the dimensions measured with ImageJ, reaching 50 µm of standard deviation. Moreover, using as core device the wires with 500 µm of diameter, in SEM (Figure 4.19 (b)) it was visible that the ink is not covering the whole perimeter, which results in a lower *W*. Since, in this case, the length of the contacts is considerably small, in the thicker wires the amount of ink that passes through the mesh is not enough to involve the wire's perimeter. The wire diameter must be large to ensure the largest possible perimeter (meaning a greater *W* of the channel) while ensuring that the ink is able to wrap it.

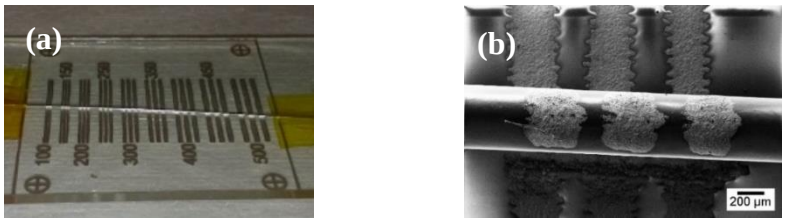

Figure 4.19. Screen-printed silver ink on a wire to define the source and drain contacts in an Ag wire with 500 µm of diameter, (a) photograph of the contacts; (b) SEM image obtained with a secondary electron detector.

In Figure 4.20 (a) and (b) are presented the transfer curve in saturation mode, V_{DS} of 50 V, and the output of a fibre-transistor with a channel length of 500 µm, using as core an Ag wire with 200 µm of diameter (*W/L* of 0.66). Besides being strongly affected on the high leakage current, the transistors' performance is also influenced by the quality of the silver ink-semiconductor interface, which has an impact on the energy barrier for electron injection that exists at the junction. A high energy barrier translates into a resistive component in series with the channel that decreases the effective voltage across the channel [16]. Comparing with the fibre-transistor with IGZO as semiconductor, despite higher operating voltage, the leakage was considerably lower, allowing for a defined channel modulation. Still,

in the output curve, at low voltages is evident the current crowding due to gate leakage current.

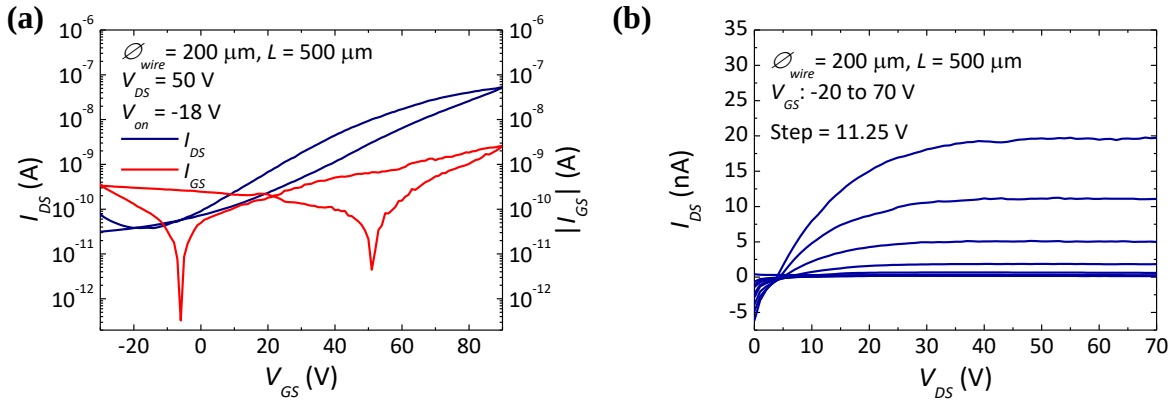

Figure 4.20. Characterization of a fibre-FET with 200 µm of Ag wire diameter, 1.17 µm of insulating thickness, ZTO as semiconductor and channel length of 500 µm, (a) transfer curve in saturation regime; (b) output curve.

In Table 4.16 and Table 4.17 are presented the results of the fibre-transistors with ZTO, using Ag wires with 200 and 500 µm of diameter, respectively, in the same order of magnitude to the results obtained in [4, 15, 41]. Comparing the results of the different wires with a channel length of 500 µm, a lower leakage current was observed with the thinner wires, however high hysteresis. The V_T and V_{on}, in both cases, presented high values, which is related to the low values of mobility and subthreshold slope.

Through the output curves, the I_{DS} value was obtained for constants V_{GS} and V_{DS} values, to compare to the different channel length, however no tendency was found (see Appendix O). As discussed in section 4.3.1, the ink spread over the wire perimeter is not occurring properly in thicker wires. Due to the process variability, the results obtained do not allow to draw great conclusions.

Table 4.16. Summary of fibre-FET parameters, using an Ag wire with 200 µm diameter, 1.17 µm of insulating thickness and ZTO as semiconductor.

L (µm)	500	350	300
W/L	0.66	0.85	1.03
I_{on}/I_{off}	1.37×10^{3}	1.28×10^{2}	9.41×10^{1}
V_{on} (V)	-18.00	-21.00	-22.00
$I_{GS,\ max}$ (A)	2.59×10^{-9}	3.38×10^{-8}	1.07×10^{-8}
Hysteresis (V)	15.00	20.00	24.00
μ_{sat} (cm²/V.s)	0.09	0.02	0.06
S (V/dec)	20.24	19.19	27.46
V_T (V)	46.25	25.49	22.04

Table 4.17. Summary of fibre-FET parameters, using an Ag wire of 500 µm diameter, 1.17 µm of insulating thickness and ZTO as semiconductor.

L (µm)	500	350	300
W/L	1.68	2.16	2.63
I_{on}/I_{off}	6.64×10^{2}	3.29×10^{2}	3.27×10^{2}
V_{on} (V)	-20.00	-24.00	-27.00
$I_{GS,\ max}$ (A)	2.43×10^{-8}	1.22×10^{-8}	1.66×10^{-8}
Hysteresis (V)	14.00	14.00	16.00
μ_{sat} (cm²/V.s)	0.10	0.11	0.07
S (V/dec)	19.57	8.80	19.40
V_T (V)	33.00	16.86	24.41

4.3.2.2.1. Aging effect on fibre-transistors

The fibre-transistors were measured again 2 months after production. In Figure 4.21 are presented the characteristic curves of a fibre-FET with 500 µm of Ag wire diameter and channel length of 300 µm. Given the very low temperature used to anneal the ZTO layer (150 °C), it is suggested that over time the desorption of weakly bonded oxygen atoms can be preponderant, increasing the free carriers within the oxide semiconductor [56]. That instability, along with the low dielectric capacitance, is responsible for the observable shift of the transfer curve, noticed in the current increase and in the more negative V_{on}.

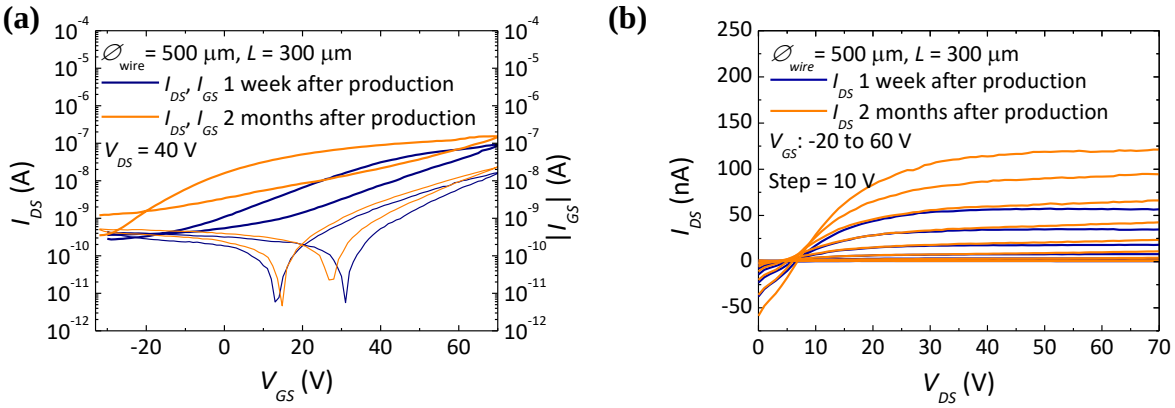

Figure 4.21. Comparison of a fibre-FET's measurements 1 week after production and 2 months after production, (a) transfer curve in saturation regime; (b) output curve.

In Table 4.18 and Table 4.19 are presented the results of the fibre-transistors measured 2 months after production, using Ag wires with 200 and 500 µm of diameter, respectively. By comparison with the previous results (Table 4.16 and Table 4.17), the I_{on}/I_{off} was maintained, the leakage current increased as well as the subthreshold slope, and the V_{on} became more negative, also related with the low capacitance and the unstable ZTO layer. About the saturation mobility, no variation trend was detected.

Table 4.18. Summary of fibre-FET parameters, using an Ag wire with 200 µm diameter, 1.17 µm of insulating thickness and ZTO as semiconductor, measured 2 months after production.

L (µm)	500	350	300
W/L	0.66	0.85	1.03
I_{on}/I_{off}	5.22×10^{2}	2.50×10^{2}	1.58×10^{1}
V_{on} (V)	-32.5.00	-19.00	-35.00
$I_{GS,\,max}$ (A)	1.22×10^{-8}	3.35×10^{-8}	4.31×10^{-8}
μ_{sat} (cm^2/V.s)	0.07	0.03	0.06
S (V/dec)	24.47	20.55	28.83
V_T (V)	36.86	33.89	8.76

Table 4.19. Summary of fibre-FET parameters, using an Ag wire of 500 µm diameter, 1.17 µm of insulating thickness and ZTO as semiconductor, measured 2 months after production.

L (µm)	500	350	300
W/L	1.68	2.16	2.63
I_{on}/I_{off}	1.68×10^{1}	1.28×10^{2}	4.38×10^{2}
V_{on} (V)	-36.7	-28.00	-30.80
$I_{GS,\,max}$ (A)	9.79×10^{-8}	5.38×10^{-8}	2.36×10^{-8}
μ_{sat} (cm^2/V.s)	0.06	0.12	0.09
S (V/dec)	30.49	19.20	13.52
V_T (V)	16.73	11.15	-6.71

4.3.2.2.2. Bending effect on fibre-transistors

To understand the effect of the bending in transistors, devices were characterized before and during the bending in a half-round cylinder, with a radius of 45 mm (9 cm of diameter), as showed in Figure 4.22.

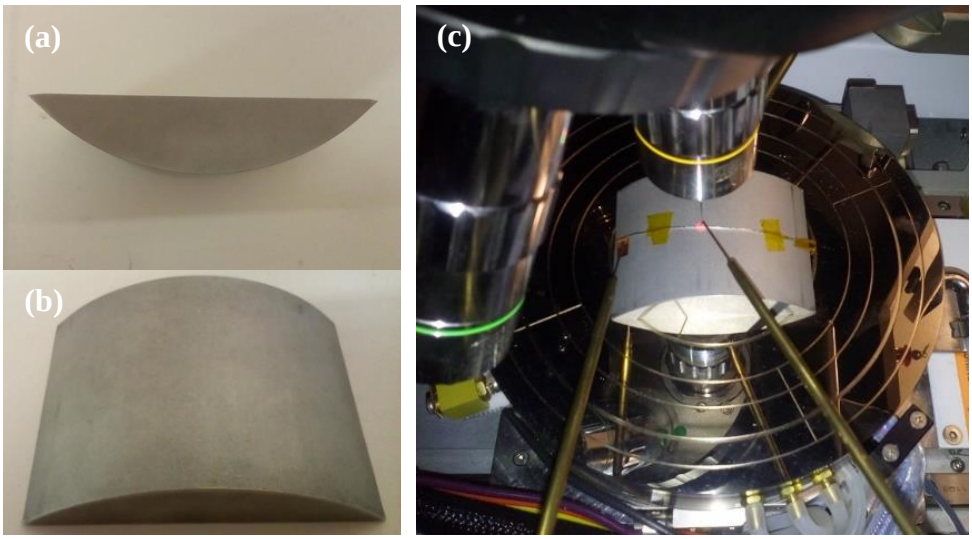

Figure 4.22. (a) and (b) half-round cylinder, with a 45 mm radius (9 cm of diameter) used to apply a constant tensile strain during the electrical measurement; (c) bending test performed in fibre-transistor.

This test was made in transistors in both Ag wires (500 and 200 µm of diameter), with a parylene thickness of 1.25 ± 0.02 µm, 50 nm of ZTO, annealed at 150 °C during 1h, and silver ink contacts printed just over the wire (one side printing).

In Figure 4.23 (a) and (b) are shown the transfer curve in saturation mode, V_{DS} of 50 V, and the output curve of a fibre-transistor with a channel length of 350 µm, using as core Ag wire with 200 µm diameter (*W/L* of 0.85). Comparing both curves before and during the bending test, the results are very similar and no significant changes were detected in the current.

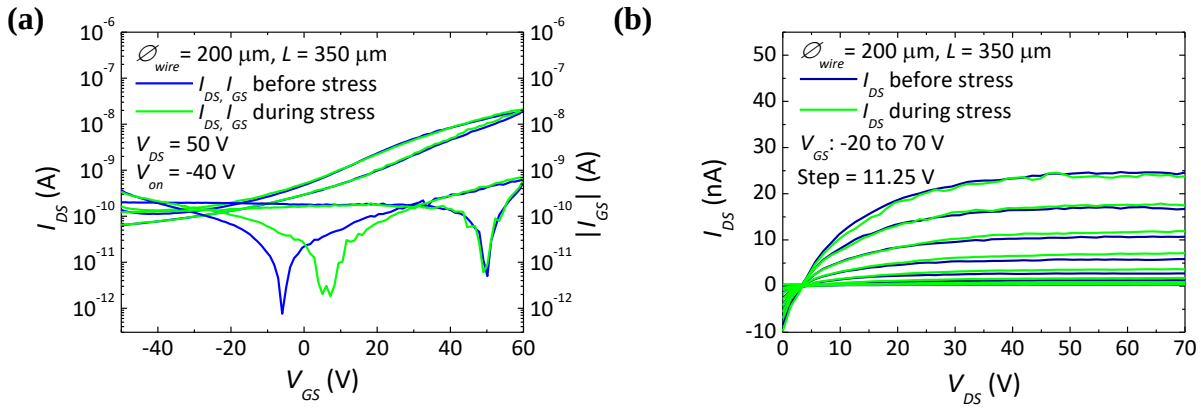

Figure 4.23. Characterization of fibre-FET before and during the bending, (a) transfer curve, in saturation regime; (b) output curve.

5. Conclusions

Hybrid transistors, composed by organic insulator and oxide semiconductor layers, were produced and optimized on conductive wires. To achieve that, several approaches were attempted during this work, involving the optimization of deposition processes and the measurement setups, resulting in three distinct structure generations.

Film deposition and device fabrication procedures over conductive wires, compared to conventional planar substrates, are more complex and difficult, not only due to the cylindrical shape of the devices, but also due to the handling of the samples themselves. For that reason, the measurement setup, to reliably access the electrical properties of fibre-based structures, was considered one of the most critical stages.

Regarding Gen2, in which aluminium contacts were evaporated, the use of a fibre-rotation system with a shadow mask caused a very low deposition rate and significant shadowing effects. The screen-printing technique applied in Gen3 proved to be a more reproducible method for both depositing and patterning the electrodes, besides the variability of 50 μm in contacts length, which still has to be solved.

The thinner wires (200 μm diameter) presented a better silver ink coating, which was reflected in the achieved electrical results. By analysing the parylene thickness required for a proper operation of MIM structures in wires, only capacitors in Gen3 with more than 1 μm presented good insulating properties, having a dielectric constant of 3.1, similar to the average value of the planar structures, and a low current density. The roughness of the silver wires limits the use of thin coatings, and so parylene layer thicknesses higher than 1 μm allows for a good planarization of the wire's surface. The performance of the transistors is also degraded by this roughness, making it difficult to perform at low operation voltage, a fundamental requirement to integrate these devices into wearable textiles.

During the first semiconductor depositions, a fibre-rotation system was used, which implied very thin and discontinuous sputtered IGZO films. When the use of that system was ceased, a channel modulation behaviour began to be obtained, although at the cost of half wire's perimeter and decrease of the *W/L*.

Despite their large operating voltage (V_{DS} = 50 V for saturation mode), attributed to the thick insulating layer, fibre-transistors with ZTO prepared below 150 °C exhibit mobilities over 10^{-2} $cm^2/V.s$, $I_{on}/I_{off} > 10^2$ and a maximum leakage current in the order of 10^{-8} A. Regarding the measurement of the devices 2 months after production, in addition to the V_{on} became more negative, an increase of the currents, even the leakage current, was detected, however I_{on}/I_{off} was essentially maintained. The results obtained during the bending with a radius of 45 mm revealed no device performance degradation.

One of the most limiting factors faced in fibre-transistors is the *W/L*, since the channel width is given by the wires' diameter. Furthermore, the interface between the silver ink and the semiconductor on wires, which is a key factor for obtaining a good transistor performance, was not ideal because of the wire's roughness.

5.1. Future perspectives

Since an initial development of fibre-transistors has been made, several actions can be implemented to enhance their performance, thus improving the current modulation. An increase in the *W/L* can be achieved by using thicker wires (which results in a higher *W*) and decreasing the channel length with accurate patterning of the source and drain contacts.

In order to increase the dielectric capacitance, a surface polishing in Ag wires can reduce the roughness, allowing for the deposition of thinner insulant layers. Furthermore, multilayer or high-κ dielectrics can be applied.

Patterning of the active layer can be implemented to reduce gate leakage by removing a large area of the gate leakage paths. Additionally, the patterning of the insulant layer can help with the bending. Isolated dielectric islands show more tolerance for flexion stress than large area films.

Alternatively, to improve the mechanical flexibility towards lower bending radius, solution-processing methods can also be attempted, since they offer a simple low-cost route to forming uniform films with full coverage over a cylindrical substrate, in contrast with vacuum processing methods. In parallel with this, hybrid materials comprising organic and oxide mixtures can be tested, both for dielectrics and semiconductors.

To improve stability, an encapsulation layer of parylene can be applied. In the case of wearable e-textiles, encapsulation may also be important for safety concerns. Furthermore, localized encapsulation could provide mechanical support, transferring flexion stress from areas with active devices to neighbouring areas.

Metallic substrate wires can simplify the device structure by providing electronic functionality themselves. After optimizing the devices performance, the Ag wires are intended to be replaced by functionalized polymeric fibres, as gate electrodes, to be applied in smart textiles.

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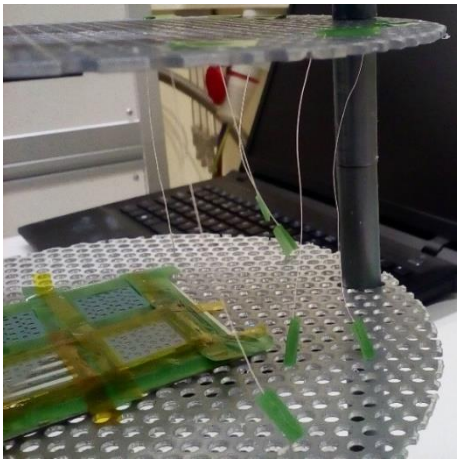
Appendixes

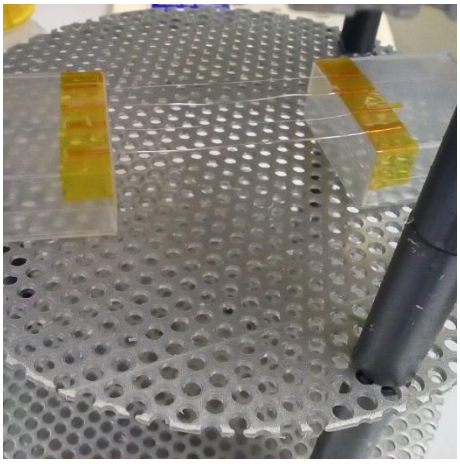
Appendix A

Disposition of wires during parylene chemical vapour deposition, 1. Gen1 wires vertically positioned; 2. Gen2 and Gen3 wires horizontally positioned.

1.



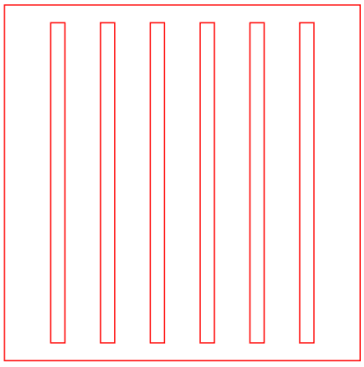
2.



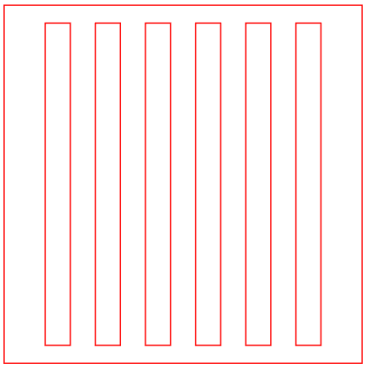
Appendix B

Masks designed in Adobe Illustrator, 1. with lines of 4 mm, separated by 10 mm, to pattern the electric contacts on wires; 2. with lines of 7 mm, separated by 7 mm, to pattern the conductive lines on a glass substrate.

1.



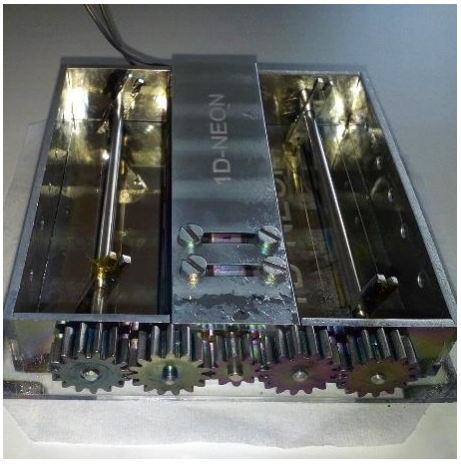
2.



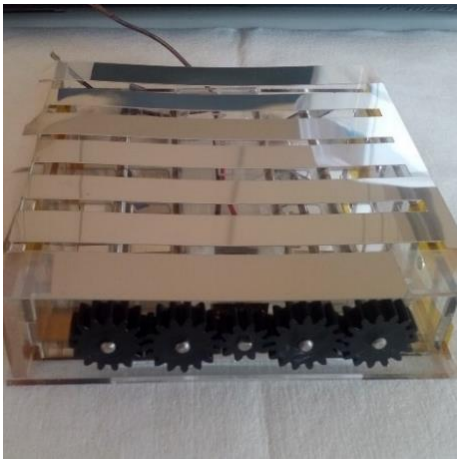
Appendix C

Fibre-rotation system used to promote the deposition of the conductive material along the wire perimeter, 1. Fixation of fibres on the system; 2. Fibre-rotation system with a PEN mask to pattern the conductive contacts on the wires; 3. patterned wires. The voltage and current applied in the motor supply control the rotation speed. During the aluminium and IGZO deposition 0.6 V and 0.6 A were used as electrical parameters.

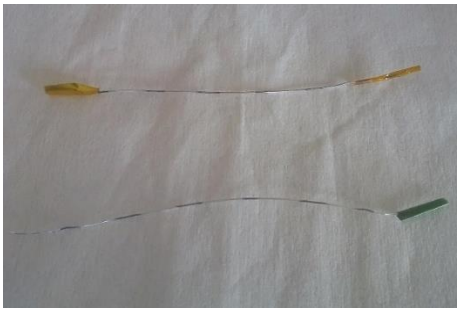
1.



2.



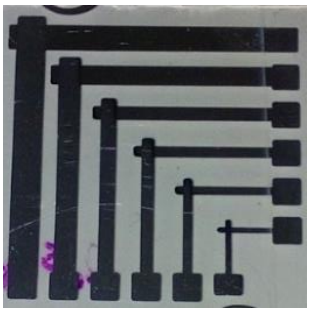
3.



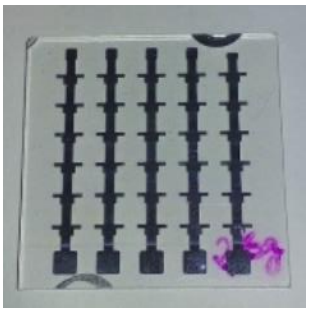
Appendix D

Planar structures fabricated, 1. planar MIM capacitors with 6 different areas, using aluminium as bottom and top electrodes, and parylene as the dielectric layer; 2. long gate planar TFTs with a *W/L* of 1000/100.

1.

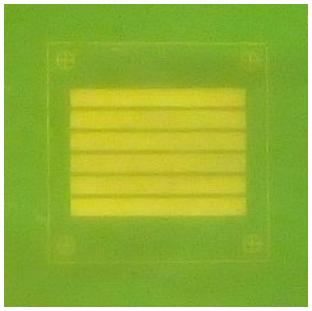


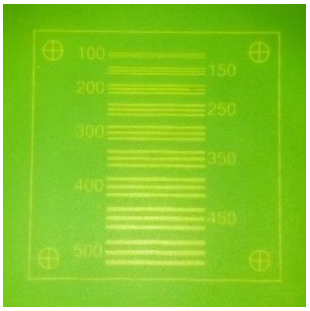
2.



Appendix E

Patterns of mesh model 120T used to print the top contacts on wires, 1. for capacitors; 2. for transistors.

1. 

2. 

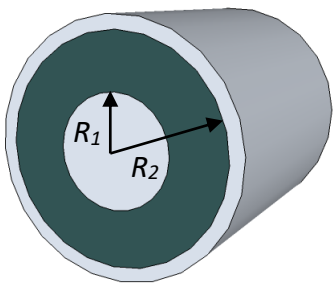
Appendix F

Wires' diameters measured in 5 different parts using a picometer.

Ag wire (500 µm diameter)		Ag wire (200 µm diameter)	
$Ø_{wire}$ (µm)	Average (µm)	$Ø_{wire}$ (µm)	Average (µm)
496		193	
495		194	
496	498 ± 3	195	195 ± 1
499		196	
502		195	

Appendix G

Schematic of a MIM capacitor in a fibre structure composed by a core electrode, an insulating layer around the core and a second electrode covering the insulator.



Appendix H

Characterization of planar MIM capacitors

1. Capacitance measured in different contact areas, for the 5 different dielectric thicknesses, at 100 kHz. The data for certain devices is not available due to high leakage current.

$d_{dielectric}$ (μm)	C (pF)					
	$A_{theoretical}$ (mm^2)					
	4.14	2.44	1.21	0.77	0.41	0.17
1.45	73.70	44.8	22.47	14.83	8.19	3.42
1.14	N/A	60.63	N/A	21.06	11.35	4.55
0.96	122.50	73.13	36.00	23.50	12.70	4.90
0.46	246.80	151.50	77.10	N/A	24.90	8.835
0.24	413.00	231.50	103.00	N/A	39.25	N/A

2. Capacitance per unit area, calculated for different contact areas, with 5 different dielectric thicknesses, at 100 kHz. The data for certain devices is not available due to high leakage current.

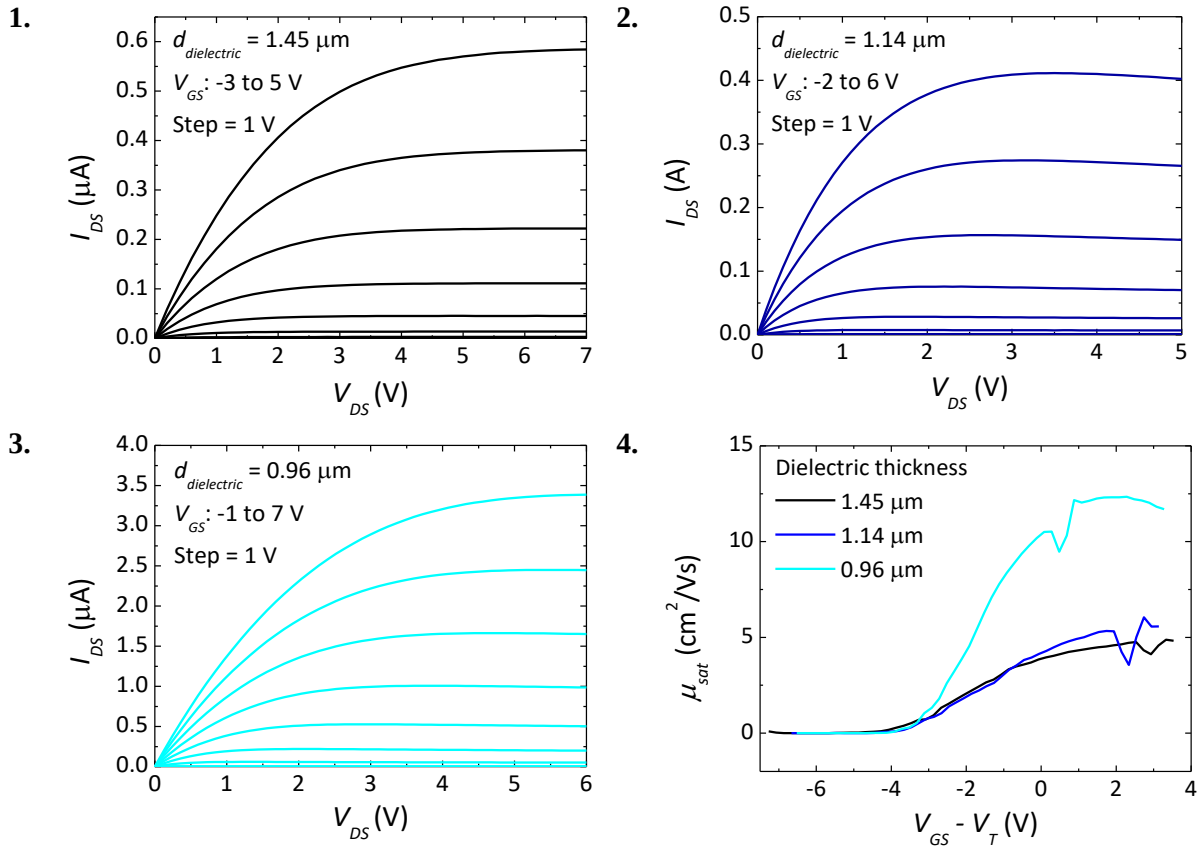
$d_{dielectric}$ (μm)	C/A (F/cm^2)					
	$A_{theoretical}$ (mm^2)					
	4.14	2.44	1.21	0.77	0.41	0.17
1.45	1.78×10^{-9}	1.83×10^{-9}	1.86×10^{-9}	1.93×10^{-9}	1.99×10^{-9}	2.04×10^{-9}
1.14	N/A	2.48×10^{-9}	N/A	2.74×10^{-9}	2.76×10^{-9}	2.71×10^{-9}
0.96	2.96×10^{-9}	3.00×10^{-9}	2.97×10^{-9}	3.06×10^{-9}	3.09×10^{-9}	2.92×10^{-9}
0.46	5.97×10^{-9}	6.21×10^{-9}	6.37×10^{-9}	N/A	6.05×10^{-9}	5.26×10^{-9}
0.24	9.98×10^{-9}	9.48×10^{-9}	8.51×10^{-9}	N/A	9.54×10^{-9}	N/A

3. Calculated electric field at 100 V for each parylene thickness.

$d_{dielectric}$ (μm)	E (MV/cm)
1.45	0.69
1.14	0.88
0.96	1.04
0.46	2.16
0.24	4.11

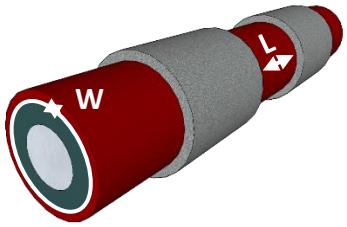
Appendix I

Output curves collected from a transistor with each dielectric thickness, 1. with 1.45 µm of parylene thickness; 2. with 1.14 µm of parylene thickness; 3. with 0.96 µm of parylene thickness; 4. comparison between saturation mobility of the three studied dielectric thicknesses.



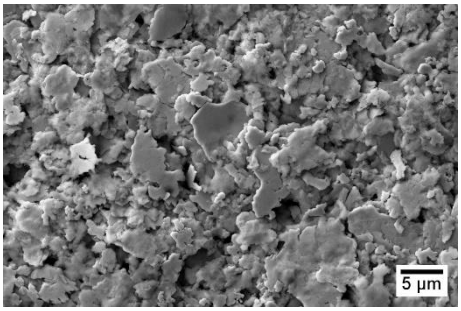
Appendix J

Schematic of the channel dimensions in fibre-transistors where the length (*L*) is given by the distance between the source/drain electrodes, and the width (*W*) is given by the perimeter of the fibre covered by the insulating layer.



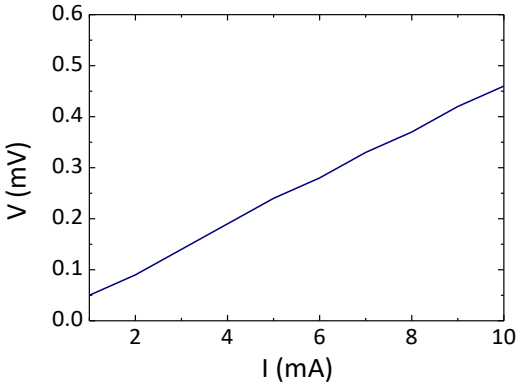
Appendix K

1. SEM-EDS analysis of the silver ink.



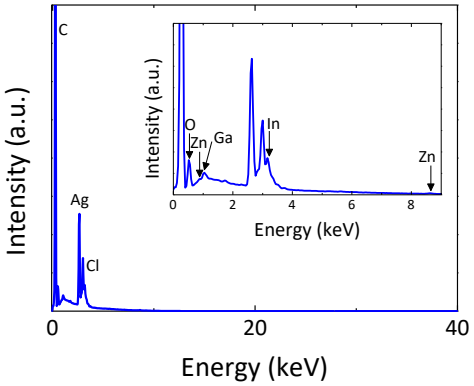
Element	Apparent Concentration	Wt %	Atomic %
C	2.93	3.69	23.25
O	1.07	2.28	10.80
Ag	93.28	94.03	65.95

2. *I-V* curve of the silver ink, annealed at 150 ºC during 5 min, using a four-point probe technique (Jandel Engineering Ltd).



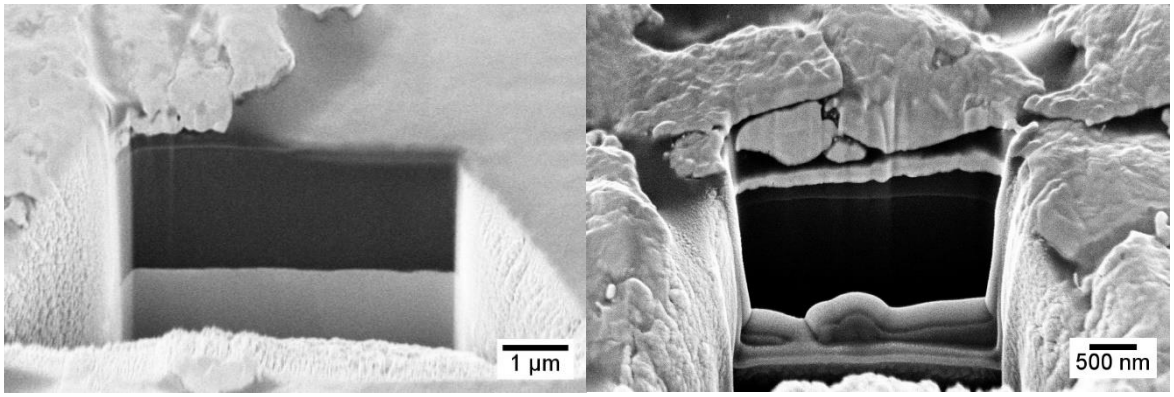
Appendix L

1. EDS analysis of the IGZO constituents (In, Ga and Zn) over the wire. The IGZO was very hard to detect, presenting a very low atomic percentage. C and Cl detection is associated to parylene C layer, and the Ag is from the wire itself.



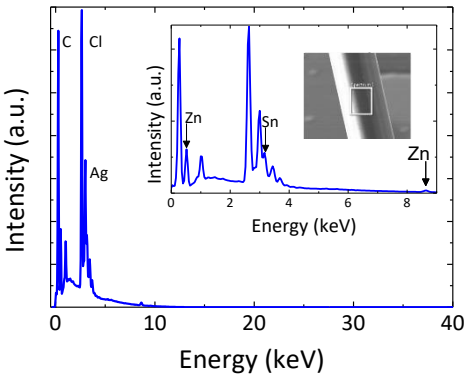
Element	Apparent Concentration	Wt %	Atomic %
C	44.23	47.56	78.97
O	12.81	9.18	11.44
Cl	5.74	4.05	2.28
Zn	0.29	0.38	0.12
Ga	0.25	0.29	0.08
Ag	39.74	37.42	6.92
In	1.30	1.13	0.20

2. Cross-sections, with 3 µm deep in a fibre-transistors, using FIB, presenting the silver ink at the surface, the parylene layer and the Ag wire.



Appendix M

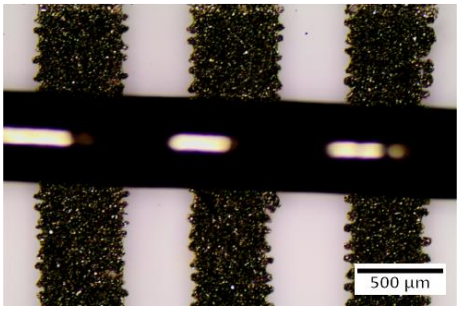
EDS analysis of the ZTO constituents (Zn and Sn) over the wire. In the spectrum, the peaks of the semiconductor constituents were visible.



Element	Apparent Concentration	Wt %	Atomic %
C	4.96	44.08	72.03
O	2.79	11.75	14.42
Cl	6.20	13.68	7.57
Zn	0.96	4.53	1.36
Ag	6.85	20.24	3.68
Sn	1.79	5.72	0.95

Appendix N

The contacts were analysed with an optical microscope and measured with ImageJ. The silver ink is not very uniform and the standard deviation is considerably high.



Mesh (µm)	Contact length (µm)	Channel length (µm)
500	520 ± 41	468 ± 34
450	450 ± 46	399 ± 51
400	405 ± 49	388 ± 31
350	348 ± 42	364 ± 43
300	292 ± 47	299 ± 35
250	259 ± 17	239 ± 25
200	233 ± 35	197 ± 46

Appendix O

The I_{DS} value, obtained in the output curves by applying a V_{GS} of 60 V and a V_{DS} of 50 V, as a function of the different channel length in both wires.