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NOVEL TECHNIQUES FOR THE DESIGN AND PRACTICAL REALIZATION OF SWITCHED-CAPACITOR CIRCUITS IN DEEP-SUBMICRON CMOS TECHNOLOGIES

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Sumário

Interruptores exibindo elevada linearidade são cada vez mais essenciais em circuitos de condensadores comutados, nomeadamente em conversores analógico-digital de resoluções entre os 12 e os 16 bits. A tecnologia CMOS evolui continuamente em direcção a tensões de alimentação cada vez mais reduzidas, e simultaneamente, novas técnicas de projecto são necessárias para possibilitarem a realização de interruptores que exibam uma elevada gama dinâmica e uma distorção compatível com as resoluções referidas. Para além disso, com a diminuição contínua das dimensões, as restrições físicas da tecnologia deverão ser tidas em linha de conta, de modo a evitar o stress excessivo dos dispositivos quando relativamente elevadas tensões são aplicadas às suas portas. Novas técnicas de linearização de interruptores com fiabilidade elevada terão necessariamente que ser investigadas e demonstradas em circuito integrado CMOS.

Também é constante a procura de novas estruturas de circuitos com condensadores comutados. São indispensáveis estruturas simplificadas e eficazes, adequadas às novas exigências decorrentes da proliferação do uso de equipamentos portáteis, necessariamente com baixo consumo de energia, mas assegurando alto desempenho de múltiplas funções.

O trabalho apresentado nesta dissertação engloba estas duas áreas. É analisado o comportamento dos interruptores face aos novos parâmetros condicionantes, sendo proposta uma solução adequada e inovadora para que mantenham a sua boa prestação. Também são apresentadas soluções para a aplicação de esquemas de relógio e controlo simplificados, assim como para uso de estruturas em malha aberta e de amplificadores com realimentação local. Os resultados, obtidos por medição laboratorial ou por simulação de vários projectos, permitem avaliar a viabilidade das propostas apresentadas.

Abstract

Switches presenting high linearity are more and more required in switched-capacitor circuits, namely in 12 to 16 bits resolution analog-to-digital converters. The CMOS technology evolves continuously towards lower supply voltages and, simultaneously, new design techniques are necessary to fulfill the realization of switches exhibiting a high dynamic range and a distortion compatible with referred resolutions. Moreover, with the continuously downing of the sizes, the physic constraints of the technology must be considered to avoid the excessive stress of the devices when relatively high voltages are applied to the gates. New switch-linearization techniques, with high reliability, must be necessarily developed and demonstrated in CMOS integrated circuits.

Also, the research of new structures of circuits with switched-capacitor is permanent. Simplified and efficient structures are mandatory, adequate to the new demands emerging from the proliferation of portable equipments, necessarily with low energy consumption while assuring high performance and multiple functions.

The work reported in this Thesis comprises these two areas. The behavior of the switches under these new constraints is analyzed, being a new and original solution proposed, in order to maintain the performance. Also, proposals for the application of simpler clock and control schemes are presented, and for the use of open-loop structures and amplifiers with local-feedback. The results, obtained in laboratory or by simulation, assess the feasibility of the presented proposals.

Symbols and Abbreviations

A	Amplifier open-loop gain
A_D	Drain area
A_{in}	Input voltage amplitude peak-to-peak
A_S	Source area
A_{VT}	Threshold voltage matching parameter
B	Stage effective resolution
b_0, b_1	Quantizer output codes
C	Capacitor
C_a	Charge pump capacitor
C_b	Bootstrap capacitor
C_{BC}	Bulk-channel capacitance
C_C	Compensation capacitor
C_F	Feedback capacitor
C_g	Gate capacitance
C_{GC}	Gate-channel capacitance
C_{GD}	Gate-drain capacitance
C_{GD0}	Gate-drain overlapped capacitance
C_{GG}	Gate-gate capacitance
C_{GS}	Gate-source capacitance
C_{GS0}	Gate-source overlapped capacitance
C_{ij}	Two-terminal, *i* and *j*, capacitance
C_{jBC}	Bulk-channel junction capacitance *per* unit area
C_{jDB}	Drain-bulk junction capacitance *per* unit area
C_{jSB}	Source-bulk junction capacitance *per* unit area
C_L	Load capacitance
clk	Master clock
C_{ox}	Oxide capacitance *per* unit area
C_P	Parasitic capacitor
c_r	Ratio of divided channel charge
C_S	Sampling capacitor
C_{SG}	Source-gate capacitance

$C_{S(MDAC)}$	MDAC sampling capacitor
$C_{S(S/H)}$	S/H sampling capacitor
C_u	Unity capacitance
D_i	Multiplier of reference voltage
EOT	Eqivalent oxide thickness
E_{ox}	Oxide field
f_{gate}	Gate corner frequency
f_{in}	Input frequency
F_S	Sampling frequency
F_ϕ	Clock frequency
g	Conductance
G	Gain
$G_C(T)$	$TDDB$ temperature dependent parameter
g_{DS}	Drain-source conductance
g_{EQ}	Equivalent conductance
g_m	Transconductance
g_{tunnel}	Tunnel conductance
h	Strong-to-weak inversion variation
i	Current
I	Current source
I_{DD}	Supply current
i_{DS}	Drain-source current
I_g	Gate leakage current
i_{GS}	Gate-source current
I_j	Gate induced drain leakage current
I_{max}	Maximum current
I_{off}	OFF-state leakage current
i_{out}	Output current
k	Boltzmann constant and scaling factor
K_1, K_2	Capacitor ratio factors
KP	Mobility factor
L	Channel length
L_D	Overlapped length
m	Ratio between mobility factors
n	NMOS or negative suffix

N	ADC resolution
n_S	Number of cascade stages
p	PMOS or positive suffix
P	Power
P_D	Power dissipation
P_U	Useful power
q	Unity charge
q0, q1, q2	Comparator outputs codes
Q_C	Channel or capacitor charge
Q_{CP}	Parasitic capacitance charge
Q_{CS}	Sampling capacitor charge
Q_i	Terminal *i* charge
Q_v	Charge *per* voltage
R_D	Degeneration resistor
R_{DS}	Drain-to-source resistance
R_F	Feedback resistor
R_L	Load resistor
r_o	Device output resistance
R_o	Amplifier output resistance
R_{out}	Stage output resistance
R_S	Voltage multiplier series resistance
SR	Slew-rate
s_T	Sub-threshold slope factor
t	Time
T	Temperature
TDDB	Time dependent dielectric breakdown
t_{ox}	Oxide thickness
t_{oxeff}	Effective oxide thickness
t_{SR}	Slew-rate time
V_B	Biasing voltages
v_{BS}	Bulk-to-source voltage
V_{CM}	Common mode voltage
V_{CMI}	Input common mode level
V_{CMO}	Output common mode level
V_{CMx}	Common mode control voltage

V_D	Diode voltage drop
V_{DD}	Positive supply voltage
v_{DS}	Drain-to-source voltage
V_{DSsat}	Drain-to-source saturation voltage
V_{En}	Early voltage *per* channel length
V_{HI}	Common mode level, high
v_G	Gate voltage
v_{GD}	Gate-to-drain voltage
v_{GS}	Gate-to-source voltage
v_{GSeff}	Effective gate-to-source voltage
v_{id}	Differential input voltage
v_{in}	Input voltage
V_j	Terminal *j* voltage
V_{LO}	Common mode level, low
v_{od}	Differential output voltage
V_{offset}	Offset voltage
v_{out}	Output voltage
$v_{outfinal}$	Steady output voltage
V_{REF}	Reference voltage
v_{sat}	Velocity saturation
v_{SB}	Source-to-bulk voltage
V_{SS}	Negative supply voltage
V_T	Threshold voltage
V_{TO}	Threshold voltage with zero biasing
v_x	Node *x* voltage
V_ϕ	Clock voltage
$V_{\phi max}$	Maximum clock voltage
$V_{\phi min}$	Minimum clock voltage
W	Channel width
X, Y, Z	Output signals from quantizer circuit
$xcap$	capacitors tolerance
X_{iGS}	gate leakage current mismatch proportionality constant
β	Feedback factor
γ	Body factor
$\gamma_B(T)$	*TDDB* temperature dependent parameter

ε	Voltage error
ε_{chi}	Voltage error, charge injection
ε_{clkf}	Voltage error, clock feed-through
ε_{tot}	Total voltage error
μ	Carrier mobility
η_c	Current Efficiency
η_v	Voltage Efficiency
ω_{-3dB}	Corner frequency
σ^2_{rms}	Total noise variance
σ_{VT}	Threshold voltage mismatch
τ	Time constant
$\tau_C(T)$	*TDDB* temperature dependent parameter
$\tau_B(T)$	*TDDB* temperature dependent parameter
$\Delta G_{gain}/G$	Relative gain error, finite gain
$\Delta G_\tau/G$	Relative gain error, time constant
ΔQ_C	Channel or capacitor charge variation
ΔQ_{CS}	Sampling capacitor charge variation
ΔQ_{CP}	Parasitic capacitance charge variation
Δt	Rise or fall period of time
ΔV	Voltage swing
Δv_{out}	Output voltage swing
ΔV_T	Threshold voltage variation
ΔV_ϕ	Clock voltage swing
ϕ	Clock phase
$\lvert\Phi_F\rvert$	Surface potential
10GBASE-T	10 gigabit Ethernet
1000BASE-T	Gigabit Ethernet
A/D	Analog-to-digital
ADC	Analog-to-digital Converter
ATG	Asymmetric Transmission Gate
BS	Bulk-switching
BW	Signal Bandwidth
CBT	Clock Bootstrapped circuit
CE	Constant Electric Field

CMFB	Common-mode Feedback
CMOS	Complementary Metal-oxide-semiconductor
CoB	Chip-on-board
CP	Charge Pump
CV	Constant Voltage
D/A	Digital-to-analog
DAC	Digital-to-analog Converter
D-FF	D Flip-Flop
DNL	Differential Nonlinearity
DR	Dynamic Range
DTMOS	Dynamic Threshold Voltage MOS Device
ENOB	Effective Number of Bits
FoM	Figure-of-Merit
FFT	Fast Fourier Transform
GBW	Gain-bandwidth Product
HS	High-speed
IC	Integrated Circuit
INL	Integral Nonlinearity
LSB	Least Significant Bit
MBTA	Multiply-by-two Amplifier
MDAC	Multiplying Digital-to-analog Converter
MiM	Metal-insulator-metal
MoM	Metal-oxide-metal
MOS	Metal-oxide-semiconductor
MOSCAP	MOS Capacitor
MSB	Most Significant Bit
NMOS	N-channel MOSFET
NAND	N-AND gate
OpAmp	Operational Amplifier
OR	OR gate
OTA	Operational Transconductance Amplifier
PMOS	P-channel MOSFET
PVT	Process-supply-temperature
SAR	Successive Approximation Register
SC	Switched-capacitor

SFDR	Spurious Free Dynamic Range
S/H	Sample-and-hold
SLC	Switch-linearization Circuit
SNR	Signal-to-noise Ratio
SNDR	Signal-to-noise-plus-distortion Ratio
SO	Switched-OpAmp
TG	Transmission Gate
THD	Total Harmonic Distortion
UWB	Ultra Wide Band

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1. Introduction

1.1. Motivation for the Thesis

The development of analog electronics during the last years has been majority pushed by the extensive proliferation of wireless communication and multimedia devices. The reduced power dissipation, while assuring the necessary high speed operation, is a mandatory goal in any electronic circuit design, more relevant when battery-powered. Moreover, also the size, weight, reliability, security and price are decisive in the devices design. Therefore, the technologies and the techniques have been pressed to answer to those challenges, with improved, efficient and secure solutions.

The complementary metal-oxide-semiconductor (CMOS) architecture has been the prevailing technology used in integrated circuits, for more than 30 years. The major reason for the success of the metal-oxide-semiconductor (MOS) transistor is the fact that it is technology possible to scale it to increasingly smaller dimensions, decreasing the transistor delay times and increasing the circuit performance. However, even though new integrated circuits technologies and techniques can offer high speed of operation, the power dissipated is frequently unable to fulfill the restrictions and demands imposed by the applications. Moreover, the continuous downsizing is putting in evidence, once again, some reliability questions thought as already answered till now.

The circuit adequate level of reliability is a major requirement for all users. The achievement of the required level has been a challenge to the designers, due to the fast changes in CMOS technology as scaling, and to the competition imposed, financial and time constrains. Scaling has allowed a higher number of transistors in a single integrated circuit, resulting in an increased number of the on-chip and in-package interconnections, and reducing the interconnect reliability. The scaling has potentially increased the current density, therefore has decreased the interconnections reliability. Moreover, the scaling has indirectly led to higher power dissipation density and to lower thermal conductivity, therefore to higher operating temperatures and thermal gradients, increasing the potential failures. Fast technology changes, as new materials or special devices, are difficultly followed by the desired reliability capabilities, which are often developed much slower.

The switched-capacitor (SC) has been the current design technique used in analog integrated circuits. SC circuits comprise capacitors, switches and amplifiers. Researchers and designers have been, and will be, developing these areas. The metal-oxide-metal (MoM) capacitors are getting more and more efficient in terms of capacitance *per* unit area. The metal-insulator-metal (MiM) capacitors can be avoided and, hence, pure cheaper logic processes can be used to design low-cost mixed-mode circuits. Moreover, matching is quite stable. The areas that can drive to design improvements with greater impact, while preserving the simplicity of the layout, are the switches and amplifiers.

The amount of charge destroyed in SC circuits, by having overlapping clocks, is getting smaller for the same switches sizing, due to the faster transition times of the CMOS gates. Therefore, the single-phase technique, addressed in this Thesis, can be applied to many SC circuits, simplifying the circuit layout.

The linearity performance of the switches in rail-to-rail operation is degrading since the threshold voltage is not scaling down proportionality to the power supply voltage reductions. Even so, the standby power and the active power ratio have been increasing. The reduced lowering of the threshold voltage decreases the gate overdrive, and therefore, the switches performance. Attempts to overdrive the gate voltage are limited by the stress over the gate and by reliability constraints. The oxide thickness has been scaled approximately proportional with the length, maintaining the ability of gate control through the scaling levels. More, as the scaling of the voltages is not as fast as the scaling of the dimensions, the applied electric field has increased and the time dependent dielectric breakdown has decreased. Even maintaining the electric field value, as the dielectric breakdown becomes a function of the voltage *per si*, the reliability issue is of the major importance when voltage overdrive techniques are used. Alternatively, a novel switch-linearization solution is proposed in this Thesis and demonstrated in silicon in a 10-bit analog-to-digital converter (ADC).

The open-loop gain of amplifiers over process-supply-temperature (PVT) corners, specially at high temperatures is subject to huge degradations. Increasing the number of amplifying stages can overcome the amplifier dropping gain issue, but the energy efficiency of the design is reduced. Complex and costly calibration techniques can also be used to calibrate and maintain the amplifier gain. The use of pure open-loop amplification structures is simple, but requires either post-calibration or servo-loop correction structures. However, robust open-loop amplification structures can be achieved by combining them with closed-loop amplifiers, in

order to avoid the need of any kind of calibration. This approach is proposed in this Thesis for the first time, and demonstrated through electrical simulations of a 6-bit 1GS/s ADC.

Table 1.1 summarizes the major Pros and Cons of designing SC circuits in sub-micron technologies. Notice that the Pros/Cons referred with an (*) are addressed and explored throughout in this Thesis, by proposing new and efficient solutions to deal with.

Table 1.1: Pros and Cons of designing SC circuits in advanced sub-micron technologies.

Pros	Cons
The frequency of operation is improving due to the reduction of the minimum channel length size.	Variability pushes the channel thermal noise and the induced gate noise correlation to be an important limitation.
Due to the fast transition times, the amount of charge destroyed by having overlapping clocks is getting smaller for the same switches sizing. (*)	The continuous reduction of the channel length underlines the importance of the saturation velocity limitation, output resistance and intrinsic gain reduction. (*)
Matching of transistors is slightly improving. Matching of capacitors is stable in the 10-11 bits range.	Open-loop gain of amplifiers over PVT corners, specially at high temperatures, is subject to huge degradations. (*)
MoM capacitors are getting more and more efficient in terms of capacitance per unity area. No MiM capacitors are required and, hence, pure Logic Processes can be used to design low-cost mixed-mode circuits.	Leakage currents are increasing and becoming more important, specially the OFF-state current due to threshold scaling, and the gate tunneling current due to oxide thickness reduction.
New technology options of materials and structures are being investigated.	Linearity performance of switches in rail-to-rail operation is degrading since threshold voltage is not scaling proportionally. (*)
Modeling is following the needs. Holistic models have been developed for accurate noise modeling.	Time-dependent breakdown reliability constraint imposes low oxide defect density and low oxide field. (*)

1.2. Research contribution

The research work presented in this dissertation lead to the following original contributions:

1) A new switch-linearization circuit (SLC), which provides the necessary control voltages to the switches to guarantee the linear behavior without overstressing the gate. Part of the results of this development can be found in [1][2][3][4].

2) A new combination of open-loop amplification structures using amplifiers with local-feedback, with increased power efficiency and avoiding the need of additional calibration or correcting schemes. Part of this development can be found in [5][6].

3) The application for the first time of a single-phase technique to pipelined ADC, simplifying the circuit while maintaining the signal integrity and the overall performance when compared with conventional clock scheme. Part of this development is available in [7][8].

Two different integrated prototypes were fully designed and electrically simulated (over PVT corners) at transistor level[1]: 1) A two-channel time interleaved 6-bit 1GS/s pipelined ADC based on open-loop amplification using amplifiers with local feedback and employing the simplified single-phase scheme (applied to pipelined ADCs for the first time) and the proposed new SLC circuits; 2) A 10-bit 4-to-32MS/s pipelined ADC, again using the proposed new SLC circuits in the front-end sample-and-hold (S/H) and employing, as well, the referred single-phase scheme. However, due to the following factors only the second prototype was laid out, fabricated and experimentally evaluated: i) due to the limited time for pursuing the Ph. D. degree, it would be possible to design a single prototype integrated circuit; ii) it would be convenient to demonstrate the performance of the new SLC circuits at higher resolutions (this is, in fact the most original contribution of this Thesis). Hence it was preferred the 10-bit ADC rather than the 6-bit resolution one. Since it would be possible to test the 10-bit ADC also in sub-sampling mode, we would be able (as we did in fact) to

[1] In fact three, instead of two, prototypes were fully designed and simulated at transistor level, namely, the circuits reported in sections 6.1, .6.2 and in chapter 7. However, it is considered here, for the sake of simplicity, that the 10-bit ADC described in Chapter 7 is an improved version with many modifications (e.g. the linearization scheme employed in the switches in the signal path) that allowed to extend the sampling-rate up to 32 Ms/s) from the original 4 MS/s ADC, with the same resolution, described in section 6.1.

extend the signal frequency range to quite high values; iii) even if the 6-bit 1GS/s was fabricated, we would not be able to test it since, on the one hand, the available logic analyzer in the laboratory had a limited maximum acquisition frequency of 200 MS/s and, on the other hand, a complete new pad ring with high-speed, low-noise performance and with dedicated electrostatic discharge (ESD) protections would be necessary to be designed (and this is not an easy task unless for experienced I/O-pad designers) and, moreover, 3.3V or 2.5V LVDS output drivers would also to be designed from scratch in order to reach the desired 1GHz conversion rate. In conclusion, the 6-bit ADC would be much more risky to be integrated and experimentally evaluated (specially due to the testing environment and auxiliary testing structures) than the 10-bit ADC integrated circuit.

1.3. Structure of the Thesis

This Thesis is organized in eight Chapters. The first one is the present introduction, beginning with the presentation of the context, and revealing the motivation that is the cause of this research work. After, the major original contributions are mentioned, and the structure of this dissertation is pointed out.

The second Chapter presents an overview of the technology scaling and its impact in the devices and circuits characteristics. The power dissipation, the conductance, the gain, the speed and noise are analyzed, and the different sources of leakage are detailed.

The third Chapter is focused in the non-ideal behavior of the switches, a major problem to be solved in low-voltage implementations of SC circuits. The main sources of error are analyzed in detail, as conductance nonlinearity, charge injection and clock feed-through. Also, the switch controllability is questioned, considering the threshold and overdrive levels.

The fourth Chapter describes other major challenges in the design of SC circuits, as amplifiers, and circuit and structure complexity. The intrinsic nonlinearity and the power dissipation at higher speed of operation of the amplifiers, point to changes in architecture selection, some of them presented in this Chapter, as the fixed gain amplifiers and the open-loop structures. Also the commonly used non-overlapped clock signals sequence is analyzed, evidencing the need of solutions to overcome its complexity.

The fifth Chapter is a systematic presentation of conventional solutions to minimize the non-ideal behavior of the switches, ending with the proposal of a new switch-linearization technique. The bootstrapping and the switched-OpAmp (SO) techniques are dissected. Moreover, before being the new solution presented and deeply explained, the reliability issue of the switches is discussed in detail, clearly anticipating the usefulness and need of the proposed technique.

The sixth Chapter describes the electrical design of two ADC, using the solutions discussed and proposed in the previous Chapters. The first example, described in the first Section, is centered in the phase complexity problem, analyzing the possibility of application of the single-phase technique to medium resolution pipelined ADCs. The second design, described in the second Section, explores the characteristics of the passive sample-and-hold, of an amplifier employing local-feedback topologies and of the proposed switch-linearization circuit technique, in the design of a low resolution and high sampling rate complete pipelined ADC, with open-loop residue amplification structure.

The seventh Chapter presents the practical realization of a pipelined ADC in integrated circuit. The description of the design is focused on the front-end S/H circuit, where the proposed new SLC circuits are used. The realization of the SLC circuits for the particular S/H, with multiple sampling switches, is described, and the linearity of the switches over rail-to-rail signal swings is confirmed by the measured results. Also, the non-existence of stress over the gate is guaranteed.

Finally, Chapter eight draws the most important conclusions and final notes of this dissertation.

2. Switched-capacitor circuits in deep-submicron CMOS technologies

The scaling of metal-oxide-semiconductor (MOS) devices has stimulated new applications with remarkable improvements in cost, speed and power dissipation. In turn, the success of such improvements is pushing the technology towards new and continuous advances, which are taken for sure and granted. The expectation is high, and the density and speed of the integrated circuits (IC) are believed to increase, however the challenges of the scaling are increasing in number and complexity.

The increased speed requires an enough current, for speed in charging and discharging capacitances. The increased density, forces to a short channel length. Simultaneously, the power dissipation reduction is mandatory, scaling the supply voltage while sustaining the leakage current. Not only the fabrication techniques, but also the design techniques, need to be adapted.

2.1. Technology scaling

During the last four decades the industry has developed new IC process technologies and products. Each generation of process technology has doubled the transistor density, with a reduction of feature size to, approximately, 0.7. Till the 1990's, a new technology generation has been introduced every 3 years, resulting in the double of transistor density achieved every 3 years[2]. Figure 2.1 [9] shows the Intel feature size (metal line width) reduction over the last decades, in particular a reduction of 0.7 raised to the power of 7, during the early 7 technology generations, over one period of 21 years. The late technology generations have been introduced every 2 years, and the downscaling has been accelerated. The MOS gate lengths have been scaling down faster than the other feature sizes, as also shown in Figure 2.1.

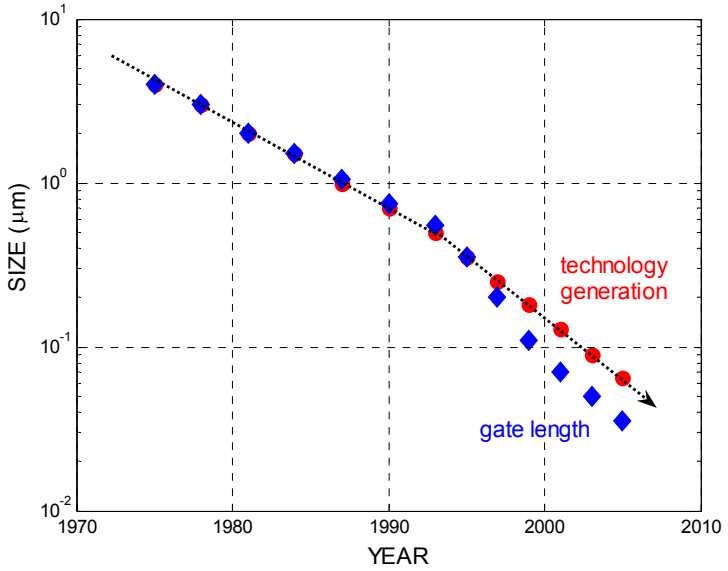


Figure 2.1: Feature size scaling [9].

Scaling so fast and so deeply has exposed new problems and constraints, solutions have been demanded, and questions about the end of MOS scaling have been placed more frequently. But the growing challenges and problems have been analyzed, numerous solutions are being proposed and presented, and the end is not yet in sight.

[2] The Moore' Law was based in an additional chip area doubling, consequently doubling the transistor count every 18 months.

The transistor or circuit parameter changes constant electric-field (CE) scaling were analyzed in detail in [10], and Table 2.1 reproduces the summarizing table, being k the scaling step. The CE scaling involves supply voltage and device dimensions scaling, being reduced by $1/k$, preserving the same electric-field in the new downscaled device.

Table 2.1: Scaling results for circuit performance [10].

Device or Circuit Parameter	Scaling Factor
Device dimension	$1/k$
Doping concentration	k
Voltage	$1/k$
Current	$1/k$
Capacitance	$1/k$
Delay time *per* circuit	$1/k$
Power dissipation *per* circuit	$1/k^2$
Power density	1

The CE scaling results in a reduction of the current, also by $1/k$, and subsequently the power dissipation is reduced by $1/k^2$ and the resistance is not changing. The area is also reduced by $1/k^2$ and, as the thickness of insulating films is reduced by $1/k$, the devices capacitances are only reduced by $1/k$ and the dynamic power dissipation by $1/k^3$. Therefore, as the resistance is constant, the delay time is reduced also by $1/k$.

As stated in [10], one area in which the device characteristics fail to scale is in the sub-threshold or weak inversion region of the turn-on characteristic. Below threshold, the current is exponentially dependent on the gate voltage, with an inverse semi-logarithmic slope that should be maintained. It was expected, as long as the tolerance spreads on the threshold voltage are also proportionally reduced, the CE scaled circuits operate properly at lower voltages.

Some key parameters, shaping the device or the circuit performance, are affected by scaling. The transconductance in strong inversion is maintained, but the available maximum transconductance in weak inversion is decreased through the current reduction, by $1/k$ [11]. Being the transconductance maintained the noise power spectral density is maintained and, as the signal voltage is decreased, the dynamic range (DR), for a fixed bandwidth, is reduced by

$1/k$. Also, the area mismatch is increased if the parameter fluctuations are not reduced with the downscaling.

The peculiar difficulties found with MOS devices threshold voltage scaling, and in keeping the adequate signal swing, and the degradation of some key parameters, forced the use of a constant voltage (CV) scaling rule, prior to the 0.5 μm technology. The supply and threshold voltages, V_{DD} and V_T, the oxide thickness t_{ox} and the matching parameter A_{VT}, are shown, for different technologies, in Figure 2.2 [12]. With CV scaling the doping concentration is increased by k^2, and the current and electric-field by k. Also, the power dissipation is increased by k and the dynamic power reduced only by $1/k$. The transconductance and DR are maintained, while the maximum transconductance and the delay time are improved. The improvements are supported in the power increase and also in the reliability degradation. In fact, in the CV scaling, the higher electric-field causes life span reduction, due to hot carriers and oxide breakdown.

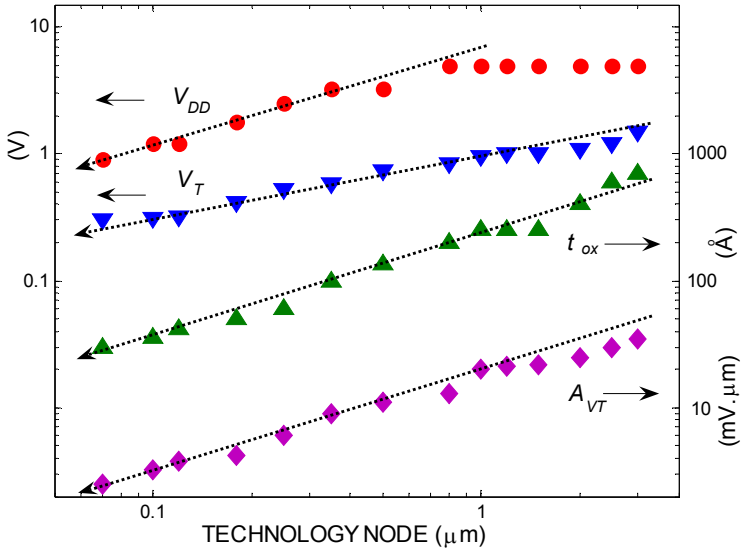


Figure 2.2: Supply and threshold voltages, thickness and matching parameter for different technologies [12].

Other scaling rules have been proposed, dealing with a constant area along with constant current or a constant power [11], but since the 0.5 μm technology the CE rule has been adopted and has been the driving force of MOS technology success.

More recently, however, the CE rule seems to have reached the lower limits of threshold voltage scaling. It was assumed [10] that the threshold voltage would scale together the supply voltage, while maintaining available the control capability over the device gate and improving the power and overall performance. However, after three decades of continuous scaling the sub-threshold leakage has increased from levels lower than 10^{-10} A/mm up to 10^{-7} A/μm [9] and, therefore, is nowadays a major limitation or constraint for deeper scaling. This is the main reason why, in deep-submicron technologies (beyond 90 nm) the "flavour" of high threshold devices is provided by the foundries.

Another assumption in CE scaling is the ability of continuously reduce the gate oxide thickness. The capacity of lowering the gate oxide thickness has contribute to the scaling success, however has reached only a few atomic layers, which can be close to the limit. Not only further thickness scaling is difficult, also the consequent gate-oxide leakage current increase, due to direct tunneling, becomes more complex to be handled and controlled.

Moreover, the CE scaling rule assumed that channel doping concentration could be continually increased, to attain threshold voltages and to limit short channel effects. However, when channel doping concentration gets too high, the proximity of the valence and conduction bands in the depletion region of the junctions causes a direct band-to-band tunneling leakage current, and an additional increase in the overall leakage current and power.

Other important issue is the interconnection lines scaling. When scaling the thickness and the width, the cross-sectional area is reduced by $1/k^2$. It is expected that the length is also scaled with a factor close to $1/k$, therefore the resistance is increased, approximately by k, as shown in Table 2.2 [10].

Table 2.2: Scaling Results for Interconnection Lines [10].

Parameter	Scaling Factor
Line resistance	k
Normalized voltage drop	k
Line response time	1
Line current density	k

Being the current also scaled, by $1/k$, the first conclusion is the current density is increased by k, which causes a reliability constraint. The other conclusion is that the voltage drop is maintained; however, as the voltage is decreased by $1/k$, the relative or normalized voltage drop is increased. Furthermore, the response time is maintained, which can be considered, relatively to the improvement in delay time of the scaled devices, not appropriated or even inadequate when complex layouts and long interconnection lines are used.

2.2. Achievable SNR and power dissipation

One major challenge for implementing precision analog circuitry in deeply scaled processes is the reduction of supply voltages. Lower supply voltages imply lower available voltage swings and limited signal-to-noise ratio (SNR). With reduced swings, and in order to maintain the dynamic-range in a noise limited circuit, the circuit noise should also be reduced [13], which requires, in a switched-capacitor (SC) circuit, the selection of a capacitor with increased size to lower the thermal noise. Increasing the capacitor size denotes a power dissipation cost.

Power dissipation of analog circuits is proportional to the level of signal integrity (SNR) and to the signal frequency, f_{in} [14]. For a simple circuit (class-A) driving a load capacitor C, the integrated thermal noise, σ_{rms}^2, and the bias current, i_{DS}, can be expressed by (2.1) and (2.2), with k the Boltzmann constant, T the temperature and A_{in} the input signal amplitude.

$$\sigma_{rms}^2 = \frac{kT}{C} \tag{2.1}$$

$$i_{DS} = 2\pi f_{in} C A_{in} \tag{2.2}$$

Introducing the voltage efficiency $\eta_v = A_{in}/V_{DD}$, and the current efficiency $\eta_c = i_{DS}/I_{DD}$, the minimum power P can be expressed as a function of the SNR (the input signal and noise power ratio) by (2.3).

$$P \propto \frac{1}{\eta_v \eta_c} T f_{in} SNR \tag{2.3}$$

More performance comes at the cost of increased current consumption. The power dissipation is technology independent, as long the voltage and current efficiency is maintained. Relation (2.3) is changed and become more explicit for the case of a transconductance amplifier operating linearly [15][16]. Assuming the MOS square law (and neglecting any body effect), the necessary transconductance, g_m, and the effective gate overdrive voltage, v_{GSeff}, can be expressed by (2.4) and (2.5).

$$g_m = 2\pi f_{in} C \tag{2.4}$$

$$v_{GSeff} = \frac{2 i_{DS}}{g_m} \tag{2.5}$$

Therefore, the power relation with frequency and SNR can be expressed by (2.6), presenting explicitly the supply voltage and the gate overdrive voltage.

$$P \propto \frac{1}{\eta_v^2 \eta_c} T f_{in} SNR \frac{V_{GSeff}}{V_{DD}} \tag{2.6}$$

The minimum power dissipation increases with decreasing supply voltage. Similar result is obtained for other thermal noise models [14][17]. Figure 2.3 shows [14] the power for a simple voltage buffer, with fixed topology and performance, for different supply voltages and technologies. The bold circles correspond to the use of the nominal supply voltage of the specific technology.

The minimum power dissipation increases with decreasing supply voltage over the same technology, and also with newer technologies at nominal voltage [14][18]. However, maintaining the supply voltage for different technologies, the newer requires lower power.

The analysis of the newest designs [15] shows that the relation defined by (2.6) is not always mandatory. Low resolution designs, in particularly, present lower power dissipation than expected when thermal noise is the dominant limitation. The accuracy of low resolution circuits is rather limited by component mismatch [13].

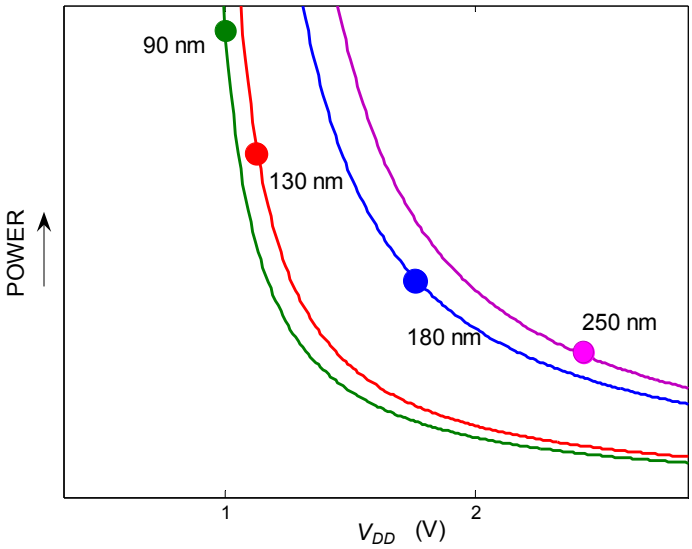


Figure 2.3: Power for a simple buffer, for different supply voltages and technologies [14].

Considering only the threshold voltage mismatch, and accepting that the voltage mismatch, σ_{VT}, is reported to scale as the oxide thickness, as shown in Figure 2.2, and to the inverse of the square root of the gate area, length (L) and width (W) product, as in (2.7), the minimum gate area for an imposed SNR can be expressed by (2.8) [12].

$$\sigma_{VT} \propto \frac{1}{\sqrt{WL}} t_{oxeff} \tag{2.7}$$

$$WL \propto \frac{1}{\eta_v^2 V_{DD}^2} t_{oxeff}^{\ 2} SNR \tag{2.8}$$

The minimum gate capacitance C_g, for the particular required accuracy, can be obtained, apart from the dielectric constants, dividing the area by the oxide thickness, as in (2.9).

$$C_g \propto \frac{1}{\eta_v^2 V_{DD}^2} t_{oxeff} SNR \tag{2.9}$$

The necessary current to support the input voltage swing, with amplitude A_{in} and frequency f_{in}, over the minimum capacitance, can be expressed as a fraction of the supply current, $\eta_c I_{DD}$, in a similar way as in (2.2), by (2.10).

$$\eta_c I_{DD} \propto \frac{1}{\eta_v V_{DD}} t_{oxeff} f_{in} SNR \tag{2.10}$$

Therefore, the power dissipation can be expressed by (2.11).

$$P = \propto \frac{1}{\eta_v \eta_c} t_{oxeff} f_{in} SNR \tag{2.11}$$

This derived expression points to a decrease of power when the oxide thickness is scaled down, and the voltage and current efficiency are maintained, in circuits where the mismatch is dominant. This result also indicates and confirms the existence of one extra power dissipation margin in certain circuits with scaled devices. These are the circuits requiring low resolution, when the value of the capacitor is determined by other constraints such as stability or matching, and that value is higher than the required by the thermal noise limitation. In this case it results in a power and area scaling trend similar to that of the digital circuits with constant speed [13]. The high resolution circuits still are dominated by the thermal noise. The diverging zone seems to be around the 55 to 65 dB [13], but also seems to be moving up with new technologies and circuits [15].

Also is relevant the voltage and current utilization factors. Newer designs are optimized to accommodate larger signal swings and to be more efficient in the current use.

2.3. MOS switches

An analog switch must present a low and linear ON-resistance for a large signal swing. The drain-to-source conductance, g_{DS}, of a MOS switch operating in the linear region is a function of the mobility in the channel, μ, the oxide capacitance *per* unit area, C_{ox}, the gate width and length, W and L, the gate-to-source voltage, v_{GS}, the threshold voltage, V_T, as represented by (2.12).

$$g_{DS} = \mu C_{ox} \frac{W}{L}\left(v_{GS} - V_T\right) \tag{2.12}$$

Scaling the device and lowering the oxide thickness, the capacitance *per* unit area is increased pointing to an increased conductance. However, that is canceled by the variation of the last term, the effective gate voltage. Considering that both the gate-to-source and the threshold voltages are lowered by $1/k$, the conductance is also lowered by $1/k$. More, as the threshold voltage is not scaling as fast as the supply and available gate-to-source voltages, the conductance is deteriorating with scaling.

Not only the achievable maximum conductance is reduced, also the linearity of the conductance is highly reduced with supply voltage, as the relatively increased threshold voltage is shrinking even more the signal amplitude span. That fact forces the use of very low signal levels and the use of common-mode signal levels close to one of the supply rails. Moreover, the body effect implies a threshold voltage variation, additionally increasing it for signal (source-to-bulk) increased voltages, and reducing even more the signal swing. In particular, the conductance of the switches used in sample-and-hold circuits operating at lower supply voltages, is more and more signal dependent.

Another challenge for highly scaled MOS devices is reducing the parasitic series source and drain resistances to tolerable values with very shallow source and drain junction depth [19]. One of the main novel aspects treated in this Thesis deals with how to solve the lack of linearity of the switches on deep-submicron CMOS.

2.4. Intrinsic gain and frequency of operation

As channel length is reduced, the effects of drain induced barrier lowering (DIBL) are increasing in importance. The DIBL is due to the fact that, as the drain voltage increases, the depletion region is increased and the potential energy barrier for electrons in the channel is lowered. In scaled devices this effect is opposed by the increased substrate doping, however it is equivalent to a threshold voltage reduction, increasing the current. This increase is additional to the channel length modulation and hot carrier impact ionization effects. Then, an increase in drain voltage is equivalent to a threshold voltage reduction, ΔV_T, as in (2.13) [20], and causes a supplementary increase in drain current, and therefore the output resistance is reduced.

$$\Delta V_T \approx V_{DD} e^{-L/i_{DS}} \tag{2.13}$$

Increasing the current or decreasing the length implies a reduction of gate control. Also the intrinsic voltage gain, the output resistance and transconductance product, is reduced.

Moreover, for very short channel lengths, the transconductance is limited by the velocity saturation. Therefore, devices from newer technologies show degraded voltage gain, even when the supply voltage is maintained. For scaled supply and threshold voltages, the gain lost is even deeper. At circuit level that lower performance can be compensated by techniques that boost the gain, such as cascoding, however it is difficult to fit within the allowed range left by the decreased supply voltage, and multi-stage (*e.g.* 3-stages) amplifiers become an alternative, more and more frequent.

Also, in scaled devices the transconductance-current ratio is not improving, as a function of effective gate voltage [15][21]. However, a higher transconductance-current ratio is achievable by new technology devices for the same operating frequency [15]. The frequency performance of devices improves with scaling. Considering the gate capacitance C_g is the product of area and capacitance *per* unit area, and assuming for simplicity the transconductance in strong inversion is as in (2.14), the maximum operating frequency f_{in} of the operation of the device is expressed as in (2.15).

$$g_m = \mu C_{ox} \frac{W}{L}\left(v_{GS} - V_T\right) \tag{2.14}$$

$$f_{in} = \frac{1}{2\pi}\frac{g_m}{C_g} = \frac{1}{2\pi}\frac{\mu}{L^2}(v_{GS} - V_T) \tag{2.15}$$

For different technologies with the same channel length, the maximum frequency hardly changes, and it is a function, apart from the mobility variation, of the effective gate voltage. However, reducing the length by $1/k$, equation (2.15) points to an increase of the maximum frequency by k^2.

This expectation is in part canceled by the lower mobility value in newer technologies, and also by the decrease of the effective gate voltage, due to the lower supply voltage allowed headroom. More, for very short channel lengths, the maximum frequency can be limited by

the velocity saturation v_{sat}, [20][22] as the transconductance is reduced to (2.16), and therefore, the maximum frequency is not any more a function of the effective gate voltage, resulting in equation (2.17).

$$g_m = C_{ox} W v_{sat} \tag{2.16}$$

$$f_{in} = \frac{1}{2\pi} \frac{v_{sat}}{L} \tag{2.17}$$

The maximum voltage gain, G, obtained in the case of infinite output impedance, is expressed as the ratio of the saturation transconductance, g_m, and the output conductance in saturation, g_{DS}, as in (2.18).

$$G = \frac{g_m}{g_{DS}} \approx e^{L/i_{DS}} \tag{2.18}$$

To increase the gain it is needed to increase the channel length or to reduce the current i_{DS}. In order to cancel the length scaling effect on the gain, the current and the drain control over the current must be also scaled. Therefore, the drain junction and depletion depths must be reduced, to reduce the size of the drain electrode and to introduce a shielding effect with the substrate region, and, most important, the oxide thickness must be reduced to increase the gate control (and the gate capacitance value).

There are changes in other capacitances causing the better frequency performance of the scaled devices. With technology scaling the junctions become shallower, roughly proportional to the technology feature size [14]. Also the junction area scales approximately in proportion to the minimum gate length. This leads to a significantly reduced junction capacitance. Also the parasitic capacitances are reduced by the feature size reduction. All these capacitance reduction cause an increased value of the maximum frequency of operation of the device. There is a clear trade-off between the lower voltage gain and the higher frequency of operation via device length; new technologies allow higher bandwidths with degraded quasi-dc performance. However, the overall result is improved, as the newer technologies deliver higher transconductance-current ratio, for the same frequency [15].

In Figure 2.4 is shown the effect of the channel length value in the intrinsic gain of a device, in a 90 nm technology. For the standard devices (standard threshold voltage), the increase of the intrinsic gain by increasing the length (as discussed before) is limited to a narrow range close to the regular length of the technology. Increasing more the channel length, has not any effect in the intrinsic gain value. One way to overcome the degradation of the gain is to use thick-oxide or high threshold devices. In Figure 2.4 is also shown the intrinsic gain of both types of device for different channel lengths, with the same technology. It is possible to increase the gain by a factor of 2, 3 or 4, by using alternative devices. Also, the thick-oxide devices can operate at high supply voltages, improving the power dissipation and the voltage swing. However, the frequency of operation is reduced, forcing to a limited use. In order to benefit from the best that technology scaling can provide, mixed device types or compound structures can be used. The use of high voltage and low leakage thick-oxide devices in certain blocks, can be combined with the use of high speed and improved matching thin-oxide devices in other blocks of the same circuit.

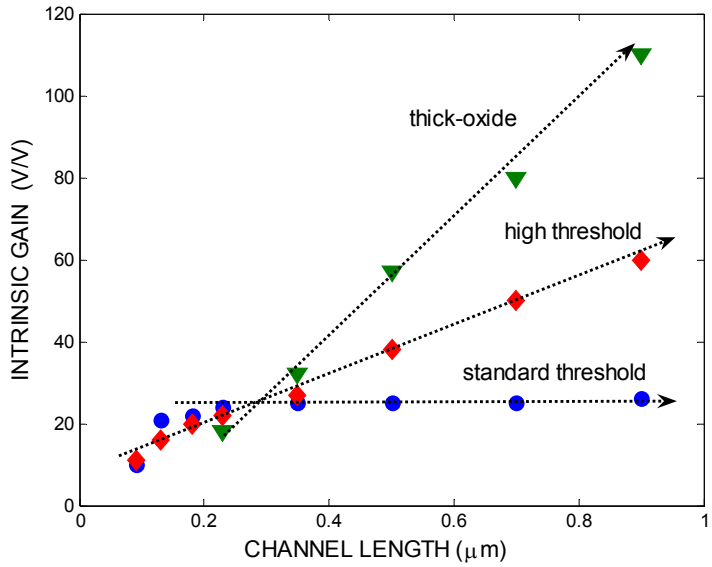


Figure 2.4: Intrinsic gain as a function of channel length, for standard, high threshold and thick-oxide devices.

BSIM4 model accuracy includes these issues [23][24]. Also, it is extended to the correction of the gate-to-source voltage at high frequencies, introducing new models for the gate intrinsic-impedance, resistive and capacitive. The gate current flowing through the impedance, a function of the length, causes a voltage drop and then lowering the internal gate voltage.

2.5. Device leakage

The device leakage issue can be divided in three different areas, corresponding to three different sources of leakage, which relative importance is changing as devices are deeply scaled: junction leakage, gate leakage and OFF-state leakage.

The junction leakage arises from the high doping concentration in the channel region, increased to attain threshold voltages and to limit short channel effects in aggressively scaled devices. The proximity of the valence and conduction bands in the depletion region of the junctions causes a parasitic tunneling current, the gate induced drain leakage (GIDL) current I_j. Although the leakage is high (approximately 1 nA/μm with L = 30 nm and 1 V reverse bias) is one to two orders of magnitude smaller relatively to the other leakages [25]. Also, when projecting the increase in doping for the next generation scaled devices, as depicted and identified by the gate length in Figure 2.5 [25], still it will be lower.

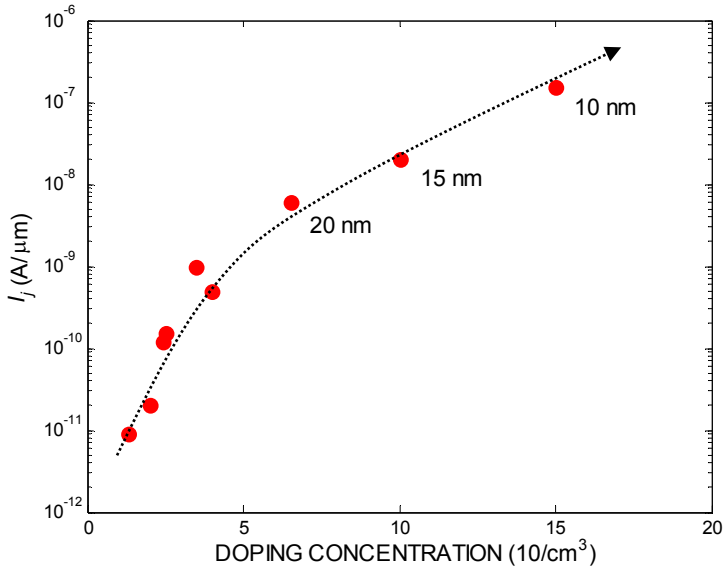


Figure 2.5: Junction leakage for different doping concentrations (1 V reverse bias) [25].

As the scaling was going further with the reduction of oxide thickness, it was predicted the gate leakage would increase and be the final limitation to scaling, becoming dominant over the OFF-state leakage. Gate current is due to direct tunneling through the gate oxide, and then the oxide thickness scaling has been controlled and restrained. However, the need to maintain

the control over the gate and to minimize the sub-threshold current is pushing the oxide scaling to continue or, in alternative, to use high-K dielectrics for MOS device applications and to apply multi-layer dielectric stacks, presently an area of active research and development. Figure 2.6 shows the gate leakage current I_g, as a function of the equivalent oxide thickness value *EOT*, for high-K dielectrics and oxide, with 1 V bias [25].

The recent BSIM4 gate tunneling model includes the gate current between the gate and the substrate, the current between the gate and the channel, being this partitioned between both the source and the drain, and the current between the gate and the diffusion regions [23][24]. BSIM4 also includes the equivalent oxide thickness parameter *EOT*, to be used for non-oxide gate insulators.

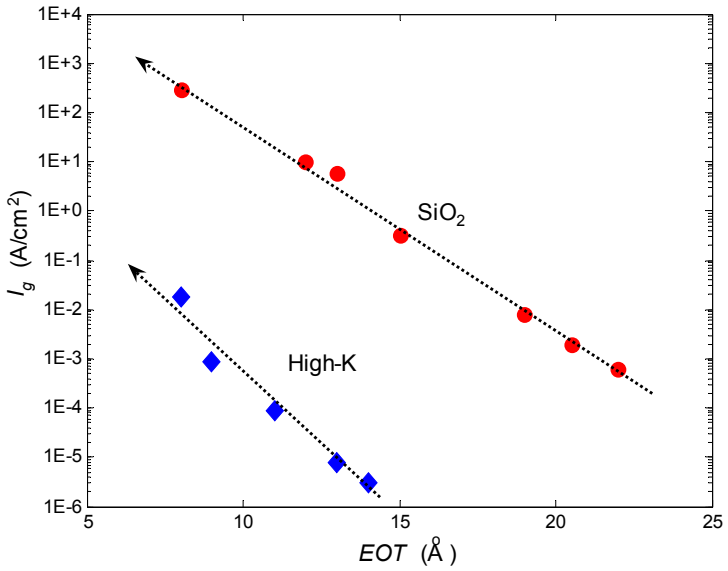


Figure 2.6: Gate leakage as a function of the *EOT*, for high-K and oxide (1 V bias) [25].

The power due to gate leakage is dominated by the turned-ON MOS devices. However attempts to reduce it by applying moderate gate voltages are not very useful, as the leakage increases fast in the range of low gate voltages, and for larger voltages the increase is slower. The leakage current value is close to 10 and 100 A/cm^2, for 1.2 and 0.8 nm oxide respectively, with the nominal supply voltage applied to the gate [25][26]. The last value implies, approximately, 1 A leakage current for one integrated circuit with 1 mm^2 oxide (active) area of turned-ON devices.

Additionally to the power related to that significant value, another issue must be considered. With the higher relevance of the leakage current, the traditional gate capacitance must be considered to be in parallel to a tunnel conductance, g_{tunnel} [14]. Both are area dependent, however the frequency associated to the parallel, f_{gate}, is area independent, as in (2.19) for an NMOS case [14].

$$f_{gate} = \frac{g_{tunnel}}{2\pi C_g} \approx 1.5 10^{16} V_{GS}^2 e^{t_{oxeff}(V_{GS}-13.6)} \tag{2.19}$$

This frequency defines the diverging point of capacitance or conductance preponderance; for lower frequencies the leakage current is dominant, and for higher frequencies the gate impedance is mainly capacitive and the device behaves as conventionally.

The thinner is the oxide, the higher is the frequency and the larger is the range of frequencies where the leakage current is dominant, possibly invading the workable frequency range. With thinner oxides, the gate current evaluation, i_{GS}, becomes mandatory (2.20) [14], such as the current gain estimation, the drain and gate current ratio.

$$i_{GS} \approx C_{ox} W L f_{gate} \tag{2.20}$$

The transistor OFF-state leakage is perhaps the greatest problem facing continued scaling. As the transistor scales, the power supply voltage is scaled to maintain a moderate electric field and active power. The OFF-state power, the supply voltage and leakage current product, is not decreasing or even maintained. The leakage current is hugely increased by scaling, as the threshold voltage is reduced. Figure 2.7 shows the OFF-state leakage current, I_{off}, as a function of the gate length, including for some research devices.

Nevertheless the threshold voltage has been moderately reduced, slower than the supply voltage as shown in Figure 2.2, the OFF-state current has increased and the power is, or will be in the new technologies, in the same order of magnitude compared with the active or ON-state power.

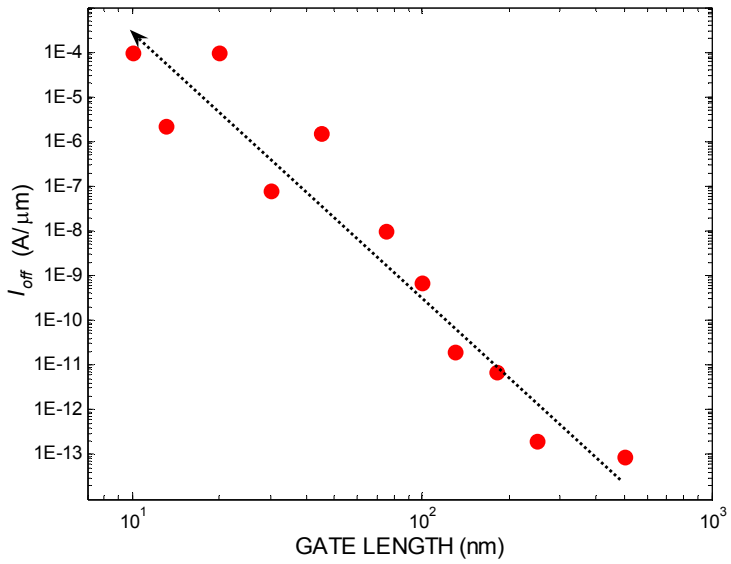


Figure 2.7: OFF-state leakage current for different gate lengths [25].

Below the threshold voltage, the drain-to-source current i_{DS}, decreases exponentially with the gate-to-source voltage v_{GS}, as in (2.21), where q is the unity charge, k is the Boltzmann constant, and s_T represents the sub-threshold slope factor, which indicates the weight of the oxide capacitance compared with the bulk-to-channel capacitance [22].

$$i_{DS} \propto e^{qv_{GS}/s_T kT} \tag{2.21}$$

Assuming the threshold voltage is defined as the gate voltage at which the drain current is 100 nA *per* unity geometry ratio W/L, equation (2.21) can be rewritten as (2.22), with the current in nA.

$$i_{DS} = 100\frac{W}{L}e^{q(v_{GS}-V_T)/nkT} \tag{2.22}$$

The OFF-state current (in nA) can be expressed by (2.23), being visible the dependency with the threshold voltage and with the temperature. The last justifies the frequent demands for the use of low temperature cooling of large ICs.

$$I_{off} = 100\frac{W}{L}e^{-qV_T/nkT} \tag{2.23}$$

2.6. Devices variability and matching

Variability is an issue of major importance, while the scaling is pushing the technology to go faster and deeper. Uncertainty, after characterization, reduction and adaptation, results in variability. The new relevant properties of the researched devices are projected and measured, the manufacturing processes are controlled and improved, and new designs are adapted and innovated.

The relative spread or matching is, usually, a major limit of the achievable performance of analog circuits. With scaling, the channel doping has increased to undesirably levels in order to gain adequate control of short-channel effects and to set the threshold voltage properly. As a result, due to the small total number of dopants in the channel of extremely small MOS devices, the percent stochastic variation in the number and location of the dopants will increase, and this will sharply increase the statistical variability of the threshold voltage.

The variance of the change of the threshold voltage of different devices is proportional to the inverse of the area, and to the area proportionality constant for the threshold voltage, A_{VT} [27][28]. The relative mismatch with the drain current (i_{DS}) can be expressed as in (2.24)[14].

$$\frac{\sigma^2}{I_{DS}^2} = \left(\frac{A_{VT}}{\sqrt{WL}} \frac{g_m}{i_{DS}} \right)^2 \qquad (2.24)$$

The factor A_{VT} is assumed as proportional to the oxide thickness [12][14], as in Figure 2.2, being reduced by 1/k. However, this is canceled by the area scaling. The classical way to reduce mismatch is to enlarge the device, spending area and power. One option is to reduce the transconductance-current ratio.

However, devices with small geometries also experience larger mismatch due to higher order terms with either short W or L. Also, when the oxide thickness is reduced to a few atomic layers, quantum effects will dominate and matching will degrade. The relative mismatch of the current must be incremented with the mismatch of the gate leakage current. Assuming it is

proportional to the gate current with a proportionality constant X_{iGS}, the total relative mismatch of the device current is as in (2.25) [14].

$$\frac{\sigma^2}{i_{DS}^2} = \left(\frac{A_{VT}}{\sqrt{WL}} \frac{g_m}{i_{DS}} \right)^2 + \left(\frac{X_{iGS}}{\sqrt{WL}} \frac{i_{GS}}{i_{DS}} \right)^2 \qquad (2.25)$$

This second term may increase with increased W and L, for large gate areas, resulting in an increased total relative mismatch of drain current differing from the usual expectation. However, reduction of mismatch can be achieved by increasing only the channel width, as both terms are improved [14].

Other issue related with the variability is the noise. The flicker noise or $1/f$ noise describes the quality of the conductive medium, and most of its power is concentrated at low frequencies. In a MOS device it is caused by the charge carriers in the channel getting trapped and later released, changing the carrier in number and mobility. The more homogeneous is the channel region, the lower is the flicker noise. The flicker noise does not depend on temperature, as the thermal noise does. It is proportional to the fabrication (homogeneousness) parameter, and to the inverse of area and frequency of operation. Then, scaling down the feature size and increasing the concentration forces to reconsider the importance and formulation of the flicker noise. BSIM4 offers an improved unified flicker noise model, which is smooth over all bias regions and considers the bulk charge effects [24].

The BSIM4 also offers an improved thermal noise model. Additionally to the charge-based model, the holistic model is provided, considering all the short-channel effects and velocity saturation effect. More, the noise-partition analysis unifies the induced gate noise and the channel noise with correlation [24]. The noise current through the gate capacitance, generated by the channel resistance high frequency noise, is now considered, such as its amplification.

2.7. Conclusions

It has been projected that MOS devices with equivalent oxide thickness of a few atoms, and with gate lengths of a few nanometers, will be in production in the next future years. New materials and alternative devices are under active research, as the non-oxide dielectrics, new

doping techniques and new device structures. The development of the manufacturing processes will provide material and solutions suitable to an easier challenges overcome. The models are being updated. From all that, the circuit design community has the task to develop techniques, architectures and circuits which must deliver high performance and throughput at low power. Additional and complementary information described in this Chapter can be found in [29] to [37].

3. Main challenge in the design of SC circuits in advanced CMOS technologies: switches

A major problem to solve low-voltage implementations of switched-capacitor (SC) circuits is the non-ideal behavior of the switches. The linearity of the switches is affected by the reduced supply voltage in advanced complementary metal-oxide-semiconductor (CMOS) processes, and the performance of the circuits depends heavily on the maximum voltage available to drive the switches. Several simple solutions such as voltage-doublers, the bulk-switching technique or the use of low-VT devices have been proposed over the past decade. This Chapter attempts to overview the most relevant techniques to improve the linearity of the switches.

3.1. Introduction

Since the conductance of the switches is signal dependent, it becomes an important source of errors (*e.g.* causing harmonic distortion) in SC circuits, as the conductance settles the charging and discharging time constants. Attempts to minimize this particular error by oversizing the switches, not only contribute to a decrease of the efficiency, but also increase the charge injection when the switch turns OFF. Charge injection creates important offset errors as well as nonlinear errors, as it is not completely signal independent.

In this Chapter, the main non-idealities of the switches are described and analyzed in detail. Most relevant existing solutions are also presented.

3.2. The switch conductance

In the linear region, for small signals, the metal-oxide-semiconductor (MOS) switch drain-to-source current, i_{DS}, can be expressed by

$$i_{DS} = \mu C_{ox} \frac{W}{L}\left(v_{GS} - V_{TO} - \frac{v_{DS}}{2} \right) v_{DS} \qquad (3.1)$$

It is a function of the mobility in the channel, μ, the oxide capacitance *per* unit area, C_{ox}, the gate width and length, W and L, the gate-to-source voltage, v_{GS}, the threshold voltage (assumed for simplicity to be constant), V_{TO}, and the drain-to-source voltage, v_{DS}. The switch drain-to-source conductance, g_{DS}, is then represented by

$$g_{DS} = \frac{\partial i_{DS}}{\partial v_{DS}} = \mu C_{ox} \frac{W}{L}\left(v_{GS} - V_{TO} - v_{DS} \right) \qquad (3.2)$$

Supposing that the mobility is constant along the channel, and the v_{DS} voltage is small and can be ignored, the g_{DS} is directly dependent on the geometry, W/L, and on the effective gate-to-

source voltage, $v_{GSeff} = v_{GS} - V_{TO}$, in the form (3.3). The drain-to-source switch conductance value, and its variation with different variables and parameters, defines the SC circuit useful dynamic range (DR).

$$g_{DS} = \mu C_{ox} \frac{W}{L} v_{GSeff} \tag{3.3}$$

Figure 3.1 illustrates a simple SC circuit, such as a sample-and-hold (S/H) block. This S/H is electrically simulated using a standard 1.2 V 130 nm CMOS technology and BSIM3v3.4 models, being the NMOS device sized with aspect ratio 5/0.13, for a constant input voltage v_{in} = 0.6 V, for a step voltage v_G = 1.2 V with 50 ps rise time and applied between the gate and V_{SS}, the capacitor C_S = 1 pF, initially discharged.

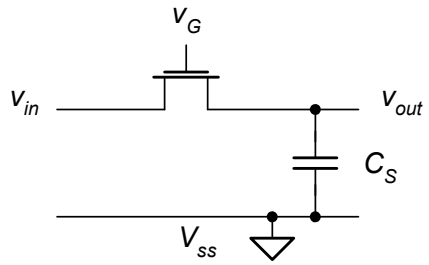


Figure 3.1: Basic sampling circuit.

The capacitor is charged following an exponential (linear) response as illustrated in Figure 3.2(a). The capacitor voltage, v_{out} item (a), ultimately (in infinite time) will reach the input voltage, v_{in}.

Observing Figure 3.2(b), it is clear that immediately after the switch is turned ON, it operates not in the linear but in the saturation region, with a large v_{DS} value. The ratio i_{DS}/v_{DS} represents the inverse of the equivalent resistance of the switch device, shown in Figure 3.2(b). Initially different from the conductance g_{DS} previously defined, both values will converge as the linear region of operation is reached. In this case, the charging time constant is smaller than the one calculated assuming the final value of conductance.

Figure 3.2(a) illustrates the output voltage, v_{out} item (b), if an ideal switch with such a conductance value is used, replacing the NMOS device. Then, in this case, the conductance value conduces to an over estimated value of the charging time.

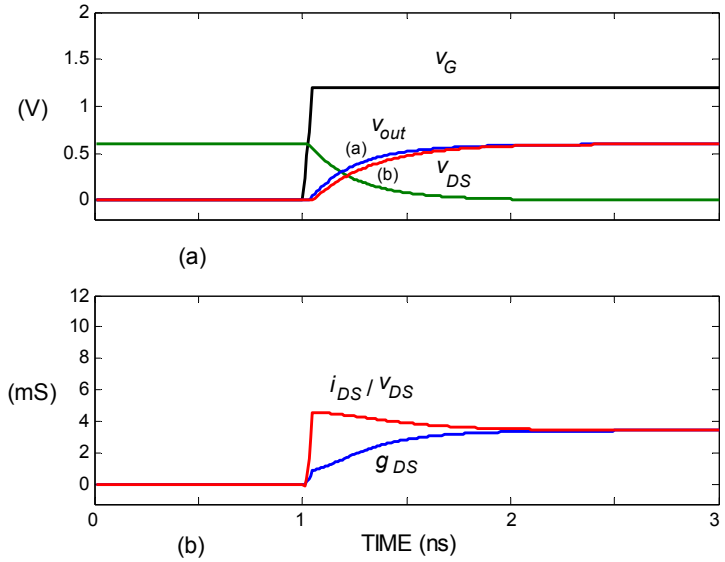


Figure 3.2: (a) Gate, drain-to-source and output voltages; (b) Conductance and inverse of drain-to-source resistance.

Figure 3.3(a) illustrates the case of the output response if the gate step voltage, with an overdrive voltage of 1.2 V, is applied between the gate and the input source.

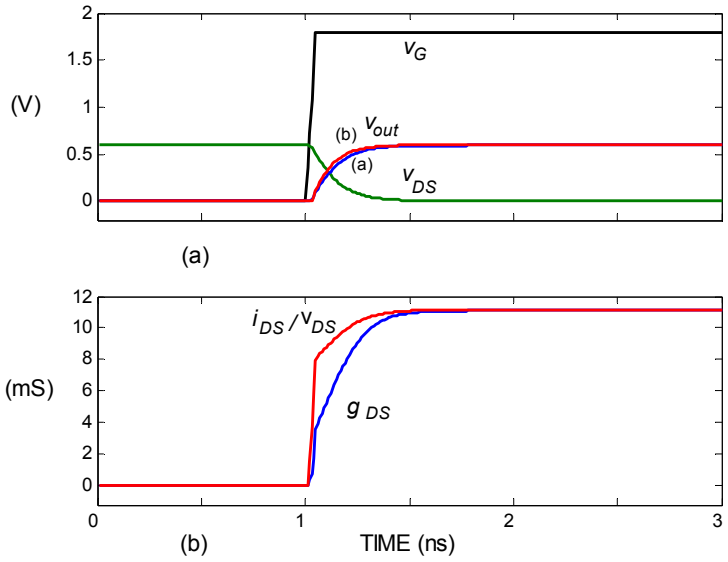


Figure 3.3: Waveforms with increased gate voltage; (a) Gate, drain-to-source and output voltages; (b) Conductance and inverse of drain-to-source resistance.

Because of the increased value of the effective gate-to-source voltage, the ratio i_{DS}/v_{DS} and the conductance g_{DS} curves will converge to a final higher value, as shown in Figure 3.3(b). The capacitor will charge faster than in the previous example. However, if the final conductance value is used for an ideal switch, the output voltage, v_{out} item (b), shows that, in this case, the use of the final conductance for the charging time calculation would conduce to a under estimated value.

Being, in certain cases, the calculation of the charging time a conservative approach, or an optimistic in other cases, the switch conductance is an important instrument to determine (and limit) the circuit response and performance. The relative error, ε, between the output, v_{out}, and the input, v_{in}, is an exponential function on the measuring time, usually half the period of the sampling frequency, F_S, and the time constant. This error is given by (3.4), where C_S represents the capacitance value of the sampling capacitor.

$$\varepsilon = e^{-\frac{g_{DS}}{2F_S C_S}} \tag{3.4}$$

The acceptable relative error for a desired number of bits accuracy, N, is given by

$$\varepsilon < 2^{-N} \tag{3.5}$$

Then, the conductance can be defined as a direct function on the sampling frequency, accuracy, and sampling capacitance, in the form (3.6).

$$g_{DS} > 2C_S F_S N \ln(2) \tag{3.6}$$

The conductance of the used switches is of the major importance, since it sets a limitation on the operating frequency[3]. As seen, the sampling process, not beginning always with the switch in the linear region of operation, will end with the lower possible drain-to-source voltage value and in the linear region.

[3] Notice that, when there are (as usual) an active element in the circuit (amplifier) the g_{DS} is made much larger (3 to 7 times) then the requiered value. The idea is to put the limitation of the speed on the active element side, rather than in the switch itself.

Assuming the same sizing, to increase the conductance of the switch, and decrease the time constant, equation (3.3) indicates two possibilities: 1) up-scaling the switch device, increasing its ratio W/L; 2) increasing the effective gate-to-source voltage.

The first possibility will cause other problems, namely will increase the clock feed-through and the charge injection and also the load of the previous circuit (if it is the case). The second possibility can be achieved either by using higher gate voltages, or by reducing the threshold voltage.

The use of lower and lower values of supply voltages evidences the challenge to use those possible solutions. With reduced voltages, the feed-through phenomena is more problematic. Also the use of higher gate voltages is difficult and implies the use of voltage multipliers. Moreover, the threshold voltage values have also increased relatively to the supply voltage.

3.3. The switch channel width scaling effects

Increasing the switches dimensions (W), will increase the clock feed-through and the charge injection. Charge injection is the process that occurs when the switches are turned OFF, of charging the capacitors in it's vicinity by means of the charges stored in the switches channels, when they are in the ON state.

The clock feed-through, in the restrict sense, is the error added to the sampled voltage by the clock signal transitions due to the switches coupling capacitances. Those phenomena add errors to the sampled capacitor voltage. Furthermore, as the switches are turned ON and turned OFF periodically, the overall error can increase as a result of the accumulation of charges.

3.3.1. The switch capacitances

A MOS switch is ON if a current can flow between the drain and the source. For that, charges must be present forming a conducting channel under the gate. The amount of charges, and thus the current controllability, is a function of the applied voltages and a function of two

capacitances: the existing capacitance between the gate and the channel region (C_{GC}), and the capacitance between the bulk and the channel (C_{BC}).

The channel is isolated from the gate by the oxide layer, forming the gate-to-channel capacitance, $C_{GC} = C_{ox}WL$, depicted in Figure 3.4. The depletion layer isolates the channel from the bulk, originating a junction capacitance, the bulk-to-channel capacitance, $C_{BC} = C_{jBC}WL$, being C_{jBC} the junction capacitance *per* unit area. This one is dependent on the applied voltage and then the channel charge and bulk-to-channel voltage have a nonlinear relation. In a standard implementation, with several MOS devices sharing the same substrate or bulk, is impossible the use of the bulk-to-channel voltage to control the charges, and then to control the current. Therefore, the control is usually done acting directly in the gate-to-source voltage, *i.e.* acting indirectly in the gate-to-channel voltage. Another difficulty is to null or compensate the bulk-to-channel capacitance dependency on applied voltage.

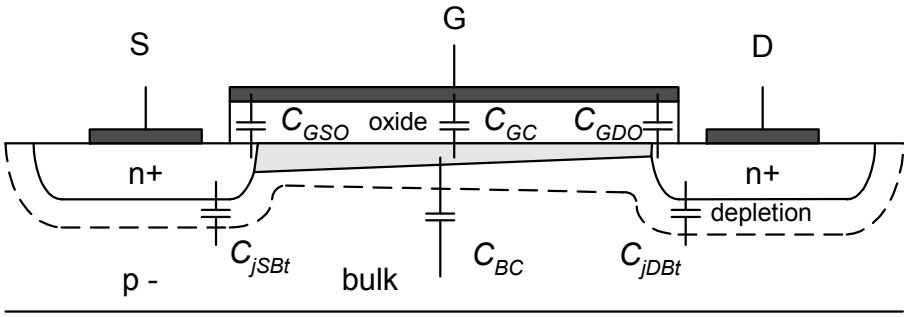


Figure 3.4: MOS capacitances illustration.

The depletion layer also isolates the source area and the drain area from the bulk, originating junction capacitances: the source to bulk capacitance, $C_{jSBt} = C_{jSB}A_S$, and the drain-to-bulk capacitance, $C_{jDBt} = C_{jDB}A_D$, being A_S and A_D the source and drain areas, and C_{jSB} and C_{jDB} the corresponding junction capacitances *per* unit area. When the channel is present the drain, source and channel are tied and the previous capacitances are extended, sharing the formed bulk-to-channel capacitance. The last is divided in two, one to be added to the former area defined source-to-bulk capacitance, and the other added to the also former area defined drain-to-bulk capacitance. The ratio is supposed to be close to 50/50 when the device is in the linear region of operation [38], as in form (3.7).

$$C_{SB} = C_{jSBt} + \frac{1}{2}C_{BC} \quad \text{and} \quad C_{DB} = C_{jDBt} + \frac{1}{2}C_{BC} \tag{3.7}$$

As the operation approaches the saturation region, the channel near to the drain becomes thinner and is replaced by the pinch-off region, and the channel at the source side becomes thicker. Then the bulk-to-channel capacitance is gradually divided with different ratios between the source and the drain sides. Usually, in saturation, the figure of 2/3 [39] is applied for hand calculations, yielding

$$C_{SB} = C_{jSBt} + \frac{2}{3} C_{BC} \quad \text{and} \quad C_{DB} = C_{jDBt} \tag{3.8}$$

The gate area, overlapped with the source and drain area by a length L_D, creates two extra oxide capacitances, the gate-to-source overlap capacitance, $C_{GSO} = C_{ox} W L_D$, and the gate-to-drain overlap capacitance, $C_{GDO} = C_{ox} W L_D$. When the channel is present, these capacitances are extended by sharing the gate-to-channel capacitance influence, in a similar way than previously, resulting in total gate-to-source capacitance, C_{GS}, and total gate-to-drain capacitance, C_{GD}.

In the linear region of operation:

$$C_{GS} = C_{GSO} + \frac{1}{2} C_{GC} \quad \text{and} \quad C_{GD} = C_{GDO} + \frac{1}{2} C_{GC} \tag{3.9}$$

and, in saturation:

$$C_{GS} = C_{GSO} + \frac{2}{3} C_{GC} \quad \text{and} \quad C_{GD} = C_{GDO} \tag{3.10}$$

The electrical schematic shown in Figure 3.1 can be re-simulated, now with a pulse voltage v_G = 1.2 V, with 50 ps rise and fall times, rising at 1 ns and falling at 3 ns, applied between the gate and V_{SS}, with three different switch sizes, the former 5/0.13 ratio, 20/0.13 and 40/0.13. The obtained transient responses are shown in Fig3.5(a) and (b). In Figure 3.5(a) the output voltages are displayed and Figure 3.5(b) shows the output current, i_{out}. It is clear that the up-scaled switches produce a faster response. In fact the conductance is proportional to the size of the switch (W), allowing for a higher peak current and a smaller settling-time. A small

inverse current can be observed, conducing to a voltage decay, when the gate voltage falls (3 ns instant).

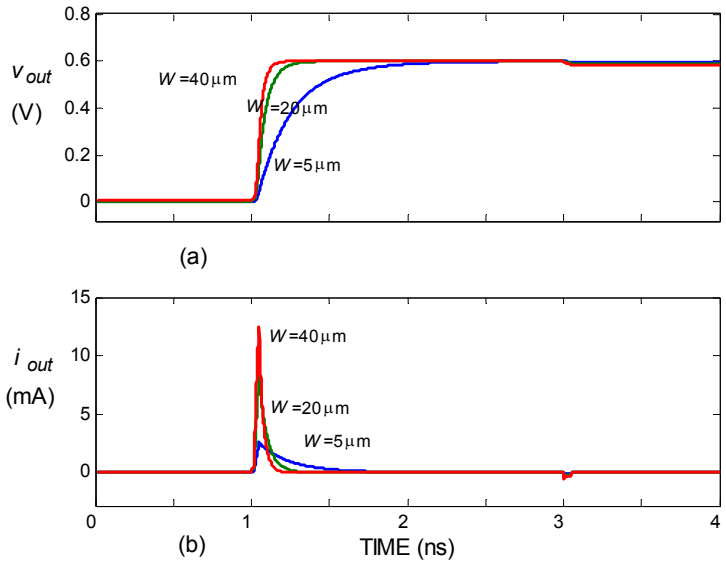


Figure 3.5: Changing switch aspect ratio; (a) Output voltage; (b) output current.

In Figure 3.6(a) and (b) an amplified image at that instant is displayed. The higher the switch width, the more significant the inverse current and the voltage drop. Up scaling the switches size can widen the conductance, however it will increase the error.

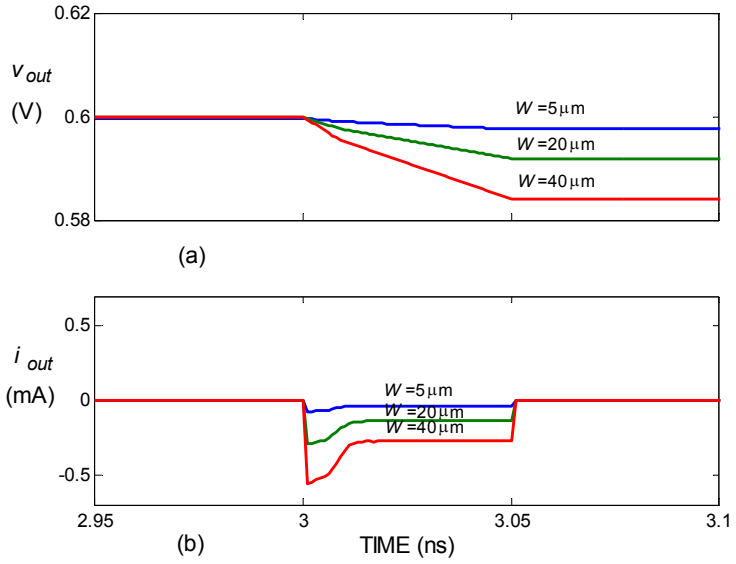


Figure 3.6: Switch turning-OFF period; (a) Output voltage; (b) Output current.

In Figure 3.7(a), the evolution of the simulated gate-to-source and gate-to-drain capacitances is presented. During the OFF state, those capacitances are reduced to the overlapped values. During the ON state they are increased by the gate-to-channel capacitance influence. Immediately after the switching-ON period, the gate-to-source capacitance assumes all influence, being this influence shared between source and drain as the linear region of operation is reached.

Figure 3.7(b) shows the total gate capacitance, C_{GG}. The total gate capacitance, defined as the change in gate charge due to a gate to bulk voltage variation, is the sum of the gate-to-source and gate-to-drain capacitances during the ON state. When the switch is OFF, the total gate capacitance reflects not only the sum of the overlap capacitances, but also the residual capacitance between the gate and the bulk, in the absence of the channel.

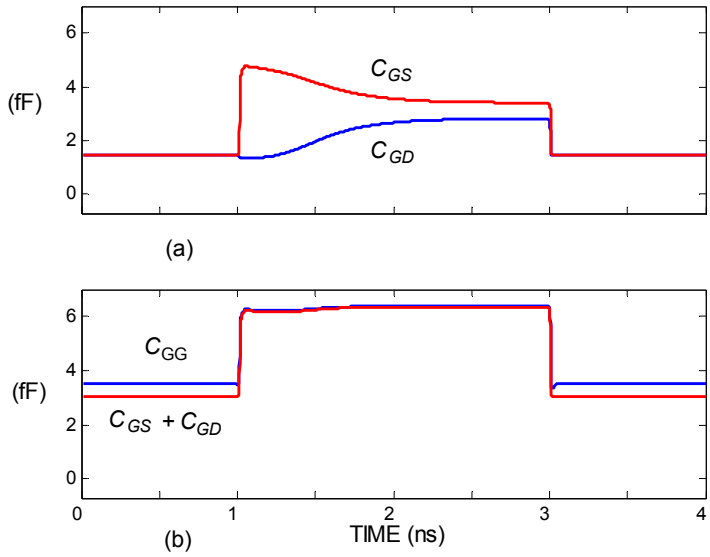


Figure 3.7: (a) Gate-to-source and gate-to-drain capacitance; (b) Sum and total gate capacitance.

In a deeper and systematic study, it should be noticed that a MOS device has four terminals and, therefore, there is a fourth terminal capacitor. The charges on those four terminals depend on the four relative applied voltages. As a matter of fact, the charge on each terminal depends simultaneously on the four applied voltages.

Thus, a set of four derivative equations can be written, or, in a matrix way, the MOS can be modeled and characterized by a four-by-four matrix as indicated by (3.11), composed by

sixteen capacitances, C_{ij}, setting the relation between the derivative of the charges, Q_i, and the derivative of the applied voltages, V_j [40].

$$[\partial Q_i] = [C_{ij}][\partial V_j] \tag{3.11}$$

Considering that the sum of the present charges in the four terminals must be zeroed, and that the charges are function on the voltage differences between the four terminals, only three of the four charges and voltage differences are independent variables. The system characterization can be made by a three-by-three matrix, resulting in a total of nine capacitances. The circuit simulator SPICE provides these nine capacitances.

3.3.2. Charge injection and clock feed-through

Mobile charges are held in the channel when the MOS device is ON. When the device is turned OFF the channel disappears and those charges go somewhere into the elements in the vicinity. In a simple S/H circuit, like the one shown in Figure 3.1, the device is between the input voltage and the sampling capacitor, so it is towards these two elements that the charges are going to move. Thus, a voltage error is added to the sampled voltage. The clock feed-through imposes an additional error via the gate-to-source or to drain capacitances. The channel charge, Q_C, is a function on effective gate-to-source voltage and on the oxide capacitance value, in a form given by

$$Q_C = -C_{ox}WL(v_{GS} - V_{TO}) = -C_{GC}(v_{GS} - V_{TO}) \tag{3.12}$$

The minus signal refers to an NMOS device, with negative mobile charges. As the source voltage is close to the input voltage, the channel charge is signal-dependent, according to the maximum clock voltage applied to gate, $V_{\phi max}$, and on the input signal, as in (3.13).

$$Q_C = -C_{GC}\left[V_{\phi\,max} - (v_{in} + V_{TO})\right] \tag{3.13}$$

The voltage error on the sampling capacitor due to charge injection, ε_{chi}, is a function of the capacitor value and of the way the channel charge is divided between input voltage source and sampling capacitor, or function on a fraction, c_r, of the channel charge going to the sampling capacitor, as in equation (3.14).

$$\varepsilon_{chi} = -\frac{c_r C_{GC}\left[V_{\phi max} - \left(v_{in} + V_{TO}\right)\right]}{C_S} \tag{3.14}$$

The clock feed-through error, ε_{clkf}, is a function of the clock voltage swing, $\Delta V_\phi = V_{\phi max} - V_{\phi min}$, and a function of the two capacitance relation, the gate-to-source or gate-to-drain capacitance, which one is at the sampling capacitor side, and the sampling capacitor itself. Supposing the source is the one selected, in equation (3.15) is used C_{SG}, denoting the computation of the error is related to a variation in the source due to a change in the gate voltage.

$$\varepsilon_{clkf} = -\frac{C_{SG}\Delta V_\phi}{C_{SG} + C_S} \tag{3.15}$$

The minus signal refers to an NMOS device, as the clock signal falls down to switch-OFF the device. When first observed, the error seems signal level independent, however the gate-to-source capacitance is not constant during the switching-OFF process.

The total error calculation has been studied thoroughly by several authors [41], despite which it is possible to make a preliminary approach considering that the gate-to-source capacitance is reduced when the effective gate voltage reaches the threshold level. In the ON state, the gate-to-source capacitance has two items: one is the overlap capacitance and, the other is the fraction of the gate-to-channel capacitance, considered to be at the source side, as in (3.16). When the device is OFF, the gate-to-source capacitance is reduced to the overlap term.

$$\varepsilon_{clkf} = -\frac{c_r C_{GC}\left[V_{\phi max} - \left(v_{in} + V_{TO}\right)\right]}{c_r C_{GC} + C_S} - \frac{C_{GSO}\Delta V_\phi}{C_{GSO} + C_S} \tag{3.16}$$

The first item needs to be corrected, since the gate-to-channel charge, and capacitance, is gradually reduced as passing through strong and weak inversion operation. The weight of it should be a fraction h of the initial values, close to one half if supposing that reduction linear. The total error can then be expressed by a single equation (3.17).

$$\varepsilon_{chi} + \varepsilon_{clkf} = -c_r C_{GC}\left[V_{\phi\,max} - \left(V_{in} + V_{TO}\right)\right]\left(\frac{1}{C_S} + \frac{h}{c_r h C_{GC} + C_S}\right) - \frac{C_{GSO}\Delta V_\phi}{C_{GSO} + C_S} \qquad (3.17)$$

Supposing the process occurs with the switch in the linear region of operation, $c_r = 0.5$, and also $h = 0.5$, and if the sampling capacitor used has a much higher value than one fourth of the gate-to-channel capacitance, the equation can be simplified as (3.18).

$$\varepsilon_{chi} + \varepsilon_{clkf} = -\frac{c_r (h+1) C_{GC}\left[V_{\phi\,max} - \left(V_{in} + V_{TO}\right)\right]}{C_S} - \frac{C_{GSO}\Delta V_\phi}{C_{GSO} + C_S} \qquad (3.18)$$

The capacitance C_{GC} present in first item can have a relatively high value. However its weight strongly depends on the effective gate voltage which can be relatively small. The effective gate voltage depends on the input signal level. Also the threshold voltage is not constant and depends on the source-to-bulk voltage, then on input signal level. The effect of those two items can be observed in Figure 3.6(b), in which, the inverse current is shown. Immediately after the gate voltage begins to fall, the sampling capacitor inverse current increases suddenly and has a peak. It follows an initial period when the inverse current falls, then a second period when it is constant. It can be said that the change happens when the effective gate voltage is definitely null and all channel charges have been already removed. Also, it can be said that the charge injection acts during the initial period, and the clock feed-through during both periods. The different current slopes during the first period are result of the transition simulation between the strong and weak inversion operation. The low importance of the over-current during the first period is apparent as it is the item that is not constant, depending on the input signal level, then much more difficult to compensate. Increasing the switch size can increase the switch conductance but, on the other hand, it will increase proportionally the errors. This is clear in the charge injection and in the clock feed-through expressions, (3.12) and (3.15), as the gate-to-channel capacitance and the gate-to-source overlap capacitance increase too.

Several attempts are made to reduce, compensate or null these errors. One of the most common is the use of a dummy device, as illustrated in Figure 3.8. If a dummy is placed at the sampling capacitor side, with half the width and controlled by a complementary gate voltage of the one used in the main device, $\overline{v}_{Gn}$, the charge injection and feed-through effect will be reduced.

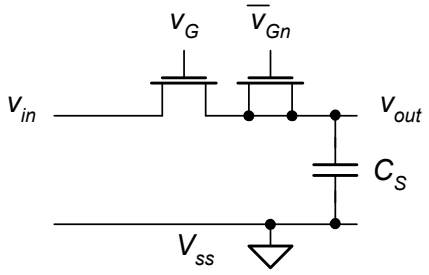


Figure 3.8: Dummy switch implementation.

In Figure 3.9(a) and (b) the simulated results can be seen, and it can be noticed the feed-through effect is immediately cleared during the switching-OFF period, and the charge injection is compensated at its end. The capacitor voltage recovers almost completely. However, it is not an easy task to generate, in practice, two precise complementary signals.

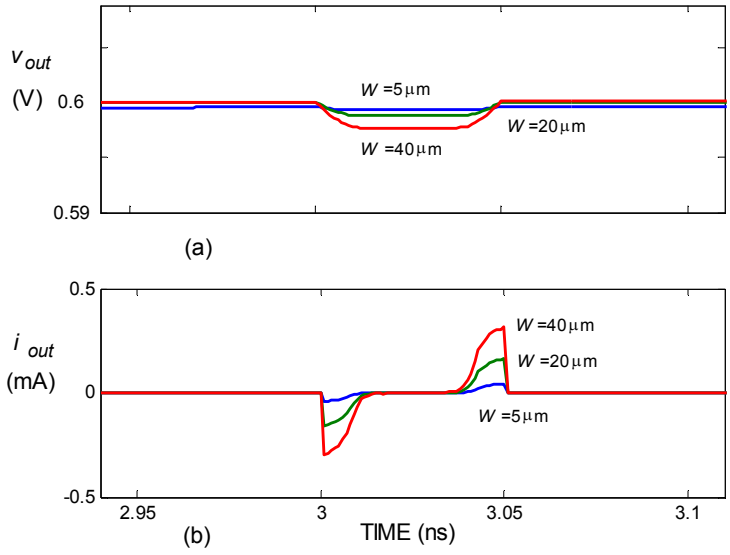


Figure 3.9: Switch turning-OFF period, with dummy switch; (a) Output voltage; (b) Output current.

If the complementary control voltage is advanced in time, the cancellation will not be adequate, as the charge injected by the dummy could escape through the main switch, still in the ON state. Accurate reduction is obtained if the applied dummy control voltage is an exact (or slightly delayed) inverted replication of the one applied to the main device [42][43].

A very common is the use of the bottom-plate sampling technique, illustrated in Figure 3.10 for a S/H circuit [44]. The charge injection will be reduced if the capacitor top-plate is connected by an NMOS device (M_2) to V_{SS} (or to any common-mode voltage). In fact, the source and drain voltages of this device, when ON, will be constant and close to V_{SS}, and then the charge injection will be mostly signal independent. On the other hand, if this device is switched OFF before the main device (M_1), the charge injection will be highly reduced, since the bottom-plate will be in high impedance.

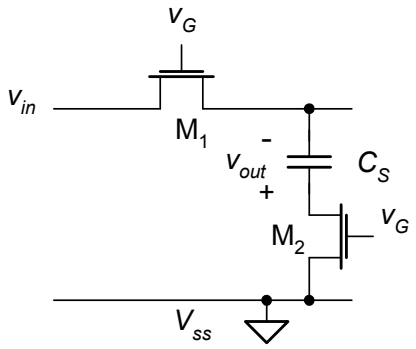


Figure 3.10: Bottom-plate sampling implementation in a S/H.

In Figure 3.11(a) and (b) simulated results are presented, for the same switches size used early. The capacitor voltage, v_{out}, and the capacitor current, i_{out}, are shown. Using two switches in series with the capacitor, the equivalent conductance will be lower and the charging time increased. To establish the same settling-time, both devices should be increased in size, then increasing the errors and the difficulty to cancel them. Comparing the results with those presented in Figure 3.6, the output voltage has a less significant variation, and the capacitor current has a reverse and significant value. However, the latter, due to the second switch turning-OFF, is mostly signal independent and can be corrected. Furthermore the capacitor current during the main switch switching-OFF, still presenting the feed-through effect, as the capacitor bottom-plate is in series with the second switch overlap capacitance, is cleared from the charge injection influence.

However, in more complex SC circuits, an adequate clocking scheme is able to provide a significant charge injection error reduction [45].

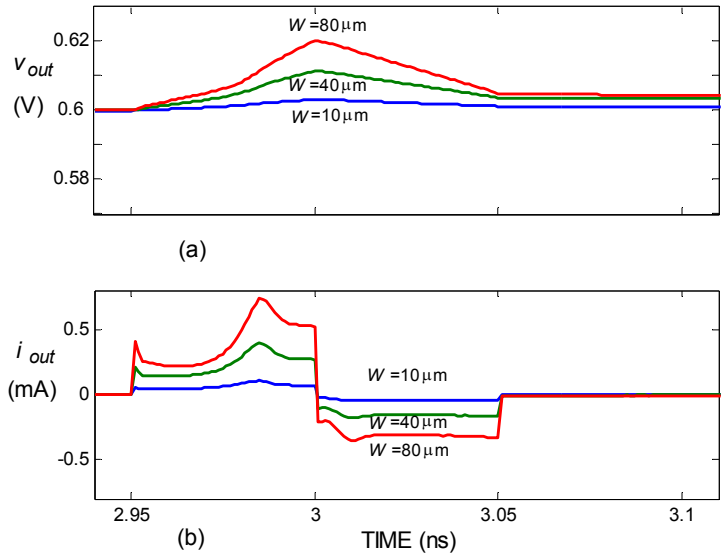


Figure 3.11: Switch turning-OFF period with bottom-plate sampling switch; (a) Output voltage; (b) Output current.

Another possible method of reducing the charge injection is switching-OFF the device in the saturation region, and assuring that it has the electrical drain, with no channel charges, at the sampling capacitor side [46].

Another possibility is the use of SC circuits designed in a way that the overall sampled voltages errors existing in the different sampling capacitors are reversed and then canceled out [47].

3.4. The switch gate driving voltage

The switch conductance improvement, achieved by the use of circuits generating higher voltage values than the supplied ones, is common. Voltage multiplier circuits can supply particular switch and amplifier blocks, or can feed only certain control nodes or gates. The use of a voltage multiplier is an instrument that allows the designer to implement low-voltage SC circuits. Feeding the blocks or controlling particular nodes with the necessary voltage level, the designer is able to extend the range of operation of the switches.

The use of voltage multipliers is more common and efficient when dealing with single switches, NMOS or PMOS, avoiding the need of complementary switches. But, usually, different control voltages or clocks are needed, delayed in time, forcing the use of one voltage multiplier *per* each switch or group of switches.

Also, another important issue is the fact that the tendency to reduce the supply voltage is tied to the switch dimension reduction, and, in particular, the reduction of the gate oxide thickness. From the reliability point-of-view, the voltage level, generated by the voltage multipliers and applied to the switches gate, must be bounded within the technology limits.

3.4.1. The Dickson multiplier

A Dickson multiplier [48] with two stages is represented in Figure 3.12. The operation is as follows. When the clock ϕ_{1n} is low, the first capacitor C is charged to a voltage close to $V_{DD} - V_D - V_{\phi min}$, being V_{DD} the nominal voltage supplied to circuit, V_D the diode voltage drop and $V_{\phi min}$ the minimum clock voltage or the voltage drop at the clock output stage. When ϕ_{1n} is high, close to $V_{DD} - V_{\phi min}$, and ϕ_1 goes down, to $V_{\phi min}$, the second capacitor C will be charged. After a few clock periods, and supposing for now that the output current is null, the output voltage v_{out} will be close to $3V_{DD} - 3V_D - 4V_{\phi min}$. In the Figure (3.12) is shown a possible load capacitor, C_L.

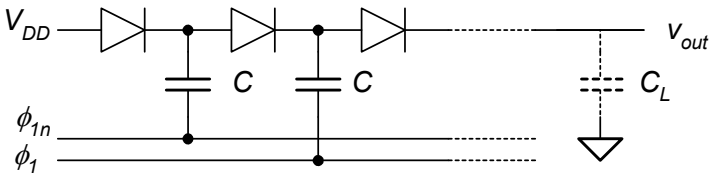


Figure 3.12: Dickson multiplier circuit [48].

If n_S represents the number of cascaded stages, the output voltage can be calculated by:

$$v_{out} = V_{DD} - V_D + n_S\left[\left(V_{DD} - 2V_{\phi\min}\right) - V_D\right] \qquad (3.19)$$

Or, in general:

$$v_{out} = v_{in} - V_D + n_S\left(\Delta V_\phi - V_D\right) \tag{3.20}$$

Being v_{in} the input voltage and ΔV_ϕ the clock voltage swing, respectively V_{DD} and $V_{DD} - 2V_{\phi min}$ in the previous example. If the output current, i_{out}, is not null, the output voltage will be lowered by an inherent ripple term, Δv_{out}, computing the partial voltage ripple in the capacitor of each stage, recharged at clock frequency, F_ϕ, in the form (3.21).

$$\Delta v_{out} = \frac{n_S}{F_\phi C} i_{out} \tag{3.21}$$

Thus, an equivalent dynamic series resistance of the global voltage multiplier, R_S, can be expressed by:

$$R_S = \frac{n_S}{F_\phi C} \tag{3.22}$$

The useful power, P_U, is the product of v_{out} by i_{out}. The total dissipation power, P_D, is the sum of the power lost in the diodes plus the power lost in the equivalent series resistance. A value of the voltage multiplier efficiency can be the ratio of the lost power and the useful power, indicated in following forms:

$$\frac{P_D}{P_U} = \frac{\left(n_s + 1\right)V_D i_{out} + R_S i_{out}^2}{v_{out} i_{out}} \tag{3.23}$$

$$\frac{P_D}{P_U} = \frac{\left(n_S + 1\right)V_D + R_S i_{out}}{v_{out}} \tag{3.24}$$

$$\frac{P_D}{P_U} = \frac{\left(n_S + 1\right)V_D + \Delta v_{out}}{v_{out}} \tag{3.25}$$

In general, the efficiency can be expressed in form (3.26).

$$\frac{P_U}{P_U + P_D} = \frac{v_{out}}{v_{out} + (n_S + 1)V_D + \Delta v_{out}} \tag{3.26}$$

Thus, the voltage multiplier with large capacitors, high operation frequency and small number of stages, will have low resistance, low ripple and high efficiency.

In low-voltage applications the multiplier became inefficient due to the relative importance revealed by the diode voltage drop. Each stage only pushes up the voltage a fraction of the input voltage. To double a 1.2 V voltage supply it will be necessary three stages, and to double a 1 V voltage supply, four stages. A higher number of stages will reduce the efficiency.

3.4.2. The voltage doubler

Replacing the diodes by NMOS devices, turned ON by a crossed bootstrap effect, the well know voltage doubler or charge pump (CP) circuit shown in Figure 3.13 is obtained.

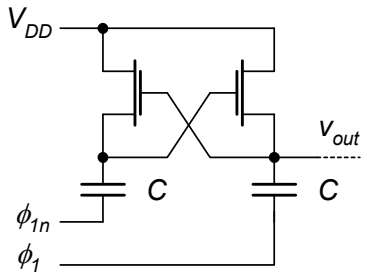


Figure 3.13: Voltage doubler circuit.

When ϕ_1 is high, the switch on the left side is ON and can charge the capacitor connected to its source. When ϕ_{1n} is high, the capacitor on the right side is charged. During the next half period, being ϕ_1 high again, the output voltage will be pushed towards V_{DD}, close to $V_{DD} - v_{DS} + \Delta V_\phi$, being v_{DS} the voltage drop at the NMOS and ΔV_ϕ again the clock voltage swing. During the next half period the same happens with the voltage on the source of the other switch. Thus, v_{out} can provide a double voltage value during ϕ_1, useful to trigger a required device (switch). If a continuous doubled voltage is required, the voltages present in both

sources can be added by means of diodes or alternate triggered switches, PMOS devices for instance.

The efficiency, neglecting the drain-to-source voltage drop on the switches, and then the lost power on them, can be calculated as in (3.27).

$$\frac{P_U}{P_U + P_L} = \frac{v_{out}}{v_{out} + \frac{2}{F_\phi C} i_{out}} \tag{3.27}$$

3.5. The basic NMOS switch

The drain-to-source conductance of an NMOS device, g_{DSn}, can be expressed by equation (3.28), being the device in the linear region of operation, $KP_n = \mu_n C_{ox}$ represents the mobility constant (provided by the foundry and given in AV^{-2} dimensions), W_n the width, v_{GSn} the gate-to-source voltage, and V_{TOn} the threshold voltage with zero bulk-to-source biasing.

$$g_{DSn} = KP_n \frac{W_n}{L}\left(v_{GSn} - V_{TOn}\right) \tag{3.28}$$

For the PMOS device the equation is similar, being the mobility constant three or four times lower, due to a lower mobility of the holes. As the threshold voltage for the PMOS case is similar to the NMOS case, it is clear that the first choice to obtain a better switch conductance is to use an NMOS.

3.5.1. The threshold voltage

If a gate voltage, v_{Gn}, is applied to the gate with reference to V_{SS}, and the source voltage is close the input signal, v_{in}, equation (3.29) is obtained.

$$g_{DSn} = KP_n \frac{W_n}{L}\left(v_{Gn} - v_{in} - V_{TOn}\right) \tag{3.29}$$

The threshold voltage with zero biasing is a parameter defined by the semiconductor physics and independent on the applied voltages. However, if the bulk-to-source voltage, v_{BS}, is not null and is negative, the charge in the depletion layer increases and the threshold voltage also increases. The actual threshold voltage, V_{Tn}, becomes a function of the source voltage, of the body factor, γ_n, and of the surface potential, $2|\Phi_F|$, respectively parameters GAMMA and PHI in circuit simulator SPICE, as in equation [39] (3.30).

$$V_{Tn} = V_{TOn} + \gamma_n\left(\sqrt{2|\Phi_{Fn}| - v_{BSn}} - \sqrt{2|\Phi_{Fn}|}\right) \qquad (3.30)$$

The body factor replicates the relation between the gate-to-channel and the bulk-to-channel capacitances, called the device controlling capacitances. Implicitly, it reflects the difference of the oxide and of the silicon dielectric constant, and also the difference between the oxide layer and the depletion layer thicknesses. The equation (3.29) can be changed into (3.31).

$$g_{DSn} = KP_n \frac{W_n}{L}\left[v_{Gn} - v_{in} - V_{TOn} - \gamma_n\left(\sqrt{2|\Phi_{Fn}| - v_{BSn}} - \sqrt{2|\Phi_{Fn}|}\right)\right] \qquad (3.31)$$

Replacing $-v_{BSn}$ by $v_{SBn} = v_{in}$, equation (3.32) is obtained.

$$g_{DSn} = KP_n \frac{W_n}{L}\left[v_{Gn} - v_{in} - V_{TOn} - \gamma_n\left(\sqrt{2|\Phi_{Fn}| + v_{in}} - \sqrt{2|\Phi_{Fn}|}\right)\right] \qquad (3.32)$$

Simulating the initial single circuit depicted in Figure 3.1, for three different device sizes, applying a constant v_{Gn} = 1.2 V voltage to the gate, and applying a ramp voltage v_{in} in the input, from 0 V to 1.2 V in 4 ns, the evolution of the conductance expressed by equation (3.32) can be displayed. Figure 3.14(a) shows that the conductances are proportional to the device size, the three values having the same knee point when the threshold voltage is reached. Also the conductance slope value is not constant. It increases in absolute value as the input voltage increases. This is clear in equation (3.32) as the input voltage affects the body factor influence on the effective gate voltage.

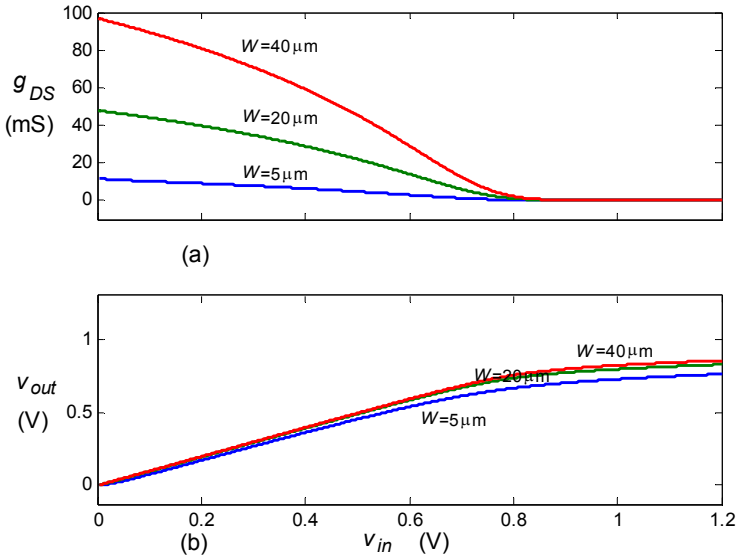


Figure 3.14: Changing the aspect ratio; (a) Conductance; (b) Output voltage.

In Figure 3.14(b) the output voltages are shown. The smallest device is not able to provide an output voltage following the input variation in such a short time. The devices with bigger width have a much better response. However, that improvement is not linear as regards the conductance and device size. It has an exponential evolution as shown in equation (3.4). Even so, all of them are not able to conduct for high input signal levels. In the previous simulated circuits, the input signal variation is up limited, *i.e.* $v_{in} < V_{DD} - V_{Tn}$.

3.6. The basic PMOS switch

The PMOS device behavior is similar and its analysis is relatively straightforward. Although the transconductance parameter is three or four times lower compared to the NMOS device, in a CMOS layout the PMOS devices are placed in a separate and floating well (n-type), and then allowing, in a standard way, the availability of the bulk as a useful terminal. That possibility can bring up some benefits, making the PMOS based S/H circuits fairly competitors of those based on NMOS devices. If a gate voltage, v_{Gp}, is applied to the gate with reference to V_{SS}, and the source voltage is close the input signal, v_{in}, the conductance can be described by equation (3.33), similar to the one obtained for the NMOS case, equation (3.29).

$$g_{DSp} = KP_p \frac{W_p}{L}\left(v_{in} - v_{Gp} - \left|V_{TOp}\right|\right) \tag{3.33}$$

However, if the bulk-to-source voltage, v_{BSp}, is not null and is positive, the charge in the depletion layer increases and the threshold voltage increases too, in absolute value. The actual threshold voltage, V_{Tp}, is a function of the source voltage, of the body factor, γ_p, and of the surface potential, $2|\Phi_{Fp}|$, as in equation (3.34).

$$\left|V_{Tp}\right| = \left|V_{TOp}\right| + \gamma_p\left(\sqrt{2\left|\Phi_{Fp}\right| + v_{BSp}} - \sqrt{2\left|\Phi_{Fp}\right|}\right) \tag{3.34}$$

If the bulk is connect to V_{DD}, the bulk-to-source voltage will be $v_{BS} = V_{DD} - v_{in}$, and the function can be rearranged as (3.35), similar to the equation (3.32) for the NMOS case.

$$g_{DSp} = KP_p \frac{W_p}{L}\left[v_{in} - v_{Gp} - \left|V_{TOp}\right| - \gamma_p\left(\sqrt{2\left|\Phi_{Fp}\right| + \left(V_{DD} - v_{in}\right)} - \sqrt{2\left|\Phi_{Fp}\right|}\right)\right] \tag{3.35}$$

The sampling capacitor voltage errors can also be described, in the same way as for the NMOS case by equation (3.18), by equation (3.36).

$$\varepsilon_{chi} + \varepsilon_{clkf} = \frac{c_r(h+1)C_{GCp}\left(v_{in} - V_{\phi\,min} - \left|V_{TOp}\right|\right)}{C_S} + \frac{C_{GSOp}\Delta V_\phi}{C_{GSOp} + C_S} \tag{3.36}$$

3.6.1. The bulk-switching technique

The body effect can be reduced or zeroed if the bulk-to-source voltage has a reduced or null value. The application of the bulk-switching technique (BS) [49], can be clarified making use of Figure 3.15. When ϕ_1 is active, the main switch M_1 is ON, and the bulk (n-well) is connected to its source by auxiliary transistors M_2 and M_3. This reduces greatly the bulk-to-source voltage. In the OFF state the bulk is then connected to V_{DD}, through the PMOS transistor M_4 controlled by a non-overlapped clock signal, ϕ_{2n}, reassuring the main device the OFF state resistance due to the increased threshold voltage.

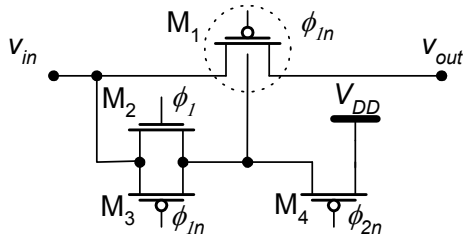


Figure 3.15: Bulk-switching circuit applied to M_1.

This simple technique has been already successfully used in 12-bit analog-to-digital converters (ADC) [50]. However, as shown by measured results, when using this technique the dynamic performance is highly degraded for high frequency input signals. Moreover, the MOS switch is bidirectional and symmetric. The source and the drain terminals may interchange depending on the input signal and on the previous sampled voltage, and then the BS technique loose efficiency and latch-up problems may occur [51].

3.7. The complementary MOS switch (transmission gate)

The utilization of the NMOS device, controlled by means of a gate voltage swinging between the supply levels, is only possible for $v_{in} < V_{DD} - V_{Tn}$. The utilization of the PMOS device is possible for $v_{in} > |V_{Tp}|$. A complementary MOS switch, CMOS switch or transmission gate (TG), allows a rail-to-rail signal swing.

3.7.1. Equivalent conductance of a CMOS switch

If m is the ratio of the mobility factor, such as $KP_p = mKP_n$, and using a size that $W_p = mW_n$, the equivalent CMOS switch conductance, g_{EQ}, can be obtained approximately by adding the two individual conductances, (3.29) and (3.33), resulting in form (3.37).

$$g_{EQ} = KP_n \frac{W_n}{L}\left(V_{DD} - V_{Tn} - \left|V_{Tp}\right|\right) \qquad (3.37)$$

A first approach shows that, as far as the supply voltage has a value $V_{DD} > V_{Tn} + |V_{Tp}|$, the CMOS switch can be used for sampling. It can also be understood, in a preliminary analysis,

that the CMOS switch conductance is free from the input signal voltage influence, adversely to the individual switches conductance. However, that only applies if both switches are ON, *i.e.* $V_{Tn} < v_{in} < V_{DD} - |V_{Tp}|$. Even then, the body effect will be present through the threshold voltages.

The circuit shown in Figure 3.16 is simulated, with $W_n = 5$ µm, $W_p = 20$ µm, $v_{Gn} = 1.2$ V, $v_{Gp} = 0$ V, $C_S = 1$ pF. A ramp voltage v_{in}, from 0 V to 1.2 V in 4 ns, is applied.

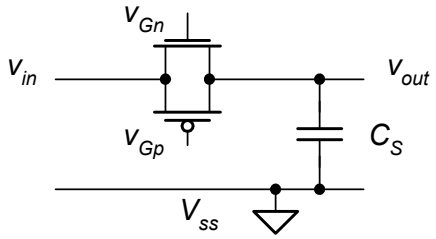


Figure 3.16: Sampling circuit with a CMOS switch.

The simulated individual conductances and the equivalent conductance are displayed in Figure 3.17(a), and in Figure 3.17(b) the output voltage is shown.

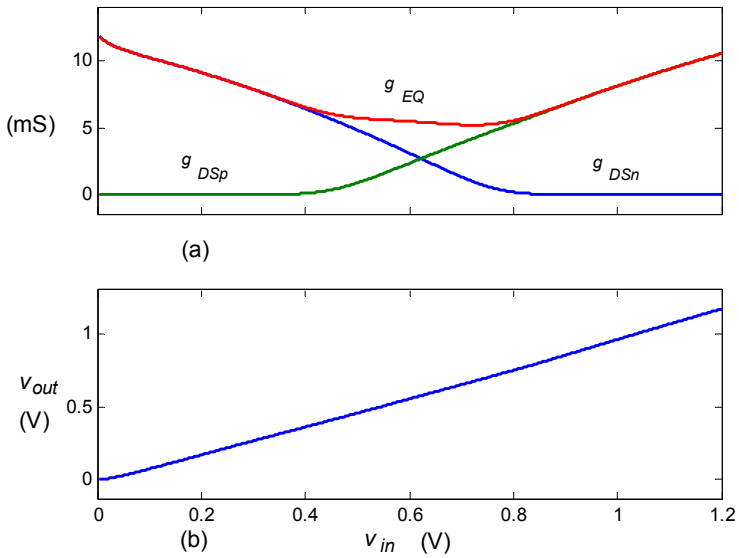


Figure 3.17: (a) Individual and equivalent conductances of a CMOS switch; (b) Output voltage.

Comparing these results with the simulated results shown in Figure 3.14, it is clear that the CMOS switch can charge the capacitor with a sampled voltage close to the input voltage, along the whole ramp.

It can be also noticed that the conductance has a lower value in the middle of the ramp. It is there that the switch will be less effective, when in ON state, and this effect tends to be even more problematic in deeper submicron CMOS technologies.

Connecting the PMOS bulk to the source, the simulated results are displayed in Figure 3.18(a). The PMOS switch threshold voltage has decreased, and its conductance has increased, mostly for low input voltage values. Thus, the CMOS switch conductance has increased as well. Figure 3.18(b) shows a zoom of the output voltage for this case, with PMOS bulk connected to the source, and for the previous case, the bulk connected to V_{DD}.

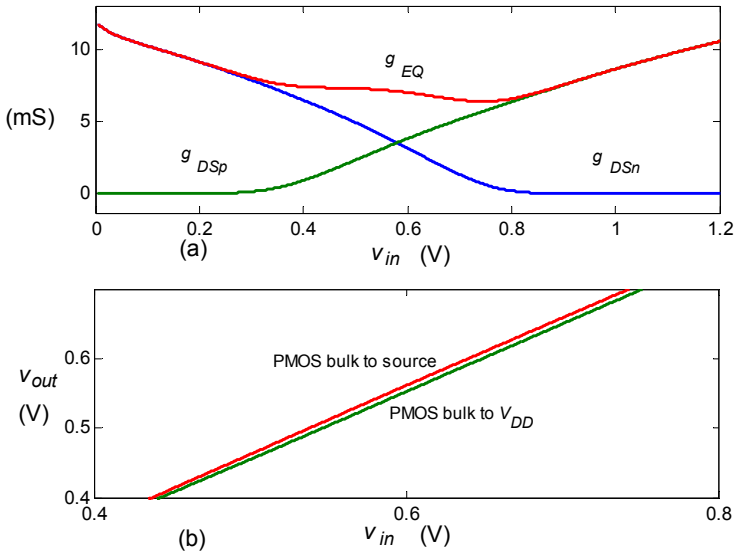


Figure 3.18: (a) Singular and equivalent conductances with a CMOS switch with bulk tied to source; (b) Output voltage comparison.

An error is evident in both voltages, but the one obtained with the bulk connected to the source is lower. It is in the middle of the input signal level that this difference is more relevant as shown also by the conductance curves.

3.7.2. Charge injection and clock feed-through of CMOS switches

Recalling functions (3.18) and (3.36), and for $\Delta V_\phi = V_{\phi max} = V_{DD}$, the clock feed-through and charge injection errors [52] can be expressed by equation (3.38).

$$\varepsilon_{chi} + \varepsilon_{clkf} = \frac{c_r(h+1)C_{GCn}\left[(m+1)v_{in} + V_{Tn} - V_{DD} - m|V_{Tp}|\right]}{C_S} + \\ + V_{DD}C_{GSOn}\left(\frac{m}{mC_{GSOn} + C_S} - \frac{1}{C_{GSOn} + C_S}\right) \qquad (3.38)$$

The first entry is signal dependent, not only directly, but also via the threshold voltages dependency. As the input voltage increases, the first entry, representing mostly the charge injection effect, also increases. The clock feed-through, mainly represented by the second entry, remains constant, and it is null if $m = 1$, *i.e.* if equal sizes are used.

Simulating the same electrical schematic illustrated in Figure 3.16, now with a pulse voltage v_{Gn} = 1.2 V, with 50 ps rise and fall time, at 1 ns and 3 ns respectively, with its complementary signal applied to v_{Gp}, for a constant input v_{in} = 0.6 V, the errors can be put in evidence through Figure 3.19. Two cases have been simulated, one with the switch widths W_n = 5 μm and W_p = 20 μm, and other with $W_n = W_p$ = 5 μm.

The Figure 3.19(a), shows the output voltage when switching-OFF the CMOS switch, and Figure 3.19(b) shows the capacitor current, evidencing a dramatic error reduction in the second case. This is implicit in function (3.38), for $m = 1$, with a minimized charge injection and a quite null clock feed-through effect. Also as predicted by the same function, the voltage variation is positive, due to the PMOS influence.

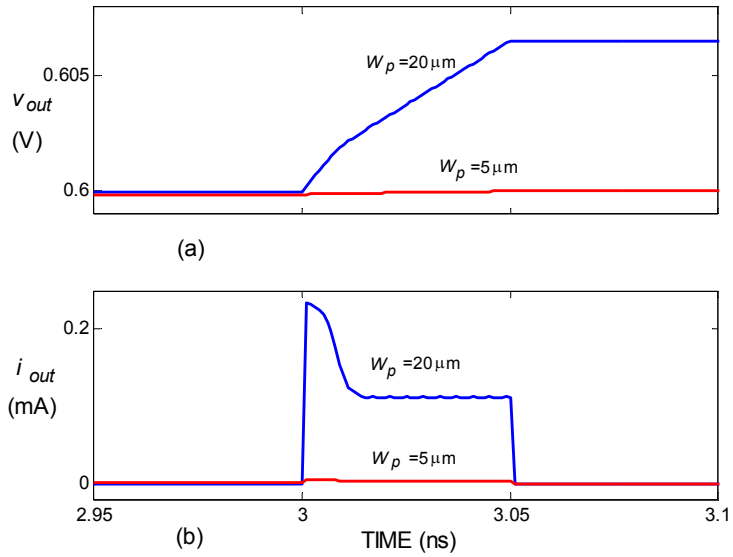


Figure 3.19: Symmetric and non-symmetric CMOS; (a) Output voltage error; (b) Injected output current.

The same circuit is simulated, maintaining $W_n = W_p = 5$ µm, now with a lower input signal, v_{in} = 0.3 V, being the simulated results shown in Figure 3.20(a) and (b). Comparing these results with the previous results for the same switch widths, it can be noticed that the output voltage has a negative error due to the input level reduction, as explicit by the equation (3.38) first term.

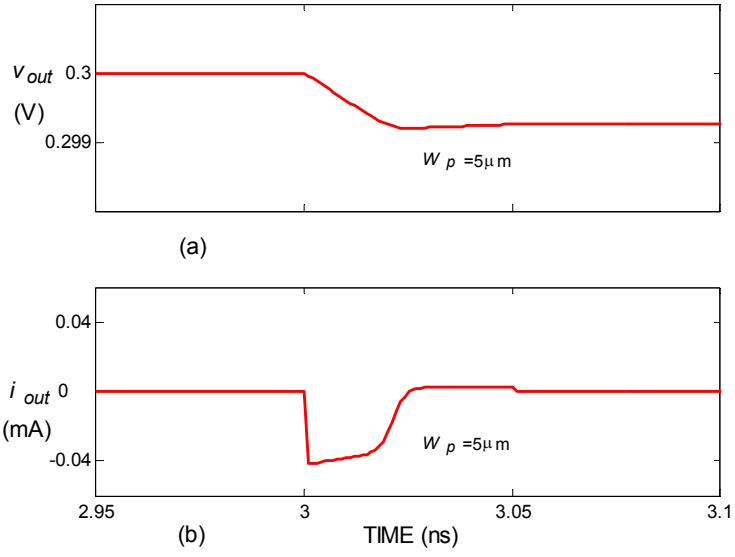


Figure 3.20: CMOS with small input voltage; (a) Output voltage error; (b) Injected current.

The CMOS switch can be controlled by clock signals between the absolute supply voltage limits. No charge pumps or voltage multipliers are needed, no over voltage is applied.

Even allowing a rail-to-rail operation, the conductance is signal dependent, with a wide variation. For input voltages close to half the supply voltage, still quite constant, the existing conductance value is low. It is in that range that the real signals have a faster variation, and then particular attention should be taken by the designers. Proposals are made to increase the conductance by a moderate overdrive in the effective gate voltages [53].

The charge injection is present and is signal dependent, but is hugely reduced if the switches have equal sizes. However, in this case, the conductance would be reduced and unbalanced.

3.8. Using reduced threshold devices (low-V_T devices)

The threshold level has been always taken into account, more now, due to the ongoing lower voltage. The technology trend has decreased much more rapidly the supply voltage than the threshold voltage. This is achieved, during device optimization, by increasing the channel doping as the oxide is scaled, therefore maintaining approximately the same device threshold voltage.

The main reason is to keep low the sub-threshold leakage, and limiting the circuit standby power. The sub-threshold leakage is of the major importance on the MOS devices operation, and is set by the threshold voltage. Even the threshold voltage has been reduced slower than the supply voltage, the standby power and active power ratio has increased hugely. In order to limit this increased standby power, the threshold voltage lowering is being limited or stopped. However, this strongly affects the device performance because of the reduced gate overdrive. The transistor drive current, and therefore the circuit performance, is a function of the gate overdrive. A general rule is to maintain the V_{DD} and V_{TO} ratio of at least four. This provides a gate swing of one V_{TO} to turn the device OFF, and three to drive the device. The current tendency is to drop the ratio below four.

One possibility to overcome this is to offer circuit designers the low-threshold devices (low-V_T), also called natural devices, which can be implemented if the threshold adjust implant process is not applied. Other possibility is, with a non-standard technology, offering the dual

threshold voltage devices. This would consist of making available a high-performance, high-leakage, low-threshold voltage device and, simultaneously, offering a low-performance, low-leakage, high-threshold voltage device. The designer will have the possibility to use the high-performance, high-leakage devices in the critical paths.

For very low supply voltage operation, the dynamic threshold voltage MOS device (DTMOS) can be an option. The DTMOS is implemented by connecting the gate to the well, causing the threshold voltage of the device to be lowered during switching-ON and, thereby, increasing the transistor current. This technique is limited to the supply voltages lower than one junction voltage, to avoid the forward bias of the well-to-source junction from conducting significant forward bias diode currents. This technique can increase transistor current through improved gate overdrive, but will lower the performance, due to the increase in the switching load capacitance, by increasing the junction and depletion capacitances.

The natural and dynamic threshold devices are out of the scope of this Thesis, since, we are focused on proposing solutions based on standard V_T devices.

3.9. Conclusions

The switches non-ideality is the major problem present in low-voltage implementations of SC circuits. The performance of the circuits is compromised and depends heavily on the switches nonlinearities. In this Chapter the switches conductance, the charge injection, the clock feed-through and other sources of error, have been analyzed and discussed. Some modes to improve the switches conductance value have been proposed, such as the device up-scaling, the increasing of the gate voltage and the lowering of the threshold voltage.

4. Additional challenges in the design of SC circuits in advanced CMOS technologies: amplifiers and phase complexity

Technology scaling is rising many issues for analog circuit design, such as intrinsic device gain, supply voltage and device variability. In particular, for switched-capacitor (SC) realizations, the referred performance degradations are increasing the difficulty to realize accurate charge transfers in the traditional manner, *i. e.*, based on closed-loop operational amplifier (OpAmp) structures. Different approaches have been recently proposed to deal with the referred issues, namely, open-loop amplification.

The sequential stages from a pipelined converter are operating alternatively, controlled in a precise and synchronous way by the clock signals. Efforts to undertake charge conservation during the switching processes, and to guarantee simultaneously reduced settling-times, usually makes it necessary to use of several clock signals in addition to the main ones, some of them advanced, some others delayed. Then, the complexity of the clock phase generation increases as well as its practical implementation in terms of layout.

4.1. Introduction

Time-domain SC circuits involve mainly three functions: sampling, amplification by a given factor and comparison with a given threshold reference. Depending on the implemented circuit architecture, the different blocks taking care of those functions have different priority requirements and specifications. At the present, not only the low-voltage supply, but also the low-power dissipation is a common requirement to all blocks and circuit architectures. Therefore, the use of simple and power efficient circuits is mandatory.

The OpAmps are common circuits used for the role of different functions, such as sampling or amplification. The control or phase signals are also delivered to the all blocks. In this Chapter, the use of the amplifiers, enabling the two main functions, sampling and amplification, are described and analyzed. Different and simpler architecture solutions for the sample-and-hold (S/H), for multiply-by-two amplifier (MBTA) and for multiplying digital-to-analog converter (MDAC) blocks are explored and suggested, since they are the main key building blocks of, for example, high-speed analog-to-digital (A/D) conversion architectures based on a residue amplification scheme, *e.g.* two-step flash and pipelined A/D converters (ADCs). Also, the complex control signals, necessary to provide the adequate operation of the different switches in a SC circuit, are investigated and analyzed in detail.

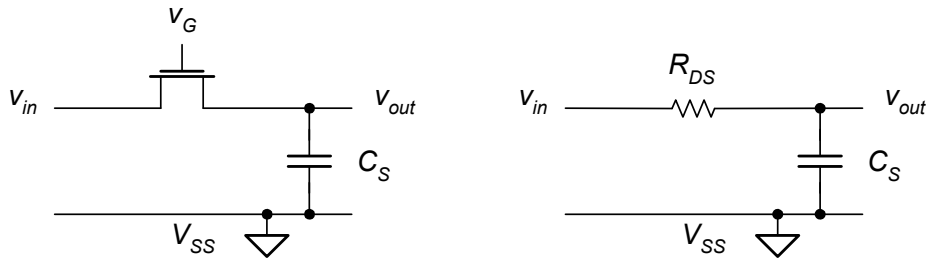
4.2. Passive and active, closed-loop and open-loop structures in low/medium accuracy SC circuits

As stated before, S/Hs, MBTAs and MDACs are key elements in most A/D architectures, such as, algorithmic, two-step or pipelined. OpAmps and operational transconductance amplifiers (OTAs), herein simply referred as amplifiers, are used to provide a virtual ground during the hold/amplification. The intrinsic nonlinearity of the amplifiers, together with the needed greater and greater sampling rate, requires changes in architecture solutions, now enabled by technology evolution towards deep sub-micron processes.

4.2.1. Active and passive S/H circuits

The function of the S/H circuit is to track and sample an analog input, during a sampling period of time (normally half clock-cycle) and at a precise moment, and afterwards to hold the corresponding value during the holding period (another half clock-cycle), so that the next circuits are able to operate with it, already in a discrete-time mode. For sampling purposes, the circuit comprises usually of one single switch and one sampling capacitor where the input signal is stored. The importance of the performance of the switch has already been, and will be again, discussed throughout this Thesis.

Figure 4.1(a) represents a simple sampling circuit. When the switch is ON, as depicted in Figure 4.1(b) through its equivalent resistance drain-to-source, R_{DS}, the sampling capacitor, C_S, is charged.



(a) (b)

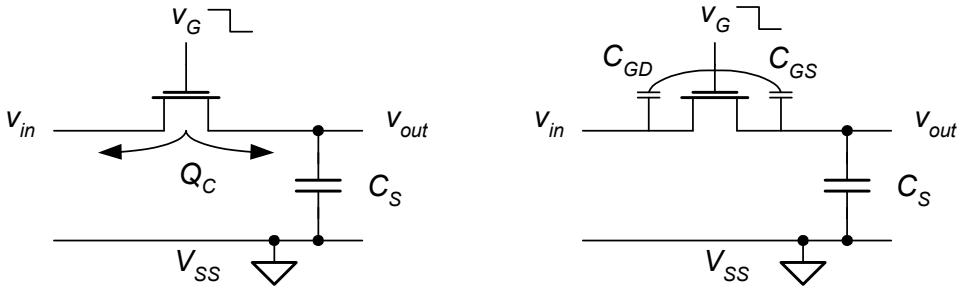
Figure 4.1: Sampling circuit; (a) Diagram with NMOS device; (b) Equivalent charging circuit.

The corner frequency of that circuit can be expressed as in (4.1).

$$\omega_{-3dB} = \frac{1}{R_{DS}C_S} = \frac{g_{DS}}{C_S} \tag{4.1}$$

The signal bandwidth (BW) is, therefore, limited. It can be enlarged, by increasing the switch conductance. The switch conductance is a function of the aspect ratio and of the effective gate voltage, as discussed previously. Another source of error is due to the charge injection phenomena. When the switch is ON, there is a channel charge, Q_C, whose value is a function of the gate-to-channel capacitance and of the applied voltages. When the switch turns OFF, as

illustrated in Figure 4.2(a), part of that charge is going to affect the sampling capacitor. Some schemes are widely used to minimize that effect, by the addition of a dummy switch half its size, to the introduction of a capacitor top-plate switch that turns OFF before the main sampling switch, which is connected to the bottom-plate of the capacitor. The parasitic capacitance between the gate and source also introduces a feed-through error, function of the capacitances values and of the gate voltage swing, as depicted in Figure 4.2(b). The use of differential topologies minimizes this error.



(a) (b)

Figure 4.2: Sampling circuit during device turn-off; (a) Charge injection; (b) Presence of parasitic capacitance.

Another important problem that has to be taken into account is related with the resistance of the switch which adds thermal noise to the sampled output signal. However, the total noise variance, σ^2, found by the integration of the noise spectral density overall frequencies, is a function of the capacitance value, and independent of the switch resistance, as expressed in (4.2), with k the Boltzmann constant and T the absolute temperature.

$$\sigma^2 = \frac{kT}{C_s} \tag{4.2}$$

Therefore, there is always a limitation to the achievable signal-to-noise ratio (SNR), for a certain capacitor value. This implies the use of a larger capacitor value, and power dissipation, when higher SNR values are required.

To perform the holding process, the S/H circuit uses also switches, and buffers or amplifiers, to limit the signal degradation. One example of an S/H block is shown in Figure 4.3. During phase ϕ_1, the sampling capacitors are connected between the differential inputs and the OpAmp inputs. Also during phase ϕ_1 the inputs and the outputs of the OpAmp are tied

together[4]. Apart from the offset voltage, V_{offset}, the capacitors are charged during this sampling period, with the differential input voltage, $v_{id} = v_{inp} - v_{inn}$.

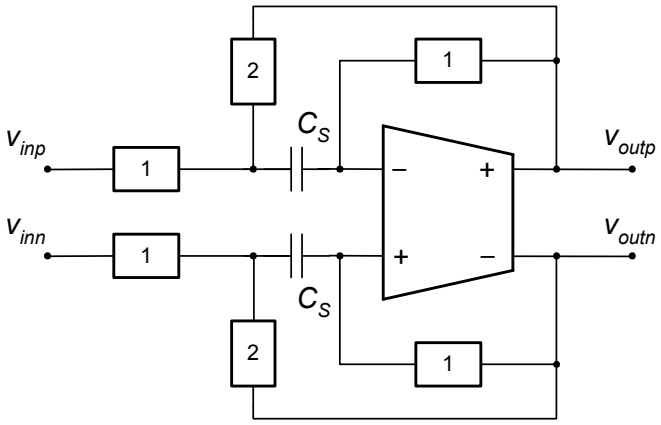


Figure 4.3: Flip-around S/H circuit.

During the holding phase, ϕ_2, the capacitors C_S are connected to the OpAmp outputs, and flipped around the amplifier. Due to the closed-loop configuration, the charge stored during the sampling phase is maintained. The differential output voltage, $v_{od} = v_{outp} - v_{outn}$, is kept approximately equal to the differential input voltage, v_{id}, if the OpAmp open-loop gain, A, is large enough, as shown in function (4.3).

$$V_{od} = V_{id}\left(\frac{1}{1+1/A}\right)+\left(\frac{V_{offset}/A}{1+1/A}\right) \tag{4.3}$$

Another source of error is the parasitic capacitor, C_P, at the amplifier input node. The differential output voltage suffers attenuation as expressed by (4.4).

$$V_{od} = V_{id}\left(\frac{1}{1+(C_S+C_P)/C_S A}\right) \tag{4.4}$$

Since the feedback factor is high, nearly equal to unity, the sampling frequency can be high, close to the unity gain frequency of the amplifier. This topology does not provide real gain, however, it uses only one capacitor in each path, avoiding the possibility of any capacitors mismatch, therefore is simple and widely used.

[4] A more commonly used circuit consists of shorting the inputs and the outputs of the OpAmp using two switches and keeping it in open-loop during ϕ_1. The advantage is that the noise of the amplifier is not sampled during ϕ_1 but, the drawback is that the offset of the amplifier is not canceled out.

Another possible configuration of a S/H block is shown in Figure 4.4, using doubled sampling. The sampling capacitor in the previous circuit, takes the place of C_F in the actual circuit. A new capacitor, C_S, is added, for sampling too, and also for charge redistribution. Both capacitors sample the input signal during phase ϕ_1. During phase ϕ_2 the charge is redistributed, *i.e.* is passed to C_F. As C_F is already charged, there is always a gain factor, being the minimum limit value equal to one.

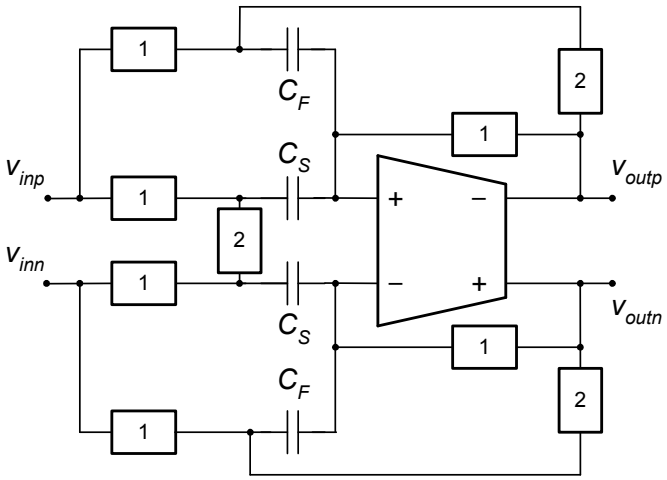


Figure 4.4: Double sampling S/H circuit.

The gain is always higher than unity, and the feedback factor in the hold phase is lower relatively to the previous circuit (about one half). The output voltage is a function of the capacitors ratio, as expressed in (4.5). When C_S is nominally equal to C_F this circuit can also be used as a MBTA circuit.

$$V_{od} = V_{id}\left(1+\frac{C_S}{C_F}\right)\left(\frac{1}{1+(C_S+C_F+C_P)/C_F A}\right) \qquad (4.5)$$

Another S/H topology [54] is shown in Figure 4.5, using charge distribution after single sampling. During phase ϕ_1 the input signal is sampled into capacitors C_S, apart from common mode voltage, V_{CMI}, and the feedback capacitors, C_F, are reset. During phase ϕ_2, the charge is transferred into the feedback capacitors, now in the feedback path. This topology is commonly named as an integrating-type S/H.

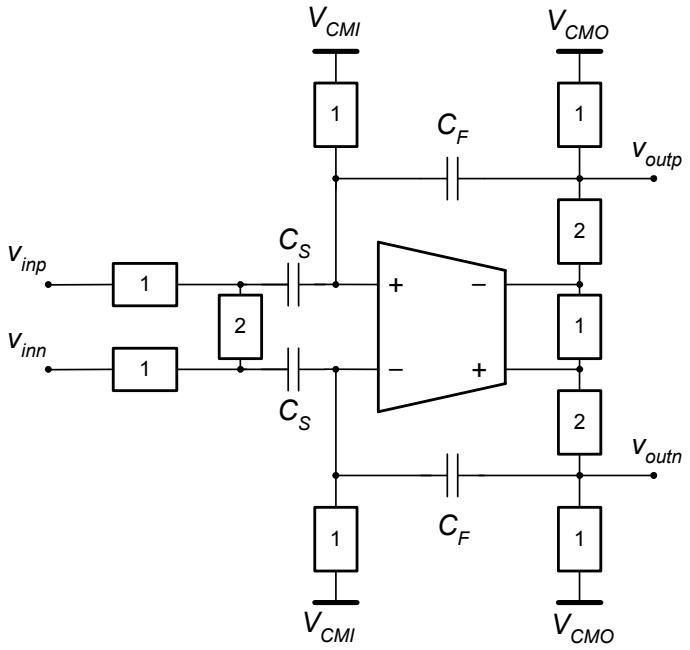


Figure 4.5: Charge redistribution S/H circuit.

The output voltage, v_{od}, is expressed as in function (4.6).

$$V_{od} = V_{id}\left(\frac{C_S}{C_F}\right)\left(\frac{1}{1+(C_S+C_F+C_P)/C_F A}\right) \tag{4.6}$$

The parasitic capacitance, C_P, has the contribution of the gate capacitance of the amplifier input transistor, and also of the capacitances of the switches connected to the node, all not signal independent. The finite value of the open-loop gain causes a voltage error in the circuit as a whole. As far as the open-loop gain of the amplifier is large enough, the introduced parasitic capacitance error is reduced.

Another source of error is the possible incomplete zeroing of the feedback capacitors. Irrespective of the previously hold charge value, the switches connected to the common mode voltages should be able to cancel it. For a large sampling rates that can be a challenge. The resetting switches cannot be oversized, as this will contribute to increase the parasitic capacitance value, and compromise the closed-loop gain and bandwidth.

Special attention should also be brought to the feedback switches, ON during hold phase, ϕ_2. Similar compromise, between conductance value and parasitic capacitance value, exists. Additionally, the conductance values, together with the capacitances values, namely from C_F,

create a increased stability difficulty, resulting in an output slow settling behavior. By placing the switches in the forward path of the amplifier, taking the output voltage as $v_{od} = v_{outp} - v_{outn}$, instead of directly from the amplifier outputs, will reduce the error [54].

Another known problem and source of error is high input signal amplitudes are applied, affecting the biasing of the amplifier transistors. The amplifier gain is compromised for large output voltage swings.

The gain of this circuit can be adjusted but the feedback factor is lower than in the previous configuration. That implies better amplifier transconductance for the same operation frequency. If a gain of 2 is implemented, the feedback factor of this last circuit (Figure 4.5) is 1/3. For the same gain, the feedback factor of the double sample circuit (Figure 4.4) is 1/2. The corner frequency for the settling in the hold mode is related with the feedback factor, β, transconductance, g_m, and load capacitance, C_L, as expressed in (4.7).

$$\omega_{-3\,dB} = \frac{g_m}{C_L}\beta \qquad (4.7)$$

Then, the transconductance of the amplifier used in the double sample S/H circuit can be only 2/3 of the transconductance value of the one used in the simple charge redistribution circuit.

The S/Hs using feedback have been largely disseminated and implemented. In general, the linearity, as a requirement, has been the mandatory reason. But, towards higher and higher sampling rates other solutions came into discussion.

Some works have been proposing circuits with source follower passive S/H, and presenting their performance [55][56]. Avoiding the feedback and its compensation delay, and using a passive differential sampling, buffered by a linear source follower, a high sampling rate can be achieved, while maintaining high linearity. The major advantage is the reduction of the power dissipation value.

The SC circuits always present a dynamic power loss due to the voltage transition over the capacitor at a certain frequency. The power loss amount is proportional to that frequency. The dynamically lost power, P_D, in a sampling capacitor operating at frequency F_S, can be

expressed by (4.8), being ΔV the transit voltage amplitude. On the other hand, the power losses of an amplifier is proportional to the current, and the latter is proportional to the square of the transconductance. By increasing the frequency and bandwidth, the amplifier power loss increases more than the sampling capacitor loss.

$$P_D = C_S F_S \Delta V^2 \tag{4.8}$$

The circuit indicated in Figure 4.6 comprises a sampling switch, the sampling capacitor, C_S, and a source follower buffer, M_1. The bulk terminal is connected to the source, to remove the body effect, and the gain is close to the unit. The transistor M_2 is used as a current source, biasing M_1.

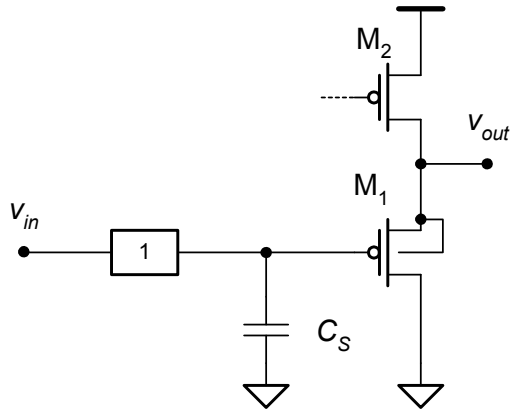


Figure 4.6: Passive S/H with source follower.

As the input voltage increases, the larger output signal will causes a variation of source drain voltage, then a third order distortion in differential schemes. Several works [57][58] show that the dynamic linearity of this circuit can be up to 9-to-10 bits for small signal amplitudes. This topology is used in 150 MS/s 8-bit A/D interleaved converters [59], with application in 1000BASE-T systems.

Introducing some major improvements, such as reducing the variation of the source-to-drain voltage, 11-bit with 800 MS/s can be achieved [60], with application in 10GBASE-T equipment. Figure 4.7 shows the used circuit, implemented with NMOS transistors.

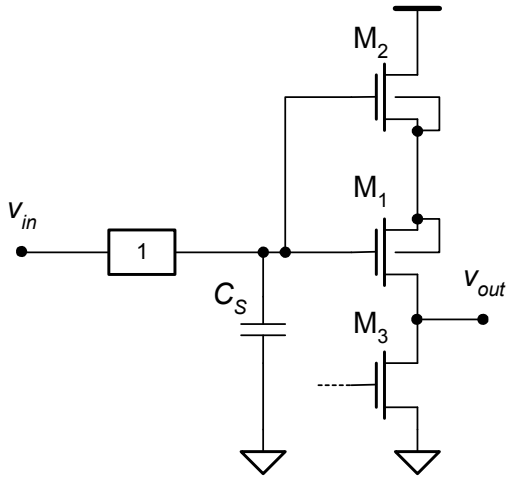


Figure 4.7: Passive S/H with improved (enhanced) source follower.

The M_2 transistor, acting as a cascode source follower, replicates the output signal at its source. The drain-to-source voltage of the main source follower transistor, M_1, is kept quite constant, thus suppressing the channel length modulation. Also, M_1 has its bulk connected to that duplicated output signal, eliminating the body effect. Additionally, being the parasitic diode capacitance of M_1 driven by M_2 instead of being by M_1 itself, the source transient response is improved. The major drawbacks are the need of triple-well technology (extra cost due to the additional masks) to allow the bulk connections, and the need of the threshold voltage of M_2 to be small enough to let the M_1 transistor work in the saturation region.

4.2.2. Closed-loop SC gain structures

As a practical example of using an MDAC circuit, the basic block of one 1.5-bit stage of a pipelined A/D converter is shown in Figure 4.8.

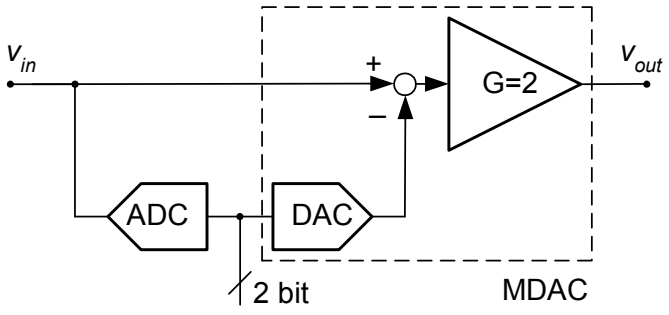


Figure 4.8: Pipelined converter stage.

The local ADC samples the input voltage, and quantizes it in a two bit code. The MDAC reconstructs that code into a voltage, which is subtracted from the sampled input voltage. The residue obtained is then amplified and delivered to the next stage as v_{out}.

One possible single-ended implementation is displayed with more detail in Figure 4.9. During phase ϕ_2, the input signal, v_{in}, is applied to the quantizer, with threshold values at $+V_{REF}/4$ and $-V_{REF}/4$. During the same phase, C_S and C_F are charged with a sampled value of v_{in}.

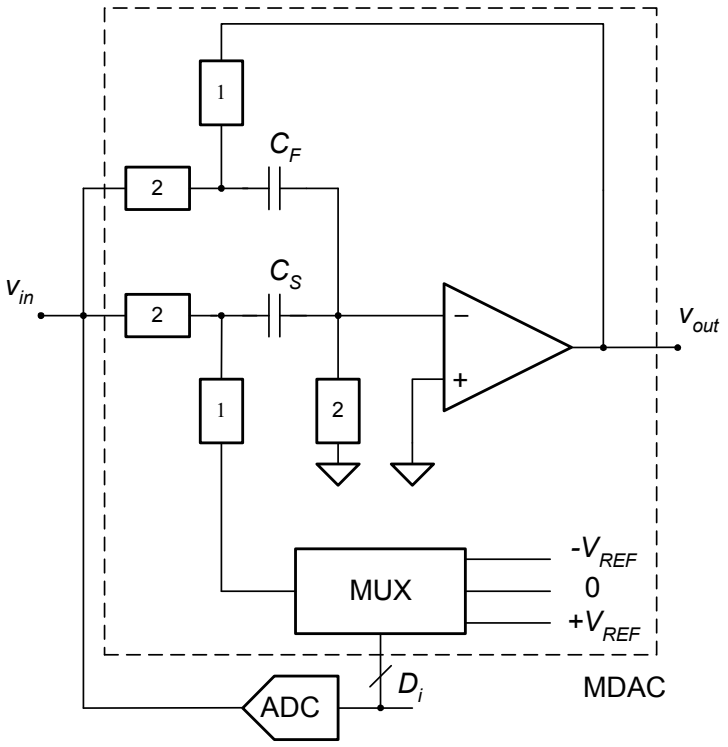


Figure 4.9: Detail of closed-loop stage switches.

During the next half clock period, ϕ_1, C_F establishes a feedback loop to the amplifier, and C_S is switched by an analog multiplexer to reference voltages, $+V_{REF}$, $-V_{REF}$ or 0, according to stored digital outputs of the local quantizer (ADC). These outputs are, for simplicity reasons, represented by the digital code D_i, with value "1" if the input signal is higher than $+V_{REF}/4$, "−1" if lower than $-V_{REF}/4$, and zero if in between. After charge redistribution, C_S is charged with $D_i V_{REF}$ and C_F with v_{out}. Due to charge conservation principle, equation (4.9) is obtained.

$$v_{out} = \frac{C_S + C_F}{C_F} v_{in} - \frac{C_S}{C_F} V_{REF} D_i \qquad (4.9)$$

If C_S value is nominally equal to the capacitance value of C_F, for this 1.5-bit stage case, the function can be reduced to the form (4.10).

$$V_{out} = 2V_{in} - V_{REF}D_i \tag{4.10}$$

However, considering the amplifier gain, A, not infinite, equation (4.9) changes into (4.11). The first term represents the attenuation due to the finite gain. The amplifier DC gain is given by the transconductance and output impedance product. The output impedance value, still high in the OTAs, is not infinite.

$$V_{out} = \frac{1}{1+\frac{1}{A}\frac{C_S+C_F}{C_F}}\left(2V_{in} - V_{REF}D_i\right) \tag{4.11}$$

If the parasitic capacitance, C_P, at the amplifier input is considered, the relative gain error, $\Delta G_{gain}/G$, introduced by finite gain is expressed approximately by function (4.12), where β represents the feedback factor.

$$\frac{\Delta G_{gain}}{G} \approx -\frac{1}{A}\frac{C_S+C_F+C_P}{C_F} \approx -\frac{1}{A\beta} \tag{4.12}$$

This feedback factor is approximately the inverse of the gain of the given stage, in general case with effective B bits, *i.e.* $\beta \approx 1/2^B$. The total error, ε_{tot}, reduced to the input, of an N-bit A/D converter with identical stages, can be expressed as in equation (4.13).

$$\varepsilon_{tot} = \frac{2^B}{A}\frac{1-\frac{1}{2^N}}{2^B-1} \tag{4.13}$$

The total error at the A/D converter input must be less than LSB/2, or as in form (4.14).

$$\varepsilon_{tot} < \frac{1}{2^N} \tag{4.14}$$

Combining (4.13) and (4.14), inequality (4.15) is obtained.

$$A > \frac{2^B\left(2^N - 1\right)}{2^B - 1} \approx \frac{2^{N+B}}{2^B - 1} \tag{4.15}$$

Another source of error is the capacitor mismatch. If capacitors C_S and C_F are not equal and differ by a mismatch error, the charge transferred, and the output voltage, are no longer a linear function of the input voltage (a gain error exists).

The third main source of error is due to the incorrect settling accuracy. The settling-time for a given settling accuracy is a function of the pole time constant, τ. The output voltage can be represented by an exponential function as in (4.16).

$$v_{out}(t) = \left(1 - e^{-\frac{t}{\tau}}\right)\left(2v_{in} - V_{REF}D_i\right) \tag{4.16}$$

The relative error $\Delta G_\tau/G$(t) introduced by the time constant is extracted from the first term, as in (4.17).

$$\frac{\Delta G_\tau}{G}(t) = -e^{-\frac{t}{\tau}} \tag{4.17}$$

The maximum allowable time to settle is half of the period at the sampling frequency, F_S. The settling error must also follow the rule (4.14), thus a first approach to the time constant value can be expressed as in form (4.18).

$$\tau < \frac{1}{2F_S N \ln(2)} \tag{4.18}$$

The time constant is a function of the amplifier transconductance and of the total capacitance to be handled. Figure 4.10 illustrates the amplifier in signal amplification mode. Notice that C_S is previously charge, as it can be C_F, and is connected to a constant reference voltage, $+V_{REF}$, $-V_{REF}$ or 0. Considering that the next stage capacitors, from the amplifier and quantizer, are reduced to a load capacitor, C_L, as shown in Figure4.10, the time constant can be expressed as in function (4.19).

$$\tau = \frac{C_L + C_F \,\|\, (C_S + C_P)}{g_m} \; \frac{C_S + C_F + C_P}{C_F} \tag{4.19}$$

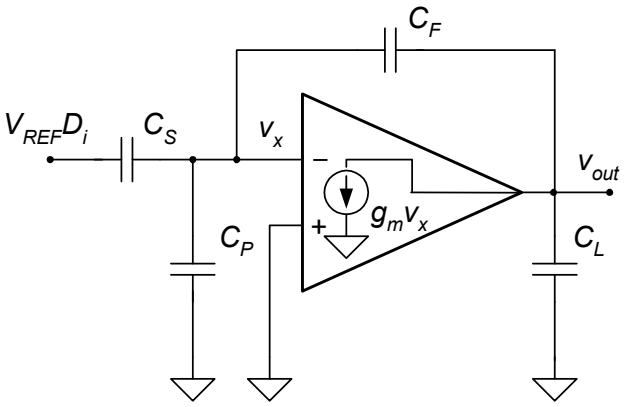


Figure 4.10: Closed-loop amplifier connections.

The upper part of the first term represents the total capacitance seen at the amplifier output, and the second term is the inverse of the feedback factor. Thus, the corner frequency for the settling response is in the form (4.20), and the amplifier g_m can be determined.

$$\omega_{-3dB} = \frac{g_m}{C_L + C_F \,\|\, (C_S + C_P)} \frac{C_F}{C_S + C_F + C_P} \tag{4.20}$$

However, the amplifier output current is limited internally by the differential pair tail current, I_{max}. At the beginning of the residue amplification, during a certain period of time, the amplifier provided current is the maximum value. The transient response is limited by the *SR*, approximately defined by expression (4.21).

$$SR = \frac{I_{max}}{C_L + C_F \,//\, (C_S + C_P)} \tag{4.21}$$

For hand calculation, if only one third of the complete half period is assumed for settling in SR limitation (roughly), a variation in output voltage, Δv_{out}, will imply a maximum current in form (4.22).

$$I_{max} > 6 F_S \Delta v_{out} \left(C_L + C_F \,//\, (C_S + C_P)\right) \tag{4.22}$$

And, assuming the remaining time, *i.e.* 2/3 of half period, for exponentially settling, recalling equations (4.18) and (4.19), the amplifier transconductance can be expressed as in (4.23).

$$g_m > 3F_S N\ln(2)\left(C_L + C_F \,||\, (C_S + C_P)\right)\frac{C_S + C_F + C_P}{C_F} \tag{4.23}$$

However, it is possible to make a more precise calculation. During that current saturation *SR* period, the output voltage follows a linear slew-rate function (4.24), where $v_{out}(0)$ represents the initial value of the output voltage.

$$v_{out}(t) = v_{out}(0) + SRt \tag{4.24}$$

Only when the voltage at the input of the amplifier, $v_x(t)$, reaches a value, at moment t_{SR}, defined by (4.25), the amplifier starts responding exponentially.

$$v_x(t_{SR})\, g_m \le I_{max} \tag{4.25}$$

The t_{SR} value can be expressed by (4.26) [61], where $v_x(0)$ is the initial voltage at the amplifier input.

$$t_{SR} = \left(-\frac{I_{max}}{g_m} - v_x(0)\right)\frac{C_L + C_F \,//\, (C_S + C_P)}{I_{max}}\frac{C_S + C_F + C_P}{C_F} \tag{4.26}$$

After that moment the output voltage is settling exponentially as shown in (4.27) [61], where $v_{out}(t_{SR})$ represents the initial output voltage of this second period, and $v_{outfinal}$ represents the required final output voltage value.

$$v_{out}(t) = v_{outfinal} + \left[v_{out}(t_{SR}) - v_{outfinal}\right]e^{-\frac{(t-t_{SR})}{\tau}} \tag{4.27}$$

The first period of time introduces an additional constraint to the sampling rate, apart from the time constant, and also apart from the transients introduced by the transition times of the clock signal. Therefore, for a specific load condition there is a minimum value for the

available maximum current for which the output voltage settles within the specified error in the required period of time.

The closed-loop structures use the feedback mainly to minimize the errors caused by the nonlinearities of the amplifiers [62]. A high enough gain is mandatory, forcing complex topologies or additional amplifier stage and increased stability care. Also, when large sampling rate values are required, the slew-rate limitation compels to increase the maximum current and transconductance values, costing power and additional parasitic capacitances.

4.2.3. Open-loop SC gain structures

Open-loop structures in pipelined A/D converters have widely been used and their main advantages are pointed out in [63 to 68]. One possible implementation when an open-loop structure is used, is illustrated in Figure 4.11. In this case there is no feedback capacitor. Then, the amplifier gain is settled internally to 2. The quantizer code D_i controls the reference level to be selected. Since that reference level is also amplified, the reference voltages need to be previously divided by 2. Capacitor C_S stays charged during amplification, not being the charge redistributed onto any feedback capacitor as in the closed-loop schemes, and imposes to the amplifier input an inverted signal. This is corrected inverting also the amplifier gain, to −2. The residue voltage, v_{out}, passed to the next stage is approximately expressed by function (4.28).

$$V_{out} = 2V_{in} - V_{REF}D_i = 2\left(v_{in} - \frac{V_{REF}}{2} D_i \right) \qquad (4.28)$$

During phase ϕ_2, the input signal, v_{in}, is applied to the local sub ADC input, with threshold values at $+V_{REF}/4$ and $-V_{REF}/4$, and C_S is charged. During the next phase ϕ_1, C_S is switched to the adequate reference voltage, according to previously stored quantizer outputs, D_i, and the amplifier processes the signal presented at its input, delivering to the next stage the produced residue.

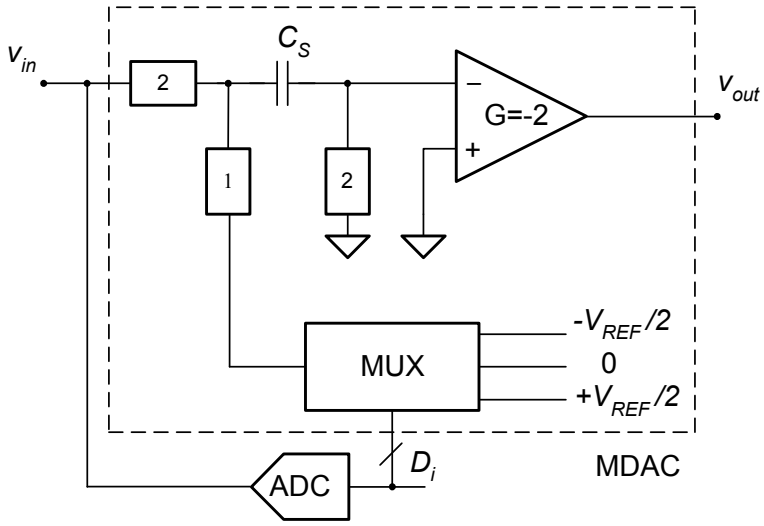


Figure 4.11: Open-loop structured stage.

The high gain requirement is avoided and a light and simple amplifier topology can be used, improving power efficiency, stability and allowed sampling rate. Another main advantage relies on the fact that a single sampling capacitor is required to implement both, sampling and DAC functions. As a consequence, the kT/C noise of this circuit is smaller when compared with the closed-loop approach.

In other words, for the same amount of noise generated by a given stage, the capacitance value adopted can be smaller for the open-loop approach, resulting in significant power savings. However, some challenging effects are introduced in open-loop solutions. Moreover, either self-calibration or servo-loop techniques have to be used to linearize the gain.

Figure 4.12 illustrates the amplifier in the residue amplification mode. The product of the transconductance by the output resistance, R_o, defines the required gain. Notice that C_S is charged previously and it is connected to a constant reference voltage, $+V_{REF}/2$, $-V_{REF}/2$ or 0.

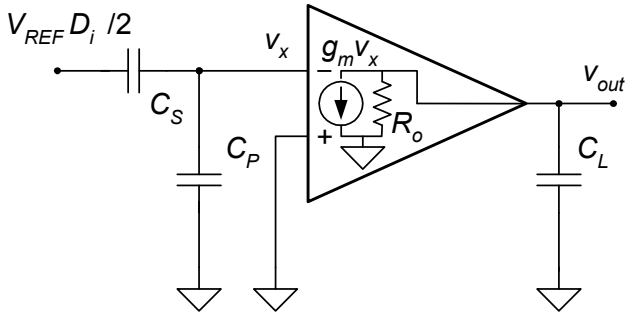


Figure 4.12: Open-loop amplifier during amplification phase.

The voltage at the input of the amplifier, v_x, should be as expressed by (4.29).

$$v_x = -\left(v_{in} - \frac{V_{REF}}{2} D_i \right) \tag{4.29}$$

The ideal open-loop amplifier operates always in the linear amplification region, not occurring slew-rate limitation. Ideally, the output voltage follows an exponential settling, expressed by (4.30).

$$v_{out}(t) = \left(1 - e^{-\frac{t}{\tau}} \right) \left(2 v_{in} - V_{REF} D_i \right) \tag{4.30}$$

The time constant, τ, is only the output resistance and load capacitance product, as in (4.31).

$$\tau = R_o C_L \tag{4.31}$$

That points to a simple time settling computation according to the available half period of the clock. Also, typical design parameters show that the available time of the overall converter is reduced [66], when compared with closed-loop structures at the same power level.

The open-loop structures might require additional circuits to mitigate the introduced errors, replica and servo amplifiers [66], or even off-chip digital processor for high resolutions [65], nevertheless the advantages are considerable, mainly when high sampling rates are needed.

The voltage amplifier, with an internally settled gain of −2, can be implemented with an open-loop or a closed-loop circuit. Figure 4.13 displays a non-inverting closed-loop OpAmp, during the residue amplification period. Being a non-inverting amplifier, in a differential scheme, the outputs delivered to the next stage should be swapped. The next stage amplifier and quantizer input capacitors are reduced to a load capacitor, C_L, and the parasitic input capacitor is represented as C_P.

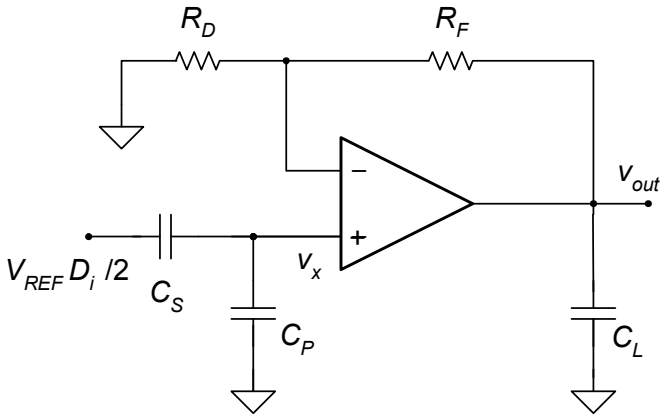


Figure 4.13: Open-loop structured 1.5-bit stage amplifier.

There are some details to be looked at and overcome. One is the importance of the parasitic input capacitance value, due to the attenuation caused to the voltage presented to the amplifier input, v_x, which is going to be amplified.

The v_x voltage, attenuated by the parasitic capacitor C_P, is in the form (4.32).

$$v_x = -\frac{C_S}{C_S + C_P}\left(v_{in} - \frac{V_{REF}}{2} D_i \right) \tag{4.32}$$

The adjustable gain, G, needs to be slightly increased to void the first term, as in (4.33).

$$G = 2\frac{C_S + C_P}{C_S} \tag{4.33}$$

The overall output impedance value determines the settling-time, and it is also relevant. The output resistance, R_{out}, is the parallel of the closed-loop resistance of the amplifier with the feedback circuit resistance, if the value of this last is low enough to be relevant, as expressed by (4.34), being R_o the output resistance of the amplifier, and A the open-loop gain.

$$R_{out} = \frac{R_o}{1 + A\dfrac{R_D}{R_D + R_F}} \,\|\, (R_D + R_F) \tag{4.34}$$

This sets a first condition for the values of R_D and R_F. Additionally, the gain can be corrected considering R_o and A, resulting in equation (4.35), and setting another relation between the resistors values.

$$G = 2\frac{C_S + C_P}{C_S} = \frac{R_D + R_F}{R_D}\frac{1}{1 + \frac{1}{A}\frac{R_D + R_F}{R_D}\frac{R_D + R_F}{R_D + R_F + R_o}} \tag{4.35}$$

4.3. Constant gain amplifiers for possible use in open-loop SC circuits

A standard topology for a differential programmable gain or variable gain amplifier is shown in Figure 4.14. It is a circuit with a degenerated differential pair with a resistor as load. The differential input voltage, $v_{id} = v_{inp} - v_{inn}$, causes a current flow in the degeneration resistors, $R_{Dp} = R_{Dn}$, a function of the sum of these and of the two transistors transconductance, g_m.

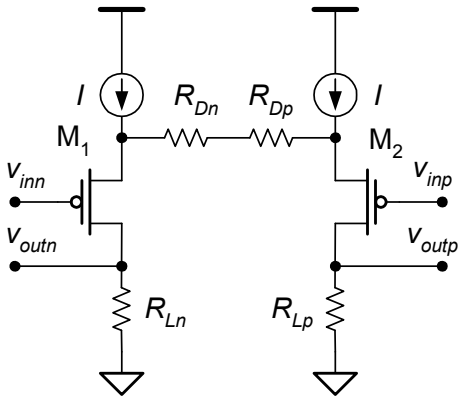


Figure 4.14: Degenerated differential pair amplifier.

The output voltage, $v_{od} = v_{outp} - v_{outn}$, is a function of the difference of the current flowing in load resistors, $R_{Lp} = R_{Ln}$, and then it can be expressed by function (4.36), where $R_D = R_{Dp} = R_{Dn}$ and $R_L = R_{Lp} = R_{Ln}$.

$$v_{od} = -v_{id}\frac{R_L}{R_D + \frac{1}{g_m}} \tag{4.36}$$

The major advantage of this open-loop architecture relies on the fact that it is easy to change the overall gain, by changing the ratios of the load and degeneration resistors, making this circuit suitable for use as variable or programmable gain amplifier.

Due to noise requirements, the resistance values have to be small, and to maintain the distortion levels low, the bias current needs to be large enough. An improvement [69] is the circuit shown in Figure 4.15, allowing a larger output swing and reduced bias current of the input transistor. The output currents are mirrored and the output currents can be higher, or the output levels easily changed.

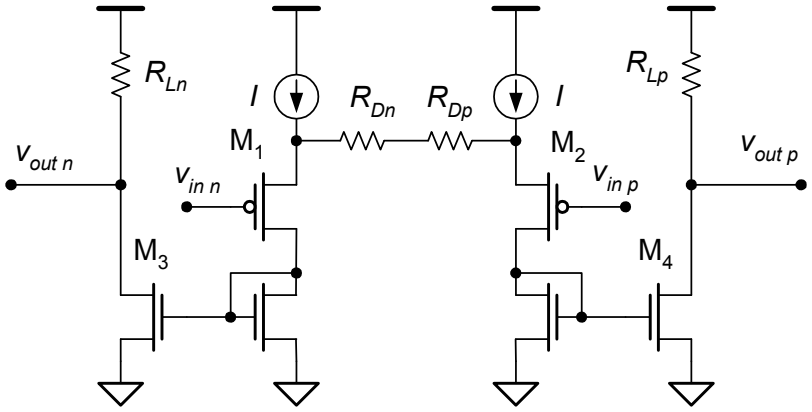


Figure 4.15: Amplifier with mirrored current.

The input transistors, M_1 and M_2, are still driving the current flowing in the degeneration resistors. The introduction of two current sources and two other transistors, M_5 and M_6, acting together with the input transistors, M_1 and M_2, as two super (enhanced) source followers [70][71], can be seen in Figure 4.16.

The input transistors, M_1 and M_2, are forced to conduct a static current defined by the current sources shown hereunder. The transistors M_5 and M_6 conduct the difference of the currents defined by the upper and lower current sources. Also they take care of the current flowing through the degeneration resistors, a function of the differential input voltage. That current can be mirrored to M_3 and M_4, and to the load resistors. The performance of this amplifier circuit is suitable, for example, for multiply-by-two stages in 10-bit A/D converters [70][71].

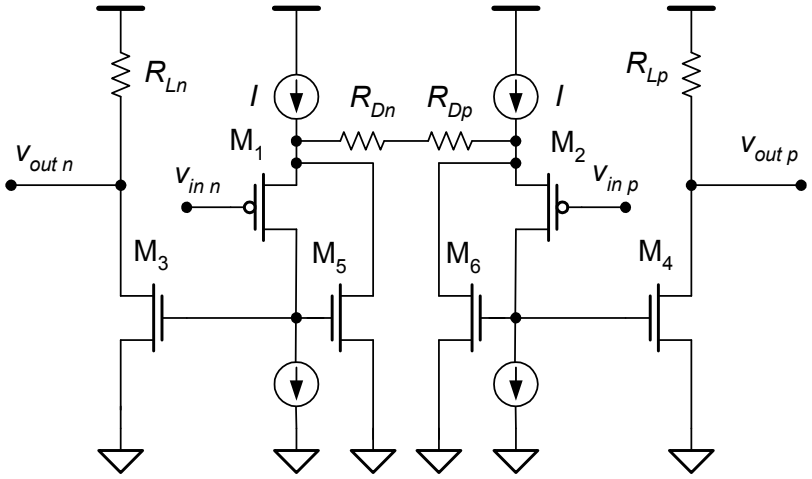


Figure 4.16: Amplifier with super source followers.

The circuit can be improved with the introduction of local feedback [69][70]. A closed-loop circuit, without the previously introduced transistors M_5 and M_6, is displayed in Figure 4.17. The load resistor is replaced by a current source, obtaining a larger gain-bandwidth product (GBW). A negative feedback from the output to the low impedance input transistor source is added.

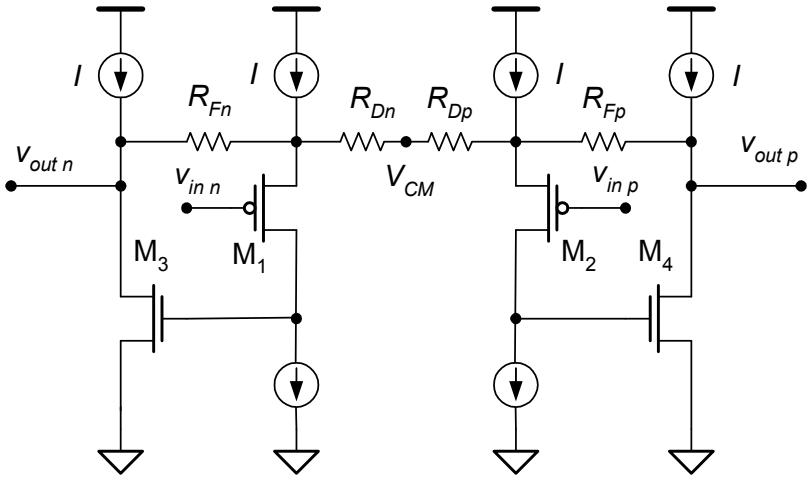


Figure 4.17: Amplifier with internal feedback.

The input transistors, M_1 and M_2, forced to drive a fixed current, are acting as source followers, placing over degeneration resistors the differential input voltage. The subsequent degeneration resistors current is compensated by current flowing through feedback resistors, from outputs. Transistors M_3 and M_4 are acting as a class-A second stage amplifier, providing the necessary output current. Its nonlinearity is highly reduced by the first stage gain. The

input transistor linearity is mandatory to achieve an appropriate overall performance. However, that requirement can be limited to small signals.

A detailed example of an amplifier, with local feedback fixing the gain, is displayed in Figure 4.18. The input transistor, M_1, is forced to drive a constant current defined by current sources, $I_1 = I_2$. It acts as a source follower, replicating at its source the input voltage swing.

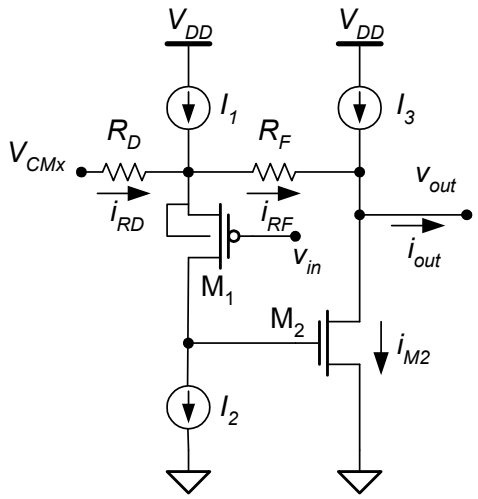


Figure 4.18: Amplifier with local feedback.

The level shift is the gate-to-source voltage, a function of aspect ratio and current (4.37).

$$V_{GS} = V_{TO} + \sqrt{\frac{2i_{DS}}{KP_p W/L}} \qquad (4.37)$$

With the bulk connected to the source, the threshold voltage is constant, V_{TO}. The factor KP_p is technology defined. The current i_{RD} is a function of the source voltage and the V_{CMx} value. That current is summed with the current from source I_3, resulting in current i_{M2} in the M_2 transistor. The output level can be adjusted by the V_{CMx} value. The input capacitance is going to attenuate the input voltage. The gate capacitance is the gate-to-source, the low impedance node, and the less significant gate-to-drain capacitance, if no external compensation capacitor is used. The feedback corrects that attenuation, nevertheless it should be contained. The second amplifier stage delivers the output voltage to the next block. The output voltage swing and common-mode level requirements define the drain-to-source saturation voltage of transistor M_2, V_{DSsat}, which must be guaranteed. Thus, a first relation between the current and the aspect ratio of the device can be set in the form (4.38).

$$V_{DSsat} = \sqrt{\frac{2i_{DS}}{KP_n W/L}} \tag{4.38}$$

A design condition is the required value of the output resistance, r_o, or output conductance, g_{DS}. It can be given in form (4.39), where V_{En} is the Early voltage *per* channel length.

$$r_o = \frac{1}{g_{DS}} = \frac{V_{En}L}{i_{DS}} \tag{4.39}$$

However, the current value should be a function of the settling-time requirement. For a positive output voltage step, the C_L load capacitor charging current is delivered mainly by I_3 current source. Not considering the effect of the R_F resistor and of the I_1 and V_{CMx} supplies, the limit of the voltage slew-rate, *SR*, is defined by (4.40).

$$SR = \frac{I_3}{C_L} \tag{4.40}$$

Considering the step amplitude of the output voltage, Δv_{out}, and the sampling frequency, F_S, and only one third of the available amplification time for the limited slew-rate approach, the value of the source current I_3 results in (4.41).

$$I_3 > 6F_S \Delta v_{out} C_L \tag{4.41}$$

The exponential settling approach is a function of the output resistance value, R_{out}. Using the remaining two thirds of the sampling period, the amplifier output resistance should follow (4.42).

$$R_{out} < \frac{1}{3F_S C_L} \tag{4.42}$$

The discharging process, for a negative output voltage step, is controlled by transistor M_2, depending on the size and effective gate voltage. The saturation must be assured. A first approach to the M_2 sizing can be done using the complementary metal-oxide-semiconductor

(CMOS) technology parameters and the expected current value. The transconductance, g_m, is expressed as in (4.43),

$$g_m = \sqrt{KP_n \frac{W}{L} i_{DS}} \tag{4.43}$$

Increasing the current and the size of M_2, transconductance will be increased. But the parasitic capacitance will increase too, and the bandwidth decreased. Being the M_1 transistor conductance moderate, the gate capacitance of M_2 is relevant. The current i_{M2} is a function of the difference between the recommended output level and the voltage at the input transistor source. The latter is shifted from the input level, which needs to be large enough to assure the operation of M_1. The current delivered by the control voltage, V_{CMx}, is going to be added to the current delivered by I_3, which can be decreased.

The gain is approximately equal to $1+R_F/R_D$, but the capacitive attenuation due to parasitic capacitor at the input (gate of M_1) reduces it. Instead of varying R_F, by linearity and stability reasons [69], the overall voltage gain can be tuned by adjusting R_D, in order to compensate for the errors, *i.e.* input parasitic capacitance, open-loop gain and output impedance. Adjusting R_D does not interfere with bias, while V_{CMx} can be also adjusted in a small range, being the offset corrected in a differential scheme. It is a non-inverting amplifier configuration, suitable to be used in 10-bit A/D converters [69].

Some major and common errors introduced by residue amplification, the offset, gain mismatch and nonlinear errors, are illustrated In Figure 4.19.

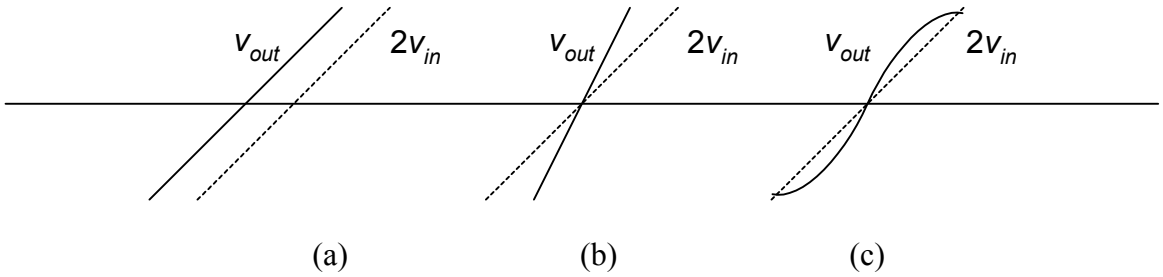


Figure 4.19: Residue amplification errors; (a) offset; (b) gain; (c) nonlinearity.

Offset errors are additive errors propagated from the input to the output. Common sources are the charge injection and the amplifier offset. Gain error is a multiplicative error introduced by

the amplifier, usually due to capacitor mismatch or attenuation, incomplete setting, and finite gain. Nonlinear errors are introduced by elements in the circuit having a response undesirably dependent on several factors. The most common sources are the gain dependence on output level, variation of parasitic and non-parasitic capacitance values with operation conditions.

Simulating a differential scheme of the circuit discussed, applying an increasing input signal from zero to 400 mV, from instant 10 ns to 20 ns, with a load of 0.5 pF, the output response at ending period is displayed in Figure 4.20(a), and at the starting instant given in Figure 4.20(b).

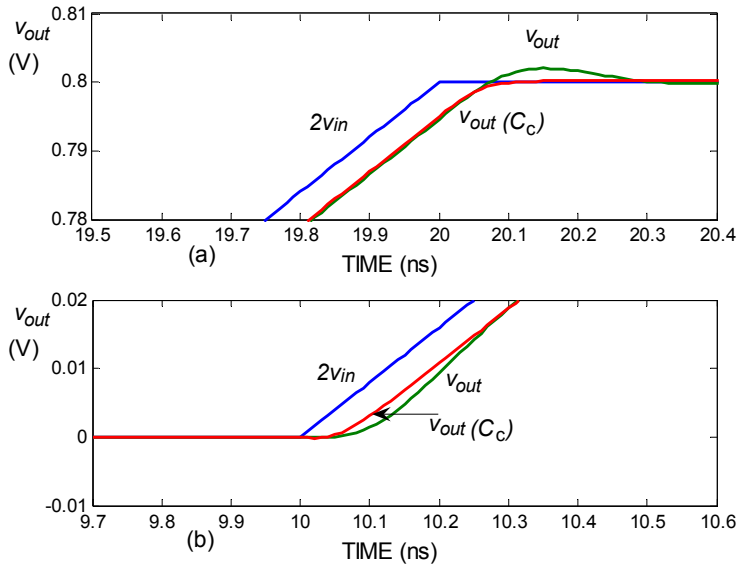


Figure 4.20: Ideal and obtained output responses; (a) ending period; (b) starting period.

The output response, without compensation, displayed as v_{out}, and with a small capacitor C_C= 10 fF applied to M_2, displayed as $v_{out}(C_C)$, can be compared with the ideal output, *i.e.* $2v_{in}$.

4.4. Phase complexity

In designed SC circuits several efforts have been made to prevent the charge injection and clock feed-through errors. Different clock sequence schemes have been studied and analyzed, concerning the preservation and integrity of the signal during the handling processes. The realization of high accuracy and sampling rate circuits is accomplished with a higher relevance given to those errors.

4.4.1. Non-overlapped clock signals sequence

Usually the switches in SC circuits are controlled by non-overlapping bi-phase control signals. This will avoid the discharge of capacitors inside the circuit, which could occur if the switches are ON simultaneously, even during a small fraction of time.

Moreover, two additional control signals are normally used [47]. These signals are advanced in time, relatively to the previous ones, and their function is to turn-OFF certain switches before others, and thus, to prevent the signal dependent charge injection into the capacitors.

Figure 4.21 displays a single ended flip-around S/H circuit. During the sampling period, switches S_2 and S_1 are ON. During the holding period, switches S_3 and S_4 are ON.

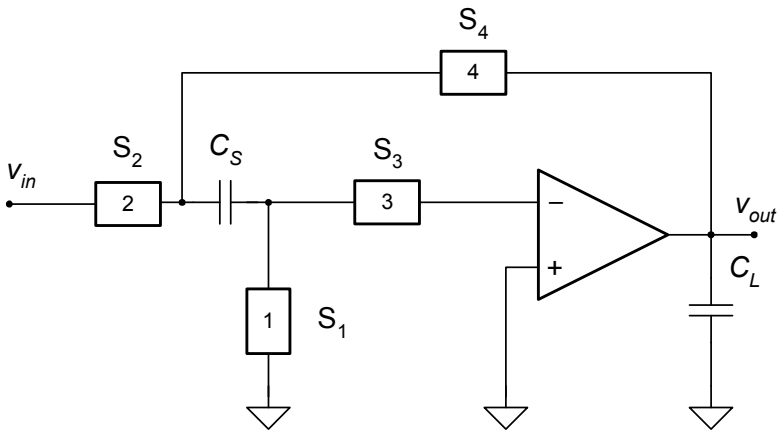


Figure 4.21: Sampling circuit with four switches.

Switches S_1 and S_3 operate at a fairly constant potential, since the common node is connected always to V_{SS} by switch S_1, and always to the amplifier input by switch S_3. Therefore, the introduced error is signal independent and can be canceled easily. This is not happening with switch S_2, as it is connected to the input signal.

At the end of the sampling phase it is important to open first switch S_1, connected to the top-plate of the sampling capacitor, and only afterwards open switch S_2 [44]. In Figure 4.22 the clock signals are represented, ϕ_1, ϕ_2, ϕ_3 and ϕ_4, which are controlling switches S_1, S_2, S_3 and S_4 respectively.

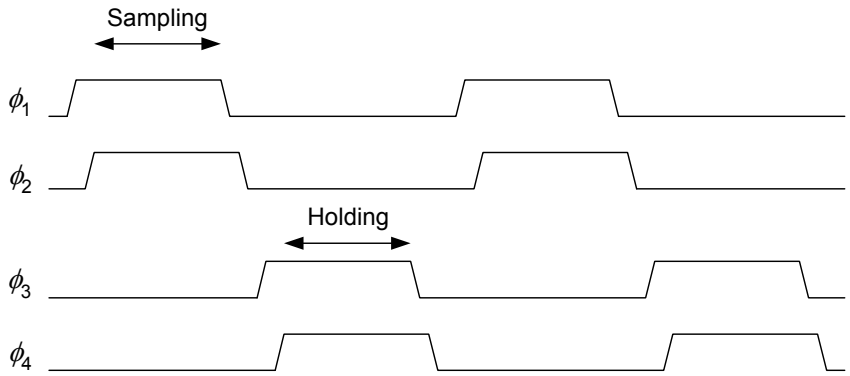


Figure 4.22: Control signals sequence.

When ϕ_2 falls, S_2 is opening and it sees one high impedance in the sampling capacitor, C_S, direction, and, in principle, the charge will be injected into the input node, *i.e.* v_{in}, preserving the charge of the sampling capacitor from signal dependent errors. For this is necessary that clock signal ϕ_1 is advanced to ϕ_2, and that switches S_3 and S_4 remain still open when ϕ_2 falls, *i.e.* being phases ϕ_3 and ϕ_4 non-overlapped to ϕ_2. The clock signals, ϕ_1, ϕ_2, ϕ_3 and ϕ_4, are usually represented as ϕ_{1a}, ϕ_1, ϕ_{2a} and ϕ_2, respectively. During the turn-ON process of switches S_3 and S_4, a similar strategy is followed.

Figure 4.23 shows a more detailed circuit drawing, with the parasitic capacitors. C_{P1}, C_{P2} and C_{P3}, distributed over the nodes.

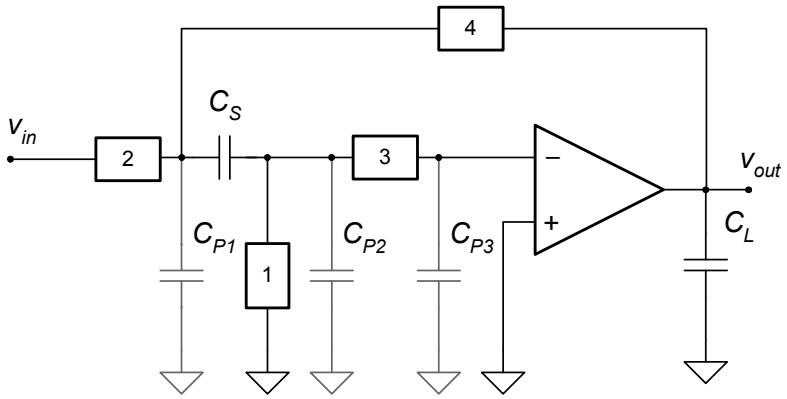


Figure 4.23: Sampling circuit with parasitic capacitances.

When S_1 opens, the charge stored at the S_1 channel, Q_{C1}, is injected and shared by C_{P2} and C_S, as particularized in Figure 4.24.

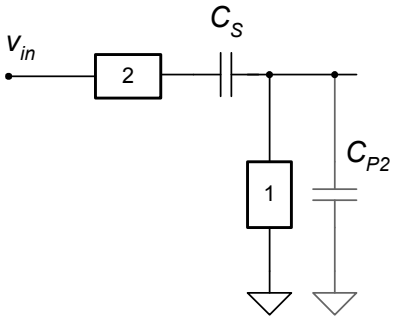


Figure 4.24: Equivalent circuit during S_1 turn-OFF.

The additional charge added into C_S and C_{P2}, ΔQ_{CS} and ΔQ_{CP2}, is function of the capacitance ratio as in (4.44) and (4.45) [45].

$$\Delta Q_{CS} = -Q_{C1}\frac{C_{CS}}{C_{CP2}+C_{CS}} \tag{4.44}$$

$$\Delta Q_{CP2} = Q_{C1}\frac{C_{CP2}}{C_{CP2}+C_{CS}} \tag{4.45}$$

When S_2 opens, the switch S_1 is already not present as specified in Figure 4.25.

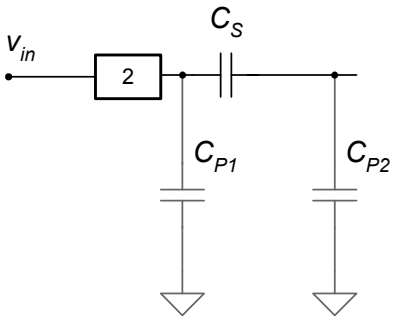


Figure 4.25: equivalent circuit during S_2 turn-OFF.

The channel charge, Q_{C2}, will be shared by the three capacitors, as in (4.46) and (4.47).

$$\Delta Q_{CP2} = \Delta Q_{CS} = Q_{C2}\frac{C_{CS} \parallel C_{CP2}}{C_{CS} \parallel C_{CP2}+C_{CP1}} \tag{4.46}$$

$$\Delta Q_{CP1} = Q_{C2}\frac{C_{CP1}}{C_{CS} \parallel C_{CP2}+C_{CP1}} \tag{4.47}$$

When switch S_3 closes, as represented in Figure 4.26, charges are collected from the vicinity. In this case, the injected charge has the opposite direction from the later situations, and moreover, the amount of charge is relatively higher. As a matter of fact, when switches S_1 and S_2 are in the turn-OFF process, only one node is connected to the capacitors, and, therefore, only half of the total charge in the channel, approximately, is injected to the capacitors side. However, when S_3 turns-ON, the nodes are shorted and the collected charge is the total channel charge.

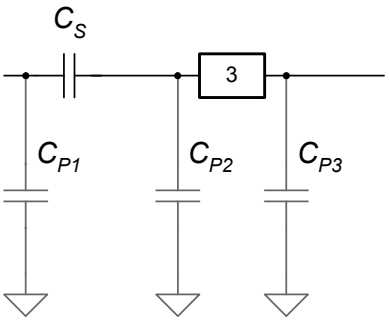


Figure 4.26: Equivalent circuit during S_3 turn-ON.

The additional charge in the relevant capacitors during the S_3 turn-ON process can be summarized by (4.48), (4.49) and (4.50).

$$\Delta Q_{CS} = -Q_{C3}\frac{C_{CS} \parallel C_{CP1}}{C_{CS} \parallel C_{CP1} + C_{CP2} + C_{P3}} \tag{4.48}$$

$$\Delta Q_{P2} = Q_{C3}\frac{C_{CP2}}{C_{CS} \parallel C_{CP1} + C_{CP2} + C_{P3}} \tag{4.49}$$

$$\Delta Q_{P3} = Q_{C3}\frac{C_{CP3}}{C_{CS} \parallel C_{CP1} + C_{CP2} + C_{P3}} \tag{4.50}$$

When S_4 closes, the capacitor C_{P1} will be connected to the output. The additional charge present in capacitor C_{P2} and C_{P3} will be passed to C_S and added to its own additional charge. After a simple computation it can be concluded that the only charge injected is the sum of the charge from S_1 and S_3. The charge from S_2 is canceled. The output voltage error, Δv_{out}, is then approximately as in (4.51).

$$\Delta V_{out} = -\frac{1}{C_S}\left(Q_{C1} + Q_{C3}\right) \tag{4.51}$$

That points to some supplementary considerations, apart from the sequence order of the clock signals.

The first one, is the size or value of the sampling capacitor. Increasing the capacitor value will minimize the error. However, it will reduce the bandwidth and, at least, switch S_2 needs to be oversized.

The second is that, the S_1 and S_3 impact can cancel each other. If the two switches are of the same type, and S_3 is half sized, the introduced charges will have the same absolute value and opposite signs.

Therefore, operating the SC circuits with non-overlapping bi-phase control signals is essential for the successful SC operation, since a capacitor inside an SC circuit can discharge if two switches are turned ON simultaneously. Moreover, two additional phases are generally used in many SC circuits, which are advanced versions of the previous control signals. These two phases overcome the problem of signal-dependent charge injection, by turning-OFF sampling switches connected to the inputs of the amplifiers slightly before the switches connecting the input signals to the bottom-plates of the sampling capacitors. Additionally, since both NMOS and PMOS switches are normally employed, this four-phase scheme becomes a complex, six or eight phase scheme, due to the need of having complementary versions of the four previous control signals for driving the PMOS devices.

4.5. Conclusions

Simpler and power efficient circuits are more and more required. The amplifiers, hugely used in closed-loop for different functions in the SC circuits, are key elements, and their limitations shape the overall performance.

The passive S/H block is an option to reduce the lost power and increase the overall energy efficiency. Also, an option to design the MDAC blocks is to use open-loop residue amplification. The simplicity and the power efficiency of the amplifiers using fixed gain, are

reasons why their use has proliferate. Not only among the projects requiring high sampling rate and moderate accuracy, but also in projects with high resolution demand.

The complexity of the phase signals, commonly used to control the different blocks of the SC circuits, as S/Hs, MBTAs and MDACs, increases the power loss. The use of simpler control signals schemes is necessary and mandatory, so the overall performance can be achieved. Simple phase schemes will reduce die area, reduce substrate noise, reduce design time and they will necessarily lead to improved design solutions.

5. Techniques for overcoming the switches limitations and new switch-linearization circuit

Present and emergent complementary metal-oxide-semiconductor (CMOS) technologies require the use of low supply voltages. Special care and requirements are mandatory to guarantee that the linearity of the switches in the signal path is kept over rail-to-rail signal swings, needed in many low-voltage switched-capacitor (SC) circuits, spanning from 10-14-bit analog-to-digital converters (ADCs) to accurate analog filters. On the other hand, the reliability constraints of the technology have to be considered, avoiding over-stress of the CMOS devices if large voltages are applied to the gates of the transistors.

5.1. Introduction

The design of the SC circuits, as sample-and-hold (S/H) circuits used at the front-end of the ADCs, is becoming more and more complex as the supply voltage is lowered. Some methods overcome the most important problems, such as the charge injection, or the clock feed-through, or the switches nonlinearity, or the lack of the switches overdrive. The implementation of correction schemes and methods, usually involve additional circuits and control clock signals, then increasing the area and power, and reducing the efficiency. The use of such techniques to mitigate the existent and emergent problems is, in general, a trade-off with respect to precision, power, speed, layout complexity, and reliability. This last is taking additional relevance as the oxide thickness is reduced towards deep sub-micron CMOS technologies.

This Chapter addresses these challenges, analyzing the existent solutions and proposing a simple SC linearization control circuit that generates suitable gate control voltages when very low distortions are targeted, within the technology limits, to drive a CMOS transmission-gate. Exhaustive corner simulation results of a practical S/H circuit show that, using the proposed circuit, linearity/distortion levels above 12-bits can be reached over the entire Nyquist band and even beyond it (in sub-sampling mode), as it will be shown, later on, in Chapter 7. The new circuit proposed in this Chapter can be readily used in any advanced CMOS technologies for boosting the linearity of low-voltage high-swing CMOS switches.

5.2. Bootstrapping techniques

5.2.1. Bootstrapping an NMOS switch

To allow an input voltage rail-to-rail swing in an NMOS switch, it is needed to apply an enough gate voltage even when v_{in} is close to V_{DD}. Figure 5.1 shows a S/H block resumed from Chapter 3, using an NMOS switch. This S/H is electrically simulated using a standard 1.2 V 130 nm CMOS technology and BSIM3v3.4 models. A voltage bootstrapped by 1.2 V is

applied between the gate and source, and a ramp voltage drives the input node, v_{in}, from 0 V to 1.2 V in 4 ns, being the NMOS device sized with aspect ratio 5/0.13, 20/0.13 and 40/0.13. The capacitor C_S= 1 pF is assumed to be initially discharged.

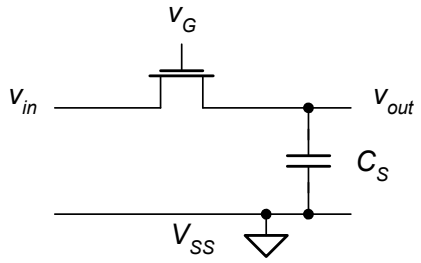


Figure 5.1: Basic sampling circuit.

The results obtained from the simulation of the circuit are shown in Figure 5.2. In Figure 5.2(a) it can be observed that the devices are ON during a complete v_{in} swing. The threshold voltage value does not impose a knee point. However, the conductance is not constant and it decreases as the input voltage increases, as it is implicit in equation (5.1), already analyzed in Chapter 3 but reproduced again here for convenience.

$$g_{DSn} = KP_n \frac{W_n}{L}\left[v_{Gn} - v_{in} - V_{TOn} - \gamma_n\left(\sqrt{2|\Phi_{Fn}| + v_{in}} - \sqrt{2|\Phi_{Fn}|}\right)\right] \qquad (5.1)$$

Figure 5.2(b) represents the output voltage variation. Although all the different sized devices seem to be able to allow the sampling capacitor to charge during the input voltage swing, two interesting subjects are revealed and need to be taken into account by the designer.

The first is the conductance value of the switching device, concerning its average, assuming that the variables and parameters in equation (5.1) remain constant. It is going to determine if the sampling capacitor, at the end of the sampling period, is charged, and presents a voltage with lower error than permitted, regarding the input voltage. This issue is being analyzed and, up to now, the device up-scaling, the increasing of the gate voltage and the lowering of the threshold voltage have been proposed.

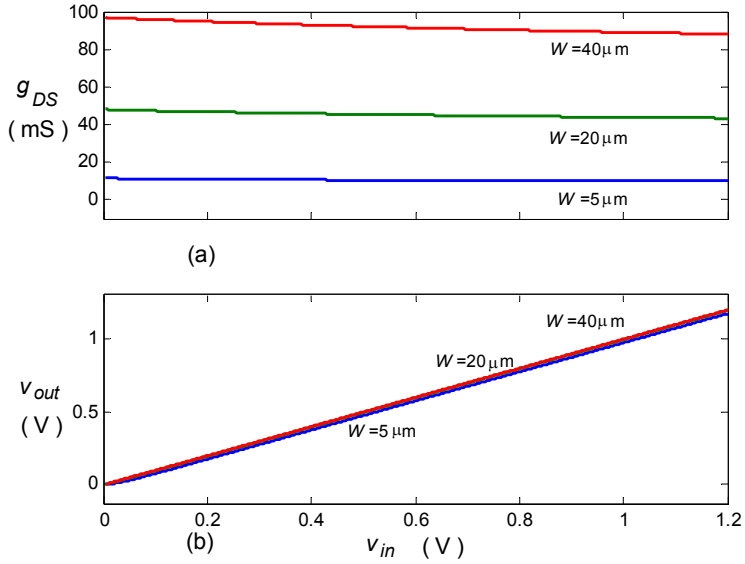


Figure 5.2: Bootstrapped switch; (a) Conductance; (b) Output voltage.

The second subject is related with the conductance variation regarding the circuit variables, such as signal input voltage. Such variation is going to define deeply the circuit response and its second order errors, needed in high level circuits, when the input signal has a significant variation during the sampling period and when high accuracy is desired.

Regarding equation (5.1), and admitting that the voltage difference between the gate and input is maintained, this issue concerns the influence of the body factor variation. It could be done by zeroing the bulk-to-source voltage. However, that is not possible in an NMOS standard implementation, where the bulk is common (the substrate is p-type)[5].

In any case, this matter is not relevant as the differential stages are normally employed. Using two circuits similar to the previous one, each with a 20µm NMOS device, the first as a positive stage (p-stage), and the second as a negative (n-stage), and applying a differential input signal to their input, a ramp varying from −1.2 to +1.2 V in 4 ns, the overall conductance can be observed.

In Figure 5.3(a) is shown the particular conductances of the switches of the two stages, regardly their differential input voltage.

[5] Deep-submicron technologies (L<130 nm) normally allow (with additional cost) to use triple-well, *i.e.*, it becomes possible to connect the bulk terminal to any potential.

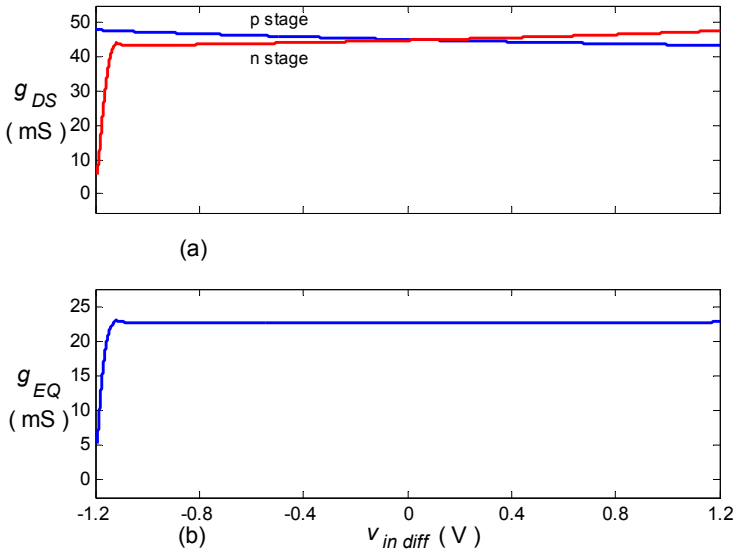


Figure 5.3: Differential scheme; (a) Partial conductances; (b) Equivalent conductance of global circuit.

It should be noticed that the switches present a symmetric slope, as in the first the input the voltage is increasing, and in the second it is decreasing. Therefore, an equivalent conductance of the two devices acting simultaneously, g_{EQ}, obtained by setting both individually conductances in series, as can be observed in Figure 5.3(b). The equivalent conductance is constant during the complete input voltage range, and puts in evidence one of several advantages of differential implementations.

5.2.2. Bootstrapping circuits

To obtain an enough and quite constant conductance operation, the gate-to-channel voltage should be held with a significant and constant value during the ON state. This can be obtained using the bootstrap technique, which consists in boosting the gate voltage of the switch beyond the power supply voltage. In the OFF state, the gate is grounded, the device is cut-off while a bootstrap capacitor C_b is charged to $v_G = V_{DD}$. Then, in the ON state, this capacitor will act as a floating voltage source in series with the input signal making the gate voltage of the switch equal to $v_G = V_{DD} + v_{in}$, resulting in an overdrive voltage nearly constant over the input signal voltage range and, as a result, the switch's conductance will be approximately constant and signal-independent.

Figure 5.4 shows a possible implementation for an NMOS bootstrapped switch (CBTn) [72][73]. During the OFF state, switches driven by phase ϕ_2 (S_4 and S_3) are ON and the bootstrap capacitor, C_b, is charged to V_{DD}. During the ON state, switches driven by phase ϕ_1 (S_1 and S_2) are ON and the resulting voltage is added to the input signal and applied to the gate of the main NMOS switch, M_1.

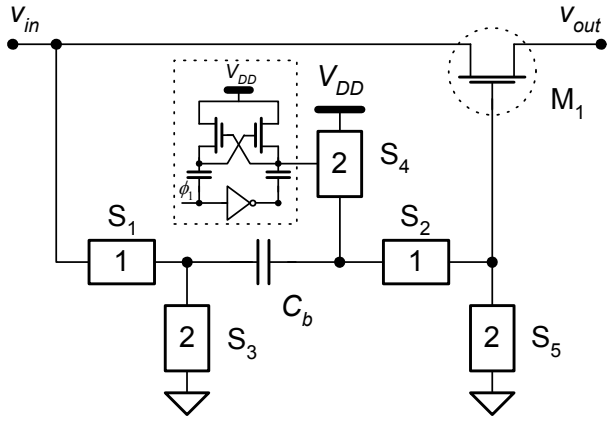


Figure 5.4: NMOS bootstrapping circuit block diagram.

Critical switch S_4 has to be implemented with an NMOS device controlled by a bootstrapped signal from a charge pump (CP) or voltage doubler, instead of using a conventional PMOS with the source connected to V_{DD}, since in that case the switch could be turned ON during phase, ϕ_1, due to the large voltage that occurs in the drain node (as high as 2x V_{DD}). Switch S_2 can be implemented by a PMOS, but leakage will occur if the bulk is connected to V_{DD}. The bulk should be connected to its source or it may be necessary to connect it to 2x V_{DD} from the CP. Switch S_5, an NMOS, will support high voltage values, drain-to-source and gate-to-drain, and can be protected by adding a cascode NMOS device.

In Figure 5.5 the simulated circuit is presented being the NMOS devices sized with aspect ratio 1/0.13, the PMOS with 4/0.13, the main switch M_1 with 20/0.13, the voltage doubler capacitors with 75 fF each, and the boosting capacitor with 150 fF. The clock signal, ϕ_1, with a 50 MHz frequency, and its complementary signal ϕ_{1n}, are used. The input signal of 0.25 V peak-to-peak amplitude and a frequency of 10 MHz, is applied.

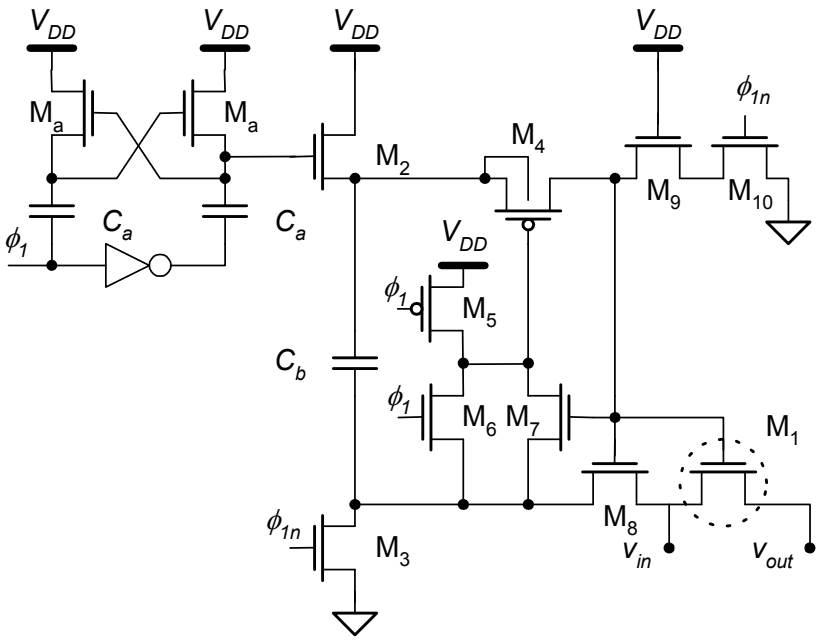


Figure 5.5: NMOS bootstrapping circuit [73].

When the clock signal ϕ_1 is OFF, M_2 is ON via the action of the voltage doubler, and charges, together with M_3, the capacitance C_b. The device M_5 forces the OFF state of M_4, and M_{10} forces M_1, M_8 and M_7 to be OFF too. When ϕ_1 goes high, M_6 will turn ON, pulling down the gate of M_4, supplying the M_8 and M_1 gates. Being M_8 ON, it tracks the input signal, v_{in}, and then the main device gate and its own gate, will be pushed close to $v_{in}+V_{DD}$. Therefore, M_1 will have enough gate voltage to turn ON during ϕ_1. The device M_7 forces the ON state of M_4, reassuring the M_6 function.

In Figure 5.6 are shown some simulated results. The applied main switch gate and the input voltages, and the main switch conductance, are shown, respectively, in Figure 5.6(a) and (b). It can be stated that the gate voltage swings together the input signal.

The gate voltage is pushed over v_{in} too, but only about 75% of V_{DD}. The CBTn efficiency is related to the capacitors size, C_a in the charge-pump circuit, and the boosting capacitor C_b. The conductance has a significant value and could be increased, should it be possible to apply a higher gate voltage. The body effect is also present, decreasing the conductance when the input voltage is far from the bulk voltage, presenting the conductance variation of 18% for the applied signal amplitude.

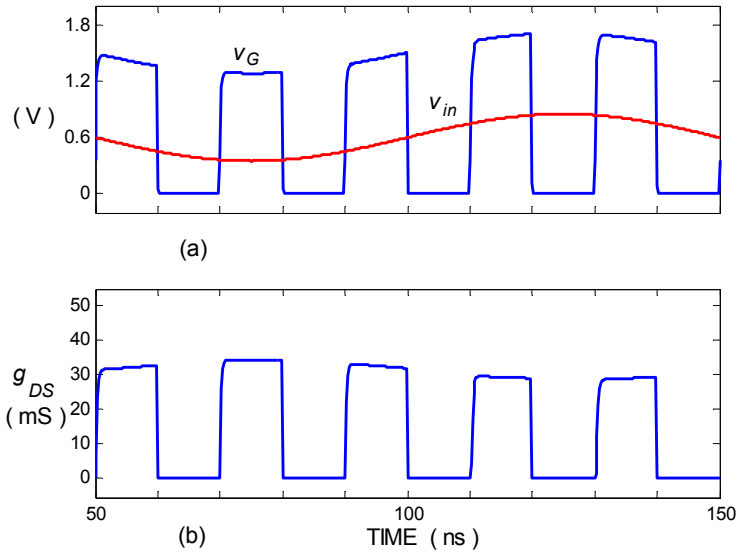


Figure 5.6: NMOS bootstrapping circuit simulated results; (a) Input and gate voltages; (b) Switch conductance.

Up-scaling the voltage doubler and boosting capacitors, to 200 fF and to 400 fF respectively, the results are improved as displayed in Figure 5.7(a) and (b). The gate-to-source voltage now reaches 80% of V_{DD}.

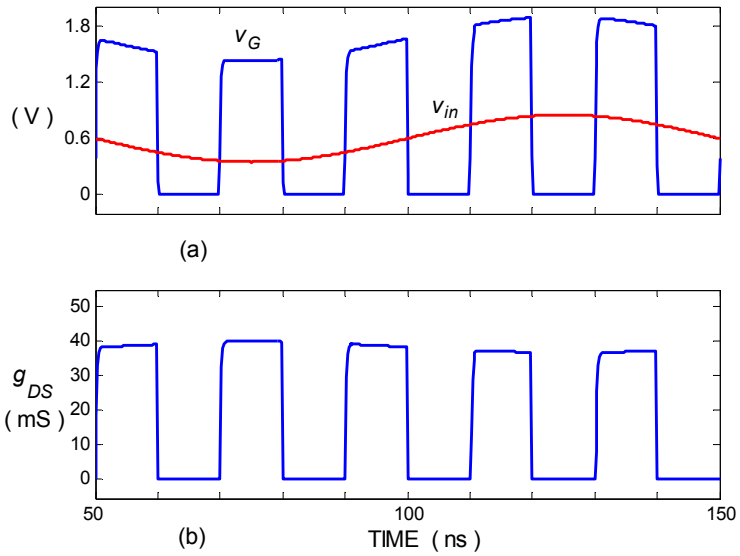


Figure 5.7: NMOS bootstrapping circuit simulated results with oversized capacitors; (a) Input and gate voltages; (b) Switch conductance.

This relatively small increase, from 75 to 80% of V_{DD}, increases the average conductance value by 25%, and minimizes the body effect, reducing by half the variability of the conductance. This improvement of the bootstrapping circuit, based on increasing the conductance while minimizing the body effect, is achieved by a huge variation of the capacitance values, close to 260% of the initial values. It is a relatively high cost in area and in power. Moreover, for such boosted voltages, even with apparently moderate values, the risk for the stress in the oxide is relevant. The stress caused in the gate oxide by the presence of higher voltages will be discussed later. Using a differential scheme the body effect is hugely reduced, as discussed previously. Two similar circuits, with two stages in a differential scheme, p-stage and n-stage, are used for simulation. The initial capacitance values are used as well, and the resulting conductances are shown in Figure 5.8(a) and (b). It can be observed that the equivalent conductance presents no variation throughout several ON periods.

The CBTn efficiency is conditioned by the size of the capacitances and by the body effect. Some authors [74][75] propose the use of an overdrive voltage to drive the gate, controlled in amplitude in a way that the body effect is compensated.

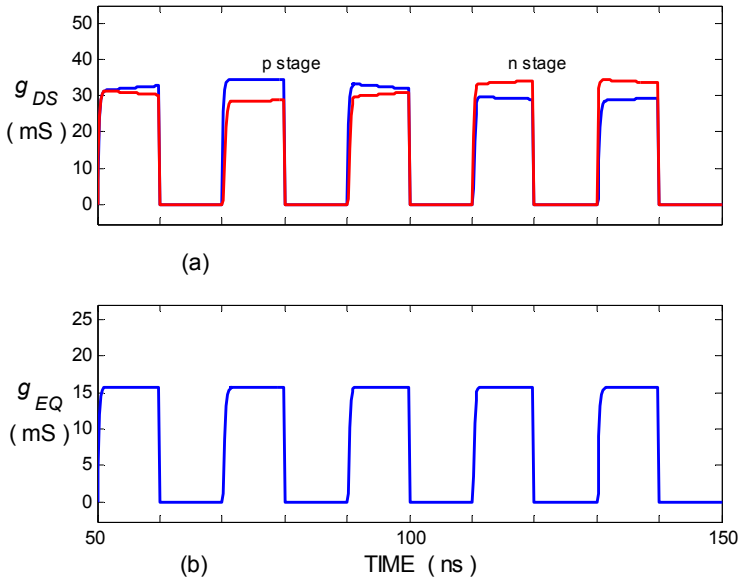


Figure 5.8: Differential bootstrapped scheme; (a) Partial conductances of the stages; (b) Equivalent conductance of global circuit.

A simple modification of the presented circuit can reduce the CBTn overall capacitance value. The voltage doubler, and its capacitors, can be removed if the NMOS used as device M_2 is simply replaced by a PMOS device [76], as shown in Figure 5.9.

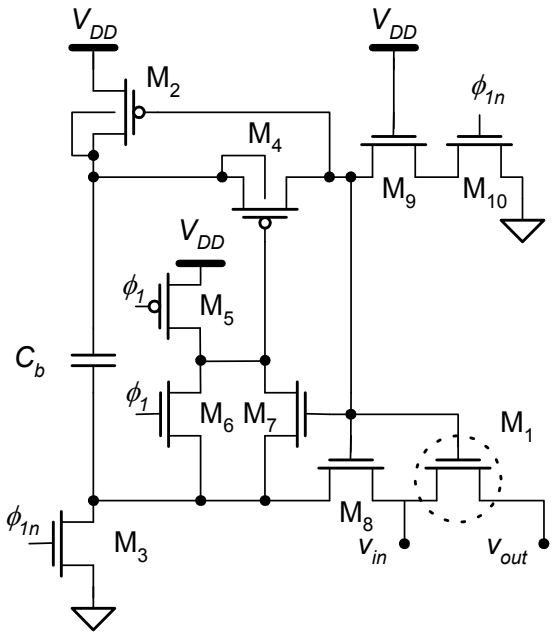


Figure 5.9: Bootstrapping circuit without voltage doubler [76].

In fact, when ϕ_1 is low, M_{10} is ON and forces M_2 to charge the boosting capacitor, C_b. When the gate voltage is pushed up, M_2 will be OFF. Special care is necessary with the high voltage node, connecting the bulk to it. It should be noticed that the same is previously done with the other PMOS in the same node, the M_4 device. The simulation results are similar to those already presented.

5.2.3. Bootstrapping a PMOS switch

In Figure 5.10 a possible implementation for a PMOS bootstrapped switch circuit (CBTp) [77] can be seen, combined with the BS technique. During the OFF state, switches S_4 and S_5 are ON and, again, the bootstrap capacitor, C_b, is charged with a voltage equal to V_{DD}. During the ON state (ϕ_1 high) switches S_1 and S_2 are ON, and the stored V_{DD} voltage is added to the input signal and applied to the gate of the main PMOS switch, M_1. Capacitor C_b, connected to the gate of M_1, is charged between 2x V_{DD} and V_{DD}, avoiding the need of an NMOS switch which would create a leakage current when the M_1 gate node voltage is highly negative. S_2 has to be implemented with an NMOS controlled by a CP circuit. Summing up, this example combines the bootstrap gate control with the BS technique described earlier. The bulk of the main switch M_1 is connected to the input terminal through S_1 when is ON, and to V_{DD} through S_3 when it is in the OFF state.

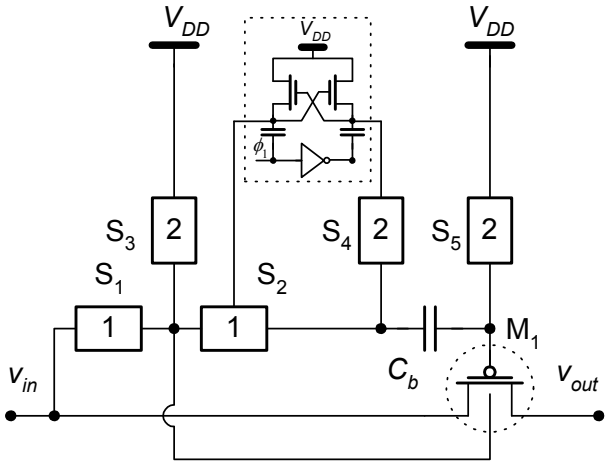


Figure 5.10: PMOS bootstrapping circuit diagram

The simulated circuit is displayed in Figure 5.11. The NMOS devices sized with aspect ratio 1/0.13, the PMOS with 4/0.13, the main switch M_1 with 20/0.13, the voltage doubler capacitors (C_a) with 200 fF each, and the boosting capacitor (C_b) with 400 fF.

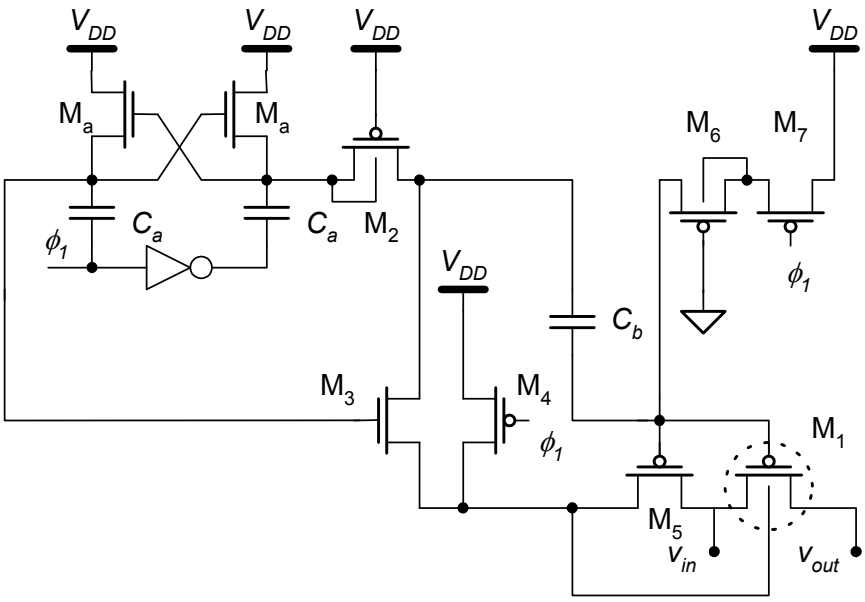


Figure 5.11: PMOS bootstrapping circuit diagram.

The clock signal ϕ_1, with a 50 MHz frequency, is used. The input signal of 0.25 V peak-to-peak amplitude and 10 MHz frequency is used as well. The M_2 device, and the M_6 and M_7, charge the boosting capacitor in the OFF state. The main device bulk is pushed to V_{DD} through M_4. During the ON state (ϕ_1 high), the input is tracked by M_5 and M_3 to the upper capacitor plate, and then the capacitor imposes a negative gate-to-source voltage to M_1.

The simulated results are shown in Figure 5.12(a) and (b). Comparing these results with the results shown in Figure 5.7, obtained in similar conditions for the NMOS case, it can be observed that the PMOS conductance has a lower value, approximately 75% less relatively to the NMOS case, said value being defined by the different mobility. The CBTp shows a lower efficiency, but on the other hand, it shows the bulk-switching action, as the conductance has no visible variation due to input signal swing.

Some authors suggest reducing the body effect of the PMOS switch, instead of using the BS, by applying a controlled voltage to the bulk in such a manner that the gate-to-source and the bulk-to-source voltages are constant during the ON state [78].

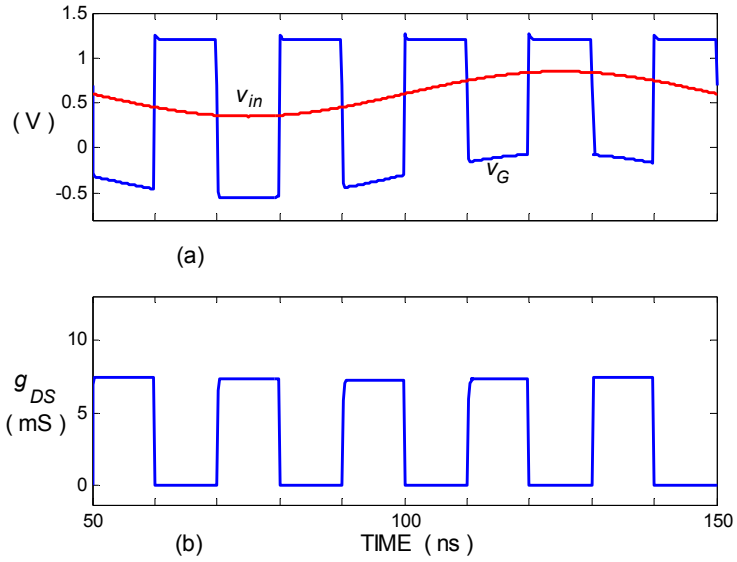


Figure 5.12: PMOS bootstrapping circuit simulated results; (a) Input and gate voltages; (b) Switch conductance

For both, the CBTn and the CBTp circuits, the conductance of switches becomes practically constant over a rail-to-rail signal swing, resulting in reduced distortion of a sampled signal. However there is still a major drawback. In all clock-bootstrapping circuits there are always reliability issues that have to be taken into account [76], (*i.e.* v_{DS}, v_{GS}, $v_{BS} >> V_{DD}$), and in order to overcome overstress and leakage problems, resulting in a complex circuit with many transistors. Moreover, to deal with these problems, several "flavours" of devices are normally employed in CBT circuits (*e.g.* 3.3 V devices in a 1.2 V shared technology). This substantially increases the cost of the ICs.

When compared with the CBTn circuit, the CBTp version is better due to the possible reduction of the body effect in the main switch transistor, revealing a higher importance when the differential schemes are not used [79]. On other hand, to accomplish a given conductance value, the CBTn main switch can be much smaller than the main switch used in a CBTp, which can be determinant for the designer as the clock feed-through and charge injection errors will be reduced.

5.3. Using feedback SC structures to overcome the switches limitations

The non-ideal behavior of the switches implies that a simple S/H circuit, as the one shown in Figure 5.1, has a limited performance. The finite conductance, the charge injection and the clock feed-through, are among several sources of error. Another source of error is the sampling jitter error due to the threshold voltage value and to the clock signal (rise and fall) transition time. The real clock waveforms have non-zero transition time, and the switch enters the ON state only when the clock signal (applied to the gate) is one transistor threshold voltage higher (for the NMOS case) than the input voltage. Also the turn-OFF is delayed. Then, as the input signal swings, the real sampling period of time is not constant.

Introducing a feedback in the S/H circuit can prevent or reduce some of those errors. One simple implementation is shown in Figure 5.13, assuming for simplicity, infinite gain and unity gain amplifiers [80]. The input impedance is highly increased, but the overall performance does not improve. Moreover, the speed of operation can be degraded, as the first amplifier will saturate during the holding period.

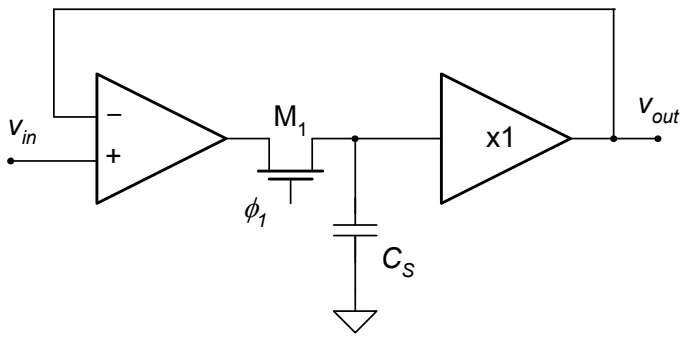


Figure 5.13: S/H circuit with feedback loop and with high input impedance [80].

An improved version of this circuit is shown in Figure 5.14 [80], with the capacitor placed in the feedback path, and with two ideal amplifiers. The main advantage of this circuit is to avoid the signal dependency of the charge injected by switch M_1. In fact, during the sampling period, the drain and the source voltages of M_1 are kept close to the ground (or reference) voltage. During the M_1 turning-OFF, the charge injected and clock feed-through effect are not reduced, but are signal independent.

Another advantage is obtained by the use of M_2. If the ground is replaced by a reference voltage close to the input signal reference level, it is clear that the switch M_2 fixes the first amplifier output to that level during holding period, and then, the first amplifier will track faster the input signal, during the next period, and the overall speed of operation is restored.

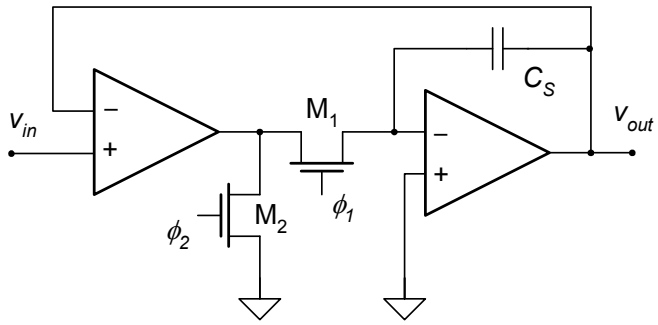


Figure 5.14: S/H circuit with capacitor placed in the feedback path [80].

Since both circuits in Figure 5.13 and Figure 5.14 require two amplifiers to build a S/H circuit, we strongly believe that this solution is not viable from the power efficiency point of view. However, the idea of using feedback to overcome the switches limitations can be further explored in future work.

5.4. The SO technique

The reduced supply voltage of the amplifiers has negative impact on the biasing schemes. The transistors of the amplifier need to operate in the saturation region, with the drain-to-source voltage higher than the effective gate voltage. High equivalent impedance implementations become more difficult. Morever, the output stage drive design presents additional limitations. Figure 5.15 shows a simplified output stage of an amplifier where M_1 represents the common-source amplifying device and M_2 the biasing current source.

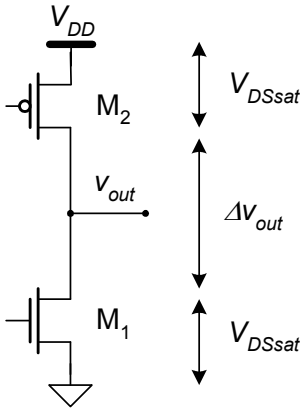


Figure 5.15: Output stage of an amplifier.

The minimum power supply voltage is the sum of the two V_{DSsat} with the output voltage swing, Δv_{out}, assuming the output voltage swing is higher than the sum of the two threshold voltages.

The constraints imposed to the supply voltage by the switches in the signal path are more restrictive. Taking an NMOS switch as an example, the minimum supply voltage (applied to the gate in the ON state) is the sum of the maximum signal amplitude, or voltage swing, Δv_{out}, with a V_{DSsat} and also with the gate-to-drain voltage, equal to the threshold voltage, V_{TO}.

Not all the switches are problematic when operating with low supply voltage. Driving the switches with the source connected to V_{DD} or ground is not so difficult, but driving the switches in the signal path, with terminals connected to the signal voltage swing, presents difficult issues. As stated previously, the increase of the gate overdrive, using CBTs or reduced threshold devices, is a possible solution. The main function of these switches is to isolate the different blocks of a circuit, to allow the execution of its particular function. Another solution is to disable (or to place in high impedance state) the output of the amplifiers of the different blocks, alternatively. That can be achieved by introducing control switches in the amplifier, disabling the current mirrors and preventing the output transistors from discharging the next stage capacitor.

The switched-OpAmp (SO) technique [81][82] has been used to overcome these driving drawbacks. In conventional schemes, the switches requiring an extra overdrive voltage are located mainly at the amplifier output, and the switches affording the amplifying or holding phases are in the signal path. In the circuits taking advantage of the SO technique, all problematic switches are removed in the signal path and the amplifier itself takes the function

of switching-ON and switching-OFF between the different phases or processes. In Figure 5.16, a simple single ended SO is shown, in charge redistribution topology, widely used in S/H and multiplying digital-to-analog converter (MDAC) blocks [83][84].

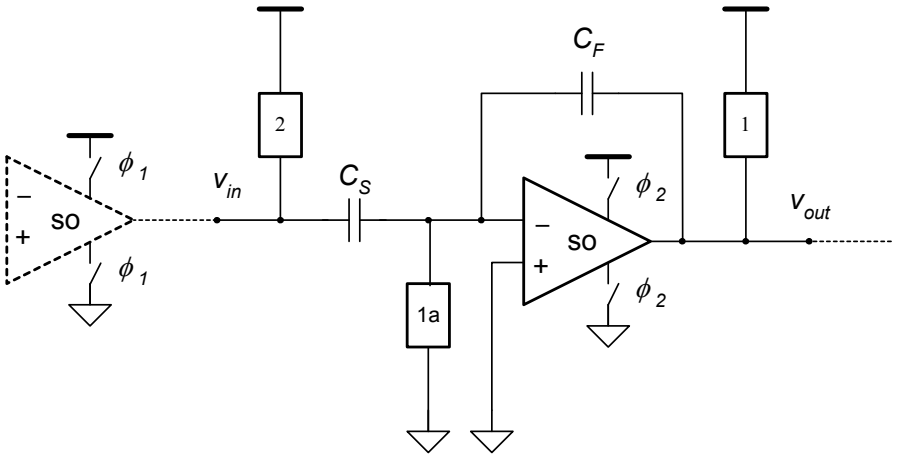


Figure 5.16: Representation of a SO based block.

The advanced phase ϕ_{1a} is the first to fall, as indicated in Figure 5.17, opening the top-plate switch, making the injected charge mainly signal independent.

Only after the drop of ϕ_{1a} the drop of ϕ_1 occurs, the output stage of the amplifier of the previous block is switched OFF, and the output of the amplifier of the actual block is released, with reduced charge injection. During phase ϕ_2, the switched-amplifier is activated and the capacitor top plate is tied to the reference voltage, also with reduced charge injection.

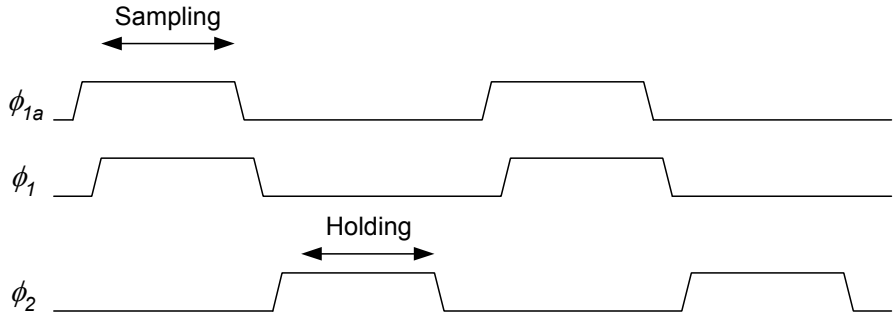


Figure 5.17: SO clock signals sequence.

On a first approach, only three clock signals are required. However, since both NMOS and PMOS switches are usually used, there is also a need to generate the complementary versions, resulting in ϕ_1, ϕ_2, ϕ_{1a}, ϕ_{1n}, ϕ_{2n}, ϕ_{1an}.

5.5. Reliability constraints

5.5.1. Oxide breakdown

The breakdown characteristics of the oxide have been always taken into account, more now, due to the ongoing down scaling.

A thinner gate oxide allows for a higher gate capacitance, then a more effective control over the gate. However, this can increase the leakage current and decrease the device reliability. It is a compromise. The reduction of the device size and the thinning of the oxide thickness usually happen simultaneously with the lowering of the supply voltage. This logic procedure gives the designers a safety feeling and induces to an easy scaling. However, and eventually, the models created to explain the breakdown phenomena need to be adjusted to address the challenges introduced by the advanced technologies.

The reliability is a probability related variable, and the number of fail events is related with technology, quality, thickness and applied voltages, among other parameters, and also with the period of time under operation. It is accepted that the failure will always occur. What needs to be established is the probable life span that can be guaranteed. The insulating failures, due to implant and general manufacturing process malfunction, occur for low electric field voltages and are promptly and easily detected. Failures occurring when large transient voltages are applied, will always be a problem, but are usually reduced or solved on another design level. Special attention should be drawn to those failure events caused by operation conditions, like voltage and temperature, close to the considered nominal conditions. The value of the time dependent dielectric breakdown (*TDDB*) is relevant. Another important value is the effective oxide thickness, t_{oxeff}: An oxide with defects, where holes can be trapped and then carriers can flow more easily, can be seen as having an effective thickness shorter than the geometric thickness.

The appearance of electrons in the oxide can have several origins, pursuant to different theories. It can originate in a stable electron from the p-Si well, also called steady state or cold

electrons, that undergo Fowler-Nordheim tunneling from cathode conduction band to the anode or gate conduction band through the oxide conduction band [85][86]. It can also be accelerated electrons coming from the drain side [87], called ballistic or hot, after ionization by impact from high energetic electrons coming from the source, and accelerated by the drain-to-source voltage.

But, in the presence of very low oxide voltages, even for lower voltages than barrier height, electrons can tunnel directly from cathode well to anode gate, without using the oxide conduction band [88]. Electrons injected into the oxide, gain energy from the oxide field when going toward the gate. The oxide voltage plays an important rule, as it directly determines the energy.

If defect points are present, positive traps, an easier and faster path can be found [89]. If the energy is enough to break silicon covalent bonds, new traps are created, initially and mostly at the gate to the oxide interface. But the energy is a function of the length during which the electron is accelerated. So, if more traps are created, the shorter the length will be, and lower energy will be gained by the electrons. Therefore, the number of new generated traps is an inverse function of the actual existing traps. The process has a self controlled behavior, where the number of traps is a square root function of the stress time.

The breakdown occurs if the number of positive trapped holes is enough to allow a current through the oxide. After the initial breakdown event, the following events occur for a lower and lower oxide voltage [90]. This indicates that a permanent damage is produced, and that the damage weight will increase. The degradation and breakdown of thin oxides is different from the thicker films [91]. The oxide electron transport is almost direct, and the new traps creation near the gate interface is caused by the cooperation of several electrons and it is strongly a function of oxide voltage. The creation of new traps may occur with less energetic electrons, even with electrons having, individually, less energy than that which would be necessary to break the bonds. There is a reduction of the self controlled process, being the number of new traps a linear function of the stress time.

Also for thinner oxides special attention should be taken with the difference between gate and oxide voltage. The oxide voltage is lower than the gate voltage by the band gap energy, the band bending near the two interface surfaces, and dopant differentials [92]. It may not so

relevant for the reliability question, as the drift between values is quite constant and the life span can be expressed as a function irrespective of its being oxide or gate voltage [86][93], however, for low stress voltages, the oxide voltage should be considered instead of the gate voltage [94].

Although the exact mechanism and the calculation and projection of the time dependent dielectric breakdown is under discussion and object of ongoing research, the *TDDB* can be represented approximately as an exponential function [92] of oxide field, or as "$1/E_{ox}$", or as "$-E_{ox}$".

Accepting the approximation of the first model, the life time integral can be expressed by (5.2), being $\tau_C(T)$ and $G_C(T)$ temperature dependent parameters and $E_{ox}(t)$ the time dependent oxide field.

$$\int_0^{TDDB} \frac{dt}{\tau_C(T)\, e^{\frac{G_C(T)}{E_{ox}(t)}}} = 1 \qquad (5.2)$$

Solving the integral for a constant oxide voltage, one obtains (5.3).

$$TDDB = \tau_C(T)\, e^{\frac{G_C(T)}{E_{ox}}} \qquad (5.3)$$

For a defect free oxide, a thirty year life time is accepted when applying a 7.5 MV/cm field, at 300ºK. The parameters values, for that temperature, are respectively 10^{-11} s and 350 MV/cm [72][95].

The oxide field can be expressed as the oxide voltage and the thickness ratio, obtaining the equation (5.4). The effective thickness, with a lower value than the geometric thickness, implicitly holds the technology and manufacturing processes characteristics.

$$TDDB = \tau_C(T)\, e^{\frac{G_C(T)\, t_{oxeff}}{V_{ox}}} \qquad (5.4)$$

However, as the oxide becomes thinner, the "$-E_{ox}$" model seems to better represent the breakdown mechanism [88], and equation (5.5) is accepted instead, being $\tau_B(T)$ and $\gamma_B(T)$ the new parameters [96].

$$TDDB = \tau_B(T) e^{-\gamma_B(T) E_{ox}} = \tau_B(T) e^{-\gamma_B(T)\frac{V_{ox}}{t_{oxeff}}} \qquad (5.5)$$

Furthermore, it is again emphasized that the reliability projection should be performed based on the oxide voltage [88], instead of on the oxide field, particularly when thin oxides and low voltages are used. Both models point to a dramatic time projection reduction even for a small voltage increase. But in switched circuits, the duty cycle also offers a huge extension. In switched circuits the time projection is not only directly dependent on the inverse of the duty cycle, but also on the transition periods of time and the frequency with they happen.

For the simple SC circuit illustrated in Figure 5.1, being the NMOS device sized with aspect ratio 5/0.13, the capacitor C_S= 1 pF initially discharged, for a step voltage v_G= 1.2 V with 50 ps rise time at 1 ns and applied between the gate and the output, if the input voltage falls at 2 ns from 1.2 V to zero with 50 ps fall time, the simulation results can be observed in Figure 5.18(a) and (b).

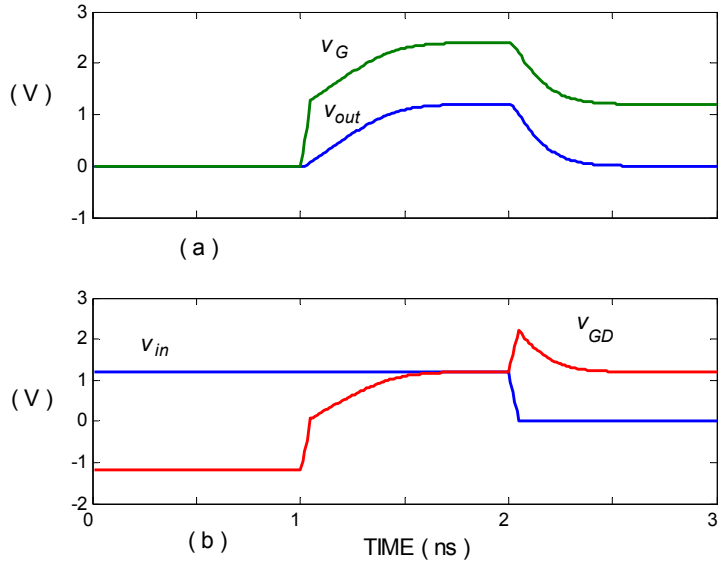


Figure 5.18: NMOS sampling circuit with input voltage fall; (a) Gate and output voltages; (b) Input and gate-to-drain voltages.

The gate-to-drain voltage, v_{GD}, presents an absolute peak value close to 2x1.2 V, the gate-to-source voltage still being limited to 1.2 V. The oxide at the physical drain side will support a much higher value than would be desirable, and then, the time failure projection will be reduced. That reduction will be a function of the decay time and its following settling-time, and of the frequency.

Thus, the use of bootstrapping auxiliary circuits to improve the conductance sets a reliability constraint, and the utilization of thinner oxides makes said restriction increasingly relevant.

5.5.2. The latch-up problem

The latch-up problem is due to the parasitic NPN and PNP transistors formed by the CMOS implementation. Figure 5.19 shows a simple diagram with a PMOS device in a n-well and the NMOS on the p-substrate. The PMOS terminals, bulk, source, drain and gate, are shown as pB, pS, pD and pG, and the NMOS terminals in a similar way.

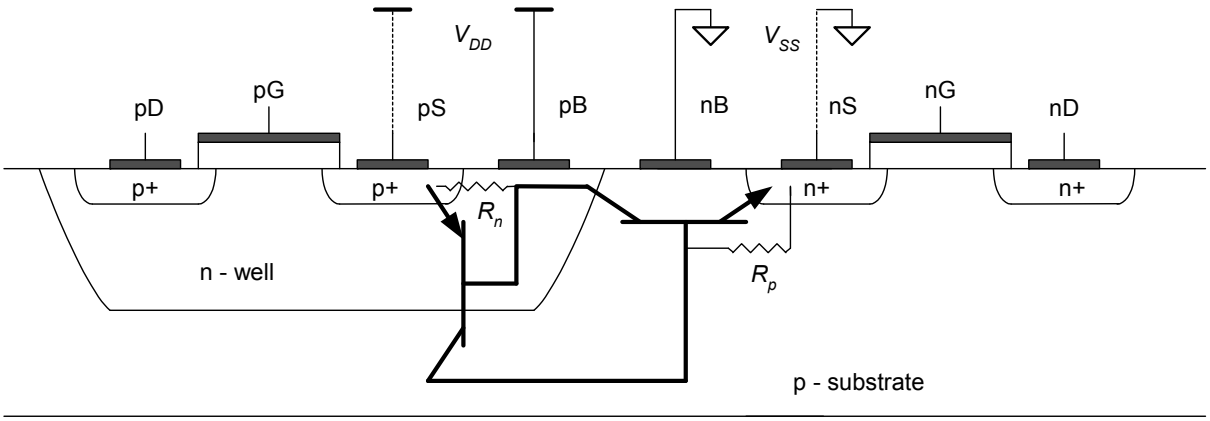


Figure 5.19: CMOS and parasitic transistors.

The PNP and NPN transistor formed a PNPN device that can be triggered as a ordinary silicon controlled rectifier. For that, is enough that the PMOS source, the emitter from the parasitic PNP, be raised up to a junction potential above the PMOS bulk, the parasitic transistor base. Then, the PNP can trigger the NPN, and a short circuit is established from the PMOS source to the NMOS source. Also a short will exist from the PMOS bulk, usually connected to the positive supply, to the NMOS source. If the NMOS source is pulled below

the negative supply, it will be the NPN to initialize the short circuit event. This latch-up problem also points to the care that should be taken when overdriving control voltages in switched circuits, as in bootstrapped auxiliary circuits.

5.6. Switch-linearization circuit (SLC)

5.6.1. The SLC approach

As stated in the previous Chapters, using CMOS technology a switch can be built by paralleling an NMOS and a PMOS device [52]. The first advantage of having a CMOS switch rather than a single-channel metal-oxide-semiconductor (MOS) switch is that the dynamic analog signal range in the ON state is greatly increased as illustrated by the conductance curves (dashed lines) in Figure 5.20. These conductance curves are obtained from DC electrical simulations using a standard 1-Poly, 8-Metal 1.2 V 130 nm CMOS technology and BSIM3 models, with V_{Tn}≈0.38 V, $|V_{Tp}|$≈0.33 V. The NMOS and PMOS devices are respectively sized with aspect ratios of 20/0.13 and 80/0.13. The values of the conductances shown in Figure 4.1 (and some other subsequent Figures) are the values directly provided by the SPICE circuit simulator.

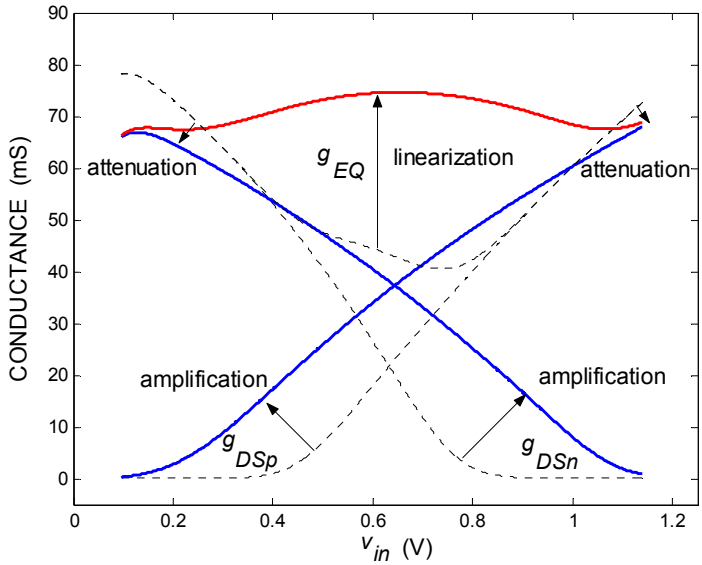


Figure 5.20: Changes in the NMOS, PMOS and equivalent (g_{EQ}) switches conductances using the proposed technique versus input signal.

A CMOS switch allows a full signal-swing. However, at low supply voltage operation, the equivalent switch conductance, g_{EQ}, has a huge variation, which results in a significant total harmonic distortion (THD).

One of the reasons relies on the fact that, as stated in previous Chapters in this Thesis, the drain-to-source conductance, g_{DS}, of a single MOS switch (NMOS or PMOS) operating in the linear region is a function of the mobility in the channel, μ, the oxide capacitance per unit area, C_{ox}, the gate width and length, W and L, the gate-to-source voltage, v_{GS}, the threshold voltage, V_T, as represented by $g_{DS} = \mu C_{ox} W(v_{GS} - V_T)/L$. Scaling the device and lowering the oxide thickness, the capacitance per unit area is increased resulting in an increased conductance. However, that is canceled out by the variation of the effective gate overdrive voltage $(v_{GS} - V_T)$. Considering the scaling factor k [10], and that both the gate-to-source and the threshold voltages are lowered by $1/k$, the conductance is also lowered by $1/k$. On the other hand, as the threshold voltage is not scaling as fast as the supply and available gate-to-source voltages, the conductance is deteriorating with scaling. Not only the maximum achievable conductance is reduced, but also the linearity of the conductance is highly reduced with supply voltage, as the relatively increased threshold voltage is shrinking even more the signal amplitude span. As a consequence, the use of very low signal levels and the use of common-mode signal levels close to one of the supply rails become mandatory. Furthermore, the body effect implies a threshold voltage variation, additionally increasing it for signal (source-to-bulk) increased voltages, and shrinking even more the signal swing.

The basic idea behind the SLC circuits [2][1] consists on attenuating the gate-to-source voltage and conductance of the NMOS switch, g_{DSn}, when low values of input signal, v_{in}, are applied, and amplifying them for higher values of v_{in}. For the PMOS switch the process is similar. The main goal is to obtain a nearly constant equivalent conductance g_{EQ}, independent on v_{in}, as shown in Figure 5.20.

A different approach to obtain nearly constant-conductance operation is to hold the gate-to-channel voltage constant during the ON state. This is obtained by using the clock-bootstrapping techniques. These techniques consist of using dedicated SC circuits for boosting the gate voltage of a single NMOS switch (CBTn case) beyond the power supply voltage [73], with a value close to $v_G = V_{DD} + v_{in}$, or, as an alternative, reducing the gate voltage of a PMOS switch (CBTp case) [77], by a value close to $v_G = v_{in} - V_{DD}$. However, these CBT circuits have

two major drawbacks as discussed earlier: 1) they suffer from over-stress of the gate capacitances (for example the gate to body) causing potential long-term oxide reliability problems; 2) usually they need charge pumps and extra leakage protection devices (for example cascode devices), reducing their area efficiency. Some authors propose alternative circuits [51][53], but either the gate voltage is not controlled, or the gate voltage is not input signal dependent.

5.6.2. Circuit architecture

The proposed circuit architecture for the new SLC circuits is shown in Figure 5.21. In the upper half-part is the PMOS switch-linearization circuit, SLCp, and in the lower half-part the NMOS linearization circuit, SLCn.

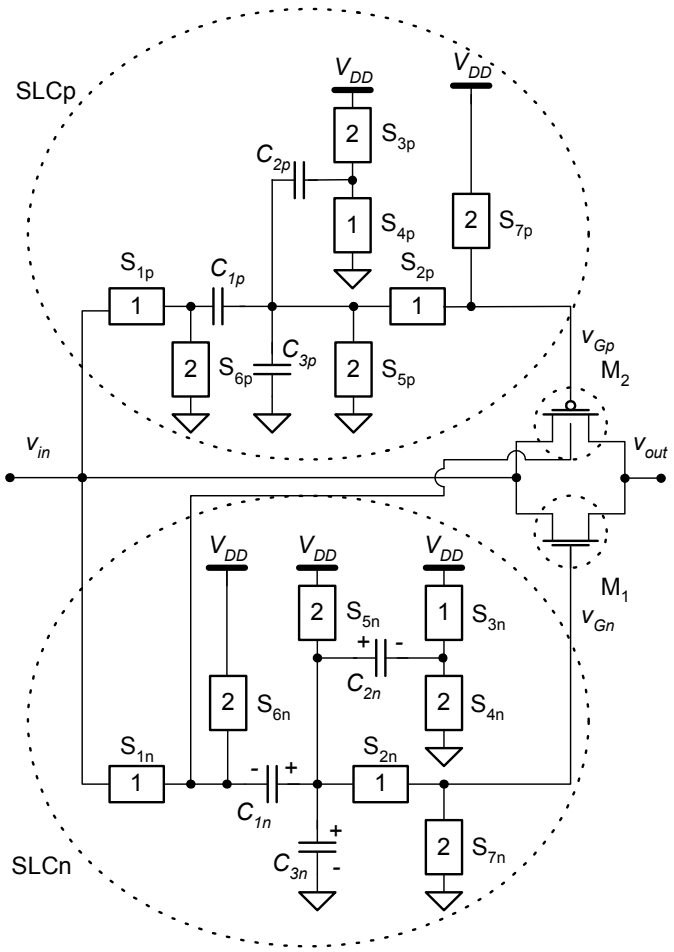


Figure 5.21: n-type and p-type SLC simplified schematic.

The SLCn circuit, driving the NMOS switch, M_1, operates as follows. During the OFF period, clock-phase ϕ_2, switch S_{7n} assures M_1 is OFF, S_{5n} charges capacitors C_{2n} and C_{3n}. During the ON period, clock-phase ϕ_1, S_{1n} and S_{3n} are ON, connected to v_{in} and to V_{DD}, forcing a redistribution of charges in the capacitors, and then the voltage in the capacitors common node is a function of those values, namely the v_{in} voltage value. S_{2n} delivers that controlled voltage to the main switch gate.

Therefore, when the input signal, v_{in}, is close to V_{SS}, the n-type SLC block reduces the gate voltage that is applied to the NMOS switch to a value lower than V_{DD}. As a result, its conductance is reduced. When v_{in} is close to V_{DD}, the SLCn circuit increases the gate voltage, overcoming the zero-conductance problem of the NMOS transistors when $v_{in} > V_{DD} - V_{Tn}$.

The charge conservation-table is shown in Table 5.1, for the n-type SLC circuit. In the transition from phase ϕ_2 to ϕ_1, there is charge conservation in node v_{Gn} (high impedance) and we get equation (5.6).

$$0 + V_{DD}C_{2n} + V_{DD}C_{3n} = (v_{Gn} - V_{in})C_{1n} + (v_{Gn} - V_{DD})C_{2n} + v_{Gn}C_{3n} \quad (5.6)$$

Table 5.1: Charge conservation-table for the n-type SLC circuit.

Q_C	ϕ_2	ϕ_1
C_{1n}	0	$(v_{Gn} - v_{in})C_{1n}$
C_{2n}	$V_{DD}C_{2n}$	$(v_{Gn} - V_{DD})C_{2n}$
C_{3n}	$V_{DD}C_{3n}$	$v_{Gn}C_{3n}$

The generated output voltage, v_{Gn}, to drive the switch, approximately (neglecting parasitic effects) is given by (5.7).

$$v_{Gn} = v_{in}\frac{C_{1n}}{C_{1n} + C_{2n} + C_{3n}} + V_{DD}\frac{2C_{2n} + C_{3n}}{C_{1n} + C_{2n} + C_{3n}}, \quad (5.7)$$

where C_{1n}, C_{2n} and C_{3n} are small capacitors of a given size, the smaller one being C_{3n}. For the p-type SLC circuit used to provide the suitable gate voltage to the PMOS switch, the analysis is similar and relatively straightforward. A slightly different linearization circuit is used to

provide the suitable gate voltage, v_{Gp}, defined approximately by (5.8), where C_{1p}, C_{2p} and C_{3p} represent small capacitors, the smaller one being C_{1p}.

$$v_{Gp} = v_{in}\frac{C_{1p}}{C_{1p}+C_{2p}+C_{3p}} + V_{DD}\frac{-C_{2p}}{C_{1p}+C_{2p}+C_{3p}} \tag{5.8}$$

In order to keep the capacitance values of the auxiliary capacitors used in the SLC circuits as low as possible and within a practical range, the effect of the gate capacitance of the main switches M_1 and M_2, C_{gn} and C_{gp} respectively, must be considered. The weight of the gate capacitances should be added to the first item in (5.7) and (5.8).

The second item should be corrected with the added charge, approximately the gate capacitance charge at $V_{DD}/2$. Hence, the SLCn circuit generates an output voltage, v_{Gn}, to drive the switch, approximately given by (5.9). The capacitance ratios, K_{1n} and K_{2n}, defined in (5.9) will be used later for simplicity.

$$v_{Gn} = v_{in}\underbrace{\frac{C_{1n}+C_{gn}}{C_{1n}+C_{2n}+C_{3n}+C_{gn}}}_{K_{1n}} + V_{DD}\underbrace{\frac{2C_{2n}+C_{3n}+C_{gn}/2}{C_{1n}+C_{2n}+C_{3n}+C_{gn}}}_{K_{2n}} \tag{5.9}$$

The output voltage, v_{Gp}, to drive the PMOS switch, is given by (5.10), where the capacitance ratios K_{1p} and K_{2p} are set.

$$v_{Gp} = v_{in}\underbrace{\frac{C_{1p}+C_{gp}}{C_{1p}+C_{2p}+C_{3p}+C_{gp}}}_{K_{1p}} + V_{DD}\underbrace{\frac{-C_{2p}+C_{gp}/2}{C_{1p}+C_{2p}+C_{3p}+C_{gp}}}_{K_{2p}} \tag{5.10}$$

Notice that the bulk-switching (BS) technique [49] is also applied to the main PMOS switch, M_2, but no additional switches are required since the SLCn circuit provides, in a direct way, the required voltage to the bulk of M_2.

5.6.3. Practical implementation

The practical implementation of the technique described in the previous Section can be done using the two dedicated SLC circuits, n-type SLCn and p-type SLCp, represented in Figure 5.22.

The complete SLC circuit is optimized based on the previous analytical expressions and following the five steps methodology (a simplified flow-chart of the several steps is provided in Figure 5.23) described next. All auxiliary NMOS and PMOS devices are sized with aspect ratios of 1/0.13 and 4/0.13 respectively, and the main switches with aspect ratios of 20/0.13 and 80/0.13.

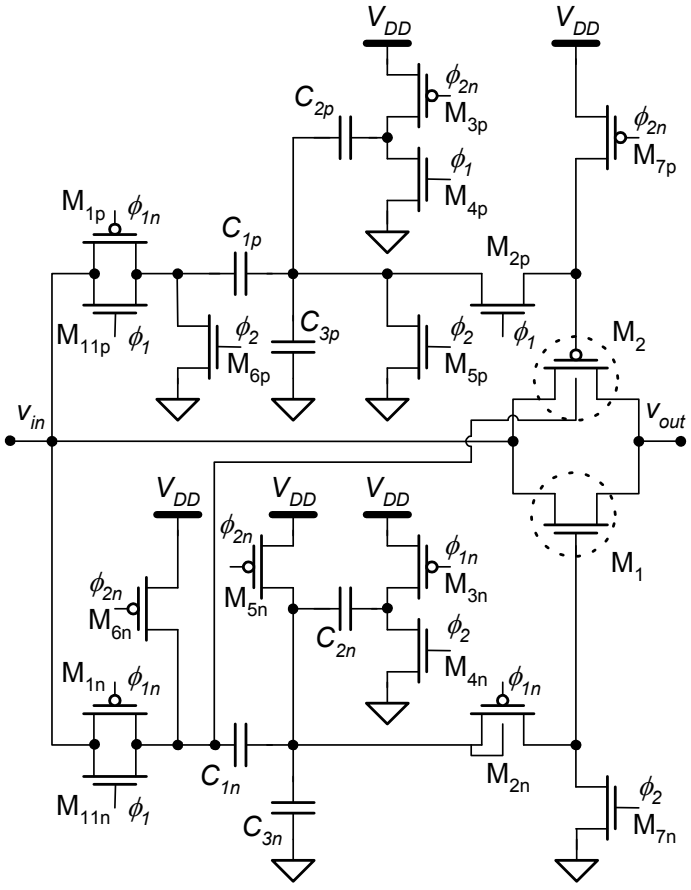


Figure 5.22: n-type and p-type SLC practical realization.

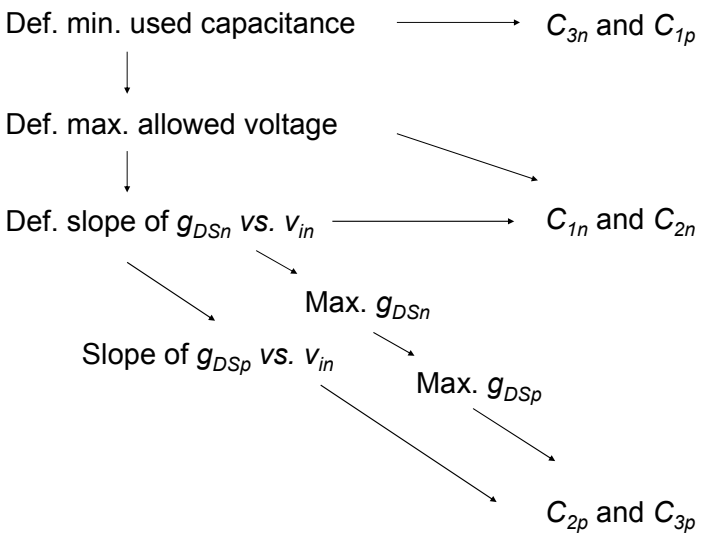


Figure 5.23: Simplified flow-chart of the main steps to optimize the sizing the auxiliary capacitors used in the SLCn and SLCp circuits.

STEP 1: Definition of the lowest practical capacitance value to be used, which will be initially applied to C_{3n}. It is assumed 30 fF in order to guarantee that, in post-layout simulations, the circuit does not become very dependent on parasitic effects. Likewise, later on for the SLCp block calculations, a similar initial value is accepted for capacitor C_{1p}.

STEP 2: Definition of the maximum value allowed for v_{in}. It is defined as 90% of V_{DD}. This value will determine the v_{Gn} maximum value, which should be lower than the sum of the supply and junction voltages. In order to avoid leakage currents, latch-up and the need of adding any protection circuits, a conservative value $V_{DD}+ V_{Tn}$ is used. Replacing these values in (5.11), and using the computed gate capacitance values, a first relation between K_{1n} and K_{2n} is obtained.

$$0.9K_{1n} + K_{2n} - 1 < V_{Tn} / V_{DD} \qquad (5.11)$$

STEP 3: Taking into account the slope of v_{Gn} as a function of v_{in}, the K_{1n} factor should cause an amplification for low v_{in} values and an attenuation for high values. If this factor is close to unity the circuit will be similar to a conventional CBT switch; if it is zero it will result in a conventional NMOS switch. Then the targeted value for K_{1n} term is 0.5 (one half). As a result, a second relation is obtained, and using the computed gate capacitance values, then C_{1n} and C_{2n} can be computed and sized with 100 and 80 fF, respectively. The sum of these values should

be sized one order of magnitude higher than the gate capacitance of the main device, C_{gn}, attenuating its nonlinear influence and ensuring an effective control of the gate voltage, v_{Gn}. Otherwise, the initial value set for C_{3n} must be set higher.

STEP 4: The NMOS switch maximum conductance value, close to 65mS for $v_{in} \approx 0$, as depicted in Figure 5.20, should be made equal to the maximum conductance of the PMOS switch, for $v_{in} \approx 0.9\,V_{DD}$. Being the CMOS switch sized asymmetrically, the effective gate voltage absolute value of the NMOS and PMOS switches should be the same in these two conditions. Then (5.12) is obtained, which sets implicitly a first relation between C_{2p} and C_{3p}.

$$0.9K_{1p} + K_{2p} = 0.9 - K_{2n} + V_{Tn} / V_{DD} - \left|V_{Tp}\right| / V_{DD} \qquad (5.12)$$

STEP 5: The slopes of g_{DSn} and g_{DSp}, as a function of v_{in}, should be symmetrical as seen in Figure5.20. The g_{DSn} slope is affected by the body factor γ_n, surface potential $2|\Phi F|$ and input signal. Hence, the slope of v_{Gp} will have a lower value than the slope of v_{Gn} (in absolute value). Then a second implicitly relation between C_{2p} and C_{3p} can be set by (5.13).

$$K_{1p} = K_{1n} - \gamma_n / 2\sqrt{v_{in} + 2\left|\Phi_F\right|} \qquad (5.13)$$

The value found for K_{1p} is 0.24, for a v_{in} DC level value of $V_{DD}/2$. Then C_{2p} and C_{3p} are computed and sized with 150 and 330 fF, respectively, and C_{1p} is sized with 30 fF, as previously stated. These values are higher than the gate capacitance of the main device, C_{gp}, and, therefore, are acceptable.

5.6.4. Simulated results and reliability

5.6.4.1. Distortion

For comparison purposes, a complete 50 MS/s flipped-around fully-differential S/H circuit, as shown in Figure 5.24, is designed. The SLC switches and circuits are sized as stated in the

previous Section. The V_{HI} voltage is 0.8 V, switches S_{3p} and S_{3n} are implemented with PMOS switches with an aspect ratio of 40/0.13.

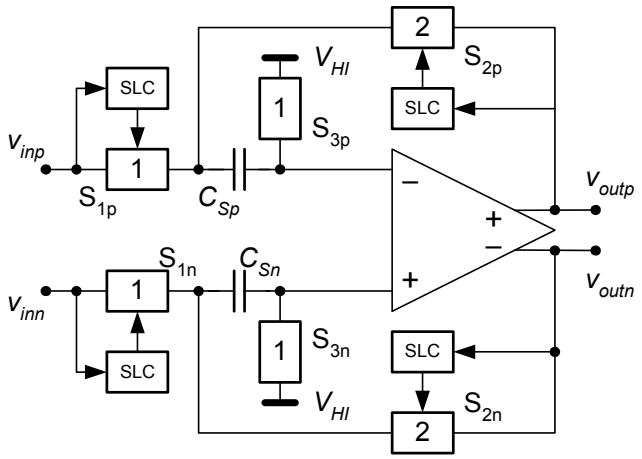


Figure 5.24: Flipped-Around S/H Circuit. Four different SLC or CBT circuits are required to drive the four switches in the signal path.

Normalized sampling capacitors, C_{Sn} and C_{Sp}, with 4 pF are used. The output common-mode (V_{CMO}) is set to 0.55 V. Figure 5.25 displays the simulated total harmonic distortion (THD) for the S/H circuit output signal ($v_{outp} - v_{outn}$), sampling at F_S = 50 MS/s. Four different linearization techniques are considered: 1) conventional CMOS (conv. CMOS); 2) CBTn; 3) SLC with bulk-switching (SLC-BS); 4) CBTp with bulk-switching (CBTp-BS).

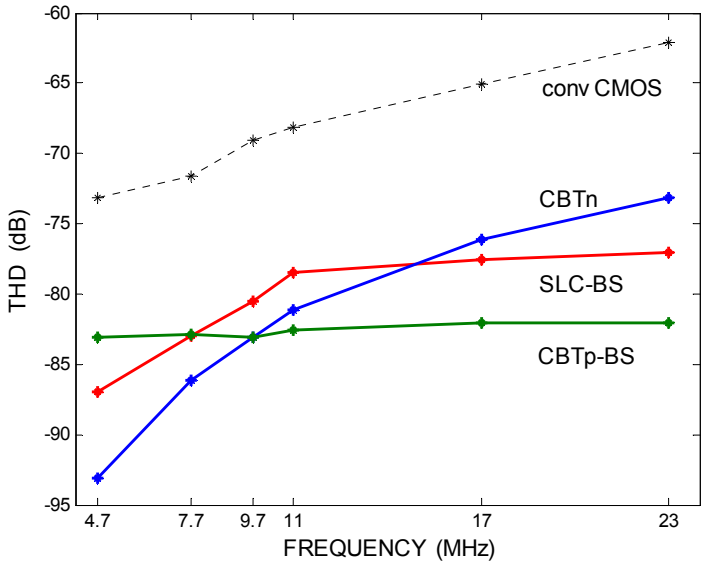


Figure 5.25: THD of a fully-differential flip-around S/H circuit for the 4 different techniques versus input signal frequency.

A differential input signal amplitude of ±0.5 V_{pp}, for six different frequencies (4.7, 7.7, 9.7, 11, 17 and 23 MHz), is used. For comparison purposes, the sums of the auxiliary capacitors used in the circuits of the last three techniques, have the same value.

As it can be observed, using the proposed SLC-BS circuits, there is a significant improvement in the THD, when comparing with conventional CMOS switches. The THD performance of the SLC-BS circuit is nearly constant above $F_S/4$ (similar to the CBTp-BS), showing the influence of the applied bulk-switching technique to the PMOS element.

Increasing the input signal amplitude to a real rail-to-rail swing, the SLC-BS circuit shows an improved THD behavior over the CBT circuits, as shown in Figure 5.26 for an input signal with a frequency of 4.7 MHz. The reason is basically due to the fact that a transmission-gate is being used rather than a single NMOS or PMOS switch.

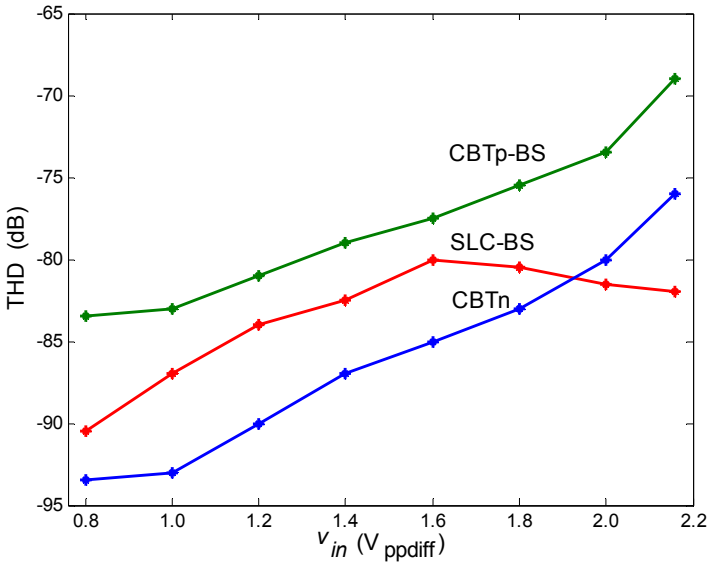


Figure 5.26: THD obtained for 4.7 MHz and large amplitude input signal.

5.6.4.2. Scalability and spread

Figure 5.27 displays THD simulations of the S/H for different sizing of the sampling capacitors, C_{Sn} and C_{Sp}, and of the width of main switches S_{1p} and S_{1n}. Multiplying factors of 0.25, 0.5, 2 and 4 are used.

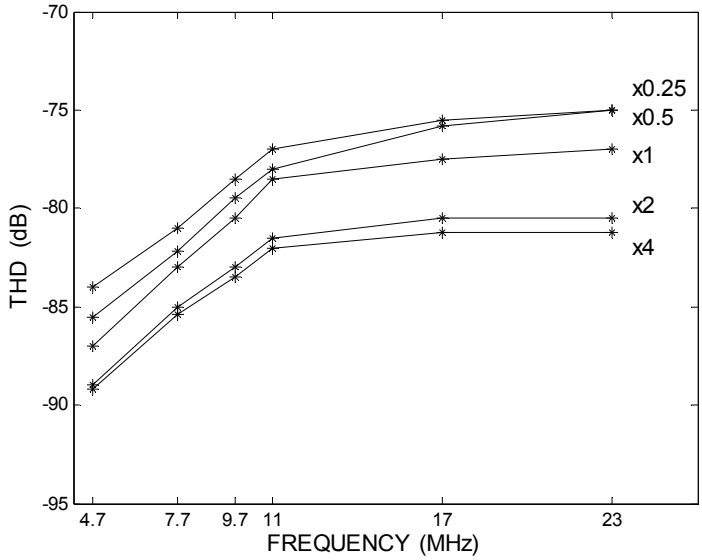


Figure 5.27: THD obtained for different main switches size.

The set of capacitors used in the corresponding SLC-BS circuits are calculated following the design methodology described previously. The maximum spread of the capacitance values is kept the same (around 11).

5.6.4.3. Corner analysis

Table 5.2 shows the simulated THD for 5 different corners (considered the most critical ones), using the typical (TT), slow (SS) and fast (FF) models provided by the foundry.

Table 5.2: Simulated THD for different process corners.

f_{in} (MHz)	4.7MHz	7.7MHz	9.7MHz	11MHz	17MHz	23MHz
TT, V_{DD}=1.2V xcap=0, +25ºC	-87	-83	-80,5	-78,5	-77,5	-77
SS, V_{DD}=1.08V xcap=+15%, +85ºC	-80	-77,5	-77	-76,5	-75	-74
SS, V_{DD}=1.32V xcap=+15%, +85ºC	-87	-84	-82,5	-79,5	-77	-76
FF, V_{DD}=1.32V xcap= -15%, -40ºC	-92	-89	-87	-85	-82,5	-81,5
FF, V_{DD}=1.08V xcap= -15%, +85ºC	-84,5	-81	-79	-77	-75,5	-74,5

Parameters V_{DD}, temperature and capacitors tolerance (*xcap*) are also considered. The circuit is simulated for an input signal amplitude of 1 V_{ppdiff} and for 6 different frequencies. As expected, the worst-case THD is achieved at Nyquist-rate and at a slow corner when V_{DD} is reduced by 10% and capacitances values increased by 15%. However, even in the worst-case, the THD is still compatible with more than 12 bits of linearity.

5.6.4.4. Reliability issues

Considering reliability issues [97][98][81], the SLC-BS solution is significantly better than the CBT ones. Figure 5.28 displays the gate voltages delivered to main switches when a 4.7 MHz input signal with ±0.5 V_{pp} amplitude is applied. The values are inside the range allowed by the used technology. Over-stress and leakage are not present, and complex circuits to prevent them are not necessary.

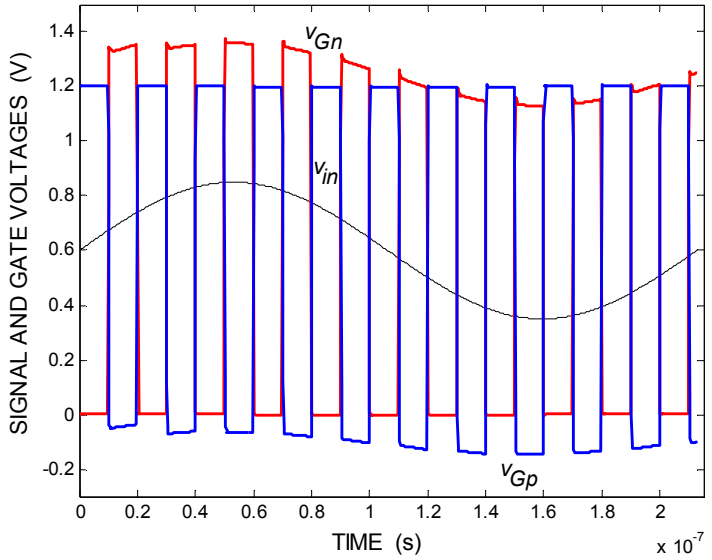


Figure 5.28: Gate voltages applied to the main switches for a ± 0.5V_{pp} input signal amplitude.

As illustrated, the highest NMOS gate voltage, v_{Gn}, is smaller than 1.38 V (+115% of the nominal V_{DD}), and the lowest PMOS gate voltage, v_{Gp}, is −0.15 V (−13% of V_{DD}). When CBTn and CBTp-BS circuits are used these values rise to about +186% and −76% of V_{DD}, respectively.

Hence, the reliability and lifetime projection are significantly improved by using the proposed SLC-BS circuit technique over any CBT solution. Furthermore, the SLC-BS circuit does not

require additional CP circuits and, as a result, the capacitance area efficiency is improved by a factor of about 2 when compared with the CBT solutions.

5.7. Conclusions

This Chapter described existing solutions to overcome the switches limitations, such as the CBT, feedback and SO techniques. In this Chapter is also presented and detailed a design methodology for improved switch-linearization control circuits to drive CMOS switches when very low distortions are envisaged.

Simulated results of a practical sample-and-hold circuit show that, using this technique, linearity levels compatible with 12-bit can be reached over the Nyquist band. It was also demonstrated that, additionally to better area efficiency, the gate stress voltages are reduced when compared with traditional CBT techniques, thus improving the reliability over existing clock-bootstrapping solutions. These two features make this technique more attractive than traditional clock boosting techniques for circuits requiring low distortion levels.

6. Electrical design and simulations of two silicon demonstrators

The principles and proposals, described in the previous Chapters, are used in this Chapter, in the practical design of two analog-to-digital converters (ADC). The first design, described in Section 6.1, is focused in the phase complexity problem, analyzing in detail and for the first time, the possibility of application of the single-phase technique to pipelined ADCs. This demonstration is made through electrical simulations in a design of a medium resolution ADC, operating at a low sampling rate. The second design, fully described in Section 6.2, demonstrates the feasibility of a high speed ADC, exploiting the particular characteristics of a passive sample-and-hold (S/H) topology, employing the proposed switch-linearization circuit (SLC), and making use of the open-loop residue amplification structure using amplifiers with local-feedback. High levels of area and power high efficiency are reached, for low/medium resolutions. Finally, Section 6.3 draws the most relevant conclusions of this Chapter.

6.1. Design of a 10-bit 4MS/s pipelined ADC using an hybrid CBT/SO approach and employing a single-phase clocking scheme.

The analogue switches in switched-capacitor (SC) circuits are operated by non-overlapping bi-phase control signals (ϕ_1, ϕ_2). The non-overlapping of these two switching phases is essential for successful SC operation, since a capacitor inside an SC circuit can discharge if two switches, driven by ϕ_1 and ϕ_2, are turned on simultaneously. Hence, to avoid any chance of overlap between ϕ_1 and ϕ_2, duty cycles of 45 to 49% have been used in practice, to allow the unavoidable variations in the finite rise/fall times of ϕ_1 and ϕ_2. Typically, periods of time when both phases are OFF, range from 100 ps to 2ns. Moreover, two additional phases, ϕ_{1a} and ϕ_{2a}, are generally used in many SC circuits, which are advanced versions of ϕ_1 and ϕ_2. These two additional phases overcome the problem of signal-dependent charge injection, by turning-off sampling switches connected to the inputs of the amplifiers slightly before the switches connecting the input signals to the bottom-plates of the sampling capacitors [44]. Since both NMOS and PMOS switches are normally employed, this four-phase scheme becomes a complex, six or eight phase scheme, due to the need to have complementary versions of phases ϕ_1, ϕ_2, ϕ_{1a} and ϕ_{2a} for driving the PMOS devices.

The technique proposed to be used here and initially demonstrated in [99] for a Sigma-Delta ADC, consists of driving all switches of the pipelined ADC using only a single clock phase, ϕ_1, and its complementary version, ϕ_{1n}. As theoretically shown in [100], as long as the fall/rise time-delay of the phases and the average equivalent conductance of the switches (g_{EQ}) during this overlapping time are both made small, the sampled signal degradation due to having various switches conducting simultaneously is negligible. With the evolution of CMOS technologies, the values of the time-delay and g_{EQ} are progressively being reduced. Hence, non-overlapping guard times might no longer be required in many SC circuits.

In the novel SLC circuits described in this Thesis (as well as in the existing CBT circuits), there is always an inherent delay between the input clock phase and the generated boosted output phase that drives the sampling switches. Hence, this single-phase scheme offers

another design simplification by eliminating the need to have delayed versions of the sampling phases, necessary to avoid any signal-dependent charge injection. Furthermore, during the sampling operation of the SO circuits, the signal-dependent charge injection added by switching off the output stage of the OpAmp is very small, even if delayed phases are not used. The reason is that the signal swing at the input of the output stage of a two-stage OpAmp is always very small, and therefore, the amount of charge that must flow out of the channel region is practically signal-independent.

These conclusions are demonstrated here in this Section thought a hybrid combination of the CBT and of the SO techniques in the complete design of a 10-bit pipelined ADC.

6.1.1. Introduction

As previously stated, this Section describes the application of a single-phase scheme to low-voltage pipelined ADCs designed in standard CMOS technologies. The single-phase technique was originally disclosured in [100] and demonstrated in silicon, for the first time, in a Sigma-Delta ADC [99]. The referred technique explores the gap between the high conductance region of PMOS and NMOS switches at low-power supply voltages and the fast clock transitions that exist in advanced CMOS technologies. To validate the theoretical findings and assess the performance of the proposed new technique, a 10-bit 4 MS/s pipelined ADC designed for a nominal supply voltage of 1.5 V (± 20%) with all switches driven by a conventional six-phase clock generator is designed and simulated in a standard 0.18 μm CMOS technology. For comparison purposes, the same ADC is simulated using only a single-phase for driving all switches, according to the proposed phase scheme. Simulated FFT results of the digital output of the ADC performed shows that, when the circuit operates at the minimum supply voltage (1.2V) and using the proposed and simplified phase scheme, the SFDR (dominated by the highest harmonic) is improved by up to 6 dB. The results clearly demonstrate that with the evolution of CMOS technologies non-overlapping guard times will no longer be required in medium conversion-rate ADCs. As a result, even for a circuit with a complexity of a 10-bit pipelined ADC, the conventional clock-phase generators are no longer required.

6.1.2. The single-phase technique

The basic idea behind the single-phase technique proposed in [100] consists of driving all switches of a given switched-OpAmp (SO) block using only a single clock-phase, ϕ_1, and its complementary version, ϕ_{1n}. The technique takes advantage of the low values of the threshold voltages and fast transition times provided by technology. In order to explain this technique, a detailed fully-differential S/H, SO based circuit, loaded by a second sampling circuit is used, as illustrated in Figure 6.1. For simplicity purposes, only a half circuit is shown.

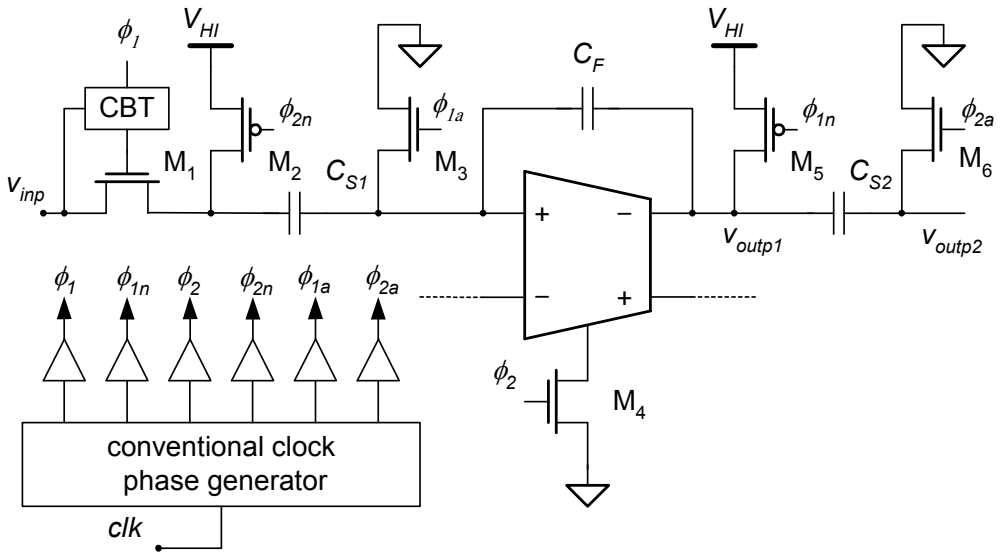


Figure 6.1: Fully-differential S/H loaded by a second sampling circuit, with switches driven by a conventional six-phase clock generator.

To overcome the problem of the sampling switches M_1 at the input of the front-end S/H (inherent to the SO principle), to enhance the linearity, and to overcome the signal-dependent charge injection due to the input sampling switches, two clock- bootstrapping circuits driven by phase ϕ_1 are employed. Using the conventional clock-phase scheme, the switches of this circuit have to be driven by six different phases, namely, ϕ_1, ϕ_{1n}, ϕ_2, ϕ_{2n}, ϕ_{1a} and ϕ_{2a}.

Assume now that PMOS and NMOS switches M_2 and M_3, driven respectively, by ϕ_{2n} and ϕ_{1a}, become driven only by ϕ_1 as depicted in Figure 6.2.

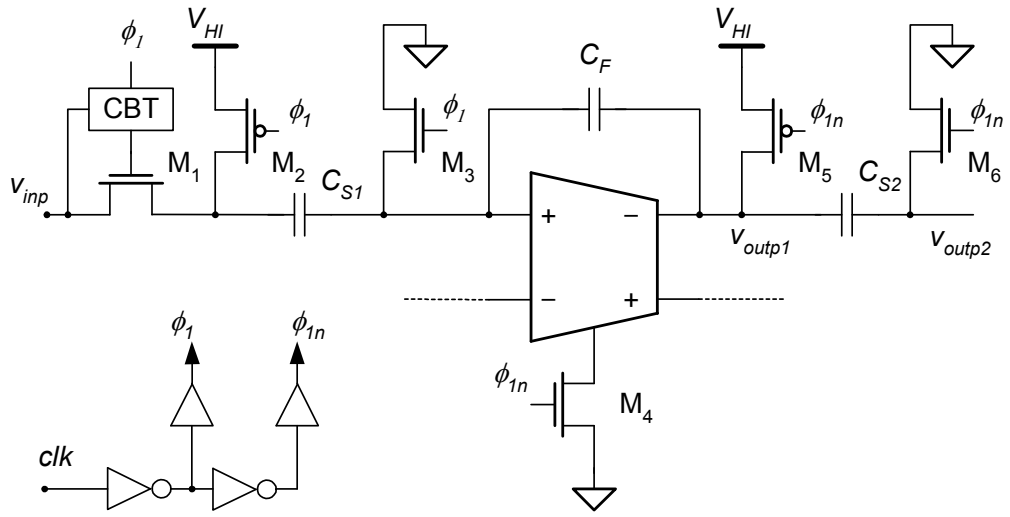


Figure 6.2: Fully-differential S/H loaded by a second sampling circuit, with switches driven by a single phase (ϕ_1) and its complement (ϕ_{1n}).

As illustrated in Figure 6.3 (a) and (b), when phase ϕ_1 goes low during a fall time, $\Delta t = t_d - t_i$, the NMOS switch conductance, g_{DSn}, decreases from its ON value, reaching zero when gate voltage is below the threshold value, V_{Tn}, at time instant t_2 (when S_3 turns-OFF).

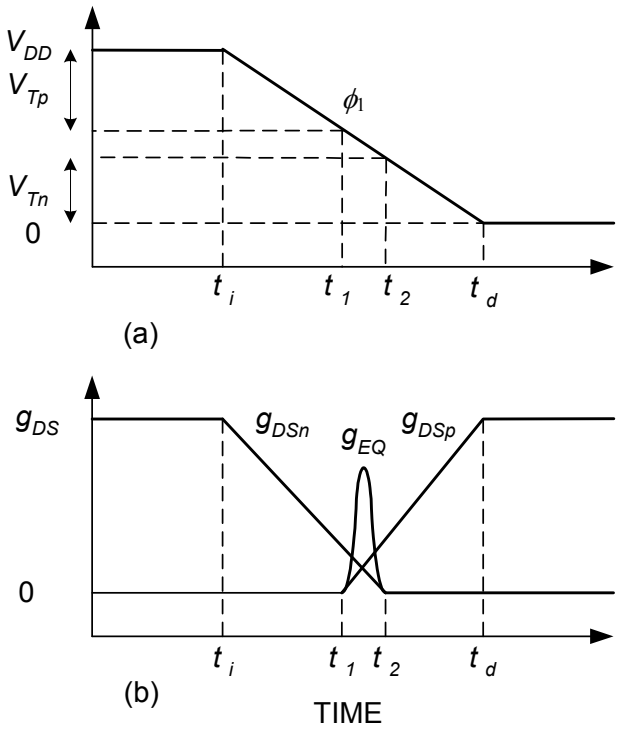


Figure 6.3: Single phase NMOS and PMOS switching; (a) phase ϕ_1 goes low; (b) switches conductances and total conductance change.

The PMOS switch conductance, g_{DSp}, increases from zero, when gate voltage is below ($V_{DD} - V_{Tp}$), *i. e.,* M_2 starts turning ON at time instant t_1, to its maximum ON value. Capacitor C_{S1} discharges if both switches simultaneously have conductances different from zero. The discharge time-constant depends on the conductance of the equivalent series resistance of M_2 and M_3. The resulting conductance, g_{EQ}, will have a peak at the gap where both devices have non-zeroed conductance.

Figure 6.4 displays the simulated conductances for relatively large NMOS and PMOS switches, with respective widths of 20 and 100 μm, when a fall time of 0.2 ns and a supply of 1.5 V are applied.

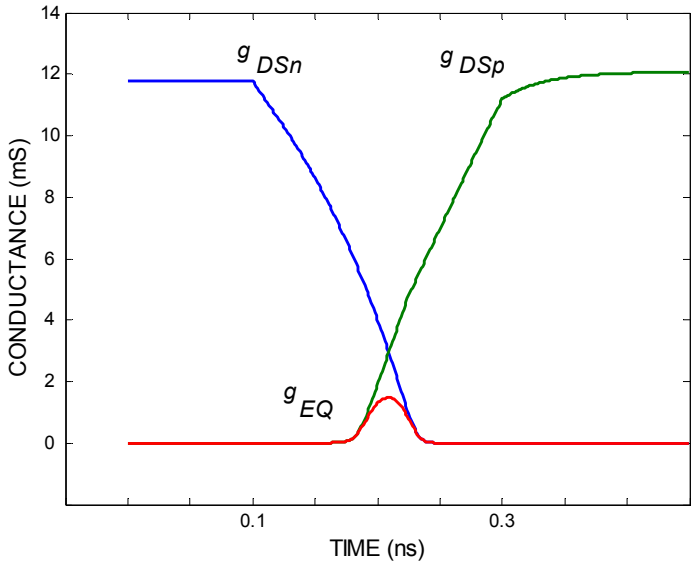


Figure 6.4: Simulated switches conductances and total conductance change.

Figure 6.5 displays the simulated equivalent or total conductance for different fall time and supply voltage. The curve a) is obtained when the previous conditions are applied, a fall time of 0.2 ns and a supply of 1.5 V. The b) representation is obtained when the fall time is reduced to 0.1 ns, and the c) result is obtained when maintaining a fall time of 0.2 ns, and increasing the supply voltage to 1.8 V.

The equivalent conductance (g_{EQ}) curve integral, Q_v, represents the charge *per* voltage or the ability of discharging the capacitor.

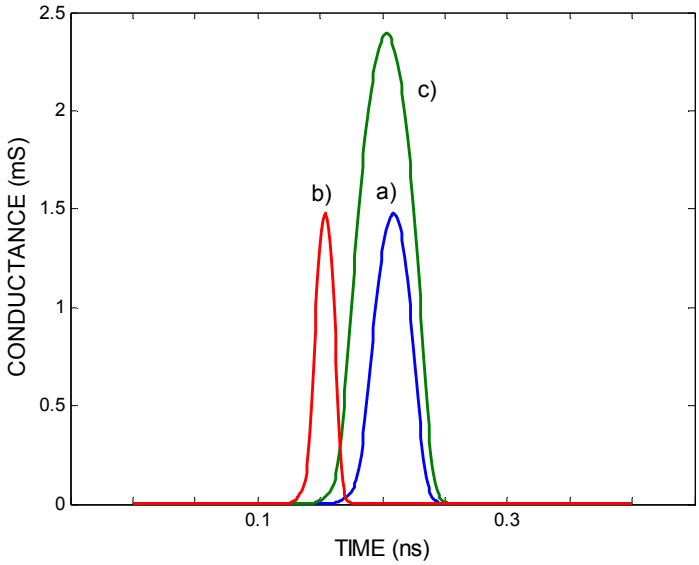


Figure 6.5: Simulated equivalent conductance for different fall times and supply voltages.

It can be demonstrated that a simple equation for Q_v, considering the integration interval of time $\Delta t = t_d - t_i$, and assuming roughly that $V_{Tn} \approx |V_{Tp}| \approx V_{TO}$ and $(g_{DSn})_{max} \approx (g_{DSp})_{max} \approx g_{DS}$, can be obtained in form (6.1).

$$Q_v \approx \frac{\left[g_{DS} \cdot \Delta t \cdot (V_{DD} - 2 \cdot V_{TO})^2\right]}{\left[6 \cdot V_{DD} \cdot (V_{DD} - V_{TO})\right]} \qquad (6.1)$$

As shown in Figure 6.6, where a representation of the evolution of Q_v is depicted, and normalized for the situation of phase voltage fall time Δt = 1ns and supply voltage V_{DD} = 1.8V, the sampled signal degradation due to having both switches conducting at the same time during the falling edge of ϕ_1 is negligible as long as those values are both small.

In a simplified analysis, the conductance of clock-bootstrapped switch M_1 can be lumped with conductance of M_3. For the second sampling circuit, the analysis is similar, considering switches M_5, M_6, capacitors C_{S2} and the falling edge of ϕ_{1n} (the complement of ϕ_1).

As demonstrated in [100] a sampled signal will be affected by a small loss of the charge stored in a capacitor C_S, approximately given by (6.2).

$$Loss\,(dB) = 20 \cdot \log_{10}\{e^{(-Qv/C_S)}\} \qquad (6.2)$$

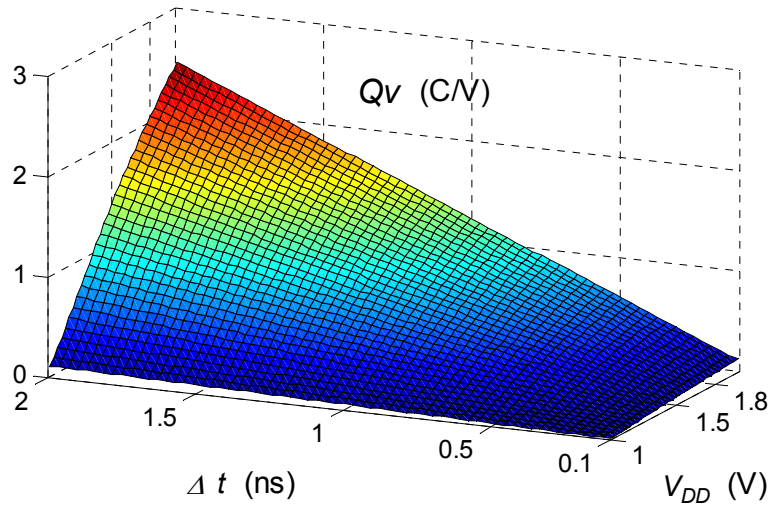


Figure 6.6: Ability of discharging the sample capacitor, Q_v (normalized), as function of V_{DD} and fall time, Δt.

With the evolution of CMOS technologies, the values of Δt and V_{DD} are progressively being reduced. Hence, non-overlapping guard times might no longer be required in SC circuits designed for modern sub-micron technologies. Notice that the example shown before is valid for any all-NMOS or any all-PMOS combinations. Moreover, there are no matching requirements concerning the switch conductances as long as their channel widths remain relatively small.

Another important simplification is also achieved using the proposed phase scheme. During the sampling operation in SO circuits, the signal-dependent charge injection added by switching-OFF (through M_4) the output-stage of the OpAmp is very small even if advanced phases, ϕ_{1a} and ϕ_{2a}, are not employed. The main reason is that the signal swing at the input of the output-stage of the OpAmp is always so small that the amount of the charge that must flow out of the channel region is practically signal-independent. Hence, as demonstrated by simulated results presented in the next Section, phases ϕ_{1a} and ϕ_{2a} can be replaced by phases ϕ_1 and ϕ_{1n}, without any degradation of THD of the circuit.

There are several advantages in using this single phase scheme by comparison with the conventional one; 1) the clock-phase generator is implemented simply by a couple of CMOS inverters, rather than by a circuit with many gates, as illustrated in Figure 6.2. As a result, the

cumulative jitter noise as well as the substrate noise introduced will be much smaller; 2) Avoiding the conventional phase generator, the area efficiency of a pipelined ADC is improved and the clock-circuitry complexity is highly reduced; 3) The dynamic performance, spurious free dynamic range (SFDR) and THD, at low-voltage operation is kept the same or even improved at lower supply voltages.

6.1.3. Architecture selection

The basic pipelined architecture is depicted in Figure 6.7 and it is optimized and tailored as reported in [101]. The system comprises a front-end S/H, followed by a cascade of two equal stages with a resolution-per-stage of 2.5-bit, followed by 4 equal stages with a resolution-per-stage of 1.5-bit and, finally, by a 2-bit flash quantizer. Each 2.5-bit (or 1.5-bit) stage comprises a 2.5-bit (or 1.5-bit) MDAC and a 2.5-bit (or 1.5-bit) quantizer.

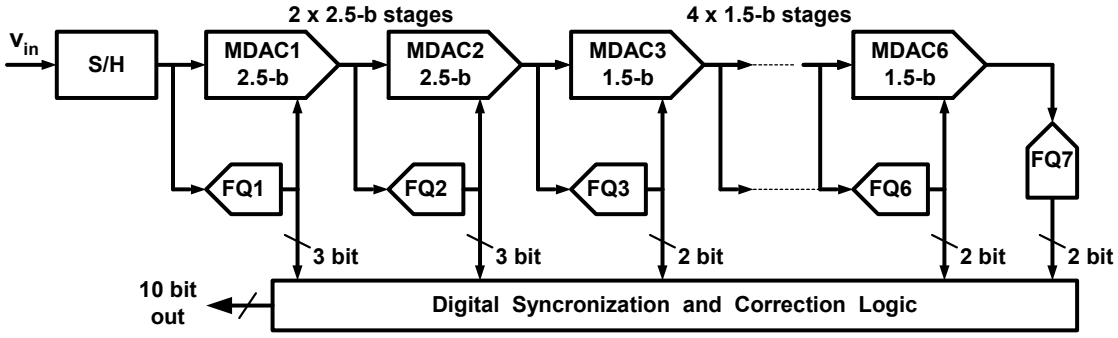


Figure 6.7: 10-bit pipelined A/D architecture.

As shown in [102], architectures using front-end stages of 2.5-bit rather than 1.5-bit per-stage are better suited for low-voltage realizations. They result in lower power dissipation and smaller differential nonlinearity (DNL) errors, since more bits in the front-end stage reduce the sensitivity to component matching errors.

An interesting solution to achieve low-voltage SC circuits, overcoming the lack of the linearity of the switches, and with high power and area efficiency, is the SO technique [82]. The idea consists of eliminating all switches in the signal path, as previously stated in this Thesis. The sampling operation in a given SC block is then obtained by switching-OFF the output-stage of the OpAmp of the previous SC block. Normally, a two-stage OpAmp is used in order to maximize the output signal-swing [103]. If the SO technique is properly

implemented, all remaining switches used in the SC circuits are connected to constant common-mode voltage levels close to $V_{LO}(\approx V_{SS})$ or close to $V_{HI}(\approx V_{DD})$, and these switches can be implemented, respectively, by NMOS and PMOS devices.

Figure 6.8 shows the combined SO/CBT (clock bootstrapped) implementation of the S/H. When the conventional sampling-phase, ϕ_{1a} (an advanced in time version of ϕ_1), is enabled, the inputs of the OpAmp are set to $V_{LO}(\approx V_{SS})$.

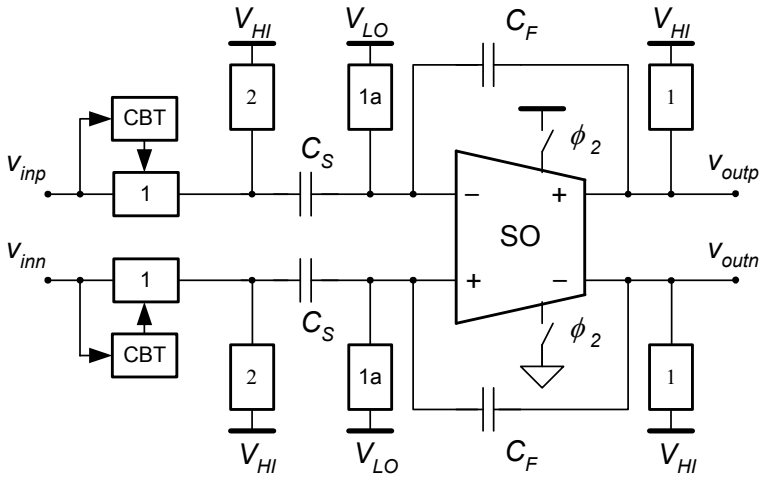


Figure 6.8: SO/CBT realization of the S/H.

At the same time, the outputs of the OpAmp are in high-impedance (with the OpAmp switched OFF) and pulled-up to $V_{HI}(\approx V_{DD})$. The input voltage is sampled into unit sampling capacitors, $C_S = C_u$, through two clock-bootstrapped switches and, the feedback capacitors, C_F (nominally equal to C_S), are charged to V_{HI}. During the second (hold) phase (ϕ_2), the bottom-plates of C_S are connected to V_{HI} and the charges stored in C_S are transferred and held into feedback capacitors C_F. Capacitors C_F are permanently connected in order to avoid additional output switches requiring CBT circuits. Nominal capacitances $C_u = 1$ pF are used in the S/H.

6.1.4. The SO 2.5-bit and 1.5-bit MDACs

Figure 6.9 shows a SO implementation of the generic M-bit MDAC. Again, when conventional sampling-phase (ϕ_{1a}) is enabled, the inputs of the OpAmp are set to V_{LO}. At the same time, the outputs of the OpAmp are in high-impedance (with the OpAmp switched OFF)

and pulled-up to V_{HI}. The input differential voltage is sampled into sampling capacitors, C_S, and the feedback capacitors, C_F, and the 6 unit capacitors, $C_{D(i)} = C_u$, are charged to V_{HI} in order to set the input common-mode voltage to V_{LO} in the next phase.

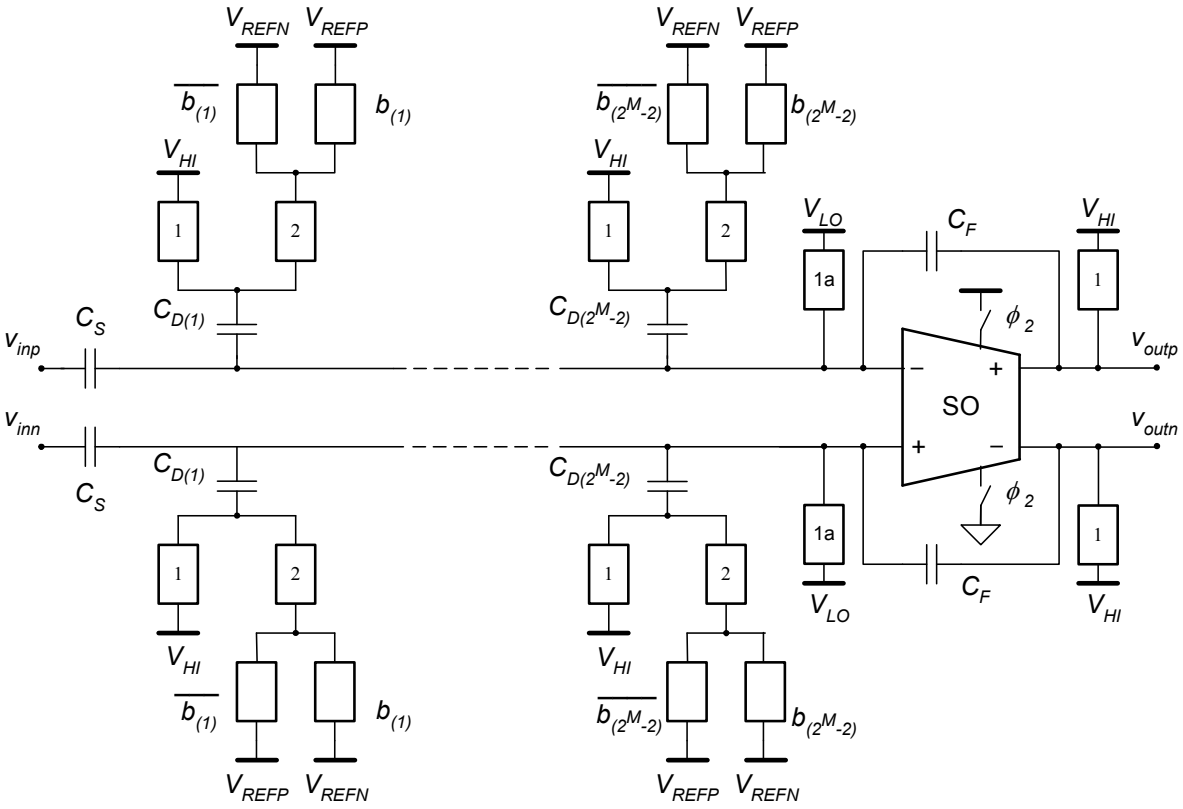


Figure 6.9: SO realization of the 2.5-bit MDACs.

During the second phase (ϕ_2), the residue obtained by subtracting the stored input voltage and the analog voltage returned from the D/A conversion (performed by capacitors $C_{D(i)}$) of the digital thermometer-code provided by the quantizer in the previous phase, is amplified and held in the permanently connected feedback capacitors, C_F. Nominal capacitances $C_u = 150$ fF are used in the capacitor-arrays of the 2.5-bit MDACs of the first and second stages, and capacitors C_S and C_F are sized according to $C_S = 2^3 C_u$ and $C_F = 2^1 C_u$.

The implementation of the 1.5-bit MDACs uses only two unit capacitors $C_{D(i)} = C_u$ rather than six. Capacitors C_S and C_F are sized according to $C_S = 2^2 \cdot C_u$ and $C_F = 2 \cdot C_u$. Nominal capacitances $C_u = 50$ fF are used in all 1.5-bit MDACs.

6.1.5. Simulated results

The S/H shown in Figure 6.1, with all switches driven by a conventional six-phase clock generator and using C_{S1} = C_{F1} = 1.0 pF and C_{S2} = 1.4 pF, is designed and simulated in a standard 0.18 μm CMOS technology with V_{Tn} = 0.50 V and V_{Tp} = − 0.52 V. The same S/H block circuit is then simulated under the same conditions, and using only phases ϕ_1 and ϕ_{1n} for driving all switches, according to the proposed new phase scheme, as depicted in Figure 6.2. Two medium size CMOS inverters ($W_p \approx 24$ μm and $W_n \approx 8$ μm) are used to generate buffered phases ϕ_1 and ϕ_{1n} from the master clock (with rise/fall times of a few hundreds of pico-seconds). Local buffers (inverters) are double-sized ($W_p \approx 48$ μm and $W_n \approx 16$ μm).

The 1024-bin FFT of the simulated results of the differential output of the second sampling block ($v_{outp2} - v_{outn2}$) is obtained, using for both circuits, V_{DD} = 1.5 V, V_{LO} = V_{SS} = 0 V, V_{HI} = V_{DD} and worst-case deviations of 10% in the channel widths of all switches. A sampling clock frequency F_S = 4 MS/s for both clock generators is adopted and a differential input signal ($v_{inp} - v_{inn}$), with a frequency f_{in} = 2.31 MHz and an amplitude A_{in} = ± 500 mV, is applied to the differential inputs of the S/H circuit. Using the proposed new phase scheme the signal loss in ($v_{outp2} - v_{outn2}$) is smaller than 0.0015 dB (less than 0.1mV, corresponding to more than 13 bits of accuracy) and the THD (dominated by the third harmonic) is slightly improved from −93.8 dB to − 98.4 dB, since the available time for settling is slightly increased and, consequently, the settling accuracy is increased. For higher power supply voltages (up to 2 V), g_{EQ} increases, but the proposed phase scheme still works with small harmonic distortion.

After analyzing these preliminary results from the S/H block, the complete 10-bit 4 MS/s pipelined ADC was designed in the same CMOS process and was electrically simulated. All capacitors used in the ADC are sized to meet both noise and DNL (linearity) specifications according to [101] in order to produce a maximum degradation in the overall SNR of about 2 dB and maximum DNL errors of ± 0.75 LSB. Therefore, the final expected signal-to-noise-plus-distortion ratio (SNDR) is about 59 dB leading to an effective number of bits (ENOB) of about 9.5 bits (in typical conditions) at Nyquist rate. Again, a sampling clock frequency F_S = 4 MS/s for both clock generators is adopted and a differential input signal ($v_{inp} - v_{inn}$), with a frequency f_{in} = 2.31 MHz and an amplitude A_{in} = ± 500 mV, is applied to the differential

inputs of the ADC. Figure 6.10 (a) and (b) show the 1024-bin FFT results of the digital output of the ADC, using the conventional scheme and the proposed new scheme, respectively.

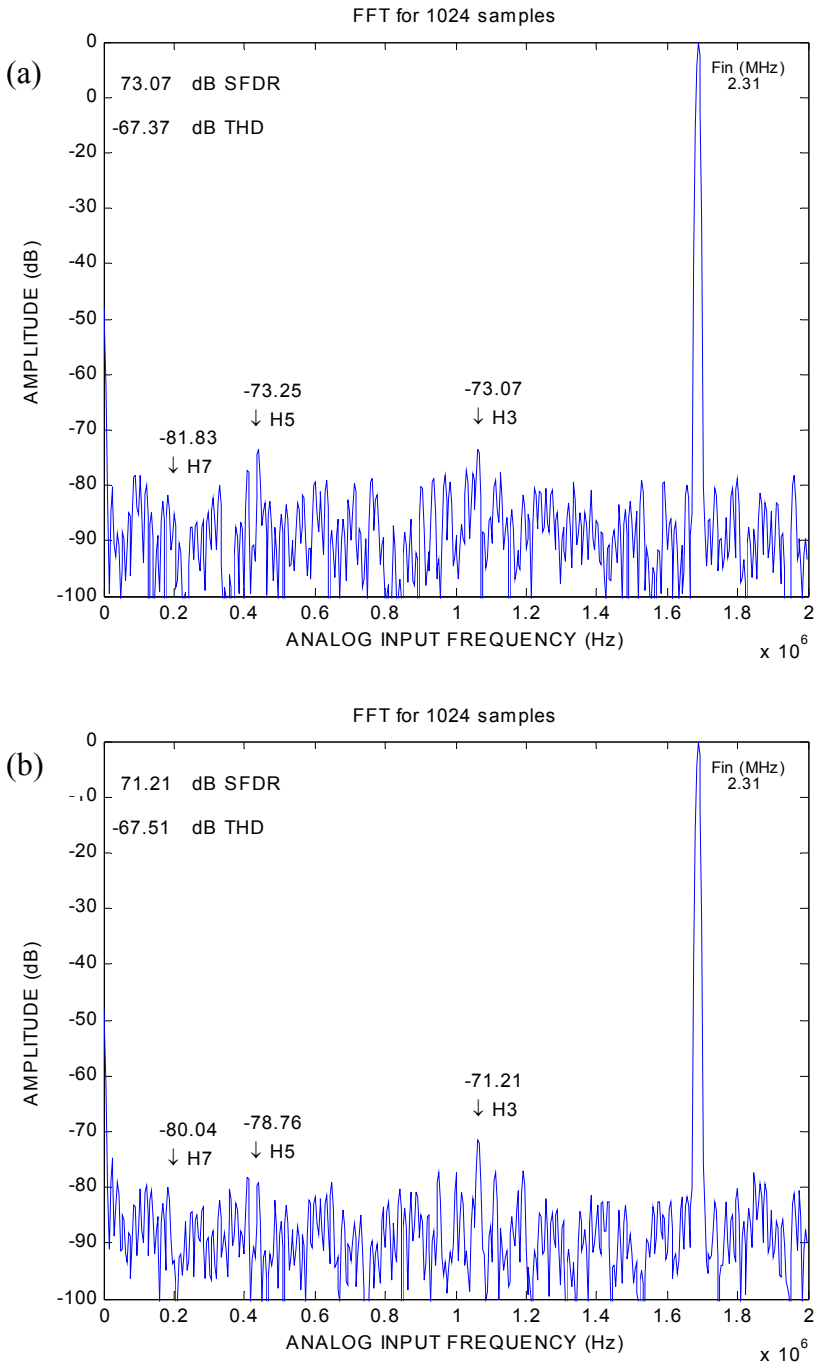


Figure 6.10: Simulated results of the digital output of the ADC with V_{DD}=1.5 V; (a) using the conventional clock generator; (b) using the proposed single-phase scheme.

Figure 6.11 illustrates the SFDR for different supply voltages ranging from 1.2 V up to 1.8 V (1.5 V ± 20%) when the ADC switches are driven by (a) the conventional clocking scheme and by (b) the single-phase scheme. It can be concluded from these simulated results that,

when the circuit operates at the minimum supply voltage (1.2V) and using the single phase scheme, the SFDR, which is dominated by the highest harmonic (usually the third), it is improved by about 6 dB. When the ADC operates at supply voltages higher than 1.4 V, the SFDR is slightly better (less than 2 dB) when a conventional clock-phase generator is used. However, the overall THD is nearly constant in both cases and within the specified supply range.

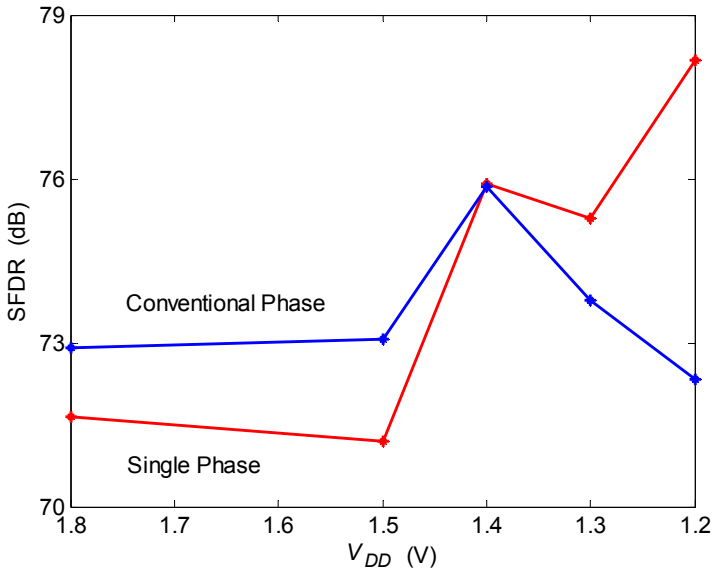


Figure 6.11: Simulated SFDR versus supply voltage (V_{DD}) when using the conventional or the single phase scheme.

Since the SNDR is dominated by the noise contribution (the ADC is optimized for a maximum SNR of about 60 dB in typical conditions) either using the conventional clocking scheme or the single phase one, the ENOBs is about the same, in both cases, as presented in Figure 6.12. Within the specified supply range the expected minimum ENOB is higher than 9.25 bits since at V_{DD} = 1.2 V the SNR is degraded to about 58 dB due to a 2 dB reduction in the input dynamic range (A_{in} is reduced from ± 500 mV to about ± 400 mV, i. e. from 2 V_{ppdiff} to about 1.6 V_{ppdiff}).

It should be noticed that, since in the single-phase scheme the clock-phase generator is implemented simply by a couple of CMOS inverters rather than a circuit with many gates (as it is used in the conventional clock-phase generator), the expected substrate noise introduced will be much smaller. As a direct consequence, it is expected a smaller measured SNR

degradation as soon as we have experimental results from silicon. Unfortunately, this claim can not be validated through simulated results, due to the lack of substrate noise modeling.

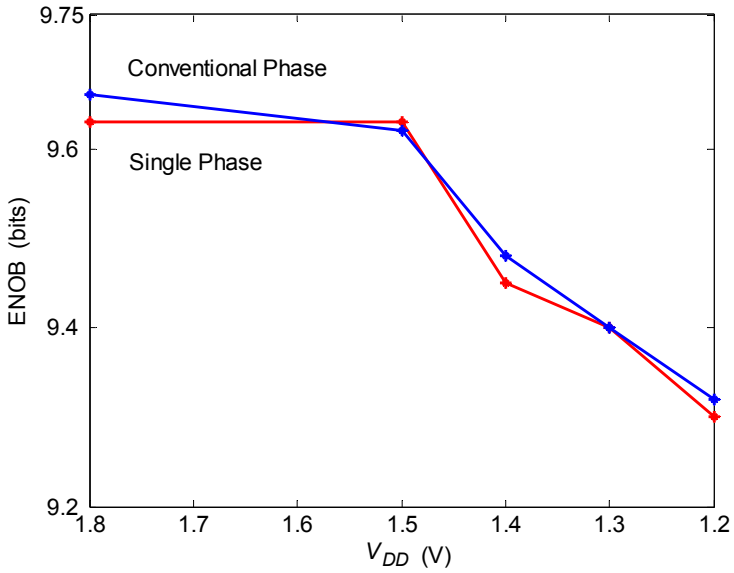


Figure 6.12: Expected ENOB values versus supply voltage (V_{DD}) when using the conventional or the single phase scheme.

6.1.6. Conclusions

It is demonstrated in this Chapter that a single-phase clock scheme technique can be successfully employed in the design of low-voltage and low-power pipelined ADCs. Simulated results using the referred technique are compared with those achieved when the conventional clock scheme is used. A complete 10-bit 4 MS/s pipelined ADC is fully designed and simulated, first with all switches driven by a conventional six-phase clock generator and, latter, using a single-phase scheme. The results achieved show that the signal integrity and overall dynamic performance are preserved (*e.g.* ENOB) and the SFDR is even improved at lower supply voltages.

6.2. Design of a two-channel 6-bit 1GS/s pipelined ADC using open-loop residue amplification and passive S/H circuits

Parallel pipelined ADCs have been used to achieve low/medium resolutions at very high sampling rates [104][105][106][107]. Also sharing some common building blocks between the two or more channels in parallel, in a time-interleaved fashion, can reduce the total power dissipation. The closed-loop multiply-by-two residue amplifiers (MBTA) usually integrated in ADCs (either pipelined, algorithmic or multi-step flash) can be replaced by open-loop amplifiers [65][66], reducing global size and power. However and so far, it becomes mandatory to employ either digital gain-calibration [65] or employ replica circuits for implementing global-gain control techniques [66].

6.2.1. Introduction

To evaluate the energy efficiency of an ADC, the Walden figure-of-merit (FoM) is commonly used. This FoM is based on the measured values of the sampling rate, (F_S=2BW), effective number of bits (ENOB), and power dissipation (P): FoM=P/(2BW2^{ENOB}), where BW is bandwidth. FoM is expressed in pico-Joule (pJ), the energy used per conversion, and it represents the cost, in terms of power dissipation, to achieve a given performance. The lower the FOM value, the better the ADC.

ADCs with 6-bit resolution and sampling rate in the range of GS/s are widely used in serial links, magnetic recording systems and ultra wide band (UWB) receivers. Flash ADCs have been dominantly used for these applications. The 4-bit flash ADC reported in [108] is, by far, the most energy efficient converter, achieving FoM=0.16 pJ. In this work, many simplifications at circuit level are carried out, since the resolution is limited to 4 bits. Low-power is basically achieved by using comparators with high offset and calibrating them in the foreground; the required calibration is performed off-chip, using external DC signals. For resolutions above 4 bits (in the range of 6 to 8 bits) successive approximation register (SAR)

[109] or pipelined architectures [105] have proven to be more energy efficient. As an example, the 6-bit, 3.5 GS/s flash ADC reported in [110] has a poor efficiency, reaching a FoM of 0.94 pJ. In [109], unlike many previously published low-power high-speed ADCs based on time-interleaved SAR, the ADC has only 2 clock-cycle latency (1.6 ns at 1.25 GS/s) and achieves 6-bit performance without any digital post-processing or off-line calibration, making it a plug-in replacement for conventional flash ADCs in many applications. However the FoM of this circuit is only 0.79 pJ/conv.-step.

The hardware cost of a pipelined ADC is approximately proportional to the number of bits. Therefore, this architecture is the most cost-effective (low power and area) to obtain higher resolutions, among all the fast Nyquist A/D architectures. Sampling rates of the order of 1 GS/s can easily be achieved in advanced CMOS technologies, for resolutions up to 8-bit, using only 2 channels in parallel. An ADC with an ENOB of 8.4 bits, operating at 1 GS/s, using 4 channels in parallel, presented in [105], achieves 1 pJ/conv.-step.

The major goal of the design reported in this Section is to demonstrate that, using the proposed techniques described throughout this Thesis, it will be possible to design a calibration-free 2-channel time-interleaved 6-bit pipelined ADC operating at over 1 GS/s using less than 0.5 pJ/conv.-step (at least two-times more efficient than cutting-edge medium-resolution 1 GS/s pipelined ADCs).

This Section presents the electrical design of a 1.2V 6-bit 1GS/s 2-channel time-interleaved pipelined ADC fully sized in a 130 nm 1P-8M complementary metal-oxide-semiconductor (CMOS) technology [5]. It uses a new 2-channel 1.5-bit multiplying digital-to-analog converter (MDAC) that performs open-loop residue amplification using a shared amplifier employing local-feedback. In each pipelined stage, the open-loop residue amplification is carried-out by using a shared amplifier between channels that maximizes the energy efficiency. This amplifier employs local-feedback in order to achieve constant closed-loop gain against process-supply-temperature (PVT) variations and thus, avoiding the need of any digital self-calibration or gain-control techniques. Timing mismatches between channels are highly attenuated, simply by using two passive front-end S/H circuits, with dedicated SLC circuits [2][1], driven by a single clock-phase scheme [7]. Again, all solutions either based on calibration or in replica-bias circuits are avoided here.

Electrical simulation results show a peak signal-to-noise-plus-distortion ratio (SNDR) of 34 dB, a spurious free dynamic range (SFDR) of 47 dB, a THD of −43 dB and 5.35 effective number of bits (ENOB), for a power dissipation of only 20 mW which corresponds to an energy efficiency better than 0.5 pJ *per* conversion-step. Moreover, all pipelined stages are made equal and no scaling is used which highly simplifies the layout effort.

6.2.2. Architecture description

Using two interleaved pipelined ADCs in parallel, the sampling rate can be doubled. In Figure 6.13, a block diagram of the architecture of the overall 2-channel ADC is shown. Basically, the fully-differential structure of each pipelined ADC comprises a passive front-end S/H, followed by a cascade of four 1.5-bit stages and by a 2-bit flash quantizer at the end of the signal path.

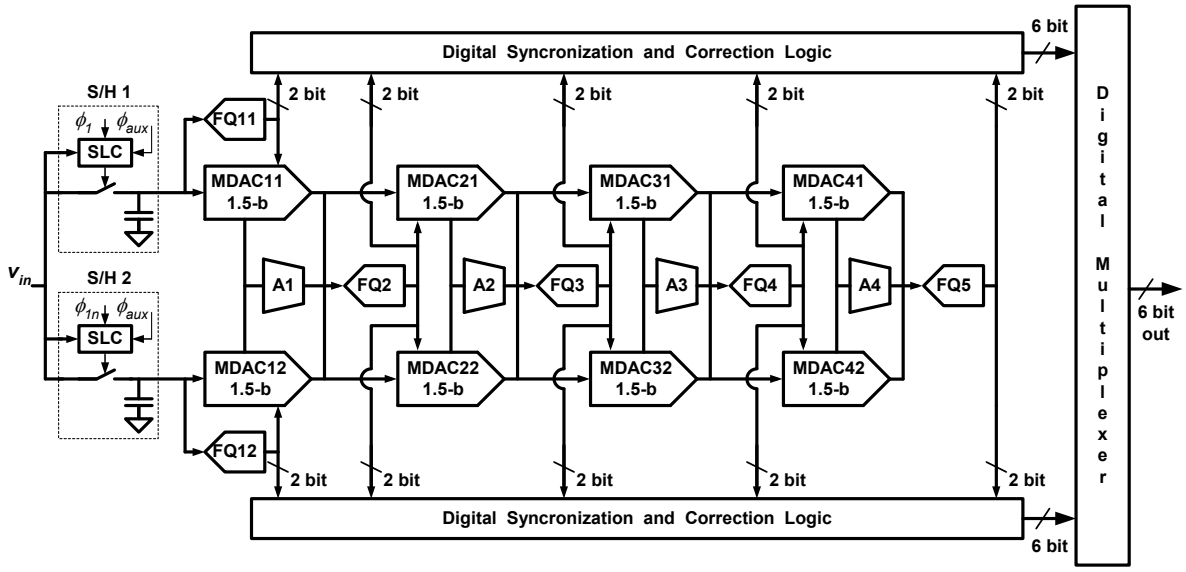


Figure 6.13: Block diagram of the architecture of the 6-bit 2-channel time-interleaved pipelined ADC.

Each 1.5-bit stage comprises a 1.5-bit MDAC and a 1.5-bit quantizer. The 10 output bits provided by the 5 quantizers are then digitally synchronized and a net resolution (N) of 6 bits is available at the output after applying synchronization and standard digital correction (summing all 5 x 2-bit words with 1-bit overlap). Each 1.5-bit MDAC block operates at 500 MS/s in order to relax the speed requirements of the amplifiers by a factor of 2. Since MDACs of the same stage and of different channel, operate in opposite phases, they are able

to share the same amplifier. Four equal sized amplifiers are, therefore, shared between channels, namely A1 to A4. The 1.5-bit quantizers FQ11 and FQ12, adjacent to the lower pipelined perform quantizations at a 500 MS/s rate. The other four 1.5-bit quantizers namely, FQ2, FQ3, FQ4 and FQ5, operate at 1 GS/s, since they are also shared between stages in order to reduce the area. Finally, at the output, a digital multiplexer operating at full speed is used in order to provide the 6-bit digital output at a 1 GS/s clock rate.

6.2.3. Timing and clock generator

The control and timing signals are indicated in Figure 6.14.

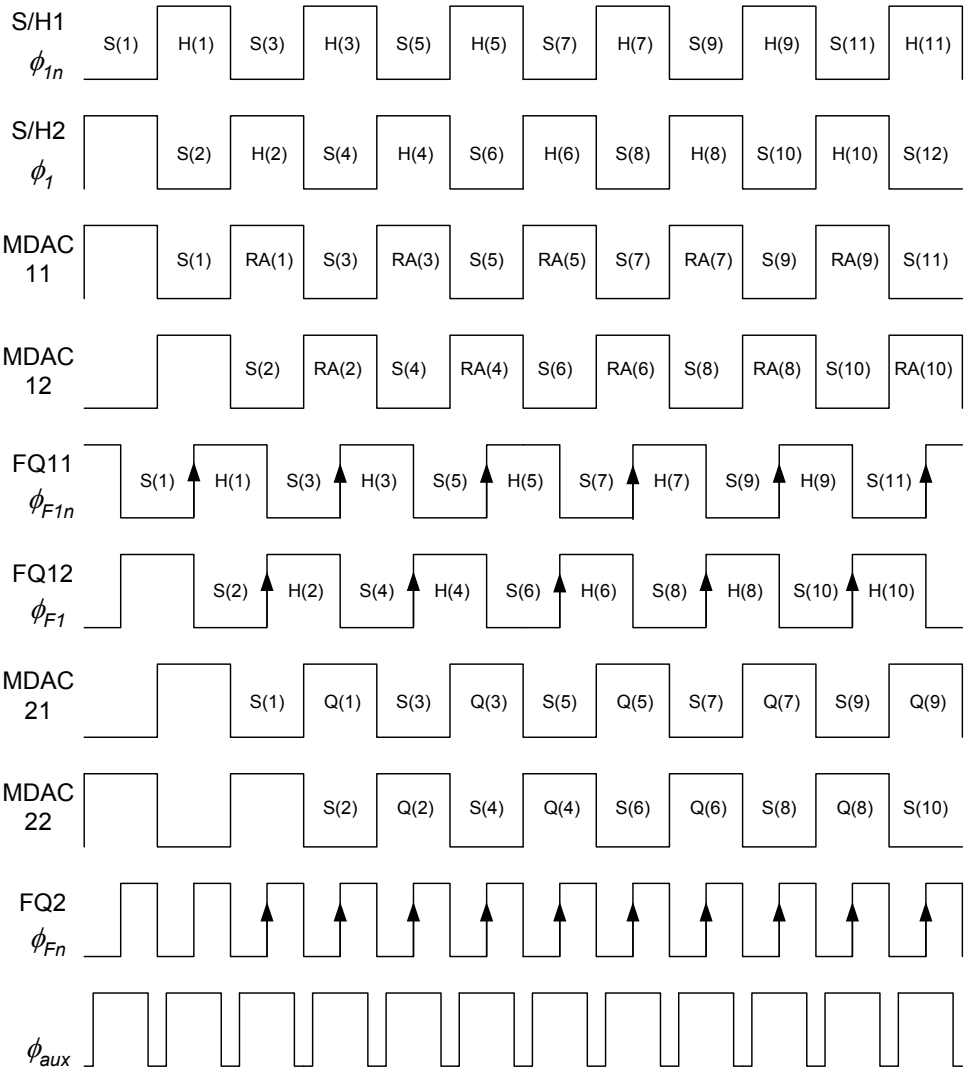


Figure 6.14: Control clock signals and corresponding ADC architecture timing.

The single-phase technique described previously is used and, hence, only one clock-phase is used, ϕ_1, and it complementary version, ϕ_{1n}. These complementary phases are used to drive the two S/H blocks and all 1.5-bit MDACs. Front-end quantizers FQ11 and FQ12 (operating at 500 MS/s) are controlled by clock signals ϕ_{F1} and ϕ_{F1n} and, the remaining quantizers (operating at 1 GS/s) are driven by phases ϕ_F and ϕ_{Fn}. In order to let the amplifiers to settle in a complete 2 ns time-slot, the quantization of all 1.5-bit flash ADCs is done in the middle of the sampling-phase of the 1.5-bit MDACs of the same stage.

Finally, an auxiliary clock signal, ϕ_{aux}, used to cancel the time-skew errors between the two channels, is also displayed.

All clock-phase signals are obtained from a 1 GHz master clock, *clk*, as depicted in Figure 6.15. No non-overlapping clock-phase generators are used. The first D Flip-Flop (D-FF) is used to obtain the divided-by-two frequency and, thus to obtain the required 500 MHz, ϕ_1 and ϕ_{1n}, complementary phases. Using ϕ_1 and ϕ_{1n} and the master clock, the 90º phase-shift phases ϕ_F and ϕ_{Fn}, used to drive quantizers FQ2 to FQ5, are generated. Thought a second D-FF, phases ϕ_{F1} and ϕ_{F1n} are produced to drive quantizers FQ12 and FQ11, respectively. Finally, the auxiliary phase ϕ_{aux} is generated, as shown in Figure 6.15, just based on a simple CMOS OR gate.

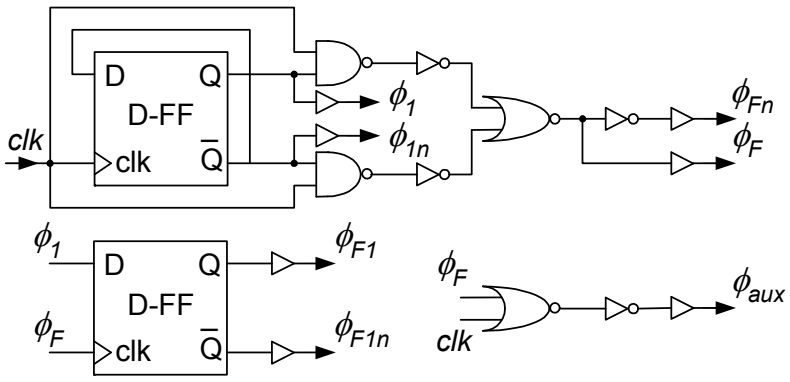


Figure 6.15: Clock signals generation.

All phases are properly buffered using digital buffers with their driving capability properly tailored according to the load.

6.2.4. The passive front-end S/H circuits

The two front-end fully-differential S/H circuits are based on a passive structure, comprising two 4 pF sampling capacitors and two asymmetric transmission gates (ATG), *per* each S/H circuit, and each ATG switch is driven by a dedicated SLC circuit. Figure 6.16 displays the block diagram of one (of two) S/H belonging to the 2-channel pipelined ADC which is sampling during ϕ_1.

The main transistors, M_1 and M_2, form the CMOS switch, and are respectively sized with aspect ratios of 20/0.12 and 80/0.12. Their controlled gate voltages are the function of the input voltage, v_{inp}, resulting in very highly linear switch without having any reliability problems [2]. The SLC circuits are controlled by ϕ_1, ϕ_{1n}, ϕ_{1s} and ϕ_{1sn} clock signals. The last two signals, generated from clock signal ϕ_1, are auxiliary signals used to avoid time-skew error and will be discussed later in this Section.

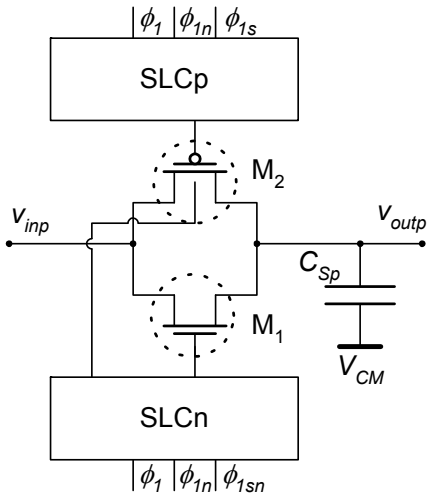


Figure 6.16: S/H block diagram.

The other S/H block is similar and it samples the input signal, v_{inn}, also during phase ϕ_1. The two S/H circuits belonging to the other parallel pipelined ADC are similar but are sampling during ϕ_{1n}. The respective SLC circuits are controlled by ϕ_{1n}, ϕ_1, ϕ_{1ns} and ϕ_{1nsn} clock signals. The last two signals, the auxiliary signals used to avoid time-skew error, are in this case generated from ϕ_{1n}.

The complete schematic of the S/H circuit is shown in Figure 6.17. The NMOS and the PMOS devices, except the main transistors, M_1 and M_2, are sized with aspect ratios (W/L) of 1/0.12 and 4/0.12 respectively.

Targeting low area and moderate linearity of the capacitance value, the parallel compensated metal-oxide-semiconductor (MOS) capacitors (MOSCAP) are used as C_1, C_2, C_3, C_4, C_5 and C_6, and are sized with aspect ratios of 3.65/3.65, 3.18/3.18, 2.5/2.5, 2.5/2.5, 5.15/5.15, and 8.5/8.5 respectively.

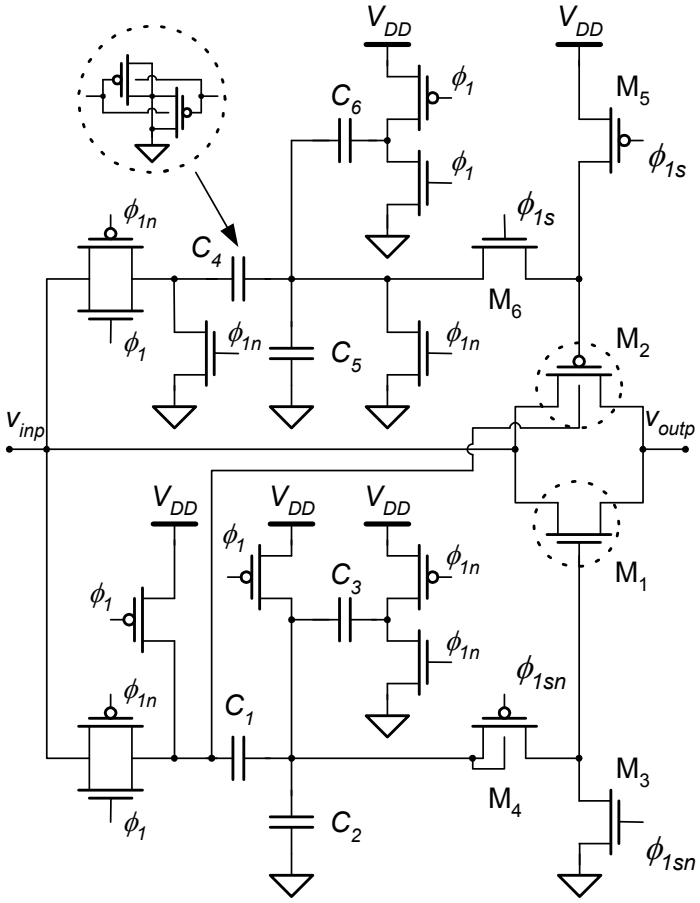


Figure 6.17: Schematic of the SLC circuit, single-phase controlled, used to linearize the CMOS (ATG type) input switches (M_1 and M_2).

Notice that, although the approach of using a passive S/H structure has the disadvantage of requiring large sampling capacitance values, the advantage relies on the fact that this passive structure provides, inherently, a low-pass filtering function when combined with the first stage.

In fact, neglecting parasitic effects, the voltage sampled into the sampling capacitors of the 1.5-bit MDAC (connected to the S/H), $v_{in}(z)$, can be expressed by (6.3), being $v_{out}(z)$ the output voltage delivered from the S/H, $C_{S(S/H)}$ and $C_{S(MDAC)}$ the S/H and MDAC sampling capacitors, respectively.

$$v_{in}(z) = \frac{v_{out}(z)z^{-1/2}\dfrac{C_{S(S/H)}}{C_{S(S/H)}+C_{S(MDAC)}}}{1-z^{-1}\dfrac{C_{S(S/H)}}{C_{S(S/H)}+C_{S(MDAC)}}} \qquad (6.3)$$

Therefore, there is a pole defined by $C_{S(S/H)}/(C_{S(S/H)}+C_{S(MDAC)})$. For low frequency signal ($z\approx 1$) we find that $v_{in}(z)/v_{out}(z)\approx 1$ (no attenuation) and for signals close to the Nyquist frequency ($z\approx -1$) the attenuation is $C_{S(S/H)}/(C_{S(S/H)}+2C_{S(MDAC)})$, which can be made smaller than 1 dB if $C_{S(S/H)}\approx 4$ pF and $C_{S(MDAC)}\approx 0.30$ pF.

It is known that the clock signals, in this case ϕ_1 and ϕ_{1n}, may not have exactly the same width, originating a sampling time error. Using the same auxiliary clock signal, ϕ_{aux}, and two NAND gates, the original clock signals, ϕ_1 and ϕ_{1n}, can be converted into synchronized signals, ϕ_{1s} and ϕ_{1sn}, according to the circuit shown in Figure 6.18. A second synchronized pair is also obtained (complementary versions, ϕ_{1ns} and ϕ_{1nsn}) by the simple circuit shown in Figure 6.18.

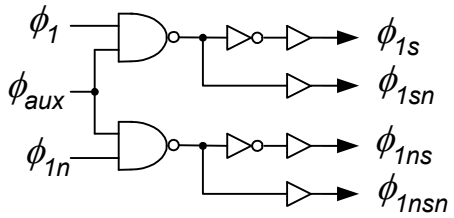


Figure 6.18: Generation of syncronization signals.

In Figure 6.19, a representation of the original clock signals is shown, ϕ_1 and ϕ_{1n}, with an intentional mismatch in their ON periods of time. Even so, the resulting synchronized signals have the same ON time.

These synchronized signals are then used to locally and accurately control the gate voltages of the main CMOS sampling switch, M_1 and M_2, acting through the SLC auxiliary transistors,

M_3, M_4, M_5 and M_6, as displayed in Figure 6.17. The switches from the first pipelined ADC S/H blocks, instead of sampling during phase ϕ_1, in fact are sampling during a smaller period of time, the ϕ_{1s} ON time. Likewise, the CMOS input sampling switches of the S/H blocks from the second pipelined bank, are sampling during ϕ_{1ns}, which has precisely the same ON time.

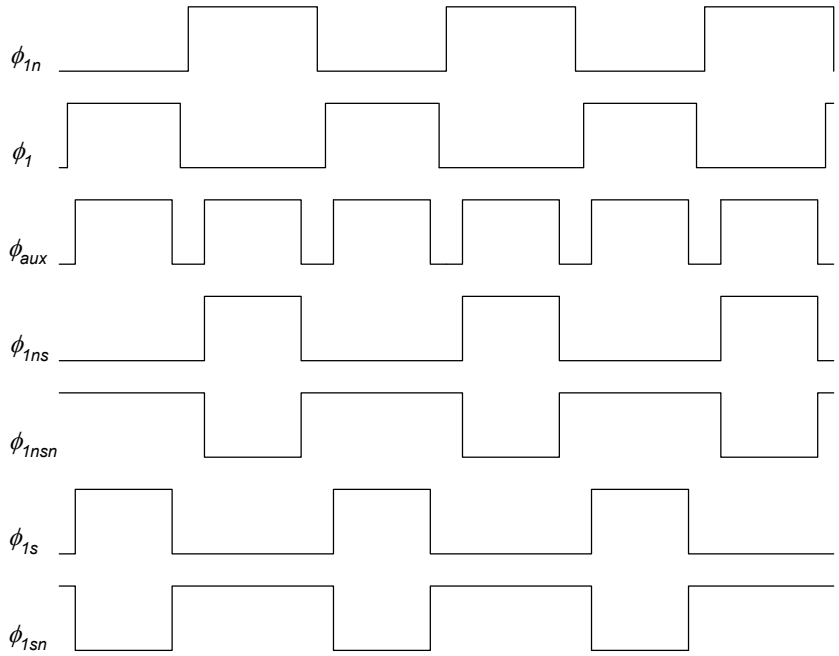


Figure 6.19: Resulting syncronization signals.

The time-skew error [111][112][113] produces, in the output data spectrum of two interleaved structures operating with input signal frequency f_{in} and with sampling frequency F_S, a folded back frequency at $f_{in}+F_S/2$.

Figure 6.20 (a) shows the simulated FFT spectrum of the output of the 6-bit ADC, without mismatch error cancellation, when a 415 MHz full-scale input signal is applied together with an intentionally set time-mismatch of 150 ps. The tone appears as a mirrored image of the main frequency, centered at $F_S/4$.

When this time-skew cancellation technique is applied, there is an efficient reduction of the time-skew effect, as shown in Figure 6.20 (b), where the same time mismatch of 150 ps, and the same input signal frequency are used.

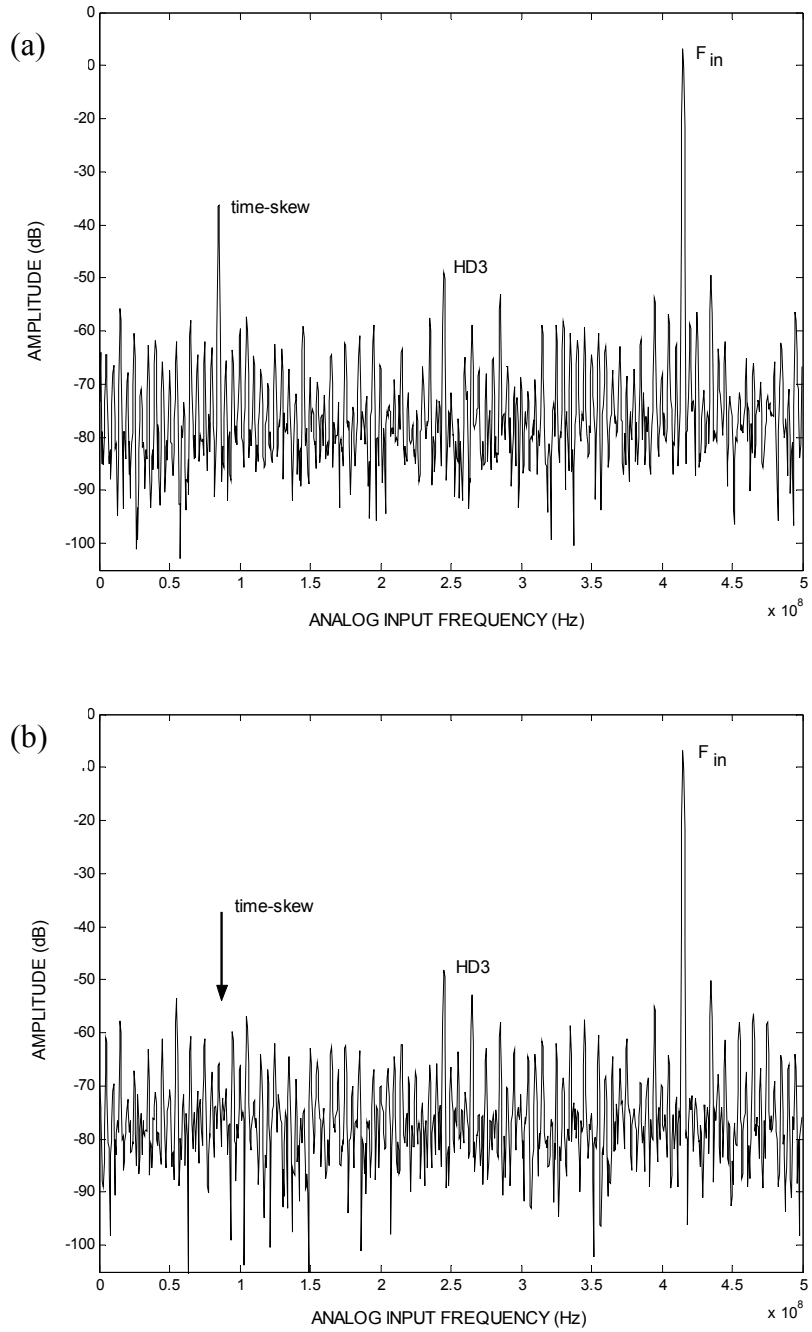


Figure 6.20: FFT spectrum of the output data of the ADC; (a) without mismatch time-skew cancelation; (b) with mismatch time-skew cancelation.

6.2.5. The 1.5-bit MDAC

Instead of using a closed-loop amplifier with high gain, as it is usually done in the conventional schemes, a switched-capacitor (SC) open-loop amplifier is used in the MDAC

stages [65][66]. As depicted in Figure 6.21, the input voltage, v_{inp}, is sampled into C_{Sp} (nominally set to 0.3 pF due to kT/C noise constraints) during phase ϕ_{1n}.

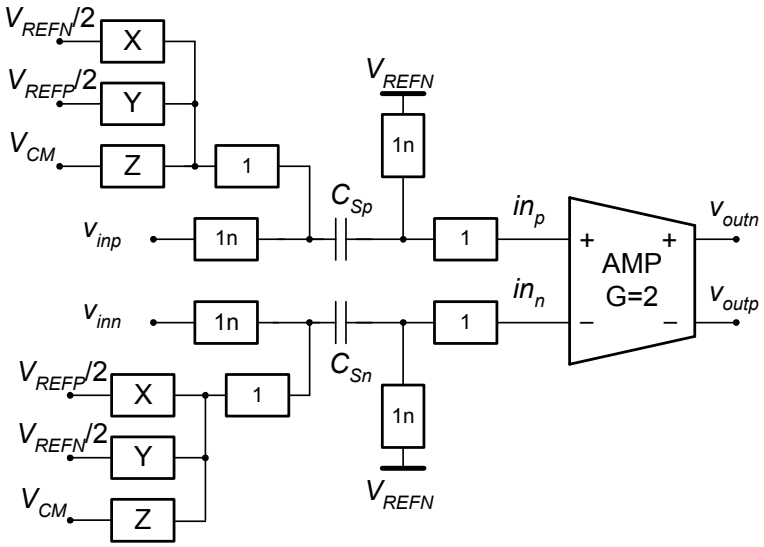


Figure 6.21: Fully-differential implementation of the 1.5-bit MDAC based on open-loop amplification.

During ϕ_1, the sampled signal is amplified by a gain of 2, and the output amplified residue is produced according to function (6.4),

$$v_{od} = v_{outp} - v_{outn} = 2\left(v_{id} + X\frac{V_{REFD}}{2} - Y\frac{V_{REFD}}{2} + Z.0 \right) \qquad (6.4)$$

where $v_{id} = v_{inp} - v_{inn}$, $V_{REFD} = V_{REFP} - V_{REFN}$, and the digital signals X, Y and Z are provided by the local 1.5-bit quantizer and only one is active at a time. The residue amplification gain, G, needs to be made accurately equal to 2 (with an error smaller than ±1.56 % for 6-bit accuracy). The reference levels used, $V_{REFP}/2$ and $V_{REFN}/2$, are, respectively, 0.675 V and 0.425 V, corresponding to V_{REFP}= 0.8 V and V_{REFN}= 0.3 V, and to an output common mode level, V_{CM}, of 0.55 V (set to this value to allow operation down to 1.08 V).

Figure 6.22 illustrates the detailed MDAC circuit. Each input switch comprises a ATG switch with bulk-switching and with dummy switch. In Table 6.1 the essential transistor dimensions are summarized.

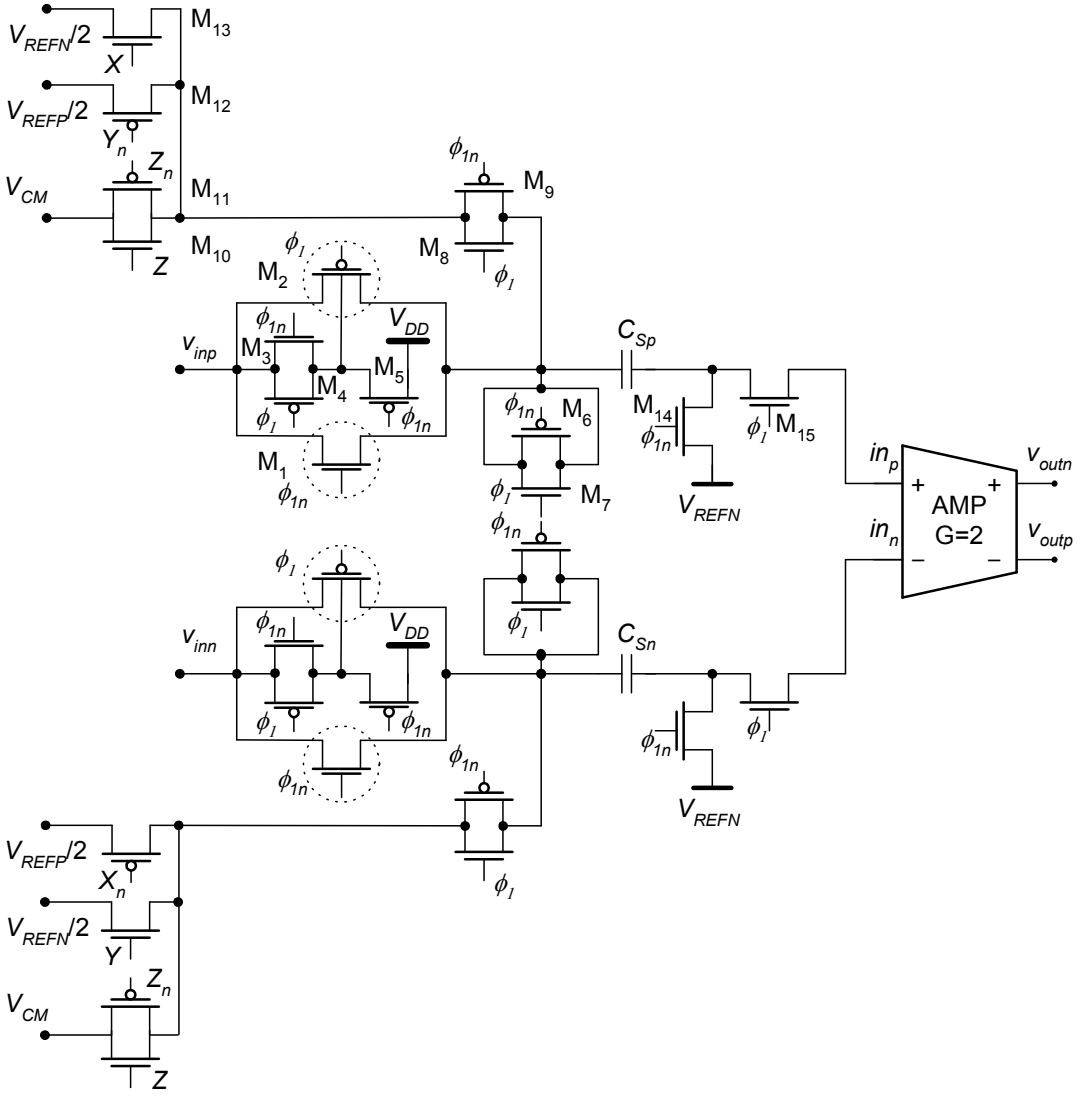


Figure 6.22: Detailed implementation of the 1.5-bit MDAC with open-loop structure.

Table 6.1: 1.5-bit MDAC transistor dimensions.

Transistor	Width (μm)	Length (μm)
M_1	5.5	0.12
M_2	20	0.12
M_3	1	0.12
M_4, M_5, M_{14}, M_{15}	4	0.12
M_6	10	0.12
M_7	2.75	0.12
M_8, M_{10}, M_{13}	2	0.12
M_9, M_{11}, M_{12}	8	0.12

The proposed amplifier structure based on local feedback is shown in Figure 6.23. It relies on a two-stage amplifier (M_2 and M_5 devices) with no inverting feedback [69][70]. Transistor M_2 acts as a source follower, copying the input signal v_{inp} to the resistor node. In the second stage, the transistor M_5 delivers the output voltage, v_{outp}, and current. The input transistor is PMOS type with bulk shorted to its source to reduce body effect, and devices M_1, M_3 and M_4 operate as current sources. The bias circuit, not shown here, provides the required bias voltages V_{Bp} and V_{Bn}.

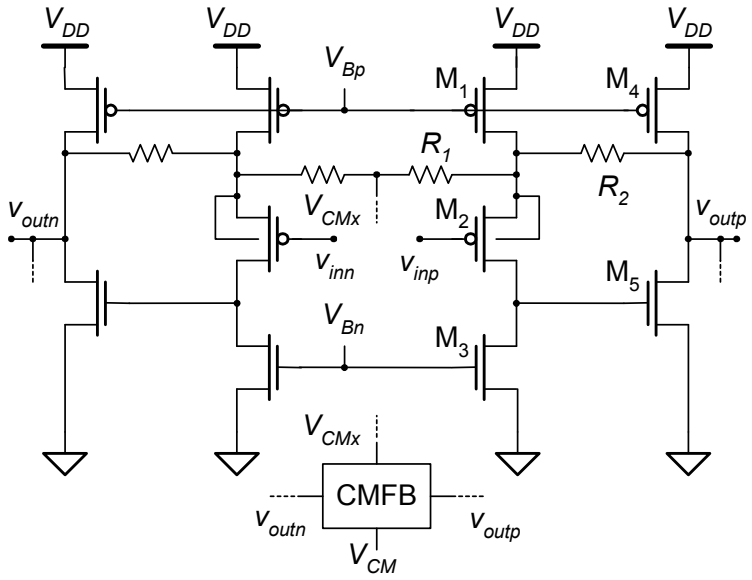


Figure 6.23: Fully-differential closed-loop amplifier.

The gain is approximately equal to $1+R_2/R_1$. However the attenuation due to parasitic capacitance at the input (gate of M_2) reduces it. The sampling capacitor, C_{Sp}, together with the input parasitic capacitance defines a trade-off between linearity, speed and power dissipation. The overall voltage gain can be adjusted varying the value of R_1. The values of 315 Ω and 500 Ω, respectively for R_1 and R_2, are adopted. Input and output stages are biased with 100 μA and 500 μA, respectively. M_2 and M_5 are sized with aspect ratios of 10/0.12 and 45/0.12, respectively.

To avoid accumulation in the common-mode errors by cascading several pipelined stages, a common-mode feedback circuit (CMFB), is employed. It senses the two output voltages, compares their level with V_{CM}, and adjusts the output common-mode voltage V_{CMx}.

6.2.6. The flash quantizer

Each 1.5-bit quantizer consists of two comparators followed by a thermometer-to-binary digital encoder and by an X, Y, Z encoder. Each comparator comprises an input switched-capacitor divider network to define the threshold level, followed by an ordinary dynamic preamplifier-and-positive-feedback latch. This comparator is optimized using exhaustive Monte-Carlo simulations in order to achieve low offset, reduced kickback noise, high mean-time to failure, and low-power dissipation at the desired speed of operation.

As displayed in Figure 6.24, the two flash quantizers at the front, FQ11 and FQ12 in Figure 6.13, are controlled by clock signals ϕ_{F1} and ϕ_{F1n}. The remaining 1.5-bit flash quantizers, FQ2, FQ3 and FQ4, are controlled by ϕ_F and ϕ_{Fn}, operating at 1 GHz.

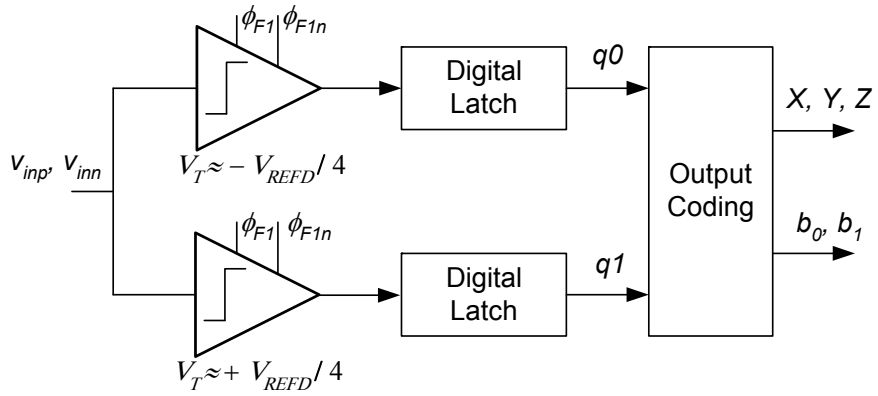


Figure 6.24: Block diagram of the first 1.5-bit flash quantizer.

Figure 6.25 shows the complete schematic of the first comparator [114], and in Table 6.2 the most relevant transistor dimensions are summarized. Targeting low area, the capacitors C_1 and C_2 are implemented with two MOSCAP each. To obtain the desired threshold value, $V_{REFD}/4$, the area used for C_1 implementation is four times higher than the area used for C_2. The MOSCAPs are then sized with aspect ratios of 2/2 and 1/1.

The embedded amplification proposed in [114] is not used, targeting lower power dissipation. The clock signal ϕ_{lat}, used to control M_{15}, and the digital latch, is a delayed version of ϕ_{F1n}, obtained through two inverters. M_6 is controlled with ϕ_{latn}, the ϕ_{lat} complementary signal.

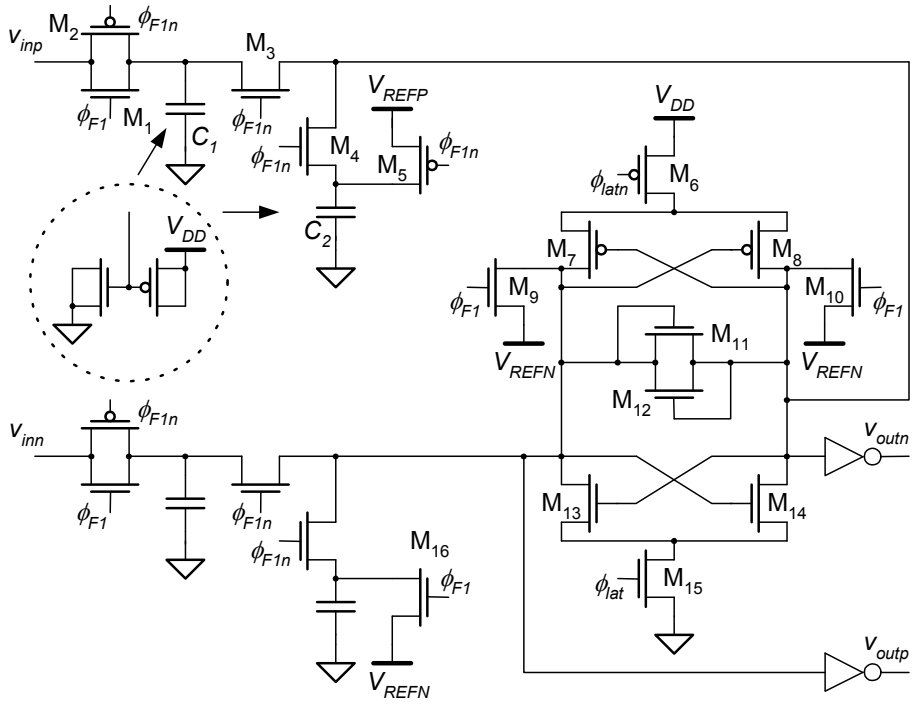


Figure 6.25: Comparator of the first flash quantizer.

Table 6.2: Comparator's transistor dimensions.

Transistor	Width (μm)	Length (μm)
M_1, M_4, M_5	2	0.12
M_2	8	0.12
M_3	10	0.12
M_{16}	0.5	0.12
M_6	20	0.12
M_{15}	5	0.12
M_{11}, M_{12}	0.25	0.12
M_7, M_8	4	0.12
M_9, M_{10}, M_{13}, M_{14}	1	0.12

Figure 6.26 represents the latch circuit used, delivering the quantizer signals *q0* and $q0_n$.

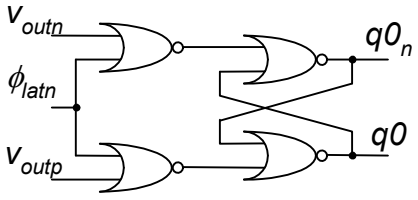


Figure 6.26: Digital latch.

The second comparator and latch displayed in Figure 6.24, are similar, but with exchanged inputs, v_{inp} and v_{inn}, and outputs, $q1$ and $q1_n$. Figure 6.27 shows the circuit used to generate the MDAC inputs, X, Y and Z, and the output codes, b_0 and b_1.

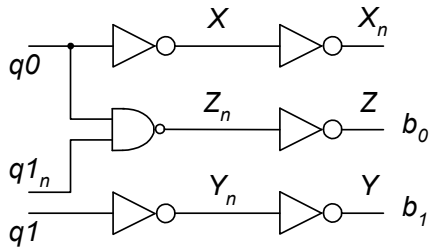


Figure 6.27: Circuit used for digital coding generation.

In Figure 6.28, the ideal residue amplification characteristic is shown, with $v_{id} = v_{inp} - v_{inn}$ and $v_{od} = v_{outp} - v_{outn}$.

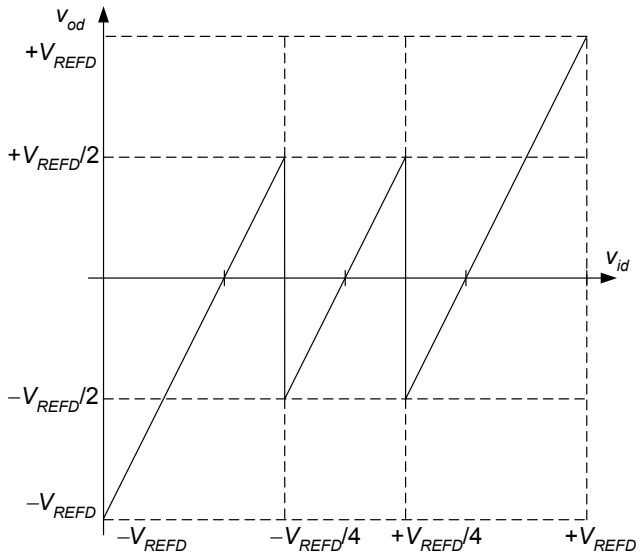


Figure 6.28: Residue amplification (ideal characteristic).

From equation 6.4, we find that

If $-V_{REFD} < v_{id} < -V_{REFD}/4$, then $v_{od} = 2\ v_{id} + V_{REFD}$,
If $-V_{REFD}/4 < v_{id} < V_{REFD}/4$, then $v_{od} = 2\ v_{id}$,
If $V_{REFD}/4 < v_{id} < V_{REFD}$, then $v_{od} = 2\ v_{id} - V_{REFD}$.

Table 6.3 summarizes the relation between input voltage and the different control and code signals.

Table 6.3: Comparator outputs and output signals as function of the input voltage in the 1.5-bit flash quantizers.

Differential input voltage v_{id}	Comparator outputs *q1*, *q0*	MDAC inputs *X*, *Y*, *Z*	Output codes b_1, b_0
$-V_{REFD} < v_{id} < -V_{REFD}/4$	00	010	00
$-V_{REFD}/4 < v_{id} < V_{REFD}/4$	01	001	01
$V_{REFD}/4 < v_{id} < V_{REFD}$	11	100	10
error	10	001	01

The block diagram of the 2-bit flash quantizer, FQ5 in Figure 6.13, is displayed in Figure 6.29. It is controlled by ϕ_F and ϕ_{Fn} clock signals, operating at 1 GHz. The 2-bit flash quantizer consists of 3 comparators and latches, followed by a thermometer-to-binary digital encoder. Each comparator comprises an input switched-capacitor divider network to define the threshold levels, $-V_{REFD}/2$, $V_{REFD}/2$ and zero.

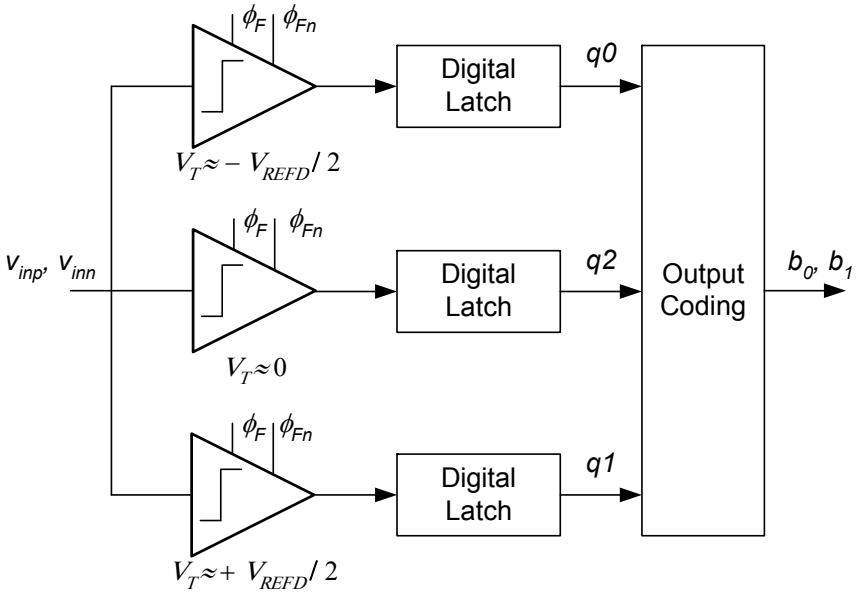


Figure 6.29: Block diagram of the 2-bit flash quantizer.

The first and the last comparators are similar to the one presented in Figure 6.25, and, as the threshold voltage is different, the relation between the capacitance values of C_1 and C_2 are different. In this case the MOSCAP devices used for C_1 implementation are sized with aspect ratios 1.4/1.4, maintaining the ratio 1/1 for the devices used for C_2. The second comparator (in the middle) uses devices sized with ratio 1/1 as C_1. Furthermore, M_4, M_5 and C_2 are removed.

Figure 6.30 shows the circuit used for generation of the MDAC control inputs and the output codes, based on the comparator/latch outputs, and Table 6.4 shows the generated values.

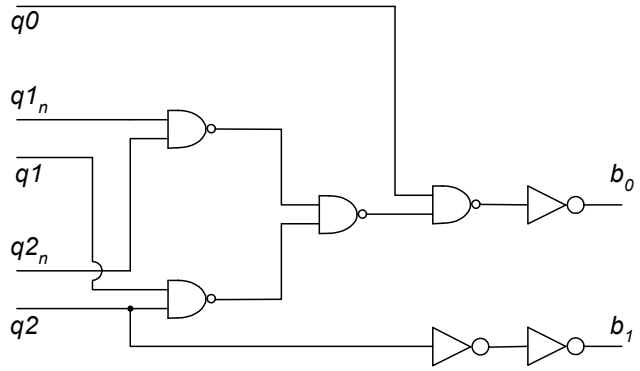


Figure 6.30: Output codes generation.

Table 6.4: Comparator outputs and output codes as function of the input voltage in the 2-bit flash quantizer.

Differential input voltage v_{id}	Comparator outputs *q1*, *q2*, *q0*	Output codes b_1, b_0
$-V_{REFD}<v_{id}<-V_{REFD}/2$	000	00
$-V_{REFD}/2<v_{id}<0$	001	01
$0<v_{id}<V_{REFD}/2$	011	10
$V_{REFD}/2<v_{id}<V_{REFD}$	111	11

6.2.7. Simulation results

The 1.2 V, 6-bit, 1 GS/s 2-channel pipelined ADC is fully designed and simulated at transistor level in a 130nm 1P-8M CMOS technology. In order to simplify the layout effort, all pipelined stages are equally sized, *i.e.* no scaling is applied to the 1.5-bit MDACs. A scaling-down approach would optimize further the overall power of the pipelined converter. In Figure 6.31 is displayed the FFT (1024 bins) of the ADC output, clocked at 1 GHz, when a full-scale input of 315 MHz is applied.

A peak signal-to-noise ratio (SNR) of 34.6 dB is obtained through analytical calculations when 4 pF and 0.3 pF unit capacitors are used respectively in the S/Hs and 1.5-bit MDACs. An RMS jitter in the clock of about 1ps was assumed in these calculations. Simulations show a THD of −43 dB, a SFDR of 47 dB, and a peak SNDR larger than 34 dB corresponding to an

ENOB better than 5.35 bits. The gain error/time-skew spur is 50 dB below the signal. Due to the single-phase scheme used, the highest harmonics are HD5 and HD11 rather than HD3.

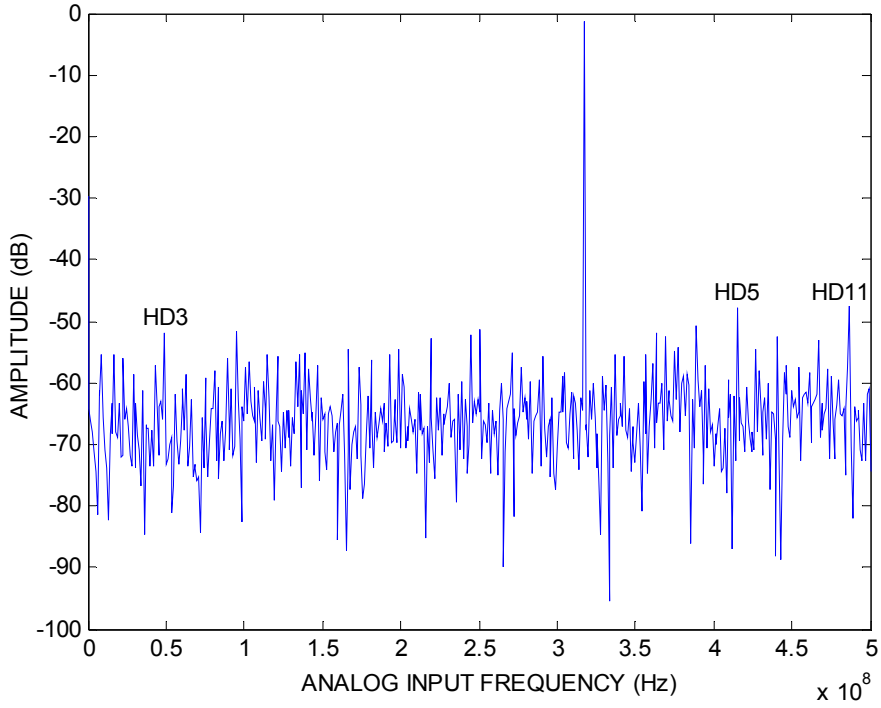


Figure 6.31: Simulated FFT spectrum with 1024 bits for F_S= 1 GHz and f_{in}= 315 MHz (coherent sampling).

The circuit dissipates less than 20 mW (11 mW analog and 9 mW digital) with 1.2 V and at 1 GS/s, corresponding to an energy efficiency better than 0.5 pJ. When comparing the energy efficiency with the state-of-the-art of low resolution pipelined ADCs employing open-loop residue amplification [66] (ENOB = 5.3 bits, F_S = 800 MS/s, Power = 105 mW), this work exhibits an improvement (based on simulation results) of a factor higher than 6.6. Furthermore, no calibration scheme is required. Notice also that about 45% of the dissipated power is from the digital circuitry (DC logic, local clock buffers, etc.). This can be highly reduced if the design is ported into a deeper submicron technology (*e.g.* 65 nm).

6.2.8. Conclusions

A low-power 1.2 V 6-bit 1-GS/s time-interleaved pipelined ADC designed in 130 nm CMOS is described. It is based on a new 2-channel 1.5-bit MDAC that performs open-loop residue

amplification using a shared amplifier employing local-feedback. Time mismatches between channels are highly attenuated, simply by using two passive front-end S/H circuits, with dedicated SLC circuits, driven by a single clock-phase. Simulated results of the ADC achieve 5.35 bits ENOB, with less than 20 mW and without requiring any gain control/calibration scheme.

6.3. Conclusions

In this Chapter, the design of two ADC and the obtained simulated results are used to demonstrate the applicability and the characteristics of the solutions proposed in the previous Chapters. The first ADC design is centered in the phase complexity and in the single-phase technique. The simulated results of the design, simplified by using a single-phase control signal, demonstrate the efficiency of the single-phase technique applied to medium resolution pipelined ADCs. The second ADC design makes use, simultaneously, of several techniques, to obtain high power efficiency while achieving moderate resolution. It uses the proposed SLCs, the MDAC open-loop structures, the local feedback amplifiers and the MOSCAPs.

7. Integrated prototype of a 10-bit 32 MS/s pipelined ADC and corresponding experimental evaluation

A practical realization of a pipelined analog-to-digital converter (ADC) in integrated circuit [4], using the proposed switch-linearization technique, is described. The switches used in the front-end sample-and-hold (S/H) are driven by switch-linearization circuits (SLC), described in the previous Chapters, ensuring they have enough linearity in the signal path over rail-to-rail signal swings and, at the same time, guaranteeing the absence of stress.

The description of the design reported in this Chapter is focused on the front-end S/H circuit where the proposed new SLC circuits are used. Although all blocks have been implemented, is out of the scope of this Thesis to explain in detail the implementation of the other main circuits of the pipelined ADC, since similar blocks have already been discussed in Section 6.1.

The measurements from the fabricated low-power 1.2 V 10-bit 32 MS/s pipelined ADC, designed in 130 nm complementary metal-oxide-semiconductor (CMOS), exhibit 10-bit compatible differential nonlinearity (DNL) and 8.8 effective bits at Nyquist rate and for low-frequency input signals. In sub-sampling mode (f_{in} = 63 MHz) the effective number of bits (ENOB) drops less than 0.5-bit. This proves that, when used, the proposed SLC circuits can provide to the front-end S/H circuits where they are embedded, very high effective resolution bandwidths. The estimated linearity of the sampling switches, obtained through FFT simulations of the S/H, is consistent with the measured results of the complete ADC.

Section 7.1 refers to a brief introduction and Section 7.2 describes the employed ADC architecture. Section 7.3 is focused in the electrical design of the front-end S/H circuit where the SLC circuits are used and Section 7.4 presents the simulation results. The description of the integrated prototype and measured results are respectively given in sections 7.5 and 7.6. Finally, Section 7.7 draws the main conclusions of this Chapter.

7.1. Introduction

As stated before throughtout this dissertation, deep submicron CMOS technologies are forcing the operation supply voltages of the circuits to become increasingly lower. Additional care and requirements are needed to guarantee the linearity of the sampling switches over the input signal swing, required by high-resolution analogue-to-digital conversion with high sampling rates. Also, the over-stress and leakage of the CMOS devices has to be taken into account, in order to obtain long-term reliability, reducing more and more the maximum amplitudes of the control gate voltages.

These challenges are all addressed by using, for example, the proposed SLC circuit. The SLC senses the input voltage level and provides the adequate voltage to drive the transistor gate of the sampling switch. The "softly" boosted gate voltages of the NMOS and PMOS transistors are controlled, resulting in a linear behavior of the equivalent conductance of the two transistors over the input voltage variations. Also, the gate voltages are limited to the level recommended by technology, preventing undesirable life span shortage.

In this Chapter the effectiveness of the SLC circuit is demonstrated through the complete implementation and evaluation of a 10-bit 32 MS/s pipelined ADC. The measured results show that the ADC exhibits a THD of −62 dB and a spurious free dynamic range (SFDR) of 63.8 dB, corresponding to an ENOB of 8.5 bits at the Nyquist rate. Also, the robustness of the front-end is secure, as reduced voltages are applied to the gate of the sampling switches when rail-to-rail input voltage is present, smaller than +112% and −6% of the nominal V_{DD}, respectively for the NMOS and for the PMOS devices.

7.2. Architecture description

The simplified block diagram of the overall architecture of the implemented 10-bit 32 MS/s pipelined ADC is shown in Figure 7.1. The system consists of an input front-end fully-differential S/H, followed by a cascade of eight stages with minimum resolution-per-stage. Each stage comprises a 1.5-bit multiplying digital-to-analog converter (MDAC) and a 1.5-bit

flash quantizer. At the end of the pipelined chain, there is a 2-bit flash quantizer. Conventional structures are employed in the main building-blocks. Both, the S/H and the 1.5-bit MDACs employ the standard closed-loop flipped-around topologies and the comparators used in the 1.5-bit and 2-bit flash quantizers are based on an input SC network to define the threshold level followed by a positive feedback latch and then by a digital SR-type latch. In order to achieve enough DC gain over PVT corners and minimum degradation in the feedback factors together with high power efficiency, two-stage cascoded-compensated amplifiers with NMOS input differential-pair are used in the S/H and in all MDACs.

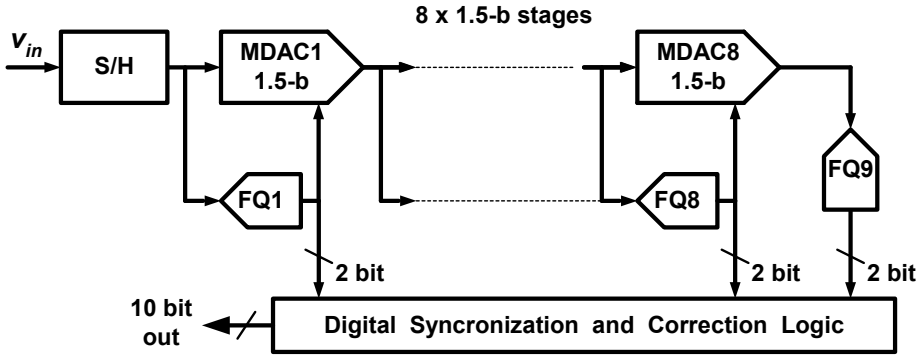


Figure 7.1: 10-bit pipelined ADC architecture.

The output bits of the different stages are synchronized and, after digital correction, a net 10-bit digital output is obtained. The circuit is controlled by two non-overlapped control signals, ϕ_1 and ϕ_2, and their complementary versions, ϕ_{1n} and ϕ_{2n}. The choice of having adopted a two-phase clocking scheme rather than the single-phase scheme described in Chapter 6 is explained by the fact that it was intended to validate in silicon the bandwidth of operation of the proposed SLC circuits. Hence, to allow a 32 MS/s sampling rate together with sub-sampling operation (with f_{in} much larger than the sampling rate), larger sampling switches had to be used and, therefore, the expected small degradation in the sampled charge would not be valid any more (the single-phase technique works perfectly as long as small switches are employed, i. e., for small input signal bandwidths and moderate sampling rates). However, a conventional four-phase clocking scheme was not employed, since the four-phase scheme (plus the four complementary ones) was simplified into a two-phase scheme. The reason is that the SLC circuits also provide an inherent delay between the input phases and the "regulated/boosted" output phases (similar to the clock-bootstrapping circuits) which implement, "by free", the bottom-plate sampling technique [44]. As a consequence, delayed versions of the sampling phases are no longer required and, hence, they were not used.

7.3. The front-end S/H circuit

The differential implementation of the S/H is shown in Figure 7.2. Each signal path of the circuit comprises four equally sized sampling blocks, for sub-sampling operation and programmable gain flexibility purposes. Each block comprises sampling switches, S_{p1} to S_{p4} and S_{n1} to S_{n4}, feedback switches, S_{p5} to S_{p8} and S_{n5} to S_{n8}, and sampling capacitors, C_{Sp1} to C_{Sp4} and C_{Sn1} to C_{Sn4}. The top-plates of the four capacitors are all tied to the inputs of the amplifier (for bottom-plate sampling operation). During the sampling phase, ϕ_1, switches S_{p9}, S_{n9}, S_{10} and the sampling switches are ON, charging the capacitors with the difference between the input voltage, v_{inp}, and the positive reference voltage, V_{HI}[6]. In this phase, both the differential inputs and outputs of the amplifier are shorted since it is in open-loop. During the holding phase, ϕ_2, the feedback switches are ON and the four sampling capacitors are flipped-around providing a feedback-loop to the amplifier.

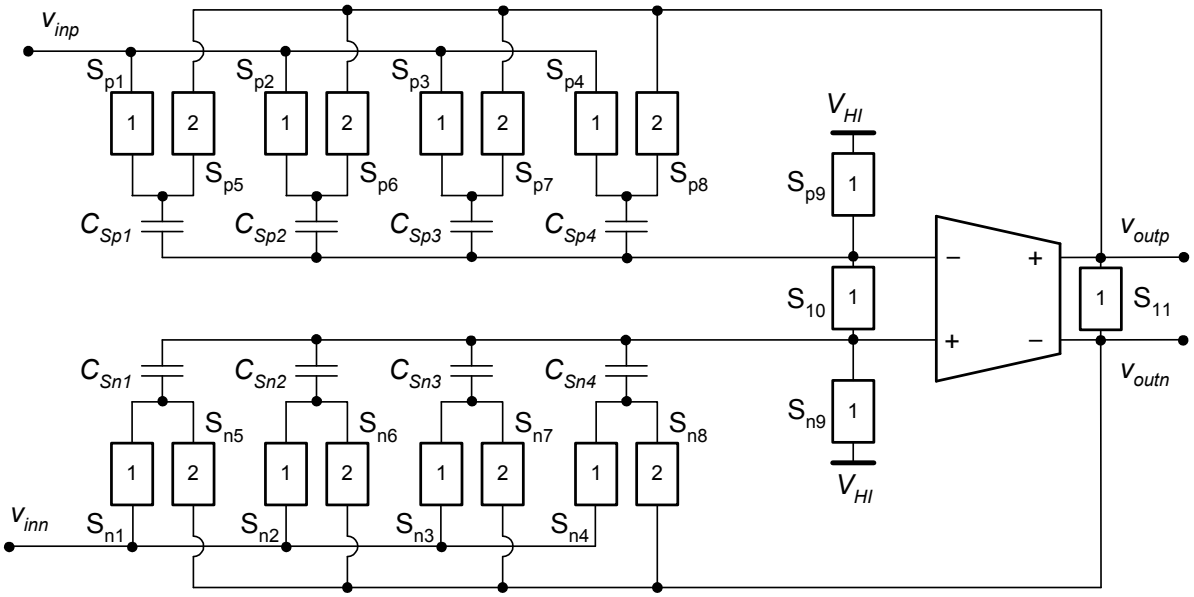


Figure 7.2: SO/CBT realization of the S/H.

Each one of the four sampling capacitor is sized with a nominal capacitance value of 1 pF due to kT/C noise constraints. The feedback switches are made of asymmetric transmission gates (ATGs) with bulk-switching, being directly controlled by holding phase, ϕ_2, and its complementary version, ϕ_{2n}. The main NMOS and PMOS switches are sized with aspect

[6] - The reason for using V_{HI} is related with the fact that the input differential-pair of the amplifier is made of NMOS devices (as stated before).

ratios of 10/0.12 and 36.5/0.12, respectively. The bulk-switching feature is ensured by two extra PMOS switches *per* each ATG, both sized with 4/0.12. The values of the used voltages are V_{HI}= V_{REFP}= 0.8 V and V_{DD}= 1.2 V. The sampling switches are also made of ATGs, with the NMOS device sized with an aspect ratio of 25/0.12, and the PMOS device with 90/0.12. The four ATGs of each path are controlled, two by two, by one SLC circuit, with bulk switching control, as suggested in Chapter 5, resulting in a total of four SLC circuits implemented. The SLC circuit provides the optimum (regulated) gate and bulk voltages, as a function of the input voltage level and sampling phase, ϕ_1. The schematic of the SLC circuit is shown Figure 7.3. The auxiliary NMOS devices are sized with aspect ratio 1/0.12, and the PMOS devices with 4/0.12. The SLC circuit provides the required gate voltages to drive the four main devices, M_{p1} and M_{n1} (CMOS switch S_{p1} in Fig 7.2), and M_{p2} and M_{n2} (CMOS switch S_{p2} in Figure 7.2). The circuit reduces the gate overdrive of the NMOS or of the PMOS devices, when the input signal is, respectively, close to V_{SS} or to V_{DD}, obtaining the linearization of the equivalent conductance. More, the circuit also provides the adequate voltages to the bulk of M_{p1} and M_{p2}. When the PMOS devices are ON, the bulk voltage is v_{in}, and during the OFF period, the bulk voltage is V_{DD}.

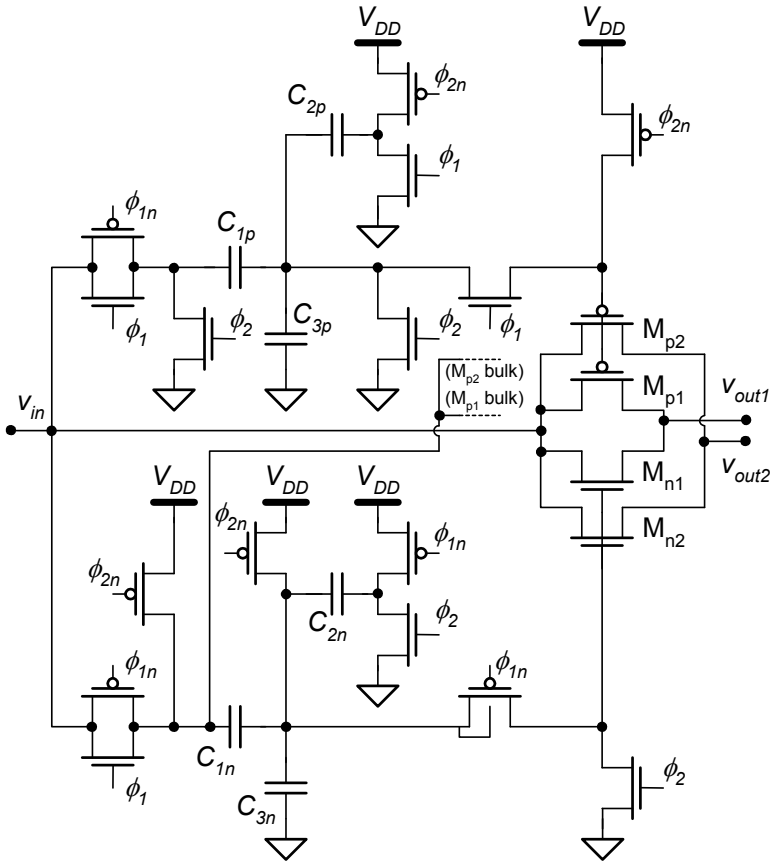


Figure 7.3: Schematic of the SLC circuit.

The output v_{out1} is connected to C_{Sp1}, and the output v_{out2} to C_{Sp2}. Other similar circuits control the S_{p3} and S_{p4}, the S_{n1} and S_{n2}, and the S_{n3} and S_{n4} CMOS switch pairs.

The SLCn circuit generates an output voltage, v_{Gn}, to drive the NMOS device, approximately given by (7.1), already presented in this Thesis but here reproduced for convenience.

$$v_{Gn} = v_{in}\underbrace{\frac{C_{1n}+C_{gn}}{C_{1n}+C_{2n}+C_{3n}+C_{gn}}}_{K_{1n}} + V_{DD}\underbrace{\frac{2C_{2n}+C_{3n}+C_{gn}/2}{C_{1n}+C_{2n}+C_{3n}+C_{gn}}}_{K_{2n}} \tag{7.1}$$

The output voltage, v_{Gp}, to drive the PMOS device, is given by (7.2) (also reproduced here for convenience).

$$v_{Gp} = v_{in}\underbrace{\frac{C_{1p}+C_{gp}}{C_{1p}+C_{2p}+C_{3p}+C_{gp}}}_{K_{1p}} + V_{DD}\underbrace{\frac{-C_{2p}+C_{gp}/2}{C_{1p}+C_{2p}+C_{3p}+C_{gp}}}_{K_{2p}} \tag{7.2}$$

The capacitance values of the auxiliary capacitors used in the SLC sub-circuits should be as low as possible. The values must also ensure an effective control of the gate voltages, v_{Gn} and v_{Gp}, by attenuating the influence of the nonlinearity of the gate capacitance of the main devices, C_{gn} and C_{gp}. Only one SLC is used to control two sampling switches, and then the value of the gate capacitance used for computation must be the sum of the values of the individual capacitances.

To compute the suitable values of the auxiliary capacitors, it is recommended to start with the definition of the value of C_{3n}. The set value must be low, but high enough to overcome the gate capacitance influence. It is assumed to be 200 fF. More, the targeted value for K_{1n} factor is assumed to be 0.5, the average value between the unity and zero, which would end up, respectively, into a conventional CBT switch or into a conventional NMOS switch. After the definition of the tolerable maximum value of the main NMOS device gate voltage, C_{1n} and C_{2n} can be computed and sized with 420 and 240 fF. The NMOS and the PMOS switches maximum conductance value must be equal. They are sized asymmetrically, and then the absolute value of the maximum effective gate voltage of both switches must be equal. More, the gate voltage variation, with respect to v_{in} variation, should present approximately the same

slope value in both cases, *i.e.* $K_{1n} \approx K_{1p}$. Therefore, assuming a value of 40 fF for C_{1p}, and using the value of the threshold voltages to obtain the effective gate voltages, C_{2p} and C_{3p} are computed and sized with 190 fF and 1 pF.

7.4. Simulation results

The S/H block circuit was simulated, in typical conditions, for a sampling clock frequency F_S = 32 MS/s and for a wide range of differential input signal frequency values. A 4096-bin FFT of the simulated results of the differential output of the sampling block ($v_{outp} - v_{outn}$) is shown in Figure 7.4, when a frequency f_{in} = 31 MHz (sub-sampling operation) and a peak-to-peak single-ended amplitude A_{in} = ± 500 mV is applied to the differential inputs of the S/H circuit. The typical simulated SFDR is 80 dB and the THD is −66.5 dB.

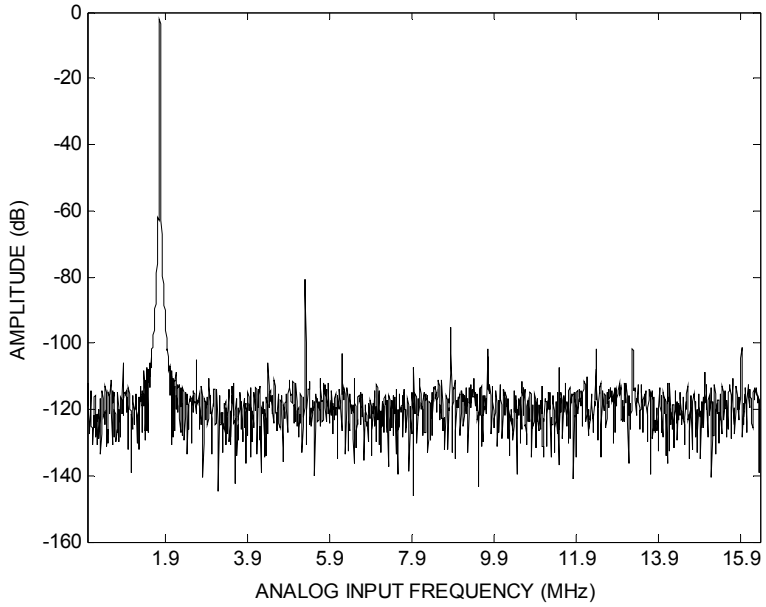


Figure 7.4: Simulated results of the output of the S/H circuit for a 31 MHz input signal.

Using the same conditions, a simulated 4096-bin FFT was also obtained, as it is shown in Figure 7.5. This time, a frequency f_{in} = 63 MHz (again with the S/H operating in sub-sampling mode) is applied to the differential inputs of the S/H circuit. The typical simulated SFDR is 67 dB and the THD degrades to about -61 dB.

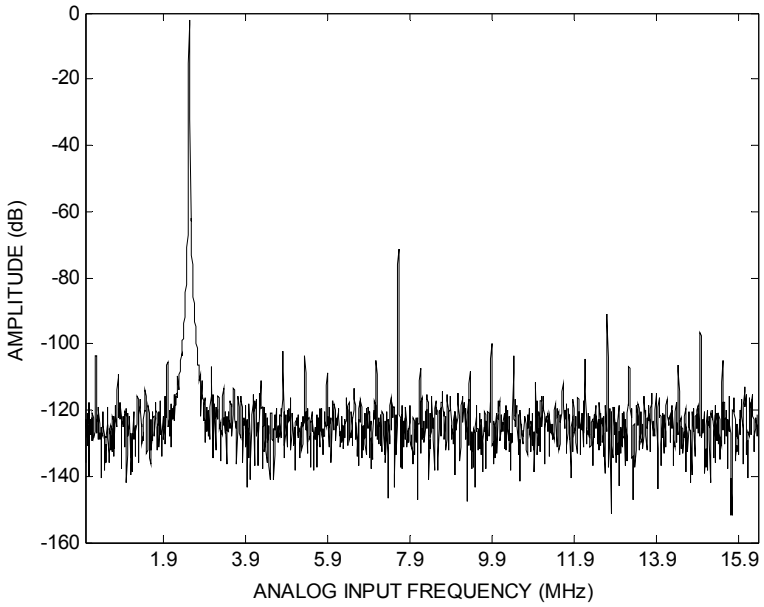


Figure 7.5: Simulated results of the output of the S/H circuit for a 63 MHz input signal.

Many other simulations were exhaustively carried out across the most important PVT corners (worst-speed, worst-gain, worst-stability and worst-power). However, since the fabricated prototype samples were close to the typical process parameters (accordingly to information provided by the foundry) and since all the measurements were performed at nominal supply voltage (1.2 V) and nominal room temperature (27 ºC), for the sake of simplicity, the referred simulated results are not listed here but they are similar to the ones shown before in Chapter 5.

7.5. Integrated prototype

An integrated prototype of a 1.2 V, 10-bit, 32 MS/s pipelined ADC, using the proposed SLC circuit technique, was fabricated in a 130 nm single-poly eight-metal (1P-8M) high-speed (HS) CMOS process with metal-insulator-metal (MiM) capacitor option. Only six levels of metal were used.

Figure 7.6 shows the die microphotograph (with overlaid layout plot) of the integrated ADC prototype and S/H block. The ADC (S/H included) occupies an area below 0.29 mm^2, and the front-end S/H occupies less than 0.052 mm^2.

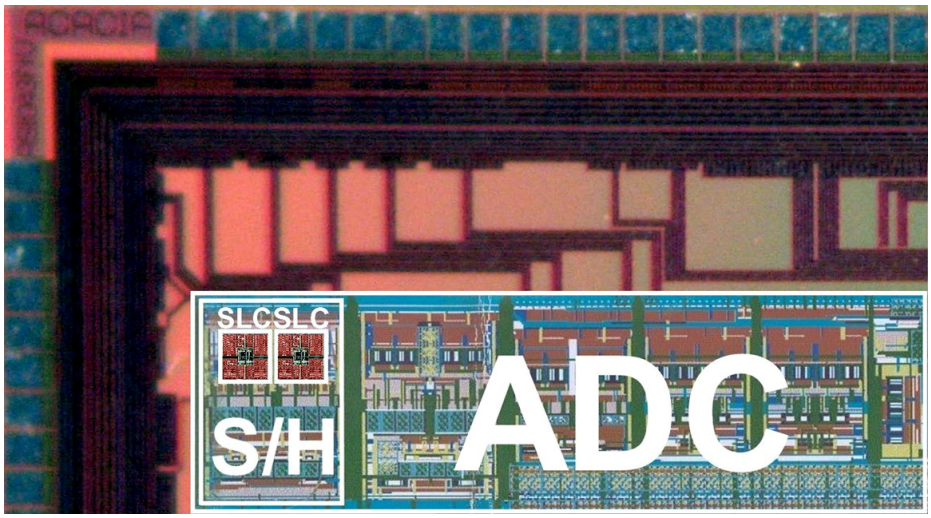


Figure 7.6: Die microphotograph (with overlaid layout plot) of the ADC, with front-end S/H block

The die microphotograph (with overlaid layout plot) of two SLC circuits is shown in Figure 7.7. In the left half part is one SLC, in the half right part is the other, as a mirrored image. The SLCp and the SLCn sub-circuits are in the upper and lower half parts, respectively, being visible the three auxiliary capacitors (that occupy most of the area) of each sub-circuit. The area is approximately squared (for convenience layout reasons) and the two SLC circuits occupy less than 0.005mm^2, *i.e.* 9 % of the S/H area. For shielding reasons (mainly related with possible substrate noise), all transistors used in the two SLC circuits were enclosed within the total of 12 capacitors employed in the proposed structure.

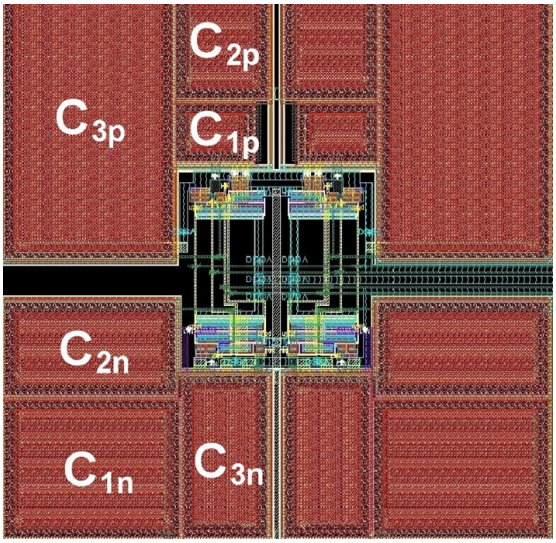


Figure 7.7: Die microphotograph (with overlaid layout plot) of two SLCs.

7.6. Measured results

In the test setup, a low-jitter square-wave obtained from a Marconi IFR 2041 is used for driving the CMOS level clock input. The input signal is generated using an Arbitrary Waveform Generator (Tektronix AWG 510) and the input signal frequency is filtered using an external discrete (and trimmed) 6^{th}-order passive 10% band-pass filter (10.7 MHz ± 500 KHz (Allen Avionics). Output data was acquired using a logic analyzer (Agilent 16702B) and then it was transferred into a PC for MATLAB analyses. The chip and all external auxiliary circuits were supplied using an HP 6624A power supply.

The results presented in this Section have been measured for Sample #1, assembled into a CQFP 120L package, at room temperature and nominal supply voltage of 1.2V. A programmable gain of 0 dB (unity gain) in the S/H was set. Two types of chip assembly were considered: a large CQFP 120L package and also direct chip-on-board (CoB) assembly. Due to the relatively low sampling rates used, performance enhancements with CoB PCB were not visible.

7.6.1. Measurement 1: static DNL/INL measurements at 32 MS/s

The ADC input was set to 1.1 V_{ppdiff} (to provide output saturation in order to allow applying an histogram testing algorithm) and the signal was sampled at 32 MS/s with f_{in} = 100 kHz. This measurement used the 0 dB programmable gain. Figure 7.8 shows the static DNL and integral nonlinearity (INL) measurement of a 10-bit ADC prototyped sample.

Measured results demonstrate that the circuit exhibits DNL (small signal behaviour) and INL (strong signal behaviour) errors compatible with, 10-bit and 9-bit of static accuracy, respectively.

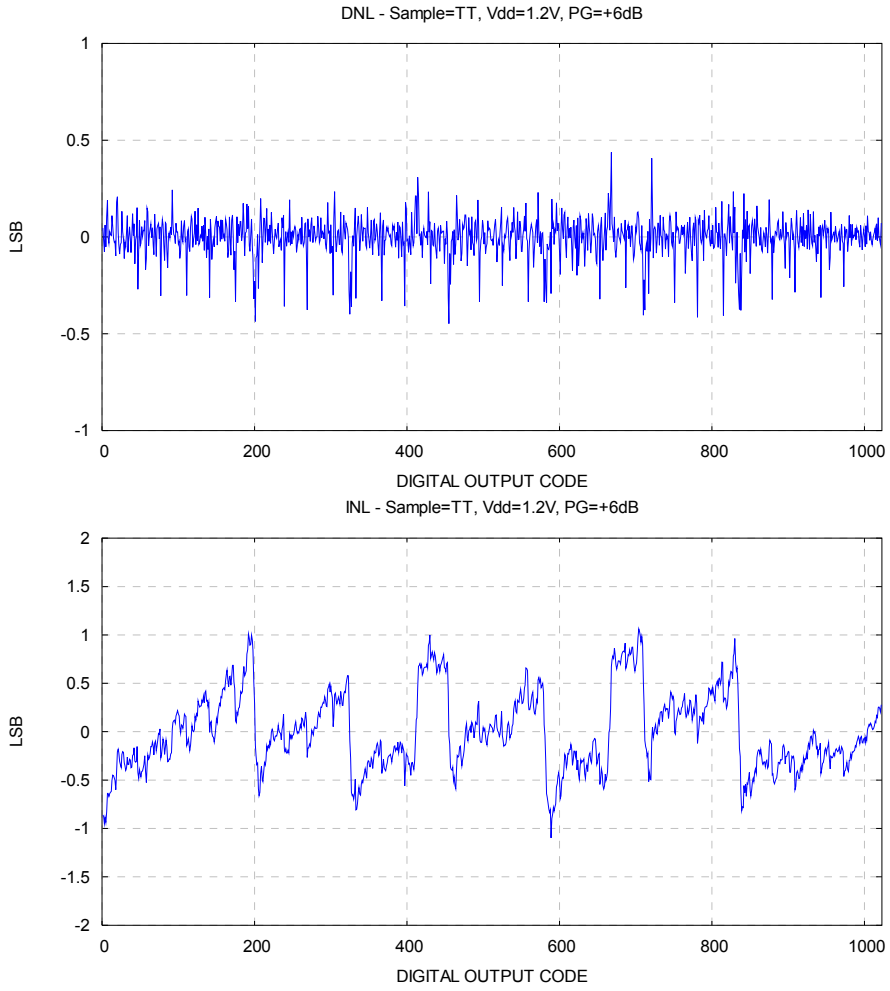


Figure 7.8: Measured DNL and INL of the 10-bit ADC in typical conditions and at 32 MS/s sampling rate

7.6.2. Measurement 2: dynamic measurements (FFTs) at 32 MS/s

Again, the results presented in this Section have been measured for Sample #1, CQFP 120L, at room temperature and nominal supply voltage of 1.2 V. ADC input was set to 0.86 V_{ppdiff} and the signal was sampled at 32 MS/s for different input signal frequencies, f_{in}.

For f_{in} very low (*e.g.* 1 MHz), the measurements of the most important dynamic performance parameters give, a SFDR, a THD, an signal-to-noise ratio (SNR) and an signal-to-noise-plus-distortion ratio (SNDR) respectively of 67 dB, −62.5 dB, 55.3 dB and 54.5 dB. These results are compatible with an ENOB of 8.8 bits.

The measured FFTs of the ADC, 4096 points and 20 averages, clocked at 32 MS/s, when a −1.8 dBFS full-scale input of 31 and 63 MHz is applied, are shown in Figure 7.9 and Figure 7.10, respectively.

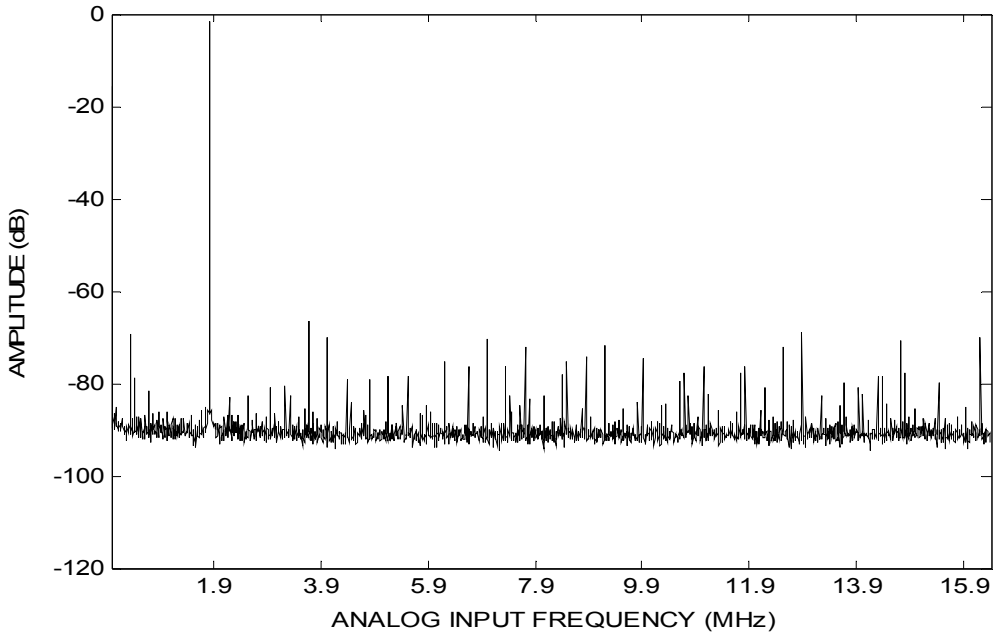


Figure 7.9: Measured FFT spectrum of the output of the ADC in sub-sampling, for a 31 MHz input signal.

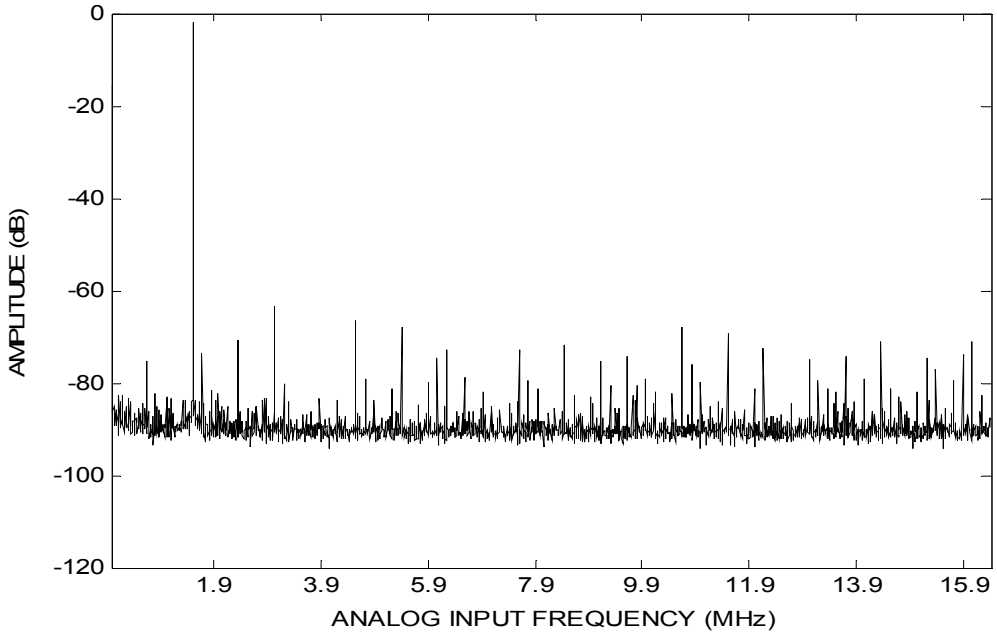


Figure 7.10: Measured FFT spectrum of the output of the ADC in sub-sampling, for a 63 MHz input signal.

The measured results of the ADC, for input frequencies, f_{in}, of 1 MHz, 31 MHz and 63 MHz, are summarized in Table 7.1. The performance of the ADC achieves a peak SNR of 55.3 dB, a THD of −62.5 dB, a SFDR of 65 dB and an ENOB of 8.8 bits at the Nyquist frequency. The SFDR measured results (with low frequencies input signals) are fully compatible with the static DNL measurements (10-bit linearity).

Table 7.1: Measured results for different input frequencies.

f_{in} (MHz)	Amplitude (dBFS)	SFDR (dBc)	THD (dB)	SNR (dB)	SINAD (dB)	ENOB (bit)
1	−1.8	65	−62.5	55.3	54.5	8.8
31 (sub-sampling)	−1.7	63.8	−61.4	53.7	53.1	8.5
63 (sub-sampling)	−1.8	61.6	−58.4	52.9	51.8	8.3

Likewise, the THD results are also fully compatible with the INL results. Hence, as expected, both, static and dynamic performance parameters are limited by the maximum achievable matching accuracy of the sub-micron CMOS process available today, which is bounded to 10-bits. As a consequence, without expensive trimming or employing self-calibration techniques, any pipeline-type ADC has its SFDR and THD performance limited to 65 to 70 dB and −62 to −68 dB, respectively.

Hence, one can conclude that, the SLC circuits used in the front-end S/H of the referred ADC do not add any significant dynamic error, since both, the SFDR and the THD results exhibit a pretty flat behaviour over an entire bandwidth of 63 MHz.

The SFDR and the THD results for different input frequencies, of the simulated S/H and of the overall implemented circuit, are respectively shown in Figure 7.11 and Figure 7.12.

As previously referred and expected, only at “very high” input signal frequencies (of course, when compared with the Nyquist rate) the SLC circuits start degrading both the SFDR and the THD performance.

Notice that five samples were tested and the measured dynamic performance parameters only have minor differences below ±1 dB.

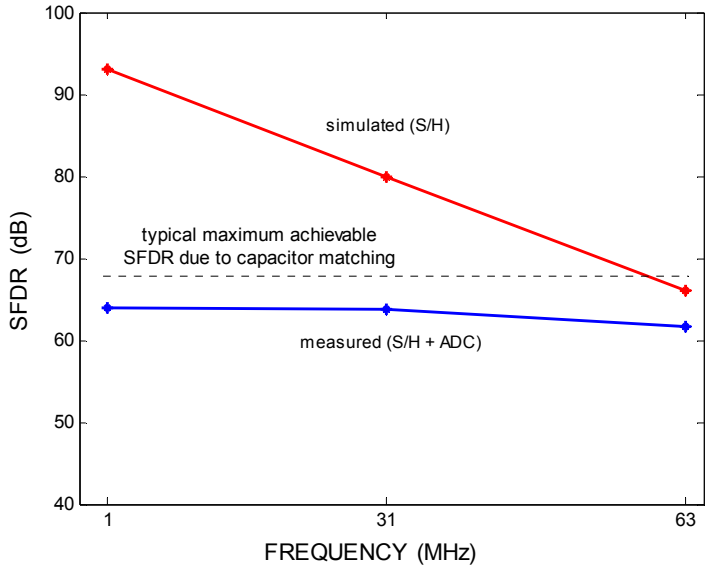


Figure 7.11: SFDR of output of the complete ADC (measured) and of the S/H (simulated), for different input signal frequency.

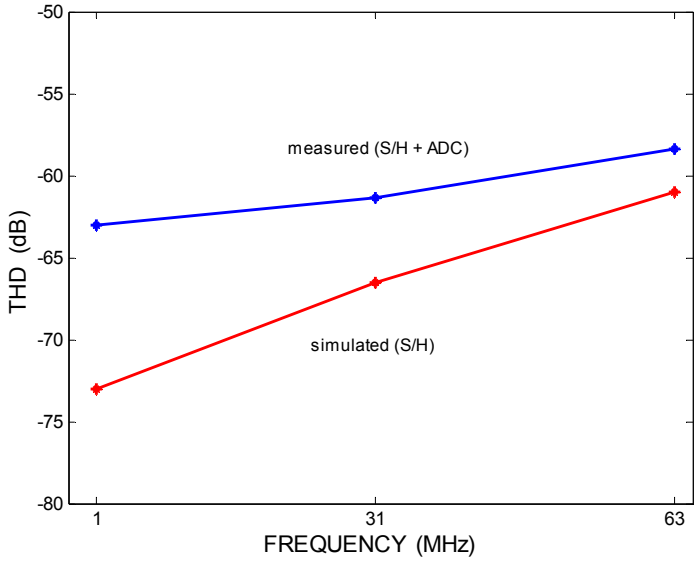


Figure 7.12: THD of output of the complete ADC (measured) and of the S/H (simulated), for different input signal frequency.

7.7. Conclusions

The design and the experimental evaluation of a 10-bit 32 MS/s pipelined ADC operating beyond Nyquist, with the sampling switches of the differential S/H employing SLC linearization circuits to guarantee linearity without over-stress, is presented. The measured

results prove the functionality and the efficiency of the proposed technique. These experimental results show that the adopted SLC technique is capable of overcome the challenges existing in the design of the S/H of a high-resolution ADC, allowing high sampling rates. The effectiveness of the SLC circuit is shown by the obtained measured results, showing a THD of −62 dB, a SFDR of 63.8 dB and an ENOB of 8.5 bits at the Nyquist frequency. Also, the life span is secure, as reduced gate voltages are applied, smaller than +112% and −6% of the nominal V_{DD}, over the rail-to-rail input voltage swings.

8. Conclusions

8.1. Reachearch overview

Several proposals and suggestions, aiming the improvement of switched-capacitor circuits, have been made in this work.

After the opening first Chapter, where an overview of this work has been presented, in the indispensable second Chapter the context set by the deep sub-micron technologies was discussed.

In the third and fouth Chapters the challenges of the switches, the complexity of the circuits and of the amplification structures are analyzed and questioned.

In the fifth Chapter, the proposed solution was analyzed in detail, step-by-step designed, and the performance and the usefulness shown.

In the sixth Chapter two design demonstrators were presented, where the effectiveness and utility of the proposals and suggestions are revealed and confirmed.

Finally, in the seventh Chapter a practical realization of a pipelined ADC in integrated circuit, where the proposed new switch-linearization technique is used, has been shown.

The results show that every single improvement contributes to achieve the goal, which is better performance. The MDAC open-loop structures, the local feedback amplifiers, their combination, the single-phase technique and the switch-linearization circuit can be used in SC designs, where the requirements are for either high linearity with high speed of operation, or for low power dissipation, or even for high reliability and security.

8.2. Future work

Further research of the work developed and presented in this Thesis can be carried out. Maintaining the initial objectives, the future work should be focused in the continuation of the

study and reseach of new contributions and solutions to improve the performance of SC circuits towards 65nm, 40nm and 32nm CMOS technologies.

In particular, we envisage the following areas can be interestingly pursued.

a) The use of other type of amplifiers with local feedback in the open-loop MBTA and MDAC schemes. For example, the use of the self-biasing inverter amplifiers [115] can provide higher energy efficiency and, at the same time, exhibiting high rouboustness against PVT variations. Searching new circuits with accurate charge transfer, either without OpAmps, or using low-performance OpAmps. Also clsed-loop SC structures insensitive to finite gain variations and also insensitive to capacitors mismatch [116 to 119] could be further investigated;
b) The area efficiency improvement of the SC circuits by using MOS capacitances instead of metal-on-metal or MiM capacitors. The demonstration in silicon that the reduced linearity (voltage dependency) of the MOS capacitances is not critical in the overall performance, at least for levels of accuracy of the order of 6 to 8 bits;
c) The demonstration of the many advantages of some of the techniques explained in this Thesis (*e.g.* the SLC circuits and the single-phase clock scheme) in 65, 40 and 32 nm technology.

In fact, we strongly believe that the investment in future research in these areas can bring additional and efficient solutions to overcome the constraints the SC circuits, based in CMOS technology, are facing nowadays.

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