NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTAMENT OF MATERIALS SCIENCE

André de Seia Fontelo Pinho Dias

BSc in Micro and Nanotechnologies Engineering

Fabrication, process optimization and copper electroplating for Through-Silicon Vias metal contacts

MASTER IN MICRO AND NANOTECHNOLOGIES ENGINEERING

NOVA University Lisbon

September, 2024

NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTAMENT OF MATERIALS SCIENCE

Fabrication, process optimization and copper electroplating for Through Silicon Vias metal contacts

André de Seia Fontelo Pinho Dias

BSc Micro and Nanotechnologies Engineering

Adviser: Michael Kraft
Full Professor, KU Leuven

Co-adviser: Joana Vaz Pinto
Associate Professor, NOVA University Lisbon

Examination Committee:

Chair: Name of the committee chairperson,
Full Professor, FCT-NOVA

Rapporteurs: Name of a rapporteur,
Associate Professor, Another University
Name of another rapporteur,
Assistant Professor, Another University

Adviser: Name of the adviser present in defense,
Associate Professor, University

Members: Yet another member of the committee,
Full Professor, Another University
Yet another member of the committee,
Assistant Professor, Another University

MASTER IN MICRO AND NANOTECHNOLOGIES ENGINEERING
NOVA University Lisbon
September, 2024

Fabrication, process optimization and copper electroplating for Through Silicon Vias metal contacts

Dedicated to my family and friends,

ACKNOWLEDGMENTS

First of all, I would like to express my sincere appreciation to everyone who made this project possible. I am grateful to KU Leuven, especially to Professor Michael Kraft for giving me the opportunity of working in KU Leuven's Nanocenter under the Micro & Nanosystems (MNS) guidance.
I also want to thank my university NOVA school of science and technology, specifically to the department of material science and all the teachers from whom I learned so much during these 5 years.
I am thankful for all the support and guidance provided by my daily supervisors, Researcher Sanjog Vilas Joshi and Dr. Sina Sadeghpour.
I would also like to express my gratitude to Prof. Joana Vaz Pinto, that made huge efforts in terms of availabilty and help provided for this project.
To all my friends, old or recent, that are spread all across the world. Every single one of you was more important for my thesis than you know, thank you for the moments we made during these past years.
I also have to thank my loving girlfriend and Billy that supported me for months while I was away, carrying out this project.
Lastly, I would like to thank my family for giving me the possibilities, throughout all the years, that allowed me to dedicate my time to my studies and live the experiences abroad that resulted in this project.

ABSTRACT

With the growing demand for Three-dimensional integrated circuits, wafers with through-silicon connections are highly advantageous, enabling for more compact designs. For the past decades, electroplating has been effectively used for metal insertion in through-silicon vias (TSVs). However, there remains a need for cost-efficient processes and viable wafer designs. This project aimed to replicate this TSV technology for vias with significantly larger diameters than previously reported, exploring various designs and methods through trial and error clean-room work.

Two types of vias were tested: 200 μm vias created by laser and 110 μm vias produced by Deep Reactive Ion Etching (DRIE), with greater emphasis on the latter. By drilling the vias post-wafer processing, promising results were achieved, including a reproducible process for vertical and selective etching. Although copper deposition proved challenging to control, this project presents a potentially viable alternative to established methods in the field. Detailed recipes for Sputtering, DRIE, Reactive Ion Etching, Spin-coating, UV Mask Aligner, and Electroplating that were all tuned, optimized or created in this project, are provided in the document.

Key Words: Through-silicon vias, Deep Reactive Ion Etching, Electroplating, Three-dimensional Integrated circuits.

RESUMO

Com a introdução e evolução de circuitos integrados tri-dimensionais, as wafers com ligações através do silício são altamente vantajosas, permitindo designs mais compactos. Durante as últimas decadas, a eletrodeposição tem sido utilizada eficazmente para inserir metais em Through-silicon vias (TSVs). No entanto, continua a existir a necessidade de processos que apresentem custos reduzidos e de designs de bolachas viáveis. Este projeto teve como objetivo replicar a tecnologia TSV para vias com diâmetros significativamente maiores do que os relatados anteriormente, explorando vários designs e métodos através de trabalho desenvolvido em ambiente de sala limpa, numa base de tentativa e erro.

Foram testados dois tipos de vias: vias de 200 μm criadas por laser e vias de 110 μm produzidas por Deep Reactive Ion Etching (DRIE), com maior ênfase nesta última. Ao perfurar as vias após o processamento da wafer, foram alcançados resultados promissores, incluindo um processo de fácil reprodução, que apresenta um etching vertical e selectivo. Embora a deposição de cobre tenha sido difícil de controlar, este projeto apresenta uma alternativa potencialmente viável aos métodos estabelecidos neste domínio. As receitas detalhadas para Sputtering, DRIE, Reactive Ion Etching, Spin-coating, UV Mask Aligner e Electroplating, todas optimizadas neste projeto, também se encontram presentes no documento.

Palavras-chave: Through-silicon vias, Deep Reactive Ion Etching, Eletrodeposição, Circuitos Intergrados tri-dimensionais.

CONTENTS

LIST OF FIGURES

List of Tables

ACRONYMS

IC	Integrated Circuit
TSV	Through-Silicon Via
DRIE	Deep Reactive Ion Etching
3D	Three-dimensional
ICP	Inductively Coupled Plasma
UV	Ultraviolet
RIE	Reactive Ion Etching

SYMBOLS

nm	Nanometer
µm	Micrometer
cm	Centimeter
m	Meter
In	Inches
rpm	Rotations per minute
min	Minutes
s	Seconds
W	Watts
sccm	Standard cubic centimeters per minute
mJ	Milijoule
r	Radius
h	Height
$\mathbf{n_v}$	Number of Vias
I	Current
Q	Charge
t	Time
$\mathbf{n_{e}}$**-**	Molar quantity of electrons
F	Faraday's constant (96485 C/mol)

A	Ampere
C	Couloumb

1

MOTIVATION AND OBJECTIVES

With the vast technological advancements of the past decades, integrated circuits research and development is now betting on stacking technology with Three-dimensional intergrated circuits, to optimize space and allow for more ambitious designs. Since reduced package size and short interconnections are very desirable, Through Silicon Vias (TSV) technology is regarded as essential for progressing in this field [1].

The initial master thesis proposal was to try and find a way to fabricate these Through Silicon Vias by using an Electroplating method on processed vias. This would have to be achieved using the tools present in the Nanocenter at KU Leuven, with the goal of making a simple and low-cost process that could have an easy reproducibility, as this would allow the Micro & Nanosystems group to incorporate this technology on their ongoing and future research. High-aspect ratio TSV's are desirable for performance reasons so, generally, the value for the vias' diameter varies from 5 μm to 20 μm, with some researchers already showing some concerns when dealing with a 30 μm diameter [2]. This presented itself as the biggest challenge for this work, since both the laser used to pre-drill the wafers and the mask that would prepare samples for the Deep Reactive Ion Etching system only allowed for diameters of 200 μm and 110 μm, respectively.

Since it was a new process being introduced to the group, most of the recipes and processes would have to either be created from scratch or optimized extensively and this made it hard to predict what realistic goals were. Using previous clean-room knowledge, experience and problem-solving skills, the main objective of this project was to bypass any limitations that the lack of some equipment and information on similar processes would bring.

2

INTRODUCTION

One of the most challenging areas of research and development in Intergrated Circuits (IC) has to do with the packaging that allows the device to be used in any system. Packaging has to take several factors into account, dealing with thermal, mechanical, environmental and electrical dilemmas [3]. In this project, the focus will be given to the electrical challenges, since it is critical to ensure an electrical connection between the package and the IC. This can be achieved with different methods and technologies, but even with transistors getting smaller each day, there is always a need for space optimization and from this, the concept of Three-dimensional (3D) IC's was created. With the growing industries of these 3D IC's, having wafers with through-chip connections is highly beneficial for the performance of these devices.

2.1 Electrical IC Packaging Timeline

Wire Bonding

The concept of wire bonding was introduced at the end of the decade of 1950, there are some different processes for this packaging method, but they all consist of creating thin wires (usually made of gold, aluminum or copper) to establish electrical connection between the bonding pads on a chip and the corresponding terminals on a package or substrate. These wires are then covered in resin to prevent them from being damaged. To this day it still is one of the most used methods for IC packaging due to its flexibility and cost-effectiveness, but it compromises in space and electrical connectivity [4].

Flip Chip

The next step forward came in the form of the Flip Chip technology, that instead of connecting these pads through wires, the chip is flipped so that the metal contacts are facing the substrate. The electrical contact between chip and substrate is established in one of several different ways, for example, by solder bumps (either on the chip or on the substrate), conductive polymer flip-chip, anisotropic conductive flip-chip, wire flip-chip or metallurgy flip-chip [4].
When compared to Wire Bonding, Flip Chip can achieve more connections per area and shorter electrical paths that are crucial for high-speed, high-frequency circuits [5].

3D Integrated Circuits and Through-Silicon Vias

Traditional IC circuits were fabricated on flat silicon wafers, which restricted this technology to only two dimensions, and with both the gate length and oxide thickness of modern transistors reaching their physical limits, a new approach that would allow researchers to integrate as many transistors into a chip as possible was necessary [6]. Stacking the flat wafers would allow for unforeseen levels of space optimization, but the old methods of ensuring an electrical connection would not work in this 3D setting and that is what ultimately led to the TSV technology, illustrated in Figure 1.

Through-silicon vias (TSV) are electrical interconnects that are placed, as the name indicates, through the wafer itself, effectively establishing a connection from the frontside to the backside. This also opens the possibility for 3D circuit integration, the exposed TSV metal on the surface of the wafer can be used as a contact and by stacking two of these wafers, a connection between the two is established. The whole process can then be repeated to achieve an electrically connected stack of wafers [7].

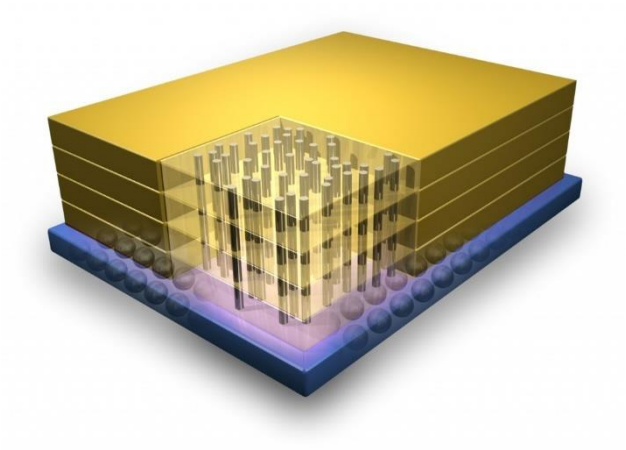

Figure 1 - Illustration of TSVs in a 3D-IC

This technology's main advantage is the reduced interconnect length with short vertical connections through the wafers/chips. They also present a reduced latency, with lower inductance and capacitance, while allowing for a higher number of interconnections and lower power, as well as high speed communication links between and within circuits [7]. They can be separated into three groups, depending on when these TSVs are fabricated in relation to the semiconductor device: via-first, via-middle and via-last [8]. Both via-first and via-last processes were implemented and experimented with during the duration of this project.

2.2 Deep Reactive Ion Etching

In order to fabricate the previously mentioned TSVs, the first thing to do is etching the wafer, in order to obtain holes that can be later filled with metal and make the desired metal vias. The DRIE is an Inductively Coupled Plasma (ICP) etching system that was introduced by Bosch in the 1990s and it can be a good solution for this goal, since it allows for quality vertical etching processes [9].

Frequently refered as dry etching, both the etchant and the by-products of the etching process are gases that, by being able to penetrate into small spaces, allow for a far more detailed etch than other methods [10]. The Bosch process, depicted in Figure 2 below, starts with the plasma ignition, that is generated under vacuum by an electromagnetic field, after this, what generally is referred to as the Strike step occurs, where a reactive gas is inserted into the chamber (Oxygen, for example) for an initial shallow etch that activates the silicon surface, making it more reactive and to facilitate the process of removing the native oxide layer that naturally forms on silicon, when it is left exposed. The etching gas is then, inserted into the chamber for the Etching step, converted into plasma from the electromagnetic field, its ions bombard the substrate vertically, creating a small depression in the Silicon [10] [11]. The last step to what is considered a DRIE cycle is what is generally called as the Deposition Step, where a C_4F_8 is introduced into the system, in order to generate a Fluorocrabon polymer that adheres to the sidewalls of the previously etched depression and passivates it. During the next etching step, the ions will attack this passivated layer at the bottom of the via, effectively etching it away to reach the silicon and etch a bit more, the sidewalls however are sufficiently protected by the polymer to prevent etching from ocurring in that direction from deflected ions [12]. This passivation and etching steps intercalate with one another, ensuring that a highly anisotropic process occurs.

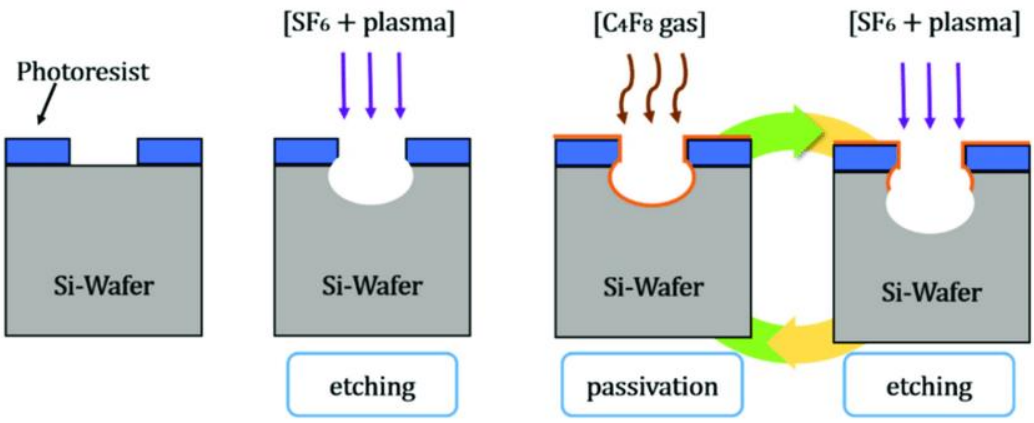

Figure 2 - DRIE process depiction [17]

2.3 Electroplating

After the vias are done via DRIE, they now need to be filled with metal. This is where Electroplating, the most common metallization method for TSV fabrication [13], comes in as an essential part of this project's goal. It is an electrodeposition process that is often used as an alternative to sputtering or evaporation processes, to produce thick layers (typically >5 μm) of metal that are challenging to achieve using those other methods, mostly due to adhesion problems [14]. This is a liquid-based process and it does not require any costly vacuum equipment, which is a big advantage [15], both an example of a typical electroplating mechanism, as well as an illustration of a common setup for fabrication of TSVs can be found below in Figure 3.

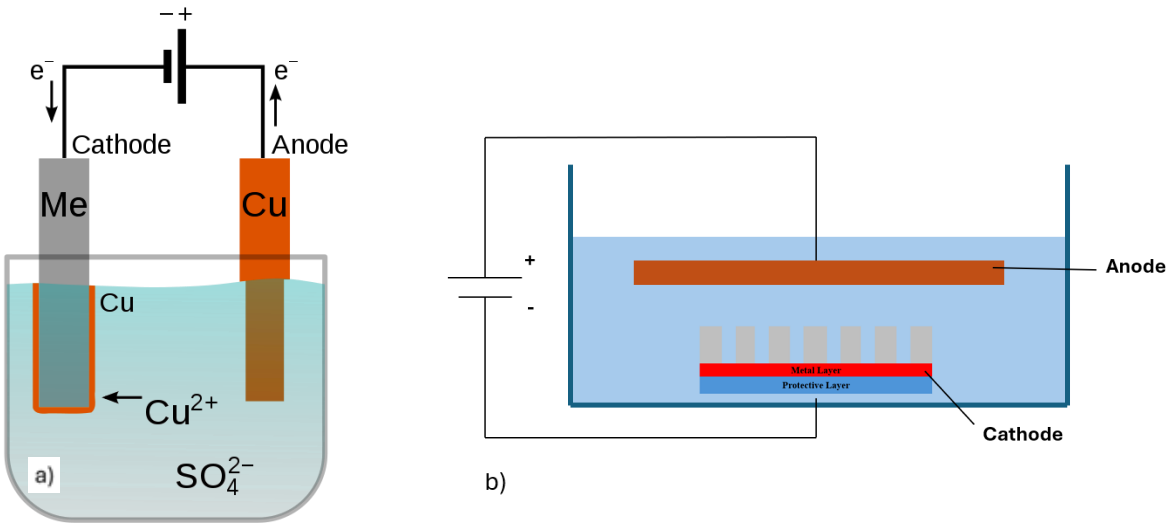

Figure 3 - Electroplating setup examples; a) electroplating working principle in typical setup [18]; b) Electroplating setup example for TSV fabrication

The basic deposition mechanism entails the flow of electrons from the anode to the cathode, making the anode release cations into the electroplating solution. The positively charged cations are attracted towards the cathode, where they are neutralized through reduction process, effectively depositing themselves and creating a metal layer [16]. This mechanism will be put in practice, by connecting a metal layer (also referred to as seed-layer) in the sample with the already drilled vias as the cathode. This allows for the bottom-up filling of the vias, since copper ions can deposit themselves on already deposited copper from the same Electroplating process, this is what creates the intended TSVs.

3

MATERIALS AND METHODS

In this chapter the materials and methods that were used at any stage on this project will be highlighted and specified. All the wafers used were p-type and had a (100) crystalline orientation, both 4 in (10.16 cm) and 3 in (7.62 cm) diameter wafers were processed. The two wafer thicknesses used were 300 μm and 380 μm.

3.1 Spin-coating of Photoresists and Polyimide layers

The photoresists and polyimide layers were deposited by spin-coating, using the Headway Spinner at the KU Leuven Nanocenter Clean Room. Different photoresists were used, namely s1818, for protective purposes and AZ125nxt, for masking purposes. Polyimide layers were also spin-coated to serve as protective layers, but these required a silane adhesion layer to be deposited first onto the wafer. The used recipes for each layer can be found in Table 1 below:

Table 1 - Spin-coating recipes

	s1818	**AZ125nxt***	**Silane adhesion layer**	**Polyimide**
Deposition Time/Rotation	1min at 3000rpm	20s at 3000rpm	1min at 2000rpm	45s at 5000rpm
Baking Time/Temperature	2min at 100˚C	15min at 125˚C	1min at 110˚C	1min at 90˚C Increase to 150 ˚C, leave 1min

*The AZ125nxt recipe optimization was performed during this work and explained in more detail in 4.2.1

3.2 Polyimide Hardbaking

To anneal the samples after the Polyimide deposition, a long 5h30min hard baking using the Despatch LCD Clean Process Benchtop Oven was required, the process followed the parameters below:

- Step 1 - Go to 200 ̊C with a 4.5 ̊C/min ramp
- Step 2 - Dwell for 30 minutes
- Step 3 - Go to 350 ̊C with a 2.5 ̊C/min ramp
- Step 4 - Dwell for 1 hour
- Step 5 - Ramp down to room temperature with a 2.5 ̊C/min ramp

3.3 Sputtering of metal layers

A thick layer of metal was required, so it could serve as the cathode in the Electroplating process. Different metals were used, namely aluminium and chromium, on the BALZERS BAE 370 coating system. In both cases, the chamber pressure value used was 3E-3 mbar, but the power had to be optimized to ensure a fixed deposition rate of 50 nm/min, for this, values of 100 W for chromium and 200 W for aluminum were defined. A layer with a thickness of 500 nm was desired in order to withstand some cycles of DRIE, so a 10 min deposition for both materials was employed. For every minute of deposition, the wafer underwent a subsequent 30 seconds of rest before moving on with the deposition, this is done to make sure that the wafer does not overheat from being directly above the target.

3.4 UV Mask Aligner and photoresist development

A couple of minutes after deposition, the negative photoresist AZ125nxt can be exposed using the EVG 620 Mask Aligner and a previously produced mask (Figure 4) with the vias pattern. Every square has 800 vias with 110 µm. The exposure variations used can be found in 4.2.1. The photoresist was later developed using the AZ 726 MIF developing solution, removing the photoresist in the needed areas. Rinsing the sample with running deionized water is essential to ensure that all the residues get removed.

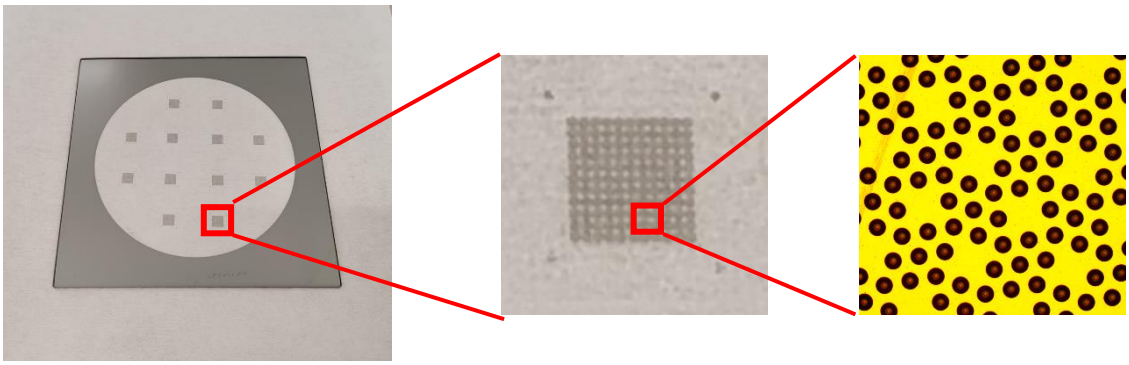

Figure 4 - Exposure Mask with vias pattern

3.5 Deep Reactive Ion Etching

The Oxford Plasma Deep Reactive Ion Etcher system was required to ensure the etching of vias throughout the wafer's thickness. Running a plasma-etching process using Oxygen (O_2), Sulfur Hexafluoride (SF_6) and Octafluorocyclobutane (C_4F_8) it was possible to etch the wafer only on the exposed silicon areas, while the rest was still being protected by the thick AZ125nxt photoresist layer. The previously explained process ensures that an anisotropic etching occurs, these processes are later revisited on 4.2, with detailed recipes used and necessary optimizations.

3.6 Reactive Ion Etching

Apart from the Si etching, the PT RIE Etcher was also used to etch samples that contained a protective layer of polyimide. After the silicon wafer is completely etched and the vias reach the Polyimide layer, it is needed to remove it in order to expose the metal layer that will work as the cathode in the Electroplating process up next. The parameters used can be seen in Table 2.

Table 2 – RIE process parameters to etch 3 µm polyimide

	Step 1	**Step 2**
O_2 (sccm)	20	20
SF_6 (sccm)	0	5
Time (min)	20	10
Power (W)	100	100

3.7 Electroplating

After drilling the vias, it is possible to fill them with copper, by connecting the wafer in an Electroplating bath. This bath is a mixture of Copper Sulfate and Sulfuric Acid (<20% w/w), the source is connected to the metal layer, through an area that was left exposed on the sample and serves as the cathode and a copper block, that serves as the anode. This circuit will release copper ions into the solution, allowing them to be deposited on the cathode. The setup used is shown in Figure 5.

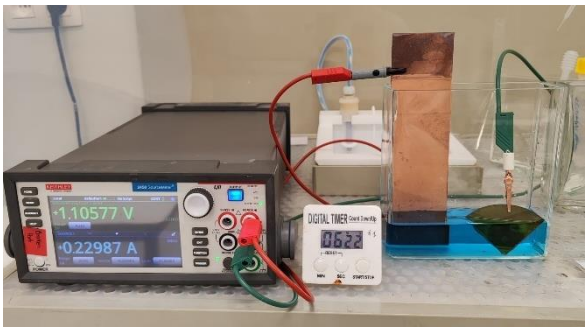

Figure 5 - Electroplating Setup

A current source was set and the circuit was turned on for 15 minutes, this amount of time that would allow for the necessary amount of copper to deposit on the metal layer and fill the vias from the bottom to top.

4

RESULTS AND DISCUSSION

This chapter presents the results and analysis of the various experimental procedures, processes, and tests conducted throughout the project, which informed the development of different design concepts for electro-plating samples. It also provides a detailed explanation of the rationale behind the discontinuation of certain designs, discussing the underlying reasons for their ineffectiveness or unsuitability.

4.1 Electroplating in Pre-drilled Wafers

One of the main questions during the beginning of this project was regarding the order in which certain steps of the procedure should be executed. Initially, the viability of drilling the vias as a first step was studied since there were pre-prepared samples for this purpose and it would remove the possibility of over-etching and damaging the layers below the Silicon.
Pre-drilled wafers with 380 µm of thickness, made by Laser Drilling, are illustrated in Figure 6, the laser made 25 vias with 200 µm of diameter each.

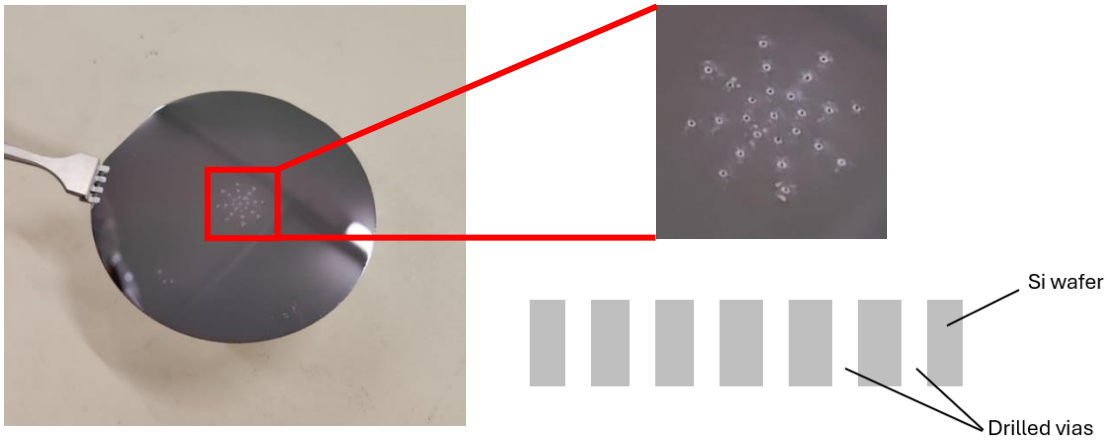

Figure 6 - Pre-drilled Wafer

In order to succeed in electroplating these vias, two approaches could be followed I) a single wafer process where a metal layer would be deposited on one of the sides of the wafer, covering the vias from one side, being able to work as the cathode of the process and as the seed-layer for the copper to grow on and II) a double wafer process where a metal coated wafer is bonded to the pre-drilled wafer, bypassing the challenge of covering the holes with deposition techniques.

I - Single Wafer Process

This process revealed itself very difficult to accomplish since the Electroplating process requires a metal layer covering the base of the vias. This could be performed either by sputtering a metal layer or by adding a photoresist layer as a flat plane (that could be removed at a later stage through an UV exposure) and only then deposit the metal layer via sputtering. However, due to the large diameter of the vias, both of these attempts were unsuccessful, since the deposited material would go inside the vias or even through them.
Some papers report that this method works for samples with 20 µm diameter vias, but already show some concerns for 30 µm[2], the huge 200 µm diameter of these vias made it very hard to coat a layer that would cover them from one side.

II - Double Wafer Process

For the double wafer process approach, instead of trying to cover the holes from one side using deposition techniques, this new process would now involve the bonding of two wafers, one with a coated metal layer and another with the pre-drilled vias, as depicted in Figure 7.

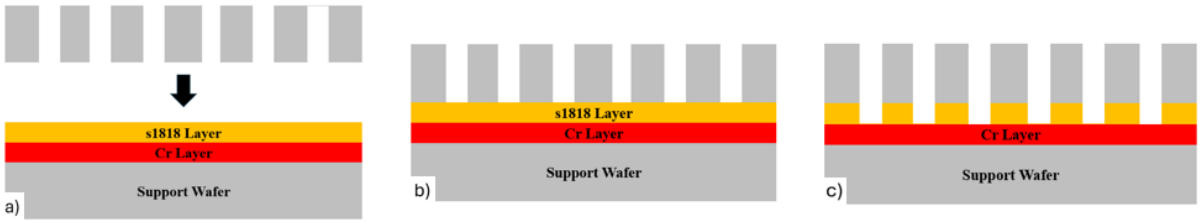

Figure 7 – Steps of the double wafer process: a) separated wafers; b) bonded wafers; c) bonded wafers after UV exposure

To achieve this configuration, firstly, a Chromium layer would be sputtered in the support wafer and then they were glued together. Two different methods were used for this step, using a Silicon paste, that served as glue and also by baking photoresist s1818 (recipe on 3.1), between the two wafers while having a small weight on top of the sample, applying constant pressure to stick them together. Both methods revealed a good mechanical adhesion, being hard to separate them, and were put through the electroplating process and had the same result.

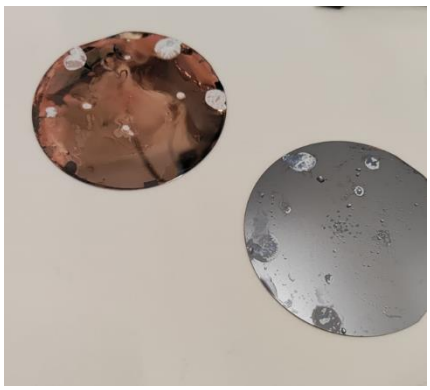

Figure 8 – Top wafer shows a copper layer, indicating copper deposition between the wafers

In the end, both of these methods failed due to the same reason: the electroplating solution was able to penetrate the area between both wafers and all the copper ions were attracted and deposited directly on the metal layer, as shown in Figure 8.

4.2 Drill vias after wafer processing

The result of these last tests marked a turning point in this project, the idea of drilling the holes as a first step was abandoned since, for the reasons explained above, both processes did not seem to work with the equipment at hand. In theory, for electroplating to work as intended, only three layers were needed: a drilled-through silicon wafer, a metal layer on the bottom to work as a cathode and seed-layer and finally, a protective layer that would cover the metal layer on the backside to prevent copper deposition on the backside. This theoretical design is pictured in Figure 9.

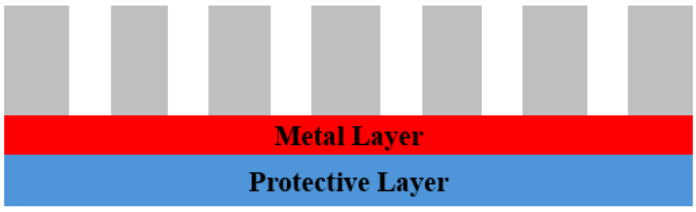

Figure 9 - Theoretical design for electroplating

Since coating the drilled wafer with the metal layer proved difficult, this new approach was based on coating the wafer with the metal first, patterning the other side with a thick photoresist and only then drill the vias using DRIE. The thick negative photoresist AZ125nxt was chosen for this, but its developer AZ 726 MIF also damaged both chromium and aluminum and that meant that the protective layer would need to be coated before developing the photoresist, which meant that all wafer processing had to be completed before the sample went into the DRIE for the via drilling.

Moving forward with this idea, wafers with 300 µm thickness were used and several different designs were experimented with, these will be further discussed and presented. There were already some pre-existing recipes in the Clean Room for the AZ125nxt spin-coating deposition and DRIE process, but while executing them, a need for a recipe optimization was created.

4.2.1 AZ125nxt Photoresist Recipe Optimization

The AZ125nxt photoresist previously used recipe by the group would make layers that would not withstand the needed cycles for the complete drilling of the wafer, being etched away before the end of the process. A final thickness of 25 µm was desired for this patterning layer. Different attempts were performed and, the trials and errors associated with the recipe optimization can be found in table 1, while the samples obtained after each recipe are also presented in Figure 10.

Table 3 - Photoresist recipes

	Recipe 1	Recipe 2	Recipe 3	Recipe 4
Spin-coating	20s at 2000	20s at 2500	20s at 3500	20s at 3000
Baking Tempera-ture/Time	15 min at 150˚C	15min at 125˚C	15min at 125˚C	15min at 125˚C
Exposure Dose	1200 mJ/cm^2	1200mJ/cm^2	1100mJ/cm^2	1000mJ/cm^2
Development	3min	3min	1min	1min
Result	>25µm, layer would not bake fully, temperature too high for the backside	>25µm, would be etched in DRIE at ~400 cycles	<25µm, would be etched in DRIE at ~350 cycles	~25µm, would withstand >480 DRIE cycles

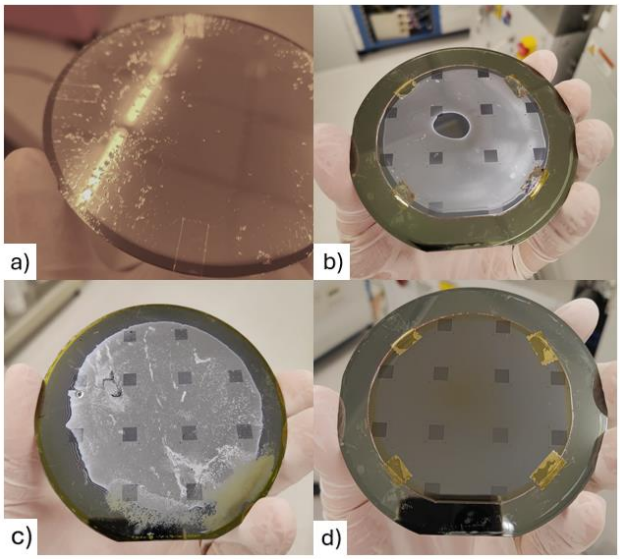

Figure 10 – a) Recipe 1, unbaked layer after contact with the mask aligner; b) Recipe 2, melted photoresist layer after 400 DRIE cycles; c) Recipe 3, melted photoresist layer after 350 DRIE cycles; d) Recipe 4, photoresist layer in good condition after 480 DRIE cycles

Even though the initial recipe surpassed the 25 µm thickness, the top part of the AZ125nxt layer would come out of the hotplate still not fully baked and the damage made to the backside (protective layer), that was in direct contact with the hotplate, would be not ideal. The temperature was then lowered to mitigate this efffect, as well as an increase in the rpm's to decrease the layer thickness, in order to fully bake it.

Also surpassing the 25μm mark, this recipe showed more promising results, but ultimately would still be fully etched at around 400 DRIE cycles. The development time was lowered, since in the three minutes the sample was immersed, some damage to the layer could arise, the rpm's were also increased to mitigate any possible under-baking problems and the exposure dose was lowered too, to prevent photoresist weakening due to the a possibly overexcessive exposure dose. Ultimately, this recipe would give layers that would be too thin and would be etched even sooner, at around 350 DRIE cycles. Lowering the rpm's to 3000 in Recipe 4 resulted in ~25μm layers that withstood DRIE processes surpassing the 480 DRIE cycles, the highest number of cycles ran on a single wafer.

4.2.2 DRIE Recipe Optimization

The DRIE recipe was set and it can be found below in Table 4, it could not be altered, the only possible variable that users could control was the number of cycles that a wafer would be put through.

Table 4 - DRIE recipe parameters

	Strike	**Deposition**	**Etch**
C_4F_8 (sccm)	10	68	3
O_2 (sccm)	50	0	30
SF_6 (sccm)	10	5	150
ICP (W)	1500	800	950
HF (W)	100	0	23
Time (s)	5	7	10

All the processes would be run at -1 ℃, with Helium cooling on the back of the wafer.

DRIE data from previous users that ran this recipe, reported that for drilling the 300μm, a value between 500-600 cycles were needed. After 480 cycles it was already possible to observe severe overetching, and this would not only damage the metal layer underneath, but also the s1818 protective one. The backside is supposed to isolate the metal completely so any damage to that layer is also extremely problematic. This led to a need for an optimization of the DRIE recipe too and using averaged data at specific points (100, 200, 300, 380 cycles) from 10 different processes, the real etch rate was able to be calculated by doing a linear regression on the graph in Figure 11, getting a value of 0.733 μm/cycle.

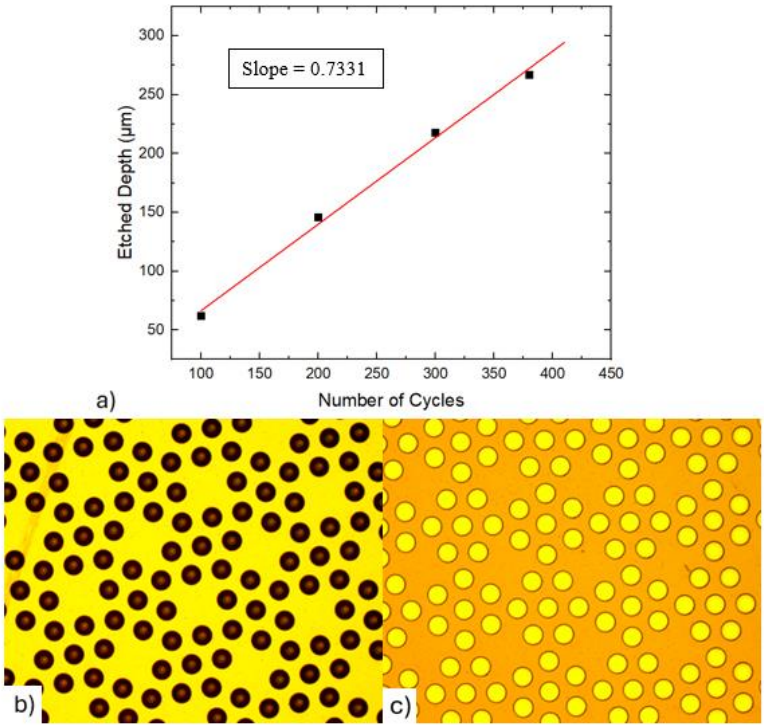

Figure 11 – a) Linear fit that led to the etch rate calculation b) unetched vias example, seen under microscope c) uncovered vias example, seen under miscroscope

According to this data, 409 cycles are needed to etch 300 µm of silicon, but this cannot be taken as set, since every wafer was under a +/- 15µm thickness tolerance. To avoid overecthing, after 390 cycles the sample would be taken out of the DRIE and checked under microscope, if the holes still presented a dark color it meant there was some silicon still left to etch in those areas, the sample would then undergo 5 more cycles and be checked again. This process would be repeated until the microscope image looked like the Figure 11 example c).

Edge and center vias comparison

The sample's vias can be separated in two different groups, vias that are closer to the center of the wafer and the ones that are closer to the edge. Since there is a spatial difference between these two, the etching could occur at different angles, potentially etching less vertically in the edge via area. This hypothesis was studied, by analyzing the cross-sections of an edge vias and a center vias side by side, this comparison can be made by looking at Figure 12. Looking at both images is possible to find a very minimal variation from the intended 90° etching in the edge vias, this was considered as negligible difference.

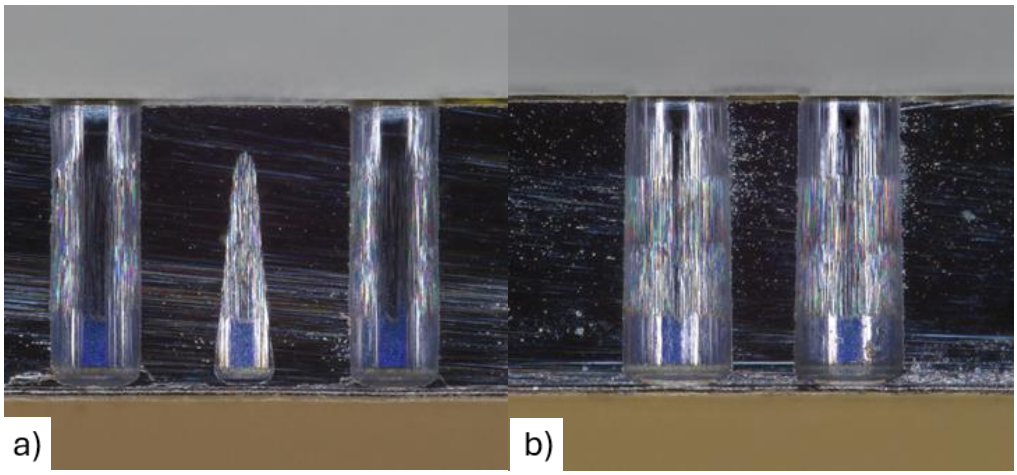

Figure 12 – Electronic microscope cross section images of drilled vias on a 300 μm substrate a) Center vias (via that is diced in the middle should be ignored); b) Edge Vias

As a conclusion, the DRIE recipe was optimized allowing the formation of vias in 300 μm thick wafers. However, the final samples should sustain the DRIE process while maintaining the integrity of the metal layer underneath to allow the subsequent electroplating process. As such, tests were performed on the selection of the metal that will work as a seed layer and protective layers.

4.2.3 Electroplating

The final process that needed to be tuned was the electroplating, how the samples would fit in the tank, how they would be connected and what current value to set the source to.

Sample Preparation

The requirements for the integration of the sample in the electroplating circuit can be boiled down to just two: leaving unprotected areas of metal exposed, that would serve as metal contacts for the crocodiles that connected the source to the cathode (metal layer) and anode (copper block) and dicing the wafer so that it could fit into the bath with the via areas immersed and the contact/crocodile area outside of the bath.
This dicing pictured on Figure 13 would be done by hand, using a scribing pencil. In regard to the contacts, a simple lift-off technique would be performed, putting a piece of polyimide tape in the desired areas for the contacts and then depositing the final protective layer.

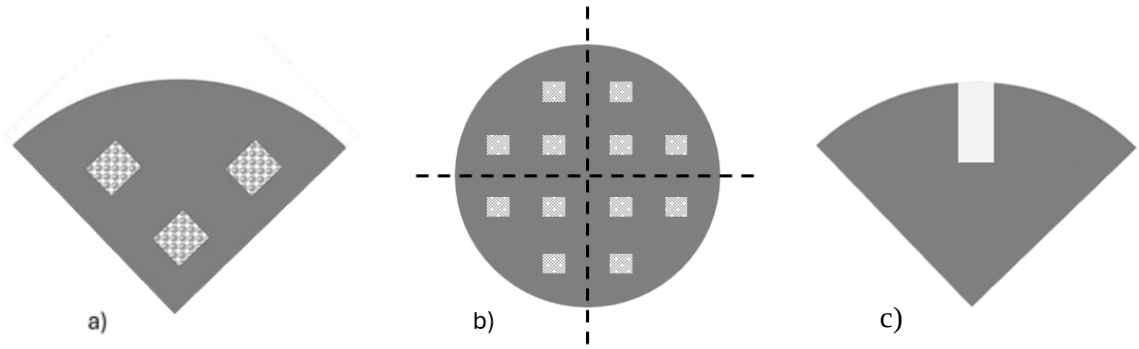

Figure 13 - Processed wafer examples; a) frontside of a 1/4 sample with the vias b) full wafer and dicing plans; c) backside of a 1/4 sample with the contact

Current Density Determination

This step consisted in the calculus of the applied fixed current on the electroplating process. In order to do this, all the vias were considered as cylinders with a 110 μm diameter and a 300 μm height and therefore, it is possible to calculate the volume of copper that would need to be deposited to fill the vias completely.
It is also known that on every "square" depicted in Figure 13, 800 vias are present, making it 2400 vias per quarter sample.

$$V = \pi r^2 h n_v = 6.84 \times 10^{-4}\, m^3$$

V – Total via volume
r – via radius
h – via height
n_v – number of vias

Knowing the Cu density (8960 Kg/m^3) and molar mass (63.55 g/mol) it is very simple to calculate the amount of copper that needed to be deposited, at 9.65E-4 mol. Due to the copper ion charge, for every deposited Cu^{2+} ion, twice as much electrons need to flow in the circuit, putting it at 1.93E-3 mol of electrons. With this value and assuming Faraday's constant as F = 96485 C/mol to calculate the charge that needs to flow in the circuit, it is possible to input a wanted duration for the process in the equation below and obtain the respective value of current needed to deposit the necessary amount of copper. The time set for each electroplating process was 15 minutes, that would require a current value of 0.21 A.

$$I = \frac{Q}{t} \Leftrightarrow I = \frac{F n_{e^-}}{t}$$

I – current
Q – charge
t – time
n_{e^-} – molar quantity of electrons
F – Faraday constant

Metal Layer Tests

What metal should be used, between Chromium and Aluminum, as a seed layer for the Electroplating process was also a big topic of interest during this thesis. Chromium was theoretically better since it takes longer than Aluminum to form an oxide layer, maintaining its conductive properties for longer, but due to limitations due to DRIE chamber contamination, chromium could only be used with an extra protective layer. Besides this, ion behavior on the electroplating solution was studied, a sample with exposed Silicon (wafer), chromium and aluminum was connected to the electroplating setup circuit and left there for 30 minutes. The results obtained can be seen in Figure 14.

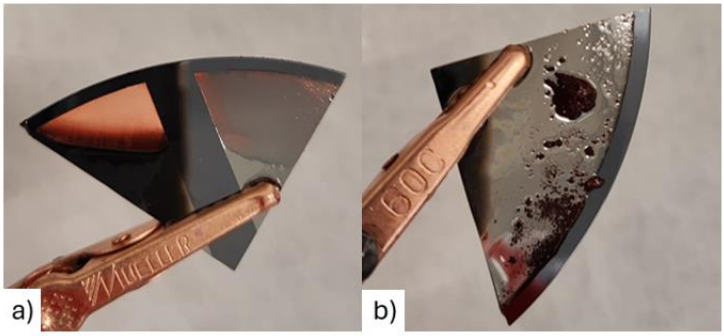

Figure 14 - a) Backside with Chromium after electroplating b) Frontside with Aluminum after electroplating

During this process, three very important things were able to be observed: Silicon does not attract any copper ions if aluminum or chromium are also connected, aluminum attracts copper ions at a much higher rate than chromium and copper ions have really good adhesion to the chromium layer compared to the aluminum layer, where most of the deposited copper fell off after removal from the setup. Prioritizing one material over the other is prioritizing ion attraction over adhesion or vice-versa. Attraction is very important since copper ions have to enter a small area inside the vias and even though adhesion does not matter as much here, since it is not a regular coating and the ions just need to deposit themselves on the vias, it might still be important for the final conductivity of the device. This being said, samples with both these materials were produced and processed.

4.2.4 Double S1818 Layer Chromium Sample

The initial reluctance to drill the holes as a last step of the wafer processing was due to the contamination chromium would bring to the DRIE chamber. The first design took that into account, with two s1818 photoresist layers, as shown in Figure 15.

Figure 15 – Double s1818 chromium sample expected evolution; a) expected design after wafer processing; b) expected result after DRIE; c) expected result after UV exposure

The photoresist layer between the metal and the wafer served as counter measure for the DRIE chamber contamination in the last cycles and could be removed later with some UV exposure through the holes. The other s1818 layer's only purpose was to isolate the metal layer from the Electroplating solution.
The problem associated with this design had to do with the photoresist layer between the metal and the wafer, that would either be too thin or it would crack, depending on the Sputtering setup used. The first setup had a lower distance from target to wafer, using a short arm to fix the sample holder, all the samples' photoresist would crack, due to the high temperature of the process (Figure 16 a), also damaging the metal layer that was

deposited. The second setup used a longer arm and would leave the metal layer too thin for the rest of the processing (Figure 16 b).

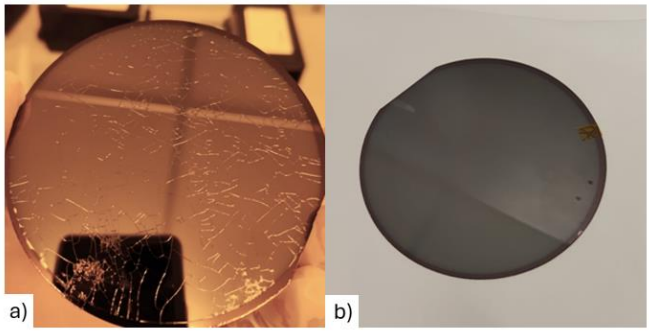

Figure 16 - a) Cracked photoresist and damaged metal layers; b) Thin metal layer

Since the middle photoresist layer was the problematic one, solutions that involved removing it completely from the design or a change in the layer material were implemented.

4.2.5 Single S1818 Layer Aluminum Sample

Even though Aluminum is more reactive than chromium, the Clean Room personnel reported less contamination on the DRIE main chamber with aluminum. With this in mind, a new design replacing Cr with Al, as shown in Figure 17 would allow for the middle photoresist layer to be removed.

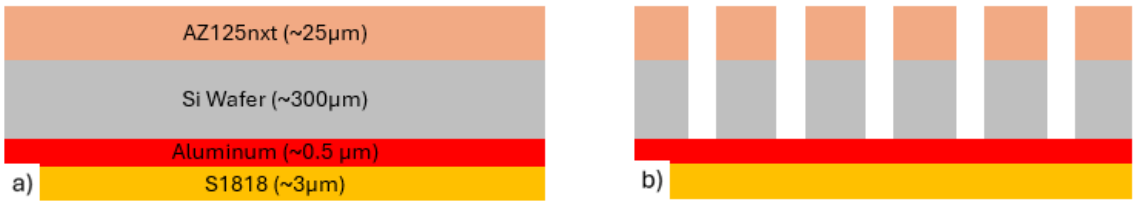

Figure 17 – Single s1818 layer aluminum sample expected evolution; a) expected design after wafer processing; b) expected result after DRIE

At this point, the photoresist recipe had been changed (4.2.1) but the DRIE process changes (4.2.2) were not. Since the expected number of cycles, for etching the full 300 µm wafer thickness, was still somewhere between 500-600 cycles, this was the wafer that was submitted to the 480 DRIE cycles, mentioned in that part of the document. This led to the overetching reported in that sub-section, as shown in Figure 18. The vias on the backside of the sample got as big as 170 µm in some cases, a 60 µm increase from the original diameter.
Since the sample was completely etched through all the layers, the electroplating solution could enter the vias from the backside, that is supposed to be isolated.

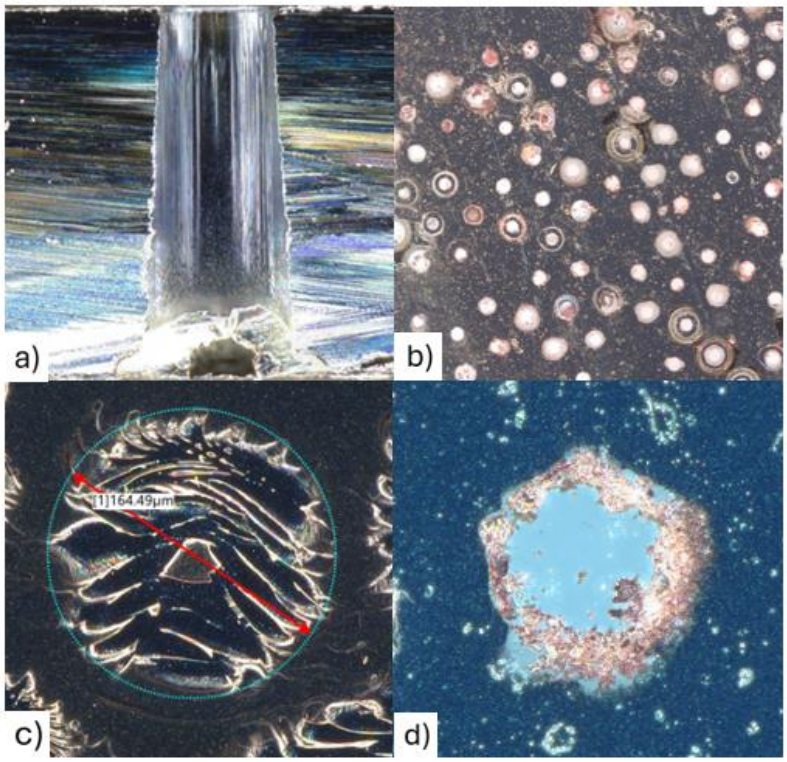

Figure 18 – Overetching visible on the sample. a) cross section view; b) backside view after electroplating; c) zoomed via before electroplating; d) zoomed via after electroplating

Even though these first electroplating tests revealed that the circuit and the setup worked, due to the metal layer damage and the copper ions being attracted into the vias from the backside, the copper filling did not occur as intended. In figure 18 b) it is possible to see the backside of the sample, that should be just an uniform layer of photoresist, but has massive holes and in figure 18 d), a close up of the via with some copper deposition. Both of these images were obtained after the electroplating process.

4.2.6 Single Polyimide Sample

Even if the DRIE etch rate on the metal layer cannot be tested, having an etch rate of 0.733 μm/cycle on Silicon and a 0.5 μm metal layer, it is better to not take any unnecessary risks and keep the protective layer, mentioned on 4.2.4, between the metal and the wafer as this would delay the overetching effect for at least some cycles. As reported in the same sub-section, s1818 does not work since it cracks easily with the metal deposition in the Sputtering, the solution for this problem was a material change to Polyimide. Following the recipe in 3.1 a 3μm protective layer is able to be obtained. This new sample design is shown in Figure 19.

Figure 19 – Single polyimide chromium sample expected evolution; a) expected design after wafer processing; b) expected result after DRIE; c) expected result after RIE

Using the extra Reactive Ion Etching method reported in 3.6, it was possible to remove the Polyimide layer after the DRIE process. It is extremely important to confirm that the layer is gone under microscope, looking for a visual change in the vias area, this change can be seen while comparing a) and b) on Figure 20. While analyzing the backside to confirm there was no damage this time around, some small dents could be seen under microscope, as shown in c). When the sample's backside was further analyzed in the optical profilometer, it was determined that the dents were only 1 µm deep and the cross-section view of the vias indicated that it even with the damaged backside, no extreme overetching (like reported in 4.2.5) occurred.

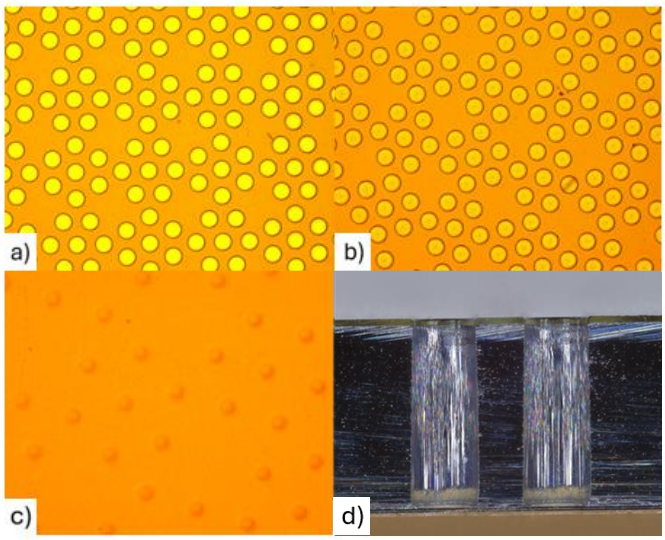

Figure 20 - a) topside view, before RIE; b) topside view after RIE; c) backside view after RIE; d) Cross-section of the vias

Most of the electroplating that was taking place in the backside of the sample was mitigated, but a new challenge came up: after breaking the sample for the electroplating process some metal was left exposed on the edges of the wafer. This led to electroplating in these areas, as illustrated in Figure 21, instead of the vias and after copper starts depositing it automatically becomes part of the circuit and this means that more copper ions can deposit on previously deposited ones, rendering this sample as a failed attempt too.

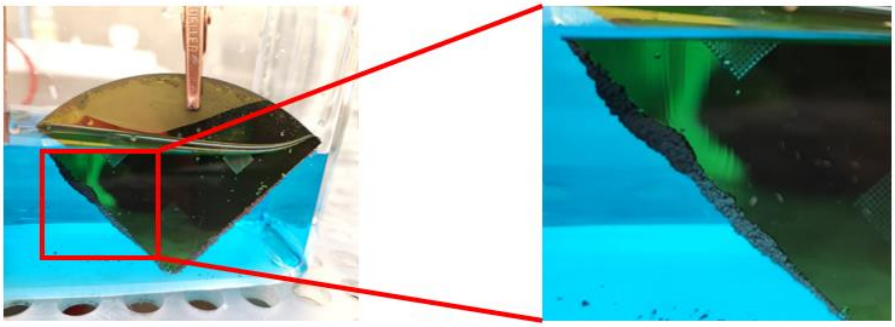

Figure 21 - Copper depositing on wafer's edges

4.2.7 Double Polyimide Samples

The final goal was to isolate the backside and the exposed sides completely, so that the copper ions would be deposited on the vias. Until now, the minimal damage to that final protective layer due to the hot plate baking in 3.1, was deemed as acceptable, but any residual electroplating on the backside affected the whole process, as it was just understood. In order to eliminate this, a material that is very resistant to high temperatures would need to replace s1818 and since polyimide was already in use and fitted into this description that is how these final samples were designed. Also, because the question about the choice for the metal layer raised on 4.2.3 remained largely unanswered, two samples, one with chromium and another one with aluminum, were produced and processed. Both designs are shown in Figure 22.

Figure 22 – Double polyimide chromium and aluminum samples expected evolution; a) expected design after wafer processing; b) expected result after DRIE; c) expected result after RIE

Even though some small changes had to be made to some steps of the process (e.g. how the metal contacts for the electroplating circuit were made) and another 5h30min oven cycle had to be added for the second polyimide layer, good results were obtained for the backside. The sample was also analyzed in the profilometer and no damage or dents could be seen, indicating a smooth and uniform protective layer, just as intended. With this, the backside was finally isolated so that no copper ions could deposit themselves on it, leaving only the edges to be dealt with. Using polyimide tape, these exposed areas were able to be covered, this can be seen in Figure 23, as well as the difference between the old s1818 backside and this new polyimide backside.

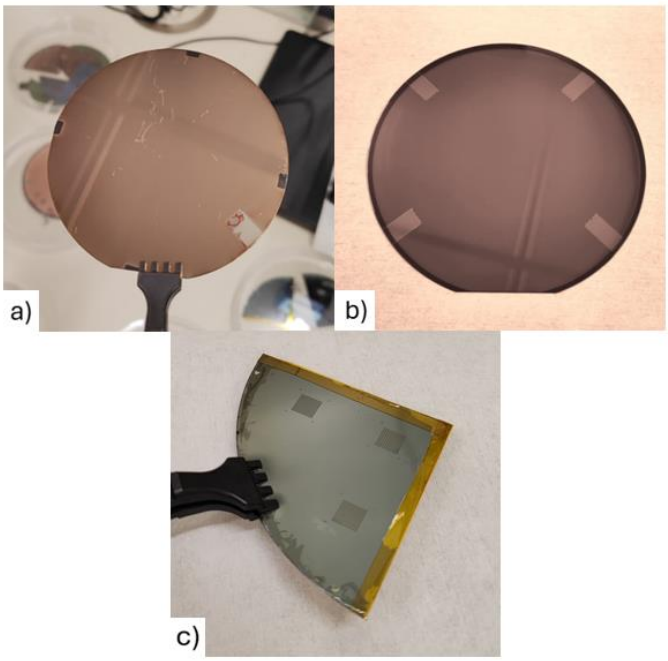

Figure 23 - a) old s1818 backside with some damage; b) new polyimide back-side; c) sealed edges

As a safety measure, a voltage limit way above the regular process values was set on the source, in case the resistance of the circuit got too high. During these last electroplating tests, this limit was always reached, which guarantees that the isolation of the backside and edges worked perfectly. Unfortunately, these results also revealed that even with the intended sample processing results, no connection could be established to the electroplating circuit, making it incomplete and therefore not allow for copper deposition to occur.

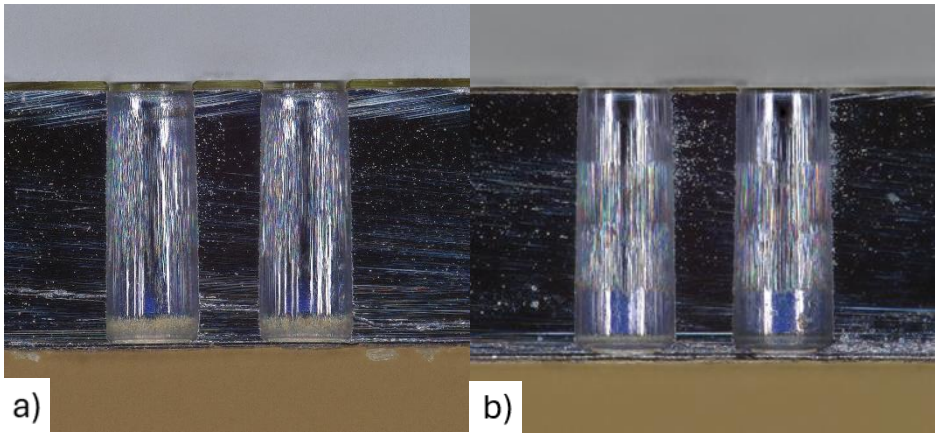

Figure 24 - Cross-section view of both samples; a) Chromium sample; b) Aluminum sample

In the end, an easy to replicate, low-cost process that could etch the vias was reached, concluding one of the major goals of this project. The final results of this project can be inspected by looking at Figure 24, where both the Cr and the Al sample show good vertical etching, without any overetching or underetching signs. But there are still some tests and studying to do, before this methodology is ready to be used in TSV fabrication, namely on the electroplating part of the process.

5

CONCLUSIONS AND FUTURE PERSPECTIVES

5.1 Conclusions

After the last set of results, it was finally concluded that even though the wafer processing objectives were hit, there was still some issue that would not allow copper deposition to occur in the vias. All the areas of the sample were properly isolated, getting samples with undamaged backsides and ultimately cutting all copper deposition on unwanted areas. Good results were also obtained on the via drilling, with practically vertical etching and a process that allowed to reduce significantly any underetching and overetching effects. Most of the results obtained in similar papers drill the vias before any wafer processing, but as explained previously that is very hard to achieve for via diameters bigger than 30 μm, since it is very hard to cover the pre-existing vias with an even layer of metal that needs to be present during the electroplating process to work as a cathode and a seed-layer for the copper to grow on.

Throughout this project it was possible to optimize the DRIE recipe to allow the full etch of 300 μm thick wafers, that included the optimization of the AZ125nxt photoresist recipe, with vias of 110 μm diameter. It was also possible to study the effect of using single or double layer protective metal films of either polyimide or s1818 resists, while verifying that both Cr or Al could be used as a seed layer on the Cu eletroplating and the optimized configuration consisted on using polymide in the two protective layers present in the device.

After all the tests and process optimizations were completed, the last tests failed to establish a circuit connection, that means that the solution was not able to reach the metal from inside the vias and that can be attributed to some different reasons: i) the density of vias per area could be too large, where it was possible to detect a selective electroplating on vias that were on the edge of each via squared region; ii) both Al and Cr, when left exposed, create a thin oxide layer that could be hindering the connection between the solution and the metal layer, but this explanation is considered unlikely, given that on every other sample tests where there was exposed metal, either on the backside or on the edges, copper deposition would occur; and iii) there was no way to calculate the etch rate of both of the metals used for seed-layers on the DRIE tool and this would imply a critically damaged metal surface. To address these possible reasons given for the lack of copper deposition, more tests that were not possible to be performed within the schedule of the program, but if the third explanation is the correct one, it makes the approach of drilling the vias after wafer processing non-viable.

5.2 Future Perspectives

Most of the limitations that transformed this into a complex project had to do with the lack of a mask that would be able to drill vias with a reduced diameter. If there is that possibility, the vias can be drilled as a first step and it is relatively easy to cover them with an even metal layer that would work as seed-layer, allowing the copper to grow from there since no damage exists on the metal.

In the case that this approach of drilling the vias as a last step is revisited there are some possible ways to move forward that could help with the lack of deposition problems described. One of them would be to put the metal layer through a surface treatment that would mitigate the oxide formation, such as the zincate process in the case of aluminum or acid etching in the case of chromium. A mask that would allow for the vias to be less concentrated, could also be a way forward when trying to achieve better results. A potentially effective way to confirm if the problem is indeed the metal layer being damaged by the DRIE would be by studying the question raised in the “Metal Layer Tests” section of 4.2.3 and to assess the etch-rate of each metal on a system where chamber contamination is not a concern. This project would also be facilitated by the possibility of running a thinning process on the wafers, making both the drilling of the vias and theur subsequent metal filling easier.

This work shows that, without the right tools, the possibility of fabricating TSVs in Si wafers is a very challenging task, nevertheless, meaningful improvements and results were achieved on wafer processing for this technology.

BIBLIOGRAPHY

[1] B. Jiao *et al.*, "Low Stress TSV Arrays for High-Density Interconnection," *Engineering*, Apr. 2024, doi: 10.1016/j.eng.2023.11.023.

[2] N. T. Nguyen, E. Boellaard, N. P. Pham, V. G. Kutchoukov, G. Craciun, and P. M. Sarro, "Through-wafer copper electroplating for three-dimensional interconnects INSTITUTE OF PHYSICS PUBLISHING JOURNAL OF MICROMECHANICS AND MICROENGINEERING Through-wafer copper electroplating for three-dimensional interconnects," 2002. [Online]. Available: http://iopscience.iop.org/0960-1317/12/4/308

[3] A. Lancaster and M. Keswani, "Integrated circuit packaging review with an emphasis on 3D packaging," Jan. 01, 2018, *Elsevier B.V.* doi: 10.1016/j.vlsi.2017.09.008.

[4] M. Schuettler and T. Stieglitz, "Microassembly and micropackaging of implantable systems," in *Implantable Sensor Systems for Medical Applications*, Elsevier Ltd., 2013, pp. 108–149. doi: 10.1533/9780857096289.1.108.

[5] J. J. Licari and D. W. Swanson, "Introduction," *Adhesives Technology for Electronic Applications*, pp. 1–37, Jan. 2005, doi: 10.1016/B978-081551513-5.50003-6.

[6] M. F. Lai, S. W. Li, J. Y. Shih, and K. N. Chen, "Wafer-level three-dimensional integrated circuits (3D IC): Schemes and key technologies," Nov. 2011. doi: 10.1016/j.mee.2011.05.036.

[7] J. P. Gambino, S. A. Adderly, and J. U. Knickerbocker, "An overview of through-silicon-via technology and manufacturing challenges," Mar. 05, 2015, *Elsevier*. doi: 10.1016/j.mee.2014.10.019.

[8] H. Guo, S. Cao, L. Li, and X. Zhang, "A review on the mainstream through-silicon via etching methods," *Mater Sci Semicond Process*, vol. 137, p. 106182, Jan. 2022, doi: 10.1016/J.MSSP.2021.106182.

[9] "Handbook of Silicon Based MEMS Materials and Technologies," 2015, doi: 10.1016/C2013-0-19270-7.

[10] R. Dorey, "Ceramic Thick Films for MEMS and Microdevices," *Ceramic Thick Films for MEMS and Microdevices*, pp. 1–191, Jan. 2011, doi: 10.1016/C2009-0-20338-2.

[11] A. M. F. R. Pinto, V. B. Oliveira, and D. S. Falcão, "Direct alcohol fuel cells for portable applications: Fundamentals, engineering and advances," *Direct Alcohol Fuel Cells for Portable Applications: Fundamentals, Engineering and Advances*, pp. 1–341, Jan. 2018, doi: 10.1016/C2016-0-00632-0.

[12] Z. Zalevsky and I. Abdulhalim, *Integrated nanophotonic devices: Second edition*. Elsevier, 2014. Accessed: Oct. 15, 2024. [Online]. Available: http://www.sciencedirect.com:5070/book/9780323228626/integrated-nanophotonic-devices

[13] S. Ma *et al.*, “Research progress on additives and mechanism of copper electroplating for TSV,” *SCIENTIA SINICA Chimica*, vol. 53, no. 10, pp. 1891–1905, Sep. 2023, doi: 10.1360/SSC-2023-0167.

[14] J. X. J. Zhang and K. Hoshino, “Molecular Sensors and Nanodevices: Principles, Designs and Applications in Biomedical Engineering, Second Edition,” *Molecular Sensors and Nanodevices: Principles, Designs and Applications in Biomedical Engineering, Second Edition*, pp. 1–581, Jan. 2018, doi: 10.1016/C2017-0-02290-5.

[15] Q. Zhao, H. Yu, S. Wang, W. Wang, and Z. Liang, “Microbial Fuel Cells—Air-Cathode Electrodes A2 - Wandelt, Klaus BT - Encyclopedia of Interfacial Chemistry,” pp. 319–327, 2018, Accessed: Oct. 15, 2024. [Online]. Available: http://www.sciencedirect.com:5070/referencework/9780128098943/encyclopedia-of-interfacial-chemistry

[16] A. A. Ojo and I. M. Dharmadasa, “Electroplating of Semiconductor Materials for Applications in Large Area Electronics: A Review,” *Coatings 2018, Vol. 8, Page 262*, vol. 8, no. 8, p. 262, Jul. 2018, doi: 10.3390/COATINGS8080262.

[17] D. H. Cho, S. M. Seo, J. B. Kim, S. H. Rajendran, and J. P. Jung, “A review on the fabrication and reliability of three-dimensional integration technologies for microelectronic packaging: Through-si-via and solder bumping process,” *Metals (Basel)*, vol. 11, no. 10, Oct. 2021, doi: 10.3390/MET11101664.

[18] “Electroplating Explained - How It Works, Types, Benefits & More | Fractory.” Accessed: Oct. 15, 2024. [Online]. Available: https://fractory.com/electroplating-explained/