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Modular nine-level single-phase inverter with quadruple voltage gain using reduced blocking voltage switches

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ABSTRACT

This paper presents a novel approach to enhancing modular voltage source inverters, focusing on achieving high-voltage gain and minimizing harmonic distortion. The suggested solution includes a transformerless, single-phase, nine-level voltage source inverter that cuts down on the number of passive parts that are needed while still achieving a high-voltage gain of up to four times the input DC voltage sources. An essential feature of this topology is that all the switches are subjected to a maximum blocking voltage four times lower than the maximum AC voltage that can be applied to the load. Consequently, this leads to a significant reduction in the Total Voltage Blocking, standardization of the power semiconductors, and converter modularity structure. Furthermore, the proposed inverter topology presents voltage self-balancing capability, eliminating any balancing issues for the two floating capacitors of each voltage source inverter. The theoretical assumptions put forward in this study will be tested through experimental results obtained from a laboratory prototype.

1. Introduction

While two-level voltage source inverters (VSIs) provide advantages in control simplicity and cost over comparable topologies, they have significant limitations, including limited output voltage levels and high total harmonic distortion (THD). Their use also necessitates high-power switches and often requires output filtering to mitigate poor power quality. In order to mitigate these limitations, various multilevel inverter (*MLI*) topologies have been considered for implementation in contemporary applications, encompassing electric vehicles (*EVs*) [1], more electric aircraft [2], renewable energy conversion systems [3], railway systems [4], and medium- or high-voltage direct current (*HVDC*) systems [5]. The utilization of *MLIs* enables the circumvention of the majority of limitations inherent in two-level inverters. *MLIs* enhance power quality through the generation of staircase-like output voltage waveforms characterized by reduced total harmonic distortion (*THD*). Depending on the requisite quality of the *AC* output voltages, *MLIs* possess the capability to obviate the need for output filters. Moreover, the distribution of voltage stress among the switches in *MLIs* results in a reduction of voltage step stresses (dv/dt) imposed on the semiconductor switches, thereby yielding a concomitant decrease in electromagnetic interference (*EMI*). Operation at reduced switching frequencies is also feasible, leading to enhanced power efficiency, particularly when semiconductor switch conduction losses are minimized. Certain *MLI* topologies exhibit modular architectures, which afford the advantage of increased voltage and current handling capabilities. One example of such a topology is the modular multilevel converter (MMC), which is designed for high-power, medium-voltage, and high-voltage energy conversion systems [6,7]. The basic concept of the modular multilevel converter is based on a modular arm structure. It utilizes classical two-level voltage source inverter arm structures, with each arm having the same voltage blocking capability. Surveys of other multilevel topologies based on classical two-level voltage source inverter arm structures can also be found in [8,9]. The cascaded H-bridge (CHB) [10,

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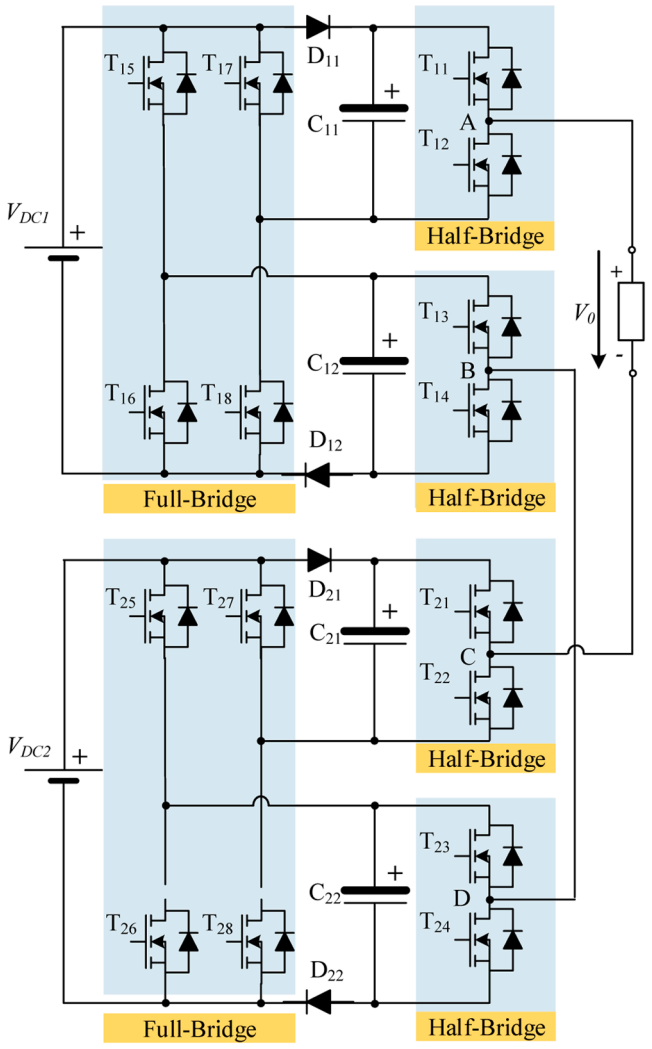

Fig. 1. Circuit topology of the proposed Boost nine-level voltage source inverter (FB2HB9 L).

11], neutral point clamped (NPC) [12], and flying capacitor (FC) [13] topologies are among the most popular multilevel converter architectures used in industrial and renewable energy applications. Other hybrid or mixed topologies have been developed over the last few years. For example, a hybrid topology that consists of an active-neutral-point converter (ANPC) stage and an H-bridge converter stage can be found in [14]. A hybrid structure utilizing a classical single-phase and three-phase two-level voltage source inverter was proposed in [15]. Another hybrid structure, integrating flying capacitor and switched-capacitor cells, was presented in [16]. Additionally, a hybrid structure incorporating T-Type and flying capacitor multilevel cells was also proposed in [17]. A review of some key mixed multilevel topologies can be found in [18,19]. However, these topologies often require a significant number of components (power devices, diodes, and capacitors), which increases with the number of voltage levels, and they typically do not provide voltage boost capability. In general, the cost of *MLIs* is directly influenced by the component count, boost capability, and the total blocking voltage (*TBV*) that the semiconductor switches must withstand [20]. Multilevel solutions with many voltage levels but relatively few power semiconductors have been proposed [21,22]. However, these solutions often require a significant number of magnetic components.

The study and development of multilevel inverters (MLIs) with higher voltage levels, lower total harmonic distortion (THD), reduced voltage stress on power switches, smaller filters, and a decreased component count have been ongoing over the past few years. Several MLIs with fewer devices and other significant features are reviewed and compared in references [20] and [23,24]. Next, some relevant topologies proposed in the literature with nine or more voltage levels are reviewed. References [25] propose a nine-level boosted multilevel inverter (MLI) topology capable of achieving double voltage gain. This solution requires ten switches, one diode, two capacitors, and a single DC source. A topology with slightly fewer switches (nine) but the same boost capability was presented in [26]. However, it requires an additional diode. Reference [27] presented a topology with the same number of switches and boost capability but requiring more capacitors. Reference [28] presented a topology with quadruple boost capability. However, this requires a significantly higher component count (switches, diodes, and capacitors). Reference [29] proposed another topology with the same boost capability but a reduced component count, requiring ten switches, one diode, and two capacitors. Reference [30] proposes another quadruple-boost topology with a further reduced switch count of eight. However, it requires three diodes and three capacitors. Reference [31] also presented a quadruple-boost topology but requires more switches (fourteen), although it eliminates the need for diodes and reduces the capacitor count to two. A nine-level topology without diodes was proposed in [32]. However, this design does not provide boost capability. In [33], a reduced component count asymmetric Envelope Type (E-Type) module is proposed. This solution requires four DC sources, ten switches, thirteen levels, and an output voltage that can be up to five times the input voltage of the DC sources. This answer utilizes a sophisticated modulation technique with selective harmonic elimination. Proposal [34] presents an expanded version of the prior solution that achieves output voltages of up to six times the input DC source. It requires two DC sources, two capacitors, and 14 switches to achieve thirteen levels. A thirteen-level SCMLI structure is also proposed in [35], which has self-balancing and six times boost capability. This topology requires a single DC source, thirteen switches, two diodes, and three capacitors. The modulation strategy is based on a fundamental frequency PWM control (FFC) technique combined with a high switching frequency PWM control (HFC) strategy. A topology with similar characteristics was also proposed in [36]. A nine-level modified Pack U-Cell (MPUC) inverter with double voltage gain for photovoltaic applications is presented in [37]. Despite requiring fewer components, it still needs two input DC sources and some filtering components. Another nine-level combined PUC and NPC topology is presented in [38], which uses eight switches, four capacitors, and a single DC source. This last topology is able to achieve capacitor self-voltage balance but is unable to provide any voltage gain relative to the input DC source. A new nine-level Packed E-Cell (PEC) structure is presented in [39]. The proposed solution is a modification of the PUC topology, where two U-Cells are replaced by one E-Cell. It requires one DC source, two capacitors, and eight switches. However, this topology presents a unity voltage gain. The modulation is based on a half-parabola carrier designed to provide active capacitor voltage balancing. In [40], another interesting topology is introduced that is based on a modular configuration using full-bridge voltage source inverters (VSI). However, it only allows for seven voltage levels and a triple voltage gain. Additionally, the switches require different blocking voltage capabilities, and half of them must support the maximum level of the output AC voltage. Thus, some switches with high voltage stress are required. From the analysis of these topologies, it is possible to see that the characteristic that defines those with a lower switch count and boost capability is their requirement for switches that can handle different voltage stresses. On the other hand, they also require switches that must support blocking voltages equal to or at least half of the maximum AC voltage level.

This paper proposes a single-phase nine-level inverter topology with a reduced number of components and high boost capability. In addition to the reduced component count, the proposed solution also features a modular structure that utilizes only single-phase full-bridge and half-

Table 1
Switching states to achieve nine-level.

Voltage Level	Switches On	C_{11}	C_{12}	C_{21}	C_{22}
$+4V_{DC}$	T_{11}, T_{14}, T_{16}, T_{17}, T_{22}, T_{23}, T_{25}, T_{28}	↓	↓	–	–
$+3V_{DC}$	T_{11}, T_{14}, T_{16}, T_{17}, T_{22}, T_{23}, T_{25}, T_{27}	↓	↓	–	–
$+2V_{DC}$	T_{11}, T_{14}, T_{15}, T_{17}, T_{22}, T_{23}, T_{25}, T_{27}	↓	↑	–	–
$+V_{DC}$	T_{11}, T_{14}, T_{15}, T_{18}, T_{22}, T_{23}, T_{25}, T_{27}	↑	↑	–	–
0	T_{11}, T_{14}, T_{15}, T_{18}, T_{21}, T_{24}, T_{25}, T_{28}	↑	↑	↑	↑
$-V_{DC}$	T_{12}, T_{13}, T_{15}, T_{17}, T_{21}, T_{24}, T_{25}, T_{28}	–	–	↓	↓
$-2V_{DC}$	T_{12}, T_{13}, T_{15}, T_{17}, T_{21}, T_{24}, T_{25}, T_{27}	–	–	↑	↓
$-3V_{DC}$	T_{12}, T_{13}, T_{15}, T_{17}, T_{21}, T_{24}, T_{26}, T_{27}	–	–	↑	↑
$-4V_{DC}$	T_{12}, T_{13}, T_{15}, T_{18}, T_{21}, T_{24}, T_{26}, T_{27}	–	–	↑	↑

↑ capacitor under charge ↓ capacitor under discharge.

bridge voltage source inverters (VSIs). Another important characteristic that is not typical in inverters with a reduced number of components is that the switches support identical blocking voltages. Moreover, the blocking voltage supported by these switches is four times less than the peak AC voltage. These two characteristics were key considerations in the development of the topology: equal voltage stress across all switches and very low voltage stress relative to the maximum output AC voltage. Finally, another advantage that can be mentioned is its high voltage gain. The topology employs two equal DC sources, sixteen switches, four diodes, and four capacitors. The maximum output AC peak voltage achieved is four times greater than the voltage of the DC sources, while the maximum blocking voltage of all the switches is four times less than the peak AC voltage. The ability to use the well-known multilevel phase opposition disposition multicarrier pulse width modulation (POD-MCPWM) is another advantage. Additionally, the proposed topology enables self-balancing voltage through the converter's intrinsic operation.

2. Proposed nine-level boost inverter

2.1. Topology configuration

The topology of the proposed Full-Bridge-Two-Half-Bridge Nine-level boost voltage source inverter (*FB2HB9 L*) is presented in Fig. 1. This topology is characterized by two *DC* voltage sources V_{DC1} and V_{DC2} ($V_{DC1} \approx V_{DC2} \approx V_{DC}$) four capacitors and sixteen unidirectional voltage switches. The topology was also developed in a modular way since eight unidirectional voltage switches can be assembled from two single-phase full-bridges and the remaining eight unidirectional voltage switches can be assembled from four single-phase half-bridges. In this context, the

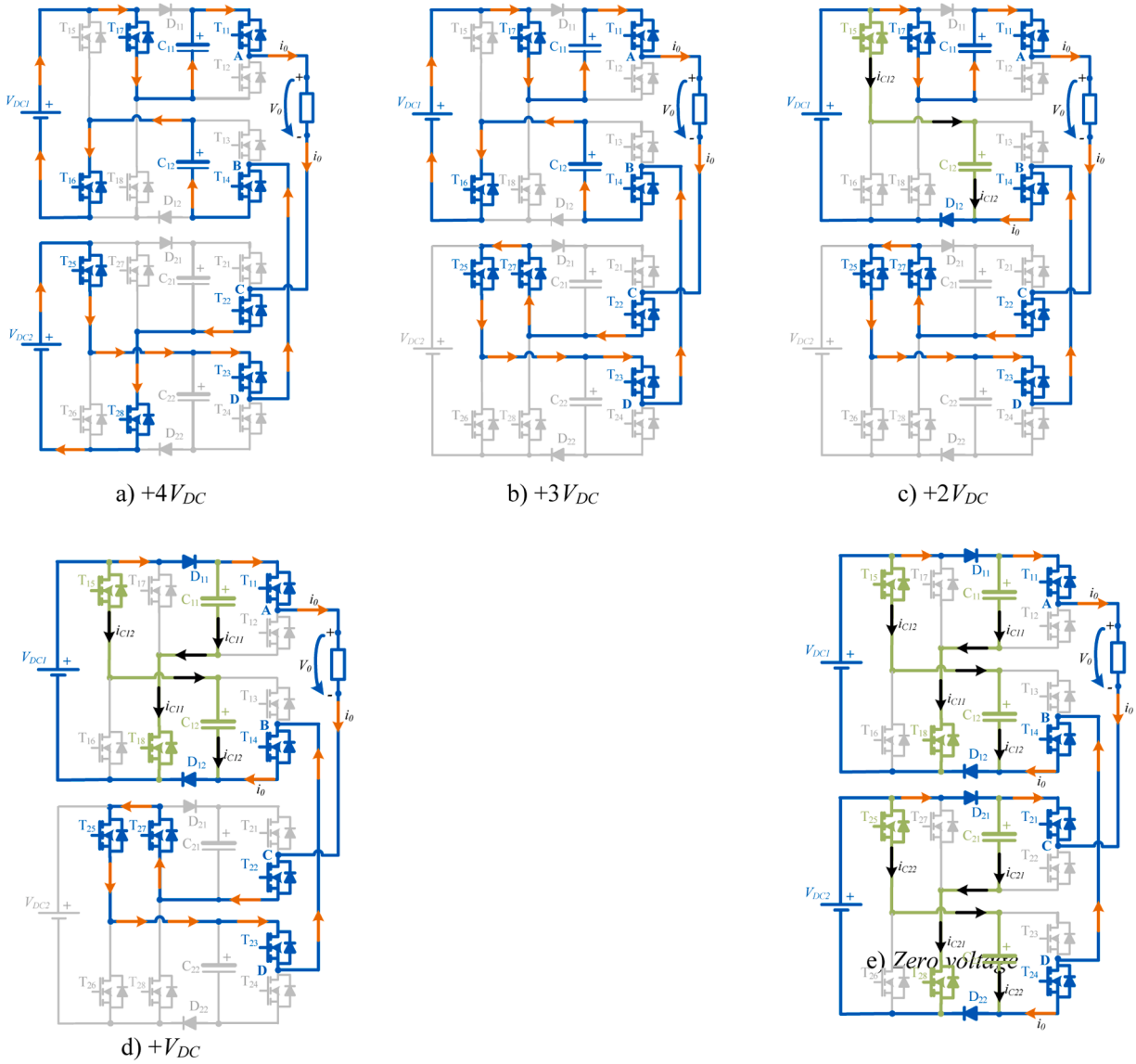

Fig. 2. Operation modes associated to each positive voltage levels associated to the proposed converter.

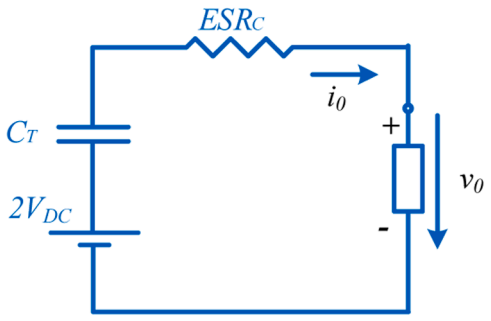

Fig. 3. Equivalent circuit for maximum output voltage $+4V_{DC}$.

mentioned modularity refers to the fact that the proposed topology was developed using classical two-level arm structures, where all the arms exhibit the same voltage blocking capability. Assuming that all components are ideal and that the circuit is operating in steady state operation at continuous conduction mode (*CCM*) each capacitor voltage equals the *DC* voltage value V_{DC}. Given all the possible switch combinations (Table 1) the maximum output *voltage V0* can attain four times the V_{DC} value. Table 1 shows the nine *AC* output voltages levels $+4V_{DC}$, $+3VDC$, $+2V_{DC}$, $+V_{DC}$, 0, $1V_{DC}$, $-2V_{DC}$, $-3V_{DC}$ and $-4V_{DC}$.

2.2. AC output voltage levels generation

The operation modes of the proposed converter leading to each positive voltage level that can be applied to the load are shown in Fig. 1.

The maximum positive voltage level ($+4V_{DC}$) is achieved by turning *ON* switches T_{11}, T_{14}, T_{16}, T_{17}, T_{22}, T_{23}, T_{25} and T_{28}, being the voltage applied to the load equal to the series connection of both *DC* voltage source V_{DC1} and *VDC2* and two capacitors (C_{11} and C_{12} as described in Fig. 2(a)). To obtain the voltage level $+3V_{DC}$, the switches T_{11}, T_{14}, T_{16}, T_{17}, T_{22}, T_{23}, T_{25} and T_{27} must be in turned *ON* (see Fig. 2(b)). In this condition the capacitor C_{11} is connected in series with both *DC* voltage source to supply the load and the capacitor C_{12} is charged by the upper *DC* voltage source. The third voltage level ($+2V_{DC}$) is achieved by turning *ON* switches T_{11}, T_{14}, T_{15}, T_{17}, T_{22}, T_{23}, T_{25} and T_{27} (see Fig. 2 (c)) In this mode the load is supplied by the series of both *DC* voltage sources and both capacitors C_{11} and C_{12} are simultaneously charged. To obtain the voltage level $+V_{DC}$, the switches T_{11}, T_{14}, T_{15}, T_{18}, T_{22}, T_{23}, T_{25} and T_{27} must be in turned *ON* (see Fig. 2(d)).

In the $+V_{DC}$ mode the load is only supplied by the upper *DC* voltage sources and both capacitors C_{11} and C_{12} are simultaneously charged. The zero voltage level is ensured by the turned *ON* (see Fig. 2(f)) of T_{12}, T_{13}, T_{15}, T_{18}, T_{21}, T_{23}, T_{25} and T_{28}. In the zero mode none of the capacitors are charged. The negative voltage levels can be obtained in a similar way, as presented in Table 1.

2.3. Self-voltage balance of the capacitors

The proposed solution to self-balance the voltage of the capacitors is equivalent to the series–parallel technique used to achieve self-voltage balance of capacitors as described in [41]. According with the example of Fig. 2(d) and (e) the capacitors C_{11} and C_{12} are in parallel with the dc source V_{DC1} and charged to the voltage Vdc when the switches T_{15} and T_{18} are turned on during the $+V_{DC}$ and zero voltage level. In this condition both diodes D_{11} and D_{12} are also turned on. Conversely, the recharged capacitors C_{11} and C_{12} are in series connection with dc source V_{DC1} when the switches T_{16} and T_{17} are turned on, while the diodes D_{11} and D_{12} become reverse biased, so that C_{11} and C_{12} and dc source V_{DC1} are able to output in series, having the total amplitude of $3V_{DC}$. This can be seen in Fig. 2(a) and (b). A similar operation happens with capacitors C_{21} and C_{22} during the remaining half-cycle of the output voltage. Notice that in the proposed topology the upper capacitors discharge/charge more than the lower capacitor. This happens during the $\pm 2V_{DC}$ levels (see example of Fig. 2(c) for $+2V_{DC}$).

When the fully recharged capacitors start to discharge and pump the internal stored energy to load for generating more voltage levels, the voltages are reduced from their expected initial value ($2V_{DC}$ or $3V_{DC}$) until the coming of the next charging period. Therefore, voltage ripple appear on each capacitor C_{11}, C_{12}, C_{13}, C_{14}. Taking the discharging durations of all capacitors and the load current at each level into consideration, the appropriate capacitance can be calculated and selected. Therefore, the voltage ripple of each capacitor can be limited within a certain allowable range according to the capacitance calculations are given in subsection *D*.

2.4. Designs of the inverter components

This section presents the general considerations to design capacitors and semiconductor ratings of the proposed topology. The total equivalent capacitance C_T can be designed based on the following relations of input and output power, assuming a *RL* constant load:

$$\eta p_i = \eta\, V_{DC} i_{in} = p_o = v_o i_o$$
$$\varphi = arctg\left(\frac{\omega L}{R + ESR_C}\right) \tag{1}$$

$$\eta\, V_{DC} i_{in} = \sqrt{2}\, U_o \sin(\omega t)\sqrt{2}\, I_o \sin(\omega t - \varphi) \tag{2}$$

$$I_o = \frac{U_o}{\sqrt{(R + ESR_C)^2 + (\omega L)^2}} \tag{3}$$

$$\eta\, V_{DC} i_{in} = \frac{2\, U_o I_o}{2}[\cos(\varphi) + \cos(2\omega t - \varphi)] \tag{4}$$

$$i_{in} = \underbrace{\frac{U_o I_o}{\eta\, V_{DC}}\cos(\varphi)}_{I_{in-AV}} + \underbrace{\frac{U_o I_o}{\eta\, V_{DC}}\cos(2\omega t - \varphi)}_{i_{in-AC}} \tag{5}$$

$$v_{C-AC} = \frac{1}{C_T}\int_0^{\omega t} i_{in-AC}\, dt = \frac{U_o I_o}{2\omega C_T \eta V_{DC}}\sin(2\omega t) \tag{6}$$

$$\Delta v_{C-AC} = 2\frac{U_o I_o}{2\omega C_T \eta V_{DC}} = \frac{U_o I_o}{\omega C_T \eta V_{DC}} = \frac{P_o}{\omega C_T \eta V_{DC}} \tag{7}$$

$$C_T = \frac{P_o}{\omega \eta V_{DC} \Delta v_{C-AC}} \tag{8}$$

where P_o is the maximum output power; ω is the fundamental frequency; η is the efficiency of the converter; ESR_C is the equivalent series resistance of the capacitors; V_{DC} is the input voltage of the converter; U_o is the maximum output voltage; I_o is the maximum output current and $\Delta v_{C\text{-}AC}$ is the voltage ripple which is usually acceptable between 2 % to 5 % of the desired output voltage. In the previous equations v_o, i_o, p_o, p_i, i_{in} and φ are the instantaneous output voltage, the instantaneous output current, the instantaneous output power, the instantaneous input power, the instantaneous input current and phase displacement between the output voltage and output current. Taking as example a simplified model where the maximum output voltage ($+4V_{DC}$) is applied, the circuit can be designed as presented in Fig. 3. In this case two capacitors and two power sources are connected in series. Eq. (9) is similar to Eq. (8) but in this case, it is considering that the two input power sources V_{DC1} and V_{DC2} ($V_{DC1} \approx V_{DC2} \approx V_{DC}$) maintains a fixed and constant voltage, leading to a more accurate calculation of the required capacitance considering only the voltage associate to two capacitors. Considering other examples presented in Fig. 3 will lead to similar results. Thus, considering that each power source (V_{DC}) maintains a fixed and constant voltage, the equivalent capacitance of each capacitor can be designed as:

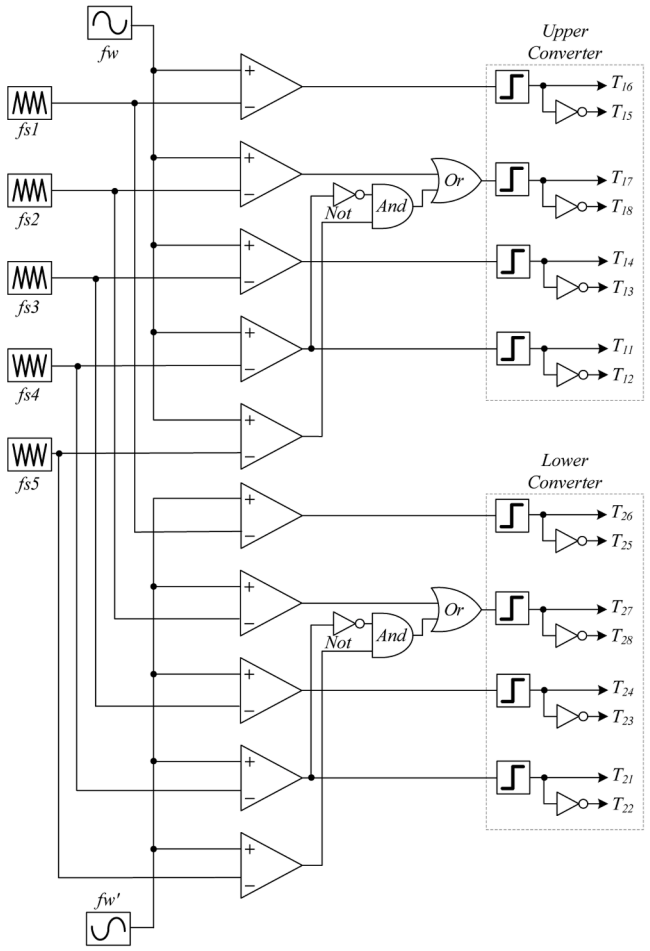

Fig. 4. Block diagram circuits for the generation of the transistor gate signals for the upper and lower converter.

$$C_T' = \frac{(U_o - 2V_{DC})I_o}{\omega\eta V_{DC}\Delta v_{C-AC}} \tag{9}$$

Since capacitors are connected in series in this structure (see Fig. 3a), each capacitor C must have $2C_T'$.

Alternatively, the capacitors design an also be calculated during the largest discharging gap for pumping the stored energy to load side in a cycle. Assuming an inductive load, the continuous discharging amount of C_T' during its largest discharging gap [θ_1, θ_2] (which happens for the highest output voltage level), can be calculated as:

$$\Delta Q_T' = \int_{\theta_1}^{\theta_2} \sqrt{2}\, I_o \sin(\omega t - \varphi) dt \tag{10}$$

Therefore, the capacitance of C_T' should satisfy:

$$C_T' > \frac{1}{\Delta v_{C-AC}} \int_{\theta_1}^{\theta_2} \sqrt{2}\, I_o \sin(\omega t - \varphi) dt \Rightarrow C_T'$$
$$> \frac{\sqrt{2}\, I_o}{\omega \Delta v_{C-AC}} [\cos(\omega\theta_1 - \varphi) - \cos(\omega\theta_2 - \varphi)] \tag{11}$$

Where θ_2-θ_1 is the total amount of time during the largest discharging gap for pumping the stored energy to load side in a cycle.

The expression of the power ripple (P_R) loss and average power conduction losses (P_C) of each capacitor can be calculated using Eqs. (12) and (13), respectively.

$$P_R = C(\Delta v_{C-AC})^2 f \tag{12}$$

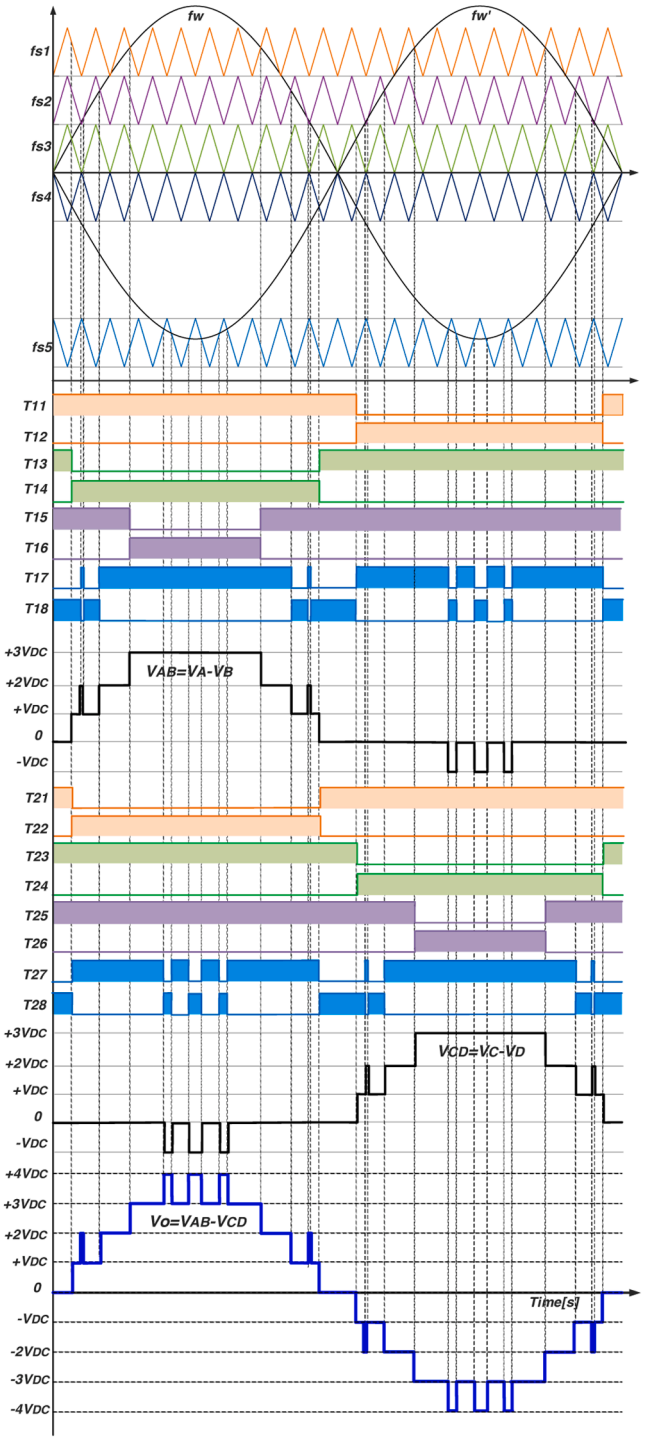

Fig. 5. Theoretical POD-MCPWM for the proposed FB2HB9 L inverter, gating signals of the switches and AC output voltage waveform.

$$P_C = \frac{1}{T} \int_0^T R_{ESR} i_{in}^2 dt \tag{13}$$

where T and R_{ESR} are the operation period and the equivalent series resistance of the capacitor, respectively. In this topology all transistors must withstand a maximum reverse voltage of V_{DC} with average current value given by (14).

$$I_T = \frac{1}{2\pi} \int_0^{2\pi} \sqrt{2}\, I_o \sin(\omega t - \varphi)\, d\omega t = \frac{\sqrt{2}\, I_o}{\pi} \cos(-\varphi) \tag{14}$$

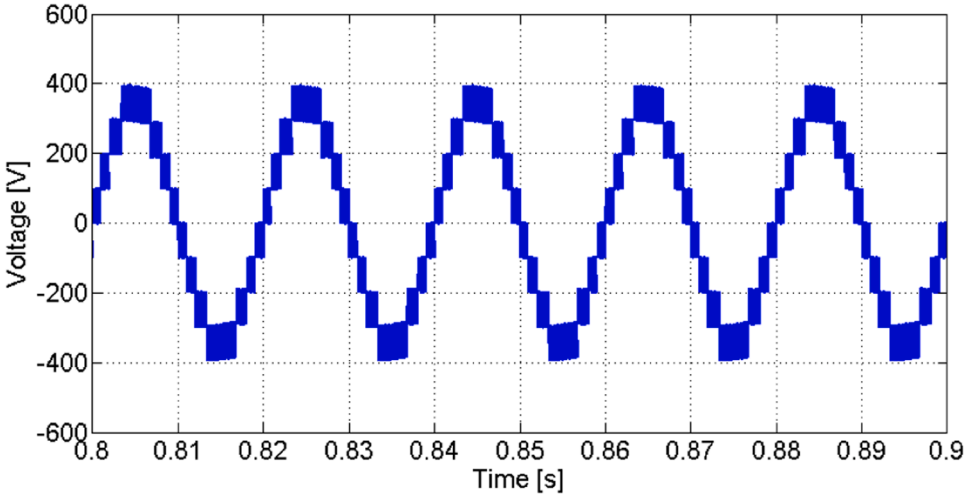

Fig. 6. Simulation result of the output voltage (V_o) of the proposed nine-level inverter. This result was obtained with $m_a = 0.93$.

Table 2
Comparison of the proposed multilevel converter with similar nine-level topologies.

Topology →	[15]	[25]	[26]	[27]	[28]	[29]	[30]	[31]	[32]	FB2HB9L
voltage gain	2	2	2	2	4	4	4	4	1	4
number of switches	8	10	9	9	24	10	8	14	10	16
number of diodes	1	1	2	1	4	1	3	0	0	4
number of capacitors	2	2	2	4	8	2	3	2	4	4
self-balance capability	yes	yes	yes	Yes	yes	yes	yes	yes	yes	yes
maximum reverse voltage of switches	V_o	$3V_o/4$	$V_o/2$	V_o	V_o	V_o	$V_o/2$	$V_o/2$	$V_o/2$	$V_o/4$
Total Blocking Voltage (pu)	5	6	6.5	5	6.5	5.75	5.75	4.75	5.5	5
All switches must support the same blocking voltage	no	no	no	No	no	no	no	no	no	yes
modularity	no	yes	no	No	yes	no	no	no	no	yes
Efficiency	96.47 % @333.3W	95 % @750W	94.18 % @200W	97.5 % @1.2kW	96.21 % @100W	94.25 % @500W	93 % @500W	93 % @250W	96.8 % @500W	93.1 % @ 1kW
Cost[€]/kW	37.2	27.9	43.1	45.8	125.9	22.3	83.4	108.4	33.6	58.32

3. Modulation strategy

The generation of driving signals to turn the switches *ON* or *OFF* will be implemented through a phase-opposition-disposition Multicarrier Pulse Width Modulation (*POD-MCPWM*). This classic modulator consists into n carrier level-shifted triangular signals (i.e. with different offset values), with half of them in phase opposition with only one sinusoidal modulating waveform. Therefore, for a nine-level converter with classic *POD-MCPWM* eight high-frequency carrier triangular waveforms and one low frequency sinusoidal modulating waveform are needed. The output pulses are thereby combined to produce the respective n-level staircase output voltage waveform [42]. As the proposed topology is composed by two cascaded converters, a modified version of the *POD-MCPWM* needing only five carrier triangular signals and two phase-opposition sinusoidal modulating waveforms is used. A simplified block diagram of this modulation for the upper and lower converter can be seen in Fig. 4.

Accordingly, the intersection of the sinusoidal modulating waveform f_W with f_{S1}-f_{S5} generate the gate drive signals for the devices of the upper converter (T_{11}-T_{18}) which corresponds to the output voltage of the top converter, namely V_{AB}. The intersection of the sinusoidal modulating waveform $f_{W'}$ (which is in phase-opposition with f_W) with f_{S1}-f_{S5} generate the gate drive signals for the devices of the lower converter (T_{21}-T_{28}) which corresponds to the output voltage of the lower converter, namely V_{CD}. Finally, the output voltage is the voltage difference between both converters (V_o). The Theoretical *POD-MCPWM* waveforms for the proposed *FB2HB9 L* inverter can be seen in Fig. 5. It should be noted that the carrier waveforms do not exhibit the typical format due to the asymmetric operation of each module. As shown in Fig. 6, the AC output voltages generated by each module are asymmetric. A symmetric AC voltage is only achieved through the combination of both modules. Each module generates three positive voltage levels and one negative voltage level (see Fig. 6). The output voltage is the difference between the two modules, V_{AB} - V_{CD}. For example, the three positive voltage levels are generated by the upper module using its three voltage levels (while the lower module remains at zero). The fourth voltage level is obtained using the negative voltage level of the lower module (the difference yields the four voltage levels). Therefore, since the fourth voltage level is generated by the lower module, instead of using a carrier above the other carriers, a carrier at the top but for the other module (in a symmetric position) must be used.

4. Comparison with other seven-level topologies

In order to evaluate the advantages and disadvantages of the proposed *FB2HB9 L*, a comparative study is performed in this section. As a basis for comparison, the analysed multilevel topologies are expected to have the same output voltage levels. The comparative analysis is done considering several characteristics as presented in 2. One of the characteristics is the Total Blocking Voltage (*TBV_pu*), which is defined in [30], and is given by the following equation:

Table 3
Parameters of the system.

Description	Value
C_{11}, C_{12}	1000 μH
C_{21}, C_{22}	1000 μH
V_{DC}	100 V
Load	100 Ω, 40 mH
POD-MCPWM modulator	12 kHz
sinusoidal modulating waveforms	50 kHz
modulation index (m_a)	0.93
Output Voltage V_o (for m_a=0.93)	240 V_{RMS}
Nominal Power (P_o)	1 kW

$$T_{BV\_pu} = \frac{\sum_{i=1}^{2}\sum_{j=1}^{8} V_{Max\_T_{ij}} + \sum_{k=1}^{2}\sum_{l=1}^{2} V_{Max\_D_{kl}}}{V_{o\_Max}} \quad (15)$$

where V_{Max_Tij}, V_{Max_Dkl} and V_{o_Max} are the transistor maximum blocking voltage, the diode maximum voltage and maximum output voltage, respectively.

Comparing the proposed multilevel *FB2HB9 L* with similar nine-voltage level topologies, taking into consideration the several parameters presented in Table 2, it is possible to see that there are advantages and also some disadvantages. None of the solutions is ideal, as expected, with each presenting strengths in different areas. It is therefore essential to consider all solutions to provide options with respect to the intended application and its specific requirements. As can be seen in this Table, the proposed *FB2HB9 L* together with the topologies [28] [29], [30], and [31] present the higher voltage gain. As disadvantages, it can be seen that *FB2HB9 L* requires more switches, diodes and capacitors than most topologies, but when this comparison is among the topologies with higher voltage gain is not the worst. On the other hand, it is the topology that requires lower maximum reverse voltage ratings in all switches and is among those that present the reduced total blocking voltage. Additionally, *FB2HB9 L* is the only topology where all the switches must hold-off the same blocking voltage, one-quarter of the peak output voltage, and presents the higher modularity (using classical full- and half-bridges). With regard to efficiency, the reported values for the other solutions were obtained under different power conditions. However, comparison of the proposed solution's efficiency reveals that it is consistent with the performance of the other solutions. Consequently, two primary advantages of the proposed solution can be identified: namely, uniform voltage stress across all switches and a substantially reduced voltage stress in comparison to the maximum output AC voltage. Another aspect presented in the comparative table is the cost of the converters. Each topology has different power characteristics, which is why the cost per kW was introduced to make the comparative analysis as fair as possible. There are several factors that are difficult to consider

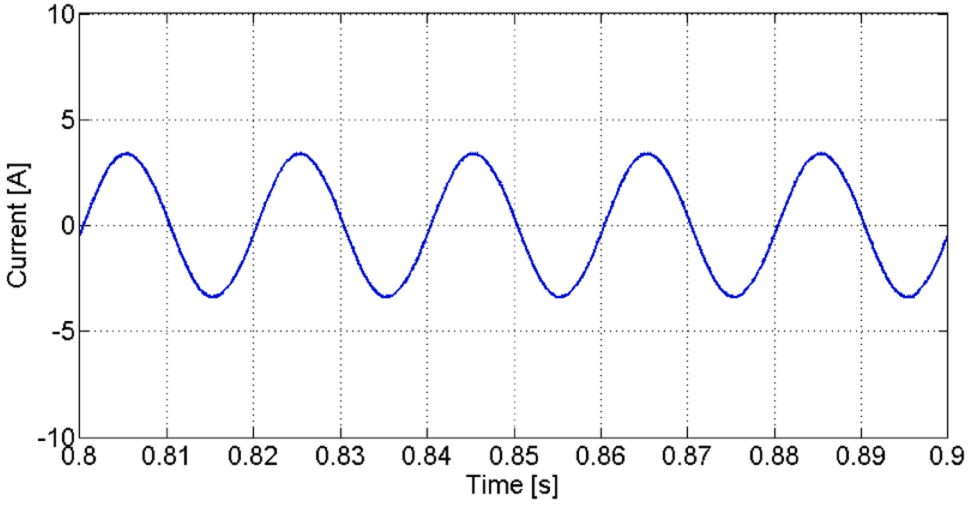

Fig. 7. Simulation result of the output current waveform (I_o) of the proposed nine-level inverter. This result was obtained with $m_a = 0.93$.

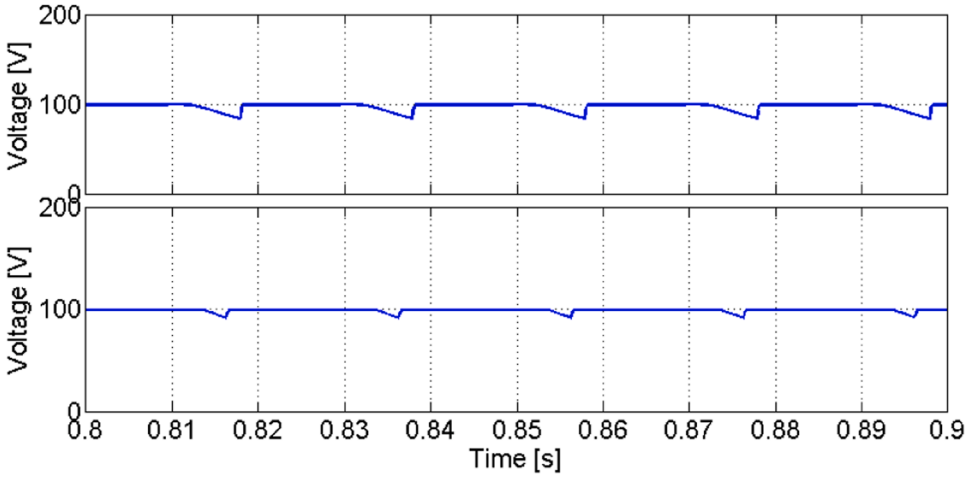

Fig. 8. Simulation result of the capacitor voltages in steady-state operation: V_{C11}(up) and V_{C12}(down).

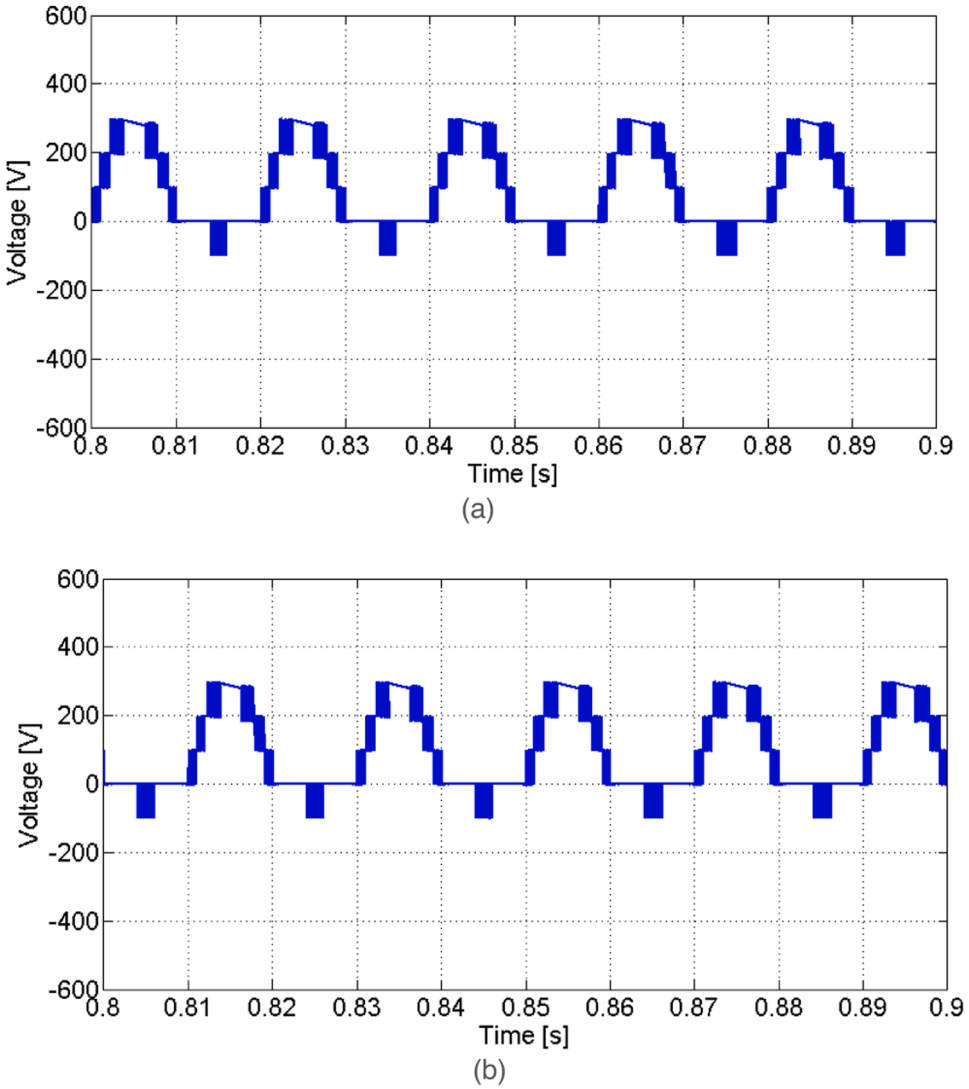

Fig. 9. Simulation results of the output voltages (a) on the first converter V_{AB} (b) on the second converter V_{CD}.

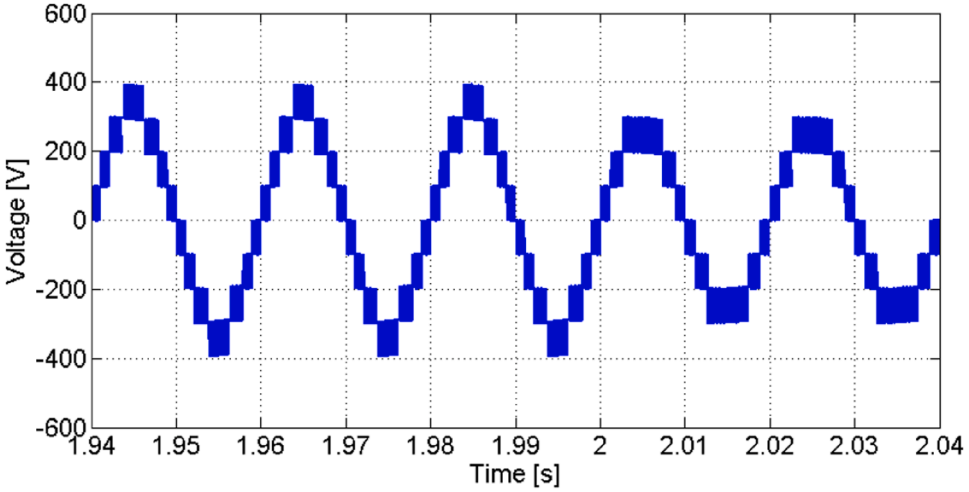

Fig. 10. Simulation result of the output voltage V_o of the proposed nine-level inverter. This result was obtained for a change in the modulation index from $m_a = 0.93$ to $m_a = 0.66$.

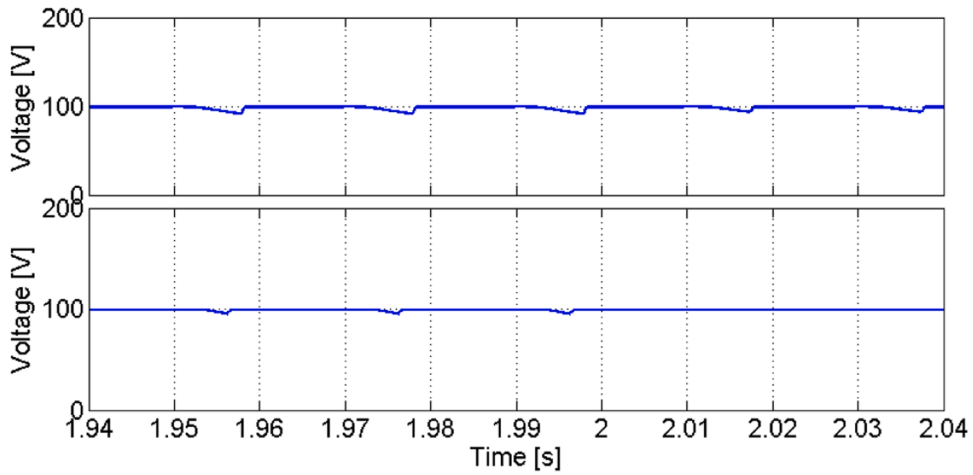

Fig. 11. Simulation result of the capacitor voltages (V_{C11}(up) and V_{C12}(down).) of the proposed nine-level inverter. This result was obtained for a change in the modulation index from $m_a = 0.93$ to $m_a = 0.66$.

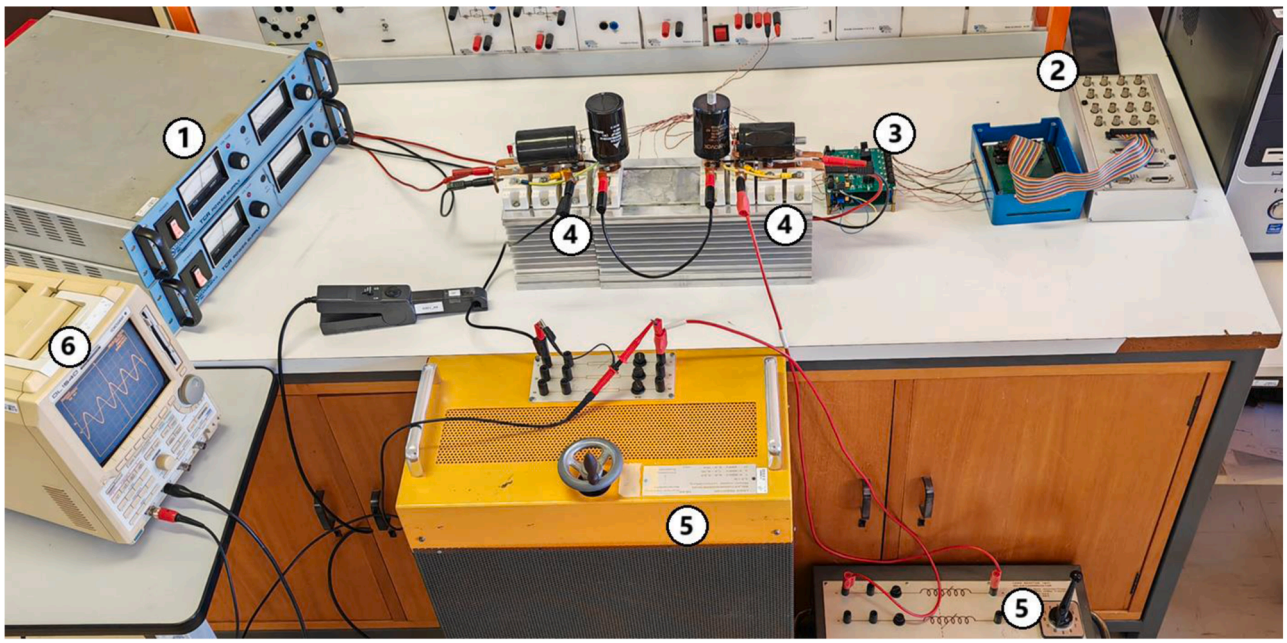

Fig. 12. Photograph of the laboratory prototype of the proposed *FB2HB9 L* topology; 1 – DC power sources VDC1 and VDC2 (each up to 150 VDC, 20 A); 2 – Digital Signal Processor model DSPACE1104 with the modulation strategy implemented; 3 – gate drive circuit board to turn on/turn off the power devices; 4 – Proposed power converter divided in two sections (the power semiconductors and diodes modules are from Semikron, namely SKM400GB12T4 - 1200 V dual IGBT and SKKE 81/08, single diode; 800 V; If: 80A; SEMIPACK1 module. The aluminium electrolytic capacitors adopted in the laboratory prototype are 1000 μF-400 VDC; 5 - Resistive and inductive load; 6 – Oscilloscope Yokogawa DL1540 with current and voltage probes.

regarding cost, as only manufacturers have the necessary experience to implement and sell converters on a larger scale. However, this provides at least some insight into the cost. This analysis reveals that no single topology exhibits advantages across all aspects, as expected. Therefore, no perfect solution exists, with each topology offering specific strengths in different areas. Regarding the proposed topology, one key advantage is that all switches experience the same voltage stress. In contrast, other topologies require switches with varying voltage ratings, which can present challenges in terms of maintenance and inventory management. It also exhibits the lowest switch voltage stress, as it is only one-fourth of the maximum output AC voltage. Finally, the topology is also found in those configurations that present greater voltage gain.

5. Simulation verification

The proposed FB2HB9 L as a boost voltage source inverter was first tested using the well-established simulator MATLAB/Simulink, utilizing components from the Simscape Electrical component libraries. For this study, the system parameters listed in Table 3 were considered.

A first test with modulation index (m_a) 0.93 was conducted. The obtained results, presented in Fig. 6 and Fig. 7, show the nine-level output voltage operation of the proposed inverter, achieving a peak voltage of $4V_{DC}$, together with the sinusoidal output current. The output current in the *RL* load presents a $THD_i = 2.1$ %. Regarding the output voltage the THD_v value is 18.2 %. The voltages in the capacitors C_{11} and C_{12} can be seen in Fig. 8. This figure shows that the upper capacitor (C_{11}) has a slightly higher ripple (discharges more) compared to the lower capacitor (C_{12}). Fig. 9 shows the output voltage on the first converter

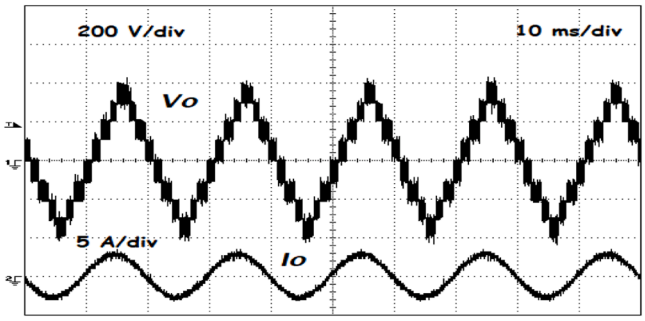

Fig. 13. Experimental result of the output voltage (V_o) (*CH1*) and output current waveform (I_o) (*CH2*) of the proposed nine-level inverter. This result was obtained with ma = 0.93.

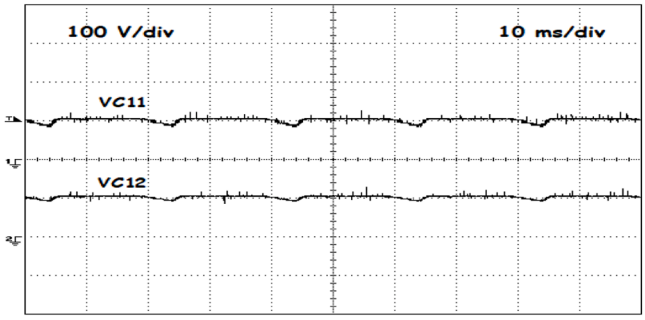

Fig. 14. Experimental result of the capacitor voltages in steady-state operation: V_{C11}(*CH1*) and V_{C12}(*CH2*).

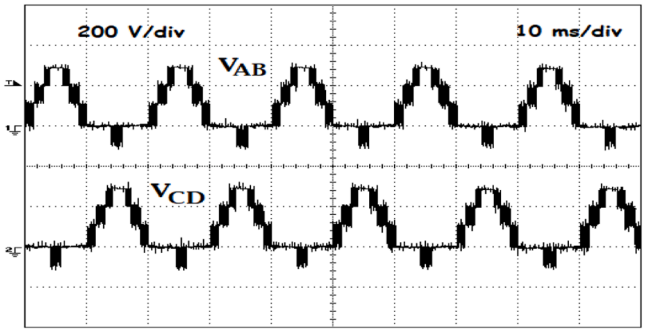

Fig. 15. Experimental result of the voltage on the first converter V_{AB}(*CH1*) and the output voltage on the second converter V_{CD}(*CH2*).

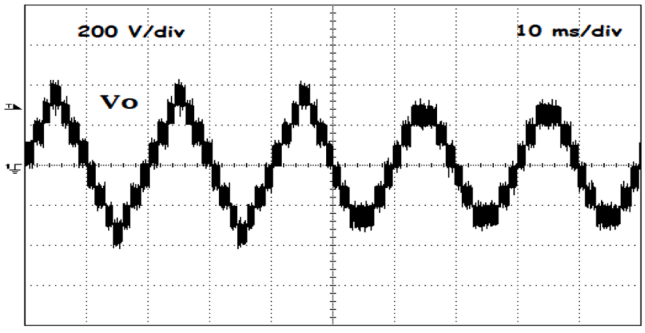

Fig. 16. Experimental result of the output voltage (V_o) of the proposed seven-level inverter. This result was obtained considering a transition in the modulation index from $m_a = 0.93$ to $m_a = 0.66$.

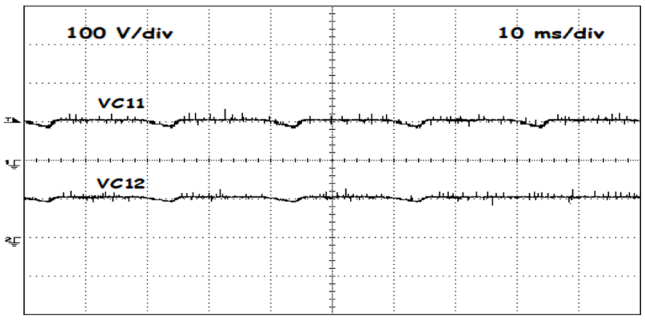

Fig. 17. Experimental result of the capacitor voltages considering a transition in the modulation index from $m_a = 0.93$ to $m_a = 0.66$: V_{C11}(*CH1*) and V_{C12}(*CH2*).

(V_{AB}) and the output voltage on the second converter (V_{CD}). From these waveforms it is possible to conclude that output voltages are in conformity with the theoretical *POD-MCPWM* proposed. The proposed *FB2HB9 L* inverter was also tested in transient conditions. Fig. 10 shows the obtained *AC* output voltage for a modulation index transition from $m_a = 0.93$ to $m_a = 0.66$. As anticipated, a reduction in the modulation index results in a decrease in both the output voltage and the number of voltage levels, as evidenced by the figure. The voltages in the capacitors C_{11} and C_{12} considering the modulation index transition from $m_a = 0.93$ to $m_a = 0.66$ are shown in Fig. 11. This figure displays that only capacitor C_{11} is affected by the duty cycle, as only seven-levels are active when $m_a = 0.66$.

6. Laboratory validation

A laboratory prototype of the proposed *FB2HB9 L* as a boost voltage source inverter was built, using off-the-shelf components, to compare experiments with simulations and theoretical assumptions. For comparison purposes, the same parameters used in the simulations were applied. A photograph of a 1 kW laboratory prototype and the laboratory workbench can be seen in Fig. 12, with some details of the adopted equipment and components. In this photograph is possible to see: 1 – DC power sources VDC1 and VDC2 (each up to 150 V_{DC}, 20 A); 2 – Digital Signal Processor model DSPACE1104 with the modulation strategy implemented; 3 – gate drive circuit board to turn on/turn off the power devices; 4 – Proposed power converter divided in two sections (the power semiconductors and diodes modules are from Semikron, namely SKM400GB12T4 - 1200 V dual IGBT and SKKE 81/08, single diode; 800 V; If: 80A; SEMIPACK1 module. The aluminium electrolytic capacitors adopted in the laboratory prototype are 1000 μF-400 V_{DC}; 5 - Resistive and inductive load; 6 – Oscilloscope Yokogawa DL1540 with current and voltage probes.

The experimental tests began with a modulation index of $m_a = 0.93$. The obtained experimental result in Fig. 13 confirms the nine-level output voltage operation of the proposed inverter, achieving a peak voltage of $4V_{DC}$, together with the sinusoidal output current. The output current in the *RL* load presents a $THD_i = 2.4$ %. Regarding the output voltage the THD_v value is 19.8 %. The voltages in the capacitors C_{11} and C_{12} can be seen in Fig. 14, where CH_1 represents V_{C11} and CH_2 represents V_{C12}. This figure confirms that the upper capacitor (C_{11}) has a slightly higher ripple (discharges more) compared to the lower capacitor (C_{12}). Fig. 15 shows the output voltage on the first converter (V_{AB}-CH_1) and the output voltage on the second converter (V_{CD}-CH_2). These waveforms demonstrate that the output voltages align with the theoretical *POD-MCPWM* proposed. The proposed *FB2HB9 L* inverter was also evaluated under transient conditions. Fig. 16 shows the obtained *AC* output voltage for a modulation index transition from $m_a = 0.93$ to $m_a = 0.66$. This figure illustrates a reduction in the output voltage and a corresponding decrease in the number of voltage levels. The voltages in the

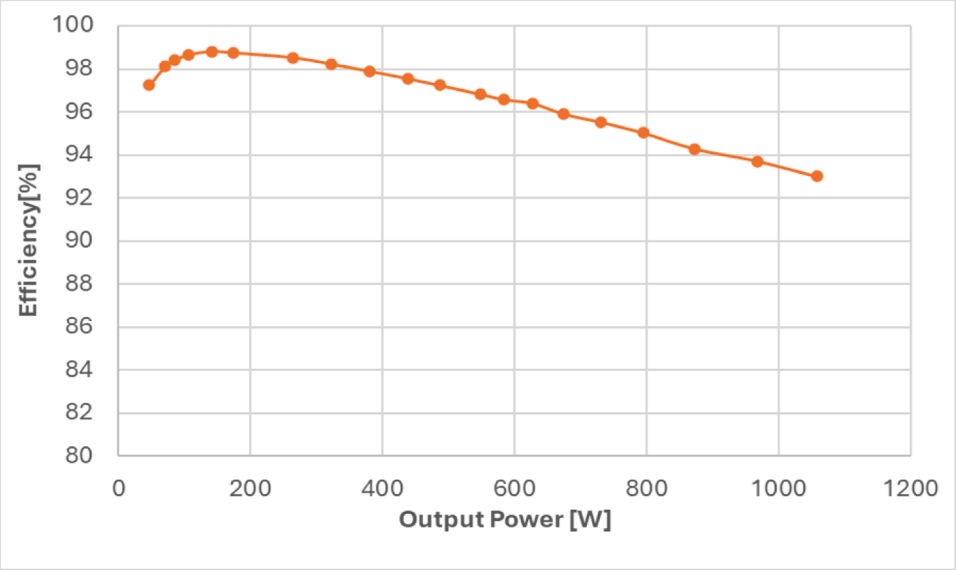

Fig. 18. Efficiency of proposed *FB2HB9 L* prototype versus output power.

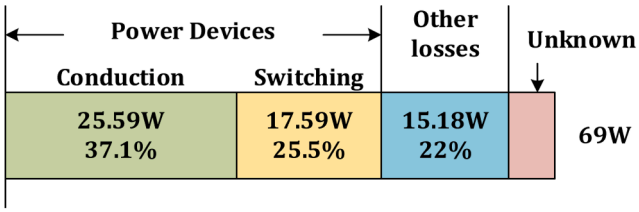

Fig. 19. Power-Loss Breakdown of the proposed *FB2HB9 L* prototype at 1 kW, 100V_{DC} input voltage, and 20 kHz switching frequency.

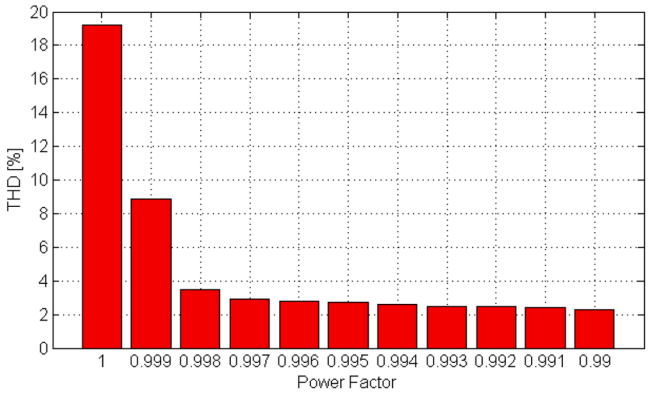

Fig. 20. Converter's load current THD at various load power factors.

capacitors C_{11} and C_{12} considering the modulation index transition from $m_a = 0.93$ to $m_a = 0.66$ are shown in Fig. 17. This figure shows that only capacitor C_{11} is influenced by the duty cycle, as only seven-levels are active when $m_a = 0.66$.

Considering the conditions of the previous tests and achieved results, several experiments were also performed in order to obtain the efficiency of the proposed converters. For the operation of the converter at different output powers, the efficiency curve is presented in Fig. 18. In general, the proposed converter presents a maximum efficiency of 98,8 % at 150 W and an efficiency of 93.1 % at nominal power of 1kW.

Besides the results of the overall efficiency, a study about the power-loss breakdown was also made. This important study points out the components that dominate the power-loss amongst the components of the power converters. Fig. 19 presents the power-loss breakdown at the nominal power output of 1 kW, considering power semiconductors conduction and switching losses, and other losses (wire losses, temperature dependent losses in power components, skin and proximity effect losses, capacitors equivalent series resistances). The gate-drive and control circuit losses were not considered. The results presented in Fig. 19 show that the majority of the losses are associated with the power semiconductor devices, being 62.6 % of total losses. The conduction losses are higher than the switching losses. That are also some unknown losses around 15,4 %.

Tests evaluating the converter's load current THD at various load power factors were also conducted. Fig. 20 presents a bar graph of the obtained THD values as a function of the load power factor. This figure shows that at unity power factor, the current THD is approximately equal to the load voltage THD. However, as the power factor decreases, the current THD rapidly approaches values between 2 % and 3 %.

7. Conclusion

This paper proposes a novel single-phase, nine-level inverter topology with a quadruple boost capability. The FB2HB9 L topology utilizes sixteen controlled power semiconductor switches, four diodes, and four capacitors. It is one of the topologies in the literature that can employ a modular structure based on single-phase full and half-bridge voltage source inverters (VSIs). Another aspect is that all switches must withstand the same blocking voltage and present a very low total blocking voltage, characterized by a value of 5. In fact, only one of the topologies exhibited a lower value, namely 4.5. The POD-MCPWM modulation strategy adopted is relatively easy to implement in microprocessor achieving a comparatively low THD content for both output current and voltage. Additionally, all capacitors, diodes, and power devices must withstand only the input DC source voltage. The solution also provides capacitor voltage self-balancing capability using the proposed modulation. Comparison with similar topologies reveals both advantages and disadvantages. However, the proposed solution offers two key advantages: uniform voltage stress across all switches and substantially reduced voltage stress compared to the maximum output AC voltage. The experimental results show the expected voltage and current waveforms in accordance with theoretical considerations. As a consequence of the converter's multilevel operation, an AC output voltage THD of 19.8 % was achieved, with corresponding output current THD values ranging from 2 % to 3 %. With respect to efficiency, a value of 93.1 %

was obtained at a nominal power level of 1 kW. In addition to confirming the anticipated characteristics of the proposed converter, the developed laboratory prototype also demonstrated the feasibility of this approach.

CRediT authorship contribution statement

V. Fernão Pires: Writing – original draft, Validation, Methodology, Investigation, Conceptualization. **Armando Cordeiro:** Writing – review & editing, Visualization, Validation, Resources, Investigation. **Daniel Foito:** Visualization, Validation, Resources. **Joaquim Monteiro:** Writing – review & editing, Visualization, Validation, Investigation. **Hao Chen:** Writing – review & editing, Visualization, Validation, Investigation. **J. Fernando Silva:** Writing – review & editing, Visualization, Validation, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

No data was used for the research described in the article.

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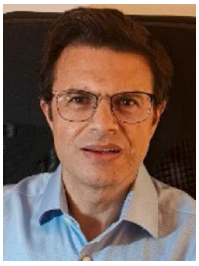

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