NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ANA CAROLINA REI AZEVEDO

BSc of Sciences in Electrical and Computer Engineering

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To my family for always supporting me.

# Acknowledgements

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”

*“Nobody who ever gave his best regretted it.”*

**— George Halas**

# Abstract

The evolution of digital communication standards, such as 5G, requires Radio Frequency Front-End (RFFE) of Radio Frequency Complementary Metal-Oxide-Semiconductor (RF-CMOS) receivers to deal with complex modulations (e.g. Orthogonal Frequency Division Multiplexing (OFDM), 64-Quadrature Amplitude Modulation (QAM)) and a congested spectrum, which makes interference management crucial. As such, filters with a high quality factor are required. However, traditional solutions, which use multiple filters dedicated to different frequency bands, increase costs and complexity. N-path filters have emerged as an efficient alternative, offering high quality filters and reconfigurability to adjust the centre frequency and bandwidth, combining performance, flexibility and simplification.

This thesis focuses on the implementation of key components of the RFFE receiver, such as the mixing, filtering, amplification and clock generation phases, with particular emphasis on the application of the N-Path filter. The design and layout of the components were developed in 65nm Bulk Complementary Metal-Oxide-Semiconductor (CMOS) technology, with a supply voltage of 1.2V, with the receiver being designed to operate in the GHz band.

The simulations carried out on the receiver schematic demonstrated fulfilment of the main performance requirements, including selectivity and quality factor, validating the effectiveness of implementing the N-path filter in the receiver chain. To assess the N-path behaviour under technology parameter variations, Monte Carlo simulations were conducted, analyzing key performance metrics such as DC gain, center frequency, and gain at center frequency. The robustness of the circuit was evaluated through the average and standard deviation of these parameters. Additionally, the post-layout simulations, with RC extraction, were consistent with the results obtained in the schematic, with minor deviations. Finally, the energy consumption revealed that the RFFE of the RF-CMOS receiver consumed 1.58mW.

**Keywords:** RF-CMOS Receivers, RFFE, N-Path filters

# Resumo

A evolução dos padrões de comunicação digital, como o 5G, exige que os recetores de RF-CMOS lidem com modulações complexas (e.g., OFDM, 64-QAM) e um espectro congestionado, que torna crucial a gestão de interferências. Como tal, são necessários filtros com elevado fator de qualidade. Contudo, soluções tradicionais, que utilizam múltiplos filtros dedicados a diferentes bandas de frequência, aumentam custos e complexidade. Os filtros N-path surgem como uma alternativa eficiente, ao oferecerem filtros com alta qualidade e reconfigurabilidade para ajustar a frequência central e a largura de banda, combinando desempenho, flexibilidade e simplificação.

Esta tese centra-se na implementação de componentes chave do RFFE de um recetor, que implementam as fases de mistura, filtragem, amplificação e geração de relógio, com particular ênfase na aplicação do filtro N-Path. O projeto e a disposição dos componentes foram desenvolvidos em tecnologia Bulk CMOS de 65nm da TSMC, com uma tensão de alimentação de 1.2V, com o recetor a ser desenvolvido para funcionar na banda dos GHz.

As simulações realizadas no esquema do recetor demonstraram o cumprimento dos principais requisitos de desempenho, incluindo a seletividade e o fator de qualidade, validando a eficácia da implementação do filtro N-path na cadeia do recetor. Para avaliar o comportamento do N-path sob variações nos parâmetros da tecnologia, foram efectuadas simulações de Monte Carlo, analisando os principais parâmetros de desempenho, como o ganho DC, a frequência central e o ganho na frequência central. A robustez do circuito foi avaliada através da média e do desvio padrão destes parâmetros. Adicionalmente, as simulações pós-layout, com extração RC, foram consistentes com os resultados obtidos no esquemático, com pequenos desvios. Finalmente, o consumo de energia revelou que o RFFE do recetor RF-CMOS consumiu 1.58mW.

**Palavras-chave:** Recetores RF-CMOS, RFFE, Filtros N-Path

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# Acronyms

**AC** Alternating Current *(p. 38)*
**ADC** Analog-to-Digital Converter *(p. 36)*

**BAW** Bulk Acoustic Waves *(p. 27)*
**BPF** Band-Pass Filter *(pp. 11, 46)*
**BW** Bandwidth *(pp. 11, 22)*

**CDMA** Code Division Multiple Access *(p. 8)*
**CMOS** Complementary Metal-Oxide-Semiconductor *(pp. vi, 1, 3, 11, 16, 18, 23, 27, 32, 44)*
**CP** Cyclic Prefix *(p. 9)*
**CS** Common-Source *(pp. 37, 39, 40)*

**DC** Direct Current *(pp. 11, 12, 24, 25, 38, 47)*
**DCR** Direct-Conversion Receiver *(pp. 6, 23, 26, 27, 29, 36, 60)*
**DSP** Digital Signal Processing *(p. 10)*

**FFD** Flip-Flop D *(pp. 52–54)*
**FFT** Fast Fourier Transform *(p. 8)*

**GBW** Gain Bandwidth *(pp. 42, 49, 50)*

**I** In-Phase *(pp. 2, 6, 7, 16, 17, 19, 20, 23, 24, 36, 39, 57)*
**I/Q** In-phase Quadrature *(pp. 3, 7, 10, 13, 16, 17, 19–24, 35, 36, 45)*
**IC** Integrated Circuit *(pp. 1, 19, 23, 27)*
**IF** Intermediate Frequency *(pp. 6, 20, 22, 29, 30)*
**IFFT** Inverse Fast Fourier Transform *(pp. 8, 9)*
**IIP2** Second-Order Input Intercept Point *(pp. 20, 21)*
**IIP3** Third-Order Input Intercept Point *(pp. 18, 20–22, 26)*

**IM2** Second-Order Intermodulation *(p. 20)*
**IoT** Internet-of-Things *(p. 2)*
**ISI** Intersymbol Interference *(p. 7)*

**LNA** Low-noise Amplifier *(pp. 21, 22, 26, 39)*
**LO** Local Oscillator *(pp. 13, 15, 16, 19, 28–31, 42, 43, 46, 53, 54, 60)*
**LOS** Line-of-Sight *(p. 7)*
**LPF** Low-Pass Filter *(pp. 6, 16, 21, 28)*
**LTE** Long Term Evolution *(p. 11)*
**LTI** Linear Time-Invariant *(p. 27)*

**MOS** Metal-Oxide-Semiconductor *(pp. 1, 18)*
**MOSFET** Metal Oxide Semiconductor Field-Effect Transistor *(pp. 27, 29, 45)*

**NF** Noise Figure *(p. 22)*
**NOMA** Non-Orthogonal Multiple Access *(p. 16)*

**OFDM** Orthogonal Frequency Division Multiplexing *(pp. vi, 1, 2, 7–10, 16, 22, 23)*
**OpAmp** Operational Amplifier *(pp. 37, 39, 40, 50)*

**PO** Polysilicon *(p. 56)*

**Q** Quadrature *(pp. 2, 6, 7, 16, 17, 19, 20, 23, 24, 36, 39, 57)*
**QAM** Quadrature Amplitude Modulation *(pp. vi, 2, 17, 24, 25)*
**QSM** Quadrature Sampling Mixers *(p. 35)*

**RF** Radio Frequency *(pp. 1–3, 5, 6, 13–16, 18–21, 23, 26, 28–30, 56)*
**RF-CMOS** Radio Frequency Complementary Metal-Oxide-Semiconductor *(pp. vi, vii, 1, 5)*
**RFFE** Radio Frequency Front-End *(pp. vi, vii, 60)*
**RHP** Right-Half Plane *(p. 41)*

**SAW** Surface Acoustic Waves *(p. 27)*
**SDR** Software-Defined Radio *(pp. 1, 27)*
**SE** Single-Ended *(p. 29)*
**SFDR** Spurious-free Dynamic Range *(pp. 21, 22)*

**VCO** Voltage-Controlled Oscillator *(p. 22)*

# 1 Introduction

This chapter presents an introduction to the theme of the thesis, offering a concise description of the main problem and a brief description of the organizational structure of the document.

## 1.1 Contextualization

In recent years, the domain of Radio Frequency (RF) communication has undergone a notable expansion, deeply influencing both our everyday lives and professional domains. This growth can be attributed to various factors, with Radio Frequency Complementary Metal-Oxide-Semiconductor (RF-CMOS) being one of the key contributors to it.

The success associated with Complementary Metal-Oxide-Semiconductor (CMOS) technology lies in the affordability achieved through integration, specifically in terms of how much functionality can be consolidated onto a single chip. RF-CMOS is a versatile and efficient technology, essential in numerous fields. Its revolutionary impact extends to commercial radio systems, where it enables practical implementations of Software-Defined Radio (SDR) on a single Metal-Oxide-Semiconductor (MOS) Integrated Circuit (IC) chip. This cutting-edge IC technology once limited to digital design, has evolved significantly to meet the demand for more cost-effective and multifunctional ICs, expanding its applications to more fields as analog-only and mixed-signals (combination of analog and digital) designs.

Figure 1.1, visually depicts the substantial growth in mobile subscriptions across diverse technologies, highlighting the significant increase in the number of subscriptions over the years.

The rapid evolution of wireless communication markets, such as the advent of 5G networks, demands for more efficient modulation schemes to achieve high-speed data transmission. Orthogonal Frequency Division Multiplexing (OFDM) is a widely used technique for high-speed communications, that offers a good spectral efficiency and resilience

to multipath fading [1]. As the need for higher data rates increases, OFDM systems often employ high-density constellation schemes such as 64-Quadrature Amplitude Modulation (QAM) and others. However, this type of schemes comes with their own challenges, and a critical one is the imbalance between the In-Phase (I) and Quadrature (Q) branches within the radio front end.

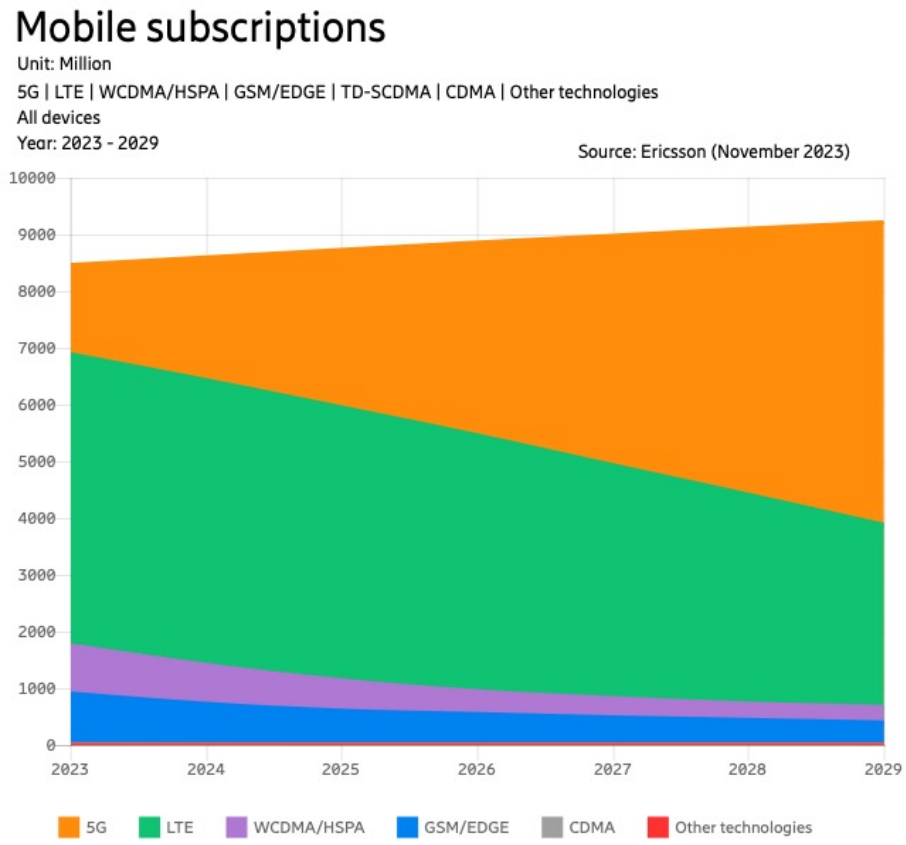



Figure 1.1: Mobile subscription trend (Ericsson mobility visualizer) [2].

The incessant growth of wireless communications systems, such as mobile networks, Wi-Fi, satellite communications, and emerging Internet-of-Things (IoT) applications, has led to a substancial increase in the spectrum demand. This has made the RF spectrum to become an highly crowded resource, leading to higher levels of interference and overall degradation in communication quality. Tradicional methods for frequency allocation are no longer sufficient to meet today's needs, which leads for the search of new approaches, such as spectrum sharing. These new approaches, involves different users or services dynamically sharing the same freqeuncy bands, increasing the risk of interference. As a result, the demands on RF transceiver are growing, as they must be able to extract the desired signal while effectively mitigate the interference. Therefore, a key capability that transceiver should be able to deliver is high-Q filtering. N-Path filters offer a promising solution to meet some RF transceivers demands, providing flexibility and high-Q filtering. These filters allow for reconfigurable frequency selection, an important factor in today's congested spectrum, and dynamic bandwidth adjustments, allowing RF systems

to adapt to crowded environments, maintaining efficient operation across a wide range of frequencies.

## 1.2 Objectives

As the demand for efficient transceiver continues to grow, this thesis aims to implement a receiver block employing N-Path filters techniques. The objective is to develop a receiver capable of delivering performance levels required in today's wireless communication systems, while offering a flexible receiver capable to reconfigure it's characteristics in response to varying spectrum demands.

The receiver must incorporate three fundamental stages: mixing, filtering, amplification and clock generation. Specifically, it will have a mixer that employes N-Path filter techniques, the main topic of study in this thesis. Before implementing the receiver block, a comprehensive study of each component's design will be conducted to ensure the desired performane. The technology used to implement the receiver will be 65nm Bulk CMOS.

## 1.3 Document Organization

Along with this first chapter, the structure of the present thesis is organized as follows:

- **Chapter 2 - State-of-Art of the RF receiver**
  Chapter 2 provides a comprehensive theoretical review to support the understanding of key aspects and design choices in the receiver architecture. A particular focus will be placed on the direct-conversion architecture. Additionally, an introduction to N-Path filters will be presented, along with a description about the importance of incorporating In-phase Quadrature (I/Q) mixing in the receiver design. Relevant literature will also be reviewed and analysed to provide context for the chosen approach.
- **Chapter 3 - RF Front-end Analysis**
  Chapter 3 delves into the detailed design of the three core blocks of the receiver, examining the mixing, filtering, amplification, and clock stages. Each block will be analysed to ensure a good performance level and alignment with the project's goal.
- **Chapter 4 - Design and Layout of the Receiver's RF Front-end Blocks**
  Chapter 4 presents the schematic results and final performance analysis of the designed components. The chapter will also feature the layout implementations of the mixer and amplifier, showcasing the physical design of this blocks.
- **Chapter 5 - Conclusion and Future Work**
  The final chapter summarizes the key conclusions drawn form the thesis, highlighting the achievements and findings. It will also propose potential areas for future

work, suggesting improvements and additional research that could further enhance the receiver's design and performance.

# 2

# RF Front-End State of the Art

In this chapter, the primary objective is to present a study on the Radio Frequency Complementary Metal-Oxide-Semiconductor (RF-CMOS) digital transceivers, Figure 2.1, with special emphasis in the receiver subblock.

## 2.1 Background

Having already covered some concepts of RF-CMOS technology and its importance in advancing the Radio Frequency (RF) field, the focus now shifts towards the components used in receiver architectures and their roles in it. Additionally, the strategic implementation of N-Path processing technique filters and passive commutating mixers will be explored.

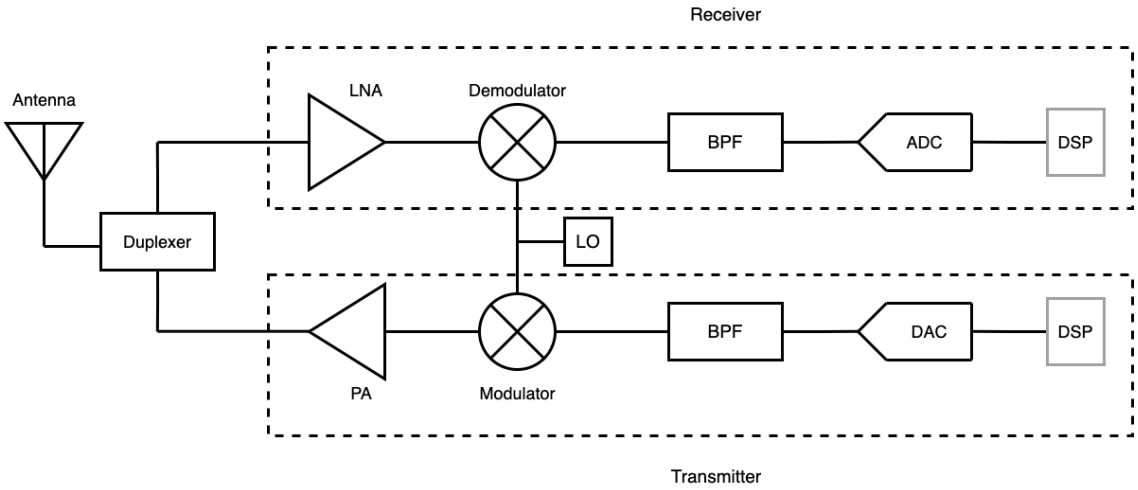



Figure 2.1: Digital transceiver block diagram.

### 2.1.1 Receiver Architectures

Various receiver architectures are utilized in contemporary wireless communication systems. As an integral part of the transceiver, these blocks must be capable of performing

three essential tasks: down conversion, demodulation, and filtering. One example is the heterodyne receiver, which downconverts the RF or bandpass signal to one or two Intermediate Frequencys (IFs). However, this kind of architectures demands, at the IF stages, crucial processes such as high-quality factor image rejection, channel selectivity filtering, and amplification to uphold selectivity and sensitivity [1].

Alternatively, we have the Direct-Conversion Receiver (DCR), also known as zero IF or homodyne receiver, that has been gaining a lot of attention due to their architecture simplicity and ease of integration. Contrarily to heterodyne receivers, DCR directly converts the bandpass/RF signal to the baseband without the need of having an IF conversion stage. Unlike their heterodyne counterpart, zero-IF receivers sidestep the challenges associated with image frequency problems. This means that the need for numerous and sensitive image rejection filters is obviated in this architecture. Furthermore, achieving channel selectivity in zero-IF receivers becomes more straightforward, as integrated Low-Pass Filter (LPF) can readily fulfill this function. For these reasons, and due to the ability of zero-IF architectures to minimize power consumption, cost, area, and the need for fewer off-chip components [3], the direct-conversion receiver architecture has garnered substantial attention and interest in recent years. Figure 2.2 illustrates a block diagram of a direct-conversion receiver.

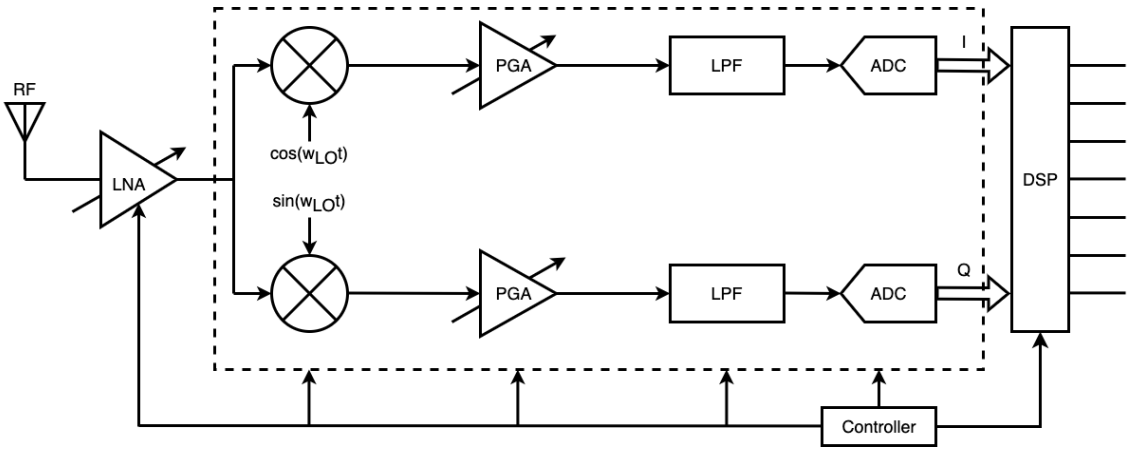



Figure 2.2: Direct-Conversion receiver.

In a zero-IF receiver, the down-conversion process is executed by a quadrature mixing process comprising both In-Phase (I) and Quadrature (Q) signal branches, as illustrated in Figure 2.2. This approach is critical because it prevents the negative-frequency component from overlapping with the positive-frequency component. Without quadrature downconversion, the negative-frequency signal would fold over and merge with the positive-frequency signal, leading to signal distortion. Thus, zero-IF architectures rely on quadrature downconversion to ensure that the full frequency spectrum is accurately captured and processed [4].

The downside is that achieving this requires both I and Q mixers to provide uniform

gain and maintain a 90° phase difference across the entire signal bandwidth in their respective branches. However, achieving this condition is challenging due to practical limitations in the analog components. Figure 2.3 visually represents the differences between the I and Q path. This In-phase Quadrature (I/Q) imbalance ultimately impacts the signal quality [5].

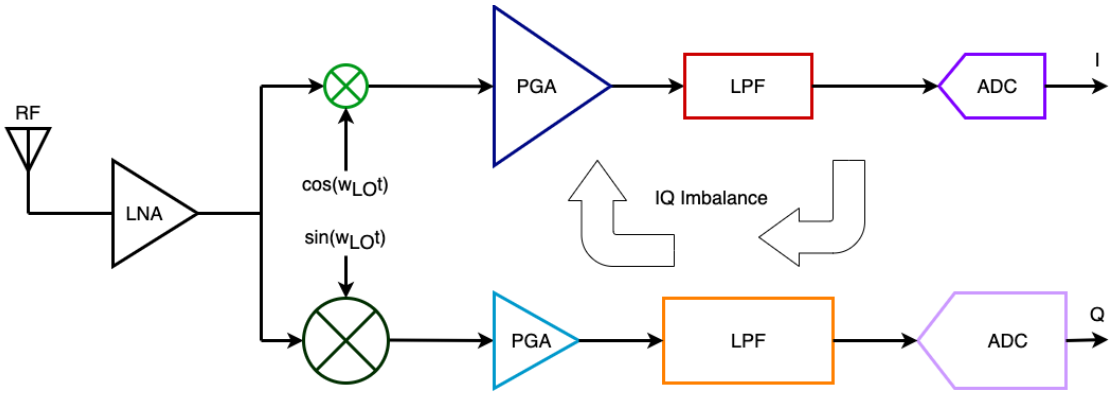



Figure 2.3: Example of I/Q imbalance.

Future wireless systems should be able to provide higher data rates and improve user mobility, all while aiming for low cost, low power consumption, and greater integration. To achieve elevated data rates, the forthcoming trajectory involves operating at higher carrier frequencies and employing higher-order signal constellations. However, these advancements turn systems more susceptible to implementation imperfections, such as I/Q imbalance, signal distortion, among others [6].

### 2.1.2 OFDM

In wireless communication, a significant challenge known as multipath propagation emerges. This phenomenon, illustrated in Figure 2.4, introduces a notable impact on the received signals, primarily manifested through a phenomenon known as Intersymbol Interference (ISI). This effect occurs because the radio channel contains multiple propagation paths. In other words, the signal reaching the receiver side is not uniquely composed of the direct Line-of-Sight (LOS) signal (Direct Path in Figure 2.4(a)), but also includes signals originating from alternative paths with differing delays (Reflective Path in Figure 2.4(a)) [7]. When the transmitted signal spreads over the various paths of the channel, each characterized by distinct propagation delays, the various signals arrive at the receiver at different points in time. Consequently, these delayed signals interfere with each other during the decoding process, causing overlapping and distortion of symbols. The challenge comes when the receiver encounters difficulty in distinguishing between individual symbols, leading to a degradation in the overall communication performance. For this reason, the ISI elimination becomes essential and techniques such as Orthogonal Frequency Division Multiplexing (OFDM) are often used to deal with the effects of multipath, and thus improve the performance of wireless communication systems with low complexity.

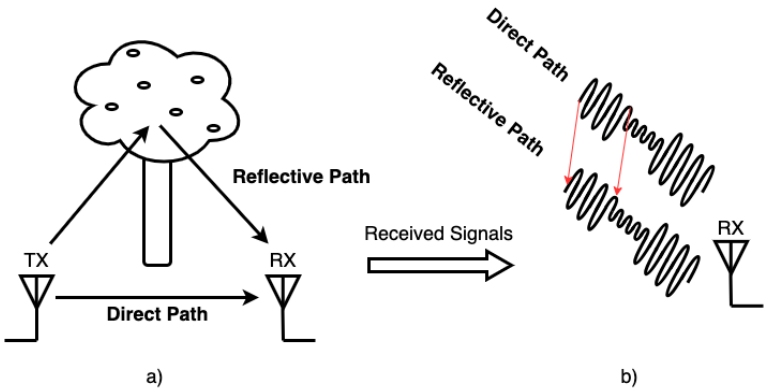



Figure 2.4: (a) Multipath propagation, (b) Effect of the multipath problem on the received signals at receiver [1].

Also, the trajectory of technological evolution further underscores the demand for accelerated data transmissions, as witnessed in the rapid transition between technological generations occurring roughly every decade. Each generation comes with their own paradigmatic change, and with it, a surge in transmission rates that seems boundless. To keep with this pace, becomes imperative the exploration of cutting-edge communication solutions to meet the voracious need for higher data rates in our interconnected world.

The second and third generations heavily utilized Code Division Multiple Access (CDMA), leveraging orthogonal signals and signal-spreading techniques for effective multiple access. However, with the growing increase described above, CDMA faced scalability limitations. In order to solve the problem, the standardization groups sought to find alternative techniques, which led to the emergence of OFDM. Between 2000 and 2004, OFDM demonstrated superior performance, particularly in terms of trasmission rates and wireless link quality, prompting its adoption over CDMA as the preferred solution for future technological generations [8].

The fundamental principle of OFDM lies in the division of the overall channel bandwidth into multiple narrowband subcarries that are orthogonal to each other. This orthogonal arrangement allows for simultaneous transmission of multiple data, significantly enhancing spectral efficiency and robustness in challenging communication environments. Employing this technique has the potential to conserve 50% of bandwidth, as depicted in Figure 2.5. Illustrated in Figure 2.5(a) is the convetional nonoverlapping multicarrier technique, while Figure 2.5(b) shows the application of overlapping multicarrier modulation [7].

On Figure 2.6 there is an illustrative depiction of the OFDM transmitter and receiver system, encompassing the intricacies of the modulation and demodulation processes, essential for high-speed data transmission in wireless communication. OFDM employs the Inverse Fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT) to modulate and demodulate on each orthogonal subcarrier, respectively.

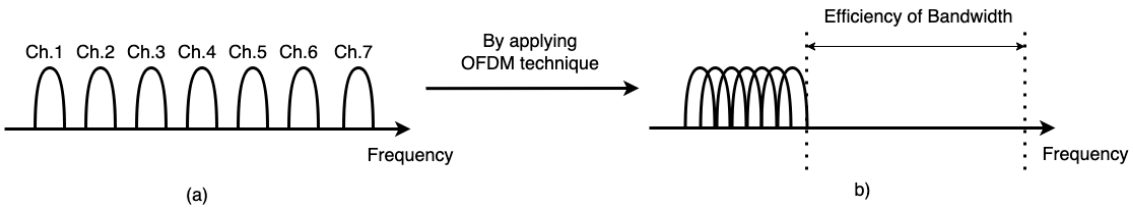



Figure 2.5: OFDM concepts (a) conventional multicarrier technique, (b) overlapping multicarrier.

The process depicted in Figure 2.6 can be described as follows, based on [9]. On the transmitter side, the process is divided as follows: 1) the input data is firstly modulated by a digital modulation scheme, which results in a complex signal, X; 2) this complex signal then passes through a Serial to Parallel Converter, resulting in N parallel symbols, X[0], X[1], . . . , X[N-1], each corresponding to the symbols transmitted over each of the N sub-carriers; 3) then, to obtain the time samples, x[0], x[1], . . . , x[N-1], of each of this discrete frequency components, it is implemented the IFFT algorithm; 4) following the IFFT, the N parallel signals x[0], x[1], . . . , x[N-1] undergo a transformation into a serial form, as opposed to what is done in step 2; 5) next, there is a crucial step of the OFDM process, the addition of the Cyclic Prefix (CP). As it was stated before, in wireless communication, signals travelling through the air can encounter multipath propagation, which results in varying delays and a phenomenon known as delay spread. The cyclic prefix is a replicated segment at the end of the OFDM symbol and functions as a guard interval. By providing time for echoes and reflections to dissipate, the cyclic prefix ensures the systems resilience to the challenges posed by multipath propagation. The duration of this surpasses the maximum excess delay encountered in the multipath propagation channel [8]. In the receiver side the inverse process is implemented.

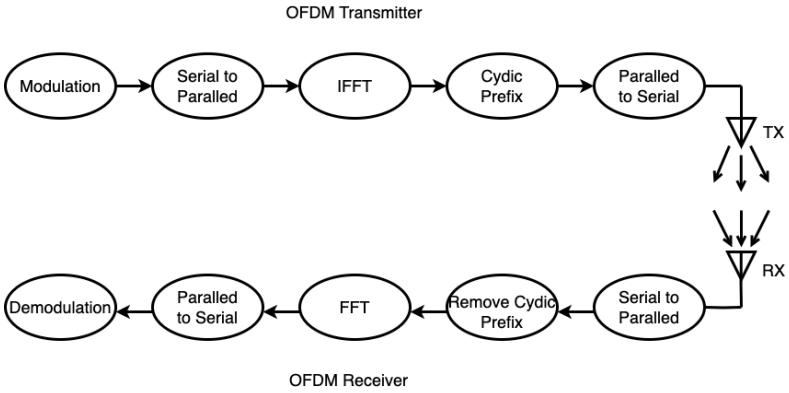



Figure 2.6: OFDM block diagram.

To end this brief descriptions of OFDM, some advantages and disadvantages will be pointed out [10]. Some of the advantages are:

1. **Resilience to Interference**: OFDM demonstrates increased resistance to the interference of the overall system, ensuring more robust data transmission.

2. **Bandwidth Efficiency**: OFDM enables efficient utilization of available bandwidth by closely spacing subchannels, allowing for the simultaneous transmission of multiple channels.

3. **Error Correction Capability**: Advanced error correction techniques can be applied to distribute overall data and compensate for small errors, contributing to the system's reliability.

4. **Correction of Multipath Effects**: OFDM can correct interference fading caused by multipath echo effects, enhancing signal quality.

5. **Guard Intervals for Multipath Mitigation**: Lower data rates on individual subchannels allow for the use of guard intervals between symbols, eliminating intersymbol interference and aiding in multipath error mitigation.

The disadvantages associated with OFDM are:

1. **Precise Transmitter and Receiver Tuning**: OFDM systems require closely tuned transmitters and receivers, demanding precise timing on signal modulators and demodulators, which can be challenging to achieve and maintain.

2. **Sensitivity to Doppler Shift**: OFDM is more sensitive to Doppler shift, making it less effective for high-speed moving vehicles.

3. **Vulnerability to I/Q Imbalance Issues**: The susceptibility of OFDM to I/Q imbalance issues underscores the importance of robust (high-performance) OFDM (digital) receivers. These receivers need to be employed with analog circuit techniques to reduce/cancel I/Q imbalance problems. Additionally, they need to include advanced Digital Signal Processing (DSP) techniques, which play a crucial role in estimating and correcting the imbalances introduced in the received signal.

### 2.1.3 N-Path Filters

In the ever-evolving landscape of wireless communication, marked by the high number of interconnected devices, addressing the challenges posed by out-of-band interferers, commonly known as blockers, and designing cost-effective RF wireless transceivers has become a critical endeavour. To strike a balance between cost reduction and enhanced performance, the on-chip integration of external components, such as filters, is deemed essential. Tackling the challenges posed by blockers (in-band, when they are generated by transmitters of the same standard or out-of-band, when created by any other standard) becomes a significant concern, drawing increased attention as the wireless landscape becomes more congested. So, in a crowded spectrum, an ideal transceiver would need to resist interference from signals at other frequencies and if possible adapt to the spectrum.

This goals can be achieved by:

- high-Q filtering capable of suppressing out-of-band interference;
- flexibility in both center frequency and Bandwidth (BW).

The need for wide frequency coverage would need the adoption of multiple filters, each meticulously designed for distinct frequency bands (e.g. in a Long Term Evolution (LTE), that can have 10 bands, it would need 10 filters [11]) which is obviously very expensive, or a highly flexible high-Q Band-Pass Filter (BPF), which is hard to do. This is why in recent years, N-Path mixers/filters have garnered attention for their full reconfigurability, allowing independent programming of bandwidth and center frequency [12]. This adaptability aligns well with the dynamic requirements of contemporary communication systems.

The fundamental concept behind N-Path filters involves down-converting the incoming signal, filtering it in the baseband (low-pass filtering), and then upconverting it back to the original frequency. This process effectively acts as a bandpass filter, allowing a specific frequency range to pass through. Although the idea of bandpass filtering through down-conversion and upconversion dates back to 1947 [13], the term 'N-Path filter' and the initial design was formally introduced later in the 1960s by researchers such as L. E. Franks and I. W. Sandberg, in their paper 'An Alternative Approach to the Realization of Network Transfer Functions: The N-Path Filter' [14]. Nevertheless, obstacles linked to these filters, such as the limited achievable switching frequency and suboptimal matching between paths (a critical factor in N-Path filter performance), resulted in a diminishing interest in research within this specific field. Due to the incorporation of components like transistors rather than mechanical switches and the integration of baseband transfer functions through capacitors or other components - which is crucial in today's context - N-Path filters have attracted renewed attention with the progress of Complementary Metal-Oxide-Semiconductor (CMOS) technology [15].

Understanding N-Path Filters behaviour in the time domain [15], particularly the interaction between clock-controlled switches and capacitors, is essential for comprehending its fundamental principles. Consider an 8-path configuration (Figure 2.7), where each path comprises, a switch controlled by the clock and a capacitor. In the case where the frequency of the input signal ($f_{\text{input}}$) aligns with the clock frequency ($f_{\text{clock}}$), Figure 2.7(a), synchronized switches open and close at intervals precisely matching the input sinusoidal signals period. This synchronization ensures that each capacitor consistently captures the same portion of the input waveform during its closing time. With the RC time constant assumed significantly larger than the switch closing time, each capacitor accumulates identical Direct Current (DC) voltages, serving as a faithful representation of the input signal. The subsequent phase involves passive mixing facilitated by the switches, acting as efficient up-converters. They transform the stored DC voltages into an approximation of

the input sinusoidal signal. This process highlights the N-Path filter's inherent capability to perform efficient up-conversion under idealized sampling conditions.

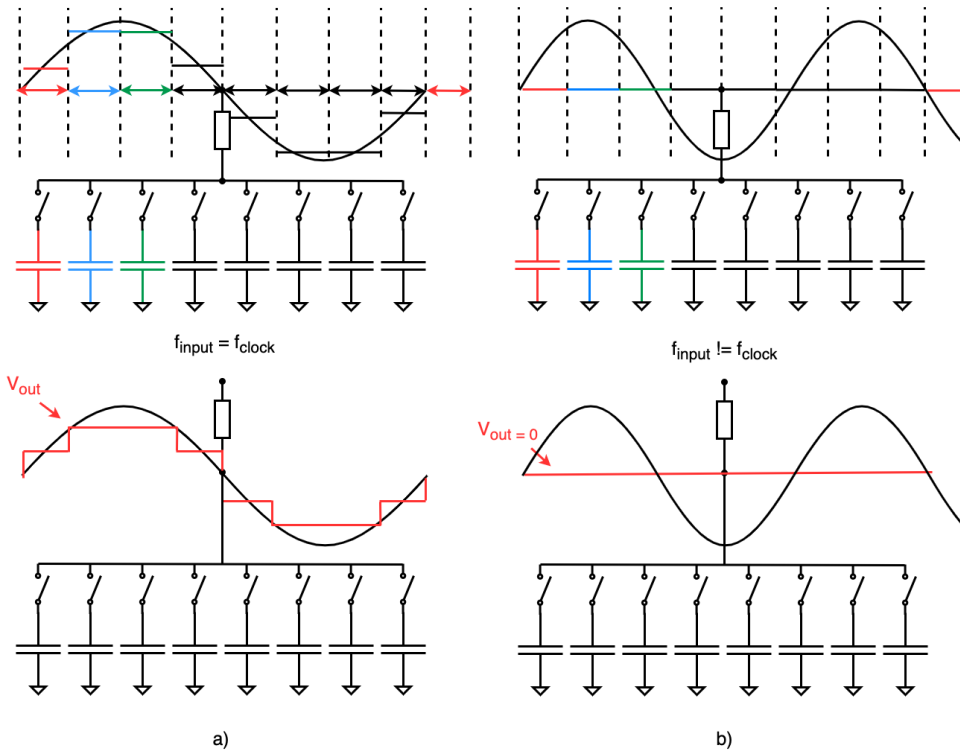



Figure 2.7: Time diagram of the voltages in an 8-path BPF with (a) equal input and clock signal frequency, (b) different input and clock frequency [13].

In contrast, Figure 2.7(b), when the frequency of the input signal deviates from the clock frequency, disrupting idealized synchronization, a different scenario unfolds. With differing frequencies, switches sample various portions of the input sinusoidal wave during their closing time. Slower charging of capacitors due to the frequency mismatch results in the over-time-average DC voltage tending towards zero after numerous settling periods. This leads to a suppression effect at the output, where sampled portions of the input sinusoidal wave, varying with the changing input frequency, do not consistently contribute to stored DC voltages. As a result, each capacitor can hold different DC values based on the average voltage of the sampled portions, leading to output variability.

In summary, under idealized sampling conditions, identical DC voltages accumulate, enabling efficient up-conversion. However, when frequencies differ, changing sampling conditions and slower charging contribute to output suppression, highlighting the N-Path filter's sensitivity to frequency dynamics in the input signal.

The core principle of an N-Path filter involves multiple signal paths, each comprising a switch made with a transistor (passive mixer) and a baseband load, as depicted in Figure 2.8.

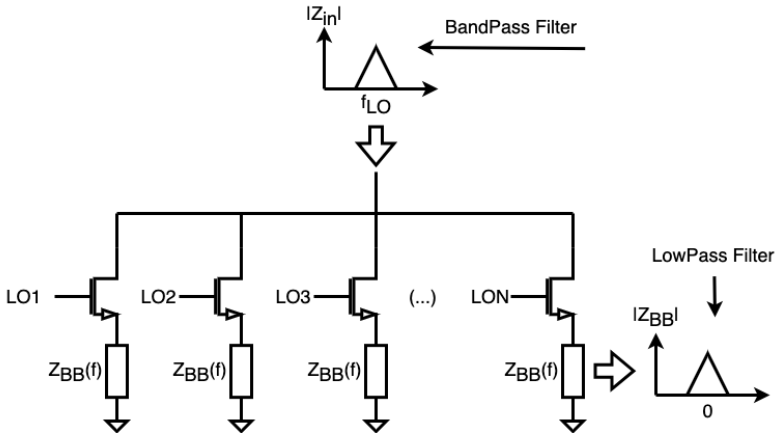



Figure 2.8: N-Path filter concept [15].

These switches, controlled by N clocks from the Local Oscillator (LO), alternate between open and closed states, allowing periodic connection and disconnection of the input signal. This controlled switching process efficiently down-converts the RF input signal to baseband. Subsequently, the baseband load, characterized by its low-pass filtering, shapes, and filters the down-converted signal, providing selective frequency response control. Following this baseband processing, the filtered signal is then up-converted back to the RF frequency through the same switches and LO control. This process is illustrated in Figure 2.9. The inherent flexibility of N-Path filters is manifested in their capacity to independently program bandwidth and center frequency, making them a versatile solution for various applications in contemporary communication systems.

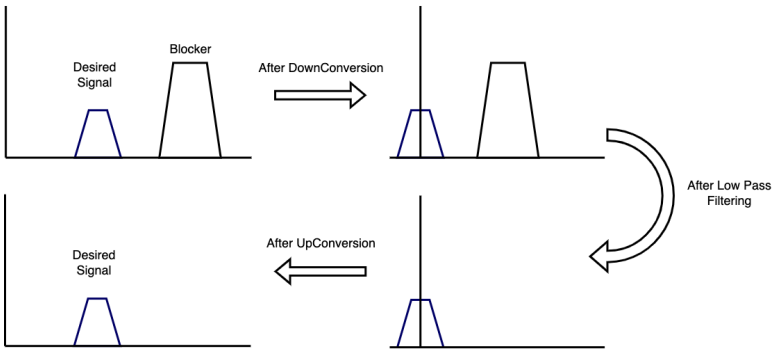



Figure 2.9: N-Path filter steps in frequency domain.

### 2.1.4 I/Q Mixing

Following the approach presented in [16] it will be explained the need for implementing the I/Q mixing. In the realm of signal processing, the transformation of RF signals to base-band is a crucial step that demands careful consideration. This process involves a mixing operation, a fundamental aspect of down-conversion, where the original RF signal is brought to a lower frequency range for subsequent processing. The choice of mixing techniques plays a pivotal role in preserving the integrity of the transmitted information.

An RF signal, denoted as r(t), can be down-converted into a baseband signal by multiplying the signal with a carrier of frequency $f_{\mathrm{LO}}$, which is the equivalent of multiplying it by $\cos(2\pi f t)$. Translating this into the frequency domain, multiplication in the time domain translates to convolution in the frequency domain, which is the equivalent of shifting the spectrum of r(t) to $f - f_{\mathrm{LO}}$ and $f + f_{\mathrm{LO}}$, also known as sidebands.

Analyzing Figure 2.10 illustrates the interference issue linked with this method. In Figure 2.10(a), when the carrier frequency matches the signal frequency, the negative-frequency image of the signal interferes with the intended signal. In Figure 2.10(b), when the desired signal frequency is higher than the carrier frequency, interference arises if there is another interfering signal below the carrier frequency. As a result, when multiplying the signal with the cosine, it leads to interference between the baseband signal and the image signal. Consequently, in both scenarios, this interference complicates the reconstruction of the original signal.

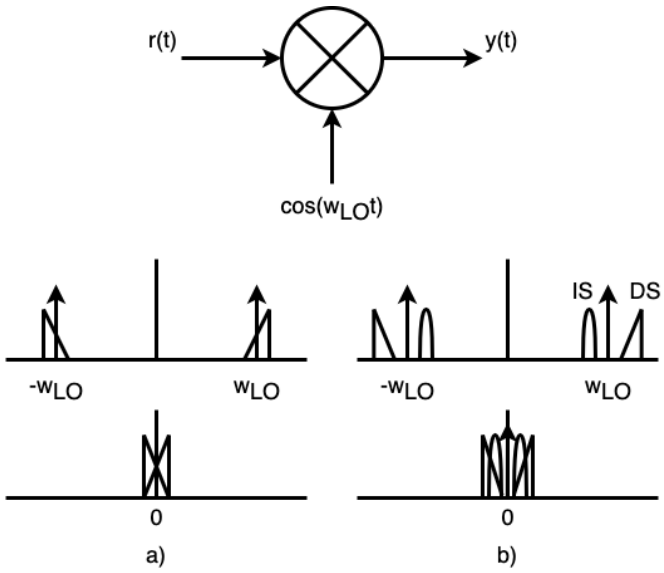



Figure 2.10: Mixing a real signal $r(t)$ with a cosine, (a) $\omega_{LO}$ equal to $\omega_{RF}$, (b) $\omega_{LO}$ different from $\omega_{RF}$ [16].

One prevalent approach to achieve this down-conversion is through the utilization of a quadrature mixing scheme, incorporating both cosine and sine functions. The motivation behind employing this complex mixing technique stems from the inherent nature of the received RF signal. The signal received at the antenna output is real valued, implying that the spectral components at negative frequencies are complex conjugates of those at positive frequencies. By engaging in complex mixing, where the signal is multiplied by both $\cos(\omega_{\mathrm{LO}} t)$ and $-j\sin(\omega_{\mathrm{LO}} t)$, a distinct advantage is gained. This method ensures that the spectral components at negative frequencies do not mirror those at positive frequencies, mitigating unwanted interference that could compromise the fidelity of the baseband signal. Complex mixing, achieved through cosine and sine components, disrupts

the symmetry between positive and negative frequency components, providing a more effective means of down-conversion.

In practical terms, a sophisticated analog front-end incorporates this quadrature mixing technique. The RF signal, represented by r(t), undergoes multiplication with $\cos(\omega_{\mathrm{LO}}t)$ and $-j\sin(\omega_{\mathrm{LO}}t)$, which results in two components $y_i(t)$ and $y_q(t)$. These components, when summed, result in the baseband equivalent, $y_(t)$, offering a faithful representation of the original RF signal. These steps are depicted in Figure 2.11.

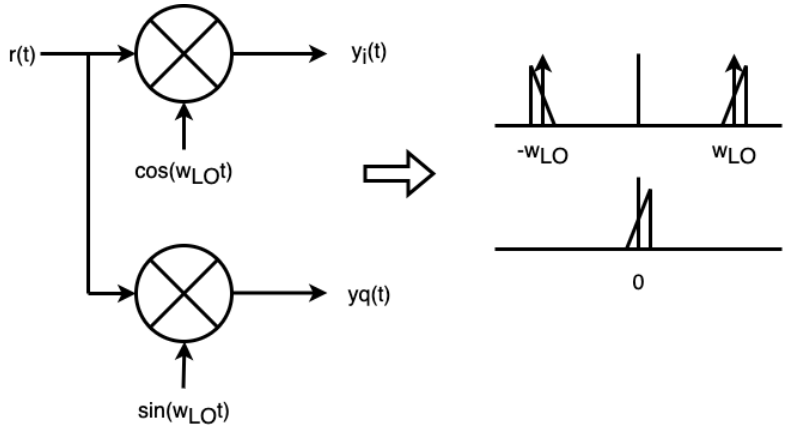



Figure 2.11: Quadrature mixing [16].

This underscores why employing quadrature mixing is important: it ensures accurate signal demodulation. This complex mixing methodology proves indispensable in scenarios where a genuine representation of the baseband signal is paramount.

### 2.1.5 I/Q Imbalance

In the process of down-converting an RF signal to the baseband, a crucial step involves complex down-conversion achieved by multiplying the RF signal with a complex waveform, typically represented as $e^{-j2\pi f_{\mathrm{LO}}}$, like it was described in the previous subsection. This complex waveform serves as the LO component in the mixing process, achieved by employing two branches - with one using the cosine component and the other the sine component of the complex waveform.

Utilizing both branches is crucial for accurately representing the real and imaginary components of the signal. This dual-branch approach ensures that the down-converted signal retains both amplitude and phase information, enabling an accurate representation of the original signal in the baseband. It is this combination of in-phase and quadrature information that forms the foundation for processing signals in complex communication systems, providing a comprehensive representation of the signal.

The down-conversion can be implemented in two ways: by shifting either the RF signal (Figure 2.12(a)) or the LO output (Figure 2.12(b)), with the latter being the more convenient option [17].

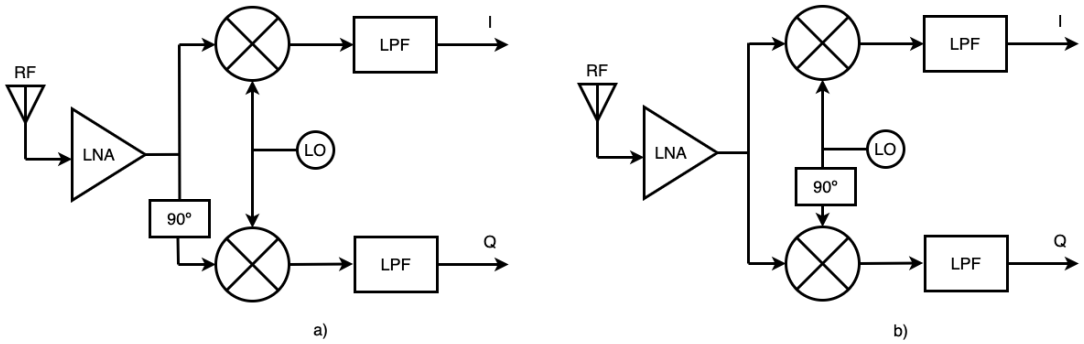



Figure 2.12: Block diagram of quadrature down conversion receiver (a) shift of RF signal, (b) shift of LO output [17].

The critical factor lies in ensuring that the gain of both the I and Q branches is precisely equal, and that the sine and cosine signals are orthogonal, i.e., their phase difference needs to be exactly 90°. Any deviation from these specified gain and phase values introduces distortion, leading to the well-known phenomenon called I/Q imbalance. The presence of I/Q imbalance has the potential to substantially degrade the performance of the system.

This requirement for a well-matched quadrature implementation poses a formidable challenge in silicon design, as achieving these orthogonal signals at radio frequencies tends to be difficult. Integrated circuit technologies, like low-cost CMOS technology, exhibit notable mismatches among components due to variations in the fabrication process. These variations include factors such as doping concentration, oxide thickness, mobility, and geometric sizes across the chip [3]. Given the sensitivity of analog circuits to these component variations, errors in the phases of LO and gains of I/Q branches are inevitable. The disparity in gain and phase is not solely confined to a singular block within each I and Q branch, as the root cause of this issue may originate from variances in the LO, mixer, or the LPFs.

This issue assumes heightened significance in OFDM schemes, where higher-order modulation is exceptionally sensitive to nonidealities at the receiver front-end. The intricate nature of OFDM setups magnifies the impact of I/Q imbalance, necessitating the development of low-complexity schemes for effective estimation and correction of I/Q imbalance [18]. Consequently, the quest for solutions to address I/Q imbalance extends beyond conventional OFDM applications, encompassing cutting-edge Non-Orthogonal Multiple Access (NOMA) systems [18]. This underscores the universal importance of mitigating I/Q imbalance in the evolving landscape of wireless communication technologies.

Examining the constellation diagrams of received signals provides a visual insight into the effects of I/Q imbalance. When there is no I/Q imbalance, all the points in the constellation present equal vertical and horizontal spacing. This arrangement of the constellation reflects the ideal scenario where the I and Q components are perfectly balanced, ensuring accurate and predictable symbol representation. However, when I/Q imbalance is introduced, this orderly grid is disrupted, and the constellation points deviate from their ideal positions, introducing distortions that affect both amplitude and phase. These distortions manifest as rotations, rotation asymmetry, or stretching along the I and Q axes, complicating the symbol detection process and impacting the overall performance of the communication system. The sources of this distortions, can be [19]:

1. **Amplitude Imbalance:** This parameter reflects the gain mismatch between the I and Q branches of the receiver. A difference in gain leads to variations in the amplitude of the received signals, causing distortions in the constellation.
2. **Phase Imbalance:** Phase mismatch between the I and Q branches introduces a rotation in the received signals, which results in shifts on the constellation points.

Figure 2.13 illustrates the ideal 16-Quadrature Amplitude Modulation (QAM) constellation diagram, where the I and Q components are perfectly balanced.

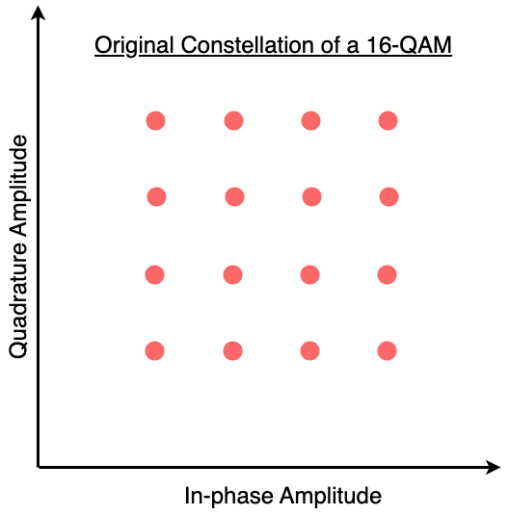



Figure 2.13: Constellation diagram of a 16-QAM signal [19].

In Figure 2.13 is the visual impact that each component of I/Q imbalance has on the constellation diagram. Through visual representation, these figures provide insights into the distortions induced by amplitude and phase imbalances, facilitating a comprehensive understanding of the effects that I/Q imbalance has on the received symbols.

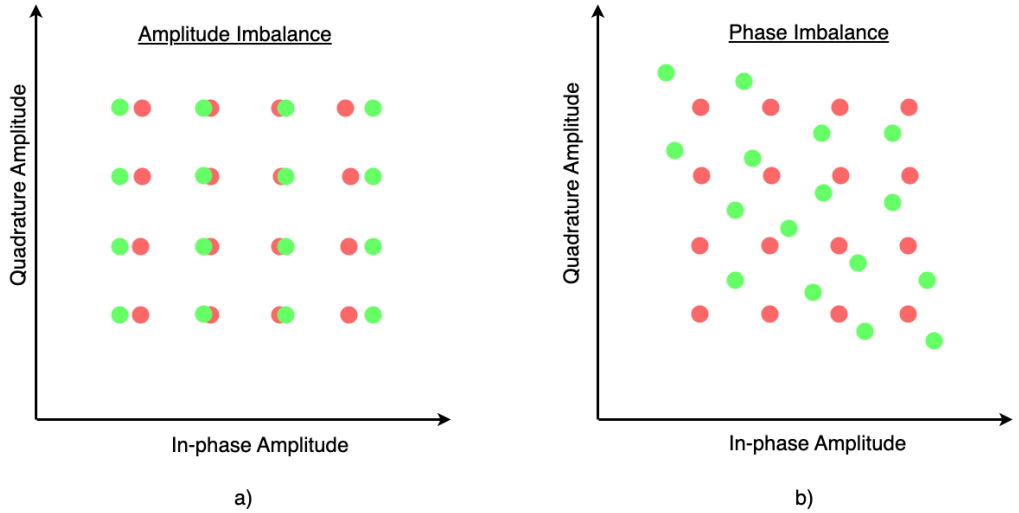



Figure 2.14: Constellation diagram errors of a 16-QAM signal (a) effect of amplitude imbalance, (b) effect of phase imbalance [19].

## 2.2 N-path Filters Literature Review

In this section, we will explore some literature related with the N-Path filters, some analyses performed on transceivers that employ passive mixers. This analyses aim to understand the impact of duty-cycle choices on performance. Additionally, it will be discussed the selection of receiver architecture, emphasising the reasons behind it. By analysing these topics, this section provides a better understanding of how these elements impact the overall performance of the receiver.

In [20], it's presented a wideband CMOS receiver front-end for radio applications operating between 300MHz and 900MHz. Both the low-noise amplifier and passive mixer incorporate N-Path signal processing techniques using a multi-phase clock to provide integrated filtering capabilities. This allows channel selection, image rejection, and attenuation of out-of-band interferers. Simulation results using a 130nm CMOS and a supply voltage of 1.2V process show the receiver achieves over 28dB voltage gain, under 6.9dB noise figure, and better than -1.54dBm Third-Order Input Intercept Point (IIP3) across the frequency band.

The key points extracted from [20], regarding N-Path filters, are the following:

- N-Path filters employ a technique that utilizes a straightforward configuration of Metal-Oxide-Semiconductor (MOS) transistors, which switch the RF current to a baseband impedance. This process transforms the originally low-pass baseband impedance (denoted as $C_{BB}$) into a high-Q bandpass filter. The center frequency of this bandpass filter is determined by the clock frequency that controls the switching of the MOS transistors. The input impedance, denoted as $Z_{RF}$, confirms this behavior,

demonstrating the conversion from a low-pass baseband impedance ($C_{BB}$) to a high-Q bandpass filter centered on the clock frequency $\omega_{LO}$.

- A notable advantage of these filters is their avoidance of flicker noise generation, thanks to their utilization of a passive circuit design.
- The performance of N-Path Filters depends highly on the number of phases and duty-cycle of the clock signal used to control the switches. Different combinations of phases (3,4) and duty-cycles ($\frac{1}{2}, \frac{1}{3}, \frac{1}{4}$) were tested to understand the optimal configuration. Simulation results showed that a 4-phase clock with $\frac{1}{4}$ duty-cycle provided the best bandpass filtering results, with high selectivity.
- Simulation also revealed that the filter exhibits diverse responses within a certain frequency range, showcasing the tunable property of N-Path Filters, influenced by the clock frequency of the LO.
- A differential version (which handles better the common-mode noise sources (e.g., substrate and supply noise) and is more immune to the clock feedthrough) of the N-Path filter was also implemented. This approach offers two advantages compared to the single-ended version. In the differential N-Path filter, the two baseband grounded impedances are replaced with a shared impedance of size $2Z_{BB}$. In the case of a capacitive baseband impedance, the two capacitors $C_{BB}$ of the single-ended version are now replaced with a capacitor of size $\frac{C_{BB}}{2}$. This leads to two advantages: 1) a reduction by a factor of 4 in the total chip area, a valuable resource in Integrated Circuit (IC) design. 2) The sharpness of the filters increases with the size of the capacitor. The fact that the total capacitor is divided between the two paths while maintaining the same value as in the single-ended version makes this type of configuration advantageous, allowing for substantial area savings while still utilizing a larger effective capacitance.

As concluded in [20], the number of phases and the duty-cycle chosen have an impact on the mixers performance. It was concluded that for best performance it was necessary to use 4 phases with ¼ duty-cycle. To better understand the reason behind this conclusion we will use [21] and [22] to find the reasons behind this choice.

The authors from [21] identified some issues with the use of a 50% duty-cycle clocks, such as:

- **Circulation of Image Currents Between I/Q Channels:** [21] pointed out that if we fed two passive mixer's, one of which has a 90° phase-shifted LO, with identical current, the RF current at the main frequency would remain the same in both mixers. However, the image components were going to be 180° out-of-phase while maintaining the same amplitude. This factor would lead to the circulation of image current between the I and Q channels. This current circulation results in a difference between high- and low-side conversion gains, as well as differences in high- and

low-side Second-Order Input Intercept Point (IIP2) and IIP3 values. Equation (25) and Figure 5 of [21], show that the conversion gain, defined as the ratio of baseband current to RF current, is unequal between the high and low sides.

- **Variations in Conversion Gain and Impact on Linearity:** The variations between conversion gain result in unequal amplification of distortion products. This variation negatively impacts the IIP3 and IIP2 values, which leads to worse performance.
- **I/Q Crosstalk and Leakage of Nonlinearities:** The lack of reverse isolation (I/Q cross-talk) causes baseband nonlinearities to leak between the I and Q channels. It was proven that despite having identical loads in both channels, the leakage of Second-Order Intermodulation (IM2) components from one channel to the other leads to constructive addition in one channel and destructive addition in the other. The presence of second-order nonlinearity, caused by random mismatches in switches and baseband loads, leads to distinct IM2 components between the I and Q channels, further degrading performance.

Following the problems encountered in [21], a comprehensive analysis on the performance of a zero-IF receiver employing current-driven passive mixers, specifically driven by 25% duty-cycle clocks, was carried out in [22]. The study highlights that mixers with a duty-cycle of 25% show superior performance compared to those with a duty-cycle of 50%. In the literature, it is recognized that employing a 25% duty-cycle enhances the down-conversion gain by 3dB, when compared to the 50% duty-cycle [1]. This improvement is attributed to the mitigation of the problems mentioned above.

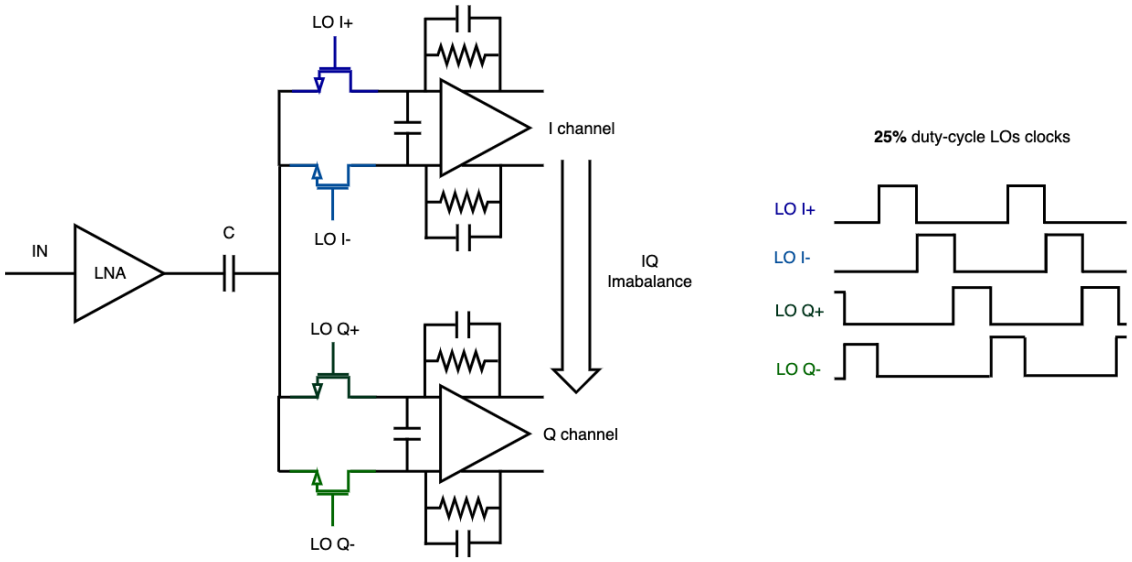



Figure 2.15: Receiver front-end with passive mixer driven by 25% duty-cycle [22].

Illustrated in Figure 2.15 is the receiver front-end with passive mixer driven by 25% duty-cycle. In the I-channel, the switches are clocked with a 25% duty cycle shift from each other, and in the Q-channel, a similar configuration is employed, having a time shift

of $\frac{T_{LO}}{4}$ from the I-channel. From this, it is implicit that during a $\frac{T_{LO}}{4}$ period, only one of the four switches is active. This operation of the switches promotes independence between the two channels, which contributes to noise reduction. Another distinction is the lack of an image component in the 25% duty-cycle mixer, which makes it more resistance to significant I/Q crosstalk, unlike the 50%.

In [22] there is an important topic that the authors explain, the property of impedance transformation. From a mathematical description in [22], the following expression for the input impedance from the RF side was derived,

$$Z_{\text{in}} \cong R_{\text{SW}} + \frac{2}{\pi^2}\left[Z_{\text{BB}}(s - j\omega_{\text{LO}}) + Z_{\text{BB}}(s + j\omega_{\text{LO}})\right]. \tag{2.1}$$

Equation (2.1) reveals that the input impedance comprises a series connection between the switch resistance and an RF impedance. There is an important property in this mixer called *impedance transformation*, that enables the mixer to transform a LPF present in the baseband impedance, into a RF domain, transforming it into a built-in high-Q bandpass filter. This property makes this structure very adequate for serving as an on-chip high-Q RF bandpass filter in various applications, including cellular receivers [22].

Some conclusions were drawn from [22], one of which was that by using a mixer with a duty-cycle of 25% instead of the 50% used in [21] solves the I/Q crosstalk by resolving the issue related to the image current, lowers the problems associated with unequal conversion gains between high- and low-side, different IIP2 and IIP3 values, the leakage problem between quadrature mixers. In [22], a significant observation about current-driven passive mixers was made, highlighting that this type of mixer exhibits superior linearity performance compared to other mixers commonly employed in receivers.

The circuit presented in this thesis is based on a mixer-first architecture, inspired by a foundational paper that demonstrated the significant advantages of this approach [23, 24]. After carefully reviewing the available design methodologies, the mixer-first architecture was the one selected due to its potential to overcome many of the limitations inherent in traditional receiver designs, like the Low-noise Amplifier (LNA)-first architecture.

Traditional receiver architectures that aim for both effective impedance matching and resilience to interference typically rely on resonant structures that are highly dependent on the operating frequency [24]. When designing receivers capable of handling multiple, widely spaced frequency bands, these conventional solutions tend to present some challenges, like significant costs in both on-chip and off-chip area. Moreover, they fall short of meeting the high-performance demands of applications such as cellular communications due to their limited ability to reject interference.

A key metric in evaluating the performance of radio receivers is the Spurious-free Dynamic Range (SFDR), which measures the range between the strongest signal that can be processed without distortion and noise of the system. SFDR essentially quantifies the

receiver's ability to handle strong signals while still accurately detecting weaker ones. The SFDR expression is given by [1],

$$\text{SFDR} = \frac{2}{3}\left[\text{IIP3} - \text{NF} + 174\,\text{dBm/Hz} - 10 \cdot \log_{10}(\text{BW})\right]. \tag{2.2}$$

To improve the SFDR, we can either improve the input-referred third order intercept point (IIP3), reduce the Noise Figure (NF), or optimize the channel BW. Given that the noise figure of the receivers is already low and the bandwidth is set by the standards, improving the linearity is the focus. Enhancing linearity is more challenging after the LNA gain stage [23], which makes the mixer-first architecture an attractive choice. By integrating a passive mixer directly into the antenna, we can achieve improved linearity - usually passive mixers tend to present > 20dB better IIP3 than LNA [25] - along with a wider tuning range, and a more power-efficient system [24].

Numerous studies have delved into the intricates of I/Q imbalance issues, recognizing their profound impact on schemes like OFDM, known for their sensitivity to such nonlinearities. The extensive research highlights the significance of addressing I/Q imbalances challenges for optimal performance in communication systems. Several research studies, such as [18, 26–29], focus on modeling, estimation, and compensation methods to improve the receivers performance, particularly for zero-IF receivers. As stated in [27], the zero-IF receiver are preferred due to their absence of intermediate stages, which facilitates the integration compared to heterodyne counterparts, as already stated.

In [27], the proposed solution for I/Q Imbalance compensation is based in OFDM training symbol. Another approach for compensating I/Q imbalance is presented in [26, 29]. The first approach were the data-aided methods, where prior information like the transmitted signals is used (e.g. training symbols), and as stated in [29], this methods are limited. Secondly, there is the blind methods, where statistical properties of the signal are utilized to compensate the I/Q imbalance, the adopted method in [29].

These previous studies focused on methods to mitigate the I/Q imbalance in the digital domain. However, it is also important to refer the analog domain, since this thesis is being developed in that domain. The analog circuits are inherently susceptible to I/Q imbalance due to the sensitivity of analog components to environmental changes and process variations. However, [18] stated that certain analog circuits, such Voltage-Controlled Oscillator (VCO) and tunable polyphase, experience less severe imbalances. Although correcting the imbalance inherent in I/Q architectures is outside the scope of this thesis, referencing these studies seemed important to highlight the existing research and solutions available for mitigating this problem.

# 3

# RF Front-End Analysis and Design

In the development of the mixer-first receiver presented in this thesis, various design decisions were made at each stage to optimize the performance and functionality of the system. Some of these choices were already introduced by the literature review in Chapter 2, where the advantages and trade-offs of different receiver architectures and components were discussed in detail. In this chapter, the key steps and decisions that shaped the final design will be described.

## 3.1 Direct-Conversion Receiver

As highlighted in Chapter 2, the Direct-Conversion Receiver (DCR) architecture was chosen primarily due to its simplicity and integration advantages. This design directly converts the Radio Frequency (RF) signal to baseband, eliminating the need for intermediate frequency stages. This approach reduces the overall circuit complexity, cost and power consumption. By operating at baseband frequencies, it causes analogue circuits to work at lower frequencies, which in turn helps to reduce the overall power consumption [30], and the compatibility with Complementary Metal-Oxide-Semiconductor (CMOS) technology allows for efficient integration and a compact design, essential for wideband applications. CMOS Integrated Circuit (IC) technology is particularly suited for realizing well-matched, highly linear oxide capacitors, while Moore's law continues to provide faster digital circuits and improved switches with lower on-resistance and parasitic capacitance [25].

Despite the positive points of DCR architectures there's also some challenges associated with it. DCR architectures face challenges related to the In-Phase (I) and Quadrature (Q) branches, particularly In-phase Quadrature (I/Q) imbalances, which can significantly impact the performance of the receiver. These imbalances arise from imperfections in the analog components, such as amplitude and phase mismatches between the I and Q paths, due to temperature changes or process discrepancies. In the context of DCR receiver, such imbalances result in distortions of the I/Q signals within the desired channel. These imbalances are particularly problematic for Orthogonal Frequency Division Multiplexing

(OFDM) systems, where higher-order modulation schemes are highly sensitive to such imperfections [18].

To investigate how much of an impact I/Q imbalances has in the performance of a receiver, a high-level model (illustrated in Figure 3.1), was employed in a 16-Quadrature Amplitude Modulation (QAM) signal, based on [19]. This model simulates the effects of various impairments within the I and Q branches, such as amplitude imbalance, phase imbalance, in-phase Direct Current (DC) offset, and quadrature DC offset. By applying these impairments, it is possible to observe their impact on the resulting constellation diagram, providing insights into how I/Q mismatches distort the signal.

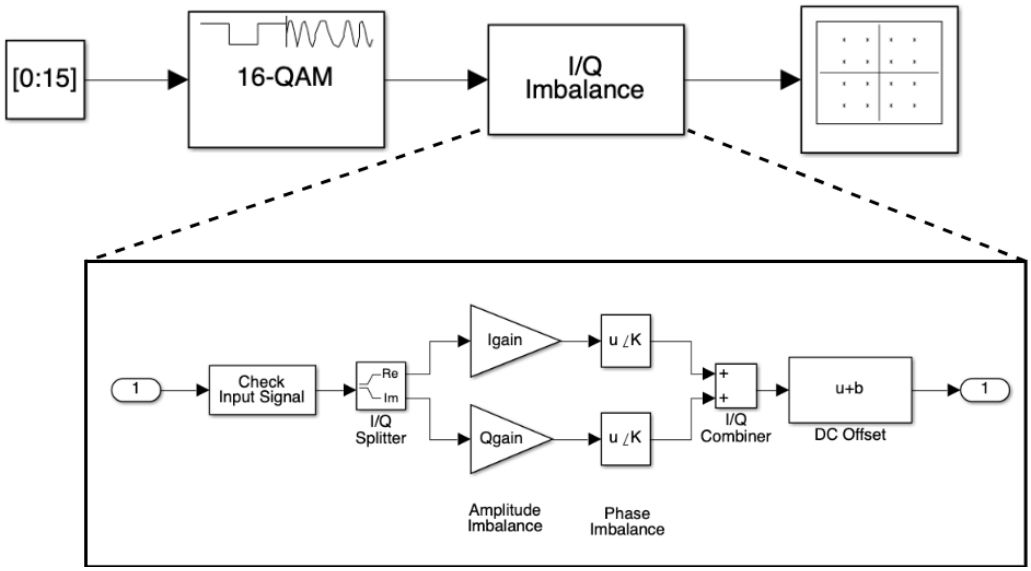



Figure 3.1: High-level model of I/Q imbalance [19].

Figure 3.2 displays the signal constellation free from any mismatches, illustrating the ideal scenario without amplitude imbalance, phase imbalance, or any other impairments in the system. Upon introducing amplitude imbalance (illustrated in Figure 3.3a), the once square-shaped constellation diagram transforms into a rectangular configuration (green dots). This alteration is indicative of the impact of amplitude imbalance on the alignment and distribution of signal samples within the constellation. For the phase imbalance impairment (Figure 3.3b). When it is introduced the previously aligned and overlaid signal samples and reference constellation points undergo notable distortions and rotations within the constellation diagram. Specifically, when observing the 16-QAM constellation with the introduction of phase imbalance, the diagram transforms from its pristine square shape to a distinctive rhombus configuration, illustrating the impact of this impairment on the overall constellation geometry.

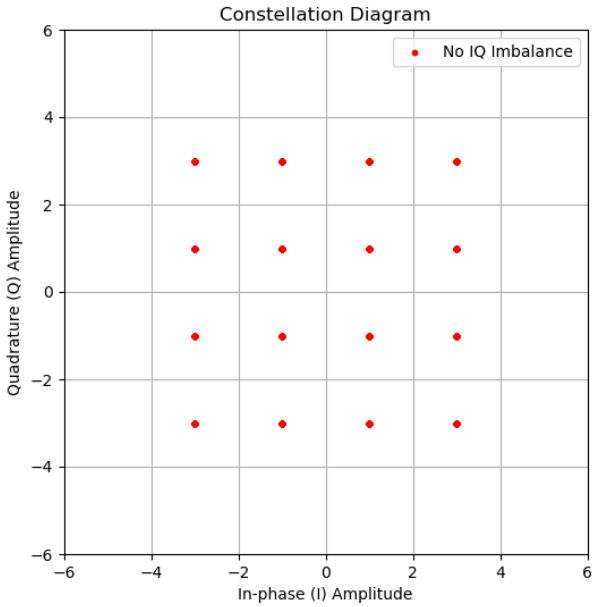
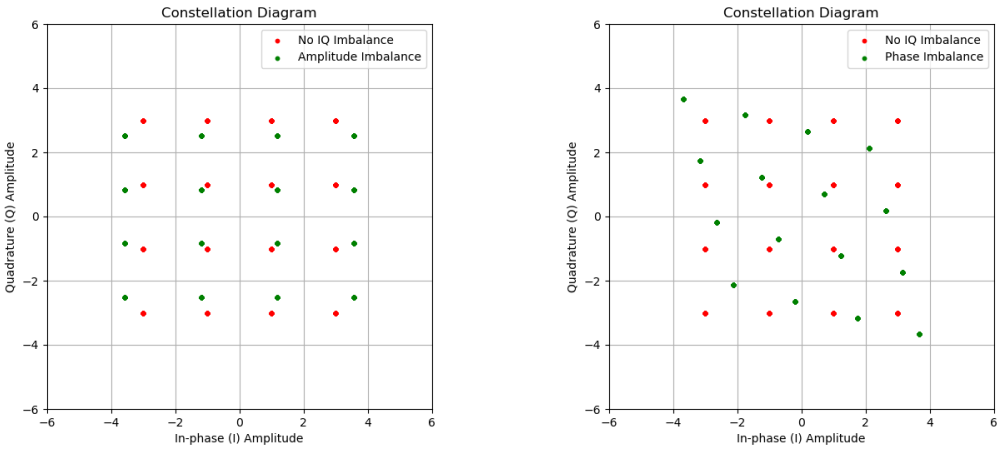


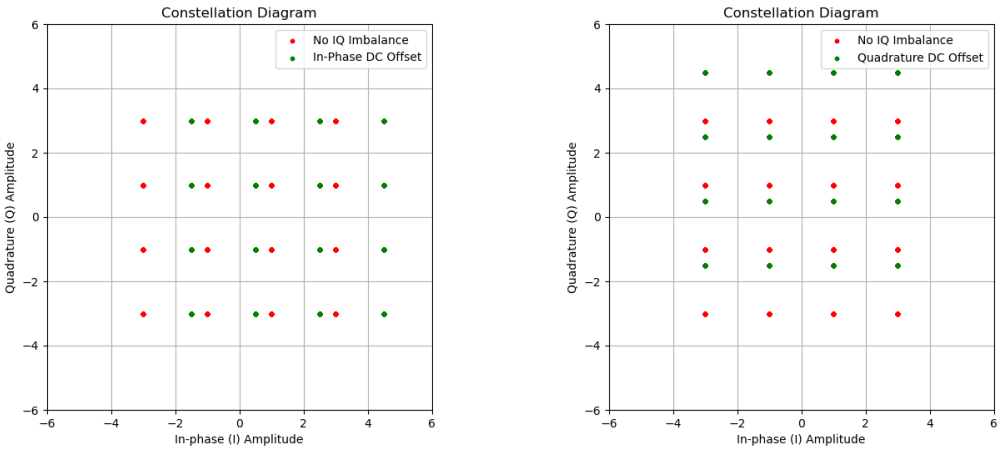

Figure 3.2: Constellation diagram for 16-QAM without any mismatch (red dots) [19].




(a) Amplitude imbalance of 3dB (green dots). (b) Phase imbalance of 30° (green dots).

Figure 3.3: Constellation diagram with amplitude and phase imbalance [19].

In Figure 3.4a, the signal constellation exclusively influenced by in-phase DC offset impairment is presented, showcasing a distinct translation of the 16-QAM constellation in the direction affected by the in-phase DC offset. When examining the signal constellation affected exclusively by quadrature DC offset impairment (Figure 3.4b), the 16-QAM constellation experiences a translation in the direction influenced by the quadrature DC offset. Similarly, in Figure 3.4a, the signal constellation exclusively influenced by in-phase DC offset impairment is presented, showcasing a distinct translation of the 16-QAM constellation in the direction affected by the in-phase DC offset.




(a) In-phase DC offset (1.5) (green dots). (b) Quadrature DC offset (1.5) (green dots).

Figure 3.4: Constellation diagram with DC offset [19].

## 3.2 Mixer-First

Following the decision to use a DCR architecture, the chosen architecture for the mixer part is to implement a mixer-first receiver architecture, as discussed in Chapter 2. In traditional receivers, a Low-noise Amplifier (LNA) is often placed at the front of the receiver chain to amplify the incoming RF signal before it reaches the mixer. However, as previously highlighted, by removing the LNA and directly connecting the mixer to the antenna, the system linearity can be improved. This is because passive mixer offer much higher linearity, with Third-Order Input Intercept Point (IIP3) values often more than 20dB higher than those of LNAs. Also, by using op-amps in the baseband stage, rather than in the RF stage, allows for even higher linearity [25]. In addition, this architecture allows for low power consumption and a wider tuning range [23].

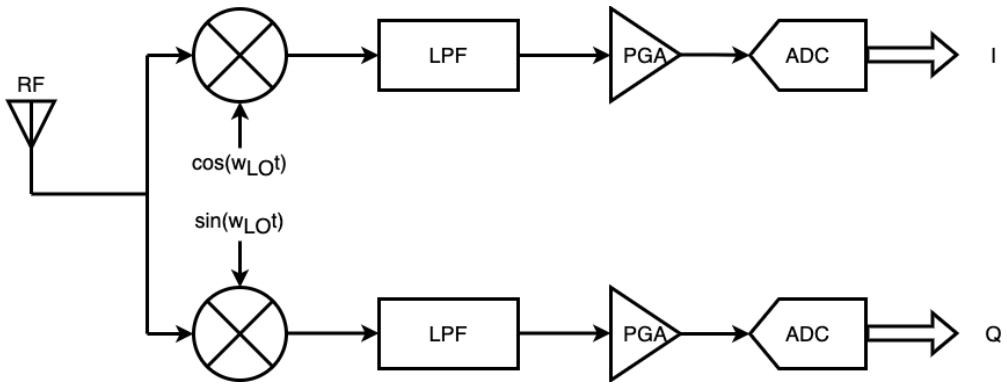



Figure 3.5: DCR with a mixer-first architecture.

## 3.3 N-Path Filter

After establishing the use of a DCR architecture with a mixer-first approach, we will now shift the attention to the key building blocks that make up the receiver. One of the most critical components in this design is the N-Path filter, which plays a dual role by functioning as both a mixer and a filter. Next, the choices and considerations made in design of the N-Path filter will be outlined, including the filter's configuration, the number of phases utilized, mostly to understand how these decisions impact the performance of this block.

In today's wireless communication landscape, two major challenges arise when dealing with interferers in crowded spectrums. First, since interferers can be as close as one or two channels away from the desired signal, extremely high selectivity is needed from the filters, with high quality values to sufficiently supress these interferers. Second, due to the dynamic allocation of carrier frequencies, it would help if the filters could have a highly precise and tunable center frequency [1], which is challenging to implement in traditional filtering methods, LC filters, Surface Acoustic Waves (SAW), and Bulk Acoustic Waves (BAW) filters. This filters provide good levels of selectivity and linearity [25], however, they have some limitations like the lack of programmability, which we now see that it can be particularly important for Software-Defined Radios (SDRs). Also, they tend to be expensive in terms of both cost and area when compared to CMOS-based solutions.

Due to the advancements on CMOS IC technology, highly programmable and integrated filters are now a viable alternative. With advancements in Moore's law, CMOS technologies now offer faster digital circuits, better low-resistance switches, and well-matched oxide capacitors, making them well-suited for implemeting N-Path filters. Additionally, the linearity offered by Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) passive mixers – which are used in N-Path filters – ensures high performance in terms of both selectivity and linearity [25]. As a result, N-Path filters are highly attractive because they offer tunable high-Q filtering, programmability, and can be integrated in CMOS technology, making them a strong alternative to traditional filters in modern wireless systems. For these reasons, the N-Path filter concept will be implemented in the receiver design.

*N-Path Filters Analysis:*

The diagram in Fig. 3.6(a) represents the fundamental structure of an N-Path filter, which is composed of several identical Linear Time-Invariant (LTI) networks. Each of these networks has a defined impulse response and is paired with two frequency mixers driven by clock signals that are phase-shifted versions of each other. The shift between paths is directly connected to the mixer clock period, which ensures proper alignment across the paths.

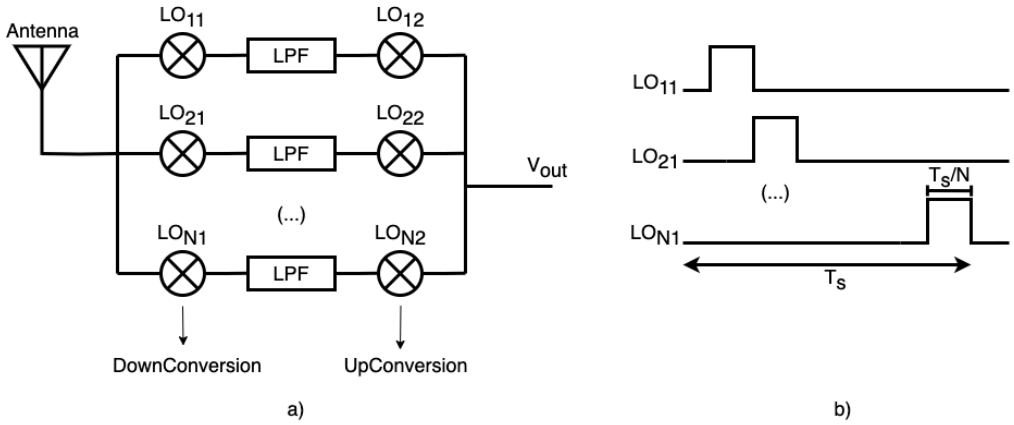



Figure 3.6: (a) N-Path general structure, (b) Polyphase clocks [31].

The operation of an N-Path band-pass filter begins with the switches, which work as passive mixers, down-converting RF input signals with frequencies near the Local Oscillator (LO) frequency. The resulting signal, now at baseband, is then low-pass filtered by the baseband capacitors. Due to the transparency property of passive mixers, this filtered signal is subsequently upconverted back to the LO frequency [15][23]. The filter's center frequency is directly determined by the mixer clock, and with a high enough mixing frequency, combined with a narrow low-pass filter bandwidth, the filter can achieve a very high Q-factor, essential for precise frequency selection. Figure 3.7 describes the stages that an N-Path filter perform.

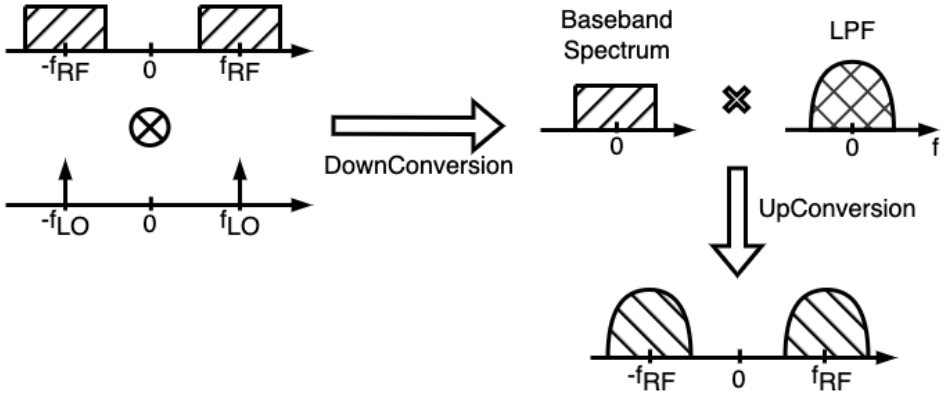



Figure 3.7: Schematic representation of the N-Path filter operation.

Ideally, N-Path filters rely on polyphase clocks to ensure non-overlapping operation between the different paths, which prevents interference between paths. Polyphase clocks mean that all clocks have the same duty-cycle and are uniformly spaced in time within the clock period, as in Figure 3.6(b) [24][32].

This gives us the starting point to address some modifications that can be made in order to simplify the N-Path filter structure from Figure 3.8(a), where the Low-Pass Filter (LPF) is now replaced by the RC time constant. As it can be seen in Figure 3.8(a), the

resistance R appears in all paths, and as resistors are a memory-less element [31], these two observation lead to a simplification of this circuit into the structure in Figure 3.8(b). Now, from Figure 3.8(b) we see that in each path there is two sets of switches, if this two switches were controlled by identical clocks, we can turn this circuit into a simplified one, Figure 3.8(c), turning $V_{out}$ into both input and output port. This simpler approach of the circuit results in a single-port Single-Ended (SE) N-Path Filter, also known as Polyphase SE kernel in the literature.

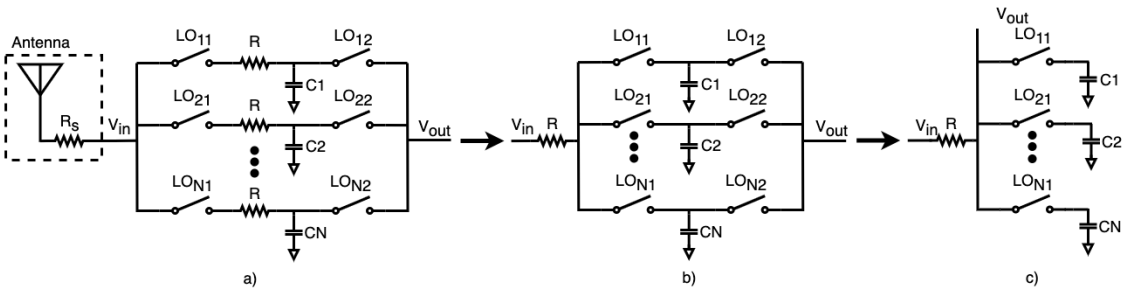



Figure 3.8: Simplification process of the N-Path architecture [13].

A problem arrives from this single-balanced mixer, that is the fact that near the harmonics of the clock we'll have signals with non-zero values, which we don't want it to happen. If instead of using, for example, the 4-path filter in Figure 3.9(a), if we use the differential version illustrated in Figure 3.9(b) two key challenges present in the single-balanced architecture can be solved: the elimination of LO-Intermediate Frequency (IF) feedthrough, and the elimination of even harmonics.

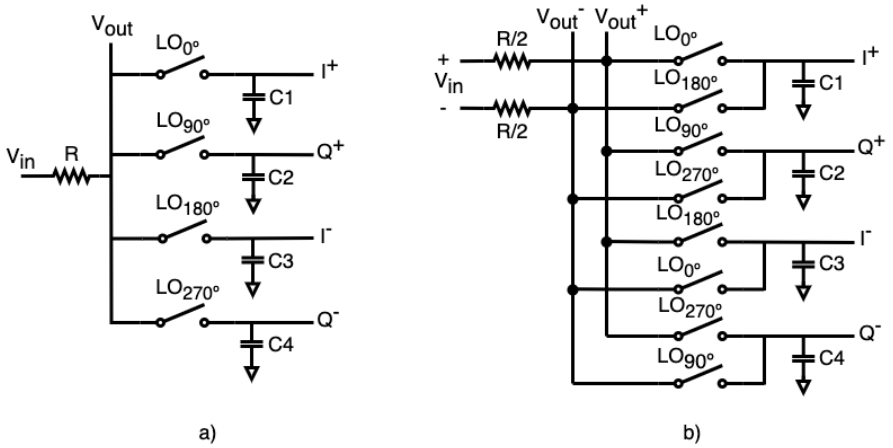



Figure 3.9: 4-Path (a) Single port SE filter, (b) Single port differential filter [25].

In passive mixers, the switching operation is typically performed by MOSFETs, as illustrated in Figure 3.10(b). In pratical implementations, each MOSFET exhibits parasitic capacitances, such as gate-source capacitance ($C_{gs}$) and gate-drain capacitance ($C_{gd}$). These parasitic capacitances create unwanted coupling between the RF, LO, and IF (with the IF port corresponding to the baseband signal in a DCR), as depicted in Figure 3.10(a).

This unwanted coupling leads to the feedthrough problem, where a portion of the LO signal leaks into the other ports, particularly talking here in the IF port. In single-balanced mixers, this issue is significant. While these mixers use balanced LO waveforms (LO+ and LO-) to drive the switches, they still rely on a single-ended RF input and generate differential baseband outputs. The problem arises because, due to the parasitic capacitances, the LO signal is capacitively coupled to the IF output, creating what is know as LO-IF feedthrough.

In a single-balanced mixer, the feedthrough isn't perfectly canceled because of the asymmetry in the circuit. Specifically, the LO signal leaks to both differential output in opposite phases (e.g., +$\alpha$VLO and -$\alpha$VLO). However, instead of canceling each other, these leakage components add up, resulting in LO leakage at the IF port equal to 2$\alpha$VLO [pg. 348][1].

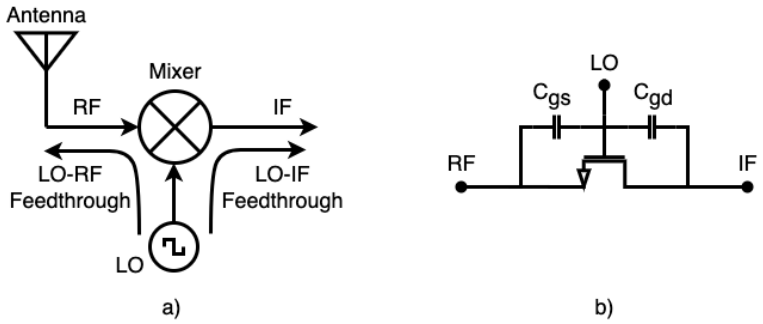



Figure 3.10: (a) Feedthrough in a mixer, (b) Parasitic Capacitances in a MOS mixer [1].

In contrast to the single-balanced mixer, the double-balanced mixer – illustrated in Figure 3.9(b) – is able to minimise or even eliminate the LO-IF feedthrough. In this architecture, both the LO and RF signal are applied differentially, which ensures that the LO leakage at the output is either minimised or entirely eliminated.

In a double-balanced mixer, the LO leaks equally but in opposite phases to the two output nodes. For instance [1]:

- At the output node $V_{\text{out}}^{+}$, the LO leakage is represented as $2\alpha V_{\text{LO}}$;
- Also, at the output $V_{\text{out}}^{-}$, the LO leakage is $2\alpha V_{\text{LO}}$.

Since the output is the difference between these two nodes, the LO leakage cancels out as we have $V_{\text{out}}^{+} - V_{\text{out}}^{-} = 2\alpha V_{\text{LO}} - 2\alpha V_{\text{LO}} = 0$. Importantly saying is that the double-balanced mixer preserves the desired baseband signal without canceling it out. The differential behaviour ensures that [1]:

1. When $V_{LO}$ is high, $V_{\text{out}}^{+} = V_{\text{RF}}^{+}$ and $V_{\text{out}}^{-} = V_{\text{RF}}^{-}$;
2. When $\overline{V_{LO}}$ is high, $V_{\text{out}}^{+} = V_{\text{RF}}^{-}$ and $V_{\text{out}}^{-} = V_{\text{RF}}^{+}$.

Thus, the differential output remains as follows:

- For high LO, $V^+_{out} - V^-_{out} = V^+_{RF} - V^-_{RF}$;
- For low LO, $V^+_{out} - V^-_{out} = V^-_{RF} - V^+_{RF}$.

Meaning that this architecture ensures that the output reflects the correct downconversion signal without interference from LO feedthrough.

Now, let's analyse the impact of the single-balanced and double-balanced mixers on the filter transfer function. For this analysis, let's assume ideal switching (ideal switches), which implies that the switching occurs instantaneously, and effects of the switch resistance are not considered in this stage, it will be a topic to discuss later on. For now, the focus will be on the filter response in both single-balanced and double-balanced mixer configurations. For that we consider the 4-path filter similarly to the one on Figure 3.9(a), with $f_s = 500\ MHz$.

The filter response for this configuration is represented in Figure 3.11. With this we can make two observations:

1. The BPF has it's center frequency aligned with the switching frequency, $f_s = 500\ MHz$;
2. The harmonics of the filter appears at $2f_s, 3f_s, \ldots, nf_s$.

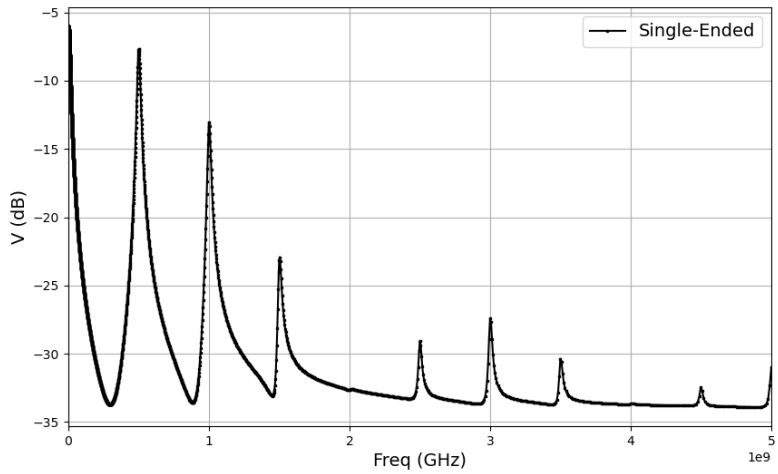



Figure 3.11: Single-port, single-ended 4-path filter transfer function at $f_s = 500\ MHz$ [31].

Now, if we use the filter of Figure 3.9(b), i.e, the differential approach, with the same switching frequency, the filter response changes to the one in Figure 3.12. Now from here we take also take two observations:

1. The bandpass filter continues to be centered at the switching frequency, $f_s$;
2. The even harmonics of the filter $2f_s, 4f_s, \ldots, nf_s$ were eliminated.

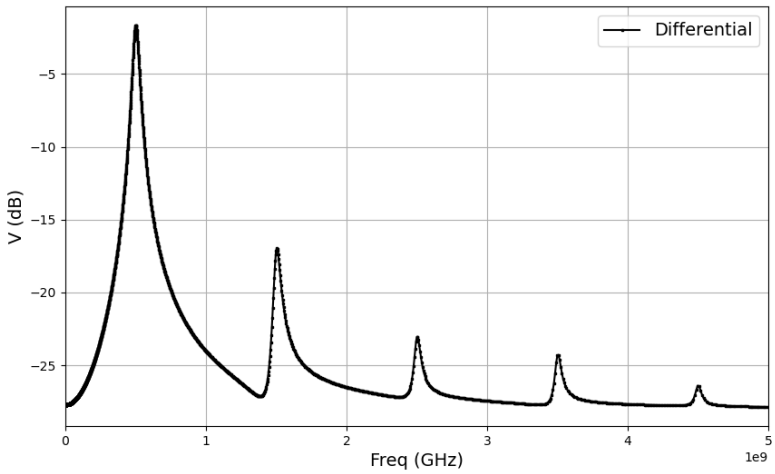



Figure 3.12: Differential 4-path filter transfer function at $f_s = 500\ MHz$ [31].

This validates what was said earlier, the differential architecture effectively eliminated even harmonic of the switching frequency, further validating the accuracy and advantages of the design.

Now that the rationale behind choosing the differential approach has been explained, we will proceed with a more detailed analysis of the architecture. This will help to gain a deeper understanding of how N-Path filters operate and identify the key intrinsic characteristics that need to be addressed to enhance their performane.

Another important consideration in the study of N-Path filters is the issue known as harmonic folding back. This problem arises when harmonics of the switching frequency fold back into the filter's passband, potentially causing distortion and interference. This issue has been examined in [25, 31]. It was stated in these papers that the frequencies responsible for causing harmonics folding back into the desired passband are typically around $(N \pm 1)f_s$. This means that for a 4-path filter, the closest folding back occurs with $3f_s$ and $5f_s$ harmonics, and for a 8-path filter occurs at $7f_s$. This led to the conclusion that increasing N results in better performance because it means that the harmonics that cause folding back into the filter band are further away from the filter's center frequency. However, this also means increasing the complexity of the architecture. But there's another point worth thinking about: the authors pointed out that to suppress these harmonics we could use a low-pass pre-filter whose requirements increase when the folding harmonics occur closer to the $f_s$ frequency. In other words, here we have a compromise between the complexity of the pre-filter and the N-Path filter. If we increase the number of paths, we relax the requirements for the pre-filter transition band, and vice-versa.

Contrarly to what was implemented in the circuit that derived Figure 3.9(a) and (b), the switches in the N-Path filter are implemented using CMOS transistors, which means that the inherent resistance of these transistors must be considered, as in Figure 3.13.

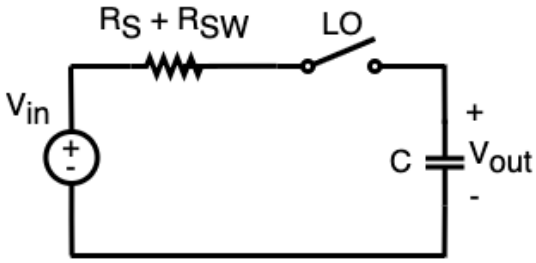



Figure 3.13: Single-ended kernel considering the switch resistance [24].

In [31], equation (14) was derived to analyse the impact of the switch resistance on the filter's transfer funciton, specially focusing on the spectral shaping of the main harmonic component ($n = 0$).

$$H_{0,SW}(f) = \frac{2R_{SW}}{R_S + 2R_{SW}} + \frac{R_S}{R_S + 2R_{SW}} H_0(f). \tag{3.1}$$

From the expression in 3.1, some conclusions can be drawn about the impact of the switch resistance on the frequency response:

1. For frequencies near the switching frequency, the switch resistance doesn't have that big of an impact, as $H_0$ its aproximately equal to 1 meaning that it's the dominant term;
2. Rather, for more distant frequencies, the term $H_0$ is now close to zero, which makes the first term of (14) the dominant one. Consequently, the output expression is equal to $V_{out}(f) = \frac{2R_{SW}}{R_S+2R_{SW}}.V_{in}(f)$. From here a conclusion was reached: the filter's maximum rejection capability is ultimately constrained by the resistance of the switches, as can be seen in Figure 3.14. This figure confirms that with higher values of $R_{SW}$ the attenuation of frequencies outside the filter band gets worse, while within the band the attenuation remains the same as if the resistance were zero.

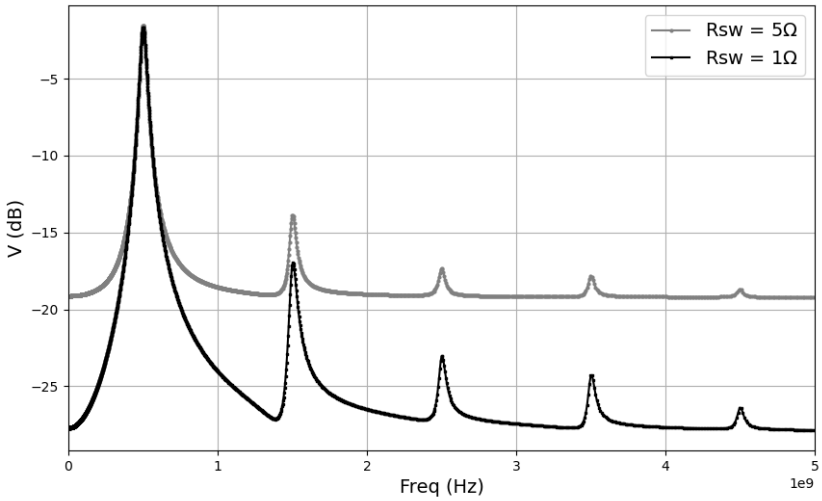



Figure 3.14: Effect of the switch resistance on the transfer function [31].

This helps us realise that in order to achieve significant attenuation of frequencies outside the filter's passband, the switch resistance $R_{SW}$ must be kept relatively low compared to the source resistance $R_S$. This ensures that, at frequencies far from $f_s$, the first term of equation (14) remains minimal, enhancing out-of-band rejection.

As per the capacitance effect, selecting the appropriate value is also a concern that must be carefully considered due to its impact in determining the filter's performance, especially regarding its bandwidth and selectivity. As the $-3dB$ bandwidth, $f_{-3dB}$, can be approximated by the expression [25],

$$f_{-3dB} = \frac{1}{\pi NRC}, \tag{3.2}$$

where $N$ is the number of paths, $R$ is equal to the sum of the switch resistance and the source resistance (50 Ω), and $C$ is the capacitance value.

If we recall the expression that represents the quality factor of a filter, $Q = f_s/BW$, and and relate it to the $-3\ dB$ bandwidth expression we have,

$$Q = \frac{f_s}{f_{-3dB}} = \pi NRCf_s, \tag{3.3}$$

where $f_s$ is the switching frequency. From this we realise that in terms of selectivity, a higher capacitance value provides better filtering of unwanted frequencies, as a narrower bandwidth reduces the range of frequencies that can pass through the filter [33]. This is demonstrated in Figure 3.15, where a higher capacitance value of 100 $pF$ results in a significantly improved quality factor when compared with a lower capacitance value of 20 $pF$.

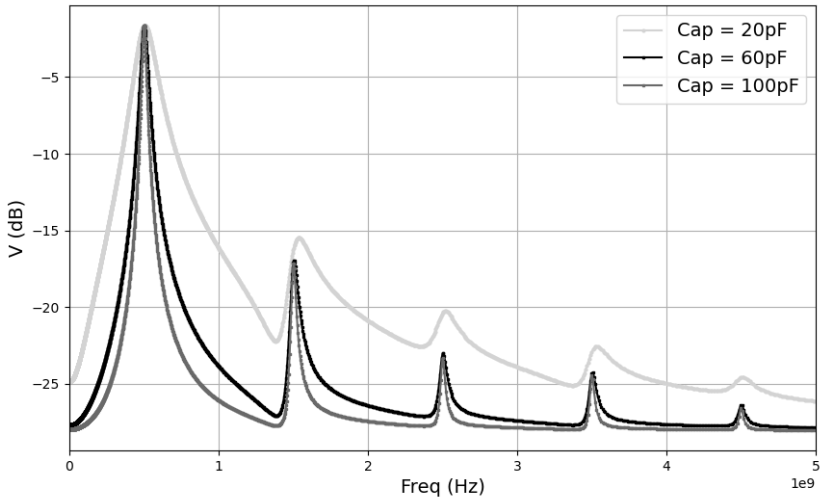



Figure 3.15: Effect of the capacitance value on the transfer function [31].

Another important point to analyse is the harmonic attenuation in N-Path filters. In [31], equation (15) was derived to provide a mathematical expression that allowed to

quantify the insertion loss on the harmonics of the switching frequency.

$$H_0(nf_s) \approx \frac{2N(1-cos(2\pi D))}{4D(n\pi)^2} + (1-ND), \quad 0 \leq D \leq 1/N. \tag{3.4}$$

From equation 3.4, it was concluded that in order to increase the insertion loss at the harmonics of the switching frequency, the number of paths, $N$, in the filter must be reduced. As shown in Figure 10(a) of [31], with $N = 8$, the insertion loss at the odd harmonics is worse compared to $N = 4$, while at the switching frequency, the insertion loss remains the same. Figure 10(b) on [31] further illustrates this point, demonstrating that the attenuation for $N = 10$ is significantly less than for lower values, such as $N = 4$.

If we recall the conclusion from the folding back discussion, it was noted that increasing $N$ helps reduce the issue of harmonics folding back into the filter's passband. However, this brings us to a critical point because:

- In order to have less folding problem a larger $N$ should be used;
- In order to have higher insertion loss on harmonic of the filter a smaller $N$ should be used.

In view of this, it is necessary to compromise on one of the issues: either we improve the folding back or the attenuation. The chosen approach was to implement an N-Path with N = 4, in order to achieve more harmonic attenuation. To supress the folding back problem, a pre-filter could be used to supress the harmonic that, in a 4-path configuration, are closer to the switching frequency. However, the design of this pre-filter it's outside the scope of my study and will not be included.

In the process of determining the optimal duty cycle for the N-Path filter, several papers were reviewed that provided key insights. Paper [32] emphasised the need for a minimum of three polyphase paths to achieve image rejection, but noted that a 4-path system ($L = 4$) is typically preferred for demodulation purposes because it provides I/Q outputs. This same paper showed an optimum noise figure around a 40% duty cycle, but highlighted that 25% was chosen to avoid switch overlap, which aligns with typical design constraints for such systems.

Another source [34] focusing on Quadrature Sampling Mixers (QSM) confirmed that a 25% duty cycle is the maximum possible without overlap between switches, ensuring even-order cancellation and image rejection.

Further analysis conducted on [31] stated that reducing the duty cycle below 25%, referred as the ideal case, increased input impedance at frequencies distant from the switching frequency, leading to decreased rejection of out-of-band signals. However, it was also noted that smaller duty cycles could reduce pass-band insertion loss, which is not the scenario we want. Despite this, the trade-off in rejection quality made the 25% duty cycle the preferred option.

In the study presented in [31], the impact of having a duty cycle $D \geq (1/N)$ was explored. This scenario allows for multiple switches to be in the "on" state simultaneously, which leads to undesirable interactions between capacitors. As demonstrated in Fig. 11(a) on [31], when using a duty cycle of D = 30% (with two scenarios for switch resistance: 1) $R_{SW} = 0$ and 2) $R_{SW} \neq 0$), the filter response is significantly compromised. This illustrates that such a duty cycle can severely degrade the filter's performance.

In summary, while there were some variations in optimum noise figures and insertion losses at slightly different duty cycles, all sources converged on the fact that a 25% duty cycle provides the best balance between avoiding switch overlap, achieving high image rejection, and maintaining good pass-band performance.

Previously, the impact if I/Q imbalance in DCR was analysed using a MatLab model. Since N-Path filters also feature an I/Q architecture, it's important to revisit this topic to understand how I/Q imbalance affects their performance similarly.

In [31], it was examined the effects of mismatches between the paths or deviations in clocking signals from the ideal case in N-Path filters. These mismatches can disrupt the cancellation of even-order terms, leading to unwanted frequency components. By analysing the sources of these mismatches, they wanted to understand how imperfections in the filter design - like differences in path characteristics or timing inaccuracies - contribute to performance degradation, including the potential for I/Q imbalance. This imbalance could occur if the I and Q paths are not perfectly aligned, causing signal distortions.

Also, [31] examines the impact of clock pulse width variations in multiphase clocks on the performance of N-Path filters. These variations deviate from the ideal case where each clock pulse has the same width and phase alignment. By introducing unequal pulse widths and applying the filter model, the researchers calculated the effects on image suppression and second harmonic folding. Their findings, illustrated in Figure 14, revealed that even a small phase error of one degree leads to a significant degradation in performance, with 42 dB of image rejection and 45 dB of second harmonic suppression. This demonstrates the sensitivity of N-Path filters to clocking mismatches, underscoring the importance of precise timing to maintain filter effectiveness.

## 3.4 Amplification Stage

As previously mentioned the mixer used in receiver chain acts as a passive mixer, which means that instead of giving gain to the input signal it attenuates it. For that reason, as the output signals of the receiver will be used in Analog-to-Digital Converters (ADCs) it is crucial to implement an amplification stage to recover the signal strength. Two amplifiers were considered: a negative feedback amplifier with single-ended input/output and a tradicional two-stage differential amplifier with a single-ended output, both being voltage amplifiers as the output of the mixer it's a voltage signal.

### 3.4.1 Negative Feedback Amplifier

The first option considered was the non-inverting feedback amplifier shown in Figure 3.16. This amplifier consists of a feedback network composed by the resistors $R_s$ and $R_f$ and a single-stage Operational Amplifier (OpAmp). The OpAmp consists of a NMOS (M1) Common-Source (CS) stage with a current-source load (M2), followed by a PMOS CS stage that drives the feedback network back to the NMOS. The CS stage is commonly used in amplifier designs when high voltage gain is needed in a single-stage configuration [35].

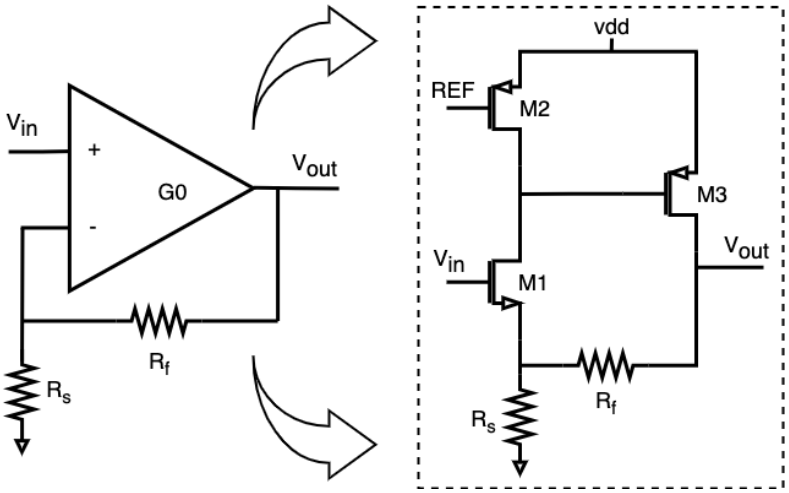



Figure 3.16: Negative feedback amplifier schematic [34].

In amplifiers, negative feedback is generally preferred over positive feedback due to its stabilizing effects and other performance benefits. The CS stage of M1 tends to be sensitive because its gain, determined by $gm_1ro_1$, is influenced by variations in process and temperature. By applying negative feedback, the closed loop gain of the amplifier becomes more independet of these variations in transistor parameters. However, a trade-off arises: while negative feedback improves stability, which is essential in amplifier designs, it requires an increase in the feedback factor. This, in turn, reduces the overall gain [35].

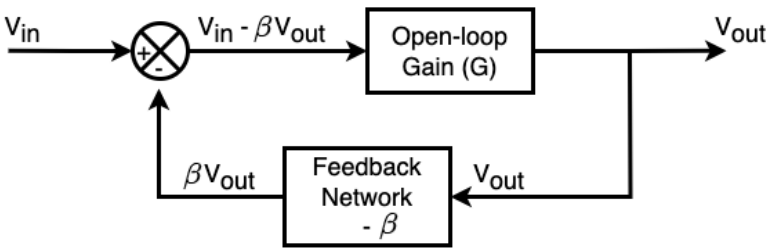



Figure 3.17: Feedback network.

The closed-loop of a feedback amplifier (Figure 3.17) can be expressed as:

$$\begin{aligned} V_{in} = V_{in} - \beta V_{out} \rightarrow V_{out} &= G(V_{in} - \beta V_{out}) \\ &= GV_{in} - \beta G V_{out} \\ &= V_{out} \\ &= GV_{in} = V_{out}(1 + \beta G) \\ &= \frac{\mathbf{V_{out}}}{\mathbf{V_{in}}} = \mathbf{G_v} = \frac{\mathbf{G}}{\mathbf{1} + \beta \mathbf{G}}, \end{aligned} \tag{3.5}$$

, where $G_v$ is the closed loop gain, $G$ the open loop gain, and $\beta$ the feedback factor.

Assuming $\beta G \gg 1$, which is desirable to improve stability ($\beta \gg$), the closed loop simplifies to,

$$\beta G \gg 1 \rightarrow G_v \approx \frac{G}{\beta G} = \frac{1}{\beta}. \tag{3.6}$$

This shows that as the feedback factor increases, the closed-loop gain decreases, which highlights the trade-off between stability and gain described above.

To derive the gain voltage equation of this amplifier, the small-signal model, shown in Figure 3.18, must be introduced. In the small-signal analysis, transistor M2 behaves like a resistor, since in Alternating Current (AC) analysis, DC voltages are treated as ground. This effectively places M2 in a diode-connected configuration, meaning that in the small-signal model it is equivalent to $r_{ds2}$.

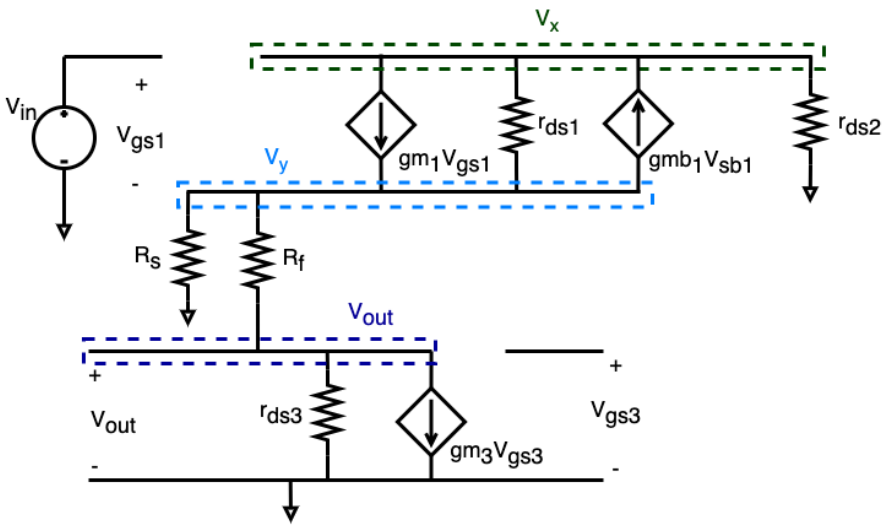



Figure 3.18: Small signal model of single-stage amplifier.

Analyzing this, we derive the following three equations from the nodes ($V_x$, $V_y$ and $V_{out}$) highlighted in Figure 3.18.

$$\text{Node } V_{out}: \quad \frac{V_{out}}{r_{ds3}} + g_{m3} \cdot V_x + \frac{V_{out} - V_y}{R_f} = 0 \tag{3.7}$$

$$\text{Node } V_y: \quad \frac{V_y}{R_s} + \frac{V_y - V_{out}}{R_f} - g_{m0} \cdot (V_{in} - V_y) + g_{mb0} \cdot (V_y - 0) + \frac{V_y - V_x}{r_{ds0}} = 0 \tag{3.8}$$

$$\text{Node } V_x: \quad g_{m0} \cdot (V_{in} - V_y) - g_{mb0} \cdot (V_y - 0) + \frac{V_x - V_y}{r_{ds0}} + \frac{V_x}{r_{ds1}} = 0 \tag{3.9}$$

By solving this system of three equations in order to $V_{out}/V_{in}$, we obtain the close-loop gain expression shown in (3.10).

$$\frac{V_{out}}{V_{in}} = \frac{g_{m_0} \cdot r_{ds_0} \cdot r_{ds_3} \cdot (R_s + g_{m_3} \cdot r_{ds_1} \cdot (R_f + R_s))}{(r_{ds_0} + r_{ds_1}) \cdot (r_{ds_3} + R_f) + r_{ds_0} + r_{ds_1} + r_{ds_3} + g_{m_3} \cdot r_{ds_1} \cdot r_{ds_3} + R_f + g_{m_0} + g_{mb_0} \cdot r_{ds_0} \cdot (r_{ds_3} + g_{m_3} \cdot r_{ds_1} \cdot r_{ds_3} + R_f) \cdot R_s} \tag{3.10}$$

The decision to use a second option was driven by more than one reason, being one of them, the fact that the first amplifier has a single-ended input. Since the mixer output produces four differential signals – $I^+$, $I^-$, $Q^+$, $Q^-$ - using the first amplifier would require four separate amplifiers to handle each signal individually, which would result in four amplified outputs. In contrast, the second amplifier option provides two advantageous, it amplifies the incoming signal like the first one, but it also converts the differential input signals ($I^+$, $I^-$, $Q^+$, $Q^-$) into two single-ended outputs – I and Q – which simplifies the design. This dual functionality of amplification and differential-to-single-ended conversion, along with the inherent advantageous of using a differential amplifier (such as improved noise rejection, higher voltage swings, a better supression of common-mode signals, even harmonics cancellation, and higher gain) [35], made the second amplifier the preferred choice for the amplification stage in the receiver chain. Also, as the architecture works as a mixer-first, the amplification from the LNA doesn't exist, which means that not only is the received signal relatively weak, but is also further attenuated by the mixer. Therefore, it is crucial that the amplifier stage provides sufficient gain to ensure that the signal at the receiver's output is strong enough for reliable processing.

### 3.4.2 Two-stage Amplifier

The two-stage OpAmp (Figure 3.19) is composed of two key stages: a differential amplifier (first stage) and a CS amplifier (second stage). The following sections describe each stage and its functions.

1. Differential Amplifier Stage (M1, M2, M3, M4, M5):
    - M1 and M2 form the differential pair at the input of the amplifier. These transistors process the differential input signals and convert them into a differential

output current. The advantageous of using a differential input is that it improves the common-mode noise rejection and doubles the gain compared to the single-ended inputs.

- M3 and M4 acts as a current mirror, which serves two purposes: 1) ensures that the differential current generated by M1 and M2 is converted into a single-ended ouput; 2) helps maintain the gain advantageous of the differential input stage by ensuring that both transistors operate in balance, doubling the effective gain.
- M5 serves as a current source to bias the differential pair (M1 and M2). Using M5 as a transistor-based current source (rather than a simple resistor) ensures: 1) High impedance at the drain of M1 and M2, improving the gain; 2) A constant bias current, which stabilizes the operating point of M1 and M2 regardless of voltage fluctuations or temperature changes.

2. CS Amplifier Stage (M6, M7):
   - The second stage of the OpAmp is a common-source amplifier formed by M6, with M7 acting as it current source load. This stage provides additional gain and amplifies the single-ended output from the first stage;
   - Like the first stage, M6 is biased with a current source (M7) to ensure stable operation and high gain.
3. Biasing (M8):
   - M8 provides the biasing voltage for both current sources, M5 and M7, ensuring that they deliver a stable current to the differential and common-source stages.

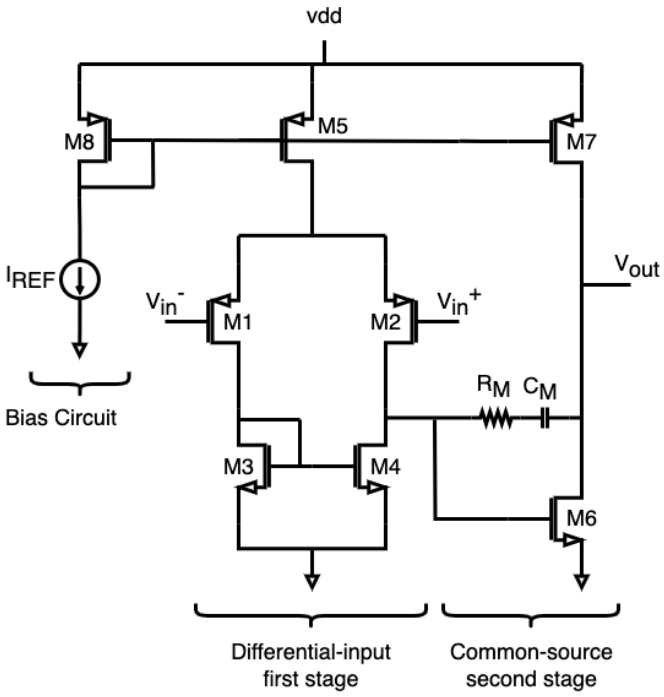



Figure 3.19: Two-stage amplifier schematic [36].

In multi-stage amplifiers like this, each stage introduces a pole in the system's frequency response, which can affect the amplifier stability. In this case the phase margin is degraded because the two dominat poles are relatively close to each other in frequency, which then leads to very poor phase margin. To address the stability issue, Miller compensation is used, implemented by a compensation capacitor ($C_M$) connected between the output of the first stage and the output of the second stage. This Miller compensation works by 'pole-splitting', which pushes the dominant pole to a much lower frequency and the second pole to a higher frequency. This separation improves the phase margin and stabilises the amplifier, ensuring that the phase shift is kept well below 180° at the gain crossover frequency, as (Phase Margin = 180° - Phase at the Gain Crossover Frequency), to avoid instability, it must be above 0°. However, Miller compensation introduces also a Right-Half Plane (RHP) zero, which further complicates the stability. A zero at the RHP behaves like,

- It contributes additional negative phase shift instead of stabilizing the phase;
- The zero reduces the slope at which the magnitude of the gain drops, which pushes the gain crossover frequency higher. As a result, the phase margin decreases, which degrades stability.

To mitigate this effect, a resistor ($R_M$) is placed in series with the Miller Compensation capacitor, $C_M$. The purpose of $R_M$ is to shift the RHP zero towards infinity, effectively making it irrelevant to the phase response [37].

The small signal model of this two-stage amplifier is illustrated in Figure 3.20.

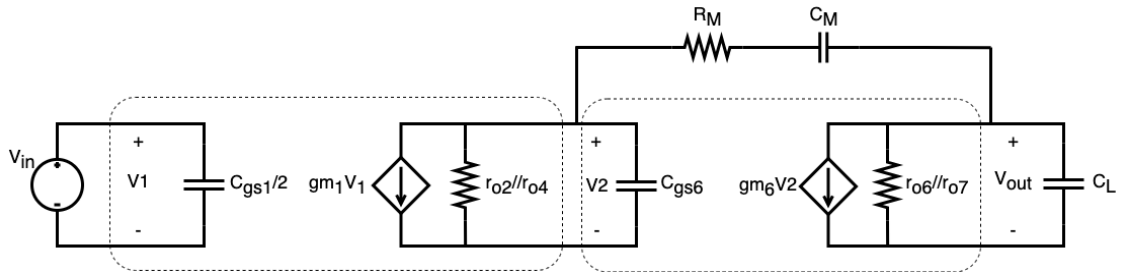



Figure 3.20: Small signal model of two-stage amplifier [36].

The gain of the first stage can be expressed as,

$$A_{v1} = gm_1(r_{o2} \parallel r_{o4}). \tag{3.11}$$

In the second stage, the gain is expressed as follows,

$$A_{v2} = gm_6(r_{o6} \parallel r_{o7}). \tag{3.12}$$

As the overall gain of the two-stage amplifier is given by $A_v = A_{v1} \cdot A_{v2}$, it can be expressed as,

$$A_v = gm_1(r_{o2} \parallel r_{o4}) \cdot gm_6(r_{o6} \parallel r_{o7}). \tag{3.13}$$

Another key consideration when designing the amplifier is the Gain Bandwidth (GBW). Assuming $f_{p1} < f_{p2}$, it can be expressed as follows,

$$GBW = A_v f_{p2}. \tag{3.14}$$

With the poles being given by,

$$f_{p1} = \frac{1}{(r_{o2} \parallel r_{o4}) \cdot gm_6 \cdot (r_{o6} \parallel r_{o7}) \cdot C_M}. \tag{3.15}$$

$$f_{p2} = \frac{gm_6 \cdot C_M}{C_{gs6} \cdot C_L + C_M \cdot (C_{gs6} + C_L)}. \tag{3.16}$$

## 3.5 Local Oscillator

Apart from the mixer and the amplifier, the LO is another important component in the receiver design, as its waveforms control the switching of the transistors in the mixer. This means its characteristics directly affect the mixer performance.

Ideally, the LO waveform should be a square wave rather than a sinusoidal signal, as square waves provide abrupt switching. In contrast, sinusoidal LO signal would result in a gradual switching, causing the transistors to remain in a partially on state for longer periods. The problem with this behaviour is that it would cause an overlap between phases, an undesirable behaviour as the signal paths would interact with each other [1].

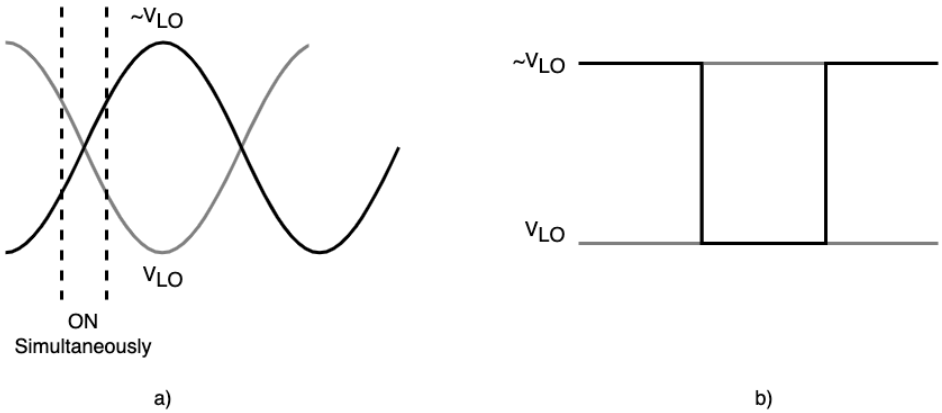



Figure 3.21: LO waveforms (a) Sinusoidal, (b) Square [1].

At higher frequencies, however, generating perfect square waves becomes more difficult, and the LO waveform begins to resemble a sinusoid. In these cases, the amplitude of the LO signal is increased to ensure a high slew rate, which minimizes the overlap time, $\delta T$, during which the transistors are both on. By ensuring the overlap time is as short as possible, the mixer can still achieve close to maximum conversion efficiency even when the LO signal is not perfectly square [1].

In these mixer design, particularly, quadrature downconversion is required, meaning that four LO phases - 0°, 90°, 180°, 270°- need to be generated. To achieve this, a phase generator will be implemented.

# 4

# Simulation Results and Layout Design

The previous chapter introduced some theorical concepts behind the building blocks of the receiver. In this chapter it will be presented the simulations, results and layout of the receiver's block. The circuits were implemented using TSMC 65nm Complementary Metal-Oxide-Semiconductor (CMOS) technology.

## 4.1 Schematic Simulation Results

### 4.1.1 Mixer

The first block in the receiver's chain to be designed was the mixer block, presented in Figure 4.1. For that, some considerations, already highlighted in Chapter 3, were taken into account when designing it, for example the source resistance $R_S$, the switch resistance $R_{ON}$, and the capacitors value.

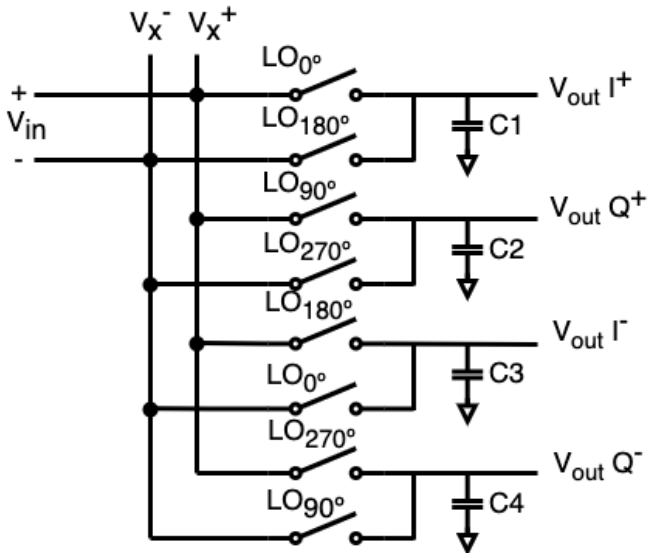



Figure 4.1: Schematic representation of the implemented mixer design.

One of the criteria we must take into account when sizing the mixer is to ensure that we have a low channel impedance so that as little energy as possible is dissipated in this block, and that the transistor work as a switch turning on and off. To guarantee this low impedance and the on and off state, it is necessary to ensure that the transistors that make up the mixer work in the triode zone, the linear conduction zone, where the transistors can function as variable resistors ($R_{ds}$).

The expression for the drain-to-source resistance $R_{ds}$ (also referred as $R_{ON}$) in the strong inversion region, where the Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) operates as an ON switch, is given by [35],

$$R_{ds} = R_{ON} = \frac{V_{DS}}{I_D} \approx \frac{1}{k_n \frac{W}{L}(V_{GS} - V_T)}, \quad k_n = u_{eff} \cdot C_{ox}, \tag{4.1}$$

where $u_{eff}$ is the electron mobility in the channel, $C_{ox}$ is the oxide capacitance per unit area, $W$ the width of the channel, $L$ the length of the channel, $V_{GS}$ the gate-to-source voltage, and $V_T$ the threshold voltage.

From this, it can be observed that the channel resistance $R_{ON}$ is inversely proportional to the ratio $W/L$ and the saturation voltage $V_{DSAT}$. However, important considerations must be made. While increasing the channel width reduces the $R_{ON}$, it comes at the cost of increased area and parasitic capacitances, which can degrade the performance, particularly at high frequencies. On the other hand, the transistor length should be kept as short as possible because the speed of transistor's swithcing behaviour is directly related to the channel length. Since velocity scales as $v \propto \frac{1}{L^2}$, a smaller $L$ results in faster transitions between the on and off states, a criticial point as the input of the transistors are square waves at high frequencies. Another point is that all transistors in the circuit should have the same $W/L$ ratio, a criteria that could not happen in the real world as mismatches between components happen, which leads to the In-phase Quadrature (I/Q) imbalance. So, when designing the mixer particular attention was taken into the factor 'region' to ensure that it is in the linear, or triode region, where the factor 'region' equals 1, and to minimise the $R_{ON}$ value.

Regarding the choice of transistors, the initial design used the 'nmos_rf_6t' transistor from the TSMC 65nm library. However, to further reduce the on-resistance, the transistor model was changed to the 'nmos_rf_lvt' transistor model. The key difference is that the 'lvt' (low-threshold voltage) transistor has a lower threshold voltage ($V_T$), which allows it to achieve a lower $R_{ON}$ compared to higher-threshold voltage devices. Table 4.1 presents the values used on the transistors parameters, such as the width per finger, length, number of fingers and multiplier.

Another important factor to consider when designing the N-Path filter is the RC time constant value. To ensure proper filter operation, it is necessary to ensure that the RC time constant is larger than the switching period, meaning that the filter must be designed

so that the circuit doesn't fully settle within a single switching cycle. This prevents the capacitor from fully charging during each phase of the clock cycle, which is necessary for the filter to function correctly. To achieve this, the value of the capacitor was chosen to be 50 $p$F, ensuring that the charging and discharging behaviour aligns with the desired filtering characteristics. It is also important to mention that the N-Path filter was designed to be connected directly into the antenna, meaning that the 50 Ω of the antenna impedance was taken into account during the design process.

Table 4.1: Switch sizing in the mixer design.

| **Transistor** | **Width ($\mu$m)** | **Length (nm)** | **Fingers** | **Multiplier** | $R_{ds}$ **(Ω)** |
|---|---|---|---|---|---|
| nmos_rf_lvt | 6 | 60 | 14 | 16 | 1.2 |

After sizing the transistor and the capacitor, the focus shifts to the performance of the mixer. Starting with a visual representation of the Band-Pass Filter (BPF) frequency response on Figure 4.2, with the center frequency being on 987 MHz, with a gain of $-5.54\ dB$. The Local Oscillator (LO) frequency was set to be at 1 GHz, however, as it can be seen by Figure 4.2, the band pass filter is not centered at the LO frequency due to the parasitic capacitances of the switches. The filter achieved a quality factor of 14.6.

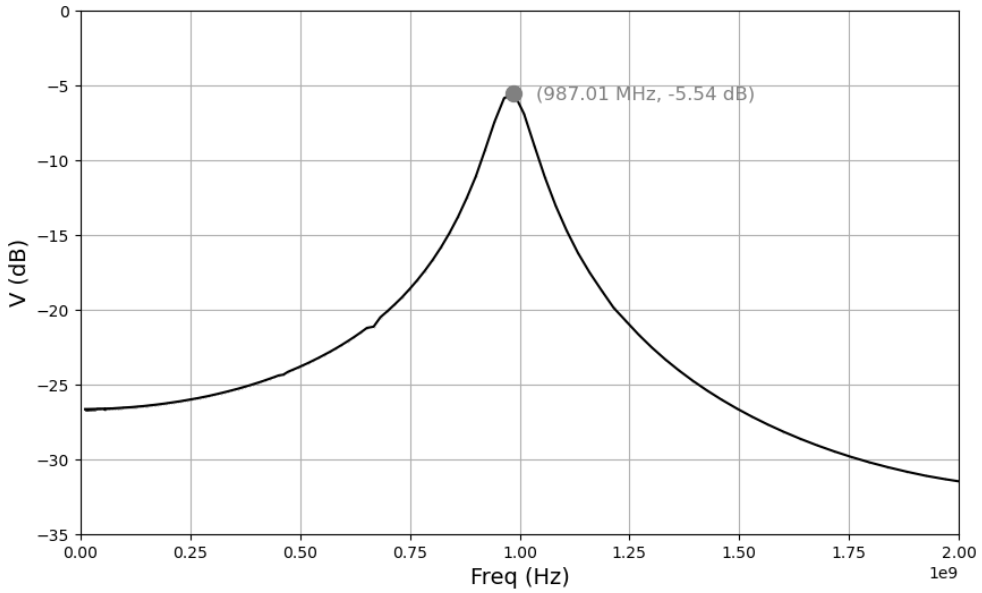



Figure 4.2: BPF frequency response.

Figure 4.3 illustrates the complete frequency response of the filter, showcasing its behaviour across a wide range of frequencies. It also highlights the elimination of even harmonics, a behaviour already described in Chapter 3.

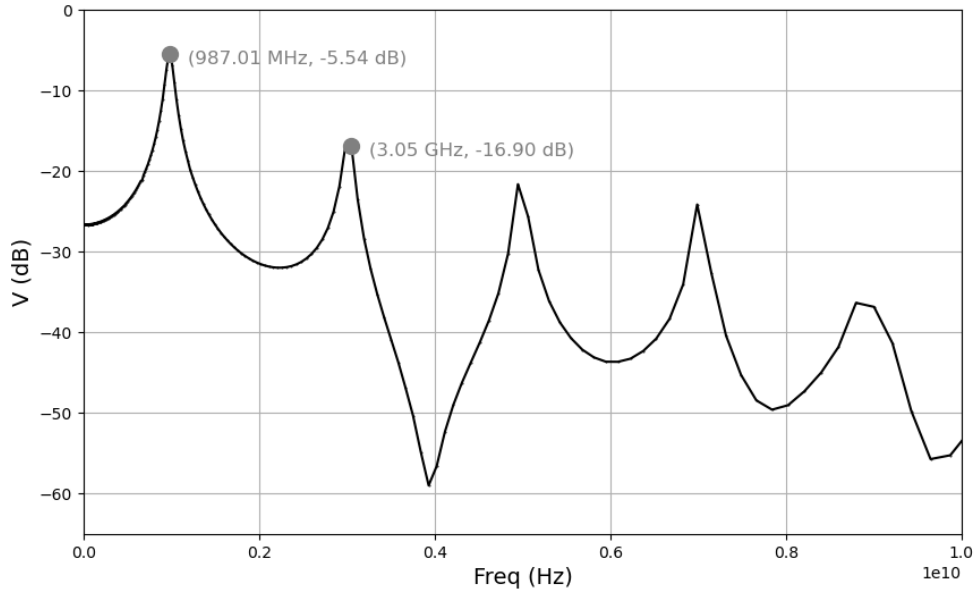



Figure 4.3: Filter performance across a wide frequency range.

In semiconductor fabrication, variations in device parameters, such as threshold voltages, channel lengths/widths, are unavoidable due to inherent process imperfections. These variations can significantly affect the circuits performance. For instance, in N-Path filters, which relies on multiple parallel paths in which ideally would have identical components, any parameter variation can lead to imbalances between the paths, resulting in undesired behaviour or performance degradation.

The Monte Carlo simulation is a powerful tool to assess the statistical impact of random variations in the parameters and values of the components. By performing multiple simulations, each with randomly variations, it is possible to evaluate how process variations affect the performance. In this case, transient analysis is repeated multiple times, with each iteration of the Monte Carlo simulation applying a different set of random variations to the model parameters. The accuracy of a Monte Carlo simulation increases with the number of runs, as more simulations provide a better statistical representation of the parameter variations. However, due to hardware limitations, the analysis was limited to 100 simulation points. Despite this limitation, it provides insights into the variability of the circuits behaviour.

The objective with these simulations is to evaluate the robustness of the circuit against component variations. Specifically, the goal is to quantify how much the circuit performance deviates from the ideal case, where there is no mismatch. To achieve this, three key performance parameters are evaluated: Direct Current (DC) gain, center frequency, and the gain achieved at the center frequency. In Table 4.2 the values obtained for a transient simulation without mismatch are presented.

Table 4.2: Performance results from a transient simulation without mismatch.

| Parameter | Without Mismatch |
|---|---|
| **DC Gain (dB)** | -26.64 |
| **Center Frequency (MHz)** | 979.0 |
| **Gain at Center Frequency (dB)** | -5.44 |

For clarity and ease of analysis, the extensive results obtained from the Monte Carlo simulation will be summarized in a table. The table is organized as follows: the second and third column display the average and standard deviation from the Monte Carlo simulations, respectively. These two values (average and standard deviation) helps to understand the impact of component variations on the circuit's performance, showing how the process variations influence the frequency response filter. The results presented in Table 4.3, Table 4.4, and Table 4.5 summarize the impact of mismatches in transistors, capacitors, and their combined effects, respectivelly.

Table 4.3: Performance results from Monte Carlo simulation with transistors mismatch.

| Parameter | Average | Standard Deviation |
|---|---|---|
| **DC Gain (dB)** | -26.85 | 2.20 |
| **Center Frequency (MHz)** | 979.0 | 0 |
| **Gain at Center Frequency (dB)** | -5.44 | 0.17 |

Table 4.4: Performance results from a transient simulation with capacitors mismatch.

| Parameter | Average | Standard Deviation |
|---|---|---|
| **DC Gain (dB)** | -26.64 | 14.21 $f$ |
| **Center Frequency (MHz)** | 979.0 | 0.17 |
| **Gain at Center Frequency (dB)** | -5.44 | 443.96 $\mu$ |

Table 4.5: Performance results from a transient simulation with capacitors and transistors mismatch.

| Parameter | Average | Standard Deviation |
|---|---|---|
| **DC Gain (dB)** | -26.85 | 2.20 |
| **Center Frequency (MHz)** | 979.0 | 0 |
| **Gain at Center Frequency (dB)** | -5.44 | 0.17 |

The analysis reveals that transistors mismatch has the most significant impact on the DC gain, as evidenced by the highest standard deviation for this parameter among all the three. Conversely, capacitor mismatch has a minimal effect on the circuit performance, with relatively small standard deviations across all three analyzed parameters and average values identical to those obtained without mismatch. When considering the global mismatch of all components, the DC gain remains the most affected parameter, aligning with the earlier findings that transistor mismatch primarly drives this behaviour, while

capacitors contribute negligibly. Interstingly, this effect was benefecial, as it lead to increased attenuation outside the desired band.

### 4.1.2 Amplifier

In this section, the simulation results for the two amplifiers designed in this study are presented. These simulations will provide insight into the performance of each amplifier, including parameters like DC gain, Gain Bandwidth (GBW), phase margin and the voltage common-mode at the output.

The transistor dimensions used for the first amplifier are listed in Table 4.6. In the table, width parameter refers to the width per finger of each transistor. In the analysis of the amplifier frequency response, shown in Figure 4.4 (gain response) and Figure 4.5 (phase response) some performance metrics are detailed in Table 4.7. It is evident that the amplifier does not provide enough gain to strengthen the signal coming from the mixer. To enhance this, increasing the current supplied (currently, $I_{REF}$ is set at 71.4 $\mu A$) or increase the transistor dimensions would be necessary. However, increasing the dimensions may push the transistor out of saturation region, as this would reduce the margin between $V_{gs}$ and $V_{th}$ that is already in a safe margin.

Table 4.6: Amplifier 1 transistors dimensions.

| Transistor | Width ($\mu$m) | Length (nm) | Fingers | Multiplier |
|---|---|---|---|---|
| $M_1$ | 1.95 | 60 | 14 | 1 |
| $M_2$ | 5.92 | 60 | 12 | 1 |
| $M_3$ | 3.52 | 60 | 32 | 1 |
| $M_4$ | 2.16 | 60 | 2 | 1 |

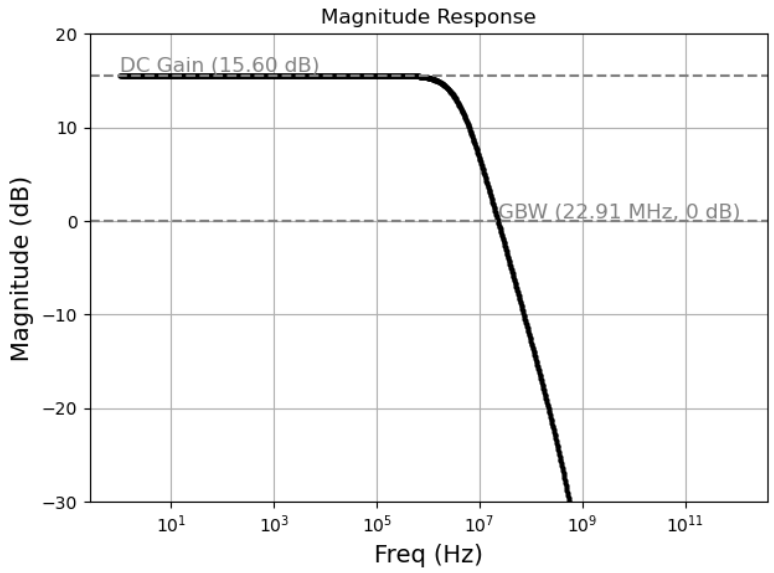



Figure 4.4: First Amplifier gain response.

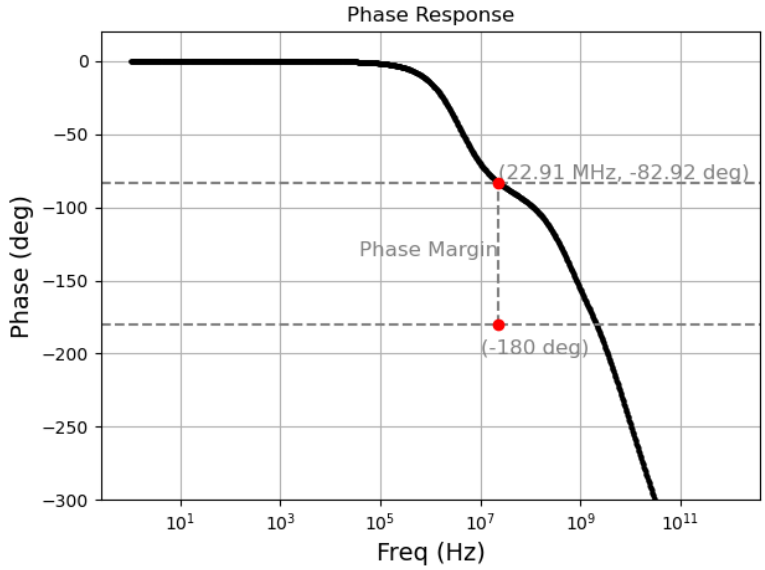



Figure 4.5: First Amplifier phase response.

Table 4.7: Performance results from the first amplifier.

| DC Gain | GBW | Phase Margin | Output VCM | Power Consumption |
|---|---|---|---|---|
| 15.6 dB | 22.9 MHz | 97.1° | 603.4 $m$V | 968.9$\mu$W |

For the second amplifier, i.e, the two-stage Operational Amplifier (OpAmp) the transistor dimensions that guarantee the DC operating point (with the transistor in the saturation region) are listed in Table 4.8. The biasing current for this amplifier was $I_d = 100\ \mu A$.

Table 4.8: Amplifier 2 transistors dimensions.

| Transistor | Width ($\mu$m) | Length (nm) | Fingers | Multiplier |
|---|---|---|---|---|
| $M_{1,2}$ | 3 | 120 | 10 | 1 |
| $M_{3,4}$ | 3.1 | 120 | 1 | 1 |
| $M_5$ | 2.9 | 120 | 4 | 1 |
| $M_6$ | 2.8 | 120 | 2 | 1 |
| $M_7$ | 4.3 | 120 | 2 | 1 |
| $M_8$ | 0.86 | 120 | 1 | 1 |

The frequency response of the two-stage amplifier is presented in Figure 4.6 (gain response) and Figure 4.7 (phase response), highlighting key performance parameters such as the DC gain, GBW, and the phase margin. These parameters are depicted in the reference figures and are further summarized in Table 4.9, which also includes the amplifier's static power consumption.

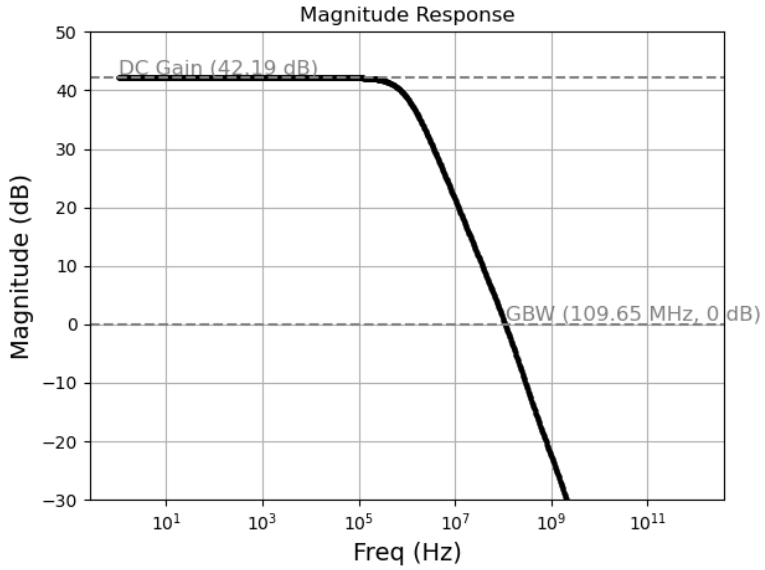



Figure 4.6: Second Amplifier gain response.

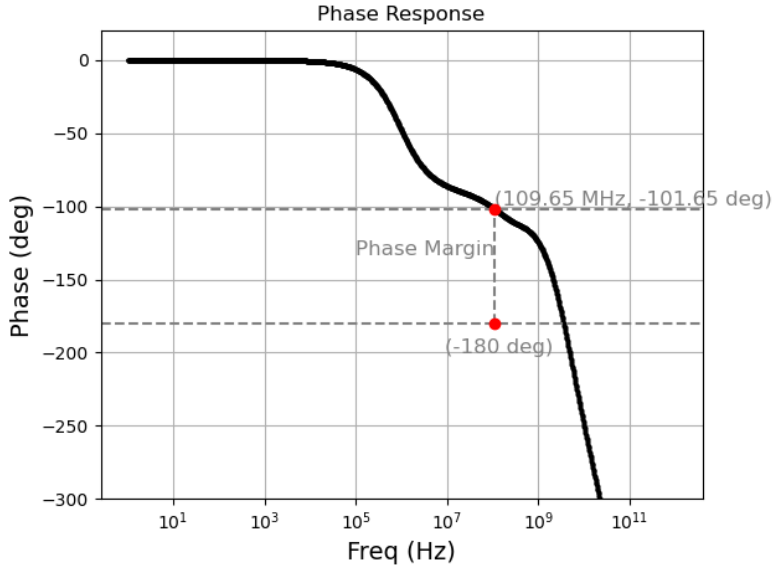



Figure 4.7: Second Amplifier phase response.

Table 4.9: Performance results from the second amplifier.

| DC Gain | GBW | Phase Margin | Output VCM | Power Consumption |
|---|---|---|---|---|
| 42.2 dB | 110 MHz | 78.4° | 602.6 $m$V | 252.6$\mu$W |

### 4.1.3 Phase Generator

To create a phase generator capable of producing four phases with a 25% duty-cycle, three essencial logic gates were first designed and constructed: an inverter, a NAND gate, and

a Flip-Flop D (FFD). Each of these blocks plays a criticial role in achieving the desired phase shifts and duty-cycle. The final phase generator was built by combining these logic gates and additional delay blocks, as explained below.

#### 4.1.3.1 Inverter

The first logic gate built was the inverter, which performs a simple function: it outputs the opposite logical state of its input. If the input is logical '1', the output will be '0', and vice versa. In terms of design, the inverter is composed of two transistors: a PMOS transistor in the pull-up network and an NMOS transistor in the pull-down network, as illustrated in Figure 4.8.

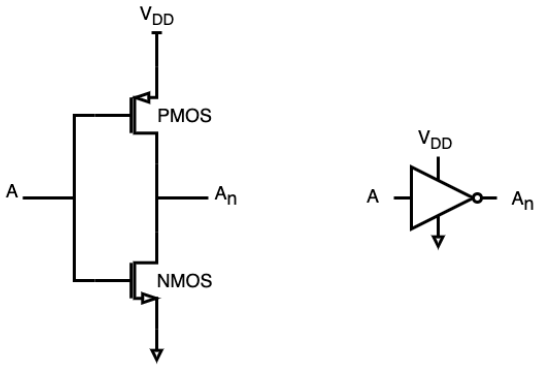



Figure 4.8: CMOS inverter schematic and symbol [38].

To ensure balanced performance, such as equal rise and fall times, it is important to size the PMOS and NMOS transistors appropriately. Typically, the PMOS transistor is sized about three times larger than the NMOS. This compensates for the lower mobility holes in the PMOS compared to the higher mobility of electrons in the NMOS. Specifically, the mobility of holes in a PMOS is approximatelly three times lower than the mobility of electrons in an NMOS. Taking the following ratio between $K_n$ and $K_p$ [38],

$$\frac{K_n}{K_p} = \frac{\mu_n C_{ox}(W/L)_n}{\mu_p C_{ox}(W/L)_p} = \frac{\mu_n (W/L)_n}{\mu_p (W/L)_p}. \tag{4.2}$$

Since the goal is to balance the switching, we want $K_n/K_p = 1$. Therefore, the width-to-length ratio of the transistors must satisfy the following condition,

$$\frac{(W/L)_n}{(W/L)_p} = \frac{\mu_n}{\mu_p} \approx \frac{1}{3}. \tag{4.3}$$

This means that the width-to-length ratio of the PMOS must be approximately three times that of the NMOS,

$$(W/L)_p \approx 3(W/L)_n. \tag{4.4}$$

Since typically it is assumed the same channel length between the PMOS and NMOS transistor, this simplifies further to,

$$W_p \approx 3W_n. \tag{4.5}$$

Thus, in order to achieve balanced switching behaviour ($R_n = R_p$), the PMOS must be sized in order to satisfy equation (4.5). Table 4.10 shows the transistors sizing for the inverter logic gate.

Table 4.10: PMOS and NMOS transistors sizing for inverter logic gate.

| Transistor | Width (nm) | Length (nm) | Fingers | Multiplier |
|---|---|---|---|---|
| PMOS | 2400 | 60 | 1 | 20 |
| NMOS | 800 | 60 | 1 | 20 |

#### 4.1.3.2 NAND

The next logic gate to be built was the NAND logic gate, illustrated in Figure 4.9. This logic gate outputs a logical '0' only when both inputs are logical '1', otherwise, it outputs '1'.

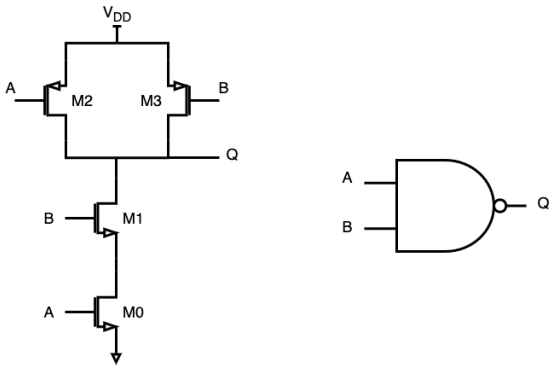



Figure 4.9: NAND schematic and symbol [38].

For the NAND gate, the same transistor dimensions as those used in the inverter were utilized. To generate the four phases (0°, 90°, 180°and 270°), the design on Figure 4.1.3 was

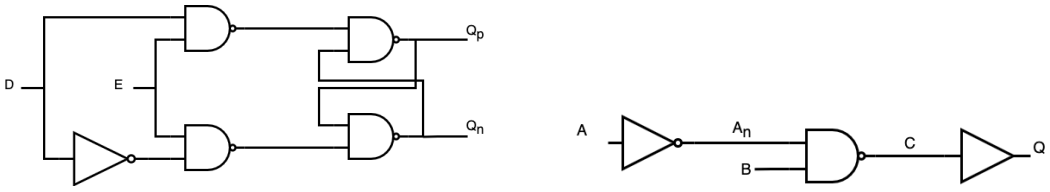
Table 4.11: PMOS and NMOS transistors sizing for NAND logic gate.

| Transistor | Width (nm) | Length (nm) | Fingers | Multiplier |
|---|---|---|---|---|
| $M_{2,3}$ | 2400 | 60 | 1 | 20 |
| $M_{0,1}$ | 800 | 60 | 1 | 20 |

developed. This uses FFDs connected in a feedback loop and four delay blocks (Figure 4.10b). The first step involved the building of a D latch (Figure 4.10a), which serves as the foudation for the FFD.

In this schematic, the outputs from the two FFDs are interconnected in a feedback loop. Specifically, the output $Q_{p1}$ from the first FFD to the D input of the second FFD, while the output $Q_{n2}$ from the second FFD feeds back into the D input of the first FFD. Both flip flops are driven by quadrature clocks (off-chip signals) with twice the frequency of the LO frequency. This feedback configuration, combined with the quadrature clocks, allows the

FFDs to toogle sequentially, generating the four quadrature outputs at a frequency that is half of the clock frequency, as each output $Q$ transitions once every two clock cycles. As the four output phases overlap, to prevent this from happening, the delay block (Figure 4.10b) was used to introduce a delay to prevent the phases from overlapping, as it has already been mentioned that the LO phases cannot overlap.




(a) D Latch. (b) Delay block.

Figure 4.10: Building block used in the phase generator block.

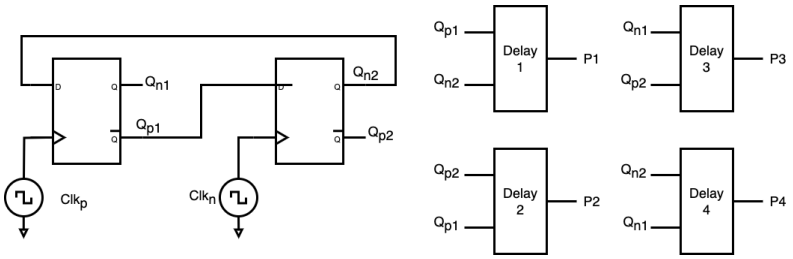



Figure 4.11: Phase Generator.

The output of the phase generator is shown in Figure 4.12, were the four phases are non-overlapping.

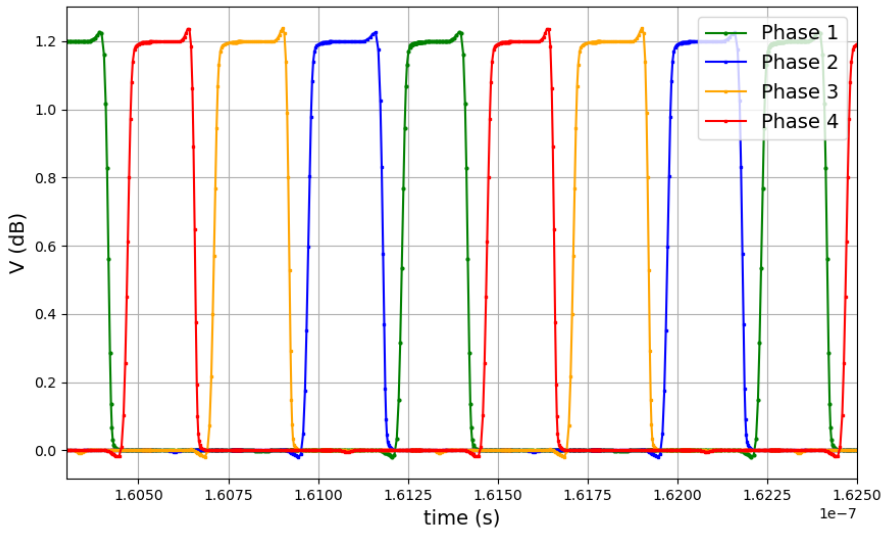



Figure 4.12: Output from the phase generator: four non-overlapping phases.

The output of the receiver is presented in Figure 4.13, illustrating the In-phase(I) and Quadrature (Q) signals. The figure confirms that the receiver sucessfully establishes a passband at 1 $GHz$, as intended, demosntrating that the RFFE effectively attenuates signals outside this band. Additionally, at the center frequency of the passband - where attenuation was previously observed at the output of the N-path filter - the amplifier now helps to enhance the signal strength for digital domain processing. The total static power consumption was measured at 1.58 $mW$.

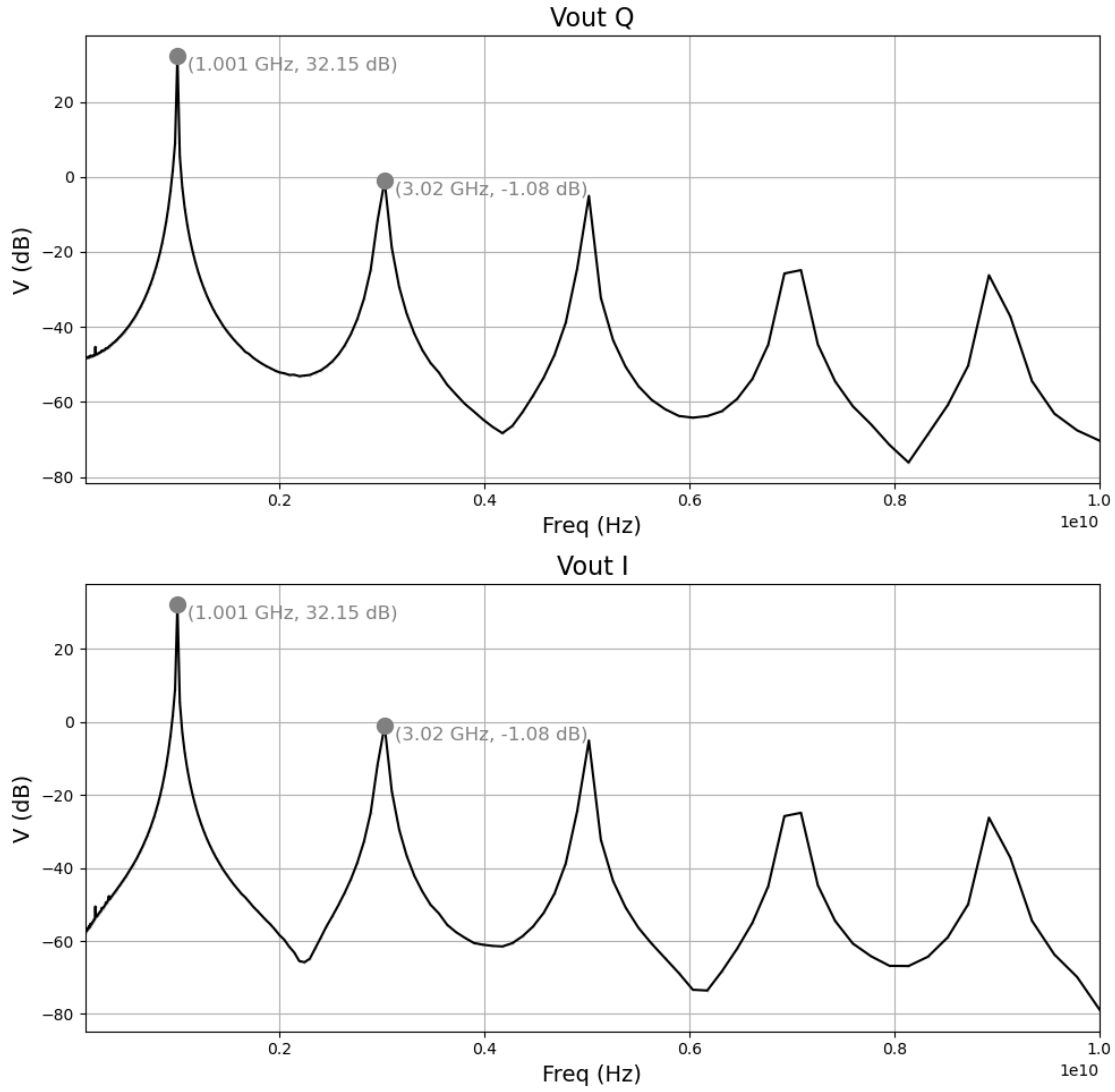



Figure 4.13: Output signals from the I (bottom graph) and Q (top graph) paths in the receiver block.

## 4.2 Layout Design

In the following section, the layout designs for both mixer and amplifier will be presented. Special attention must be given to the layout process, as this blocks are intended for

use in Radio Frequency (RF) systems, where circuit performance is highly sensitive to parasitics. The transistors and capacitors inherently introduce parasitic elements, and its crucial to minimize the addition of further parasitics during the layout. This can be achieved by carefully managing wiring strategies, paying close attention to the length of interconnections, selecting appropriate metal layers for connections and ensuring symmetrical placement of input and output signals, and also the layout in general, attention to the symmetry of the layout should be considered.

For instance, in the transistor gate, which is typically made of Polysilicon (PO), a more conductive metal was used for connections to avoid the resistance associated with the poly. Care was also taken to find the shortest routing paths, avoid metal layer overlap, and place vias strategically to use different metals layers when different paths cross each other. This minimizes parasitic resistance and capacitance while optimizing signal integrity. Additionally, components and wiring were spaced with sufficient safety margins to prevent mutual interference and account for potencial fabrication inaccuracies.

In cases where connections had to branch to multiple paths, multiple routes made of the same metal were used to distribute the current evenly. This reduces the risk of overloading a single path. Similarly, when placing vias, multiple contacts were used instead of a single one to ensure reliable current distribution. Using multiple contacts improves the robustness by reducing the risk of circuit failure if one contacts breaks, while also distributing the current reducing the pressure on individual contacts.

Component placement was done with careful attention to two main factors: layout symmetry and proximity of interconnected components. Symmetry is critical for minimizing offsets, suppressing common-mode noise, and reducing even-order nonlinearities [35]. To maintain symmetry, component parameters were adjusted, such as the width and number of fingers of the transistors, to ensure a better fit and minimize imbalances. Componentes sharing the same nets were placed close together to reduce connection lengths and parasitic effects. In cases where differential pairs were used, such as in the amplifier, their signal paths were designed to be as identical as possible to maintain symmetry.

When transistors required a large gate length, the strategy was to split them into multiple fingers in order to reduce the resistance of the polysilicon gate and also to ensure less process variation and better fitting of the model. An even number was prefered over odd fingers, as a rule of thumb.

The common-centroid layout technique, often used for matching identical transistors, was not used in here due to the inclusion of guard rings around the RF transistors. The RF transistor models already incorporated guard rings, and it was decided to retain those and work with the original model of this transistors. The NMOS transistors were surrounded

by three guard rings, and PMOS by two guard rings. A deep n-well (DNWELL) layer was also added around the circuit to shield the NMOS transistors from p-substrate noise.

For the resistance used in the Miller compensation on the amplifier, the total resistance was divided into six smaller resistors connected in series to achieve the desired value. Although a serpentine layout could have been used, they introduce high resistance at the corners. Also, the chosen implementation was preferred for better matching and reproductibility. The total resistance was calculated using the formula [38]:

$$R_{\text{total}} = \frac{R_{\text{sheet}} \cdot L}{W}, \tag{4.6}$$

with $R_{\text{sheet}}$ being equal to 14.9255 $\Omega$/per square in the resistance model. This total resistance was then divided by six to determine the resistance value of each individual unit.

The N-Path filter layout was designed using a modular building-block approach. The mixer is composed of four identical blocks, each comprising two transistors (that perform the switching mechanism) and a capacitor. To simplify the design process and ensure that all four paths have identical layouts, the layout for a single basic block was created first.

As the N-Path filter consists of four identical blocks, its layout was designed using a modular building-block approach. Each of this building-blocks are composed of two transistors (that perform the switching mechanism) and a capacitor. To simplify the design process and ensure that all four paths have identical layouts, the layout for a single basic block was created.

As an example of the receiver layout's block diagram, Figure 4.14 illustrates the Quadrature (Q) path, which is identical to the In-Phase (I) path. In this diagram, two building blocks from the previously described N-Path filter are used: one for the Q+ path and the other for the Q- path. Following the N-Path block is the OTA layout, where the differential input receives the two outputs generated by the Q path.

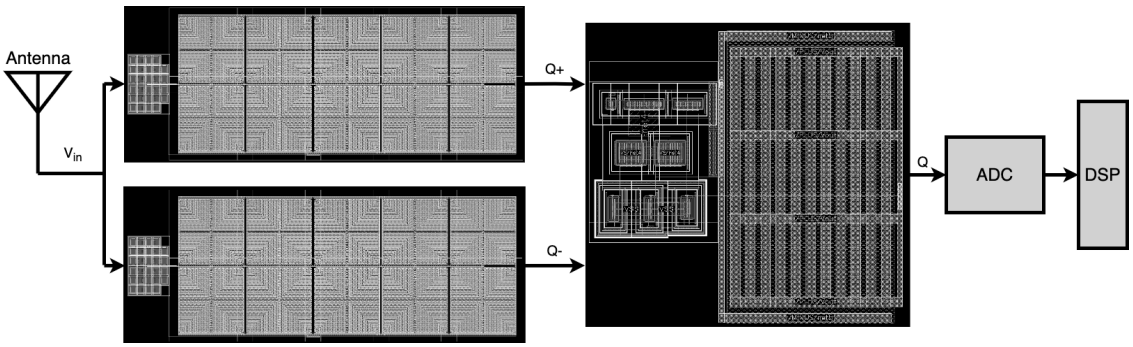



Figure 4.14: Receiver block diagram describing the Q path with the N-Path and OTA layout.

The layout of the basic block of the N-Path is shown in Figure 4.15. The amplifier layout is illustrated in Figure 4.16.

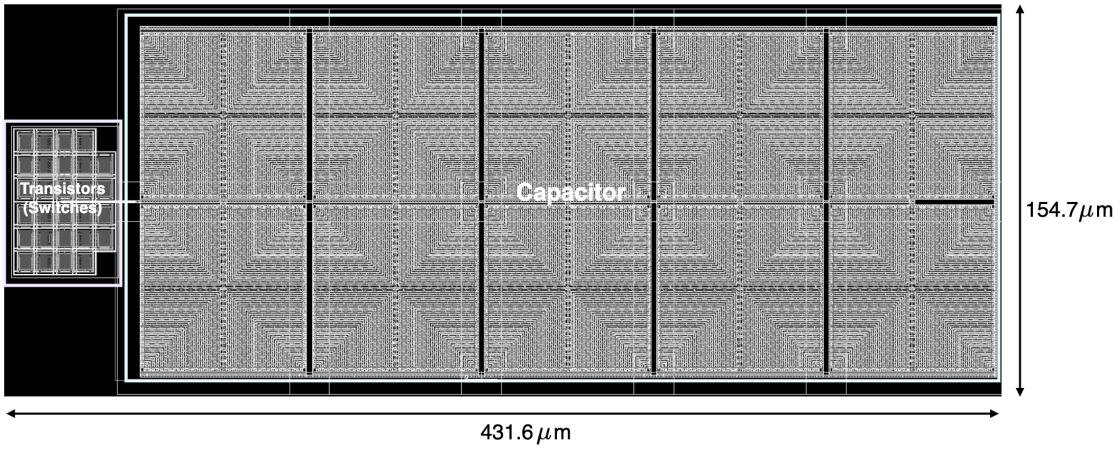



Figure 4.15: Layout of the designed N-Path basic building block.

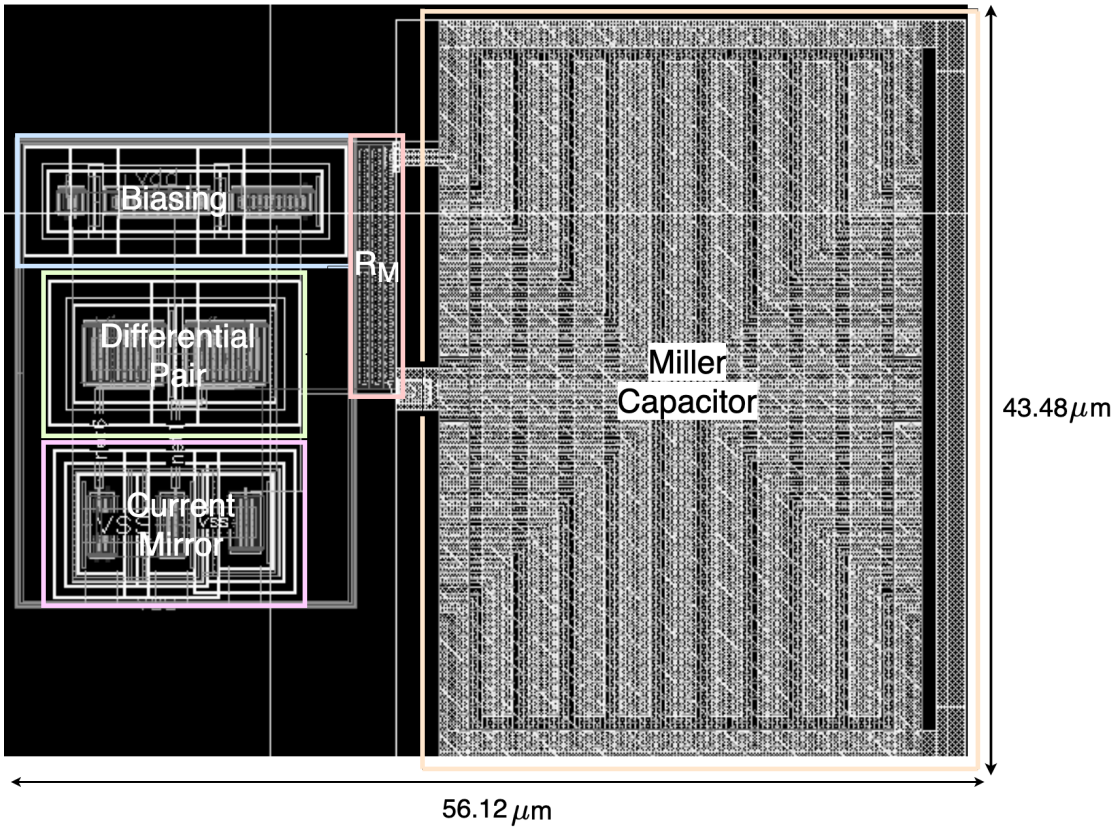



Figure 4.16: Layout of the designed two-stage amplifier.

To clearly illustrate the resistance configuration described above, a zoomed-in view (Figure 4.17) is included, highlighting the detailed connections.

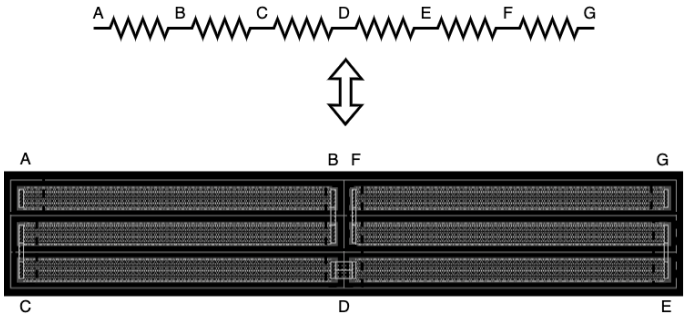



Figure 4.17: Equivalence between the schematic and layout connections on the segmented resistance.

# 5

# Conclusion and Future Work

## 5.1 Conclusion

The rapid growth of digital communications has led to a congested spectrum, posing significant challenges in managing increasing interference. As a result, modern trasnceivers require robust receiver architectures capable of effectively mitigate this interference.

In this thesis, the design of an N-Path Radio Frequency Front-End (RFFE) receiver was presented, utilizing N-Path filtering techniques to supress out-of-band signals while preserving both the integrity and introduce strength to the input signal, ensuring a robust signal for subsequent digital processing. The receiver employs a Direct-Conversion Receiver (DCR) architecture with a mixer-first approach. The differential N-Path filter is implemented through passive mixers controlled by a LO frequency, which allows for adjustable filtering. Regarding the amplification stage, two design approaches were considered, with the second one being preferred. Additionally, the layout of the building blocks for the receiver architecture was implemented.

The results, detailed in Chapter 4, begin with the frequency response of the filter, showing a filter centered near 1 *GHz* with a quality factor of 14.6. Monte Carlo simulations were conducted to assess the impact of transistor and capacitor mismatches on the performance of the N-Path filter. The AC response of the two-stage amplifier was also evaluated to assess its gain and phase margin. The phase generator block was tested, confirming the generation of four non-overlapping output phases. Finnally, the overall performance of the receiver was tested with all the blocks integrated to analyse its functionality. It was observed that the receiver was able to deliver a front-end capable of filtering out-of-band frequencies around 1 *GHz*. Additionally, the receiver demonstrated its ability to provide gain to in-band frequencies, ensuring proper signals amplification. The total power consumption of the receiver's RFFE was measured to the 1.58 $mW$. Furthermore, the layout simulation results were consistent with those obtained from the schematic, validating the design's robustness and accuracy.

In conclusion, the primary objective of implementing an RF Front-end receiver has been achieved, although there are still improvements and tests that could have been done.

## 5.2 Future Work

This thesis lays the groundwork for future work to enhance performance:

- I/Q Impairments: As mentioned, this architecture is susceptible to I/Q impairments that can degradate overall performance. Future efforts could focus on developing methods to mitigate these impairments, particularly in the analog domain, to improve signal integrity.
- Impact on OFDM Modulation: A more in-depth study can be conducted to quantify the impact of I/Q impairments on OFDM modulation. This could involve creating algorithms or a model to assess and calculate the overall effects of these impairments.
- Automatic Phase Generator: Developing a phase generator that automatically adjusts the Local Oscillator frequency when needed could enhance the adaptability of the receiver. This would allow for real-time tunning based on changing signal conditions.
- Layout Improvements: The layout can also be enhanced to further minimize I/Q impairments, pottentially thorugh a more vaste usage of layout techniques.

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