NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NEURO-INSPIRED ULTRA-LOW-POWER CMOS ELECTRONIC SYSTEM (μW RANGE) FOR ECG AND BMI APPLICATIONS

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Master in Science

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Adviser: João Carlos da Palma Goes
Full Professor, NOVA School of Science and Technology of NOVA University of Lisbon

Co-adviser: José Carlos Príncipe
Distinguished Professor, University of Florida

Examination Committee

Chair: José António Barata de Oliveira
Full Professor, NOVA School of Science and Technology of NOVA University of Lisbon

Rapporteurs: Fábio Moreira de Passos
Assistant Professor, Instituto Superior Técnico of Universidade de Lisboa
Vítor Manuel Grade Tavares
Assistant Professor, Faculty of Engineering of University of Porto

Adviser: João Carlos da Palma Goes
Full Professor, NOVA School of Science and Technology of NOVA University of Lisbon

Members: Guiomar Gaspar de Andrade Evans
Assistant Professor, Faculty of Sciences of Universidade de Lisboa
José António Barata de Oliveira
Full Professor, NOVA School of Science and Technology of NOVA University of Lisbon
Nuno Filipe Silva Veríssimo Paulino
Associate Professor with Habilitation, NOVA School of Science and Technology of NOVA University of Lisbon

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Neuro-Inspired Ultra-low-power CMOS Electronic System (μW range) for ECG and BMI Applications

To Helena, Luísa, and Júlia, my beautiful wife and daughters.

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believe anything is possible. Thank you, you are my life.

"You cannot teach a man anything; you can only help him discover it in himself." (Galileo)

Abstract

Brain-machine interfaces (BMIs) require major advances in electronics, so that constrains such as the need of low power, small size, lightweight, and high bandwidth wireless-communications with small data-rates can be solved, Sanchez *et al.* [1]. Continuous time (CT) asynchronous data converters namely, analog-to-digital converters (ADCs) and analog-to-time converters (ATCs), can be beneficial for certain types of applications, such as, processing of biological signals with sparse information. A particular case of these converters is the integrate-and-fire converter (IFC) that is inspired by the neural system. This dissertation presents and compares two CT asynchronous ATC that do not require an external clock signal. They are two low power IFC solutions, one analog and the other a fully digital dynamic IFC [2, 3]. The first is a closed-loop analog IFC with conventional blocks and on-chip capacitor, although not sacrificing either the chip area or power. The latter, is an open-loop standard cell-based (SCB) IFC, fully synthesizable (with the addition of two on-chip capacitors) and dynamic as each individual block can be powered off. Both can be used as an analog frontend (AFE) without requiring external blocks. Being fully-differential - the analog solution is fully-differential, the SCB one is pseudo-differential, it also benefits its performance in AFE applications. As both systems are asynchronous, having a low power dissipation, and with pulse outputs with low data rates, they are a good solution for edge applications, such as low power sensors AFE in internet of things (IoT). Both have been designed and prototyped in a 130 nm CMOS standard process. The analog version has a power dissipation of 53 µW, an energy *per* pulse of 1060 pJ, and it can convert signals with a peak-to-peak amplitude of 0.6 mV to 2.4 mV and a frequency range of 10 Hz to 4 kHz, and the SCB version: 59 µW, 18 pJ - which is one of the lowest energy *per* pulse consumption reported for IFC circuits, and

1.6 mV to 32 mV and 2 Hz to 42 kHz, respectively. The maximum pulse density (average firing rate) for analog version is 50 kHz and SCB version 3300 kHz.

Keywords: IFC, Neuroelectronics, BMI, electrocardiogram (ECG), Analog mixed-signal, SCB

Resumo

Interfaces cérebro máquina estão dependentes de avanços drásticos em electrónica, para que os constrangimentos de: baixa potência (BP), tamanho pequeno, leves e comunicações sem fios numa gama de frequências larga com baixas taxas de dados (BTD) possam ser endereçados, Sanchez *et al.* [1]. Conversores de dados assíncronos contínuos no tempo (CnT) (conversor analógico digital e conversor analógico temporal (CAT)) podem ser vantajosos para determinadas aplicações, como por exemplo, no processamento de sinais biológicos com escassa informação. Um caso particular destes conversores é o integração com disparo (ID) que é inspirado no sistema neuronal. Esta tese apresenta e compara dois CAT assíncronos, CnT, que não necessitam de um sinal de relógio externo. Consistem em duas soluções de ID de BP, uma analógica e a outra digital e dinâmica [2, 3]. A primeira consiste num ID analógico em malha fechada, com blocos convencionais e um condesador integrado, não sacrificando, no entanto, a área do chip ou potência. A segunda é um ID em malha aberta composto por blocos digitais, inteiramente sintetizável e dinâmico pois pode-se desligar cada bloco. Ambos são capazes de, sem necessitarem de blocos externos, serem usados como primeira interface analógica (PIA) num dispositivo que interage com o exterior. Sendo totalmente diferenciais - a solução analógica é totalmente e a baseada em células digitais padrão (BCD) é pseudo, apresentam uma melhor performance em aplicações de PIA. Como ambos sistemas são assíncronos, com uma BP e com sinais de saída em pulsos com BTD, são uma boa solução para aplicações limítrofes, como sensores de BP na internet das coisas. Ambos circuitos foram projectados e prototipados num processo CMOS padrão de 130 nm. A versão analógica dissipa 53 μW, tem uma energia por pulso de 1060 pJ e converte sinais com amplitude pico a pico de 0.6 mV a 2.4 mV e cobre uma gama de frequências de 10 Hz a 4 kHz e, a versão BCD: 59 μW, 18 pJ - que é

uma das energias por pulso mais baixas, reportadas para circuitos de ID, 1.6 mV a 32 mV e 2 Hz a 42 kHz, respectivamente. A densidade de pulsos máxima (taxa média de disparo) para a solução analógica é 50 kHz e para BCD é 3300 kHz.

Palavras-chave: Integração com disparo, Neuroelectrónica, ECG, AMS

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Acronyms

ac Alternating Current i

ADC Analog-to-Digital Converter i, xv, 2, 3, 15, 24, 25, 29, 31, 109, 113, 114

AFE Analog Frontend i, xv, 5, 12, 18, 21, 22, 25, 28, 30, 31, 113, 117, 118

AMS Analog Mixed Signal i

ASIC application-specific IC i, 109

ATC Analog-to-Time Converter i, xv, 2, 5, 6, 7, 24, 30, 34

BCD Baseada em Células Digitais Padrão i, xvii, xviii

BCI Brain-Computer Interface i, 2

BioCAS IEEE Biomedical Circuits and Systems Conference i, 6

BMI Brain-Machine Interface i, xv, xvi, 1, 2, 4, 21

BP Baixa Potência i, xvii

BTD Baixas Taxas de Dados i, xvii

BW Bandwidth i, 15, 20, 21, 25, 31, 37, 49, 50, 55, 57, 72, 74, 96, 99, 104, 109, 110, 111, 113, 114, 115

CAD Computer Automated Design i

CAT Conversor Analógico Temporal i, xvii

CM Common-Mode i, 20, 33, 39, 42, 47, 61, 63, 74, 75, 84, 85, 86, 87, 89, 90, 91, 96, 104, 110, 111

CMFB Common-Mode Feedback i, xxi, xxv, 39, 40, 42

CMOS Complementary Metal-Oxide-Semiconductor i, xv, xvii, xxii, 4, 7, 17, 20, 21, 23, 26, 27, 39, 55, 56, 57, 58, 59, 60, 105, 117, 119

CMRR Common-Mode Rejection ratio i, 13

CNEL Computational NeuroEngineering Laboratory i, xxv, 3, 18, 22, 23, 24, 25, 28

CnT Contínuos no Tempo i, xvii

CPU Central Processing Unit i, 1, 2, 4

CT Continuous Time i, xv, xxi, 2, 5, 7, 24, 30, 40, 107, 119

dc Direct Current i, xxiii, 13, 27, 36, 43, 60, 61, 62, 69, 81, 91, 92, 93, 94, 95, 96

DSP Digital Signal Processing i, 1, 4, 118

ECG Electrocardiogram i, xvi, xxiii, 1, 2, 4, 26, 29, 84, 85, 86, 87, 105, 107, 109, 115, 117, 118

ECoG Electrocorticogram i, 2

EEG Electroencephalogram i, 26

EMG electromyography i

ENG electroneurogram i, 109

ENOB Effective Number of Bits i, 16, 20, 21, 25, 31, 114

ESD Electrostatic Discharge i, 56

EU European Union i, 3

FCT NOVA School of Science and Technology i

FDSOI Fully-Depleted Silicon-on-Insulator i, 31, 114, 119

FFT Fast Fourier Transform i, xxiii, 72, 99, 100

FinFET Fin Field Effect Transistor i, 119

FoM Figure-of-Merit i, 15, 20, 21, 23, 24, 25, 28, 31, 112, 113, 114

FPAA field-programable analog array i, 109

FPGA Field Programmable Gate Array i, 4, 115, 118

FWIRE Florida Wireless Implantable Recording Electrodes i, 3

GAA Gate All Around i, 119

GPU Graphic Processing Unit i, 2, 4

IC Integrated Circuit i, xxvii, 3, 4, 55, 56, 63, 72, 96, 109, 115
ID Integração com Disparo i, xvii, xviii
IFC Integrate-and-Fire i, xv, xvi, xix, xx, xxi, xxii, xxiii, xxiv, xxv, 2, 3, 4, 5, 7, 10, 11, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 33, 34, 35, 36, 37, 38, 39, 40, 41, 43, 44, 45, 46, 47, 48, 49, 50, 51, 53, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 117, 118, 119
IoT Internet of Things i, xv, 5, 30, 117
IPI Inter-Pulse Interval i, xxiii, 34, 38, 44, 50, 55, 71, 72, 74, 75, 77, 78, 79, 81, 83, 84, 85, 86, 88, 89, 90, 91, 92, 93, 94, 96, 97, 100, 102, 103, 104, 110, 111
ISCAS IEEE International Symposium of Circuit and Systems i, 28

KARMA Kernel Adaptive Autoregressive-Moving-Average i, 29, 118

LC level-crossing i, 109
LFP Local Field Potentials i, 2, 21, 25
LNA Low Noise Amplifier i, 25, 28, 31, 114

MIM Metal Insulator Metal i, 42, 45, 47, 56
MNCLM Overall Morhpological Neuron Cell Behavior Model i, 7, 8
MOSFET Metal Oxide Semiconductor Field Effect Transistor i, 119

NMAE normalized mean absolute error i, 106, 107, 108
NMOS N-Channel Metal Oxide Semiconductor Field Effect Transistor i, 10, 11, 12, 37, 39, 41, 42, 43, 44, 50, 52, 54
NOVA NOVA University Lisbon i
NOVAthesis NOVAthesis LaTeX Template i, 6
novathesis.cls novathesis.cls class i

NRMSE normalized root mean square error i, 106, 107, 108

OP-AMP Operational Amplifier i, 10, 11, 13, 18, 19, 26, 37

OTA Operational Transconductance Amplifier i, xxi, xxv, 10, 12, 13, 19, 20, 21, 23, 27, 34, 36, 37, 39, 40, 41, 42, 43, 45, 59, 89, 104, 110, 111

PCB Print Circuit Board i, xx, xxii, 5, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 115

PIA Primeira Interface Analógica i, xvii

PLL Phase-Locked Loop i

PMOS P-Channel Metal Oxide Semiconductor Field Effect Transistor i, 10, 17, 18, 19, 39, 41, 43, 50, 52, 54

PSRR Power Supply Rejection Ratio i, 13, 47, 58

PVT Process, Voltage, and Temperature i, 10, 20, 23, 45, 50, 104

R&S Rohde & Schwarz i, 72

RAM Random Access Memory i, 27

RBC Replica Bias Circuit i, 43, 44, 61

RC Resistor Capacitor i, 8, 12, 23, 33, 34, 36, 110

RF Radio Frequency i, 56, 59

RMS root mean square i

SCB Standard Cell-Based i, xv, xvi, xx, xxi, xxii, xxiii, xxiv, xxv, 4, 5, 10, 12, 18, 20, 22, 24, 26, 30, 34, 36, 45, 46, 47, 48, 49, 50, 55, 57, 58, 60, 62, 63, 68, 70, 72, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 110, 111, 112, 113, 114, 115, 117, 118

SFDR Spurious Free Distortion Ratio i, 99

SNDR Signal-to-Noise-and-Distortion Ratio i, 15, 16, 24, 25, 31, 112, 113, 114

SNR Signal-to-Noise Ratio i, 25, 26, 31, 114

SoA State of the Art i, 5, 7, 17, 28, 29, 107, 111

TEM time encoding machine i, 2, 5, 7, 29, 118

TFF Toggle Flip-flop i, 37, 45, 46, 47, 58, 63, 64, 71, 72, 74, 115

VLSI Very Large Scale Integration i, 3

WLPK Weighted Low-Pass Kernel Method i, 28, 71

1

Introduction

1.1 Introduction and Background

Brain-machine interface (BMI) is a bustling research area aiming at recuperating communication and control for daily activities in disabled individuals.

The possibility of using direct neural interfaces, BMIs, to assist disabled people is driving great innovations in neurotechnology, which will revolutionize our ability to deal with various health problems such as spinal-cord injury, movement disorders, stroke, epilepsy, hearing loss, and blindness [4].

Ideally, BMIs should be designed as plastic, intelligent tools that, beyond executing user intention, evolve while in use, Sanchez [5]. In order to achieve this purpose, better understanding of the system neurophysiology should be paralleled by major advances in electronics, so that constrains such as the need of low power, small size, lightweight and high bandwidth wireless-communications with small data-rates can be solved, Sanchez *et al.* [1].

On the other hand, cardio vascular diseases are the major cause of death in the world according to the World Health Organization, responsible for the lost of 17.9 million lives *per* year (estimate of 32% of deaths in the world) [6]. Electrocardiogram (ECG) measurement devices, as for example Holter monitors still require data to be transmitted and processed externally in bulkier devices, or more frequently in central processing units (CPUs). As processing continuously recorded data for, for example, arrhythmia detection still requires a dedicated processor with a considerable power dissipation, using conventional digital signal processing (DSP) methods for pattern recognition. New signal

processing methods are required to reduce power dissipation, size and achieve portable Holter monitors that recognize anomalies in heart signals. Online or measured in the previous minutes, locally, near the patients body.

Asynchronous continuous time (CT) analog-to-time converter (ATC) can contribute for that advancement in electronics required by BMIs, as well as, ECG. Being low power and with low output data rates. Further more, if there is no output signal reconstruction and the system works with time information (output time series), as for example pulse processing, than that is a great advancement and a revolution in electronics, that in this way mimic the brain behavior. And may be implemented with lower power dissipation and reduced size than conventional CPUs and graphic processing units (GPUs).

Asynchronous CT ATCs and analog-to-digital converters (ADCs) present interesting capabilities for certain applications, for example, those dealing with low frequency signals with sparse information. Biological signals such as ECG or neuron signals, electrocorticogram (ECoG) - for brain-computer interfaces (BCIs), local field potentialss (LFPs) or single neuron action potentials - for BMIs, are potential examples. On the other hand, CT based ADCs have been the subject of increased interest in the last years due to expected better performance with technology scaling-down, when compared to conventional ADCs. For certain cases, particularly for higher frequency input signals, as these topologies can take advantage of gate delay reduction and work at reduced voltage headroom [7], as they are single bit implementations.

Asynchronous CT ATC are a particular case of these types of samplers, where the analog input is converted to a time vector indexed to the time of conversion. This is the case of an integrate-and-fire converter (IFC) circuit, it creates an amplitude-to-time conversion, having a stream of pulses as output. As it is asynchronous, the circuit only fires a pulse when the input signal time integration is above a defined threshold. This means that small variations in the input signal, that for certain applications do not contain relevant information, will not be converted, reducing the overall system power dissipation and creating a converted signal with lower data rate than in a common ADC. The output pulse stream of an ATC can be then converted into a digital signal through a time to digital circuit, or processed in the time domain. The latter allows to transmit signals with low data rates, and only when there is relevant information in the input signal, thus reducing power dissipation. Asynchronous CT ATC can also be called time encoding machines (TEMs), as information is encoded in time.

It is possible to reconstruct the input signal from the output pulse stream as shown in [8–10], and [11], or work in time domain with the pulse output, doing pulse processing [12–20]. The IFC followed by input signal reconstruction requires higher energy consumption than a common ADC. Thus pulse processing should be used to achieve the lowest energy consumption possible.

The applicant did research for four years at the University of Florida Computational NeuroEngineering Laboratory (CNEL), that is making important progress in this direction. As for example:

1. fourteen years ago by developing the Florida Wireless Implantable Recording Electrodes (FWIRE), Bashirullah *et al.* [21],
2. Since 10 years ago until now, heart arrhythmia detection using IFC and pulse processing Alvarado *et al.*, and Nallathambi and Principe [12, 13],
3. IFC circuit development and output pulse reconstruction [9, 22–27],
4. pulse processing operations [15–17],
5. and developing a framework for learning from pulse output to create an automaton that allows signal characterization and classification in pulse domain [18–20].

During this time the applicant achieved the Master of Science in Electrical and Computer Engineering in the University of Florida and took various courses in integrated circuit (IC) design, very large scale integration (VLSI), nanotechnology, solid-state electronic devices, and micro-electromechanical devices. Doing research in CNEL and in strong collaboration with the Analog Mixed Signal Laboratory and the Integrated Circuit Research Laboratory, all from the University of Florida Electrical and Computer Engineering department.

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1.2 Research Question

This PhD thesis has the aim of answering the following Research Question:

What would be a suitable way to do a low power system on-chip (100's of μW) that performs advanced computations for low frequency signals (below 10 kHz) as the brain does, as for example pattern recognition - namely ECG complete Arrhythmia detection, or fully implanted closed loop BMI with brain signals complex interpretation; without the use of a general purpose CPU, or GPU?

1.3 Hypothesis

Considering the following Hypothesis:

One possible way is to develop a system on-chip for low frequency sparse signals, inspired by the brain, that uses neurotechnology and neuromorphic circuits. Creating an amplitude-to-time conversion with an integrate-and-fire converter (IFC) circuit, which gives a stream of pulses. That system can then use pulse processing to do computations with the output pulses, for example with an automaton - without using conventional DSP. If such kind of system is designed and prototyped then it may do these advanced computations with power dissipation below 100 μW. Because its pulse timing structure only has information for relevant input amplitudes, defined by the user, reducing the redundancy and lowering the hardware specifications.

1.3.1 Motivation

With such power dissipation, the system could be implanted in the brain as a battery less standalone device to compensate for loss brain function, or could be used as a small ECG recording and arrhythmia detection device that is in contact with the patient chest. Currently these kinds of devices do not exist for ECG, or have very simple functions in the case of BMI, due to the limitation in computation power of such systems on-chip.

1.3.2 Hipothesis development

With the scaling down of CMOS technologies, digital cells perform better than more complex analog blocks and can work at reduced voltage headroom. Is it possible to develop a standard cell-based (SCB) IFC circuit to perform well in advanced technology nodes, that can be synthesizable? If yes, it would also benefit from the simplicity of SCB circuit designs and could be implemented in widely available field programmable gate arrays (FPGAs), without requiring dedicated IC circuitry and tapeouts. Would this

IFC circuit have lower energy consumption, higher dynamic range and versatility than a conventional IFC circuit with analog blocks? Would the analog counterpart be more stable and robust than the SCB circuit version?

To verify this hypothesis this dissertation presents and compares two CT asynchronous ATCs that do not require an external clock signal. These are two low-power IFC solutions, one analog and the other a fully-digital - SCB, dynamic IFC that works in the analog domain. The first is a closed-loop analog IFC with conventional blocks and on-chip capacitors, although not sacrificing either the chip area or power. The latter, is an open-loop IFC with digital blocks, fully synthesizable and dynamic as each individual block can be powered off. Both can be used as an analog frontend (AFE) without requiring external blocks. Being fully-differential - the analog solution is fully-differential, the digital one is pseudo-differential, it also benefits its performance in AFE applications. As both systems are asynchronous, having a low power dissipation, and with pulse outputs with low data rates, they are a good solution for edge applications, such as low-power sensors AFE interfaces in internet of things (IoT) applications.

1.4 Document Structure

This dissertation is organized as follows. Chapter 2 presents the state of the art (SoA) of IFC TEM and similar ATCs in section 2.2, section 2.3 presents a summary of input signal reconstruction methods and section 2.4 how to extract features about the input signal from the pulse outputs in time domain, finally section 2.5 presents a summary of the proposed work. Chapter 3 presents the circuits design with a IFC sampler introduction, 3.1.1, the design, sections 3.2 and 3.2.1, and the specific design of the analog IFC in section 3.2.2 and the design of SCB IFC in section 3.2.3. Chapter 4 presents the integrated prototypes and results. Section 4.1 presents the integrated prototypes, section 4.1.1 the design of the testing print circuit board (PCB), section 4.1.2 the input signal reconstruction details and measurement requirements, section 4.2 the analog IFC simulation 4.2.1 and measurement 4.2.2 results, section 4.3.1 the SCB IFC simulation 4.3.1 and measurement 4.3.2 results, section 4.5 presents the comparison between the analog and SCB IFC versions, section 4.6 the proposed IFCs *versus* the SoA, and finally section 4.7 the prototypes and testing PCB future improvements. Followed by the conclusions and future work drawn in Chapter 5.

This document was written based on João Lourenço's NOVAthesis LaTeX template (NOVAthesis) [28].

1.5 Original Contributions

Up to date, two papers related to this work have been published by the author [2, 3]:

1. M. Lima Teixeira, J. P. Oliveira, J. C. Príncipe, and J. Goes, "A Standard-Cell-Based Neuro-Inspired Integrate-and-Fire ATC for Biological and Low-Frequency Signals" in 2023 IEEE Biomedical Circuits and Systems Conference (BioCAS).

2. M. Lima Teixeira, J. P. Oliveira, J. C. Príncipe, and J. Goes, "A Standard-Cell-Based Neuro-Inspired Integrate-and-Fire Analog-to-time converter for Biological and Low-Frequency Signals - Comparison with Analog Version" in IEEE Transactions on Biomedical Circuits and Systems Journal, published July 4, 2024), invited paper from 2023 BioCAS, Toronto.

2

State of the Art

2.1 Introduction

This Chapter presents the state of the art (SoA) of integrate-and-fire converter (IFC) samplers, a specific type of continuous time (CT) analog-to-time converters (ATCs), also called time encoding machines (TEMs).

The IFC was originally developed as a neuron model, as it is inspired by the behavior of individual neurons. There are at least three distinct methods to analyze an individual neuron: detailed model, overall morphological model, and overview model. The detailed model consists in the membrane ionic transfer equations - differential equations that translate the membrane ionic exchange behavior of an individual cell (Hodgkin-Huxley Model [29]). The overall morhpological neuron cell behavior model (MNCLM) describes each "main block" of the cell: dendrite, soma, and axon. The overview model describes the output to input signal relation of the neuron, treating the neuron as a transfer-function. The MNCLM is focused on the description of the neuron main signal through each of its individual blocks: input signal integration in the dendrites, comparison in the soma and action potential - also named spike or pulse, transmission in the axon. This work is based on the MNCLM and its implementation in standard complementary metal-oxide-semiconductor (CMOS) electronics.

The neural signal paths in a neuron are compromised of several distinct signals, generated by ion flows in each of the neuron structures. The action potential is usually consider the main signal in the neuron that is created by the soma, but there are other very important parallel signals as: calcium accumulation in the synapse region, ion regulation in the axon membrane, and signals that allow direct communication between the external medium and the nuclei/soma through neuromodulation and transmission of

control messages between cells.The neural signal that creates action potentials is transmitted from neuron to neuron through synapses that occur in the vicinity of dendrites of the following neuron(s). A synapse in the end of a neuron axon creates an electrostatic potential variation in the extracellular medium surrounding the axon, through the influx and out flux of ions from the end of the axon. This extracellular medium voltage variation consists in the beginning of the neural signal that then passes from the extracellular aqueous medium electrostatic potential through ions currents that flow from the exterior of the cell - next neuron, to inside its dendrites, through ion channels. Then the current in the neuron dendritic tree is integrated and low pass filtered in a resistor capacitor (RC) network created by the characteristics and arrangement of the dendritic tree. This integration done by many dendrites contribute to an increase of the voltage in the base of the dendritic tree, next to the soma. When this base voltage crosses a certain threshold voltage, different for each type of neuron, the soma fires and action potential that flows through the axon. The action potential consists in a voltage signal that propagates for relatively large distances, the length of the axon, with very little signal loss, because ion currents flow, transversely to the voltage signal propagation, through ion channels to the exterior of cell. This exchange of ions between the interior and exterior of the cell and special segments of the axon, allow the propagation of the signal with almost no signal loss. The action potential when reaches the end of the axon creates a synapse that will affect the dendrites of the surrounding neurons and this process repeats in these neurons.

2.2 Analog-to-time converters / Time encoding machines

Based on the MNCLM, Carver Mead explored methods to relate electronic circuits and neuron modeling [30].

Figure 2.1 presents Carver Mead's [30, p. 198] textbook picture of his original spiking neuron hardware model. It consists of an axon-hillock circuit with a capacitor voltage-divider with the addition of a self-reset. This way it can recover to the initial condition and fire more than once. It should be noted that, in all schematic drawings in this dissertation, crossed lines are connected and a bridge is drawn when a crossing is not connected.

The axon-hillock circuit consists of an input capacitor plus two inverters (M1-4) with a positive feedback through an integrating capacitor. The input current, I_{in}, is integrated in C_i increasing the input voltage v_i and so v_o. When v_i crosses a certain threshold

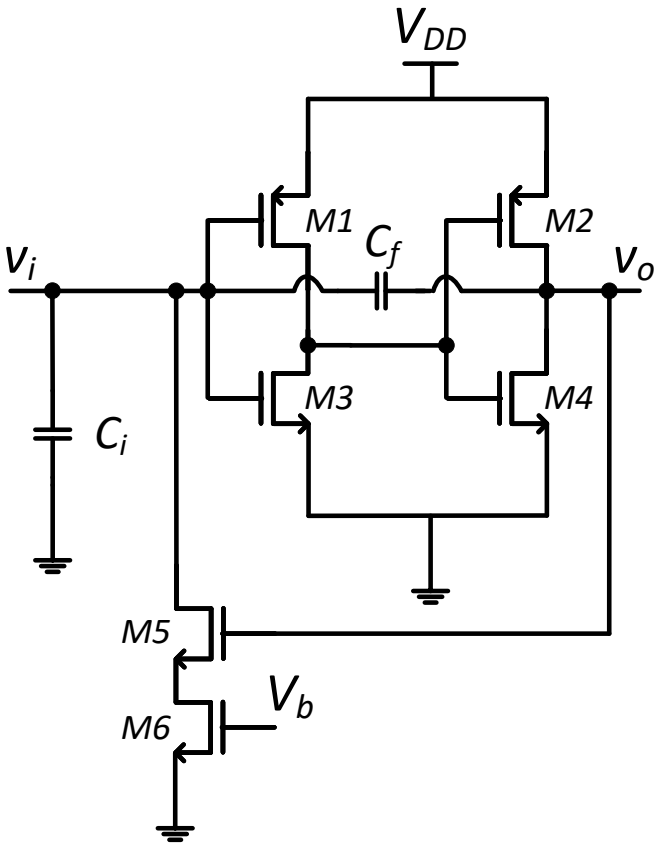

Figure 2.1: Original Spiking Neuron model obtained from Carver Mead's book [30, p. 198].

the positive feedback makes v_i increase further and so v_o increases rapidly, creating a drastic change in v_o and a pulse is generated. Although v_o changes from ground to V_{DD}, when a pulse is generated, the input voltage only increases by ΔV_i, equation (2.1), due to capacitive division, [30, p. 199].

$$\Delta V_i = V_{DD} \frac{C_f}{C_i + C_f} \tag{2.1}$$

The time that it takes the input current to charge the capacitors by ΔV_i is the time between pulses and is given by equation (2.2), [30, p. 200].

$$t_{low} = \frac{C_f V_{DD}}{I_{in}} \tag{2.2}$$

When a pulse is generated it discharges C_i and C_f through the reset transistor M5, that creates a leakage current I_{pl}. During the pulse the output voltage is constant and

it discharges v_i with the rate given by equation (2.3) as I_{in} is still trying to charge the capacitors.

$$\frac{dv_i}{dt} = \frac{I_{in} - I_{pl}}{C_i + C_f} \tag{2.3}$$

After certain voltage v_i the output voltage drops abruptly as v_i decreases, due to the positive feedback. The voltage v_i decreases by the equation (2.1). The pulse duration is given by equation (2.4), [30, p. 200] and can be controlled by V_b.

$$t_{hi} = \frac{C_f V_{DD}}{I_{pl} - I_{in}} \tag{2.4}$$

Equation (2.2) is also the refractory period, as during this time there are no new pulses, it is the time required to generate a new pulse.

This implementation has a fixed firing threshold that varies with process, voltage, and temperature (PVT). Moreover, if the input is close to the inverters mid point, both p-channel metal-oxide-semiconductor field effect transistor (PMOS) and n-channel metal-oxide-semiconductor field effect transistor (NMOS) inverter transistors are ON, increasing the power dissipation due to a short-circuit current. It also has a fixed refractory period.

The proposed analog IFC [3] has variable firing thresholds defined by the user, variable refractory period also defined by the user, and no short-circuit current due to the input voltage, as the input voltage is integrated with an operational transconductance amplifier (OTA) and isolated from the digital blocks. The proposed standard cell-based (SCB) IFC [2, 3] has fixed firing thresholds and refractory period, and also presents short-circuit current due to the input voltage, but it is fully synthesizable with the addition of a on-chip capacitor, while Carver Mead's neuron, Figure 2.1, is not.

The conventional IFC sampler circuit, Figure 2.2, consists in a current integrator. The current $i(t)$ charges the capacitor C_m, increasing the voltage v_{mem} (neuron membrane voltage), v_{mem} is then compared with a reference voltage V_{ref}, using an operational amplifier (OP-AMP) as a comparator, or a normal comparator. The comparator has two possible states: $v_{mem} = V_{ref}$ and $v_{mem} \neq V_{ref}$, when $v_{mem} = V_{ref}$ the comparator output is zero Volt and when $v_{mem} \neq V_{ref}$ the comparator output is a positive voltage that is approximately the positive voltage rail of the OP-AMP, because the OP-AMP tries to set the voltages in it is two input terminals to be equal. From now on we define v_{out} the voltage in the output node (Pulse) after the two inverters, that connect to C_f and the gate of the feedback

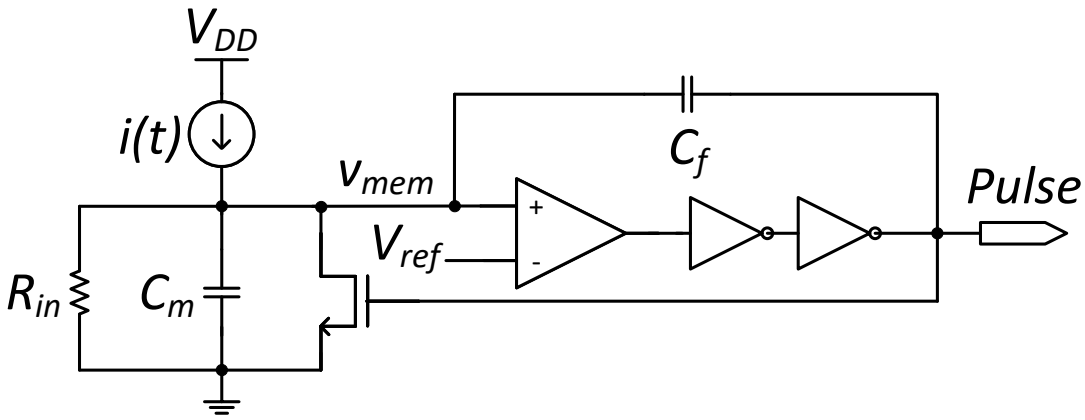

Figure 2.2: Conventional IFC Sampler.

transistor. When $v_{mem} \neq V_{ref}$ the output of the comparator, OP-AMP, is in the high state, meaning that the OP-AMP has a constant positive output voltage. The voltage difference between v_{mem} and Pulse output v_{out} charges capacitor C_f. This increase in charge creates an increase in the output signal and when v_{out} is larger than the threshold voltage of NMOS, V_T, the NMOS discharges C_m, grounding its terminals. This way, the NMOS transistor allows the charge reset of Capacitor C_m. After this discharge, $i(t)$ can again charge C_m and the process repeats and another pulse can be created. This process creates a voltage pulse in the output that is similar to an action potential in a neuron cell that propagates along the axon. The two inverters act as a buffer and add a delay to the time the OP-AMP takes to change between the two comparator states.

The OP-AMP has a positive feedback (path through C_f, connecting to the OP-AMP positive terminal), meaning that if there was no reset mechanism (reset transistor) the amplifier would not have an attenuation feedback path (negative feedback path) and so the OP-AMP would have an unstable behavior. In fact, a positive feedback can make a harmonic system positively reinforce it self and go for uncontrollable growing oscillation with time behavior and ultimately damage itself. This growing oscillation does not happen in this circuit due to the NMOS transistor that creates a negative feedback path, it ensures that after a certain v_{out} (Pulse voltage), the capacitor C_m is discharged, reducing v_{mem} and so the system returns to its initial stage.

Implementing this model on hardware requires the implementation of a current source that generates $i(t)$ to charge the capacitor C_m. This is a good neuron model, as the

current in the neuron dendritic tree is integrated and low pass filtered in a RC network created by the characteristics and arrangement of the dendritic tree - the path the signal has to travel can be thought as a resistance, main contribution for R, to the current propagation and the cell membrane all along the dendritic tubes contributes with a capacitance value, C, and also an parallel resistance to ground. But when implementing this circuit on hardware the current source has to be created, as most commonly the circuit source will be a non ideal voltage source and the sensors signals most of the times will be in voltage. There are several ways to do this voltage-to-current conversion:

1. the simpler way, with a resistor,
2. a voltage controlled current source with one NMOS transistor, the voltage in the gate of the transistor translates to a current I_D between the drain and the source, as in Figure 2.3, [31],
3. with a G_m operational transconductance amplifier (OTA), that converts voltage into current, as a normal OTA, as in [9, 26, 27].
4. A possible configurable solution with an controllable G_m OTA, analog frontend (AFE), with a G_m amplifier and a resistor in the feedback path.
5. Our proposed analog solution with and active RC integrator using an OTA [3]. The feedback capacitor is the integrating capacitor. The accumulation of charge in the integrating capacitor, increases the OTA output voltage that above a certain threshold, using a comparator, creates a pulse and discharges the integrating capacitor, resetting it.
6. Our proposed SCB solution [2, 3] with differential input cross-switching feeding an inverter-based amplifier - OTA, in open-loop topology. The integrating capacitor is in the OTA output.

A biology analogy with the neuron, to do this voltage to current conversion, can again be made, if one thinks how the neural signal passes from the extracellular aqueous medium electrostatic potential (voltage) to an ion current that flows from the exterior of the cell to inside the neuron dendrites. Both options 2 and 3 have a nonlinear behavior that affects the voltage to current conversion and so the accuracy of the RC value that in the worse case can affect the number of pulses, i.e., how many spikes *per* input wave

are created. In option 2, the transistor has a highly nonlinear behavior, it has a quadratic dependence, $I_d \propto {V_{GS}}^2$ and the direct current (dc) bias of the transistor affects its g_m (A/V) value possibly making it go to linear region, if the bias voltage decreases by some reason. The transconductor case, 3, is better than the transistors option, in terms of nonlinearity, but depending on how the transconductor is designed and the technology used, the linear range of the amplifier is limited to certain input voltage range. In fact usually this range in the best analog designs and with the correct technology choice (mainly affected by the technology voltage supply rails and transistors threshold voltages) can go roughly from 10 to 30 % of the negative supply and positive supply voltage difference. Choosing the design to improve this range has also trade offs mainly in power dissipation, amplifier noise, common mode rejection ratio (CMRR), and power supply rejection ratio (PSRR).

The Gm transcoductor used by Dazhi Wei, PhD Dissertation [26], Du Chen [9] and Manu Rastogi [27] consists in a current mirror cascode OTA [26, Fig.6-1 p. 72].

Sarpeshkar, Watts, and Mead present in [31] their sodium-potassium neuron circuit, Figure 2.3, with an OP-AMP, used as a comparator, to have variable firing threshold. It is based on the neuron detailed model and the transistors directly translate the neuron ionic behavior. Transistors M1-5 model the sodium conductance behavior, when the membrane potential, V_m, increases through I_{in} charging C_m, I_{M1} increases, increasing the mirrored excitatory sodium current I_{Na}. M1-3 form this way a positive feedback. M3, M4 and M7 are sized so $I_{Na} = 3I_{M1}$ and $I_{MC} = I_{M1}/3$ [31]. V_{Na}^{th} sets the firing threshold that is the sodium conductance activation threshold. V_{Na}^{max} defines the maximum current, I_{Na}^{max}, that controls the maximum sodium current and so the pulse (action potential) width. Transistors M8-9 model the potassium conductance behavior. Voltage V_N sets the activation state of the potassium conductance, that is coupled to the sodium conductance by I_{MC}. A larger V_N translates in a larger inhibitory potassium current I_K and in a neuron with larger refractory period. The refractory period is controlled by V_R. When $I_K > Iin + I_{Na}$ the action potential ends, as I_K pulls down V_M and resets the charge in C_m. For $V_m < V_{Na}^{th}$, I_{Na} and I_{MC} tend to zero. When V_N is small enough, $I_K < I_{in}$ the refractory period ends and I_{in} starts charging Cm again, it is then possible to occur a new action potential. It has positive feedback through M1 and M4, and negative feedback through M1, M3, M7, and M9. This neuron has variable firing threshold and pulse width, and refractory period control.

Schaik [32] presents a spiking neuron, Figure 2.4, with a single diode tied OP-AMP,

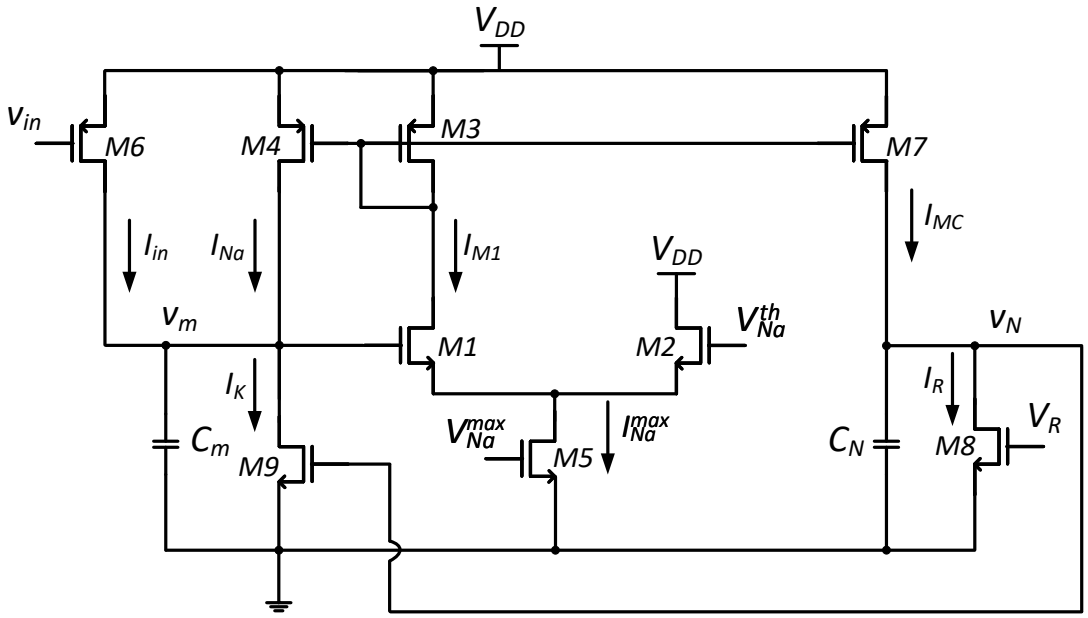

Figure 2.3: Sarpeshkar, Watts, and Mead's sodium-potassium neuron [31].

used as a comparator, to have variable firing threshold, as in [31]. It is based on Sarpeshkar, Watts, and Mead's sodium-potassium neuron circuit [31], being very similar, but has more flexibility. Again it is based on the neuron detailed model. It does not use the positive feedback created by the comparator left wing, as Figure 2.3, [31], which adds flexibility in controlling the neuron parameters. It has positive feedback created by: M1, M4, M9-10, and M5, and a delayed negative feedback created by the reset path: M1, M4, two inverters, M9-12, and reset transistor M6. The sodium current, I_{Na} is controlled by the output v_{out}. v_{out} stays at high voltage and drops when a pulse occurs in V_{inv2}, so it is an inverted pulse signal. I_{Kup} controls the pulse width and I_{Kdown} controls the refractory period. It also presents a leakage current, not present in [31], that is controlled by I_{leak}.

To have better power management than Mead's spiking neuron [30], Culurciello, Etienne-Cummings, and Boahen [33–35] developed a current-feedback latch that reduces the short-circuit power dissipation in the input stage, Figure 2.5. The current in the inverter M2-3 is mirrored by transistor M5, forming a positive feedback. v_{in} starts close to V_{DD} after a reset pulse, M2 is off, v_{out} is low and M6 is off. M7 is ON and capacitor C is charged. The photocurrent through the photodiode decreases the charge in C, decreasing v_{in} and so M2 starts conducting. Before reaching M2 threshold voltage, a subthreshold current flows through the inverter and feedback to the input through the

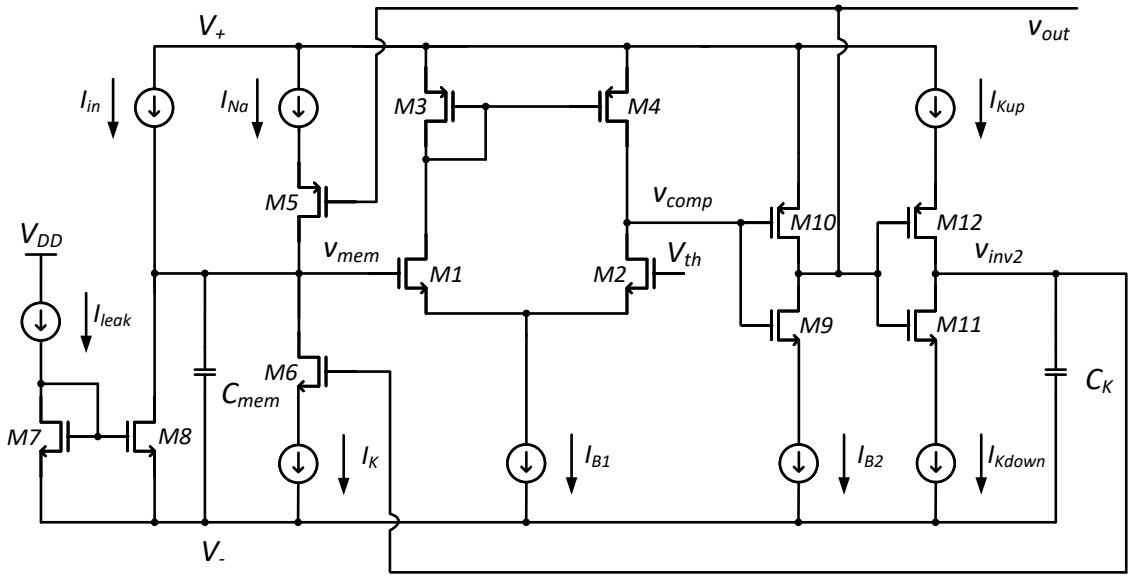

Figure 2.4: van Schaik Spiking Neuron model [32].

positive feedback, M4-6. The mirror current starts in subthreshold region but increases exponentially. The latch switching process starts when the feedback current is equal or larger than the photocurrent. At this point v_{in} is pulled to ground and v_{out} to V_{DD}, M7 turns off, accelerating the transition. When v_{in} decreases below M3 threshold voltage it turns off the current mirror feedback which turns of the current in M2-4 and pulls v_{out} to V_{DD} even further. The transition happens before M2 threshold voltage is reached [35]. This latch was designed to achieve a very fast transition and low power dissipation. The pulse ends with a external reset signal through M1. The very fast transition and external reset make this spiking circuit ideal for optical circuits, being different from the other presented IFCs.

In a IFC the average pulse rate is proportional to the input signal amplitude and inversely proportional to input signal frequency. This way, to make a fair comparison between IFCs, the same input signal conditions should be used, to be able to compare power dissipation, average firing rate, and signal-to-noise-and-distortion ratio (SNDR), if there is reconstruction from the pulse output. If that is the case, a possible comparison is to use conventional analog-to-digital converter (ADC) Figure of Merit (FoM), considering [27, p. 69] equation (also presented in [25]), equation (2.5), and the condition of 2 times bandwidth (BW), as there is no sampling frequency for asynchronous IFC (f_{sample}), if

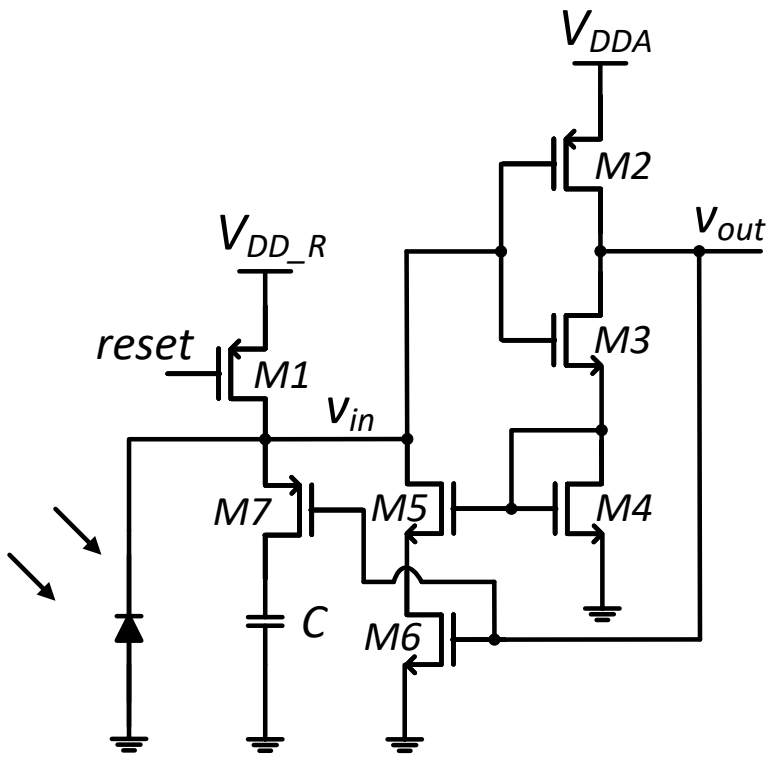

Figure 2.5: Culurciello, Etienne-Cummings, and Boahen IFC pixel for image sensor [33–35].

effective number of bits (ENOB), or SNDR is know. As in some cases the ENOB or SNDR was not presented, or measured (for example, if there is no recontruction) and as it is not possible to test all IFC systems with same input conditions, the energy *per* pulse consumption was calculated for each prototype, for a fairer comparison. The energy *per* pulse was calculated for the presented average firing rate, or stated otherwise, considering equation (2.6). The firing rate is defined as the number of output pulses in a certain time window divided by the time of a that time window, equation (2.7). The different available values are presented in this dissertation, although the comparison should be done taking in account all these factors.

$$\text{FoM} = \frac{Power}{2^{ENOB}\ min\ (f_{sample},\ 2BW)} \quad [Joule/conversion-step] \tag{2.5}$$

$$Energy\ per\ Pulse = \frac{Power}{Firing\ Rate} \tag{2.6}$$

$$Firing\ Rate = \frac{Number\ of\ Output\ Pulses\ in\ a\ Time\ Window}{Time\ of\ the\ Time\ Window} \tag{2.7}$$

The energy *per* pulse can also be defined as the amount of energy consumed to generate a single pulse. To differentiate from the previous definition we define it as energy *per* single pulse. The energy *per* single pulse can be calculated using, for example, equation (2.8), where $Pulse\ Width$ is the pulse width in time domain. The energy *per* pulse values presented in this dissertation text and tables are calculated considering the definition generally used in the SoA, equation (2.6).

$$Energy\ per\ Single\ Pulse = Power \times Pulse\ Width \tag{2.8}$$

Indiveri presents an ultra low power IFC [36] with refractory period programmability and spike frequency adaptation. It uses [33] current-feedback latch, but with current mirroring in the PMOS transistor side. It has an average power dissipation of 300 nW, with 10 Hz average firing rate, and a maximum power dissipation of 1.5 μW, in a a 5 V, 1.5 μm CMOS technology. The circuit is shown in Figure 2.6. The circuit compromises a source follower, M1, to increase the linear integration range, a inverter-based positive feedback latch, M3-6 and M8, (as [33–35]) to reduce the short-circuit currents at the input, a current starved inverter, M9-12 to control the refractory period, a normal inverter, M13-14, that creates the digital pulse, a reset transistor, M7, a transient current mirror integrator to have pulse frequency adaptation, M15-19, and a transistor to set the leakage current, M20 [36]. V_{rfr} controls the refractory period and V_{sf} through M2 controls the threshold voltage. V_{adap} sets how much V_{ca} increases with each pulse, as it sets a current amplitude that charges the parasitic capacitance sourced by V_{ca} [36]. This mechanism sets the spike frequency adaptation.

Livi and Indiveri present a phenomenological IFC [37] based on the detailed neuron model, that consists in a expansion of Idiveri's circuit [36], Figure 2.6, with a current based differential pair integrator in the input to implement adjustable dynamic conductances. It consumes 271 pJ/spike, 100 ms spike duration considering current integration phase (10 Hz average firing rate), with 350 nm CMOS technology and 3.3 V supply. Being one of the best IFC in terms of power dissipation, 2.71 nW at a biologically plausible firing rate [27, 37]. Both Indiveri's [36] and Livi with Indiveri's [37] circuits can operate

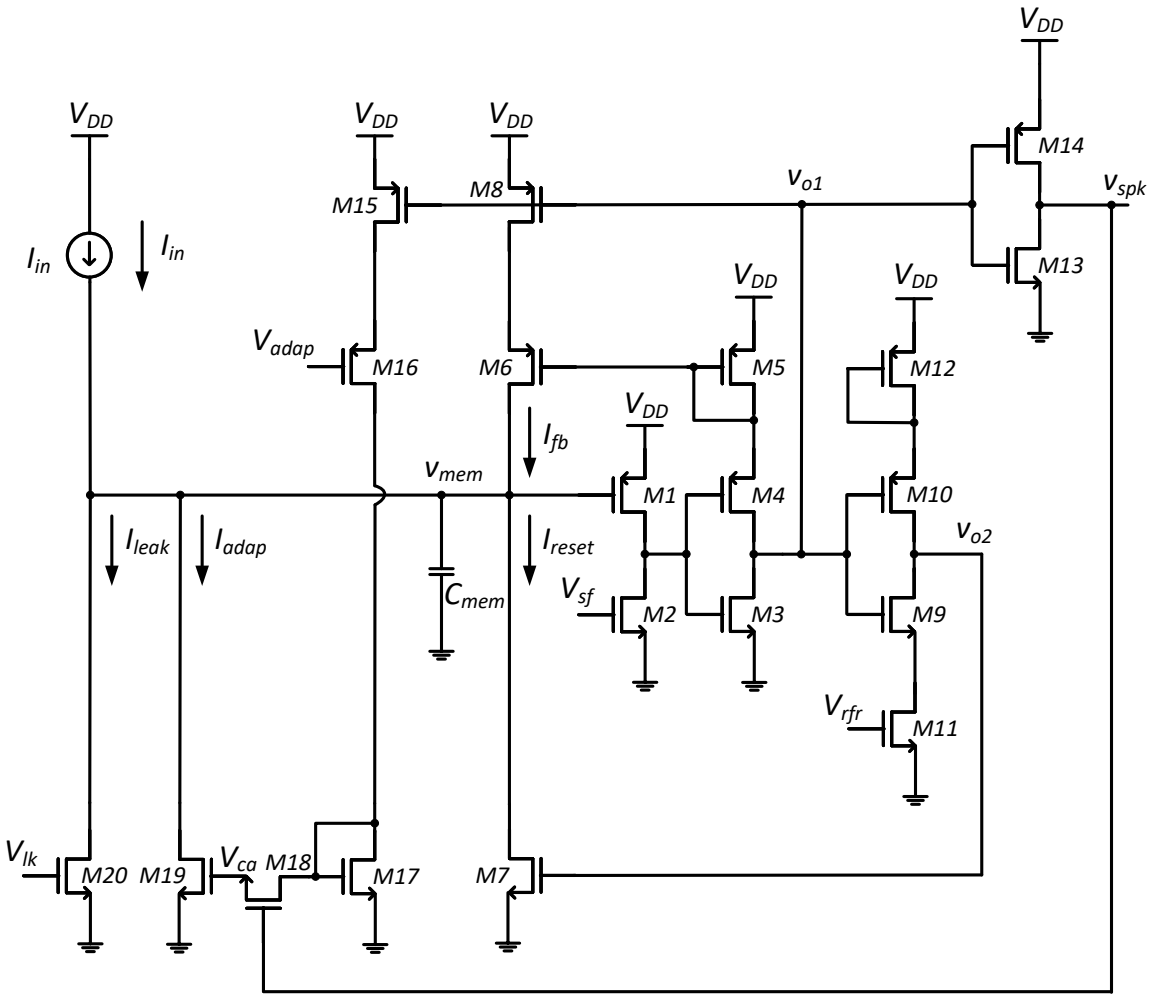

Figure 2.6: Giacomo Indiveri Spiking Neuron [36].

in biological plausible timings due to the spike frequency adaptation mechanism and refractory period control, with low power dissipation.

The proposed analog and SCB IFC solutions, although being more complex and with higher power dissipation than [36] and [37], they are biphasic and capable of being used as AFE. This is also an advantage, when comparing with [31] Figure 2.3, [32] Figure 2.4, and [33–35].

Computational NeuroEngineering Laboratory (CNEL), at the University of Florida, developed several IFCs [9, 10, 22–26]. Dazhi Wei [26, p. 76] presents a spiking neuron, Figure 2.7, using two [33–35] current-feedback latches, with current mirroring in the PMOS transistor side. It consists of an OP-AMP, M1-6, with a current-feedback latch M7-12, a delay block with a current-feedback latch M13-22, and auxiliary and bypass

circuits M23-27.

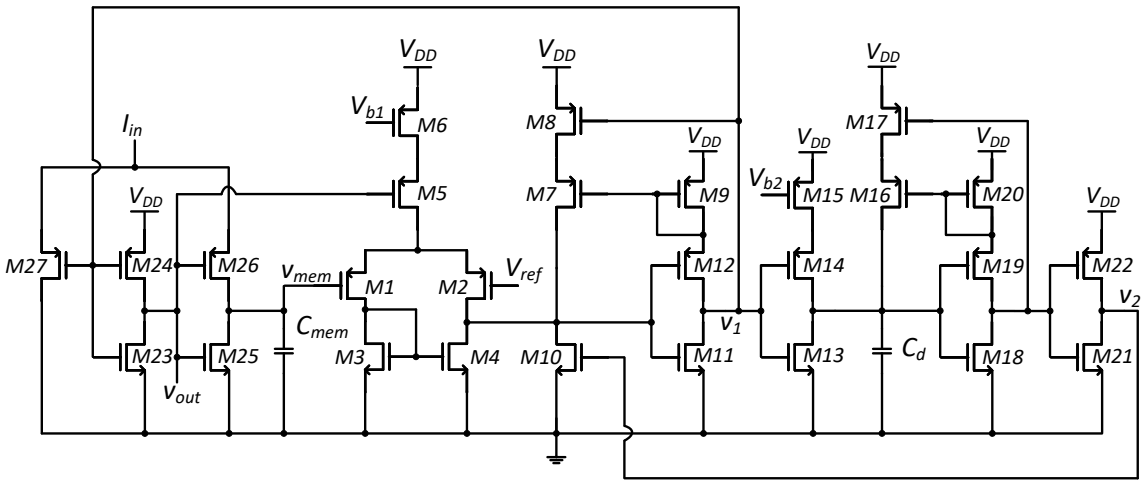

Figure 2.7: Dazhi Wei IFC neuron [26, p. 76]

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Assuming that initially v_{mem} and v_{out} are low, M26 is on, M27 and M25 are off. I_{in} from the previous OTA starts charging C_{mem} and so v_{mem} starts to increase. M5 is also ON and so the OP-AMP is working as a comparator. When v_{mem} becomes larger than V_{ref}, the OP-AMP output (drain of M4,10) becomes closer to the current-feedback latch threshold, threshold voltage of M11, v_1 is pulled quickly to ground by the current-feedback latch - with the positive feedback as explained for the [33–35] latch but reverse as it has PMOS current mirror, and so v_out is pulled quickly to V_{DD}. M26 is now off, M27 is on, and I_{in} is bypassed by M27. M25 is ON and discharges C_{mem} decreasing v_{mem} to ground level. As M5 is off the OP-AMP is off and v_1 and v_{out} are not affected by v_{mem} going low. Since v_1 is low, M14 is ON and C_d is being charged by I_D of M15, controlled by voltage V_{b2}. After some time - the delay created by this block, C_d top plate voltage gets close to M18 threshold voltage and activates the following current-feedback latch (M16-20), M18 drain voltage goes quickly to ground and C_d top plate voltage goes quickly to V_{DD}, by positive feedback. And so v_2 goes quickly to V_{DD} also pulling the drain voltage of M10 to ground (OP-AMP output) and making v_1 high and so v_{out} goes low. So now M26 and M5 are ON and M25 and M27 are off. The OP-AMP is back ON and current I_{in} starts charging C_{mem} again. As v_1 is high, M13 is now ON and it quickly discharges capacitor C_d, making v_2 low and so turning off M10, the circuit is now again in the initial condition, [26, p. 76]. The pulse width is defined by the delay. The power dissipation of this neuron

circuit is 45 µW for V_{DD} = 5 V in 0.6 µm CMOS technology, [26, p. 80]. With a FoM of 2.2 pJ/conv-step, FoM was calculated considering [27, p. 69] equation (also presented in [25]), equation (2.5), and the condition of 2 times BW as there is no sampling frequency for asynchronous IFC (f_{sample}) and data from [26, p. 83], ENOB equal to 10 bits.

Although the power dissipation is close to the proposed IFCs, for an older technology node, the proposed analog and SCB IFCs have the advantage of being biphasic, fully and pseudo-differential, respectively, and less sensitive to PVT as it does not use pseudo-resistors, as will be explained next.

Du Chen *et al.* developed a CMOS implementation of a biphasic IFC, as shown in Figure 2.8, [9] and [10, p. 96], with positive and negative thresholds and with refractory period control. That is an extension of the conventional single-phase IFC, shown in Figure 2.2, using two comparators [10, p. 97], with input shifted by a common-mode (CM) voltage V_{mid} and with positive and negative firing thresholds relative to this CM voltage. This way, the IFC only fires when there is relevant information in the input signal. For a conventional single threshold (single-phase) IFC, the input signal has to be strictly positive. Hence, a positive bias has to be added to the input signal. This way the IFC creates pulses permanently, as the IFC charging is relative to ground. Even when the input is constant at the added biasing voltage, meaning at idle level, or at zero level, before adding the positive bias [10, p. 75], wasting energy. The biphasic IFC is then a major improvement to a conventional single threshold IFC and optimizes energy consumption.

The input voltage is converted to $i(t)$ through a G_m OTA, as referred before. This current can charge C increasing v_{mem}, or discharge C decreasing v_{mem}. When $i(t)$ is positive, it charges C, increasing v_{mem}. When $v_{mem} > V_{thp}$, a pulse is fired in $P_{outp}(t)$ that makes the reset signal r high through a OR gate, discharging C through a CMOS transistor to V_{mid} level. The pulse $P_{outp}(t)$ ends when v_{mem} becomes smaller than V_{thp}. If $i(t)$ is negative, it discharges C, decreasing v_{mem}. When $v_{mem} < V_{thn}$, a pulse is fired in $P_{outn}(t)$ that again makes r high, charging C back to V_{mid} level. The pulse $P_{outn}(t)$ ends when v_{mem} becomes larger than V_{thn}. It has a power dissipation of 100 µW for 5 V supply in 500 nm CMOS technology, achieving ENOB of 7 [10, p. 107] for a 10 kHz BW. This gives a FoM of 39 pJ/conv-step, calculated considering again [27, p. 69] equation (also presented in [25]), equation (2.5), and the condition of 2 times BW.

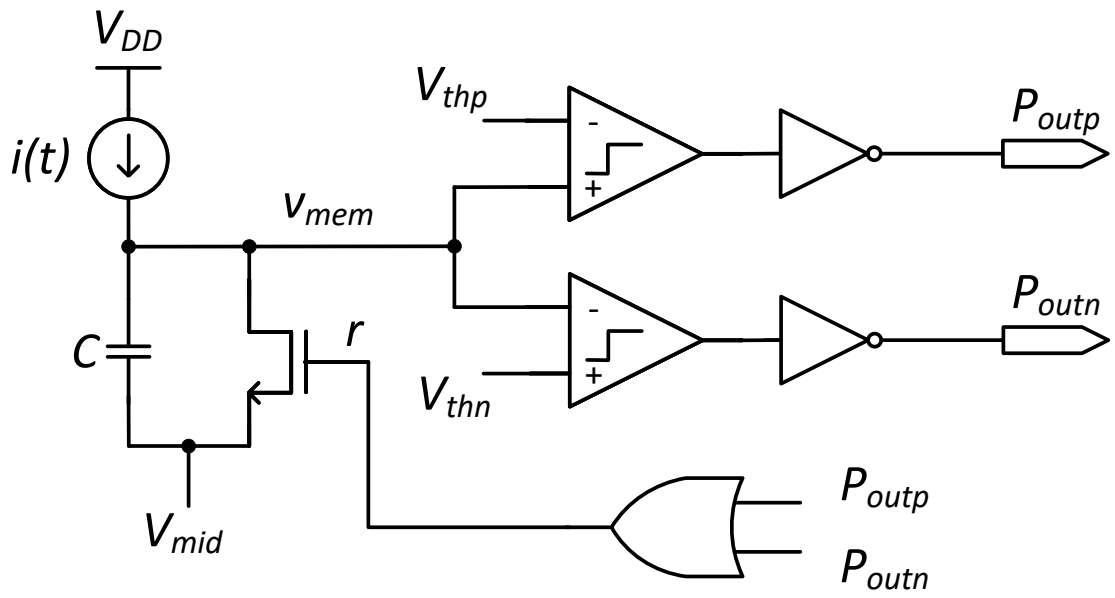

Figure 2.8: Du Chen's *et al.* biphasic IFC [9] and [10, p. 96].

Du Chen also presents a monophasic IFC solution [10, p. 74], [9], similar to the conventional IFC, Figure 2.2, that consumes 300 µW (total power dissipation considering the bio amplifier power dissipation, referred next) in 500 nm technology, achieving a ENOB of 13 for a 5.4 kHz BW. This represents a FoM of 2.5 pJ/conv-step, considering only the IFC with OTA conversion power 300 – 80 µW = 220 µW. And developed two bio amplifiers, one for action potentials and local field potentials (LFP)s measurement, and the other for action potentials measurement, doing *in vivo* measurements. The bioamplifiers are based on the popular Harrison's amplifier structure [38] with an OTA and pseudo-resistors [10, p. 20], [9]. Both bioamplifiers have 39 dB gain, input referred noise of 5.94 μV_{RMS} and BW of 0.3 Hz to 5.4 kHz for the first one and 4.93 μV_{RMS} and BW of 102 Hz to 5.4 kHz for the latter, consuming both 80 µW for a 5 V supply in 500 nm CMOS technology [9], [10, p. 32 and p. 34]. This bioamplifier together with the monophasic IFC with OTA voltage to current conversion was protototyped and creates a complete AFE channel for action potentials and LFPs measurements. Being able to measure input signals with tens of µV, consuming 300 µW/channel in 500 nm technology.

For brain-machine interface (BMI) applications, in particular with intracranial recording, the AFE has to have input referred noise below around 5 μV_{RMS} as the recorded

signals have amplitude of tenths of μV. All the IFC presented here require a previous AFE block that has this low input referred noise level. The monophasic IFC developed by [10] is the only one prototyped with the required preamplifier block, to record intracranial neural signals.

The proposed analog and SCB IFC versions are also biphasic, but are more robust than this biphasic solution as they do not use pseudo-resistors in the voltage to current conversion, as will be explained next.

Rastogi [27] presents a new CNEL biphasic IFC circuit, also similar to the conventional IFC, Figure 2.2, with refractory period control (V_{delay}), Figure 2.9, trough a starved inverter, M17-19, but using a different comparator, M1-12, from [9, 10] and changing the refractory period control location. The refractory period control was moved from the pulse high voltage period to the pulse low voltage period. In the first case the refractory period control drives an inverter, which would have an increased short-circuit current consumption due to the refractory period, in the second case, the refractory period control drives the reset transistors, Figure 2.9. Passing the refractory period to the pulse low voltage period avoid this short-circuit current period.

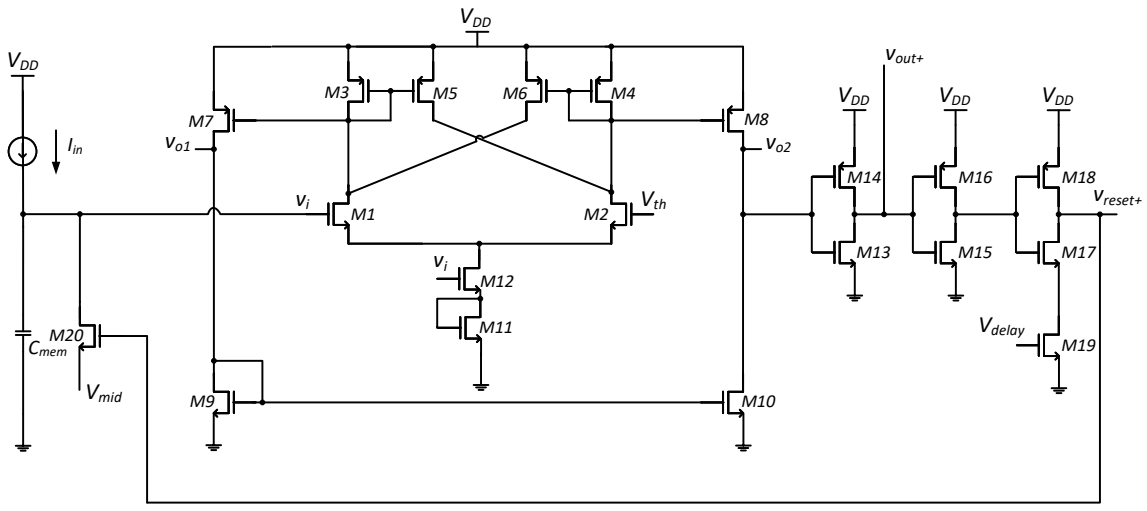

Figure 2.9: Adapted from positive channel of Manu Rastogi's IFC Spiking Neuron with dynamically biased comparator [27, p. 45, p. 57]. Adapted comparator with M11 connected to ground instead of V_{ctrl}, as in [27, p. 57].

Three versions of this IFC were implemented: one with a fixed bias comparator, one with a dynamically biased comparator, and one with a current limited dynamically biased comparator. The presented version has the dynamically biased comparator, that

turns off (or reduces substantially the bias current) when voltage v_i is below a certain voltage threshold, through tail transistor M12. Using the same transconductor as [10, 26], as a current input to the IFC sampler, as also a new energy harvester circuit with 26 % efficiency to recover the energy used to charge the main capacitor after each pulse. This energy harvester has a small chip area footprint, but it has the drawback that it uses two large 100 nF off chip capacitors, due to their value and size, that work as ping pong buffers. And is lacking a voltage regulator to efficiently return the harvested energy back to the IFC. These circuits were developed having the goal of achieving the lower energy consumption *per* pulse possible. The FoM obtained was 0.6 pJ/conv-step, [27, p. 70]. A study developed estimates that the minimum energy consumption *per* pulse possible for IFC circuits (lower bound) is of the order of tenths of fJ. This estimate was done disregarding the static power dissipation. Because, citing Manu Rastogi's work: "At lower pulse rates the static power dissipation (power consumed in between pulses) is high resulting in an higher energy pulse/pulse for lower pulse rates.", Rastogi's PhD dissertation, [27, p. 113]. Rastogi's solution for the IFC main conversion circuit implements a 20 pF charging capacitor, named C_m (membrane capacitor) in one side of the differential comparator.

The proposed analog IFC circuit also uses a starved inverter to obtain refractory period control as [27], Figure 2.9. This starved inverter delay element, was proposed by [39]. It also uses a dynamically biased comparator with the addition of a tail transistor controlled by the input, inspired by Rastogi's comparator version.

Previous CNEL developed versions [9, 10, 22, 23, 26, 27] can be sensitive to PVT variations as they use an OTA with pseudo-resistors in feedback to transform the input voltage in current, that is then integrated in a capacitor. The issue of using a transconductor with pseudo-resistors is that, first the pseudo-resistor show large variation in resistance value from chip to chip and second they are quite sensitive to PVT variations. And so it can change the sampler results for the same input, when V_{DD} voltage or temperature varies. As well as, if the fabrication process has tiny variations in the feature sizing from chip to chip, as it is usual does, two IFC samplers from different chips, will not have the same output for the same input even with no change in temperature and V_{DD} voltage.

The proposed analog IFC design is more robust than these previous circuits as it is fully-differential and it does not relay on pseudo-resistors. Instead it has an active RC integrator with an integrated CMOS resistor, with a high-gain OTA.

Yen and Harris [40] present an adaptive IFC circuit. It adds an adaptive component to previous CNEL IFC circuits that creates an adaptive firing threshold. This is more robust than the adaptation presented by [36]. [36] adaptation consists in using a leaky current from the integrating capacitor ($Iadap$ in Figure 2.6). When a pulse is fired the leakage current is increased by $Iadap$ removing some charge from the integrating capacitor C_{mem}. [40] adapts the threshold value in accordance with the firing rate. Meaning that the firing threshold value is know for [40] and not for [36] due to the variable leakage. And so input signal reconstruction is possible for this new adaptation mechanism [40] and it is not so feasible for [36]. In other words, input signal reconstruction for [36] would give larger reconstruction errors than [40].

Table 2.1 presents a first IFC prototype comparison with detailed comparison for CNEL prototypes. Again, as referred previously, the presented power dissipation, average firing rate, SNDR is not for the same input signal conditions. The comparison should be done taking in account all these factors and FoM, if available. This way, for a fairer comparison the energy *per* pulse consumption was calculated for each prototype.

Patil *et al.* [45] present a low power 10 MHz CT ADC that consists in an ATC with off-chip reconstruction of the original input signal from the output time series. It uses a simple comparator block that requires calibration, complex clocks, and offline time. It has a simple comparator block with four inverters that requires calibration every 2 ms, that lasts 1.5 µs, to set up the comparator threshold. This calibration scheme requires 3 signals similar to clocks. This increases system complexity due to the comparator choice. As referred, another comparator could be used in the same architecture. This means the sampler has an offline time and is not sampling the signal every 2 ms, which could be a constraint in some applications. In the proposed asynchronous SCB IFC solution the comparator is based on a NAND latch, not requiring any calibration. Therefore, the sampler does not have offline time. Moreover, the system becomes simpler, by not requiring clocks or control signals. It only uses a nominal power supply. Instead of resetting the integrating capacitor, the differential input is switched in the amplifier input ports. As in chopping, this way the capacitor is discharged.

Previously other IFC circuits have been developed that require an external reference signal or clock, as in [46]. The proposed analog and SCB IFC circuits do not require a clock.

Indiveri and Linares-Barranco [47] present a good review of neuromorphic circuits.

Table 2.1: IFC Prototype comparison with detailed CNEL prototypes

Work	[36]	[37]	[41]	[42–44]	[26]	[10]	[10]	[24, 25] [27]
Phases	Mono	Mono	Mono	Mono	Mono	Mono	Bi	Bi
Technology node (nm)	1500	350	180	180	600	500	500	600
Supply (V)	1.75-5.0	3.3	1.8	1.8	5	5	5	5
Area (mm^2)	-	0.001	$0.18_{(a)}$	-	0.018	0.093	0.036	-
SNDR (dB)	-	-	-	-	$59_{(b1)}$	$80_{(b2)}$	$44_{(b3)}$	$57_{(b4)}$
Input BW	-	-	3 Hz-2.5 kHz	0.8 Hz-10 kHz	10 kHz	5.4 kHz	10 kHz	-
Total Power (µW)	0.3-1.5	0.003	55 @ 100 Hz	$27.3_{(c)}$	45	220	100	1.2
Energy *per* Pulse (pJ)	3 $\times 10^4$	-	5.5 $\times 10^5$	-	1364	-	-	10 @ 200 Hz
Average Firing Rate (kHz)	0.01	0.01	0.1	-	33	-	47	40
FoM (pJ/conv-step)	-	-	-	-	$2.2_{(d1)}$	$2.5_{(d2)}$	$39_{(d3)}$	0.6
Prototyped	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Spike frequency adaptation	Yes	Yes	No	Yes	No	No	No	No
IFC as AFE Block	No	No	$No_{(e)}$	$No_{(e)}$	Yes	$Yes_{(f)}$	-	No

(a) Total area with low noise amplifier, bandpass filter, delta modulator ADC and pulse ADC, analog trough and peak detector. (b) Signal-to-noise ratio (SNR) and not SNDR, (b1) from [26, p. 83],(b2) calculated from ENOB 13 [10, p. 74] and 7 [10, p. 107] for (b3), considering $SNDR = 6.02\ ENOB + 1.76\ dB$, (b4) from [24]. ($c$) 27.3 µW average and 0.096 µW static power dissipation. (d) FoM was calculated considering [27, p. 69] equation (also presented in [25]), equation (2.5), and in the condition of 2 times BW as there is no sampling frequency for asynchronous IFC (f_{sample}) and data from: (d1) [26, p. 83], ENOB equal to 10 bits, (d2) [10, p. 74], ENOB equal to 13 bits, and (d3) [10, p. 107], ENOB equal to 7 bits.
(e) Requires a low noise amplifier (LNA) and analog filters. (f) With an included integrated bioamplifier (total power dissipation of 300 μW) for action potentials and LFPs.

Table 1, [47, Table 1], in this review categorizes well the main silicon neuron computational blocks and the different circuit design styles. These type of circuits are based on the detailed model and so emulate the brain to the detail of ion channels, being a transistor channel equivalent to an ion channel, that is a different approach from the one proposed in this dissertation.

Arthur and Boahen's paper [48] presents a design method to achieve the desired silicon neuron circuit from response equations, applying a dynamical systems approach. Watson *et al.*'s work [49] shows the advantages of using a network of several IFC neurons to process higher frequency signals with IFC circuits that fire at much lower firing rates than

the input signal frequency. A SNR reduction from modulation of, rate coded, coupled neuron population network is also shown in Mar *et al.*'s paper [50]. This allows the uses of unsynchronized, slower, and unprecise individual IFC neurons to process higher frequency signals, similar to what is believed to occur in brain processing. This approach could allow processing signals with frequencies higher than the maximum switching frequency of the fastest CMOS devices available. Sahoo [51] presents a ring oscillator based IFC circuit with programmable refractory period and spike frequency adaptation.

The IFC circuit based on Indiveri's IFC [36], as well as more recent versions [41, 47, 52, 53], are included in neuromorphic systems with different applications, as for example pattern recognition in biological signals (neuronal local field potentials, intracranial electroencephalogram (EEG), and electrocardiogram (ECG)) [41, 43, 44, 54], or classification of visual symbols [42]. Some of these IFC, based on [36], were further improved taking in consideration the neuron detailed model, with blocks that modulate each individual cell ionic transfer mechanism and behavior [52, 53].

Two single-ended IFC neuron models that use an OP-AMP with integrating capacitor in feedback, followed by a comparator, have been proposed for resistive synaptic neural networks with synaptic learning by Serrano-Gotarredona and Linares-Barranco [55] and Wu, *et al.*, [56]. Both IFC neuron models implementations have similarities to the proposed analog IFC, but there is no detailed information available to make a better comparison. Wu *et al.*'s neuron model [56] has been prototyped in an 180 nm CMOS technology node with an area of 0.01 mm^2 *per* neuron, and with energy consumption of 9.3 pJ/spike/synapse for synaptic plasticity (1000 resistive synapses with 1 MΩ each). It has shown spike time dependent plasticity associative learning with three neurons.

A digital IFC neuron is presented in [47, 57], which is quite different from the proposed SCB IFC. It performs the neuron function by using digital logic and operations, while the proposed SCB IFC reproduces the analog IFC behavior, using digital blocks that perform in the analog and mixed-signal domains. Another work with a digital IFC neuron is presented in [58] and compared with an analog IFC. It also performs in the digital domain with spike/pulse input and output. It follows a synapse block that can be excitatory, or inhibitory to the neuron. The neuron has digital counters to increase or decrease the membrane potential and count the leakage period, if there is no synapse, together with a comparator block, [58, Fig. 5]. The analog IFC presented and compared with the digital IFC in this work [58], was presented previously in [59]. It uses a clocked

comparator and these IFCs were design for neuromorphic signal processing in high speed applications. Both designs are clocked and the pulse input is clocked at 500 MHz, the digital IFC runs with a 256 MHz clock. This way, both systems can be considered to be synchronous. Both analog and digital IFC are similar with the same block structure, to have a fair comparison. Both operate at a maximum pulse rate of 1.9 MHz the digital has an energy *per* pulse of 41 pJ and the analog 2 pJ in a 65 nm technology node. The analog IFC occupies 5 times less area and consumes 20 times less energy *per* pulse than the digital IFC. It is predicted in [58] that the analog IFC would still have an energy *per* pulse at least 3 times smaller than the digital IFC in a 22 nm technology node, with both occupying a similar area.

A synchronous IFC array is presented in [60] with 256 IFCs and an energy *per* pulse consumption of 1.52 pJ. Each IFC has an high gain OTA with reconfigurable feedback loop, presenting multiple operation modes. It has correlated double sampling for periodic offset cancellation and dc operating point definition in the capacitively coupled OTA. The IFC has 3 activation function modes: step activation function with one or two threshold voltages for monophasic or biphasic operation, respectively, sigmoid activation function with the addition of pseudo-random noise in the IFC state transitions, monophasic or biphasic, and rectified linear unit activation function with the IFC output being sampled and fed back to its input, implementing this way a delta-sigma modulator. The correlated double sampling and activation mode function configuration is done with clocking wave forms. The array has 141 uW power dissipation in 130 nm CMOS technology and is used in a convolutional neural network with high accuracy - 96.9 % with rectified linear unit activation, in digit recognition (MNIST database).

The work in [61] presents a switch capacitor based neuromorphic system with 64 IFC neurons that uses an internal clock to control the neurons, a finite state machine, and synaptic weight random access memory (RAM). It was tapedout in a 28 nm node and has a minimum energy *per* pulse consumption of 2.3 nJ. It is not assynchonous as the proposed IFCs presented in this dissertation.

A biphasic IFC is proposed in [62]. It is based on the single-phase [36, 37, 63] IFC using only one comparator, but having two current based differential pair integrators. The input currents of these integrators have 180 degree phase shift between each other, having reverse polarity, and their outputs are superimposed in the membrane capacitor. This implementation was chosen to reduce the number of transistors and possible device

missmatch in two compartor branches of a conventional biphasic implementation. The number of transistor required was reduced when compared to other implementations and has a FoM of 0.26 pJ/conv-step. [64, 65] present two IFC for neuromorphic applications, the two with the lowest energy *per* pulse consumptions reported until now, 4 fJ and 0.43 fJ, respectively.

An IFC differential solution is better than having two IFCs, one for each differential input, because it has less mismatch between the two input branches. It also provides better balancing, as the bias current increases in one input branch and decreases in the other. This is particularly important in the comparator stage and improves linearity. Although, nonlinearity can be used as an advantage in IFC systems, as shown in [50]. Two IFCs in parallel could be a possible alternative, but there would be a mismatch between transistors and firing thresholds.

The work in [66] presents a new IFC system with delta and pulse frequency modulations that has an inbuilt AFE with an LNA, being different than the proposed IFCs in which the neuron/IFC is in itself an AFE. The work [67] presents an assynchronous biphasic delta modulator with adaptive thresholding capable of being used as an AFE. It presents interesting characteristics to be used as a permanent online system, the adaptive thresholding is used to reduce sensibility to baseline and background signals, and noise. If the threshold adaptation is too prominent, the input reconstruction will not be possible, unless the thresholds are also recorded. But even in such a case, without recording the thresholds, the system can perform well doing time domain feature extraction.

Table 2.2 presents a summary of the SoA with prototype comparison.

2.3 Input Signal Reconstruction

Wei, Harris, and Príncipe's 2004 IEEE International Symposium of Circuit and Systems (ISCAS) proceedings paper [8] presents a signal reconstruction weighted low-pass kernel method (WLPK) for spiking neuron signals, the IFC reconstruction model. Feichtinger *et al.* [11] developed this reconstruction model and proved that it is always possible to approximately reconstruct a bandlimited input signal from the output pulse train under certain constraints and the reconstruction error is bounded by the IFC firing threshold. CNEL further details the reconstruction WLPK in Du Chen's work [10] and in other works as John Harris' *et al.* patent [23] and [26]. Perfect reconstruction from bandlimited signals

sampled by IFC models has been explored and demonstrated by other authors as [68–70], in the last two decades, and more recently [71, 72].

2.4 Time Domain Feature Extraction

The IFC TEM followed by input signal reconstruction requires higher energy consumption than a common ADC. To further optimize energy consumption and avoid reconstruction errors, the system should work in time domain with the pulse output, doing pulse processing. The pulse processing enables the extraction of features from the input signal. Alvarado, Lakshminarayan, and Principe show in [12] that it is possible to classify ECG signals from a IFC time domain compressed information, without having to reconstruct the input signal. It was shown that from the time-based compressed information in the pulse domain it is possible to discriminate features from the ECG signals, discriminating different heartbeat shapes and classifying normal and irregular heartbeats - arrhythmia. The classifier was used in the MIT-BIH arrhythmia database and the classification metrics are similar with the compared methods in [12].

Nallathambi and Principe [13] further developed the classifier algorithm to be able to discriminate not only the QRS complex shapes but also its time structure, using a deterministic finite automaton. The algorithm was used in the MIT-BIH arrhythmia database and the performance in arrhythmia detection is comparable with the best in the SoA with above 99 % total peak detection in QRS complexes. Nallathambi and Principe have also developed a pulse processing theoretic framework and online algorithms for the mathematical operations of sum and multiplication in the pulse domain [14–17]. In [14, 15] work it is shown as an example the baseline noise subtraction from an ECG signal in pulse domain, reducing the pulse density significantly.

Li and Principe [18–20] developed the kernel adaptive autoregressive-moving-average (KARMA) algorithm that enables the creation of an automaton from pulse domain time series from a certain input data sample. This automaton then allows the extraction of relevant features from similar input data. This way it enables the creation of an automaton, as the one in [13], from the input signal, without manual automaton definition for a certain time structure know *a priori*.

2.5 Proposed work summary

This dissertation presents and compares two CT asynchronous ATC that do not require an external clock signal. They are two low power IFC solutions, one analog and the other a fully digital - SCB, dynamic IFC. The first is a closed-loop analog IFC with conventional blocks and on-chip capacitor, although not sacrificing either the chip area or power. The latter, is an open-loop IFC with digital blocks, fully synthesizable and dynamic as each individual block can be powered off. Both are capable of, without requiring external blocks, being used as an AFE. Being fully-differential - the analog solution is fully-differential, the SCB one is pseudo-differential, it also benefits its performance in AFE applications. The designed analog IFC ATC is, to our knowledge, the first fully-differential IFC circuit. As both systems are asynchronous, having a low power dissipation, and with pulse outputs with low data rates, they are a good solution for edge applications, as low power sensors AFE in internet of things (IoT).

Table 2.2: Prototype comparison

Work	ISCAS [36]	JSSC [45]	TCASI [52]	FNeuro [64]	TCASI [65]	TBCAS [41]	TBCAS [42, 43] [44]	PhDD [26]	ISCAS [24, 25] [27]
Technology node (nm)	1500	28 (*a*0)	22 (*a*0)	65	28	180	180	600	600
Supply (V)	1.75-5.0	0.65	0.8	0.2	0.2-1	1.3-1.8	1.8	5	5
Area (mm^2)	-	3.2×10^{-3}	-	35×10^{-6}	13.28×10^{-6}	0.18 (*a*)	1.8×10^{-2}	-	-
SNDR (dB)	-	32-42	-	-	-	-	-	59 (*b*1)	57 (*b*2)
Input BW	-	10 MHz-50 MHz	-	-	-	3 Hz-2.5 kHz	0.8 Hz-10 kHz	10 kHz	-
Total Power (µW)	0.3-1.5	24	-	1×10^{-4}	1.85×10^{-4}	55	27.3 (*c*)	45	1.2
Energy *per* Pulse (pJ)	3×10^{4}	-	16 @30 Hz 1 @2.1 kHz	4×10^{-3}	0.43×10^{-3}	5.5×10^{5}	883 @30 Hz	1.4×10^{3}	10 @ 200 Hz
Average Firing Rate (kHz)	0.01	-	0.07	25	430	0.1	-	33	40
FoM (pJ/ conv-step)	-	3×10^{-3}-1×10^{-2}	-	-	-	-	-	2.2 (*d*)	0.6
Prototyped	No	Yes	No	Yes	No	Yes	Yes	Yes	Yes
Aim	IFC	ADC	IFC	IFC	IFC	IFC (*e*)	IFC	IFC (*e*)	IFC
Fully Differential	No	Yes	No	No	No	No	No	No	No
Phases	Mono	Mono	Mono	Mono	Mono	Mono	Mono	Mono	Bi
Spike frequency adaptation	Yes	-	Yes	No	Yes	No	Yes	No	No
External Clock	No	Yes	No	No	No	No	No	No	No
IFC as AFE Block	No	-	No	No	No	No(*f*)	Yes	No(*f*)	No
All Digital	No	No	No	No	No	No	No	No	No

(*a*0) fully-depleted silicon-on-insulator (FDSOI) (*a*) Total area with low noise amplifier, bandpass filter, delta modulator ADC and pulse ADC, analog trough and peak detector. (*b*) SNR and not SNDR, (b1) from [26, p. 83], (b2) from [24]. (*c*) 27.3 µW average and 0.096 µW static power dissipation. (*d*) FoM was calculated considering [27, p. 69] equation (also presented in [25]), equation (2.5), and in the condition of 2 times BW as there is no sampling frequency for asynchronous IFC (f_{sample}) and data from [26, p. 83], ENOB equal to 10 bits. (*e*) IFC integrated in a neural processor. (*f*) Requires a LNA and analog filters.

3

Integrate-and-Fire

3.1 Integrate-and-fire converter (IFC) Introduction

The integrate-and-fire converter (IFC) circuit has a similar behavior to a single neuron. The input voltage signal is converted to current through R_{in} that is then integrated by the active resistor capacitor (RC) integrator, Figure 2.2. This process is similar to the lowpass filtering in the dendritic tree (equivalent to an RC network) and integration in the soma. The integrated signal is then compared with a defined threshold value. If it is higher than that threshold the circuit fires a pulse to the circuit pulse output, as the soma fires an action potential through the axon. The pulse also resets the integrator by discharging C_f to common-mode (CM), putting the IFC in rest state, as in a neuron after firing an action potential.

3.1.1 Sampler

In the theoretical model, the IFC is a sampler that converts a continuous signal amplitude into time with an injective 1 to 1 mapping, and therefore, it has a defined reconstruction, under certain constraints [11]. The leaky IFC, inspired by the model of what occurs between the dendrites and the axon in a neuron, can be represented by equation (3.1) with the IFC sampler values defined recursively [11, 12, 73]:

$$\int_{t_k+\tau}^{t_{k+1}} x(t)e^{\alpha(t-t_{k+1})}dt = q_k \tag{3.1}$$

where $q_k \in V_{thp}, V_{thn}$ the positive, or negative spiking threshold, respectively (relative to the amplifier input common-mode voltage (V_{iCM})), t_k and t_{k+1} are the occurrence timings of two successive pulses, τ is the refractory period, α is the leakage parameter,

and $e^{\alpha(t-t_{k+1})}$ the integration leaky factor [12]. The inter-pulse interval (IPI) is defined as the time between two adjacent pulses, corresponding to the integrating time (3.2).

$$\mathrm{IPI}(t_{k+1}) = t_{k+1} - t_k \tag{3.2}$$

For the circuit in Figure 2.2 $x(t) = \frac{v_i(t)}{R_{in}C_f}$, where $v_i(t)$ is the input voltage as a function of time. For the circuit in Figure 2.8 $x(t) = \frac{i(t)}{C}$, where $i(t)$ is the input current as a function of time. Equation (3.1) provides the relation between the IPI and the input signal, the leakage is due to the circuit non ideal components, as the operational transconductance amplifier (OTA), reset switches, and feedback capacitor (C_f), which have capacitive and resistive parasitics.

The designed analog IFC block consists in an active-RC integrator with a comparator block. When the integrated signal crosses the positive or negative thresholds, defined externally, a pulse is generated and the integrator capacitor charge is reset. The designed analog IFC analog-to-time converter (ATC) is, to our knowledge, the first fully-differential IFC circuit. It has refractory period control. The designed standard cell-based (SCB) open-loop IFC consists in an open-loop integrator with input cross switching. When the integrated signal crosses the internal NAND latch thresholds a pulse is generated and the amplifier inputs are cross switched, discharging the integrator capacitors.

3.2 Integrate-and-fire converter Design

3.2.1 Description

The IFC sampler integrates the input signal over time, generating a pulse when the integrated signal crosses the defined threshold, considering triangular linear interpolation integration. A pulse is generated when the area under the input signal curve is larger than a value ka, equation (3.3). Figure 3.9 presents a representation of an input signal and the corresponding pulse outputs for a biphasic IFC, the area ka is the trapezoidal grey area under the input signal.

$$Area = \left(\frac{M_{t_k} + M_{t_{k+1}}}{2} - V_{iCM}\right)\Delta t > ka \tag{3.3}$$

where Δt is the time interval, $\Delta t = t_{k+1} - t_k$, M_{t_k} is the signal magnitude in instant t_k (voltage, or current, for the time interval Δt), t_k and t_{k+1} are the occurrence timings of two successive pulses.

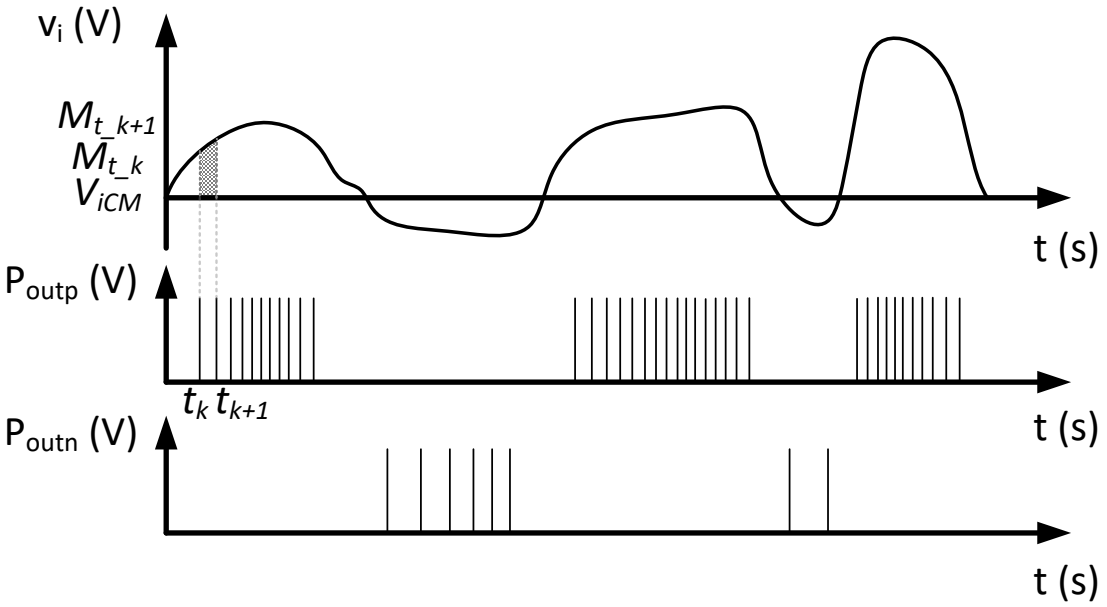

Figure 3.1: Biphasic IFC input and pulse output.

Considering a sinusoidal differential input signal represented by equation (3.4):

$$x(t) = A\sin(2\pi f t + \phi) + B \tag{3.4}$$

Being A the signal amplitude, f the signal frequency, ϕ the signal phase and B a constant that represents the input´s common mode level. The integrated signal for a non-leaky IFC is represented by equations (3.5) and (3.6):

$$y(t) = -D\int x(t)dt \tag{3.5}$$

$$y(t) = D\left\{\frac{A}{2\pi f}\cos(2\pi f t) - Bt + C\right\} \tag{3.6}$$

For an input signal with phase $\phi = 0\ rad$ for simplicity, being C an integration constant that represents the active integrator common mode output level, i. e., the amplifier common mode output level, and D the circuit integration gain. When $y(t)$ reaches the value ka the integration is reset and an output pulse is generated by the comparator block. So the integration result is actually represented by equation (3.7):

$$z(t) = \begin{cases} D\left\{\frac{A}{2\pi f}\cos(2\pi f t) - Bt + C\right\}, & \text{if } \left|y(t)\right| \leq k \\ C, & \text{if } \left|y(t)\right| > k \end{cases} \tag{3.7}$$

Figure 3.2 presents a simple IFC block diagram, with an integration block, where K_I is the integration gain $\frac{1}{RC}$, a comparison block which adds the quantization error q_e, a reset negative feedback path that resets the integration by discharging the integration capacitor. This reset path corresponds to a return-to-zero, as in [74], and it is the subtraction of the integrated value, integrated previously in the integration block. This structure is similar to a delta modulator, in fact the IFC is a special case of an asynchronous first order $\Sigma\Delta$ modulator [75, 76]. With direct current (dc) input, the IFC fires pulses, as the dc voltage charges the integration capacitors.

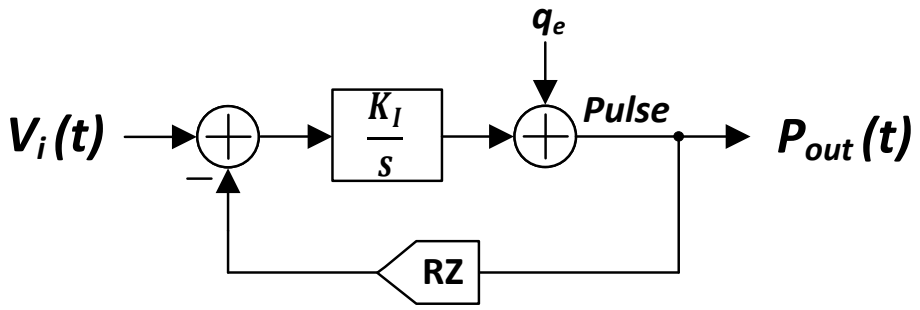

Figure 3.2: Simplified IFC block diagram.

The number of output pulses, i.e., the pulse density, is proportional to the input signal amplitude and inversely proportional to the input frequency. The comparators voltage thresholds V_{th} define the resolution of the IFC circuit together with C value, in the case of the analog biphasic IFC version described in chapter 2, Figure 2.8. The comparator voltage thresholds, V_{thp} and V_{thn}, define the resolution of the IFC circuit together with R_{in} and C_f values, in the case of the proposed analog IFC version, Figure 3.2. However, only C_f and the SCB comparator inherent thresholds set the resolution, in the case of the proposed SCB IFC version, Figure 3.8.

The proposed IFCs were designed and prototyped in a 130 nm technology node.

3.2.2 Design of the Analog IFC Circuit

The analog IFC version circuit is presented in Figure 3.3. It consists in a resettable active RC integrator with a fully-differential two-stage OTA connected to two fully-differential comparators. The comparators have differential/double threshold voltage reference. The comparators are connected in parallel (one for the positive part of the

input and the other for the negative part of the input), each comparator is then connected to two inverters and an edge detector that creates a pulse each time the state of the comparator is switched. The positive and negative pulse outputs are each connected to a transmission gate that shorts the integrating capacitor in the feedback-loop of the OTA, resetting the capacitor. The positive pulse and negative pulse outputs short the capacitors on both circuit differential sides. Figure 3.4 presents the analog IFC inputs, amplifier outputs, and pulse outputs timing diagram.

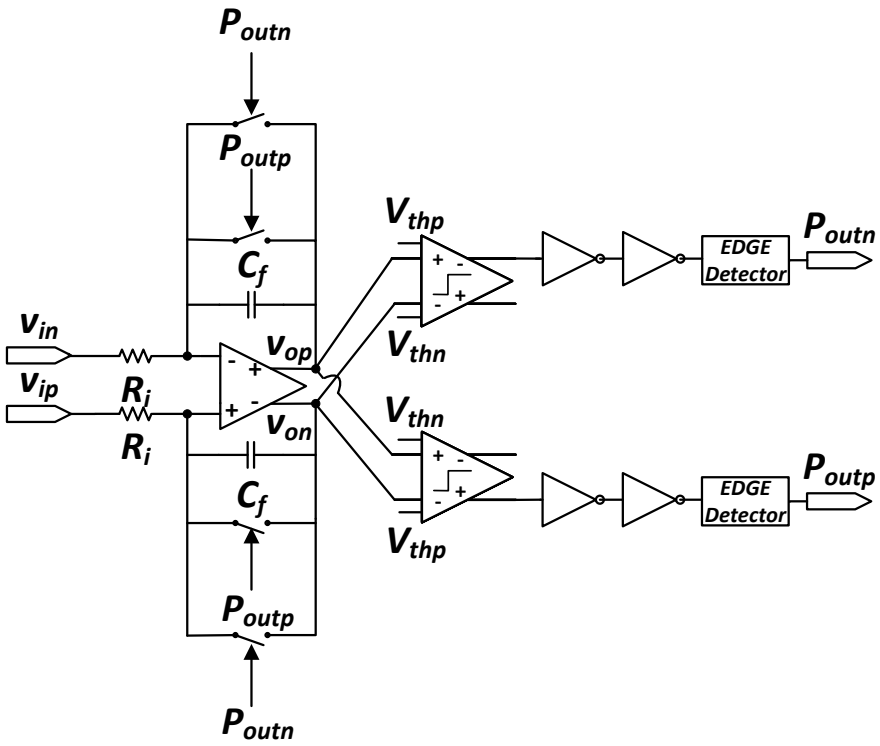

Figure 3.3: Analog IFC circuit. Switches are transmission gates with bootstrapped NMOS and Pouts drive TFFs, both not shown.

The ideal integrator transfer-function is simply defined by:

$$H(j\omega) = -\frac{1}{j\omega R_{in} C_f} \tag{3.8}$$

Considering an operational amplifier (OP-AMP) with limited open-loop gain, A_{OL}, but with infinite bandwidth (BW), the dominant pole is then located at:

$$\omega_p = \frac{1}{R_{in} C_f A_{OL}} \tag{3.9}$$

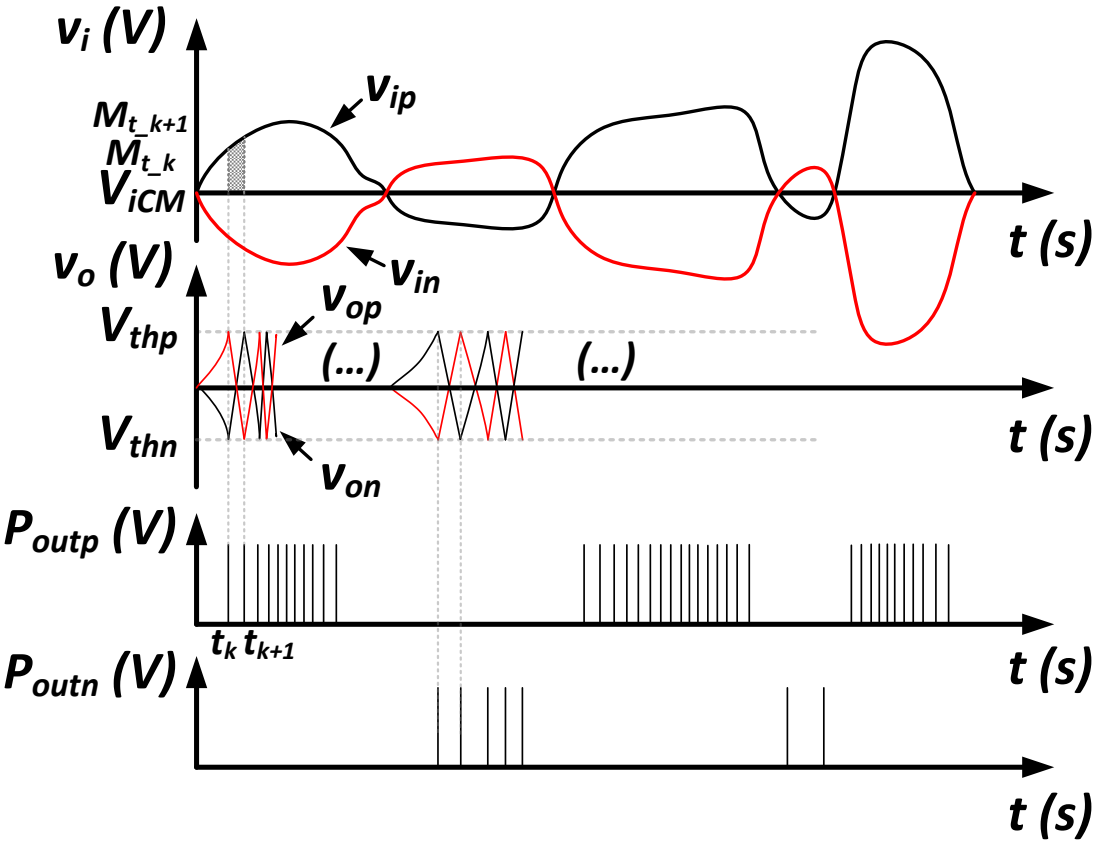

Figure 3.4: Biphasic analog IFC inputs, amplifier outputs, and pulse outputs timing diagram.

and the integrator transfer-function becomes:

$$H(j\omega) = -\frac{A_{OL}}{1 + \frac{j\omega}{\omega_p}} \tag{3.10}$$

As the inverse of the $R_{in}C_f$ product defines the integrator gain, the integrated resistor and capacitor are chosen depending on the input amplitude and frequency range. The designed analog IFC circuit was tuned to input signals with amplitude and frequency range of $[100, 2000]$ µV and $[1, 1000]$ Hz, respectively.

Removing the leaky integration factor, equation (3.1) can be rewritten for this circuit as:

$$\int_{t_k}^{t_{k+1}} \frac{v_i(t)}{R_{in}C_f} dt = V_{th} \tag{3.11}$$

and it gives the relation between the IPI and the input signal for an ideal circuit without leakage, where $v_i(t)$ is the input voltage as a function of time. V_{th} can be the positive or negative threshold (relative to the amplifier input common-mode voltage (V_{iCM})). In

reality the circuit is composed of non ideal components, as the OTA, reset switches, and feedback capacitor (C_f) that present parasitics and leakage. Hence, the correct model is the leaky IFC. The equation is then rewritten as:

$$\int_{t_k}^{t_{k+1}} \frac{v_i(t)}{R_{in}C_f} e^{\alpha(t-t_{k+1})} dt = V_{th} \tag{3.12}$$

where α is the leakage parameter and $e^{\alpha(t-t_{k+1})}$ is the integration leaky factor [12], as shown in equation 3.1.

The analog IFC has been implemented with conventional blocks. It comprises: a two-stage Miller-compensated differential OTA with nulling resistor and an output common mode circuitry, a differential dynamic latch comparator, with dynamic bias (close to power off capability), a NAND based edge detector, and a bootstrap circuit for the reset signal. As it is biphasic the comparator section is doubled, one for each threshold condition. Creating each comparator a pulse output (positive or negative pulse output). The pulse outputs control the transmission gates that reset C_f.

The amplifier of the integrator is a two-stage Miller compensated differential OTA, Figure 3.5, with 73 dB gain, 4 kHz bandwidth and 14 MHz unity gain bandwidth with 1 μA p-channel metal-oxide-semiconductor field effect transistor (PMOS) polarization, dissipating 42.2 μW. With a phase-margin of 69 degrees. This OTA topology has been chosen due to the requirements of high-gain and wide output swing, larger than 150 mV for each branch, so output swing $v_{op} - v_{on} > 300$ mV.

The OTA output CM is adjusted with a common-mode feedback (CMFB) circuit, shown in Figure 3.6, through voltage V_{bn} at the gate of M1-2 (NMOS active loads). The CMFB circuit presents good linearity as it replicates the OTA PMOS input differential pair and its load. The PMOS input pair and the second stage common sources were designed to operate in the subthreshold region to provide the maximum g_m/I_D ratio.

The OTA design, as all the other blocks design, was based on complementary metal-oxide-semiconductor (CMOS) square law model [77].

The drain current in the input pair PMOS transistors, M3 and M4, is given by equation (3.13), [77]:

$$I_{D(sub-th)} \cong I_{D0}\left(\frac{W}{L}\right) e^{\left(\frac{qV_{eff}}{nk_BT}\right)} \tag{3.13}$$

where:

$$n = \frac{C_{ox} + C_{j0}}{C_{ox}} \approx 1.5 \tag{3.14}$$

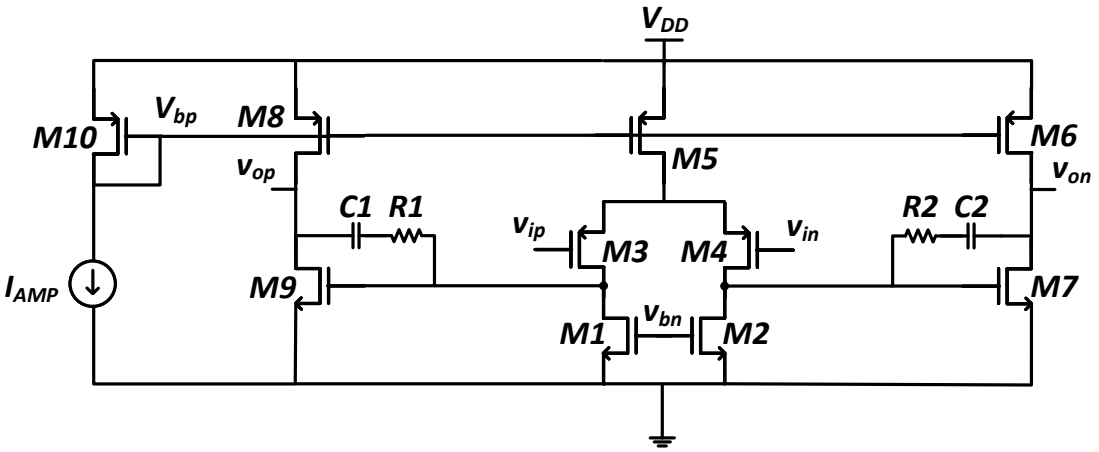

Figure 3.5: Analog IFC two-stage Miller-compensated OTA circuit.

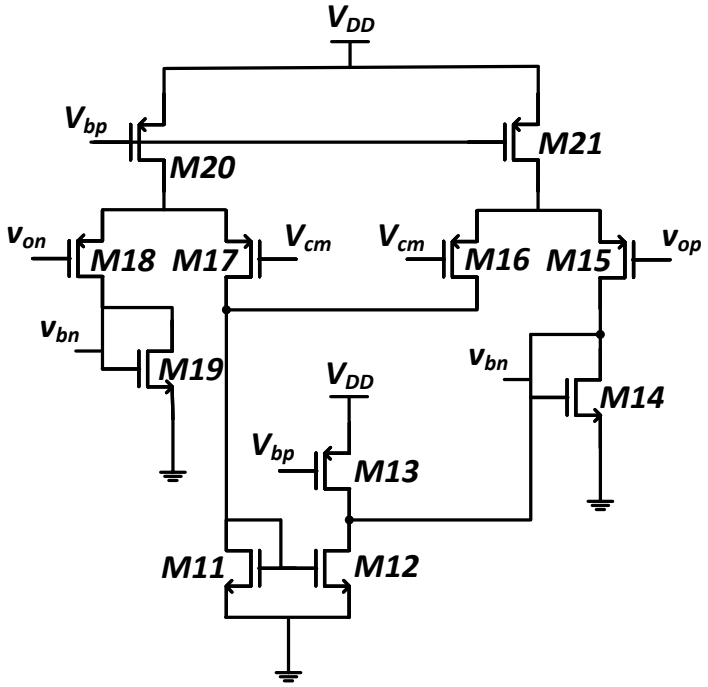

Figure 3.6: The CT CMFB circuit used in the OTA.

$$I_{D0} = (n-1)\mu_{n,p}C_{ox}\left(\frac{k_B T}{q}\right)^2 \tag{3.15}$$

$$V_{eff} = V_{GS} - V_T \tag{3.16}$$

$$C_{ox} = \frac{K_{ox}\varepsilon_0}{t_{ox}} \tag{3.17}$$

$$C_{j0} = \sqrt{\frac{qK_s\varepsilon_0}{2\Phi_0}\frac{N_A N_D}{n_i^2}} \tag{3.18}$$

$$\Phi_0 = \frac{k_B T}{q} ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{3.19}$$

where q represents the electron charge, k_B is the Boltzmann constant, $\mu_{n,p}$ it the charge mobility for NMOS and PMOS transistors, respectively, $K_{ox} \cong 3.9$ is the relative permittivity of SiO_2, $K_s \cong 11.8$ is the relative permittivity of silicon, ε_0 is the permittivity of free space, Φ_0 the junction built in potential [77], N_A and N_D are the acceptor and donor doping concentration, respectively, n_i^2 is the intrinsic carrier concentration.

The transconductance of the input pair is then given by equation (3.20).

$$g_{m(sub-th)3,4} = g_{m3} = g_{m4} = \frac{qI_{D(sub-th)3,4}}{nk_B T} \tag{3.20}$$

The OTA second stage common sources have the transconductance given by equation (3.21).

$$g_{m(sub-th)7,9} = g_{m7} = g_{m9} = \frac{qI_{D(sub-th)7,9}}{nk_B T} \tag{3.21}$$

The remaining transistors are in the active region (with the exception of M20-21, that are in the triode region) and have their transconductance given by equation (3.22):

$$g_m = \sqrt{2\mu_{n,p}C_{ox}\frac{W}{L}I_D} \tag{3.22}$$

where the drain current I_D, in the active region, is given by equation (3.23), square law approximation without channel modulation effects.

$$I_{Dn,p} = \frac{1}{2}\mu_{n,p}C_{ox}\frac{W}{L}V_{eff}^2 \tag{3.23}$$

The OTA output resistance and open-loop gain are given by equation (3.24) and equations (3.25),(3.26), and (3.27), respectively.

$$R_{out} = r_{o6,8} \parallel r_{o7,9} \tag{3.24}$$

$$A_{OL} = g_{m(sub-th)3,4}g_{m(sub-th)7,9}R_{out} \tag{3.25}$$

$$A_{OL} = g_{m3,4} g_{m7,9} (r_{o6,8} \parallel r_{o7,9}) \tag{3.26}$$

Assuming that all transistors are matched:

$$A_{OL} = g_{m3} g_{m9} (r_{o8} \parallel r_{o9}) \tag{3.27}$$

Transistor M10 is diode tied and sets the bias voltage V_{bp}. It is biased by the current source I_{AMP}, with 1 µA. The input pair branches were design to have I_D = 5 µA each and the output branches I_D = 15 µA each. The CMFB circuit was designed to have drain currents, I_D, of approximately: 1.3 µA in M20 and in M21, half of this current in each branch they bias, and so in M15-18, 0.8 µA in M14 and M19, 1.7 µA in M13, and 1.3 µA in M11 and M12.

Tables 3.1 and 3.2 present the OTA and its CM sizing, respectively. Table 3.4 presents the passive components sizing used in the OTA and integrator. All capacitors are of the type metal-insulator-metal (MIM).

Table 3.1: OTA transistors dimensions

Transistor	M1,2	M3,4	M5	M6,8	M7,9	M10
W (μm)	6	36	30	45	18	3
L (μm)	1	0.3	1	1	0.3	1

Table 3.2: OTA CMFB transistors dimensions

Transistor	M11,12	M13	M14	M15-18	M19	M20,21
W (μm)	2	5	1	3	1	5
L (μm)	1	1	1	2	1	1

The reset signal discharges the capacitor C_f through the transmission gates that connect the OTA virtual ground node to the OTA output. This reset signal brings each plate of the capacitor to the OTA input CM and output CM, respectively.

The two comparators are identical, presented in Figure 3.7, having 3.3 µW power dissipation each. The comparators output inverters are current starved inverters, with a tail NMOS with gate voltage V_{refrac}, that sets the refractory component, as in Rastogi's dissertation, [27, p. 44], Figure 2.9. The current starved inverter delay element was proposed in [39]. It should be noted that, as in all schematic drawings in this dissertation, crossed lines are connected and a bridge is drawn when a crossing is not not connected.

The dynamic latched comparator is close to a StrongARM comparator [78], with only one cross-coupled pair (PMOS cross-coupled pair, Mc13-14) - without the NMOS cross-coupled pair. This way there is a dc path and so the static current is not zero, as in a StrongARM comparator [79]. And it also requires output inverters to have rail-to-rail outputs, as the pre-amplifier/latch presents a strong 1 (high output level) and weak 0 (low level) because of the lack of the NMOS cross-coupled pair. And also, in this case, as the system is asynchronous, there is no clock in secondary PMOS transistors and tail NMOS transistors, as in a StrongArm comparator.

The comparator has a replica bias circuit (RBC) to set the voltage in the cross-coupled pair, before the output inverters. The RBC is a copy of one of the comparator branches with a feedback-loop with a simple single-ended single stage diode tied amplifier to set the desired voltage, Figure 3.7. The comparator is dynamically biased, as [27, p. 57], having a close to power off capability through the NMOS tail transistors Mc7a and Mc8a with gate voltage controlled by the comparator input signal. Considering there is no mismatch between the tail transistors, the comparator "turns ON" - has enough bias current with Mc7 out of the triode region and in the beginning of the saturation region ($V_{DSMC7} > V_{bn} - V_{T7}$) and Mc7a not in the subthreshold region, only when the comparator input signal is above approximately $V_{DSMC7} + V_{thMC7a}$, and the same for Mc8,a.

The comparator state changes when $(v_{ipc} - V_{thp}) > (v_{inc} - V_{thn})$, so one comparator has the input configure to change state for $(v_{ipc} - v_{inc}) > (V_{thp} - V_{thn})$ with output connected to v_{opc} and the other has switched inputs with output connected to v_{onc} and so it changes state when $(v_{ipc} - v_{inc}) < (V_{thn} - V_{thp})$.

Table 3.3 presents the complete comparators transistor dimensions.

Table 3.3: Comparator transistors dimensions

Transistor	Mc1-6	Mc7-9a	Mc10-12	Mc13-15	Mc16-19	Mc20,21
W (μm)	1.96	6	1.75	1.4	0.64	1.92
L (μm)	0.66	1	3.3	3.3	1	1

Table 3.4: Passive components dimensions

Component	R_{in} (kΩ)	C_f (pF)	$R_{1,2}$ (kΩ)	$C_{1,2}$ (pF)
Value	268	2.04	5.5	1.04

To discharge the C_f capacitor plates to the OTA input and output common mode it is

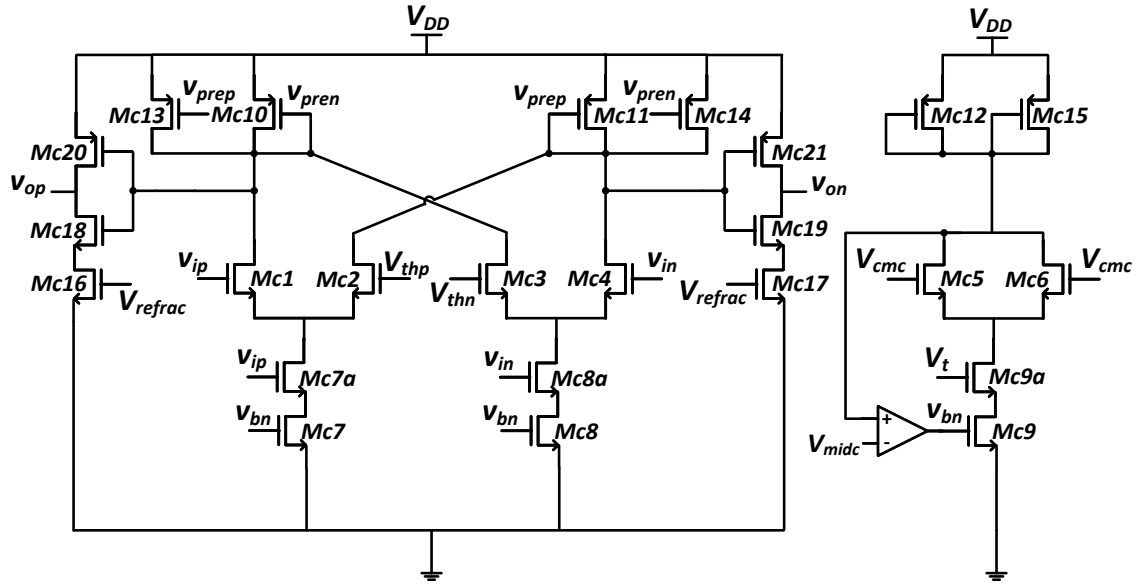

Figure 3.7: Fully-differential latch comparator circuit with dynamic biasing through MC7a and 8a, plus RBC.

required that the reset signal controls very large transmission gates, or with unreasonable multiplier. For this reason a bootstrap circuit, as presented in [80, Fig. 1] and in [81], was used in the reset signal before it drives the transmission gate NMOS transistor. The reset time has to be smaller than the minimum desired IPI. This time comprises the comparison delay, inverter chain delay, edge detector delay (that is the block that defines the pulse width), and the bootstrap circuit delay. The bootstrap voltage driving the transmission gates NMOS transistors, when the reset signal is high, is defined by equation 3.28,

$$V_{BS} = V_{Reset} + V_{CB} \tag{3.28}$$

where V_{CB} is defined externally and has the default value of 0.5 V, the bootstrap voltage is then $V_{BS} = 1.4$ V, as V_{Reset} is equal to $V_{DD} = 0.9$ V, when the reset signal is high (P_{outn} or P_{outp} high).

The threshold voltages, V_{thp} and V_{thn}, together with R_{in} and C_f values define the resolution of the analog IFC circuit. They were set to have an high input dynamic range while achieving the lowest possible firing rate for this technology node, but generally with a good IPI range of at least 2 to 3 times between maximum and minimum IPI for the same input signal, considering a maximum C_f value of 2 pF. This maximum C_f design constraint was set to not have a disproportional capacitor area when compared with the transistor area and have a small prototype area.

This IFC topology requires two high-gain blocks, namely the OTA and the comparator, presented in Figure 3.7.

Corner simulations were run for all circuit blocks ensuring that they work in the most stringent process, voltage, and temperature (PVT) conditions.

3.2.3 Design of the SCB IFC Circuit

A SCB dynamic IFC version composed of logic ports and switches has also been designed and prototyped, Figure 3.8, [2, 3]. It consists in an open-loop integrator with input cross switching and is composed of logic gates and switches, performing in the analog domain. It has inverter-based amplifiers with enable and two double 3-port NAND latch comparators. Both blocks have enable inputs ($ENAmp$ and $ENComp$) and they can be powered-off, independently, making this IFC version a fully-dynamic system. Since all blocks rely on custom sized standard-cells, the system is fully synthesizable, simply with the addition of two on-chip MIM integrating capacitors. As the input for these IFC circuits was chosen to be differential, it is possible to discharge the integrating capacitors through a simple input inversion, or cross-switching the input ports, as in a chopping amplifier. Although in this case there is no chopping after the amplifier outputs (in the analog domain) and there is only in the pulse outputs, to have a pulse in the correct output, positive or negative, even with cross-switched inputs, as described in [45]. Figure 3.9 presents the timing diagram with important signals, v_{ic} is the comparator input voltage.

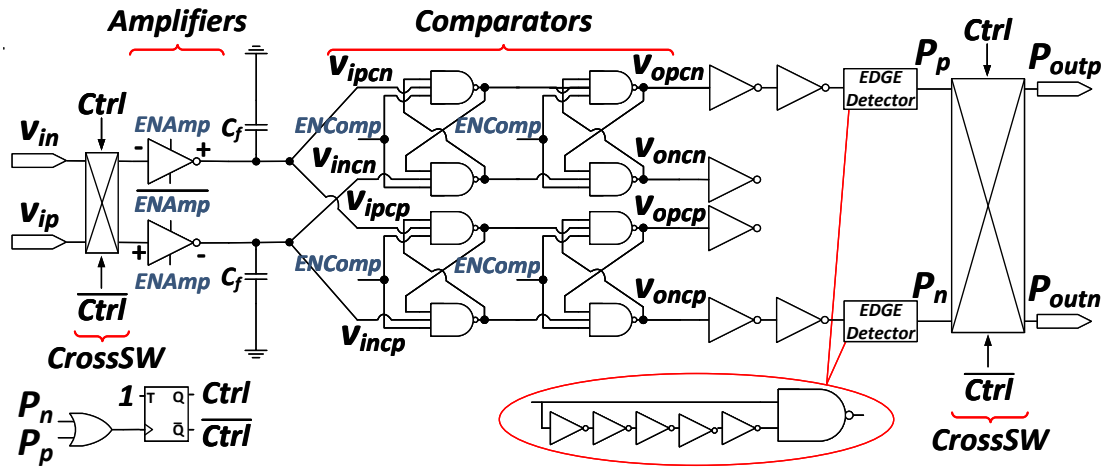

Figure 3.8: SCB IFC circuit. Pulse outputs (P_{outp} and P_{outn}) drive TFFs, not shown.

When the integrated signal crosses the NAND latches internal thresholds, a pulse is

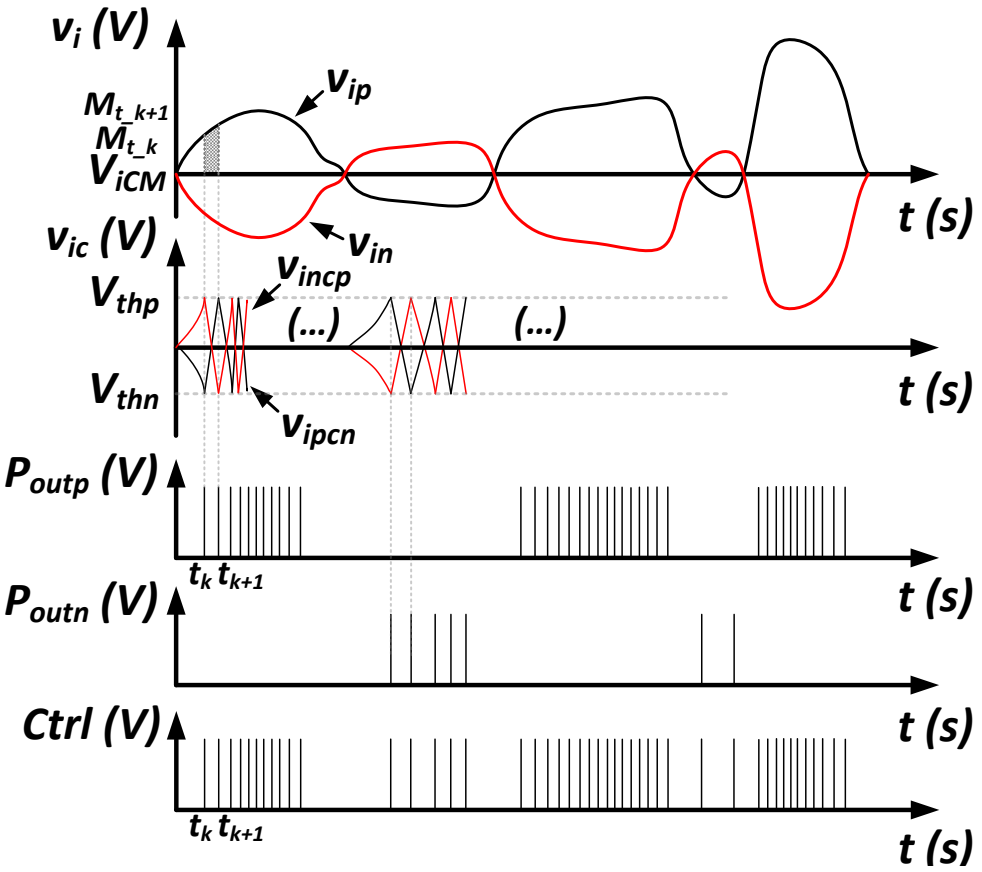

Figure 3.9: Biphasic IFC input and pulse output and timing diagram of important signals for the proposed SCB IFC.

generated and the amplifier inputs are cross switched, discharging the integrator capacitors. The comparators inherent thresholds, together with C_f, define the resolution of the IFC circuit. The input switches are controlled by two comparators that are triggered by the integrated signal. The cross-switching of its differential input discharges the integrating capacitors. The integration is reset by the lower and upper inner thresholds of the 3-port NAND latch. One comparator switches when the input is positive and the other when it is negative, creating pulses in the positive and negative pulse outputs, respectively. The reset path is similar to [45], using TFFs to retain the comparator last state, but has edge detectors (not used in [45]), as in the analog IFC version, to create the output pulses. The two inverters with inputs, v_{oncn} and v_{opcp}, are used only as load of the NAND latches. This ensures that the NAND latches have the same load in both outputs. The outputs of these two inverters are not connected.

The input signal is integrated in capacitors C_f. For example, assuming that $Ctrl$ is at

high level, if v_{in} is negative relative to V_{iCM}, the amplifier output v_{ipcn} charges the top capacitor C_f. As the input signal is differential, v_{ip} is positive and the amplifier output: v_{incn}, v_{incp} is negative (note that $v_{incn} = v_{incp}$), discharging the bottom capacitor C_f. When v_{ipcn} rises above the NAND internal threshold, its output becomes low level, and so the NAND with v_{incn} output passes to high level. The double NAND latch comparator output v_{opcn} passes to high level creating a square wave after the top edge detector. This rapid square wave corresponds to a pulse in P_p and P_{outp}. Note that node v_{incp} is discharging and, therefore, the NAND latch with v_{incp} input has high level output and v_{oncp} has low level output, and P_n and P_{outn} stay at low level. The positive output in P_p creates a transition in the TFF with $Ctrl$ outputs, lowering $Ctrl$, that switches both the IFC inputs and outputs. The cross switches change position and v_{in} is now connected to the bottom amplifier and v_{ip} to the top amplifier, P_n is now connected to P_{outp} and P_p is now connected to P_{outn}. As v_{in} is still negative and v_{ip} is positive relative to the input CM, the top capacitor C_f is now discharging and the bottom one is charging. As v_{incp} voltage increases, when it passes the NAND latch internal threshold, the bottom double latch comparator has a similar behavior as the top comparator before, it passes v_{oncp} to high level and creates a pulse in P_n, and so another pulse in P_{outp}. As P_n passes to high level, the $Ctrl$ signals switch again due to the bottom TFF, making the inputs and outputs cross-switch again. The process repeats, if the integrated signal passes one of the double NAND laches internal threshold, until v_{in} becomes positive, relative to input CM. When this happens, the IFC has the same behavior, but with opposite polarity, and if the integrated signal passes one of the double NAND latches internal thresholds, the IFC creates pulses in P_{outn}.

A fully-digital - SCB, IFC was implemented with this topology that is quite different from the proposed analog IFC. It benefits from being an open-loop approach, without a feedback-loop in the amplifier section. This reduces the Nyquist noise contribution, and it improves noise performance, sacrificing linearity, gain control, and power supply rejection ratio (PSRR) [82, p. 15].

The SCB open-loop IFC version consists in an open-loop integrator with cross-switched input, Figure 3.8. It only has custom sized standard-cells with the addition of two MIM integrator capacitors, C_f. It has an inverter-based amplifier with enable, Figure 3.10, and two double NAND latch comparators, Figure 3.11 and Figure 3.12. Both blocks have enable inputs ($ENAmp$ and $ENComp$) and they can be powered-off independently, making

this IFC version a fully-dynamic system. The enable inputs can also be used to control the refractory period changing the amplifier and comparator performance. As in a starved inverter.

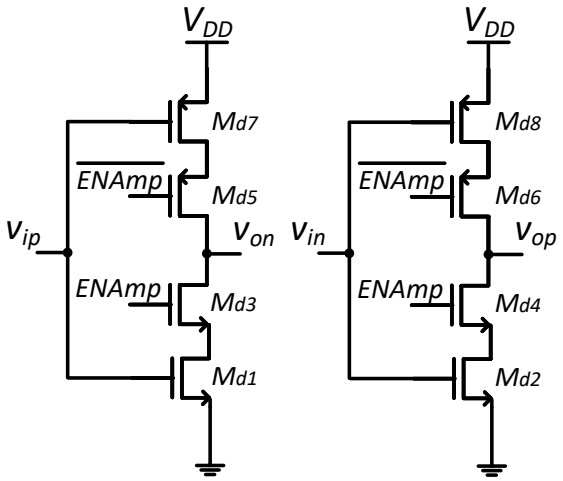

Figure 3.10: SCB IFC inverter-based amplifier circuit.

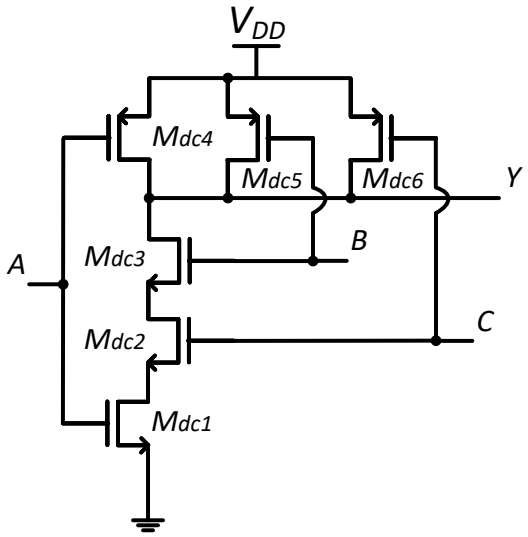

Figure 3.11: SCB IFC 3 port NAND circuit.

The IFC block outputs the positive and negative pulse outputs, and the reset control signal ($Ctrl$). It has differential input, enable amplifier, and enable comparators signals. In this implementation there is no need for a reference clock, as in [45] where it is used in the comparator block.

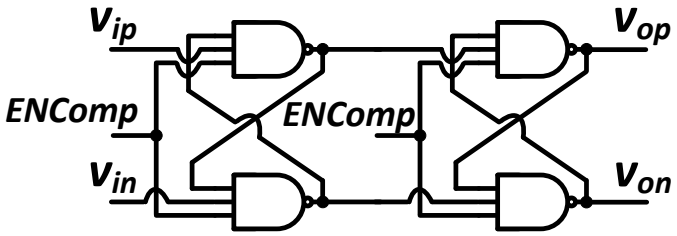

Figure 3.12: SCB IFC comparator, based on a double NAND latch circuit.

Transistors with small length, close to the minimum length, can present velocity saturation. The gain of an inverter, with its transistors in the active region and without velocity saturation is given by 3.29 [83, p. 203]. In fact, both SCB IFC versions have the input transistors (Md1,2 and Md7,8) in the active region and without velocity saturation, and the enable transistors (Md3-6) in the triode region. The gain in this case is given by equations (3.30), (3.32).The output resistance is given by equation (3.31).

$$A_{inverter} \cong -\left(g_{mn} + g_{mp}\right) r_{dsn} \parallel r_{dsp} \tag{3.29}$$

$$A_{EnInverter} \cong -\left(g_{mn} + g_{mp}\right) R_{outEnInverter} \tag{3.30}$$

$$R_{outEnInverter} = g_{md3,4} r_{0d3,4} r_{0d1,2} \| g_{md5,6} r_{0d5,6} r_{0d7,8} \tag{3.31}$$

$$A_{EnInverter} \cong -\left(g_{md1,2} + g_{md7,8}\right) \left[g_{md3,4} r_{0d3,4} r_{0d1,2} \| g_{md5,6} r_{0d5,6} r_{0d7,8}\right] \tag{3.32}$$

Table 3.5 summarizes the transistors dimensions for the inverter-based amplifier and comparators.

Table 3.5: Inverter-based Amplifier and Latch comparators NAND3 transistors dimensions.

Transistor	Md1-4	Md5-8	Mdc1-3	Mdc4-6
W (μm)	2.8	8.4	12	2.4
L (μm)	0.36	0.36	1.2	1.2

For comparison purposes, a lower BW SCB IFC has also been designed and prototyped. It comprises a inverter-based amplifier with larger length transistors, $L = 2$ μm (Md1-8) instead of the length $L = 0.36$ μm in Table 3.5.

In both versions, an edge detector circuit is required to generate a pulse because the comparators digital output stays at V_{DD} if one of the previous firing conditions is met. This way the edge detector creates a pulse with a width set by its delay cells, whenever the comparator output goes high. This pulse resets the integrating capacitor C_f, making again the comparator change to its low output state.

Both designed IFC versions do not require a clock signal, and the prototypes can be simply tested with a regular power supply and voltage regulators to properly generate the reference voltages. In fact the complete IFC analog version, with internal reference voltages (described in the next Chapter, 4), just requires a power supply to be tested. The SCB IFC requires a power supply and just two voltage regulators to supply the enable inputs, that ultimately, if the enable inputs are at V_{DD} level (power rail level), they can be supplied by the main voltage supply directly. If the enable inputs have another constant value, an internal voltage reference could be easily integrated in a future prototype, that was done with the complete analog IFC version. This makes the developed prototypes easy to be tested and used, without laboratory equipment, just requiring a voltage supply.

The SCB comparator inherent thresholds together with C_f capacitor value define the resolution of the SCB IFC circuit. The comparator transistor dimensions set the comparator internal threshold voltages and were designed to have an high input dynamic range while achieving a low firing rate, but with a good IPI range of at least 5 to 8 times between maximum and minimum IPI for the same input signal, considering a maximum C_f value of 2 pF. This maximum C_f design constraint was set to not have a disproportional capacitor area when compared with the transistor area and have a small prototype area, as for the analog IFC. The C_f value is 2.04 pF, as in the analog IFC.

Corner simulations were run for all circuit blocks ensuring that they work in the most stringent PVT conditions.

It should be noted that the small signal equation (3.32) is valid for the proposed inverter-based amplifier due to the transistors length, that is three times the minimum feature size (130 nm) for the higher BW amplifier and ten times for the lower BW amplifier, table 3.5. But if considering that all inverter-based amplifier transistors, input and enable transistors, NMOS and PMOS, are velocity saturated due to their short channel and are in the triode region ($V_{GS} > V_T$ and $V_{DS} \leq V_{eff}$) the gain calculation is more complex. The gain derivation for that case is presented next. If the input voltage is equal to the inverter switching threshold voltage V_M (designed to be located at the inverter mid point). The

transistors current is given by equation (3.33), ignoring the channel length modulation effects.

$$I_D = \mu_{n,p} C_{ox} \frac{W}{L} \left[V_{DS} (V_{GS} - V_T) - \frac{V_{DS}^2}{2} \right] \tag{3.33}$$

In this conditions the current through all devices is the same. And so considering just the input transistors V_M can be calculated, similar to a normal inverter ([84, p. 185]), equation (3.34).

$$k_n \left[V_{DSn} (V_M - V_{Tn}) - \frac{V_{DSn}^2}{2} \right] + k_p \left[V_{DSp} \left(V_M - V_{DD} - V_{Tp} \right) - \frac{V_{DSp}^2}{2} \right] = 0 \tag{3.34}$$

where

$$k_n = \mu_n C_{ox} \frac{W_n}{L_n} \tag{3.35}$$

and

$$k_p = \mu_p C_{ox} \frac{W_p}{L_p} \tag{3.36}$$

Solving equation (3.34) for V_M:

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSn}}{2} \right) + r \left(V_{DD} + V_{Tp} + \frac{V_{DSp}^2}{2} \right)}{1 + r} \tag{3.37}$$

where

$$r = \frac{k_p V_{DSp}}{k_n V_{DSn}} \tag{3.38}$$

Equating the currents for the enable transistors. For v_{ip} inverter case, being V_E the $ENAmp$ voltage:

$$\begin{aligned} k_{n3} \left[V_{DS3} (V_E - V_{DS1} - V_{T3}) - \frac{V_{DS3}^2}{2} \right] + \\ k_{p5} \left[V_{DS5} (V_{DD} - V_E - V_{DS7} - V_{DD} - V_{T5}) - \frac{V_{DS5}^2}{2} \right] = 0 \end{aligned} \tag{3.39}$$

Simplifying, it yields:

$$k_{n3} \left[V_{DS3} (V_E - V_{DS1} - V_{T3}) - \frac{V_{DS3}^2}{2} \right] - k_{p5} \left[V_{DS5} (V_E + V_{DS7} + V_{T5}) + \frac{V_{DS5}^2}{2} \right] = 0 \tag{3.40}$$

To calculate the amplifier static gain for an input around the inverter switching threshold, the channel length modulation effects have to be taken into consideration, or the gain would be infinite, [84, p. 189]. The drain current becomes ([84, p. 93]):

$$I_D = I'_D(1 + \lambda V_{DS}) \tag{3.41}$$

where I'_D is the drain current without channel length modulation and λ is the empirical channel-length modulation parameter.

Equating again the currents in the inverter, for the input transistors:

$$\begin{aligned} k_n\left[V_{DSn}(v_i - V_{Tn}) - \frac{V_{DSn}^2}{2}\right][1 + \lambda_n(v_o - V_{DSnen})] + \\ k_p\left[V_{DSp}\left(v_i - V_{DD} - V_{Tp}\right) - \frac{V_{DSp}^2}{2}\right]\left[1 + \lambda_p\left(v_o - V_{DSpen} - V_{DD}\right)\right] = 0 \end{aligned} \tag{3.42}$$

where nem and pen indexes refer to the NMOS and PMOS enable transistors, respectively, and $\lambda_{n,p}$ are the empirical channel-length modulation parameters for NMOS and PMOS transistors, respectively.

Equation (3.42) can be written as a function $v_o(v_i)$. The gain is obtained differentiating equation (3.42) with respect to v_i.

To simplify the derivation let

$$a = k_n\left[V_{DSn}(v_i - V_{Tn}) - \frac{V_{DSn}^2}{2}\right] \tag{3.43}$$

$$b = k_p\left[V_{DSp}\left(v_i - V_{DD} - V_{Tp}\right) - \frac{V_{DSp}^2}{2}\right] \tag{3.44}$$

$$v_o = \frac{a(\lambda_n V_{DSnen} - 1) + b\left[\lambda_p\left(V_{DSpen} + V_{DD}\right) - 1\right]}{\lambda_n a + \lambda_p b} \tag{3.45}$$

In fact a and b are I'_D for NMOS and PMOS transistors, respectively. Expanding the

equation:

$$v_o = \frac{k_n\left[V_{DSn}(v_i - V_{Tn}) - \frac{V_{DSn}^2}{2}\right](\lambda_n V_{DSnen} - 1)}{\lambda_n k_n\left[V_{DSn}(v_i - V_{Tn}) - \frac{V_{DSn}^2}{2}\right] + \lambda_p k_p\left[V_{DSp}\left(v_i - V_{DD} - V_{Tp}\right) - \frac{V_{DSp}^2}{2}\right]} + \frac{k_p\left[V_{DSp}\left(v_i - V_{DD} - V_{Tp}\right) - \frac{V_{DSp}^2}{2}\right]\left[\lambda_p\left(V_{DSpen} + V_{DD}\right) - 1\right]}{\lambda_n k_n\left[V_{DSn}(v_i - V_{Tn}) - \frac{V_{DSn}^2}{2}\right] + \lambda_p k_p\left[V_{DSp}\left(v_i - V_{DD} - V_{Tp}\right) - \frac{V_{DSp}^2}{2}\right]} \tag{3.46}$$

and the gain is given by equation (3.47).

$$\frac{dv_o}{dv_i} = \frac{k_n V_{DSn}(\lambda_n V_{DSnen} - 1) + k_p V_{DSp}\left[\lambda_p\left(V_{DSpen} + V_{DD}\right) - 1\right]}{\lambda_n a + \lambda_p b} - \frac{\left(\lambda_n k_n V_{DSn} + \lambda_p k_p V_{DSp}\right)\left\{a(\lambda_n V_{DSnen} - 1) + b\left[\lambda_p\left(V_{DSpen} + V_{DD}\right) - 1\right]\right\}}{\left[\lambda_n a + \lambda_p b\right]^2} \tag{3.47}$$

Expanding the equation:

$$\frac{dv_o}{dv_i} = \frac{k_n V_{DSn}(\lambda_n V_{DSnen} - 1) + k_p V_{DSp}\left[\lambda_p\left(V_{DSpen} + V_{DD}\right) - 1\right]}{\lambda_n k_n\left[V_{DSn}(v_i - V_{Tn}) - \frac{V_{DSn}^2}{2}\right] + \lambda_p k_p\left[V_{DSp}\left(v_i - V_{DD} - V_{Tp}\right) - \frac{V_{DSp}^2}{2}\right]} - \frac{\left(\lambda_n k_n V_{DSn} + \lambda_p k_p V_{DSp}\right)\left\{k_n\left[V_{DSn}(v_i - V_{Tn}) - \frac{V_{DSn}^2}{2}\right](\lambda_n V_{DSnen} - 1)\right\}}{\left\{\lambda_n k_n\left[V_{DSn}(v_i - V_{Tn}) - \frac{V_{DSn}^2}{2}\right] + \lambda_p k_p\left[V_{DSp}\left(v_i - V_{DD} - V_{Tp}\right) - \frac{V_{DSp}^2}{2}\right]\right\}^2} - \frac{\left(\lambda_n k_n V_{DSn} + \lambda_p k_p V_{DSp}\right)\left\{k_p\left[V_{DSp}\left(v_i - V_{DD} - V_{Tp}\right) - \frac{V_{DSp}^2}{2}\right]\left[\lambda_p\left(V_{DSpen} + V_{DD}\right) - 1\right]\right\}}{\left\{\lambda_n k_n\left[V_{DSn}(v_i - V_{Tn}) - \frac{V_{DSn}^2}{2}\right] + \lambda_p k_p\left[V_{DSp}\left(v_i - V_{DD} - V_{Tp}\right) - \frac{V_{DSp}^2}{2}\right]\right\}^2} \tag{3.48}$$

substituting by I_Ds (similar to equation (3.47)):

$$\frac{dv_o}{dv_i} = \frac{k_n V_{DSn}(\lambda_n V_{DSnen} - 1) + k_p V_{DSp}\left[\lambda_p\left(V_{DSpen} + V_{DD}\right) - 1\right]}{\lambda_n I'_{Dn} + \lambda_p I'_{Dp}} - \frac{\left\{\lambda_n k_n V_{DSn} + \lambda_p k_p V_{DSp}\right\}\left\{I'_{Dn}(\lambda_n V_{DSnen} - 1)\right\}}{\left\{\lambda_n I'_{Dn} + \lambda_p I'_{Dp}\right\}^2} - \frac{\left\{\lambda_n k_n V_{DSn} + \lambda_p k_p V_{DSp}\right\}\left\{I'_{Dp}\lambda_p\left(V_{DSpen} + V_{DD}\right) - 1\right\}}{\left\{\lambda_n I'_{Dn} + \lambda_p I'_{Dp}\right\}^2} \tag{3.49}$$

Being I'_D the drain current neglecting the channel length modulation effect. Without substituting by I_Ds, the equation can be simplified to:

$$\frac{dv_o}{dv_i} = \frac{2k_n V_{DSn} V_{DSp} \left\{\lambda_p + \lambda_n \left[-1 + \lambda_p (V_{DD} - V_{DSnen} + V_{DSpen})\right]\right\} (2V_{DD} - V_{DSn} + V_{DSp} - 2V_{Tn} + 2V_{Tp})}{\left[\lambda_n k_n V_{DSn} (V_{DSn} - 2v_i + 2V_{Tn}) + \lambda_p k_p V_{DSp} (2V_{DD} + V_{DSp} - 2v_i + 2V_{Tp})\right]^2} \tag{3.50}$$

As the currents in PMOS and NMOS transistors are the same, equation (3.49) can be further simplified and the gain can be written setting $v_i = V_M$, equation (3.51).

$$\begin{aligned} G = \frac{dv_o}{dv_i} = \frac{1}{I'_D(V_M)} \frac{k_n V_{DSn} (\lambda_n V_{DSnen} - 1) + k_p V_{DSp} \left[\lambda_p \left(V_{DSpen} + V_{DD}\right) - 1\right]}{\lambda_n + \lambda_p} - \\ \frac{1}{I'_D(V_M)} \frac{\left(\lambda_n k_n V_{DSn} + \lambda_p k_p V_{DSp}\right) (\lambda_n V_{DSnen} - 1)}{\left(\lambda_n + \lambda_p\right)^2} - \\ \frac{1}{I'_D(V_M)} \frac{\left(\lambda_n k_n V_{DSn} + \lambda_p k_p V_{DSp}\right) \left[\lambda_p \left(V_{DSpen} + V_{DD}\right) - 1\right]}{\left(\lambda_n + \lambda_p\right)^2} \end{aligned} \tag{3.51}$$

It should be noted that the equation (3.51) was written without $\frac{1}{I'_D(V_M)}$ multiplying once by all fractions, so it would be possible to split the equation in multiple lines. Equation (3.51) is the open-loop gain of the inverter amplifier.

4

Integrated Prototypes and Results

4.1 Integrated Prototypes

Both prototypes were designed in 130 nm standard process. Simulations and layout were run in Cadence software and results were obtained with layout extraction. Results processing, as inter-pulse interval (IPI) calculations and input signal reconstruction from the measured pulse stream have been done in Matlab. Figures 4.1 and 4.2 present the analog and standard cell-based (SCB) integrate-and-fire converter (IFC) chip layouts, respectively. Figures 4.3 and 4.4 present the die photos of the prototyped integrated circuits (ICs) fabricated in a 1.2 V, 130 nm standard complementary metal-oxide-semiconductor (CMOS) technology. The layout of the analog IFC version occupies an area of 0.027 mm^2 and the SCB IFC 0.021 mm^2. The area of the SCB IFC circuit could be further optimized. Two versions of the SCB IFC were prototyped, one with an higher bandwidth (BW) inverter-based amplifier, and the second one relying on a lower BW inverter-based amplifier. The SCB circuit layout presented here is the higher BW amplifier version. The lowers BW amplifier version is similar but the inverter amplifier transistors have a larger length, $L = 2\ \mu$m (Md1-8). The available empty area in the amplifier section is filled in the case of the lower BW inverter amplifier. This layout disposition was chosen to simplify the circuits tape out (higher and lower BW SCB versions).

All layouts were done using stack transistors and without common centroid techniques. The standard cells are always disposed horizontally and with typical standard cell layout: supply on the top bar with metal zero and ground in the bottom bar, also with metal zero. The standard cells can be stacked horizontally with these lanes, and are stacked whenever possible in the layout. The following rule was always respected for metal routing: metals with pair layer number are always drawn in horizontal lanes

and odd layers metals are always drawn in vertical lanes. To have an easier layout and avoiding short circuits done by mistakes in routing. This rule was only not respected in the main power lanes in the analog complete channel prototype, as shown, in Figure 4.5. The floor planing respected approximately the schematic block disposition. Inside each cell the metal layers used are typically from 0 to 4, or 5, with exception of the metal-insulator-metal (MIM) capacitors that have higher layer metals. The top layer metals from 5 to 8, were mostly used for routing. The metal widths are slightly above minimum width for signals and larger for supply voltage and ground. The metal width and number of vias increased proportionally with the increase in layer number. The radio frequency (RF) pads have diode protections to prevent IC damage from electrostatic discharges (ESDs). All signals driving transistor gates have a small resistor in series with the transistor gate in the ICs to protect the transistors gates from peaks, when connecting and disconnecting signals.

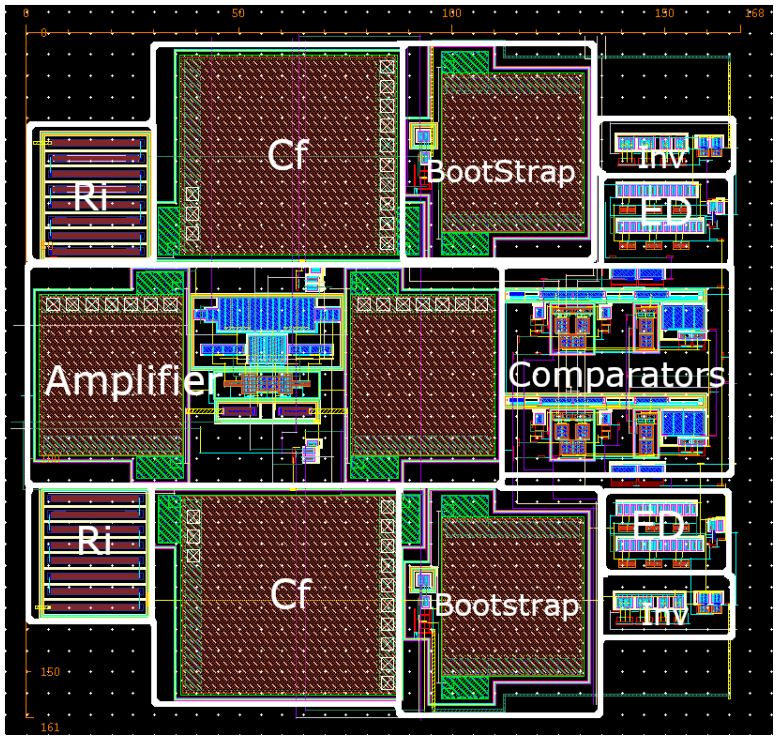

Figure 4.1: Plot of the analog IFC circuit layout in 130 nm CMOS technology, area 0.027 mm^2 (157 µm by 165 µm, width - vertical, by length - horizontal, respectively). Label ED stands for edge detector, Ri is R_{in} in the schematic. Layout done in Cadence.

Three analog IFC protoypes were designed and tapeout. The first prototype had direct pulse output without output flip-flops. The analog IFC system was also prototyped and taped out as a complete analog channel, with designed circuits for internal biasing and

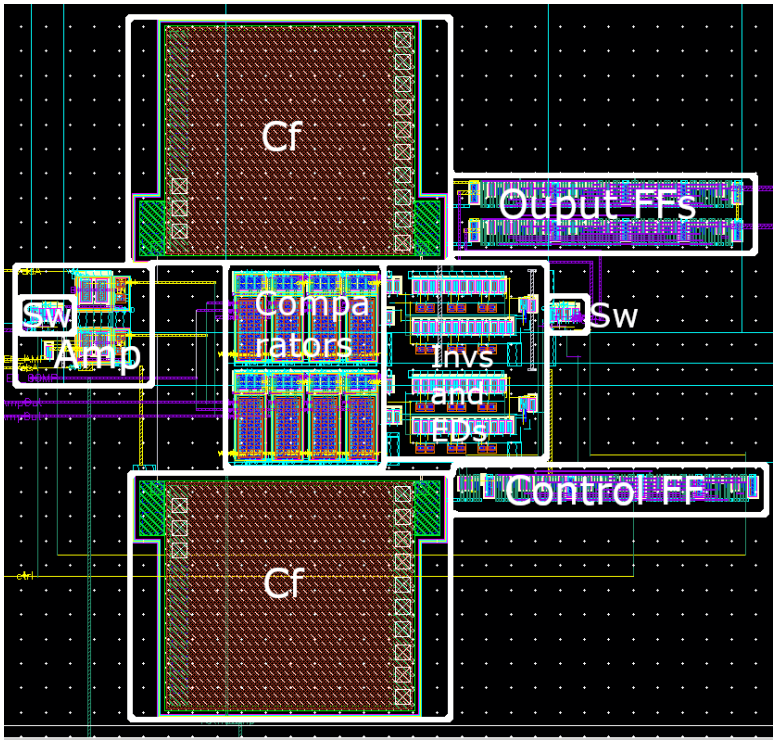

Figure 4.2: Plot of the SCB IFC circuit layout in 130 nm CMOS technology, area 0.021 mm^2 (143 µm by 149 µm, width - vertical, by length - horizontal, respectively). Higher BW amplifier version. Label ED stands for edge detector, Sw for switches, and Invs for inverters. Layout done in Cadence.

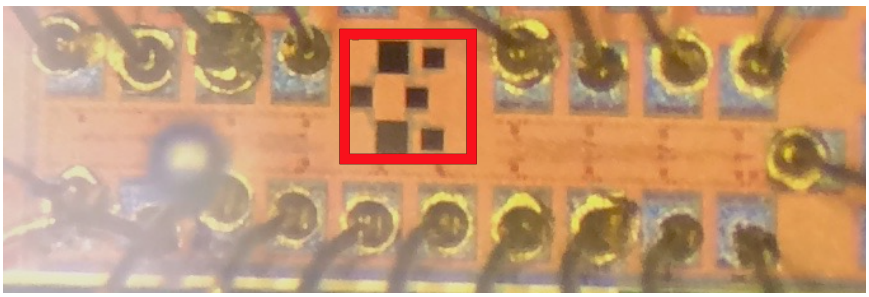

Figure 4.3: Analog IFC prototyped circuit layout in 130 nm CMOS technology. Circuit and contact pads wirebonded (active area in red). For reference, pad size is 74 µm by 92 µm.

generation of reference voltages, including the thresholds voltages V_{thp} and V_{thn}. Figures 4.5 and 4.6 present its layout. The complete analog channel voltage reference circuit was designed with a resistive ladder between V_{DD} and ground, generating the positive and negative threshold voltages, V_{thn}, V_{thp}, and reference voltages: VCB, V_{midc}, V_t, V_{cm}, V_{cmc} of 0.5 V, and V_{refrac} of 0.24 V. In this implementation these voltages are fixed by the resistive ladder internal connection. This reference voltage generation circuit is the

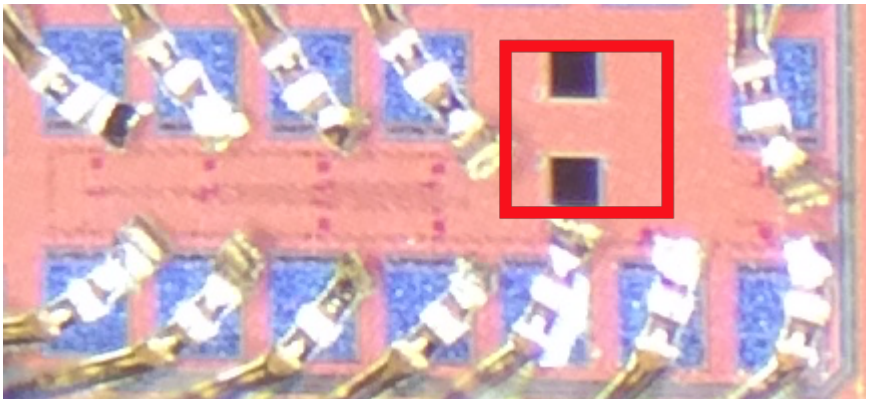

Figure 4.4: SCB IFC prototyped circuit layout in 130 nm CMOS technology Circuit and contact pads wirebonded (active area in red). For reference, pad size is 74 µm by 92 µm.

simplest one but is not the best choice as it connected directly to the external supply, having a low power supply rejection ratio (PSRR) and low precision voltage generation. Is was also implemented with no programability due to layout constrains in the number of external pads to control the bits.

A low voltage bandgap voltage reference circuit, as the one proposed in [85] together with: the implemented resistor ladder, or with a diode transistor reference circuit, would be a good solution for a stable voltage reference generation. Another option, would be a low voltage bandgap voltage reference circuit, as the ones proposed in [86, 87]. A circuit as the one proposed in [86] could be used to directly supply the reference voltage of 0.5 V, together with diode tied transistor to generate a secondary reference relative to this main one, for example. A circuit as the one presented in [87] could generate directly V_{refrac} voltage of 0.24 V, for example.

The only inputs to the complete analog channel IFC prototype are: V_{DD}, V_{SS}, analog channel inputs, enable bit, and 10 control bits. Figure 4.6 presents a layout close up, without the switches to increase R_{in} on-chip and the decoupling capacitors, present in Figure 4.5. This IFC analog channel has the capability of increasing R_{in} with a on-chip resistance. Which is necessary for higher input amplitude signals $A > 10$ mV at frequencies above 1 kHz. This capability of increasing R_{in} on-chip with a control bit, adds versatility to the IFC system, as it can convert a higher range of input signals, with higher amplitude and frequency. The third analog IFC was prototyped including output toggle flip-flops (TFFs) in the pulsed outputs, as will be detailed in Sections: 4.2.1, 4.2.2, 4.3.1, and 4.3.2.

With the exception of the complete analog channel, for these analog IFC prototypes

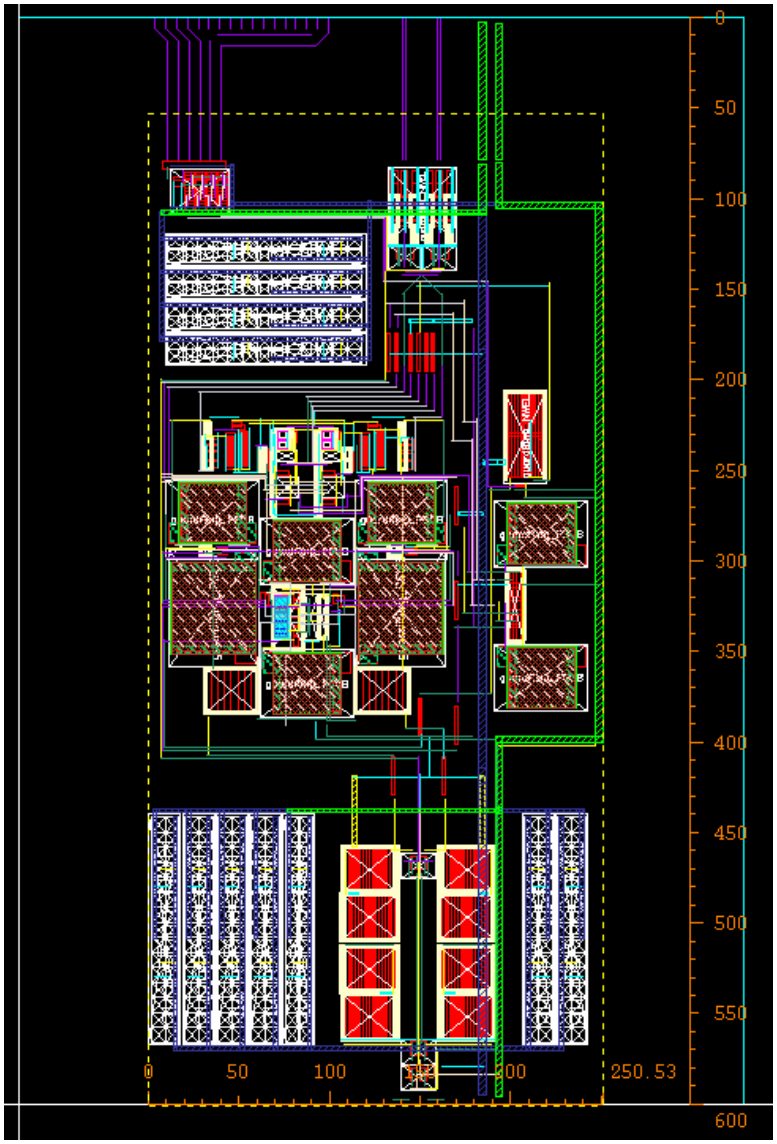

Figure 4.5: Plot of the analog IFC circuit layout with the complete analog channel - with internal reference voltage and bias currents supply circuits, in 130 nm CMOS technology, $Area = 250\ \mu m * 600\ \mu m = 0.15\ mm^2$. Layout done in Cadence.

to have prototype full testing capabilities it was decided to have RF pads to supply many reference voltages and pads for intermediate outputs, operational transconductance amplifier (OTA) outputs: v_{op} and v_{on} in the analog IFC chip. Although, this choice of having OTA output pads adds: the pad capacitance, line resistance, and parasitic capacitance, resistance and inductance from wire bonding and also PCB - if this pad is soldered, which can affect the prototype response. This was noticeable in the analog IFC measurements, as even the capacitance from a probe touching these pads would affect the pulse output and prototype behavior. Although, through simulation after R+C+CC extraction type

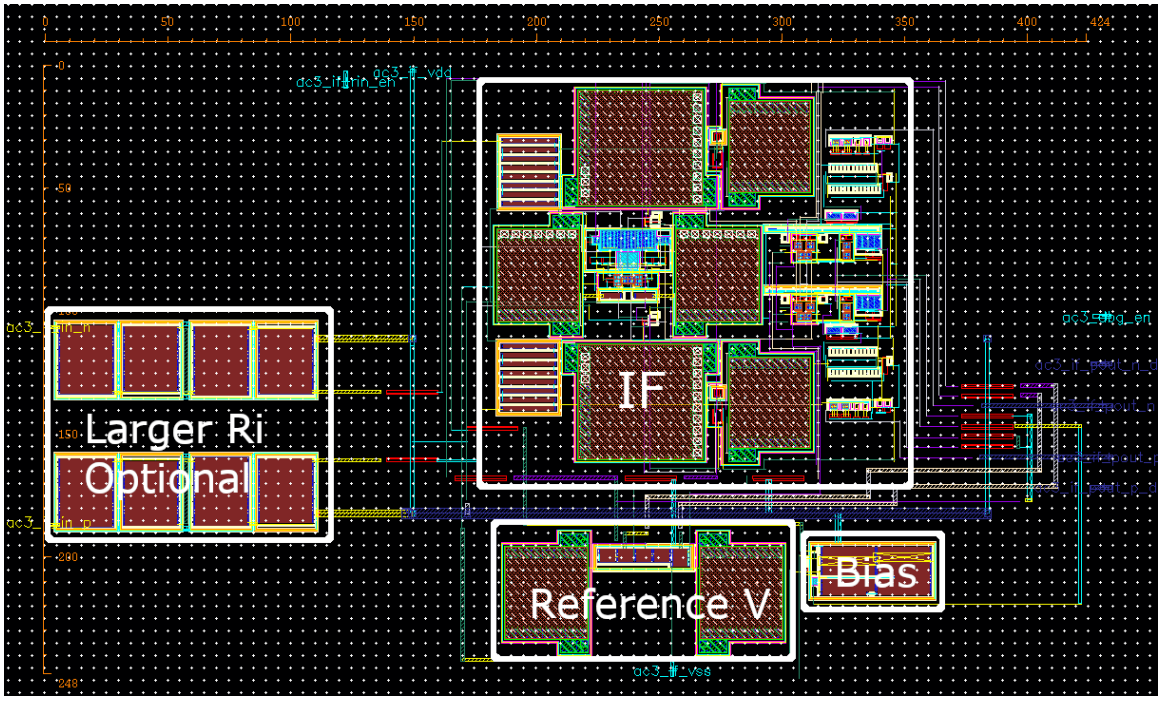

Figure 4.6: Close up plot of analog IFC circuit layout with the complete analog channel - with internal reference voltage and bias currents supply circuits, in 130 nm CMOS technology, $Area = 250\ \mu m * 600\ \mu m = 0.15\ mm^2$. Without inverter bank and transmission gates, present in Figure 4.5. Layout done in Cadence.

with wirebond parasitics and 2 pF load in every output did not affect the circuit behavior and pulse output. But, as expected, during measurement these intermediate outputs were important to debug the prototype.Table 4.1 presents the analog IFC pad list. Table 4.2 presents the complete channel analog IFC pad list. Table 4.3 presents the SCB IFC pad list. The direct current (dc) values are indicative default values and can be changed, as for example for all references.

Table 4.1: Analog IFC prototype pads

Schematic Name	PCB Label	Type	dc Value (V)	Description
v_{ip}	IN-P	input	-	Positive input signal
v_{in}	IN-N	input	-	Negative input signal
v_{op}	AMPOUT-P	output	-	Amplifier output
v_{on}	AMPOUT-N	output	-	Amplifier output
P_{outp}	POUT-P	output	-	Positive pulse output
P_{outn}	POUT-N	output	-	Negative pulse output
V_{DD}	VDDA	power	0.9	Power Supply Rail
$Ground$	GND	power	0	Ground
V_{thp}	VTH-P	reference	0.6	Positive threshold voltage
V_{thn}	VTH-N	reference	0.4	Negative threshold voltage
VCB	VCB	reference	0.5	Bootstrap reference voltage
V_{refrac}	VSTARVEDINV	reference	0.24	Starved inverter voltage, sets refractory period
$Ground$	VCTRLCOMP	power	0	Comparator Ground, connected outside to ground
V_{midc}	VMIDCOMP	reference	0.5	Comparator output intermidiate point, before starved inverters, set by RBC
V_t	VTURNOFF	reference	0.5	Comparator dynamic bias reference
I_{COMP}	IBIASCOMP	power	draws 2 µA	Comparators reference current
I_{AMP}	IBIASAMP	power	draws 1 µA	Amplifier reference current
V_{cm}	VCMAMP	reference	0.5	Amplifier output CM
V_{cmc}	VCMCOMP	reference	0.5	Comparator input CM

Acronyms: replica bias circuit (RBC), common-mode (CM).

Table 4.2: Analog complete channel IFC prototype pads

Schematic Name	PCB Label	Type	dc Value (V)	Description
v_{ip}	IN-P	input	-	Positive input signal
v_{in}	IN-N	input	-	Negative input signal
P_{outp}	POUT-P	output	-	Positive pulse output
P_{outn}	POUT-N	output	-	Negative pulse output
V_{DD}	VDDA	power	0.9	Power Supply Rail
$Ground$	GND	power	0	Ground

Table 4.3: SCB IFC prototype pads

Schematic Name	PCB Label	Type	dc Value (V)	Description
v_{ip}	IN-P	input	-	Positive input signal
v_{in}	IN-N	input	-	Negative input signal
P_{outp}	POUT-P	output	-	Positive pulse output
P_{outn}	POUT-N	output	-	Negative pulse output
$Ctrl$	IBIASAMP	output	-	Control signal, OR of both pulse outputs
v_{op}	AMPOUT-P	output	-	Amplifier output
v_{on}	AMPOUT-N	output	-	Amplifier output
V_{DD}	VDDA	power	0.9	Power Supply Rail
$Ground$	GND	power	0	Ground
$ENAmp$	VCMAMP	reference	0.9	Amplifier enable
$ENComp$	VCB	reference	0.9	Comparator enable
$Ground$	VCTRLCOMP	power	0	Comparator Ground, connected outside to ground

4.1.1 Design of the Testing PCB

A print circuit board (PCB) to test the IFC prototypes has been designed and fabricated. Figure 4.7 presents the IFC prototype test board block diagram. The input adaptation block can be connected to the input, or not, using jumpers, it sets the input CM and adds the capability of adding a capacitor and resistor in series with the input signal before the IFC, as in the complete analog channel IFC prototype described in 4.1, Figures 4.5 and 4.6, adding versatility to the test of the analog and SCB IFCs. As described in section 4.1, the analog IFC has pads with the amplifier output nodes, signals v_{op} and v_{on} in the schematic, Figure 3.3, that have label AMPOUTP and AMPOUTN in the PCB. These two signals were measured directed with the oscilloscope and were also connected to the external IC chips to replicate the comparison stage of the IFC. These external IC chips to amplify and compare the analog IFC intermediate AMPOUT signals were only used in the case of the first analog IFC that did not have output TFFs, to debug the IC, in case the pulse outputs did not have enough current to drive the output probes. These blocks, external output signal processing ICs and negative supply generation block, were not used and not soldered to the PCB, when testing the second analog IFC prototype, Figure 4.1, and the SCB IFC prototype, Figure 4.2, that have output TFF after the pulse outputs. As the external negative supply generation IC chip uses a switched-capacitor voltage converter circuit and can add noise to the measurement, through ground coupling. Certain blocks of the PCB circuit were electronically simulated in SPICE.

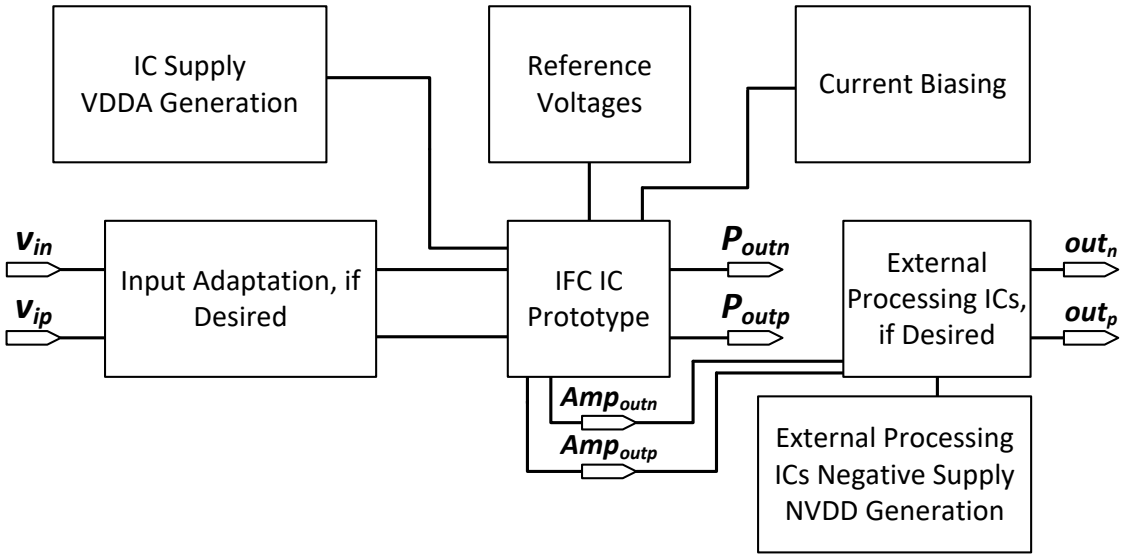

Figure 4.7: IFC prototype test board block diagram.

Figures 4.8, 4.9, and 4.10 present the PCB schematic. The board was designed with two layers. The top layer has three power planes: V_{DD} at 5 V (named VDD in the board), analog power V_{DDA} of 0.9 V generated on the board (named VDDA in the board), negative supply generated on the board – NV_{DD} (named NVDD in the board), for external PCB optional chips that process the IFC chip outputs; and a ground plane in the bottom layer. As described previously, these optional external PCB chips were included to be used in a first analog IFC prototype without output TFF. Because without the output TFFs it was not certain that the available laboratory oscilloscope could measure the fast and low width pulse outputs. Due to resolution limitation, 2 GHz, and available active and passive probes impedance. These external chips were not needed and were not used in the measurements presented in this dissertation, as all following prototypes had TFFs in the pulse outputs, as will be detailed in sections: 4.1.2, 4.2.1, 4.2.2, 4.3.1, and 4.3.2.

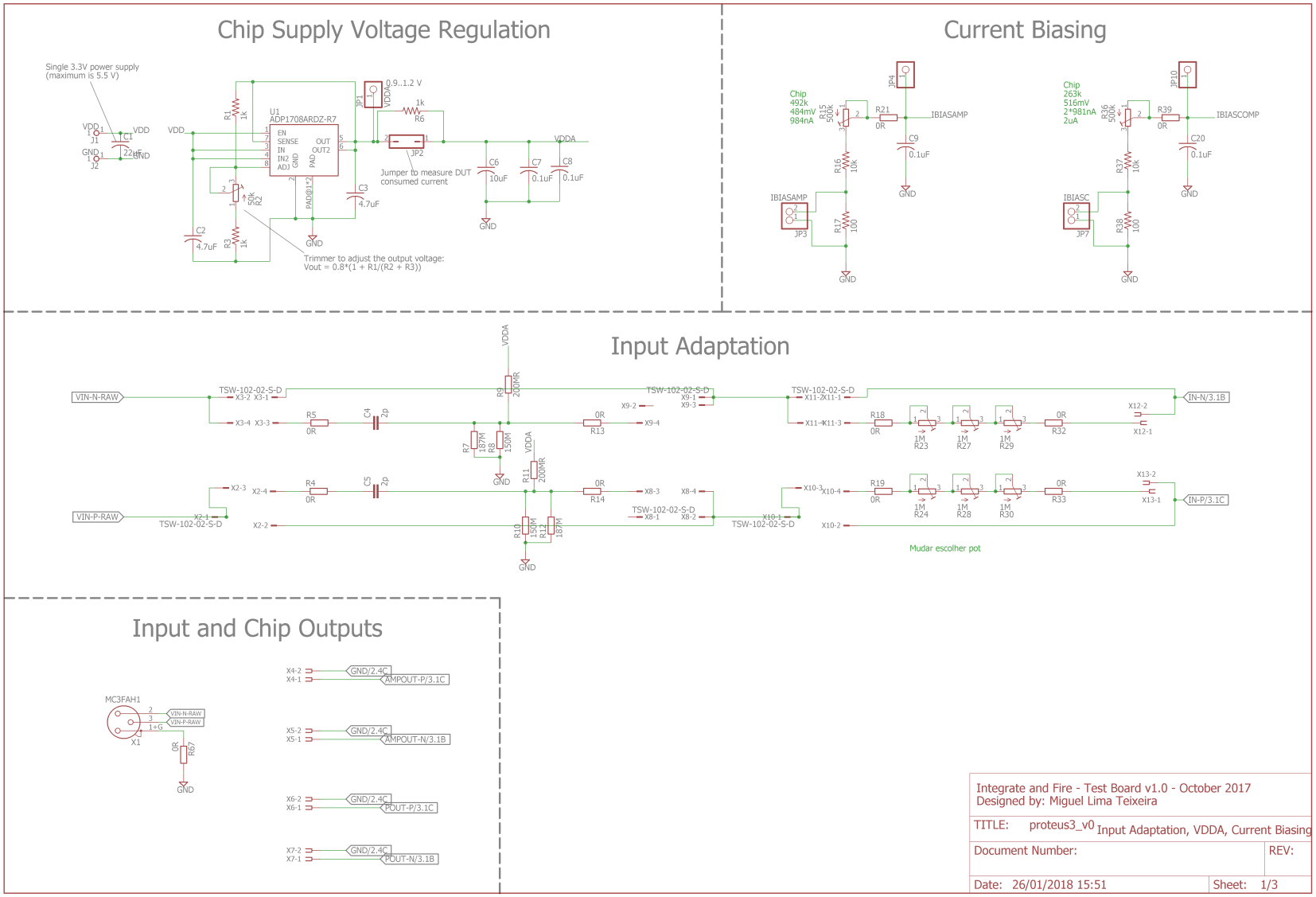

Figure 4.8: IFC prototype test board schematic for PCB, page 1.

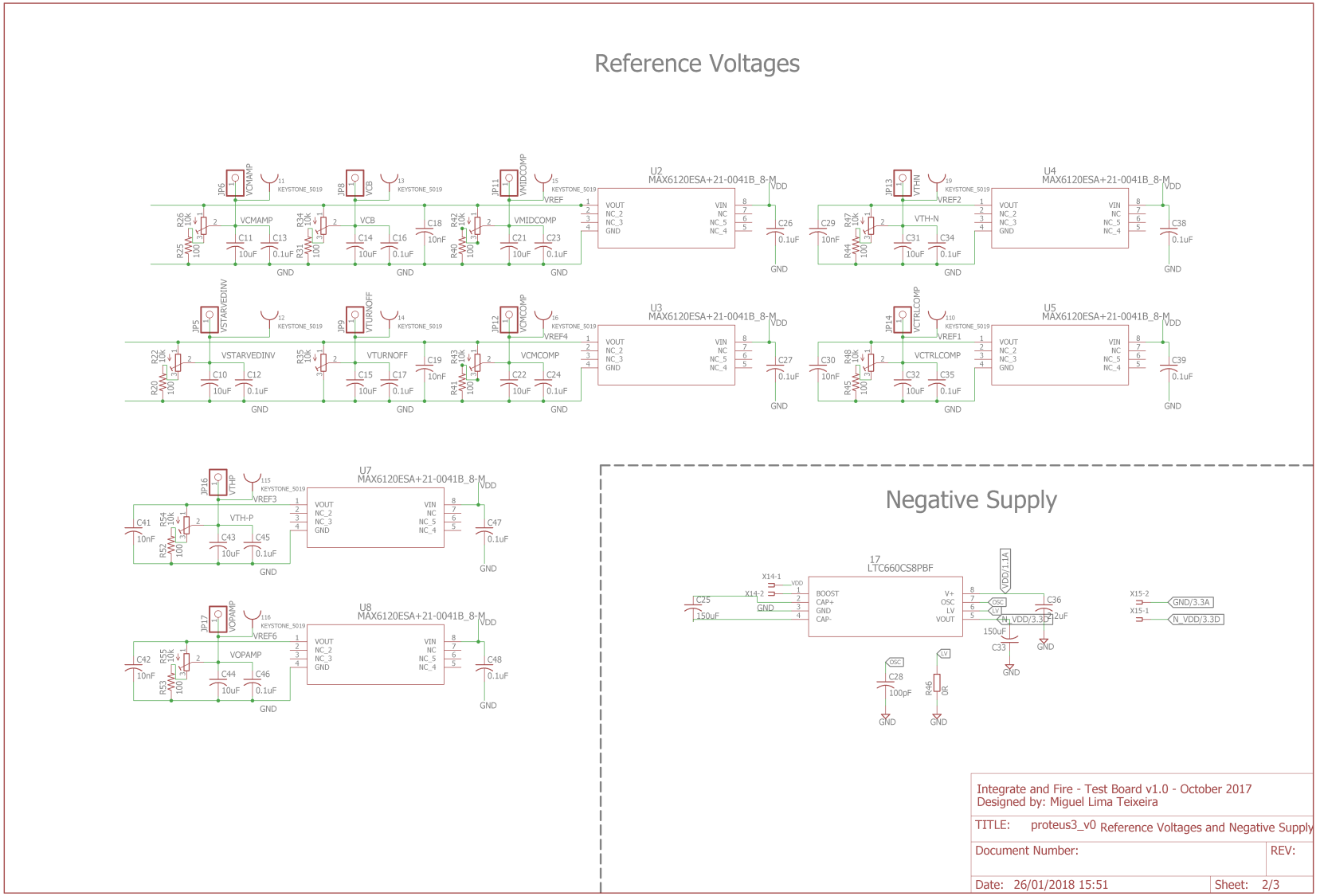

Figure 4.9: IFC prototype test board schematic for PCB, page 2.

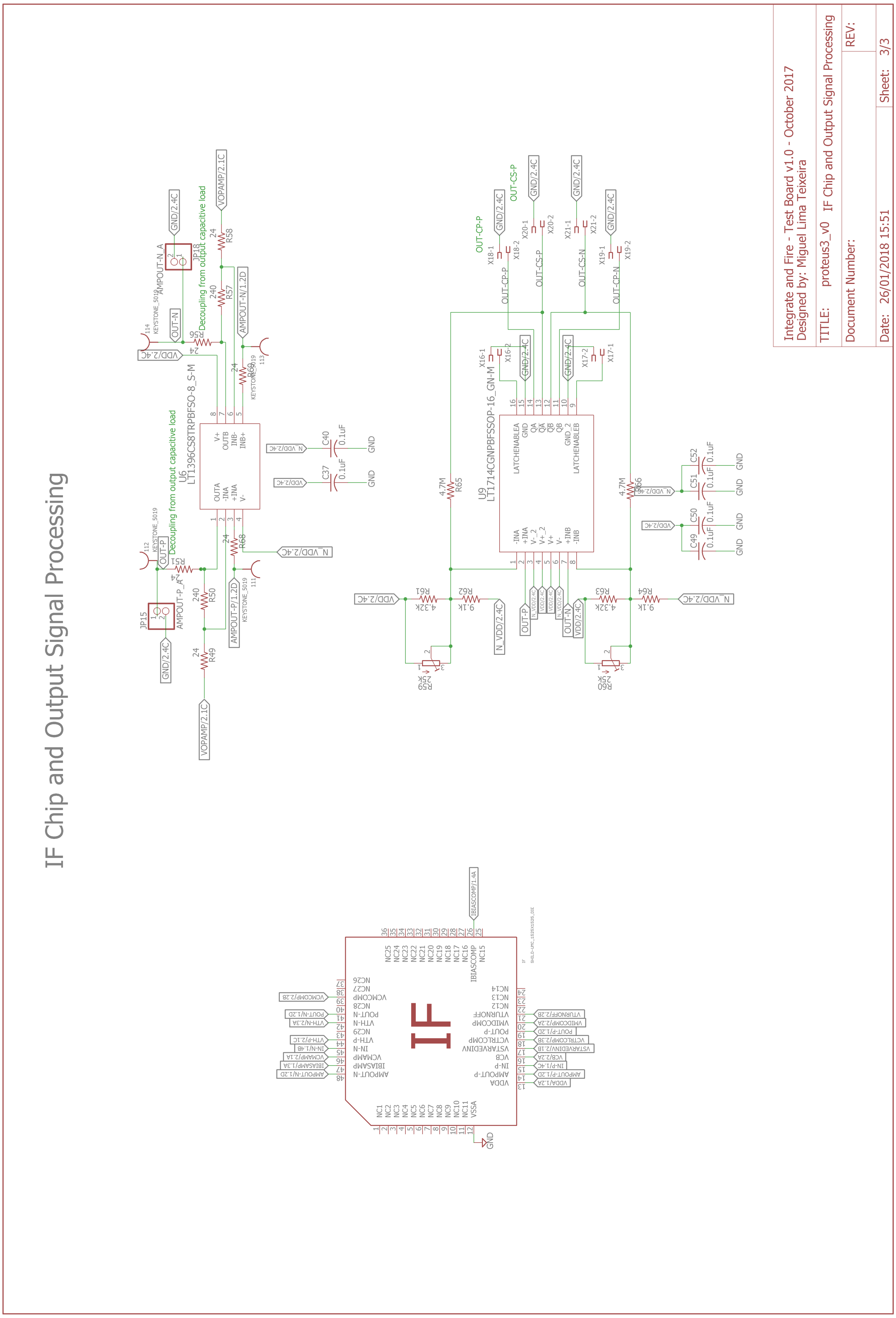

Figure 4.10: IFC prototype test board schematic for PCB, page 3.

Figure 4.11 presents the PCB layout with power planes. Figure 4.12 presents the PCB layout without showing the power planes, to clearly show the connections. The PCB only has an analog power supply ranging from 0.9 V to 1.2 V, named VDDA generated from VDD external power supply ranging from 3.3 V to 5.5 V, and also a NVDD of -5 V generated from VDD. As referred before, the PCB top layer has VDD power plane in all the board, with exception of a square with VDDA next to VDDA pin of the chip breakout board and a small square in the PCB bottom right corner with NVDD power plane. The PCB bottom layer has ground power plane. The chip was wirebonded to a small PCB break out board to have versatility in changing breakout boards in the main PCB, by soldering and desoldering only the breakout board, when required. This together with the fact that the smaller pitch is only required in the smaller breakout board reduced the PCB production cost significantly. the PCB routing was carefully designed to reduce parasitics in signal lanes and increase decoupling capacitance in power lanes. The PCB floor-planing was done to minimize the area, reducing the PCB cost, and having a signal flow from left to right, input to output, respectively. With an easy and intuitive disposition of control voltages, input and output signal, to make it easier to test the prototypes in the lab. The PCB versatility was obtained by having jumpers to connect certain PCB circuit parts and also reroute the input signal, and having the possibility of testing different prototypes, analog and SCB IFCs in the same PCB. All regulator voltages and chip intermediate signals - only present in the analog IFC prototype, have probe pads for easy measuring.

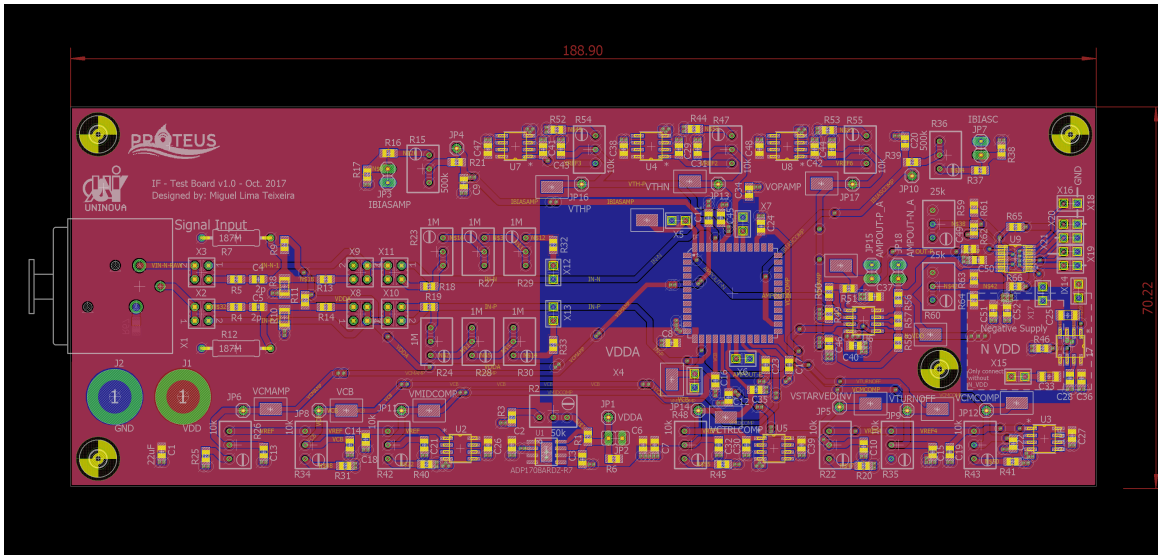

Figure 4.11: PCB layout of the IFC prototype test board, showing the power planes.

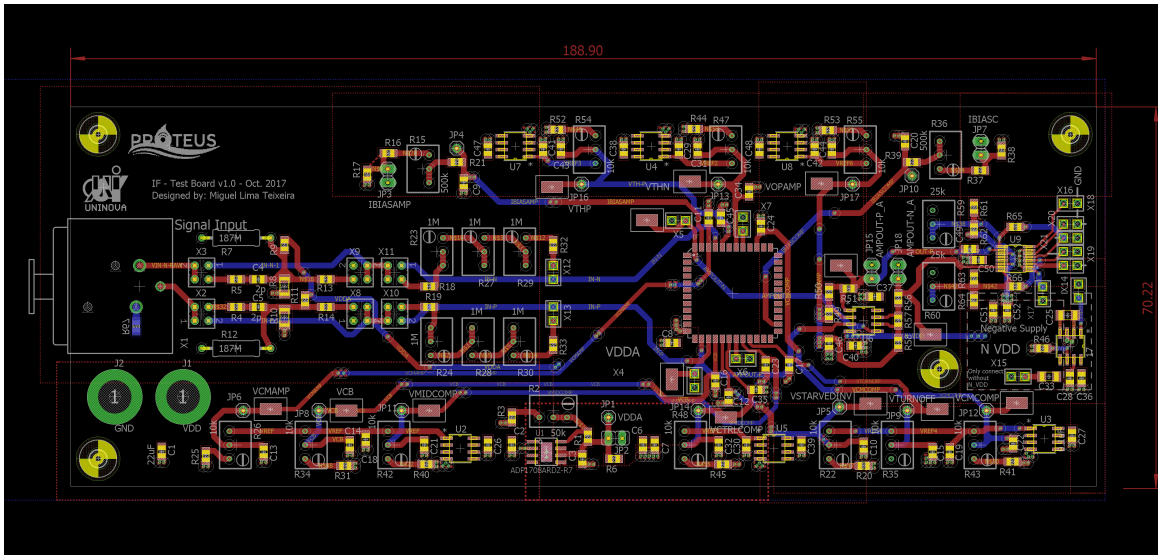

Figure 4.12: PCB layout of the IFC prototype test board, not showing power planes.

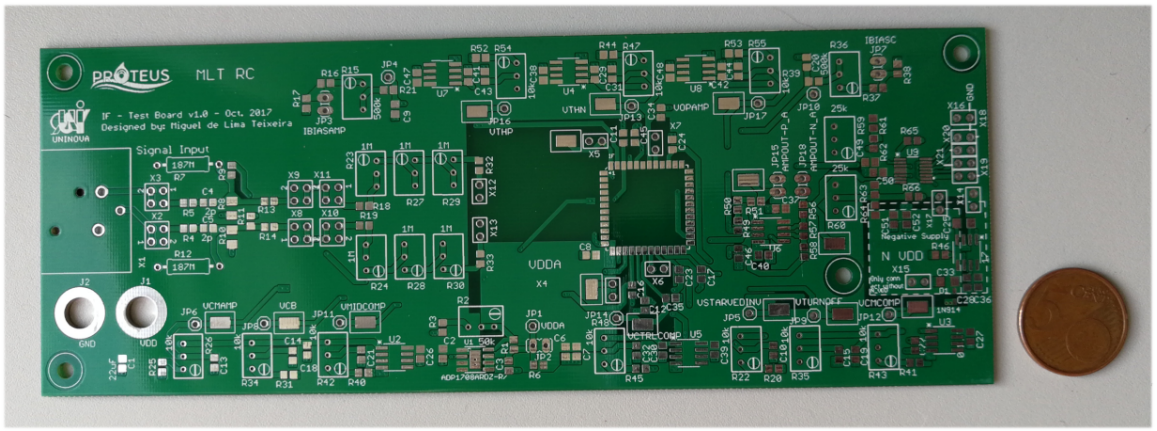

Figure 4.13: Unpopulated PCB IFC prototype test board, front.

The current biasing in the analog IFC amplifier and comparators is set by voltage drop with variable resistor, instead of the ideal current source present in their schematic, as can be seen in the prototype PCB schematic 4.8. $V_{biasAmp}$ and $V_{biasComp}$ are the voltages measured in IBIASAMP and IBIASCOMP nets in 4.8, respectively, that connect to the chip pads. The default values, that are the same as the voltage measured in the dc operating point simulation for the ideal current sources, are $V_{biasAmp}$ = 484 mV and $V_{biasComp}$ = 516 mV.

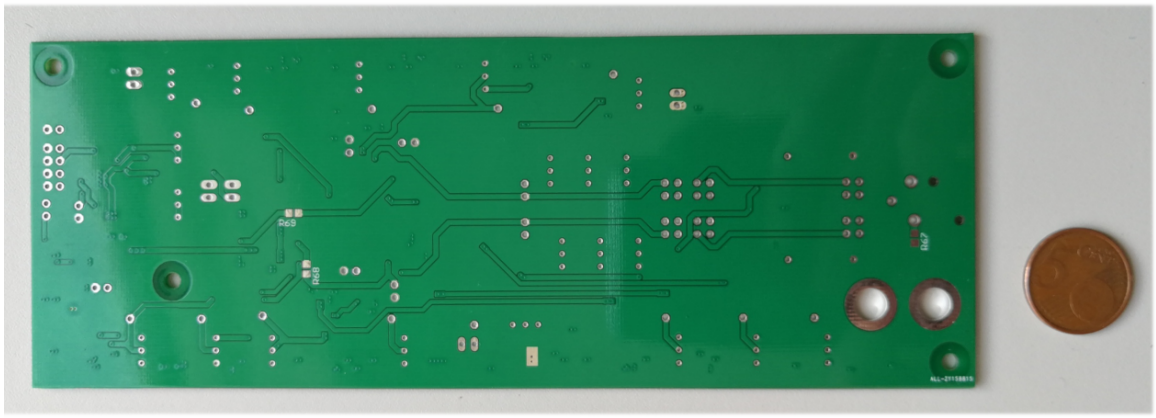

Figure 4.14: Unpopulated PCB IFC prototype test board, back.

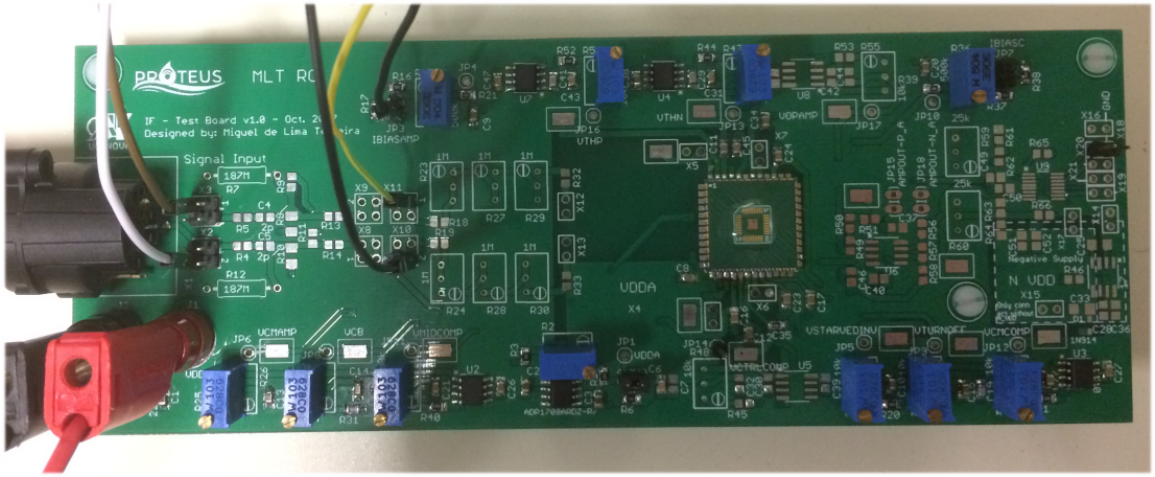

Figure 4.15: PCB IFC prototype test board, assembled for Analog IFC chip measurement.

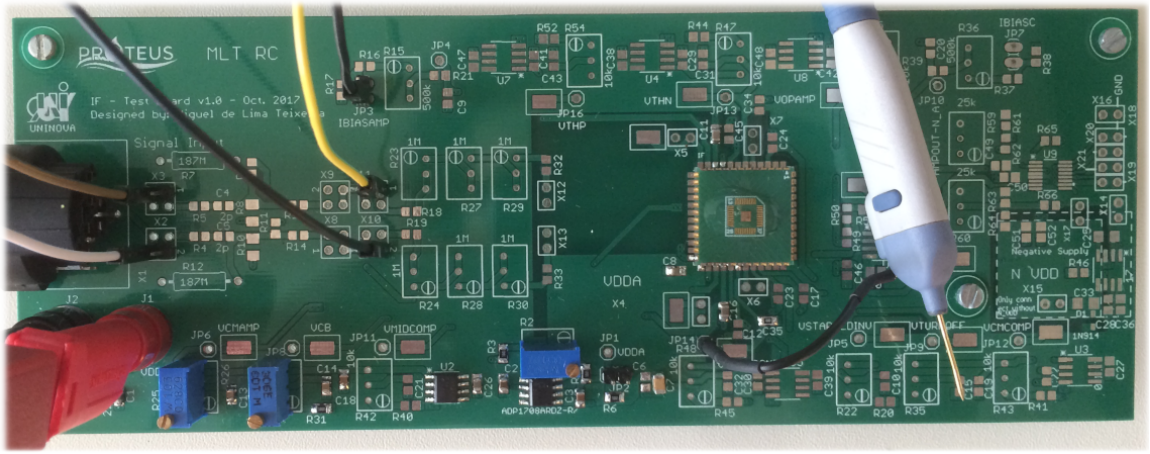

Figure 4.16: PCB IFC prototype test board, assembled for the SCB IFC chip measurement.

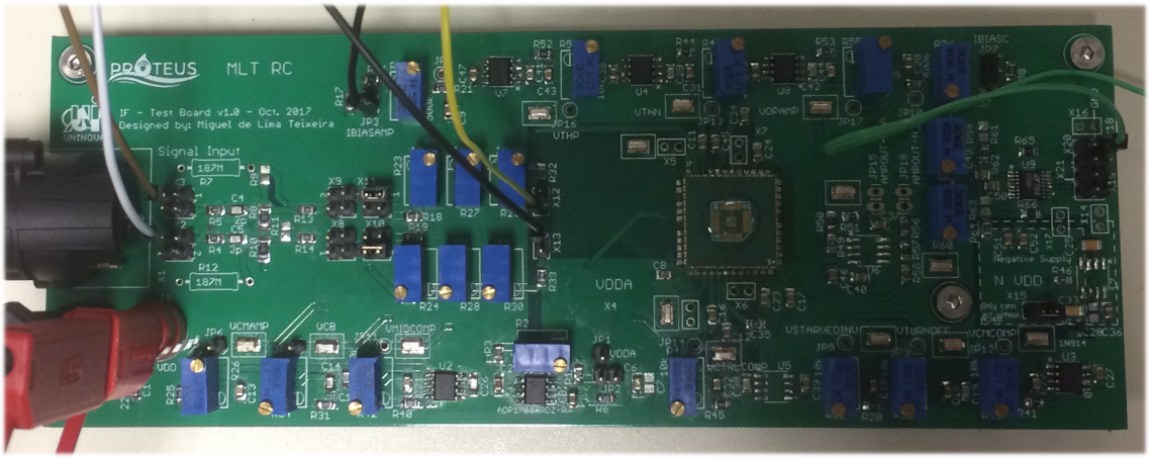

Figure 4.17: PCB IFC prototype test board, assembled for Analog IFC chip measurement. Full Assemble, analog IFC first version, chip without TFF in pulse outputs.

4.1.2 Input Signal Reconstruction

The input signal reconstruction from the output pulse train can be achieved either by direct interpolation of the integration curve, or by more advanced methods, such as weighted low-pass kernel method (WLPK) for spiking neuron signals [8, 11], or [68–72] as presented in 2.3. All reconstruction methods present a reconstruction error. From the triangular interpolation of the integration curve, the input signal information can be obtained from the IPI, equation (3.2), considering that the integration value is constant.

The first approximation of the integration area, constant ka, for the defined thresholds is given by:

$$ka = v_{outpp}\, R_{in} C_f \tag{4.1}$$

where v_{outpp} is the amplifier output peak-to-peak voltage, for the defined comparator thresholds.

In practice ka is calculated for a certain measurement by equation (4.2):

$$ka = v_{inp}\, \mathrm{IPI}_{min} \tag{4.2}$$

where v_{inp} is the input peak voltage and IPI_{min} the minimum IPI, that occurs at the input voltage peak.

The accuracy of the IFC pulse output measurement should be high to minimize the error in determining the rise and fall timings of the pulse outputs, that are the square wave outputs of the TFFs. The accuracy of this measurement introduces an error in the

IPI calculation and so in the input signal reconstruction. The TFFs in the pulse outputs reduce the measurement accuracy requirement. Each square wave transition corresponds to a IFC pulse. Without TFFs the measure accuracy would correspond to a minimum detectable signal requirement in the time domain of 0.2 ns, as the pulse width is approximately 2.65 ns, for the two IFC versions. With TFFs in the pulse outputs, the accuracy requirement is set by the output square wave transition time and the minimum IPI. The minimum IPI is approximately 1.3 μs for the analog conventional IC and approximately 0.2 μs for the SCB IFC. The output square wave transition takes approximately 18 ns from low to high level and 7 ns from high to low level. Considering the minimum transition time, it is found that a measurement sampling rate of 0.2 GSa/s is enough to capture the transitions from the TFFs, measuring correctly the pulse outputs. This corresponds to a minimum detectable signal requirement in the time domain of 5 ns. The prototype measurements were made with a Rohde & Schwarz (R&S) RTO 1022 2 GHz, 10 GSa/s, oscilloscope that is capable of clearly measuring the fast transitions with high resolution, using passive probes, as R&S RT-ZP10 500 MHz, or the high BW single ended active probes R&S RT-ZS30 2 GHz. All measurements have been made with the R&S RT-ZS30 active probes. The low amplitude input signals were generated with an Audio-Precision ATS-2 Audio Test System. The inverter-based amplifier fast-Fourier-transform (FFT) and Bode plot were measured with the ATS-2. Figure 4.18 presents the laboratory measurement setup. The AMPOUT signals were only measured in the ATS-2 for the SCB IFC, to measure the FFT and Bode plot. The ATS-2 sends a trigger signal to the R&S oscilloscope during the pulse outputs measurement.

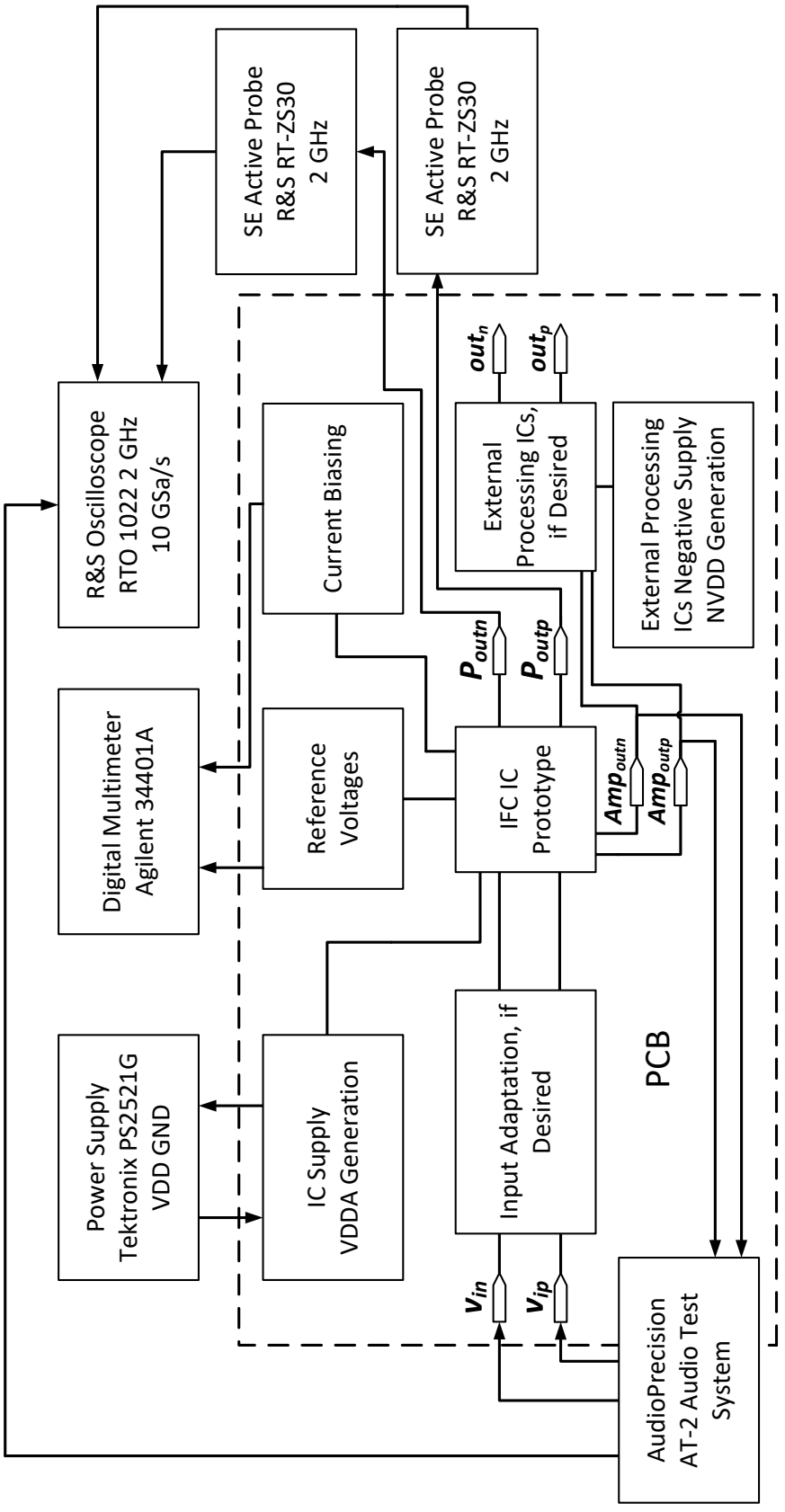

Figure 4.18: IFC prototype test board block diagram and laboratory measurement setup.

The reconstruction algorithm consists in the following steps:

1. The prototypes pulse train outputs (square wave outputs of the TFF) are recorded with the RTO oscilloscope.

2. A software algorithm detects the transitions in the square waves and stores in a time series: the time of occurrence of each transition and the time difference to the previous transition - the IPI, (3.2). Note that each transition corresponds to an output pulse.

3. Considering that the integration value ka is constant, ka is calculated for a certain measurement by equation $ka = v_{inp}\ \mathrm{IPI}_{min}$, where v_{inp} is the input peak voltage and IPI_{min} the minimum IPI that occurs at the input voltage peak.

4. The input wave is reconstructed calculating the input amplitude value for each IPI, considering equation $v_{in}(t_{k+1}) = \frac{ka}{\mathrm{IPI}(t_{k+1})}$, t_{k+1} is the time of occurrence of the second output pulse, that corresponds to the input signal time.

4.2 Analog IFC

The analog IFC version can convert signals with a peak-to-peak amplitude from 0.5 mV to 5 mV and a frequency range of 100 Hz to 4 kHz. The maximum pulse density (average firing-rate) is 50 kHz and the minimum number of pulses is one.

Simulations and measurements with different sinusoidal inputs were performed to measure the firing-rate, the input BW, minimum and maximum input amplitude, and power dissipation of each IFC circuit.

4.2.1 Analog IFC Simulation Results

Figures 4.19 and 4.23 present the simulation results after layout extraction (C+CC and R+C+CC extraction type): the pulse output, IPI - equation (3.2), and reconstructed input signal from pulse output for a differential sinusoidal input with 1 mV amplitude and 1 kHz frequency (A = 1 mV, f = 1 kHz, B = 400 mV, and $/phi$ = 0 rad in equation (3.4) for v_{in} input signal - in- in both figures). The results for the same frequency, but with input amplitude A = 10 mV are presented in Figure 4.20, for A = 600 µV with f = 100 Hz and f = 500 Hz in Figures 4.21 and 4.22, respectively. The input CM is V_{iCM} = 400 mV and

the amplifier output CM is V_{oCM} = 500 mV. The comparator thresholds were set as V_{th-} = 400 mV and V_{th+} = 600 mV. Pout+ (P_{outp} in schematic) is the pulse output for input signal v_{in} larger than the common mode (positive input signal) and Pout- (P_{outn} in schematic) is the pulse output for input signal v_{in} smaller than the common mode (negative input signal). Figures 4.21, 4.22, and 4.23 present simulation results for three different input signals. The IPIs are obtained through step 2 of the reconstruction algorithm, described previously in section 4.1.2, and the reconstruction curves are obtained considering steps 3 and 4. The input signal is reconstructed in Matlab from the measured pulse stream. Through the calculation of the IPI and correspondent input signal voltage, using the simple approximation of equation (3.3) and considering a constant integration area. The area value approximation is given by equation (4.2). Figures 4.21, 4.22, and 4.23 show that for a fixed input amplitude the IPI is inversely proportional to the input frequency.

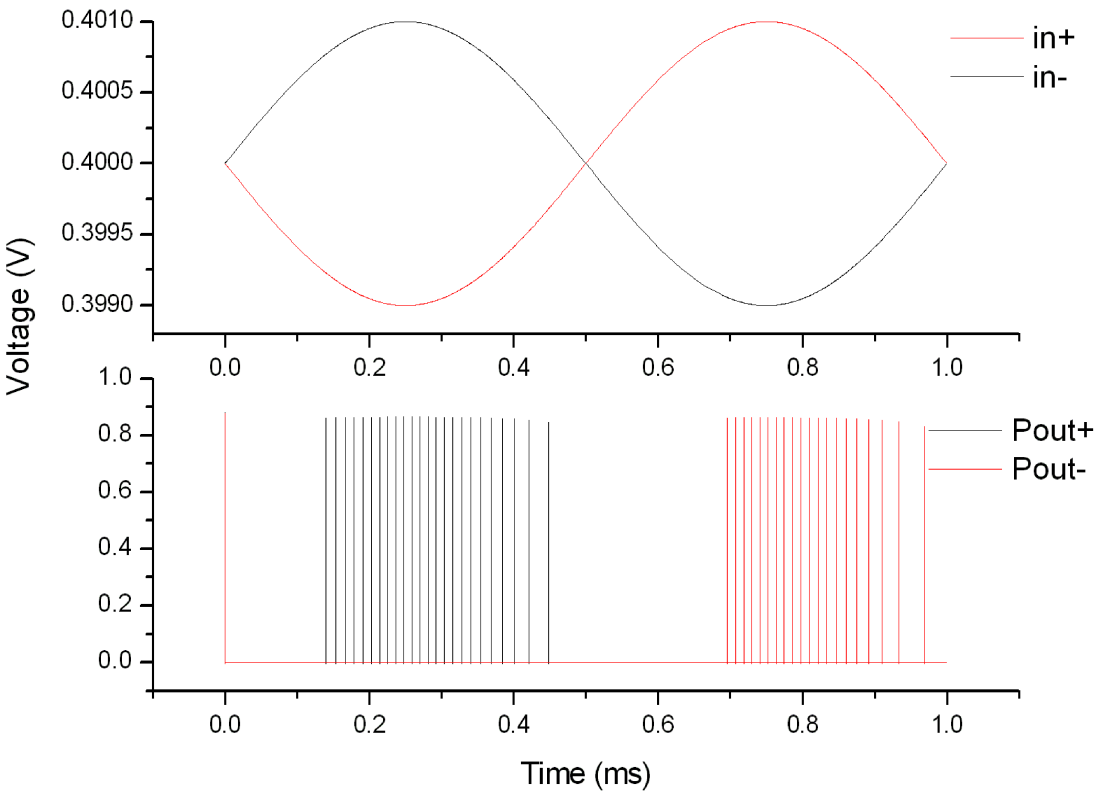

Figure 4.19: Analog IFC simulation results after layout extraction (C+CC extraction type), pulse outputs for input signal with 1 mV peak amplitude and 1 kHz.

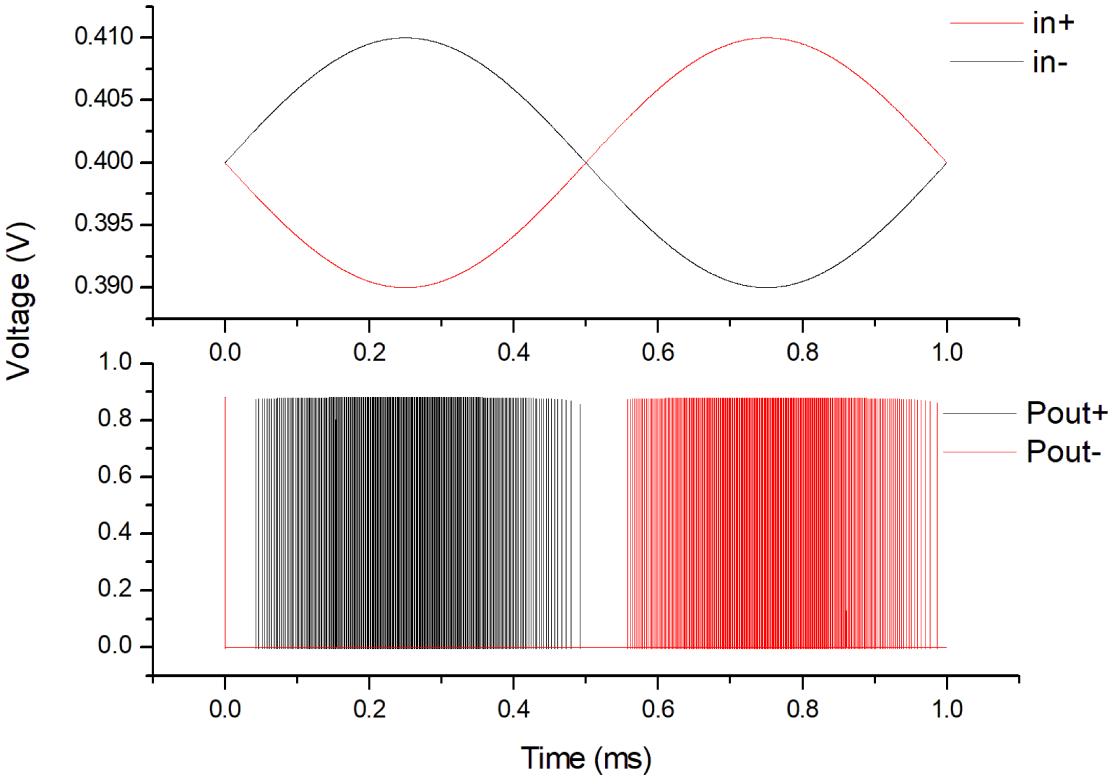

Figure 4.20: Analog IFC simulation results after layout extraction (C+CC extraction type), pulse outputs for input signal with 10 mV peak amplitude and 1 kHz.

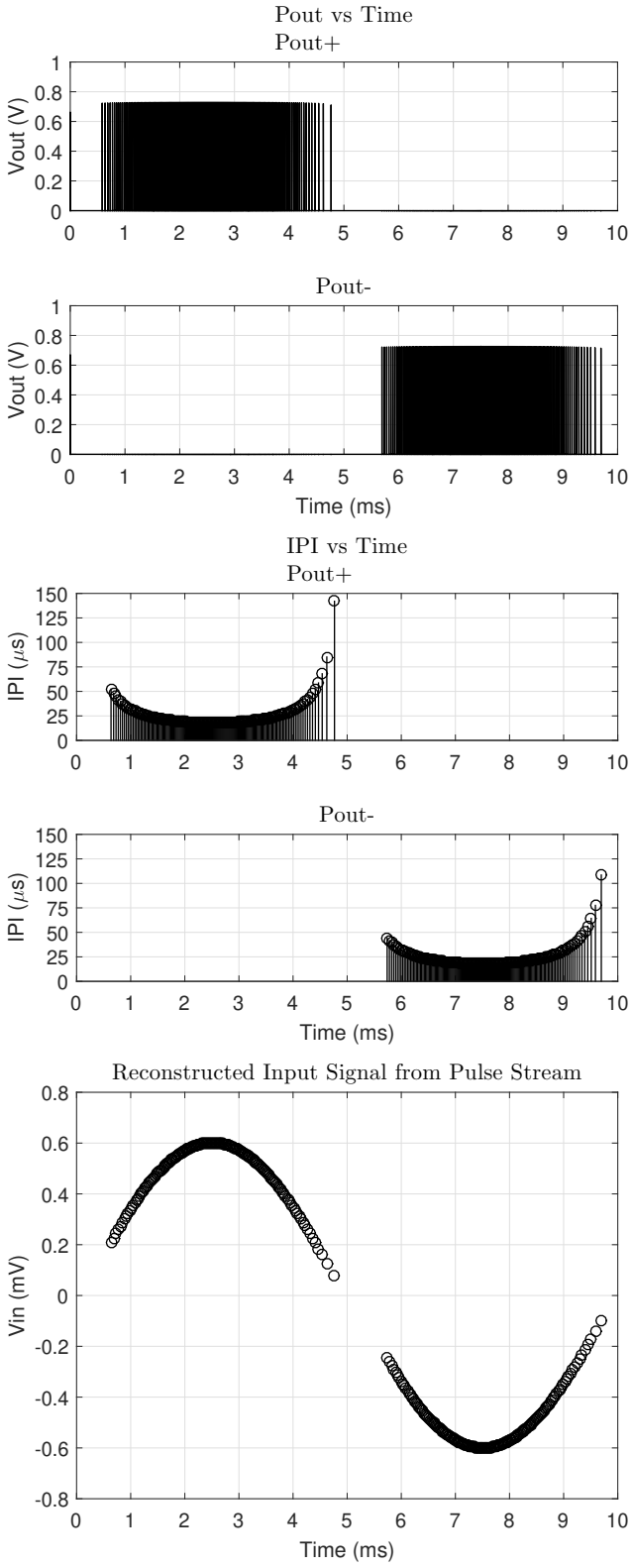

Figure 4.21: Analog IFC simulation results after layout extraction (C+CC extraction type). The top row presents the pulse outputs, the middle row the IPI and the bottom row the reconstructed input sine wave from the pulse outputs for an input signal with 600 µV peak amplitude and a frequency of 100 Hz.

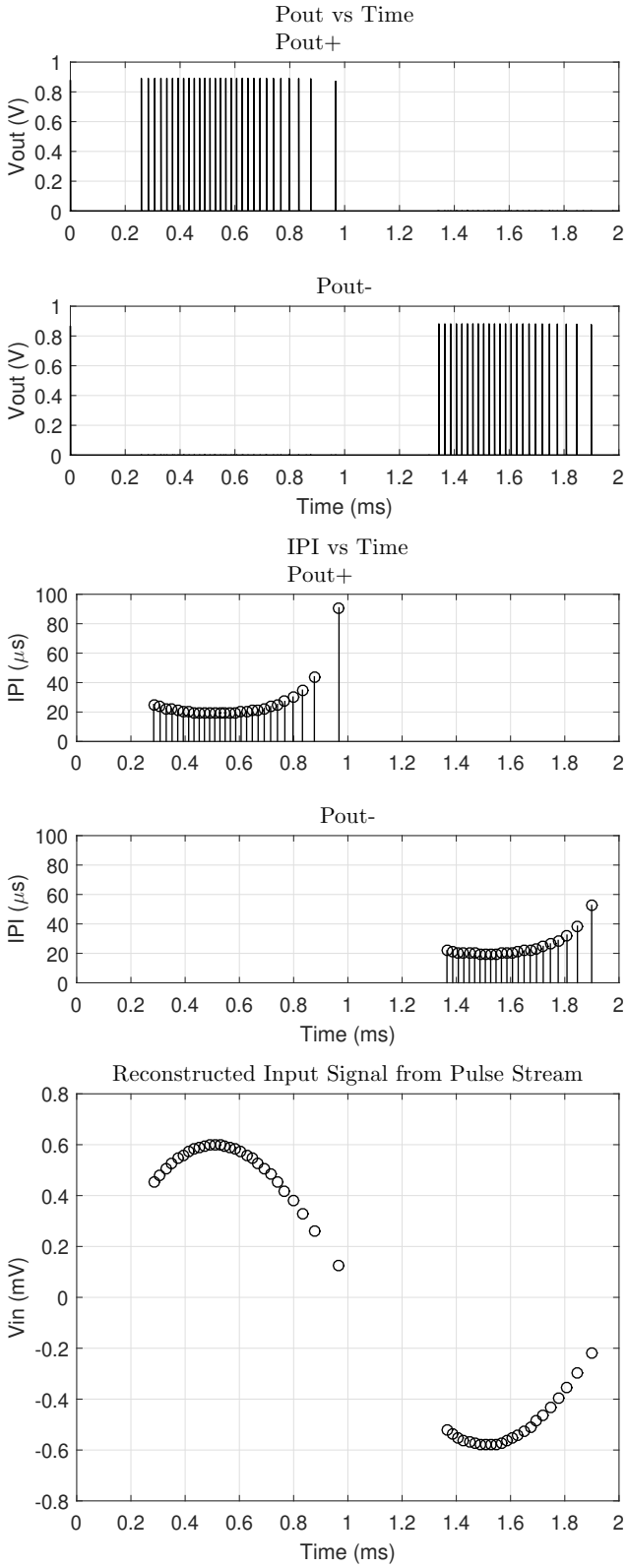

Figure 4.22: Analog IFC simulation results after layout extraction (R+C+CC extraction type). The top row presents the pulse outputs, the middle row the IPI and the bottom row the reconstructed input sine wave from the pulse outputs for an input signal with 600 μV peak amplitude and a frequency of 500 Hz.

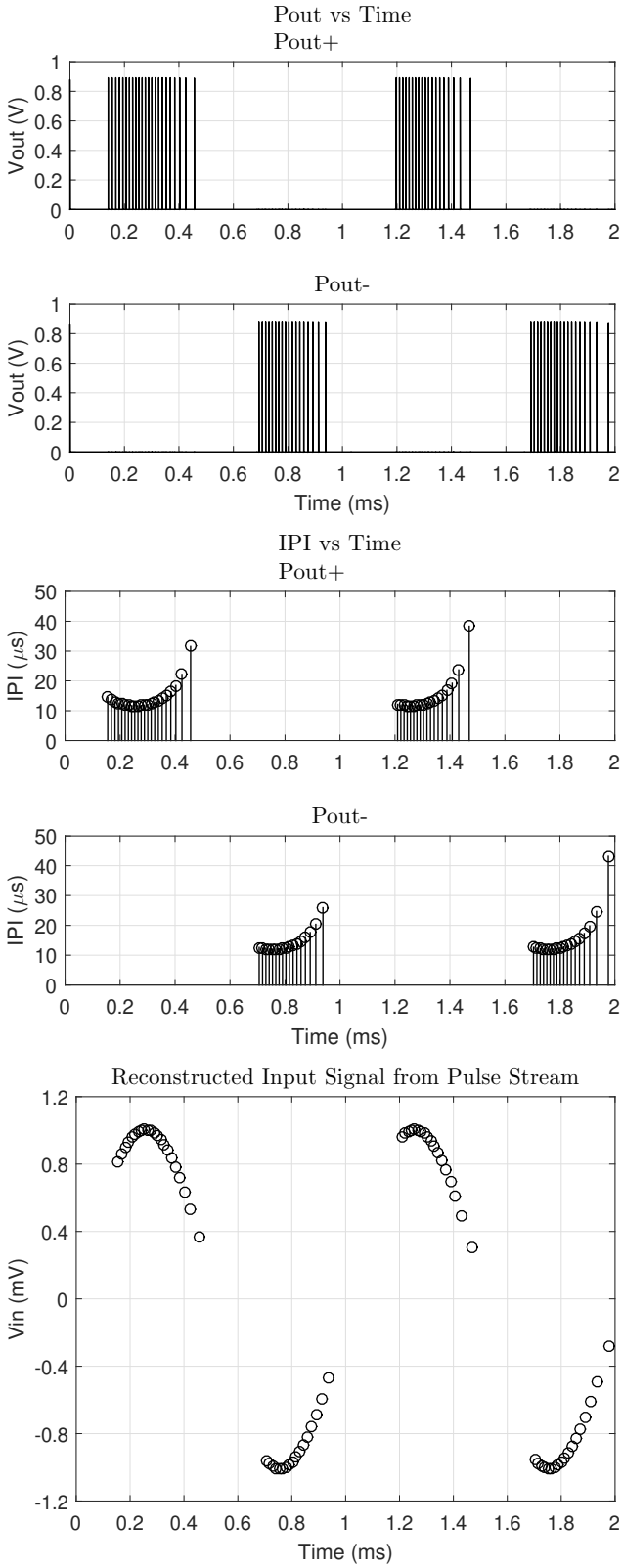

Figure 4.23: Analog IFC simulation results after layout extraction (C+CC extraction type). The top row presents the pulse outputs, the middle row the IPI and the bottom row the reconstructed input sine wave from the pulse outputs for an input signal with 1 mV peak amplitude and a frequency of 1 kHz.

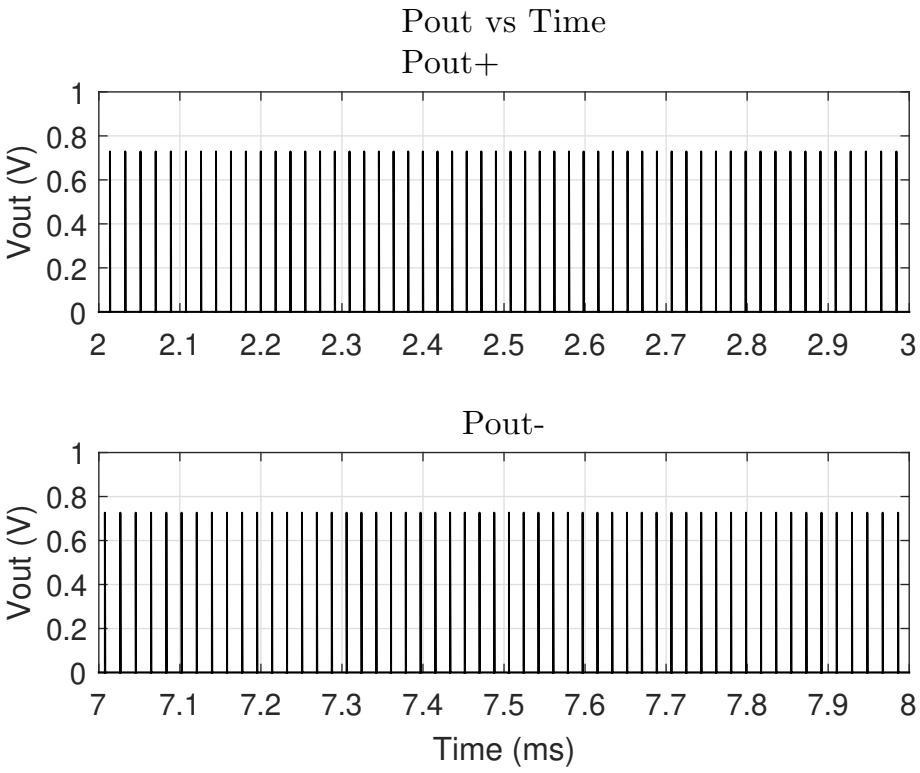

Figure 4.24: Analog IFC simulation results after layout extraction (C+CC extraction type), pulse outputs zoom for input signal with 600 µV peak amplitude and 100 Hz.

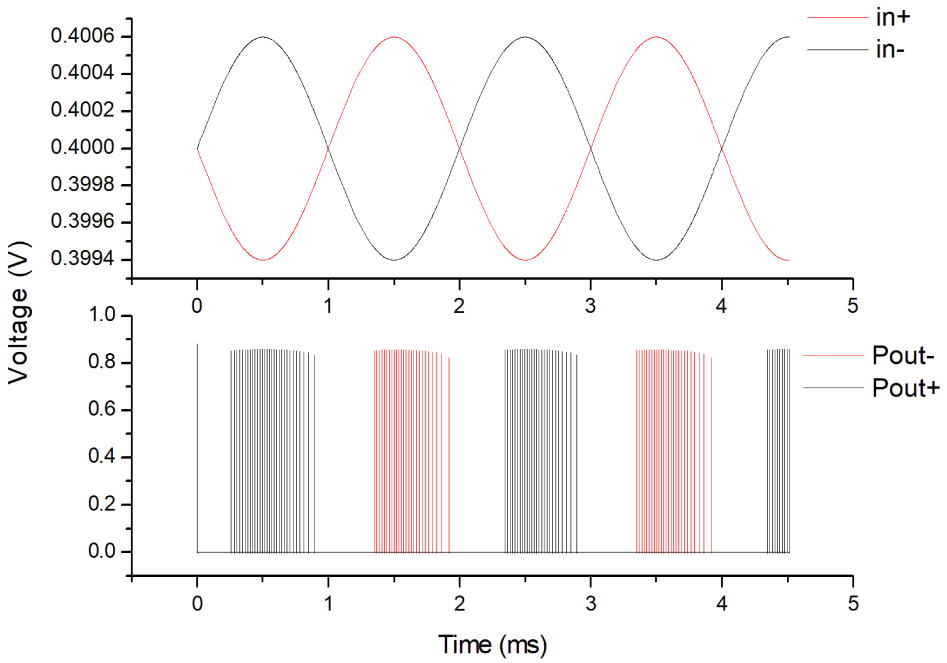

Figure 4.25: Analog IFC simulation results after layout extraction (C+CC extraction type), pulse outputs for input signal with 600 μV peak amplitude and 500 Hz.

As expected, the simulation results show that for higher input amplitude the number of output pulses increases; therefore, the IPI decreases. The minimum IPI is obtained when the input reaches its maximum value, the sinusoidal peaks, positive and negative. The minimum IPI for 1 mV amplitude and 1 kHz input is approximately 11 µs, for 10 mV and 1 kHz input is approximately 1.3 µs, and for 600 µV and 500 Hz input is approximately 18 µs. The first pulse of Pout- at 0 ms is a simulation artifact due to the initial step to define the dc point in the transient simulation. Thus, this pulse should be disregarded. This fact can be verified in Figure 4.25, that presents two input wave periods. Here the artifact pulse appears in Pout+, only in the simulation beginning and not in the other input wave crossings.

Figures 4.26,4.27,4.28, and 4.29 present the complete IFC analog channel simulation results after layout extraction (C+CC extraction type): the pulse output for a differential sinusoidal input with 1 mV peak amplitude and 1 kHz frequency. Internal reference voltages, including thresholds, current biasing, and input resistance value are the same as independent prototyped analog IFC block simulation and measurement results. The minimum IPI for these input signal conditions is 8.6 µs, without the increase of R_{in}, meaning with the same R_{in} of the standalone analog IFC chip.

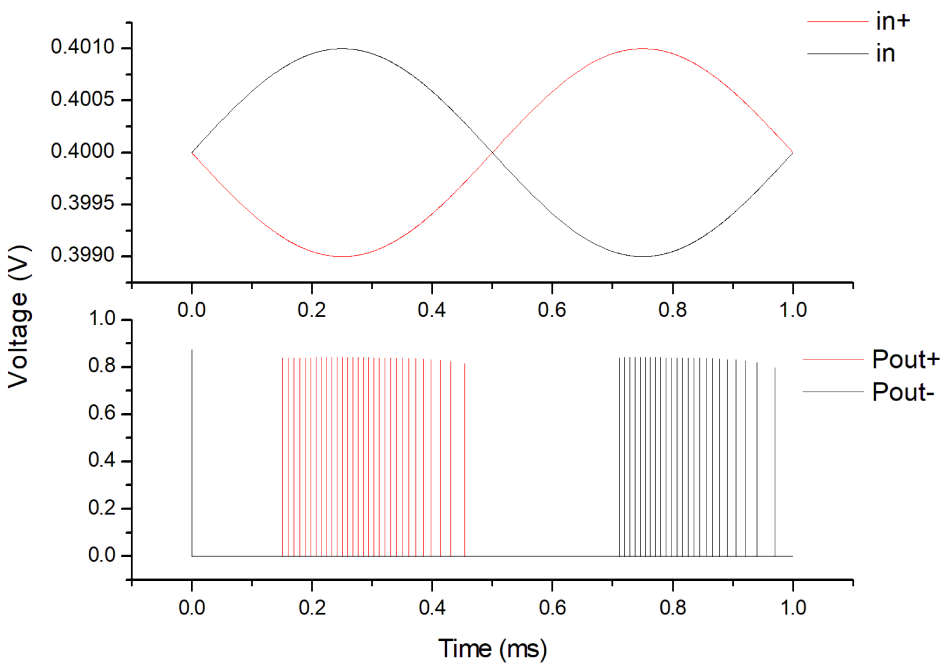

Figure 4.26: Complete analog channel IFC simulation results after layout extraction (C+CC extraction type), pulse outputs for input signal with 1 mV peak amplitude and 1 kHz.

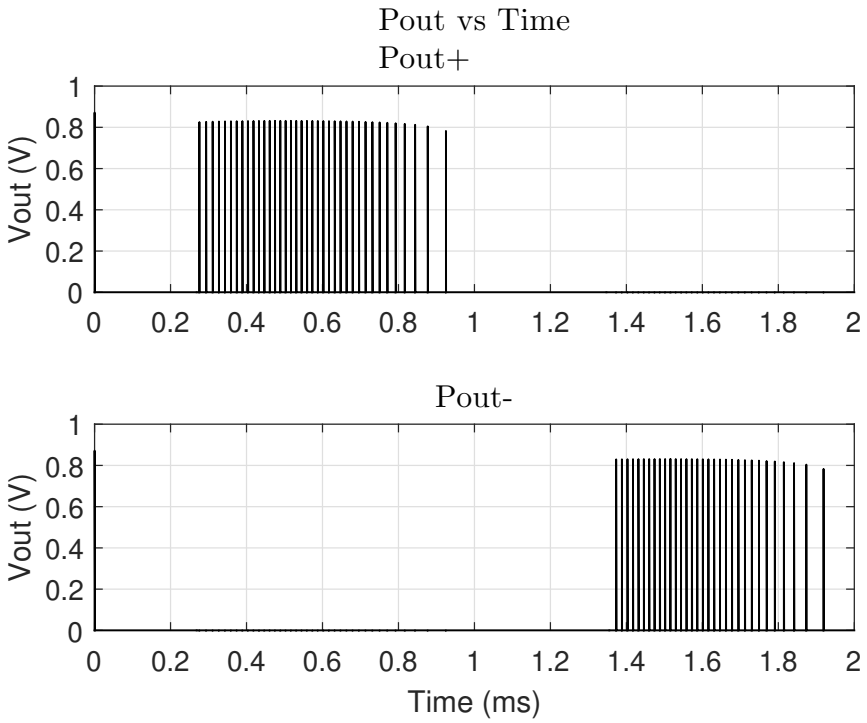

Figure 4.27: Complete analog channel IFC simulation results after layout extraction (C+CC extraction type), pulse outputs for input signal with 600 µV peak amplitude and 500 Hz.

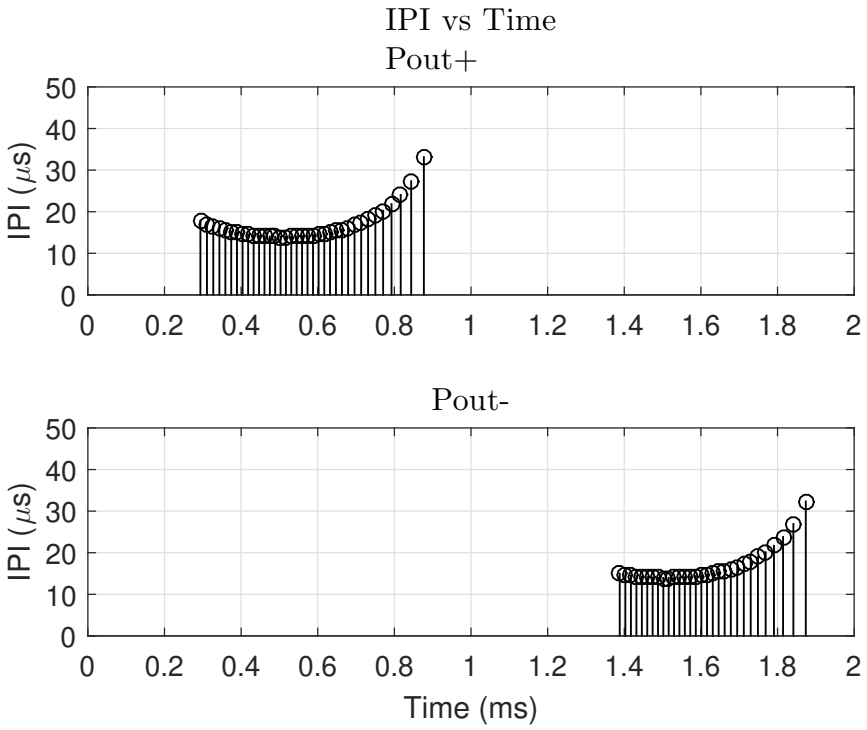

Figure 4.28: Complete analog channel IFC simulation results after layout extraction (C+CC extraction type), IPI from pulse outputs for input signal with 600 μV peak amplitude and 500 Hz.

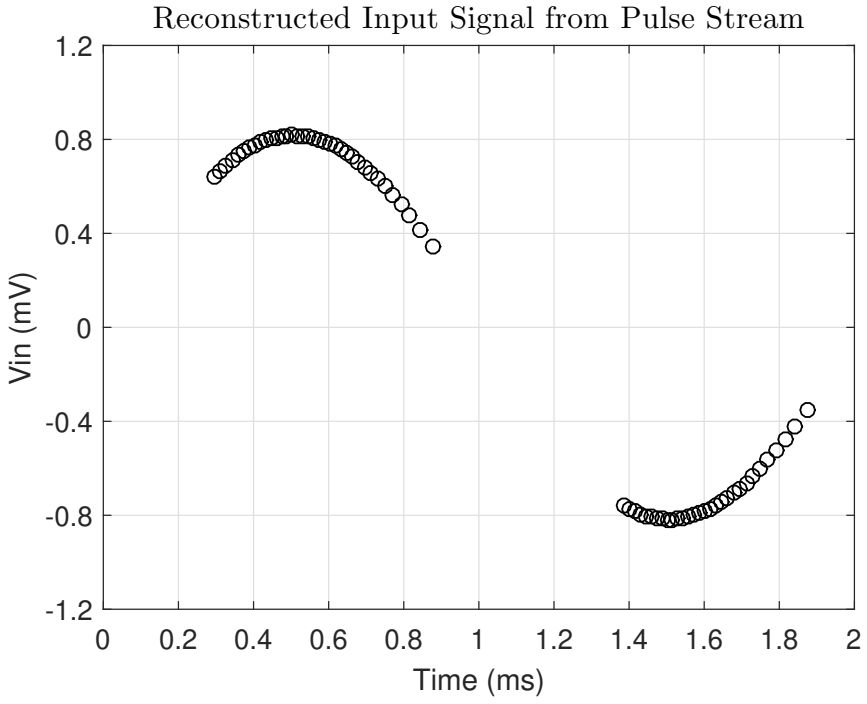

Figure 4.29: Complete analog channel IFC simulation results after layout extraction (C+CC extraction type), reconstructed input sine wave from pulse outputs for input signal with 600 μV peak amplitude and 500 Hz.

As previously referred, the number of output pulses, i.e., the pulse density, is proportional to the input signal amplitude and inversely proportional to the input signal frequency, as can be seen in Figures 4.21, 4.22, and 4.23. On the other hand, the firing-rate is proportional to the input signal amplitude and frequency. The maximum firing-rate as a function of input signal frequency and amplitude is presented for the analog IFC in Fig. 4.30.

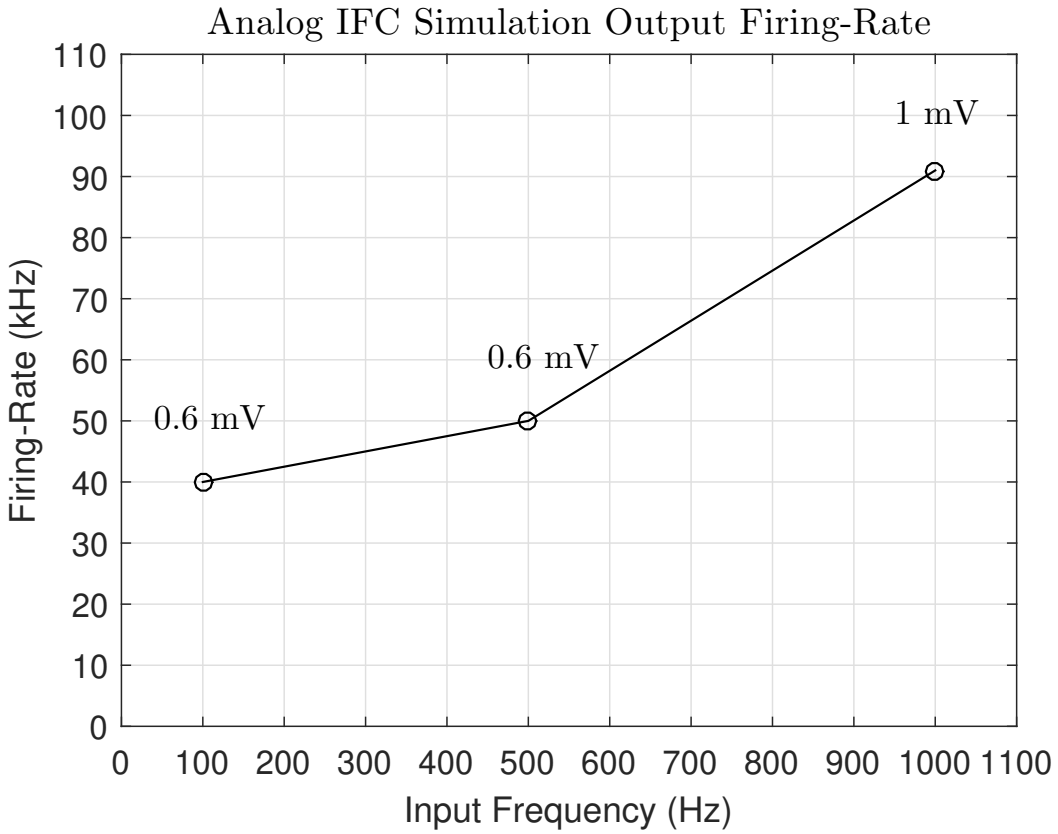

Figure 4.30: Analog IFC Simulation output firing-rate, input peak amplitude in the data points label.

Simulations were run with an electrocardiogram (ECG) input signal to verify the IFC circuit behavior when presented with a biological signal with sparse information. Figure 4.31, Figure 4.32, and Figure 4.33 present the simulation results after R+C+CC layout extraction for an accelerated ECG input signal. The ECG signal is from the PhysioNet ECG-ID database [88, 89], the signal has the original time and amplitude divided by 100. A differential input with adjusted CM, V_{iCM} = 400 mV was created from this ECG signal and used as the analog IFC input. The positive and negative pulse outputs were used to calculate the respective IPI and then make the reconstruction of the ECG signal.

Figure 4.31 presents the positive and negative pulse outputs relative to the positive and negative portion of the ECG signal. Figure 4.32 presents the respective IPI and Figure 4.33 presents the reconstructed ECG signal. The reconstructed signal in Fig. 4.33 shows that the analog IFC is capable of processing ECG signals preserving the QRS complex timing and amplitude information.

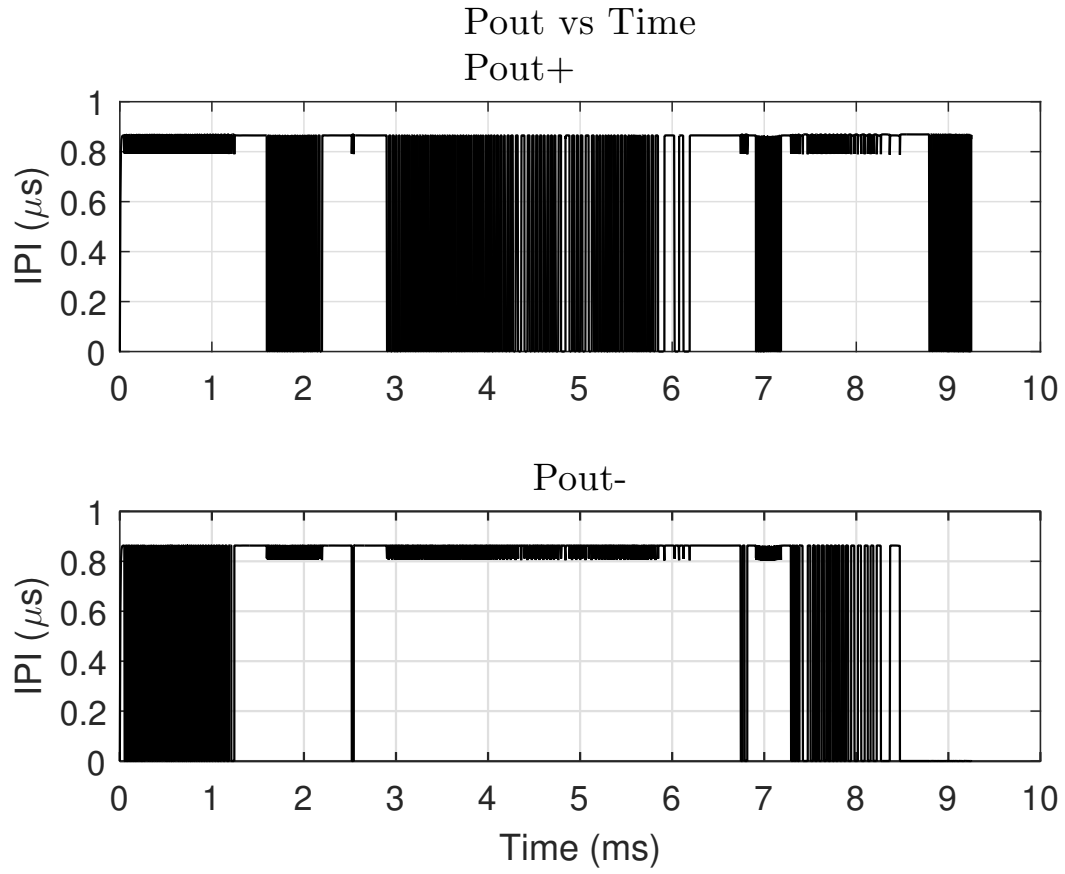

Figure 4.31: Analog IFC version ECG simulation results, pulse output for accelerated ECG input signal (R+C+CC extraction). PhysioNet ECG-ID database ECG [88, 89], with time and amplitude divided by 100. Differential input with adjusted CM, V_{iCM} = 400 mV .

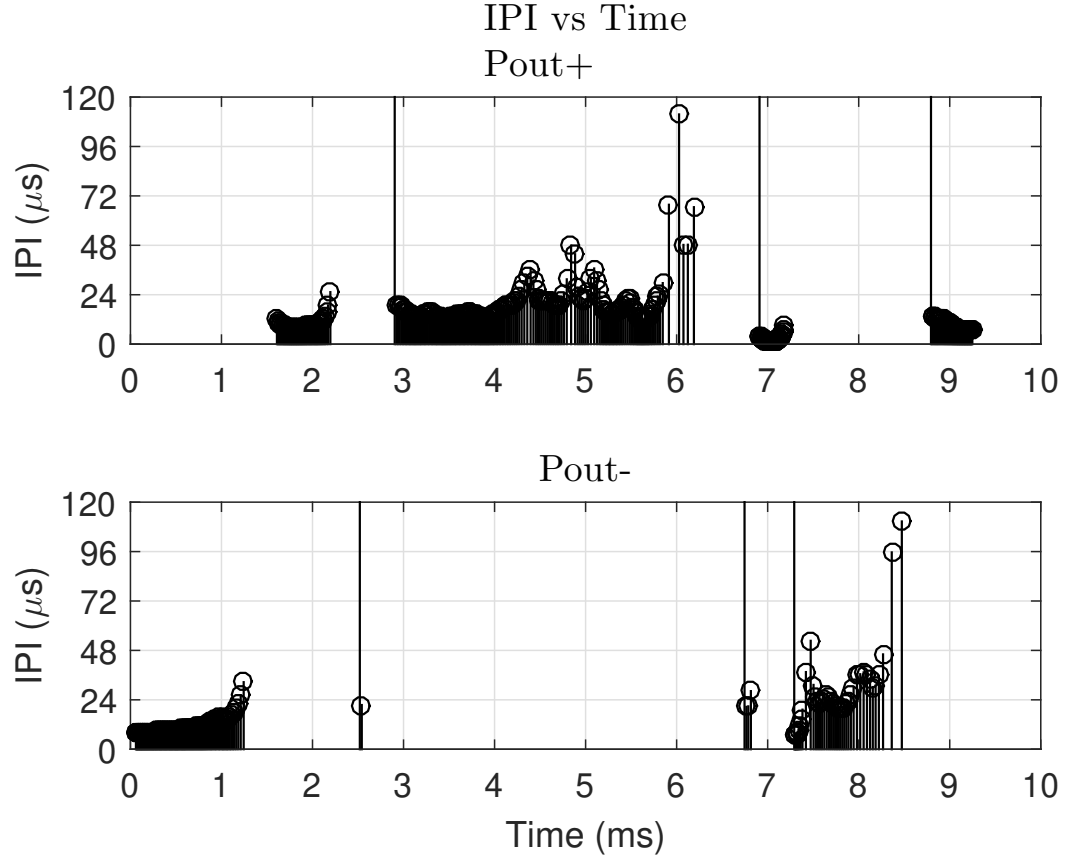

Figure 4.32: Analog IFC version ECG simulation results, IPI from pulse outputs for accelerated ECG input signal (R+C+CC extraction). PhysioNet ECG-ID database ECG [88, 89], with time and amplitude divided by 100. Differential input with adjusted CM, $V_{iCM} = 400$ mV .

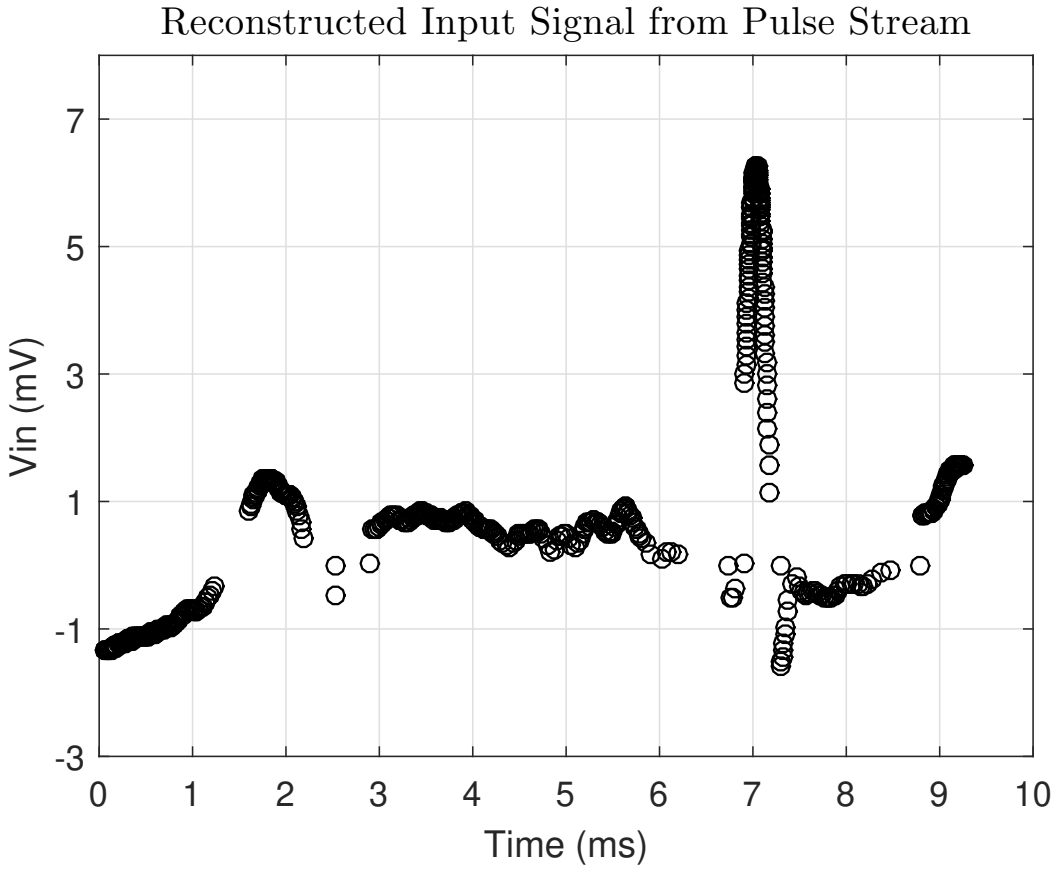

Figure 4.33: Analog IFC version ECG simulation results, reconstructed input signal from pulse outputs for accelerated ECG input signal (R+C+CC extraction). PhysioNet ECG-ID database ECG [88, 89], with time and amplitude divided by 100. Differential input with adjusted CM, V_{iCM} = 400 mV .

4.2.2 Analog IFC Measurement Results

Figure 4.34 and Figure 4.35 present the measured IPI and respective reconstruction for a sinusoidal input signal with 600 µV peak amplitude and 100 Hz frequency.

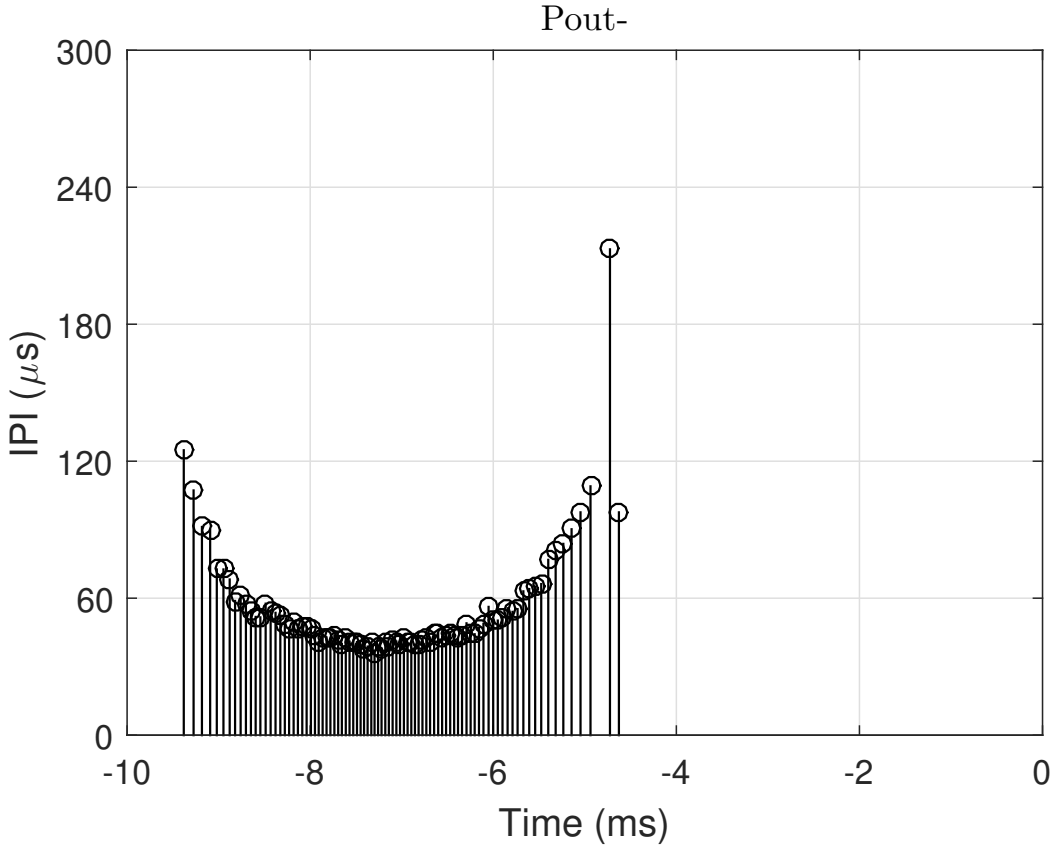

Figure 4.34: Analog IFC prototype measurement, IPI of pulse outputs for input signal with 600 µV peak amplitude and 100 Hz. Only P_{outn} side.

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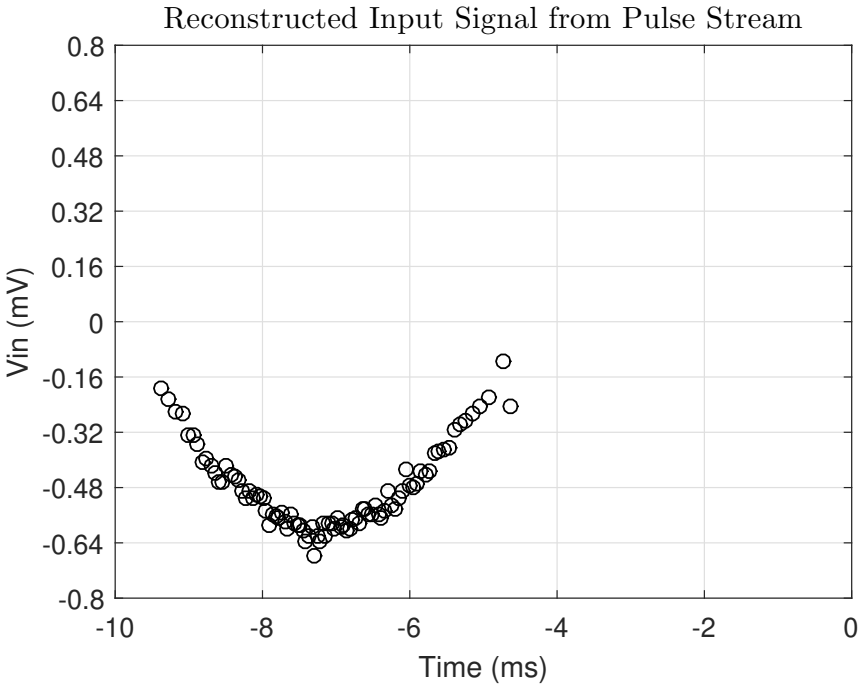

Figure 4.35: Analog IFC version reconstructed signal from pulse output for input signal with 600 µV peak amplitude and 100 Hz. Only P_{outn} side.

The analog IFC circuit has a static and dynamic power dissipation of approximately 53 µW obtained in simulation after R+C+CC layout extraction and in measurement, with a 1µA biasing current for each block: OTA and each comparator. For the complete IFC analog channel, with internal reference voltages and bias currents, the simulated total static power dissipation is approximately 62 µW, the average dynamic power dissipation is also approximately 62 µW, with a 1 µA biasing current in the OTA and in each comparator.

A different mode of operation was found for the analog IFC circuit, during measurement. This is achieved by momentaneously unbalancing the amplifier output with the added probe capacitance. In this mode, the pulse output P_{outn} always presents pulses and P_{outp} stays at ground. In this mode, although the analog IFC consumes more power (175 µW to 228 µW, depending on the tested chip) it is more linear than in the normal operation. As there are always pulses in P_{outn}. In this mode the input frequency range is 10 Hz to 4 kHz and the peak amplitude is 300 µV to 1600 µV. Figures 4.36,4.37, 4.38, 4.39, and 4.40 present the measurement results for this operation mode.

Figure 4.36 presents the analog IFC prototype measured IPIs for an input signal with 600 µV peak amplitude and frequency of 500 Hz in this mode. The input CM

is V_{iCM} = 400 mV and the amplifier output CM is V_{oCM} = 500 mV. The comparators thresholds were set as V_{thn} = 400 mV and V_{thp} = 600 mV. For this input signal and defined thresholds the minimum IPI is 11 µs corresponding to the sine wave positive and negative peaks. The reconstructed signal is presented in Figure 4.37.

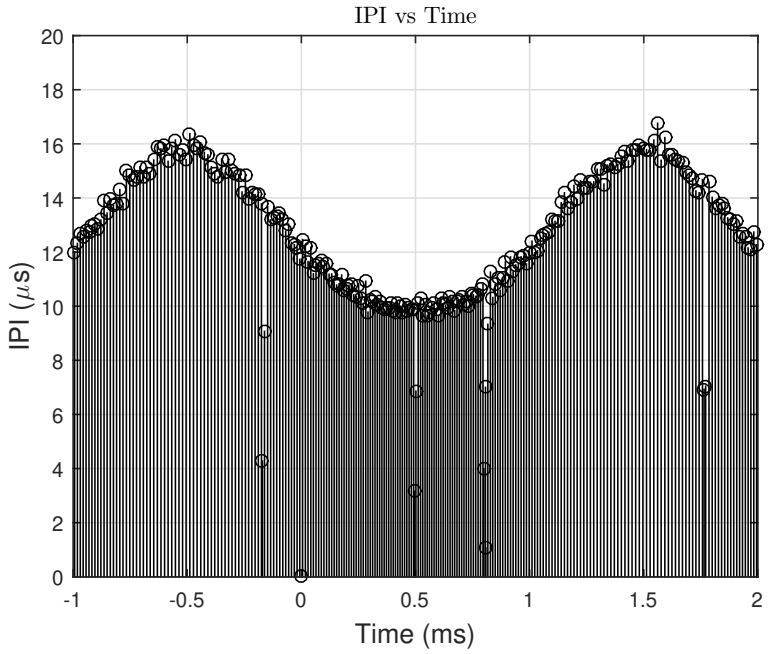

Figure 4.36: Analog IFC prototype measurement, IPI of pulse outputs for input signal with 600 µV peak amplitude and 500 Hz. Always Pulses in P_{outn}

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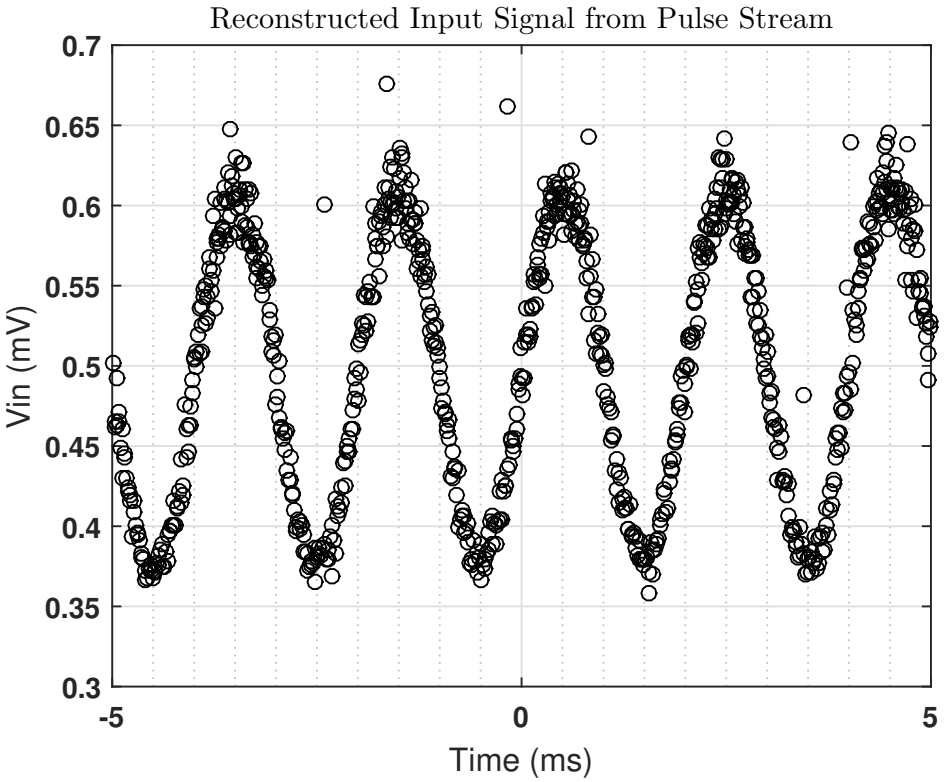


Figure 4.37: Analog IFC version reconstructed signal from pulse output for input signal with 600 µV peak amplitude and 500 Hz. Always Pulses in P_{outn}.

Figures 4.38, 4.39, and 4.40 present the analog IFC prototype measurement results in this mode for input signals with 600 µV peak amplitude and frequencies: 100 Hz, 500 Hz, and 1 kHz, respectively. The first row presents the measured IPIs, the second and third rows present the corresponding reconstructed signals - not subtracting and subtracting the dc component, respectively. The input CM, amplifier output CM, and comparator thresholds are the same as those for analog IFC simulation results, with the exception of the results in Figure 4.40 that have V_{thn} = 460 mV, V_{thp} = 540 mV.

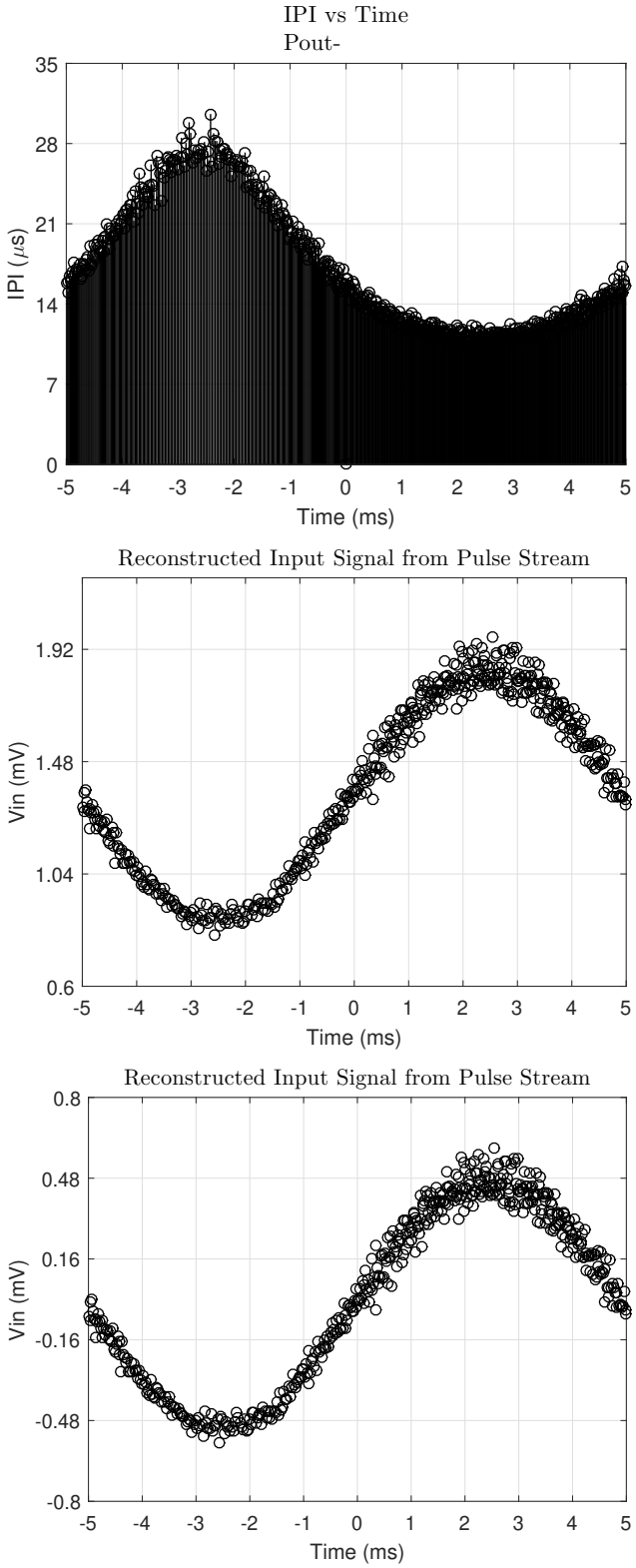


Figure 4.38: Analog IFC measurement results, always Pulses in P_{outn}. The first row presents the IPI and the second and third rows the reconstructed input sine waves from the pulse outputs - not subtracting and subtracting the dc component, respectively, for an input signal with 600 µV peak amplitude and frequency of 100 Hz. With V_{thn} = 400 mV, V_{thp} = 600 mV, and $V_{biasAmp}$ = 566 mV.

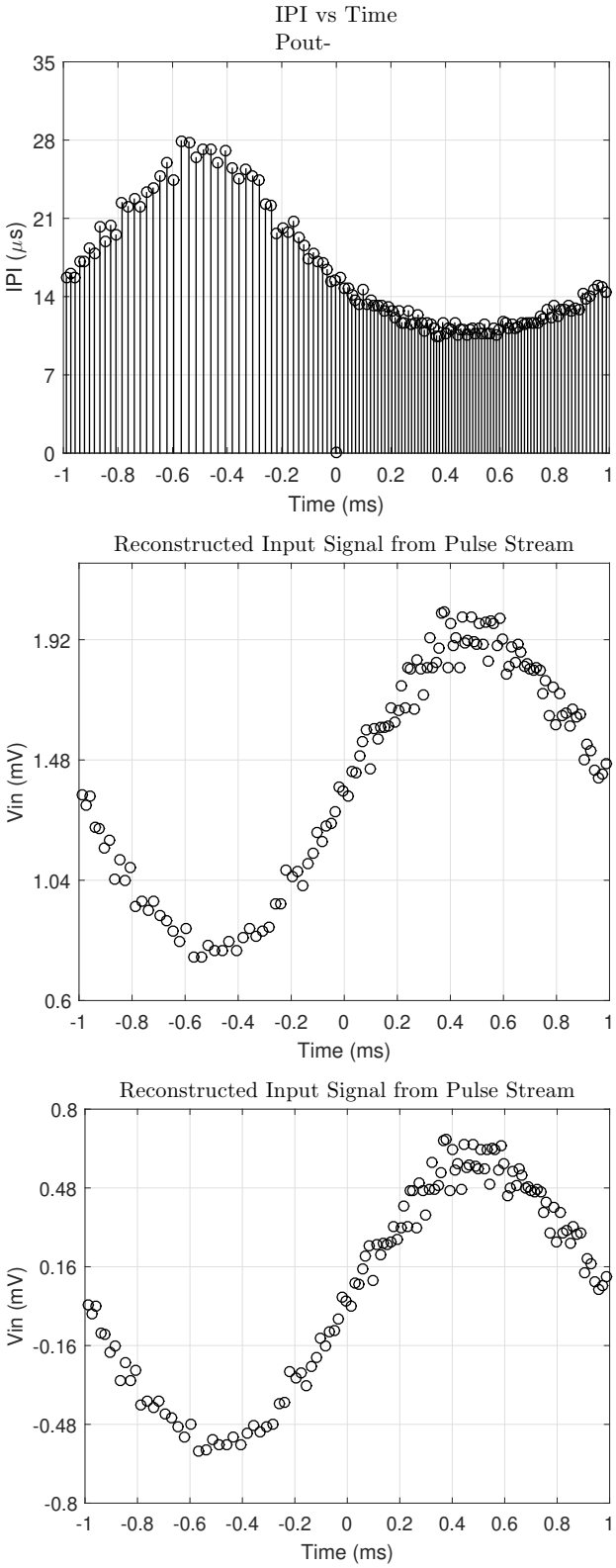


Figure 4.39: Analog IFC measurement results, always Pulses in P_{outn}. The first row presents the IPI and the second and third rows the reconstructed input sine waves from the pulse outputs - not subtracting and subtracting the dc component, respectively, for an input signal with 600 µV peak amplitude and frequency of 500 Hz. With V_{thn} = 400 mV, V_{thp} = 600 mV, and $V_{biasAmp}$ = 485 mV.

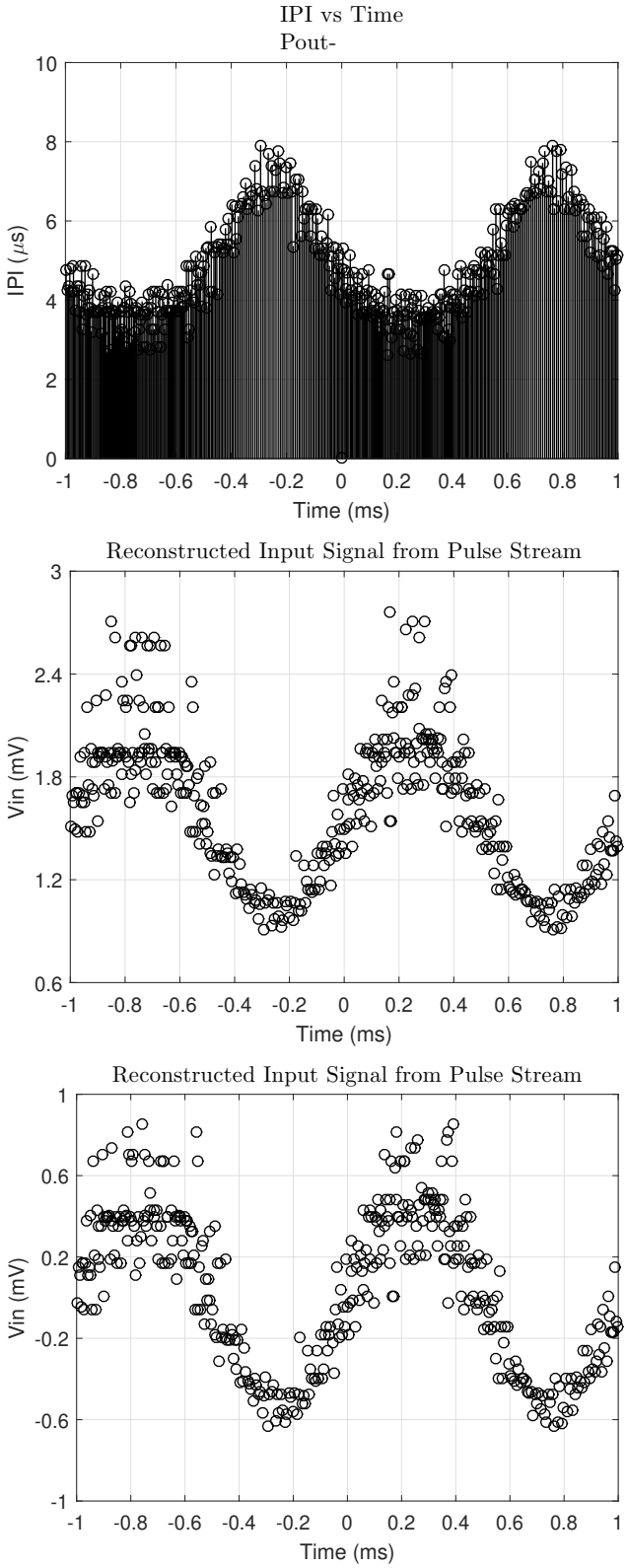


Figure 4.40: Analog IFC measurement results, always Pulses in P_{outn}. The first row presents the IPI and the second and third rows the reconstructed input sine waves from the pulse outputs - not subtracting and subtracting the dc component, respectively, for an input signal with 600 µV peak amplitude and frequency of 1 kHz. With V_{thn} = 460 mV, V_{thp} = 540 mV, and $V_{biasAmp}$ = 566 mV.

Figures 4.41 and 4.42 present the analog IFC prototype reconstructed signal from measurement results in this mode for an input signal with 600 µV peak amplitude and frequency of 500 Hz, for a 10 period time window, not subtracting and subtracting the dc component, respectively. The dc component referred here was obtained from the IFC pulse output measurement in this mode with a dc input signal at V_{iCM} = 400 mV voltage level.

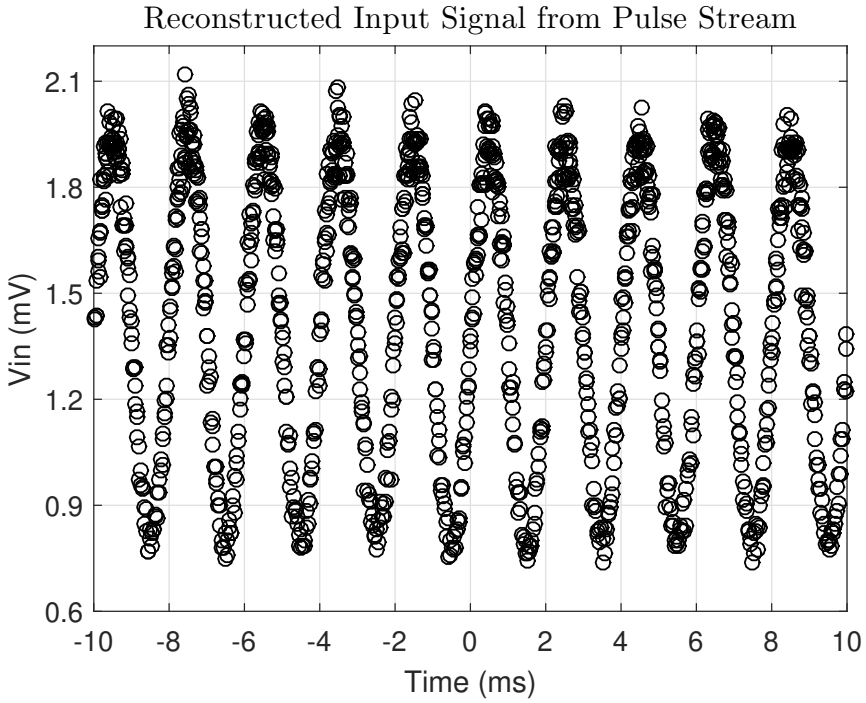


Figure 4.41: Analog IFC version reconstructed signal from pulse output for input signal with 600 µV peak amplitude and 500 Hz (V_{thn} = 400 mV, V_{thp} = 600 mV, and $V_{biasAmp}$ = 484 mV). Always Pulses in P_{outn}.

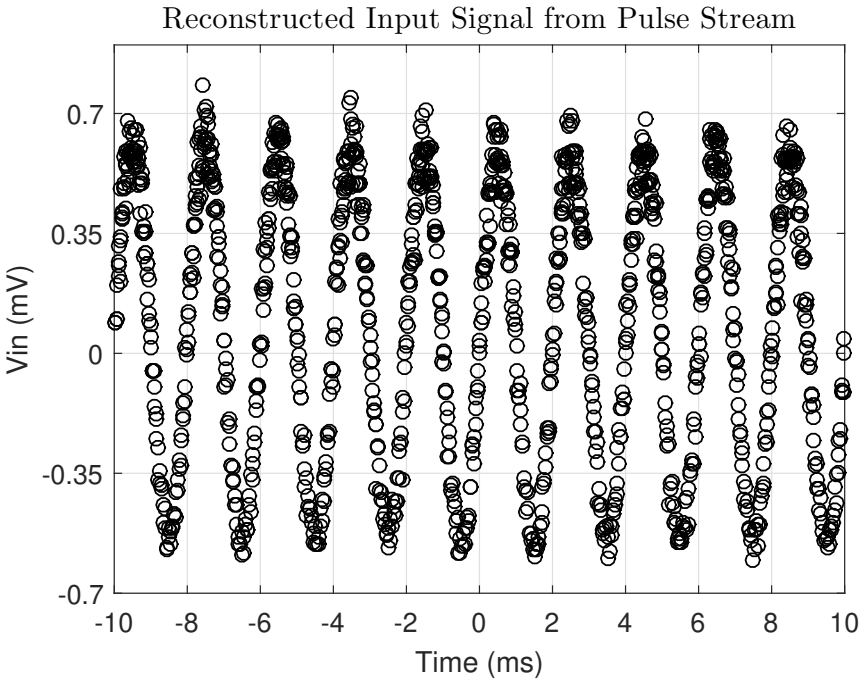


Figure 4.42: Analog IFC version reconstructed signal from pulse output for input signal with 600 µV peak amplitude and 500 Hz (V_{thn} = 400 mV, V_{thp} = 600 mV, and $V_{biasAmp}$ = 484 mV, subtracting the dc component). Always Pulses in P_{outn}.

4.3 SCB IFC

The SCB IFC can convert signals with a peak-to-peak amplitude from 1.6 mV to 28 mV and a frequency range of 2 Hz to 42 kHz The maximum pulse density (average firing-rate) is 3300 kHz and the minimum number of pulses is one.

4.3.1 SCB IFC Simulation Results

Figure 4.43 presents the SCB IFC IC prototype (higher BW version) simulated IPIs (3.2) for an input signal with 11 mV peak amplitude and frequency of 100 Hz (A = 11 mV, f = 100 Hz, input CM voltage $B = V_{iCM}$ = 427 mV, and $/phi$ = 0 rad in equation (3.4) for v_{in} input signal). The amplifier and comparator enable voltages were set to V_{DD} level, $ENAmp = ENComp$ = 900 mV. The input signal CM voltage was chosen to be V_{iCM} = 427 mV as, in simulation for the higher BW IFC version, it is the inverter amplifier mid point, V_{Mid}, with amplifier enable at V_{DD} level. Figure 4.44 presents the corresponding reconstructed input signal from the pulse outputs.

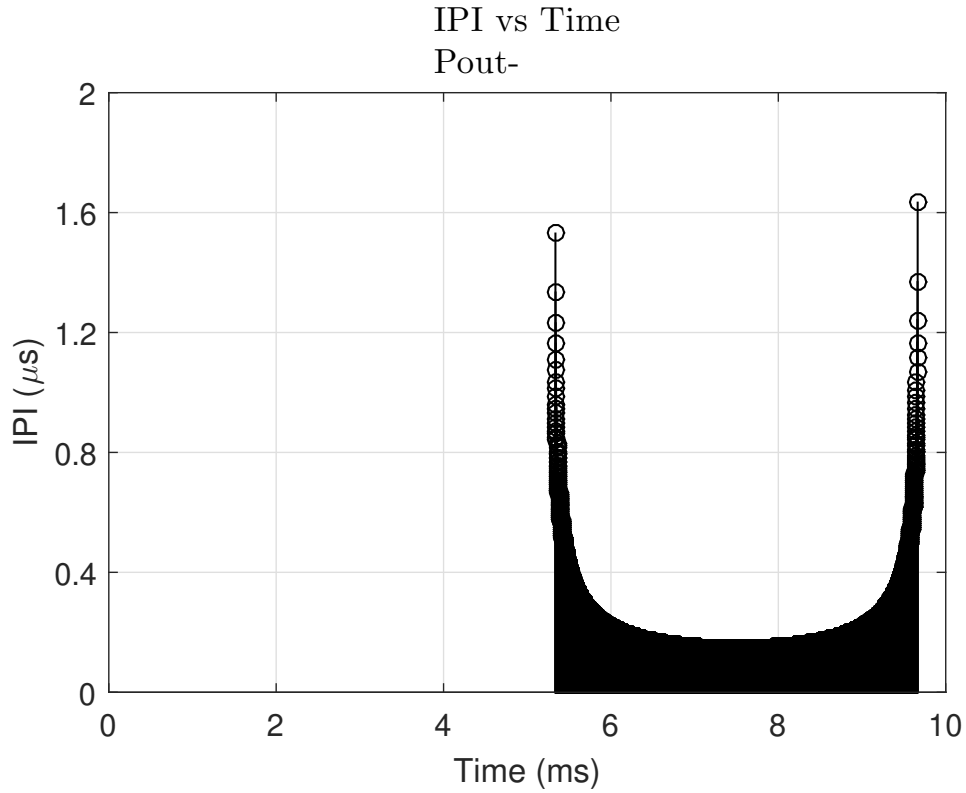


Figure 4.43: SCB IFC version simulation results, IPI graph from pulse output for input signal with 11 mV peak amplitude and 100 Hz. $ENAmp = ENComp$ = 900 mV V_{iCM} = 427 mV. Only P_{outn} side.

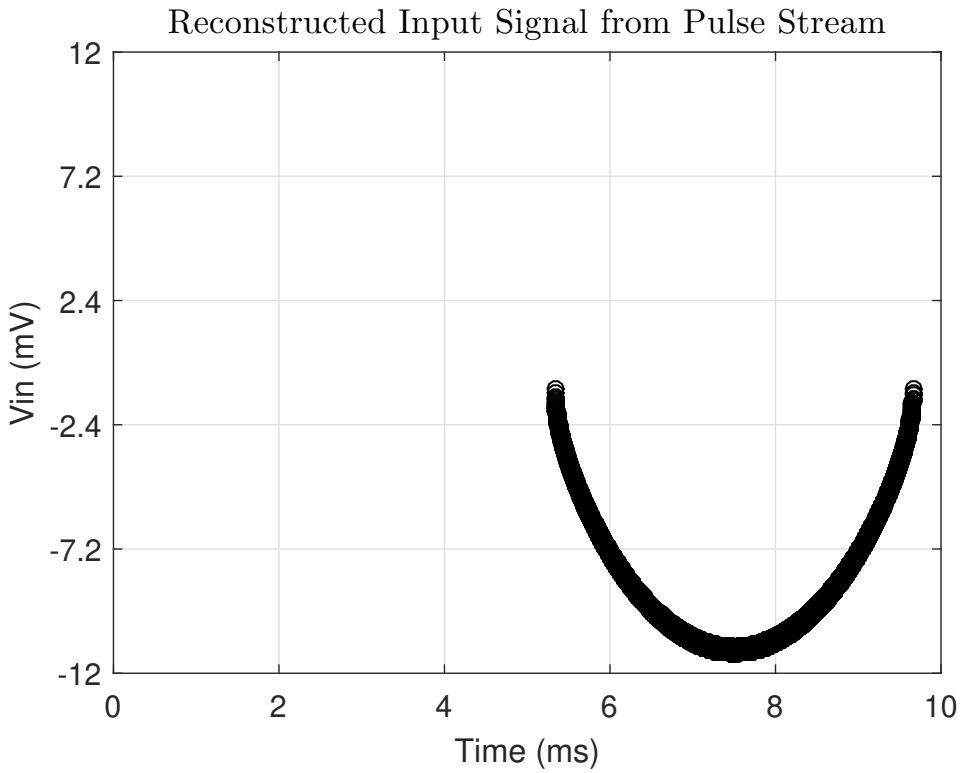


Figure 4.44: SCB IFC version simulation results reconstructed signal from pulse output for input signal with 11 mV peak amplitude and 100 Hz. $ENAmp = ENComp = 900$ mV, $V_{iCM} = 427$ mV. Only P_{outn} side.

4.3.2 SCB IFC Measurement Results

Figure 4.45 presents the measured inverter-based amplifier differential magnitude response for a −47 dBV ≅ 4.5 mV_{RMS} ≅ 6.3 mV_p input signal, with 27 dB gain and approximately 8 kHz bandwidth (BW). The measured gain is in accordance with the theoretical gain calculated with equation (3.32), considering the operating point simulation results. Figure 4.46 presents the measured inverter-based amplifier differential FFT for an input of −60 dBV = 1 mV_{RMS} ≅ 1.4 mV_p at 100 Hz. The spurious free distortion ratio (SFDR) is 53 dB.

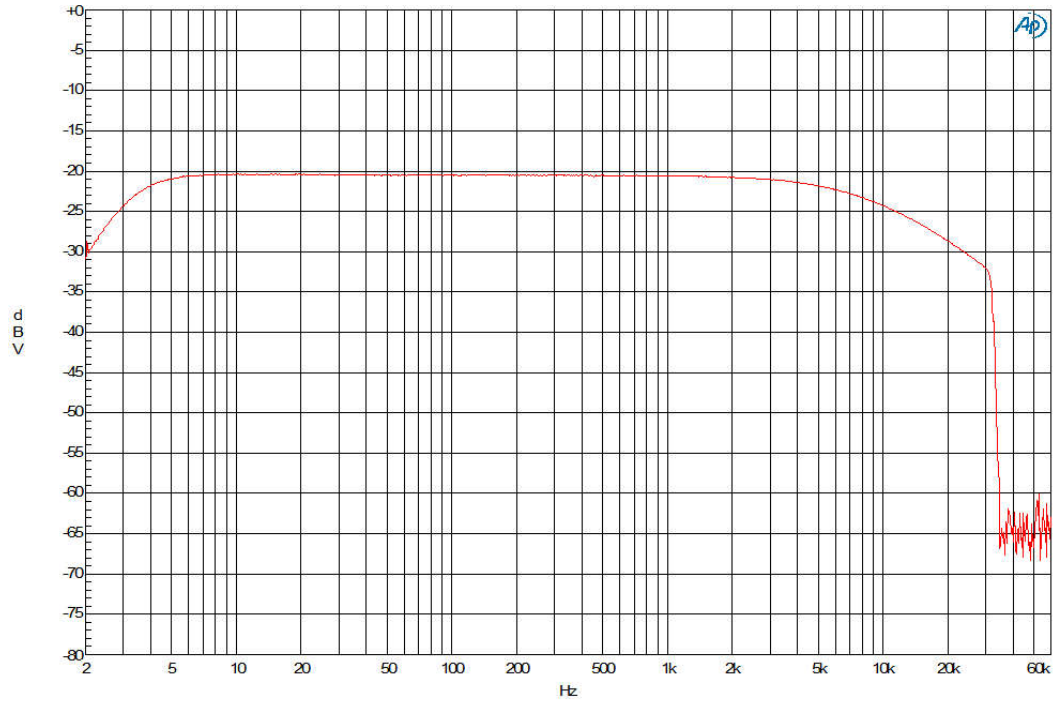
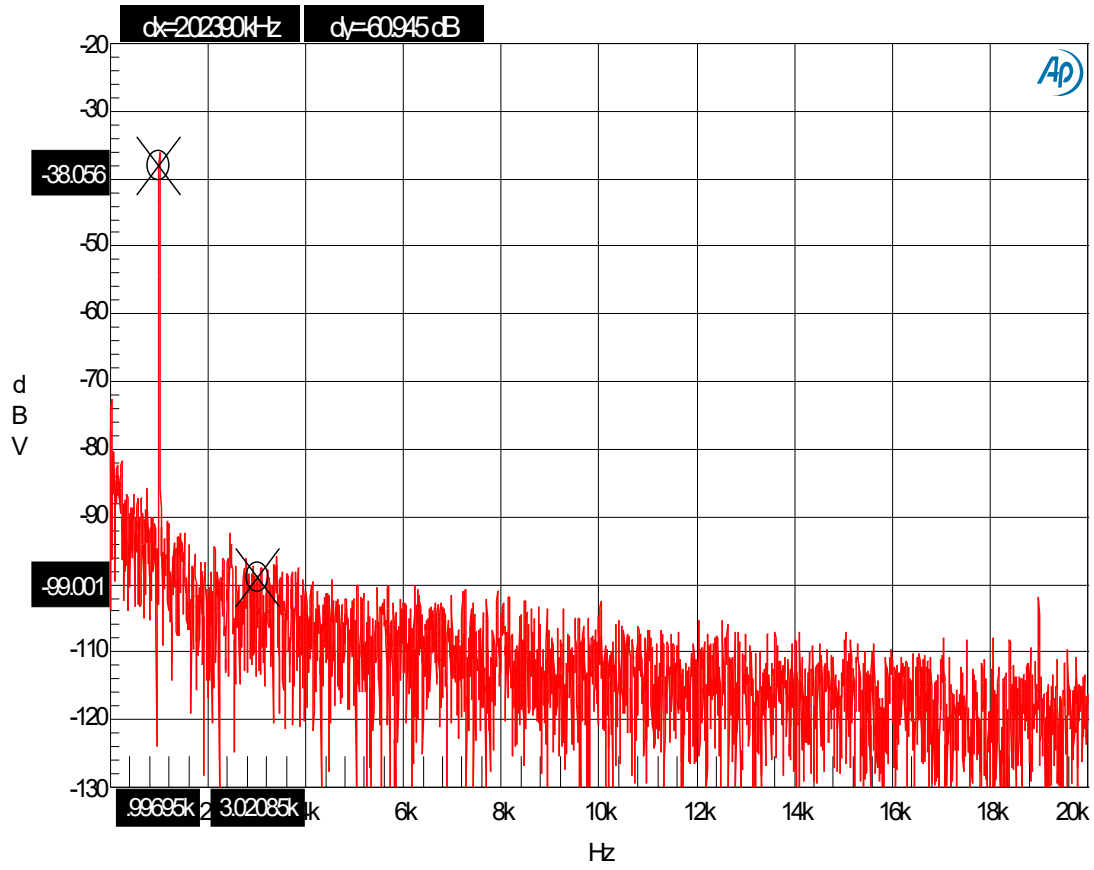


Figure 4.45: Inverter-based amplifier differential magnitude response for −47 dBV ≅ 6.3 mV_p input signal.



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1
5	1	Red	Solid	1	FFT.ChA.Amplitude	Left		*-38.056 dBV

Figure 4.46: Inverter-based amplifier FFT, measured with an input signal of −60 dBV ≅ 1.4 mV_p at 1 kHz.

Figures 4.47,4.48,4.49, and 4.50 present the SCB IFC prototype measured pulse output and respective IPIs for an input signal with 14 mV peak amplitude and frequency of 1 kHz ($A = 14$ mV, $f = 1$ kHz, $B = 478$ mV, and $/phi = 0$ rad in equation (3.4) for v_{in} input signal).

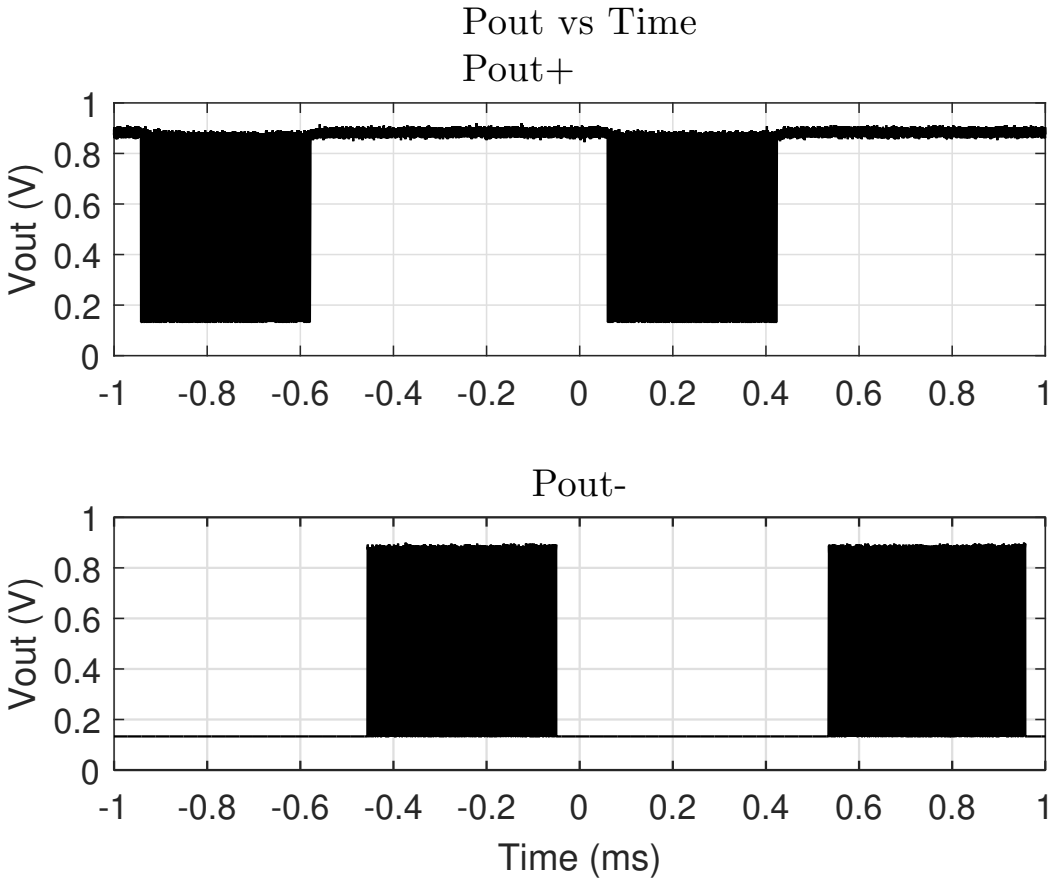


Figure 4.47: SCB IFC version measured pulse output signals (one period) for input signal with 14 mV peak amplitude and 1 kHz. $ENAmp$ = 465 mV, V_{iCM} = 478 mV.

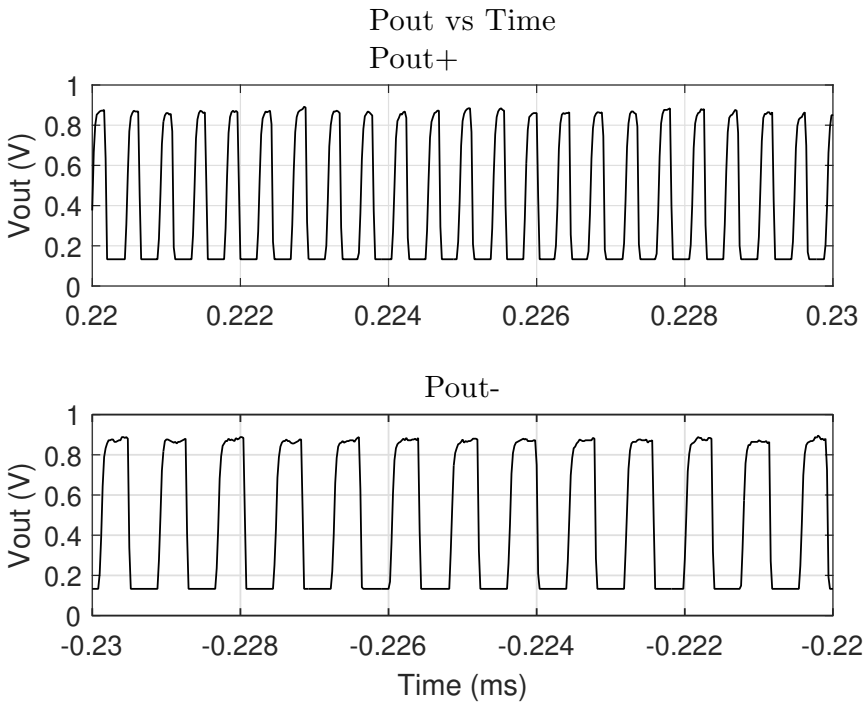


Figure 4.48: SCB IFC version measured pulse output signals zoom for input signal with 14 mV peak amplitude and 1 kHz. $ENAmp$ = 465 mV, V_{iCM} = 478 mV.

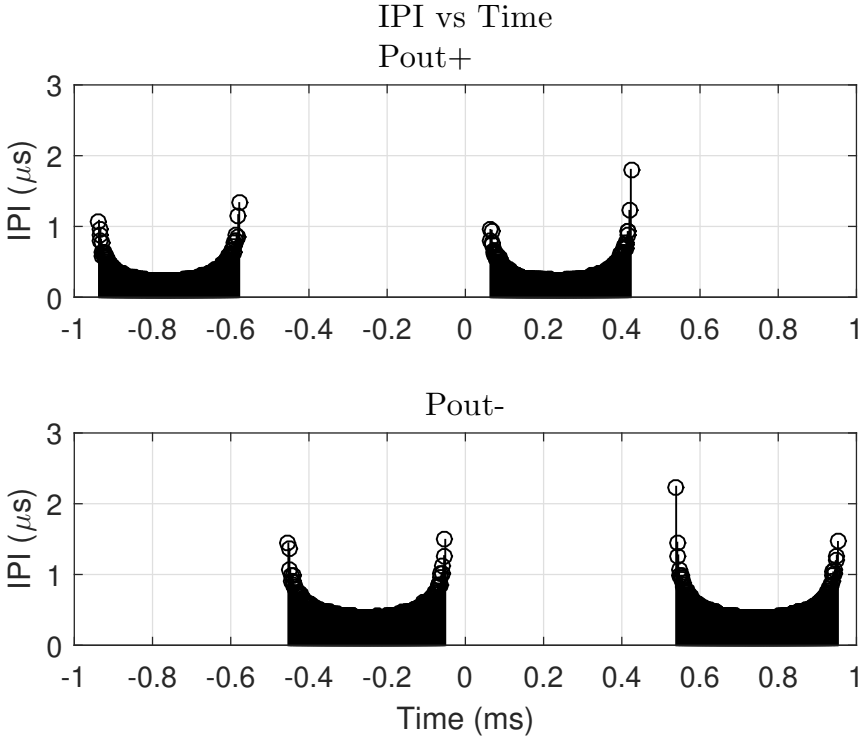


Figure 4.49: SCB IFC version IPI graph for measured pulse output signals (one period) for input signal with 14 mV peak amplitude and 1 kHz. $ENAmp$ = 465 mV, V_{iCM} = 478 mV.

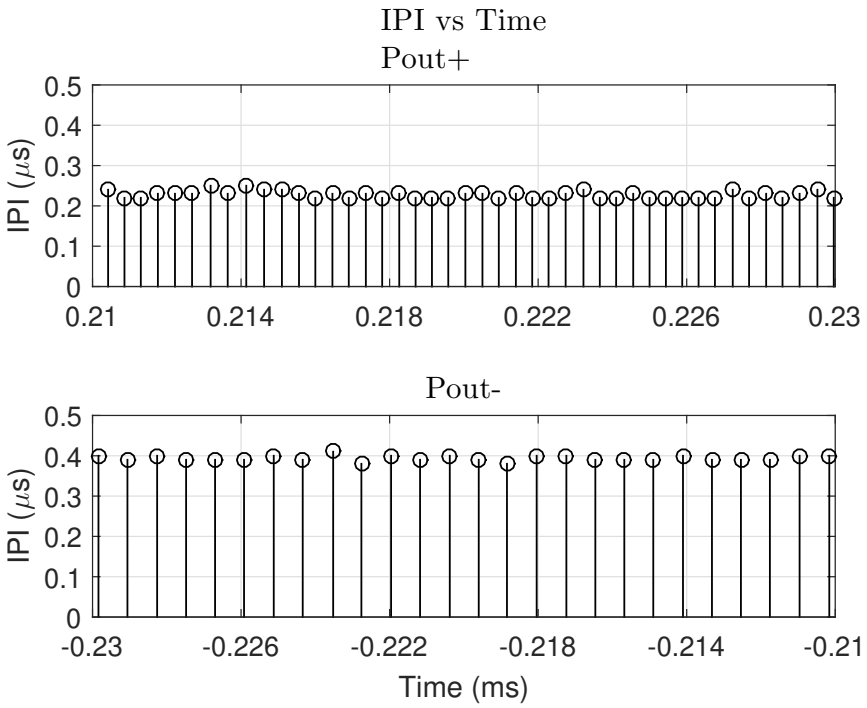


Figure 4.50: Zoom of the SCB IFC version IPI graph for measured pulse output signal (one period) for input signal with 14 mV peak amplitude and 1 kHz. $ENAmp$ = 465 mV, V_{iCM} = 478 mV.

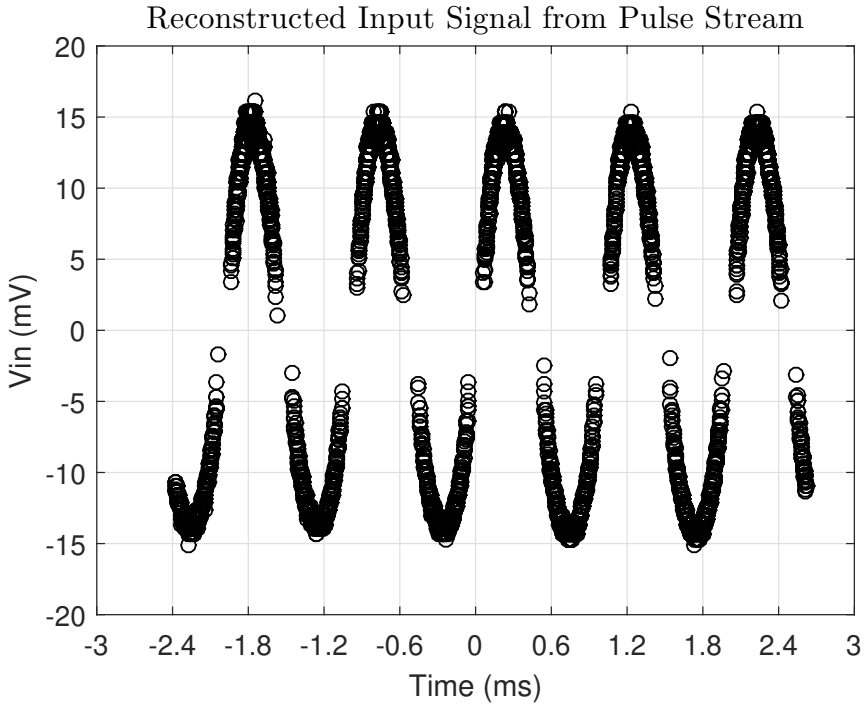


Figure 4.51: SCB IFC version reconstructed signal from pulse output for input signal with 14 mV peak amplitude and 1 kHz. $ENAmp$ = 465 mV, V_{iCM} = 478 mV.

Figure 4.51 presents the corresponding reconstructed signal. In the SCB IFC, the measurements were made with amplifier enable voltage and comparator enable voltage at V_{DD} level, as well with enable voltage close to V_{Mid} of each block to test linearity. This measurement was obtained with amplifier enable voltage $ENAmp$ = 465 mV, instead of V_{DD} level, and comparator enable voltage at V_{DD} level, $ENComp$ = 900 mV, and input CM V_{iCM} = 478 mV instead of V_{iCM} = 435 mV (that is the amplifier inverter mid point V_{Mid} for this measured chip - SCB IFC higher BW version, when $ENAmp$ = 900 mV), because this provides better linearity. Due to the open loop configuration and inverter-based amplifier, the circuit is more sensitive to V_{iCM} and supply voltages when compared to closed loop implementations. The amplifier has maximum gain when $V_{iCM} = V_{Mid}$ and process, voltage, and temperature (PVT) simulation results with R+C+CC extraction show a V_{Mid} range of 425 mV to 435 mV, from fast fast to slow slow corners, respectively. Without a closed loop feedback to relate V_{iCM} with the amplifier output, the V_{iCM} has to be adjusted manually to have the optimal amplifier gain. Although the third harmonic for the inverter-based amplifier is more than 61 dB below the fundamental frequency, with −60 dBV = 1.4 mV_p input signal, Figure 4.46, the SCB IFC presents some crossover distortion. Due to the choice of minimalist inverter-based amplifier and open-loop configuration. And as the SCB IFC input has to be larger than 7 mV to trigger the latch comparator, to generate output pulses due to integration reset. The feedback described previously would also reduce the crossover distortion. To further increase linearity, a Gm amplifier could be used instead of the inverter amplifier, as in [45, 90]. However, the proposed architecture, based on a minimalist inverter-based amplifier (class B amplifier) and open-loop configuration achieves the required linearity while being fully synthesizable. The SCB IFC has a static and dynamic power dissipation of approximately 59 µW, from prototype measurements.

As it can be seen in Figures 4.48 and 4.50, the SCB IFC minimum IPI is different for each pulse output side for a sinusoidal input. For a well balanced differential IFC system the minimum IPI should be the same for both pulse outputs and so for both differential inputs. This unbalance is due to the miss match between the inverter amplifier input stages and the sensitivity this kind of amplifier has to input CM and transistor miss match. An improved inverter amplifier could be used or a different OTA to mitigate this nonlinearity. But to design a fully synthesizable SCB IFC the amplifier has to be made of normal standard-cells. To achieve a fully synthesizable digital system with

standard-cells, only with the addition of two on-chip integrating capacitors, the linearity and versatility, for example in threshold definition, have to be compromised. For the application of monitoring biological signals or even low frequency signals this drawback is not significant and it is fully compensated by the fact that these systems present low power dissipation and low output rates. Only generating an output when there is a significant change in the input. They are not suited for high definition analog to digital conversion, as expected. The typical bit rate conversion in this type of converters is 6 to 10 bits [45], or in some cases 4 to 5 bits [91] for ECG signals, if only simple reconstruction with triangle interpolation is done. [91] presents a simulation of Manu's IFC [27], Figure 2.9, scaled down to a 22 nm CMOS technology node.

The maximum firing-rate as a function of input signal frequency and amplitude is presented for the SCB IFC in Fig. 4.52 and Fig. 4.53. At high input amplitude and frequency the SCB IFC saturates and presents a nonlinearity that makes the firing-rate drop substantially. Note that the input peak amplitude is already above 14 mV that is considered the linear input range.

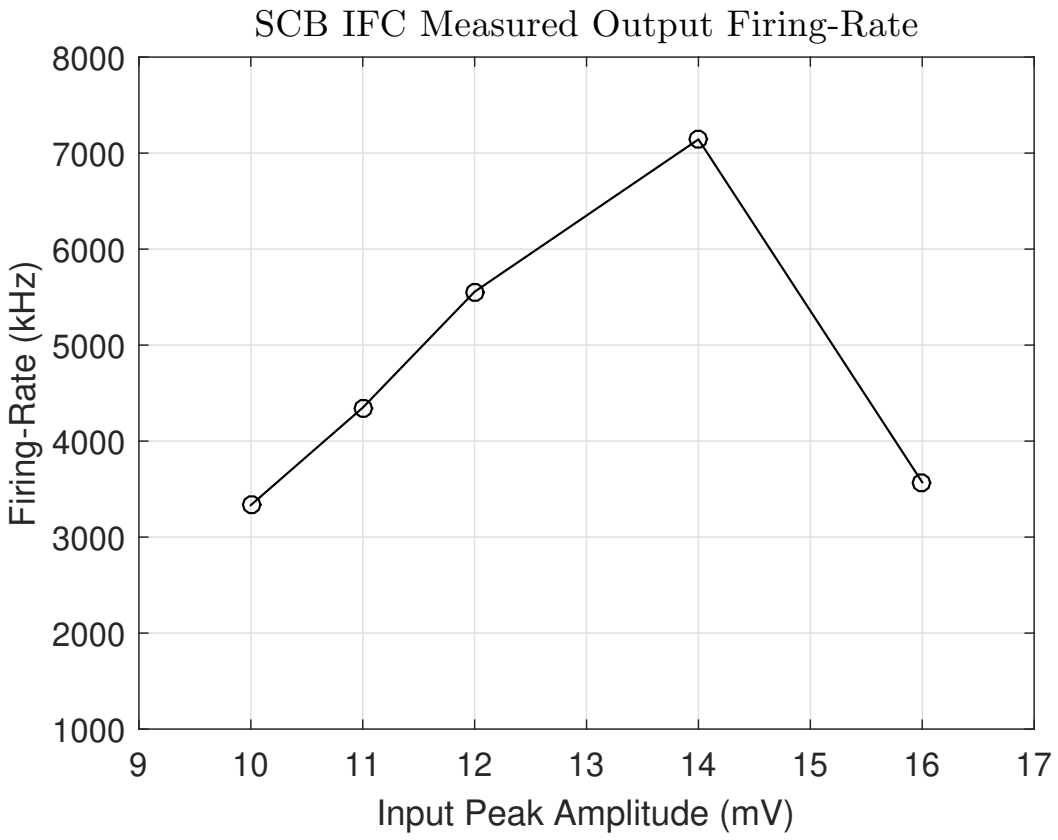


Figure 4.52: SCB IFC prototype firing-rate measurement for an input signal frequency of 100 Hz.

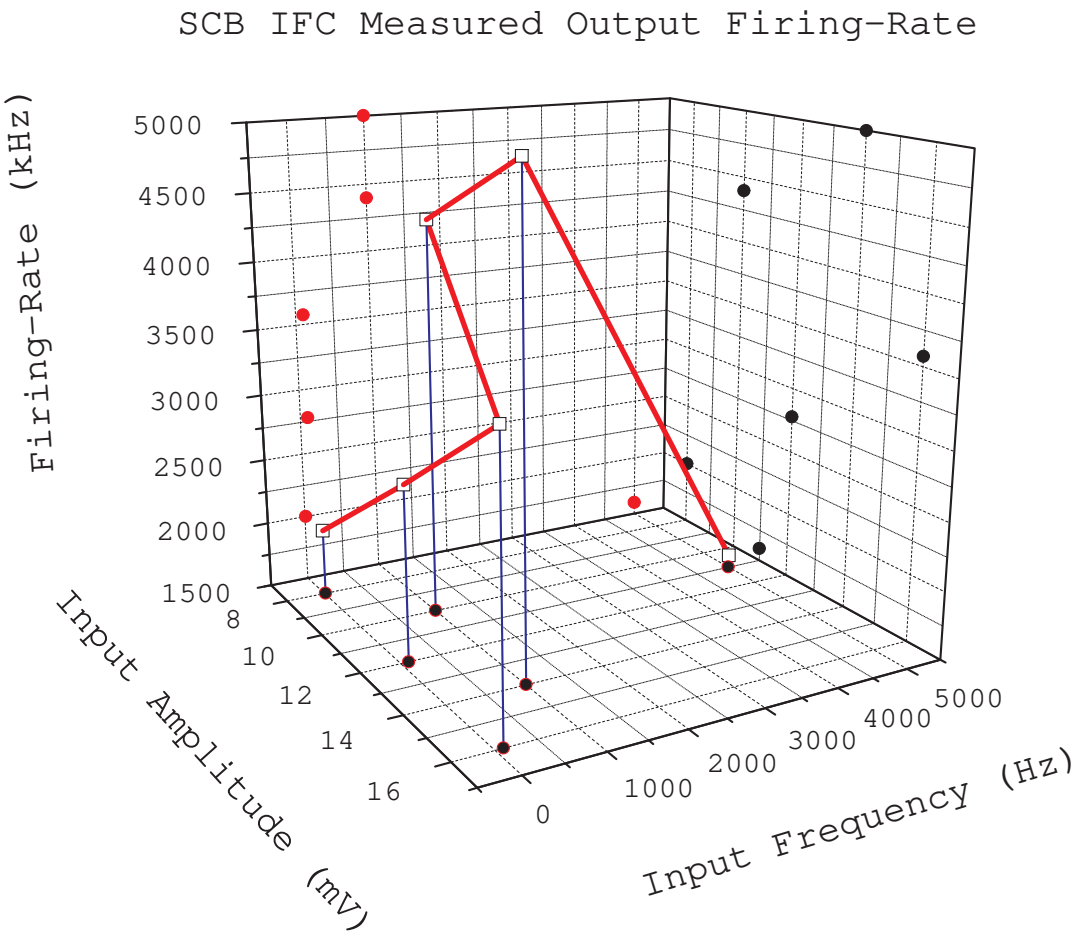


Figure 4.53: SCB IFC prototype output firing-rate measurement, varying the input signal peak amplitude and frequency.

4.4 Conversion Plus Reconstruction Error

The conversion plus reconstruction error (conversion and reconstruction errors together) was calculated with the normalized mean absolute error (NMAE) and normalized root mean square error (NRMSE), considering a similar definition to the one in work [92]:

$$\text{NMAE} = \frac{\|V_i - V_{iR}\|_1 / N}{max(V_{iR}) - min(V_{iR})} \times 100\% \tag{4.3}$$

$$\text{NRMSE} = \frac{\|V_i - V_{iR}\|_2}{\|V_{iR} - < V_{iR} >\|_2} \times 100\% \tag{4.4}$$

where V_i is the IFC input signal magnitude vector, meaning a vector with the input signal magnitudes at the the time the second and consequent output pulses were generated,

t_{k+1} in IPI(t_{k+1}), V_{iR} the reconstructed input signal magnitude vector with reconstructed input signal magnitude at the same time t_{k+1}, for each row, and N the number of points in V_i. The errors are presented in Table 4.4. The sine wave NRMSE is approximately 31 and 3 times smaller than the one presented for a quadratic chirp in [93] (4.4 %), for the SCB and analog IFC, respectively. The NRMSE for analog IFC reconstructed ECG is approximately 5 times smaller than the one in [93] (26.1 %), but at the cost of approximately 11 and 4 times more power dissipation for the ECG and quadratic chirp conversion, respectively. On the other hand, our reconstruction is much simpler, as we do not use polynomial interpolation, as in [93], which increases reconstruction complexity and power dissipation in the reconstruction phase. Fig. 4.54 presents the NMAE and NRMSE for the analog IFC *versus* input signal frequency. It represents the conversion plus recontruction errors for the IFC curve in Fig. 4.30. The SCB IFC with measured pulse outputs for 11 mA input signal peak amplitude and 5 kHz frequency (the lower point in Fig. 4.53 that is in the nonlinear conversion region) has conversion plus recontruction NMAE and NRMSE of 3.1 % and 0.88 %, respectively. Table 4.5 compares the proposed IFCs NMAE and NRMSE with the continuous time (CT) asynchronous sparse input signal state of the art (SoA) for different applications, platforms, and biological signals. The proposed IFCs have NMAE and NRMSE conversion plus reconstruction errors in line, or lower than the other works presented here.

Table 4.4: Conversion Plus Reconstruction Errors

Signal & IFC	Sine in SCB	Sine in Analog	ECG in Analog
Type	Measured 14 mVp 1 kHz	Simulation 0.6 mVp 100 Hz	Simulation Acc. 100×
Fig.	4.51	4.21 (bottom)	4.33
NMAE (%)	2.64	0.31	1.21
NRMSE (%)	0.14	1.19	5.18

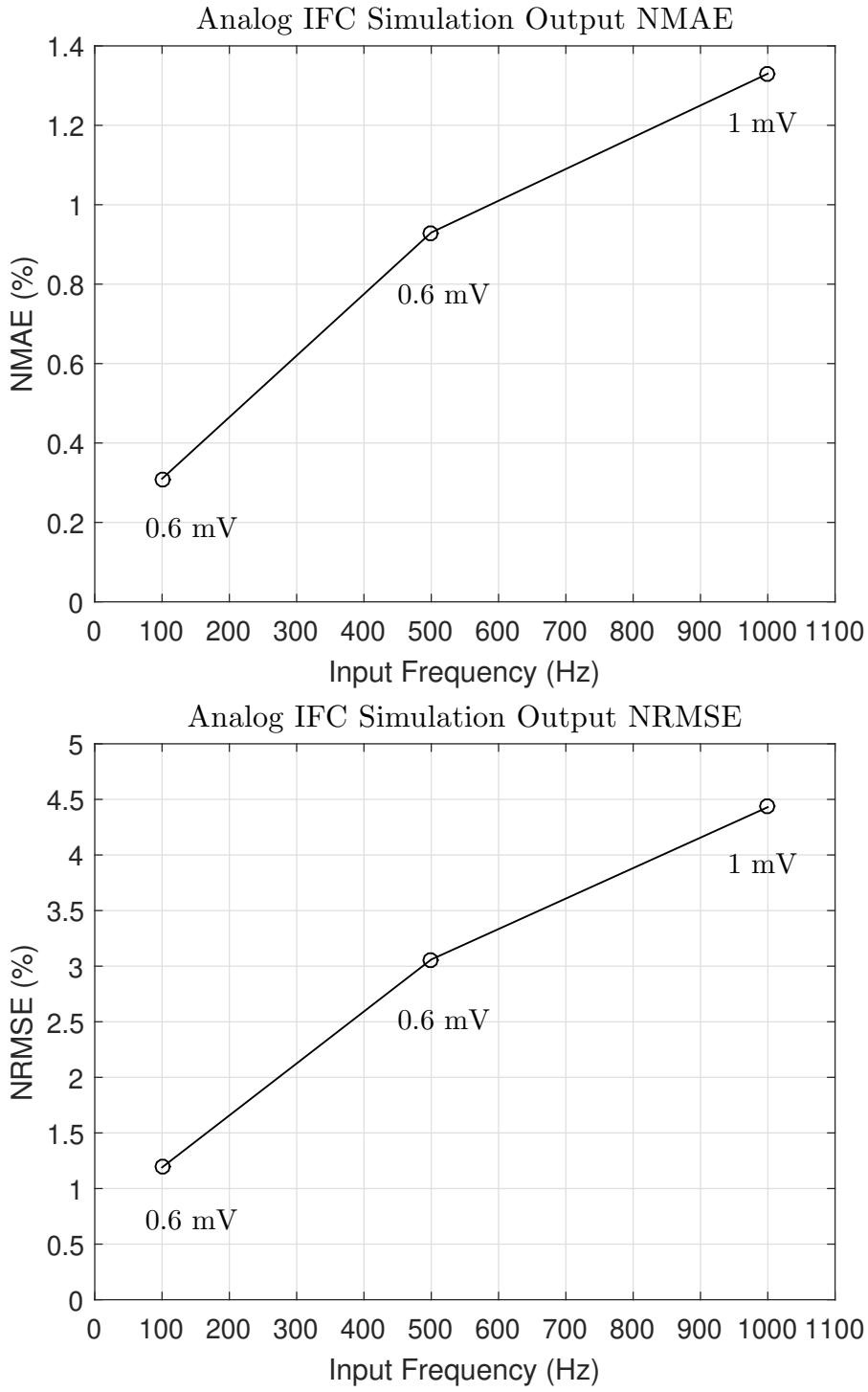


Figure 4.54: Analog IFC Simulation output conversion plus reconstruction errors versus input signal frequency: NMAE (top) and NRMSE (bottom), input peak amplitude in the data points label.

Table 4.5: Conversion Plus Reconstruction Error Comparison

Work	ISCAS JLPEA [94, 95]	JSSC [96]	**This Work Analog [3]**	**This Work SCB [2, 3]**
Application	Extrema Det.	LC-ADC	IFC	IFC
Platform	FPAA	ASIC	ASIC	ASIC
Tech. (nm)	350	40	130	130
Signal	ECG, Chirp	ENG	ECG, Sine	Sine
Input BW (Hz)	60, 1000	10000	10 - 4000	2 - 42000
Power (μW)	4.3, 12.3	50	53	59
NRMSE (%)	26.1, 4.4	4	5.18, 1.19	0.14

Table Acronyms: level-crossing (LC), field-programable analog array (FPAA), application-specific IC (ASIC), electroneurogram (ENG)

4.5 Analog *versus* SCB IFC

The comparison between the proposed analog IFC and SCB IFCs is presented in Table 4.6. They have similar power dissipation and area. Although the SCB IFC area could be further reduced with layout optimization, that was not done due to time restrictions during prototype tape out. The area could be reduced to approximately 0.018 mm^2, at least (112 μm by 163 μm, $142 + 14 + 7$ μm), just passing the flip-flops to the bottom, underneath the capacitor. For an 130 nm technology the power dissipation of a SCB IFC circuit is almost the same as for a conventional analog IFC circuit. Although the energy *per* pulse is approximately 60 times smaller for the SCB IFC circuit, because it has approximately 100 times higher firing rate. Considering the power dissipation and firing rate for each prototype and using equation (2.6), the energy *per* pulse is 1060 pJ and 18 pJ for analog and SCB IFC circuits, respectively. Scaling down the technology this relation may not be the same. Considering the pulse width, that is approximately 2.65 ns for both prototypes and using equation (2.8), the energy *per* single pulse is 140 fJ and 156 fJ for analog and SCB IFC circuits, respectively.

The input BW and amplitude is quite different for the two prototypes. This difference is due to topology (pulse timing, pulse delay t_d, integration type, resistor capacitor (RC) integration *versus* load capacitor current integration), amplifier gain and comparator thresholds. In fact it was seen that integration and firing was much faster in the SCB IFC, giving a much smaller minimum IPI for the SCB prototype than the analog IFC prototype. The SCB IFC presents minimum IPI values of approximately 0.2 μs *versus* 10 μs for the analog IFC for 1 kHz input signal, this is also due to the fact that the input signal amplitude is much larger for the SCB IFC to have pulses. This is also due to the fact that there was much work in slowing down the analog IFC with RC and transistor sizing, OTA and comparator. This was not possible in the SCB IFC as there is no RC and the transistor dimensions were chosen such that the synthesis of the SCB circuit would be possible with custom size cells. Meaning, that the blocks have transistor dimensions not too different from the technology standard-cells. The firing thresholds are defined externally for the analog IFC and are inherent for the NAND gate latch in the SCB IFC. During measurement it was noticed that the SCB IFC is more robust and insensitive to parasitics than the analog IFC. Although for the SCB IFC the input CM has to be finely adjusted to the amplifier inverters mid point, while the analog IFC accepts a larger

range of input CM, from approximately 0.35 V to 0.5 V. The SCB IFC circuit has a simpler design with less optimization than the analog IFC circuit. The SCB IFC circuit has an higher dynamic range than the analog IFC circuit. The analog IFC circuit is more versatile than the SCB IFC circuit, as it is possible to change the firing thresholds and so the number of output pulses, which reflects in the reconstruction accuracy, or feature extraction capability, when doing pulse processing.

Table 4.6: Analog and SCB IFC Versions Comparison

IFC Version	Analog [3]	SCB [2, 3]
Supply (V)	0.9	0.9
Area (mm^2)	0.027	0.021 $_{(a)}$
Total Power (µW)	53	59
Energy *per* Pulse (pJ)	1060	18
Average Firing Rate (kHz)	20-50	3.3 $\times 10^3$
Input BW	10 Hz - 4 kHz	2 Hz - 42 kHz
Input Amplitude V_p (mV)	0.3 - 1.2	0.8 - 16
Input CM (mV)	400	435
Input Impedance Type	R	C
Minimum IPI (µs) (1 kHz input)	10	0.2
Fire Thresholds (mV)	500 +/− 100 $_{(b)}$	415 +/− 200 $_{(c)}$
IFC minimum ΔV_{th} (mV)	40 $_{(d)}$	-
Minimum comparator input difference (mV)	18 $_{(e)}$	22 $_{(f)}$

(a) Area could be reduced to approximately 0.018 mm^2, at least (112 µm by 163 µm), as mentioned in Section 4.5. (b) Thresholds defined by user. Typical threshold settings. (c) Simulation measured fixed thresholds (nominal simulation with R+C+CC extraction type), defined by the latch sizing. (d) Prototype measurement. (e) Simulation measured minimum input difference to trigger the comparator with both thresholds set at V_{oCM} = 500 mV (OTA output CM and comparator input CM). (f) Simulation measured minimum input difference to trigger the SCB comparator.

4.6 Proposed IFCs *versus* the State of the Art

Table 4.7 presents the prototype comparison, analog and SCB IFCs with the SoA. Again, as referred previously in Chapter 2, the presented power dissipation, average firing rate,

signal-to-noise-and-distortion ratio (SNDR) are not for the same input signal conditions. The comparison should be done taking in account all these factors and Figure of Merit (FoM), equation (2.5), if available. This way for a fairer comparison the energy *per* pulse consumption was calculated for each prototype. The energy *per* pulse was calculated for the presented average firing-rate, or stated otherwise in table 4.7, considering equation (2.6). The average firing rate approximation of 20 - 50 kHz for the proposed analog IFC was obtained for input signals with frequency and peak amplitude of 100 Hz 600 μV, Figure 4.34, to 1 kHz and 1 mV, Figure 4.23, respectively. The average firing rate approximation of 3300 kHz for the proposed SCB IFC was obtained for an input signal with frequency of 1 kHz and 14 mV peak amplitude, Figure 4.49.

The energy *per* pulse scales significantly with process node, [27, p. 72]. As the protoypes were fabricated in an 130 nm tech node, the presented energies *per* pulse could be further reduced, if prototyped in smaller nodes as 65 nm, 28 nm, and 22 nm, or even with more recent FinFET or Gate All Around technologies. The work [52] in Table 4.6 presents a low energy *per* pulse, but uses an FDSOI process that has 2 V back gate bias to reduce the overall power consumption. This implies the use of one more power supply, or a voltage doubler to generate this voltage on chip. The proposed IFCs only need a simple power supply and a few voltage regulators present in the protoyped PCB. These intermediate voltages could be easily generated on chip. Also, FDSOI technology has not become a main trend in semiconductor industry. The main ones are FinFET and Gate All Around technologies and these do not allow the use of a back gate voltage. So the work [52] may not achieve so low power dissipation when scaled to more recent technologies. Considering the example in [27, p. 72] work, the estimated reduction in energy consumption for the proposed analog and the SCB IFCs with scaling to 12 nm technology node, for example, would probably not be enough to be more energy efficient than the works presented in [64] and [65]. Although, in the case of the SCB IFC, as it is SCB, the energy consumption reduction would probably be higher than in the proposed analog IFC.

Table 4.7: Prototype comparison

Work	[36]	[45]	[52]	[64]	[65]	[41]	[42] [43] [44]	[26]	[24] [25] [27]	**This Work Analog [3]**	**This Work SCB [2, 3]**
Tech. node (nm)	1500	28 (*a*0)	22 (*a*0)	65	28	180	180	600	600	**130**	**130**
Supply (V)	1.75-5.0	0.65	0.8	0.2	0.2-1	1.3-1.8	1.8	5	5	**0.9**	**0.9**
Area (mm^2)	-	3.2 $\times10^{-3}$	-	35 $\times10^{-6}$	13.28 $\times10^{-6}$	0.18 (*a*)	1.8 $\times10^{-2}$	-	-	**2.7 $\times10^{-2}$**	**2.1 $\times10^{-2}$**
SNDR (dB)	-	32-42	-	-	-	-	-	59 (*b*1)	57 (*b*2)	-	-
Input BW	-	10 MHz-50 MHz	-	-	-	3 Hz-2.5 kHz	0.8 Hz-10 kHz	10 kHz	-	**10 Hz-4 kHz**	**2 Hz-42 kHz**
Total Power (μW)	0.3-1.5	24	-	1 $\times10^{-4}$	1.85 $\times10^{-4}$	55	27.3 (*c*)	45	1.2	**53**	**59**
Energy per Pulse (pJ)	3 $\times10^{4}$	-	16 @30 Hz 1 @2.1 kHz	4 $\times10^{-3}$	0.43 $\times10^{-3}$	5.5 $\times10^{5}$	883 @30 Hz	1.4 $\times10^{3}$	10 @ 200 Hz	**1.06 $\times10^{3}$**	**18**
Average Firing Rate (kHz)	0.01	-	0.07	25	430	0.1	-	33	40	**20-50**	**3.3 $\times10^{3}$**
FoM (pJ/ conv-step)	-	3 $\times10^{-3}$-1 $\times10^{-2}$	-	-	-	-	-	2.2 (*d*)	0.6	-	-
Prototyped	No	Yes	No	Yes	No	Yes	Yes	Yes	Yes	**Yes**	**Yes**
Aim	IFC	ADC	IFC	IFC	IFC	IFC (*e*)	IFC	IFC (*e*)	IFC	**IFC**	**IFC**
Fully Differential	No	Yes	No	No	No	No	No	No	No	**Yes**	**No (Pseudo)**
Phases	Mono	Mono	Mono	Mono	Mono	Mono	Mono	Mono	Bi	**Bi**	**Bi**
Spike frequency adaptation	Yes	-	Yes	No	Yes	No	Yes	No	No	**No**	**No**
External Clock	No	Yes	No	No	No	No	No	No	No	**No**	**No**
IFC as AFE Block	No	-	No	No	No	No$_{(f)}$	Yes	No$_{(f)}$	No	**Yes**	**Yes**
All Digital	No	No	No	No	No	No	No	No	No	**No**	**Yes**

Table 4.8: Prototype comparison table footnotes

Work presented in	ISCAS [36]	JSSC [45]	TCASI [52]	Front. Neuro. [64]	TCASI [65]	TBCAS [41]	Nature Com. [42] [43] [44]	PhD Dis. [26]	ISCAS [24] [25] [27]	**TBCAS This Work Analog [3]**	**TBCAS BioCAS This Work SCB [2, 3]**

(*a*0) fully-depleted silicon-on-insulator (FDSOI) (*a*) Total area with low noise amplifier, bandpass filter, delta modulator ADC and pulse ADC, analog trough and peak detector. (*b*) signal-to-noise ratio (SNR) and not SNDR, (b1) from [26, p. 83], (b2) from [24]. (*c*) 27.3 µW average and 0.096 µW static power dissipation. (*d*) FoM was calculated considering [27, p. 69] equation (also presented in [25]), equation (2.5), and in the condition of 2 times BW as there is no sampling frequency for asynchronous IFC (f_{sample}) and data from [26, p. 83], effective number of bits (ENOB) equal to 10 bits. (*e*) IFC integrated in a neural processor. (*f*) Requires a low noise amplifier (LNA) and analog filters.

4.7 Future Improvements

Improvements could be done to the prototypes and to the testing PCB. A field programmable gate array (FPGA) with high speed input, higher than 150 MSa/s, see 4.1.2, could be added to measure and sample the pulse outputs, and even process them locally, if desired. This would avoid the issue of sampling the pulse outputs with an oscilloscope, that can degrade the measurement due to the defined sampling windowing, if the sampling window is set as a large time window relative to the input signal frequency. On the other hand, improvements could be made to IC prototypes, adding adaptation to 50 Ohm in the pulse outputs, or add it to the testing PCB, to measure the pulse outputs in the oscilloscope with 50 Ohm adaptation, minimizing the losses in transmission as the output TFF transitions occur in 7 ns, corresponding to a 143 MHz BW, see 4.1.2. Output drivers should also be increased in the IC prototypes and to test with ECG, or neural signals a dedicated amplifier should be added to the IC prototypes for best performance. Also the input/output pads connected to the intermediate signals from the analog IFC amplifier outputs, v_{op} and v_{on}, should be removed in future prototypes, to not have parasitic capacitance and disturbances in the analog IFC internal nodes, as explained in sections 4.1 and 4.2.2. The input/output pads connected to the intermediate signals from the SCB IFC amplifier outputs could also be removed in future prototypes. These pads were important for debug purposes for both IFC versions, as for example in the SCB IFC they were used to set the V_{iCM} that gives the optimal amplifier gain, as well as for characterizing the inverter based amplifier. But with the laboratory reference from these prototypes, the future analog and SCB IFC prototypes could have optimal performance without internal intermediate signal pads.

5

Conclusions and Future Work

5.1 Conclusions

Two novel differential - the analog version is fully-differential [3] and the standard cell-based (SCB) one [2, 3] is pseudo-differential, voltage mode integrate-and-fire converter (IFC) circuits with 0.9 V supply voltage are proposed. They were prototyped in a 1.2 V 130 nm complementary metal-oxide-semiconductor (CMOS) standard process. The analog IFC circuit occupies an area of 0.027 mm^2 and the SCB version 0.021 mm^2. They are both the first of their kind. The analog IFC is fully-differential and can be used as analog frontend (AFE) in sensor-to-digital interfaces. The SCB IFC is fully digital, dynamic, synthesizable and can also be used as AFE in sensor-to-digital interfaces. They have a total power dissipation of 53 μW and 59 μW, analog and SCB, respectively. And an energy per pulse consumption of 1060 pJ for the analog version and 18 pJ for the SCB, which is one of the lowest energy *per* pulse consumption reported for IFC circuits. The maximum pulse density (average firing rate) for analog version is 50 kHz and SCB version 3300 kHz, the minimum number of pulses can be one, for both.

The SCB IFC circuit has a simpler design with less optimization than the analog IFC circuit. The SCB IFC circuit has higher dynamic range and is more stable and robust than the analog IFC circuit. The analog IFC circuit is more versatile than the SCB IFC circuit, as it is possible to change the firing thresholds. Both circuits present interesting characteristics to be applied in electrocardiogram (ECG) and neural signals, provided that a good AFE is used before the IFC circuit, in the latter case (because of minimum detectable signal constraints). They represent a low power solution with low output data rates, that can be considered for biological implantation, or as an AFE for low frequency signals, as required in internet of things (IoT). Even more, if the power dissipation is

further reduced. Through simulation it was seen that in the analog IFC it is possible to reduce the power dissipation to the 20s μW range, mainly by halving the amplifier and comparator bias currents to 0.5 μA. As the proposed SCB IFC is fully synthesizable, with only the addition of two on-chip integrating capacitors, it can be used in various systems. For example, it can be straightforwardly implemented as an AFE in a field programmable gate array (FPGA), with or without neural processing capability. This is an interesting feature for future all digital synthesizable systems.

5.2 Future Work

Reconstruction from the IFC time encoding machine (TEM) pulse output is not energy efficient and adds a reconstruction error to the system output, as described in section 2.4, thus the future work should focus on time domain feature extraction from the IFC TEM. A classifier algorithm as the ones proposed in [12, 13] for a specific signal type, as ECG, could be implemented in hardware together with the proposed IFC circuits. This could have lower energy consumption than a conventional AFE followed by a digital signal processing (DSP) unit.

The next step would be to implement an algorithm as the one proposed in [18–20] for an automaton creation in hardware. This way the IFC TEM would be capable of characterizing different input signals. It would learn the input signal time structure for a certain type of input signal and create an automaton that retrieves the important features from that input signal type, all in time domain. First the algorithms could be adapted to process the measured IFC pulse stream (also named pulse train) in software with real measured data and then they could be implemented in hardware. This is not a simple task and it could be an interesting topic for a future dissertation. The implementation of this algorithm can be done with one IFC, or with multichannel IFCs, meaning multiple IFCs in parallel to implement a kernel adaptive autoregressive-moving-average (KARMA) network operating on multichannel pulse trains, as shown in Figure 2 of the work presented by Li and Principe [20]. In the case of speech recognition, using multiple IFC in parallel allows to segment the multichannel pulse trains, similar to conventional speech segmentation, and the similarity measure can be summed, or averaged over all channels [20].

Electronic circuits operating in time domain can take advantage of more recent technologies with fin field effect transistors (FinFETs), or gate all around (GAA) metal-oxide-semiconductor field effect Transistors (MOSFETs) due to faster switching devices, and work with low supply voltage due to the lower threshold voltage provided by these technologies, as well as with technology scaling down [7]. Continuous time (CT) operating circuits performance is not severely degraded by transistor missmatch and lower intrinsic transistor gain, that are characteristic of these newer technologies and more advanced nodes [97], as it can be with other circuit implementations. GAA technologies, similarly with fully-depleted silicon-on-insulator (FDSOI) based technologies can achieve lower power dissipation, as in [45, 52] that use FDSOI technology. The work in [52] explores the possibility of having currents in the range of pico-Amperes to emulate biologically plausible dynamics and circuit behavior, using subthreshold FDSOI based circuits with 2 V reverse back gate bias. [45] also uses the FDSOI backgate bias capability, to lower the transistor threshold, reducing the supply voltage and so the power dissipation. The BrainDrop neuromorphic system presented by Neckar *et. al* in [98] also uses FDSOI technology to have reverse back bias that reduces static power dissipation, operating in deep suthreshold regime. Generally, GAA MOSFETs do not have back gate bias capability. Even though, GAA MOSFETs have a better insulation between channel and substrate than bulk CMOS, reducing the undesired bulk effects, as source and drain leakage and parasitic junction capacitance, substrate noise coupling, and susceptibility to latch-up [52]. The undoped channel, or a channel with much lower dopant concentration than bulk CMOS, also reduces transistor missmatch due to threshold voltage variation [52]. This points the direction for future CT operating circuits and in particular neuromorphic IFC based circuits that will use technology scaling down together with these novel technologies in few nanometers nodes to their advantage.

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