NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTAMENTO DE ENGENHARIA ELETROTÉCNICA E DE COMPUTADORES

TOMÁS ALEXANDRE DE OLIVEIRA VALDEIRA CAETANO

STUDY AND DESIGN OF A LOW-POWER PHASE-LOCKED LOOP FOR ISM APPLICATIONS

MESTRADO EM ENGENHARIA ELETROTÉCNICA E DE COMPUTADORES

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To my family and friends.

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"But still try, for who knows what is possible?"
(Michael Faraday)

Resumo

Esta dissertação tem como foco o desenvolvimento e implementação de uma Malha de Captura de Fase (PLL) Analógica de baixa potência como um Sintetizador de Frequência Inteiro com uma razão de divisão N para aplicações ISM, com especial ênfase na sua aplicação em sistemas de comunicação LoRa e na sua importância em emissores-receptores RF.

O modelo do Sintetizador proposto engloba componentes fundamentais, como um Oscilador LC Controlado por Tensão (VCO), um Detector de Fase e Frequência (PFD) com base em lógica NOR, uma Bomba de Carga com comutação por porta (CP) e um Filtro passa-baixo de Segunda Ordem (LF). O VCO apresenta um nível de ruído de fase de -103.11 dBc/Hz a 1 MHz e atinge um *jitter RMS* de 14.095 ps. Além disso, a CP fornece uma corrente de 125 μA. Nesta configuração, são cruciais dois tipos de Divisores: um Divisor de Frequência, operando com uma topologia TSPC e uma razão de divisão de 128, e um Divisor em Quadratura colocado à saída do PLL.

O estudo realizado centra-se na análise dinâmica e em condições estacionárias para determinar a estabilidade e a largura de banda do Sintetizador. O PLL, desenvolvido com tecnologia CMOS de 130 nm, tem um tempo de bloqueio de 5 μs e uma largura de banda de 0.73 MHz com um consumo de 3.50 mW, assumindo uma alimentação de 0.9 V. Este PLL tem uma gama de frequências de 4.864 GHz a 5 GHz, que se estende a 1.736 GHz até 1.738 GHz com o uso de um banco de condensadores de dois bits.

A inclusão do Divisor em Quadratura permite a cobertura da gama de frequências de 868 MHz a 869 MHz e de 2.432 GHz a 2.5 GHz. Tornando o Sintetizador adequado para ambas as bandas LoRa, tanto a de 2.4 GHz e a de 868 MHz.

Os processos de design e simulação deste trabalho foram realizados com recurso o software Cadence Virtuoso Design Environment, proporcionando precisão e eficácia durante o estudo.

Abstract

This dissertation focuses on developing and implementing a Low-Power Analog Phase-Locked Loop (PLL) as an Integer-N Frequency Synthesiser for ISM applications, with a special emphasis on its application in LoRa communication systems and its importance in RF transceivers.

The Synthesiser model presented encompasses several vital components: an LC-Voltage Controlled Oscillator (VCO), a NOR logic-based Phase-Frequency Detector (PFD), a gate-switched Charge Pump (CP) and a Second-order Loop Filter (LF). The VCO showcases a phase noise level of -103.11 dBc/Hz at 1 MHz and achieves an RMS jitter of 14.095 ps, also the CP provides a current of 125 μA. A key feature of this design is the inclusion of two distinct types of Dividers: the first is a Frequency Divider employing a ratioed TSPC topology with a division ratio of 128, while the second is a Quadrature Divider is placed at the output of the PLL. These Dividers play a crucial role in the overall functionality of the Synthesiser.

The performed study emphasises both dynamic and steady-state analysis, aiming to evaluate the stability and bandwidth of the Synthesiser. The PLL in focus, which is designed using 130 nm CMOS technology, exhibits a lock time of 5 μs and a bandwidth of 0.73 MHz. It operates with a power consumption of 3.50 mW at a supply voltage of 0.9 V. This PLL has a tuning range that spans from 4.864 GHz to 5 GHz, and it broadens its range to include 1.736 GHz to 1.738 GHz with the use of a two-bit capbank.

Including the Quadrature Divider enables frequency coverage from 868 MHz to 869 MHz and 2.432 GHz to 2.5 GHz. This enhancement makes the Synthesiser suitable for both the 2.4 GHz and 868 MHz LoRa bands.

This work's design and simulation processes were conducted using the Cadence Virtuoso Design Environment software, which provided accuracy and effectiveness throughout the study.

Keywords: LoRa, Frequency Synthesiser, PLL, low-voltage, LC-VCO

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Acronyms

CMOS Complementary Metal-Oxide-Semiconductor *(pp. vi, vii, 3, 19, 21, 23, 61, 81)*
CP Charge Pump *(pp. vi, vii, 4, 6, 8–10, 13, 32, 48–55, 57, 58, 70, 75, 77, 80)*
CSS Chirp Spread Spectrum *(pp. 2, 27, 63)*

DCO Digitally Controlled Oscillator *(p. 18)*

IoT Internet of Things *(pp. 1, 4, 81, 82)*
ISM Industrial, Scientific and Medical radio bands *(pp. vi, vii, 1, 2, 78, 81, 82)*

LF Loop Filter *(pp. vi, vii, 4, 6–9, 13, 32, 48, 51, 52, 56, 67, 70, 75, 80)*
LoRa Long Range wireless communication technology *(pp. vi, vii, 1, 2, 4, 27, 44, 63, 81, 82)*
LPWANs Low-Power Wide-Area Networks *(pp. 1, 2)*

NMOS N-type Metal-Oxide Semiconductor *(pp. 21, 22, 28, 34, 36, 37, 63, 66, 81)*

Op-Amp Operational Amplifier *(p. 10)*

PDK Process Design Kit *(p. 27)*
PFD Phase-Frequency Detector *(pp. vi, vii, 4–10, 48–53, 57, 60, 75, 77, 80–82)*
PLL Phase-Locked Loops *(pp. vi, vii, 2, 4–8, 10–20, 22, 35, 38, 43, 48–52, 54, 56, 58, 60, 61, 67–72, 74–83)*
PMOS P-type Metal-Oxide Semiconductor *(pp. 21, 28, 36, 37, 63, 66)*
PVT Process, Voltage and Temperature *(pp. 27, 82)*

RF Radio Frequency *(pp. vi, vii, 2–5, 18, 30, 62)*

TSPC True Single-Phase Clocking *(pp. vi, vii, 61, 63, 81)*

VCO Voltage Controlled Oscillator *(pp. vi, vii, 2, 4–12, 16, 18, 19, 21–23, 25, 27, 29, 31, 32, 35, 37–39, 41–44, 46, 48–51, 60, 62, 63, 70, 71, 74, 75, 79–82)*

Symbols

b	Ratio of frequency of a pole to frequency of a zero *(pp. 16, 17)*
ζ	Damping factor of a second-order PLL *(p. 68)*
E(s)	Closed-loop error transfer function of a PLL *(p. 67)*
$\mathbf{f_{out}}$	Oscillation frequency of the VCO *(p. 6)*
$\mathbf{f_{ref}}$	Frequency of the reference or input signal *(p. 6)*
F(s)	Transfer function of a loop filter *(pp. 67, 72)*
$\mathbf{g_m}$	Transistor transconductance *(pp. 25–27)*
$\mathbf{I_{CP}}$	Charge Pump current *(pp. 58, 68, 70)*
L	Value of the inductance H *(p. 23)*
K	Loop gain of a PLL (rad/sec) *(p. 16)*
$\mathbf{K_{PFD}}$	PFD gain (V/rad or A/rad) *(pp. 13, 16, 49, 51, 57)*
$\mathbf{K_{VCO}}$	VCO gain (rad/sec.V) *(pp. 16, 28, 32, 43, 68, 70, 71, 81)*
N	Loop divide ratio *(pp. vi, vii, 6, 8, 12, 70, 82)*
Q	Quality factor *(pp. 23, 25, 29, 34, 39–41, 46)*
τ_2	Time constant of stabilizing zero in a type II PLL (sec) *(p. 16)*
$\mathbf{V_{cntrl}}$	Control Voltage of the VCO *(pp. 5, 6, 9–11, 22, 32, 43, 46, 53, 58, 76, 77, 81)*
ω_n	Natural frequency (rad/sec) of a second-order PLL *(p. 68)*
ω_0	Oscillation frequency (rad/s) *(pp. 23, 25, 28, 38, 40)*

1 Introduction

The primary topics covered in this thesis are highlighted in this chapter, which begins by outlining the motivation behind this work and providing a quick synopsis of the relevant background information, concluding with a description of this thesis organisation.

1.1 Motivation and Background

Internet of Things (IoT) has become a pivotal technological breakthrough in the 21^{st} century. Its capability to connect billions of devices to the Internet, enabling data exchange and communication among them, marks a significant technological evolution. The potential applications of IoT extend across diverse sectors, including smart homes, connected vehicles and healthcare, fueling its rapid growth and expansion. However, its most profound impacts are observed in transportation, agriculture, urban development, environmental management, electrical grids and water management systems, as discussed in [2] and [3].

The use of IoT often implies high energy efficiency, as the devices used are expected to have battery lives extending over several years. In addition, applications like traffic management, environmental monitoring and healthcare demand dependable long-range communications capabilities, sometimes exceeding 10 km. These needs for low-power consumption and long-range connectivity have spurred the development of Low-Power Wide-Area networks (LPWANs). These networks function within the unlicensed industrial, scientific and medical (ISM) radio bands, catering to the specific requirements of IoT applications.

ISM band encompasses a spectrum of radio frequencies designated by international regulatory bodies, such as the ITU Radio Regulations, for unlicensed use in industrial, scientific and medical applications. This band is commonly utilised for low-power, short-range communication technologies including WiFi, Bluetooth, Zigbee, RFID and NFC. Among these technologies, LoRa (Long Range) has emerged as a prominent player in the domain of LPWANs, providing critical support for a wide array of IoT applications.

LoRa is a long-range, low-power, wireless, non-cellular technology. Its radio frequency

(RF) signal modulation is based on Chirp Spread Spectrum (CSS), a technique distinct from those used in previous technologies [4]. CSS employs a frequency spreading method for modulation, enabling the recovery of data from weak signals. In LoRa, chirp pulses, symbols that gradually vary in frequency, are transmitted and arranged sequentially for data transmission. CSS modulation proves invaluable in scenarios requiring reliable and robust communication, even in difficult environments, offering robustness and security while maintaining low power consumption. Consequently, LoRa is characterised by high processing efficiency, low energy usage and resilience to multipath interference. Depending on the environment (urban, rural or mixed), this modulation technique can significantly enhance receiver sensitivity and extend communication distance, potentially covering several hundred kilometres. This range is notably greater than other narrowband transmission methods like Frequency Shift Keying (FSK), providing a distinct advantage in various applications [5].

Consequently, Low-Power Wide-Area Networks (LPWANs) that use Chirp Spread Spectrum (CSS) modulation can adopt a variety of technical strategies. These strategies range from ETSI GS LTN or Weightless to RPMA (Random Phase Multiple Access) and LoRaWAN. Each of these methods is tailored for encoding information from sensors in low-energy environments. Notably, LoRaWAN, developed by the LoRa Alliance, facilitates communication among multiple LoRa modules over the Internet.

Typical parameters for LoRaWan analysis and planning include spreading factor (SF), code rate (CR), channel bandwidth (BW) and received signal strength intensity (RSSI). Each LoRa signal is transmitted on specific channels in the sub-GHz ISM band, typically 430 MHz, **868 MHz** in Europe and 915 MHz in North America [2][6]. These frequencies ensure minimal impact on bridgeable distance from free space attenuation. However, a recent variant of LoRa uses the **2.4 GHz** ISM band, offering a shorter range with a higher carrier frequency and increased bandwidth [7].

For reliable frequency synchronisation in LoRa communication systems, Phase-Locked Loops (PLLs) are crucial. These circuits generate specific frequencies and synchronise them by aligning the Voltage Controlled Oscillator's (VCO) frequency and phase with a reference signal, thus amplifying a low-output reference into a high-frequency output. The feedback loop in a PLL ensures ongoing synchronisation between the input signal and the internal oscillator.

PLLs in LoRa systems serve various purposes, including Modulation and Demodulation, Frequency Tracking, **Frequency Synthesis**, Frequency Generation, Skew Cancellation, Clock Recovery and Frequency Hopping. These functions are vital for the efficiency and reliability of LoRa communication systems.

1.2 Scope of Thesis

While Phase-Locked Loops (PLLs) are extensively used in systems operating in the ISM band, this dissertation will primarily focus on their application as Frequency Synthesisers.

Advancements in technology and submicron CMOS processes have yielded faster, more precise digital circuits with reduced footprints. However, these developments have set higher standards for their Analog | RF counterparts, demanding size, phase noise and gain improvements. The design of Analog | RF devices has become increasingly complex due to two main challenges associated with newer technologies: the reduction in oxide thickness leading to increased parasitic capacitances and diminished output resistances owing to short-channel effects. Therefore, a key challenge in Analog | RF design involves working with low supply voltages to minimise power consumption while achieving low phase noise and meeting performance requirements, despite transistors having lower intrinsic gain and heightened susceptibility to parasitic effects. Additionally, matching the performance of on-chip devices with their off-chip counterparts remains a crucial goal. In light of these challenges, this thesis aims to design a Low-Power Analog Frequency Synthesiser using 130 nm CMOS technology, utilising low-power and low-voltage techniques [8–11].

In radio frequency (RF) transceivers, the Frequency Synthesiser plays a pivotal role by supplying the reference frequency necessary for frequency translation. These transceivers can be broadly categorised into two segments: the baseband (BB) and RF components. The baseband block, typically managed by a microcontroller or a digital signal processor (DSP), is tasked with acquiring, processing and formatting signals. On the RF side, the focus shifts to up-converting (in transmission, TX) and down-converting (in reception, RX) signals for a specific channel, as determined by the Synthesiser [6].

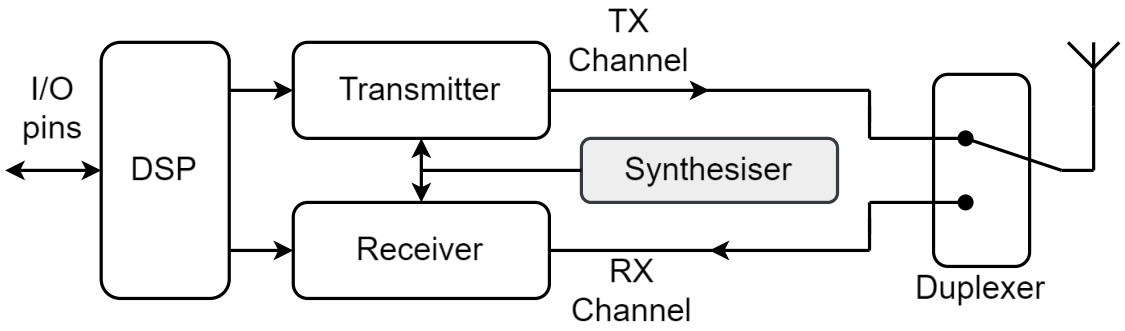


Figure 1.1: Transceiver building blocks.

As shown in figure 1.1, the Synthesiser is a crucial element, bridging the transmitter and receiver [6]. During the up-conversion process, a baseband signal modulates the Synthesiser's signal, creating an RF signal suitable for transmission. Conversely, in down-conversion, the Synthesiser adjusts the RF signal to retrieve the baseband signal. This adaptability of the Frequency Synthesiser across the full RF bandwidth is vital for channel selection. This thesis focuses on the frequencies of 868 MHz and 2.4 GHz, each encompassing specific frequency bands for various channels. In the 867 to 869 MHz range, there are about 10 channels, each with bandwidths of 125 kHz to 4 kHz. For the 2.4 GHz to 2.5 GHz band, the channels feature bandwidths of 203, 406, 812 and 1625 kHz [7]. The Synthesiser must be capable of tuning over this broad frequency range, effectively serving

as the channel selector in the RF transceivers.

1.3 Chapter by Chapter Overview

This thesis is structured into seven distinct chapters, beginning with an introduction that presents the key topics of the study and emphasises the significance of Phase-Locked Loops (PLLs) in achieving frequency synchronisation in Internet of Things (IoT) applications, with a special focus on LoRa communication systems.

Chapter 2 provides a foundational understanding of PLLs, beginning with an overview of Frequency Synthesisers. It then delves into the components, types and diverse performance characteristics of PLLs. Additionally, the chapter includes a literature review, providing context and background on the topic.

Chapter 3 discusses the proposed topology and design of the Voltage Controlled Oscillator (VCO). It encompasses all theoretical aspects of Voltage Controlled Oscillators, ranging from oscillation startup conditions to large signal conductance analysis. The chapter also addresses crucial parameters of the VCO, such as frequency tuning, phase noise and jitter.

Chapter 4 focuses on the characterisation and design of the Phase-Frequency Detector (PFD), including its essential components like the Charge Pump (CP) and Loop Filter (LF). It starts with an in-depth characterisation of its behaviour and concludes with an analysis of the results derived from the PFD's transient response studies.

Chapter 5 centres on the analysis and design of Frequency Dividers, covering both the PLL Frequency Divider and the Quadrature Divide-by-2 circuit.

Chapter 6 unveils the design of the PLL, starting with an exploration of its dynamic behaviour and the design aspects of the Loop Filter. Additionally, it delves into the PLLs transient response and power consumption, providing a comprehensive understanding of its overall performance.

The thesis concludes with *Chapter 7*, where a summary of the findings and suggestions for further work are presented.

2

Phase-Locked Loop Fundamentals

This chapter covers the background knowledge required to comprehend several important elements about the fundamentals of a Phase-Locked Loop (PLL) structure and how it functions. Furthermore, the current PLL architectures and analytical methods have also been discussed.

2.1 Overview

As mentioned in section 1.2, a PLL is commonly used as a Frequency Synthesiser in RF transceivers due to its low output noise, since maintaining data integrity during transmission requires a low noise reference frequency in both up and down conversion procedures.

Although a Crystal Oscillator would be ideal, it is unsuitable for this purpose due to two drawbacks. The first is that the Crystal Oscillators produce low frequencies and the second is that their frequencies are set, meaning that the transceiver cannot change the frequency to select other channels.

An alternative approach is incorporating a Voltage Controlled Oscillator (VCO) where the output signal frequency can be tuned by modifying the control voltage (V_{cntrl}) to choose the channel. The drawback of the output frequency is its susceptibility to control voltage noise, which is affected by the internal noise of the VCO. This can lead to the frequency deviating over time, causing tuning outside the desired channel.

Integrating both oscillators in a PLL produces a low-noise signal with a tunable frequency. Essentially, a PLL functions as a tracking circuit that aligns the phase and frequency of an input signal originating from the Crystal Oscillator with an output signal from the VCO. It operates as a closed-loop feedback system integrating a VCO and a Phase-Frequency Detector (PFD) to ensure the oscillator maintains a consistent phase angle relative to the reference signal. To synchronise with the reference signal from the Crystal Oscillator the Frequency Divider scales down the VCO's signal when it operates as a Frequency Synthesiser [12][13].

Figure 2.1 represents the simplified structure of a Charge Pump PLL and its operation

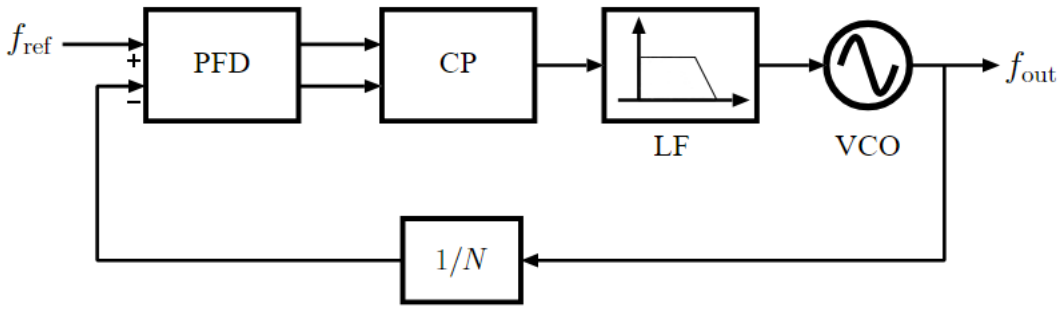


Figure 2.1: Structure of a charge pump PLL.

can be described as follows: the PFD generates an error signal that is proportional to the difference between the phases and frequencies of the two signals, one of which comes from the Crystal Oscillator (identified as f_{ref}) and the other from the VCO, but the latter is divided by N, by the Frequency Divider before the comparison is made. As previously mentioned, this Divider is necessary to allow operation at output frequencies much higher than the crystal frequency.

The Charge Pump (CP) then transforms the signals from the PFD into a current. Subsequently, this current is converted into a voltage by the Loop Filter (LF), eliminating the high-frequency components. The error signal, being proportional to the control voltage (V_{cntrl}), is subsequently fed to the VCO, acting as a controlling input.

Ultimately, the oscillator generates an output signal (f_{out}) that is a multiple of the reference frequency, with this multiple being a linear function of V_{cntrl}. This process continues until the error becomes negligible or reaches equilibrium.

Once the PLL attains a locked state, it maintains the alignment of the feedback frequency with the reference frequency. If there's any deviation in this alignment, an error signal is triggered. This error then leads to an adjustment of the VCO's frequency using a corresponding voltage, which realigns the output to the intended frequency.

Given that a PLL is a feedback system, stability considerations are crucial during its design process. As a result, PLL performance is dependent on several sequentially set parameters, including locking time, acquisition range and tracking range, in addition to the output noise level.

Before diving into the analysis of each PLL building block, it's crucial to clarify a few terms that are frequently used in PLLs:

1. **Hold-In Range:** is a measurement of the DC loop gain and the frequency range that the PLL can maintain a lock on;

2. **Pull-In Range or Capture Range:** is the measurement of the frequency range at which the PLL can lock by missing only a few clock cycles;

3. **Lock-In Range:** defines the frequency range at which a PLL may obtain lock without slipping any clock cycles;

4. **Acquisition Range:** Maximum phase error value for which PLL can reach lock state;
5. **Tracking Range:** Maximum deviation of the phase error for which a locked PLL will remain in a lock state;
6. **Lock time:** total time the PLL takes to establish the lock.

It's important to note that the lock-in range is the smallest of the three metrics, and the hold-in range is the largest.

2.2 PLL Components

In contrast to many feedback systems, a PLL features a unique characteristic where the variable of interest undergoes a change in its dimensions within the loop. Specifically, it transitions from phase to voltage (or current) at the PFD, then is processed by the LF in this altered state before being converted back to phase by the VCO. As noted in [14], regardless of the loop gain's magnitude, the input and output frequencies of the system align when the PLL is in a locked state, even though there might still be a nonzero phase error. This feature is crucial since many applications are unable to accommodate even minor regular fluctuations in input and output frequencies.

Consequently, it's critical to thoroughly examine each of the many PLL circuit components, as shown in the figure 2.1.

2.2.1 Reference frequency

Crystal Oscillators are often used as the reference clock in PLLs due to their exceptional noise performance, as was previously indicated. The phase noise generated by a Crystal Oscillator is considerably less than that of other PLL components. However, not all of the necessary reference frequencies can be easily obtained from Crystal Oscillators that are available on the market. To obtain the required reference frequency, many PLLs use a Frequency Divider in addition to a crystal clock.

In this study, a reference clock is generated from a Crystal Oscillator. This choice is based on the minimal noise contribution from this source compared to other components within the PLL. The crystal being discussed is a temperature-compensated Crystal Oscillator (TCXO) that includes a temperature-sensitive reactance circuit in its oscillation loop to offset the natural frequency-temperature properties of the crystal unit.

2.2.2 Phase-Frequency Detector (PFD)

Phase Detectors are separated into two broad categories: memoryless detectors, whose output is independent of the inputs that came before them. These are built using mixers, such as the diode ring mixer or XOR gates. The second set of detectors is memory-dependent; they are built on sequential circuits that commence with flip-flops and logical

ports and whose output is determined by the preceding inputs. The second type of detector provides greater benefits than the first, including improved frequency acquisition, a longer phase detector range and increased sensitivity to input signal levels.

To generate an output signal similar to the phase error, it's necessary to analyse a Phase Detector (PD) which compares the phase of the feedback signal with the reference signal and produces a voltage proportional to the phase difference.

The PD functions as an error amplifier to minimise the phase difference in the feedback loop. When the phase difference is notable, the phase detector may not provide the correct phase error signal, leading to rapid oscillations between -180° and 180° in each cycle.

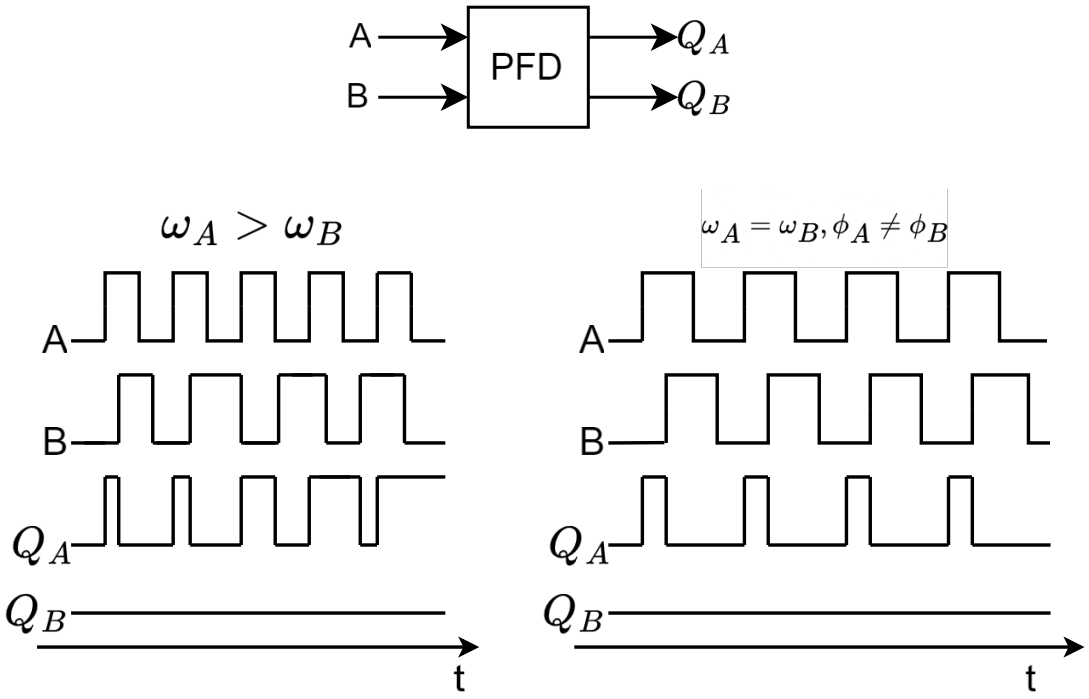
When the N-divided VCO frequency is far from the reference frequencies the PLL may not lock, a problem known as inadequate acquisition range, because the PD is insensitive to the frequency difference at the input. Therefore, a PFD is required to track both phase and frequency.

A PFD analyses both the phase and frequency of the signal from the Frequency Divider and compares these with the reference signal. The logical portion and the CP make up its basic structure. Occasionally, the CP includes the LF and appears separate from the PFD. The logical portion is made up of two D-Flip-Flops (DFFs) with resets. The PFD functions as a three-state state machine and its behaviour can be summarised as follows: when both the VCO and the reference signal are initially high (state 0), both D flip-flops will reset. In state -1, the output voltage decreases, triggered only by the activation of the current sink, which leads to the depletion of charge. In state 0, both the current sink and source are disconnected, maintaining a steady output voltage as no charge is either added to or removed from the output node. Conversely, in state 1, the output voltage increases due to the sole operation of the current source, resulting in a charge being injected into the node.

Figure 2.2 illustrates a PFD's operation conceptually, showing how these state changes are controlled by the edges of the VCO signal and the reference. The circuit functions according to the following principles and generates two outputs, Q_A and Q_B: If Q_A is low, a rising edge on A produces a rising edge on Q_A; if Q_A is high, a rising edge on B resets Q_A. The circuit shows symmetry for A and B as well as Q_A and Q_B. From fig. 2.2a, it is evident that Q_A generates pulses while Q_B stays at zero if $\omega_A > \omega_B$. On the other hand, positive pulses arise at Q_B and Q_A if $\omega_B > \omega_A$. In contrast, the circuit produces pulses at Q_A or Q_B with a width equal to the phase difference between A and B if $\omega_A = \omega_B$, as shown in fig. 2.2b. The average value of Q_A - Q_B thus represents the frequency or phase difference [15].

Put simply, when the reference signal is faster than the feedback signal, the UP signal is activated (high) while the DOWN signal is deactivated (low), and the reverse is true when the feedback signal is faster. It's important to note that both UP and DOWN signals are high when they are synchronised.

While the PFD offers advantages over a basic Phase Detector (PD), it's important to recognise its limitations. Specifically, if the phase difference between the inputs is very small, the inherent delay in the logic gates of the D Flip Flops can create a dead zone. In



(a) (b)

Figure 2.2: Response of a PFD to inputs with unequal (a) frequencies, or (b) phases, adapted from [15].

the specified region, the PFD cannot precisely detect phase differences. Consequently, the CP and LF lose their ability to regulate the VCO's control voltage (V_{cntrl}). This effectively leaves the VCO to function like an open circuit, however, the dead zone can be avoided by introducing a small phase error delay in the reset path, which leads to an increase in loop gain and a decrease in jitter. This guarantees that the reset path's delay exceeds the CP currents' switching time.

Charge Pump (CP)

The Charge Pump is often made up of two current sources that are switched by the PFD's control signals. The duration needed to establish the correct voltage at the control terminal of the VCO by turning on and off the current source and sink dictates the amount of charge required from the Loop Filter to attain and sustain loop synchronisation.

The CP is responsible for converting the PFD's UP and DOWN digital signals into a current signal. Thus, the two switched current sources that make up the CP inject or remove charge based on the PFD output. The PFD detects when the referencing frequency has a rising edge, this triggers a high signal that turns on the UP switch and makes the CP inject current into the filter. As a result, the control voltage (V_{cntrl}) increases. To prevent current phase shifts, the currents flowing through the I_{up} and I_{down} switches must be equivalent. Furthermore, the switching speed requirements establish a restriction on the

minimum current in the CP.

There are a few non-idealities in the CP and their majority lead to spurious tones, so it's critical to analyse and minimise them when designing the CP. In every reference cycle, an excessively unwanted amount of charge is injected into the Loop Filter due to a mismatch in the current sources. Leakage currents from the CP are also a design concern.

Loop Filter (LF)

The Loop Filter not only sets the capture and tracking ranges and ensures loop stability but also determines the dynamic characteristics of the PLL. Although faster frequency changes are possible with a high cutting frequency, the high-frequency PFD components must be eliminated, as they may cause spurious signals at the VCO's input. As a result, the filter transforms the CP signals into a control voltage (V_{cntrl}) that polarises the VCO. Based on this, the VCO oscillates at a frequency that is higher or lower, changing the phase and frequencies of the feedback.

Loop Filters in a system can be categorised as either passive or active low-pass filters. Passive filters, which consist solely of passive components like resistors and capacitors, are easier to implement and are more power-efficient. However, in a Charge Pump PLL, the operational voltage range is limited to ensure the current source remains in the saturation region when the PLL is locked.

To address the limitations of passive filters, active filters can be utilised. These filters incorporate resistors and capacitors, along with an operational amplifier (Op-Amp), expanding their voltage handling capabilities, the Op-Amp boosts the gain of the loop. Active filters are typically employed when a high VCO tuning voltage is required. However, it's important to note that active filters consume more power, require more area and make the design more complex. Due to these factors, a passive filter will be used in the present work.

Furthermore, a higher-order Loop Filter can be used to improve reference spur attenuation. However, it's crucial to carefully consider its design, as it can impact the stability of the loop. A higher-order filter extends the filter transfer function by introducing additional poles. The presence of these additional poles reduces the phase margin and subsequently affects the stability margin of the loop [16].

2.2.3 Voltage Controlled Oscillator (VCO)

The most crucial and complex component of a PLL design is the Voltage Controlled Oscillator (VCO), primarily because it is the main contributor of noise to the PLL output. This noise extends beyond the loop bandwidth and is subsequently filtered by the loop bandwidth within the PLL's frequency range of interest. A VCO is a tunable oscillator whose output frequency is dependent on the control voltage (V_{cntrl}). It's designed to produce a signal according to the Barkhausen criterion. The first criteria for feedback loop stability dictates that the total loop gain should be equal to one. The second criteria

requires that the total phase shift around the loop be either 0° or an integer multiple of 360°. It should be noted that, in an ideal world, the output rate would be directly proportional to the control voltage given to the input. As was previously stated, the VCO oscillates in its normal working mode at a free running frequency until a signal is applied (V_{cntrl}).

Ring oscillators and LC tank oscillators are the two most prevalent forms of oscillators. Connecting numerous inverters in a closed loop to ensure that the total phase delays are a whole number multiple of 2π allows for the creation of a ring oscillator. A ring oscillator has the benefit of having a wide tuning range. Nevertheless, its phase noise performance is subpar. In addition, the active components of the ring oscillator have significant power consumption [17].

An LC tank oscillator, on the other hand, creates a resonant circuit using passive components such as an inductor and a capacitor. Consequently, it consumes less power than a ring oscillator. An LC oscillator is increasingly preferred in Frequency Synthesisers due to its superior noise performance. Additionally, this oscillator can be implemented using different topologies, such as Colpitts, Hartley and cross-coupled oscillators. A notable downside of the LC tank oscillator is its substantial requirement for die area. The chosen design configuration for this work is the cross-coupled topology.

Figure 2.3 illustrates that the resonant LC cross-coupled oscillator can be modelled as an RLC parallel circuit. In an ideal LC tank, the resistance component is considered to be negligible. Nonetheless, in real-world applications, resistive components in the inductor and capacitor are considered, these components are shown as a lumped R_p. To sustain oscillation it's essential to introduce a negative resistance in parallel.

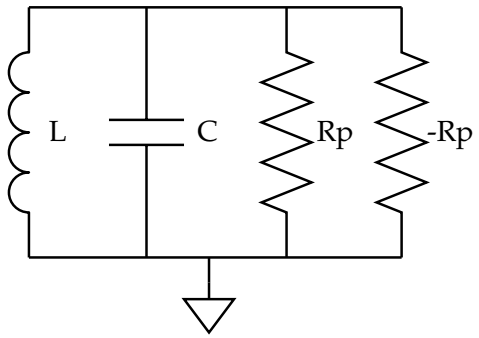


Figure 2.3: RLC parallel circuit.

The inductor and capacitor's resistive components are shown as a parallel resistance, or R_p. To account for the loss in R_p, a negative resistance, -R_p, is introduced.

2.2.4 Frequency Divider

Typically, the output frequency of the VCO is considerably higher than the reference frequency. To lock the PLL, the output frequency of the VCO needs to be reduced to match the reference frequency. This is achieved by using a sequence of Frequency Dividers known as a prescaler. Because of its high working frequency, the first Frequency Divider

following the VCO must be carefully designed. Additionally, the modern low-supply voltage technologies used further complicate the design. In the PLL, Frequency Dividers are also utilised to generate quadrature output signals.

There are several architectures for the Frequency Divider, however, in this thesis, they will be grouped into integer-N dividers and fractional-N dividers depending on the value of N, with the second group covering a larger range for the selection of frequencies [18].

2.3 PLL Types

PLL topologies are categorised into types and orders. The type, as defined in [19], indicates the number of integrators in the circuit, and the order, the number of poles in the open loop transfer function.

2.3.1 Type I

The oscillator in this kind of PLL functions as a phase integrator and employs an XOR or a mixer as a Phase Detector. It is rarely utilised in Analog Frequency Synthesisers due to its narrow lock range, although it might be useful for clock recovery and frequency demodulation.

1^{st} Order

A first-order type I PLL will have a phase margin of 90° and when a step is applied to the input, it will lock with a steady-state phase error inversely proportional to the loop gain. There are other drawbacks to this kind of PLL. These include:

- The bandwidth of a closed-loop PLL is determined by its DC gain.;
- In the band, the output phase follows the input, and the VCO noise is rejected. Outside, the phase is determined by the frequency of VCO;
- For phase error to be reduced, a high loop gain is required, which implies a large bandwidth (which is undesirable in some applications where it is necessary to filter the phase noise of the reference signal);
- The phase detector output is not filtered, which causes a second harmony to appear in the mixer (the XOR output signals must be filtered).

2^{nd} Order

Second-order PLLs provide additional degrees of freedom while resolving some of the aforementioned issues. However, unless the loop filter has an infinite DC gain, the loop will have a phase error other than zero if there is a step in the frequency.

In summary, a 2^{nd} order type I PLL faces three key trade-offs: one between the damping factor (ζ) and the low-pass filter cutoff frequency (ω_{LPF}), another between ζ and the Phase Frequency Detector gain (K_{PFD}), and a third between the acquisition range and ω_{LPF}. The initial step involves devising a method to overcome limitations in the acquisition range, followed by an analysis of the trade-offs associated with ζ.

2.3.2 Type II

Type II PLLs feature a Charge Pump, leading to a scenario where the Loop Filter capacitor acts as a second integrator by integrating the current from the Charge Pump. Type II PLLs are highly favoured in Frequency Synthesisers, owing to their extensive lock range and the capability of achieving a near-zero phase difference between the output and reference phases.

2^{nd} Order

The behaviour of a second-order PLL can be understood through control theory parameters like the natural frequency (ω_n) and damping factor (ζ). Second-order Type II PLLs are extensively covered in application notes [20] and academic literature [21]. A key advantage of Type II PLLs is their ability to maintain zero phase error, even in the presence of frequency offsets. However, for stability purposes, a zero in the Loop Filter is necessary for a Type II PLL. This inclusion, while necessary, can introduce additional peaking in the frequency response.

3^{rd} Order

Frequently, adding a secondary capacitor provides additional filtering to reduce reference spurs. These are the most prevalent types and orders (PLLs with a CP and 2^{nd} order LF), which can be found in implementations of Frequency Synthesisers meant for wireless applications as well as in literature [22]. This approach is also employed in the present work.

Higher Order

In certain instances, the utilisation of a higher-order filter is crucial for reducing noise and spurious tones in a PLL. This is because, in transmit mode, it is imperative to limit spur levels to prevent interference with users in the same or adjacent systems. In receiver mode, local oscillator (LO) spurs can significantly impair the demodulation of the mixed-down signal. Nevertheless, PLLs incorporating more than two integrators are uncommon in frequency synthesisers and are generally reserved for specialized applications [22].

2.4 Phase and Frequency Relationships

Because a PLL transforms the phase variable into voltage and then back to phase, grasping the interaction between phase and frequency is essential before beginning the design.

At first, it's crucial to recognise that angular frequency is essentially the first derivative of phase with respect to time. This leads to:

$$\frac{d\phi(t)}{dt} = \omega(t) \tag{2.1}$$

$$\phi(t) = \int_0^t \omega(\tau) d\tau \ . \tag{2.2}$$

Considering the following sinusoid $u_1(t)$ with angular frequency $\omega_1(t)$ and phase $\phi_1(t)$:

$$u_1(t) = sin(\omega_1(t) + \phi_1(t)) \ . \tag{2.3}$$

As shown in figure 2.4 when a Phase Step is applied

$$\omega_1(t) = \Delta\Phi u(t) \text{ with} \tag{2.4}$$

$$u_1(t) = sin(\omega_1(t) + \Delta\Phi u(t)) \ , \tag{2.5}$$

there is no change in frequency.

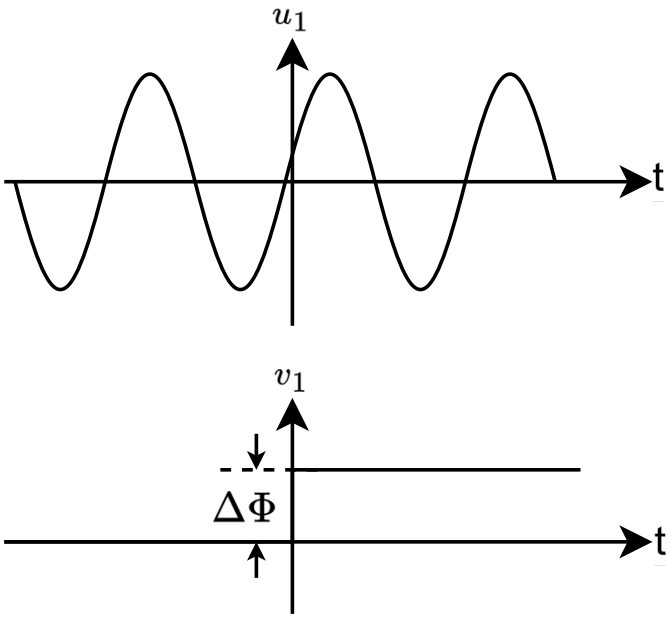


Figure 2.4: Phase and Frequency Relationships: Phase Step.

Applying a Frequency Step, as shown in figure 2.5, will produce a ramp in phase:

$$\omega_1(t) = \omega_0 + \Delta\omega \tag{2.6}$$

$$u_1(t) = sin(\omega_0(t) + \Delta\omega t) = sin(\omega_0(t) + \phi_1(t)) \,, \tag{2.7}$$

where $\phi_1(t) = \Delta\omega t$.

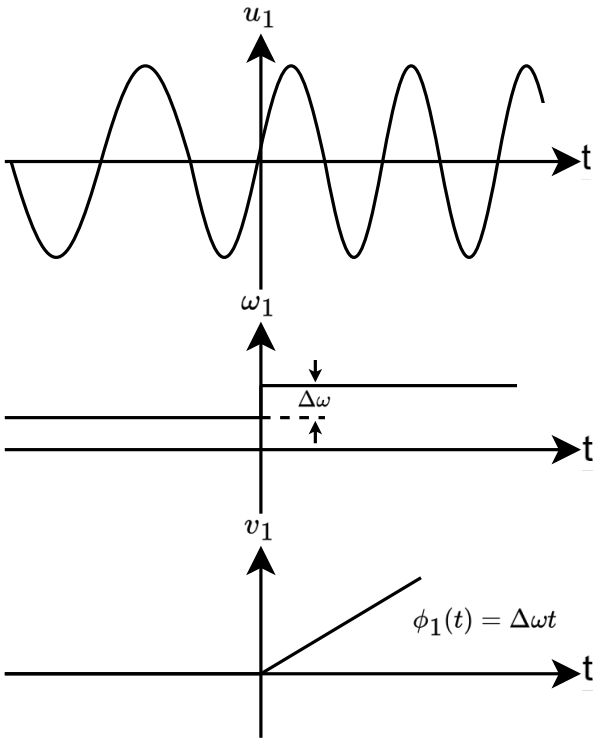


Figure 2.5: Phase and Frequency Relationships: Frequency Step.

Finally, a Frequency Ramp, as shown in figure 2.6, will produce a quadratic change in phase:

$$\omega_1(t) = \omega_0 + \Delta\omega t \tag{2.8}$$

$$u_1(t) = sin(\int_0^t (\omega_0 + \Delta\tau)d\tau) = sin\left(\omega_0 t + \frac{\Delta\omega}{2}t^2\right) = sin(\omega_0 t + \phi_1(t)) \,, \tag{2.9}$$

where $\phi_1(t) = \frac{\Delta\omega}{2}t^2$

2.5 Loop Characteristics

As was stated before, the 2^{nd} Order Type II PLL is a simplification that is frequently seen in PLL literature but is less common in real-world applications. At higher frequencies, PLLs frequently has additional poles. It's possible that some of these poles were added on purpose to suppress disturbances at higher frequencies coming from the Phase Detector

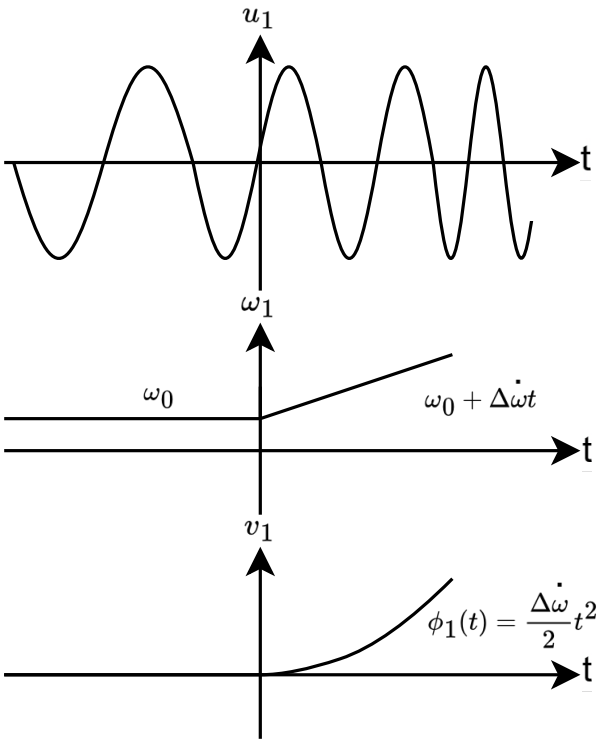


Figure 2.6: Phase and Frequency Relationships: Frequency Ramp.

or to provide a sharper roll-off in the system frequency response. The additional poles are regarded as parasitic because they result from practical aspects of the feedback loop that inevitably have limited frequency responses. Examples of these elements include stray capacitances, amplifier bandwidth restrictions or low-pass circuits in the VCO circuit's control path. In many instances, the frequencies of these poles are significantly higher than the desired loop bandwidth, allowing them to be initially disregarded in the design analysis. However, there are situations where it's necessary to take into account one or more high-frequency poles [23].

This section concentrates on a basic scenario involving just a single additional pole that is of importance. Describing the dynamic behaviour of the entire PLL, where the open-loop was obtained from the time analysis and obtaining the impulse response, then applying the Laplace transform [15].

Figure 2.7 illustrates the simplified PLL closed-loop transfer function, and the open-loop Type II 3^{rd} Order Forward Path Gain can be represented by

$$G(s) = \frac{K_{PFD}K_{VCO}}{s}\frac{s\tau_2+1}{s\tau_1(s\tau_3+1)} = \frac{K}{s}\left(1+\frac{1}{s\tau_2}\right)\frac{1}{s\tau_3+1} = \frac{K}{s}\left(1+\frac{1}{s\tau_2}\right)\frac{1}{1+\frac{s\tau_2}{b}}, \quad (2.10)$$

where the 3^{rd} pole is located at $s = \frac{-1}{\tau_3}$, K=$K_{PFD}K_{VCO}\frac{\tau_2}{\tau_1}$ and b= $\frac{\tau_2}{\tau_3}$. This being a 3^{rd} order PLL, it has three parameters, K, τ_2 and b.

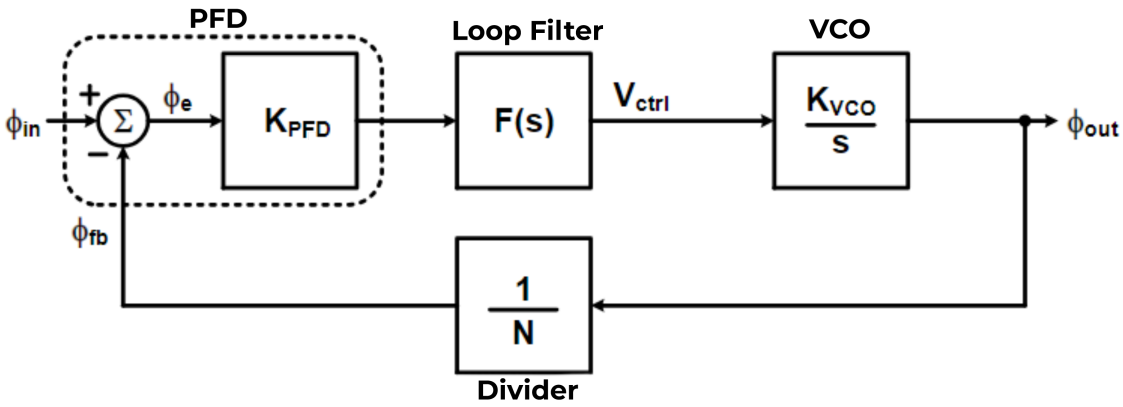


Figure 2.7: PLL Transfer Function Structure.

Manipulating equation 2.10, the closed-loop transfer function and error function become, respectively

$$H(s) = \frac{K\tau_2(s\tau_2 + 1)}{\frac{s^3\tau_2^3}{b} + s^2\tau_2^2 + Ks\tau_2^2 + K\tau_2} \tag{2.11}$$

$$E(s) = \frac{s^2\tau_2^2(\frac{s\tau_2}{b} + 1)}{\frac{s^3\tau_2^3}{b} + s^2\tau_2^2 + Ks\tau_2^2 + K\tau_2}\,. \tag{2.12}$$

It's important to point out that substituting $\tau_3 = \tau_2$ (i.e., b = 1) into equation 2.10 results in the cancellation of the stabilising zero by the 3^{rd} order open-loop pole. This leads to transfer functions identical to those of Type II 2^{nd} order PLL, where the Loop Filter functions as a basic integrator. Therefore, b = 1 marks a boundary for stability; the loop becomes unstable if b falls below 1. Note that damping will be unacceptably small for a large loop gain [19].

2.6 Literature Review

A comprehensive search of the literature has been conducted to find papers on Phase Locked Loop design. A Phase-Frequency Detector is used by the Charge Pump PLLs to achieve faster locking and better tracking performance. Also, all Digital Phase Locked Loops have drawn interest recently because they can shorten system turnaround times and provide improved testability, programmability, stability and portability across various processes.

Table 2.1 presents a summary of the characteristics of Analog and Digital PLLs. These articles were published between 2015 and 2022, inclusive. The aforementioned PLLs realises the various building components using Analog, Digital or semi-digital approaches.

The oscillator block of the Phase Locked Loop is implemented using either a Digitally Controlled Oscillator (DCO) or a Voltage Controlled Oscillator (VCO).

Table 2.1: Comparison of published PLL papers.

Ref.	CMOS (nm)	Method	Type	Area (mm^2)	Lock time (μs)	Frequency (GHz)	Vdd (V)	Power (mW)	Phase Noise (dBc/MHz)	Jitter RMS(ps)
[24]	55	Analog	Frac-N	0.413	—	0.840 - 0.975	1.2	38.4	-138.9@1.8	—
[25]	130	Analog	Frac-N	—	1.8	1 - 2	1.5	—	-78.8@1	—
[26]	65	Analog	Cascaded Frac-N	0.28	—	26.2 - 32.4	1	26.9	-112.6@1	$70.4{\cdot}10^{-3}$ [1]
[27]	65	Analog	Frac-N	—	12	1.9 - 2.7	1	2.94	-110@1	—
[28]	28	Analog	Frac-N	0.092	—	0.5 - 4	—	9.56	-86@1	2.13
[29]	90	Analog	Frac-N	—	135	4.78 - 5.87	1.2	4.5-5	-117.5@1	—
[30]	90	Analog	Int-N	0.00208	8	0.176 - 0.433	1	0.28	-106@1	—
[31]	65	Digital	Frac-N	0.23	4.2	2 - 2.8	1	0.98	-111@500 to -109@500	1
[32]	40	Digital	Frac-N	0.22	22	1.7 - 2.7	1/0.8	1.19	-109@1	1.7
[33]	65	Digital	Frac-N	0.38	48	3.3 - 3.8	1	9.7	-110@1 to -107.8@1	$390{\cdot}10^{-3}$ to [2] $560{\cdot}10^{-3}$

2.7 Other PLL design considerations

In delineating a valid product, it is imperative to articulate a set of supplementary performance requirements beyond those mandated by the wireless standard. While these parameters, encompassing facets such as the operational environment and current consumption, do not exert a direct influence on the transceiver's core functionality, they often serve as decisive factors in demarcating a product's competitive viability.

Operation temperature:
On-chip temperature may be a few degrees above room temperature, depending on the packaging and power consumption [34].

The circuit is required to operate effectively within a specified temperature range and must be capable of tolerating variations in temperature. This becomes particularly pertinent in instances where automatic calibration mechanisms are employed. Typically, calibration is initiated upon the circuit's power-up, however, the potential arises for alterations in performance consequent to temperature elevations during operation. Temperature-induced variations can negatively impact the phase noise performance of the circuit, which could lead to a loss of lock in the PLL.

Power supply domains and isolation:
The quality of the signal and the separation between different blocks in a circuit are highly dependent on the design of supply domains and the physical layout. Achieving effective isolation requires precise segmentation of the chip. In Radio Frequency (RF) circuits,

[1] Integrated Jitter from 10 kHz to 10 MHz
[2] Integrated Jitter from 10 kHz to 10 MHz

where there are often limitations on the number of available pads, it's crucial to determine the appropriate number of supply and ground pins strategically. This decision is crucial for achieving effective isolation while also handling a manageable number of pins [22].

Testing and calibration:
Discrepancies between measured data and simulations persist as a recurring phenomenon. Such disparities may be attributed to either process variations or inaccuracies in the underlying models. It is optimal to accommodate substantial process variations while upholding robust circuit performance to achieve an elevated yield.

Output power:
For components that rely on the signal from the PLL to operate effectively, the output amplitude must stay within a defined range. Notably, the output power level of the VCO often fluctuates with changes in the operating frequency, a situation that becomes more pronounced when dealing with a wide tuning range, as discussed in [35].

Start-up and shutdown duration:
The time it takes for the circuit to switch from an idle state to an active state depends on various factors. These include how quickly it reaches the ideal bias values, the time required for the VCOs to reach their final amplitudes and other influential elements. It's important to note that the switch time of the PLL is closely related to the power-up time of the circuit.

Supply voltage and power consumption:
As processes get more complicated, the supply voltage that can be used tends to drop because of limits set by CMOS scaling. While the adoption of swifter devices and a lower supply voltage is conducive to diminished power consumption, it concurrently imposes limitations on the range of analog circuits.

In the context of low-power applications, due consideration must also be given to power downtime and idle current consumption. The latter assumes significance, particularly if the PLL is operational for brief intervals, where the idle current may significantly contribute to the overall power consumption.

Chip area:
Minimising the silicon area of the chip is a desirable objective, concurrently with the reduction of power consumption. In this context, a trade-off is inherent between performance and area. While the integration of inductors may yield superior performance and decreased power consumption, it comes at the expense of considerable spatial occupation. Notably, high-quality (high-Q) on-chip inductors, in contrast to their low-Q counterparts, take up greater space.

Moreover, a trade-off prevails between area and isolation. Greater spatial separation

between critical blocks and interconnecting wires can increase chip area while concurrently improving isolation.

2.8 Summary

This chapter presents a PLL's basic operating principle. PLL types are reviewed along with their distinctions, furthermore, this chapter covers PLL architectures. Given that a Charge Pump PLL was selected for this project, a thorough explanation of each block is given. PLL simulation, circuit design and architecture selection are all part of the difficulty. In addition, a literature review was carried out to learn how PLL circuits are designed.

3

Voltage Controlled Oscillator

This chapter elucidates the design and simulations of a Voltage Controlled Oscillator. A comprehensive overview is provided, firstly, the chosen topology is presented and then the set of equations needed to characterise the oscillator behaviour, including detailed explanations for each stage of the circuit, the components utilised and their respective characterisations.

3.1 Proposed Topology

As previous chapters have covered, LC-VCOs topologies are frequently preferred over other structures like relaxation or Ring Oscillators when dealing with high-frequency applications. However, in the context of this thesis where operational frequencies are 868 MHz and 2.4 GHz, the decision between a Ring Oscillator and an LC-VCO becomes more challenging. At these frequencies, the values of inductance and capacitance required for the LC-VCO topology are high for an integrated circuit leading to increased area requirements. To address this challenge and implement an LC-VCO suitable for integrated circuits, the operational frequency of the VCO will be doubled. To do this, a 2-Divider that can also provide quadrature outputs is suggested [36]. These quadrature outputs prove beneficial for quadrature modulation.

Within various LC oscillator structures, the CMOS cross-coupled LC-VCO stands out for its superior noise performance and improved symmetry in rise and fall times [37]. The two most widely implemented topologies within this category are the NMOS VCO or PMOS VCO and the Complementary VCO.

Concerning the two LC-VCOs topologies, the primary differences originate from the placement of the resonator and the oscillation frequency. Two integrated inductors are employed in the VCO structure occupying a larger area. The tuning range and oscillation frequency of the Complementary VCO, on the other hand, are affected by the parasitic capacitances (C_{gs} and C_{gd}) introduced by the PMOS pair. When taking into account the same current consumption, small signal analysis shows that the Complementary VCO generates an output signal amplitude double that of the VCO design [38]. Additionally,

for a specific current level, a complementary topology provides a higher transconductance and its symmetrical design also facilitates quicker switching in the cross-coupled pair. The improved phase noise performance linked to this architecture is an additional benefit [39]. Moreover, the complementary structure guarantees that all gate voltages remain within the supply voltage, ensuring stable operation within process limits over time. However, a major drawback of this design becomes apparent when operating with low supply voltages, primarily due to the stacking of transistors.

In the design of an oscillator, there's a trade-off between power consumption and phase noise and since the PLL in this dissertation works in low-voltage the NMOS VCO topology will be chosen.

3.2 LC-VCO Characterisation

Before going into the chosen topology it's necessary to understand the VCO's linear relation between the output frequency and the input control voltage (V_{cntrl}). As such, the Laplace transform of the VCO is presented below:

$$\omega_{out}(t) = K_{VCO} v_{cntrl}(t) \tag{3.1}$$

$$\mathscr{L}[\omega_{out}(t)] = K_{VCO} v_{cntrl}(s) \tag{3.2}$$

$$\phi(t) = \int_0^t \omega_{out}(\tau)\, d\tau = \int_0^t K_{VCO} v_{cntrl}(\tau)\, d\tau \tag{3.3}$$

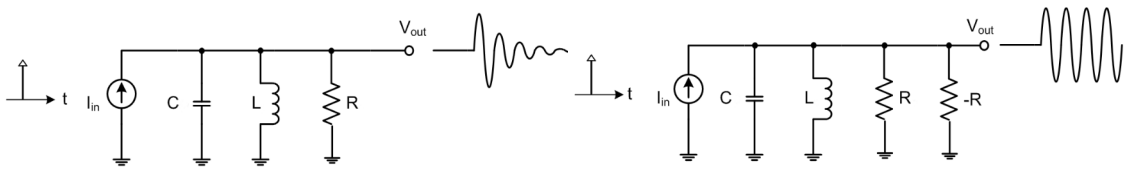
$$\mathscr{L}[\phi_{out}(t)] = \phi_{out}(s) = \frac{\omega_{out}(s)}{s} = \frac{K_{VCO} v_{cntrl}(s)}{s}\,. \tag{3.4}$$

Resulting in

$$H_{VCO}(s) = \frac{\phi_{out}(s)}{v_{cntrl}(s)} = \frac{K_{VCO}}{s}\,. \tag{3.5}$$

A fundamental understanding of negative resistance is imperative because as mentioned in section 2.2.3, the LC-VCO topology leverages this concept to counterbalance the losses arising from the resonator.

To delve deeper into this concept, consider the simple tank circuit represented in figure 3.1a. This setup includes a coil with inductance L, a capacitor with capacitance C and a resistor represented by R, which accounts for the losses in the reactive components, these elements are connected in parallel and driven by a current impulse. The tank displays a fading oscillatory behaviour because part of the energy transmitted between the inductor and capacitor in each cycle is lost as heat in the resistor. As demonstrated in figure 3.1b, putting a negative resistor equal to -R in parallel with R affects the dynamics. Retrying the experiment with R$||$(-R) = ∞ will cause the tank to oscillate indefinitely.



(a) (b)

Figure 3.1: (a) Decaying impulse response of a tank, (b) addition of negative resistance to cancel the loss represented by R.

In essence, for oscillations to occur, certain criteria must be satisfied, leading to a closed-loop gain that is greater than or equal to one in magnitude and free of any imaginary components:

1. The negative conductance generated by the active network offsets the positive conductance (or loss) inherent in the tank circuit;

2. The phase shift of the closed-loop gain is zero.

Following the introduction of the fundamental principles of an LC-VCO, it becomes essential to advance to its analytical characterisation. A VCO with a tail current source is illustrated in figure 3.2. The oscillator's primary component is the tank resonator which comprises capacitors (C) and inductors (L), this LC tank also includes the tunable capacitors or varactors (C_{var}) that are used for continuous tuning (section 3.2.1.1) and the CapBank for the discrete tuning (section 3.2.1.2). The tank losses are compensated for by the (M_n) transistors which provide a negative resistance. Finally, while restricting the voltage swing across the resonator and potentially degrading VCO noise, the tail current source offers the advantage of delivering a consistent current to the cross-coupled differential pair of the LC-tank. This characteristic makes the VCO less susceptible to variations in voltage supply [40]. In conclusion, the tail current provides a means for designers to strike a balance between power dissipation and phase noise performance.

For the complete characterisation of the LC-VCO, the subsequent equations apply, along with a few additional constraints that are inherent in the circuit behaviour.

In conventional CMOS technology, the Q of symmetric inductors increases from around 3 or 4 at 1 GHz to approximately 8 at 5 GHz, 10 at 10 GHz and 15 at 20 GHz. Higher Q values are achieved through processes that create thick metal layers [15].

The quality factor Q_L of the inductor is given by

$$Q_L = \frac{\omega_0 L}{R_s}, \tag{3.6}$$

where ω_0 is the oscillation frequency, L is the value of the inductance and R_s is the inductor's equivalent series resistance.

Assuming a non-ideal inductor, ideal varactors and MOSFETs, the oscillation frequency is determined by

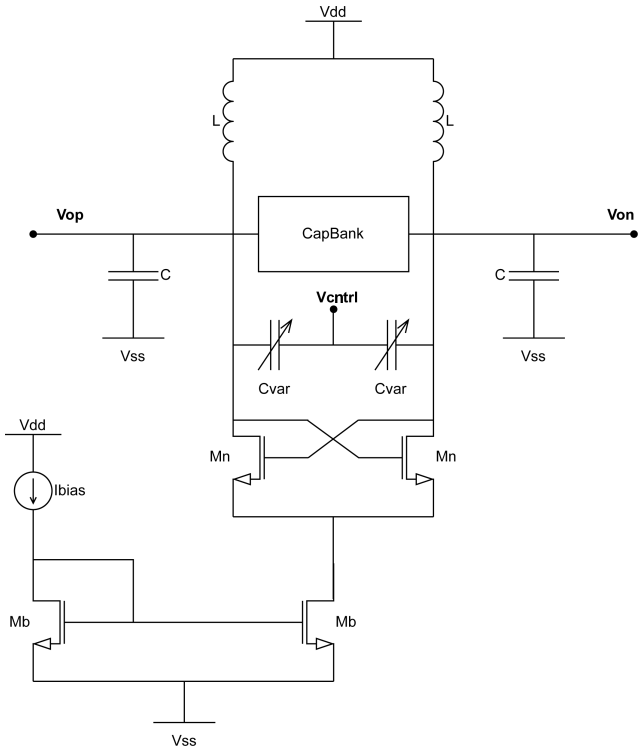


Figure 3.2: LC-VCO structure NMOS-only with a tail current source.

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}\sqrt{1 - \frac{R_s^2 C}{L}} \qquad \text{considering } \overline{Y}_{LC} = \frac{1}{R_s + jX_L} + \frac{1}{-jX_C} \tag{3.7}$$

$$\alpha g_{tank,max} \leq g_{active} \ , \tag{3.8}$$

here, α refers to the starting factor which is guaranteed to be at least 1 and usually lies between 2 and 3 to ensure the startup condition. The conductances of the tank and active components are referred to as g_{tank} and g_{active}, respectively.

Taking into account the input signals v_1 and v_2, which are applied to transistors M_1 and M_2 respectively (as shown in fig. 3.2, with M_1 on the left and M_2 on the right), each transistor in this pair primarily operates as a common-source amplifier. These amplifiers are characterised by a complex, tuned load that consists of a lossy inductor and a capacitor connected in parallel. As displayed in figure 3.2:

$$v_1 - v_2 = v_x \tag{3.9}$$

$$i_x = -gm_1 v_1 = gm_2 v_2 \ , \tag{3.10}$$

it follows that

$$\frac{v_x}{i_x} = -\left(\frac{1}{gm_1} + \frac{1}{gm_2}\right) \ , \tag{3.11}$$

which, for $gm_1 = gm_2$, and assuming ideal MOSFETs (i.e. no parasitic resistances or capacitances), the entire differential amplifier can be modelled as a negative resistance -R $= \frac{-2}{gm}$.

By the definition of Q $\left(Q = \frac{\omega_0}{\omega_1 \omega_2}\right)$ it can also be equal to $\frac{R_p}{\omega_0 L}$, with ω_0 being the resonant frequency of the lossless tank represented by

$$\omega_0 = \frac{1}{\sqrt{LC}} \, . \tag{3.12}$$

Within this framework, the parallel resistance R_p, which signifies the total parallel losses in the tank circuit, is connected to the individual loss factors of both the inductor and capacitor components.

The Q of the inductor and the capacitor is given by $Q_L = \frac{\omega_0 L}{R_s}$ and $Q_C = \frac{1}{R_s \omega_0 C}$, where R_s represents the series resistance of the inductor and capacitor, respectively.

Since it's frequent for capacitors to exhibit considerably higher Q values than inductors in silicon-integrated processes (although this might not hold if varactors are employed as capacitors). As such, the Q of the inductors dominates the losses of the VCO tank, meaning that $Q_L \ll Q_C$ resulting in $Q_L \approx Q_{Total}$.

One can then write

$$Q_{Total} = \frac{R_p}{\omega_0 L} = Q_L = \frac{\omega_0 L}{R_s} \tag{3.13}$$

as the quality factor of the lossy tank. And so

$$R_p = \frac{(\omega_0 L)^2}{R_s} = \left(\frac{\omega_0 L}{R_s}\right)^2 R_s = Q_{Total}^2 R_s \, , \tag{3.14}$$

R_s being the series resistance of the inductor, R_p the equivalent parallel resistance of the lossy tank and Q_{Total} is the quality factor of the lossy tank.

The performance of the LC-VCO is impacted by parasitic components, as they lead to increased losses. Consequently, a higher transconductance (g_m) is required compared to what would be ideal in an optimal transistor scenario. Through their interaction with the tank capacitance, parasitic capacitances lower the oscillation frequency, necessitating a drop in the tank's C. In addition, parasitic resistances raise oscillator phase noise through their contribution to thermal noise.

Given the symmetry of the circuit and the assumption that there is no a.c. voltage between any of the elements, the current source node can be considered a virtual ground. So as shown in figure 3.3, ignoring the effects of gate resistance rg, rds (rds is not an actual resistance adding noise. Rather, it derives from channel path length modulation, which lowers the MOSFET's a.c. output resistance and partially de-Qs the LC tank) appears in parallel with R_p. Note that parasitic elements from the current source, varactors or the CapBank were not included in figure 3.3, and drain-bulk capacitances of the are also not included, but were considered in the final design.

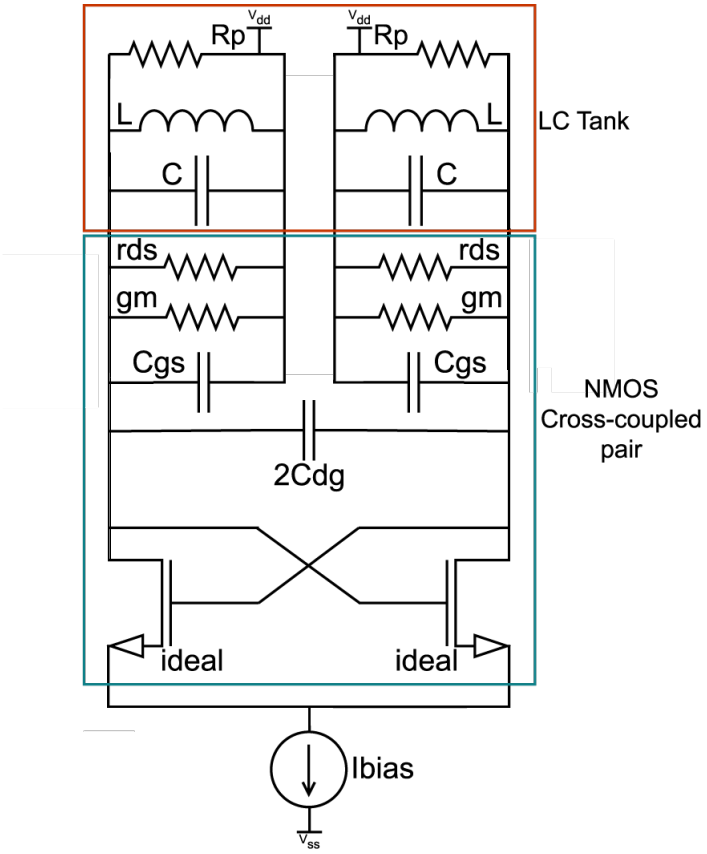


Figure 3.3: LC tank with parasitic elements.

As such the oscillation frequency will change to

$$f_{osc} = \frac{1}{2\pi\sqrt{L(C + C_{gs} + 4C_{gd})}}\sqrt{1 - \frac{R_s^2(C + C_{gs} + 4C_{gd})}{L}}\,. \tag{3.15}$$

According to the aforementioned equation, the transistors' capacitances effectively increase the tank capacitance, C. Furthermore, there is an adjustment to the start-up g_m condition that changes the absolute minimum g_m needed for oscillation to become

$$gm \geq \frac{1}{r_{ds}} + \frac{R_s(C + C_{gs} + 4C_{gd})}{L}\,. \tag{3.16}$$

Achieving the necessary transconductance (g_m) to offset all losses, both from the tank and the transistors, requires precise transistor biasing. If the value of V_{gs} - V_t (where V_t is the MOSFET threshold voltage) is excessively high, g_m may decrease due to mobility degradation and the effects of saturating velocity in channel carriers. On the other hand, if V_{gs} - V_t is too low, the transistor's width (W) must be significantly increased, which could lead to difficulties in fitting the transistor within the designated area or might result in a g_m that is excessively high.

To accurately estimate the required g_m it's necessary to repeatedly work through the device equations for drain current (Id), g_m, drain-source resistance (rds), gate-source

capacitance (C_{gs}), gate-drain capacitance (C_{gd}), along with the start-up criterion detailed in equation 3.16. This process should be based on the assumption that the MOSFETs are in saturation. The equations referred to are as follows:

$$gm = \frac{dI_{dsat}}{dV_{gs}} = k_p \frac{W}{L_{channel}}(V_{gs} - V_t) \tag{3.17}$$

$$W = \frac{gmL_{channel}}{k_p(V_{gs} - V_t)} \tag{3.18}$$

Model parameters like $L_{channel}$, V_t (threshold voltage), k_p, λ (channel length modulation), C_{ox} ($= \frac{t_{ox}}{\epsilon_{ox}}$) and G_{GD} (gate-to-drain capacitance per unit gate width) are determined from the Process Design Kit (PDK).

The iterative procedure assumes that the components are ideal and include just the tank losses represented by R. Since a greater g_m is necessary for the non-ideal condition, W should be adjusted per equation 3.18. This iteration process continues until convergence is reached. Once reached, tank's capacitance is adjusted to get the necessary f_{osc}, following equation 3.15. The mentioned technique is only an estimate, thus W and g_m may require further changes when using practical lower-level models.

3.2.1 Frequency Tuning

As shown in section 3.2, the inductance and capacitance of the LC tank circuit determine the output frequency of an LC-VCO. A range of output frequencies may be achieved by varying these variables. The comprehensive tuning range of LC oscillators must encompass two key components: PVT variations, which are limited to a few per cent, and the necessary operating frequency range. Given the challenges associated with tuning inductors, particularly in integrated circuits, the focus shifts to using varactor tuning.

Considering that the VCO has to cover a range of different frequencies, 867 to 869 MHz and 2.4 to 2.5 GHz, two different tuning techniques must be employed: Continuous Tuning (section 3.2.1.1) and Discrete Tuning (section 3.2.1.2).

3.2.1.1 Continuous Tuning

Since LoRa employs CSS modulation and similarly to other protocols provides dedicated frequency channels for communication where the user is allocated a channel at the beginning of every communication session. It is necessary to modify the Local Oscillator (LO) frequency to implement this allocation. The Synthesiser assigned to this configuration has to be able to smoothly transition between channels in the 867 to 869 MHz and the 2.4 and 2.5 GHz frequency bands.

As previously mentioned, to vary the capacitance in an LC-VCO, a common practice is to implement a varactor, which is a voltage controlled capacitance device. Changing the voltage varies the device capacitance, thus changing the VCO output frequency.

Reverse bias-configured pn-junction diodes are widely used varactors. Nevertheless, because of its small depletion capacitance, a diode varactor has a restricted tuning range. It also shows a non-linear relationship between the depletion capacitance and the control bias voltage. Additionally, the varactor diode's tuning range capacity is compromised by its inadequate quality factor which rapidly decreases as a forward bias approaches.

The MOS varactor, which can be used in both accumulation and inversion modes, offers an alternative varactor approach. More precisely, the I-MOS varactor in inversion mode is preferred due to its considerably wider tuning range compared to the D=S=B MOS varactors. This is because the I-MOS capacitor operates exclusively in strong, moderate or weak inversion regions, avoiding the accumulation region. It can be implemented in either p-channel (PMOS) or n-channel (NMOS) configurations.

For PMOS, the gate terminal voltage governs the capacitance, with the bulk terminal connected to the power supply voltage. In contrast, for NMOS varactors, the gate voltage determines the capacitance, and the bulk is connected to the ground. NMOS varactors have an advantage over PMOS varactors due to their lower parasitic resistance. However, they are more susceptible to noise induced by the substrate, as they cannot be implemented in a separate p-well [41].

Varactors operate in three regions: inversion (where I-MOS is exclusively active), depletion and accumulation, depending on the relationship between V_{BG} and $|V_t|$. The overall capacitance of the PMOS varactor is expressed as $C_{MOS} = C \cdot S$, with C representing capacitance per unit area and S the transistor channel area. The highest capacitance per unit area is achieved under strong inversion and accumulation conditions, where carrier flow is greater than in other zones [42]. Also

$$\text{in accumulation: } C_{MOS} = C_{ox} = \frac{\epsilon_0}{t_{ox}} WL = C_{max} \tag{3.19}$$

$$\text{in depletion: } C_{MOS} = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}} \approx C_{min} \ , \tag{3.20}$$

where $C_{dep} = \frac{\epsilon_s WL}{W_m}$ and $W_m = \sqrt{\frac{2\epsilon_s(2\phi_F + V_{SB})}{qN_{sub}}}$.

Recently, active varactors have been introduced to overcome the tuning range limitation in a passive varactor, however, they won't be discussed in this thesis.

Two competing factors affect the varactor capacitance choice. First, achieving a reasonable continuous tuning range is desirable to avoid a dead zone in the discrete characteristics. Secondly, to lessen the effect of noise on the control line, it is also preferred to maintain a moderate K_{VCO}, usually a few per cent of ω_0 per volt.

3.2.1.2 Discrete Tuning

Although continuous tuning can cover almost all the frequencies inside the desirable bands (cannot cover all the frequencies inside the 4.8 to 5 GHz band) it's not enough to change between those bands, 1.734 to 1.738 GHz and 4.8 to 5 GHz (frequencies are

doubled because of the reasons explained in section 3.1). To obtain such a wide variation it is necessary to employ switch capacitors or a CapBank.

The objective of the CapBank is to increase the VCOs' capacitance by activating different branches with specified capacitance values. In this specific design, one branch is designed to decrease the frequency from 5 GHz to 4.95 GHz, ensuring that the continuous tuning can encompass all frequencies within the band. Meanwhile, the other branches serve to reduce the frequency to the 1.736 GHz range. It can be stated that the switches are governed by a "thermometer" code with only 2 bits. As the number of 1s in the thermometer code rises, the load capacitance increases correspondingly.

The design of the switches requires particular attention, with due consideration for parasitic capacitances. Even when the switches are turned off, their parasitic capacitances load the tank. Additionally, even if the resistors employed in the selected topology do not compromise the Q of the oscillator, their noise does modulate the junction capacitances, consequently affecting the tank resonance frequency.

3.3 LC-VCO Design

This section presents the selected designs for the previously described VCO, utilising a CMOS 130 nm technology from United Microelectronics Corporation (UMC) with a 0.9 V supply.

3.3.1 LC-VCO

The first step in designing the VCO is to define a power budget, represented as P, which determines $I_{bias} = \frac{P}{Vdd}$ and a starting oscillation frequency. The maximum frequency of 5 GHz is considered in the design, albeit it will fluctuate depending on the control voltage. This choice is justified by the fact that, as previously mentioned, the VCO will operate at twice the frequency. In addition, if the varactors have the lowest capacitance in the design — as will be further discussed in section 3.3.2 — both discrete and continuous tuning techniques will only increase the circuit's initial capacitance, decreasing the frequency of operation.

Therefore, beginning with P = 1 mW[1] yields I_{bias} = 1.11 mA. It's important to note that because analog design uses an iterative process, these figures are just meant to be used as an early approximation and only via simulation where every variable is considered, can the final design be decided upon. Next, a value of $Q_L = 8$ was initially assumed at the frequency of 5 GHz. However, further testing of the inductor's quality factor, as shown in figure 3.4, reveals that it can achieve a quality factor of approximately 10.5 at 5 GHz.

By applying the formula $V_{tank} = I_{bias}R_p = I_{bias}\omega_0 L Q_L$, the value of the inductance L[2] is determined to ensure that V_{tank} reaches the minimum voltage swing necessary for the

[1] this power assumption is for the 5 GHz frequency; it will increase for the 1.738 GHz frequency

[2] values of L must be chosen such that it is in a practical value range to be fabricated as well as being at a value that results in a practical value of capacitance, C, for the varactor

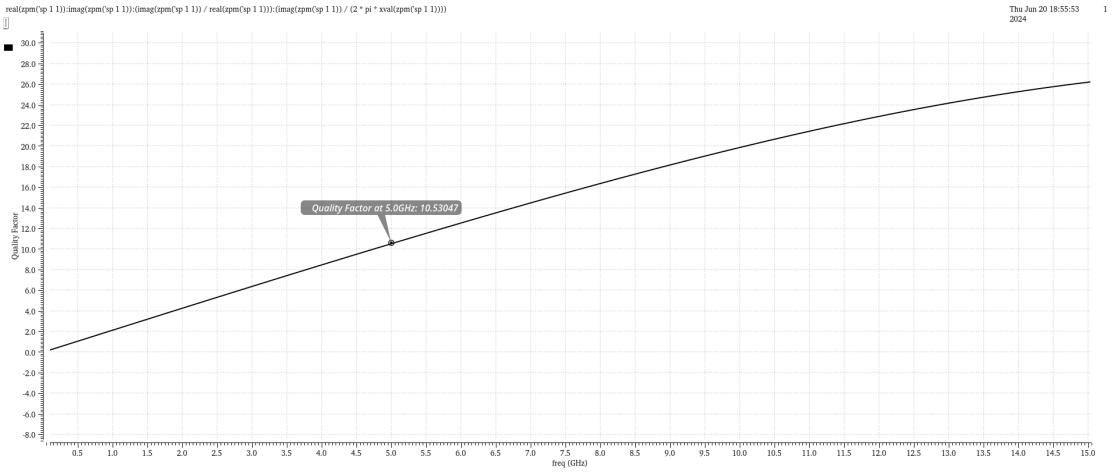


Figure 3.4: Quality Factor of the Inductor.

design. This approach sets L such that it aligns with the required operational parameters of the circuit. For the lowest phase noise, the swing is chosen as large as possible without driving the into the triode region, e.g. the peak-to-peak single-ended swing can reach V_{TH} [15].

Examining eq. 3.15 without factoring in the parasitic capacitances for simplicity in the initial design, where R_s was previously defined, provides the value of C for the LC tank with ω_0 set at 5 GHz. Now, by applying eq. 3.16 and considering $\alpha = 2$ in eq. 3.8, the minimum transconductance of each transistor is determined. Note that C will eventually encompass the parasitic capacitances of the inductor and the input capacitance of the subsequent stage.

Using equations 3.17 and 3.18, the value of W is determined by considering the transistors' minimal channel length to minimise their capacitance contributions. Since abrupt current steering is often preferred, wider transistors are chosen. Given the high frequency involved, RF transistors are chosen as they perform better in RF frequencies. Subsequently, transistor non-idealities are factored in to arrive at a new g_m and transistor width.

Lastly, a Basic Current Mirror is implemented into practice, using the previously established current as the reference, this current should be generated from a self-biasing circuit, which is independent of the power supply or temperature. The reference current is converted to voltage using a diode-connected transistor and this voltage is applied between the gate and the source of another MOSFET. By adjusting the $\frac{W}{L_{channel}}$ ratio of the two transistors as per equation 3.21, a current multiple of the reference current can be generated. It is crucial to ensure that the MOSFET operates in the saturation region. While a MOS transistor in cascode configuration could be used to achieve higher gain, this approach may encounter issues with headroom voltage.

$$I_D + \Delta I_D = \frac{\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)_{REF}} I_{REF}(1 + \lambda \Delta V_{DS}) \tag{3.21}$$

Figure 3.5 illustrates the design of the VCO, while table 3.1 presents the parameters of all components. Note that due to the circuit's symmetry, the values listed in table 3.1 pertain to just one side. Additionally, the depicted current is applicable for the 5 GHz frequency, with higher values anticipated for the 1.738 GHz frequency.

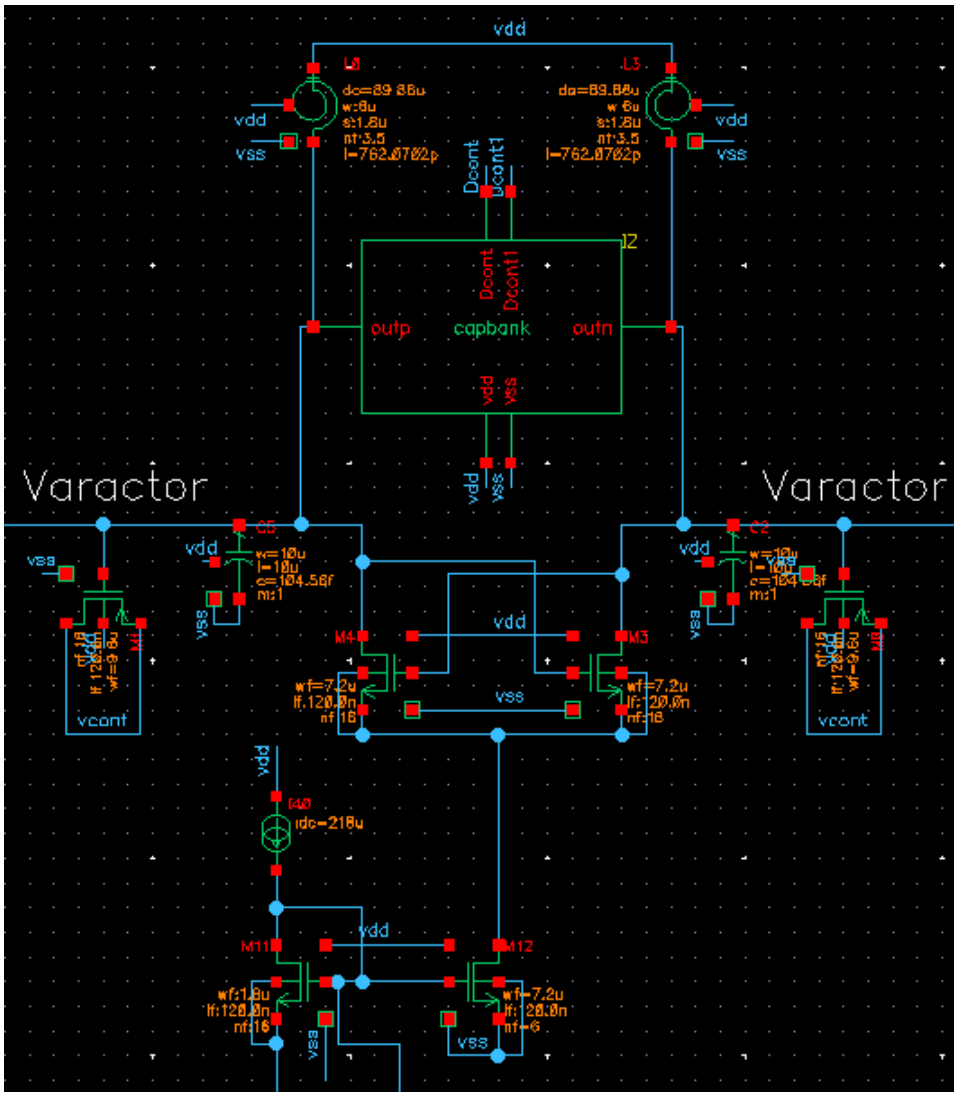


Figure 3.5: Schematic of LC-VCO implemented.

Table 3.1: LC-VCO parameters values.

	Wf	Lf	nf	I_D	gm	C	L
NMOS	7.2 μm	120 nm	16	1.80788 mA	26.9282 mS	—	—
CAP	—	—	—	—	—	104.56 fF	—
IND	—	—	—	—	—	—	759.9608 pH

3.3.2 Varactor

Section 3.2.1.1 explores various structures of MOS varactors, but this work focuses on implementing I-MOS varactors (this MOS transistor, also known as an I-MOS capacitor, only functions in the inversion zone). In this configuration, the drain and source are connected as one node of the varactor, while the gate serves as the other node. Additionally, the bulk is connected to the highest available voltage in the circuit (typically V_{DD}).

The decision to use I-MOS varactors was influenced by their significantly wider tuning range compared to D=S=B MOS varactors, as well as the nonlinear nature of both characterisation curves. However, it's worth noting that the transition of the I-MOS varactor from C_{min} to C_{max} is quite sharp [42].

Figures 3.5, 3.6 and 3.7 depict the two I-MOS varactors controlled by V_{cntrl} and their corresponding C-V curve. To minimise channel resistance and gate resistance, a minimum channel length of $L_{channel}$ = 120 nm is selected for the transistor.

As depicted in figure 3.6, the varactor was subjected to a voltage variation ranging from -2 V to 2 V. The plot illustrates that the capacitance fluctuates between approximately 180 fF and 580 fF. This implies that an increase in the control voltage will result in a decrease in the frequency of the VCO.

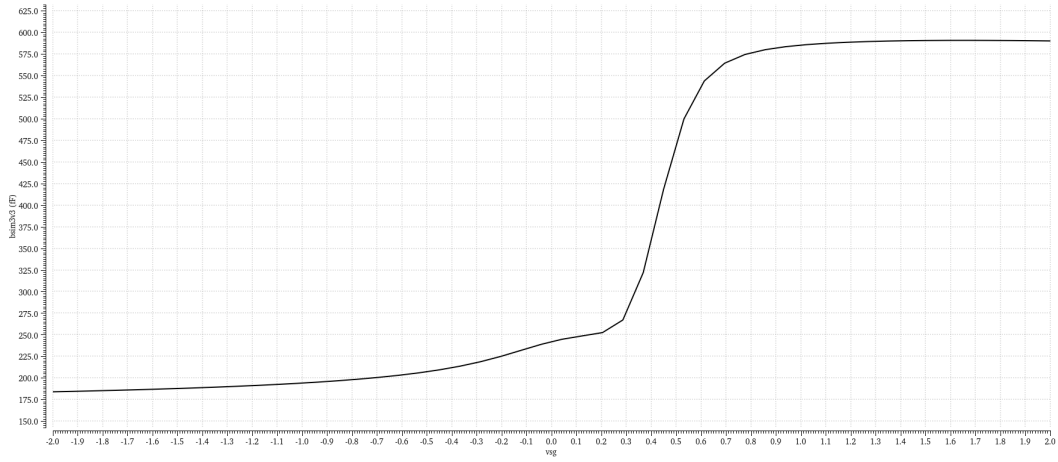


Figure 3.6: C-V curve of the I-MOS varactor from -2 V to 2 V.

However, the objective is to establish a linear relationship between the control voltage and capacitance. Since the voltage is contingent on the CP | LF combination, it cannot exhibit such variation.

In the present work, the tuning voltage is adjusted within the range of 25 mV to 875 mV, as illustrated in fig. 3.7. This range is chosen to match the voltage range of the CP | LF and leverage the sharp transition of the I-MOS, resulting in a capacitance spanning from approximately 240 fF to 580 fF. The frequency range achieved with this variation will be detailed in section 3.5 and quantified by the K_{VCO} parameter. Table 3.2 lists the sizes for the I-MOS varactors.

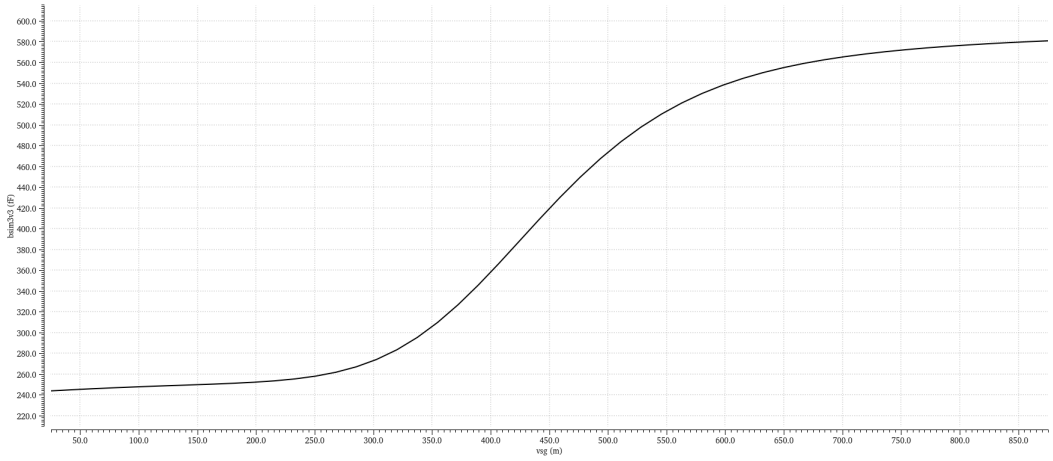


Figure 3.7: C-V curve of the I-MOS varactor in the range of interest.

Table 3.2: Varactor parameters values.

	Wf	Lf	nf	multiplier
PMOS	9.6 μm	120 nm	16	4

3.3.3 CapBank

As previously stated, covering the whole frequency spectrum — from 5.1 to 5.9 GHz to 1.734 to 1.738 GHz — is the key objective of this bank. In designing the capacitor bank, a common approach is to employ MOS switches to control the binary-weighted MIM capacitors. However, this setup comes with drawbacks, particularly concerning the resistance and parasitic capacitances of the switches. Capacitors C_1 never leave the circuit completely, as they are now in series with the switch's parasitic elements (C_{gs}) and (C_{gd}). This situation can potentially impact losses and the capacitance tuning range.

A simplified design of a coarse unit cell, consisting of two MIM capacitors differentially coupled by a series switch M_S, is shown in figure 3.8.

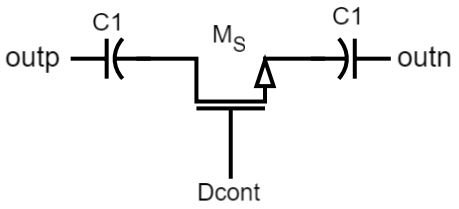


Figure 3.8: Basic schematic of a coarse unity cell.

Finding the best trade-off between losses and the tuning ratio $\left(\frac{C_{off}}{C_{on}}\right)$ is necessary when choosing values for the switch. Transistor M_S is turned on when the control bit is set to high, meaning $D_{cont} = V_{DD}$. Its resistance is regulated by its parameters, eq. 3.22.

$$R_{on} = \frac{1}{k_p \frac{W}{L}(V_{gs} - V_{th})} \tag{3.22}$$

The equivalent capacitance in this context is the series combination of the two capacitors labelled C_1. To evaluate the impact of losses, the quality factor of this configuration can be analysed using equation 3.23. Achieving higher Q requires minimising the on-resistance of the switch.

$$Q_{on} = \frac{1}{R_{on} C_{on} \omega} \tag{3.23}$$

There are two methods for reducing the NMOS's on-resistance. One way to reduce R_{on} is to modify the width and length parameters, which will lower the parasitic capacitance of the source and drain. Alternatively, maximising the gate-source voltage can also help minimise the on-resistance. To properly toggle the cell between its high and low capacitance states, two pull-down transistors are added (designated as M_{S1} and M_{S2}). In this setup, during the on-state, the internal plates of the capacitors are grounded.

Despite these adjustments, the parasitic capacitances to ground produce a slight decrease in the voltage swings at **outp** and **outn** when the switches are turned off. This occurs as the leakage currents of M_{S1} and M_{S2} discharge these nodes to the ground. The flicker noise generated by these transistors then contributes to significant phase noise, particularly because M_{S1} and M_{S2} have small dimensions and operate in the saturation region [15].

To address these issues, the design was revised, as illustrated in fig. 3.9. In this configuration, large resistors are used to connect the two nodes to V_{DD} when M_{S1} to M_S are switched off. These resistors do not degrade the Q of the oscillator but their noise modulates the junction capacitances of M_{S1} to M_{S3}, consequently affecting the tank resonance frequency [15].

The overall capacitance comprises the MIM capacitors and a small capacitance representing the switch in its off state. The minimum capacitance is attained when the switch is off.

The transistor sizes outlined in table 3.3 were selected with a focus on minimising the equivalent series resistance. Achieving a low series resistance entails using larger values for both width (W) and length ($L_{channel}$) parameters. However, this approach increases parasitic capacitances and occupies more area. To mitigate these effects, all transistors except MS are set to the minimum width.

The CapBank consists of a single tuning cell designed to cover frequencies within the 4.8 to 5 GHz range. Additionally, it employs a thermometer code logic, utilizing four

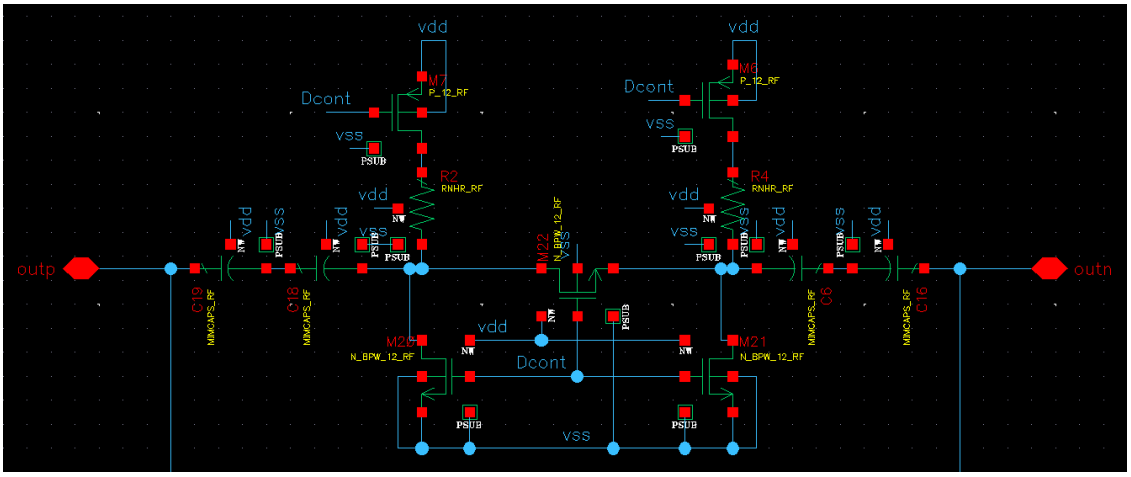


Figure 3.9: Final Design of the Discrete tunning cell.

tuning cells with equal capacitance values to address the lower frequency bands ranging from 1.734 to 1.738 GHz.

Table 3.3: CapBank component values.

	Wf	Lf	Nf	R	C
NMOS M_S	6 μm	240 nm	16	—	—
NMOS	900 nm	240 nm	16	—	—
PMOS	1.6 μm	240 nm	16	—	—
Resistor	—	—	—	10 kΩ	—
MIMCAP 1^{st} cell (each side)	—	—	—	—	79.96 fF
MIMCAP (each side)	—	—	—	—	2.20 pF

3.3.4 Buffer

The sine wave output of the VCO must be converted to make it more compatible with other PLL blocks that use square waves. Additionally, buffers are employed to isolate the VCO's output from other circuits with high input impedance and also, thanks to their voltage gain, they ensure rail-to-rail swings.

A buffer typically consists of two inverters. But in this instance, three inverters were included, as seen in fig. 3.10. Although it may appear that the signal will be inverted at the output, the inherent delay in each logic gate ensures that the signal is only slightly out of phase with the VCO output and not by a full 180°.

When designing the inverters several factors must be considered. Initially, their size will progressively increase, bolstering the buffer's driving capacity and enabling it to supply more current. This increment ensures efficient driving of heavier loads while preserving signal integrity.

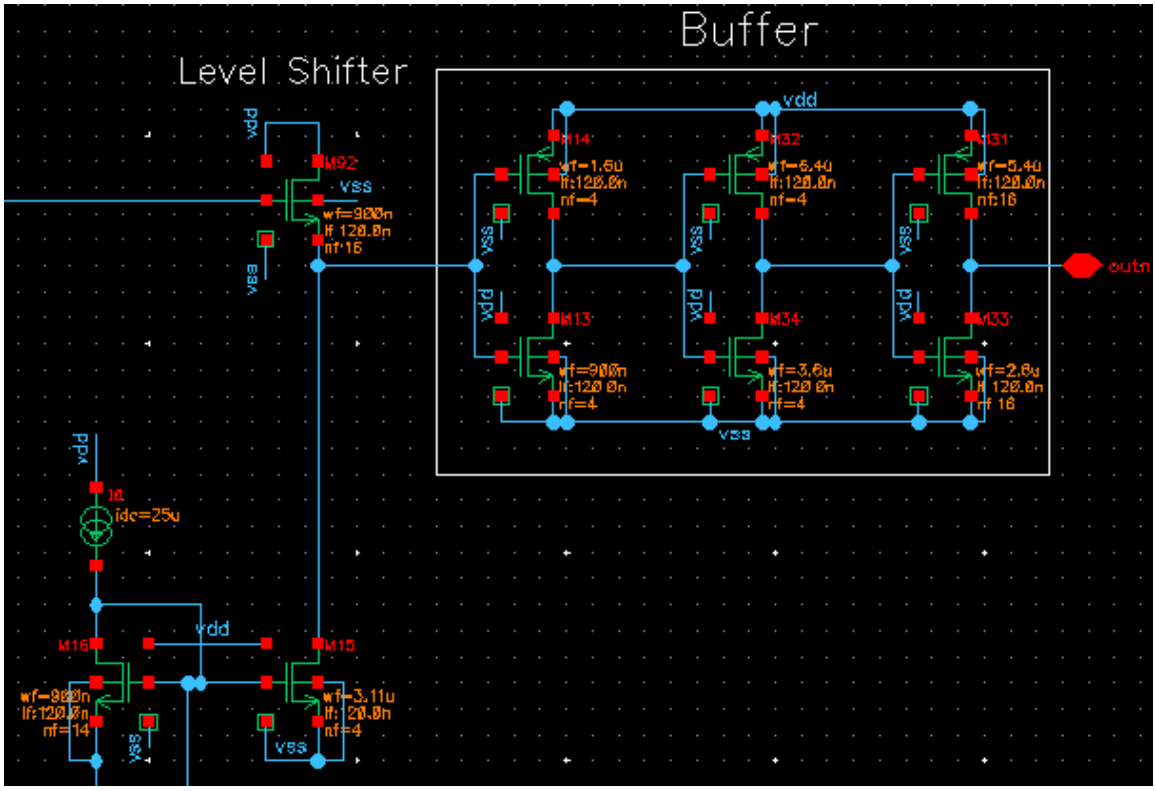


Figure 3.10: Buffer and Level Shifter Implementation.

However, the change in size also influences other key parameters:

- Propagation Delay: increasing the inverter size the delay is reduced;
- Noise Immunity: bigger inverters are more resilient to noise-induced voltage changes;
- Signal Integrity: reducing distortion or deterioration of the signal is necessary to maintain signal integrity. This feature aids in reducing the effects of parasitic resistance and capacitance;
- Power Consumption: although larger inverters consume more power, strategically increasing their size can optimise power consumption.

The behaviour of the inverter can be described as follows: the NMOS transistor turns off and the PMOS turns on when a low input voltage is provided to the inverter. This permits electrons to pass through the gate, raising the logic output voltage. In contrast, the NMOS transistor goes on and the PMOS switches off when a high input voltage is provided. This prevents electrons from reaching the output voltage and results in a low logic output voltage.

In the transition region, there's a switching threshold point where the output voltage equals the input voltage, known as the midpoint voltage or V_M. At this point, both the

PMOS and NMOS transistors are in saturation. The midpoint voltage V_M can be expressed as

$$V_M = \frac{V_{DD} - |V_{tp}| + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}, \tag{3.24}$$

considering that

$$\frac{\beta_n}{\beta_p} = \frac{\mu_n C_{oxn} \left(\frac{W}{L}\right)_n}{\mu_p C_{oxp} \left(\frac{W}{L}\right)_p} = \frac{\mu_n}{\mu_p}. \tag{3.25}$$

If $\beta_n \approx \beta_p$ and $V_{tn} = |V_{tp}|$ then the switching threshold $V_M = \frac{V_{DD}}{2}$. Resulting in the Voltage Transfer Characteristic curve shown in figure 3.11.

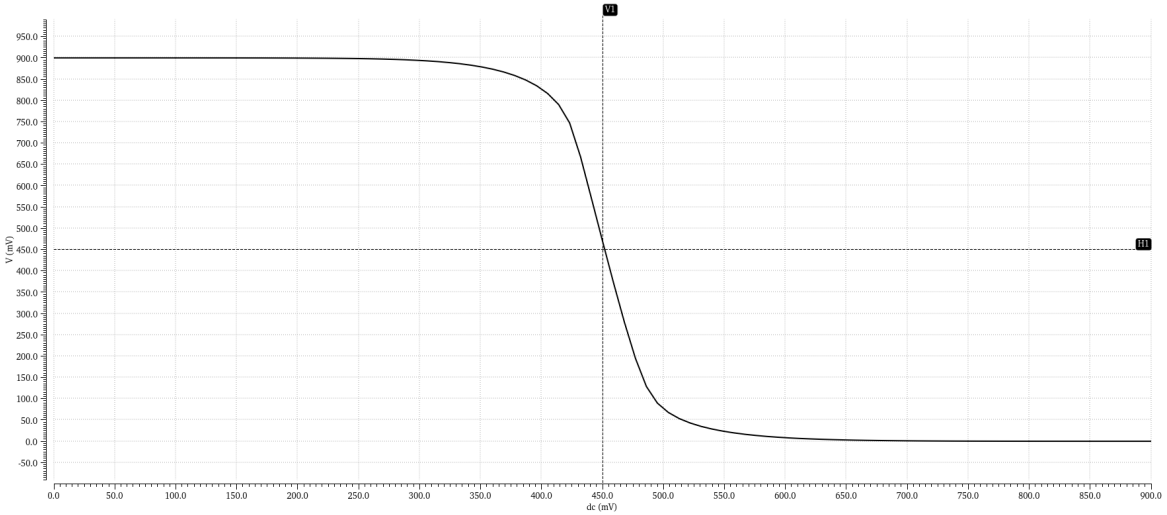


Figure 3.11: Inverter Voltage Transfer Characteristics.

However, the DC voltage output from the VCO is approximately 895 mV (due to the voltage drop in the inductor), which is not close to V_M. This misalignment necessitates the introduction of a level shifter circuit between the VCO's output and the buffer, as illustrated in figure 3.10. The purpose of this circuit is to translate signals from one voltage domain to another, effectively setting the DC level of the signal entering the buffer to 450 mV $\left(\frac{V_{DD}}{2}\right)$ or more precisely 406 mV, thereby making it suitable for the subsequent switching stage in the buffer.

The values of each component in the buffer and level shifter circuits are shown in table 3.4. It's worth noting that I_D is solely shown in the level shifter section, as it's the only component that requires biasing with an independent current source formed by the Basic Current Mirror.

Table 3.4: Buffer and level shifter component values.

	Wf	Lf	Nf	I_D
1^{st} Inverter PMOS	1.6 μm	120 nm	4	—
1^{st} Inverter NMOS	900 nm	120 nm	4	—
2^{nd} Inverter PMOS	6.4 μm	120 nm	4	—
2^{nd} Inverter NMOS	3.6 μm	120 nm	4	—
3^{rd} Inverter PMOS	5.4 μm	120 nm	5	—
3^{rd} Inverter NMOS	2.6 μm	120 nm	5	—
Level Shifter	900 nm	120 nm	16	308.989 μA

3.4 Phase Noise and Time Jitter

3.4.1 Phase Noise

Phase noise of a VCO plays a pivotal role in determining system performance in wireless communication systems. This is because the oscillator's phase noise directly influences the phase noise in the PLL, especially far away from the carrier frequency. Oscillator noise arises from amplitude and phase fluctuations in the signal, each contributing equally to the output power. Nevertheless, due to an amplitude limiting mechanism built into the VCO, amplitude noise can be substantially reduced. This allows for a focus primarily on the phase noise, as detailed in [43].

The output of an ideal oscillator is a perfect sinusoidal wave of frequency ω_0, which can be expressed as

$$V_{out} = Acos(\omega_0 t + \varphi) \, , \tag{3.26}$$

where A represents the amplitude and φ the phase. In the frequency domain, this corresponds to a Dirac impulse at ω_0, denoted as $\delta(\omega_0)$. However, in a real oscillator, noise induces fluctuations in both the phase and amplitude of the signal, leading to the following output:

$$V_{out}(t) = A(t)cos(\omega_0 t + \varphi(t)) \, . \tag{3.27}$$

Fluctuations in phase $\varphi(t)$ and amplitude A(t) mean that the output spectrum of the oscillator is not a single Dirac impulse. Instead, it displays sidebands near the oscillation frequency, as illustrated in figure 3.12. In well-designed, high-quality oscillators, amplitude stability is usually very high, allowing for the assumption that A(t) remains constant over time.

To measure phase noise, the power of the noise within a unit bandwidth at a certain offset frequency $\Delta\omega$ from the resonant frequency (ω_0) is taken into account. This power is then divided by the carrier power at ω_0. Following the definition provided in [44], this calculation results in a single-sided spectral noise density. This density is expressed in decibels relative to the carrier power per Hz (dBc/Hz):

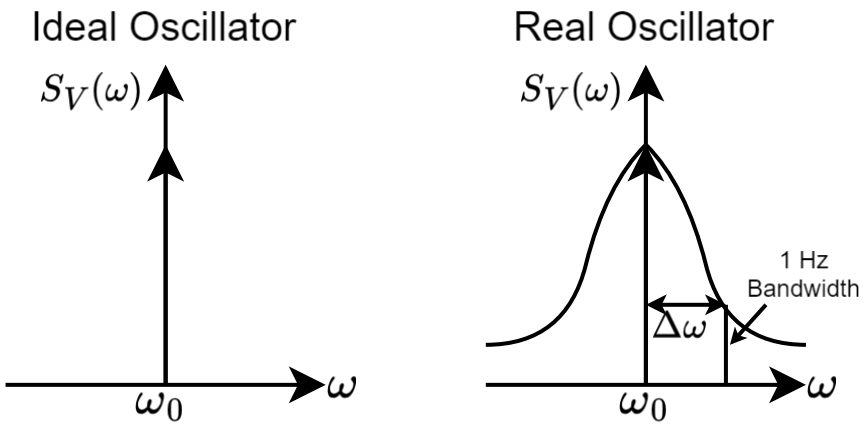


Figure 3.12: Spectrum of the signal around the oscillation frequency showing his sidebands and the phase noise at $\omega_0 + \Delta\omega$ (ω_0 = carrier frequency; $\Delta\omega$ = frequency offset from ω_0).

$$L(\Delta\omega) = 10\log_{10}\left(\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right) \text{ (dBc/Hz)} . \tag{3.28}$$

Various models have been developed to characterise phase noise in oscillators. Among these, the Leeson-Cutler model stands out as a significant framework for understanding single-sideband phase noise in oscillators. This model was first proposed by David B. Leeson in 1966 and has since been influential in the field [45] [46]. It assumes that the oscillator behaves like a Linear Time-Invariant (LTI) system concerning internal or external noise sources affecting output phase noise. The linear transfer function is used to determine the individual contribution of each noise source to the output.

Given an LC-VCO with thermal losses represented by R for C and L and a noiseless negative resistance maintaining the oscillation, the sole source of noise is the tank resistance's white thermal noise. The noise may be represented as a current source flowing through the tank, with its root mean square value determined by

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R} . \tag{3.29}$$

During the steady-state regime, with R = 0, oscillations are sustained by compensating for the positive resistance of the tank with a restoration element exhibiting negative conductance. The impedance of the parallel LC tank, when $\Delta\omega \ll \omega_0$, can be computed as

$$|Z_{tank}(\omega_0 + \Delta\omega)|^2 = \left(\frac{R\omega_0}{2Q\Delta\omega}\right)^2 . \tag{3.30}$$

It becomes apparent in this situation that the quality factor, Q, significantly impacts phase noise. The impedance of the tank at $\Delta\omega$ varies inversely with the square of Q and

the square of $\Delta\omega$. Equation 3.30 demonstrates a passband characteristic of $\frac{1}{\Delta f}$ centred on ω_0. The spectral density of the mean-squared noise voltage may be obtained by combining equations 3.29 and 3.30,

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f}|Z_{tank}|^2 = \left(\frac{4kT}{R}\right)\left(\frac{R\omega_0}{2Q\Delta\omega}\right)^2 = 4kTR\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 . \tag{3.31}$$

Equation 3.31 indicates that enhancing the quality factor can result in reduced phase noise. According to the Equipartition Theorem in [47], in equilibrium, the power of amplitude and phase noise are equal. Consequently, this noise power is evenly divided between amplitude and phase, resulting in

$$\begin{aligned} L\{\Delta\omega\} &= 10\log_{10}\left[\frac{\left(\frac{1}{2}\right)\frac{\overline{v_n^2}}{\Delta f}}{v_{sig}^2}\right] = 10\log_{10}\left[\frac{\left(\frac{1}{2}\right)4kTR}{v_{sig}^2}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] = \\ &= 10\log_{10}\left[\frac{2kT}{P_{sig}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \ (dBc/Hz) . \end{aligned} \tag{3.32}$$

In the equation 3.32 the $\frac{1}{\Delta\omega^2}$ characteristic arises from thermal noise filtered by the LC tank, resulting in a -20 dB/dec slope away from the carrier. Furthermore, the phase noise improves when the carrier power and quality factor rise. Nevertheless, tank thermal noise is responsible for only a fraction of the phase noise conundrum, as oscillator transistors also contribute their thermal noise and flicker ($\frac{1}{f}$) noise.

To comprehensively describe the phase noise, a more refined model is necessary. Leeson's model adjusts the previously derived expression to accommodate the high-frequency noise floor and $\frac{1}{f}$ noise upconversion. The formula representing the model is provided below:

$$L\{\Delta\omega\} = 10\log_{10}\left[\frac{2FkT}{P_{sig}}\left\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\left(1+\frac{\Delta\omega_{\frac{1}{f^3}}}{|\Delta\omega|}\right)\right\}\right] \ (dBc/Hz) . \tag{3.33}$$

In this context, L signifies the single-sideband phase noise density. F is an empirical fitting parameter that accounts for increased thermal noise, often termed the "device excess noise number". P_{sig} represents the average power dissipated in the resistive component of the tank circuit. k is Boltzmann's constant, while T refers to the absolute temperature in Kelvin. ω_0 denotes the oscillation frequency and Q is the effective quality factor of the tank, considering all loadings. $\Delta\omega$ stands for the frequency offset from the carrier. The term $\frac{\omega_1}{f^3}$ indicates the corner frequency between the $\frac{1}{f^3}$ and $\frac{1}{f^2}$ regions of the phase noise spectrum.

In line with Leeson's model, as the quality factor Q of the tank and the signal strength increase, the phase noise decreases. Moreover, Leeson's model incorporates a factor F. It is crucial to recognise that F is an empirical fitting parameter and, as such, must

be determined via measurements. This diminishes the predictive accuracy of Leeson's equation for true phase noise. Without a thorough understanding of the variables impacting F, it gets difficult to pinpoint certain approaches to diminishing it. Nevertheless, by increasing Q using this approach, F is simultaneously increased due to the introduction of noise by active devices. Consequently, the anticipated improvements in phase noise are unsuccessful [40].

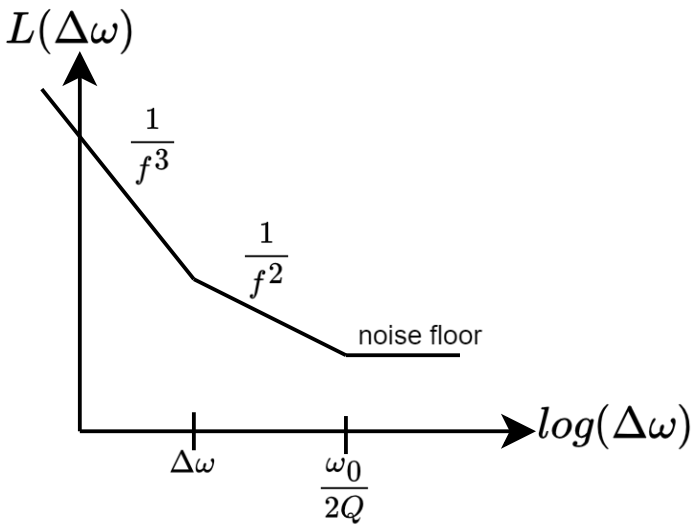


Figure 3.13: Asymptotic graphic of phase noise Leeson [47].

Figure 3.13 represents the phase noise L{$\Delta\omega$} of an oscillator, measured in dBc/Hz. The curve may be divided into several regions, where each region has a slope of $\frac{1}{f^n}$. At high offset frequencies, phase noise tends to level off, exhibiting a constant noise level or noise floor. However, at lower offset frequencies, the noise spectrum displays slopes characterised by $\frac{1}{f^3}$ and $\frac{1}{f^2}$ patterns. At very low offset frequencies, the noise spectrum becomes flat again, as detailed in [37].

In summary, the phase noise produced by a VCO is affected by a range of factors. These include the quality factor (Q) of the resonator, the Q of the varactor, flicker noise from active devices and noise from the power supply. By meticulously choosing the power supply, its contribution to the total phase noise of the system can be minimised. Therefore, the phase noise of the VCO is predominantly dictated by the overall quality factor (Q) of the circuit.

3.4.2 Time Jitter

Phase noise and jitter, though defined in the frequency and time domains respectively, both characterise the same underlying phenomenon.

Jitter refers to the deviation of zero crossings of a nominally periodic waveform from their ideal time points, resulting in small, rapid variations in the waveform due to

fluctuations in signal timing [15]. These variations can degrade system performance and arise from two main sources: deterministic sidebands and random phase noise. Random jitter is a broadband stochastic Gaussian process, often referred to as "intrinsic noise" because it is present in every system. In phase noise plots, the smooth sections along the bottom represent the intrinsic noise floor, indicative of random jitter. Conversely, deterministic jitter has a specific cause, is often periodic and narrowband, making it identifiable and correctable. It can be further classified as correlated or uncorrelated. Correlated jitter, which is deterministic, is always linked to and caused by a specific noise source. Uncorrelated jitter, on the other hand, is not statistically connected to any identifiable noise source.

Clock jitter is quantified by the following metrics:

- Absolute Jitter: defined as the phase difference between a noisy oscillator and a noiseless oscillator running at the same nominal frequency.
- Period (Cycle) Jitter: measures the difference between an observed clock period and the ideal or average clock period.
- Cycle-to-Cycle Jitter: measures the variation in duration between adjacent clock periods.
- Time Interval Error (TIE) Jitter or Phase Jitter: also known as accumulated jitter or phase jitter, is the actual deviation from the ideal clock period over all clock periods.

Given the relationship between phase noise and jitter, it becomes evident that specifying a peak-to-peak jitter value is impractical when dealing with random jitter, especially that arising from phase noise. This is due to the statistical nature of the variations. Instead, the root mean square (RMS) value is typically used to quantify the jitter. Equation 3.34 captures this relationship, with S(f) = 2·L(f), where L(f) represents the single-sideband phase noise.

$$J_{rms} = \frac{1}{2\pi f_{VCO}} \sqrt{\int S_{\phi}(f) df} \tag{3.34}$$

3.5 LC-VCO Results and Discussion

This section presents and discusses the simulated transient response and amplitude, tuning range and phase noise of the VCO design.

3.5.1 LC-VCO Transient Response and Amplitude

In figure 3.14, the transient behaviour of the LC-VCO is displayed, focusing only on its steady-state performance without illustrating the initial startup phase. Typically, in practical circuits, oscillations are initiated by ambient noise or external interference.

However, during simulations, oscillations may not commence unless disrupted by an external stimulus like a current pulse or a damped sinusoidal current. Once the oscillator reaches its steady state, the transistors function as commutating switches, effectively channelling the bias current into the resonant circuit. At this stage, the post-buffer VCO, produces outputs that are rail-to-rail but not exactly square waves. The output frequency, also depicted in fig. 3.14, registers around 5 GHz, corresponding to a control voltage (V_{cntrl}) of approximately 150 mV.

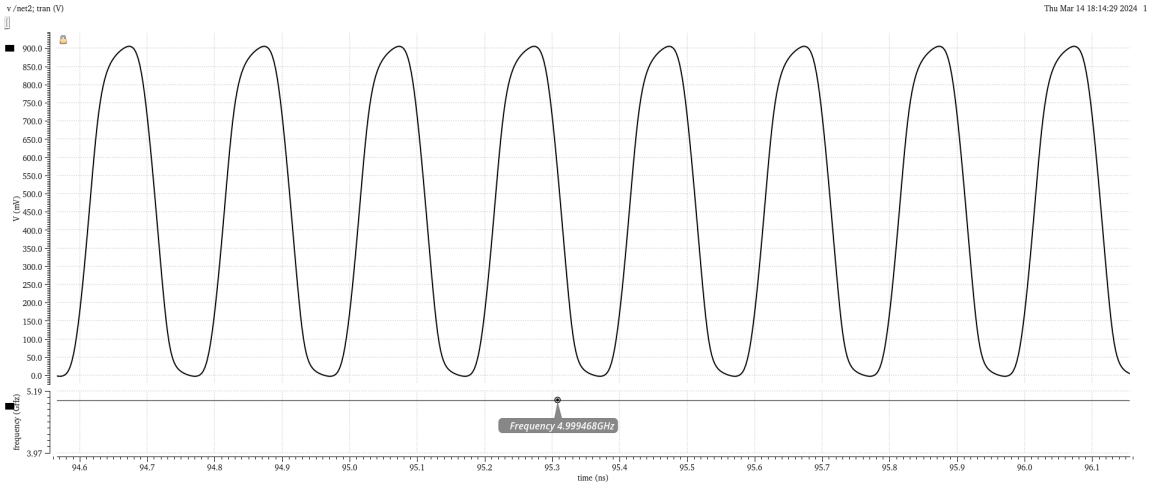


Figure 3.14: LC Oscillator - Output waveform and frequency of at V_{vcntrl} = 150 mV.

3.5.2 LC-VCO Tuning Range

A crucial parameter in a PLL's VCO is its gain (K_{VCO}), which ideally should be modest, amounting to just a few percent of ω_0 per volt. This helps in reducing the impact of noise on the control line. By adjusting the tuning range from 150 mV to 850 mV, the VCO demonstrates a K_{VCO} value of approximately 100 MHz/V. Note that with the implementation of the Quadrature Divider, this gain will amount to 50 MHz at the output of the PLL.

Figure 3.16 demonstrates the tuning range of the oscillator, showing a frequency shift from 4.93 GHz to 5 GHz when the V_{cntrl} is set at 150 mV.

Section 3.3 details the tuning range of the LC-VCO, including continuous and discrete tuning. The continuous tuning is achieved through K_{VCO}. Discrete tuning, necessary to span frequencies from 4.8 GHz to 5 GHz which continuous tuning alone can't cover, is displayed in figure 3.17. This is achieved by activating a stage of the capbank, as depicted in figures 3.17a and 3.17b. The results demonstrate that the VCO has a tuning range spanning from 4.81 GHz to 4.95 GHz, effectively covering almost all frequencies within the 2.4 GHz band. It's noteworthy that the VCO doesn't quite reach 5 GHz, due to the addition of more capacitors in the capbank and the increased capacitance from parasitics to encompass the lower frequencies. Furthermore, figure 3.17c demonstrates the VCO capability to function at a lower frequency range, namely at 1.736 GHz. More precisely, it

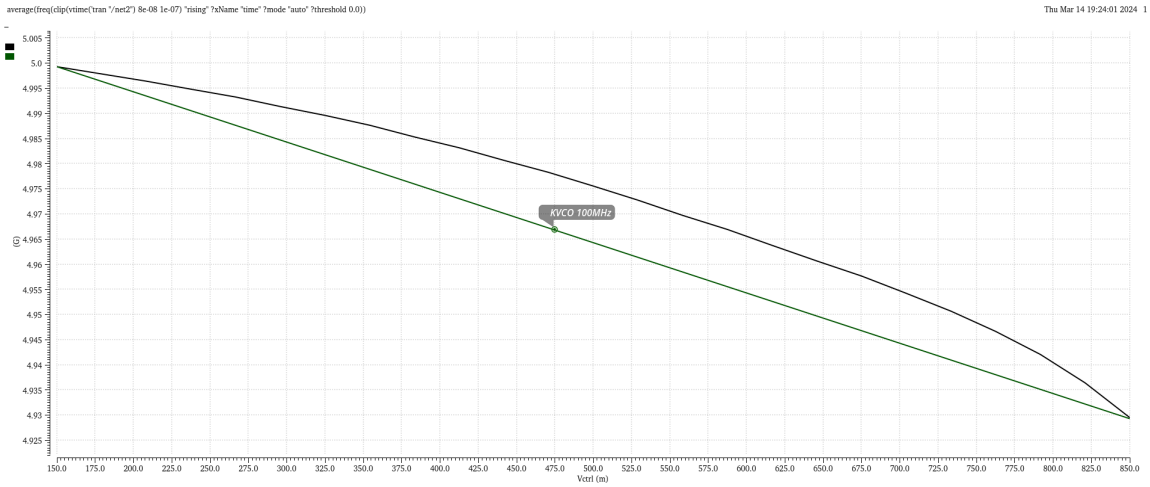


Figure 3.15: LC Oscillator - Oscillation frequency vs V_{vcntrl}.

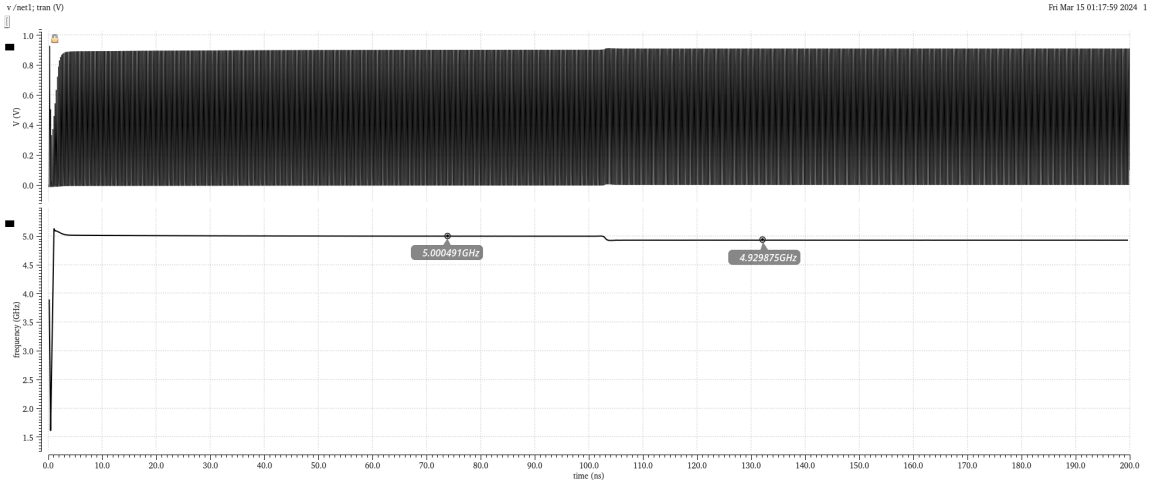


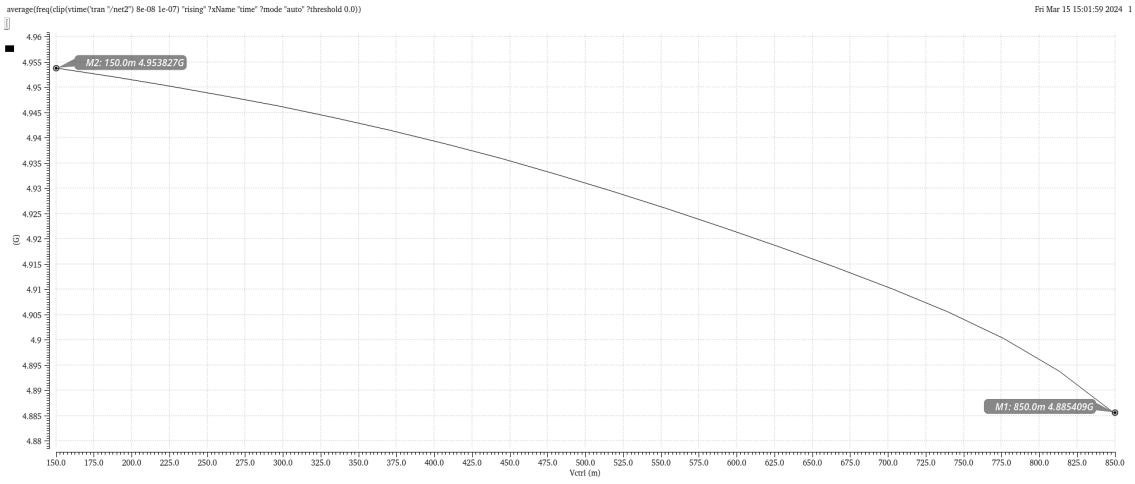
Figure 3.16: LC Oscillator Tuning range.

adjusts its frequency from 1.736 GHz to 1.739 GHz, effectively covering all LoRa channels inside the 868 MHz range. To achieve these lower frequencies, not only were more nodes activated in the capbank, but the current mirror of the VCO was also adjusted to supply 6 mA.

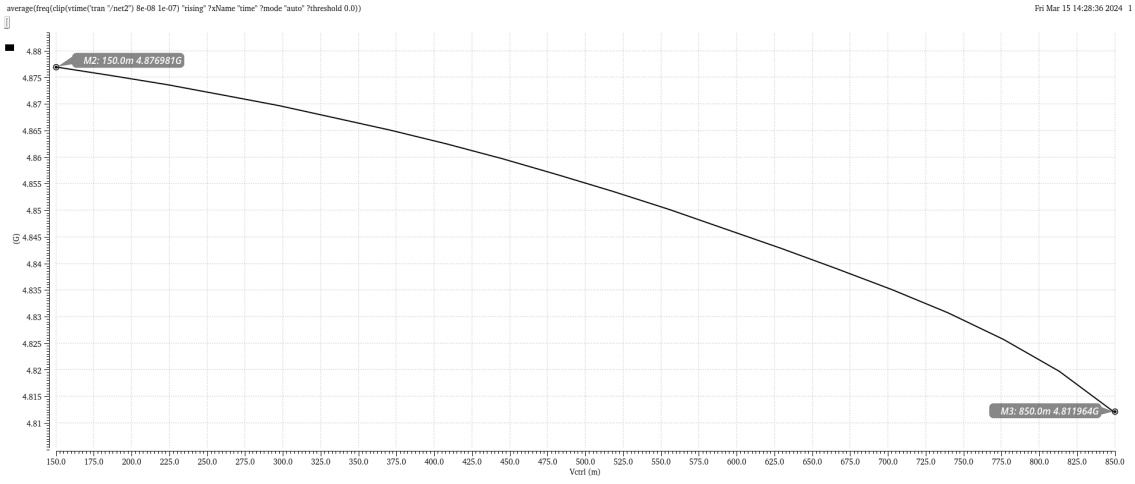
3.5.3 LC-VCO Phase Noise

Subsection 3.4.1 delves into the basics of phase noise. The phase noise characteristic of the LC-VCO is depicted in figure 3.18, where the simulation shows a phase noise slope of approximately -30 dBc/decade. This suggests that flicker noise is the primary noise contributor in VCOs, as illustrated in figure 3.13.

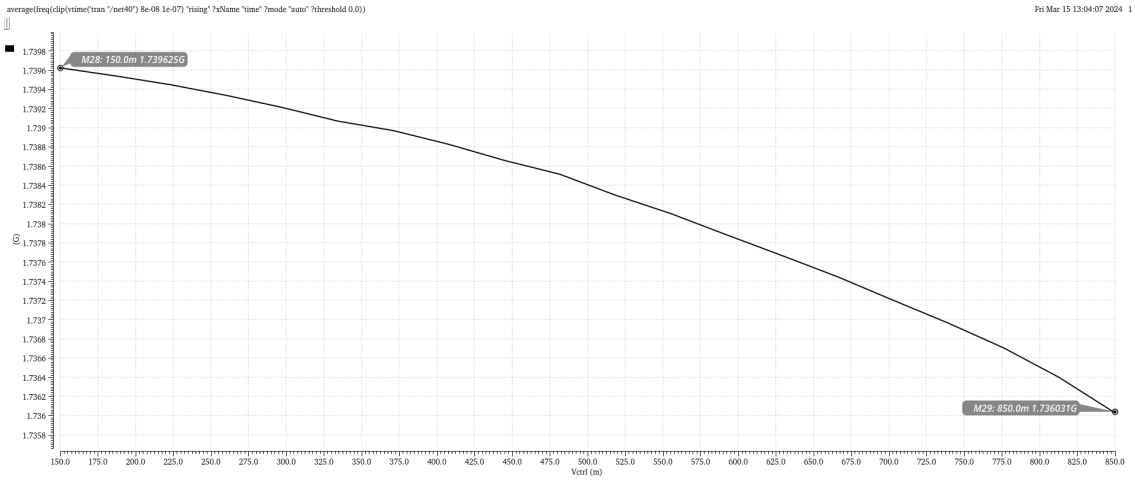
Efforts to mitigate tail noise, particularly flicker noise, involved a redesign of the current mirror in the LC-VCO schematic (figure 3.5). This was achieved by configuring transistor M_{11} as a series of 10 devices. Consequently, the effective length of M_{11} became 10 times that of M_{12}, leading to $ID_{12} = 4ID_{11}$. This substantial increase in M_{11}'s channel



(a)



(b)



(c)

Figure 3.17: LC Oscillator Discrete Tuning.

area significantly reduces its flicker noise. It is important to note that these 10 series devices function as a singular diode-connected transistor rather than employing a cascode topology as per [15].

This modification results in a final phase noise value at 1 MHz of approximately -103.11 dBc/Hz. Nevertheless, when compared to the theoretical value obtained from equation 3.32[3], around -123.6 dBc/Hz, a significant disparity is observed. However, it's important to note that equation 3.32 does not consider flicker noise, which, as evident in figure 3.13, is one of the main contributors. Additionally, only the quality factor of the inductor was included; yet, in reality, the quality factors of all elements degrade the total Q of the LC-VCO, decreasing the phase noise.

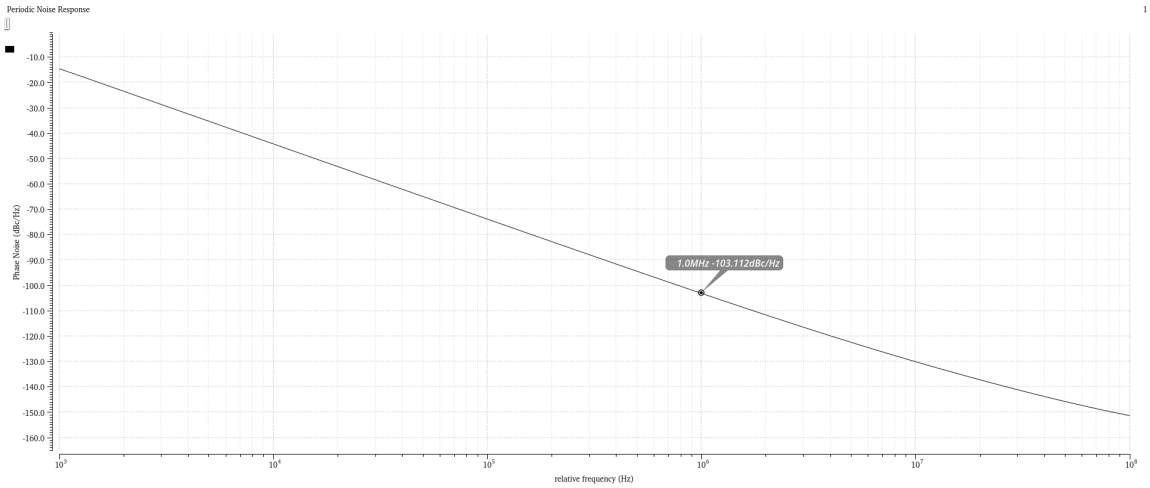


Figure 3.18: LC Oscillator Phase Noise with V_{cntrl} = 150 mV.

To ascertain the worst-case scenario regarding V_{cntrl}, phase noise was also plotted in fig. 3.19. While the value doesn't vary significantly, the highest phase noise, at -102.7337 dBc/Hz, occurs at a V_{cntrl} of 850 mV.

3.5.4 LC-VCO Jitter

Since the VCO is not driven by externally generated periodic signals, self-referred jitter metrics must be used in the absence of ideal reference transitions. This type of jitter is accumulating jitter, where each cycle's transition is influenced by the previous cycle's output, leading to the accumulation of jitter variance over time.

The accumulating jitter is computed using phase noise. As mentioned in subsection 3.4.2, RMS jitter, which naturally represents the unbounded probability distribution function of a random process, can be calculated from phase noise data using equation 3.34. The integration range depends on the application, typically stopping at $\frac{f_0}{2}$ to avoid capturing the carrier and its harmonics.

[3]Although equation 3.33 would provide a better estimate, it was not used since it requires an empirical fitting parameter that must be determined through measurements.

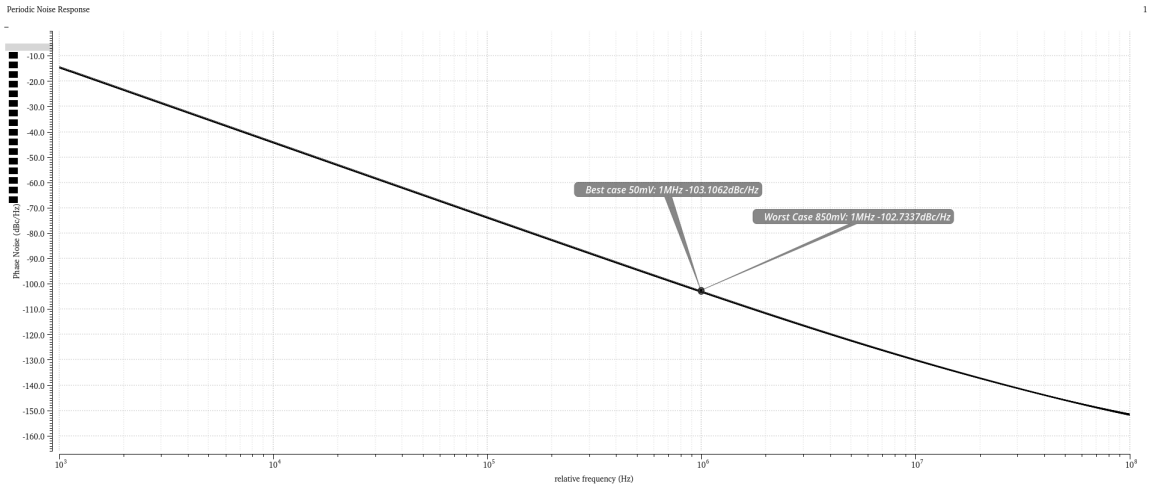


Figure 3.19: LC Oscillator Phase Noise for different V_{cntrl}.

Integrating over the interval from 10 kHz to 10 MHz results in an RMS jitter of 14.095 ps for a 5 GHz carrier.

Furthermore, cycle fm jitter was measured in a pnoise analysis, yielding an RMS value of 11.7515 fs with integration limits from 10 kHz to 10 MHz. To effectively combine random jitter with deterministic jitter, which is bounded, RMS jitter can be converted to a peak-to-peak bound under specific conditions. By assuming a finite allowable error, the jitter value beyond which errors are less probable than a defined limit, such as a bit error rate (BER), can be determined. For a Gaussian distribution of jitter, a scaling factor is used to convert RMS to peak-to-peak jitter, resulting in 72.6242 fs.

4

Phase-Frequency Detector

The design and simulations of a PFD, which includes the Charge Pump (CP) and Loop Filter (LF) are discussed in this chapter. An overview is presented, followed by a breakdown of the selected topology and the equations required to define the PFD behaviour.

4.1 PFD Characterisation

As mentioned, PLL operation necessitates phase and frequency detection. In instances where the frequency error is substantial, the Phase Detector (PD) output may not provide useful information but the Frequency Detector (FD) output does, effectively driving the VCO frequency towards the desired value. As $|f_{out} - f_{in}|$ diminishes, the PD starts generating a significant DC value, ultimately ensuring phase-lock and, consequently, $\omega_{out} = \omega_{in}$.

The operation of the Phase-Frequency Detector was detailed in section 2.2.2. But in essence, the DWN signal is set to Low and the UP signal is set to High if the reference clock speed exceeds the divider clock speed, and vice versa. It's crucial to emphasise that the UP and DWN signals are set to High when the reference and division clocks are synced. figure 4.1 shows the PFD state diagram, mentioned in section 2.2.2.

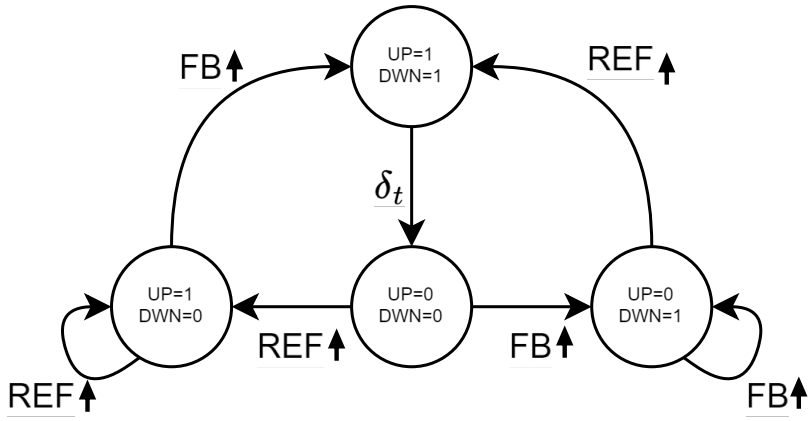


Figure 4.1: Tri-state PFD transition state diagram.

The PFD translates these phase and frequency differences into voltage signals in a linear fashion, and then the ideal average input/output ratio is expected to be

$$V_e = K_{PFD} * \phi_e \quad \text{where} \quad |\phi_e| < 2\pi \ , \tag{4.1}$$

K_{PFD} being the gain of the PFD.

Even though it was addressed previously, it is important to investigate the difficulties related to the PFD response when the phase error is small. Owing to the employment of actual components in the implementation of the PFD, the gates integrated into it introduce delays. So it's essential to ensure these components' delays are synchronised because any discrepancy results in a dead zone, highlighted in figure 4.2. A dead zone in a Synthesiser impairs the corrective capabilities of the loop, preventing the VCOs' control voltage from achieving the intended adjustments.

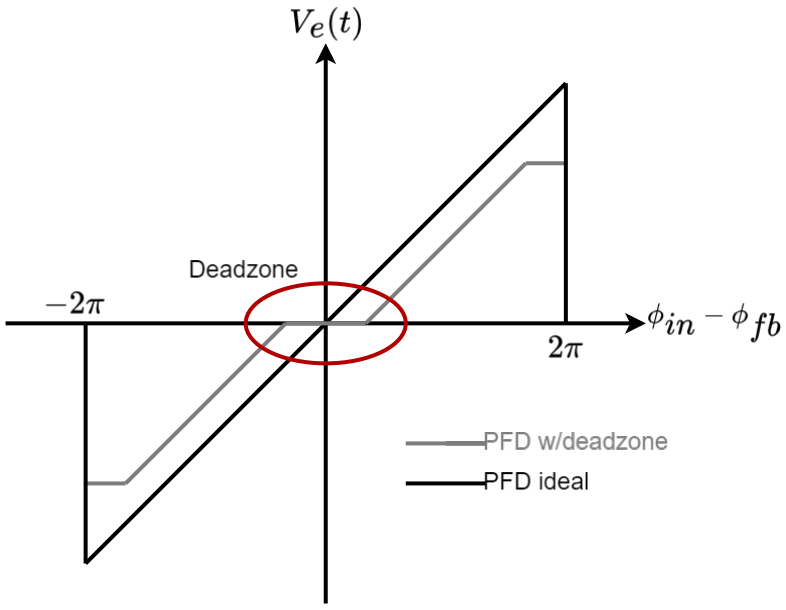


Figure 4.2: Transfer characteristics of an ideal PFD and one highlighting the Deadzone problem.

So PLLs must incorporate circuitry for dead zone elimination, ensuring that the Charge Pump is consistently activated for a certain duration to prevent operation within the dead zone [21]. In Frequency Synthesisers, eliminating the dead zone is crucial for accurate frequency synthesis and reducing phase noise. As mentioned, one commonly used approach to effectively address the dead zone issue is introducing a delay in the reset pathway.

The PFD produces DWN and UP outputs, which are non-complementary and remain high until reset by each other, enabling efficient detection of frequency variations. Both DWN and UP current sources are still active for T_{rst} even in a locked condition. As a result, current spikes occur on the CP's output at the reference frequency as it toggles on and off

(ideally with no net current provided to the Loop Filter). However, if the reset delay of the PFD is excessively prolonged, it may result in increased noise generation.

One important factor affecting the dead zone is the PFD reset path's delay, which must be carefully taken into account since it may cause problems close to 2π:

- During reset, the PFD cannot respond to input rising edges, such a scenario might skew the loop in the wrong way with the next rising edge;
- PFD's maximum operating frequency is determined by the reset delay, which may increase the acquisition time;
- Reset delay in the PFD can lead to the generation of inaccurate frequency information;
- PFD may be unable to acquire frequency lock if the reset delay difference takes up a sizable percentage of the reference cycle, which calls for a deeper look at the equations 4.2 and 4.3.

$$Max \;\; T_{rst} = \frac{T_{ref}}{2} \tag{4.2}$$

$$Max \;\; PFD \;\; Frequency = \frac{1}{2T_{rst}} \tag{4.3}$$

4.1.1 Charge Pump

Before the phase error to be effectively integrated with the VCO, it must first be encoded as the width of the UP and DWN pulses. Usually, a Charge Pump is used to complete this conversion. The CP converts the pulse-modulated phase error into a precisely specified charge by functioning as a three-position electronic switch that is governed by the three states of the PFD. In essence, it transforms the PFD's digital UP and DWN impulses into analog signals. Without going into current steering techniques, the CP can be realized using three distinct topologies: a source-switch Charge Pump, a drain-switch Charge Pump and a gate-switch Charge Pump [48].

In this work, a gate-switch Charge Pump was selected. This configuration successfully mitigates the problem of current spikes by maintaining the transistors in the current mirrors either in the off state or in saturation. Nevertheless, the inclusion of switch transistors connected to the gate terminals adds extra gate capacitance which limits the operating frequency range of the Charge Pump.

The phase error should ideally be zero after the PLL reaches lock which makes the width of the UP and DWN pulses go to zero as well, and the PFD|CP transfer function can be expressed as follows

$$K_{PFD} = \frac{I_{CP}}{2\pi} \, . \tag{4.4}$$

Sometimes the loop is unable to track minuscule phase errors because the CP's switches cannot respond to extremely short pulses. As previously shown, this region can be successfully closed off by appropriately delaying the reset signal route. This delay guarantees that the CP temporarily operates throughout each cycle by ensuring that the UP and DWN pulses have finite on-time during the locked situation.

Incorporating a delay introduces several drawbacks. Firstly, despite the CP outputting zero net charges in the locked condition, it generates noise during its brief activation. Additionally, inherent and external propagation delays within the reset path of the PFD impose a maximum operational frequency constraint, defined as $f_{max} = \frac{1}{2\delta t}$, where δt represents the total delay of the reset path. The difference in UP and DWN CP's currents is another important constraint on the PFD | CP. This discrepancy causes K_{PFD} to assume varying values depending on the polarity of the phase error, introducing a nonlinear parameter in the locked PLL transfer function.

Depending on the design, nonlinearities like current mismatch, leakage current and timing inconsistencies can cause various kinds of spectral distortions. Although these effects usually do not cause problems for the PLL as a whole, they frequently result in spectral purity being degraded at close-in offsets.

4.1.2 Loop filter

As detailed in chapter 3, VCOs are regulated by voltage rather than current. This requires the use of a device that can convert the current output from the CP into a voltage. This is usually accomplished by applying the charge generated by the CP to a capacitor's terminals, however, employing only a capacitor is insufficient since that would make the loop unstable because two integrators (two poles at the origin) provide zero phase margin. As a result, a combination of resistors and capacitors is usually used.

As detailed in section 4.1.2, the Loop Filter plays a crucial role in the PLL system, filtering out high-frequency noise originating from the PFD and regulating the loop's switching speed during lock, thus ensuring the stability of the PLL loop. Conventional PLLs often adopt a strategy of maintaining a constant and relatively conservative bandwidth in their Loop Filters to uphold loop stability amidst variations in process conditions or operating frequency, however, due to VCO noise, this approach typically results in inferior tracking jitter performance. To optimise the loop bandwidth across the entire operating frequency range, the loop gain needs to synchronise with the operating frequency. Furthermore, to maintain loop stability, the zero point of the LF must align with the operating frequency, this ensures a stable phase margin and a consistent scaling of the loop bandwidth with the operating frequency.

In this work, a second-order passive Loop Filter was utilised, as illustrated in figure 4.3, where C_1 is responsible for integrating low-frequency phase errors to determine the average frequency, thereby influencing the PLL bandwidth. The resistor (R), acting as the proportional gain, differentiates phase correction from frequency correction. Additionally,

it generates thermal noise, which the PLL then processes through band-pass filtering. The establishment of a zero frequency is essential for maintaining stability in the PLL.

Note that in figure 4.3, the resistor R is positioned above capacitor C_1. Theoretically, irrespective of the RC components' order, the LF preserves the same transient response and transfer function. However, changes in bottom-plate capacitance and switch resistance can affect the desired transfer function. The presence of bottom-plate capacitance introduces an additional high-frequency pole when the capacitor is positioned on top. Conversely, placing the resistor on top leads to heightened variability in switch resistance with fluctuations in the control voltage level.

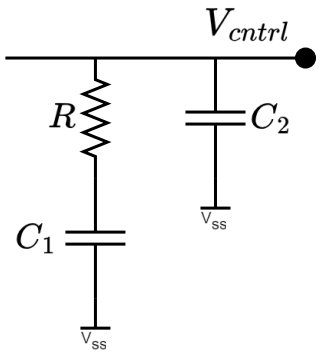


Figure 4.3: Second-order passive loop filter.

The purpose of the capacitor C_2 is to reduce control voltage ripple, however, it must not be excessively large to avoid loop instability. Typically, it is chosen to be less than $\frac{C_1}{10}$ for stability or greater than $\frac{C_1}{50}$ for reduced jitter. The selected value corresponds to $\frac{C_1}{5}$, which negligibly affects the loop settling time.

4.2 PFD Design

This section presents the design for the PFD, included in its design is the CP and the LF, utilising a CMOS 130 nm technology from United Microelectronics Corporation (UMC) with a 0.9 V supply.

4.2.1 PFD

The PFD operates as a sequential phase detector with a memory function so its circuit, depicted in figure 4.4, is comprised of two resettable D flip-flops where Inputs **ref** and **fb** function as the clocks of the D flip-flops along with a NAND gate and an inverter. Each latch consists of cross-coupled NOR gates with the output of each latch driving one input of the other. The inclusion of a NAND gate and an inverter contributes to a total delay of approximately five gate delays from **UPpfd** or **DWNpfd** through the reset loop [15]. This configuration effectively eliminates the dead zone.

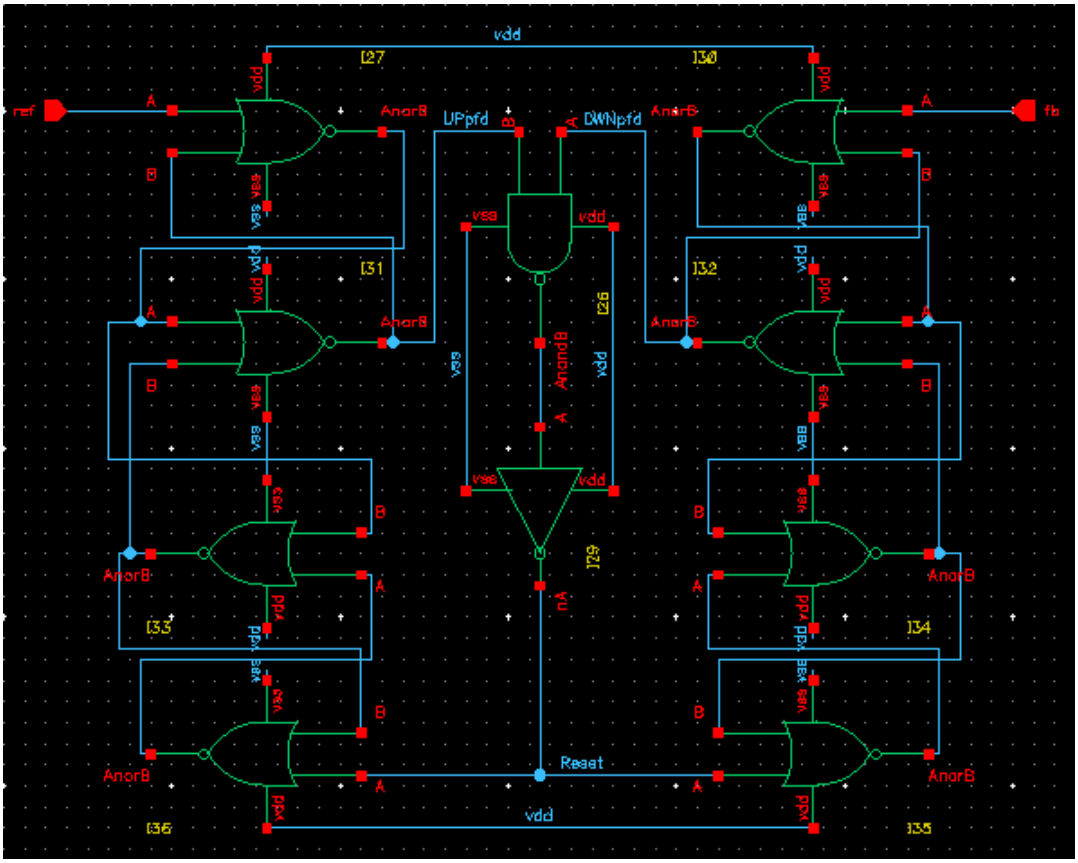


Figure 4.4: NOR PFD Implementation.

Figure 4.5 shows the transistor-level implementation for each of the circuits in figure 4.4 with the appropriate sizing, considering that $L_{channel}$ = 120 nm and W = 20 μm.

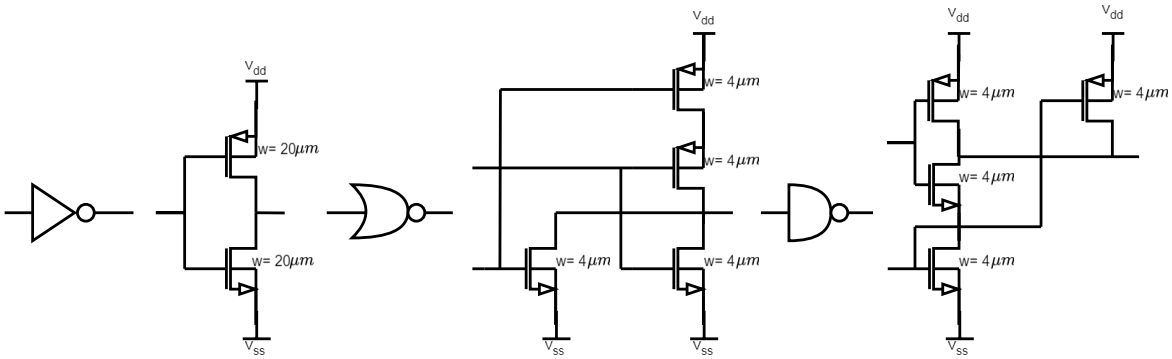


Figure 4.5: PFD Transistor Level Circuit Blocks.

The CP depicted in figure 4.6 requires UP and DWN pulses, as well as their complements. The PFD|CP interface setup includes a pass gate to synchronise with the delay of the inverter (I45), providing a first-order correction for the deterministic skew between the UP and DWN pulses as they reach the CP. The primary aim is to minimise skew between the current pulses as this reduces ripple in V_{cntrl}, rather than focusing on the skew between the UP and DWN pulses. Additionally, the final inverters act as buffers to

improve drivability.

All transistors are set to W = 4 μm and $L_{channel}$ = 120 nm, except for the last inverters, where W = 8 μm. To ensure alignment of the CP's up and down currents, especially considering the different capacitances seen at the inputs of the pass gate and inverter (I45), the initial inverters are also incorporated as buffers [15].

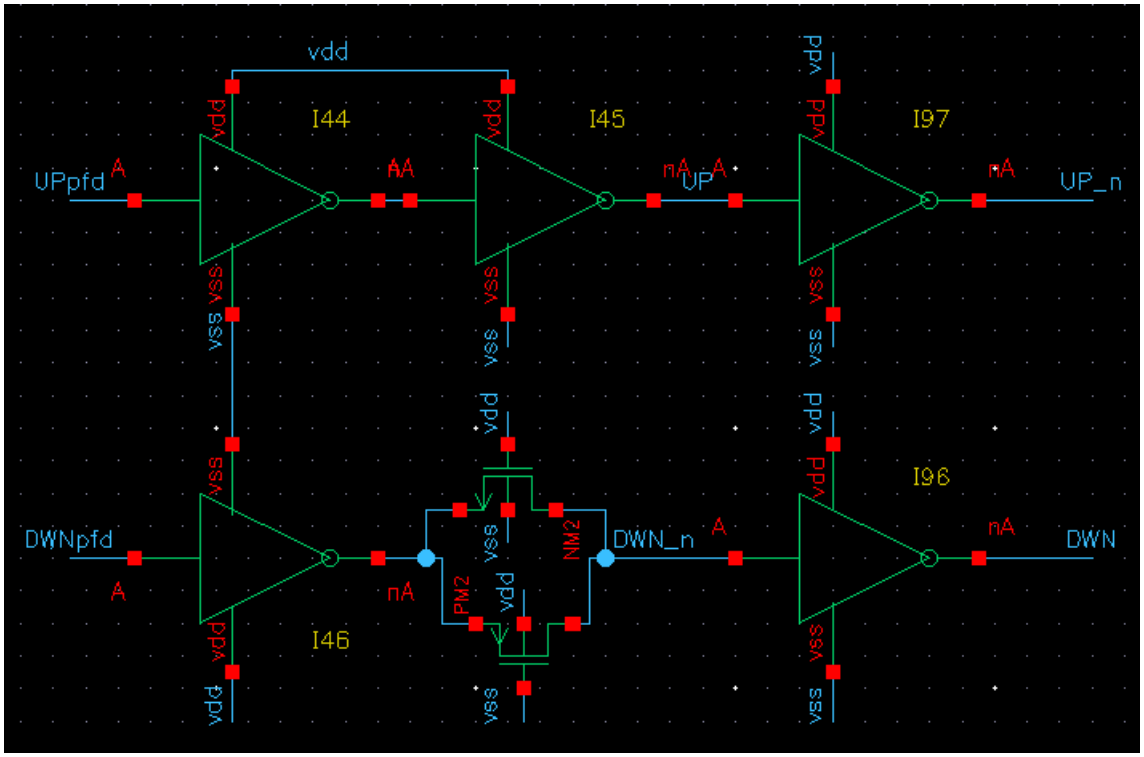


Figure 4.6: Interface between PFD and CP.

4.2.2 CP

Designing a Charge Pump poses challenges primarily due to concerns surrounding output voltage compliance, which defines the range of output voltage where the Charge Pump can operate while ensuring balanced up and down currents and channel-length modulation in the current sources. These factors often counterbalance each other. Drain-switched and Source-switched Charge Pumps face a decrease in voltage headroom due to the on-resistance of the switches, so Gate-switching is one strategy employed to mitigate this issue.

The topology depicted in figure 4.7 employs Gate-switching to control the current sources by connecting their gates either to a bias voltage or their source terminal. The output is tailored to accommodate a restricted voltage range, guaranteeing that the current source stays within the saturation region upon PLL lock. This is computed as V_{DD} - $|V_{DS_{PM2},min}|$ - $V_{DS_{NM2},min}$ = V_{DD} - $|V_{GS_{PM2}} - V_{TH_{PM2}}|$ - $(V_{GS_{NM2}} - V_{TH_{NM2}})$. Additionally, this structure eliminates charge sharing. However, the primary drawback of the Gate-switched CP is the skew between the up and down paths. Increasing the size of the CP transistors

might reduce the random mismatch between the up and down currents; nevertheless, it results in higher capacitances and related challenges.

Typically, the deterministic mismatch due to channel-length modulation is more significant than random mismatches. Its behaviour can be described as follows: PM2 is activated when UP decreases to V_{DD} - $|V_{TH_{PM2}}|$ - $|V_{TH_{PM4}}|$, while NM2 is triggered when DWN increases to $V_{TH_{NM2}}$ + $V_{TH_{NM4}}$. As a result, a notable discrepancy in the turn-on and turn-off timings exists between PM2 and NM2. The primary reason is that PM4 and NM4 have a low overdrive voltage, leading to high on-resistance. Consequently, I_{UP} and I_{DWN} exhibit significant misalignment and different peak values, even when the up and down pulses are aligned. Feedforward capacitors are added from UP and DWN (figure 4.7) to ensure that the voltages change in the same way as indicated by UP and DWN. This modification improves the alignment of the CP's currents [15].

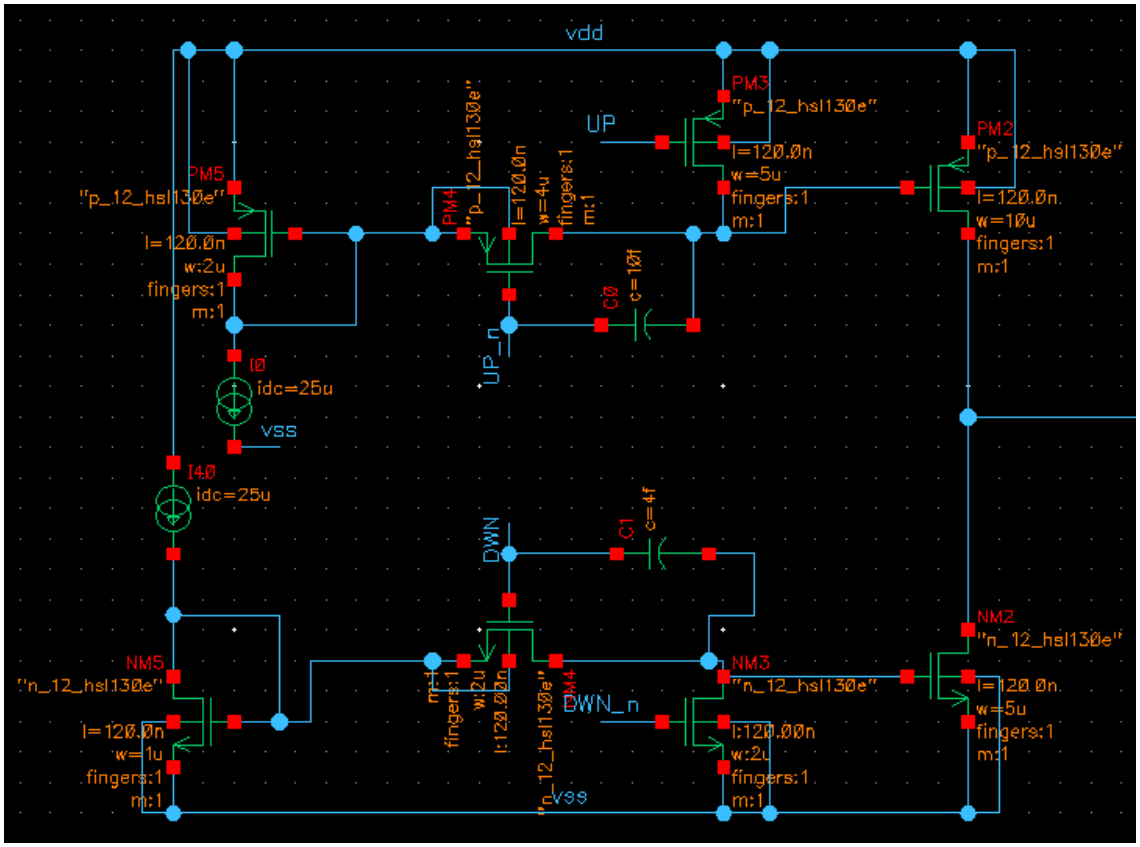


Figure 4.7: Switched-gate CP design.

The values of the CP's parameters are shown in table 4.1. For fast gate-switching, transistors with short-channel characteristics were chosen. Additionally, the capacitors depicted in figure 4.7, specifically C_0 and C_1, are Metal-Insulator-Metal Capacitors (MIM-CAPS), with C_1 being a combination of three capacitors in series.

Table 4.1: Charge Pump component values.

	W	L	C
PM2	10 μm	120 nm	—
PM3	5 μm	120 nm	—
PM4	4 μm	120 nm	—
PM5	2 μm	120 nm	—
NM2	5 μm	120 nm	—
NM3	2 μm	120 nm	—
NM4	2 μm	120 nm	—
NM5	1 μm	120 nm	—
C_0	—	—	20 fF
C_1	—	—	7.32 fF

4.2.3 LF

Designing the Loop Filter is an essential task since it greatly impacts the parameters of the PLL. Choosing component values for the LF requires careful consideration to achieve a compromise, since adding more poles and zeros to the loop transfer function may impact both the noise and dynamic behaviour of the loop [49]. Initially, Loop Filter component values are estimated through a series of calculations, as outlined in [50].

The schematic of the second-order Loop Filter is illustrated in figure 4.8 and table 4.2 presents its parameter values. These values are interdependent with parameters from other components of the PLL and significantly influence its performance. Therefore, their selection is deferred to section 6.2, where the PLL's loop responses are thoroughly analysed. In figure 4.8, resistor R_0 and capacitors C_1 and C_2 are shown; R_0 is an p-implanted polysilicon resistor without silicide (RNPPO) connected in series, while C_1 and C_2 are Metal-Insulator-Metal Capacitors (MIMCAPS) arranged in parallel to increase capacitance.

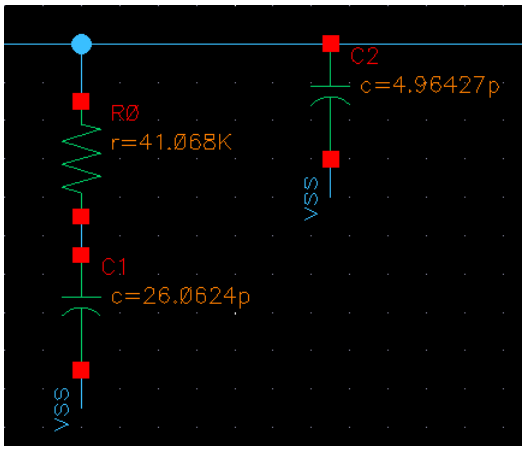


Figure 4.8: 2^{nd} order Loop Filter Implementation.

Table 4.2: Loop Filter component values.

	R	C
R	37.7905 k	—
C_1	—	28.8546 p
C_2	—	5.3779 p

4.3 PFD Results and Discussion

This section presents an overview and analysis of the simulated transient response of the PFD. The complete transient response analysis of the PFD is not included, as accurate results require the PFD circuit to operate within a closed loop. In an open-loop configuration, the CP tends to stabilise at either V_{DD} or V_{SS}. The results for the Loop Filter are exclusively provided in section 6.2.

4.3.1 PFD Transient Response

Because the simulation is conducted in an open loop, the PFD and CP are analysed independently.

4.3.1.1 Phase Frequency Detector

The functioning of the PFD was previously discussed in section 2.2.2. The output waveform illustrated in figure 4.9 corroborates this explanation. This depiction shows the reference signal trailing the feedback signal by 25° or 1.79 ns at a frequency of 38.75 MHz. Consequently, when the reference lags, the DWN pulses rise, activating the DWN switches. It's important to note that, as shown in fig. 4.4, the UP signal in this scenario exhibits spikes. These spikes transfer the pulses to the switch Charge Pump, causing fluctuations in the current. The duration of these spikes is equivalent to the reset time and likely to induce glitches in the control voltage.

When the reference signal leads by 25° or 1.79 ns at a frequency of 38.75 MHz, as shown in fig. 4.10, the opposite occurs. Additionally, it's important to observe that as the phase difference grows, the pulse width of the UP signal also increases.

4.3.1.2 Charge Pump

To expedite the gate waveforms, as shown in figure 4.11, feedforward capacitors were introduced, leading to a more synchronised alignment of the UP and DWN currents, as depicted in figure 4.12. The gain of the PFD (K_{PFD}) is influenced by the Charge Pump's current, which is set at 125 μA.

Even in a locked state, the PFD exhibits minor spikes, as demonstrated in the gate voltage waveforms in figure 4.11. This is further confirmed by the contrasting currents in figure 4.12, where one current feeds into the Loop Filter and the other is extracted

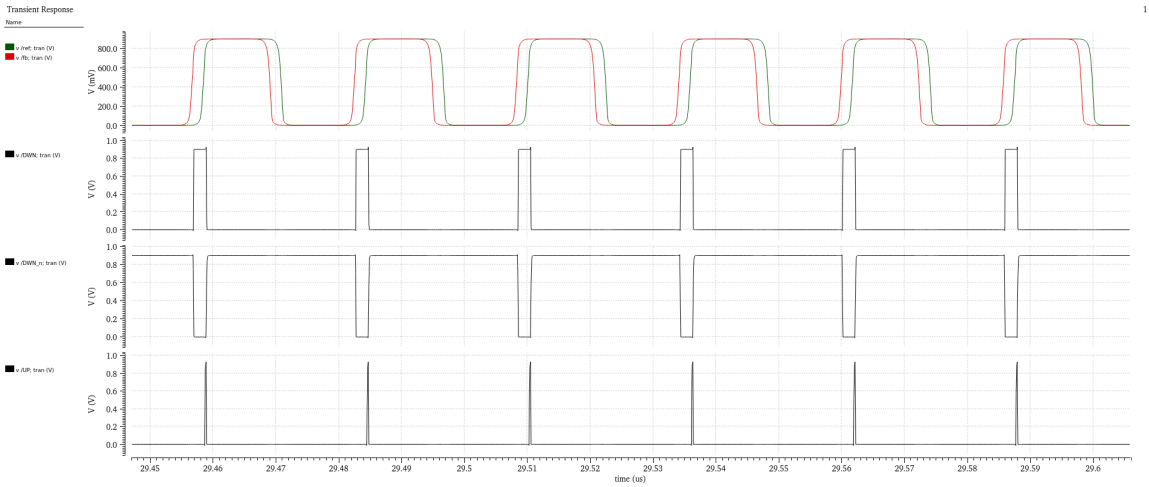


Figure 4.9: Output Waveform when the reference signal lags by 1.79 ns.

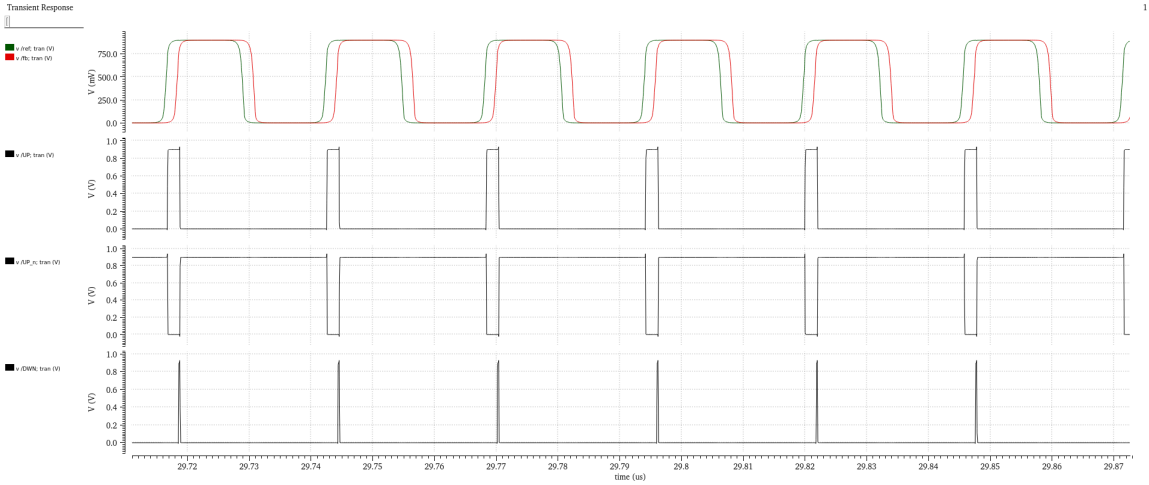


Figure 4.10: Output Waveform when the reference signal leads by 1.79 ns.

from it. A short transition, induced by the reset delay, leads to leakage current in the CP, affecting the stability of V_{cntrl}. The extent of this leakage current, approximately 8.397 μA or 6.7% of I_{CP}, is well depicted in figure 4.12. As noted in the research [51], the magnitude of this leakage could be sufficient to cause a phase offset of up to 0.42 rad, potentially exacerbating reference spurs in the PLL's output. Where the phase offset is

$$\phi = 2\pi \frac{I_{leak}}{I_{CP}} \ . \tag{4.5}$$

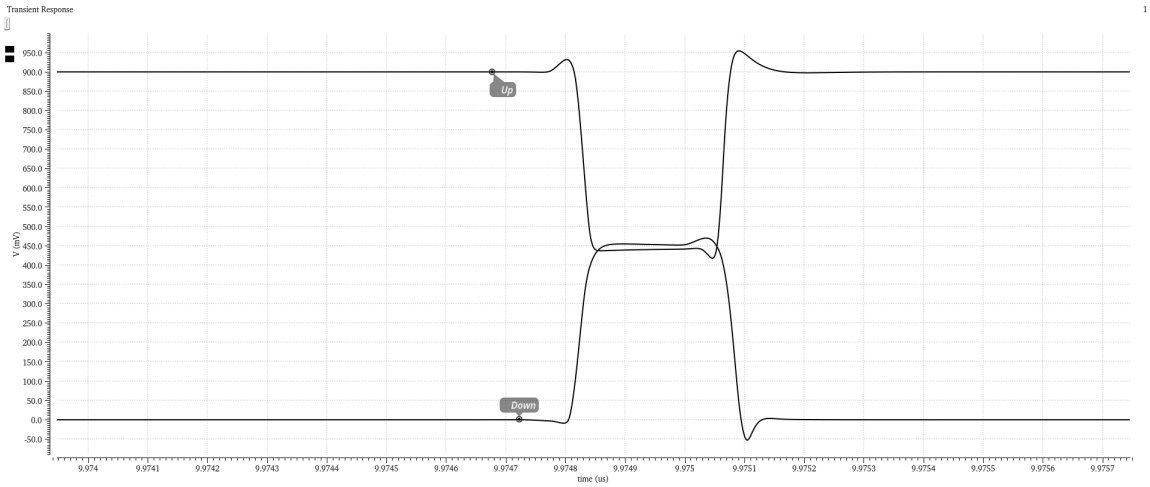


Figure 4.11: Gate Voltages waveforms.

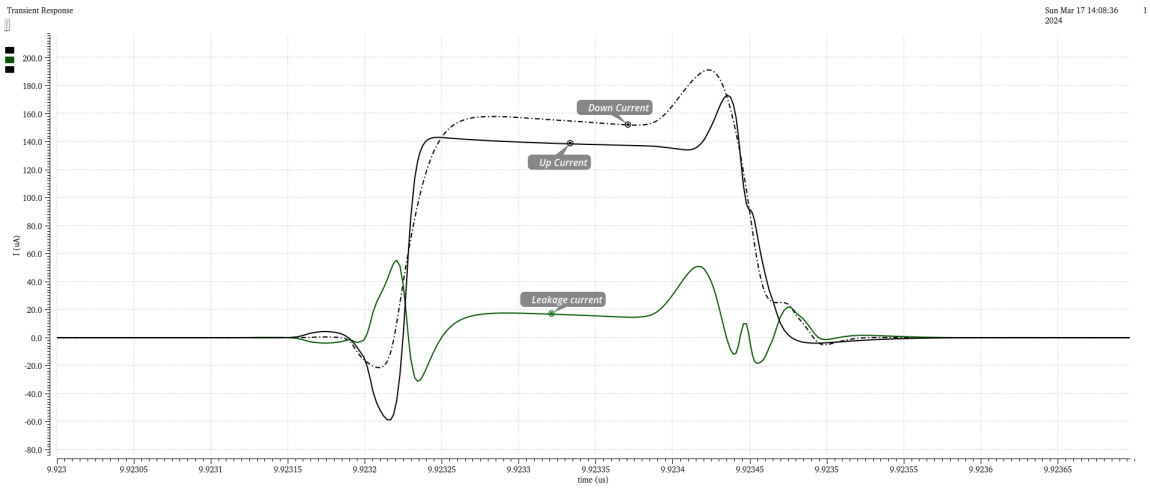


Figure 4.12: Up and Down currents with Leakage current.

5

Frequency Divider

This chapter covers the design and simulation of a Frequency Divider. After an overview, the chosen topology is laid down and the equations needed to define the Divider behaviour are provided. As previously noted, the VCO operates at twice the required frequency, necessitating a 2-Divider in its output within the PLL. Based on the rationale outlined in section 3.1, a Quadrature Divider will be employed for this purpose.

5.1 Frequency Divider Characterisation

As described in section 2.2.1, a Crystal Oscillator establishes the PLL reference clock. These crystals usually function in the 13 to 55 MHz range. Nevertheless, as mentioned in section 3.2.1.2, the VCO works at frequencies between 1.734 and 5 GHz (not covering all these frequencies). A Frequency Divider is used to ensure that the PFD is operating properly. As stated in section 2.2.4, these dividers modify the VCO frequency to match the reference frequency.

Frequency Dividers are typically characterised by four main parameters, according to [15]:

- Divide ratio;
- Maximum allowable input frequency (f_{max});
- Power dissipation;
- Minimum allowable input voltage swing, also referred to as "sensitivity".

Despite being essential, phase noise in Dividers is frequently seen as insignificant as most Divider topologies prevent phase noise from building up around their feedback loop. Rather, they have a phase noise profile akin to that of delay lines. To minimise any risk to the system as a whole, Dividers are usually designed with a maximum input frequency (f_{max}) that is far higher than the required value. Supply noise from Dividers, however, needs to be carefully managed since it might cause spurs [15].

Given that the Divider is dimensionless in the PLL linear model, the time-domain model can be formulated as

$$\omega_{fb}(t) = \frac{1}{N}\omega_{out}(t) \tag{5.1}$$

$$\phi_{fb} = \int \frac{1}{N}\omega_{out}(t)dt = \frac{1}{N}\phi_{out}(t)\ . \tag{5.2}$$

5.2 Frequency Divider Design

The design for the Frequency Divider is shown in this section. It uses a 0.9 V supply and CMOS 130 nm technology from United Microelectronics Corporation (UMC).

Most Frequency Dividers use D latches, which may be static or dynamic. In this thesis, a dynamic latch topology is selected, because dynamic latches store states on device capacitances instead of using back-to-back amplifying stages, so they typically involve fewer transistors compared to static latches and generally offer a more favourable trade-off between speed and power consumption. However, due to device leakage, dynamic latches may lose their states if the clock frequency is not sufficiently high. Therefore, they impose a lower bound on the operating frequency [15].

The present thesis looks into a straightforward and efficient dynamic logic design technique called *True Single-Phase Clocking* (TSPC) [52]. TSPC circuits were created to replace complementary clocks and provide faster speed and lower power consumption than C^2MOS (clocked CMOS) circuits. The TSPC dynamic logic style offers several advantages, including reasonably fast operation, compact size and the absence of static power consumption, moreover, it requires only one phase of the clock for operation. However, it also comes with some drawbacks, as signal propagation through three gates per input cycle can introduce delays. Additionally, full-swing CMOS inputs are necessary and the dynamic flip-flop may fail at low frequencies, particularly in test mode, due to leakage as different nodes are left floating during different clock phases and output states. These implementations are unrationed; however, a modified version of TSPC logic uses ratioed devices to improve speed, although this comes at the cost of static power. The schematic shown in fig. 5.1 removes the stacked transistors in the last two stages [53].

The ratioed TSPC circuit shown in figure 5.1 behaves as follows: when the signal CK is high, the first stage operates in the sense mode. Simultaneously, the second stage keeps node B low, where B represents the node connecting the second and third stages, while the output Q retains its current state. If both M16 and M0 are active, M16 must be powerful enough to prevail over M0. When CK decreases, B matches A, where A is the node linking the first and second stages, and Q matches B, which equals A if M17 is stronger than M15. The second and third stages draw a constant current in the first and second modes [15].

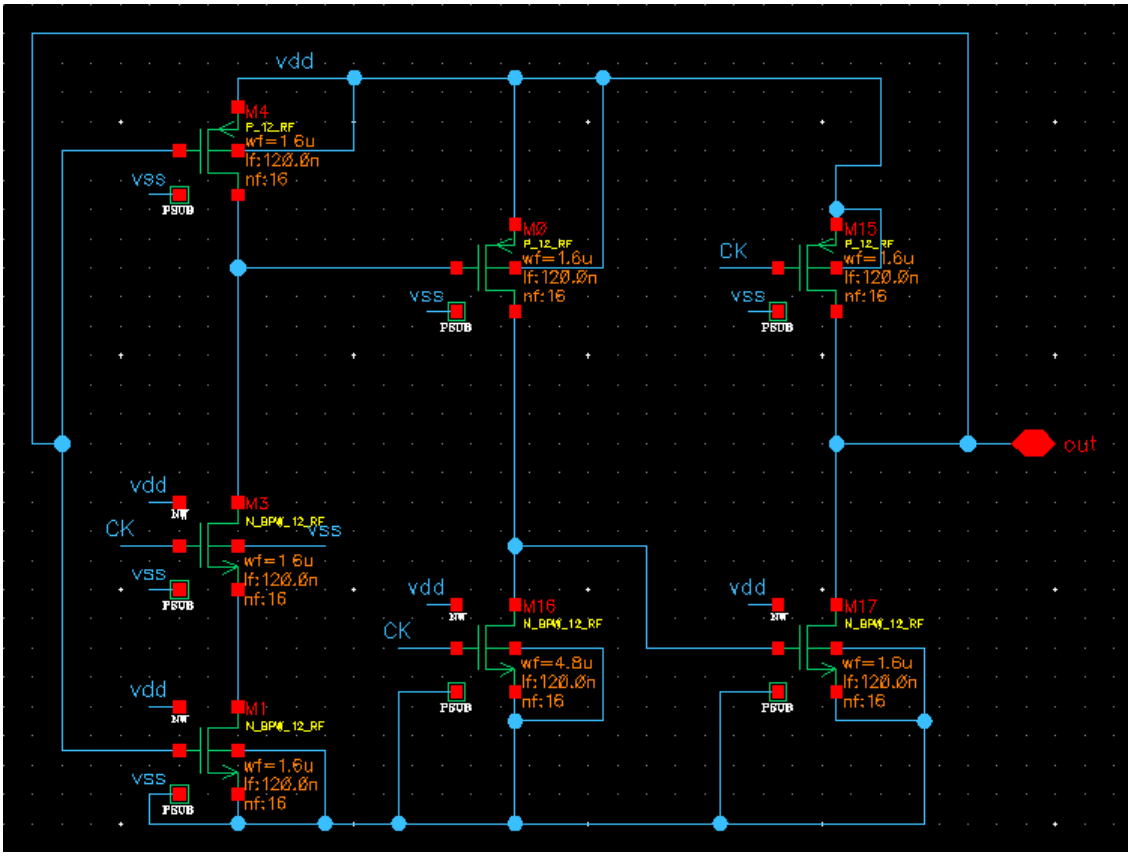


Figure 5.1: Divider by 2 circuit Implementation.

Typically, the transistors have the same width, except for $M16$, which should be two to three times wider for optimal speed [15]. These parameters are detailed in table 5.1. Moreover, RF transistors are employed due to the higher frequencies involved.

Table 5.1: 2-Divider component values.

	Wf	Lf	nf
M0	1.6 μm	120 nm	2
M16	4.8 μm	120 nm	4
M3	1.6 μm	120 nm	4

To ensure proper operation and synchronise the VCO frequency of 5 GHz with the Crystal Oscillator operating in the 13 to 55 MHz range, a division ratio of 128 is required. Achieving this ratio entails connecting 7 dividers in series, as illustrated in figure 5.2.

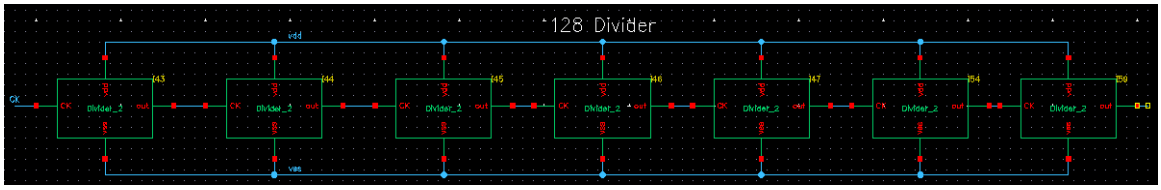


Figure 5.2: 128-Divider circuit Implementation.

5.2.1 Quadrature Divide-by-2 circuit

Multiple techniques use both the in-phase and quadrature components of the chirp signal to encode information bits, such as in-phase and quadrature (IQ) chirp spread spectrum (CSS) [54] or IQ chirp index modulation (IQCIM) [55]. Nevertheless, these strategies will not be discussed in this thesis.

To leverage these LoRa-based schemes, the Divider responsible for halving the output frequency of the VCO will generate quadrature outputs with a 25% duty cycle. The flip-flop-based 2-Divider circuit, configured as a controller-responder flip-flop for robustness, is depicted in fig. 5.3 [14].

A more comprehensive examination of the circuit demonstrated in figure 5.3 is provided in section 5.3.2. However, it can be observed that only one of the four outputs can be high when CK is either high or low. Assuming that the NMOS devices are stronger than the PMOS transistors, they cannot all remain low simultaneously [15]. When CK is low and nCK is high, it may be inferred that out90 and out270 are at 0 V, keeping M4 and M5 off. Yet, due to the regenerative effect around M1 and M3, either out0 or out180 must be high [15].

Table 5.2 presents the dimensions of each transistor. It's worth noting that since the circuit is symmetrical only half is shown. Furthermore, the controller's dimensions are the same as those of the responder.

Table 5.2: Quadrature Divide-by-2 component values.

	Wf	Lf	nf
M2	9.6 μm	120 nm	4
M1	7.2 μm	120 nm	4
M5	7.2 μm	120 nm	4

5.3 Frequency Divider Results and Discussion

This section presents and discusses both Dividers' simulated transient response and phase noise characteristics.

5.3.1 Divider Transient Response

For the 128-Divider, which consists of 7 divide-by-2 stages, the effective performance of the Ratioed TSPC latch is crucial. Figure 5.4 illustrates its output when driven by a 5 GHz clock. The successful functionality of this latch is further corroborated by spectral analysis, which reveals that the frequency output of the Divider is at 2.5 GHz.

Dynamic latches, known for potential state loss due to device leakage at lower clock frequencies, need verification to ensure stable operation. This is addressed by presenting the output of the 128-Divider in figure 5.5. An analysis of its Discrete Fourier Transform (DFT), as shown in fig.5.6, confirms its expected behaviour. Here, a 5 GHz clock signal

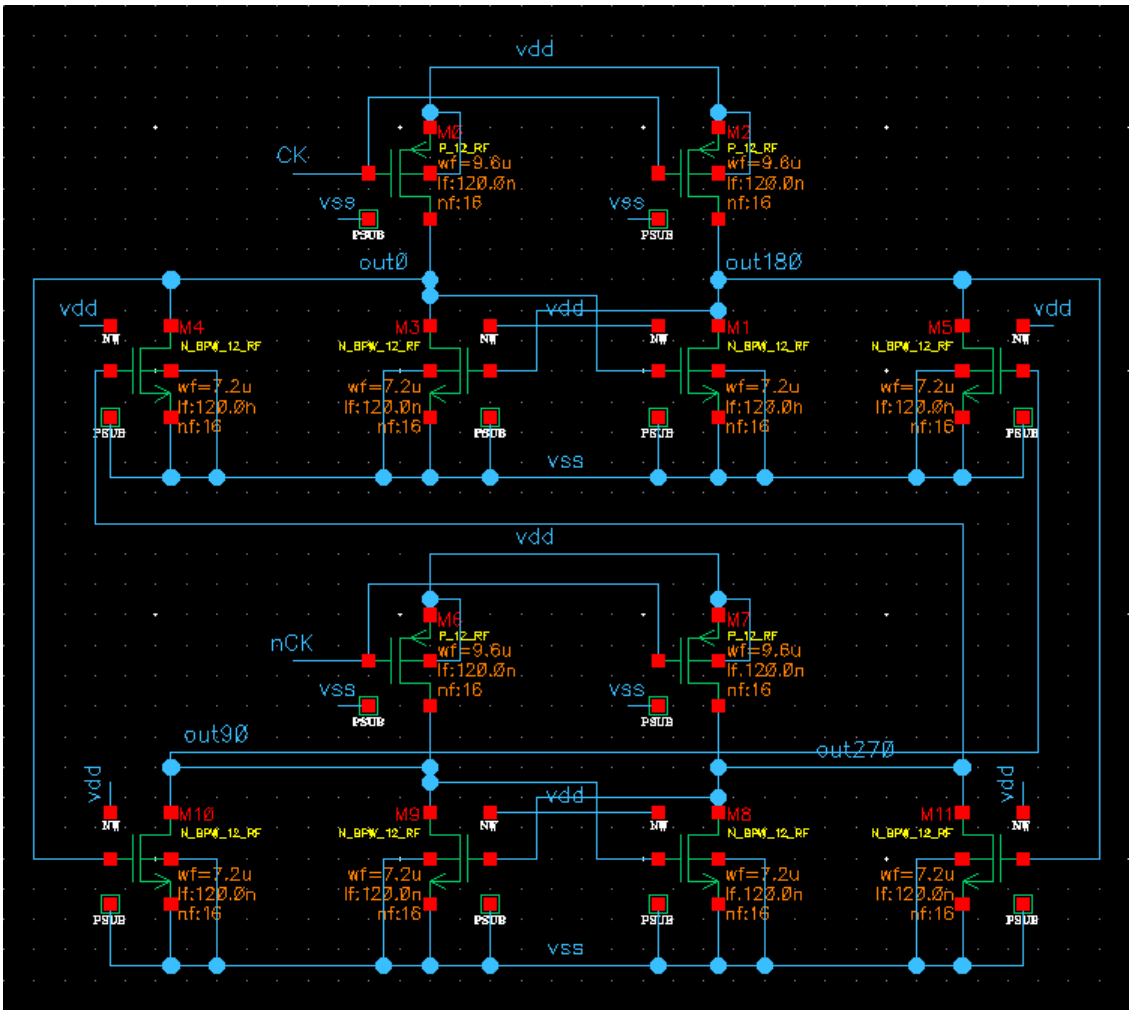


Figure 5.3: Quadrature Divide-by-2 circuit Implementation.

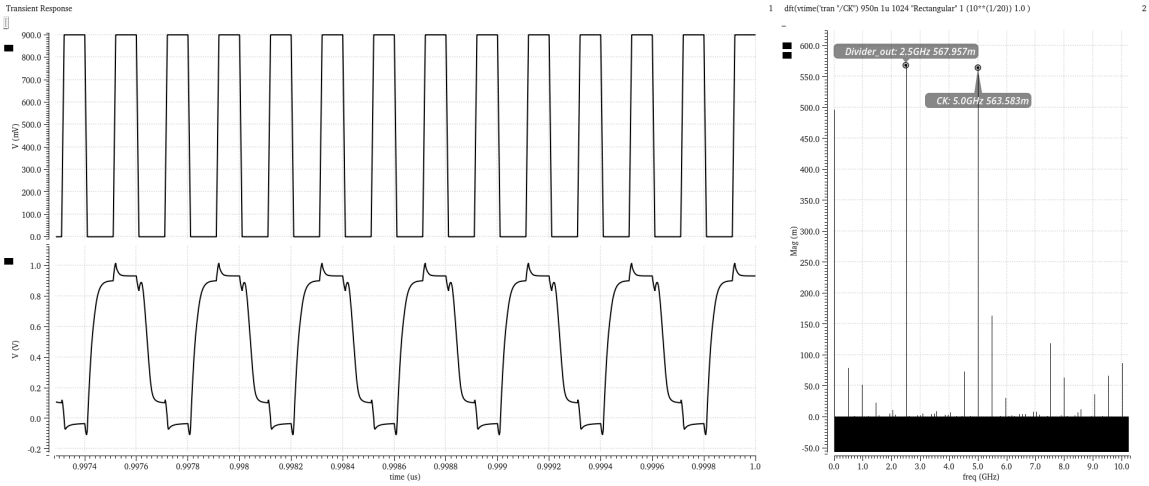


Figure 5.4: Ratioed TSPC output.

produces a 39.06 MHz output. It should be noted that the frequencies depicted in figure 5.6 might not match precisely with the anticipated frequency, which can be attributed to the DFT method used.

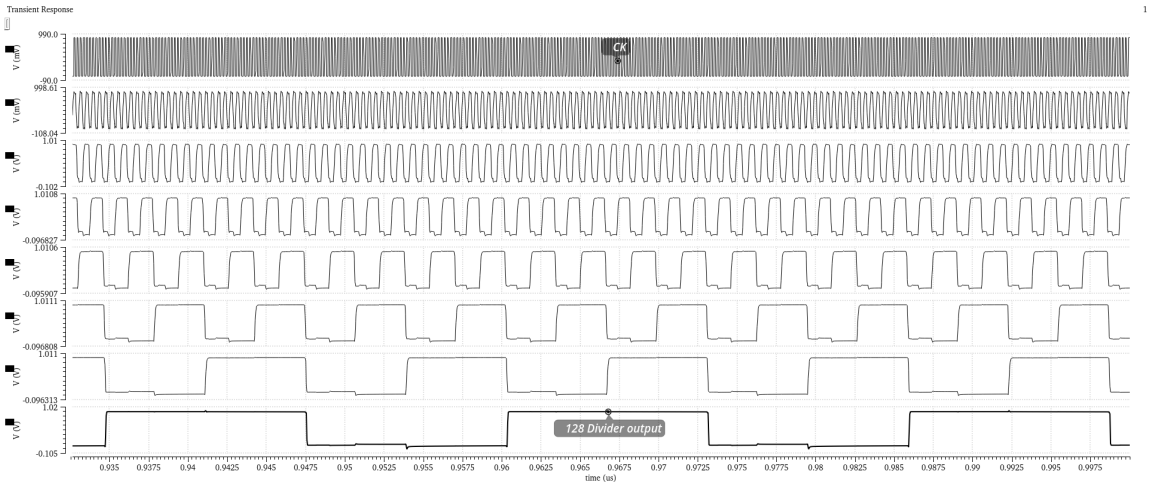


Figure 5.5: 128-Divider waveform output.

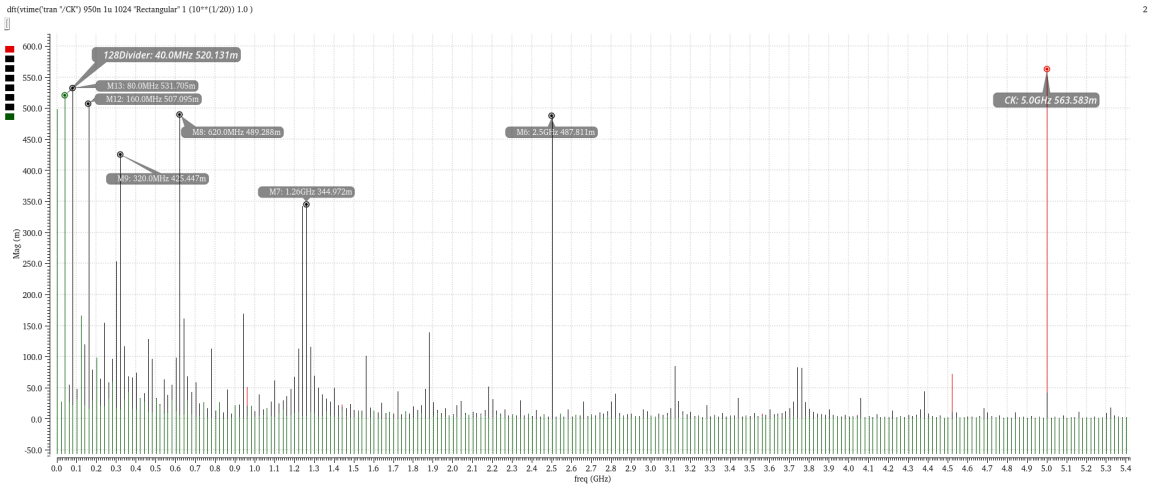


Figure 5.6: 128-Divider frequency output.

5.3.2 Quadrature Divide-by-2 circuit Transient Response

In the scenario depicted by figure 5.7, a low CK value corresponds to a high out0. This suggests that M3 is active, out180 is low and M4 is inactive. Moreover, the activation of M11 leads to a decrease in out90 due to M2 being disabled. At this juncture, M8, M6 and M9 are inactive, leaving out270 either low or high. However, out270 cannot be high, as this would force out0 to be low, countering the initial condition due to M5's influence. When CK voltage rises, M9 activates, raising out270 to V_{DD}, while M8 and M6 remain inactive, the other three outputs stay low. A decrease in CK voltage causes an increase in out180, as both M3 and M0 turn off [15]. With a low CK, out0 and out180 display contrasting states,

whereas out90 and out270 remain at zero. Conversely, with a high CK, out0 and out180 stay at zero but out90 and out270 exhibit opposing states [15].

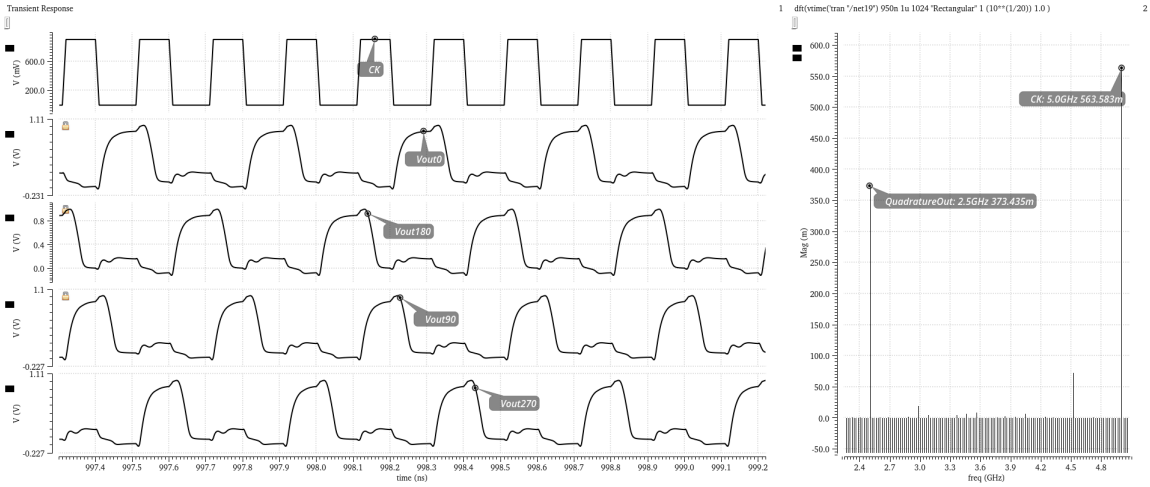


Figure 5.7: Quadrature Divide-by-2 waveform output.

However, when the PMOS transistors activate, they compete with the functioning NMOS transistors. If out0 is high, it implies that M1 is drawing a static current through M2, elevating out180 above zero. Therefore, the PMOS transistors must be sufficiently weak to prevent significant degradation of the logical zero level. To address the issues of level degradation and static current in the circuit, a minor speed reduction might be acceptable. Introducing a cross-coupled PMOS pair in series with the clocked transistors can effectively interrupt the current flow on the side, maintaining a low-level [15].

6

PLL

This chapter delves into the analysis and simulations of the PLL, commencing with an exploration of its dynamic behaviour. Each component of the PLL was individually designed before being integrated into the complete PLL system.

6.1 PLL Characterisation

This section describes the dynamic behaviour of the entire PLL. Where the open-loop was obtained from the time analysis and obtaining the impulse response, then applying the Laplace transform [15]. First, the loop-gain factor is defined in equation 6.1, expressed in rad/s.

$$K = \frac{K_{PFD} K_{VCO} R}{N} \tag{6.1}$$

Considering the second-order Loop Filter F(s) denoted by equation 6.2, the forward path gain can be represented by equation 6.3, yielding the closed-loop transfer function H(s) = $\frac{\Phi_{out}(s)}{\Phi_{ref}(s)}$ (equation 6.4). Indicating a low-pass response whose overall order is set by the LF. The low-pass characteristic of a PLL is advantageous because it filters out input noise frequencies higher than the PLL's bandwidth.

$$F(s) = \frac{(s + \frac{1}{RC_1})}{s(s + \frac{C_1+C_2}{RC_1C_2})} \tag{6.2}$$

$$G(s) = \frac{\Phi_{out}(s)}{\Phi_e(s)} = \frac{K_{PFD} K_{VCO}(s + \frac{1}{RC_1})}{s^2(s + \frac{C_1+C_2}{RC_1C_2})} = \frac{NK(s + \frac{1}{RC_1})}{Rs^2(s + \frac{C_1+C_2}{RC_1C_2})} \tag{6.3}$$

$$H(s) = \frac{K_{PFD} K_{VCO}(\frac{1}{C_2})(s + \frac{1}{RC_1})}{s^3 + (\frac{C_1+C_2}{RC_1C_2})s^2 + (\frac{K_{PFD} K_{VCO}}{NC_2})s + \frac{K_{PFD} K_{VCO}}{NRC_1C_2}} = \frac{NK(s + \frac{1}{RC_1})}{RC_2s^3 + (\frac{C_1+C_2}{C_1})s^2 + Ks + \frac{K}{RC_1}} \tag{6.4}$$

The phase error E(s)= $\frac{\Phi_e(s)}{\Phi_{ref}(s)}$ can be expressed by equation 6.5, and ideally should be zero, however, it generally increases with frequency.

$$E(s) = \frac{s^2(s + \frac{C_1+C_2}{RC_1C_2})}{s^3 + (\frac{C_1+C_2}{RC_1C_2})s^2 + (\frac{K_{PFD}K_{VCO}}{NC_2})s + \frac{K_{PFD}K_{VCO}}{NRC_1C_2}} = \frac{RC_2s^2(s + \frac{C_1+C_2}{RC_1C_2})}{RC_2s^3 + (\frac{C_1+C_2}{C_1})s^2 + Ks + \frac{K}{RC_1}} \tag{6.5}$$

Considering that the third pole is at a high frequency, the PLL can be approximated as a second-order system [1]. To grasp the dynamic characteristics of the PLL, the denominator of the second-order closed-loop response is transformed into a standard form often utilised in control theory: $s^2 + 2\zeta\omega_n s + \omega_n^2$, where ζ represents the damping factor and ω_n denotes the natural frequency. Consequently, the closed-loop response can be articulated as

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}\,, \tag{6.6}$$

where

$$\omega_n = \sqrt{\frac{K_{PFD}K_{VCO}}{NC_1}} = \sqrt{\frac{K}{RC_1}} \tag{6.7}$$

$$\zeta = \frac{\omega_n}{2}RC_1 = \frac{1}{2}\sqrt{KRC_1}\,. \tag{6.8}$$

The natural frequency is directly proportional to the square root of the loop gain. This relationship holds because the Charge Pump's current, designated as I_{CP}, as well as the constants K_{VCO} and C_1 are typically set by design. In contrast, the damping factor is inversely related to the zero frequency. Changing the zero frequency, typically done by adjusting the Loop Filter resistor (R) and Charge Pump's current (I_{CP}), allows for the manipulation of the damping factor (ζ) and natural frequency (ω_n).

The open-loop transfer function may be defined, by using the prior equations:

$$LG(s) = \frac{K_{PFD}F(s)K_{VCO}}{Ns} = \frac{K_{PFD}K_{VCO}(s + \frac{1}{RC_1})}{NC_2s^2(s + \frac{C_1+C_2}{RC_1C_2})}\,. \tag{6.9}$$

From the open-loop gain it's noticeable that $\omega_{p1} = \omega_{p2} = 0$, $\omega_z = \frac{1}{RC_1}$ and $\omega_{p3} = \frac{C_1+C_2}{RC_1C_2}$ indicate the zero and third pole frequency, respectively. Resulting in

$$LG(s) = \frac{K_{PFD}K_{VCO}(s + \omega_z)}{NC_2s^2(s + \omega_{p3})}\,. \tag{6.10}$$

Changing ω_z and I_{CP} will have an impact on the bandwidth and the occurrence of frequency response peaks. Reducing ω_z results in decreased frequency response peaking, but it leads to an increase in the loop bandwidth.

The phase margin will be

$$PM = \arctan\left(\frac{\omega_u}{\omega_z}\right) - \arctan\left(\frac{\omega_u}{\omega_{p3}}\right)\,, \tag{6.11}$$

[1] In a third-order system, the concept of ζ is not formally defined. Therefore, we use the loop parameter values from the second-order type-2 PLL.

where ω_u is the open-loop unity-gain bandwidth and $\omega_z < \omega_u$. It takes a careful selection of C_1 and C_2 values to attain the highest phase margin. The first-order derivative of eq. 6.11 with respect to ω_u is calculated and set to zero to derive the formula for PM_{max}:

$$\omega_u = \omega_z \sqrt{\frac{C_1}{C_2} + 1}\,. \tag{6.12}$$

Subsequently [2],

$$PM_{max} = \arctan\left(\sqrt{\frac{C_1}{C_2} + 1}\right) - \arctan\left(\frac{1}{\sqrt{\frac{C_1}{C_2} + 1}}\right) = \arctan\left(\frac{\frac{C_1}{C_2}}{2\sqrt{1 + \frac{C_1}{C_2}}}\right). \tag{6.13}$$

The conceptual magnitude and phase of the open-loop transfer function for a third-order PLL is shown in figure 6.1.

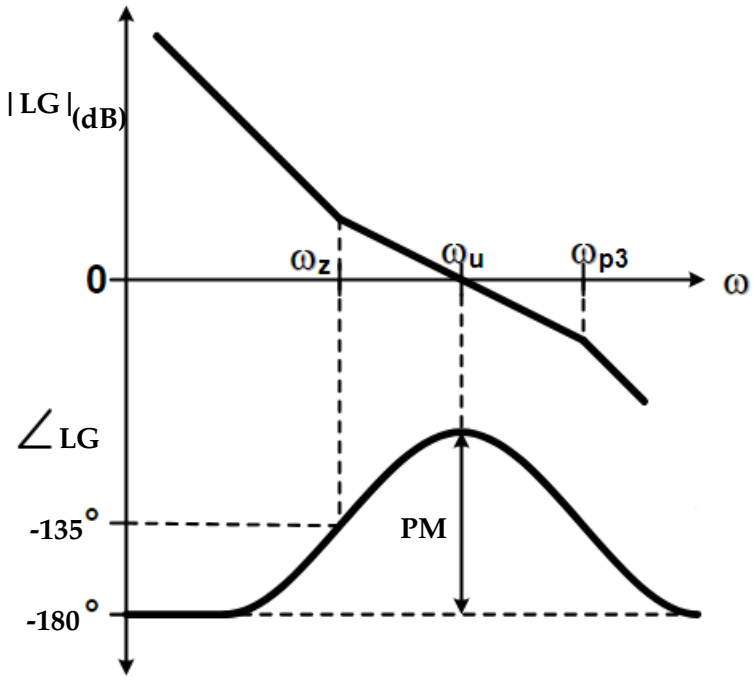


Figure 6.1: Third-order loop-gain Bode plot.

Analytically confirming that the PLL will lock at the input when a frequency step is applied is essential. Given a frequency step input of $\omega_{in} = \frac{\Delta\omega}{s}$, $\Phi_{in}(s) = \frac{\Delta\omega}{s^2}$ may be used to express the input phase deviation. First, deriving the closed-loop transfer function results in:

$$H_{PLL}(s) = \frac{LG(s)}{1 + LG(s)}\,. \tag{6.14}$$

[2]Note that this result is valid only if $\zeta \geq 1$ and ω_{p3} is well above ω_u.

Finally, defining the error transfer function for steady state as

$$\frac{\Phi_{error}(s)}{\Phi_{in}(s)} = H_e(s) = 1 - H_{PLL}(s) = \frac{1}{1 + LG(s)} \,. \tag{6.15}$$

The steady-state error, as determined by the final value theorem, is

$$\begin{aligned} \Phi_{ss_error}^{F_{step}} &= \lim_{s \to 0} s \cdot H_e(s) \cdot \Phi_{in}(s) \\ &= \lim_{s \to 0} s \cdot \frac{1}{1 + LG(s)} \cdot \frac{\Delta\omega}{s^2} \\ &= \lim_{s \to 0} \frac{[RC_1C_2s^2 + (C_1 + C_2)s]\Delta\omega}{RC_1C_2s^3 + (C_1 + C_2)s^2 + K_{VCO}K_{PFD}s + 1} \\ &= \frac{0}{1} \\ &= 0 \,. \end{aligned} \tag{6.16}$$

When a frequency step is provided at the input, the proposed PLL may eliminate any steady-state phase error and relock [56], as shown by equation 6.16.

6.2 PLL Design

This section is dedicated to the PLL design, acknowledging that all components except the Loop Filter, were addressed in previous chapters. The LF, which plays a crucial role in the PLL's phase margin and stability is designed in this section. This is based on equations 6.17 and 6.18, which are adaptations of equations 6.7 and 6.8, serving as the foundational basis for this process.

$$\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi N C_1}} \tag{6.17}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{I_{CP}K_{VCO}C_1}{2\pi N}} \tag{6.18}$$

Parameters such as the VCO gain (K_{VCO}), CP's current (I_{CP}) and loop divide ratio (N) were established earlier and are listed in table 6.1. Choosing ζ to be 1 focuses attention on ω_n. The loop's discrete-time nature necessitates reducing the bandwidth (BW) to approximately one-tenth of the reference frequency, a commonly applied heuristic to accommodate gradual changes within the loop. A key parameter is the open-loop unity-gain bandwidth, approximated as $\omega_u \approx 2.1\omega_n$ when ζ is set to 1 [15].

Table 6.1: Circuit Parameters.

Parameter	Value
Supply Voltage V_{DD}	0.9 V
Reference Frequency f_{ref}	38.75 MHz
Output Frequency f_{out}	4.96 GHz
Divider N	128
CP current I_{CP}	125 μA
VCO gain K_{VCO}	100 MHz/V

Another significant metric is the -3 dB bandwidth, particularly relevant when assessing the PLL's filtering effect on input phase noise; for $\zeta = 1$ the ω_{-3dB} is around $2.5\omega_n$. Therefore

$$\omega_u = 2.1\omega_n = \frac{\omega_{Ref}}{10} . \tag{6.19}$$

From equations 6.17 and 6.18:

$$2.1\sqrt{\frac{I_{CP}K_{VCO}}{2\pi N C_1}} = \frac{2\pi \times (38.75MHz)}{10} . \tag{6.20}$$

The discrete tuning in section 3.5.2 yield a K_{VCO} of 100 MHz/V and since it needs to be expressed in radians/s/V gives $K_{VCO} = 2\pi\times$ 100 Mrad/s/V, with N = 128 results in

$$C_1 = 28.68pF . \tag{6.21}$$

Equating eq. 6.20 to unity leads to

$$R = 37.79k\Omega . \tag{6.22}$$

A critical constraint in selecting loop parameters is that the value of R cannot be excessively high when C_2 is included. This is because if $R \rightarrow \infty$, the series connection of R and C_1 effectively disappears resulting in only C_2 remaining in the loop, which equates to having only two ideal integrators.

As mentioned in section 4.1.2, C_2 is chosen such that $C_2 = 0.2C_1 = 5.74$ pF. However, this decision leads to a complication. With $C_{eq} = \frac{C_1C_2}{C_1+C_2}$, the combination of C_{eq} and R forms a pole at $\omega_{p2} = R(C_{eq})^{-1}$, located at 5.53 MHz. If this pole is below ω_u, it results in a Phase Margin (PM) of less than 45°. This occurs because, at ω_{p2}, the phase profile is influenced by a $-45°$ shift from ω_{p2} leading to a more negative impact at ω_u. Therefore, ω_{p2} is configured to be higher than ω_u, which is 3.88 MHz. While this choice still reduces the phase margin, it leads to a more pronounced peaking in the PLL input-output response compared to a one-pole approximation. It's important to note that for $\zeta = 1$, the VCO's phase noise suppression bandwidth is equal to $\omega_n = 1.85$ MHz. Also, the best way to eliminate noise from the PLL's output clock is to change the loop's bandwidth and frequency response based on the noise source. Changing the loop's parameters lets you control its bandwidth and peaking characteristics.

The phase margin can now be calculated as

$$PM \approx \arctan(4\zeta^2) - \arctan\left(4\zeta^2 \frac{C_{eq}}{C_1}\right) . \tag{6.23}$$

This leads to a phase margin of approximately 44°. It's important to remember that this outcome applies only when $\zeta \geq 1$ and ω_{p2} is significantly higher than ω_u.

The Loop Filter transfer function is given by

$$F(s) = \frac{1}{s\tau_0} \frac{(1 + s\tau_1)}{(1 + s\tau_2)} , \tag{6.24}$$

where τ_0 is the low frequency filter gain, and τ_1 and τ_2 are the time constants. Defined as

$$\tau_0 = C_1 + C_2 , \tag{6.25}$$

$$\tau_1 = RC_1 \tag{6.26}$$

$$\tau_2 = \frac{RC_1C_2}{C_1 + C_2} . \tag{6.27}$$

So the transfer function of the second-order filter is

$$F(s) = \frac{sRC_1 + 1}{s^2(RC_1C_2) + s(C_1 + C_2)} . \tag{6.28}$$

The frequency response of the system is depicted in figure 6.2, which clearly illustrates the two poles and one zero. The initial pole is at the origin, while the zero occurs at $\frac{1}{RC_1} = 0.85$ Mrad/s and the final pole at $\frac{C_1+C_2}{RC_1C_2} = 5.1$ rad/s.

Given that the open-loop transfer function for a PLL is defined as G(s) = $\frac{K_{VCO}K_{PFD}F(s)}{s}$, there is inherently one pole at s = 0, alongside any additional poles from the integrators in F(s), while the zeros determine the open-loop zeros in F(s).

The root locus plot for a third-order type II PLL is shown in fig. 6.3. The system exhibits stability since all the poles reside in the left half of the s-plane. The plot also identifies the two poles at frequencies 0 rad/s and 5.84 Mrad/s, and a zero at 0.917 Mrad/s.

The stability of the loop is evident from the Bode Plot shown in figure 6.4, which displays a phase margin of 46.4°. This phase margin, a key indicator of stability, is coupled with a gain plot that shows a consistent low-pass filter behaviour gradually decreasing with frequency. Notably, the absence of peaking on the magnitude plot suggests stable behaviour without the risk of resonant peaks indicating potential instability or under damping.

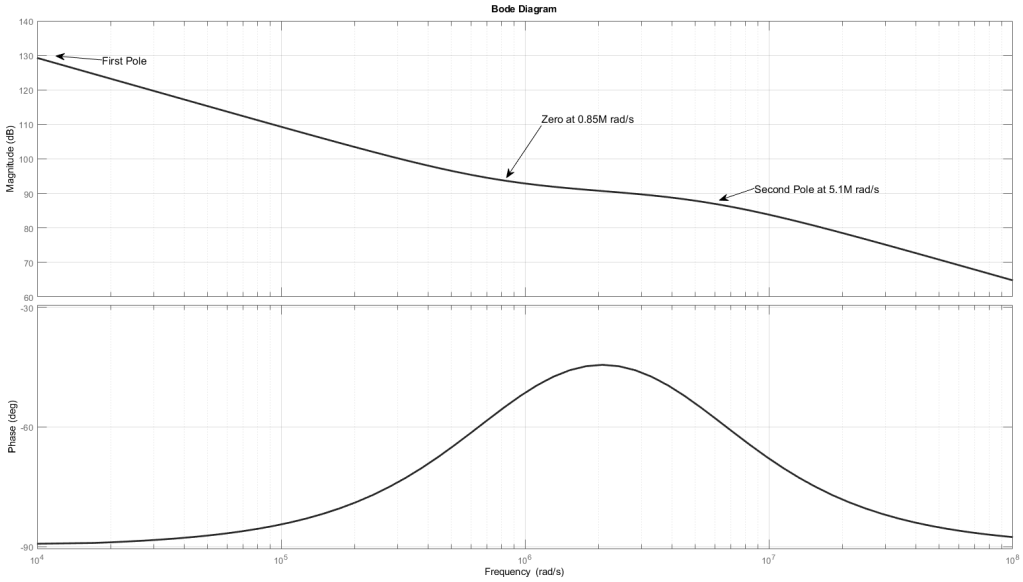


Figure 6.2: Loop Filter response Bode Plot.

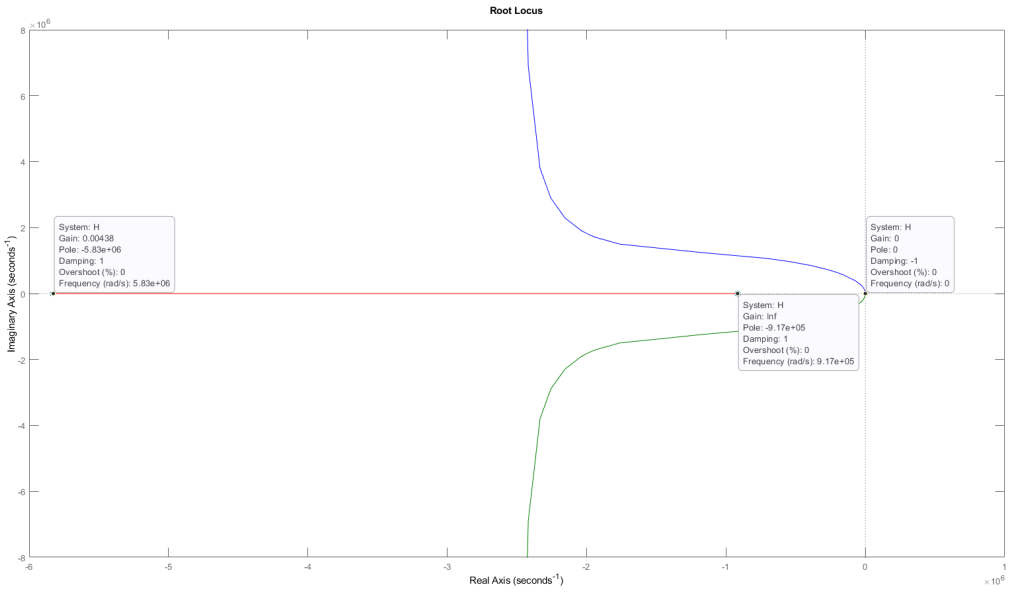


Figure 6.3: PLL Root locus.

Moreover, for the third-order type II PLL being discussed, the phase lag does not reach -180° at any positive finite frequency, rendering the gain margin non-applicable [19]. The unity gain or crossover frequency, where the gain measures 0 dB, along with the phase margin provide valuable insight into the PLL's response time and overall stability.

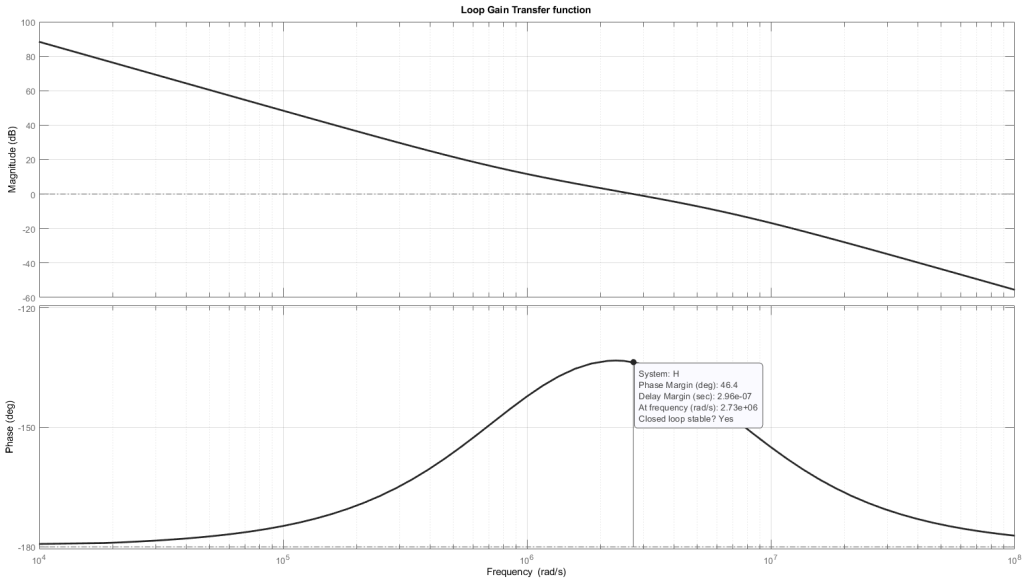


Figure 6.4: PLL Open-Loop response Bode Plot.

Table 6.2 presents key loop parameters, including the phase margin and the closed-loop bandwidth. These parameters can be cross-referenced with the open-loop response highlighted in figure 6.4 and the closed-loop response illustrated in figure 6.5, respectively.

Table 6.2: PLL Parameters.

Parameter	Value
Phase Margin PM	46.36°
Max Phase Margin PM_{MAX}	46.76°
Zero frequency f_z	0.16 MHz
3^{rd} Pole frequency f_{p3}	0.93 MHz
Unity-Gain BW f_c	0.44 MHz
Closed-Loop BW	0.73 MHz

The amplitude response of the closed-loop system shown in figure 6.5 illustrates that the transfer function H(s) serves as a lowpass filter on the input signal's phase modulation. This means the loop accurately follows phase modulations within its bandwidth while struggling with those outside it. Consequently, phase modulations within this bandwidth are conveyed to the VCO's phase output, whereas those outside are weakened.

A key aspect of this response is its gradual decline without sharp transitions, implying a stable system free from complex conjugate poles close to the imaginary axis, which

might cause oscillations or instability.

The bandwidth of the PLL, as indicated in table 6.2, is typically determined at the frequency where a notable decrease in gain occurs. This is generally identified at the point where the magnitude response drops by 3 dB from the lower frequency plateau. Such a measurement signifies the PLL's capacity to rapidly adjust to variations in the input signal. Furthermore, in the context of the PLL, there is an inverse relationship between bandwidth and settling time.

The system exhibits a minor peak in the response linked to a zero within the system. This zero is critical for the stability of type II PLL but leads to a necessary compromise in the gain peak, although undesirable, this peaking is an inevitable side effect of using integrators in the Loop Filter. Furthermore, the poles of the system are significantly higher than the desired loop bandwidth, implying that these high-frequency poles have minimal effect on the PLL's performance and can be mostly ignored. Consequently, an analysis of H(s) indicates that gain peaking in a third-order type II PLL (eq. 6.29) stems from this particular system design [19].

$$gain\ peaking = 10 \log \frac{8\zeta^4}{8\zeta^4 - 4\zeta^2 - 1 + \sqrt{8\zeta^2 + 1}} \tag{6.29}$$

From equation 6.29, the gain peaking is calculated to be around 1.25 dB. Yet, an examination of figure 6.5 indicates that the actual gain is closer to 2.7 dB. This level of peaking is minor when considering a standalone PLL. However, without appropriate safeguards, more significant peaking can occur in cascaded systems, like a chain of repeaters in a telecommunications network. In such a setup, the cumulative peaking can become substantial and problematic, as detailed in [19]. This highlights the importance of managing peak gain in interconnected systems to prevent potential detrimental effects.

6.3 PLL Results and Discussion

This section offers an insight into the simulated transient response of the established PLL, as presented in figure 6.6. The schematic includes all the previously designed components, with a noteworthy point that the LF is integrated within the CP block and the series of 7 dividers together form the 128-Divider.

Simulating PLLs can be time-consuming due to the extensive number of cycles and the large count of transistors in the loop. To expedite transient simulation, a strategy was employed to avoid using signal sources with abrupt changes. Specifically, discontinuous derivatives were avoided by modelling the reference signal with a sinusoidal wave, which is then transformed into a square wave using an inverter, as suggested in [15].

Due to the use of a varactor in the VCO, where an increase in voltage leads to higher capacitance and a subsequent decrease in VCO frequency, a specific design adjustment is made. To counter this behaviour, the connections of the PFD and the CP are reversed, as

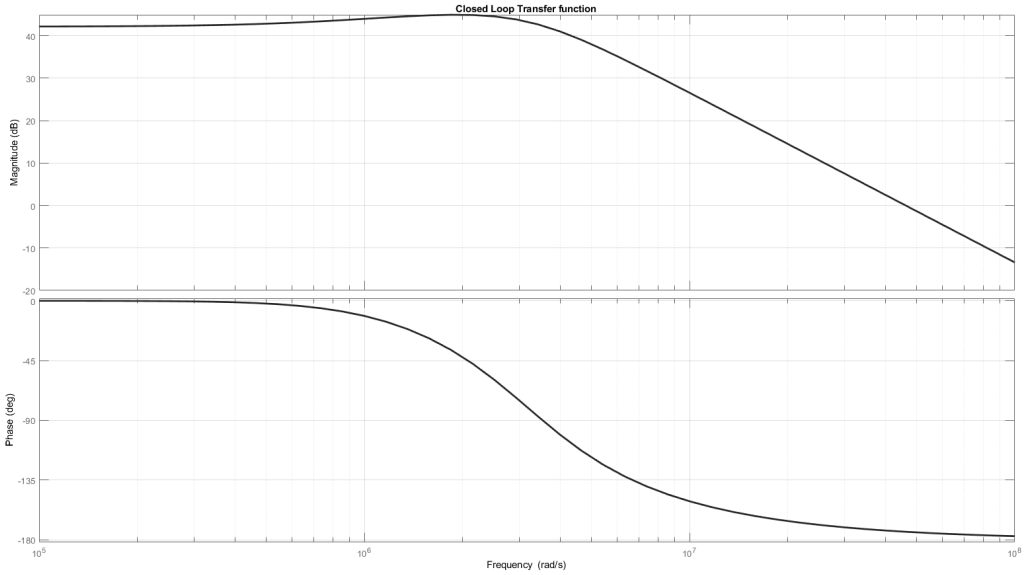


Figure 6.5: PLL Closed-Loop response Bode Plot.

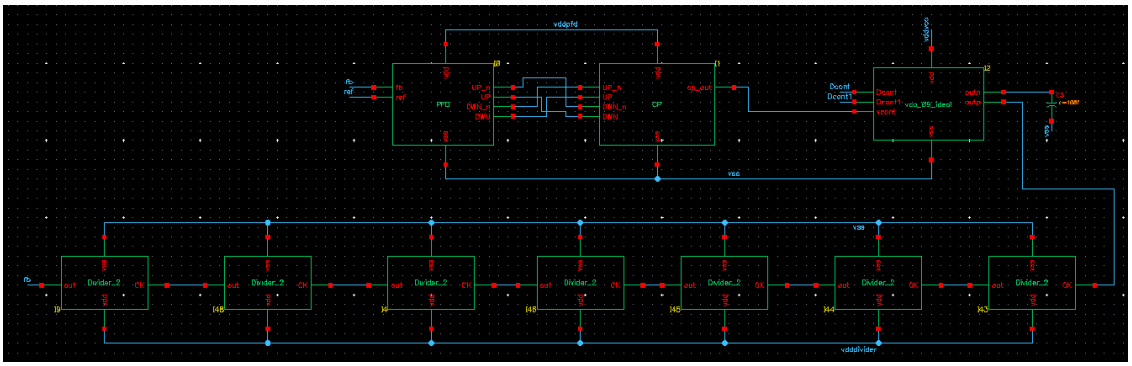


Figure 6.6: Schematic of the PLL.

illustrated in figure 6.6. Nevertheless, despite this alteration, the operational characteristics of these blocks remain akin to those discussed in section 4.3.

6.3.1 PLL Transient Response

To confirm that the PLL successfully locks onto the reference frequency, it's essential to examine its locking behaviour. Figure 6.7 provides key insights into this, demonstrating that the V_{cntrl} voltage stabilises and flattens out after a few microseconds, which indicates that the PLL has reached a steady-state locked condition. This is further corroborated by the frequency plots in the same figure, where the feedback signal frequency (shown in black) aligns with the reference frequency (showcased in red) at approximately 38.75 MHz.

Observing figure 6.7, it is possible to determine the locking time of the PLL. The data

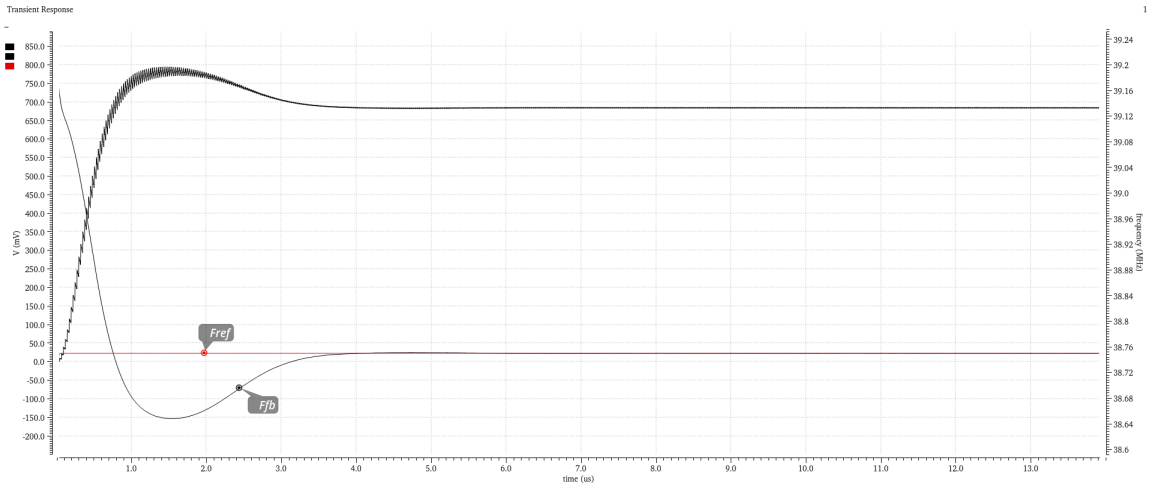


Figure 6.7: PLL V_{cntrl} Voltage and PLL frequency Locking.

indicates that the PLL locks in approximately 5.5 μs when the V_{cntrl} reaches 683 mV.

Although the control voltage appears consistent at first glance, a closer examination reveals a subtle ripple. This phenomenon is analysed in greater detail in figure 6.8 to assess its acceptability. Additionally, the observed settling behaviour exhibits minimal ringing, implying that the $\zeta = 1$ is satisfied.

By examining figure 6.7, it's evident that the initial glitch is a result of the Charge Pump's turn-on and turn-off. Furthermore, the ripple detailed in figure 6.8, characterised by a peak-to-peak amplitude of 2.46 mV, displays spikes approximately every 2.5 ns. This timing corresponds to the reset period of the system, which in turn relates to the issues highlighted in section 4.3.1.2. To minimise fluctuations in V_{cntrl} while keeping the PFD | CP block unchanged, the value of C_2 could be increased. However, this alteration would modify the PLL's transfer function, potentially affecting its stability.

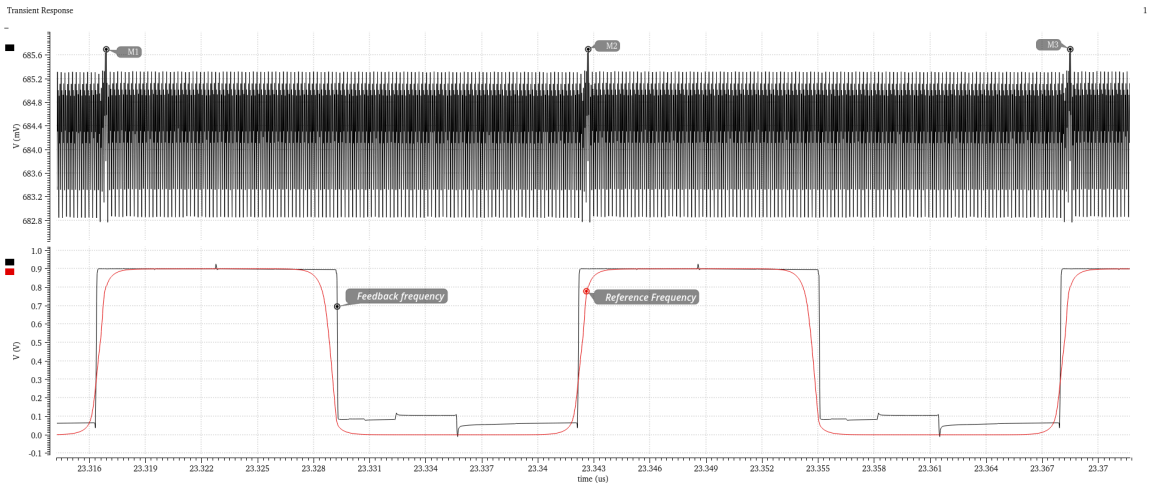


Figure 6.8: PLL V_{cntrl} Voltage after Lock.

In figure 6.9, the input and output frequencies of the PLL are shown. The PLL is

configured with a reference frequency of 38.75 MHz resulting in an output frequency near 4.96 GHz. Notably, there's a fluctuation of approximately 10 MHz in the output frequency as a consequence of the control voltage ripple. Although this might initially appear to be a minor issue since the impact is effectively halved to a 5 MHz fluctuation due to the implementation of a Quadrature Divide-by-2 block at the PLL output. These frequency variations can create significant challenges, particularly in the precise selection of channels in communication systems.

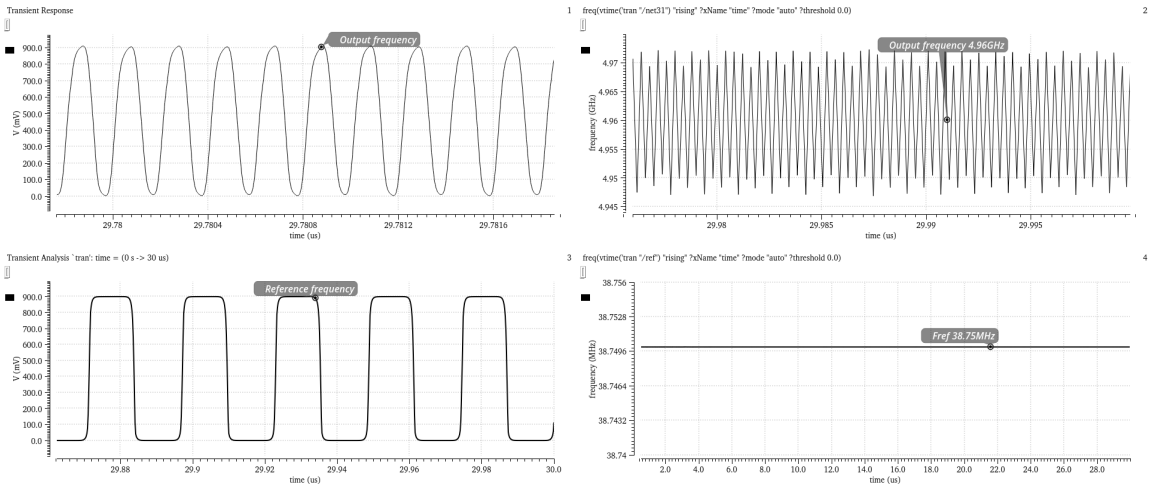


Figure 6.9: PLL Settled Transient Simulation Input and Output.

In figure 6.10 the output of the PLL, incorporating a Quadrature Divide-by-2 block, is displayed. When a reference signal of 38.75 MHz is inputted, the PLL produces a quadrature output signal at a frequency of 2.48 GHz. As outlined in section 5.2.1, the addition of the quadrature divider enables the PLL to span the frequency range within the ISM bands.

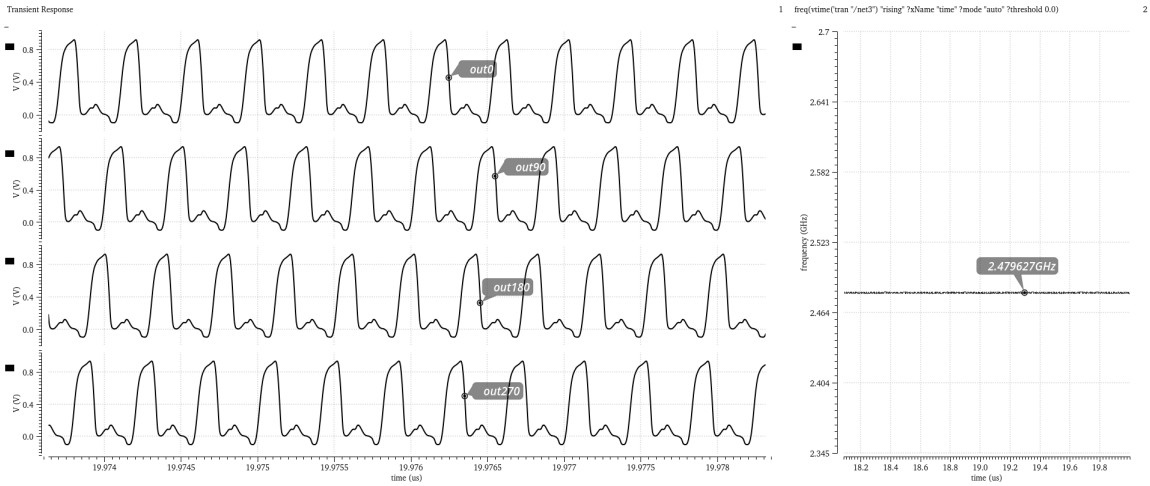


Figure 6.10: PLL Settled Transient Simulation with the Quadrature Divider.

The tuning range of the PLL is essential for locking onto various frequency channels

within its band, ideally aligning with the tuning range of the VCO. In simulations, it was observed that the PLL's tuning range was somewhat more limited than anticipated. To evaluate this, the reference frequency was altered, which is not a common practice in Frequency Synthesisers where a stable Crystal Oscillator typically serves as the reference and frequency adjustments are made by changing the division ratio of the Divider. For this assessment, the reference frequency varied from 38.55 MHz to 39.05 MHz, leading to output frequencies ranging from 4.934 GHz to 5 GHz. This shift in reference frequency affected the PLL's lock time, especially at the extremities of this range, with lock times significantly increasing to 7.15 μs and 11.5 μs for the lower and higher frequencies, respectively.

Comprehensive testing of the designed PLL included evaluation of the capbank tuning over a one-bit range. In this configuration, with input frequencies between 38 MHz and 38.5 MHz, the PLL successfully locked and generated output frequencies within the 4.864 GHz to 4.928 GHz band. The lock times recorded in these tests were in line with those observed earlier. Further testing with a two-bit range to access the lower frequency band resulted in a substantial increase in lock time, approximately 60 μs, achieving a frequency of 1.737 GHz.

6.3.2 PLL Power Consumption

Power consumption is a key factor in low-power and low-voltage applications. Figure 6.11 shows the power consumption of the PLL in a steady-state lock condition, operating at a 0.9 V supply. The power oscillates between 0 mW and 7 mW, but the critical metric here is the average power consumption, which is approximately 3.50 mW. This measurement is taken with a reference signal of 38.51 MHz.

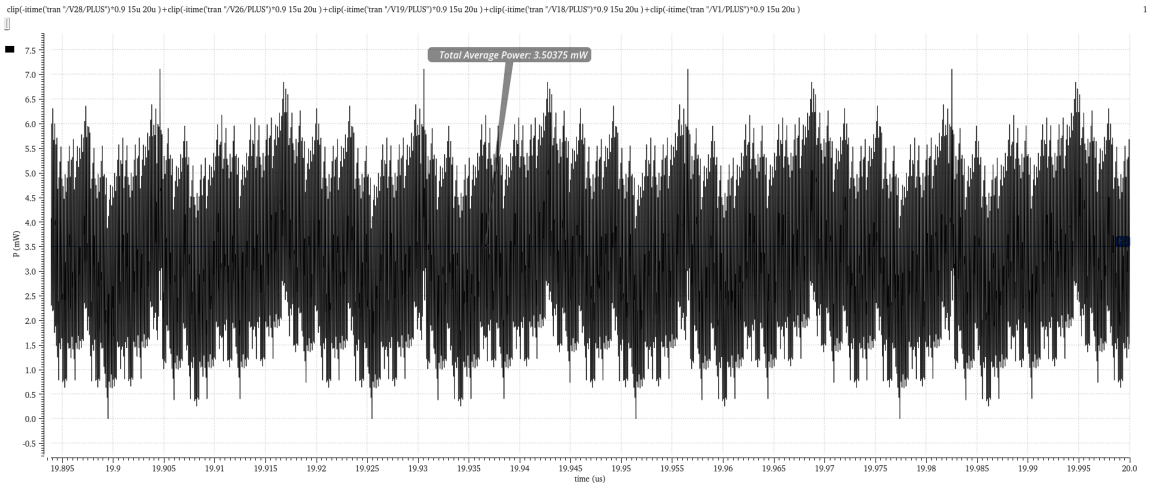


Figure 6.11: PLL Power Consumption in Steady-State.

Figure 6.12 presents the power consumption of each component in the system. It is evident from this data that the majority of power usage originates from the VCO's block,

with the VCO Buffer consuming 1.03 mW and the LC-VCO itself using 1.02 mW. Additionally, the Divider consumes approximately 1.37 mW. This implies that the combined average power consumption of the PFD | CP | LF block, as well as the VCO Level Shifter, is relatively negligible, amounting to only about 20.75 μW and 60.92 μW, respectively, particularly when the PLL is in a locked state.

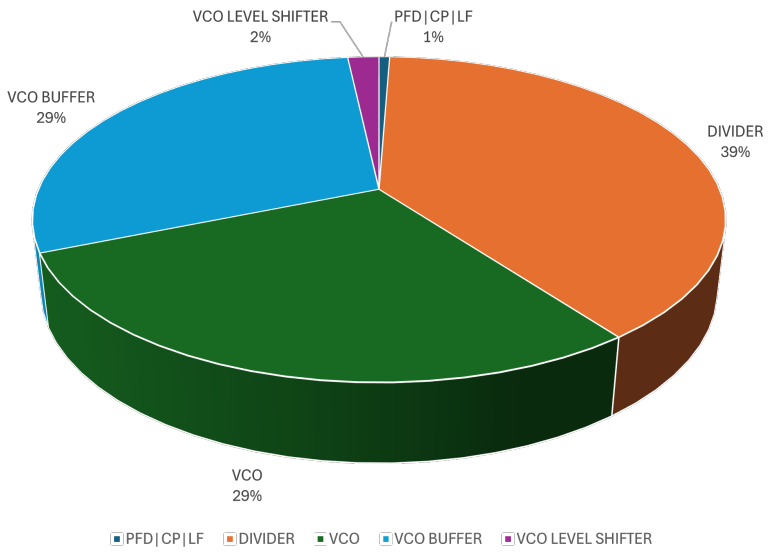


Figure 6.12: Average Power Consumption per block.

Incorporating the Quadrature Divider into the PLL setup results in an increased power consumption by 4.35 mW at a reference frequency of 38.51 MHz, representing a doubling of the power consumption compared to the PLL without the Quadrature Divider.

Adjusting the reference frequency within the PLL has a limited impact on its overall power consumption. Notably, adding a single bit to the capbank does not significantly alter the PLL's power consumption. However, the inclusion of a second bit in the capbank results in a decrease in power consumption to 3.1 mW. This reduction is more pronounced in the VCO, which now consumes 770 μW.

7

Conclusions

This dissertation undertakes the task of designing and implementing a low-power Phase-Locked Loop for ISM applications, showcasing the crucial role of PLLs in ensuring reliable frequency synchronisation in IoT systems with a focus on LoRa communication technology. Delving into the intricate details of PLL components such as the Voltage Controlled Oscillator, Phase-Frequency Detector and Frequency Divider, this study provides deep insights into their characteristics and design considerations. All blocks were designed in 130 nm CMOS technology using the UMC library with a voltage supply of 0.9 V.

The proposed LC-VCO with an NMOS topology suitable for the low voltage supply, operates at double the frequency, allowing for integration within an integrated circuit. Continuous tuning is implemented using an I-MOS varactor, achieving a K_{VCO} of about 100 MHz. Discrete tuning covers frequencies between the 4.8 to 5 GHz band and shifts to the 1.734 to 1.738 GHz band, with phase noise achieving -103.112 dBc/Hz at 1 MHz for a V_{cntrl} of 150 mV. Additionally, integrating over the interval from 10 kHz to 10 MHz results in an RMS jitter of 14.095 ps for a 5 GHz carrier.

Incorporating the PFD block are a Phase-Frequency Detector, a Charge Pump and a Loop Filter. The PFD includes two resettable D flip-flops with a NAND gate and an inverter to increase the delay in the reset path, preventing a dead zone. A gate-switch Charge Pump provides 125 μA current and a second-order low pass filter acts as the Loop filter.

Two Dividers were designed: one as the PLL's Frequency Divider following a ratioed TSPC topology implementing an integer division ratio of 128, and a Quadrature Divider at the PLL output for quadrature output and frequency targeting within the 868 MHz and 2.4 GHz bands.

The dynamic behaviour of the Type II third-order PLL was thoroughly characterised, including both open-loop and closed-loop responses. This analysis yielded a phase margin of 46.36° and a closed-loop bandwidth of 0.73 MHz. Transient simulations showed a lock time of 5.5 μs when using a 38.75 MHz reference frequency. The PLL's tuning range was demonstrated to be from 4.864 GHz to 5 GHz, adjustable with reference frequencies ranging from 38 MHz to 39.05 MHz. The average power consumption was measured

at 3.50 mW, primarily due to the Divider, VCO Buffer and VCO. Furthermore, adding two bits to the capbank enabled the PLL to access a frequency of 1.737 MHz with an approximate lock time of 60 μs, providing coverage for the lower frequency band (1.734 to 1.738 GHz). This adjustment resulted in a further reduction in power consumption to 3.1 mW, primarily due to the decreased power requirements of the VCO.

Ultimately, the addition of the Quadrature Divider leads to an increase in the overall power consumption by 4.35 mW, while simultaneously expanding the frequency coverage to range from 868 MHz to 869 MHz and from 2.432 GHz to 2.5 GHz.

In summary, this work contributes to the design and application of PLLs for ISM band applications, laying a foundation for future explorations in low-power, high-efficiency PLL design, particularly in LoRa communications within IoT systems.

7.1 Problems and Limitations

Throughout this dissertation, a range of challenges and limitations emerged. A key issue was the incomplete analysis of the PLL, specifically in terms of phase noise and jitter, which weren't thoroughly investigated. Although the noise from the VCO is acknowledged as a major source of noise in the PLL output, additional factors also influence the performance. Notably, at low offset frequencies, the noise generated by the Charge Pump's current and the noise from the Divider are significant contributors to the PLL's output noise. However, beyond the PLL's loop bandwidth, it's primarily the VCO noise that affects the output.

Another limitation lies in the Frequency Divider design because the integer Divider's fixed division ratio restricts the ability to switch between different frequency channels, which could limit the circuit's versatility in certain applications.

Finally, for comprehensive Process-Voltage-Temperature (PVT) characterisation, corner simulations are essential to verify voltage and temperature effects, and Monte Carlo simulations are necessary to account for process variations. These additional simulations would provide a more robust and thorough understanding of the circuit's performance under various conditions.

7.2 Suggestions for Future Work

Addressing the issues outlined in section 7.1 presents a promising direction for future work. The implementation of a low-power delta-sigma fractional-N Frequency Divider stands out as a significant enhancement for the PLL's performance. This modification aims to reduce power consumption and enable finer tuning of frequency channels.

Exploring further enhancements in the different components of the PLL presents a significant opportunity for improvement. A crucial focus could be on refining the PFD, especially in terms of reducing spike occurrences. Additionally, increasing the number of levels in the capbank and incorporating switched current mirrors could ensure sufficient current for the VCO to access lower frequency ranges.

Moving these theoretical improvements into practical testing phases, through the layout and fabrication of these components, would provide tangible evidence of their efficacy. Such steps are crucial for the continued refinement of the PLL's design, ensuring its functionality aligns with the advancing technological demands.

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