Halyna Korol

Licenciada em Engenharia Electrotécnica e de Computadores

Switching Mode Power Amplifier for Bluetooth Applications

Dissertação para obtenção do Grau de
Mestre em Engenharia Electrotécnica e de Computadores

Orientador: Luís Augusto Bica Gomes de Oliveira,
Professor Doutor, Universidade Nova de Lisboa

Júri:

Presidente:	Professor Doutor Paulo Montezuma de Carvalho
Arguente:	Professor Doutor João Pedro Abreu de Oliveira
Vogal:	Professor Doutor Luís Augusto Bica Gomes de Oliveira

FACULDADE DE
CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

Setembro, 2015

Switching Mode Power Amplifier for Bluetooth Applications

"Every solution breeds new problems" - Arthur Bloch
(Murphy's law)

Acknowledgements

Chegando a esta fase, é de reflectir nas inúmeras oportunidades e concretizações, tanto a nível pessoal como a nível profissional, que aconteceram graças à FCT-UNL. Esta, não só é uma instituição com espaço de admirar, mas que também oferece distintas áreas de aprendizagem com professores notáveis nas respectivas áreas. A isto devo um muito obrigado!

Em segundo lugar, gostaria de agradecer a todos os professores do departamento de electrónica. Mas devo um especial agradecimento à professora Helena Fino, porque foi ela que desde princípio criou a minha paixão pela electrónica; ao professor João Goes por ter feito crescer a minha paixão ainda mais, mas desta vez pela micro-electrónica; ao professor Luís Oliveira, que tanto como professor como meu orientador sempre me guiou e sempre me motivou; aos professores João Oliveira, Nuno Paulino e Rui Tavares por serem esplêndidos professores. Um especial obrigado também ao professor Luís Bernardo, André Mora e Anabela Pronto, por serem mais do que professores.

Quero também expressar a minha gratidão para com os meus colegas da sala 3.5, que sem a companhia deles o trabalho nunca seria o mesmo, nem os almoços, nem os pequenos intervalos num espaço que muito bem podia ser chamado de "a nossa casa". Por isso, a eles, sem exclusão alguma, mesmo os que já "partiram", outro muito obrigado.

Um obrigado também às pessoas que mais me marcaram neste percurso académico: Jorge Silva, Denise Solange, Dilcarina Duarte, Tiago Bento, Celso Almeida e a Ana Carreira, a minha companheira de comboio.

E por último deixo o meu maior agradecimento às pessoas mais especiais na minha vida: à minha melhor amiga Carla Borges, que nos piores momentos sempre esteve lá para me apoiar; ao meu namorado Ricardo Neves (FCT :)), que tornou este percurso inesquecível, mais especial ainda, deu-me forças e sempre acreditou em mim quando nem eu já acreditava. E sem deixar de parte a pessoa mais importante da minha vida, porque sem ela nada disto era possível: Obrigado Mãe!

ABSTRACT

Modern fully integrated transceivers architectures, require circuits with low area, low cost, low power, and high efficiency. A key block in modern transceivers is the power amplifier, which is deeply studied in this thesis.

First, we study the implementation of a classical Class-A amplifier, describing the basic operation of an RF power amplifier, and analysing the influence of the real models of the reactive components in its operation.

Secondly, the Class-E amplifier is deeply studied. The different types of implementations are reviewed and theoretical equations are derived and compared with simulations. There were selected four modes of operation for the Class-E amplifier, in order to perform the implementation of the output stage, and the subsequent comparison of results. This led to the selection of the mode with the best trade-off between efficiency and harmonics distortion, lower power consumption and higher output power. The optimal choice was a parallel circuit containing an inductor with a finite value. To complete the implementation of the PA in switching mode, a driver was implemented. The final block (output stage together with the driver) got 20 % total efficiency (PAE) transmitting 8 dBm output power to a 50 Ω load with a total harmonic distortion (THD) of 3 % and a total consumption of 28 mW.

All implementations are designed using standard 130 nm CMOS technology. The operating frequency is 2.4 GHz and it was considered an 1.2 V DC power supply. The proposed circuit is intended to be used in a Bluetooth transmitter, however, it has a wider range of applications.

Keywords: Power amplifier, Bluetooth, CMOS, efficiency, distortion, switching mode, driver, Class-A, Class-E.

RESUMO

As arquiteturas modernas de *transcievers* totalmente integradas, requerem circuitos de reduzida área, de baixo custo, mínimo consumo de energia e alta eficiência. Um bloco chave em *transcievers* modernos é profundamente estudado nesta tese, o amplificador de potência (AP).

Em primeiro lugar, estudou-se a implementação de um amplificador clássico Classe-A, descrevendo o funcionamento básico de um amplificador de potência de RF, e analisando a influência dos modelos reais dos condensadores e das bobinas no seu funcionamento.

Em segundo lugar, o amplificador de Classe-E é profundamente estudado. Os diferentes tipos de implementações são revistos e as equações teóricas são derivadas e comparados com as simulações. Foram selecionados quatro modos de funcionamento para o amplificador de Classe-E, a fim de realizar a implementação do andar de saída e a posterior comparação de resultados. Esta comparação levou à seleção do modo com o melhor compromisso entre eficiência e distorção harmónica, menor consumo de energia e potência de saída superior. O escolhido, acabou por ser um circuito em paralelo contendo um indutor com um valor finito. Para completar a implementação do AP no modo de comutação, foi implementado um *driver*. O bloco final (andar de saída, juntamente com o driver) tem 20 % de eficiência total (PAE), transmitindo 8 dBm de potência a uma carga de saída de 50 Ω, uma distorção harmónica total (DHT) de 3 % e um consumo total de 28 mW.

Todas as implementações foram projetados usando uma tecnologia CMOS standard de 130 nm. A frequência de trabalho é de 2,4 GHz e foi utilizada uma fonte de alimentação DC 1,2 V. O circuito proposto destina-se a ser utilizado num transmissor Bluetooth, no entanto, tem uma ampla gama de aplicações.

Palavras-chave: Amplificador de potência, *Bluetooth*, eficiência, distorção, *driver*, Classe-A, Classe-E

CONTENTS

List of Figures

LIST OF TABLES

GLOSSARY

AC alternating current.

BPF bandpass filter.

CMCD current-mode Class-D.

CMOS complementary metal-oxide-semiconductor.

CW continuous wave.

DAC digital-to-analog converter.

DC direct current.

DSP digital signal processor.

GFSK Gaussian frequency shift keying.

IC integrated circuit.

IF intermediate frequency.

IM intermodulation.

IP3 3rd order intercept point.

ISM industrial scientific medicine.

LO local oscillator.

NMOS n-type MOS transistor.

PA power amplifier.

PAE power added efficiency.

PAN personal area network.

PC personal computer.

PMOS p-type MOS transistor.

PSS periodic steady state.

PU pulse-current.

RF radio frequency.

RFC radio-frequency choke.

RMS root mean square.

SoC system-on-chip.

THD total harmonic distortion.

VMCD voltage-mode Class-D.

ZCS zero-current switching.

ZDS zero-derivative switching.

ZVS zero-voltage switching.

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

In the recent years, a significant effort has been made towards improving efficiency in electronic devices. Besides this, the efforts to improve lifetime and size of batteries of these devices is the principal objective. The mobile phone is just a small example where highly efficient power amplifier is required. But it is the one that have shown remarkable growth in the last decade. The evolution to the smartphones of today demanded development of mobile phones with more and more features, requiring more space but without going outside of the desirable size for the smartphones. Longer battery lifetime and lower cost, in order to keep competitiveness between manufacturers, have been also a big demand for the mobile devices. But the biggest challenge have been to develop some applications, for smartphones or other electronic devices, in the integrated circuit (IC) design field, where implementation in higher frequency is required for these systems. The power amplifiers are the primarily block of any wireless communication.

With the need to provide more efficient equipments, the technology is also evolving. Wide bandgap and narrower bandgap specify which materials the technology uses. For instance, technologies for the wide bandgap are: SiC (Silicon Carbide CMOS), GaN (Gallium nitride HEMPT), SOI (Silicon on Insulator), etc.; for the narrower bandgap devices: Si (Silicon CMOS), GaAS (Gallium Arsenide pHEMT), etc.. The research in [1] contains collected information from Class-E power amplifier implementations, made in the most diverse technologies. The

conclusion was that wide bandgap devices can support more power than the narrower bandgap devices, due to the higher voltage breakdown, lower substrate loss and higher quality of the monolithic passive components, hence can deliver higher power with higher efficiency. However, they are much more expensive compared with complementary metal-oxide-semiconductor (CMOS). The development of the radio frequency (RF) front-end circuits that use CMOS technology have made a great advance, with performance increasingly nearest to the performance with the others technologies. Additionally, the urge to integrate digital blocks, analog and RF circuits on a single chip to implement system-on-chip (SoC) solutions with lower cost made the CMOS technology the most preferable.

The main purpose of the present work is to study the variate possibilities of designs and implement, using 130 nm CMOS technology, an RF power amplifier to be integrated in RF transmitter for the Bluetooth applications. The principal classes of the power amplifier are analysed, classes from the linear power amplifiers as well as from the switching mode power amplifiers. From these classes, Class-A (linear power amplifiers (PAs)) and Class-E (switching PAs) were chosen for detailed theoretical study and their implementation. However, the biggest focus is given to the second one, since the switching mode PAs promises to achieve higher efficiency.

1.2 Bluetooth Features

Bluetooth is one of the wireless applications within the personal area network (PAN). In other words, it is an application with combined specifications for common short range wireless communication between several devices like mobile phones, laptops, personal computers (PCs), printers, etc. Bluetooth is defined by radio standard with the aim to consume low power within short range communication and with a low-cost transceiver microchip in each device. Its operating frequency band is the 2.4 GHz industrial scientific medicine (ISM), that ranges from 2.4 GHz to 2.4835 GHz[2]. It is divided into 78 channels, each using 1 MHz of bandwidth, with frequency hopping [3] and, from its first version, uses Gaussian frequency shift keying (GFSK) modulation. GFSK provides a constant envelope signal, and thus a switching amplifier can be used.

There are three power levels referring to the output power specification of the Bluetooth applications, all using point-to-point communication. One must be chosen, so that the PA can operate for the desirable specifications. For each of these levels corresponds a particular range of the PAs output power, as can be seen in

Table 1.1.

Table 1.1: Power distance characteristics of the Bluetooth applications [4].

	Maximum Output Power	Minimum Output Power	Distance [m]
Higher-distance	*100 mW (20 dBm)*	*1 mW (0 dBm)*	*100*
Medium-distance	*2.5 mW (4 dBm)*	*0.25 mW (-6 dBm)*	*10*
Lower-distance	*1 mW (0 dBm)*	*N/A*	*1*

1.3 Thesis Outline

In the present section, the key topics discussed in this thesis are presented with a guide to the adopted structure. The thesis has been organized in six chapters (including the introductory chapter), which are summarized as follows:

Chapter 2 - Power Amplifier Basic Concepts

In this chapter important concepts of the power amplifiers are discussed, such as: efficiency, output power, linearity, distortion and an overview about transmitter architectures.

Chapter 3 - Power Amplifiers

The most important classes of RF power amplifiers are presented in this chapter. The conventional and switching mode classes are discussed in the separate sections. In the Section 3.1 summarized mode of operation and relevant theory of the classes such as Class-A, Class-B, Class-AB and Class-C are presented. The Section 3.2, by its turn, presents a general vision for the switching mode classes, such as: Class-D, Class-E and Class-F. The current source, used by conventional classes, and switch mode operation of the transistor are compared in Section 3.3. Finally, a discussion of all classes are summed up into tables giving relevance to the most important characteristics in Section 3.4.

Chapter 4 - Class-A Power Amplifier

This chapter shows the Class-A design and implementation. The simulation results of the implementation using ideal models for the reactive components are presented in Section 4.2.1. In the Section 4.2.2, the simulation results with regard to the implementation with the real models of the inductors and capacitances are shown and compared with the previous results.

Chapter 5 - Class-E Power Amplifier

The biggest focus of this thesis occurs in this chapter, where Class-E is analysed

in more detail. The simplified equations that allow to design the zero-voltage switching (ZVS) Class-E are presented for each mode of operation. This modes of operation are differentiated by the way that the resonant circuits behave and four modes were considered: radio-frequency choke (RFC), parallel-circuit, even-harmonic resonance and subharmonic resonance. The design for each mode of operation of the Class-E PA (considered as output stage of the complete PA design) is performed in Section 5.2.1, as well as the design of the Class-A driver in Section 5.2.2. Finally, the simulations of the two blocks were carried out separately, in Section 5.3.1 and in section 5.3.2, and then put together with a final solution in Section 5.3.3.

Chapter 6 - Conclusions and Future Work

This chapter gives the general conclusions, as well as, possible future development and research referent to the work presented.

1.4 Main Contributions

The main contribution of this thesis is essentially the study, design and implementation of a Class-E power amplifiers, which was targeted to the Bluetooth applications. Additionally, it can be implemented in a wider range of applications. It is expected that the deep study of the Class-E and its design variety, could be taken into account. It is also expectable that this project will provide some guidelines to the power amplifier design for other wireless application, or for the Bluetooth application with different specifications.

CHAPTER 2

POWER AMPLIFIER BASIC CONCEPTS

In order to build the PA, it is first desired to know better its basic concepts. Parameters like efficiency, output power, gain, linearity (1 dB compression point and IP3) and distortion define an RF PA. On the follow of this chapter it will be summarized its definitions, as well as two types of transmitter architectures will be presented.

2.1 Efficiency

The most important key point of the PA is efficiency, which aims to clarify if the PA delivers a certain amount of power without consuming too much power itself. There are three types of efficiencies: drain efficiency, Equation (2.1), conversion efficiency, Equation (2.2) and overall efficiency, Equation (2.3).

Drain efficiency is usually the most used and gives the ratio between output power at fundamental frequency (P_o) and direct current (DC) power consumption of the PA ($P_{DC,PA}$),

$$\eta_d = \frac{P_o}{P_{DC,PA}}. \tag{2.1}$$

Sometimes it is needed to know how much DC power is converted into RF power, hence the utility of conversion efficiency. The primary difference between this kind of efficiency and the first one, is that in conversion efficiency the output power has also in account the output power at other harmonics, so it is called total output power ($P_{o,Tot}$), and conversion efficiency equation is given by

$$\eta_{conv} = \frac{P_{o,Tot}}{P_{DC,PA}}. \tag{2.2}$$

The overall efficiency has a slight difference regarding to drain efficiency, taking into account the DC power consumptions of all driver stages ($\sum_{i=0}^{n} P_{DC,Drive,i}$, where n represents total number of drivers used). From Equation (2.3) it is evident that additional driver stage with DC power consumption will imply lower overall efficiency.

$$\eta_{oa} = \frac{P_o}{P_{DC,PA} + \sum_{i=0}^{n} P_{DC,Drive,i}}. \tag{2.3}$$

Finally, there is another way of measuring efficiency of the PA, which is more realistic, since it takes into account the power input (P_{in}), and it is called power added efficiency (PAE). In other words, PAE measures the efficiency of the PA between the linear and saturated regions, allowing to find the optimal point where the amplifier can maximize the transference of input power to output power, and is given by

$$\begin{aligned} PAE &= \frac{P_o - P_{in}}{P_{DC,PA} + \sum_{i=0}^{n} P_{DC,Drive,i}} \\ &= \eta_{oa} \left(1 - \frac{1}{G_P}\right), \end{aligned} \tag{2.4}$$

where G_P is power gain of the PA.

2.2 Output Power

So that the PA can be driven, it needs a certain amount of RF power input. As a result, the power gain must be determined and it can be expressed in dB as follows:

$$G_P(dB) = 10 \cdot \log_{10} \left(\frac{P_o}{P_{in}}\right). \tag{2.5}$$

Besides the input power P_{in} and the output power P_{out}, there is also the DC power consumption P_{DC}, represented in Figure 2.1, where V_{in} represents input voltage and V_{DD} is DC voltage supply. The P_{DC} power can be simply depicted by

$$P_{DC} = I_{DC} \cdot V_{DD}. \tag{2.6}$$

Regarding the output power, it is important to take into account the connection losses between the PA and the antenna. Since antenna presents a load impedance to the source circuit, usually defined by R_L resistance of 50 Ω, any mismatch between the antenna and output impedance of the source circuit will lead to power dissipation in form of radiation. The total average of the output power can

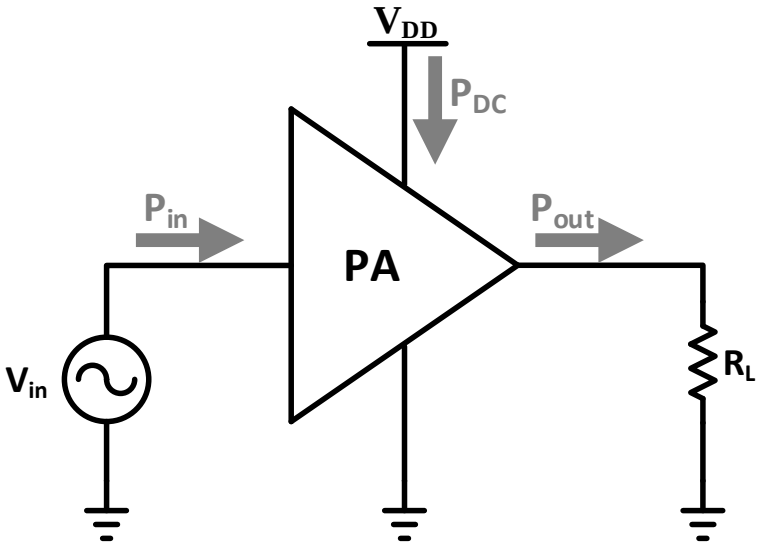


Figure 2.1: Representation of a PA block with the associated powers.

be given by Equation (2.7), where V_{rms} is root mean square (RMS) value of output voltage.

$$P_{o,tot} = \frac{V_{rms}^2}{R_L}. \tag{2.7}$$

However, this is not helpful for the study of a PA, because it represents the output power also at other integer multiples of the fundamental frequency, f_o [2]. In fact, the desirable is to know the average output power at fundamental frequency, which can be obtained by Equation (2.8), where V_o is the amplitude voltage of the sinusoidal output signal at frequency f_o.

$$P_{o,fc} = \frac{V_o^2}{2R_L}. \tag{2.8}$$

2.3 Linearity and Distortion

The linearity of the RF system is of big importance, so it must be measured to understand the impact of the devices non-linearities in the output signal. The main PAs characteristics that allows to measure and improve its linearity and quality factor, are the 1 dB compression point and 3rd order intercept point (IP3) analysis. The relation between the output voltage and the input voltage of a nonlinear PA can be expressed by a Taylor's power series at some operating point [5] as

$$v_{out} = f(v_{in}) = V_{o(DC)} + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + ... + a_n v_{in}^n, \tag{2.9}$$

where $a_1, a_2, ...a_n$ are the n order nonlinear coefficients.

The 1 dB compression point is defined by the point where the linear relationship between the output power and input power is lost. Additionally, being the line slope represented by the gain, the point also identify the gain drop (1 dB) where the input power level can be restricted to prevent signal distortion.

The IP3 value is an imaginary point where the amplitude of the intermodulation (IM) products equals the input signal. These IM effects are caused by non-linear operations. Improving IP3 value, the linearity will increase and will consequently lower the IM distortion.

The effect of 1 dB compression point and of the IP3 can be seen in Figure 2.2, where 1 dB compression point occurs when there is a difference of 1 dB between the ideal linear characteristic and the real characteristic (at fundamental frequency), with IP_{1dB} and OP_{1dB} meaning input and output power at 1 dB compression point, respectively. In its turn, the IP3 occurs when there is the intersection of the idealized responses of output power of the first-order and of the 3rd order IM product. This intersection occurs in the correspondent points of the input power (IIP_3) and of output power (OIP_3). Usually, for good practice, IP3 must be about 10 dB greater than the 1 dB compression point.

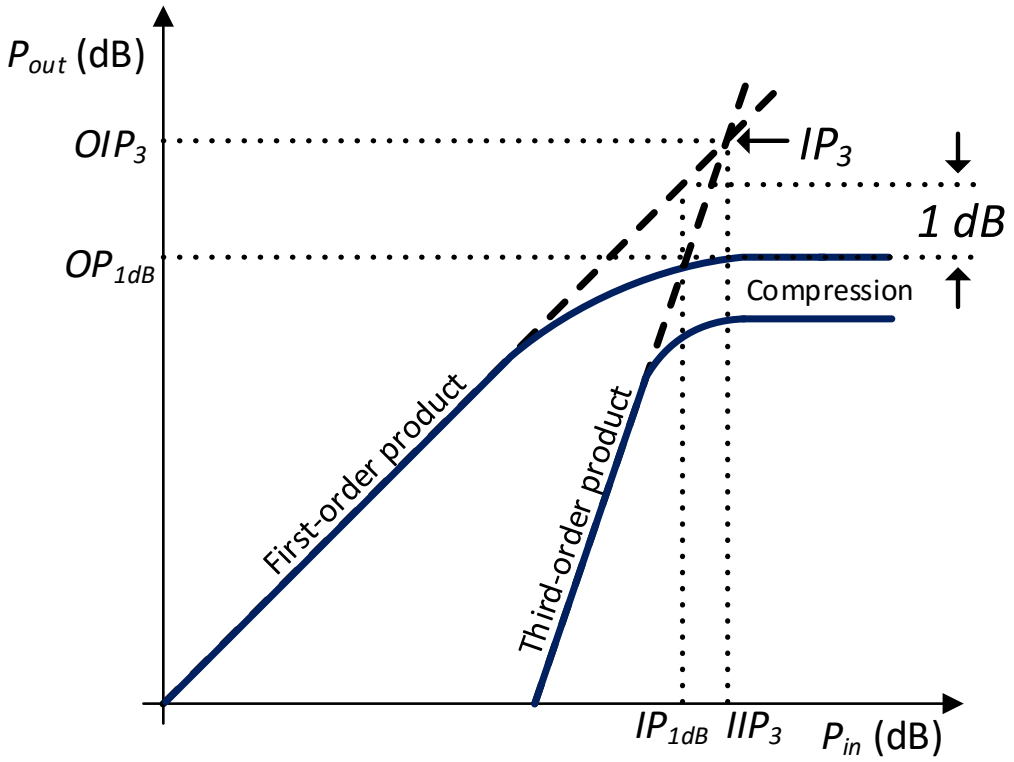


Figure 2.2: 1 dB compression point and 3rd order intermodulation intercept (IP3).

Most of the PAs operate near to the 1 dB compression point in order to achieve higher efficiency, but it suffers from distortion of the higher order harmonics. Such requires that the power of the higher harmonics should be below at least 30 dBm from the power of the carrier frequency, i.e., -30 dBmc. This undesired harmonics may corrupt the signal of interest and can be classified as:

- Harmonics of the carrier frequency: $f_h = nf_c$.
- IM products: $f_{IM} = nf_1 \pm mf_2$.

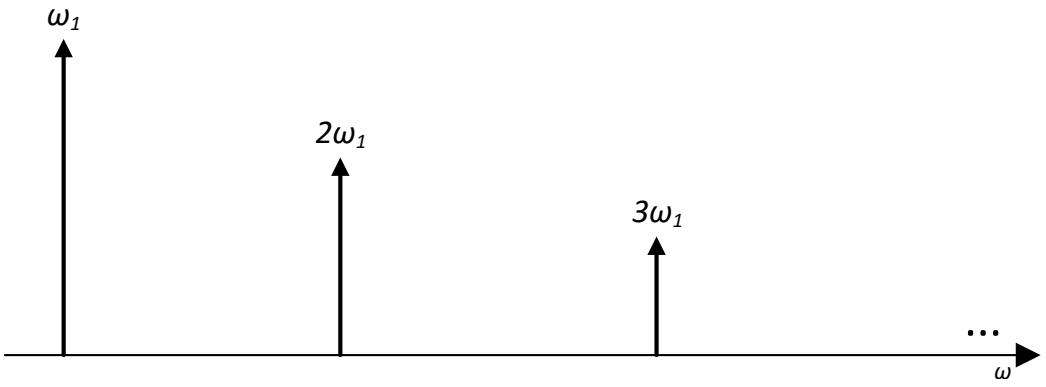


Figure 2.3: Spectrum of the output voltage with harmonics effect.

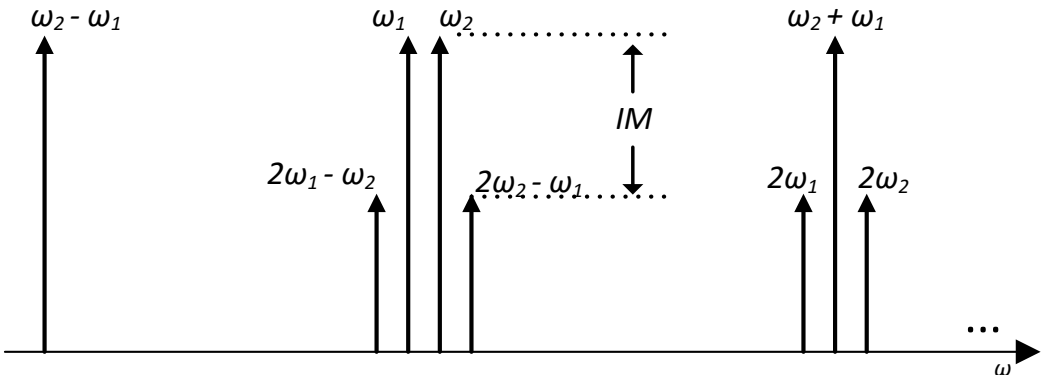


Figure 2.4: Spectrum of the output voltage with the respective intermodulation products.

There is two ways of testing this distortion: one is using a single-tone test and other one is using two-tone test. The first one requires a sinusoidal input signal in the single-frequency and the second requires two sinusoidal input signals, connected in series, of different frequencies [5]. The Figure 2.3 and Figure 2.4 represents the spectrum of the output voltage with respective harmonics.

In the case of the two-tone test, the order of an IM product can be determined by n and m coefficients, where this two coefficients are integers, resulting in

$$order_{(IM)} = n + m. \tag{2.10}$$

Therefore, in the case of the 3rd order IM (IM_3) the products are: $2\omega_1 + \omega_2$, $2\omega_1 - \omega_2$, $2\omega_2 + \omega_1$ and $2\omega_2 - \omega_1$.

The simple way to measure the total distortion of the amplifier with a single-tone test, besides the 1 dB CP and IP3, is through the total harmonic distortion (THD). Whenever the amplifier operates in non-linear region it generates an extra number of harmonics, which may distort the signal of interest.

$$THD = \frac{\sum_{i=2}^{n} P_i}{P_1}. \tag{2.11}$$

2.4 Transmitter

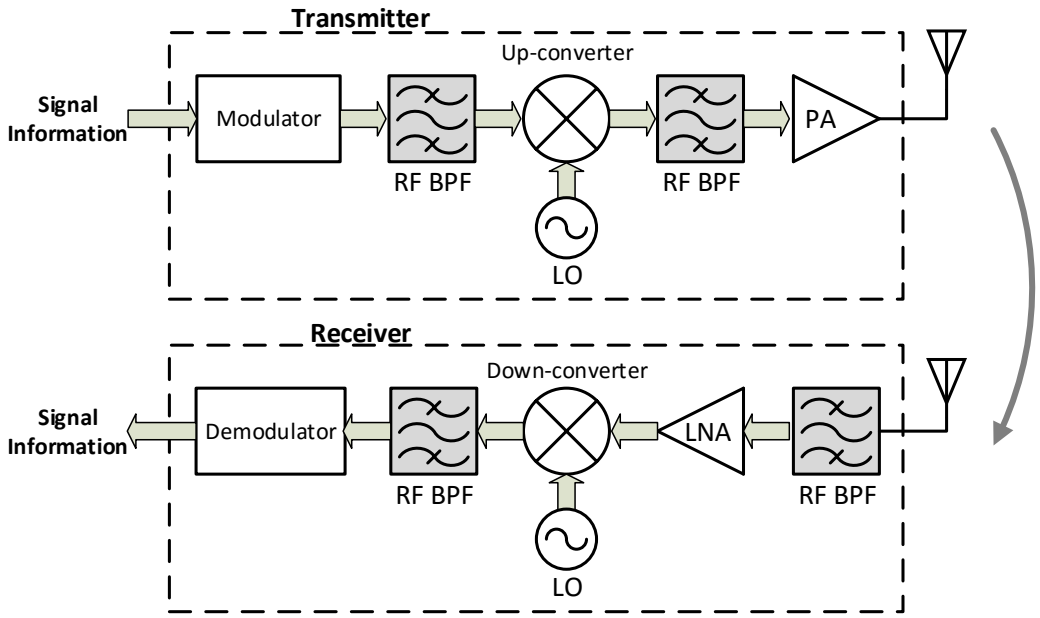


Figure 2.5: Simplified block diagram of the transmitter (top) and receiver (bottom) for wireless communication.

The PA is the last stage, but not the least important of the RF transmitter, quite the contrary, it is the most important block since it is responsible to deliver the signal with high enough power to arrive to its destiny and with its information undamaged, or capable to be recovered.

Since in the wireless communication systems there is no transmitter without the receiver, it is shown in Figure 2.5 the block diagram of the receiver and transmitter to give an overall idea of the complete wireless transceiver.

Giving more emphasis to the transmitter, there are two typical architectures: Heterodyne upconversion and Direct upconversion. Each of them has a digital signal processor (DSP), digital-to-analog converter (DAC), Mixers (represented by X symbol), local oscillator (LO) and PA.

2.4.1 Heterodyne Upconversion

The heterodyne upconversion architecture, sometimes called as 2-step upconversion, is the most often used in the transmitters, represented in Figure 2.6. Since in nowadays systems transmit data in the form of quadrature baseband signals, the transmitter must be able to processes this signal. As a result, the signal is processed in the DSP where signal is split into the in-phase, I, and quadrature, Q, channels. These are converted to analog trough DAC and latter are upconverted to the RF signal, carrier frequency.

This architecture, in particular, has distinction in using the intermediate frequency (IF) to process quadrature modulation, up-converting to $\omega_{IF} + \omega_{LO}$, usually using two mixers and two LO signals with phase differentiated by 90º. Then, first bandpass filter (BPF) suppresses the IF harmonics, while the second BPF removes the unwanted mirrored sideband, $\omega_{IF} - \omega_{LO}$. This architectures brings as the main advantage not having LO pulling, compared with the direct upconversion [6, 7].

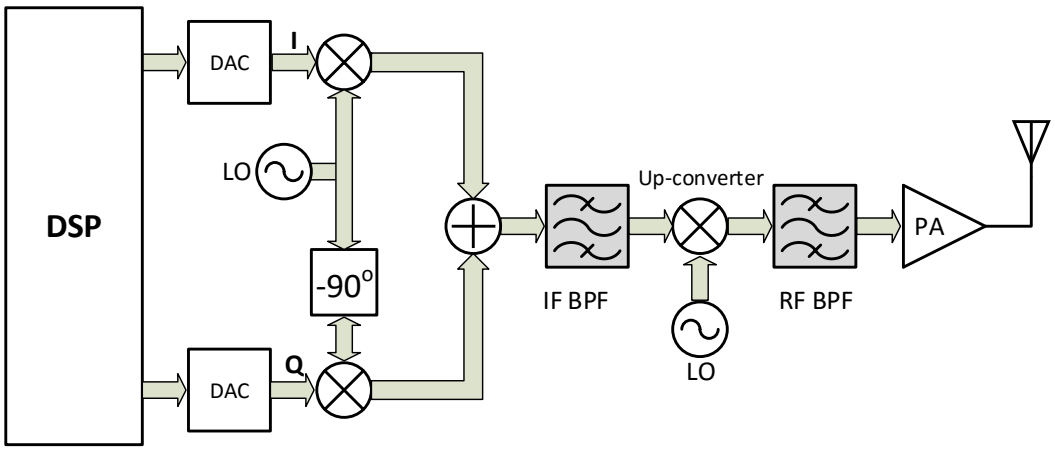


Figure 2.6: Block diagram of the Heterodyne transmitter.

2.4.2 Direct Upconversion

Direct upconversion transmitter, can be also called as homodyne upconversion, is defined principally by having its carrier frequency equal to the LO frequency. By this means that the signal from the baseband is directly upconverted to the carrier frequency. This architecture is shown in Figure 2.7, which seems to be very simple, but this presents a drawback of introducing LO pulling. In other words, putting the PA close to the LO, in terms of frequency domain, causes injection of the PA noise into the spectrum of the LO, which may stay "locked" if the noise increase. However, modern direct conversion have tried to alleviate this effect by moving the output spectrum of the PA far from the LO frequency [6, 7].

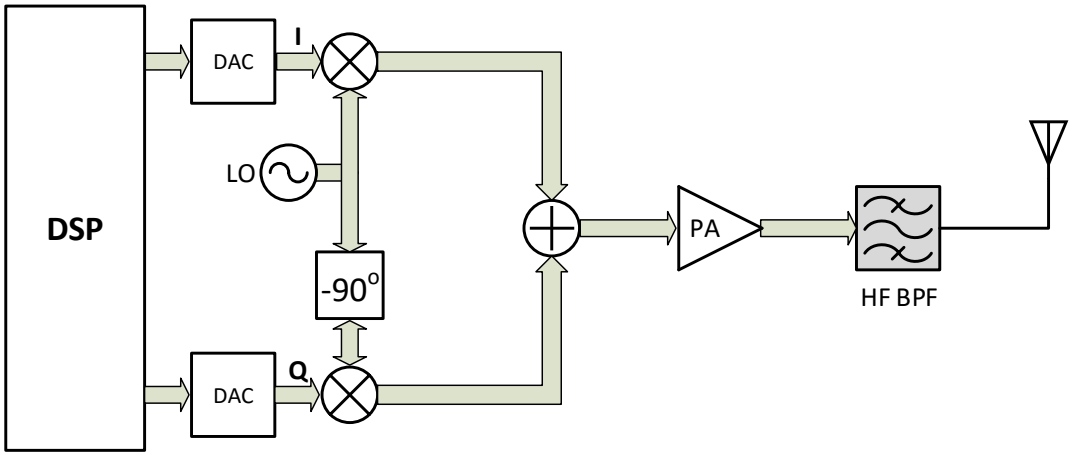


Figure 2.7: Block diagram of the Heterodyne transmitter.

The PA blocks plays a big role in both architectures, as the output power from quadrature usually is too low for radio transmission, so there is a need to amplify the signal before being transmitted to the antenna. Thus, this block is the one that defines the bigger power consumption of the transmitter, as well as the one that must comply to the requirements of the targeted application.

CHAPTER 3

POWER AMPLIFIERS

There are many ways to classify the power amplifiers, but the most important is by their class of operation, which essentially depends on trade-off between linearity, efficiency, signal gain and output power of the PA.

There are classes named alphabetically from A to T and they can be lumped into two basic groups: conventional amplifiers (A, AB, B and C) and switching mode amplifiers (D, E, F ...). The last group is mostly preferred by the wireless systems, despite of its amplitude non-linearities, because those amplifiers can achieve higher efficiency. Amplitude linearity is not necessarily needed, since phase modulation is greatly used by these systems. As a consequence, the amplitude non-linearities do not affect those wireless systems, but phase linearity does, and non-linear amplifiers can provide that [2].

The following sections describe those two groups in some detail, bearing in mind that the design of the RF power amplifier assumes CMOS technology, MOS transistors and its equations are used to explain each class operation. But that does not mean that the classes operation are not adaptable to a different technology.

3.1 Conventional Amplifiers

The group of conventional amplifiers is defined as the one that mostly has not only phase linearity but also amplitude linearity. This means that all input and output waveforms are assumed to be sinusoidal. However, if this assumption is not verified, i.e. the output waveform is not sinusoidal, it is possible to achieve better performance of the PA [8]. This allows the distinction between the classes

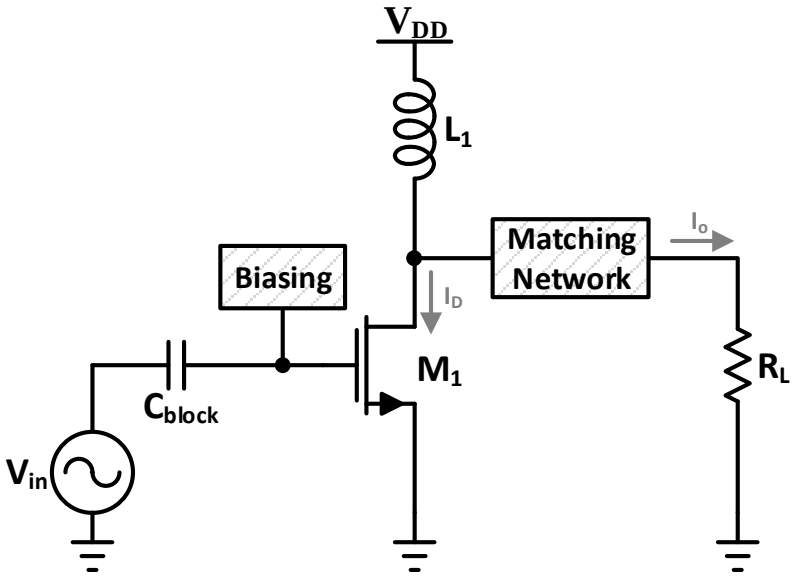


Figure 3.1: Classical RF PA with inductive load

within the group of conventional amplifiers, turning the conduction angle into a concept with great importance. The conduction angle, θ, varies between 0 and 2π (or in degrees: between 0 and 360), and defines the duration of the period in which the given transistor is conducting, where 2π (or 360^o) corresponds to the full cycle of conduction.

All these classes, named alphabetically from A to C, can be implemented using the same circuit, depicted in Figure 3.1, where C_{block} is a DC blocking capacitor, L_1 is a load inductor, R_L represents load impedance of the antenna and M_1 is an output transistor that operates as a controlled current source. The bias voltage at the gate is the one that allows to shape the current conduction angle and therefore differentiate those classes. A load inductor is preferred over a resistor, because if the radio-frequency choke (RFC) inductor is used the voltage drop trough this inductor will be practically zero. The RFC inductor is also desired because of its definition of passing DC current and blocking everything else. For that purpose, the RFC must have large enough inductance in order to pass DC current ripple and block or reduce significantly the alternating current (AC) current ripple.

3.1.1 Class-A

The Class-A PA is the most classical RF power amplifier and its principal characteristic is having the transistor, biased and driven in such way, that it never turns

off, i.e. it will conduct during all of its conduction angle, which is 360º. This is why, between all the classes, this one is the most linear. The CMOS transistor must operate in the active region (saturation region) and so its drain current is given by the square law

$$i_D = \frac{1}{2}K_n(\frac{W}{L})(v_{GS} - V_{th})^2 \quad for \quad v_{GS} \geq V_{th} \quad and \quad v_{DS} \geq v_{GS} - V_{th}, \tag{3.1}$$

where L and W are the channel length and width of the transistor, respectively, v_{GS} is gate-to-source voltage, V_{th} is the threshold voltage, v_{DS} is drain-to-source voltage and

$$K_n = \mu_{n0}C_{ox}, \tag{3.2}$$

where μ_{n0} is the low-field surface electron mobility in the channel, $C_{ox} = \epsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area of the gate, t_{ox} is the oxide thickness, $\epsilon_{ox} = 0.345\ pF/cm$ is the silicon oxide permittivity [5].

Typically it is used the topology shown in Figure 3.1 with the addition of a LC parallel-resonant circuit (as illustrated in Figure 3.2 by L_o and C_o) and also a coupling capacitor C_c, which may be included in the matching network. The parallel-resonant circuit is used for the narrowband Class-A RF PA to suppress the undesired harmonics and filter the narrowband spectre of the signal. Although this is not need for the wideband power amplifiers. In its turn, the coupling capacitor, which is also known by DC-blocking, ensures that only AC current is flowing through the load resistor R_L.

Supposing that the AC input signal is a sinusoidal wave, the output voltage will have a sinusoidal wave too and the power in the load, or output power, will be given by

$$P_o = \frac{V_o^2}{2R_L}, \tag{3.3}$$

where V_o is the amplitude (or peak value) of the sinusoidal output voltage. Recalling the formula of the drain efficiency:

$$\eta_d = \frac{P_o}{P_{dc}}, \tag{3.4}$$

and having into account that the maximum drain efficiency occurs at the maximum output power, which in turn is maximum at the maximum output voltage, since the value of the R_L is a constant. Maximum output voltage occurs when the transistor drain current is almost zero, considering ideal components, where L_1 inductance is an RFC and then the current from the supply will flow completely to the load, maximum output voltage is then equal to V_{DD}. Having that, the

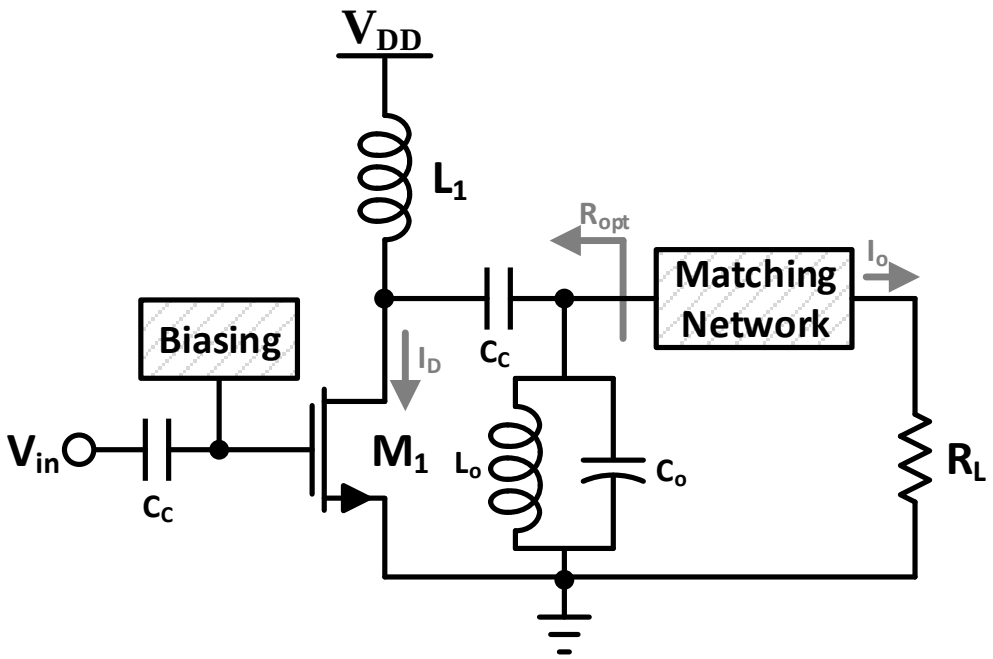


Figure 3.2: Class A stage

maximum theoretical drain efficiency results into 50 % [9], as demonstrated in Equation (3.5).

$$\eta_{d(max)}(\%) = 100 \times \frac{V_{o(max)}^2/(2R_L)}{V_{DD}I_{DC}} = 100 \times \frac{1}{2}\left(\frac{V_{o(max)}}{V_{DD}}\right)^2 = 50\ \%. \tag{3.5}$$

The drain current can be expressed as

$$i_D = I_D + i_d = I_D + I_{pk} \cdot cos(\theta), \tag{3.6}$$

where I_D is the DC component of the drain current, i_d is the AC component of the same and its peak amplitude is defined by I_{pk}.

The drain current and drain-to-source voltage are represented in Figure 3.3, that considers maximum voltage swing (by ignoring pinch-off voltage, which defines the division between the saturation and the linear region of the transistor) and ideal components, where

$$I_{D(max)} = 2 \cdot I_{pk(max)} = 2 \cdot I_{DC}, \tag{3.7}$$

$$V_{DS(max)} = 2 \cdot V_{o(max)} = 2 \cdot V_{DD}. \tag{3.8}$$

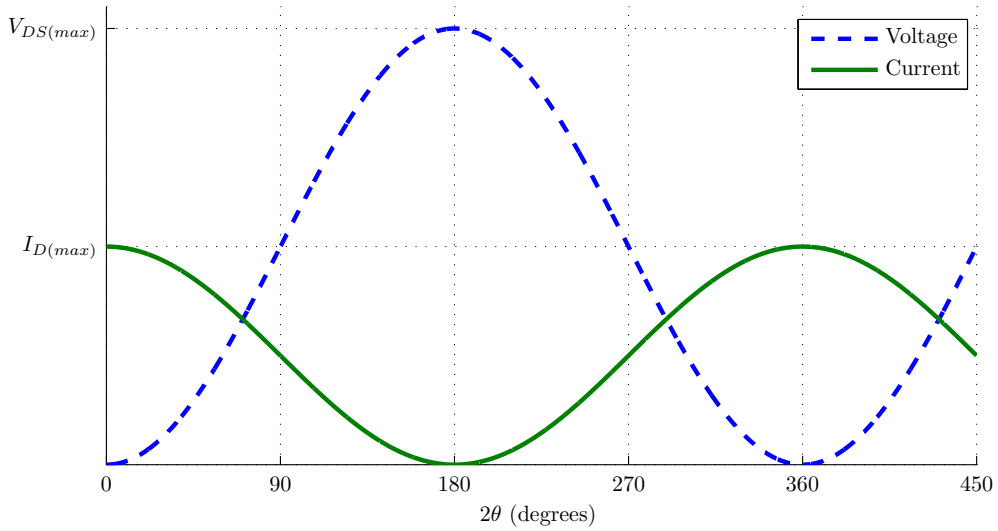


Figure 3.3: Class-A ideal drain voltage and current waveforms

By a proper managing of the Equations (3.7) and (3.8) into a general equation of the output power capability it results into

$$c_p = \frac{P_{o(max)}}{V_{DS(max)} I_{D(max)}} = \frac{1}{2} \cdot \frac{V_{o(max)} I_{o(max)}}{V_{DS(max)} I_{D(max)}} = \frac{1}{8} = 0.125. \tag{3.9}$$

To sum up, the Class-A RF power amplifiers can achieve high linearity, producing an amplified replica of the input voltage or current waveforms, at the expense of poor efficiency.

3.1.2 Class-B

Higher efficiency is achieved by reducing the conduction angle, i.e., transistor do not conduct the drain current all the time. This way, the power dissipation of the transistor is reduced, since the multiplicative factor of the drain-to-source voltage by the drain current is decreased.

The Class-B RF power amplifiers is the category on which the transistor conducts only during half of its period, or by other words, the drain current waveform has a conduction angle of 180^o and so has a sinusoidal wave during only for half of its period. To achieve that, the transistor must be biased close to the threshold voltage value (V_{th}), so that the transistor can exchange its operation quickly between cut-off and active region.

It can be designed with the same topology of the Class-A, with high Q LC resonant circuit, in order to shunt the undesired harmonics to ground and this way to obtain a sinusoidal voltage. Other circuit topology used for this class PA is

using two transistors instead of one, with each of them delivering a half sinusoidal voltage and the transformer will recover the full sinusoid at the load.

Like in Class-A amplifier, the maximum peak value of the output voltage reaches V_{DD} and leads to the maximum drain efficiency of 78.5 %, which also can be calculated as follows (further demonstration can be seen in [5]):

$$\begin{aligned}\eta_{d(max)}(\%) &= 100 \times \frac{V_{o(max)}^2/(2R_L)}{2V_{o(max)}V_{DD}/(\pi R_L)} = 100 \times \frac{\pi}{4}\frac{V_{o(max)}}{V_{DD}} \\ &= 100 \times \frac{\pi}{4}\frac{V_{DD}}{V_{DD}} = 100 \times \frac{\pi}{4} =\simeq 78.5\ \%.\end{aligned} \tag{3.10}$$

The maximum drain current, in this case, increases by a factor of π relatively to the supply current, I_{DC}, but the maximum drain-to-source voltage remains twice of the V_{DD}.

$$I_{D(max)} = 2 \cdot I_{pk(max)} = \pi \cdot I_{DC}, \tag{3.11}$$

$$V_{DS(max)} = 2 \cdot V_{o(max)} = 2 \cdot V_{DD}. \tag{3.12}$$

Under the same considerations mentioned at the Class-A definition, the drain current and the drain-to-source voltage of the Class-B RF power amplifier are presented in the Figure 3.4.

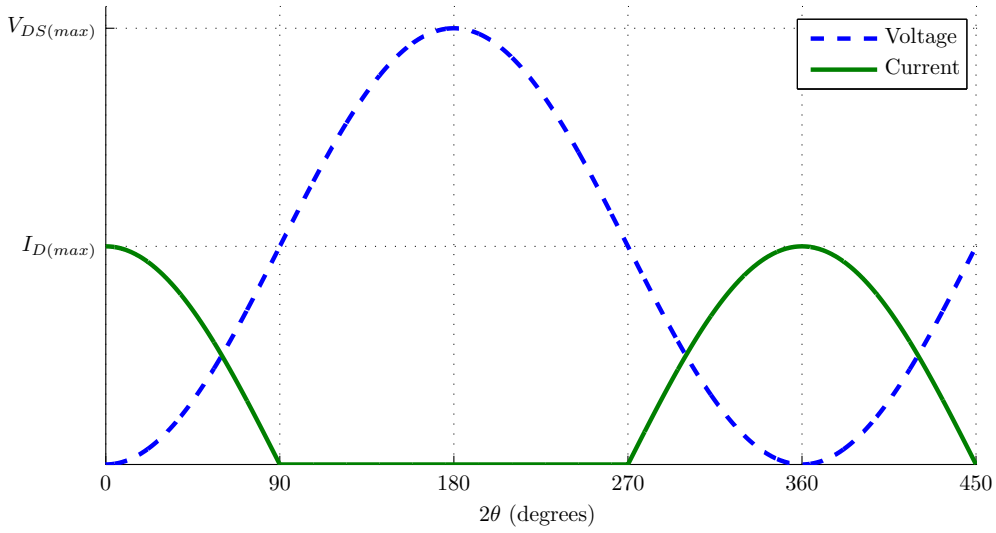


Figure 3.4: Class-B ideal drain voltage and current waveforms

As the relation between $V_{DS(max)}$, $I_{D(max)}$ and $V_{o(max)}I_{o(max)}$ did not change comparatively to the Class-A, the output power capability of the Class-B RF power amplifiers remains the same

$$c_p = \frac{P_{o(max)}}{V_{DS(max)}I_{D(max)}} = \frac{1}{2} \cdot \frac{V_{o(max)}I_{o(max)}}{V_{DS(max)}I_{D(max)}} = \frac{1}{8} = 0.125. \tag{3.13}$$

The efficiency is improved, however there are always drawbacks together with the benefits. The turning off the transistor creates higher undesired harmonics, as well as the transistor becomes less linear. In the Class-A it was referred to the use of the parallel-resonant circuit, but it takes more importance now. Thus, higher quality of these components is desired in order to better suppress those harmonics, which can be calculated as follows:

$$L_o = \frac{R_{opt}}{Q_L \cdot \omega_o}, \tag{3.14}$$

$$C_o = \frac{Q_L}{R_{opt} \cdot \omega_o}, \tag{3.15}$$

where Q_L is loaded quality of the parallel-resonant circuit at frequency of work, ω_o, and R_{opt} is an optimum value for the desired output power before matching.

3.1.3 Class-AB

The Class-AB RF power amplifiers, as the name suggests by itself, is the category which fits between the Class-A and Class-B and therefore its conduction angle is in the range of 180º to 360º, as well as the efficiency lays between 50 % and 78.5 %. This category allows to choose the better trade-off between the efficiency and linearity, i.e., a power amplifier that could be more linear than the Class-B and more efficient that the Class-A.

The waveforms of the drain current and drain-to-source voltage that exemplify Class-AB RF power amplifiers operation is showed in Figure 3.5

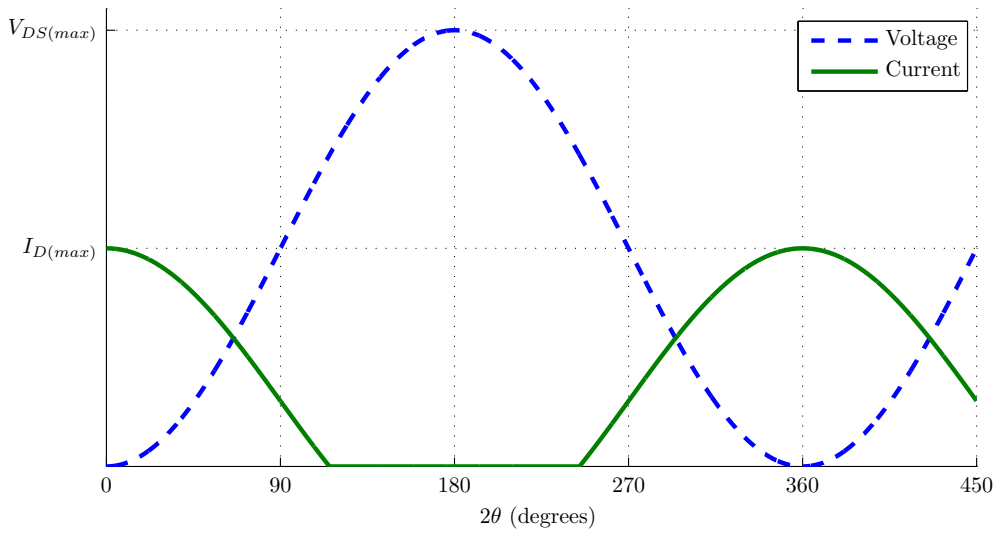


Figure 3.5: Class-AB ideal drain voltage and current waveforms

Further equations are presented in Section 3.1.4, Class-C, as they are common to both Class-AB and Class-C power amplifiers, since it is only the range of the conduction angle that differentiates them from what they are.

3.1.4 Class-C

The last category of the conventional power amplifiers, and the less linear, is the Class-C. This one has its transistor biased to operate mostly in the cut-off region and therefore its conduction angle is below 180 %. This one is even more efficient than the previous classes, which reaches efficiency range from 78.5 % to 100 %. For some applications it is desirable to have more efficiency in exchange of its linearity. The radio station could be an example, which need to transmit large powers with an efficient operating mode.

The maximum drain and maximum drain-to-source voltage in function of conduction angle are

$$I_{D(max)} = I_{pk(max)} \cdot 2\pi \cdot \frac{1 - cos(\frac{\theta}{2})}{\theta - sin(\theta)}. \tag{3.16}$$

An example of the drain current and drain-to-source voltage waveforms are illustrated in Figure 3.6.

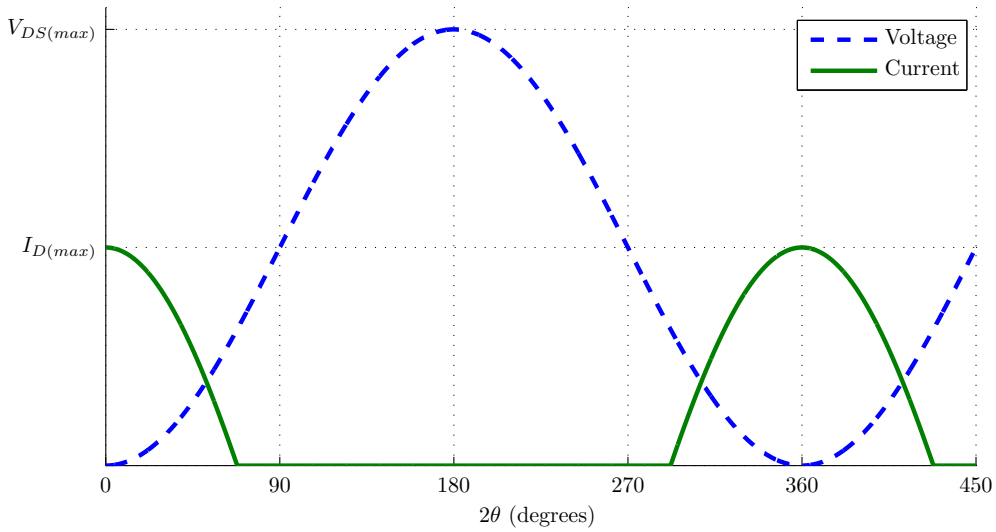


Figure 3.6: Class-C ideal drain voltage and current waveforms

The maximum drain efficiency, $\eta_{D(max)}$ is now in function of conduction angle [9], as given by

$$\eta_{D(max)}(\%) = 100 \times \frac{\theta - sin(\theta)}{4 \cdot \left(sin(\frac{\theta}{2}) - \frac{\theta}{2} \cdot cos(\frac{\theta}{2}) \right)}, \tag{3.17}$$

where θ is the conduction angle, the equality $V_{DS(max)} = 2V_{DD}$ and zero pinch-off voltage are still taken into account. This function is also valid for other conventional classes.

In the same way, output power capability can be calculated,

$$c_p = \frac{1}{8\pi} \times \frac{\theta - sin(\theta)}{1 - cos(\frac{\theta}{2})}. \tag{3.18}$$

The drain efficiency and the output power capability functions are shown through a plot in Figure 3.7.

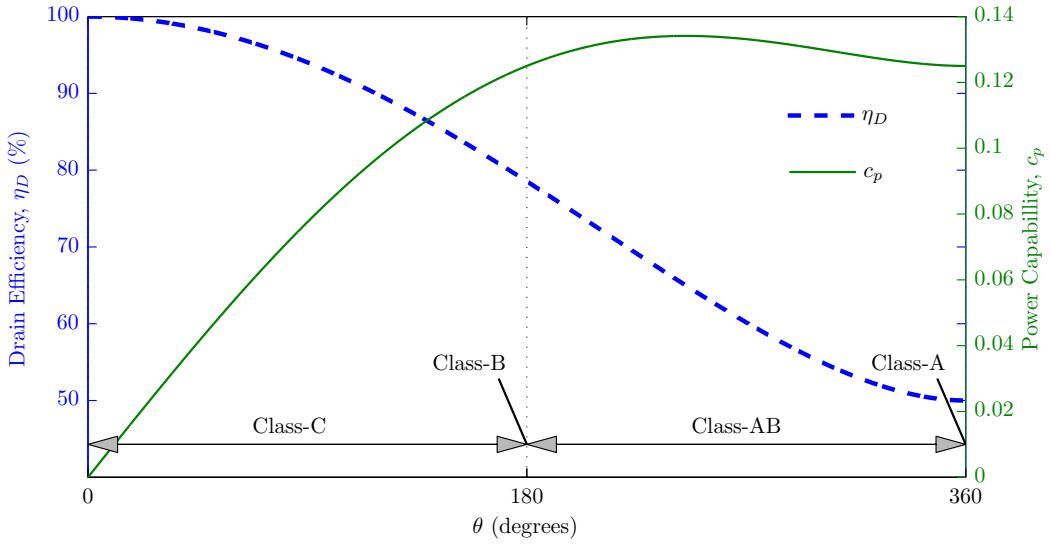


Figure 3.7: Drain efficiency and power capability in function of conduction angle

Analysing this plot (Figure 3.7), it is possible to sum up what already have been told in these sections, that is: conventional classes are categorized in function of conduction angle, and as it decreases the efficiency is increased. But at the same time, the output power capability decreases, which also means that the maximum output power decreases too. So, there will be always a trade-off between efficiency, output power and linearity.

3.2 Switching Amplifiers

Switching amplifiers are the ones that have no amplitude linearity and transistors operate as switch or in overdriven mode, in such way that the transistor is either on or off. In the on state the transistor must operate in triode region (more about the transistor operating regions can be consulted in Appendix B), its drain-to-source voltage is zero and its drain current is determined by the load circuit. In its turn, in

the off state, the transistor operates in cut-off region and opposite waveforms are acquired, i.e. drain current is zero and drain-to-source voltage is determined by load circuit [5]. In the ideal cases, where the transistor behaves like an ideal switch and ideal passive components are considered, there is no overlap in time between the current and voltage, and so there is no power dissipation, which leads to 100 % of drain efficiency. Of course that happens only theoretically, because there are no ideal components in practice, even so, this group of amplifiers are much better when high efficiency is needed.

In this section, the most "popular" switching power amplifiers will be discussed, such as Class-D, Class-E and Class-F. As the Class-E RF power amplifiers are the main object of this thesis it will be discussed in more detail in Chapter 5, a chapter dedicated only to its theoretical study and its design. Even so, a brief analysis of Class-E is described in this chapter.

3.2.1 Class-D

Class-D power amplifiers can be classified into two groups [10]:

- voltage-mode Class-D (VMCD) with series-resonant circuit;
- current-mode Class-D (CMCD) with parallel-resonant circuit.

Typically, both groups use two transistors that operate in a push-pull switching pair and very similarly to an CMOS inverter. The VMCD produces voltage across transistors with square wave and half-wave sinusoid current. In case of the CMCD opposite is produced: a square wave current and half-wave sinusoid voltage. Both transistor are driven by a square input wave and the output signal is tuned to the fundamental frequency. The circuit topology for each Class-D mode and its principal waveforms are represented in Figure 3.8.

In [5, 11, 12, 13] detailed study and comparison between them two are made. Their theoretical analysis and implementation made possible to conclude that whereas the VMCD has the inability to work at high-frequencies, the CMCD can achieve higher frequencies with help of ZVS condition, the one that makes a huge influence in Class-E, as it will be seen in shortly. This inability of the VMCD occurs because the parasitic reactances induced by the two transistors lead to substantial power loss at higher frequency.

Even if VMCD can not achieve high frequency, it can achieve high-voltage at the output, as the voltage drop through the transistors is low, and thus, this one is good for other types of applications in lower frequency that require high-voltage.

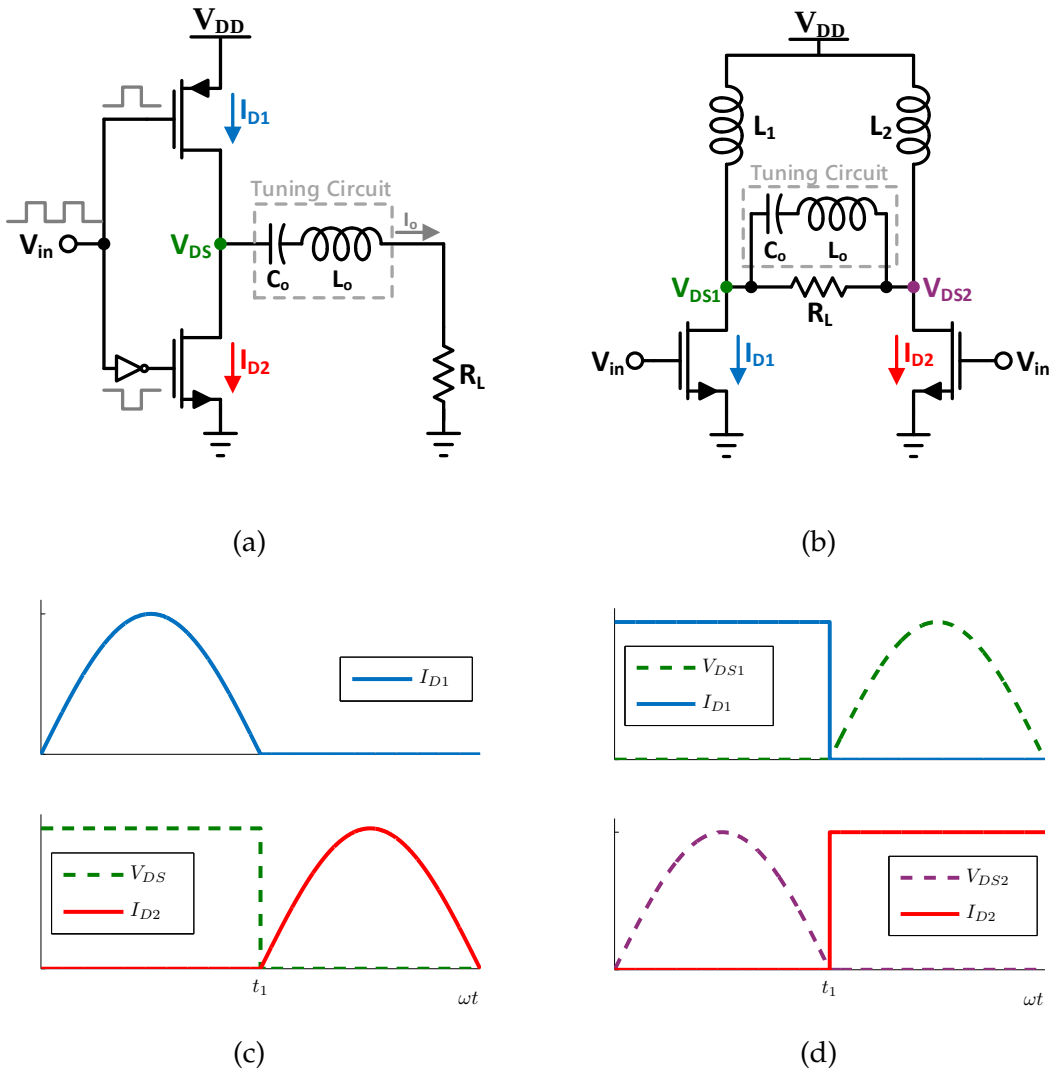


Figure 3.8: The Class-D power amplifiers: (a) VMCD, (b) CMCD and their respective currents and voltages

3.2.2 Class-E

Class-E power amplifiers has the same functions of the Class-D, though using only one transistor. There are two types of Class-E as well: zero-voltage switching (ZVS) and zero-current switching (ZCS). More detailed information about them and their equation are discussed in Chapter 5. The most basic circuit of this class in ZVS mode is shown in Figure 3.9.

Initially the switch is turned on and charges L_1 inductance, which may be an RFC or a finite DC-feed inductance, maintaining zero output voltage. When the transistor is switched off and a pulse of current is applied to the output tuning circuit, this circuit then determines how the system will behave. It is to mention

that the capacitance C_1 is used in ZVS mode, allowing a soft-switching. A hard-switching happens in ZCS mode, where abrupt voltage drop through the transistor occurs from high value to zero, this causes a lower efficiency in the ZCS mode, and therefore, the ZVS is more preferable. Given these points, the design of the shunt capacitance C_1 plays a big role, when it comes to avoid power loss on the transistor [14]. This capacitance absorbs, so to speak, the voltage through the transistor when it is on, and this way, avoids overlapping between voltage and current waves, consequently, minimizes the product voltage-current. Ideally this product would be always zero and hence, there would be no power dissipation, leading to the efficiency of 100 %.

The $V_{Biasing}$ voltage represented in Figure 3.9 plays a big role, because it defines the V_{GS} voltage of the transistor M_1 and consequently defines its operation region.

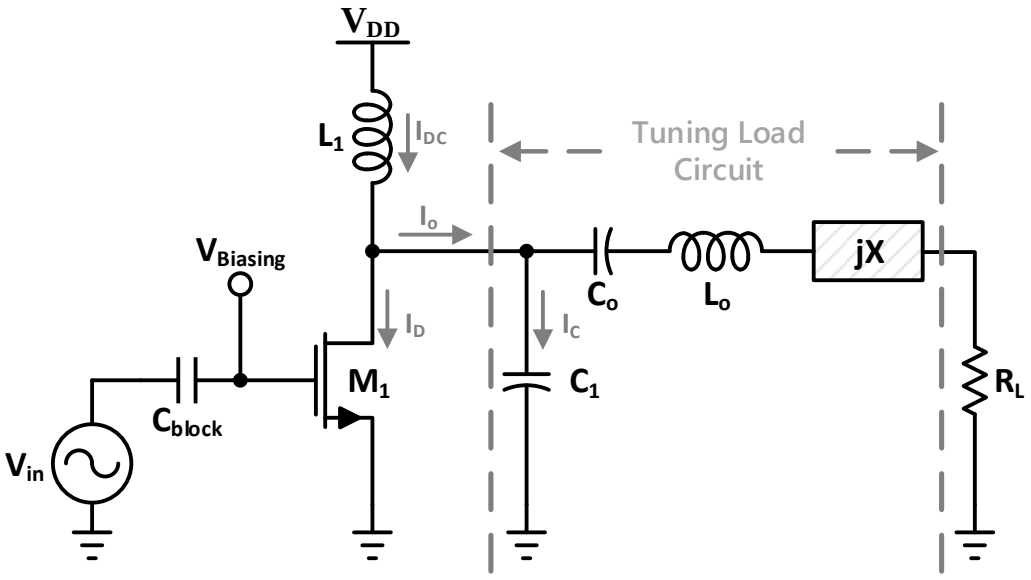


Figure 3.9: Basic topology of the ZVS Class-E power amplifier.

3.2.3 Class-F

Similar to the Class-E, the Class-F amplifier employs drain voltage or current waveform shaping to achieve a high efficiency. It is defined principally by a load network with resonance at one or more harmonics of the operating frequency as well as at the operating frequency itself. The harmonic control techniques allow to specify which termination each harmonic would have. The even and the odd harmonics can see either an open and a short circuit or a short and an open

circuit, respectively. This way, the undesired harmonics are eliminated and only a fundamental harmonic is seen at the load.

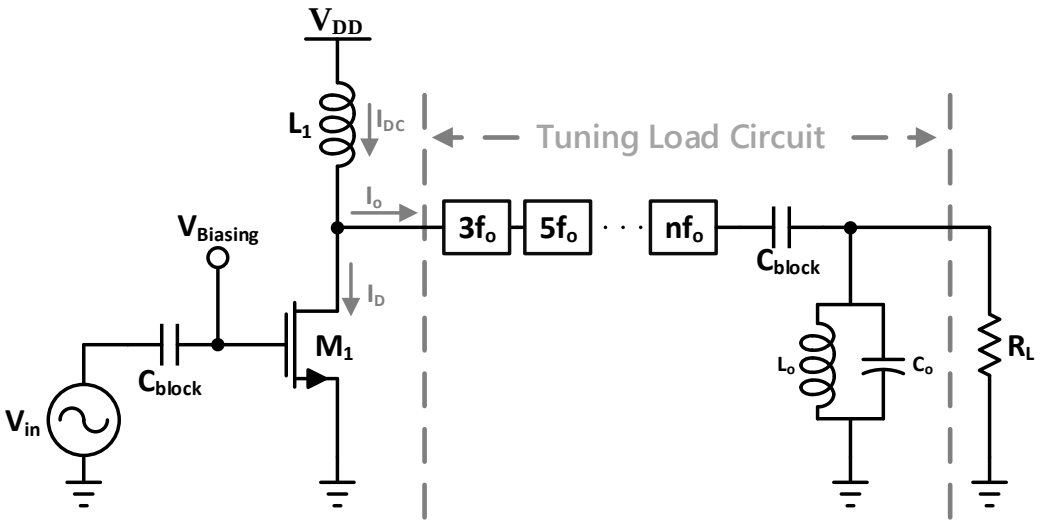
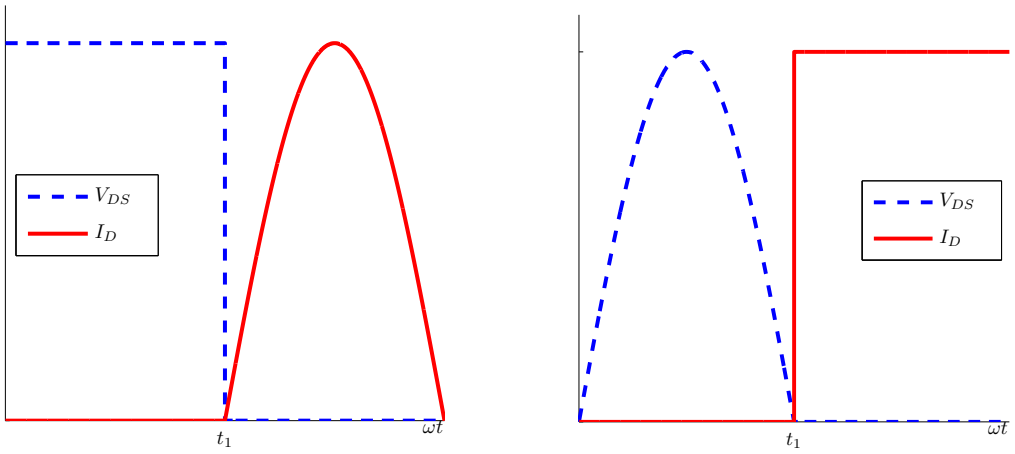


Figure 3.10: Basic topology of the Class-F power amplifier.

If open circuits are chosen for the odd harmonics, as represented in Figure 3.10 by $3f_o, 5f_o, ...nf_o$ filter blocks, the square wave is obtained for the output voltage. The load network on this case is defined by parallel-resonant $L_oC_oR_L$ circuit tuned to the operating frequency f_o and n number of parallel-resonant circuits tuned to the n number of odd harmonics, all of them connected in series. This implies that the parasitic impedances of the transistor end up in parallel with short-circuits, making them negligible [15].

If the opposite is chosen, i.e., short circuit for the odd harmonics, the square wave is obtained for the output current. This results in a zero impedance in each resonant circuit and an infinite impedance at even harmonics [14]. But, usually, the square voltage is preferred.

The current and voltage waveforms for the first case are represented in Figure 3.11a and for the second case in Figure 3.11b. The idealized square waves are obtained with the assumption that a infinite harmonic tuning is used, but this is not possible in practice. Thus, sometimes the circuit at the higher harmonics has an unexpected behaviour, consequently the waveforms lose its square form which leads to power dissipation.



(a) (b)

Figure 3.11: The Class-F drain current and drain-to-source voltage: (a) square voltage, (b) square current.

3.3 Current Source Versus Switched-Mode Operation

Unwilling to seem redundant, the difference between these two modes of operation is mainly the same as the difference between a switch and an high impedance current source. Typically, Class-A and Class-B topologies are considered as linear PA's, despite, not just they lack consistency, but also they keep modelling for small-signals approaches of amplifiers that operate in the large-signal regime. In this subsection, the differentiation between the current source and switched-mode operation, in terms of their large-signal currents and voltages, will be made. Furthermore, it will be possible to divide the current source into pulse-current (PU) operation and continuous wave (CW) operation, as was differentiated by the group of the conventional amplifiers. The most important difference between both modes of operation (current source and switch) during conduction, is the range of voltages that are available on the transistor [16].

- Working in switched-mode: the transistor is cycled between triode region (low impedance conduction) and cut-off (that is an high impedance state) (more about the transistor operating regions can be seen in Appendix B).

  - When $V_{DS} \leq (V_{GS} - V_{th})$, for $I_D \neq 0$, is possible to enter the triode region. This regime of operation is shown in the far left of the Figure 3.12.

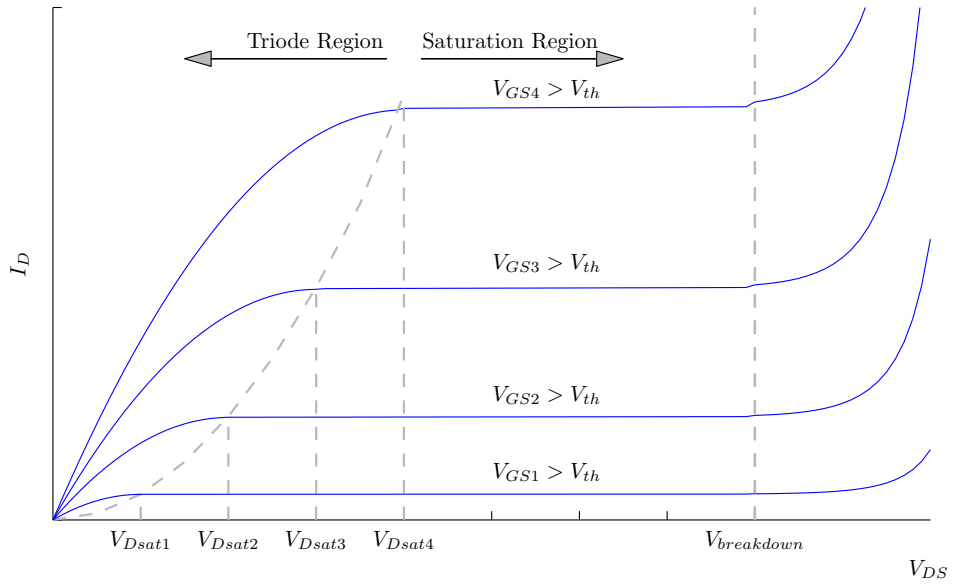


Figure 3.12: Characteristic curves of drain current versus drain-to-source voltage.

In low impedance conduction, the voltage through the transistor, V_{DS}, is as low as possible.

- When the device is cut-off, means that the voltage can freely cross the horizontal axis while the current remains zero.

- Operating as a current source: the transistor can be driven in the two modes of conduction presented early, the continuous or the pulse-current one.
  - For the CW conduction, the device is biased at a finite current and voltage. From there, as long as the triode region is avoided, with V_{DS} preventing to reach breakdown voltage, V_{DS} and I_D are free to assume any non-zero value.
  - The PU operation is comparable to switched-mode, the device is cut-off during portion of the cycle. But otherwise, the voltage across the device is likely to be under the same conditions as in continuous conduction of a current source.

3.4 Discussions

To conclude the overview on RF power amplifiers, in Table 3.1 are presented the relevant characteristics of the discussed PA classes.

Table 3.1: Most important characteristics of the linear and switching mode power amplifier classes.

	Class-A	Class-AB	Class-B	Class-C
Conduction Angle (^{o})	*360*	*180 $\sim$ 360*	*180*	*0 $\sim$ 180*
Ideal Efficiency, $\eta_d(\%)$	*50*	*50 $\sim$ 79*	*79*	*79 $\sim$ 100*
Linearity	*Good*	*Good*	*Moderate*	*Weak*
Maximum Power Capability	*0.125*	*0.134*	*0.125*	*0.125*
Gain	*Large*	*Large*	*Moderate*	*Low*
	Class-D	Class-E	Class-F	
Ideal Efficiency, $\eta_d(\%)$	*100*	*100*	*100*	
Linearity	*poor*	*poor*	*poor*	
Gain	*small*	*small*	*small*	

As have been seen in this chapter, the number of solutions for highly efficient RF power amplifier is big, principally for the switching amplifier. Even so, a more complex design, analysis and modelling of the transistors are required for this group of amplifiers.

CHAPTER 4

CLASS-A POWER AMPLIFIER

Class-A is the simplest power amplifier, not only because of its simple design, but also because of its simple implementation. Moreover, the understanding of its operation mode and of its design is crucial to comprehend all other classes, which originate from this basic design with addition of some specific biasing, driving or tuning circuits.

This chapter has no intention to repeat the theory of the Class-A, as it was discussed in the previous chapter, but it aims to present a simple design and implementation of the Class-A, with and without real reactive components. The main focus is given primarily to the comparison of the simulation results using ideal LC components and using real models. In this regard, Planar Inductor RF and Planar MIM Capacitor RF models are used. This type of RF power amplifier is implemented in 130 nm CMOS technology with voltage supply of 1.2 V at frequency of 2.4 GHz.

4.1 Implementation of the Class-A Power Amplifier

4.1.1 Design of Class-A Power Amplifier

The amplifier design consists in a basic single-ended PA with a common source accomplished by an inductive load. To properly set the DC conditions, a current mirror is used as biasing circuit. Circuit schematic is shown in Figure 4.1.

In order to proceed to the circuit design it is important to establish the desired specifications (Table 4.1).

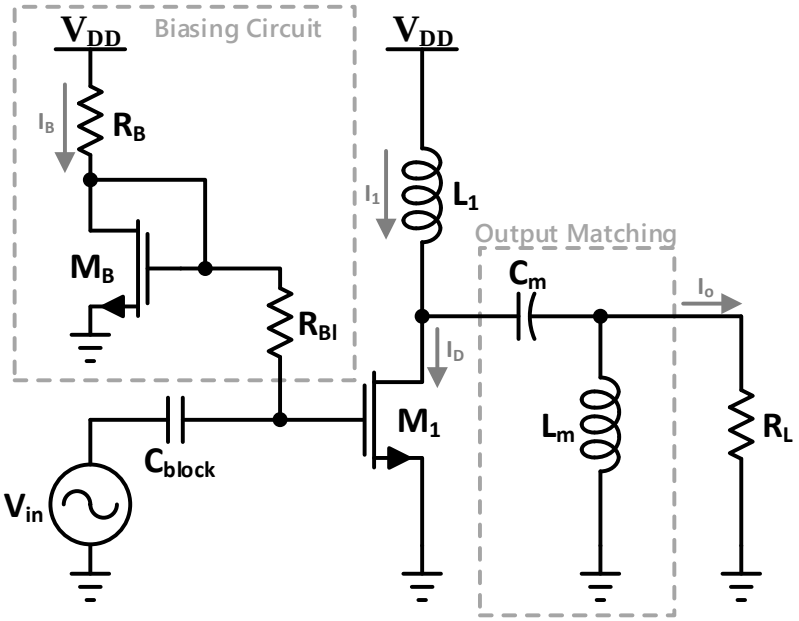


Figure 4.1: Basic Class-A PA with circuit biasing and output matching

Table 4.1: Class-A PA specifications

Specifications	Value
V_{DD}	*1.2 V*
f_o	*2.4 GHz*
G_P	$\geq$ *10 dB*
Z_{out}	*50* Ω
P_{out}	*[0* $\sim$ *20] dBm*

As a starting point, it was decided to establish the biasing factor of the circuit. To minimize the current consumption, the biasing transistor M_B is sized to be smaller than the PA transistor, hence the biasing factor is taken as 10:1, which implies the same current ratio, as presented in Equation (4.1).

$$I_B = \frac{I_D}{10}. \tag{4.1}$$

The parameters must be calculated based on the fundamental notions about CMOS transistors. Hence, bearing in mind that the transistor M_1 must operate in saturation mode, which leads to Equation (4.2), the width of the transistor M_1 can be determined by sizing the saturation voltage, V_{Dsat}, of the same transistor and

by sizing drain current, I_D, that were set at 200 mV and 10 mA, respectively.

$$W_{M1} = \frac{2I_D L_{M1}}{K_N V_{Dsat1}^2}. \tag{4.2}$$

Therefore, this scaling has led to the transistors design presented at Table 4.2 (assuming same length for both transistors: $L = L_{min} = 120nm$).

Table 4.2: Transistor's design

Transistor	Width $[\mu m]$	$I_D[mA]$	$V_{Dsat}[mV]$
M_1	*120*	*10*	*200*
M_{bias}	*12*	*1*	*200*

Initially, it was used an ideal inductive load. The purpose of this inductor is to behave like an AC open circuit at work frequency, so it can carry a constant current. Henceforth, its L parameter must be sufficiently large but well designed in order to cancel the circuit's resonance. Bearing that in mind, the imaginary part of itself plus the parasitic capacitances of transistor M_1 should be nullified, which is possible to achieve with Equation (4.3). The blocking capacitor is also wanted to be large enough to prevent DC passage and allow to pass only AC.

$$\omega_o = \frac{1}{\sqrt{L \cdot C}}. \tag{4.3}$$

Finally, the output matching must be designed in order to adapt the PA signal to the antenna's impedance, R_L, which also allows efficiency improvement, since it yields to lower reflection losses. For that purpose, the LC mesh was considered (Inductor in parallel and capacitor in series), as showed in Figure 4.1. Before that, the output impedance of the PA must be found in order to calculate the appropriate values for the LC mesh.

The circuit from Figure 4.1 (ignoring the output matching circuit) can be easily redesigned to its small signals form, by nullifying DC voltages, short-circuiting the blocking capacitors and introducing parasitic capacitors, which work at high frequencies Figure 4.2. Analysing the impedance seen from the output, shunting the input source, which implies $V_{gs1} = 0$, through Kirchhoff's Current Law the output current i_{out} is given by Equation (4.4),

$$i_{out} = v_{out}\left(\frac{1}{j\omega L_1} + j\omega Cds_1 + \frac{1}{rds_1} + j\omega Cgd_1\right). \tag{4.4}$$

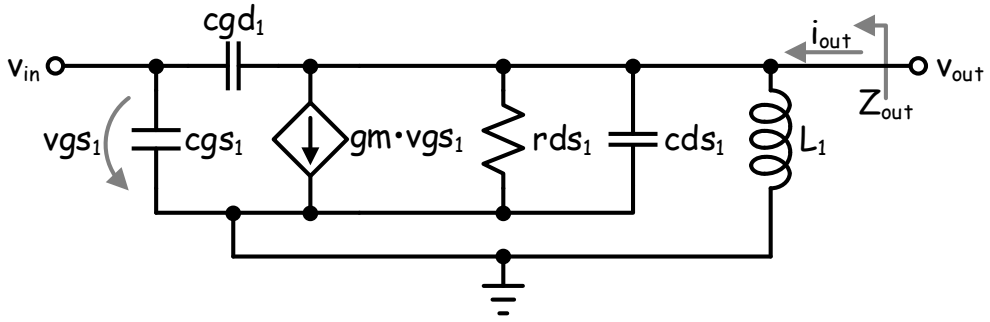


Figure 4.2: Small signal circuit of the classic PA.

From Ohm's Law, rewriting the previous equation as $Z_{out} = v_{out}/i_{out}$, the output impedance expression leads to (4.5).

$$Z_{out} = \frac{1}{\left(\frac{1}{j\omega L_1} + j\omega Cds_1 + \frac{1}{rds_1} + j\omega Cgd_1\right)}. \tag{4.5}$$

Regarding to the LC mesh illustrated in Fig. 4.3, its input impedance Z_m is given by (4.6).

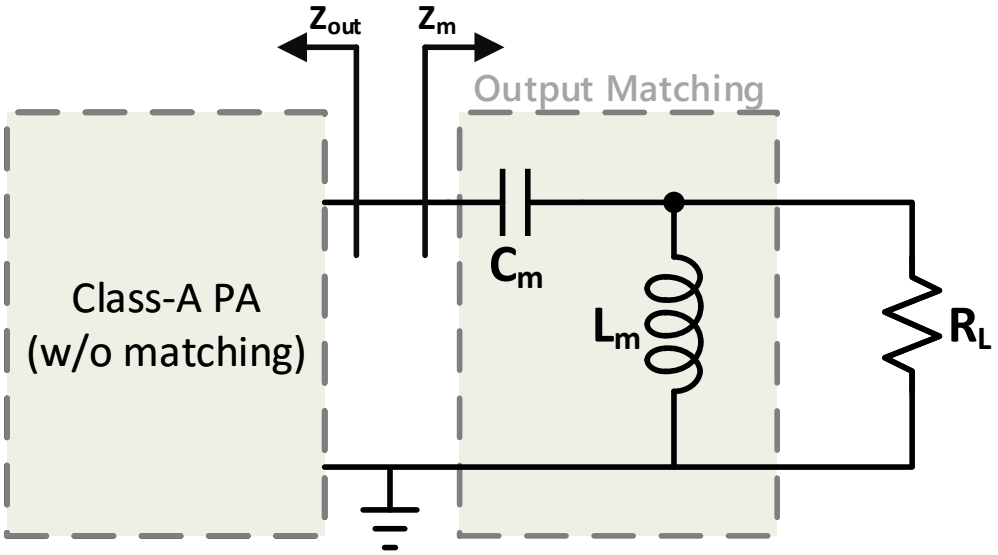


Figure 4.3: LC matching network

$$Z_m = C_m + \left(\frac{L_m \cdot R_L}{L_m + R_L}\right). \tag{4.6}$$

To summarize, the real part of Z_m and Z_{out} expressions must be equal, and the imaginary part of Z_{out} should be equal to the $-Z_m$ or vice versa. As a result, the

system solution in Equation (4.8) allows to obtain the L_m and C_m values, which are presented in Table 4.3.

$$\Re\{Z_{out}\} + \Im\{Z_{out}\} = Z_m \Leftrightarrow \tag{4.7}$$

$$\Leftrightarrow \begin{cases} C_m = \dfrac{L_m^2\omega_o^2 + R_L^2}{Im\{Z_{out}\}L_m^2\omega_o^3 + Im\{Z_{out}\}R_L^2\omega_o + L_m R_L^2\omega_o^2}, \\ L_m = \dfrac{R_L\sqrt{Re\{Z_{out}\}}}{\sqrt{R_L\omega_o^2 - \omega_o^2 Re\{Z_{out}\}}}. \end{cases} \tag{4.8}$$

Table 4.3: Design of the parameters L and C

Parameter	Value
L_1	*7.58 nH*
L_m	*5.395 pF*
C_m	*2.24 pF*

4.2 Simulations Results

The simulations analysis of PA design were performed using the SpectreRF engine from Cadence Design Systems. For validation purposes of Class-A PA designed, operating at 2.4 GHz, four types of analysis were verified at output stage. The S-parameter simulation was performed to generate plots of the return losses (S_{22}), small signal gain (S_{21}) and noise figure (NF). For large signal analysis to measure output power levels, 1 dB compression point and power added efficiency (PAE), the periodic steady state (PSS) simulation were performed. The third order intercept point (IP3) plot was given by the Periodic AC (PAC) simulation. Lastly, the transient simulation was performed to plot the output voltage and current, used to measure the DC power consumption and conduction angle.

In the Section 4.1.1, the PA was designed considering ideal components. However, it is important foresee its real behaviour, therefore it is also presented a simulation result based on real models. The schematics taken from Cadence tool for the Class-A simulation with ideal LC components, as well as for the Class-A simulation with real models LC components are presented in Appendix A.1, where variables of the ports, presented in Appendix A.3, were set as follows: $rin = 5\ K\Omega$, $fin = 2.4\ GHz$ and $pin = -5\ dBm$.

4.2.1 Class-A Simulation

The S-parameter simulation results are shown in Figure 4.4 and Figure 4.5. The measured small signal gain (S_{21}) and output return losses (S_{22}), are 9.56 dB and - 35.25 dB, respectively. The Re[Z_{22}] and Im[Z_{22}] shows that the PA is well adapted to the antenna at f_o, as well as the (S_{22}), since it is below than -10 dB and low enough to not interfere with the signal conduction.

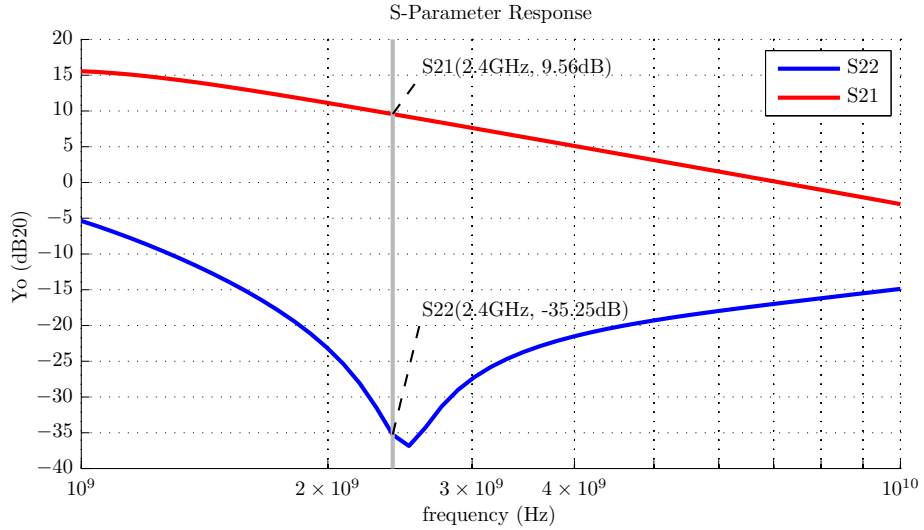


Figure 4.4: Small signal gain, (S_{22}), and output return losses, (S_{21}).

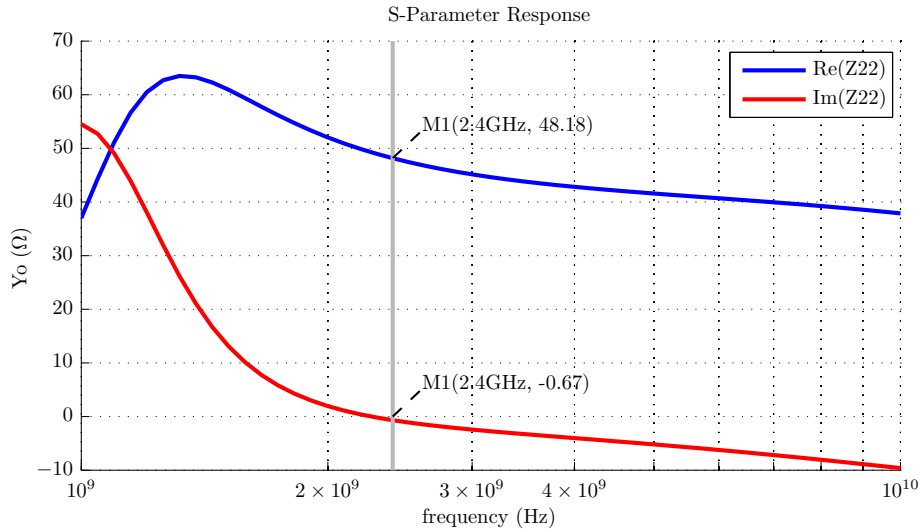


Figure 4.5: Class-A PA adapted to 50 Ω.

Figure 4.6 illustrates that the 1 dB compression point (P1dB) is reached when the input power is 0.162 dBm, being respectively the maximum output power of 8.72 dBm. At this point the amplifier starts to saturate and can potentially produce signal distortion and intermodulation products.

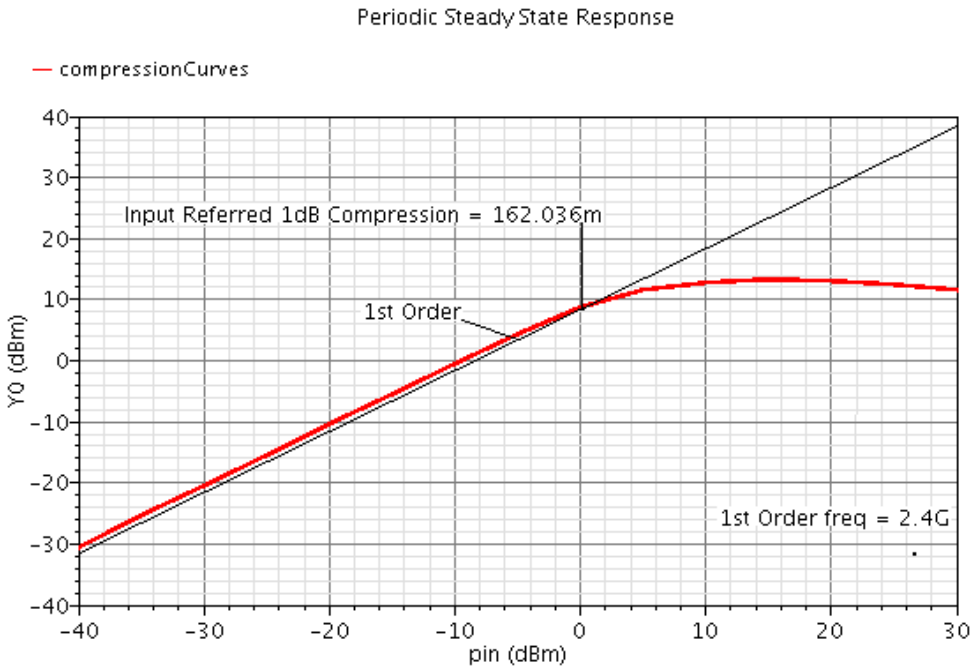


Figure 4.6: 1 dB compression point measured at 2.4 GHz.

The plot result of the power added efficiency (PAE) simulation is shown in Figure 4.7. Considering two input power references, at P1dB and IP3, the following results were achieved, 34% and 60% respectively. When compared to the theoretical value, it is possible to verify that the PAE specification is met.

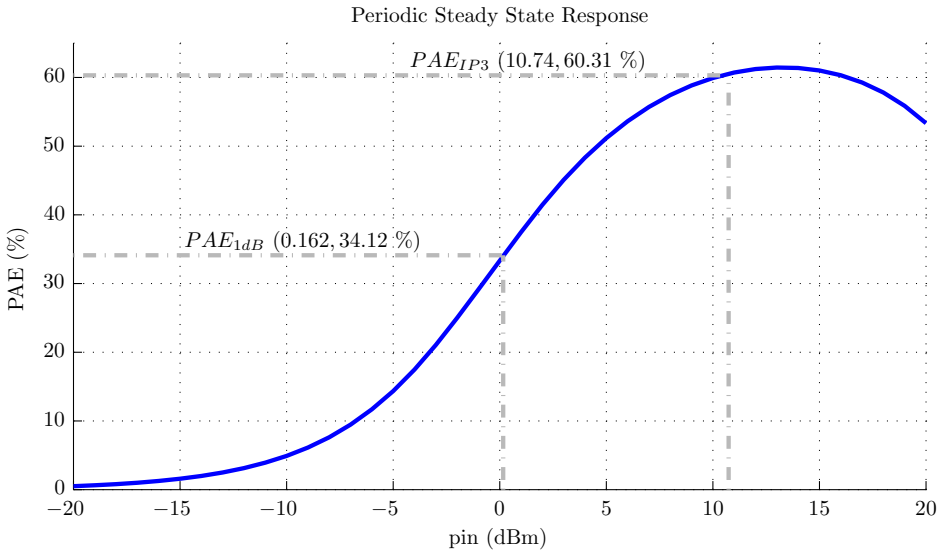


Figure 4.7: PAE vs. input power at 2.4 GHz.

Following into PAC analysis, measuring the third order intercept point (IP3), in a way to prevent intermodulation distortion from third order mixed harmonics,

there were used two close tones 2,398 GHz and 2,402 GHz. The outcome, as shown in Figure 4.8, is an input power of 10.74 dBm, which is a satisfactory result, since this value is 100 times higher (20 dB) than P1dB.

Finally, to prove that Class-A is operating in its entire conduction angle, the transient results of the drain current and drain-to-source voltage are presented in Figure 4.9, where it is possible to conclude that the drain current conduction occurs, indeed, all the time. Therefore the Class-A PA with ideal components meets the requirement of 360º conduction angle.

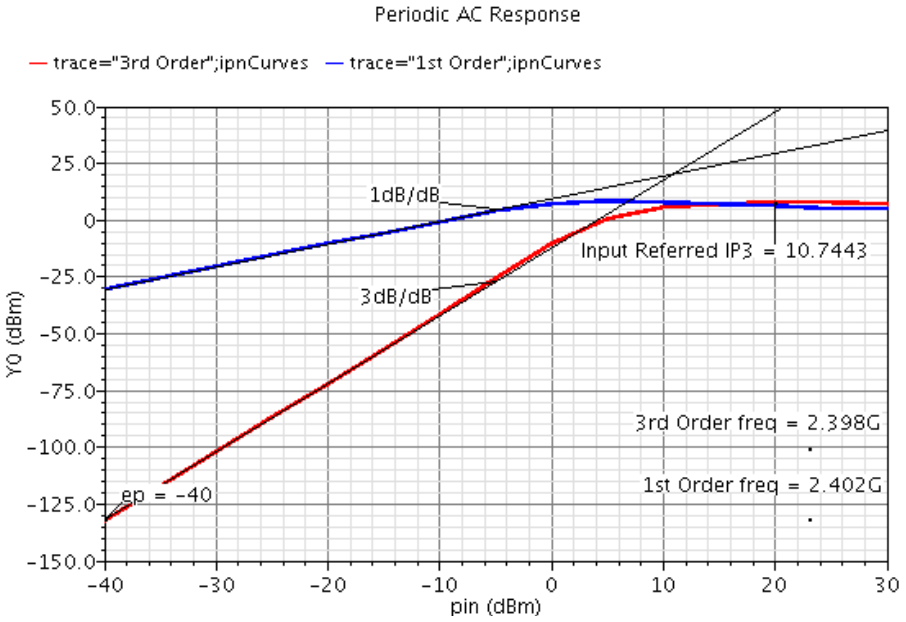


Figure 4.8: IP3 vs. input power at 2.4 GHz.

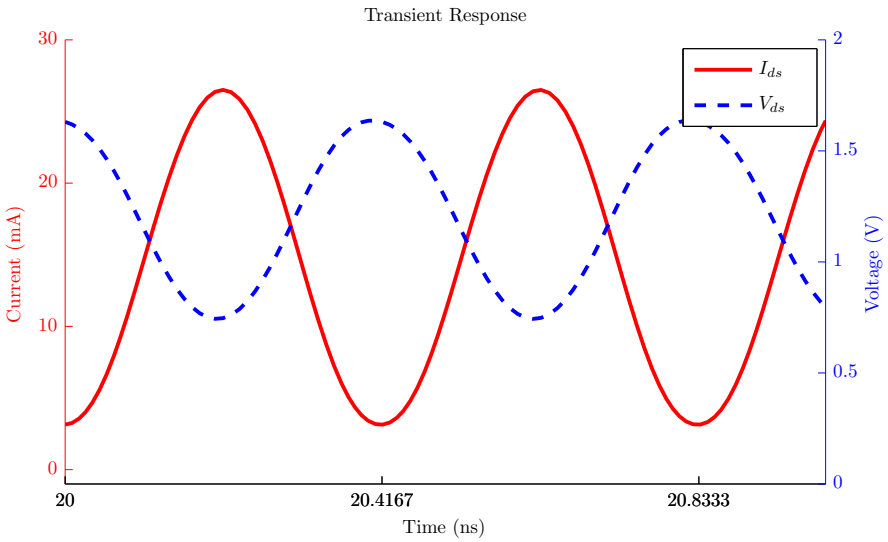


Figure 4.9: Transient results of the drain current and drain-to-source voltage.

4.2.2 Class-A Simulation with Real Models of the Reactive Components

The major change at real Class-A design was at the level of reactive components. The Planar Inductor RF model was used for L_1 and L_{match} inductors, and the Planar MIM Capacitor model for C_{match} capacitor. The aforementioned simulations were performed. Theoretically, this change will produce an output power reduction, due to the power dissipated by the reactive components. Consequently a gain reduction is expected, as well as a efficiency decrease, which is explained by intermodulation distortion increase.

According to the S-parameters, a slight reduction of small signal gain, as also, a similar return losses were measured, as shown in Figure 4.10 and in Figure 4.11, respectively.

In Figure 4.12 it is illustrated a significant decrease of the PAE in relation to the ideal result. This can be explained by decrease of the output power, as Equation (2.4) can prove.

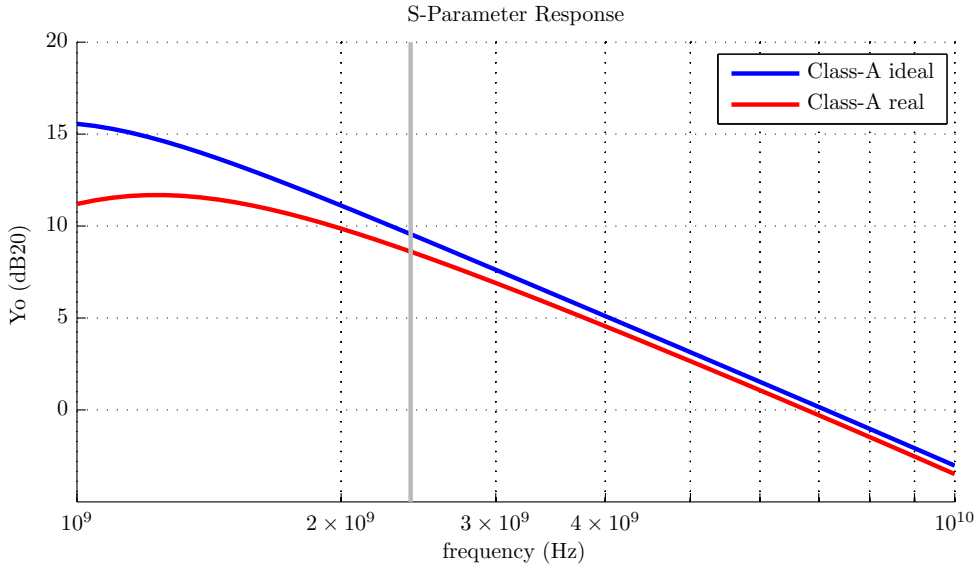


Figure 4.10: Gain (S21) versus frequency

A comparison of the obtained results between the design with ideal LC components and real models of the same components is presented in Table 4.4.

Simulation results showed that at 2.4 GHz, the amplifier voltage gain operating with ideal LC models or with real LC models, is about 9 dB. Concerning to the PAE, the maximum value (at IP3) of 60% is achieved with ideal models, which is quite good when comparing to the theoretical value. However, real models

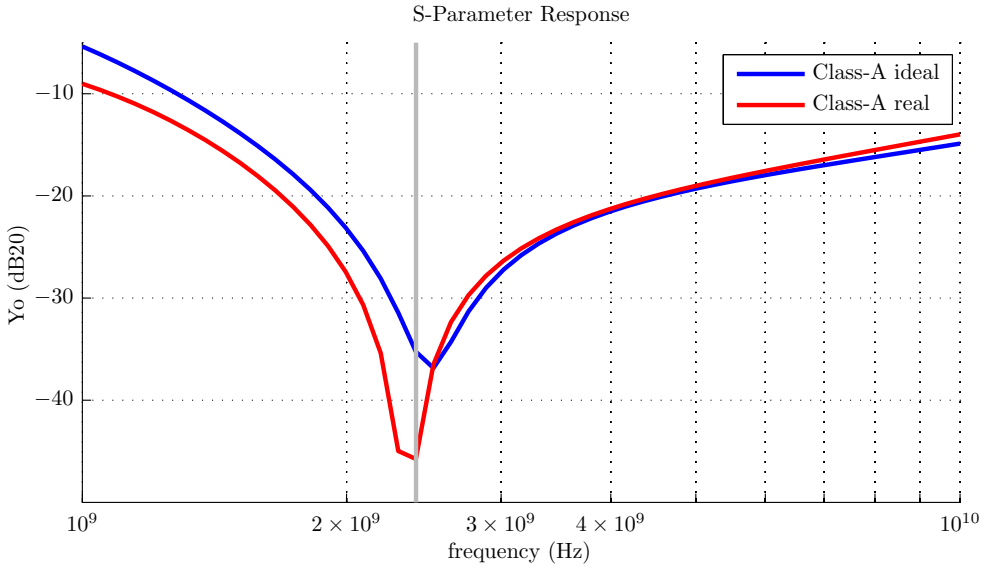


Figure 4.11: Output return losses (S22) versus frequency

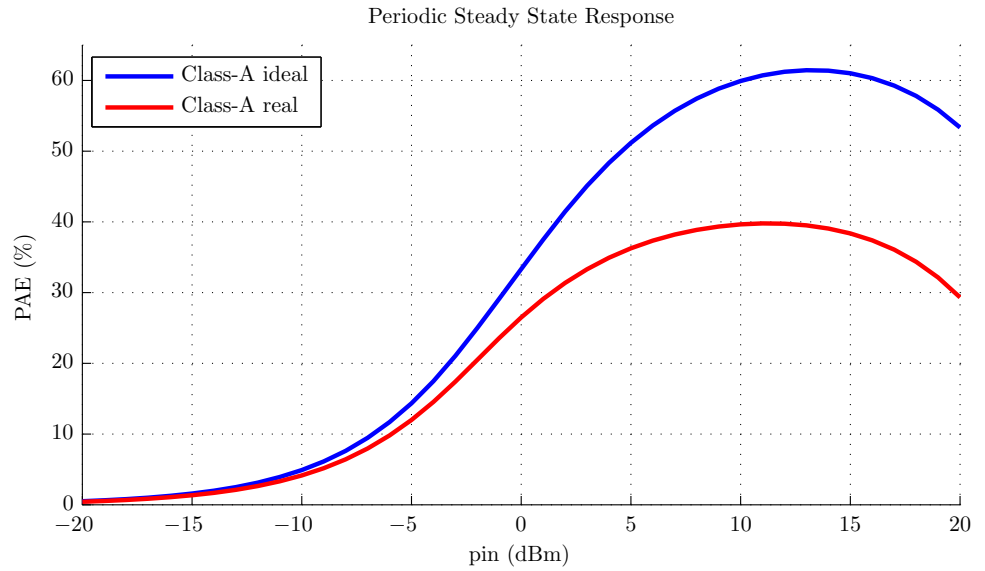


Figure 4.12: Comparison of the PAE with ideal and real components versus frequency.

have decreased the maximum value of PAE to 41%. Indeed, this result was also expected, due to the real models introduce power dissipation.

The proposed PA circuit fulfils the output power requirement of 8.7 dB and 6.5, respectively to ideal and real models, for Bluetooth applications.

Table 4.4: PA classes simulation results and comparison

Specification	Class-A with ideal LC	Class-A real real LC
Input 1dB Compression Point $[dBm]$	*0.16*	*-1.31*
Output 1dB Compression Point $[dBm]$	*8.72*	*6.45*
Power added efficiency (PAE) [%]	*34-60*	*24-41*
Max. linear output power $[dBm]$	*8.72*	*6.45*
Small signal gain (S_{21}) $[dB]$	*9.56*	*8.77*
Output return losses (S_{22}) $[dB]$	*-30.87*	*-31.22*
Real Z_{22} *[*Ω*]*	*49.26*	*49.65*
Imaginary Z_{22} *[*Ω*]*	*-0.73*	*-0.94*
Input harmonic IP3 $[dBm]$	*10.74*	*9.67*
Output harmonic IP3 $[dBm]$	*20.29*	*18.43*
Conduction angle $[^o]$	*360*	*360*
Noise Figure $[dB]$	*3.40*	*3.44*
L_{match} $[nH]$	*5.72*	*5.15*
C_{match} $[pF]$	*2.36*	*2.03*
L_1 $[pF]$	*7.56*	*7.56*

CHAPTER 5

CLASS-E POWER AMPLIFIER

Switchmode Class-E power amplifiers are largely defined by a single transistor with shunt capacitance and series-tuned LC circuit. This type of amplifiers offers a simple design and high-efficiency operation and, for that reason, they have been used for a wide-spread applications. Switchmode definition comes by the fact the single transistor operating as a switch, providing voltage and current waveforms where the high peak of each do not occur simultaneously. This way, in ideal case, when there is a zero slope the transistor turns on and the voltage drops to zero, henceforth, its power dissipation is zero too. Even if there is some overlap between the two waves, in other words, the circuit has some power dissipation, because the transistor can not operate as an ideal switch, it still brings a lot of benefits, principally the high efficiency [5, 17].

In the following sections, the basic operation and analysis of the Class-E power amplifier are presented. Moreover, different solutions of the Class-E power amplifier for the output stage are implemented and analysed, where the solution with better results at 2.4 GHz frequency and with supply voltage of 1.2 V is chosen and implemented together with Class-A driver stage. Finally, complete design of the RF power amplifier is implemented in a 130 nm CMOS technology at 2.4 GHz frequency, in order to be suited for Bluetooth application.

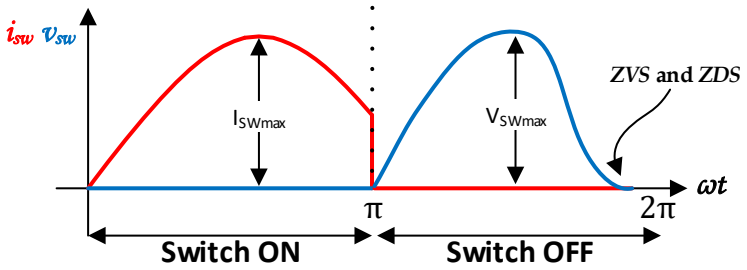
5.1 Class-E Theory

The first proposal of the Class-E power amplifier was made by Sokal in 1975 [18], though the first concept of the Class-E was introduced in a doctoral thesis by

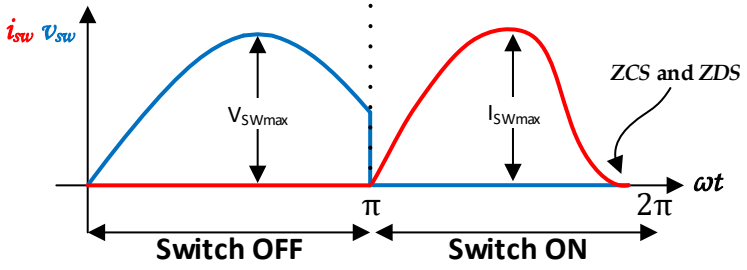
Ewing in 1964 [19]. Since then this topic has been widely studied and implemented in miscellaneous ways.

There are a lot of topologies already implemented, for instance, single-ended (common-source or common-gate [20, 21]), differential [22] and cascode mode [23], a brief overview of these topologies is also presented in Appendix C. For the purpose of this thesis, the single-ended common-source topology was considered and only this one is henceforth to be discussed.

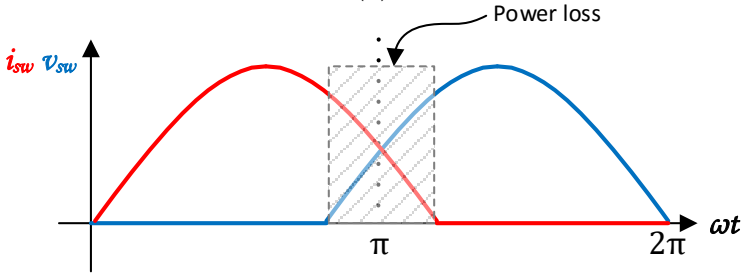
Within this topology there are two possible implementations: zero-voltage switching (ZVS) and zero-current switching (ZCS), both of them using zero-derivative switching (ZDS) technique, which define whether switch turns on with zero voltage or turns off with zero current, respectively, so that at the switching time there must be no overlapping waveforms between I_{DS} and V_{DS}.



(a) ZVS



(b) ZCS



(c) Overlapping time

Figure 5.1: Current and voltage waveforms through the switch.

The ZVS method forces V_{DS} to be zero just before the transistor turn on with its derivative also equal to zero at the same time, ZDS, yielding to system of

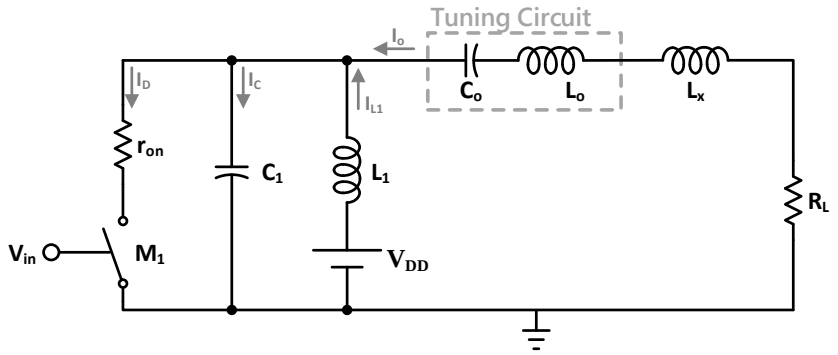
equations (5.1).

$$ZVS\ and\ ZDS = \begin{cases} v_{DS}(\omega t)\Big|_{t=t_1} = 0, \\ \dfrac{\partial v_{DS}(\omega t)}{\partial \omega t}\Big|_{t=t_1} = 0. \end{cases} \tag{5.1}$$

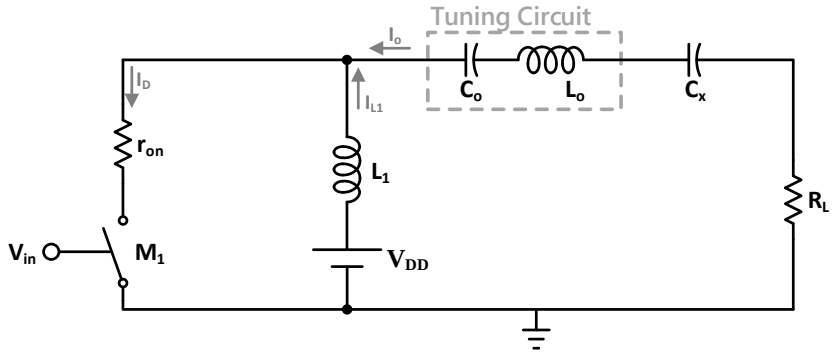
The ZCS, in its turn, forces I_{DS} to be zero just before the transistor turn off, again with respective derivative equal to zero, yielding to system of equations (5.2).

$$ZCS\ and\ ZDS = \begin{cases} i_{DS}(\omega t)\Big|_{t=t_1} = 0, \\ \dfrac{\partial i_{DS}(\omega t)}{\partial \omega t}\Big|_{t=t_1} = 0, \end{cases} \tag{5.2}$$

where, for both cases, t_1 corresponds to the transition time from off to on state or from on to off [5]. The current I_{DS} and voltage V_{DS} waveforms trough the switch transistor are shown on Figure 5.1.



(a)



(b)

Figure 5.2: Class-E equivalent circuits. (a) ZVS circuit. (b) ZCS circuit.

The two cases were carefully studied by Kazimierczuk [5] and equivalent circuits for both cases were presented, just like shown in Figure 5.2. However, only ZVS method will be from now discussed and implemented. The reason is simple,

since the ZCS does not include shunt capacitance in its basic topology and the switch turns on at non zero voltage, the energy stored by switch output capacitance is dissipated and, therefore, the efficiency is reduced. Under those circumstances, the Class-E ZVS amplifier has greater efficiency than that of the Class-E ZCS amplifier for the same operating frequency and using the same transistor, and that is why this one is largely preferred.

The general circuit for a single-ended Class-E ZVS power amplifier is illustrated in Figure 5.3.

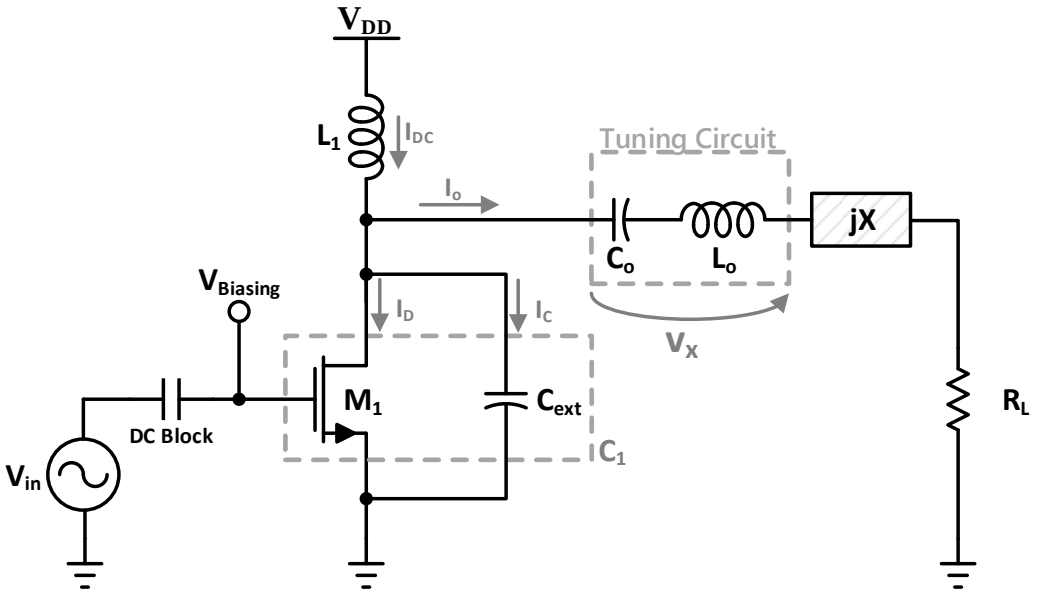


Figure 5.3: Circuit of single-ended Class-E power amplifier with general load network.

5.1.1 Assumptions

In order to present analytical expressions based on the analysis of the Class-E ZVS, based on the equivalent circuit represented in Figure 5.2a, some assumptions were made, as follows [5]:

- The transistor works as an ideal switch with zero on-resistance (r_{on}), infinite off-resistance, zero saturation voltage and zero switching time, which implies to lose no power.
- The load R_L is the only one of the circuit to have real power loss.

- The duty cycle of 50% for optimum operation is considered because of its simplicity.
- Total shunt capacitance, C_1, is assumed to be linear and includes all parasitics capacitances of the transistor.
- Current through the L_oC_o resonant circuit is sinusoidal, implying a high enough quality factor, Q_L.

5.1.2 Circuit Description

Analysing Figure 5.3, the capacitances and inductances, namely L_1, C_1, C_o and L_o, are what allow to define an Class-E ZVS. The inductance L_1 can be set as either an RFC or a finite DC-feed inductance. Though, it is more advantageous to set L_1 as a finite DC-feed inductance, minimizing its value will bring several benefits, which will be discussed shortly.

As the transistor is assumed to be an ideal switch, its output capacitance plus external shunt capacitance are included in C_1, which brings a big benefit to efficiency enhancement.

While the L_1C_1 form parallel-resonant circuit, the capacitance C_o and inductance L_o are set to be series-resonant circuit tuned to the fundamental frequency, $\omega_o = 2\pi f_o$, in order to allow to pass only a sinusoidal current on the frequency of interest. The series excessive reactance can be either inductive (positive) or capacitive (negative), depending on the values of L_1 and C_1, and has the purpose of putting suitable phase shifting between output voltage, V_o, and switching voltage, V_{DS}, so that the desired waveforms can be achieved [24].

The switching condition of the transistor imply different operation during two states (on state and off state), as was said earlier. Hence, these states define different equations of the circuit currents and voltages. And so, to understand its waveforms, these equations must be specified in time domain. As the circuit current and voltage have periodicity and a duty cycle of 50 % is considered, half of the period transistor is on and other half is off. Assuming the on period in the range $0 \leq \omega t < \pi$ and off in $\pi \leq \omega t < \pi$, the expressions of the circuit currents and voltages are as follows

$$i_D(\omega t) = \begin{cases} i_{L1}(\omega t) + i_o(\omega t), & 0 \leq \omega t < \pi, \\ 0, & \pi \leq \omega t < \pi, \end{cases} \tag{5.3}$$

$$i_o(\omega t) = I_o \cdot \sin(\omega t + \phi), \tag{5.4}$$

$$v_D(\omega t) = \begin{cases} 0, & 0 \leq \omega t < \pi, \\ V_{DD} - v_{L1}(\omega t), & \pi \leq \omega t < \pi, \end{cases} \tag{5.5}$$

$$v_{L1}(\omega t) = \omega L_1 \cdot \frac{\partial i_{L1}(\omega t)}{\partial \omega t}, \tag{5.6}$$

$$i_{C1}(\omega t) = \begin{cases} 0, & 0 \leq \omega t < \pi, \\ i_{L1}(\omega t) - i_o(\omega t), & \pi \leq \omega t < \pi, \end{cases} \tag{5.7}$$

$$i_{C1}(\omega t) = \omega C_1 \cdot \frac{\partial v_D(\omega t)}{\partial \omega t}. \tag{5.8}$$

The proper manipulation and derivation of these equations leads to the simplified and generalized equations that allow to design the circuit parameters for some specific mode operation. The first derivation of these equations, assuming an L_1 with infinite value and lossless components, was performed by Raab in [25]. Then followed the attempts to get the generalized equations or to include some non-linearities or some circuit limitations. The design equations under the assumption of non sinusoidal output current and with different values of duty cycle were derived by Kazimierczuk in [26]. The consideration of the non-linear parasitic output capacitance of the transistor and the finite on-resistance are made in [27, 28, 29] and in [30], respectively. Equations with the regard to the maximum frequency of operation and some circuit limitations are presented in [31, 32, 33]. Most of these works assumed an RFC (L_1 with infinite value), but in [32, 34, 35] new explicit design equations under assumption of the finite DC-feed inductance were developed and tested. So, as can be seen, a large investigation was made to find better design equations for the Class-E power amplifier. As a result, the demonstration of the simplified design equation is not shown here, but it can be followed in [5, 17].

Thus, the full-load resistance (also called as an optimum resistance), the L_1 inductance and C_1 capacitance can be calculated from the following equations:

$$R_{opt} = K_P \cdot \frac{V_{DD}^2}{P_{out}}, \tag{5.9}$$

$$L_1 = K_L \cdot \frac{R_{opt}}{\omega_o}, \tag{5.10}$$

$$C_1 = K_C \cdot \frac{1}{\omega_o R_{opt}}, \tag{5.11}$$

where K_P, K_L and K_C are parameters that depend on the Class-E operation mode, such as:

1. **RFC:** L_1 is assumed to be an RFC, which allows only a constant dc current to pass through it.

2. **Parallel-circuit:** uses a finite DC-feed inductance, and is designed to have maximum output power.

3. **Even-harmonic resonant:** also a finite DC-feed inductance is used, but L_1C_1 resonant circuit is tuned at even harmonics of the fundamental frequency f_o.

4. **Subharmonic resonant:** with finite DC-feed inductance and L_1C_1 resonant circuit is tuned at half of the fundamental frequency f_o.

The use of a finite DC-feed inductance have been of the great study, as it allows a great variety of solutions. Smaller DC-feed inductance brings a lot of benefits, as it implies smaller electrical series resistance of it, and hence, lower power loss. Not to mention that smaller DC-feed inductance allows to decrease the circuit area and cost.

Apart from these modes of operation, it is possible create more solutions for the case where finite DC-feed inductance is used. That is possible through the setting of q parameter, which is a multiplicative number by the operating frequency, ω_o, which defines a parallel resonant L_1C_1 circuit tuned to the frequency ω_p,

$$\omega_p = q \cdot \omega_o = \frac{1}{\sqrt{L_1C_1}}. \tag{5.12}$$

The analysis of the best q values for Class-E design with finite DC-feed inductance were thoroughly studied by Grebenikov in [17] and by Acar in [36, 37]. They presented fitted design through polynomial equations in function of q, which approximates to the exact analytical relations with only 2% of error. However, the range of this variable is considered of: $0.6 < q < 1.9$, because, as presented in [36, 37], in other range of values extreme waveforms behaviour occurs, which turns those solutions impractical. These equations are represented in Table 5.1. Through that equations and respective plots, presented in Figure 5.4, it was discovered that $q = 1.412$ maximizes output power for given R_{opt} and V_{DD}, which is desired for the parallel-circuit solutions. The even-harmonic resonant condition means that it could be used to tune on any even harmonic component with $q = 2n$, where $n = 1, 2, 3..\infty$, even so, the most practical and simple case with $n = 1$ is considered, i.e., tuning to the second harmonic component. Bringing all these conditions together, as well as for the subharmonic resonant Class-E where $q = 0.5$ is defined, the design of the parameters of the load network is introduced in Table 5.2.

Table 5.1: Load-network for variable q.

$0.6 < q < 1$	
K_P	$0.74q^2 - 0.6q + 0.76$
K_L	$44.93q^2 - 94.32q + 52.46$
K_C	$0.426q^2 - 0.379q + 0.3$
K_X	$-0.73q^2 + 0.411q + 1.03$
$1 < q < 1.65$	
K_P	$-11.90q^3 + 42.753q^2 - 49.63q + 19.70$
K_L	$8.085q^2 - 24.53q + 19.23$
K_C	$-6.97q^3 + 25.93q^2 - 31.071q + 12.48$
K_X	$-2.9q^3 + 8.8q^2 - 10.2q + 5.02$
$1.65 < q < 1.9$	
K_P	$6.25q^2 - 24.73q + 24.56$
K_L	$16.17q^2 - 52.26q + 42.94$
K_C	$2.55q^2 - 10.53q + 10.92$
K_X	$-16.84q^2 + 51.38q - 39.83$

Table 5.2: Design of the Load Network Parameters.

K	RFC	Parallel-Circuit	Even-Harmonic Resonant	Subharmonic Resonant
K_P	0.5768	1.365	0.056	0.635
K_L	$\to \infty$	0.732	3.534	18.9
K_C	0.1836	0.685	0.071	0.212
K_X	1.152	0	0.204	1.058

5.2 Implementation

The Section 5.1 presented a detailed analysis of the Class-E power amplifier, which allowed to find simplified expressions and those are now used to implement a Class-E ZVS RF PA in 130 nm CMOS technology. This implementation aims to be designed for a Bluetooth application in the technology already referred.

The presented power amplifier requires at least two distinct stages, as illustrated in Figure 5.5. One is output stage, which is of bigger importance, since it is the one that define the greater part of efficiency of the PA and for that reason must be designed in the first place. In the Section 5.2.1 its design is presented with the aim to choose the better solution for Bluetooth application within the four

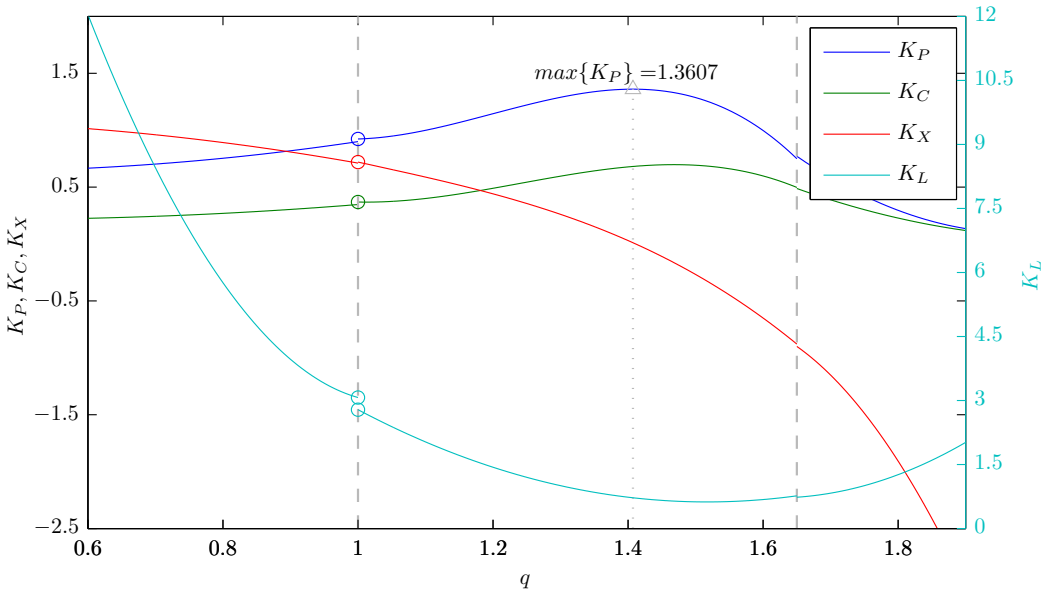


Figure 5.4: The K_P, K_L, K_C and K_X parameters in function of q for Class-E design with finite-DC feed inductance.

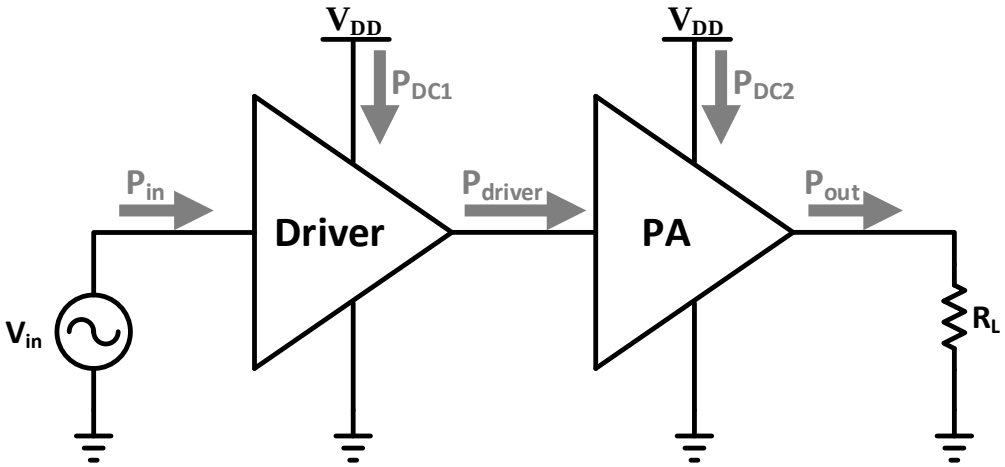


Figure 5.5: General RF switching power amplifiers blocks.

modes of operation presented in the previous section (RFC, parallel-circuit, even-harmonic and subharmonic resonant). And so, these designs do not present any novelty to the actuality, as they were already developed by the Sokal, Kazimierczuk, Acar, Grebenikov and others [5, 17, 36, 38], but only a theoretical validation here will be presented.

Other stage is a pre-amplifier, also called as driver stage, which has a significant contribution in avoiding drain voltage and current overlap, which, of course, will

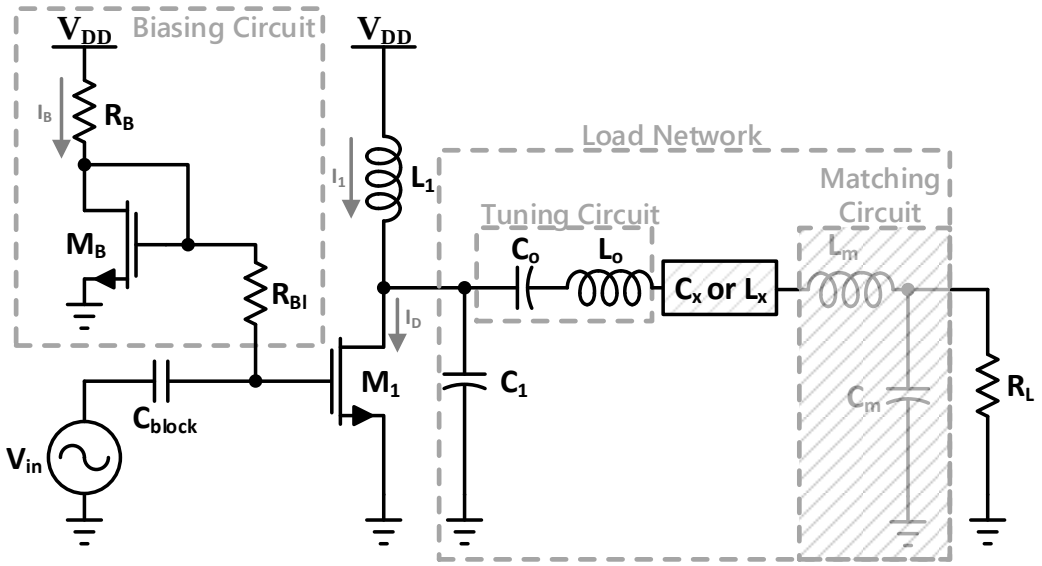


Figure 5.6: Class-E RF power amplifier.

lead to better efficiency at the end. This stage generates the input waveform that must turn the power transistor on and off, and has a big role in avoiding long transition times from one switching state to the other, which would reduce the referred overlap.

5.2.1 Design of the Output Stage Class-E Amplifier

The circuit topology of a ZVS Class-E RF power amplifier with a biasing circuit (current mirror) is used to design a output stage and is shown in Figure 5.6.

The proper design of the load network, represented in Figure 5.6, will allow this circuit to work in a switching mode and providing high-efficiency. For that purpose the design must be set in order to comply the next specifications.

Table 5.3: Class-E PA specifications.

Specifications	Value
V_{DD}	*1.2 V*
f_o	*2.4 GHz*
P_o	$[0-20]$ *dBm*
R_L[1]	*50* Ω

[1]It is to mention that the resistor R_L does not form part of components design, it is there to represent the impedance needed to match circuit to the antenna.

Despite the output power range presented on Table 5.3, which is desired for Bluetooth application, the target output power is chosen to be on the range of $[20 - 100]\ mW$, or in dBm $[13 - 20]$, to provide margin for some losses due to transistor and real reactive components parasitics. More specifically, two values for the output power were chosen, the maximum and minimum values of the range considered ($P_o = 13\ dBm$ and $P_o = 20\ dBm$). Given that, now it is possible to calculate the values of the R_{opt}, L_1 and C_1, and recalling those equations:

Table 5.4: Equations of the R_{opt}, L_1 and C_1.

R_{opt}	L_1	C_1
$K_P \cdot \frac{V_{DD}^2}{P_{out}}$	$K_L \cdot \frac{R_{opt}}{\omega_o}$	$K_C \cdot \frac{1}{\omega_o R_{opt}}$

where K_P, K_L and K_C take different values for each operation mode, as shown in Table 5.2. It is important to remember that the shunt capacitance C_1 is defined by output capacitance of the transistor, which includes all parasitic capacitances and the exterior capacitance added to allow adjustment resonance with L_1. Therefore, the exterior capacitance, C_{ext}, can be calculated by

$$C_{ext} = C_1 - C_p, \tag{5.13}$$

where C_p is the output capacitance of the transistor. A large channel width of the transistor is wanted in order to diminish the on-resistance, r_{on}, as it in practice can not be neglected. Since the current conduction initially occurs in the triode region, the on-resistance has the following relationship with size of the transistor given by

$$r_{on} = \frac{V_{DS}}{I_D} = \frac{1}{K_N \cdot \frac{W}{L} \cdot (V_{GS} - V_{Th} - V_{DS})}. \tag{5.14}$$

From Equation (5.14) it is possible to conclude that the r_{on} is inversely proportional to the channel width of the transistor and directly proportional to the channel length. And thus, besides the large channel width, the minimal length is needed, which within the technology used for this project is of 120 nm. However, a large width imply bigger parasitic capacitance of the transistor, which may turn to be difficult to control it. As a result the channel width need to be set in the middle point in order to achieve better trade-off between parasitic capacitance and on-resistance.

Thereby, the saturation voltage of the V_{DS}, V_{DSsat}, and I_D were set to 200 mV and 18 mA, respectively, and considering the threshold voltage: $V_{Th} = 340\ mV$,

the channel width of the transistor, through the square law, results into:

$$W_{M1} = \frac{2 \cdot I_D \cdot L_1}{K_N \cdot V_{DSsat}^2} = 216\ \mu m. \tag{5.15}$$

It is to notice that the Equation (5.15) corresponds to the saturation region of the transistor, that is because in this design it was opted to set the transistor in saturation region, but usually it is designed in triode region.

The biasing factor must be set in such a way that the size of the M_B transistor is minimized and the size of the M_1 transistor is enough to pass the desirable current. Thus, as the size of the M_1 transistor was already calculated, the biasing factor was set to 15:1, that seemed to be the ideal for that purpose, such that $I_B = I_D/15 = 1.2\ mA$. Ideally, a current source would be enough to include in a current-mirror, but, as it is pretended to be as close as possible to reality, the ideal current source must be exchanged for a resistance, and its value can be calculated as follows:

$$R_B = \frac{V_{DD} - V_{GS}}{I_B}. \tag{5.16}$$

Let V_{GS} be of 500 mV, then $R_B \simeq 583\ \Omega$. With the same current factor relation it is calculated the channel width of the biasing transistor, giving $W_B = W_1/15 = 14.4\ \mu m$.

Concerning to the resonant circuit design, it is important to not forget to take into account the excessive inductance or capacitance, depending on the operation mode. The parallel-circuit operation mode do not need any excessive reactance, and so, the resonant components L_oC_o can be calculated simply as follows:

$$L_o = \frac{Q_L \cdot R_{opt}}{\omega_o}, \tag{5.17}$$

$$C_o = \frac{1}{Q_L \cdot \omega_o \cdot R_{opt}}. \tag{5.18}$$

The RFC and subharmonic resonant operation mode use an excessive inductance, L_x, which can be added to the L_o, resulting in

$$L_{total} = L_o + L_x = \frac{Q_L \cdot R_{opt}}{\omega_o}, \tag{5.19}$$

where L_x is

$$L_x = K_x \cdot \frac{R_{opt}}{\omega_o}, \tag{5.20}$$

yielding

$$L_o = \frac{Q_L \cdot R_{opt}}{\omega_o} - L_x = \frac{(Q_L - K_x) \cdot R_{opt}}{\omega_o}. \tag{5.21}$$

Since C_o must resonate with L_o at the operating frequency, ω_o, this leads to

$$C_o = \frac{1}{\omega_o^2 \cdot L_o} = \frac{1}{\omega_o \cdot R_{opt} \cdot (Q_L - K_x)}. \tag{5.22}$$

The excessive capacitance is used in even-harmonic resonant operation mode and the same analogy can be used to calculate resonant components L_o and C_o. The equivalent capacitance of the C_x in series with C_o is given by

$$\frac{1}{C_{total}} = \frac{1}{C_o} + \frac{1}{C_x} = Q_L \cdot \omega_o \cdot R_{opt}, \tag{5.23}$$

where C_x is

$$C_x = K_x \cdot \frac{1}{\omega_o \cdot R_{opt}}, \tag{5.24}$$

leading to

$$C_o = \frac{1}{Q_L \cdot \omega_o \cdot R_{opt} - \frac{1}{C_x}} = \frac{1}{\omega_o \cdot R_{opt} \cdot (Q_L - \frac{1}{K_x})}, \tag{5.25}$$

and, once again, the resonance of L_oC_o is desired, which induces to

$$L_o = \frac{1}{\omega_o^2 \cdot C_o} = \frac{(Q_L - \frac{1}{K_x}) \cdot R_{opt}}{\omega_o}. \tag{5.26}$$

In the Table 5.2 the parameter K_L for the RFC mode was considered as infinitive, because the infinite inductor is desired, but such is not possible in reality, so it was set to 43.57, as it is calculated and presented in [5]. This value sets the minimum inductance value that will allow to keep the current ripple in the L_1 below 10 % of full-load DC input current I_{DC}.

Having analysed the generalized equations, and, with correct replacement of K parameters from Table 5.2 into those equations, the theoretical design for $P_o = 20\,dBm$ and $P_o = 13\,dBm$ are presented in Table 5.5 and Table 5.6, respectively.

Table 5.5: Class-E parameters design $P_o = 20\,dBm$.

	$R_{opt}\ [\Omega]$	$L_1\ [nH]$	$C_1\ [pF]$	Q_L	$C_t\ [pF]$	$L_t\ [nH]$
RFC	8.31	24	1.47	2	9.42	1.1
Parallel-circuit	19.66	0.954	2.31	1	3.37	1.3
Even-harmonic	0.806	0.188	5.84	12	6.85	0.380
Subharmonic	9.14	11.46	1.54	2	7.7	1.21

The C_t and L_t values presented correspond to the total capacitance and total inductance in load network, such that, in the cases where there is an excessive inductance or capacitance its series value is added to the L_o or to the C_o, i.e.,

Table 5.6: Class-E parameters design for $P_o = 13\ dBm$.

	$R_{opt}\ [\Omega]$	$L_1\ [nH]$	$C_1\ [pF]$	Q_L	$C_t\ [pF]$	$L_t\ [nH]$
RFC	41.63	120	0.293	2	1.88	5.52
Parallel-circuit	98.51	4.78	0.461	1	0.673	6.53
Even-harmonic	4.04	0.947	1.17	8	2.05	0.830
Subharmonic	45.83	57.44	0.307	2	1.54	6.08

$C_t = C_o//C_x = (C_o \cdot C_x)/(C_o + C_x)$ and $L_t = L_o + L_x$. Those values are calculated accordingly to the value chosen for Q_L, which is set as minimum as possible, in order to minimize the size of the inductance and, therefore minimize the area and cost of the circuit.

5.2.2 Design of Driver Stage Class-A Amplifier

There are many ways to design the driver stage, but its design, usually, is not simple. It has to be designed very carefully, because if the driving signal to the output stage is not optimum, all the expected results at the output stage, can be ruined.

Ideally, it would be desired that driver could provide a square wave signal to the output stage. The circuit that could provide this would be an inverter, or a Class-D power amplifier. However, its design at 2.4 GHz within 130 nm CMOS technology would be difficult as it would imply a high frequency noise that could affect frequency of interest, as well as the charging and discharging of the large capacitances in the transistors depletion zone results in a lot of power dissipation. The solution to this problem would be adopting a class-F circuit, which is capable of producing an almost square wave signal at 2.4 GHz [39]. Although knowing that Class-F would provide better results for driver stage design, the Class-A power amplifier was chosen for its design and implementation. Since this class has been thoroughly studied in the previous chapters, it is desired find better conclusions of its operation as a driver.

The purpose of this driver is to provide a large input voltage waveform, so that the transistor of the output stage could exchange from saturation to triode mode, and this way operate as switch.

Firstly, it is needed set some specifications, besides the frequency and voltage, as those were already fixed to 2.4 GHz and 1.2 V, respectively. Thus, the principal specification to be set is the output power, which must be set in order to comply with the input power required by the output stage. As it will be seen in Section 5.3.1,

sufficient input power to overdrive the output stage is about 6 dBm (4 mW). The circuit to be designed as driver Class-A is represented in Figure 5.7. The basic Class-A power amplifier would need a parallel-resonant circuit to filter only a signal in the frequency of work, as was seen in Section 3.1.1. However, it was decided to not include this resonant circuit, since the principal purpose of the driver is to amplify the input signal and addition of this circuit not only would increase a solution's cost and board space requirements, but also would introduce the possibility of additional distortion due to nonlinearities of the filter components.

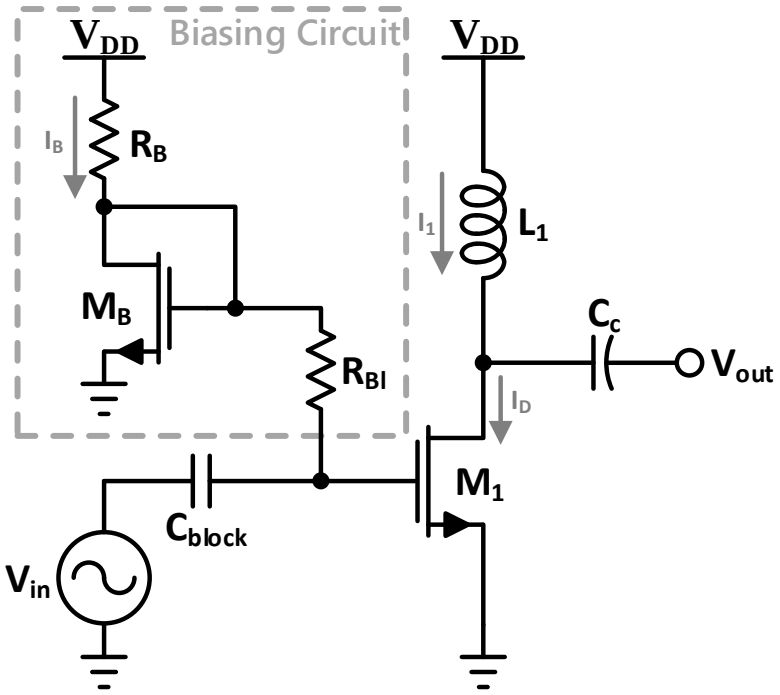


Figure 5.7: Class-A driver circuit.

Considering the minimum drain-to-source voltage drop, $v_{DS(min)}$, of 0.1 V and P_o of 7 dBm (5 mW), just to have some safety margin, the load resistance, that represents output impedance of the circuit, is

$$R_{load} = \frac{V_{o(max)}^2}{2P_o} = \frac{(V_{DD} - v_{DS(min)})^2}{2P_o} = \frac{(1.2 - 0.1)^2}{2 \times 0.005} = 120.7\ \Omega, \tag{5.27}$$

where the $V_{o(max)}$ is the maximum amplitude of the output voltage and the amplitude of the output current is

$$I_{o(max)} = \frac{V_{o(max)}}{R_{load}} = \frac{1.1}{120.7} = 9.11\ mA. \tag{5.28}$$

The DC component of the drain current can be calculated as follows

$$I_D = I_{DC} = 1.25 I_{o(max)} = 1.25 \times 9.11 \times 10^{-3} = 11.39\ mA. \tag{5.29}$$

And consequently, the maximum drain current peak is

$$I_{Dpeak} = I_D + I_{o(max)} = 11.39 \times 10^{-3} + 9.11 \times 10^{-3} = 20.5\ mA. \tag{5.30}$$

In order to suppress the imaginary part that the reactive components would create, the inductance and the coupling capacitor are set in resonance. This way, setting the quality factor of the resonant circuit to $Q_L = 1$, the inductance L_1 and coupling capacitor C_c are

$$L_1 = \frac{Q_L \cdot R_{load}}{\omega_o} = \frac{1 \times 120.7}{2\pi \times 2.4 \times 10^9} = 8\ nH, \tag{5.31}$$

$$C_c = \frac{1}{Q_L \cdot \omega_o \cdot R_{load}} = \frac{1}{1 \times 2\pi \times 2.4 \times 10^9 \times 120.7} = 549.4\ fF. \tag{5.32}$$

Now, the size of the transistors M_1 and M_B must be determined. Once again, the minimum channel length of the transistor is considered (120 nm). Considering the others transistors parameters with the following setting: $K_N \approx 0.5\ mA/V^2$, $V_{Th} = 340\ mV$ and the gate-to-source voltage $V_{GS} = 500\ mV$ (so that $V_{GS} > V_{Th} - V_{DSsat}$), the channel width is calculated trough the equation of the saturation region, as follows

$$W_{M1} = \frac{2 \cdot I_D \cdot L_{min}}{K_N \cdot (V_{GS} - V_{Th})^2} = \frac{2 \times 11.39 \times 10^{-3} \times 120 \times 10^{-9}}{0.5 \times 10^{-3}(0.5 - 0.340)^2} \simeq 214\ \mu m, \tag{5.33}$$

and the ratio between channel width and length results in

$$\frac{W_{M1}}{L_{M1}} = \frac{214\ \mu m}{120\ nm} = 1.78 \times 10^3. \tag{5.34}$$

The transconductance of the CMOS M_1 at the operating point is

$$\begin{aligned} g_m &= \sqrt{2K_N \left(\frac{W_{M1}}{L_{M1}}\right) I_D} \\ &= \sqrt{2 \times 0.5 \times 10^{-3} \times 1.78 \times 10^3 \times 11.39} = 142.4\ mS. \end{aligned} \tag{5.35}$$

As for the size of the biasing transistor, the biasing factor is set to 70:1, which means that the transistors have the same current ratio, as well as the ratio of channel sizes. Assuming that both transistors have the same channel length, the biasing current and channel with of the M_B are

$$I_B = \frac{I_D}{70} = 162.7\ \mu A, \tag{5.36}$$

and

$$W_{MB} = \frac{W_{M1}}{70} = 3.05\ \mu m. \tag{5.37}$$

Finally, the bias resistance is

$$R_B = \frac{V_{DD} - V_{GS}}{I_B} = \frac{1.2 - 0.5}{162.7 \times 10^{-6}} = 4.3\ K\Omega. \tag{5.38}$$

5.3 Simulation Results

In this section both output stage and driver simulations results are presented in the same order as previously their design was made. In Section 5.3.1 results of different operation modes of the output stage, designed in previous section, are compared and the better one is chosen with corresponding interpretation. In Section 5.3.2, by its turn, the driver simulation results are presented separately, and final simulation results are shown in Section 5.3.3.

All simulations were taken using Cadence Tools with the purpose of validating the theoretical design. Transistors were implemented in a 130 nm CMOS technology, with voltage supply V_{DD} of 1.2 V. In some cases ideal inductance was used, as it will be explained in shortly, but, most of the cases, the inductor is replaced by a model with close real effects, as well as the capacitor. The model used for those inductors and capacitors were Planar Inductor RF and Planar MIM Capacitor RF, respectively.

The schematics simulated with Cadence Tool of the driver stage, output stage and of the final blocks of the complete PA are shown, respectively, in Appendix A.2.2, in Appendix A.2.1 and in Appendix A.2.3. Input port variables presented in Appendix A.3 were set as follows: $rin = 50\ \Omega$, $fin = 2.4\ GHz$ and $pin = -15\ dBm$ for the driver, and $rin = 5\ K\Omega$, $fin = 2.4\ GHz$ and $pin = 6\ dBm$ for the output stage. It is to note that those schematics present the final solution of the proposed switching mode PA.

5.3.1 Output Stage Simulation Results

Whenever possible, the results of the four operation modes of the output stage circuit will be merged into one single plot, in order to facilitate a comparison between all circuits. The operating modes will be differentiated with letters (a), (b), (c) and (d), in which these correspond to RFC, parallel-circuit, even-harmonic resonance and subharmonic resonance, respectively.

Firstly, the transistors size is adapted to its DC operating point and input voltage has to have a sufficiently hight peak-to-peak value in order to overdrive

the transistor. Having that, the width of the NMOS transistors M_1 and M_B was set to 212.7 μm and 29.25 μm, respectively, and both use a minimal length of transistor of 120 nm. Through the analysis of Table 5.5 and Table 5.6 it is possible to conclude that some of L_1 values are either too big or too small to be implemented with real inductance model, since its range within frequency of 2.4 GHz is about $0.36 - 10.6\ nH$ (considering Planar Inductor RF model). It is possible to achieve those values through the association (in series or parallel) of several real model inductances, but this would interfere into the control of the output impedance, and consequently, it would be harder to design the output matching. Thus, it was decided to use ideal inductances for the circuits (a), (c) and (d), in order to still have a comparison between those four modes of operation. The DC operating points of the four circuits are resumed in Table 5.7.

Table 5.7: DC operating points of the Class-E output stage.

	P_{out} $[dBm]$	I_{D1} $[mA]$	I_{DC} $[mA]$	V_{Dsat} $[mV]$	V_{DS} $[V]$	gm $[mS]$
(a), (c) and (d)	20 13	14.88	16.12	161.4	1.198	120.2
(b)	20	14.68	15.93	160.7	1.17	119.5
	13	13.78	15.02	157.4	1.054	116

The load network design used in simulations was the same from Table 5.5 and Table 5.6. Even so, the output matching must also be implemented. Simple LC matching was used and two topologies were needed, which are represented in Figure 5.8. The respective parameters values of the output matching for each mode of operation and each power design are presented in Table 5.8.

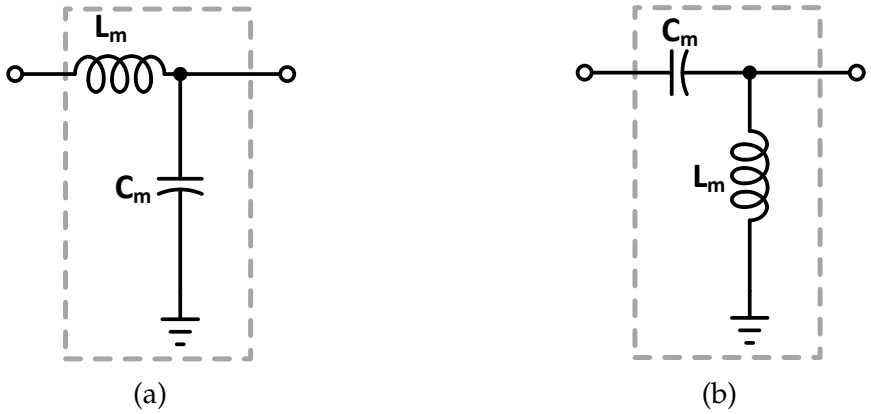
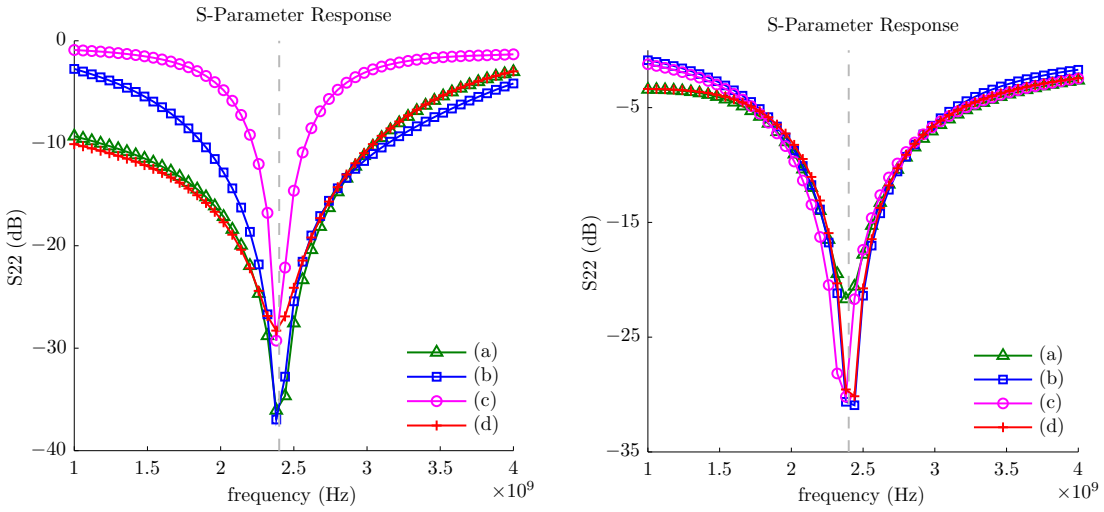


Figure 5.8: LC output matching circuits: (a) series inductance, parallel capacitance and (b) series capacitance, parallel inductance.

Table 5.8: LC dimensions of the matching circuit.

	P_{out} $[dBm]$	L_m $[nH]$	C_m $[pF]$	Type of matching
(a)	20	1.68	1.265	Figure 5.8a
	13	5.4	0.905	Figure 5.8b
(b)	20	1.28	1.31	Figure 5.8a
	13	0.862	0.655	Figure 5.8a
(c)	20	1.03	3.285	Figure 5.8a
	13	2.29	1.61	Figure 5.8a
(d)	20	1.65	1.26	Figure 5.8a
	13	4.58	0.846	Figure 5.8b

Through the S-parameters simulation of the S_{22}, results represented in Figure 5.9, it is possible to verify that, of all operating modes and of the two power designs, the output return loss S_{22} ranges from $-20\ dB$ to $-37\ dB$, which is quite good, since it can be considered as well matched if S_{22} is lower than -10 dB.



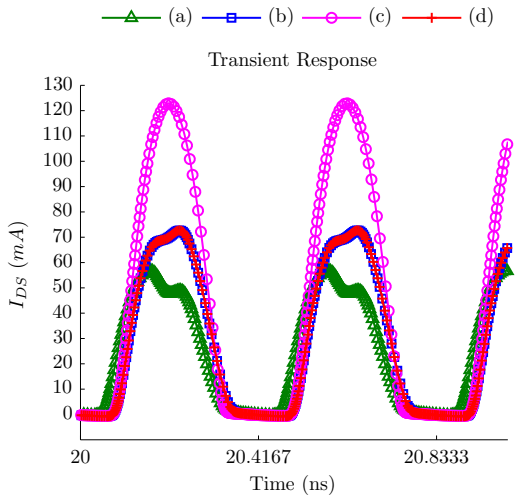
(a) Design for $P_{out} = 20\ dBm$.

(b) Design for $P_{out} = 13\ dBm$.

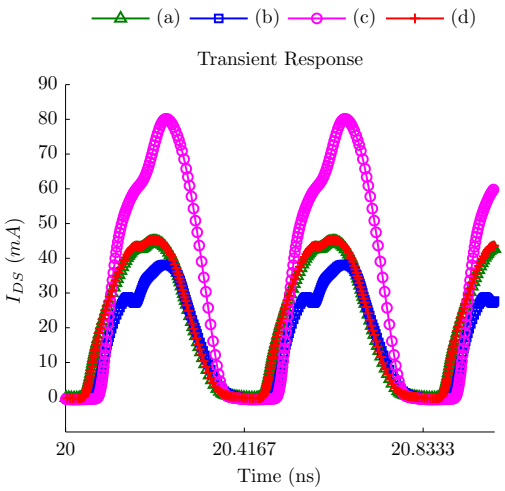
Figure 5.9: S22 parameter simulation results versus frequency.[2]

But to prove that those circuits are operating as a Class-E power amplifier it is necessary to run transient simulation of the drain current of the transistor M_1 and drain-to-source voltage. These results are shown in Figure 5.10 and Figure 5.11, where it should be noted that (c) circuit presents too high current, as well as voltage

[2]in the legend embedded within the figure the alphabetical letters mean: (a) - RFC, (b) - parallel-circuit, (c) - even-harmonic resonance and (d) - subharmonic resonance.

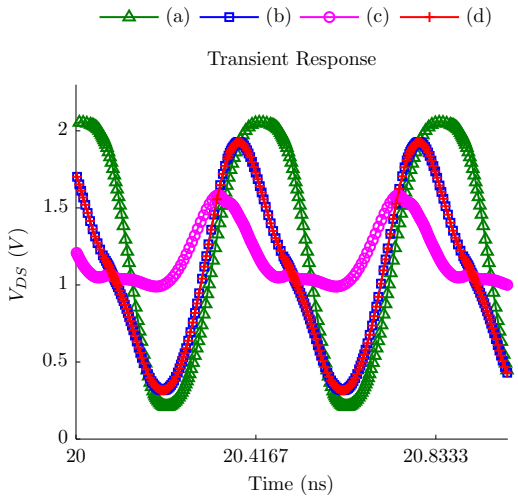


(a) Design for $P_{out} = 20\ dBm$.

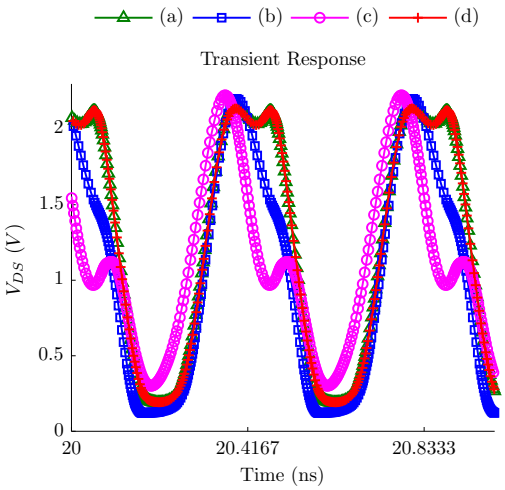


(b) Design for $P_{out} = 13\ dBm$.

Figure 5.10: Transient waveforms of the drain current.[2]



(a) Design for $P_{out} = 20\ dBm$.

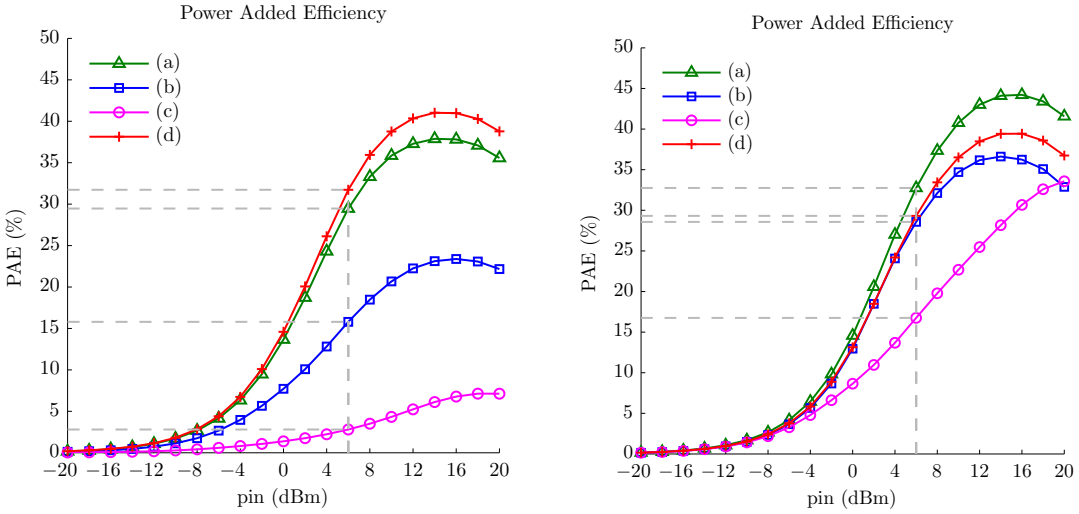


(b) Design for $P_{out} = 13\ dBm$.

Figure 5.11: Transient waveforms of drain-to-source voltage.[2]

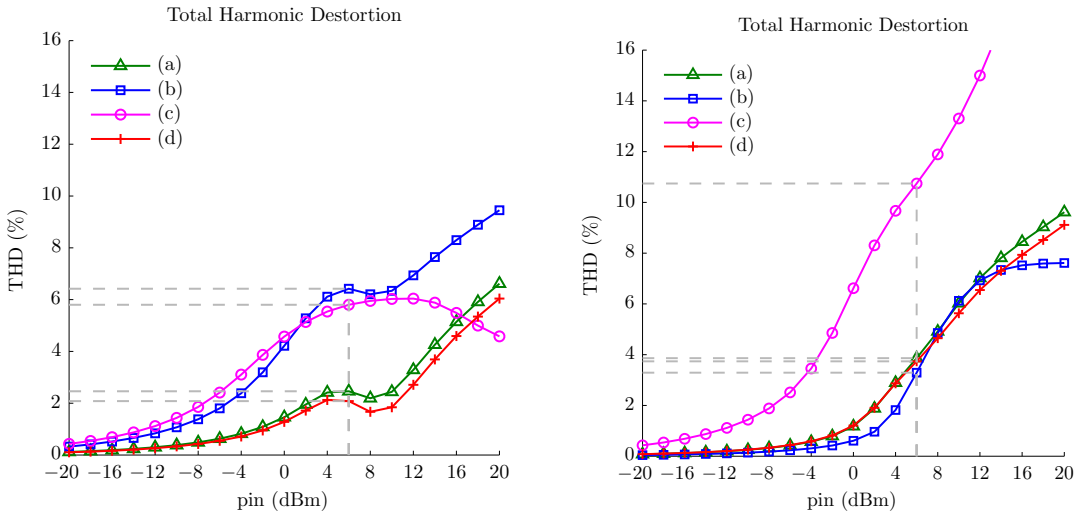
of all circuits does not have the desired waveform for design of $P_{out} = 20\ dBm$. By that means that voltage waveform should reach zero value (or almost) at the same period that current waveform moves away from zero value. Those are the drawbacks, but, as advantage, the design of $P_{out} = 13\ dBm$ present satisfactory waveforms.

What follows are the PAE, THD and output power simulations in function of input power, presented in Figure 5.12, Figure 5.13 and in Figure 5.14, respectively. These simulations were performed by using, once again, the SpectreRF engine from Cadence Design Systems and all of three were held with swept PSS simulation.



(a) Design results for $P_{out} = 20\ dBm$. (b) Design results for $P_{out} = 13\ dBm$.

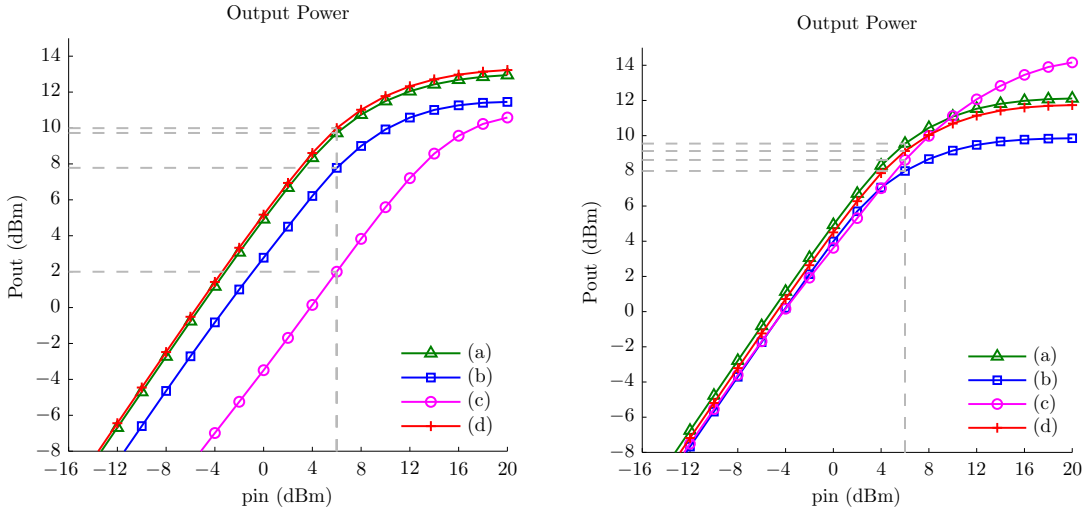
Figure 5.12: PAE simulation versus input power.[2]



(a) Design results for $P_{out} = 20\ dBm$. (b) Design results for $P_{out} = 13\ dBm$.

Figure 5.13: THD simulation versus input power.[2]

Analysing these figures it is possible to conclude immediately that the (c) circuit presents the worst results, too small PAE and too big THD, which turns it impracticable for any application at 2.4 GHz, even more for Bluetooth application, that requires efficiency as high as possible with the lowest THD as possible. It is not only impracticable because of its results, but also because of its too small parameters sizing, which also may justify the results. It is also possible to see instantly from Figure 5.14 that it does not matter if the circuit was designed to higher output power or lower, since the output power at the required input power had changed practically nothing along two power designs. The explanation is



(a) Design results for $P_{out} = 20\ dBm$. (b) Design results for $P_{out} = 13\ dBm$.

Figure 5.14: Output power simulation versus input power.[2]

simple, since the same transistors size was used for all designs, which is optimum for lower power design, i.e. for $P_{out} = 13\ dBm$, as it was seen from transient results, for higher power design it suffers from transistors size limitation. Even so, if analysing only one of the four circuits for the two power designs, when higher PAE is obtained higher THD is as well followed. So there is always a trade-off between efficiency and distortion. The output matching also plays a big role when it comes to distortion, as it is affected principally by reactive components, and that might be the reason for the unexpected results of the (b) circuit for $P_{out} = 20\ dBm$.

Summing it all, the results for the input power considered, which was tested by specifying the input power of the input port, are shown in Table 5.9.

The circuit (c) and the design for $P_{out} = 20\ dBm$ were already put away, so there are only three circuits remaining for $P_{out} = 13\ dBm$ design to be discussed. The circuit (a) presents the better result for PAE for the input power of 6 dBm and the circuit (b) better results for THD. It is worth recollecting that the circuit (b) is the only one that was simulated with L_1 with real model and, even if the real model had been used for the other circuits it is obvious that PAE would decrease and THD would have increased, as it was discussed in Chapter 4. Additionally, there are size issues, bigger size of the L_1 implies evidently bigger circuit area, as well as its cost. Recalling to the Table 5.6, the L_1 values used for circuits (a), (b) and (d) were of 120 nH, 4.78 nH and 57.44 nH, respectively, and, as a result, the circuit (b) is the preferred one and chosen to be implemented with driver stage.

Table 5.9: Performance of the output stage Class-E power amplifier for pin=6 dBm.

	Design for P_{out} $[dBm]$	PAE [%]	THD [%]	$P_{out}[dBm]$ $(pin = 6\,dBm)$	Input 1dB C.P. [dBm]	IIP3 [dBm]
(a)	20	29.47	2.46	9.72	4.03	13.75
	13	32.75	3.86	9.55	4.13	15.27
(b)	20	15.8	6.42	7.78	2.29	10.6
	13	28.57	3.29	7.99	3.1	14.45
(c)	20	2.81	5.8	1.99	-1.94	5.74
	13	16.75	10.74	8.62	0.319	9.42
(d)	20	31.73	2.08	9.99	4.09	13.84
	13	29.31	3.74	9.13	4.1	15.17

5.3.2 Driver Stage Simulation Results

The designed parameters of the drive stage are presented in Table 5.10, where the size of the transistors was adjusted in order to approximate DC operating point to the theoretical values. Thus, the DC operating point achieved by those values is

Table 5.10: Theoretical and simulated dimensions of the driver stage.

	W_{M1} $[\mu m]$	W_{MB} $[\mu m]$	L_1 $[nm]$	C_c $[fF]$	$R_{(b)}$ $[K\Omega]$
Theoretical	*214*	*3.05*	*8*	*549*	*4.3*
Simulated	*144*	*3.6*			

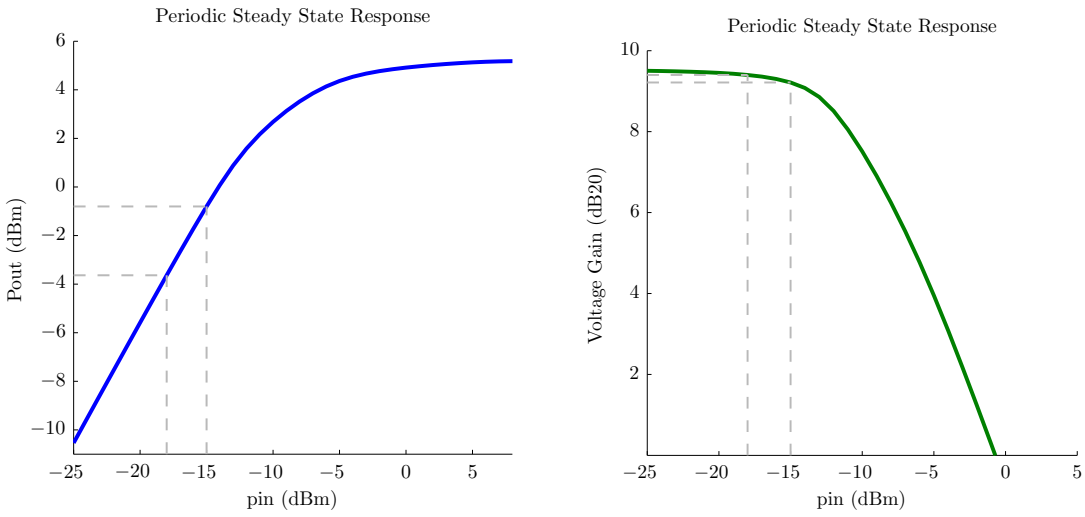
represented in Table 5.11

Table 5.11: DC operating points of the driver stage.

I_{D1} $[mA]$	I_{DC} $[mA]$	V_{Dsat1} $[mV]$	V_{DS} $[V]$	gm $[mS]$
9.99	10.14	161.5	1.04	80.82

Through a swept PSS analysis, it is represented in Figure 5.15 output power and voltage gain results, as well as in Figure 5.16 PAE and THD, all in function of input power.

The required output power from the driver design (6 dBm) is almost reached, but for higher input power level, which presents worst results for voltage gain and THD. Yet, the most important aspect that need to have better results are the voltage gain and THD. High voltage gain would mean a sufficiently high voltage



(a) (b)

Figure 5.15: Results of the Driver: a) output power; b) voltage gain.

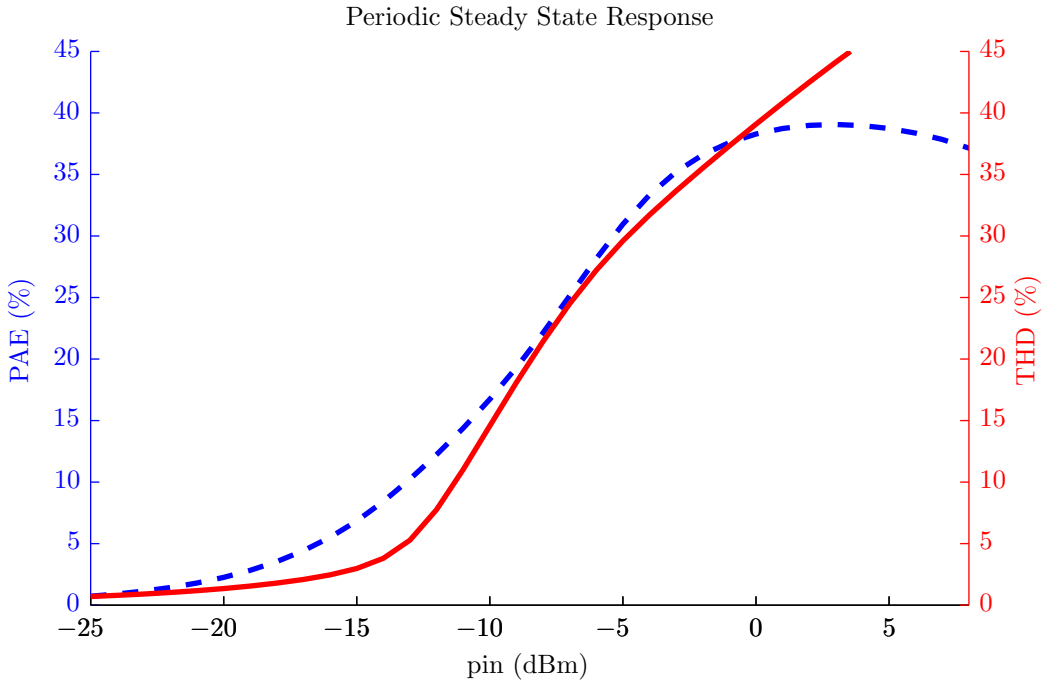


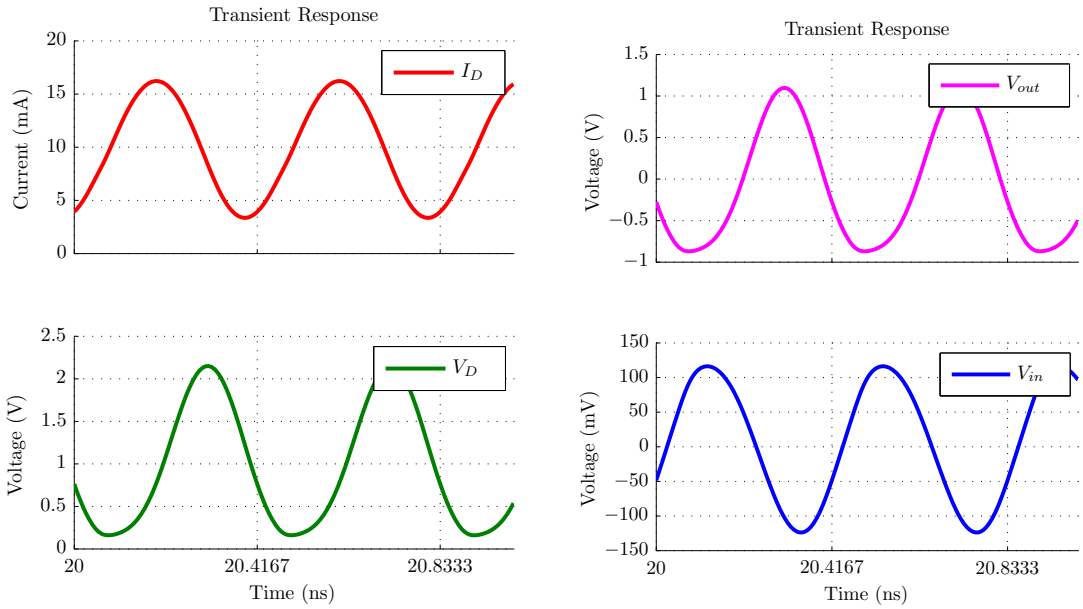
Figure 5.16: PAE and THD of the driver. stage.

amplitude in the driver output and lower THD is needed in order to not add more distortion to the output stage.

From Figure 5.16 it is seen what already has been said, that there are always a trade-off between PAE and THD. Hence, analysing these three figures, the range of the input power level that allows a better trade-off is from -18 dBm to -15 dBm.

Considering a input power of -15 dBm, the transient response is shown in Figure 5.17. The amplitude of the input voltage is about 100 mV (peak voltage),

while the amplitude of the output voltage achieves near to 1 V, resulting in an amplification of 10 times.



(a) (b)

Figure 5.17: Transient waveforms of the Driver: a) drain current (top) and drain-to-source voltage (bottom); b) output voltage (top) and input voltage (bottom).

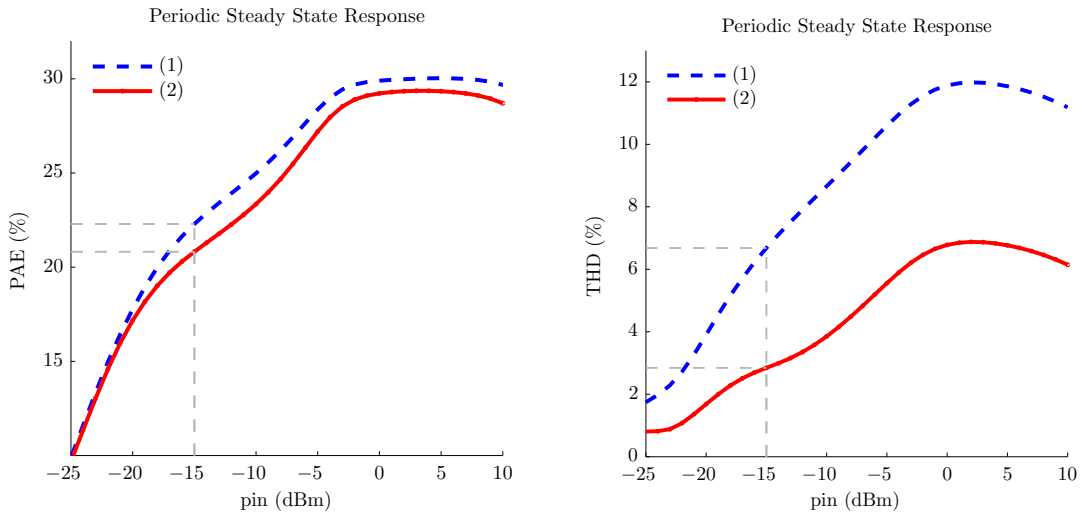
5.3.3 Simulation Results of the Complete PA

In the previous sections, simulation results of the output and driver stages were presented separately. Thus, it is desirable to analyse the overall results and the real effect that driver has on the output stage. Interconnecting the two stages by a sequence of blocks already represented in Figure 5.5, the simulations were performed and it was noted that THD increased a lot. As a result some adjustments were made in order to improve that. Some improvement could be done on the driver stage, as it has no tuning load, but it would reduce the voltage amplitude and, hence, reduce the overdriven condition. So, it was opted for adjustment of the load network at the output stage.

The previous design and a new one are presented in Table 5.12. The results of the two designs, driver together with the output stage with previous design and driver plus the output stage with the adjustments, are presented through graphics in Figure 5.18 and in Figure 5.19.

Table 5.12: Load network dimensions of the output stage: (1) before adjustments; (2) after adjustments.

	$L_1\ [nH]$	$C_1\ [pF]$	$L_o\ [nH]$	$C_o\ [pF]$	$L_m\ [nH]$	$C_m\ [pF]$
(1)	4.78	0.461	6.53	0.673	0.862	0.655
(2)	8.87	0.495	6.51	0.679	0.900	0.600



(a) PAE. (b) THD.

Figure 5.18: Simulation results of the two designs versus input power.[3]

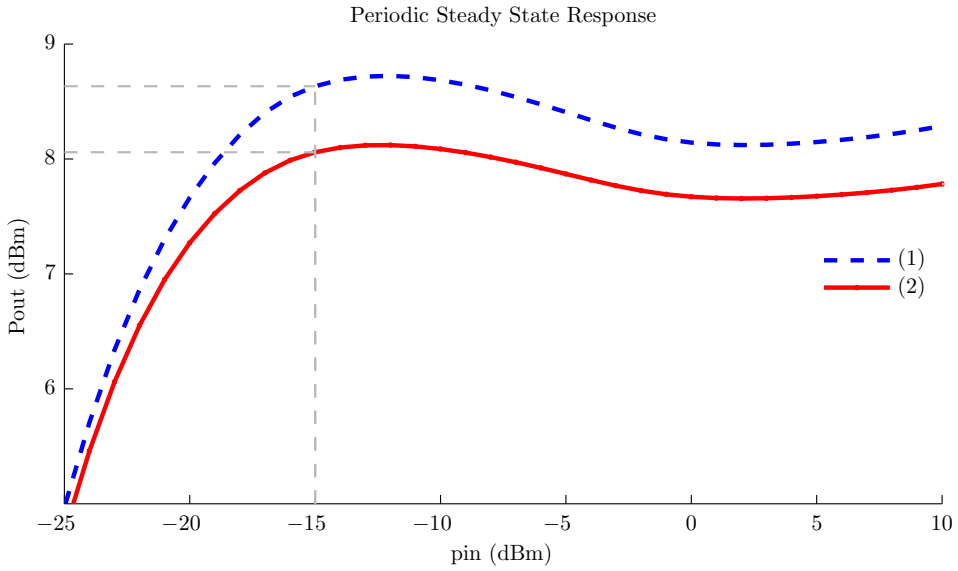


Figure 5.19: Output power simulation of the two designs versus input power.[3]

[3]in the legend embedded within the figure the numbering means: (1) driver together with the output stage with previous design and (2) driver plus the output stage with the adjustments.

In the Table 5.13 is presented the overview of the results presented in the figures above for input power of -15 dBm. Once again, there is the trade-off between the THD and PAE/P_{out}. It is achieved better THD in exchange of a lower PAE and output power. Even so, with new adjustments this trade-off is much better than the previous one, since the improvement of the THD compensates the loss of the PAE and P_{out}.

Table 5.13: Comparison of the performance of the two designs for pin=-15 dBm.[3]

	P_{out} $[dBm]$	PAE [%]	THD [%]
(1)	*8.63*	*22.29*	*6.68*
(2)	*8.06*	*20.81*	*2.84*

Yet, analysing the Figure 5.18 and Figure 5.19, it is possible to conclude that the input power level that achieves better trade-off between the THD and PAE/P_{out} is, indeed, at -15 dBm. Therefore, the transient waveforms and the final results for the proposed design are stated in Figure 5.20, in Figure 5.21 and in Table 5.14, respectively.

Analysing Figure 5.20 and Figure 5.21, it is possible to verify that drain current has some irregular spikes, which may occur because of the non-linear effect of the output parasitic capacitance. Additionally, since sinusoidal input drive was considered, the drain current tend to follow the drive signal, resulting in mis-match between drain current and drain-to-source voltage. However, a good voltage amplification is obtained, where with input peak-to-peak voltage of 0.2 V resulted in driver peak-to-peak voltage of 1 V and an amplification to 1.6 V of output voltage.

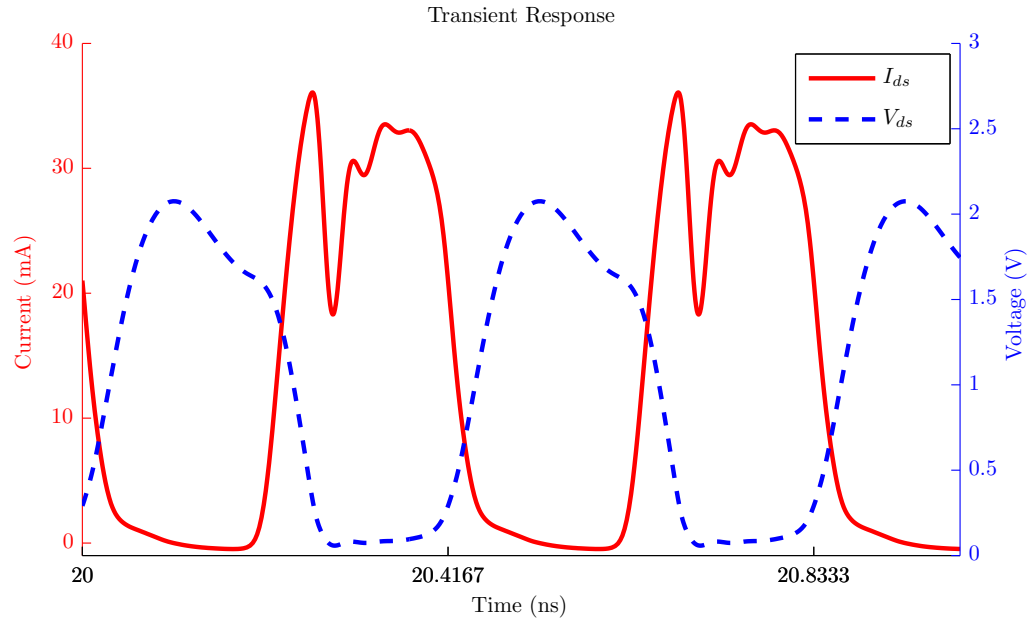


Figure 5.20: Transient Response of the drain current and drain-to-source voltage.

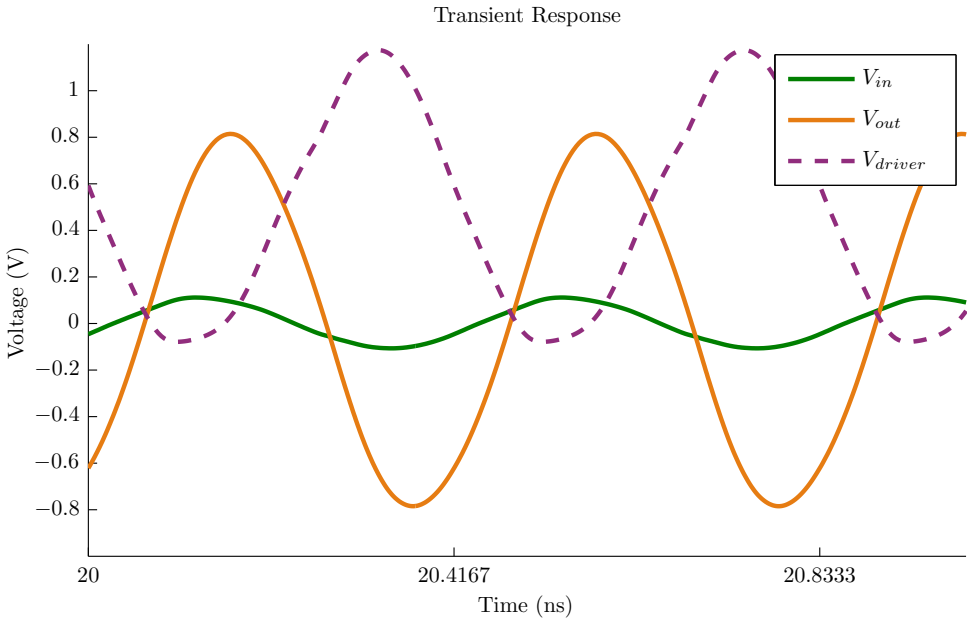


Figure 5.21: Transient Response of the input voltage, output voltage and voltage from the driver.

The comparison between this Bluetooth power amplifier design and other solutions is shown in Table 5.15. It is to mention that all other solutions were designed to comply to the 20 dBm output power for Bluetooth application, while this work was designed for 13 dBm. These solutions suppose higher input power level, while this work is capable to work with -15 dBm. Additionally, they propose some specific techniques/topology that allow to have better performance, whereas

Table 5.14: Performance of the proposed power amplifier for pin=-15 dBm

	Value		Value
Output Power P_o $[dBm]$	*8.06*	*Input 1 dB C.P.* $[dBm]$	*-18.68*
Output Power P_o $[mW]$	*6.4*	*Output 1 dB C.P.* $[dBm]$	*7.59*
PAE [%]	*20.81*	$InputIP3$ $[dBm]$	*-17.5*
THD [%]	*2.84*	$OutputIP3$ $[dBm]$	*5.96*
$2 \cdot f_o$ *Harmonic* $[dBc]$	*-35.82*	*Power Gain* P_G $[dB10]$	*30.62*
$3 \cdot f_o$ *Harmonic* $[dBc]$	*-32.73*	*Power Consumption* $[mW]$	*29.74*

this one uses no additional technique and still has good performance. Techniques and topologies such as: driver with positive feedback [40], latch-structured driver [41], cascode topology with self-biasing [42], differential PA connected with LC balun [43] and output power control with voltage combining transformer in [44].

Table 5.15: Performance comparison of Bluetooth.

Reference	Technology	P_out [dBm]	PAE [%]	η_d [%]	V_{DD} [V]	Fully Integrated	Differential	Single-ended
[40]	0.35 $\mu mCMOS$	19	35	37	1		x	
[41]	0.25 $\mu mCMOS$	20	65	66.4	2			
[45]	0.35 $\mu mCMOS$	13	30.7	-	-	x		x
[42]	0.18 $\mu mCMOS$	19.2	27.8	-	3.3			x
[43]	0.13 $\mu mCMOS$	23	29	35	1.5	x		x
[44]	0.13 $\mu mCMOS$	27	-	32	1.2	x		x
[22]	0.13 $\mu mCMOS$	22.7	36	48	1		x	
this work	0.13 $\mu mCMOS$	8	20.8	21.5	1.2			x

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

In this thesis an RF Class-E ZVS power amplifier together with RF Class-A driver in standard 130 nm CMOS technology were presented. Each circuit was implemented in a single-ended configuration. The validation of the presented work was performed through the design and schematics simulation, using real models for the reactive components.

From the initial design of the Class-E power amplifier four modes of operation were considered: RFC, parallel-circuit, even-harmonic resonance and subharmonic resonance. The even-harmonic and the subharmonic resonances aim to use LC circuit in order to resonate at even harmonics or at harmonic below the fundamental, respectively. On the other hand, the RFC mode uses a load inductance with infinite value and the parallel-circuit, with small finite DC-feed inductance, has a lot of possibilities of designs (design to the maximum output power was chosen). Comparison between all these modes of operation was made with the simulation results. While the even-harmonic resonance presented the worst results from all other modes of operation, the parallel-circuit brought out the best results. Thus, the final output stage is summed up to 28.6 % PAE, 3.3 % THD and 8 dBm output power.

The final simulation results, driver plus output stage, showed reduction of about 10 % of the PAE and similar results for the THD and output power. Even so, this was expected, since the driver was implemented as Class-A amplifier greatest linearity is achieved, but worst efficiency is obtained because its transistor

operate all the time and this results in great power loss. Even so, the final circuit consumption is of 28 mW, using a 1.2 V supply voltage and the power at undesired harmonics is at least -30 dB below the power at the fundamental (2.4 GHz), which makes this circuit suitable to cope with the requirements of the Bluetooth application.

6.2 Future Work

In the present work there are always changes and improvements that can be made, in order to make this project more compatible to the targeted application. The possible improvements to be made in the future works, that fall outside the scope of this thesis, are listed in the following topics:

- The design and implementation of the switching mode PA obtained reasonable values of parameters, like PAE, THD and output power, and small dimensions of the circuit designed for the work application. However, nowadays the Bluetooth application need even more efficient PA, with more output power to reach higher distance of the signal transmission, and with smaller circuit occupation in the transmitter, as well as lower power consumption, so that the batteries lifetime could be improved. This could be improved by redesigning the switching transistor, as in this work it was designed to maximum output power of 13 dBm, as well as by considering other type of driver.

- The output matching sometimes was difficult to be designed. As it is composed by reactive components, they caused some reduction of the PAE, but specially, their greatest influence is in the THD increasing. Thus, the better techniques to match to the load antenna should be investigated.

- The design of the present Class-E PA were made by the assumption of linear output capacitances of the transistor and a fixed duty cycle of 50 %. Thus, it is would be interesting to consider output capacitances non-linearities and test with other values of duty cycle.

- The proposed design tested the theoretical equation through the simulations, being somewhat theoretical. Therefore, the circuit design should be implemented in the layout process and validated by means of a test of post-layout circuit.

- Study of new techniques to improve efficiency of the PA remains as one of the greatest challenges in the standard CMOS technology. This improvement could be done by using some linearisation technique.
- Full integration of the PA into the whole transmitter could also be made.
- Use improved standard technology, such as 90 nm or even 65 nm CMOS technologies, so that the area occupation and its cost could be minimized.
- Improvement of this power amplifier towards the higher frequency applications should also be considered.

BIBLIOGRAPHY

[1] A. Rajaie, A. Khorshid, and A. Darwish. "Recent Implementations of Class-E Power Amplifiers". In: *2012 Japan-Egypt Conference on Electronics, Communications and Computers*. 2012.

[2] P. Reynaert and M. Steyaert. *RF Power Amplifiers for Mobile Communications*. Springer, 2006.

[3] J. Decuir. "Bluetooth 4.0: Low Energy". In: *Cambridge, UK: Cambridge Silicon Radio SR plc* (2010).

[4] SIG Bluetooth. "Specification of the Bluetooth System, version 1.2". In: *Bluetooth SIG Standard* (Nov. 2003).

[5] M. K. Kazimierczuk. *RF Power Amplifiers*. John Wiley & Sons, 2014.

[6] A. Zolfaghari. *Low-Power CMOS Design for Wireless Transceivers*. Springer Science & Business Media, 2013.

[7] J. Crols and M. Steyaert. *CMOS Wireless Transceiver Design*. Vol. 411. Springer Science & Business Media, 2013.

[8] B. Razavi. *RF Microelectronics*. 2nd Edition. Prentice Hall, 2012.

[9] H. S. Ruiz and R. B. Pérez. *Linear CMOS RF Power Amplifiers*. Springer, 2014.

[10] B. Berglund, J. Johansson, and T. Lejon. "High Efficiency Power Amplifiers". In: *Ericsson Review* 83.3 (2006), pp. 92–96.

[11] W. J. Chudobiak and D. F. Page. "Frequency and Power Limitations of Class-D Transistor Amplifiers". In: *IEEE Journal of Solid-State Circuits* 4.1 (1969), pp. 25–37.

[12] H. Kobayashi, J. M. Hinrichs, and P. M. Asbeck. "Current-Mode Class-D Power Amplifiers for High-Efficiency RF Applications". In: *IEEE Transactions on Microwave Theory and Techniques* 49.12 (2001), pp. 2480–2485.

[13] T.-P. Hung, A. Metzger, P. Zampardi, M. Iwamoto, and P. Asbeck. "Design of High-Efficiency Current-Mode Class-D Amplifiers for Wireless Handsets". In: *IEEE Transactions on Microwave Theory and Techniques* 53.1 (2005), pp. 144–151. ISSN: 0018-9480.

[14] D. Oliveira. "CMOS-RF Power Amplifier for Wireless Communications". M.S. Thesis. Faculdade de Engenharia da Universidade do Porto, 2009.

[15] F. M. Barradas. "RF Parametric Amplifiers". M.S. Thesis. Universidade de Aveiro, 2012.

[16] D. K. Choi. "High Efficiency Switched-Mode Power Amplifiers for Wireless Communications". Ph.D. Thesis. University of California Santa Barbara, 2001.

[17] A. Grebennikov, N. O. Sokal, and M. J. Franco. *Switchmode RF and Microwave Power Amplifiers*. 2nd Edition. Academic Press, 2012.

[18] N. Sokal and A. Sokal. "Class E-A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers". In: *IEEE Journal of Solid-State Circuits* 10.3 (1975), pp. 168–176. ISSN: 0018-9200.

[19] G. D. Ewing. "High-Efficiency Radio-Frequency Power Amplifiers". Ph.D. Thesis. Oregon State University, 1964.

[20] C. Yoo and Q. Huang. "A Common-Gate Switched 0.9-W Class-E Power Amplifier with 41% PAE in 0.25-μm CMOS". In: *IEEE Journal of Solid-State Circuits* 36.5 (2001), pp. 823–830.

[21] K.-W. Ho and H. Luong. "A 1-V CMOS Power Amplifier for Bluetooth Applications". In: *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 50.8 (2003), pp. 445–449. ISSN: 1057-7130.

[22] J. Fritzin and A. Alvandpour. "Low Voltage Class-E Power Amplifiers for DECT and Bluetooth in 130nm CMOS". In: *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2009. SiRF'09*. IEEE. 2009, pp. 1–4.

[23] A. Mazzanti, L. Larcher, R. Brama, and F. Svelto. "Analysis of Reliability and Power Efficiency in Cascode Class-E PAs". In: *IEEE Journal of Solid-State Circuits* 41.5 (2006), pp. 1222–1229.

[24] T. Sowlati, C. Salama, J. Sitch, G. Rabjohn, and D. Smith. "Low Voltage, High Efficiency GaAs Class E Power Amplifiers for Wireless Transmitters". In: *IEEE Journal of Solid-State Circuits* 30.10 (1995), pp. 1074–1080. ISSN: 0018-9200.

[25] F. H. Raab. "Idealized Operation of the Class E Tuned Power Amplifier". In: *IEEE Transactions on Circuits and Systems* 24.12 (1977), pp. 725–735.

[26] M. K. Kazimierczuk and K. Puczko. "Exact Analysis of Class E Tuned Power Amplifier at any Q and Switch Duty Cycle". In: *IEEE Transactions on Circuits and Systems* 34.2 (1987), pp. 149–159.

[27] P. Alinikula, K. Choi, S. Long, et al. "Design of Class E Power Amplifier with Nonlinear Parasitic Output Capacitance". In: *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 46.2 (1999), pp. 114–119.

[28] D. K. Choi and S. Long. "The Effect of Transistor Feedback Capacitance in Class-E Power Amplifiers". In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* 50.12 (2003), pp. 1556–1559.

[29] X. Wei, H. Sekiya, S. Kuroiwa, T. Suetsugu, and M. K. Kazimierczuk. "Effect of MOSFET Gate-to-Drain Parasitic Capacitance on Class-E Power Amplifier". In: *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2010, pp. 3200–3203.

[30] P. Alinikula. "Optimum Component Values for a Lossy Class E Power Amplifier". In: *Microwave Symposium Digest, 2003 IEEE MTT-S International*. Vol. 3. IEEE. 2003, pp. 2145–2148.

[31] S. Jee, J. Moon, J. Kim, J. Son, and B. Kim. "Switching Behavior of Class-E Power Amplifier and Its Operation Above Maximum Frequency". In: *IEEE Transactions on Microwave Theory and Techniques*, 60.1 (2012), pp. 89–98.

[32] C.-H. Li and Y.-O. Yam. "Maximum Frequency and Optimum Performance of Class E Power Amplifiers". In: *IEE Proceedings-Circuits, Devices and Systems* 141.3 (1994), pp. 174–184.

[33] D. Y. Lie, P. Lee, J. D. Popp, J. F. Rowland, H. H. Ng, and N. H. Yang. "The Limitations in Applying Analytic Design Equations for Optimal Class E RF Power Amplifiers Design". In: *IEEE VLSI-TSA International Symposium on VLSI Design, Automation and Test, 2005.(VLSI-TSA-DAT). 2005*. IEEE. 2005, pp. 161–164.

[34] A. V. Grebennikov and H. Jaeger. "Class E with Parallel Circuit - A New Challenge for High-Efficiency RF and Microwave Power Amplifiers". In: *Microwave Symposium Digest, 2002 IEEE MTT-S International*. Vol. 3. IEEE. 2002, pp. 1627–1630.

[35] D. Milosevic, J. van der Tang, and A. Van Roermund. "Explicit Design Equations for Class-E Power Amplifiers with Small DC-Feed Inductance". In: *Proceedings of the 2005 European Conference on Circuit Theory and Design*. Vol. 3. IEEE. 2005, pp. 101–104.

[36] M. Acar, A. Annema, and B. Nauta. "Analytical Design Equations for Class-E Power Amplifiers". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 54.12 (2007), pp. 2706–2717. ISSN: 1549-8328.

[37] M. Acar, A. Annema, and B. Nauta. "Generalized Design Equations for Class-E Power Amplifiers with Finite DC Feed Inductance". In: *Microwave Conference, 2006. 36th European*. 2006, pp. 1308–1311.

[38] A. Grebennikov. "Load Network Design Techniques for Class E RF and Microwave Amplifiers". In: *High Frequency Electronics* 3.7 (2004), pp. 18–32.

[39] R. Kubowicz. "Class-E Power Amplifier". M.S. Thesis. University of Toronto, 2000.

[40] K. W. Ho. "A 1-V CMOS Power Amplifier for Bluetooth Applications". M.S. Thesis. The Hong Kong University of Science and Technology, 2002.

[41] Y.-S. Choi, H.-H. Choi, and T.-H. Kwon. "A 2.4-GHz Latch-Structured Power Amplifier for Bluetooth". In: *The 9th Russian-Korean International Symposium on Science and Technology, 2005. KORUS 2005. Proceeding*. IEEE. 2005, pp. 834–837.

[42] S. Murad, R. Pokharel, H. Kanaya, and K. Yoshida. "A 2.4 GHz 0.18-μm CMOS Class E Single-ended Power Amplifier without Spiral Inductors". In: *2010 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*. 2010, pp. 25–28.

[43] P. Reynaert and M. Steyaert. "A 2.45-GHz 0.13-CMOS PA With Parallel Amplification". In: *IEEE Journal of Solid-State Circuits*, 42.3 (2007), pp. 551–562.

[44] G. Liu, P. Haldi, T.-J. K. Liu, and A. M. Niknejad. "Fully Integrated CMOS Power Amplifier with Efficiency Enhancement at Power Back-off". In: *IEEE Journal of Solid-State Circuits* 43.3 (2008), pp. 600–609.

[45] T. Oshima and M. Kokubo. "Simple Polar-loop Transmitter for Dual-mode Bluetooth". In: *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*. IEEE. 2005, pp. 3966–3969.

[46] D. A. Johns, K. W. Martin, and T. C. Carusone. *Analog Integrated Circuit Design*. 2nd Edition. John Wiley & Sons, 2012.

[47] R. Harrison. “MOSFET Operation in Weak and Moderate Inversion”. In: *University of Utah* ().

APPENDIX A

SCHEMATICS

A.1 Class-A Schematic

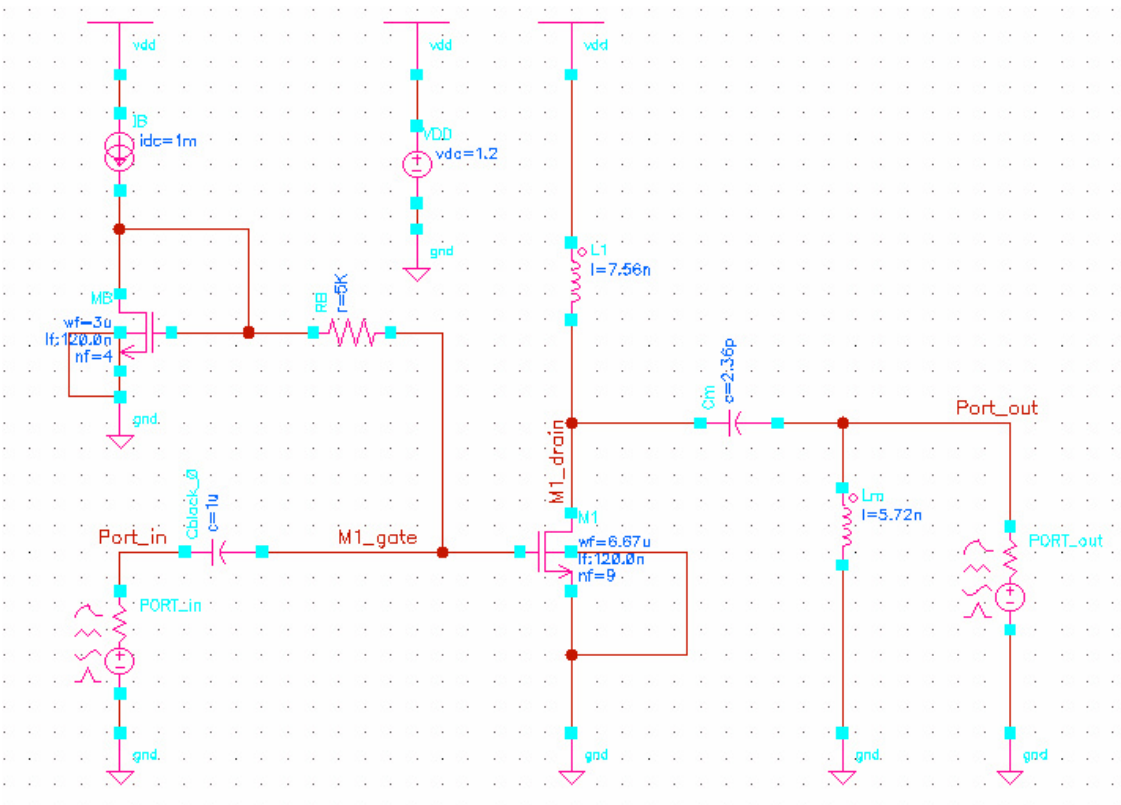


Figure A.1: Schematic of the Class-A power amplifier with ideal models of the LC components.

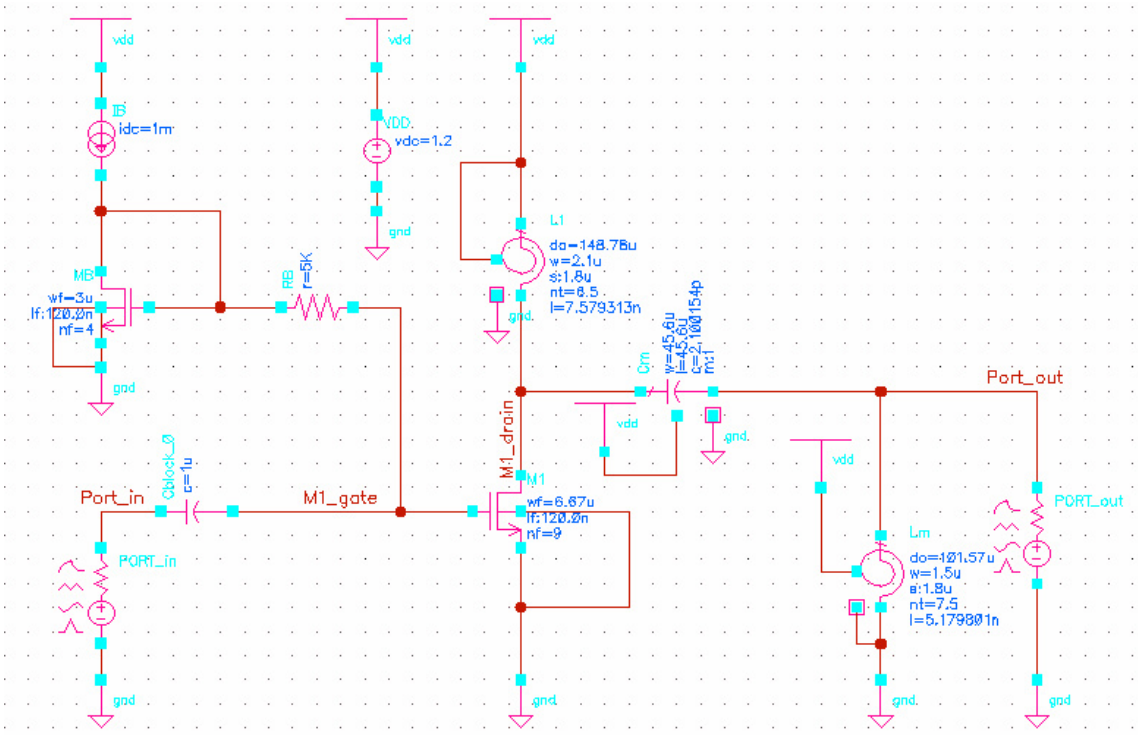


Figure A.2: Schematic of the Class-A power amplifier with real models of the LC components.

A.2 RF PA Final Solution Schematics

A.2.1 Class-E Schematic

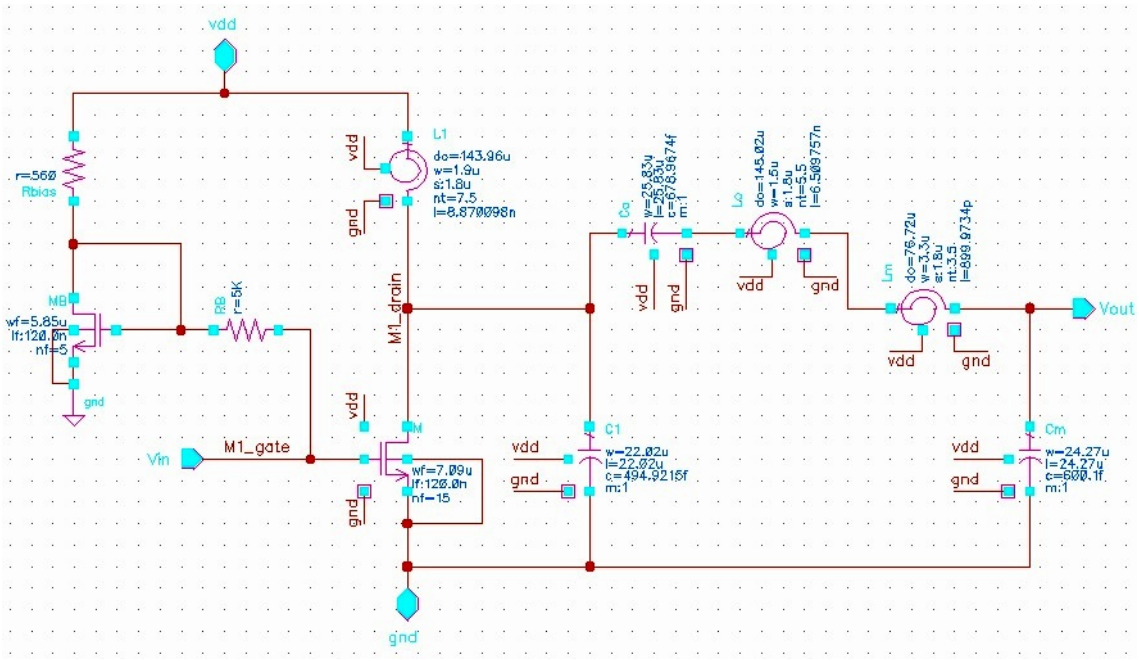


Figure A.3: Schematic of the Class-E power amplifier with parallel-circuit operation mode.

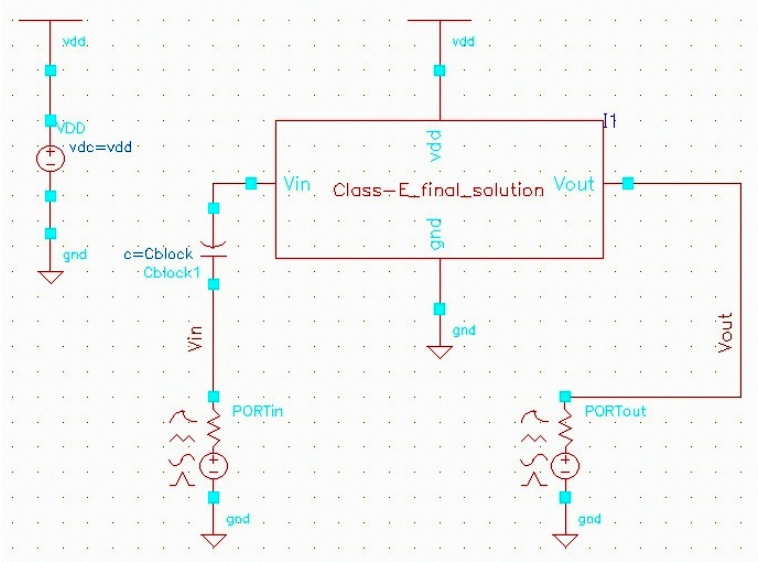


Figure A.4: Schematic of the simulated driver block.

A.2.2 Driver Schematic

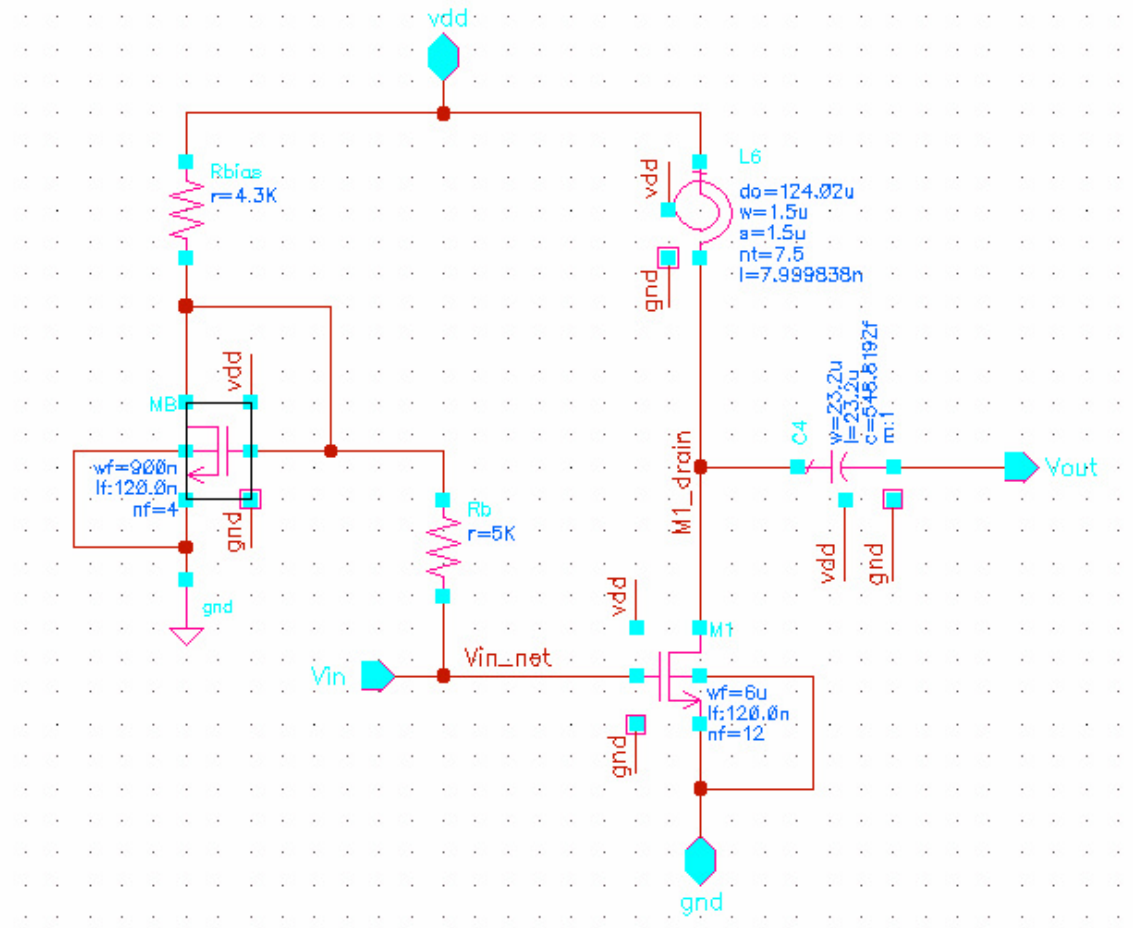


Figure A.5: Schematic of the Class-A driver.

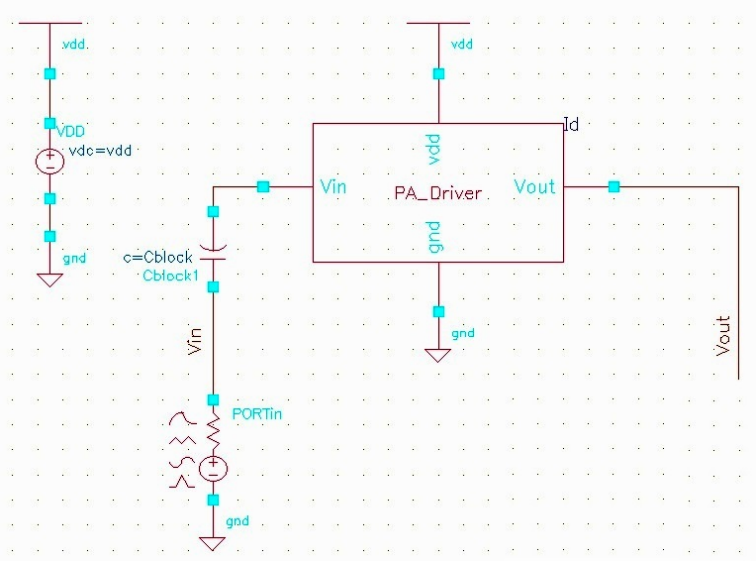


Figure A.6: Schematic of the simulated driver block.

A.2.3 Final Blocks Schematic

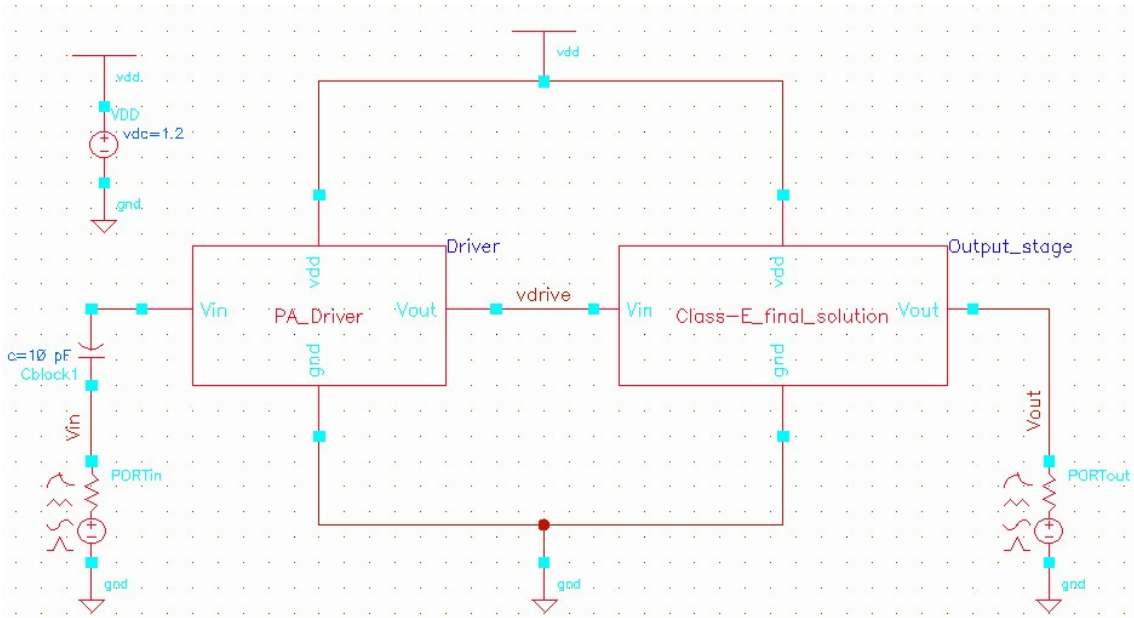
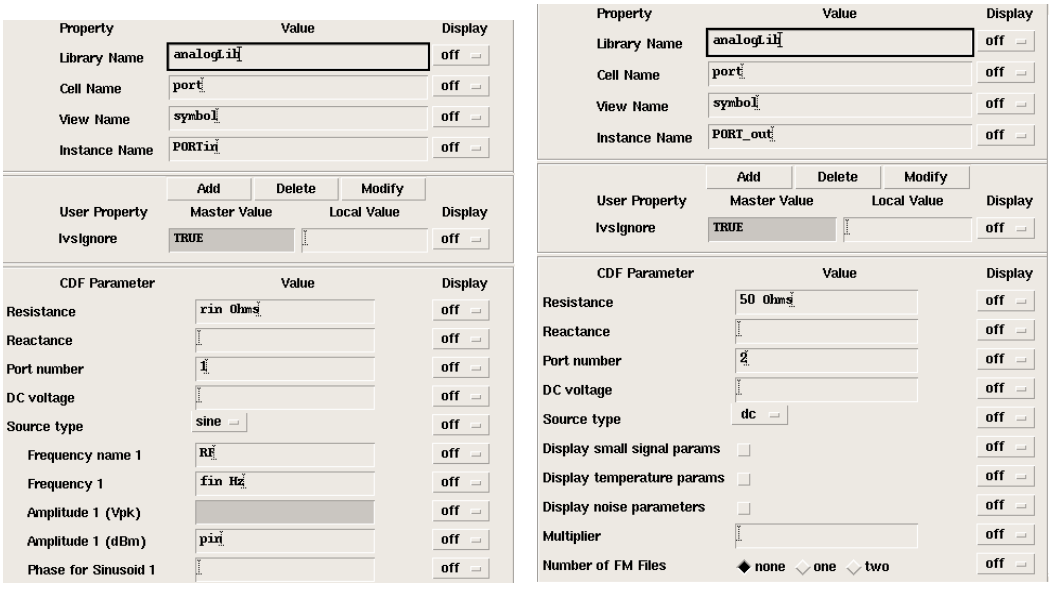


Figure A.7: Schematic of the blocks, one containing driver schematic and other output stage schematic.

A.3 Input and Output Ports Setting



(a) Input port parameters. (b) Output port parameters.

Figure A.8: Definition of the input and output ports parameters.

APPENDIX B

CMOS TRANSISTORS

B.1 Structure of MOS transistors

Figure B.1 represents the basic geometric top view of the CMOS transistor layout. It can be characterized by three main components, they are: the gate (G), source (S) and drain (D). The gate of the MOS transistor is usually made of polysilicon, which has relatively good conductance. The source and drain of the transistor are formed by diffusion metal inside a substrate. The L and W parameters are the length and width of the conducting channel between the source and drain, respectively.

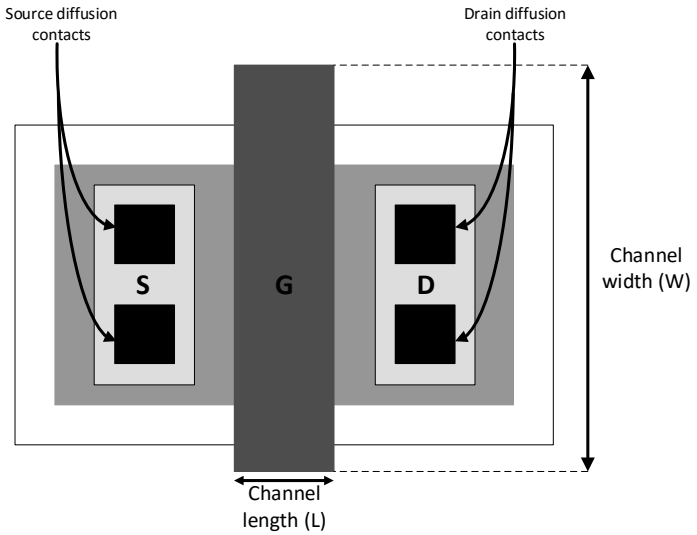


Figure B.1: Basic geometric top view of a CMOS transistor.

The cross-section view of the n-type MOS transistor (NMOS) and p-type MOS transistor (PMOS) is illustrated, respectively, in Figure B.2 and in Figure B.3. Both of them have the layer of the silicon dioxide, SiO_2, (also called oxide insulator) which has the purpose of insulating the gate from channel existing between the two diffusion areas. The t_{ox} parameter represents thickness of the oxide insulator layer. The fourth component is also represented: bulk (B), which usually is connected to a fixed voltage, i.e., the bulk of the NMOS is connected to the GND and in the PMOS case is connected to VDD.

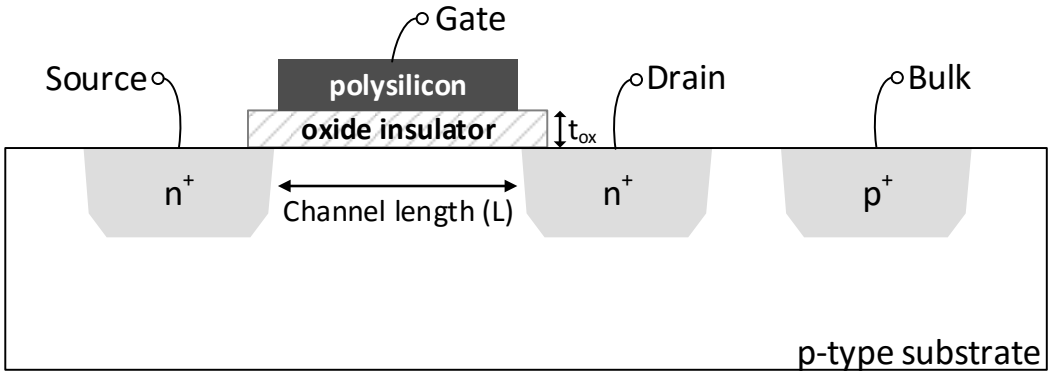


Figure B.2: An internal structure of an NMOS transistor.

The NMOS transistor is built on the p-type semiconductor substrate (p^-). The drain and source areas are built on n^+ diffusion regions, where + indicates the high degree of the silicon with donors. When applying voltage to the gate, the voltage drop between the gate and substrate leads to the forming of an n-type channel between the source and drain with electric field, which controls the flow of the carriers (electrons) in that channel.

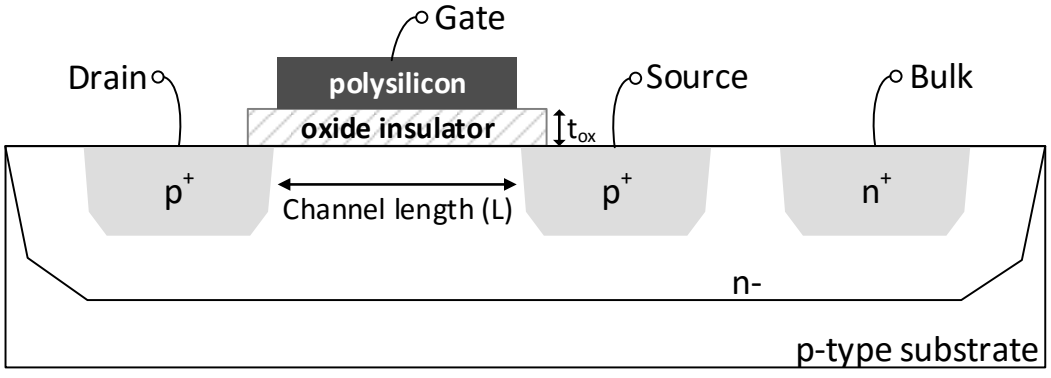


Figure B.3: An internal structure of an PMOS transistor.

The PMOS transistor has a complementary structure to the NMOS transistor. In this case, the PMOS transistor is built on the n-type layer (n^-), characterized as

the donor-doped silicon, which is placed firstly on the p-type substrate. Now the source and drain areas are built on p^+ diffusion regions. This type of transistor has the similar operation to the NMOS transistor, but with doping and voltages reversed, and the carriers in the channel are now positive holes.

In the Figure B.4 is shown the most commonly used symbols in order to represent the NMOS and PMOS transistors in terms of the circuit schematics.

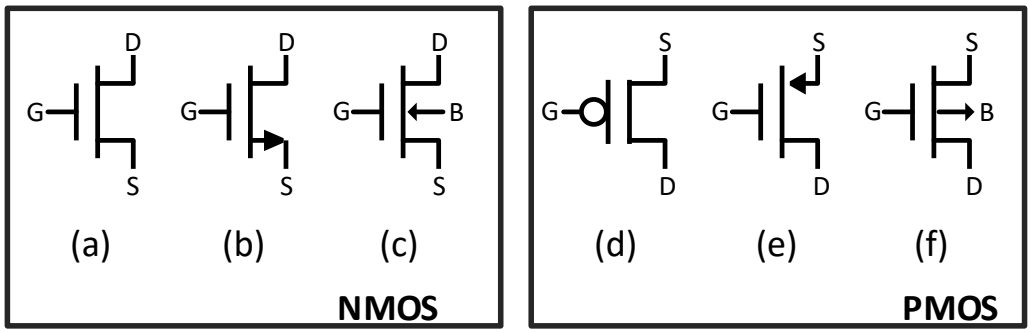


Figure B.4: Commonly used symbols for NMOS and PMOS transistors.

B.2 Basic operation of MOS transistors

The basic operation of MOS transistors will be described with respect to an NMOS transistor, but operation of the PMOS transistor is in all equivalent. As was seen above, depending on the voltage applied at the gate, the electric field is created if the gate voltage is positive (negative gate voltage for the PMOS transistors), hence the transference of current between drain and source may occur. Thus, there are two big voltage dependencies on how and how much current is transferred between drain and source, they are: v_{GS} (gate to source voltage) and v_{DS} (drain to source voltage).

Let assume a simple circuit represented in Figure B.5 to analyse the current behaviour that passes trough the transistor, I_D, where the source and bulk are connected to ground and drain is $V_D > 0$. Now, if analysing the variation of the gate voltage there are three distinct regions, which are represented at the right side of the Figure B.5 and are described in the following topics.

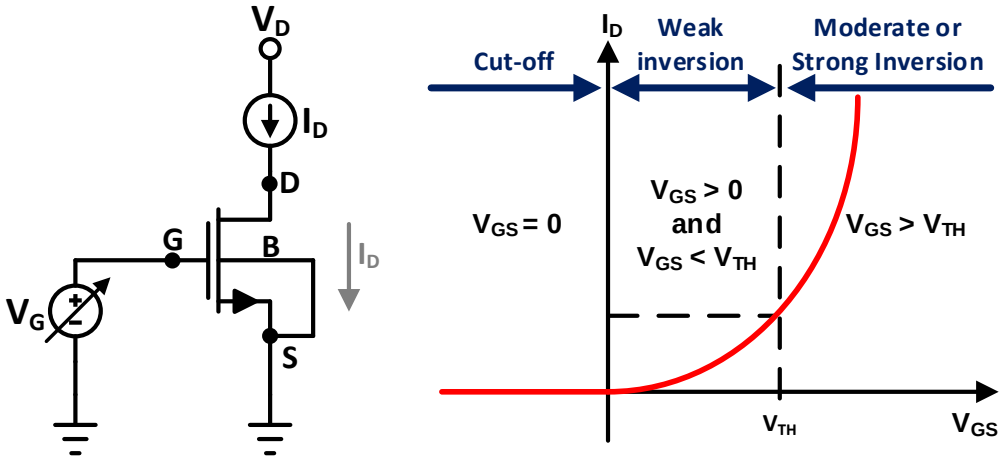


Figure B.5: Basic NMOS circuit (left) and I_D versus V_{GS} with respective representation of the operating regions (right).

1. **Cut-off region:** $V_G < 0$

   If negative gate voltage is applied, positive charge will be attracted to the channel region. Hence, channel accumulation occurs, as the substrate was originally doped, this negative gate voltage has the effect of simply increasing the channel doping to p^+. So no current will flow from the source to drain, except for leakage current, even if one of the source or drain voltages becomes large. Also a depletion zone (region free of holes) will form at the source-substrate, drain–substrate junctions, as represented in Figure B.6.

$$I_D = 0. \tag{B.1}$$

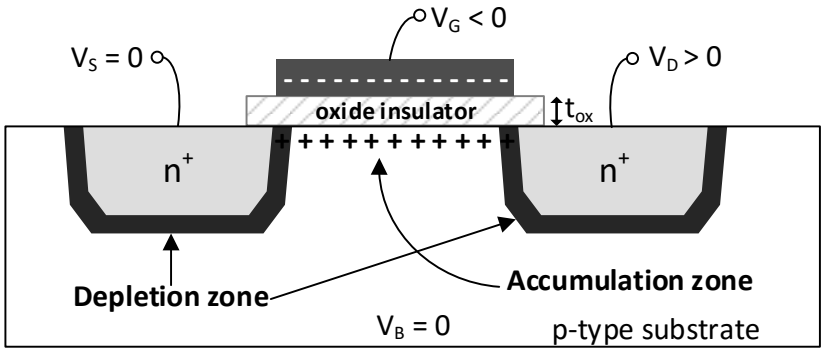


Figure B.6: Cross-view of an NMOS transistor in cut-off region.

2. **Weak inversion region:** $0 < V_G < V_{TH}$

   When the gate voltage is gradually increased with positive voltage, but below the threshold voltage (V_{TH}), the holes under the gate are repelled to

produce a depletion region, and it becomes continuous under the gate from source to drain, as shown in Figure B.7. The transistor threshold voltage, V_{TH}, defines the gate-source voltage for which the concentration of electrons under the gate is equal to the concentration of holes in the p^- substrate far from the gate, or by other words, it is a minimum gate voltage at which a MOS transistor begins to conduct. Even so, in this region there are still, but very small, current passage, which can be calculated by [46]

$$I_D = I_{D0}\, e^{V_{GS}/(nV_T)} \left(e^{-V_S/V_T} - e^{-V_D/V_T} \right), \tag{B.2}$$

where V_T is thermal voltage

$$V_T = \frac{kT}{q} \approx 25\ mV \ \ at\ T = 300\ K\ (\simeq 25^oC), \tag{B.3}$$

n is slope factor

$$n = \frac{C_{ox} + C_{depl}}{C_{ox}}, \tag{B.4}$$

with C_{ox} meaning oxide capacitance per unit area and C_{depl} meaning depletion capacitance per unit area, and, finally, I_{D0} is process-dependant constant, which ranges from 10^{-15} A to 10^{-12} A [47].

Having that all in account, the I_D has not null value only if there are significant voltage difference between drain and source terminals, otherwise and mostly, the current is considered as

$$I_D = \approx 0. \tag{B.5}$$

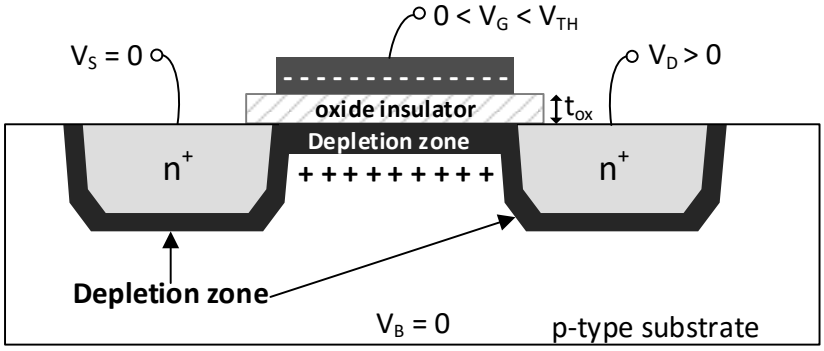


Figure B.7: Cross-view of an NMOS transistor in weak inversion region.

3. **Moderate or strong inversion region:** $V_G > V_{TH}$

   As a more positive gate voltage is applied, in this case with $V_G > V_{TH}$, the gate attracts carriers (negative charge) that were situated in the p^- substrate, in a way that the channel beneath the gate becomes an n region. This process is called inversion. The number of electrons that reach the channel under the gate depends on the voltage difference $V_{GS} - V_{TH}$. Hence a conducting channel is produced because of this transverse electric field.

   Now, as the channel is established, as can be visualized in Figure B.8, let assume a fixed value for the V_G and analyse the effect that the drain voltage variation has on the current I_D. Thus, this region can be further subdivided into three subregions. The current relation with the voltage V_{DS} and those subregions are illustrated in Figure B.9

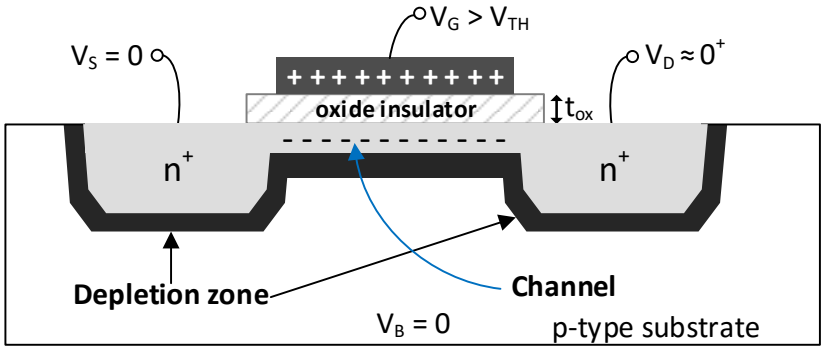


Figure B.8: Cross-view of an NMOS transistor in moderate inversion region.

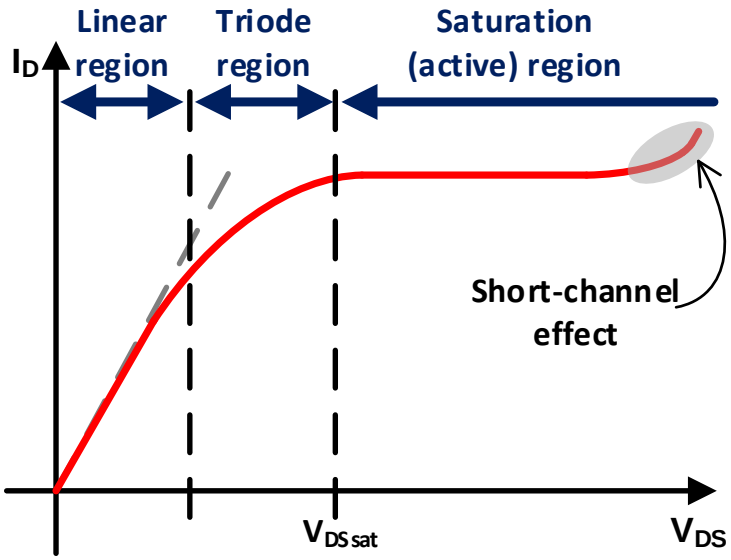


Figure B.9: I_D versus V_{DS} for fixed V_{GS} ($V_{GS} > V_{TH}$) with respective representation of the operating subregions.

a) **Linear region**: $V_{DS} \approx 0^+$

When the V_{DS} voltage is small, the current flow has linear relation with the V_{DS} and hence the reason of the name of this region. Actually, the channel region behaves like a resistor and implying the relation of the Ohm equation: $I_D = V_{DS}/R$, where R is the channel resistance. And this relationship is given by

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) \cdot V_{DS}, \tag{B.6}$$

$$R = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}, \tag{B.7}$$

where μ_n is the mobility of electrons near the silicon surface, the C_{ox} is oxide capacitance per unit area, as indicated previously, and the W and L defines the width and length of the channel, respectively. It should be noted that as the channel length increases, the drain current I_D decreases, whereas this current increases as the transistor width increases. The cross-view of the transistor that represents this situation is the same as in Figure B.8, where the channel is stable.

b) **Triode region**: $0^+ < V_{DS} < (V_{GS} - V_{TH})$

As the drain-source voltage increases, channel depth at the drain terminal decreases, as can be seen in Figure B.10. Therefore, the I_D current has no longer linear relation with V_{DS} voltage, but a quadratic function of that voltage, and is given by

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{V_{DS}^2}{2}\right]. \tag{B.8}$$

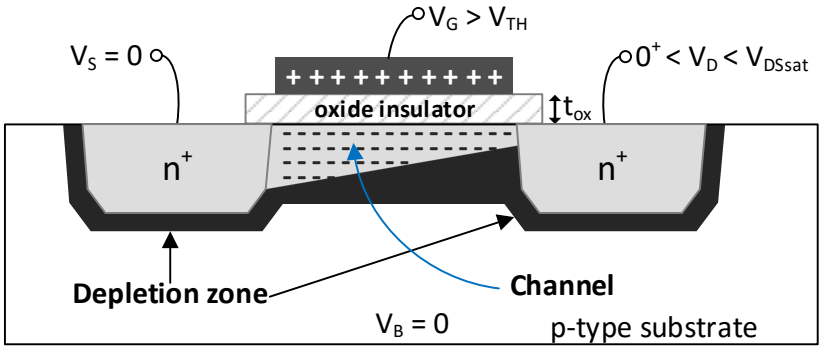


Figure B.10: Cross-view of an NMOS transistor in triode region.

That means that the increase of the I_D current slows down when the V_{DS} increases and that happens until the V_{DS} voltage reaches the V_{DSsat}

voltage (V_{DS} saturation voltage, also called as overdrive voltage). Once the V_{DS} voltage reaches V_{DSsat} value, the channel depth at drain end is reduced to zero. This definition is called as the pinch-off point, as represented in Figure B.11.

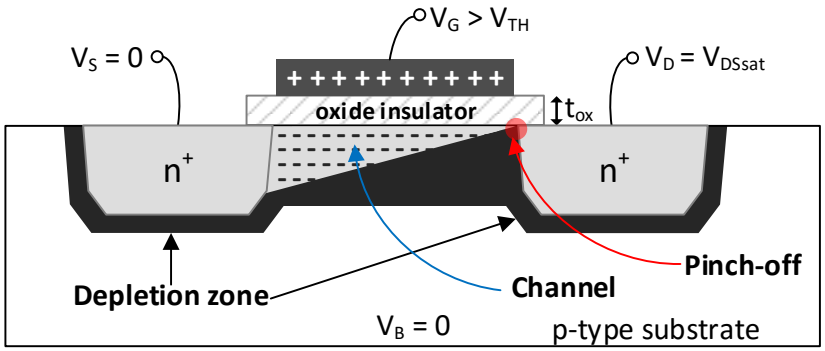


Figure B.11: Cross-view of an NMOS transistor when: $V_{GS} > V_{TH}$ and $V_{DS} = V_{DSsat}$. Pinch-off point.

c) **Saturation (active) region**: $V_{DS} > (V_{GS} - V_{TH})$

When the V_{DS} voltage exceeds the V_{DSsat} value (recalling that $V_{DSsat} = V_{GS} - V_{TH}$), the gate-to-channel voltage close to the drain is not enough to keep the channel formed. The depletion region adjacent to the drain is enlarged, interrupting the channel, as illustrated in Figure B.12. Consequently, the I_D current is saturated and no longer dependent of the V_{DS} voltage. Mobile channel carriers reach the drain through the depleted part of the channel due to the acceleration promoted by the existing electric field induced by the V_{DS} voltage. Having that, the current transference from source to drain is given by

$$I_D \cong I_{Dsat} \equiv \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2. \tag{B.9}$$

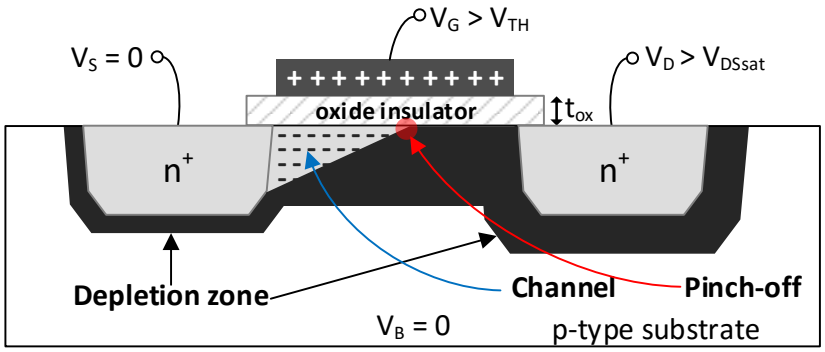


Figure B.12: Cross-view of an NMOS transistor in saturation region.

Indeed, the variation of the V_{DS} voltage has influence on the effective length of the channel. As already said, the increase of the V_{DS} voltage causes depletion region enlargement, reducing this way the effective length of the channel. This effect is generally represented by parameter λ and is called channel modulation constant. Because of these channel modulation effects, the I_D current increases a little with V_{DS}, which is more significant when short channels (minimum L) is used, as represented in Figure B.9. Thus, I_D current becomes dependent of the V_{DS} accordingly to

$$I_D \equiv \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda \cdot V_{DS}). \tag{B.10}$$

APPENDIX C

TOPOLOGIES OF THE CLASS-E POWER AMPLIFIER

Usually, the switch of the Class-E PA is implemented using a common-source configuration, i.e., the input signal is applied at the gate of the transistor and the output signal is read at the drain. However, some authors used other topologies in order further to reduce the power stress on the power transistor. Here are presented some implemented examples of different topologies of the Class-E PA, despite all of them consisting in a common-gate topology (input signal is applied at the source of the switching transistor).

C.1 Class-E Cascode Common-Gate Topology

C. Yoo and Q. Huang published an article entitled "A Common-Gate Switched 0.9-W Class-E Power Amplifier with 41% PAE in 0.25-μm CMOS", where they presented an implementation of the Class-E with common-gate topology in a standard 0.25-μm CMOS technology, as its title suggests. In fact, the Class-E PA is combined by a common-source stage and the common-gate switch into a cascode as shown in Figure C.1, where in the left part of the circuit is used a push–pull input stage operating in class-C mode. Their experimental results showed that the power amplifier can deliver 0.9-W output power to 50 Ω load at 900 MHz with 41% PAE from a 1.8-V supply.

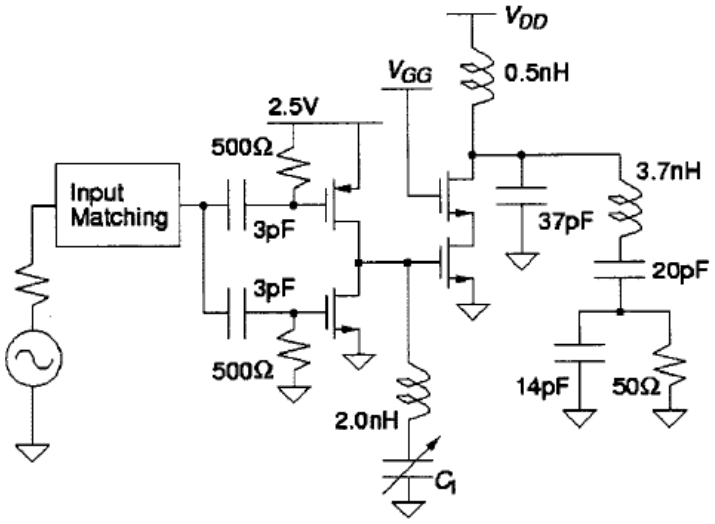


Figure C.1: Complete schematic of the common-gate switched Class-E power amplifier with finite dc-feed inductance, including both driver and output stage (adopted from [20]).

A. Mazzanti, L. Larcher and others published an article entitled "Analysis of Reliability and Power Efficiency in Cascode Class-E PAs". This article presents an implementation of the Class-E PA in a 0.13-μm CMOS technology, quite similar to the one presented above. Though, this one presents a simple Class-C mode driver and a circuit solution to minimize the effects of the discovered new dissipative mechanism, consisting of the L_p inductance and a blocking capacitor C_{BL} that was inserted between the inductor and ground, both of them together with the capacitive parasitic were tuned at the desired frequency of operation, as shown in Figure C.2. The simulation of this solution presented 67 % PAE while delivering 23 dBm peak power at 1.7 GHz from a 2.5-V supply.

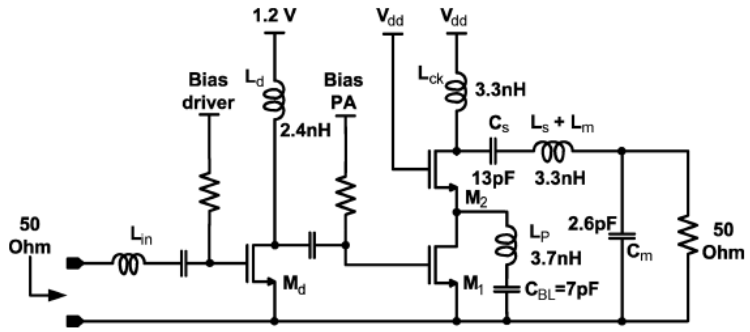


Figure C.2: Complete schematic of the proposed PA, including both driver and output stage (adopted from [23]).

C.2 Class-E Differential Topology

K.-W. Ho and H.C. Luong published an article entitled "A 1-V CMOS Power Amplifier for Bluetooth Applications", where the proposed power amplifier consists of a pre-amplifier with positive feedback configuration and a common-gate Class-E output stage, both in differential configuration, operating at 2.4 GHz and fabricated in a standard 0.35-μm CMOS technology.

Considering the single-ended configuration for the Class-E output stage, the authors studied the cascode common-gate topology, shown in Figure C.3 and already discussed in the previous section. However, they decided to improve it by replacing the cascode connection by the configuration shown in Figure C.4, where the input signal is directly applied to the source and this allows to overcome the voltage drop across the switch. The complete schematic of the proposed solution with differential configuration is presented in Figure C.5. This configuration (differential) not only allows the doubling of the output power, which relaxes the requirements of the optimum load by a factor of two, which in turn lowers the matching losses, but also the size of the transistors can be smaller, as the current flow through the transistor is reduced for the same supply voltage and same output power.

Thus, the proposed circuit, operating at 2.4 GHz, achieved an 18-dBm output power with 34 % PAE for a single 1-V supply voltage and 20-dBm output power with 35 % PAE for a 1.2-V supply voltage.

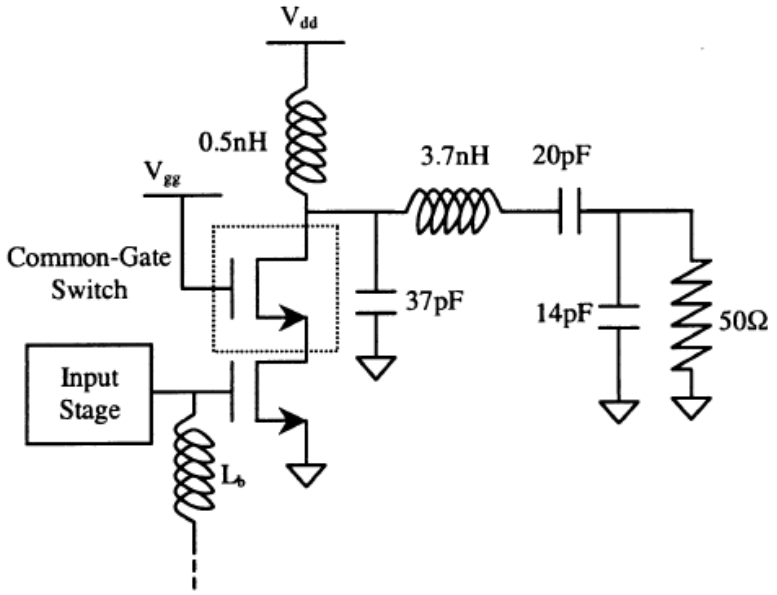


Figure C.3: Schematic of the published common-gate class-E power amplifier in single-ended configuration (adopted from [21]).

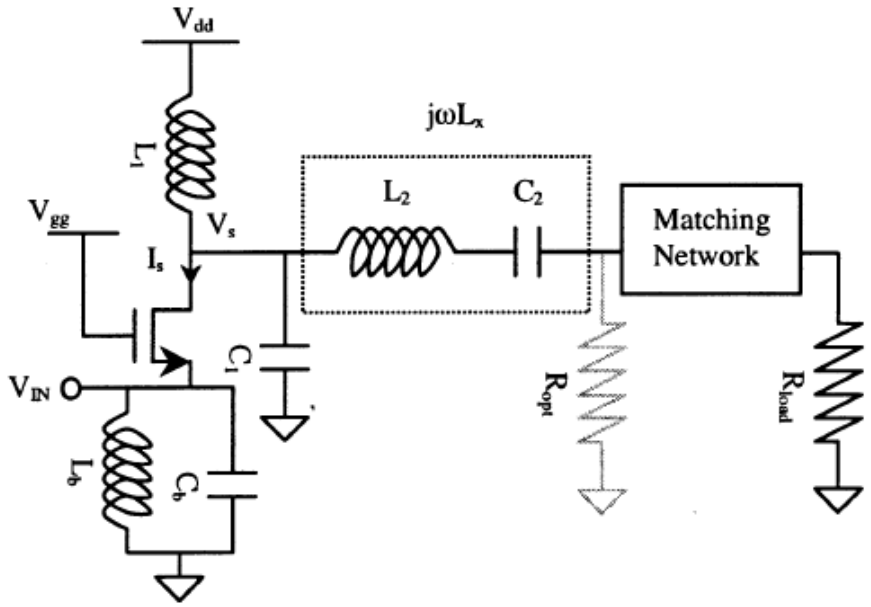


Figure C.4: Proposed common-gate class-E power amplifier in single-ended configuration (adopted from [21]).

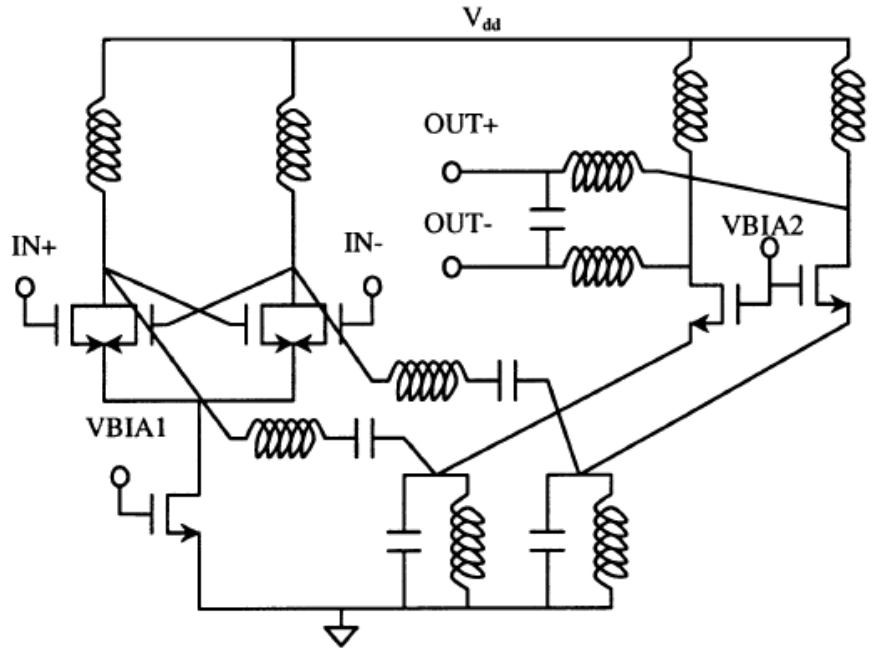


Figure C.5: Complete schematic of the proposed power amplifier (adopted from [21]).

J. Fritzin and A. Alvandpour published an article entitled "Low Voltage Class-E Power Amplifiers for DECT and Bluetooth in 130nm CMOS". Despite their article not showing the detailed circuit schematic, it presents the simplified schematic of the single-ended section of their solution, as shown in Figure C.6. However, they say it was implemented using a differential structure intended for DECT and Bluetooth application. Their results show that a DECT PA achieves an +26.4 dBm output power with 30 % PAE at 1.5-V supply voltage. In the other hand, the results for the Bluetooth PA show reliable operation at 1-V supply voltage, an output power of +22.7dBm with PAE of 36 %.

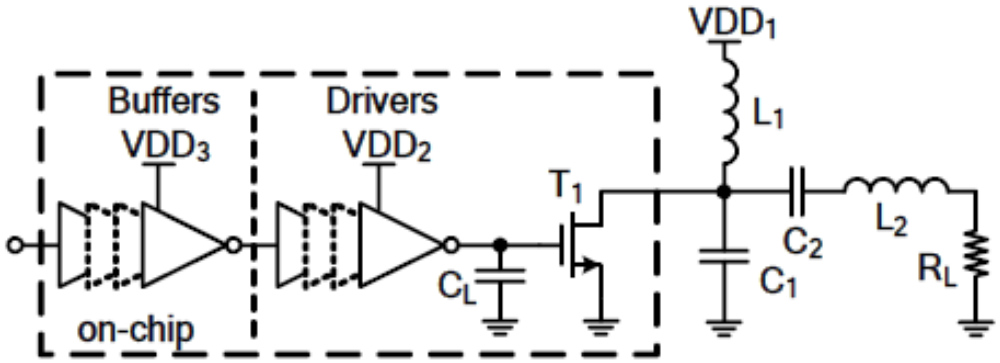


Figure C.6: Simplified schematic of the proposed PA, single-ended section(adopted from [22]).