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Non-Gyrator Type Active Inductors

Dissertação para obtenção do Grau de Mestre em Engenharia Electrotécnica e de Computadores

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“We grew up learning to cheer on the underdog because we see ourselves in them”- Shane Koyczan

Acknowledgments

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Resumo

Receptores modernos de rádio frequência (RF) permitiram um eficiente e significativo crescimento de aplicações em CMOS.

O requisito principal consiste em ter o sistema num só chip, de maneira a optimizar área e o custo. Para o efeito, é necessário o desenvolvimento de circuitos sem bobines, para os blocos-chave de um receptor RF. Osciladores RC, filtros passa-banda RF, e LNAs são exemplos destes blocos-chave. A presente dissertação introduz um "*inductorless wideband MOSFET-only RF Non-Gyrator Type of Active Inductors*" com reduzida área de consumo, baixo custo e reduzida potência de consumo, capaz de cobrir a gama de frequências de WMTS e ISM, para aplicações biomédicas.

O circuito proposto baseia-se num "floating capacitor" associado a duas fontes de corrente. A primeira fonte de corrente, controlada pela tensão de entrada, tem dois objectivos: fornecer corrente ao condensador (C_{gs2}) e desenvolver tensão deslocada 90º em relação à primeira corrente. Esta tensão tem a responsabilidade de controlar a segunda fonte de corrente. A introdução de um transístor no circuito existente permite compensar a parte activa, e a corrente vista pela tensão de entrada torna-se puramente indutiva.

Este modelo, baseado em bobines activas (AI) usa tecnologia MOS $130\,nm$, de maneira a optimizar o controlo do factor de qualidade. Neste sentido, as bobines activas desenvolvidas comportam-se como um oscilador RLC paralelo e são dados exemplos que suportam a oscilação do circuito para uma gama de frequências entre 662 MHz e 4.1 GHz. Uma fonte de tensão de 1.2 V fornece 56.4 μW ao circuito à máxima frequência de oscilação. Com os resultados obtidos, é possível confirmar os objectivos propostos, de maneira a ter bobines activas operacionais como um bloco chave em *RF transceiver*.

Palavras-chave: Bobines activas, CMOS, Filtro, Factor de Qualidade, Oscilador RLC, Ruído de fase.

Abstract

Modern CMOS radio frequency (RF) Receivers have enabled efficient and increasing applications. The main requirement is to have system in a single chip, in order to minimize area and cost. For the purpose it is required the development of inductorless circuits for the key blocks of an RF receiver. Examples of this key blocks are RC oscillators, RF band pass filters, and Low Noise Amplifiers. The present dissertation presents an inductorless wideband MOSFET-only RF Non-Gyrator Type of Active Inductors with low area, low cost, and very low power, capable of covering the whole WMTS, and ISM, band and intended for biomedical applications.

The proposed circuit is based on a floating capacitor connected between two controlled current sources. The first current source, which is controlled by the circuit input voltage, has two objectives: supply current to the capacitor (C_{gs2}) and develop a voltage with 90º degrees in regard to the first current. The capacitor controls the second current source. The addition of one transistor compensates the capacitive parcel of the input current, in order to become purely inductive.

This model, based on Active Inductors (AI) takes advantage of the $130\,nm$ MOS technology to optimize the control of the quality factor. In this sense, the proposed AIs can behave as a parallel RLC Oscillator, and examples of realizations for 662 MHz to 4.1 GHz range are given. A 1.2 V power source, supply the circuit with 56.4 μW at the maximum oscillation frequency. With this results, it is possible to confirm the proposed objectives, in order to have a functional Active Inductor as a key block in RF transceivers.

Keywords: Active Inductors, CMOS, Filter, Quality Factor, RLC Oscillator, Phase Noise.

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Abbreviations

AI	**A**ctive **I**nductor
CD	**C**ommon **D**rain
CG	**C**ommon **G**ate
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CS	**C**ommon **S**ource
DC	**D**irect **C**urrent
IF	**I**ntermediate **F**requency
LO	**L**ocal **O**scillator
NMOS	**N**channel **M**etal-**O**xide-**S**emiconductor
RF	**R**adio **F**requency

Chapter 1. Introduction

1.1 Background and Motivation

Modern CMOS RF Receivers have enabled efficient and increasing applications. The main requirement is to have “system-on-a-chip” (SOC), in order to minimize area and cost. For the purpose it is required the development of inductorless circuits for the key blocks of an RF receiver.

CMOS active inductors are active networks that consist essentially of MOS transistors. Sometimes, resistors are used as feedback elements to improve the performance of active inductors. According to certain dc biasing conditions, the aforementioned networks exhibit an inductive characteristic in a given frequency range. In this thesis we will present a detailed study about CMOS active inductors and describe their advantages in area and cost in comparison with traditional passive inductors [Yua, 2008; Than, 2000].

Active inductors have some attractive advantages: low silicon area, large and tunable inductance, large and tunable quality factor, large and tunable self-resonant frequency and small chip area.

In fact, it is fair to say that CMOS active inductors have found increasing applications in areas where an inductive characteristic is not only useful but also necessary. There are many possible applications for active inductors: LC and ring oscillators, RF bandpass filters, limiting amplifiers for optical communications and low-noise amplifiers. In this work we try to solve the main problem of active inductors, which is their typical low quality factor [Yua, 2008; Wu, 2003].

From a motivational standpoint, it is remarkable not only the capability that the proposed AIs have in improving the control of the inductance Q-factor, but also the fact that because of their wide tuning ability, a filter can assume an oscillatory behavior, similar of an parallel RLC-circuit [Dun, 1997; Rej, 2010].

A circuit prototype designed in 130 nm standard CMOS technology validate the proposed approach, in which obtain a Q of 235.8 and operating range of 4.1 GHz, with a power consumption of 56.4 μW.

1.2 Main Contributions

In terms of main contributions of the present dissertation, it presents an inductorless wideband MOSFET-only RF Non-Gyrator Type of Active Inductors with low area, low cost, and very low power, capable of covering the whole WMTS and ISM band and intended for biomedical applications.

The model, based on Active Inductors, takes advantage of the $130\,nm$ MOS technology to optimize the control of the quality factor.

Additionally, it is fair to mention that the proposed circuit behaves as a RF oscillator with very low power at the maximum oscillation frequency.

1.3 Thesis Organization

In addition to the introductory chapter this thesis is organized with five more chapters as follows:

Chapter 2 – Receiver Architectures and RF blocks.

This second chapter covers and provides sufficient considerations on devices, processes, issues and techniques applied to circuit design in modern wireless receiver RF front-ends and respective building blocks implemented with integrable CMOS technology.

The primary idea is to emphasize the theoretical bases and to uncover the initial process of development related to the present project.

Given that CMOS technology is used for implementation, some of the structures, concepts and parameters of performance that offer relevance are also showed.

Chapter 3 – CMOS Active Inductors.

This chapter has the responsibility to carry out a brief survey of the most important theoretical basis on active inductors. Specifically, are presented not only the most important advantages that CMOS active inductors offer, but also principles of Gyrator-C active inductors and its characterization.

In addition to these considerations, this chapter introduces the proposed circuit and its most relevant equations.

Chapter 4 – Prototype Design and Simulation Results.

Given that the simulation process of this thesis is essentially a result of successive sizing, that is, each simulation involved the redefinition of the size of transistors and the value of a particular current source, it was decided to include both in the same chapter.

In this sense, the sizing related to the first circuit, or in other words, the circuit without the contribution of transistor M_3 are presented.

Figures with simulations done for Q-factors as well as simulations results for the oscillator are presented.

Chapter 5 – Oscillator Design.

In the present chapter, strategies that allowed the circuit to oscillate, the frequency of oscillation, the power consumption and the value of phase noise are discussed.

Chapter 6 – Conclusions and future works.

In this chapter, the most important conclusions of this thesis, that is, the results and corresponding validity and relevance are discussed.

The faced problems as well some adjustments and optimization guidelines are also addressed. Future research directions are also advised for further studies.

Chapter 2. Receiver Architectures and RF Blocks

The primary objective of the present chapter is to provide background and support for the analysis and design of Radio Frequency circuits.

In this sense, it will offer a brief theoretical overview of the fundamental aspects required for the understanding of this thesis, specially taking into account an implementation in CMOS technology.

Some common receiver architectures and common RF concepts will be presented, as well as simple topologies used in CMOS design.

2.1 Receiver Architectures

In every wireless system, the open space is used as the propagation channel and the message is sent over a RF modulated signal.

The motive behind the use of high frequencies is related to the fact that at high frequencies there is higher bandwidth.

Additionally, in some cases the use of higher frequencies is also imposed by the characteristics of the antenna.

Regardless this fact, many relevant issues occur when using this type of transmission, due to the fact that open space is a communication path that cannot be corrected neither controlled.

While traveling, the transmitted signal suffers from significant attenuation and reaches the receiver as a low power signal.

It is important to say that the receiver antenna captures much more than the desired signal, which implicates that there is the problem of the arising of noise and interfering signals at the reception.

This is the reason why designing a receiver is not an easy task: apart from the inherent physical and performance constraints of the hardware, it is mandatory to deal with noisy and weak input signals.

The RF front-end is the RF interface with the transmission channel and has as key blocks the LNA, the LO and the Mixer.

Careful design is required since the front end is responsible to downconvert a low power input signal, or in other words, it has to ensure a high gain at the desired frequency.

It is then one of the key blocks since is also responsible to loose up the performance requirements of the receiver's remaining blocks.

A few commonly used receiver topologies are considered, which differ in the type and number of frequency translations that are realized.

2.1.1 Heterodyne Receiver

The Heterodyne, also known as IF receiver, is one of the most used receiver architectures in wireless communication systems. Figure 2.1 [Cro, 1997] shows the aforementioned receiver architecture.

The down-conversion is realized in two steps.

In the first step, the input signal translated to the IF band, that is fixed. Another translation brings the signal to baseband. The system has a first block responsible to choose the target band, then the input RF signal is amplified by a LNA and translated, as previously mentioned.

This is the result of a multiplication by a sinusoid, which is provided by the LO and yields two replicas of the input signal (images) and is performed by a mixer.

Then an image reject filter removes all the unwanted image signals.

Subsequently, the RF signal is again down-converted to the baseband. The mixer output is filtered, by a specific channel selection filter, that isolates the signal of interest (IF signal) from other signals in adjacent channels.

It is important to say that the signal can be down-converted to baseband, which requires perfect LO quadrature signals (I/Q balance).

Considering the circumstance that the signal is actually on baseband it has just an elementary low pass filter.

And last but not least, has an ADC responsible to prepare the signal to be demodulated in the digital domain [Raz, 1998].

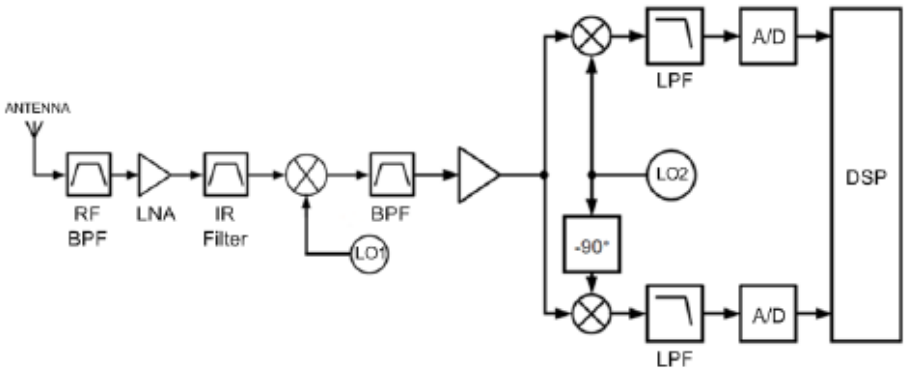

Figure 2.1- Heterodyne Receiver.

The channel filtering leads to precise selection, in other words it must be designed with a high quality factor.

This requirement is impossible to realize On-Chip because high performance filters are extremely challenging to be made in CMOS technology.

In this sense, it has to be realized OFF-Chip.

There is another fundamental matter in this architecture that has to be discussed: the signal is not directly transmitted to baseband and frequency overlap can occur due to the presence of the images that can corrupt the desired band.

Figure 2.2 illustrates the image problem related to the Heterodyne Receiver.

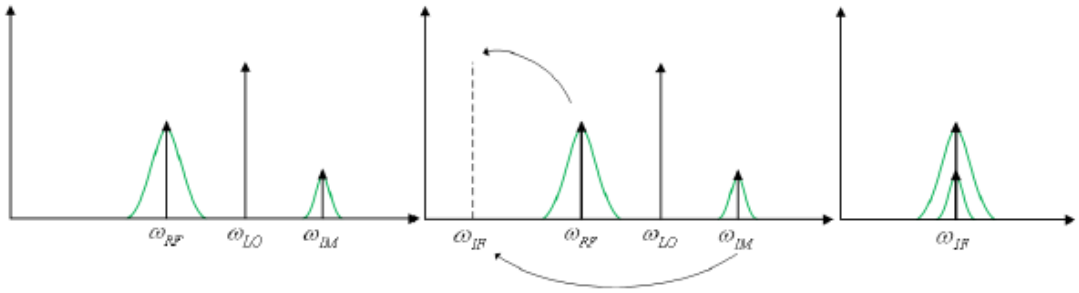

Figure 2.2- Image problem in Heterodyne Receiver.

Considering that the input of the system is a RF modulated signal, it is possible to identify two bands: image is the band signal that is as distant to the LO frequency as the RF signal (the RF and IM signal are $2\omega_{IF}$ apart from each other).

In fact, with an image rejection filter this signal is not completely clear and it will still be present, at the mixer input along with the signal of interest.

Considering only the mixing effect on the image signal, the output can be expressed by equation (2.1).

$$y(t) = \frac{V_{IM}.V_{LO}}{2}\cos\big((\omega_{Im} - \omega_{LO})t\big) + \frac{V_{IM}.V_{LO}}{2}\cos\big((\omega_{Im} + \omega_{LO})t\big) \qquad (2.1)$$

Considering the relation $\omega_{Im} = 2\omega_{LO} - \omega_{RF}$, the equation (2.1) can be re-written:

$$y(t) = \frac{V_{IM}.V_{LO}}{2}\cos\big((\omega_{LO} - \omega_{RF})t\big) + \frac{V_{IM}.V_{LO}}{2}\cos\big((3\omega_{LO} + \omega_{RF})t\big) \qquad (2.2)$$

One can see that one of the components coincides with the IF frequency, overlapping the desired signal, which implicates that the IF band must be thoroughly selected to prevent this constraint.

In retrospective, it can be said that the heterodyne receiver was developed to enable reception from numerous broadcasters.

Indeed, it works with several IF frequencies.

2.1.2 Homodyne Receiver

The Homodyne receiver depicted in Figure 2.3 [Ort, 2011] also known as Zero-IF receiver, directly translates to the baseband the input signal.

The aforementioned translation leads to a more elementary architecture and allows the possibility of complete integration given the fact that it does not imply high quality filters (such as the image rejection filter).

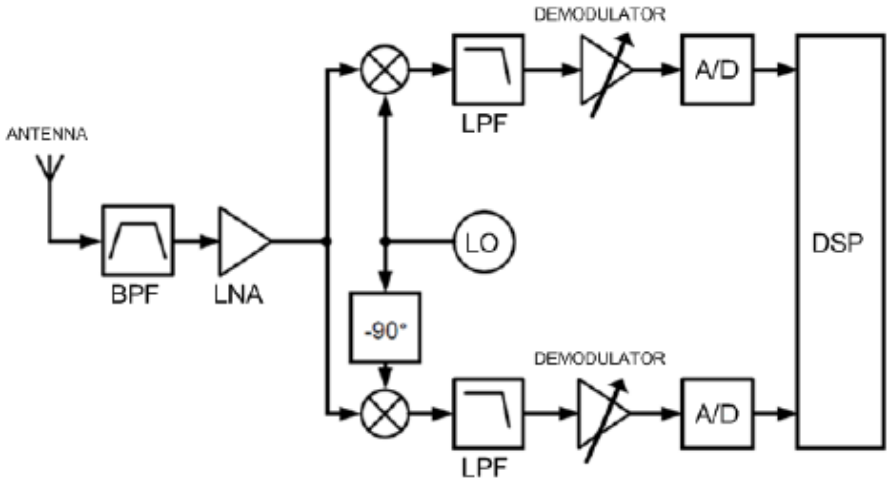

Figure 2.3- Quadrature Homodyne Receiver.

Nevertheless, because the signal is shifted to baseband, it is affected by flicker noise that is a low frequency noise, caused by active devices.

Moreover, it should be noted that this particular receiver does not guarantee perfect isolation between its blocks and as a consequence, oscillator leakage can occur.

The leakage is the result of ground problems and capacitive coupling, and can originate unwanted DC components, which eventually result in receiving process corruption.

2.1.3 Low IF Receivers

It was mentioned before that the homodyne receiver allows the possibility of full integration.

In terms of performance and flexibility, it is fair to say that the heterodyne receiver is better. Regardless this aspect, it requires external elements, so it does not allow complete integration.

In this sense, a new architecture, commonly known as Low IF receiver, arises from combining both receivers, ideally joining some important advantages of each receiver previously presented.

A mixed approach is used: basically the approach consists in using the homodyne receiver but instead of doing a direct conversion to baseband, the signal is shifted to allow intermediate frequency.

Thus, the baseband constraints are avoided. Regardless this consideration, it is still mandatory to overcome the image problem.

Since the main objective is to develop a receiver that allows fully integration instead of using a rejection filter to deal with the image signal, two extremely important image rejection techniques are used: the Hartley and Weaver architectures.

The idea is to process the signal after the low pass filter and combine both outputs into a single output.

This leads the image to be suppressed through its negative replica.

First, it will be explained and analyzed the Hartley architecture principle of functioning, detailed in Figure 2.4 [Ort, 2011].

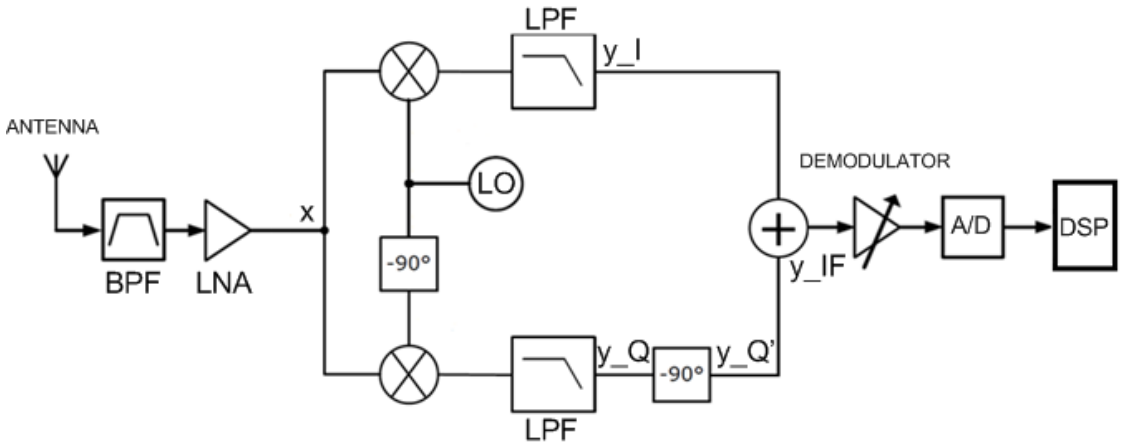

Figure 2.4- Low IF Receiver with Hartley Image rejection Architecture.

Considering the following input

.

$$x(t) = V_{RF}\cos(\omega_{RF}t) + V_{Im}\cos(\omega_{Im}t) \quad (2.3)$$

After low pass filtering

$$y_I(t) = \frac{V_{RF}V_{LO}}{2}\cos\big((\omega_{LO} - \omega_{RF})t\big) + \frac{V_{Im}V_{LO}}{2}\cos\big((\omega_{Im} - \omega_{LO})t\big) \quad (2.4)$$
$$y_Q(t) = \frac{V_{RF}V_{LO}}{2}\sin\big((\omega_{LO} - \omega_{RF})t\big) + \frac{V_{Im}V_{LO}}{2}\sin\big((\omega_{Im} - \omega_{LO})t\big)$$

Because a phase shift of -90 is realized on the quadrature signal $y_Q(t)$

$$y_Q(t) = \frac{V_{RF}V_{LO}}{2}\cos\big((\omega_{RF} - \omega_{LO})t\big) + \frac{V_{Im}V_{LO}}{2}\cos\big((\omega_{LO} - \omega_{Im})t\big) \quad (2.5)$$

Finally, when the two signals, $y_{IF}(t)$ and $y_Q(t)$, are summed the image is suppressed

$$y_{IF}(t) = V_{RF}V_{LO}\cos((\omega_{RF} - \omega_{LO})\mathrm{t}) \quad (2.6)$$

The Weaver architecture is similar but is used a second mixer stage at the frequencyω_{IF}.

Both solutions are dependent on the accuracy of the oscillators in terms of producing quadrature signals (phase and gain imbalances occur).

Regardless this fact, those deviations are far more noticeable in the Weaver approach because of the second mixer previously discussed since it introduces more phase deviations.

Figure 2.5 [Ort, 2011] presents a Low IF Receiver with Weaver Image Rejection.

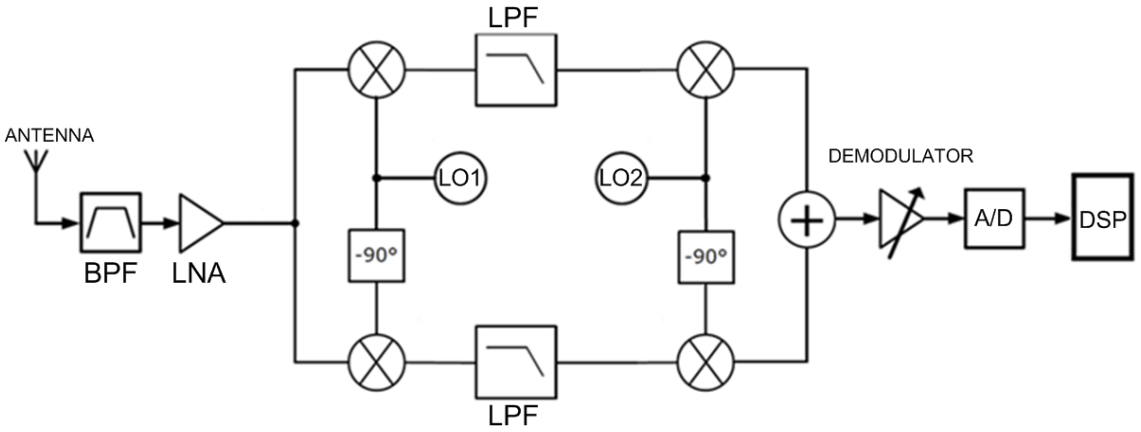

Figure 2.5- Low IF Receiver with Weaver Image Rejection.

2.2 CMOS Implementation Basic Concepts

2.2.1 Gain

In electronics the gain is one of the most important parameter of an amplifier.

Specifically, the gain quantifies the ability of a given system to increase or decrease the amplitude of an input signal and it is determined as the ratio between the output and the input signal.

It is considered that a system has amplification when it presents a gain greater than one, and attenuation when it has a gain equal or less than one.

In the field of electronics two types of gain are normally considered (usually expressed in dB) and they are both expressed by equations (2.7) and (2.8).

$$Power\ Gain = 10log\left(\frac{P_{out}}{P_{in}}\right) \quad (2.7)$$

$$Voltage\ Gain = 20log\left(\frac{V_{out}}{V_{in}}\right) \quad (2.8)$$

The base element of a CMOS circuit is the MOSFET transistor.

It can assume different behaviors according to its operation region as shown in Figure 2.6, which is defined by the biasing voltages.

Considering the saturation region the drain current produced by the transistor is approximated given by Equation (2.9):

$$I_D = k_{p/n}\frac{1}{2}\frac{W}{L}\left(V_{gs} - V_{th}^2\right) \quad (2.9)$$

where k is the mobility constant and it is a technology parameter (k_p refers to PMOS transistors and k_n refers to NMOS transistors), W is the width of the transistor, L is the length of the transistor, V_{gs} is the gate-to-source voltage drop and V_{th} is the threshold voltage (transistor operating voltage).

In this region the drain current is weakly dependent upon drain voltage and it is controlled essentially by the gate-source voltage (considering small variations of the threshold voltage).

Figure 2.6 presents MOSFET N-Type model and Figure 2.7 illustrates MOSFET regions [Lop, 2010]

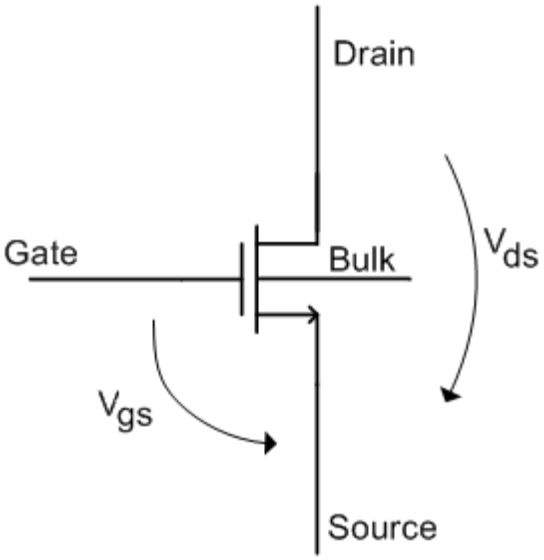

Figure 2.6- MOSFET N-type Model.

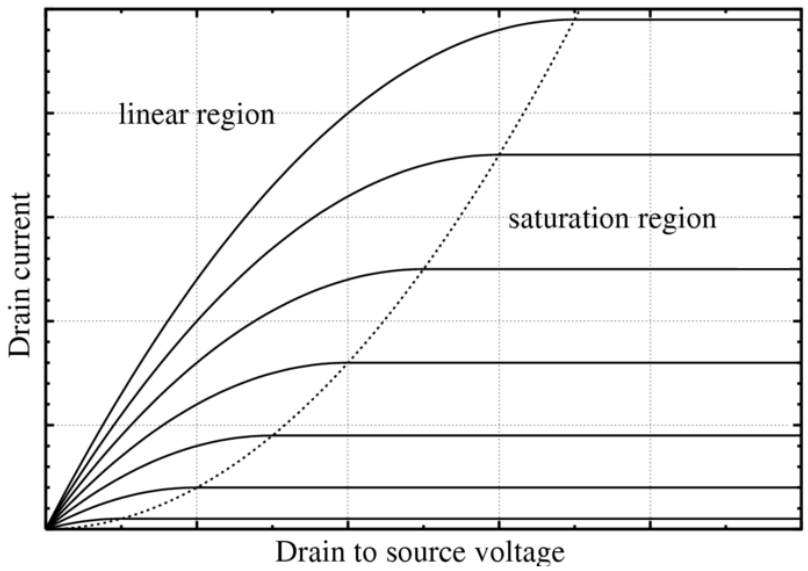

Figure 2.7- MOSFET regions.

Considering the facts aforementioned, it is possible to obtain the I-V characteristic of the transistor and define the MOSFET transconductance, given by Equation (2.10) which is a current gain and a key design parameter for a transistor [Lee, 2004].

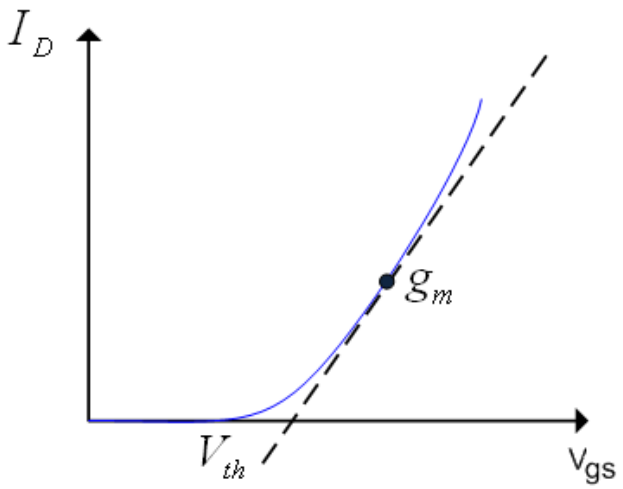

Figure 2.8- I-V curve and transconductance.

$$g_m = \frac{\delta I_D}{\delta V_{gs}} \tag{2.10}$$

It is also possible to calculate the general voltage gain if a load with resistance R_{out} is applied, expressed by Equation (2.11).

$$A = 20log(g_m R_{out}) \tag{2.11}$$

To prevent parasitic coupling, the bulk must be at the same voltage potential as the source in a NMOS transistor and the same voltage potential as the drain in a PMOS transistor.

Nevertheless, this is not always guaranteed. Considering the NMOS case (the development of the circuit related to this thesis, only required the use of NMOS transistors) the body effect describes how much the threshold voltage is affected by the change in the source-bulk voltage. This effect, expressed in a constant γ, is expected in differential pairs and diode connected NMOS [Lee, 2004].

The small signal linear model for the saturation region is showed in the figure 2.9.

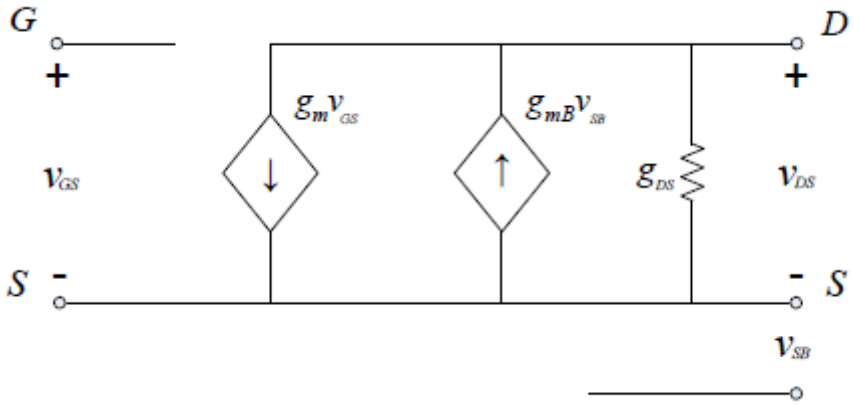

Figure 2.9- Body effect demonstrated using small signal analysis.

The Equation 2.12 relates the body effect and threshold voltage:

$$\Delta V_{th} = \gamma \left(\sqrt{2|\phi_p| + V_{sb}} - \sqrt{2|\phi_p|} \right) \tag{2.12}$$

ϕ_p is the surface potential parameter and V_{sb} is the source to bulk voltage.

This effect leads to the appearance of an extra transconductance term (Equation 2.13).

$$g_{mb} = -\frac{i_{ds}}{V_{sb}} = -\frac{\partial I_{ds}}{\partial V_{sb}} = -\frac{\partial I_{ds}}{\partial V_{th}} \frac{\partial V_{th}}{\partial V_{sb}}, \text{ with constant } V_{ds,}\, V_{gs} \tag{2.13}$$

$$g_{mb} = \frac{\gamma}{2\sqrt{2|\phi_p| + V_{sb}}} g_m = \frac{C_s}{C_{ox}} g_m = \eta g_m, \text{ with } 0.1 \leq \eta \leq 0.3$$

The aforementioned “extra” transconductance is related to the current consumption and is equivalent from 10 % up to 30 % of the g_m value.

Given the fact that the transconductance parameter is vital in CMOS design this effect must be taken into consideration for the best approaches, hence, for the best results.

Some considerations present not only in chapter three, but also in chapter four, will highlight the importance of this parameter.

2.2.2 Input Impedance

When conceiving complex structures as a RF receiver, some blocks are cascaded together.

Regardless, the connection between the blocks can be realized immediately. Typically, the output impedance of one block is different to the input impedance of the following one, which reflects back in the amount of power transferred between the devices [Ort, 2011].

In this sense, it is crucial not only to identify the input impedance of one device, but also how it can be adapted to maximize power transfer.

The input impedance is the one seen by the power source. It can be modeled by a Thevenin Equivalent.

Figure 2.10 presents an equivalent system input assuming reactive load.

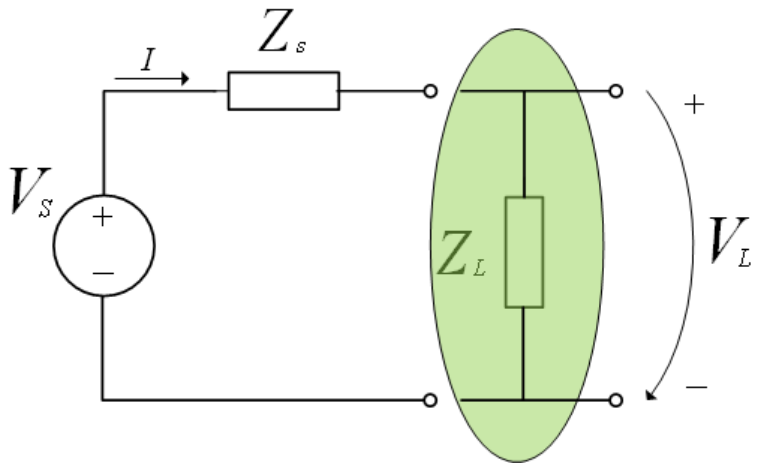

Figure 2.10- Equivalent system input assuming reactive load.

Briefly, V_S is the voltage supply source, Z_S is the source impedance and Z_L is the impedance of the load network.

Considering the classical Ohm's law, the current that flows through the circuit can be expressed by Equation 2.14.

$$|I| = \frac{|V_S|}{|Z_S + Z_L|} = \frac{|V_L|}{|Z_L|} \tag{2.14}$$

To obtain the condition that guarantees the maximization of power transfer it is mandatory to determine the power delivered to the load:

$$P = IR_L$$
$$= \frac{1}{2}|I|^2 R_L = \frac{1}{2}\left(\frac{|V_S|}{|Z_S+Z_L|}\right)^2 R_L \quad (2.15)$$
$$= \frac{1}{2}\frac{|V_S|^2 R_L}{(R_S+R_L)^2+(X_S+X_L)^2}$$

Synthetically, resistance R_S and reactance X_S are the real and imaginary parts of Z_S and the same considerations can be applied for the resistance R_L and reactance X_L but related to Z_L. The condition that maximizes the power transfer can be calculated by differentiating the above equation with respect to Z_L and equalize to zero:

$$\frac{\delta P}{\delta Z_L} = 0 <=> Z_S = -Z_L \quad (2.16)$$

According to Equation 2.16, load and source impedances should be complex conjugates of each other to guarantee the maximization of power transfer between the two systems.

Likewise, this is also relevant for the inter-connections receiver's RF blocks.

Not only input but also output impedance of each single block must be characterized for appropriate connection.

Often an impedance match must be realized to adapt the impedances.

Merely as an example, this is critical at the input of the LNA, since as previously studied on other subjects, the antenna has a characteristic impedance of 50 ohms and it captures a weak signal, the receiver must not lose power.

Because of this, the LNA has to be designed very thoroughly in order to match the antenna impedance.

Given the circumstances of dealing with CMOS technology, blocks present in its constitution, MOSFET transistors, which have typically a resistive or capacitive input.

It is also crucial to mention that capacitive match must be realized through the use of inductors which results sometimes in constraints in CMOS design mainly because of area consumption.

2.2.3 Quality Factor

The Quality Factor (Q) is the most common figure of merit for oscillators, and it is associated to the local oscillator phase-noise. Q is usually defined within the context of second order systems.

In fact, this particular figure of merit is extremely important to the realization of the proposed approach, because one of the fundamental goals of the present work, is to force the circuit to oscillate. And to realize this task, it is important to investigate the value of Q-factors (in this case, ideally, higher Q- factors).

Synthetically, there are three definitions of Q that gather consensus in the scientific community:

(1) The first definition is assumed considering a bandwidth calculated for -3 dB and a carrier frequency ω_0:

$$Q = \frac{\omega_0}{B} \tag{2.17}$$

This is applied to filters and oscillators characterized as second order resonant circuits.

Below is shown Figure 2.11 [Oli, 2008] that summarize Q-factor for a second order system.

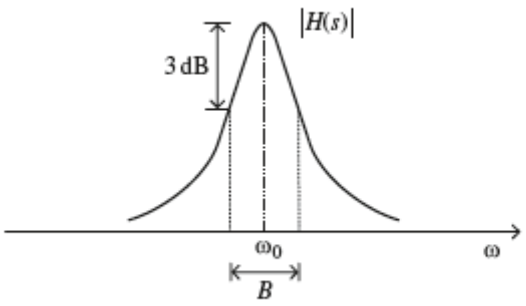

Figure 2.11- Q definition for a second order system.

Due to considerations previously studied it is known that the transfer function of a second order bandpass filter can be expressed as:

$$H(s) = \frac{K\frac{\omega_0}{Q}s}{s^2+\frac{\omega_0}{Q}s+{\omega_0}^2} \tag{2.18}$$

K is the mid-band gain and Q is the pole quality factor. For $Q \gg 1$ the transfer function is symmetric as shown in figure 2.11.

This definition of Q is reasonable for filters and can be used for oscillators.

However it is important to consider the resonator circuit as a second order filter.

(2) A second definition of Q, can be expressed through Equation 2.19, considers a given circuit and associates the maximum energy stored and the energy dissipated in a period.

(3)

$$Q = 2\pi \frac{Maximum\ energy\ stored\ in\ a\ period}{Energy\ dissipated\ in\ a\ period} \quad (2.19)$$

The Equation (2.19) is normally related to a common RLC circuit and associates the maximum energy stored (in C or L) and the energy dissipated (by R) in a period.

As a mere example, this second definition can be applied to an RLC series circuit.

The energy is stored in the inductor and in the capacitor, and the maximum energy stored in the inductor and the capacity is equal.

Correspondingly, the energy stored in an inductor (W_L) can be expressed as:

$$W_L = \int_0^T i(t)\, L \frac{di(t)}{dt} dt = LI_{rms}^2 \quad (2.20)$$

I_{rms} is the root-mean-square current in the inductor.

The energy dissipated in a resistor (W_R) per cycle (in the period T_0) is:

$$W_R = I_{rms}^2 R T_0 \quad (2.21)$$

Then, the value of Q-factor is:

$$Q = 2\pi \frac{LI_{rms}^2}{I_{rms}^2 R T_0} = 2\pi f_0 \frac{L}{R} = \frac{\omega_0 L}{R} \quad (2.22)$$

Likewise, it is also plausible to express the energy stored in the capacitor:

$$W_c = \int_0^T v(t)\, C \frac{dv(t)}{dt} dt = CV_{rms}^2 \quad (2.23)$$

In the Equation 2.23, V_{rms}^2 is the root-mean-square voltage in the capacitor, and $V_{rms} = \frac{I_{rms}}{(\omega_0 C)}$

In this sense, the value of Q is:

$$Q = 2\pi \frac{CV_{rms}^2}{I_{rms}^2 RT_0} = 2\pi f_0 \frac{\frac{CI_{rms}^2}{\omega_0{}^2 C^2}}{RI_{rms}^2} = \frac{1}{\omega_0 CR} \tag{2.24}$$

(4) In the third and final definition of Q the oscillator is taken as a feedback system and the phase of the open-loop transfer function $H(j\omega)$ is evaluated at the oscillation frequency, ω_{osc} and is not necessarily the resonance.

In a single RLC circuit the oscillation frequency is the resonance frequency, but with coupled oscillators the oscillation frequency may be distinct.

To clarify the third definition, the oscillator Q can be defined as:

$$Q = \frac{\omega_0}{2} \sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\theta}{d\omega}\right)^2} \tag{2.25}$$

Additionally, A is the amplitude and θ is the phase of $H(j\omega)$. This definition, called open loop Q considers the amplitude and phase fluctuations of the open-loop transfer function.

This Q definition is frequently related to a single resonator, and to demonstrate that Figure 2.12 is presented [Oli, 2008].

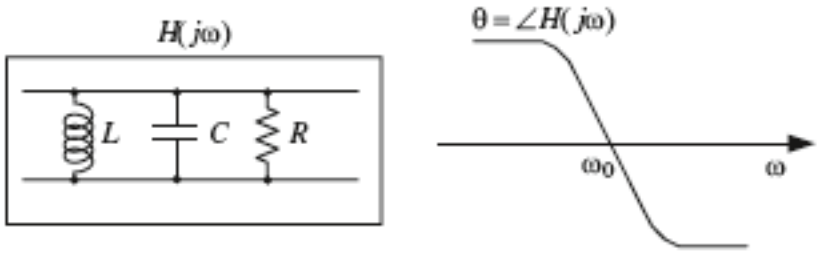

Figure 2.12- Definition of Q based on open-loop phase slope.

In fact, the last definition is an important “tool” to obtain the oscillator quality factor, which has its higher value at the resonance frequency.

2.3 Oscillators

Synthetically, it can be said that an oscillator converts a given DC level in pure sine-wave signal. It is of significant importance in terms of blocks in a receiver, because the quality of a down-conversion depends on the quality of the oscillator signals.

In terms of groups, it is possible to divide oscillators into two major groups: quasi-linear and strongly non-linear oscillators.

The second group, referred to strongly non-linear or relaxation oscillators, are typically performed by RC-active circuits.

The primary advantage of this group of oscillators lies in the fact that only resistors and capacitors are used together with the active devices.

In terms of disadvantages that relaxation oscillators present, the most obvious one, is their phase-noise value, which is high.

LC oscillators are normally quasi-linear oscillators. As resonator element, LC oscillators can use dielectric resonators, crystals, striplines, and LC tanks.

These oscillators are known by their good phase-noise performance, since Q is normally much higher than unity.

LC Oscillators

The LC oscillator, as shown in Figure 2.13, is a pure reactance feedback circuit.

Synthetically, the circuit presents a differential pair operating as a commutator. The aforementioned differential pair will be responsible to alternate the current conduction path through the feedback network thus producing an alternate signal.

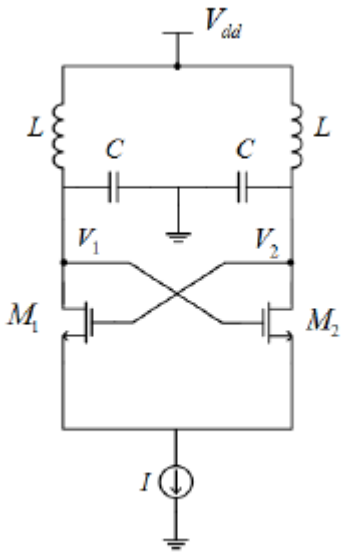

Figure 2.13- LC Oscillator.

Considering the fact that in a practical context the feedback network evidently present losses, the differential pair presents cross coupled outputs for compensation (thereby respecting the conditions relative to the Barkhausen criterion).

It is known that the small signal equivalent of the mentioned differential pair “imitates” a negative resistance. Indeed, the circuit can be modeled as Figure 2.14 shows.

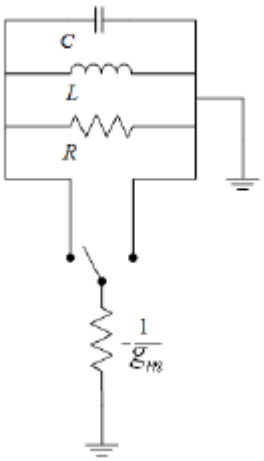

Figure 2.14- LC Oscillator Model.

Regardless the advantage of normally presenting a high quality factor value (current is exchanged between the capacitor and inductor), a low phase noise and a quasi-linear behavior, LC oscillators also present some disadvantages.

For instance, considering the fact that the feedback network parameters are fixed ($\omega_0 = \frac{1}{\sqrt{LC}}$), these oscillators have low frequency tuning capability.

Additionally, the integration in CMOS technology would definitely require large area consumption and this situation requires additional costs.

To conclude the considerations related to the LC oscillators drawbacks, it is fair to mention that modern receivers require quadrature outputs.

This type of oscillator, by itself, is not able to provide.

As a way to overcome the aforementioned constraint, it is possible to coupling an additional oscillator, but it will increase even more the area consumption and will contribute to the degradation of the frequency response because of the additional parasitic capacitances.

RC Oscillators

Literature shows that there has been a great interest in the last decade over the study and design of this type of oscillators.

If we establish a comparison in terms of area consumption between LC oscillators and RC oscillators, the second ones occupy far less area and they present other advantage: RC oscillators are highly integrable.

Regarding to structure and behavior, a RC oscillator is very similar to the one encountered in the LC oscillator.

In terms of quality factor, it is important to emphasize a difference in regard of the assumptions previously discussed about LC oscillators.

In RC Oscillators the feedback network is constituted by a capacitor and a resistor, which results in a lower Q factor.

This type of oscillator has the same differential pair that is responsible for the loss compensation and commutation behavior.

The capacitor is responsible to transform the DC current into voltage (Equation 2.26) and the resistor is used for biasing.

The Figure 2.15 shows a common RC oscillator, more precisely the relaxation Oscillator.

$$v(t) = \frac{1}{C}\int_{t_0}^{t} i(\tau)\, d\tau + v(t_0) \qquad (2.26)$$

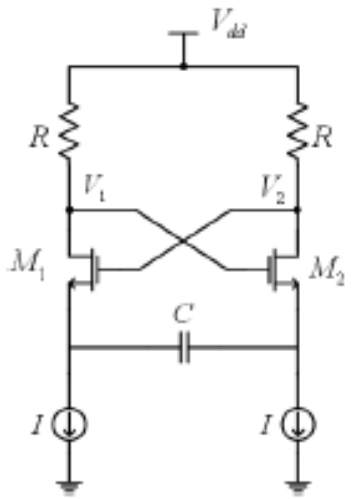

Figure 2.15- Relaxation oscillator.

It is known that the block diagram of a relaxation oscillator, can be modelled using an integrator and a Schmitt trigger [Oli, 2008].

The Schmitt- trigger is a memory element, and controls the sign of the integration constant.

Below, the oscillator waveforms are presented in Figure 2.16. It is important to mention that the square waveform is the Schmitt-trigger output, and the triangular waveform is the integrator output.

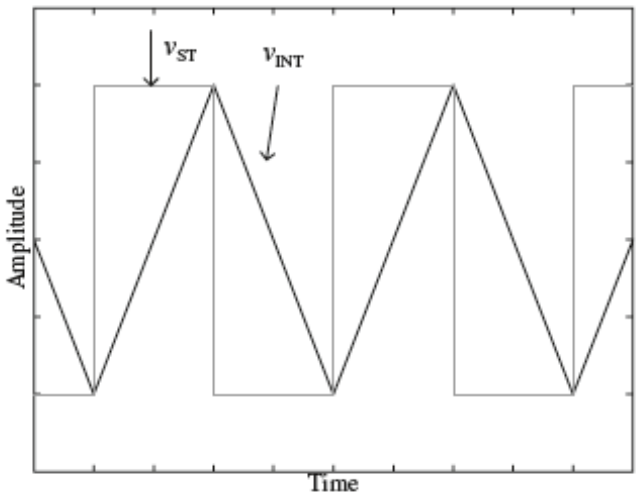

Figure 2.16- Relaxation oscillator: Oscillator waveforms.

To implement the oscillator at very high frequencies we need a circuit as simple as possible (Figure 2.15).

In this sense, we should replace the integrator and the Schmitt trigger by simple circuits that ensure some correspondence between the high level and the circuit level.

The integrator previously discussed is implemented simply by a capacitor (Figure 2.17).

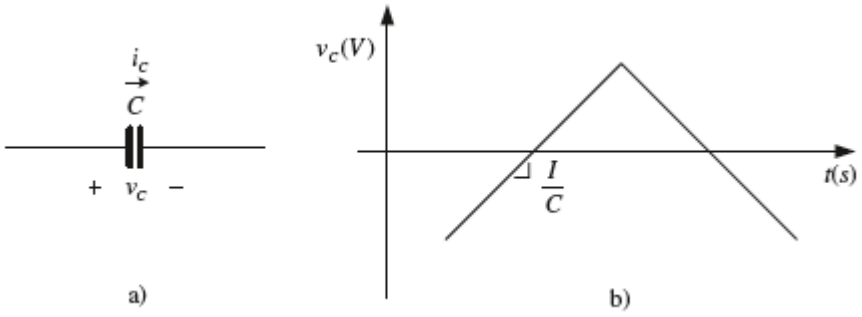

Figure 2.17- a) Integrator implementation. b) Integrator waveforms.

Its input is the capacitor current (i_C) and the output is the capacitor voltage (v_C).

This voltage is the input of the Schmitt-trigger (Figure 2.18), the output of which is i_C. The transfer characteristic of the aforementioned Schmitt-trigger is shown in Figure 2.18b.

It is important to mention that it is assumed that the switching occurs abruptly when the sign of $v_{BE1} - v_{BE2}$ changes.

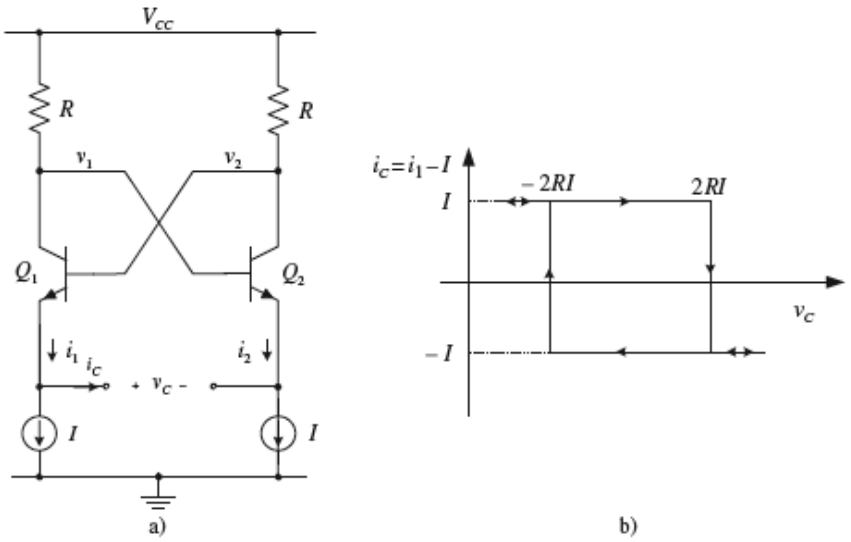

Figure 2.18- Schmitt- trigger: a) Circuit implementation. b) Transfer characteristics.

Regardless the fact that in terms of the model related to the Figure 2.16 the Schmitt-trigger output is i_C, it is important to use as the oscillator output the voltage $v_{OUT} = v_1 - v_2$, with an amplitude of 4*IR*, as shown in Figure 2.19.

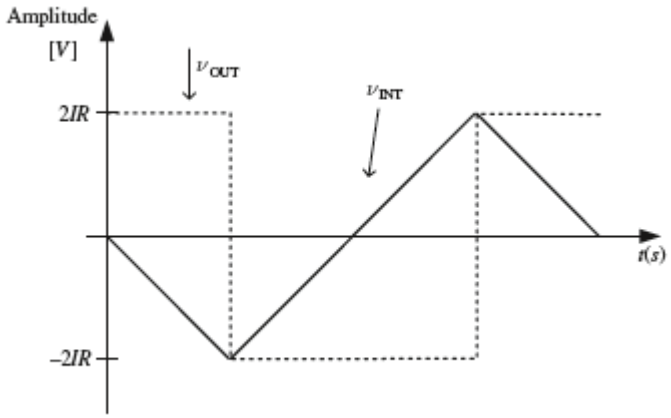

Figure 2.19- Relaxation oscillator waveforms.

At very high frequencies the outputs are approximately sinusoidal with an amplitude lower than 4*IR*. A circuit with MOS transistors has the exact performance as described above.

The circuit presented in Figure 2.15 is one possible implementation, the oscillator integration constant is *I/C* and the amplitude is 4*IR*.

The resonant frequency is expressed through Equation 2.27.

$$f = \frac{1}{2C(4RI)} = \frac{1}{8RC} \tag{2.27}$$

Designing this type of oscillator in CMOS technology, provides an interesting advantage, since the capacitor can be materialized by the simple presence of the MOS parasitic capacitances, which will reduce the area needed for implementation [Wes, 1998].

Next in subchapter 2.3.1 and 2.3.2, it will be addressed not only a well-known criterion, as well as an important measure of performance of an oscillator.

2.3.1 Barkhausen Criterion

The basic objective of an oscillator is to convert a DC signal into a periodic signal. A sinusoidal oscillator generates a sinusoid with frequency ω_0 and amplitude V_0.

$$v_{OUT}(t) = V_0 \cos(\omega_0 t + \theta) \tag{2.28}$$

For digital purposes, oscillators generate a clock signal (square-waveform with period T_0).

Figure 2.20 [Oli, 2008] shows a sinusoidal oscillator output in time domain and Figure 2.21 shows the aforementioned output in frequency domain [Oli, 2008].

As shown in Figure 2.22, sinusoidal oscillators can be interpreted as a feedback system, with the transfer function expressed by the Equation (2.29).

$$\frac{Y_{out}(j\omega)}{X_{in}(j\omega)} = \frac{H(j\omega)}{1-H(j\omega)\beta(j\omega)} \tag{2.29}$$

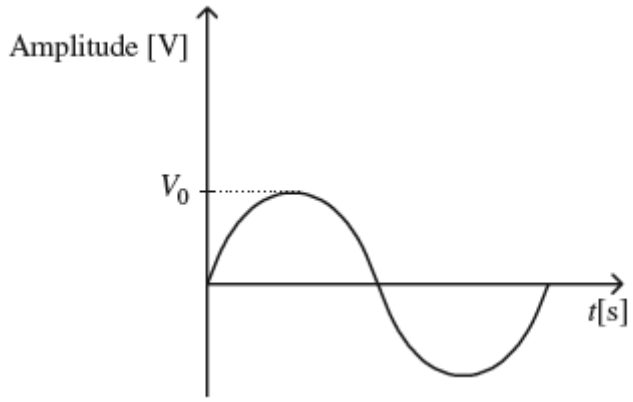

Figure 2.20- Sinusoidal oscillator output in time domain.

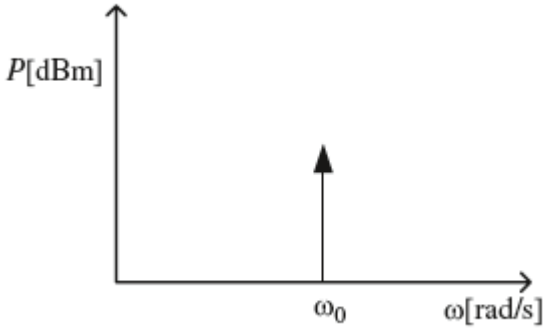

Figure 2.21- Sinusoidal oscillator output in frequency domain.

The necessary conditions related to the loop gain for steady-state oscillation with frequency ω_0 are known as the Barkhausen conditions.

Figure 2.22 presents a feedback system block diagram [Oli, 2008].

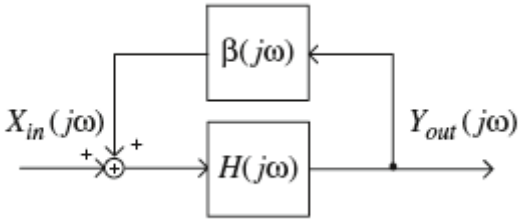

Figure 2.22- Feedback system block diagram.

Below it will be addressed the aforementioned conditions.

The loop gain has to be unity (this is the gain condition), and the open-loop phase shift must be $2k\pi$, where k is obviously an integer including zero (this is the phase condition).

$$|H(j\omega_0)\beta(j\omega_0)| = 1 \quad (2.30)$$

$$arg[H(j\omega_0)\beta(j\omega_0)] = 2k\pi \quad (2.31)$$

The Barkhausen criterion is very important because it gives the appropriate and necessary conditions for stable oscillations. Nevertheless, does not guarantee the start of oscillation.

This means that for a circuit to oscillate, or in other words, for the oscillation to start, triggered by noise, when the system is switched on, the loop gain must be greater than unity, $|H(j\omega_0)\beta(j\omega_0)| > 1$ [Lee, 2001].

2.3.2 Phase-noise

In modern transceiver applications, the most significant difference between ideal and real oscillators is the phase-noise [Raz, 1996].

The noise generated at the oscillator output originates random fluctuation of the output amplitude and phase.

This implies that the output spectrum has bands around ω_0 and its harmonics.

The noise can be generated inside the circuit, or outside the circuit: inside due to passive and active devices and outside due to power supply.

Some effects, such as nonlinearity and periodic variation of circuit parameters make it very difficult to foresee phase-noise.

The noise causes fluctuations of both amplitude and phase.

The oscillator noise can be characterized in two domains: the frequency domain (phase-noise), or in the time domain (jitter).

The first one is used by analog and RF designers, while the second is used by digital designers.

There are numerous ways to quantify the variations of phase and amplitude in oscillators.

Normally, they are characterized in terms of the single sideband noise spectral density, $\mathcal{L}_{(\omega)}$, expressed in decibels below the carrier per hertz (dBc/Hz).

This characterization makes sense for all types of oscillators and can be described as:

$$\mathcal{L}_{(\omega_m)} = \frac{P(\omega_{m)}}{P(\omega_0)} \qquad (2.32)$$

In Equation 2.32 $P(\omega_{m)}$ is the single sideband noise power at a distance of ω_m from the carrier ω_0 in a 1 Hz bandwidth and $P(\omega_0)$ is the carrier power.

The advantage associated with this parameter is related to its ease in terms of measurement.

This can be done in two ways: 1) with the use of a spectrum analyzer, which is a general-purpose equipment, but will definitely provide errors; 2) with phase or frequency demodulators with particular and well known properties.

In regard to Equation 2.32, the spectral density includes not only phase noise, but also amplitude noise, and it should be noted that they cannot be separated.

Regardless this fact, practical oscillators have an amplitude stabilization mechanism, which strongly reduces the amplitude noise, while the phase-noise is unaffected.

The Equation 2.32 is dominated by the phase-noise, so $\mathcal{L}_{(\omega_m)}$ is known merely as phase-noise.

The carrier-to-noise ratio (CNR) can also be used to describe the oscillator phase-noise.

Figure 2.23 shows the spectrum of oscillator output with phase noise [Oli, 2008].

The CNR in a 1 Hz frequency band at the distance of ω_m from the carrierω_0, can be described through the Equation (2.33).

$$CNR(\omega_m) = \frac{1}{\mathcal{L}_{(\omega_m)}} \qquad (2.33)$$

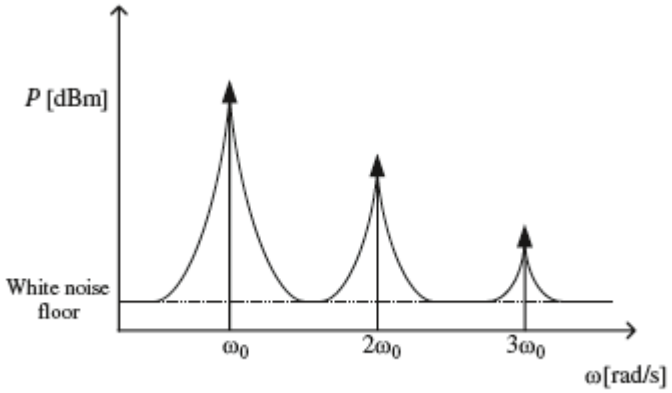

Figure 2.23- Spectrum of oscillator output with phase.noise.

2.3.3 Importance of Phase Noise in Wireless Communications

The phase-noise in the local oscillator will spread the power spectrum around the oscillation frequency of interest.

As a consequence of this fact, the immunity against adjacent interferer signals will be restricted.

Notably, in the receiver path it is intended to down convert a specific channel located at a given distance from the oscillator frequency; due to the oscillator phase-noise, not only the desired channel is downconverted to an intermediate frequency, but also the nearby channels or interferers, corrupting the wanted signal.

This phenomenon is usually called “reciprocal mixing”.

In the case of the transmitter path the phase-noise tail of a strong transmitter can corrupt and overwhelm close weak channels.

As a mere example, if a receiver detects a weak signal at ω_2, this will be affected by a close transmitter signal at ω_1 with significant phase-noise.

Figure 2.24 shows the phase-noise effect on the receiver and the unwanted down conversion [Oli, 2008] and Figure 2.25 presents the phase-noise phenomenon on the transmitter path [Oli, 2008].

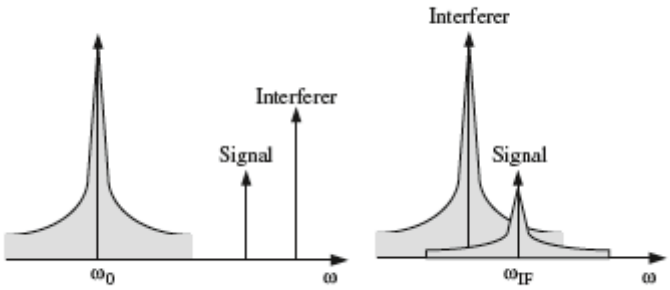

Figure 2.24- Phase-noise effect on the receiver and the unwanted down conversion.

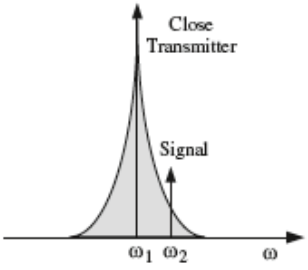

Figure 2.25- Phase-noise phenomenon on the transmitter path.

Chapter 3. CMOS Active Inductors

3.1 Definition and characteristics

CMOS Active inductors (AI) are active networks that consist essentially of MOS transistors.

Resistors are often used as feedback elements to optimize the performance of active inductors.

Through certain dc biasing conditions and signal-swing constraints, AI exhibit an inductive characteristic in a specific frequency range.

In this sense, it is crucial to highlight some attractive advantages that CMOS active inductors offer.

Low silicon area: Given the fact that just MOS transistors are normally required in the realization of CMOS active inductors and the inductance of the aforementioned networks, is inversely proportional to the transconductances of the MOS transistors, the silicon consumption of CMOS active inductors is insignificant.

Large and tunable inductance: The smaller the width of the transistors, the larger the inductance.

Besides this fact, the inductance can be tuned appropriately by differing the dc biasing condition of the transistors synthesizing the inductor with a large inductance tuning range.

Large and tunable self-resonant frequency: The passband center frequency of an active inductor RF bandpass filter is normally set to the self-resonant frequency of the AI of the filter.

In chapter four, it will be clear that the larger the self-resonant frequency of the AI, the higher the passband center frequency of the filter.

To conclude these considerations, it can be said that a large self-resonant frequency of active inductors ensures that the active inductors will have an inductive characteristic over a large frequency range.

Large and tunable quality factor: The quality factor of CMOS active inductors is defined with the ohmic loss of the inductors, arising essentially from the finite output resistance of the transconductors of the inductors.

In fact, the quality factor of CMOS AI can be maximized through the increase of the output resistance [Oli, 2011].

There are several strategies to increase the output resistance. Just as an example, it can be referred cascodes, regulated cascodes or negative resistor compensation. However it is important to highlight the fact that each one of these methods has its own degree of compensation, that is, every single one can be varied.

Considering the first method discussed, the cascode approach, the output resistance of a cascade-configured transconductor can be adjusted by changing the biasing voltage of the cascading transistor.

Compatibility with digital CMOS technologies: CMOS active inductors can be performed with the use of standard digital CMOS processes.

Regardless some attractive advantages that CMOS active inductors offer, they present several disadvantages.

As an example, although they reveal an extraordinary ability to optimize the control of the quality factor, typically Active Inductors have a low quality factor.

In summary, one can say that higher noise, nonlinearity and power consumption are the major disadvantages of active inductors due to the fact that these circuits are realized using active devices which have higher noise.

Several of the active inductors configurations considered in previous work can be simplified to the model shown in Figure 3.1.

It is important to mention that the aforementioned figure presents Newton's notation for differentiation, also known as the dot notation for differentiation.

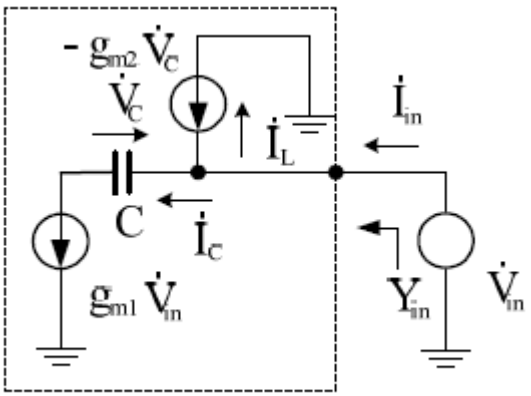

Figure 3.1 – Simplified model of AI configuration.

Figure 3.2 represents the phasor diagram that describes the operation of the model previously discussed.

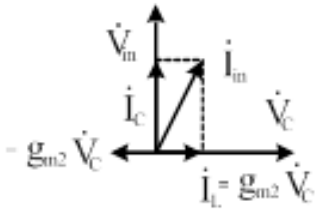

Figure 3.2 – Phasor diagram that illustrates the operation of the simplified model.

In fact, considering a sinusoidal input voltage $\dot{V}_{in}$ applied to the active two-port situated within the dotted line of Figure 3.1, the controlled current source $g_{m1}\dot{V}_{in}$.realizes the current expressed in Equation 3.1:

$$\dot{I}_C = g_{m1}\dot{V}_{in} \tag{3.1}$$

Assuming that the voltage $\dot{V}_C = -j\left[\left(\frac{g_{m1}}{\omega C}\right)\right]\dot{V}_{in}$ at the capacitor C is responsible or used for control another current source, in circumstance $g_{m2}\dot{V}_C$, which develops the current:

$$\dot{I}_L = g_{m2}\dot{V}_C = -j\left[\left(\frac{g_{m1}g_{m2}}{\omega C}\right)\right]\dot{V}_{in} \tag{3.2}$$

The input current can be expressed as follows:

$$\dot{I}_{in} = \dot{I}_C + \dot{I}_L = \dot{V}_{in}\dot{Y}_{in} \tag{3.3}$$

The input impedance $\dot{Y}_{in}$ is equal to $g_{m1} - j\left[\left(\frac{g_{m1}g_{m2}}{\omega C}\right)\right]$ (3.4)

This means that $\dot{Y}_{in}$ possesses the necessary inductive component. The Figure 3.3 (3.3) is related to the equivalent circuit of the two-port that will include the inductance

$$L_{oe} = \frac{C}{(g_{m1}g_{m2})} \tag{3.5}$$

Shunted by the resistor $R_{oe} = \frac{1}{g_{m1}}$

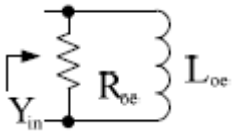

Figure 3.3 – Equivalent circuit of the two-port.

Normally, designers try to minimize the influence of the resistance aforementioned.

This objective centered in the reduction of the influence indicated, can be reached by two methods:

1) By selecting accurately the parameters g_{m1} and g_{m2}.
2) Choosing accurately the parameters of the specific circuit where the active inductor is employed.

3.2 Proposed approach

Equation 3.3 shows that the input current $\dot{I}_{in}$, has in its constitution the component $\dot{I}_C$. This is actually an active component for the input current and the strategy embraced relates to a compensation of this particular component. The compensation process results by adding a third current source $-g_{m1}\dot{V}_{in} = -\dot{I}_C$.

In terms of the components that the input current now includes, with this compensating current, it is only noted the inductive component $\dot{I}_L$.

In other words, it can be said that the compensated two-port behaves as a pure inductor.

Although this compensation may seem complicated, since the third current source involves the addition of an inverting transconductance amplifier, previous work proved that this is possible just by associate one additional transistor.

It is important to say that this approach changes the point of view on design of active inductors shown in Figure 3.1.

Indeed, this modified design provides an interesting control in regard of Q-factor, that is, it is possible to achieve high Q-factor stable active resonators.

Figure 3.4 shows the two-port with inductive input current and Figure 3.5 demonstrates the compensation process and how the current seen by the input voltage source becomes purely inductive.

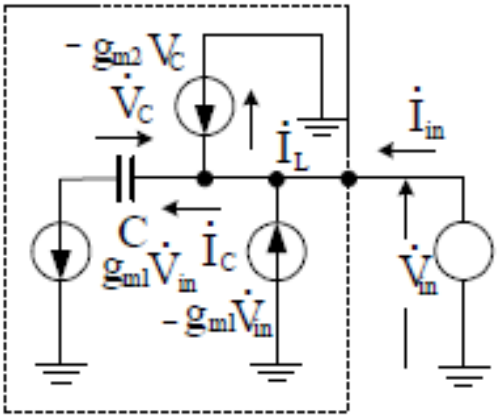

Figure 3.4 – Two- port with inductive input current.

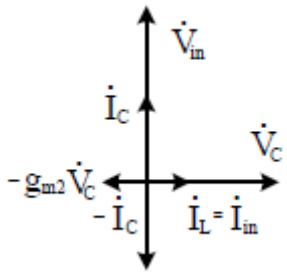

Figure 3.5 – Compensation of the component $\dot{I}_C$.

The modification previously discussed is shown in Figure 3.4, and it is fair to mention that it modifies the properties of basic configuration.

Additionally, will be presented next Figure 3.6, which embodies the realizations of the basic model and, evidently, the model with compensation of the active component in the input current.

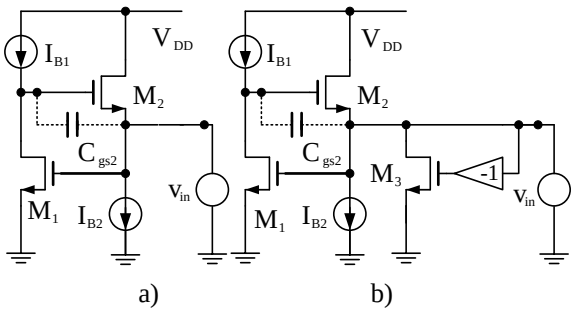

Figure 3.6 – a) Standard realization and b) the addition of the compensation source.

It is crucial to note that the circuits use the capacitor C_{gs2} to make the compensation process a reality. Taking into consideration this compensation, through the use of small-signal models and by analyzing Figure 3.7 it is possible to establish a comparison between the two circuits.

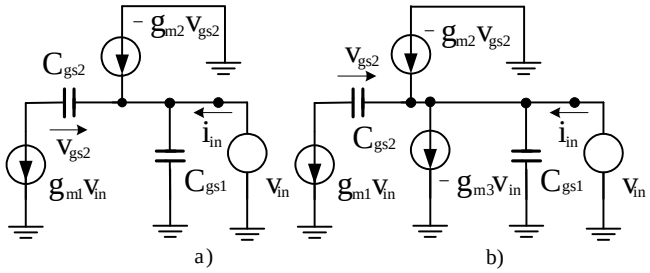

Figure 3.7 – Small signal analysis of circuits of figure 3.6.

Considering Figure 3.7 the Equation (3.6) and Equation (3.7) can be written:

$$i_{in} = g_{m1}v_{in} - \left(-g_{m2}v_{gs2}\right) + sC_{gs1}v_{in} \tag{3.6}$$

and $v_{gs2} = \left(\frac{1}{C_{gs2}}\right)(g_{m1}v_{in})$ (3.7)

Substituting (3.7) into (3.6), the input admittance of the circuit given in figure 3.7, can be expressed as follows:

$$Y_{in} = g_{m1} + \frac{g_{m1}g_{m2}}{sC_{gs2}} + sC_{gs1} = \frac{1}{R_{oe}} + \frac{1}{L_{oe}} + sC_{oe} \tag{3.8}$$

$R_{oe} = \frac{1}{g_{m1}}$, $L_{oe} = \frac{C_{gs2}}{(g_{m1}g_{m2})}$ and $C_{oe} = C_{gs1}$

In fact, this active inductor can be associated to a parallel RLC circuit, since in a practical perspective, it resumes in an active resonator. In chapter four, it will be presented the theoretical and simulation results of the parallel RLC-circuit.

The resonance frequency of the circuit is given by:

$$\omega_p = \frac{1}{\sqrt{L_{oe}C_{oe}}} = \sqrt{(g_{m1}g_{m2})/(C_{gs1}C_{gs2})} \tag{3.9}$$

And the value of Q-factor can be expressed as:

$$Q = \omega_p C_{oe} R_{oe} = \sqrt{(g_{m2}/g_{m1}}\sqrt{C_{gs1}/C_{gs2}} \quad (3.10)$$

Regardless the constitution of Equation 3.10, in terms of sizing (this consideration will be more detailed in chapter four) it was decided to choose the same value of transconductance for g_{m1} and g_{m2}, and capacitors C_{gs1}

Normally, designers are interested to control resonance frequency and Q-factor, independently. Through previous work, it is known that by analyzing the circuit shown in figure 3.7, input admittance is:

$$Y_{in} = g_{m1} - g_{m3} + (g_{m1}g_{m2})/(sC_{gs2}) + sC_{gs1} \quad (3.11)$$

In terms of Q-factor, there is a difference in terms of the value of R_{oe}, that is:

$R_{oe} = \frac{1}{(g_{m1}-g_{m3})}$. This means that Q-factor equation becomes:

$$Q = \left(\frac{1}{g_{m1}-g_{m3}}\right)\sqrt{\frac{C_{gs1}}{C_{gs2}}}\sqrt{g_{m1}g_{m2}} \quad (3.12)$$

Equations (3.11) and (3.12) emphasizes the idea that the addition of a compensating circuit, provides the advantage of better control of the Q-factor of the equivalent RLC-circuit.

Indeed, this control is extremely important whenever active inductors are involved and the chapter dedicated to the simulation process highlight the key role that this control took during the realization of the present work.

It should be mentioned the fact that to improve the drive of I_{D1} (drain current of M_1) into the gate-to-source capacitor of M_2, it is used cascoding at the drain of M_1.

In this sense, Figure 3.8 presents the cascoding at the drain of M_1.

Moreover, it is important to highlight the fact that each one of the current sources presented in the proposed circuit is ideal.

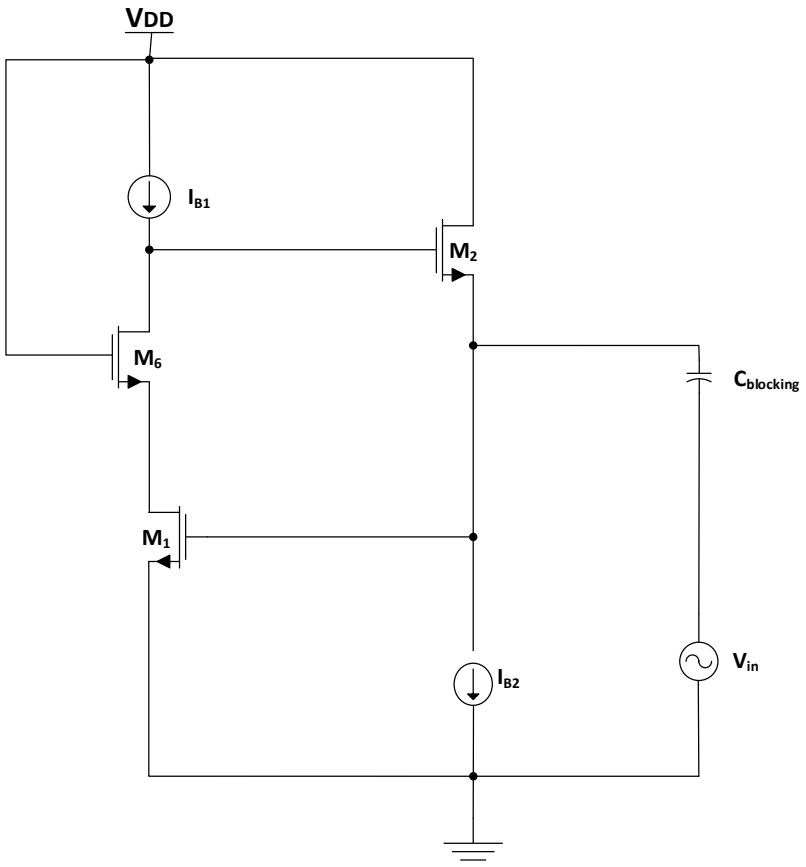

Figure 3.8 – Cascoding at the drain M_1.

Indeed, this control is extremely important whenever active inductors are involved and the chapter dedicated to the simulation process highlight the key role that this control took during the realization of the present work.

The cascoding above discussed is responsible for the compensation of active component in the circuit.

The drive from the input to the source of cascoding transistor gives the necessary gain of $\frac{-g_{m1}}{g_{m6}}$ in regard to the input signal. The addition of one transistor, in this case M_3, guarantees the desired compensation.

Figure 3.9 shows the introduction of the aforementioned device in order to achieve the compensation discussed.

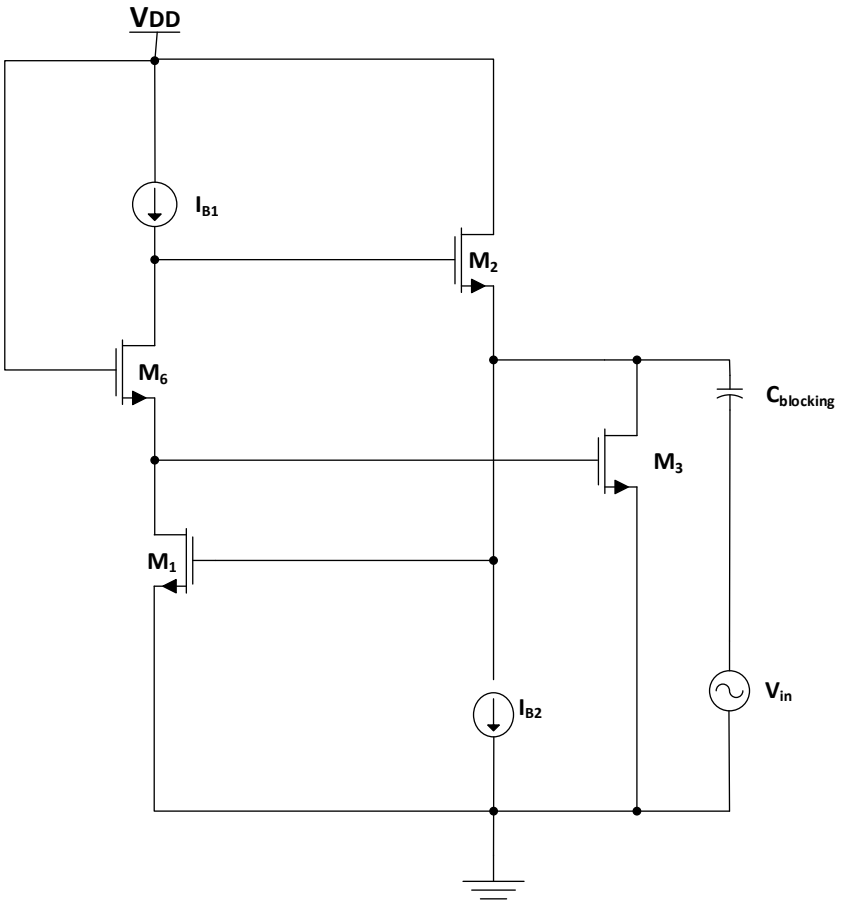

Figure 3.9 – Addition of transistor M_3 to the realization of the required compensation.

The input admittance associated to figure 3.9 can be described as:

$$Y_{in} = g_{m1} - \frac{(g_{m3}g_{m1})}{g_{m6}} + \left(\frac{(g_{m1}g_{m2})}{sC_{gs2}}\right) + sC_{gs1} \tag{3.13}$$

In terms of resonance frequency, there is no variation. But the quality factor of this active inductor is given by:

$$Q = \left(\left(\frac{1}{g_{m1}}\right) - \left(\frac{g_{m1}g_{m3}}{g_{m6}}\right)\right)\sqrt{\frac{C_{gs1}}{C_{gs2}}}\sqrt{g_{m1}g_{m2}} \tag{3.14}$$

Chapter 4. Prototype Design and Simulation Results

4.1 Initial premises of first sizing

The design process and all simulations carried out in the present chapter, refer to the circuit show in Figure 3.8.

To clarify this fact, the aforementioned figure is purposely presented again.

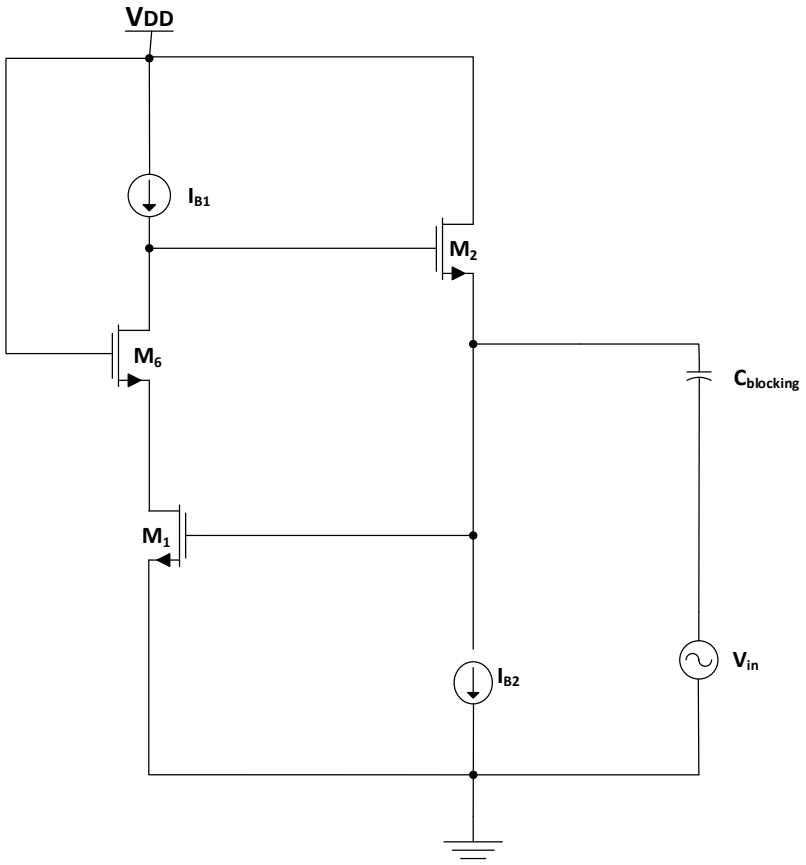

Figure 4.1 – The proposed circuit.

In order to study and comprehend all the relevant premises related to the circuit with the maximum possible property, firstly it was decided to proceed to the design of transistors M_1 and M_2 and setting W_6 and L_6, of transistor M_6.

This approach allows more clear interpretations regarding to the influence of transistor M_1 and M_2, more precisely the transconductances, since the aforementioned

parameters and the gate-to-source capacitances of transistor M_1 and M_2 constitute the expression that makes possible to obtain the quality factor.

Again, it is important to highlight the equations:

$$\omega_p = \frac{1}{\sqrt{L_{oe}C_{oe}}} = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} \tag{4.1}$$

$$Q = \omega_p C_{oe} R_{oe} = \sqrt{g_{m1}g_{m2}}\sqrt{C_{gs1}C_{gs2}} \tag{4.2}$$

These equations are related to the circuit designated as “basis” (indeed, it is an abuse of language), that is, without the presence of transistor M_3.

Moreover, below it is shown the Table 1, which contains the values of the first sizing regarding to the transistors present in the respective circuit.

Table 1- First sizing of M_1 and M_2.

Device	$\boldsymbol{Length\ L(nm)}$	$\boldsymbol{\frac{W}{L}}$	$\boldsymbol{Width\ W(\mu m)}$
M1	825	32	26.4
M2	825	32	26.4

The strategy adopted was based on adjust the minimum number of parameters, in order to investigate the contribution/importance of the sizing of transistors M_1 and M_2.

In this sense, initially it was defined $L_1 = L_2 = 825\ nm$ and assumed $I_{B1} = I_{B2} = 20\ \mu A$.

Additionally, it was considered $V_{DSAT1} = V_{DSAT2} = 50\ mV$. It is extremely important to mention that all the examples considered in this part of the present work, were designed for $130\ nm$ MOS technology using BSIM3V3 models, simulated with Cadence software, with the following parameters:

$\mu C_{ox} = 500 \frac{\mu A}{V^2} V_{TH} = 0.38\ V$, $C_{ox} = 12.3\ fF/\mu m^2$. The circuits were designed for the power supply voltage $V_{DD} = 1.2\ V$.

One can also find the relation $\left(\frac{W}{L}\right)_1 = 32$. Taking into consideration the aforementioned values of L_1 and L_2, it was possible to obtain W_1=$W_2 = 26.4\ \mu m$.

As previously discussed in chapter three, Initially it was considered the possibility of defining different sizes for transistor M_1 and M_2, specifically because of Equation (3.10).

Nevertheless, since quickly it became obvious that there would be evident discrepancies between theoretical and simulated results (transistors are operating in weak inversion), it was intentionally decided to choose the same size for both devices.

This strategy simplified the circuit behavior investigation. Regarding to the transconductances of the transistors previously indicated, and giving the fact that was assumed $20\,\mu A$ in the drain of transistor M_1 and M_2 ($I_{D1} = I_{D2}$), the value of V_{DSAT} presented above, and $C_{gs1} = \left(\frac{2}{3}\right) C_{ox} W_1 L_1$, one also found $g_{m1} = g_{m2} = 773\,\mu A/V$ and $C_{gs1} = C_{gs2} = 178.6\,fF$.

It is fair to mention that the threshold voltage of M_1 and M_2 can also be found as $V_{TH1} = V_{TH2} = 0.38\,V$ and this allows one to find $V_{gs1} = V_{gs2} = 0.43\,V$.

Still, in the field of theoretical sizing, it was found that $V_{G1} = 0{,}43\,V$ and $V_{G2} = 0.86\,V$.

Finally, in terms of transistor M_6, giving the fact that $V_{GS} = 0.7\,V$ one finds the relation $\left(\frac{W}{L}\right)_6 = 0.69$ and since it was chosen $L_6 = 250\,nm$ (because it is a value close to $2L_{min}$) it results in $w_6 = 0.17\,\mu m$.

For all examples considered in the present document, it was decided not to realize any changes in the size of M_6.

Through the well-known equations that allow to determine the transconductance and gate-to-source capacitance of a transistor, since $V_{TH6} = 0.367\,V$ and $V_{DSAT6} = 0.33\,V$, it became possible to find $g_{m6} = 120\,\mu A/V$ and $C_{gs6} = 0.4\,fF$.

This theoretical sizing, supported by equations presented in chapter three, results in the following parameters of the parallel RLC circuit:

Table 2 – Parameters of the parallel RLC-circuit.

$\boldsymbol{R_{oe}(k\Omega)}$	$\boldsymbol{L_{oe}(nH)}$	$\boldsymbol{C_{oe}(fF)}$
1.3	299	179

Taking into consideration not only the values obtained and shown in Table 2, but also the equations 4.1 and 4.2, the calculations result in the following values, in terms of frequency center (f_p) and quality factor (Q) :

Table 3 - f_p and Q factor obtained, related to first sizing.

$f_p(GHz)=\frac{\omega_p}{(2\pi)}$	Q
0.69	1

Moreover, the aforementioned results are very important because through these values it is possible to make a theoretical prediction.

Later in the present chapter, it will be possible to analyze the discrepancy between these theoretical values and the simulation results.

4.2 Simulation results for active inductor without M_3

Largely because the simulations were based on successive sizing of the transistors, it becomes very difficult to separate considerations related to the sizing process and respective simulations.

This is the reason that explains the strategy of including in the same chapter, all the premises referring to the sizing process and simulation results.

Subsequently, it will be realized considerations related to the simulation results, regarding not only to the first sizing, but also the following ones.

It will be presented the most relevant simulation results related to the sizing of M_1 and M_2, which allowed to find different values of f_p and Q.

Table 4 – First simulation results of the proposed circuit.

	M_1	M_2	M_6
$C_{gs}(fF)$	102.63	96.49	0.297
$g_m(\mu A/V^2)$	442.6	449.68	36.30
$V_{DSAT}(mV)$	69.84	69.14	412.93
$V_{GS}(mV)$	264.77	280.76	830.39
$V_{TH}(mV)$	248.22	280.20	317.2

The circuit presented in Figure 3.8 was simulated. The static voltages obtained in simulation were $V_{G1} = 264.77\ mV$ (since $V_{G1} = V_{GS1}$, with $V_{S1} = 0$), $V_{D1} = 370\ mV$ ($V_{D1} = V_{DD} - V_{GS6}$) and $V_{G2} = 545.53\ mV$ ($V_{G2} = V_{GS1} + V_{GS2}$).

The values of transconductances obtained in simulation were $g_{m1} = 442.6\,\mu A/V$, $g_{m2} = 409\,\mu A/V$ and $g_{m6} = 36\,\mu A/V$.

By establishing a comparison between the theoretical values and the values obtained in simulation, one can see that there is a significant reduction of the values of the transconductances. Nevertheless this reduction was expected, because transistors are functioning in weak inversion and devices of small feature technologies suffer from velocity saturation.

In terms of capacitances, although the sizing of transistor M_1 and M_2 was the same, the simulation results allow to conclude that C_{gs2} presents the most significant reduction.

Specifically, simulation results for gate-to-source capacitors were $C_{gs1} = 102.63\,fF$, $C_{gs2} = 96.49\,fF$ e $C_{gs6} = 0.297\,fF$. In terms of frequency center and quality factor, simulation results obtained were $f_p = 458.14\,MHz$ and $Q = 1.5$.

It is possible to confirm the discrepancy previously discussed, that is, the theoretical results predicted $f_p = 690\,MHz$ and $Q = 1$.

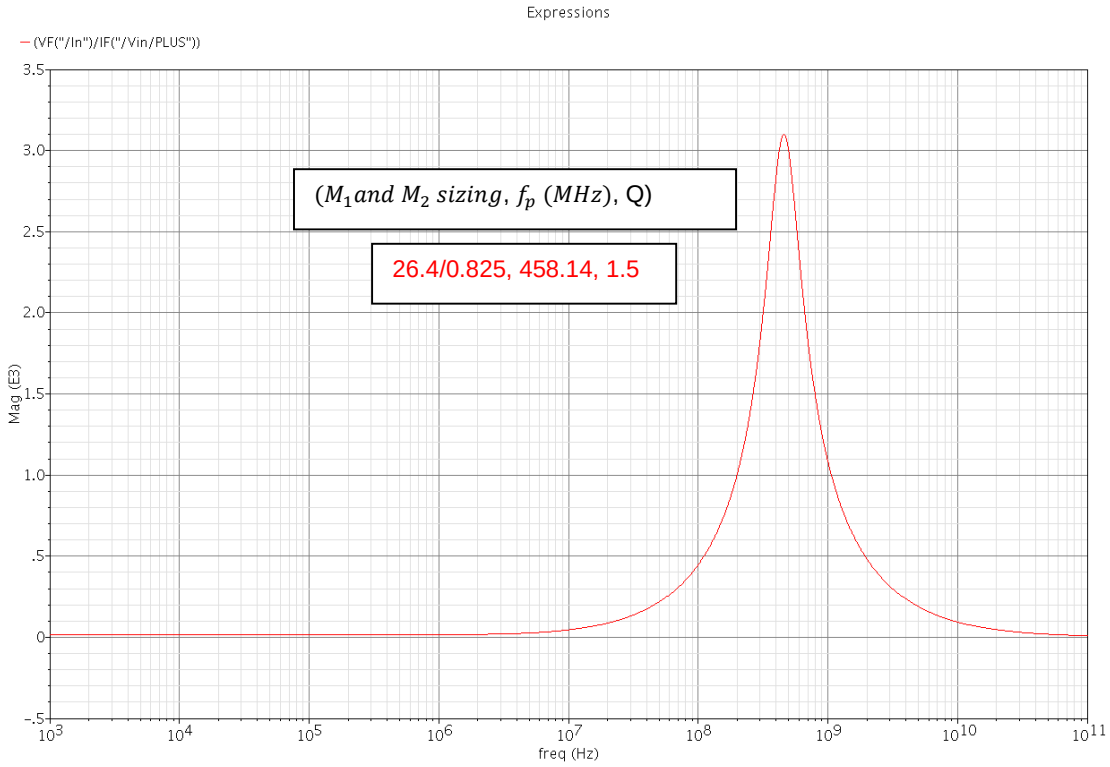

Figure 4.2- – First simulation results for active inductor of Figure 4.1.

The next step consisted of reducing the value of L_1 and L_2, keeping the same relation $\left(\frac{W}{L}\right)$, in order to investigate the impact of the reduction of the sizes of aforementioned transistors, regarding to the value of the quality factor.

Table 5- Second sizing of M_1 and M_2.

Device	$Length\ L(nm)$	$\frac{W}{L}$	$Width\ W(\mu m)$
M1	720	32	23.04
M2	720	32	23.04

Table 6 - Second simulation results of the proposed circuit.

	M_1	M_2	M_6
$C_{gs}(fF)$	77.60	72.6	0,297
$g_m(\mu A/V^2)$	442.92	450.3	37
$V_{DSAT}(mV)$	69.42	68.57	409.28
$V_{GS}(mV)$	258.56	284.41	825.3
$V_{TH}(mV)$	252.94	285.29	317.65

The values of transconductances obtained in simulation were $g_{m1} = 442.92\ \mu A/V$, $g_{m2} = 450.3\ \mu A/V$ and $g_{m6} = 37\ \mu A/V$.

By establishing a comparison between the theoretical values and the values obtained in simulation, one can see the same reduction previously discussed, that is, that there is a significant reduction of the values of the transconductances.

Again, this reduction was absolutely expected, since transistors are functioning in weak inversion and devices of small feature technologies suffer from velocity saturation.

In terms of capacitances, regardless the fact that the sizing of transistor M_1 and M_2 was the same, the simulation results allow to conclude that C_{gs2} still presents the most significant reduction.

Specifically, simulation results for gate-to-source capacitors were $C_{gs1} = 77.60\ fF$, $C_{gs2} = 72.6\ fF$ e $C_{gs6} = 0.297\ fF$. In terms of frequency center and quality factor, simulation results obtained were $f_p = 588.8\ MHz$ and $Q = 1.67$.

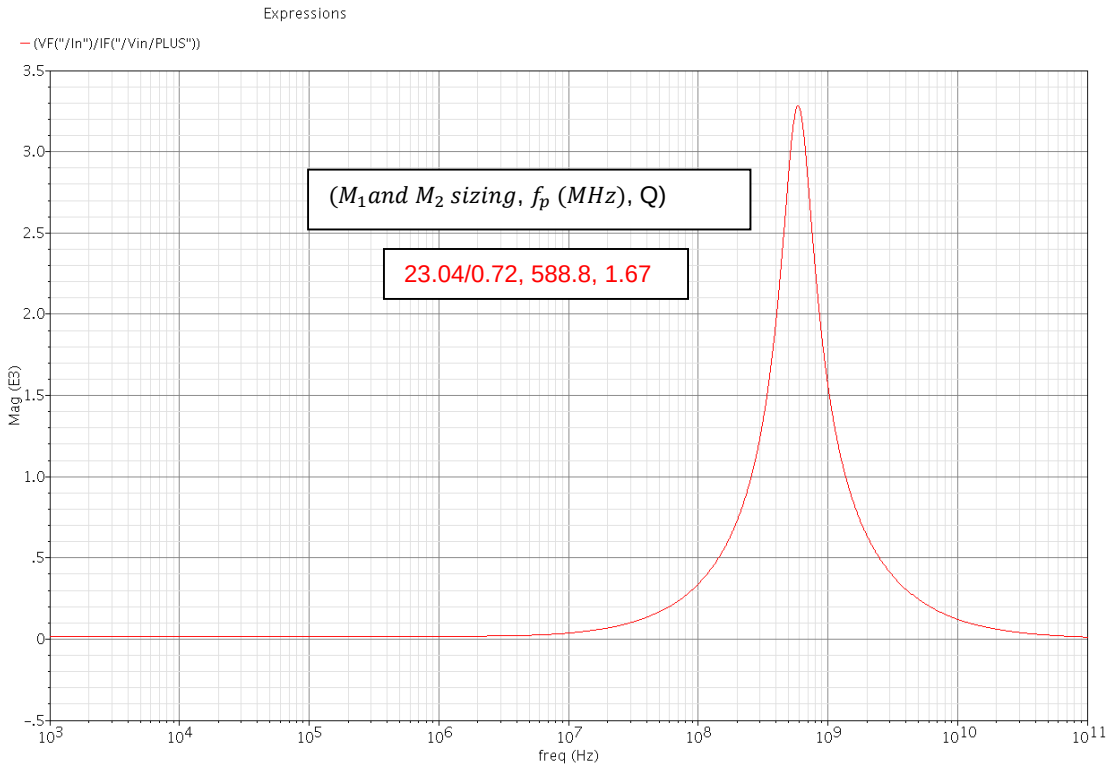

Figure 4.3 - Second simulation results for active inductor of Figure 4.1.

Table 7 - Third sizing of $M_1$and M_2.

Device	$Length\ L(nm)$	$\frac{W}{L}$	$Width\ W(\mu m)$
M1	560	32	17.92
M2	560	32	17.92

Table 8 - Third simulation results of the proposed circuit.

	M_1	M_2	M_6
$C_{gs}(fF)$	47.13	43.63	0.302
$g_m(\mu A/V^2)$	442.31	450.05	38.71
$V_{DSAT}(mV)$	68.81	67.73	403.13
$V_{GS}(mV)$	267.36	293.18	813.55
$V_{TH}(mV)$	262.93	296.17	318.70

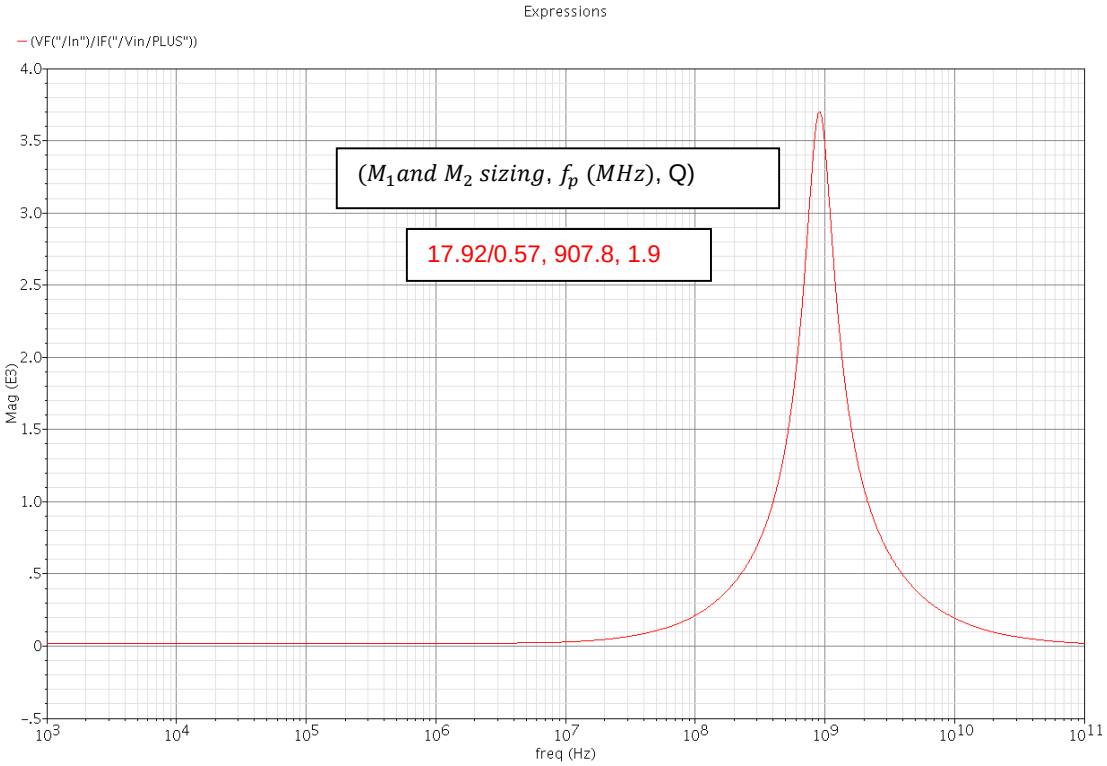

Figure 4.4 - Third simulation results for active inductor of Figure 4.1.

Table 9 - Fourth sizing of $M_1$and M_2.

Device	$Length\ L(nm)$	$\frac{W}{L}$	$Width\ W(\mu m)$
M1	530	32	16.96
M2	530	32	16.96

Table 10 - Fourth simulation results of the proposed circuit.

	M_1	M_2	M_6
$C_{gs}(fF)$	42.27	39.05	0.303
$g_m(\mu A/V^2)$	442.18	449.98	39.15
$V_{DSAT}(mV)$	68.64	67.51	401.45
$V_{GS}(mV)$	269.53	295.37	810.69
$V_{TH}(mV)$	265.43	298.9	318.96

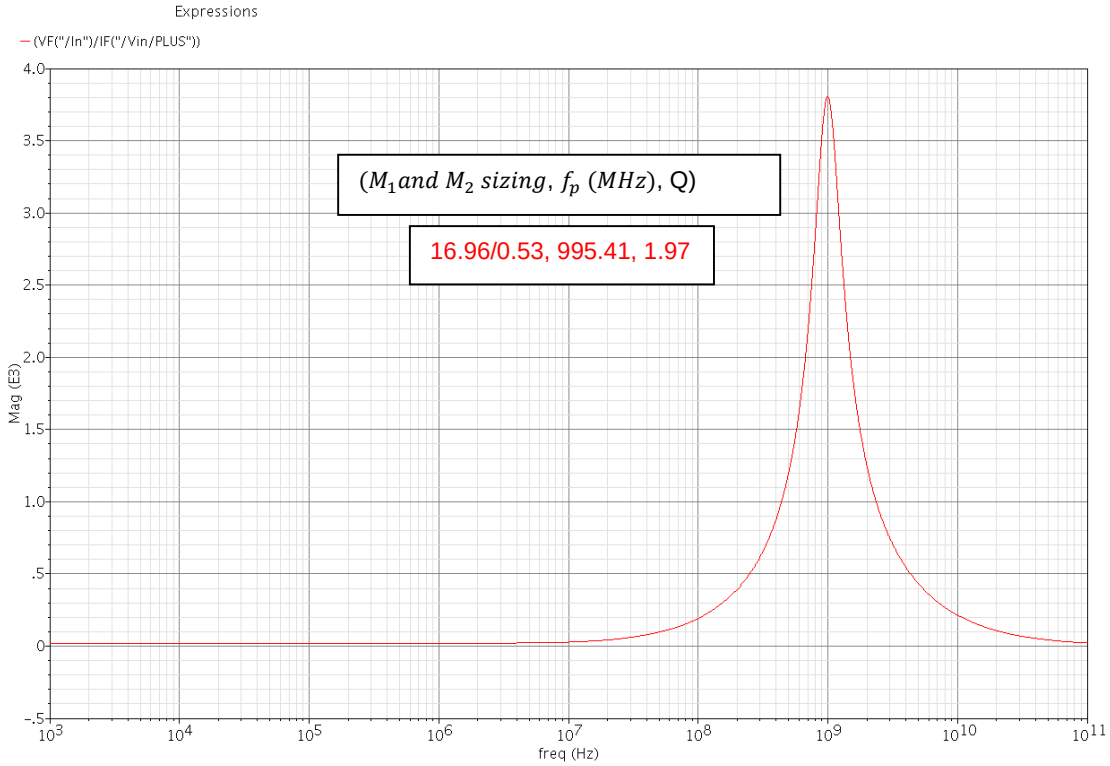

Figure 4.5 - Fourth simulation results for active inductor of Figure 4.1.

Figure 4.5 shows that the reduction of size of the transistors M_1 and M_2, did not implicate a substantial increase of Q-factor.

In order to make clear the difference between the values predicted theoretically and the values obtained by simulation, Table 11 is presented.

Table 11 – Theoretical f_p values and f_p values obtained through simulation.

Simulation results $\boldsymbol{f_p(MHz)}$	Theoretical values $\boldsymbol{f_p(MHz)}$
458.14	688
588.84	904
907.8	1400
995.410	1495

It can be said that for a 450 MHZ to 1 GHz range, the predicted values for f_p are always higher than the f_p values obtained through simulation.

This difference is due to the fact that transistors are operating in weak inversion.

In fact, since the beginning of the theoretical study that the aforementioned difference was expected, because all the design process was based on equations related to strong inversion regime.

As previously discussed, it was intentionally decided to choose the same size for M_1 and M_2. Taking into account the Equation 4.2, it becomes clear that the theoretically expected value for Q- factor is unity.

Below, it is shown not only Table 12, which presents the values of quality factor for each sizing previously discussed and its frequency center, but also Figure 4.6 that allows a comparison between every single simulation result conducted.

Table 12 – Q-factor obtained for each f_p.

$f_p(MHz)$	$Q - factor$
458.14	1.5
588.84	1.67
907.8	1.9
995.410	1.97

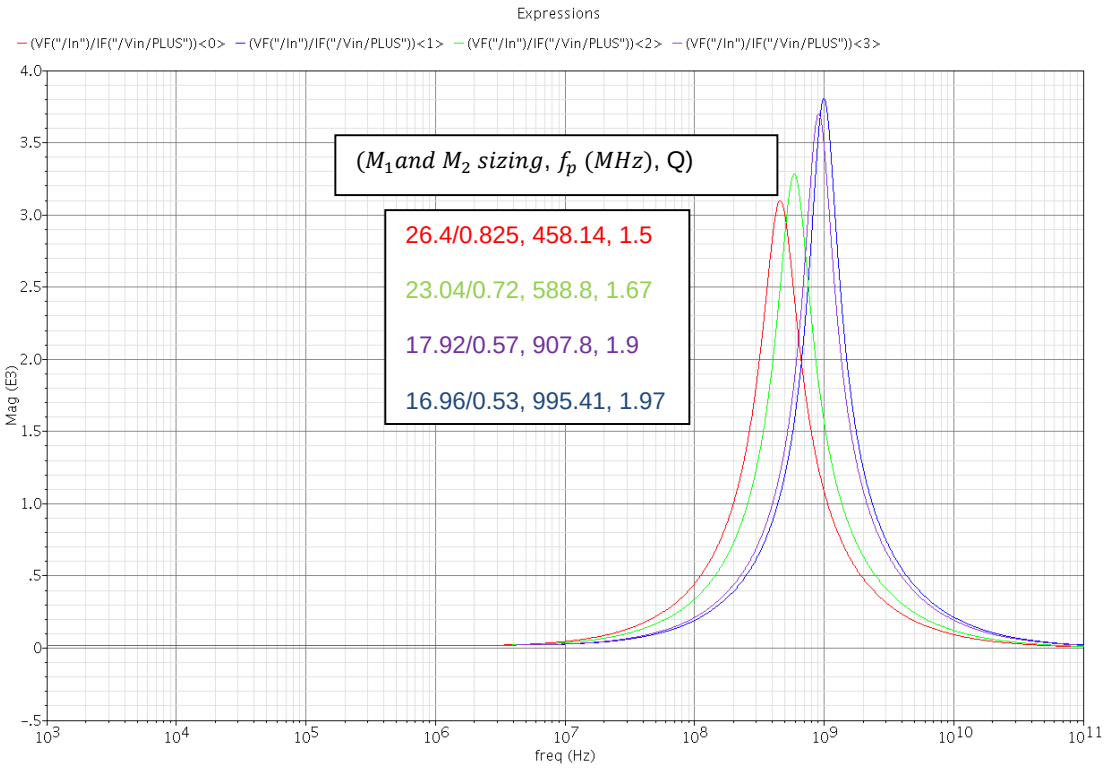

Figure 4.6 – Most relevant simulation results for active inductor.

After the realization of the sizing above indicated, it was possible to conclude that for a 450 MHz to 1 GHz range, the Q-factor did not change significantly.

For instance, the first simulation result led to a quality factor $Q = 1.564$ and the following examples of sizing, led to very similar results, which means that in this particular case, the reduction, even substantial, of size of the transistors M_1 and M_2, did not implicate a significant increase of Q-factor.

Thus, it was embraced a different and perhaps more ambitious approach, in terms of sizing. Taking into consideration this goal, it was decided to choose the value theoretically known as $2L_{min}$, for L_1 and L_2.

Additionally, the value of V_{DSAT} was increased to 68mV and the relation $\left(\frac{W}{L}\right)$ was changed from 32 to 17.3.

Further, the Table 13, which has the parameters mentioned, is shown:

Table 13 – Fifth sizing of $M_1$and M_2.

Device	$\boldsymbol{Length\ L(nm)}$	$\boldsymbol{\frac{W}{L}}$	$\boldsymbol{Width\ W(\mu m)}$
M1	240	17.301	4.15
M2	240	17.301	4.15

It is crucial to say that for this specific example, was considered: $g_{m1} = g_{m2} = 588.235\ \mu A/V$ and $C_{gs1} = C_{gs2} = 8.172\ fF$.

The threshold voltage of transistor M_1 and M_2 can be found as $V_{TH1} = V_{TH2} = 0.38\ V$ and through these parameters it is also possible to find the gate-to-source voltage, that is, $V_{gs1} = V_{gs2} = 0.448\ V$.

Also in regard to the theoretical design, considering the architecture in study, it was obviously possible to define $V_{G1} = 0.448\ V$ and $V_{G2} = 0.896\ V$.

Finally, for transistor M_6, the relations previously presented are still valid. For all the examples realized, it was purposely determined not to make any alteration of L_6 and W_6.

Again, giving the fact that $V_{TH6} = 0.367\ V$ and $V_{DSAT6} = 0.33\ V$, the transconductance and gate-to-source capacitor of M_6 is $g_{m6} = 120\ \mu A/V$ and $C_{gs6} =$

$0.4\ fF$, respectively. As done for the first theoretical example, it was possible to obtain the parameters of the parallel RLC-circuit. Table 14 emphasizes that fact.

Table 14 - Parameters of the parallel RLC-circuit.

$R_{oe}(k\Omega)$	$L_{oe}(nH)$	$C_{oe}(fF)$
1.7	23.6	8.17

The theoretical design led to a frequency center $f_p = 11.457\ GHz$.

Table 15 - Fifth simulation results of the proposed circuit.

	M_1	M_2	M_6
$C_{gs}(fF)$	5.95	5.63	0.337
$g_m(\mu A/V^2)$	390.89	398.21	58.14
$V_{DSAT}(mV)$	76.44	75.04	351.69
$V_{GS}(mV)$	343.99	374.94	728.5
$V_{TH}(mV)$	316.29	357.26	326.04

Similarly, the circuit was simulated. The static voltages obtained were $V_{G1} = 343.99\ mV$ (since $V_{G1} = V_{GS1}$, with $V_{S1} = 0$), $V_{D1} = 471\ mV$ ($V_{D1} = V_{DD} - V_{GS6}$) and $V_{G2} = 718.93\ mV$ ($V_{G2} = V_{GS1} + V_{GS2}$).

The simulated transconductances were $g_{m1} = 390.89\ \mu A/V$, $g_{m2} = 398.21\ \mu A/V$ and $g_{m6} = 58.14\ \mu A/V$.

In terms of capacitances, the conclusions detailed previously regarding to the transistors M_1 e M_2 are still valid, that is, the gate-to-source capacitor C_{gs2} was the parameter that presented the most significant reduction.

Moreover, $C_{gs1} = 5.95\ fF$, $C_{gs2} = 5.63\ fF$, $C_{gs6} = 0337\ fF$, $f_p = 5\ GHz$ and $Q = 4.172$.

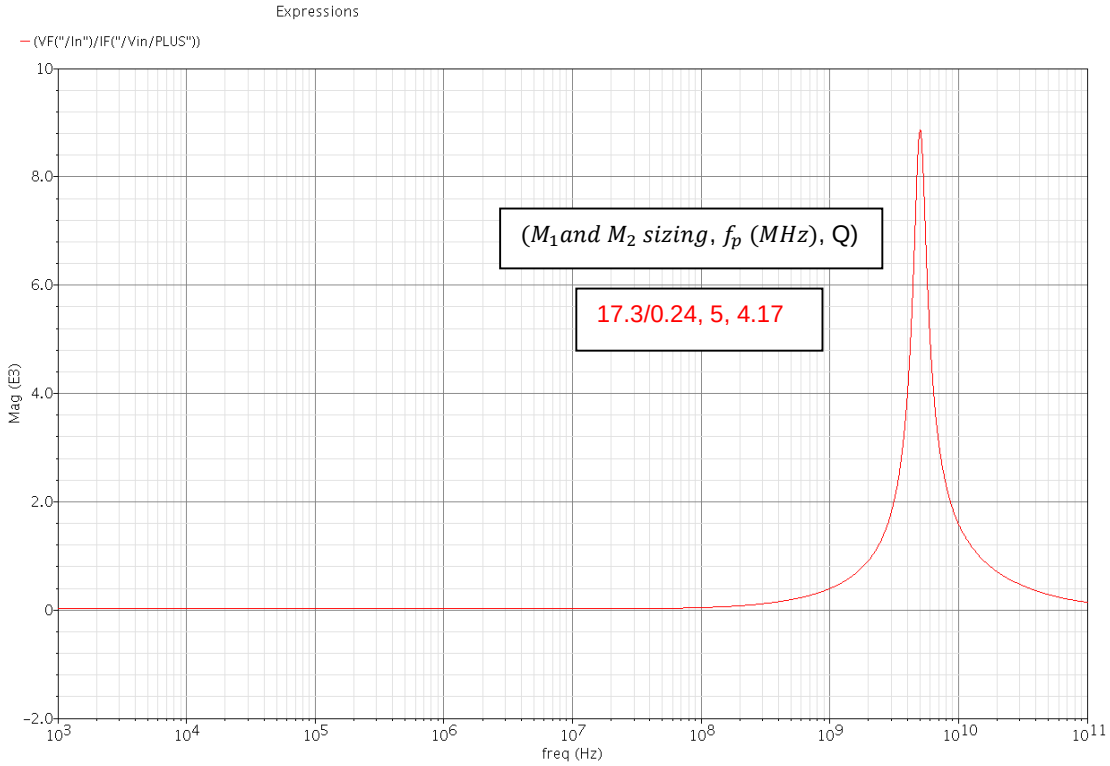

Figure 4.7 – Fifth simulation results for active inductor of Figure 4.1.

Next, Figure 4.8 is shown, which includes the simulation results for the last two realizations discussed.

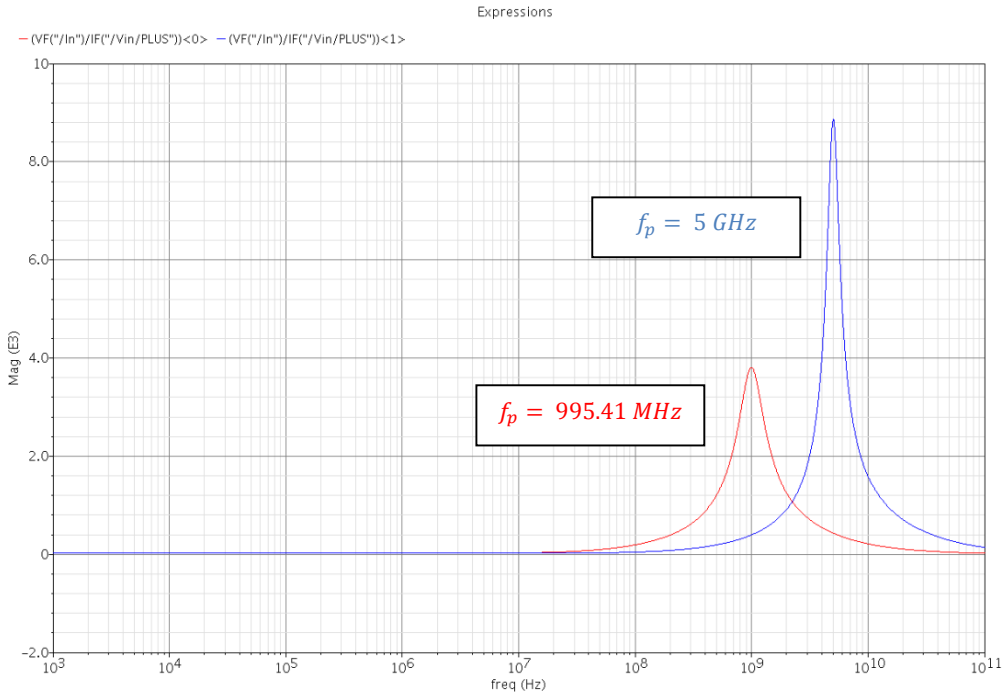

Figure 4.8 - Simulation results of last two examples.

Since the last simulation for a 450 MHz to 1 GHz range led to a quality factor $Q = 1.97$ and the fifth simulation results for active inductor led to a quality factor $Q = 4.17$, it is fair to mention that the increase of Q-factor is evident.

Regardless this conclusion, it is important to highlight the fact that in order to obtain a frequency center approximately of 1 GHz and 5 GHz, it was necessary to perform a theoretical study that pointed to $f_p = 995.4\ MHz$ and $\mathrm{f_p} = 11.5\ GHz$ respectively.

Chapter 5. Oscillator Design

5.1 The addition of M_3 to force the oscillation of the circuit

After proceeding a meticulous study in relation to the circuit initially presented, it was concluded that to increase the quality factor, it was necessary to introduce one more device.

Similarly to what was stated in subchapter 4.1, it is important to mention that the design process and all simulations carried out in the present chapter, refer to the circuit show in Figure 3.9.

In this sense, to emphasize this consideration, the aforementioned figure is deliberately presented again.

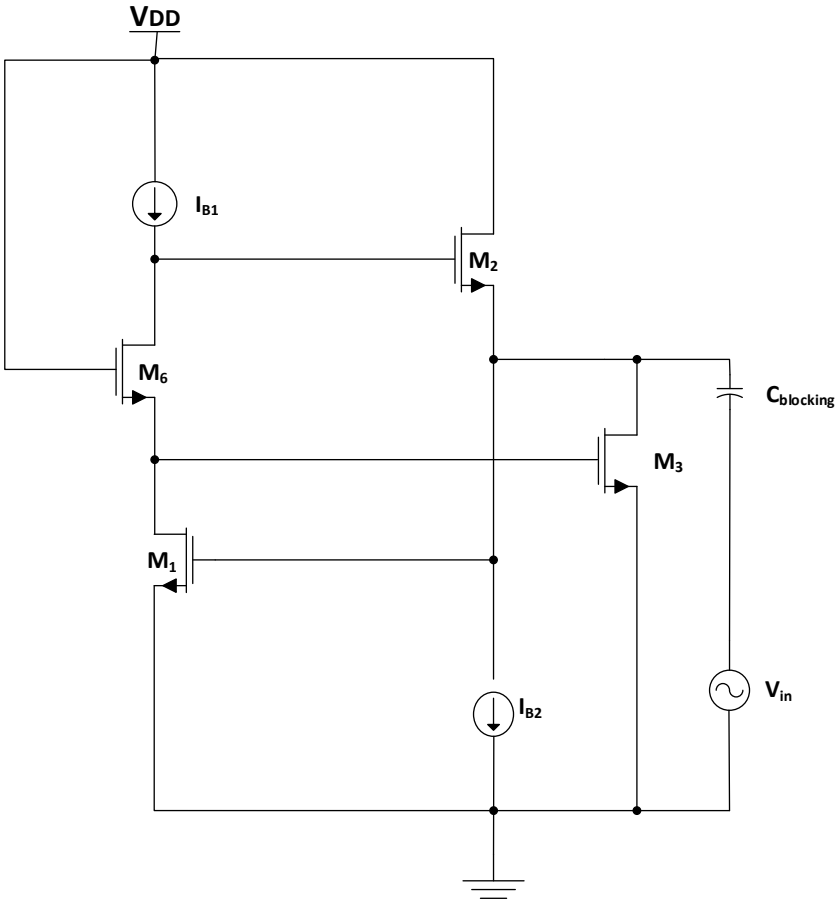

Figure 5.1 – Proposed circuit and the addition of transistor M_3 to achieve higher Q- factors.

After the investigation of the contribution of transistors M_1 and M_2, as can be seen in Figure 5.1, it was added one transistor to the existing circuit.

The addition of the aforementioned transistor had a very clear purpose: in order to obtain higher values of the quality factor.

This purpose can be explained with the fact that to force the oscillation of the circuit it is absolutely necessary that Q-factor assumes significantly high values ($\text{ideally Q} \approx$infinite).

Specifically, the additional device, named M_3, was designed with the following strategy: firstly, it was chosen $L_3 = 1\ \mu m$, and then it was decided to vary W_3.

Regardless the careful design of transistor M_3, it is extremely important to establish a compromise regarding to the current source I_{B2}, since the sum between this particular current and the drain current of M_3, is equal to the drain current of transistor M_2.

Although the necessity of preserving the drain current of M_2 equals to $20\mu m$ is justified, mainly when the circuit behaviors as a filter, it was still decided to try to maintain the value discussed to the current aforementioned, in order to investigate with the maximum possible depth, the influence of I_{B2} and design of M_3, in terms of increasing the quality factor.

Indeed, the strategy embraced consisted of vary W_3 with a step of $0.5\ \mu m$.

In other words, to be more precisely, firstly was chosen $W_3 = 0.5\ \mu m$, and then gradually was increased this size with a variation/step of the same value (from $W_3 = 0.5\ \mu m$ to $W_3 = 2.5\ \mu m$). Additionally, M_3 was realized with $L_3 = 1\ \mu m$.

Similarly as a strategy adopted previously, in terms of design it was decided to choose a solution that implicates the less possible changes of parameters, so that could be possible to better understanding the importance of the reduction of current source I_{B2} and the increase of width of transistor M_3, in the determination of a higher quality factor value.

These steps were taken in successive design, always with the final goal of knowing the associated Q-factor.

In this sense, choosing $W_3 = 0.5\ \mu m$, and setting L_3 with the value previously discussed, was found that the drain current of W_3 is $I_{D3} = 2.65\ \mu A$.

In order to guarantee $20\ \mu m$ in the drain current (I_{D2}) of device M_2, by taking into consideration the relation of currents above indicated, it was mandatory to set $17.35\ \mu m$ in the current source I_{B2}.

One also found that $f_p = 901.7\ MHz$, with bandwidth $B = 284.7\ MHz$.

The first sizing led to a quality factor $Q = 3.167\ MHz$. Evidently, this value is not interesting since, ideally, the bandwidth should be zero, in order to obtain a high quality factor value.

Taking into account the results obtained through this first design, other examples, with the variation of W_3 already explained were realized.

It was perfectly clear that as the width of M_3 increased and simultaneously was reduced the current source I_{B2}, f_p and B evidently decreased, and the quality factor gradually began to take on higher values.

With the variation only of the two parameters above indicated, was possible to obtain $Q = 122.973$. More specifically, by choosing $W_3 = 2.1\ \mu m$ and setting $I_{B2} = 8.463\ \mu A$.

Table 16 not only presents the most relevant realizations for W_3 and I_{B2} but also shows the simulation results for f_p and Q.

Table 16 – Sizing of M_3, I_{B2} and simulation results of f_p and Q of figure 5.1.

$\boldsymbol{W_3(\mu m)}$	$\boldsymbol{I_{B2}(\mu A)}$	$\boldsymbol{f_p(MHz)}$	$\boldsymbol{Q}$
0,5	17,35	901,7	3,167
1	14,48	816,68	5,15
1,5	11,668	743	10,561
1,9	9,8	696,93	44,83
2	9	682,34	122,94

In order to investigate if the aforementioned Q-factor was the maximum possible value to obtain, the next step consisted of increasing the width of M_3 and reducing I_{B2}.

By choosing $W_3 = 2.5\ \mu m$ and $I_{B2} = 6.6\ \mu A$, the Q-factor dropped significantly, more precisely to 13.99.

After reaching a sufficiently relevant quality factor, it was decided to fix the two parameters above mentioned, and began to investigate the influence of increase/ decrease L_3.

One can be noted that, primarly, it was chosen $L_3 = 1\mu m$.

Some realizations of design were carried out, so it is fair to conclude regarding to this particular matter, that the variation of L_3 is irrelevant, or at least, it does not have impact in the calculation of higher Q-factors.

Figure 5.1 shows the first simulation results for higher Q-factors, after the addition of M_3.

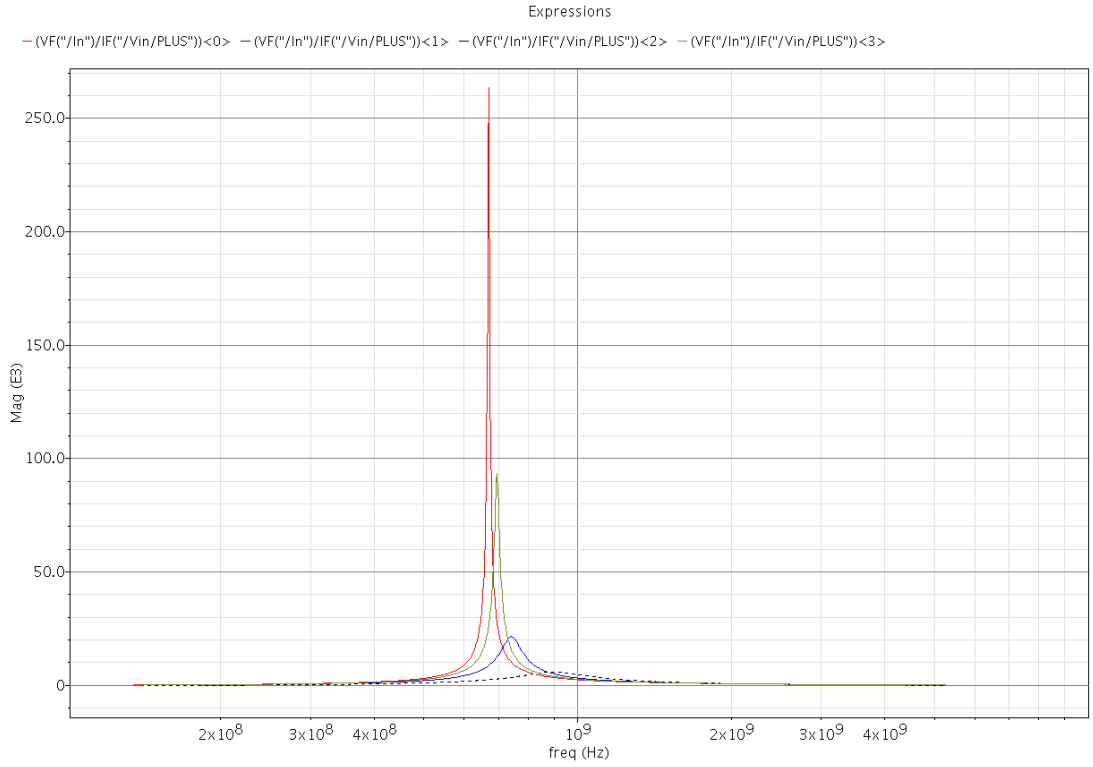

Figure 5.2 – First simulations results for Q- factors, after adding M_3.

Moreover, by selecting $W_3 = 2{,}1\ \mu m$ and setting $I_{B2} = 9{,}3\ \mu A$, the bandwidth decreases, which is a necessary condition to obtain a higher Q-factor, in order to force the oscillation of the circuit.

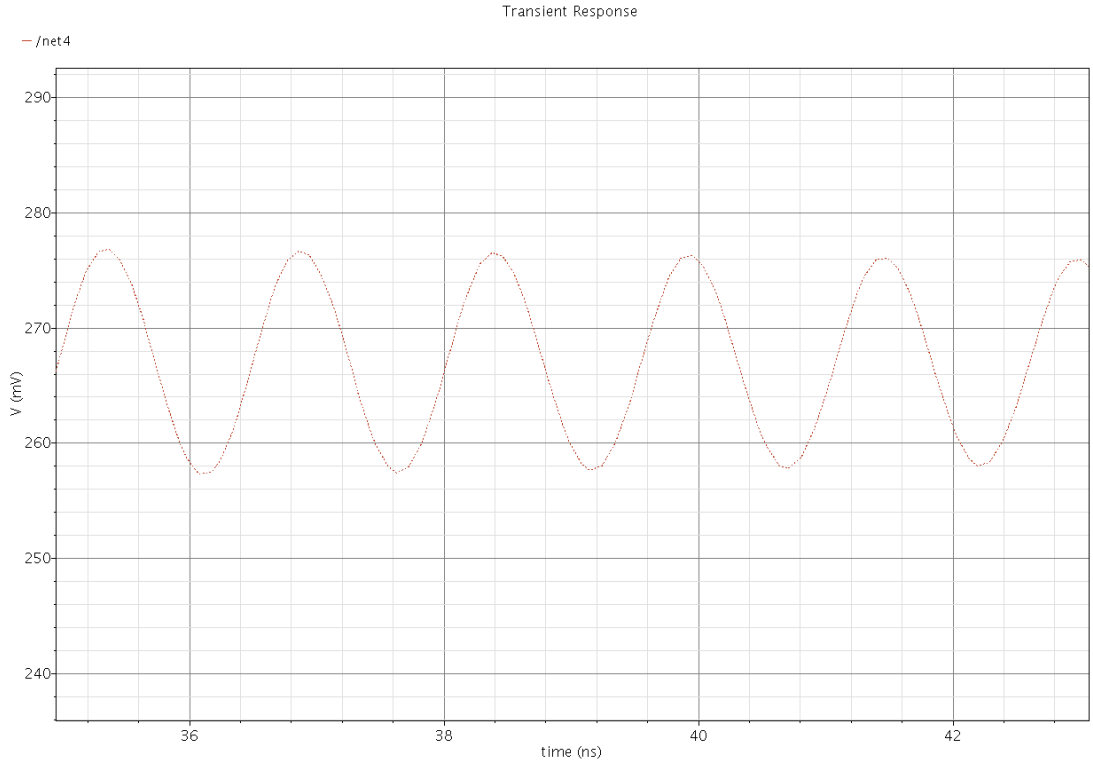

Figure 5.3 - Simulation results for the oscillator with oscillator frequency $f_p = 662.3\ MHz$.

5.2 Final design and simulation results

Given the fact that it was possible to force the oscillation of the circuit (oscillation frequency of 662,3MHz), a strategy related to the investigation of the increase of the current source I_{B2} and the reduction of W_3 in order to obtain an even higher Q-factor was considered.

Table 17 – Second sizing of M_3, I_{B2} and simulation results of f_p and Q of figure 5.1.

$\mathbf{W_3(\mu m)}$	$\mathbf{I_{B2}(\mu A)}$	$\mathbf{f_p(MHz)}$	**Q**
1,1	7,163	2971	6,268
1	8,463	3062	6,789
0,9	9,163	3155	7,695
0,7	11,363	3403	10,806
0,35	15,363	4009	235,824

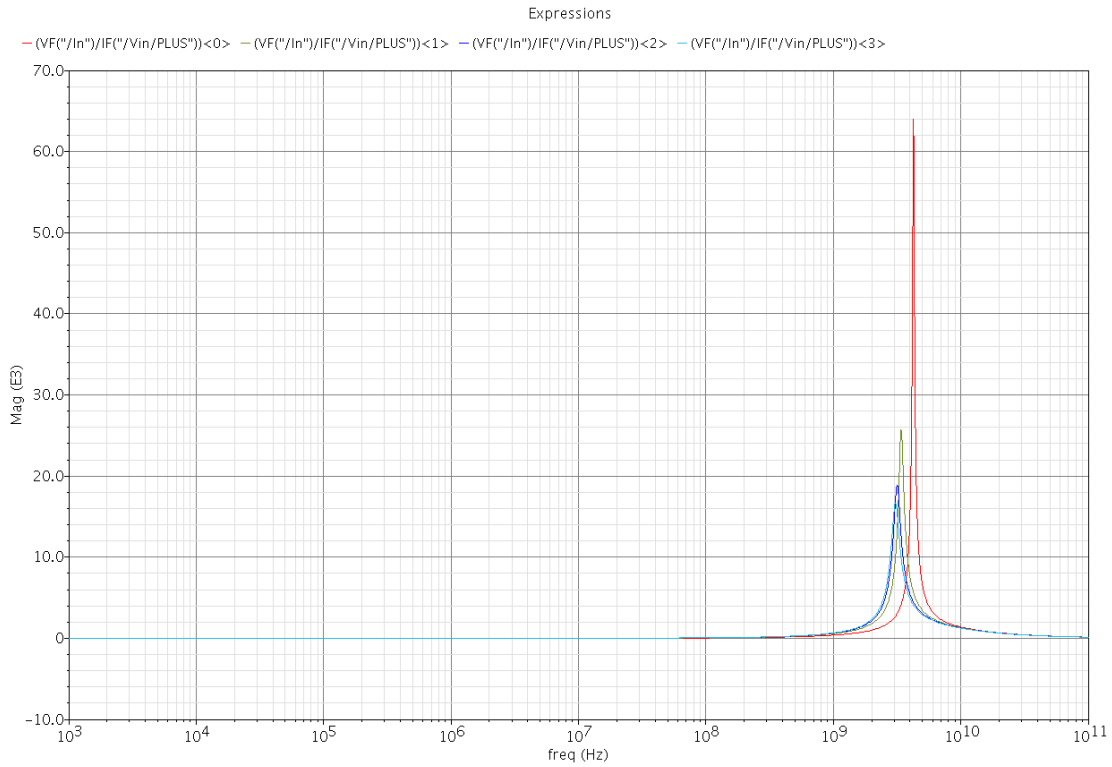

Figure 5.4 – Final simulation results for even higher Q- factors.

Through a substancial reduction of W_3, setting $W_3 = 0.35\ \mu m$, and ensuring $I_{B2} = 22.356\ \mu A$, it is possible to confirm the oscillation of the circuit.

Moreover, the oscillation frequency is now 4.1 GHz (figure 5.5), phase noise is -86 dBc/Hz at the offset of 10 MHz.

One may notice that the power consumption of this oscillator is 56.42 μW only.

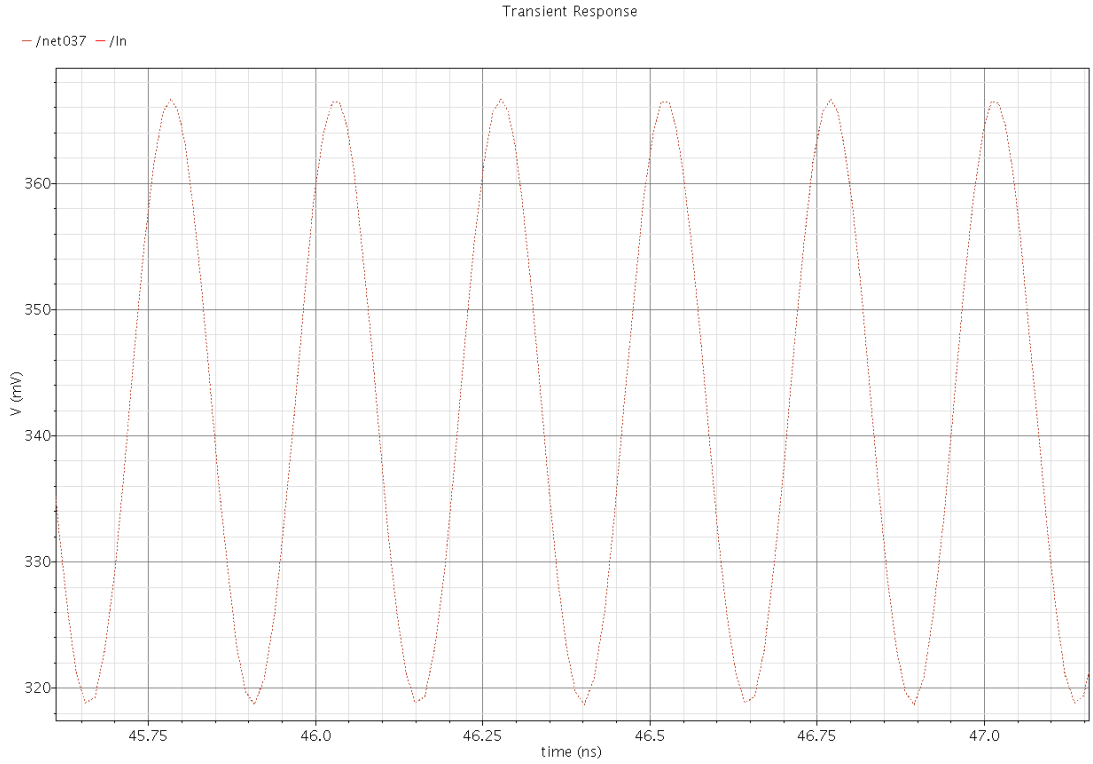

Figure 5.5 - Simulation results for the oscillator with oscillator frequency $f_p = 4.1\ GHz$.

Next, Figure 5.6 shows the value of the phase noise of the aforementioned oscillator at the offset of 10 MHz.

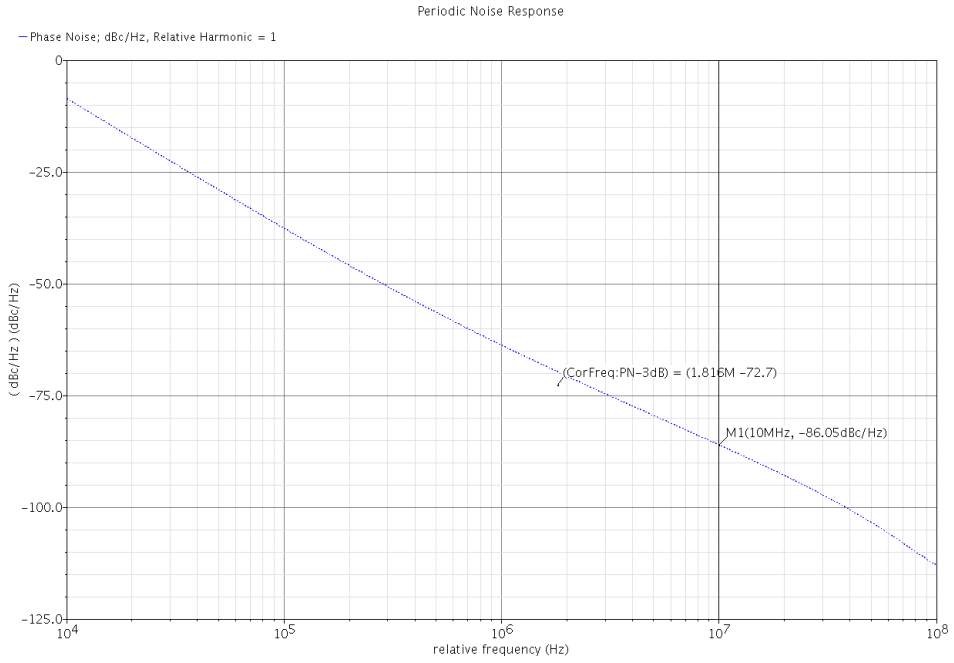

Figure 5.6 – Phase noise at the offset of 10 MHz.

Table 18 compares the performance of the proposed circuit with recent state of the art circuits in literature, using the conventional figure-of-merit (FOM) expressed in Equation 5.1 [Oli, 2010].

$$FOM = \mathcal{L}_{\text{measured}} - 10\log\left(\left(\frac{\Delta f}{f}\right)\left(\frac{P_{DC}}{1\ mW}\right)\right) \quad (5.1)$$

where P_{DC} is the power consumption.

Taking into account not only the phase noise value of the aforementioned oscillator at the offset of 10 MHz, but also the power consumption and the examples of realizations for 662 MHz to 4.1 GHz previously discussed, it is possible to calculate the FOM of the present oscillator.

$$\text{FOM}_{\text{present oscillator}} = -86\ (\text{dBc/Hz}) - 10\log\left(\left(\frac{10\ \text{MHz}}{4.1\ \text{GHz}}\right)\left(\frac{56.4\ \mu\text{W}}{1\ \text{mW}}\right)\right)$$

This means that $\text{FOM}_{\text{present oscillator}}$ is $-151\ \text{dBc/Hz}$.

Table 18 – Comparison of state-of-the-art inductorless oscillators.

References	**Technology**	$\mathbf{f_{min}}-\mathbf{f_{min}}\mathbf{(GHz)}$	$\mathcal{L}(\Delta f)$ (dBc/Hz)	**Power (mW)**	**IQ**	**FOM (dBc /Hz)**
[Dai, 2007]	0.35	$0.9 - 0.97$	-117 @ 1 MHz	79.2	YES	-158
[Tan, 2002]	BiCMOS 30 GHz	$9.8 - 11.5$	-94.3 @ 2 MHz	75	YES	-154
[Gro, 2003]	0.18	$0.1 - 3.52$	-106 @ 4 MHz	16.2	YES	-153
[Oli, 2009]	SiGe 0.25	$5 - 6$	114 @ 10 MHz	20	YES	-154
[Fer, 2009]	0.35	$2.3 - 2.5$	-105 @ 1 MHz	48	YES	-155
[Fil, 2009]	0.18	$5.6 - 6.3$	-97 @ 1 MHz	36	YES	-154
[Par, 2009]	0.13	$2.2 - 2.8$	-95.4 @ 1 MHz	2.86	NO	-159
[Par, 1999]	0.6	$0.75 - 1.2$	-117 @ 0.6 MHz	30	NO	-166
[Bad, 2004]	0.18	$0.65 - 1.04$	-116.5 @ 0.6 MHz	18.95	NO	-167
[Kia, 2004]	0.18	$0.55 - 0.76$	-109.6 @ 0.6 MHz	15.35	NO	-159
This work	0.13	$0.66 - 4.1$	-86 @ 10 MHz	0.06	NO	-151

The proposed oscillator is similar to those of other state-of-the-art RC oscillators, because of its ultra-low power.

Regardless the high value of the phase noise of the aforementioned oscillator, it is important to mention another consideration.

Taking into account the context of biomedical applications where the proposed oscillator falls, the main focus relies on power consumption.

Moreover, it has the advantage of having significant tuning range, since the transistors are most of the time operating in weak inversion.

Chapter 6. Conclusions and Future Work

6.1 Conclusions

Regardless the fact that the most relevant conclusions related to the simulation results have been already detailed in chapter four, in order to emphasize the most relevant conclusions, it will be synthetized the most important results obtained.

In this dissertation we have presented an inductorless wideband MOSFET-only RF Non-Gyrator Type of Active Inductors with low area, low cost, and very low power, capable of covering the whole WMTS, and ISM, band and intended for biomedical applications.

This model, based on Active Inductors (AI) takes advantage of the $130\,nm$ MOS technology to optimize the control of the quality factor. In this sense, the proposed AIs can behave as a parallel RLC Oscillator, and examples of realizations for 662 MHz to 4.1 GHz range are given. A 1.2 V power source, supply the circuit with 56.4 μW at the maximum oscillation frequency. Moreover, with this results, it is possible to confirm that the circuit prototype designed validate the proposed approach, in which obtain a Q of 235.8 at the frequency previously discussed.

It was also confirmed a substantial discrepancy between theoretical values and the simulated results obtained. This difference is due to the fact that transistors are operating in weak inversion.

Since the beginning of the theoretical study that the aforementioned difference was expected, that is, all the design process was based on equations related to strong inversion regime.

To emphasize the discrepancies, it is important to mention that in order to obtain a frequency center approximately of 600 MHz and 5 GHz, it was necessary to perform a theoretical study that pointed to $f_p = 904.4\,MHz$ and $\mathrm{f_p} = 11.5\,GHz$ respectively.

The present work led to conclude that the addition of transistor M_3 is absolutely determinant to increase significantly the quality factor.

In fact, the investigation of the relation between the increase of the current I_{B2} and the reduction of W_3, it was concluded that this strategy led to even higher Q-factors.

6.2 Future Work

In terms of future work, the optimization of the value of the current source I_{B2} might be an interesting starting point.

Although the compensation results in a low power inductor-less oscillator and examples of realization for 662 MHz to 4.1 GHz range are given, it is a fact that the value of the second current source should be reduced.

Another possible future work, can be related to a more thorough study in regard to the theoretical assumptions concerning the behaviour of this particular circuit.

Since transistors are operating in weak inversion, it will be a challenging task, since its equations are extraordinarily complex.

Regardless this consideration, it is crucial to highlight the fact that even without correct theory, the proposed active inductors can be successfully used in wideband amplifiers and oscillators.

Another possible future project could focus on reducing power consumption, through the use of modern CMOS technology $65\ nm$ and$28\ nm$.

Finally, a possible future project can be related to the realization of the layout of the present circuit in order to validate the results and circuit performance by fabrication and testing of the circuit.

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