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Licenciatura em Ciências da Engenharia Electroctécnica e de Computadores

Design of a Low-voltage CMOS RF Receiver for Energy Harvesting Sensor Node

Dissertação para obtenção do Grau de
Mestre em Engenharia Electrotécnica e de Computadores

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Setembro, 2014

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Dedicated to my lovely family

Acknowledgements

The acknowledgment is a delicate section that requires special attention in the writing, mainly because it sums up the importance that some people have had in my academic path. In case I forget to mention anyone important, I assure that I remember all the help was given to me.

I would like to express my appreciation to the Department of Electrical Engineering of the Faculty of Sciences and Technologies for their excellent teaching standards, which allow their students to acquire a broad knowledge and experience in various areas of the course under an enriching, friendly and knowledgeable guidance. To the teachers Prof. Luís Oliveira, Prof. João Pedro Oliveira and Prof. João Carlos Goes that have influenced my final course path leading me to choose the area of electronics, in particular the RF circuit design area, I want to thank for making electronics a captivating world. My advisor, Prof. Luís Oliveira, deserves a special mention, since he has always shown commitment, dedication and motivation in helping, which was a fundamental contribution during this work. I also would like to thank for the guidance and help of Prof. Fortunato Carlos Dualibe from Faculté Polytechnique (UMOS) in Belgium, it was certainly essential in the course of my work.

I also wanted to express my appreciation for the friendly environment, the companionship and helpful assistance of my colleagues from lab 3.5. I mention my boyfriend and working partner Nuno Mancelos, with whom I share fond memories since the first day of college and in recent years have shared success and frustrations.

Finally, but not less important, I'm thankful to my family for their patience and perseverance over the years, the remarkable environment and good support they have provided me. They were often deprived of my presence in various circumstances and yet continued to be my pillars in this sometimes frustrating path. With all this, I dedicate this work to my family, knowing that without their support it would be more difficult.

Abstract

In this thesis a CMOS low-power and low-voltage RF receiver front-end is presented. The main objective is to design this RF receiver so that it can be powered by a piezoelectric energy harvesting power source, included in a Wireless Sensor Node application. For this type of applications the major requirements are: the low-power and low-voltage operation, the reduced area and cost and the simplicity of the architecture. The system key blocks are the LNA and the mixer, which are studied and optimized with greater detail, achieving a good linearity, a wideband operation and a reduced introduction of noise.

A wideband balun LNA with noise and distortion cancelling is designed to work at a 0.6 V supply voltage, in conjunction with a double-balanced passive mixer and subsequent TIA block. The passive mixer operates in current mode, allowing a minimal introduction of voltage noise and a good linearity.

The receiver analog front-end has a total voltage conversion gain of 31.5 dB, a 0.1 - 4.3 GHz bandwidth, an IIP_3 value of -1.35 dBm, and a noise figure lower than 9 dB. The total power consumption is 1.9 mW and the die area is 305x134.5 μm^2, using a standard 130 nm CMOS technology.

Keywords: CMOS RF receiver front-end; Low-power ; Low-voltage; Wideband balun LNA; Double-balanced passive Mixer; Wireless Sensor Networks.

Resumo

Nesta tese é projectado o front-end analógico de um receptor RF CMOS com baixo consumo e baixa tensão de alimentação. O receptor é projectado com o intuito de ser incluído num nó sensor, alimentado por uma fonte de alimentação baseada em energy harvesting piezoeléctrico. Os requisitos mais importantes das aplicações wireless deste tipo de nós sensores prendem-se com o baixo consumo e baixa tensão de alimentação, a redução de área e custo e a simplicidade da arquitectura. Os blocos mais importantes do receptor são o LNA e o misturador, estudados e optimizados com maior detalhe de forma a alcançar boa linearidade e reduzida introdução de ruído.

A implementação do receptor inclui um LNA wideband balun, com capacidade de cancelamento de ruído e distorção. O LNA é projectado para funcionar com uma tensão de alimentação de 0,6 V, juntamente com um misturador passivo e amplificador de transimpedância. O misturador passivo opera em modo corrente, garantindo uma boa linearidade e uma reduzida introdução de ruído.

O ganho de conversão total do receptor é 31,5 dB, a sua largura de banda é 0,1 – 4,3 GHz, o seu valor de IIP_3 é -1,35 dBm, e a sua figura de ruído é inferior a 9 dB. O consumo total é de 1,9 mW e a área ocupada pelo circuito é 305x134.5 μm^2, usando uma tecnologia standard CMOS de 130 nm.

Palavras-chave: Receptor RF CMOS; Baixo consumo; Baixa tensão; LNA wideband balun; Mixer passivo.

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Abbreviations

AC	**A**lternating **C**urrent
ADC	**A**nalog to **D**igital **C**onverter
BER	**B**it **E**rror **R**ate
BW	**B**and**W**idth
CG	**C**ommon-**G**ate
CL	**C**onversional **L**oss
CMOS	**C**omplementary **M**etal-**O**xide-**S**emicondutor
CS	**C**ommon-**S**ource
DC	**D**irect **C**urrent
DRC	**D**esign **R**ule **C**heck
DTMOS	**D**ynamic **T**hreshold **MOS**
FET	**F**ield **E**ffect **T**ransistor
FoM	**F**igure of **M**erit
FSK	**F**requency **S**hift **K**eying
HR	**H**igh-**R**esistance
IC	**I**ntegrated **C**ircuit
IF	**I**ntermediate **F**requency
IIP	**I**nput Reference **I**ntercept **P**oint
KVL	**K**irchhoff's **V**oltage **L**aw
LDO	**L**ow-**D**rop**O**ut
LNA	**L**ow **N**oise **A**mplifier

LO	**L**ocal **O**scillator
LPE	**L**ayout **P**arameter **E**xtraction
LPF	**L**ow-**P**ass **F**ilter
LVS	**L**ayout **V**ersus **S**hematic
MIM	**M**etal-**I**nsulator-**M**etal
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
NEF	**N**oise **E**xcess **F**actor
NF	**N**oise **F**igure
NMOS	**N**channel **M**etal-**O**xide-**S**emicondutor
OOK	**O**n/**O**ff **K**eying
OTA	**O**perational **T**ransconductance **A**mplifier
PMOS	**P**channel **M**etal-**O**xide-**S**emicondutor
PSSR	**P**ower **S**upply **R**ejection **R**atio
PWM	**P**ulse **W**idth **M**odulation
Q	**Q**uality factor
RF	**R**adio **F**requency
RMS	**R**oot-**m**ean-**s**quare
SC	**S**witched **C**apacitor
SNR	**S**ignal-to-**N**oise **R**atio
SoC	**S**ystem-on-**C**hip
TIA	**T**rans**I**mpedance **A**mplifier
VCVS	**V**oltage **C**ontrolled **C**urrent **S**ource
VDD	**V**alue-**D**riven **D**esign
WSAN	**W**ireless **S**ensor **A**ctuator **N**odes
WSN	**W**ireless **S**ensor **N**etwork

1

Introduction

1.1 Background and Motivation

Integrated circuits (ICs) have been experiencing a remarkable progress in terms of device size reduction, range of operation frequencies and overall performance. The most influential factor was the advent of the field-effect transistor (FET), which operates as a conducting semiconductor channel, responsible for the flow of charge carriers in the channel. The FET is a voltage-controlled device with four terminals: the source (S), the drain (D), the gate (G) and the bulk (B). The channel is formed between the terminals S and D. While, the terminal G modulates the channel conductivity, controlling the density of charges carriers in the channel. The terminal B allows a connecting to the device's substrate [1–3].

The dominant type of transistor in today's integrated circuits is the metal-oxide-semiconductor field-effect transistor (MOSFET). These transistors offer a dense integration of the circuits in terms of the number of transistors per unit area of silicon substrate, a low cost of fabrication, an improvement in the overall performance and a low power consumption. The CMOS technology is growing towards to integration of digital blocks, analog and RF circuits on a single chip to implement the so called system-on-chip (SoC) solutions [1–3].

So, in order to originate a Wireless Sensor Networks (WSNs), several individual sensor nodes, Wireless Sensor Actuator Nodes (WSAN), are energetically autonomous and wirelessly interconnected. These WSANs share information through the communication channel, where the commands are transmitted through their radio transceivers by modulating the different characteristics of the radio frequency (RF) signal. The transceivers are responsible for connecting individual nodes of the network because of their function

of receiving and transmitting information, allowing the WSN to be formed. The main blocks of the transceiver are the transmitter and the receiver.

In the transmitter side, the information suffers a process called modulation, where the signal goes through several changes as it passes from baseband to higher frequency. This process makes the wave carry more information and also helps reducing the size of the antennas. In addition, other important matter for the wireless sensor is in the way the signal propagates by the communication channel. This channel causes attenuation in the transmitted RF signal during propagation. The attenuated RF signal must be amplified by the receiver, which is also responsible for filtering eventual interferences. After amplification, the receiver converts the input signal to baseband, in order to demodulate and access the original information [4].

Moreover, the wireless sensor node installation depends on their characteristics and communication range, which influences the total circuit area. Also, these nodes should be energetically autonomous and individually powered. A common solution to make these nodes energetically autonomous is the use of batteries. Although it guarantees the node's wireless operation, this type of power solution has limited energy supply, requiring periodical maintenance.

In an ideal situation, the wireless sensor node should operate with low power consumption, where the node is self-sufficient in terms of energy, or self-powered. The possibility of making the node autonomous, maintenance-free and unattended is feasible by energy harvesting. This type of energy solution makes use of residual energy that is present in the different enviroments where the WSANs are installed. This residual energy is present in different forms and has numerous sources, mainly solar, thermal gradient, electromagnetic or electromechanical. So the energy harvesting faces the challenge of scavenging and converting enough residual energy to power different circuits [5].

The scope of this work is to design and implement, through CMOS technology, a low power consumption front-end RF receiver, enabling to be powered by an energy harvesting power supply. The included RF receiver blocks are the LNA, mixer, local oscillator (LO) and the transimpedance amplifier (TIA). However, the main focus is over the new implementation of LNA and mixer combination, where the signals are treated in current mode. This approach plays an important role in the present work, which verifies if the considerations made on each block are sufficient to validate the main objectives.

1.2 Thesis Organization

Besides the introductory chapter, this thesis has been organized in five chapters as will be presented:

In **chapter 2**, the state-of-the-art is presented, which means the information is gathered about the architectures, devices, processes and techniques that are applied to RF receivers front-end. Some RF receiver topologies and characteristics are briefly described. Also, some basic concepts are introduced, the scattering parameters, the noise and the

linearity. The LNA and mixer topologies are presented and discussed, making a distinction between narrowband and wideband LNAs and active and passive mixers.

Chapter 3 presents the main attributes of the LNA, mixer and complete receiver of this work, including the analysis of the most relevant equation for each of them. The main characteristics of the LNA module are specified, and the changes made to the original LNA are presented. The deduction of the main equations regarding the LNA is given, namely the differential voltage gain, the input impedance and noise factor. The mixer design includes the development strategies that were considered in order to enable this module to perform the mixing operation in current mode. At the end of the chapter, the design of the complete receiver circuit is demonstrated, including the deduction of the conversion gain equation and some important characteristics.

Chapter 4 presents the dimensioning of the proposed receiver circuit, as well as the schematic and post-layout simulations. The implementation procedures used to dimension the receiver circuit before the layout are summarized and the initial values and parameters are given. Also, this chapter gives focus to the LNA block because of its importance and influence on the final results of the entire proposed circuit. The theoretical expressions and characteristics obtained in the previous chapter are combined and validated through simulation results and thus a comparison with state-of-art LNAs is made. Before the circuit layout, the transistor dimensions are optimized for the receiver circuit, with its behaviour and performance analysed through the simulation results. Then, the circuit layout is produced, and post-layout simulations are performed, enabling the comparison of the schematic and layout simulation results. Finally, the discussion of results is made and it is verified if the circuit satisfies the requirements for the target application.

Chapter 5 gives the general conclusions and further research suggestions.

1.3 Contributions

The main contributions of this thesis are as follows.

There are several low voltage techniques responsible for the functioning of the circuits at low voltage, lower than 0.7 V. The technique explored in this thesis was the dynamic threshold MOS (DTMOS), which is applied on the first block of the RF receiver front-end and takes into account the transistors choice in which the technique should be used. However, before using this technique of low voltage in the proposed receiver of the thesis, it was explored and studied in a two-stages rail-to-rail input/output, constant G_m amplifier. This work was submitted to the **DoCEIS**, **5th Doctoral Conference on Computing, Electrical and Industrial Systems**, entitled "*Stability improvements in a Rail-to-Rail Input/Output, constant G_m Operational Amplifier, at 0.4 V operation, using the low-voltage DTMOS technique*" [6].

Another article was submitted to **DoCEIS**, **5th Doctoral Conference on Computing, Electrical and Industrial Systems**, with the title "*Piezoelectric energy harvester for a CMOS*

wireless sensor" [7], where the concept of energy between wireless sensor nodes and energy harvesting is explored. Therefore, this technique of energy harvesting is promising in collecting the residual energy present in diversified environments and forms, giving special emphasis to the piezoelectric energy harvesting. Also, it presents a range of WSAN with different functionalities, characteristics and estimated power consumption levels. A study and experimental evaluation of a flexible piezoelectric material is made to validate the use of a piezoelectric harvester in a CMOS WSAN. This work has lead to the conclusion of the requirements for the energy harvesting solution in the proposed receiver of this thesis, which are low-voltage supply and low-power consumption.

The RF receiver design has a wideband balun LNA with noise cancelling and a passive mixer. The combination of these two blocks treats the signals in current mode, enabled by the local oscillator (LO). The TIA is placed after the mixer module, and is responsible for converting the current signal to a voltage signal. The proposed receiver circuit is designed in 130 nm CMOS technology and its requirements present a suitable solution for the target application. This work also presents the theoretical analysis, the key parameters, some characteristics and simulations results. This work was submitted to the **MIXDES**, **21th International Conference (2014)**, entitled "*A Low-Voltage LNA and Current Mode Mixer Design for Energy Harvesting Sensor Node*" [8].

An extended version, entitled "*Co-design of a Low-power RF Receiver and Piezoelectric Energy Harvesting Power Supply for a Wireless Sensor Node*" was published in the **International Journal of Microelectronics and Computer Science**. In the extended version, the previous work of a low-voltage RF CMOS receiver front-end is presented in conjunction with a piezoelectric energy harvesting power circuit for a wireless sensor node solution. The energy harvesting power circuit is composed by an active full-bridge cross-coupled rectifier and a low-dropout (LDO) regulator [9].

2

Receiver architectures and RF Blocks

In this chapter, the supply and support for theoretical analysis and design of front-end RF circuits, mainly in the receiver's side, is presented. In section 2.1, an overview of the three main conventional receiver architectures, namely, heterodyne, homodyne and low-IF, is offered, including some advantages and disadvantages, characteristics and conclusions.

Section 2.2 presents the importance of impedance matching on RF circuits and the necessary requirements for maximize the energy transferred between blocks. The section 2.3 focus in the scattering parameters, which relates the electromagnetic waves incident and reflected . In section 2.4, a common noise sources overview is given, namely, thermal noise, flicker noise and noise figure. The section 2.5 gives an overall notion of the most important characteristics of linearity measurement and presents the 1 db linearity compression point and third-order intermodulation product.

The typical structures and important front-end blocks are introduced in sections 2.6 and 2.7. In the case of section 2.6, the main focus is given in the narrowband and wideband LNAs topologies. While, in section 2.7 is emphasized the differences and characteristics of active and passive mixers.

2.1 Receiver Architectures

To understand the rules that prevail when designing receiver for WSN, was chosen deepen the knowledge about these structures. The receiver's architectures are used to fulfil processes such as amplification and down-conversion of the signal. Also nowadays, their requirements are more demanding in terms of interference rejection, band selectivity, full integration and dimensions. This section emphasizes three receiver types, describes some of their characteristics, advantages and disadvantages.

2.1.1 Heterodyne Receiver

The Wireless Sensor Networks (WSNs) have used for a long time heterodyne receiver topology, shown in Fig. 2.1. The RF signal from the transmitter is received by the antenna and filtered through a baseband filter, which removes the unwanted frequencies. Also, the received signal is weak and needs to be amplified by the Low Noise Amplifier (LNA). Then, other filter is applied to the signal, the image rejection filter, his function is attenuate signals at image band frequencies from the LNA. The down-converted process places the signal frequency to an intermediate frequency (IF), which is done through the signal multiplier (mixer) that is applied by the output signal of the Local Oscillator (LO). At the multiplier output is used another baseband filter, the channel selection filter, that isolates the desired signal from the others adjacent IF signals from nearby channels. In this receiver topology, the blocks responsible for the demodulation process are the Analog to Digital Converter (ADC) and the digital signal processor.

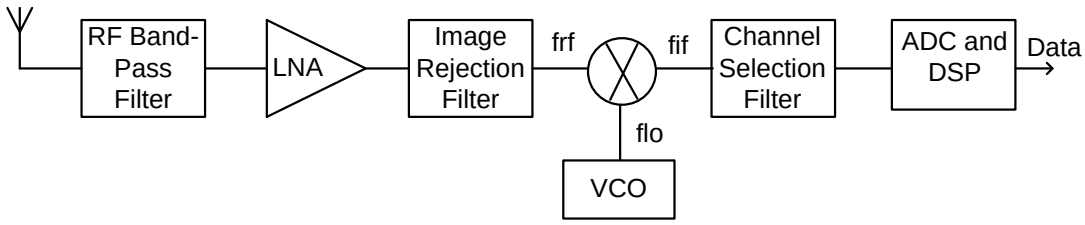


Figure 2.1: Heterodyne Receiver

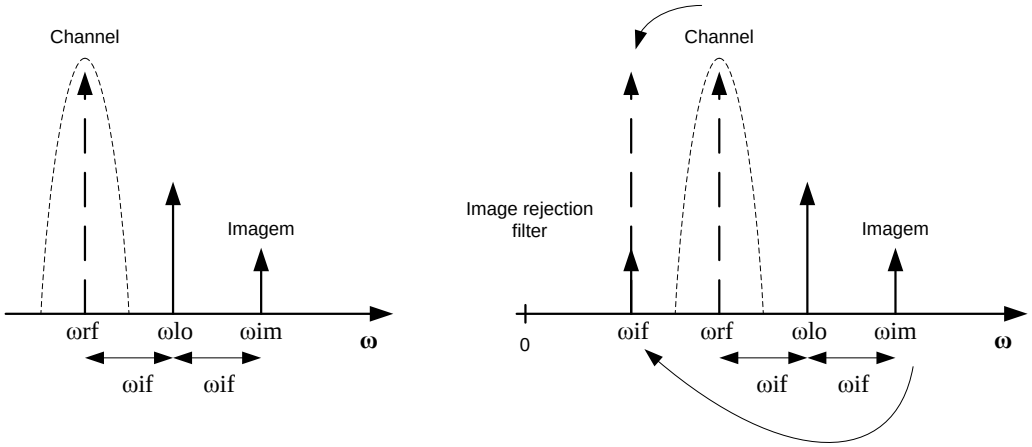


Figure 2.2: Image rejection

The frequency image problem occurs when the input mixer has a resultant signal called signal image, which after the multiplications generates two signals at the output mixer. Unfortunately, one of them coincides with the intermediate frequency (IF) causing an overlap in the interest signal, which makes impossible separate both. That's why is necessary to have before the multiplier a filter called image rejection filter, show in

Fig. 2.2.

A further disadvantage associated with the choice of IF frequency value is caused by its increase. With the highest IF frequency becomes easier to develop the filter that rejects the image (image rejection filter), because the image became farther from the desired frequency. On the other hand, this architecture has a compromise between the quality factor (Q) and the Intermediate Frequency (IF). What makes the specifications for the channel selection filter more difficult to realize on-chip [4, 10, 11].

2.1.2 Homodyne Receiver

The homodyne receiver (Fig. 2.3) known by other names such as direct conversion and Zero-IF receiver, converts the Radio Frequency (RF) signal to baseband. This conversion is done using a Local Oscillator (LO) with the same frequency as the RF signal. This receiver type has advantages compared with heterodyne receiver. First, the inexistence of image signal makes unnecessary the use of the image filter rejection. Second, the filter that performs the channel selection is done through a Low-Pass Filter (LPF), making the design and implementation simpler. Finally, it allows the possibility of complete integration of the receiver on-chip.

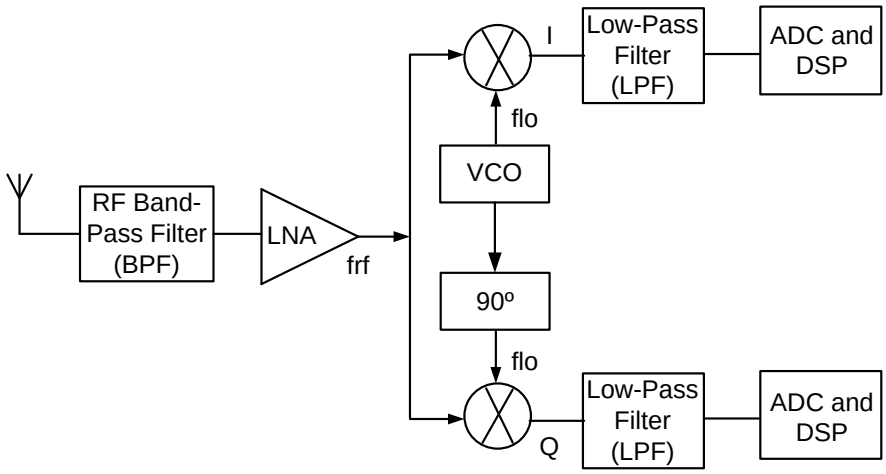


Figure 2.3: Homodyne Receiver

The direct converter architecture has some downsides:

- **Flicker Noise -** The Flicker noise can significantly corrupt the low frequency of the baseband signal, which is a big problem in CMOS implementations (1/f corner at low frequency).

- **LO leakage -** Local Oscillator (LO) leakage happens when the insulation is imperfect between the LO port and the input ports of the LNA and mixer. This leakage

signal appears when the LNA and mixer's inputs are mixed with the signal coming from LO, producing an unwanted DC component at the mixer output, which can cause the saturation of the following blocks. To minimize this effect is necessary the use of differential LO and mixer outputs to cancel common mode components.

- **DC offsets –** Since the down-converted band extends down to zero frequency, any offset voltage can corrupt the signal and saturate the receiver's baseband output stages. Hence, DC offset removal or cancellation is required in direct-conversion receivers.

- **Quadrature error and mismatches -** Quadrature error and mismatches between the amplitudes of the I and Q signals results in the corruption of the received signal constellation, which increase the Bit Error Rate (BER). The ideal baseband signals should have similar amplitude and phase difference of 90 degrees.

- **Intermodulation -** In the intermodulation, the receivers must have a high IIP_2 (second-order intermodulation intercept point) to avoid producing DC offset. [4, 10, 11]

2.1.3 Low-IF Receiver

The previous two architectures were useful once, but the combination of both advantages gave the Low-IF receiver. This receptor cancels the image frequency by using special mixing circuits that allows the selection of a low intermediate frequency. The problem that arises in the homodyne receiver is avoided by relaxing the quality factor of the channel selection filter, in particular the flicker noise that affects baseband signals.

The technique for cancellation of image signal is used to avoid the use of image rejection filter which is one of the problems associated with the heterodyne receiver. Cancellation of image is done through two architectures: Hartley and Weaver. This method of image rejection is achieved using the quadrature architectures, in which the image is suppressed by its negative replica.

The Hartley architecture has the block diagram represented in Fig. 2.4(a). The idea is to process the RF signal after the Low-Pass Filter (LPF) and combine both outputs into a single one. Assuming that the RF signal is represented by the expression 2.1, then after the filtering process the expressions are 2.2 and 2.3, respectively.

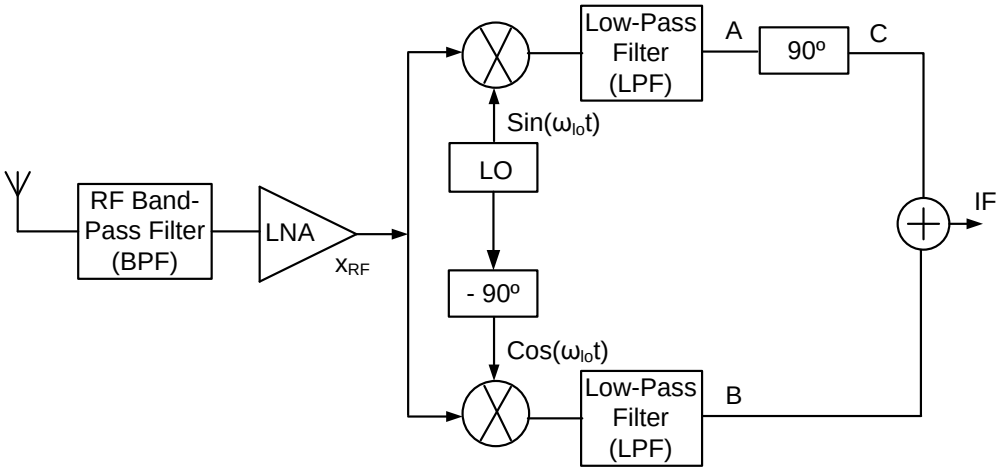
$$x_{RF}(t) = V_{RF}cos(\omega_{RF}t) + V_{IM}cos(\omega_{IM}t) \tag{2.1}$$

$$y_A(t) = \frac{V_{RF}}{2}sin[(\omega_{LO} - \omega_{RF})t] + \frac{V_{IM}}{2}sin[(\omega_{LO} - \omega_{IM})t] \tag{2.2}$$

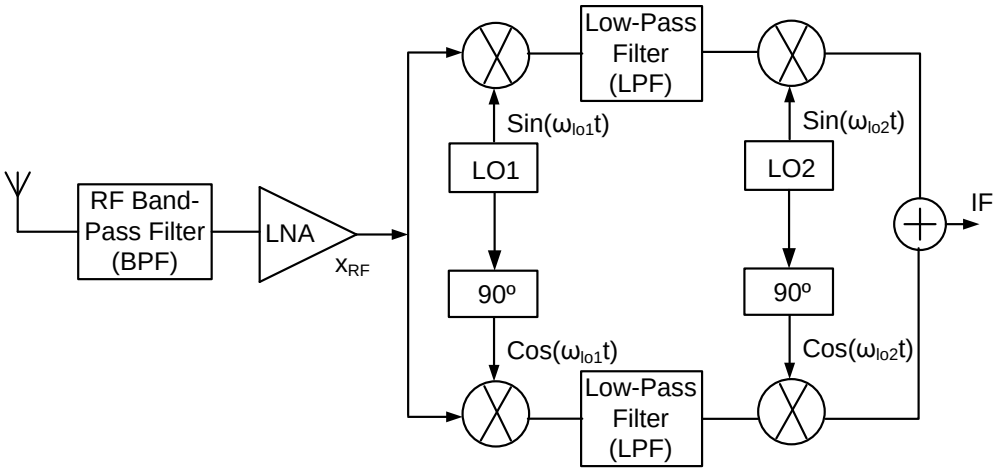
$$y_B(t) = \frac{V_{RF}}{2} cos[(\omega_{LO} - \omega_{RF})t] + \frac{V_{IM}}{2} cos[(\omega_{LO} - \omega_{IM})t] \tag{2.3}$$

Since sin(θ - $\frac{\pi}{2}$)= -cos(θ), after a 90^{o} shift, the signal at C is,

$$y_C(t) = \frac{V_{RF}}{2} cos[(\omega_{RF} - \omega_{LO})t] - \frac{V_{IM}}{2} cos[(\omega_{LO} - \omega_{IM})t] \tag{2.4}$$



(a) Hartley



(b) Weaver

Figure 2.4: Image rejection architectures

Finally, by adding the expressions 2.3 and 2.4 the wanted signal is recovered and the image is suppressed.

Lastly, the Weaver architecture, represented in Fig. 2.4(b),has similar results but it uses a second mixer stage at the intermediate frequency. Both architectures enabled the cancellation of image signal, which depend on the precision of the oscillators to produce quadrature signals. However, both solutions are susceptible to quadrature errors resulting phase and gain imbalances.

In conclusion, the Low-IF receiver becomes more flexible compared to the previous topologies [11].

2.2 Impedance matching

The transmission line is one of the main focus of a complex structure of an RF circuit. The signal that goes through the transmission line has to ensure that the impedance of output block is equal to the characteristic impedance of the next block. If is verified the mismatch of the impedances this originates a reflected voltage and current which reduces the transmitted energy between blocks. The voltage and current at any point along the line may be expressed as:

$$V(z) = V_i e^{-\gamma z} + V_r e^{\gamma z} \tag{2.5}$$

$$I(z) = I_i e^{-\gamma z} - I_r e^{\gamma z} \tag{2.6}$$

where the term $e^{-\gamma z}$ represents the wave propagation in the $z+$ direction and $e^{\gamma z}$ in the $z-$ direction. Also the terms V_i, V_r, I_i and I_r are the amplitudes voltages and currents of the incident and reflected waves, respectively. The expression γ represents the propagation constant with the resistance R that represents the conductor loss and the conductance G, which is the dielectric loss between the two conductors.

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.7}$$

The characteristic impedance of the transmission line is expressed by using the Ohm's law and the equations 2.5 and 2.6:

$$Z_0 = \frac{V_i}{I_i} = \frac{V_r}{I_r} = \frac{R + j\omega L}{\gamma} \tag{2.8}$$

While the load impedance is expressed as follows:

$$Z_L = \frac{V(0)}{I(0)} = \frac{V_i + V_r}{V_i - V_r} Z_0 \tag{2.9}$$

The reflection coefficient is the ratio between the normalized reflection and the incident waves of load impedance at the end of the transmission line:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.10}$$

The reflection coefficient is inexistent ($r_L = 0$) when the characteristic impedance is equal to the load impedance ($Z_L = Z_0$)), which maximizes the energy transferred between the blocks. As an example, for the RF systems the impedance matching is important because of the antenna and the first block, usually LNA, must coincide with an impedance of 50 Ω [12].

2.3 Scattering parameters

The traditional system characterization is done through two ways. At low frequencies, the system uses measurements of open and short-circuits to determine the admittance and hybrid parameters. While, at high frequencies, the methods used by the system at low frequencies are not possible because of the port voltages or currents measurements that include magnitude and phase of the travelling waves. Therefore, the s-parameters also called as scattering parameters, are used to characterize the inputs and outputs variables of systems working at high frequencies, in order to auxiliary the adaptation of impedance matching, to provide the maximum value gain, the input and the output impedance and even possible instabilities. The scattering parameters that relate the input and output of electromagnetic waves, are shown in the Fig. 2.5 below as a_1, b_1, b_2 and a_2, when the system is viewed as a diport. These waves are generated by the input and output ports from the diport who represents the system.

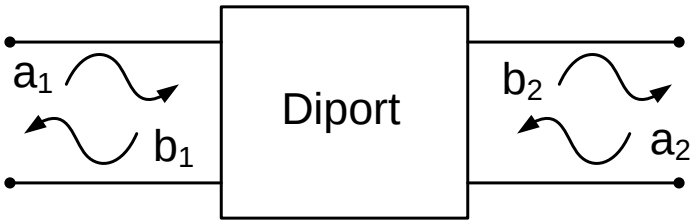


Figure 2.5: Diport with incident and reflected waves.

The s-parameters relate the electromagnetic waves as follows:

$$S_{11} = \frac{b_1}{a_1}(\text{com } a_2 = 0) \tag{2.11}$$

$$S_{12} = \frac{b_1}{a_2}(\text{com } a_1 = 0) \tag{2.12}$$

$$S_{21} = \frac{b_2}{a_1}(\text{com } a_2 = 0) \tag{2.13}$$

$$S_{22} = \frac{b_2}{a_2}(\text{com } a_1 = 0) \tag{2.14}$$

Therefore, the s-parameters have the following designation: the S_{11} is the input reflection coefficient, while S_{21} is the transmission gain since relates an output wave (b_2) to an input wave (a_1). The S_{12} corresponds to the reverse transmission gain considering the input and output diport swapped, which means the electromagnetic wave that enters on the diport is a_2 and not a_1. Finally, the last s-parameter is S_{22}, the output reflection coefficient.

The calculations of the s-parameters are made relating the terms of incident and reflected voltages of electromagnetic waves a_1, a_2, b_1 and b_2, , enabling the development of

design circuit without internal detailed knowledge [12].

2.4 Noise

Noise is one of the most important parameters in analog design more precisely, in RF circuits. This parameter is responsible for the degradation of circuit performance and its appearance is caused by external interference or by the intrinsic nature of the circuit materials. Due to its random behaviour and difficult prediction which mean that unwanted signals are added to the desired signal, therefore it is necessary to find an approach to minimize this effect. This section will describe the common sources of noise present in CMOS technologies [13].

2.4.1 Thermal Noise

The thermal noise depends on the temperature that causes variation in the resulting current, which is generated by the random motion of electrons that pass through the ohmic resistance devices. As the temperature of the device increases, the random motion of the molecules increase, and so does the corresponding noise level; therefore, it is known as thermal noise. The average noise power remains nearly independent of frequency and can be adequately approximated as

$$\overline{V_n^2} = 4KTR\Delta f \tag{2.15}$$

where the absolute temperature T (in Kelvin), the Boltzmann constant K and the bandwidth of the system is Δf. This can be quantified by a series voltage source using the Thevenin equivalent, or by a parallel current using the Norton equivalent [3, 13].

The thermal noise also appears in MOS transistors due to the carrier motion through the channel and is represented as shown in Fig. 2.6 by a parallel current source to the conduction channel.

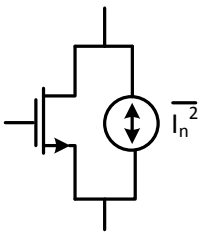


Figure 2.6: Thermal noise represented in MOS transistors.

The equations of thermal noise are defined depending on the region of the transistor. If the transistor is operating in the triode region ($g_{d0} >> g_m$), the g_{d0} is the drain-source conductance for $V_{ds} = 0$ and γ is the Noise Excess Factor (NEF). If it is in the saturation

region ($g_m >> g_{d0}$), the transistor operates in a long channel with the value $\gamma = 2/3$ [2, 13].

$$\overline{I_n^2} = 4KT\gamma g_m \Delta f \tag{2.16}$$

2.4.2 Flicker Noise

The flicker noise or 1/f noise is a low-frequency noise resulted by the surface and gate effects in the semi-conductor material, which means by the interface between the gate oxide (SiO_2) and the silicon substrate (Si). The measured noise power in MOSFET devices has a dependence on the gate bias and the oxide thickness. The flicker noise equation that is represented in 2.17,has parameters like the process dependent constant (k_f), the gate oxide capacitance per unit area (c_{ox}), the width (W) and length (L) of the transistor.

$$\overline{V_n f^2} = \frac{k_f}{c_{ox} W L f^{\alpha f}} \tag{2.17}$$

This type of noise becomes more crucial to provide enough dynamic range and better circuit performance [2, 14].

2.4.3 Noise figure

One of the most important parameter in an RF circuit is the noise factor (F), or the noise figure (NF), when calculated in dB. The noise factor represents the ratio of the total output noise and the input noise of the system. When is modelled as a diport, as represented in Fig. 2.7, in this case, the measurements are relative to the total noise power between the output, input and its gain for each frequency.

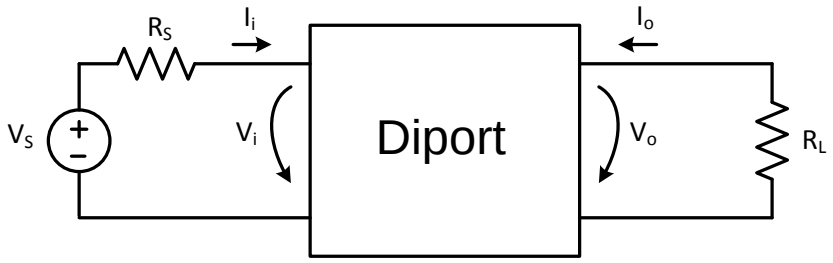


Figure 2.7: Noisy diport with gain A

The noise factor can be expressed by:

$$F = \frac{N_o}{A^2 N_i} \tag{2.18}$$

The noise factor can also be expressed as the power ratio between the desired signal to the total noise (unwanted signal), which is done through the ratio of signal-to-noise

ratio (SNR) at the input and at the output. This expression demonstrates how much the SNR degrades as the signal passes through the system [13].

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{2.19}$$

2.5 Linearity

The measurement of the RF system linearity is really important to understand the impact of nonlinear devices have in the output signal. The linearity can be characterized by the 1 dB compression point and by third-order intermodulation product.

The RF circuits are constituted by devices with nonlinear characteristics, such as MOS transistors, which in addition to this feature they are also memoryless, time invariant and can be represented by the Taylor series:

$$y(t) = a_0 + a_1 x(t) + a_2 x^2(t) + ... + a_n x^n(t) \tag{2.20}$$

Suppose a sinusoidal 2.21 as an input signal:

$$x(t) = Acos(\omega t) \tag{2.21}$$

The system response can be expressed by:

$$y(t) = a_0 + a_1 Acos(\omega t) + a_2 A^2 cos^2(\omega t) + a_3 A^3 cos^3(\omega t) \tag{2.22}$$

Nonlinear devices produce the same harmonic as the order of their nonlinearities with multiples of the fundamental frequency (nω). The order coefficients have different effects on the nonlinear devices. When is odd, the order coefficients have impact on the amplitude of the fundamental frequency, while in case of even order coefficients the impact is on the DC component.

In the case where two sinusoidal signals are applied at the nonlinear device input with different fundamental frequencies,

$$x(t) = Acos(\omega_1 t) + Bcos(\omega_2 t) \tag{2.23}$$

The intermodulation products emerge at the output signal as it is expressed in 2.24, which illustrates the operations between the input signal frequencies and their multiples of the fundamental frequency. The nonlinearity of order 3 (IM_3) is an example that the intermodulation product appearing in the frequency band of interest and can't be removed by a filter [1, 4, 13].

The intermodulation products are generated at the output signal, given by:

$$
\begin{aligned}
y(t) = {} & a_0 + a_1\Big(Acos(\omega_1 t) + Bcos(\omega_2 t)\Big) + \\
& a_2\left[\frac{A^2}{2}(1 + cos(2\omega_1 t)) + \frac{B^2}{2}(1 + cos(2\omega_2 t)) + AB(cos(\omega_1 + \omega_2)t) + cos((\omega_1 - \omega_2)t))\right] + \\
& a_3\left[(\frac{3}{4}A^3 + \frac{3}{2}AB^2)cos(\omega_1 t)) + (\frac{3}{4}B^3 + \frac{3}{2}BA^2)cos(\omega_2 t)) + \frac{3}{4}A^2B(cos(2\omega_1 + \omega_2)t) + \right. \\
& cos(2\omega_1 - \omega_2)t)) + \frac{3}{4}B^2A(cos(2\omega_2 + \omega_1)t) + cos(2\omega_2 - \omega_1)t)) + \frac{3}{4}A^3cos(3\omega_1 t) + \\
& \left.\frac{3}{4}B^3cos(3\omega_2 t)\right]
\end{aligned}
\tag{2.24}
$$

2.5.1 1 dB Compression Point

The 1 dB compression point is a linearity measure of the circuit and it's also known as gain compression or saturation. Their effect takes into account the gain of the circuit, the relation between the output and input power, by checking its linearity measure. Through the Fig. 2.8 can be seen the ideal linear characteristic with the real characteristic of the circuit over a limited range. However, its real characteristic begins to saturate, resulting in reduced gain. To check the circuit's linearity measure, the compression point 1 dB is defined through the difference of 1 dB from the ideal linear characteristic, this happens due to the increase of input power which makes the higher order harmonics more notable [1].

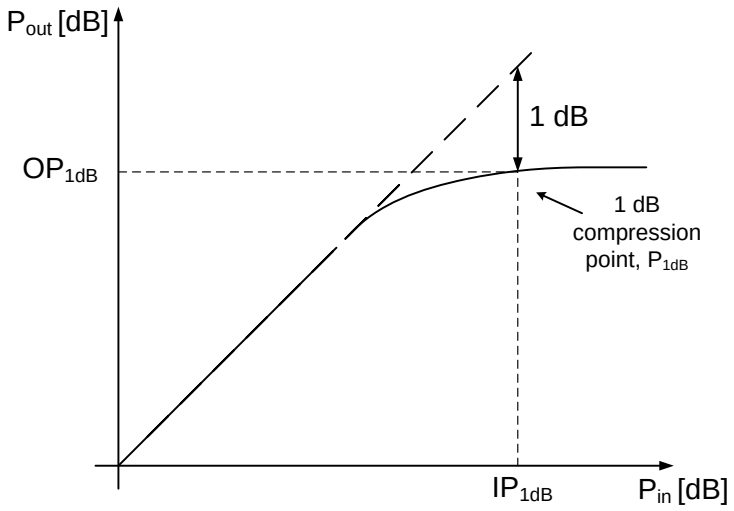


Figure 2.8: Definition of the 1 dB compression point

2.5.2 Third-order Intercept Point

The third-order intersection point, denoted as IP_3, is the intersection point where the hypothetical idealized responses of output power of the first-order and the intermodulation product of third-order intersect, typically at a point above the onset of compression. This third-order intersection point can be specified as either an input power level (IIP_3) or an output power level (OIP_3). This effect can be seen in Fig. 2.9, where the amplitude of the fundamental frequency would be equal to the amplitude of the intermodulation product of third-order.

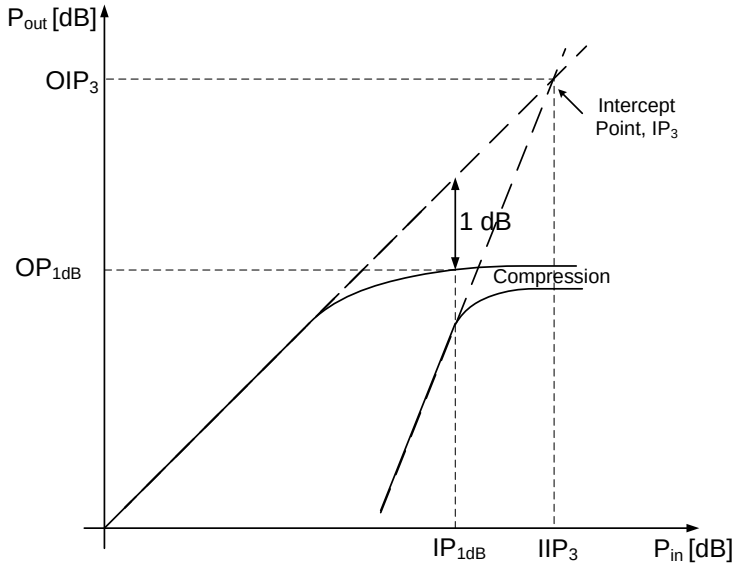


Figure 2.9: Definition of the third-order intercept point.

The point of third-order intercept (IP_3) occurs at a higher power level than the 1 dB compression point, being applied a practical rule that IP_3 is 10-15 dB greater than the 1 dB compression point [1, 4, 13].

2.6 Low Noise Amplifiers

This section aims to provide an overview of the main LNA topologies existing for the CMOS technology, giving focus to the bandwidth LNAs the narrowband and the wideband.

The LNA, Low Noise Amplifier, is an essential building block for receivers of wireless circuit. The signals received at the antennas of these circuits are very weak and must be amplified so that they can be handled. This amplification, however, must be done with care to reduce noise and amplify to the maximum the desired signal, as much as possible, this way the signal proceed to the rest of the circuit in the best possible conditions. Therefore, according to the Friis' formula, which shows the relation between the signal-to-noise ratio (SNR), the noise factor (F) of these circuits can be represented in cascade

stages:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_m - 1}{G_1 G_2 ... G_{m-1}} \tag{2.25}$$

where F_m and G_m are the noise factor and the available power gain of the n stage. Through the interpretation of the equation 2.25 is concluded that the noise factor of the first stage (LNA) is dominant, becoming essential to increase the gain to reduce the noise contribution in the following stages.

To maximize the gain has to ensure that the power transmission is maximized. This happens when there is not reflected wave either in the input or output of the LNA. In turn, the absence of reflection ensures the adaptation of the source impedance and the load impedance, which ensures optimal noise impedance. Another parameter which is represented by the cascade stages is the linearity that can be characterized by the following equation:

$$\frac{1}{IIP_3} = \frac{1}{IIP_{3,1}} + \frac{G_1}{IIP_{3,2}} + \frac{G_1 G_2}{IPP_{3,3}} \tag{2.26}$$

where IIP_3 and G are the input reference of the third-order intercept point, expressed in power, and the power gain of the m state respectively. From the analysis of the expression 2.26, the gain of the preceding stages affects directly the IIP_3 of the last stage, but a low noise figure demands a high gain for the first stage. This results in a trade off between noise and linearity [4, 10, 13].

2.6.1 Narrowband LNAs

The LNA function is add minimal noise of its own and be straight enough to withstand incoming interferers. Although various narrowband LNA topologies exist, the two topologies widely used are the common-source (CS) and common-gate (CG) LNA with inductive source-degeneration. The common-source (CS) LNA has good gain and noise figure, while the common-gate (CG) LNA has the advantage of broadband input impedance.

In any manner, the subsection will only focus in one of two topologies, as narrowband LNA example, in this case the common-source (CS), shown in Fig. 2.10 [10].

2.6.1.1 Common-Source LNA with Degenaration

For a common-source (CS) LNA with inductive source generation structure is easier to achieve input matching for the power gain and the noise figure.

The input impedance of the common-source (CS) LNA can be written as:

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs1}} + \frac{g_{m1}}{C_{gs1}} L_s \tag{2.27}$$

where C_{gs1} and g_{m1} are respectively the parasitic gate-to-source capacitance and L_s

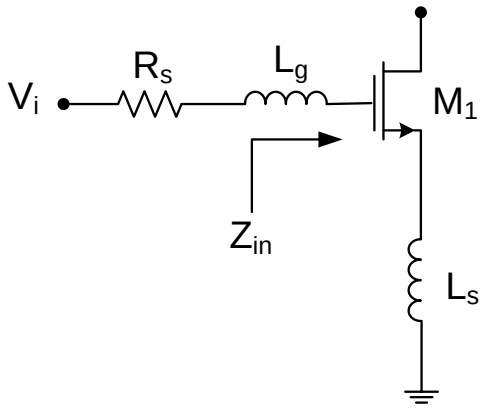


Figure 2.10: Degenerated common-source (CS) LNA topology

and L_g are the inductances of the transistor M_1. The input matching of the resonance frequency (ω_0) can be achieved by setting the real part of 2.27 to the source impedance (R_s) and the imaginary part to zero. The matching conditions are:

$$R_s = \frac{L_s g_{m1}}{C_{gs1}}, L_g + L_s = \frac{1}{{\omega_0}^2 C_{gs1}} \tag{2.28}$$

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs1}}} \tag{2.29}$$

The effective transconductance of the CS LNA stage neglecting the gate resistance is:

$$G_{m,CS} = \frac{\omega_T}{\omega_0 R_s (1 + \omega_T) L_s / R_s} \tag{2.30}$$

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}} \tag{2.31}$$

where ω_T is the transition frequency.

The expression 2.30 can be used approximately by the following expression for the voltage gain, assuming input matching.

$$|A_v| \approx \frac{R_L}{2\omega_0 L_s} \tag{2.32}$$

where R_L is the load resistance of the LNA.

In conclusion, this sort of narrowband LNA topology are good for the improvement of noise, but the use of the inductors becomes the die area larger which increases the production cost [10, 15, 16].

2.6.2 Wideband LNAs

There are various wideband LNA topologies; however, this subsection will give an overview of a common-gate (CG) with a resistance input matching and two types of Wideband

Balun LNAs: with resistors and a MOSFET-only.

2.6.2.1 Common-Gate with Resistive Input Matching

The common-gate (CG) LNA topology, shown in Fig. 2.11, is used as a wideband LNA and it has the simplest way to get a stable input impedance using a resistive input matching. Also, this topology has low power consumption as well as its compact size, being inductorless, allow portability and make it suitable for CMOS technology.

The input signal is applied to the source terminal and the output is collected at the drain. The resistor (R_D) is used for both biasing and current to voltage conversion at the output.

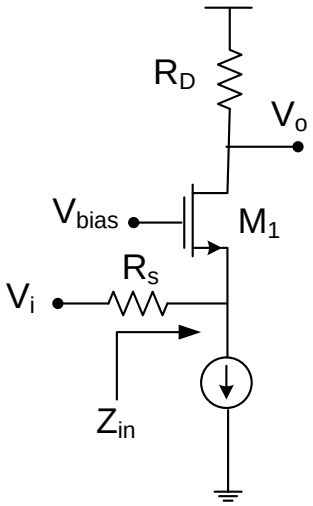


Figure 2.11: Common-gate LNA with resistive input matching

The common-gate (CG) voltage gain can be written as:

$$A_{cg} = (g_m + g_{mb})R_D \tag{2.33}$$

The input impedance can be calculated, if visualize from the source terminal, as:

$$Z_{in} = \frac{1}{(g_m + g_{mb})} \tag{2.34}$$

It can be seen in the expression 2.34 that the input impedance is typically resistive. However, CG amplifier has the disadvantage that it's imposed by the matching condition, since the total gain of the amplifier is dependent only on the load output. If the load output increases, causes a higher gain and a higher noise factor, which is usually 3 dB [17, 18].

2.6.2.2 Wideband Balun LNA with resistors

The Wideband Balun LNA with resistors represented in Fig. 2.12 has two stages: a common-gate (CG) and a common-source (CS) stage. This circuit has the functionality of balun

because in the entry of the LNA has a single-ended, unbalanced input, and delivers a balanced output.

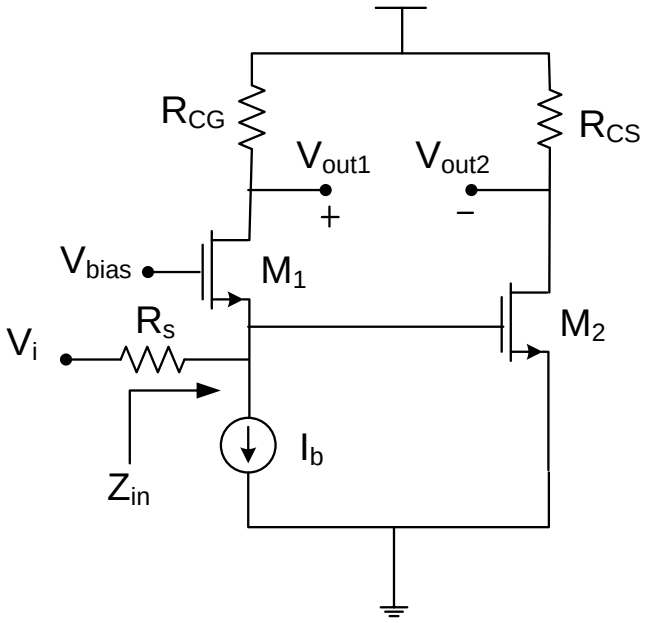


Figure 2.12: Wideband Balun LNA

The output is balanced since the magnitudes of the gains of the two stages are adjusted to an approximate value, because the common-source (CS) stage has the function of an inverter, while the common-gate (CG) isn't. Therefore, the differential voltage gain is taken between the drains of the two transistors and their expressions can be written as:

$$A_{Vout1} = (g_{m1} + g_{mb1} + g_{ds1})(r_{CG}//r_{ds1}) \tag{2.35}$$

$$A_{Vout2} = -g_{m2}(r_{CS}//r_{ds2}) \tag{2.36}$$

The differential gain is given by:

$$\begin{aligned} A_{vdiff} &= A_{Vout1} - A_{Vout2} \\ &= (g_{m1} + g_{mb1} + g_{ds1})(r_{CG}//r_{ds1}) + g_{m2}(r_{CS}//r_{ds2}) \end{aligned} \tag{2.37}$$

The approximate differential gain is then given by the expression

$$A_{vdiff} \approx g_{m1}(r_{CG}//r_{ds1}) + g_{m2}(r_{CS}//r_{ds2}) \tag{2.38}$$

The input impedance can be expressed as:

$$R_{in} = \frac{1 + g_{ds1}r_{CG}}{g_{m1} + g_{mb1} + g_{ds1}} \tag{2.39}$$

To cancel the noise contribution of the first stage, the common-gate (CG) stage, is possible as long as both of the stages have the same voltage gain. This happens because the first stage's noise appears as a common-mode signal at the differential output.

Therefore, the dimensioning of common-gate (CG) and common-source (CS) devices with different sizes and bias allows this circuit achieve the gain required in the common-source (CS) stage to cancel the distortion products of the common-gate (CG) stage. The gain required equals to the necessary obtained balancing, leading to the conclusion that is possible to have the output balancing abilities, the noise and distortion cancellation of common-gate (CG). This circuit can achieve very good linearity as long as the common-source (CS) stage's linearity is assured.

However, as shown in 2.40, the noise factor of the circuit is obtained from the influence of the noise power output of its elements and divided by the noise contribution of the signal source.

So, the different influences from the expression below are discriminated by the contributions of the common-gate (CG) transistor, common-source (CS) transistor and load resistance, which are represented by the second, the third and the last term of the expression, respectively [19].

$$F = 1+\frac{\gamma g_{mCG}(r_{CG} - r_S g_{mCS} r_{CS})^2}{r_s A_V^2}+\frac{\gamma g_{mCS} r_{CS}^2 (1 + g_{mCG} r_S)^2}{r_s A_V^2}+\frac{(r_{CG} + r_{CS})(1 + g_{mCG} r_S)^2}{r_s A_V^2} \tag{2.40}$$

Nonetheless, in order to achieve a low noise figure and simultaneously good output balancing. It's used a factor m in the CG transconductance and resistor (r_{CG}), which with the increasing of this factor (m), the CG transconductance becomes smaller than the CS transconductance and the CS resistor (r_{CS}) is m times smaller than the CG resistor (r_{CG}), thus: $g_{mCS} = m.g_{mCG}$ and $r_{CS} = r_{CG}/m$ [19, 20].

2.6.2.3 MOSFET-only Wideband Balun LNA

The MOSFET-only LNA circuit version is presented in Fig. 2.12. This version was based on Wideband Balun LNA with resistors, with the aim of achieving a better performance. The scaling of CMOS technology makes it possible to reach a low consumption, low cost and a reasonable noise figure, making imperative the search and development of new circuits with improved performance.

The MOSFET-only LNA replaces the resistors common-gate (CG) and common- source (CS), shown in Fig. 2.13, by PMOS transistors. The PMOS transistors M_3 and M_4, respectively, operating in the triode region but close to the saturation region, which is reached when the g_m has almost the same amplitude value of g_{ds}, allows an increase to the incremental load resistance and, consequently, in the LNA's gain, for the same DC voltage drop.

The substitution of the resistors by PMOS devices results in a reduced circuit area and

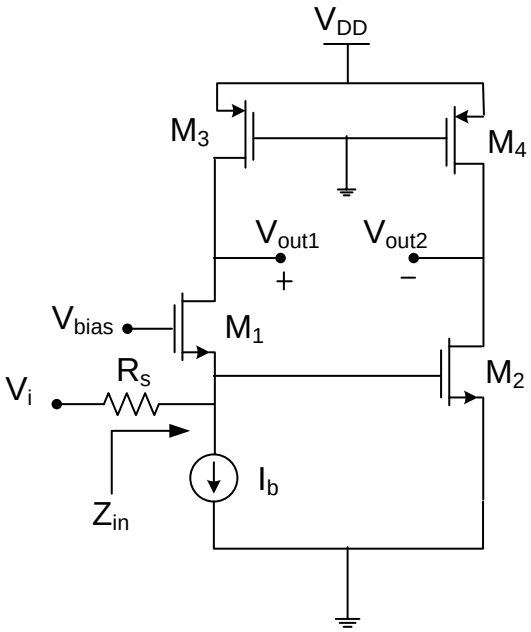


Figure 2.13: MOSFET-only Wideband Balun LNA

cost, minimizes the effect of process variation, supply variation and mismatch. Also, optimizes the gain of the LNA and minimize the noise figure by controlling the polarization state of PMOS transistors.

Regarding the original LNA, this circuit has the disadvantage of an increased distortion and a reduction in bandwidth.

This subsection on wideband LNA is important for the comprehension of some topologies, but also to help in the understanding of Chapter 3 that focuses on the development of the proposed circuit [21].

2.7 Mixer

As fundamental blocks in an RF analog front-end receiver circuit, the mixers have the function of frequency translation of the input signal, Radio Frequency (RF) signal to a baseband or an Intermediate Frequency (IF) signal, where this process is known as down-conversion. The mixer operates as a multiplication operation which is performed by two inputs, the Local Oscillator (LO) signal and the Radio Frequency (RF) signal, obtaining two signals with equal frequencies to both sum and difference of the input frequencies.

The mixers have different types of possible implementations: the active and passive mixers.

Therefore, the mixer conversion gain is important for relax the performance requirements of both previous topologies and following blocks. The voltage conversion gain is defined by 2.41 as the ratio of the root-mean-square (RMS) voltage of the Intermediate Frequency (IF) signal and the root-mean-square (RMS) voltage of the Radio Frequency

(RF) signal:

$$\text{Voltage Gain}(dB) = 20\log\left(\frac{V_{out}}{V_{in}}\right) \tag{2.41}$$

It can be seen as a measure of the mixing efficiency and allows distinguish the passive mixer having conversion loss (CL) from the active mixer having conversion gain (CG).

The mixing is a nonlinear operation and when nonlinear devices, such as MOS transistors, are used for mixing higher operation, order effects and intermediation issues appear. In the third-order intermodulation distortion can be generated two harmonics, which is difficult to filter without removing the IF signal. So, the levels of third-order products can be verified from the Input Reference Intercept Point (IIP_3), which uses the power of the Radio Frequency (RF) input and output to increase the direct down-converted product.

This subsection will be focused on two types of mixer topologies referring the main characteristics and properties of each [10, 11].

2.7.1 Active Mixer

Active mixers provide gain and strength to the IF signal, as they deliver it to subsequent receiver stages. They are most commonly based in differential pair and can be single-balanced or double-balanced, depending on whether the RF signal coming from the LNA is balanced or unbalanced.

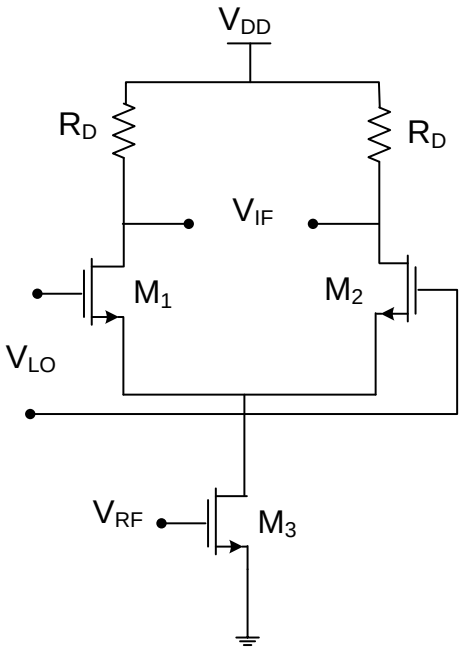


Figure 2.14: Single Balanced Mixer

The single-balanced active mixer, represented in Fig. 2.14, has a differential pair with

the inputs driven by the LO signals, applied at the both gates, and a current source controlled by the RF unbalanced signal. The RF input voltage is converted to current that is drawn alternately by the two sides of the differential pair and they preferably switched between saturation region and OFF states. For this mixer, the output spectrum includes the LO frequency. It is a simple active mixer that has moderate gain and noise figure, high input impedance and low 1 dB compression point, low IIP_3 and low port-to-port isolation.

The double-balanced active mixer, represented in Fig. 2.15, called Gilbert cell, is more complex, having Local Oscillator (LO) and Radio Frequency (RF) differential inputs. It features improvements when compared to the single-balanced active mixer, namely higher gain, lower noise figure, high port-to-port isolation and good linearity. It is also able to remove the local oscillator (LO) frequency from the output spectrum. These improvements increase the power consumption and circuit area and cost. A reduction of the supply voltage leads to worse linearity performance.

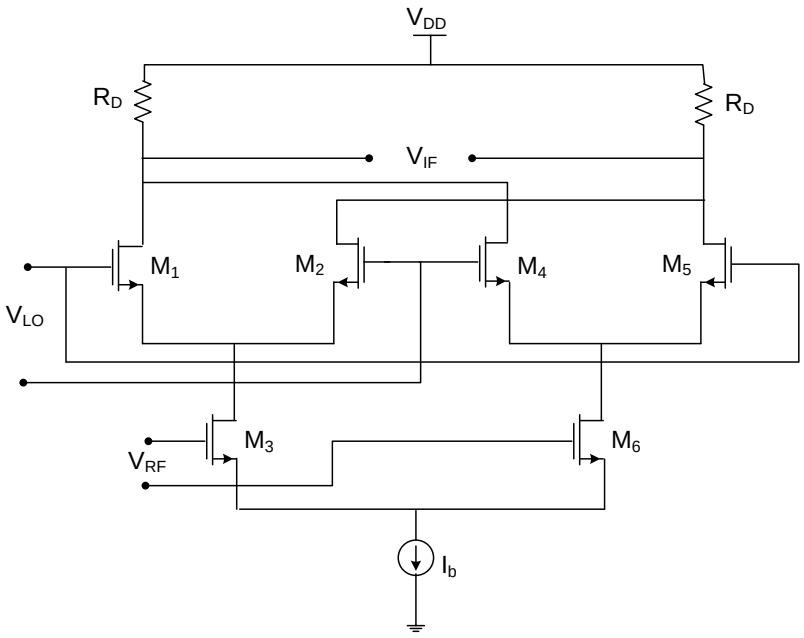


Figure 2.15: Gilbert Cell

The voltage conversion gain (CG) is given by:

$$A_v = \frac{2}{\pi g_{m1} R_L} \tag{2.42}$$

There are two ways to increase the mixer gain by increasing the current flowing through the transconductors or increasing the load impedance or both them [10, 11, 22, 23].

2.7.2 Passive Mixer

The simplest mixer configuration is a CMOS transistor-implemented switch, shown in Fig. 2.16, whose gate is driven by the Local Oscillator (LO) signal, with the RF signal being applied at its drain and the Intermediate Frequency (IF) signal being taken at its source. This passive mixer has no DC consumption, no gain and provides high linearity and bandwidth.

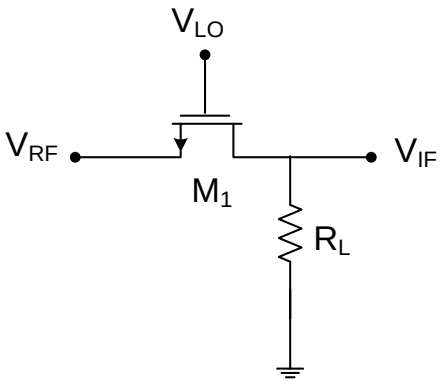


Figure 2.16: Passive Mixer using switch.

The implemented switch operates between the driving and cutting region, since the LO power is applied to the gate at the oscillation frequency, presents a channel resistance (R) varying with time. For small drain to source voltage, the channel resistance can be found as:

$$R = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th})} \tag{2.43}$$

where μ_n is electron mobility, C_{ox}, gate oxide capacitance per unit area, W, gate width, L, gate length, V_{gs}, gate to source voltage and V_{th}, threshold voltage.

The channel resistance R influences some important characteristics of the passive mixer, to achieve a good impedance matching between the RF and IF ports and a Conversion Loss (CL), it has to have a low resistance.

Therefore, during the passive mixer' projection the choice of the ratio W/L, which is the size of the transistor must have in mind the best Conversion Loss (CL), impedance matching and minimum LO capacitive feed-through [10, 11, 24].

3

Low-voltage receiver analog front-end

A design of a low-voltage CMOS RF receiver has been proposed and the complete circuit implementation is shown in Fig. 3.7. The building blocks of this circuit are the LNA, the mixer, the LO and the TIA. The TIA is able to buffer the final output, filter frequencies higher than the chosen IF frequency and convert the current signal to a voltage signal. A DC voltage source is added between the mixer and the TIA as a common-mode voltage for the TIA inputs. The presented receiver circuit does not include the design of the oscillator, OTA block from the TIA.

The organization of this chapter is divided by the LNA and the receiver subsections. In both subsections some theoretical expressions and characteristics are analysed. In the receiver front-end subsection an overall notion of the most important characteristics and particularities of all blocks is given. In the same subsection the mixer structure is highlighted with more detail. However, both the LNA and mixer structures were already known and didn't constitute an actual novelty by themselves. Some novel considerations are taken into account, as will be shown in the following subsections. The main contribution of the presented circuit is not the introduction of a new LNA and mixer architectures, but rather a new implementation of their combination: the signals are treated in current mode.

3.1 LNA

The proposed LNA circuit is presented in Fig. 3.1, it's wideband balun LNA composed by two stages: a common-gate (CG) and common-source (CS) stage. The balun functionality is important for the LNA performance because in its entry has a single-ended, unbalanced input and provides a balanced output. This balanced output is a consequence of the matching magnitudes of the two gains stages when their values are approximate.

It can be said that the proposed LNA is a new version of the MOSFET-only LNA presented in section 2.6.2.3, designed to work at V_{DD} supply voltage of 0.6 V. The design optimization and several processes have been taken into account to make the LNA working with this V_{DD} value without losing too much gain, such as the meticulous dimensioning of the transistors, the use of a low-voltage technique and the introduction of independent stage biasing, that will be shown in chapter 4 with the values and the simulations results.

The current output of the LNA can be optimised by using PMOS active devices loads that through the adjustments of their dimensions can increase the LNA's output resistance. The PMOS devices not only help to increase the output resistance of the LNA, as well as they are responsible for the improving of the LNA's voltage gain and noise. However, the LNA's voltage gain is not the main concern, but rather its transcondutance gain, which is essentially given by the transistors M_1 and M_2 gm values. The fact that the LNA's output resistance depends on the dimensions of PMOS devices is relevant because the chosen mixer works in current mode, which will be explained in section 3.2.1.

The biasing voltage from the common-gate (CG) stage (V_{bias1}) applied in the transistor M_1 gate terminal is limited to the supply voltage value, for that reason it wouldn't be sufficient to assure both transistors M_1 and M_2 gate-source voltage (V_{gs}) needed values. Therefore, an additional biasing voltage was added to the common-source (CS) stage the V_{bias2} to ensure enough gate-source voltage (V_{gs}) across transistor M_2. Also, along with the V_{bias2} was added between the stages of the LNA the decoupling capacitor C_1, to help stop the influence among them. These changes in the LNA circuit allow the reduction of the V_{DD}.

Additionally, the Dynamic Threshold MOS (DTMOS) low-voltage technique is used in transistor M_1 to allow the low supply voltage operation. The technique consists in connecting the bulk of the transistor to its gate terminal [25, 26], introducing a dynamic regulation of the transistor's threshold voltage. The use of this technique allows enough drain-source voltage (V_{ds}) for the current-source transistor connected to the LNA's first stage, which substitutes the ideal current source presented in Fig. 3.1. It does so by reducing the threshold voltage of transistor M_1. The DTMOS technique is also responsible for a small increase in the effective g_m of device M_1, slightly contributing to the CG voltage gain. The DTMOS technique also has some disadvantages, such as the increase of the parasitic capacitances, in this case on the transistor M_1 and the possibility of latch-up appearance. The latch-up will not be an issue for this work because the whole circuit

voltages supply is lower than 0.7 V, which is the typical problematic threshold that the latch-up effect becomes a problem. The increase of parasitic capacitances decreases the bandwidth (BW), but they aren't relevant to reflect a problematic situation in terms of the BW. Therefore, the choice of this low-voltage technique becomes the best choice regarding the other techniques for the same purpose [25, 26].

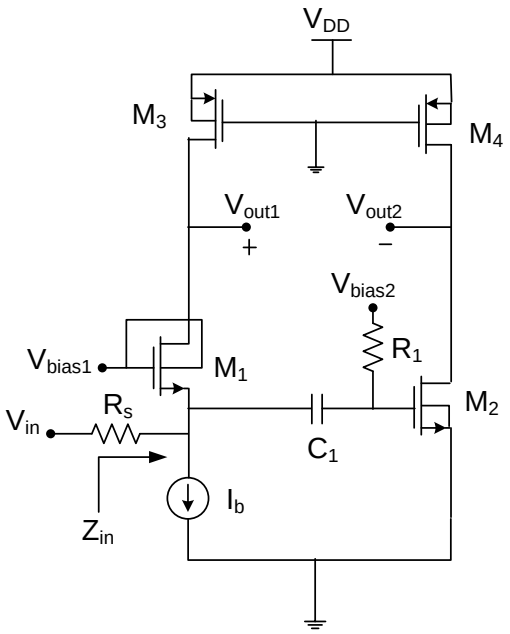


Figure 3.1: Proposed LNA Circuit.

3.1.1 Gain

The small signal model for low frequencies of the LNA proposed is represented in Fig. 3.2. Since the signal V_{in} is applied in the transistor M_1 source terminal, the bulk effect has to be considered. However, due to the use of the DTMOS technique on the transistor M_1 where consists of connecting the bulk to the gate terminal, the body effect contributes positively to the CG voltage gain. The body effect appears due the transistor configuration where the source and bulk terminals don't have the same value. So, the body effect is represented in the incremental analysis by a voltage controlled current source (VCVS) which is dependent on bulk-source voltage (V_{bs}).

The expression for the LNA differential voltage gain is achieved by the subtraction of the CG and CS voltage gains, which were deduced using the Fig. 3.2. To obtain the voltage gain of the two stages, a nodal analysis is performed at nodes N1 and N2 using the rules of KVL (Kirchhoff's Voltage Law) as established.

The considerations $V_{gs1} = -V_{in}$ and $V_{bs1} = -V_{in}$ are taken from the node N1:

$$g_{m1}v_{gs1} + (v_{out1} - v_{in})g_{ds1} + g_{mb1}v_{bs1} + v_{out1}g_{ds3} + g_{m3}v_{gs3} = 0 \tag{3.1}$$

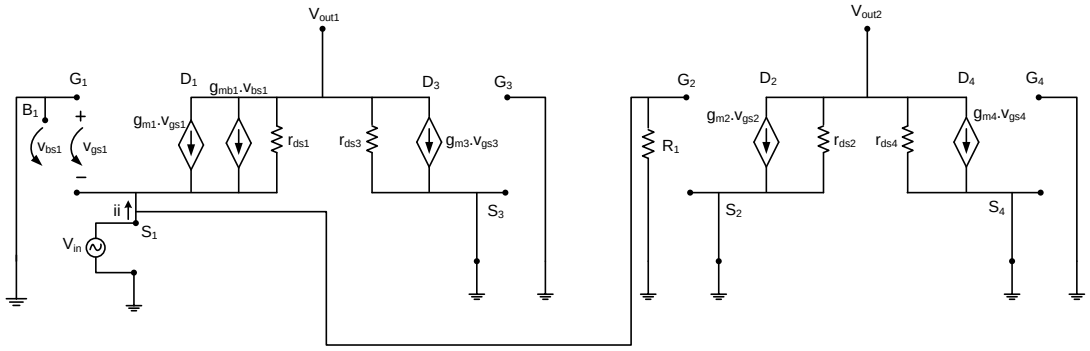


Figure 3.2: The small signal model for low frequencies of the LNA.

At node N2 is taken into account the consideration $V_{gs2} = V_{in}$:

$$g_{m2}v_{in} + v_{out2}(g_{ds2} + g_{ds4}) + g_{m4}v_{gs4} = 0 \tag{3.2}$$

With the respective substitutions from 3.1 the common-gate (CG) gain is,

$$A_{vCG} = \frac{V_{out1}}{V_{in}} = \frac{g_{m1} + g_{mb1} + g_{ds1}}{g_{ds1} + g_{ds3}} \tag{3.3}$$

Can be expressed also:

$$A_{vCG} = \frac{((g_{m1} + g_{mb1})r_{ds1}) + 1)r_{ds3}}{r_{ds1} + r_{ds3}} \tag{3.4}$$

In the case where it's considered that the resistance R_S and the signal V_{in} are applied together on the source terminal of the transistor M_1. The current i_{n2} is taken at node N2 and some considerations are $i = V_{out1}/r_{ds3}$ and $V_{gs1} = i.R_s - V_{in}$:

$$i_{n2} = \frac{V_{out1}}{r_{ds3}} + (g_{m1} + g_{mb1})V_{gs1} \tag{3.5}$$

From the KVL rule, V_{out1} can be expressed as:

$$V_{out1} = V_{in} - i.R_s - i_{n2}r_{ds1} \tag{3.6}$$

The voltage gain of CG stage is:

$$A_{vCG[Rs]} = \frac{V_{out1}}{V_{in}} = \frac{r_{ds3}(1 + r_{ds1}(g_{m1} + g_{mb1}))}{r_{ds3} + r_{ds1} + R_s(1 + r_{ds1}(g_{m1} + g_{mb1}))} \tag{3.7}$$

The result of common-source(CS) gain (3.8) is obtained by the same procedure of the common-gate (CG) gain (3.3), but in this case is made the manipulation of the expression 3.2.

$$A_{vCS} = \frac{V_{out2}}{V_{in}} = -\frac{g_{m2}}{g_{ds2} + g_{ds4}} \tag{3.8}$$

The common-source (CS) stage gain can also be expressed through output resistances:

$$A_{vCS} = -g_{m2}(r_{ds2} \| r_{ds4}) = -g_{m2}\frac{r_{ds2}r_{ds4}}{r_{ds2} + r_{ds4}} \tag{3.9}$$

The LNA differential voltage gain is obtained through the subtraction of (3.3) and (3.8):

$$A_{vdiff} = \frac{V_{out1} - V_{out2}}{V_{in}} = \frac{g_{m1} + g_{mb1} + g_{ds1} + g_{m2}(\frac{g_{ds1}+g_{ds3}}{g_{ds2}+g_{ds4}})}{g_{ds1} + g_{ds3}} \tag{3.10}$$

The approximate expression for the LNA differential voltage gain is possible to get it if it's considered that the values of g_{ds1} and g_{ds2} ($g_{ds1} \approx g_{ds2}$) and the values of g_{ds3} and g_{ds4} ($g_{ds3} \approx g_{ds4}$) are similar between them.

$$A_{vdiff} \approx \frac{g_{m1} + g_{mb1} + g_{m2}}{g_{ds1} + g_{ds3}} \tag{3.11}$$

3.1.2 LNA input-impedance

The LNA input-impedance expression (Z_{in}) is achieved from the transistor M_1 source terminal, as shown in Fig. 3.1. It's obtained through the analysis of the small signal for low frequency as shown in Fig. 3.2, where is verified the current ii flowing through the transistor source.

$$-ii - g_{m1}v_{gs1} - g_{mb1}v_{bs1} - (v_{out1} - v_{in})g_{ds1} = 0 \tag{3.12}$$

The considerations $V_{gs1} = V_{bs1} = -V_{in}$ are substituted in the expression 3.12 to obtain a simpler current expression 3.13.

$$ii = g_{m1}v_{in} + g_{mb1}V_{in} - V_{out1}g_{ds1} + V_{in}g_{ds1} \tag{3.13}$$

$$\frac{1}{Z_{in}} = \frac{ii}{V_{in}} \tag{3.14}$$

Noting that 3.14 and then substituting on it with the current expression 3.13, the following expression is obtained:

$$\frac{1}{Z_{in}} = \frac{V_{in}(g_{m1} + g_{mb1} + g_{ds1}) - V_{out1}g_{ds1}}{v_{in}} \tag{3.15}$$

Using the expression of the common-gate (CG) gain (3.3) to replace V_{out1} in the expression 3.15, we obtain the input-impedance:

$$Z_{in} = \frac{g_{ds1} + g_{ds3}}{(g_{m1} + g_{mb1} + g_{ds1})g_{ds3}} \tag{3.16}$$

3.1.3 Noise Factor

The complete LNA's noise factor is formed by three main noises sources: the thermal noise influenced by the transistors and resistors and the flicker noise generated by transistors. The LNA circuit, shown in Fig. 3.1, had to suffer some approaches and considerations, in order to simplify the analysis of the noise factor, demonstrated in the Fig. 3.3. These are the following ones:

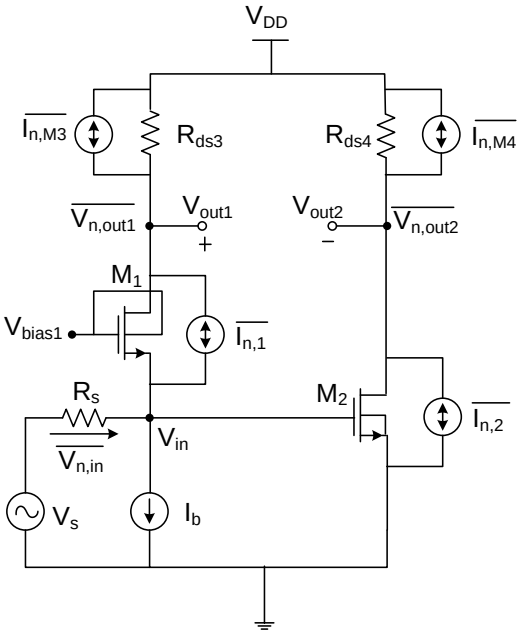


Figure 3.3: The result of the LNA circuit' approaches and approximations, including some noise sources.

- The thermal noise's effect that is generated by the source resistor R_S and the input source of CG stage is neglected at the beginning of this analysis, but afterwards is considered in the final equation, as will be established (3.48).

- The thermal noise generated by the transistor M_1 of the CG stage is represented by the current source ($\overline{i_{n,1}}$) which corresponds the current that flows into to resistor R_S, producing a noise voltage ($\overline{V_{n,in}}$) at the input of CG stage. The noise voltage ($\overline{V_{n,in}}$) is opposed to the output noise of the CG stage ($\overline{V_{n,out1}}$) and in phase with the output noise CS stage ($\overline{V_{n,out2}}$), their respective associated conditions are: $\overline{V_{n,out1}} = -\overline{V_{n,in}}A_{vCG}$ and $\overline{V_{n,out2}} = \overline{V_{n,in}}A_{vCS}$. The thermal noise produced by transistor M_1 is cancelled if the Balun conditions are satisfied. Which means that the CG and CS gains should be equals ($A_{vCG} = -A_{vCS}$) to obtain a balanced differential output and cancellation of thermal noise of the M_1.

- The PMOS transistors (M_3 and M_4) were dimensioned as LNA's output resistances,

its area of operation is the triode zone which considered that $g_m << g_{ds}$. Therefore, for the analysis of the LNA's noise factor was neglected the gm effect on the M_3 and M_4 transistors and considered as typically resistances r_{ds3} and r_{ds4} (dimensions in the order of ohms), respectively, demonstrated in the Fig. 3.3.

- The thermal noise effect of the resistor R_1 is negligible in the overall noise factor of the LNA. Although the resistor R_1' dimension has an order of Kohms compared to the dimensions of the LNA's output resistances (r_{ds3} and r_{ds4}), the current source that is applied in parallel with R_1 to obtain the thermal noise is $\overline{I_{n,R1}} = 4kT/R_1$. So their contribution isn't relevant to the total noise factor.

- The effects of the parasitic capacitances are negligible because the LNA's noise factor is at low frequencies.

Initially, this analysis will be done by separating the LNA stages and considers each noise source at once.

Common-gate (CG) stage

The Fig. 3.4 represents all noise sources in the common-gate (CG) circuit and small signal model. From the superposition theorem and assuming that the noise sources aren't correlated, each noise source is analysed independently.

Flicker noise: The flicker noise source in the gate of transistor M_1 ($\overline{V_{n,f}}$) is modeled in series with a voltage ($\overline{V_{nf1,out}}$), shown in Fig. 3.4(b), with the conditions mentioned above.

Considering the voltage that goes to the gate until ground $\overline{V_{n,f}} = V_{gs1} - V_{bs1}$, the expression (3.17) of bulk-source voltage is:

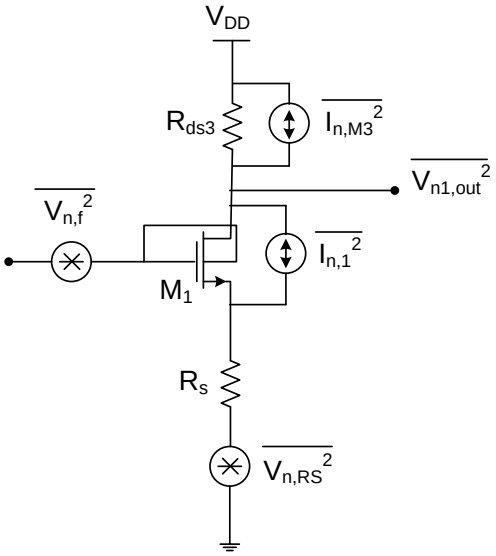
$$V_{bs1} = iiR_s \tag{3.17}$$

Substituting the expression (3.17) on ($\overline{V_{n,f}} = V_{gs1} - V_{bs1}$):

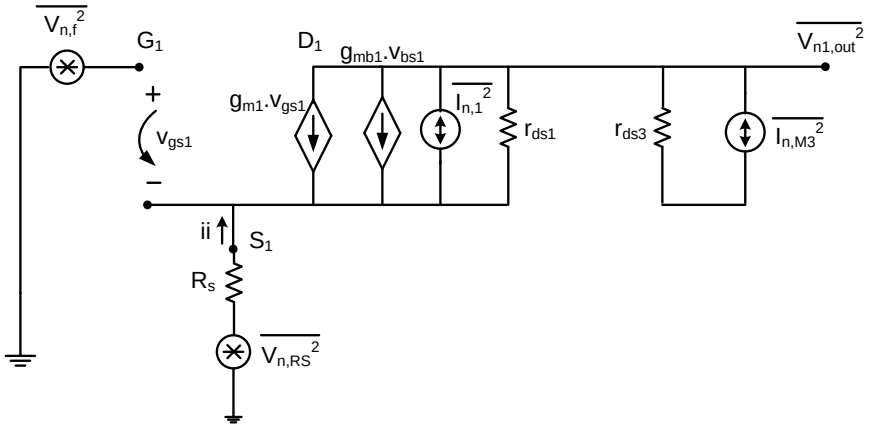
$$V_{gs1} = iiR_s + \overline{V_{n,f}} \tag{3.18}$$

At node 1 is taken the current (ii):

$$ii = -(g_{m1}V_{gs1} + g_{mb1}V_{bs1}) + \frac{(-V_{bs1} - \overline{V_{nf1,out}})}{r_{ds1}} \tag{3.19}$$



(a) CG circuit



(b) The small signal model for low frequencies of CG circuit

Figure 3.4: Common-gate (CG) model for all the noise contributions.

Using the equations (3.17) and (3.18), then substituting on (3.19) and solving in order ii:

$$ii = \frac{-g_{m1}\overline{V_{n,f}} - g_{ds1}\overline{V_{nf1,out}}}{1 + R_s(g_{m1} + g_{mb1} + g_{ds1})} \tag{3.20}$$

The output noise voltage ($\overline{V_{nf1,out}}$) from the flicker noise ($\overline{V_{n,f}}$) is calculated by substituting the equation (3.20) on (3.21) and solving in order $\overline{V_{nf1,out}}$:

$$\overline{V_{nf1,out}} = iir_{ds3} = -\frac{g_{m1}r_{ds1}r_{ds3}}{r_{ds1} + R_s(r_{ds1}(g_{mb1} + g_{m1}) + 1) + r_{ds3}}\overline{V_{n,f}} \tag{3.21}$$

The output voltage noise power ($\overline{{V_{nf1,out}}^2}$) is:

$$\begin{aligned}\overline{V_{nf1,out}^2} &= \left(\frac{g_{m1}r_{ds1}r_{ds3}}{r_{ds1} + R_s(r_{ds1}(g_{mb1} + g_{m1}) + 1) + r_{ds3}}\right)^2 \overline{{V_{n,f}}^2} \\ &= \left(\frac{g_{m1}r_{ds1}r_{ds3}}{r_{ds1} + R_s(r_{ds1}(g_{mb1} + g_{m1}) + 1) + r_{ds3}}\right)^2 \frac{k_f}{c_{ox}W_1L_1f^{\alpha f}}\end{aligned} \tag{3.22}$$

Thermal noise: The thermal noise source in transistor M_1 is presented as a current source ($\overline{I_{n,1}}$) between the drain and the source, shown in Fig. 3.4(b).

From the condition ($V_{gs1} = V_{bs1}$) the gate-source voltage is,

$$V_{gs1} = iiR_s \tag{3.23}$$

The current that flows in the resistance r_{ds3} is:

$$ii = -(g_{m1} + g_{mb1})V_{bs1} + I_{n,1} + \left(\frac{-V_{bs1} - V_{n1,out}}{r_{ds1}}\right) \tag{3.24}$$

By substituting (3.23) on (3.24), the expression (3.25) is solved on ii:

$$ii = \frac{\overline{I_{n,1}} - g_{ds1}\overline{V_{n1,out}}}{1 + R_s(g_{m1} + g_{mb1} + g_{ds1})} \tag{3.25}$$

The output thermal noise ($\overline{V_{n1,out}}$) is calculated from the thermal noise source ($\overline{I_{n,1}}$) when (3.25) is substituted on (3.26):

$$\overline{V_{n1,out}} = iir_{ds3} = \frac{\overline{I_{n,1}}r_{ds1}r_{ds3}}{r_{ds1} + R_s(r_{ds1}(g_{m1} + g_{mb1}) + 1) + r_{ds3}} \tag{3.26}$$

The thermal noise power at the output ($\overline{V_{n1,out}{}^2}$) is:

$$\begin{aligned}\overline{V_{n1,out}{}^2} &= \overline{I_{n,1}{}^2}\left(\frac{r_{ds1}r_{ds3}}{r_{ds1}+R_s(r_{ds1}(g_{m1}+g_{mb1})+1)+r_{ds3}}\right)^2 \\ &= 4KT\gamma g_{m1}\left(\frac{r_{ds1}r_{ds3}}{r_{ds1}+R_s(r_{ds1}(g_{m1}+g_{mb1})+1)+r_{ds3}}\right)^2\end{aligned} \tag{3.27}$$

Thermal noise due to the resistance r_{ds3}: The thermal noise source ($\overline{I_{n,M3}}$) of the resistance r_{ds3} is modeled as a current source parallel to it, as shown in Fig. 3.4.

To obtain the expression of the output noise ($\overline{V_{nM3,out}}$) from the thermal noise source ($\overline{I_{n,M3}}$), the R_S is neglected (R_S = 0), so the small signal incremental model is simplified (Fig. 3.5).

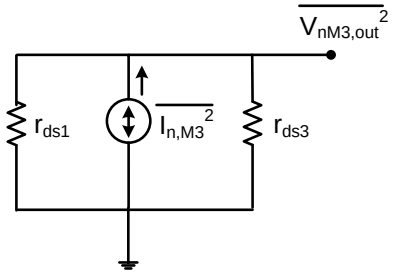


Figure 3.5: The approximate small signal model of CG circuit.

$$\overline{V_{nM3,out}} = \overline{I_{n,M3}}(r_{ds1}\|r_{ds3}) \tag{3.28}$$

Considering the condition V_{gs2} = 0 and (3.28), the thermal noise power of the output ($\overline{V_{nM3,out}}$) is:

$$\overline{V_{nM3,out}{}^2} = \overline{I_{n,M3}{}^2}(r_{ds1}\|r_{ds3})^2 = \frac{4KT}{r_{ds3}}(r_{ds1}\|r_{ds3})^2 \tag{3.29}$$

In the case of considering the resistance R_s, the output thermal noise ($\overline{V_{nM3,out}}$) is calculated by rely on the input noise ($\overline{V_{n,in}}$) and on the CG gain stage (3.4):

$$\overline{V_{nM3,out}{}^2} = \overline{V_{n,in}{}^2}A_{vCG}{}^2 \tag{3.30}$$

By substituting (3.28) and the gain (3.4) on the expression (3.31), the input noise power ($\overline{V_{n,in}{}^2}$) is,

$$\overline{V_{n,in}{}^2} = \frac{4KTr_{ds3}(r_{ds1})^2}{((r_{ds1}(g_{m1}+g_{ds1})+1)r_{ds3})^2} \tag{3.31}$$

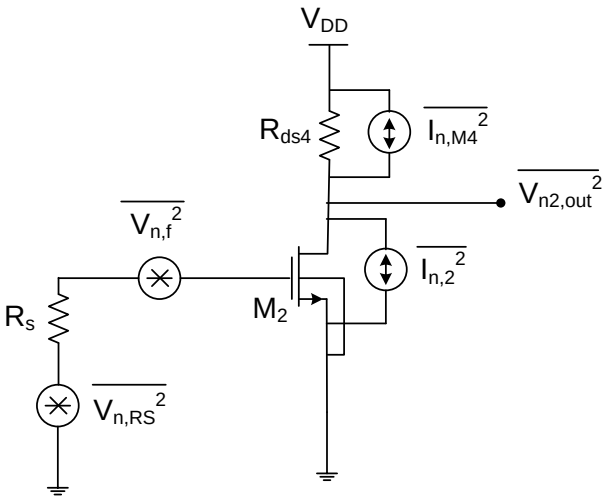
The output noise power ($\overline{V_{nM3,out}{}^2}$) of the circuit (3.3) is calculated by multiplying the input noise power (3.31) and the transfer function obtained in (3.7) that corresponds

to the CG gain expression that includes the resistance R_s. The noise power at the output is,

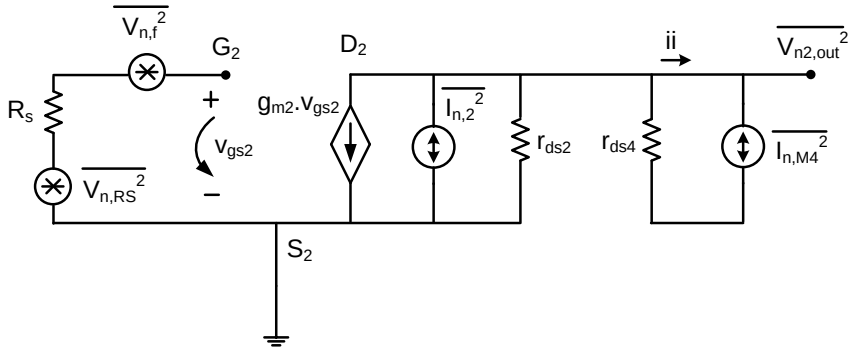
$$\overline{V_{nM3,out}}^2 = \frac{4KTr_{ds3}(r_{ds1})^2}{((r_{ds1}(g_{m1}+g_{ds1})+1)r_{ds3}R_s + r_{ds1} + r_{ds3})^2} \tag{3.32}$$

Common-source (CS) stage

All noise sources of the common-source (CS) circuit and the incremental analysis model are represented in Fig. 3.6. Assuming that the analysis of each noise source is independent and uncorrelated, that's why it's used the superposition theorem.



(a) CS circuit



(b) The small signal model for low frequencies of CS circuit

Figure 3.6: Common-source (CS) model for all the noise contributions.

Flicker Noise: The flicker noise source ($\overline{V_{n,f}}$) of the transistor M_2 is modeled as a voltage source in series with the gate, shown in Fig. 3.6(b).

The flicker noise power at the output ($\overline{V_{nf2,out}{}^2}$) is calculated using the transfer function of the CS gain (3.8):

$$\overline{V_{nf2,out}{}^2} = \overline{V_{n,f}{}^2} A_{vCS}{}^2 = \frac{k_f}{W_2 L_2 c_{ox} f^{\alpha_f}} g_{m2}{}^2 \left(\frac{r_{ds2} r_{ds4}}{r_{ds2} + r_{ds4}} \right)^2 \tag{3.33}$$

Thermal Noise: The current source ($\overline{I_{n,2}}$) lying between the drain and the source of transistor M_2 is used as the presentation of the thermal noise source.

As shown in Fig. 3.6(b), the current source $\overline{I_{n,2}}$ is,

$$\overline{I_{n,2}{}^2} = 4KTg_{m2} \tag{3.34}$$

The output noise power ($\overline{V_{n2,out}{}^2}$) due to the current source $\overline{I_{n,2}}$ is,

$$\overline{V_{nf2,out}{}^2} = \overline{I_{n,2}{}^2} (r_{rds2} \| r_{ds4})^2 = 4KTg_{m2} \left(\frac{r_{ds2} r_{ds4}}{r_{ds2} + r_{ds4}} \right)^2 \tag{3.35}$$

Thermal noise due to the resistance r_{ds4}: It's represented as a current source ($\overline{I_{n,M4}}$) parallel to resistance r_{ds4}.

$$\overline{I_{n,M4}{}^2} = \frac{4KT}{r_{ds4}} \tag{3.36}$$

Taking into account that V_{gs2} = 0, the output noise power ($\overline{V_{nM4,out}{}^2}$) is:

$$\overline{V_{nM4,out}{}^2} = \overline{I_{n,M4}{}^2} (r_{rds2} \| r_{ds4})^2 = \frac{4KT}{r_{ds4}} \left(\frac{r_{ds2} r_{ds4}}{r_{ds2} + r_{ds4}} \right)^2 \tag{3.37}$$

After acquiring the individual analysis of each noise stage, it's necessary obtained the noise contributions that are from the CG stage and will appear at the CS output stage and vice-versa. To access this effect, the input referred represents the noise generated by the stage that will influence the other, divided by its own gain and then amplified by the influenced stage. Furthermore, to simplified the complete noise power process, the noise effect that is generated by the source resistor R_S and the input source of CG stage is neglected, but added in final equation (3.48).

Thus, the case that the noise generated by the CG stage, divided by (3.4) and multiplied by (3.9), will appear at the CS output stage as:

$$\begin{aligned}\overline{V_{nf1CG,outCS}{}^2} &= \frac{\overline{V_{nf1,outCG}{}^2}}{A_{vCG}{}^2} A_{vCS}{}^2 = \\ &= \frac{(g_{m1}r_{ds1}r_{ds3})^2(g_{m2}r_{ds2}r_{ds4})^2}{(r_{ds3}(r_{ds1}(g_{m1}+g_{mb1})+1))^2(r_{ds2}+r_{ds4})^2}\frac{k_f}{c_{ox}W_1L_1f^{\alpha f}}\end{aligned} \tag{3.38}$$

$$\begin{aligned}\overline{V_{n1,outCS}{}^2} &= \frac{\overline{V_{n1,outCG}{}^2}}{A_{vCG}{}^2} A_{vCS}{}^2 = \\ &= 4KT\gamma g_{m1}\left(\frac{r_{ds1}r_{ds3}}{r_{ds3}(r_{ds1}(g_{m1}+g_{mb1})+1)}\right)^2\left(\frac{g_{m2}r_{ds2}r_{ds4}}{r_{ds2}+r_{ds4}}\right)^2\end{aligned} \tag{3.39}$$

$$\begin{aligned}\overline{V_{nM3,outCS}{}^2} &= \frac{\overline{V_{nM3,outCG}{}^2}}{A_{vCG}{}^2} A_{vCS}{}^2 = \\ &= 4KTr_{ds3}\left(\frac{r_{ds1}}{r_{ds3}(r_{ds1}(g_{m1}+g_{mb1})+1)}\right)^2\left(\frac{g_{m2}r_{ds2}r_{ds4}}{r_{ds2}+r_{ds4}}\right)^2\end{aligned} \tag{3.40}$$

In the same situation occurs the noise generated by the CS stage, which appears at the CG output stage as:

$$\overline{V_{nf2CS,outCG}{}^2} = \frac{\overline{V_{nf2,outCS}{}^2}}{A_{vCS}{}^2} A_{vCG}{}^2 = \left(\frac{r_{ds3}(r_{ds1}(g_{m1}+g_{mb1})+1)}{r_{ds1}+r_{ds3}}\right)^2 \frac{k_f}{c_{ox}W_2L_2f^{\alpha f}} \tag{3.41}$$

$$\overline{V_{n2,outCG}{}^2} = \frac{\overline{V_{n2,outCS}{}^2}}{A_{vCS}{}^2} A_{vCG}{}^2 = \frac{4KT\gamma}{g_{m2}}\left(\frac{r_{ds3}(r_{ds1}(g_{m1}+g_{mb1})+1)}{r_{ds1}+r_{ds3}}\right)^2 \tag{3.42}$$

$$\overline{V_{nM4,outCG}{}^2} = \frac{\overline{V_{nM4,outCS}{}^2}}{A_{vCS}{}^2} A_{vCG}{}^2 = \frac{4KT}{r_{ds4}g_{m2}{}^2}\left(\frac{r_{ds3}(r_{ds1}(g_{m1}+g_{mb1})+1)}{r_{ds1}+r_{ds3}}\right)^2 \tag{3.43}$$

The complete LNA's noise factor of its differential output is obtained by the sum of all the noise power contributions available at the outputs (3.45) and (3.46), assuming that the noise sources are uncorrelated. Also, the thermal noise's effects that are generated by the source resistor R_S and the input source of CG stage are added to the final expression

(3.48). However, the thermal noise voltage generated by transistor M_1 is full cancelled according to cancellation conditions, where was explained above. The equation of the output thermal noise power due to the source resistor R_S is:

$$\overline{V_{n,RS}{}^2} = 4KTR_s \tag{3.44}$$

$$\overline{V_{n,outCG}{}^2} = \overline{V_{nf1,outCG}{}^2} + \overline{V_{nf2CS,outCG}{}^2} + \overline{V_{n2,outCG}{}^2} + \overline{V_{nM3,outCG}{}^2} + \overline{V_{nM4,outCG}{}^2} \tag{3.45}$$

$$\overline{V_{n,outCS}{}^2} = \overline{V_{nf2,outCS}{}^2} + \overline{V_{nf1CG,outCS}{}^2} + \overline{V_{n2,outCS}{}^2} + \overline{V_{nM4,outCS}{}^2} + \overline{V_{nM3,outCS}{}^2} \tag{3.46}$$

Moreover, the LNA's noise factor uses in the final equation (3.48) the differential voltage gain that is simplified, considering various conditions such as: $r_{ds1}(g_{mb1}+g_{m1}) >> 1$, $r_{ds1} = r_{ds2} = r_0$, $r_{ds3} = r_{ds4} = r_ds$ and $g_{m1} + g_{mb1} = g_{m2} = g_m$. The simplified differential voltage gain is obtained based on the subtraction of (3.4) and (3.9) is,

$$A_{vLNA} = \frac{2g_m r_0 r_{ds}}{r_0 + r_{ds}} \tag{3.47}$$

Assuming that the current source (id) represented in Fig. 3.3, is ideal and also, simultaneously, considering all previous approaches and considerations are applied to achieve the complete noise factor. The simplified LNA's noise factor is given by (3.48) [19].

$$\begin{aligned} F &= \frac{\overline{V_{n,RS}{}^2}A_{vLNA}{}^2 + \overline{V_{n,outCG}{}^2} + \overline{V_{n,outCS}{}^2}}{\overline{V_{n,RS}{}^2}A_{vLNA}{}^2} = 1 + \frac{\overline{V_{n,outCG}{}^2} + \overline{V_{n,outCS}{}^2}}{\overline{V_{n,RS}{}^2}A_{vLNA}{}^2} = \\ &= 1 + \frac{k_f}{8KR_s c_{ox} f^{\alpha f}}\left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_s g_m} + \frac{1}{R_s {g_m}^2 r_{ds}} \end{aligned} \tag{3.48}$$

3.2 Receiver front-end circuit

The complete schematic of the receiver front-end implementation is shown in Fig. 3.7 and the theoretical expression of the overall conversion gain is composed by the influence of each block that constitutes it. In the expression 3.49, the greatest influences on the circuit are the LNA's transconductance gain and the transimpedance amplifier (TIA) module. The LNA's transconductance gain is obtained from the transistors M_1 and M_2 g_m values while the PMOS transistors work as the LNA' output resistance. The passive mixer designed to work in current mode, shown in subsection 3.2.1, has no relevant influence on the receptor, because of its conversion loss (CL). In the case of LO signals, its square waves with a 50% duty-cycle varying between 0 V and 0.6 V are represented by the fundamental Fourier component of 50% duty-cycle that equals to a factor of $2/\pi$ [27]. The

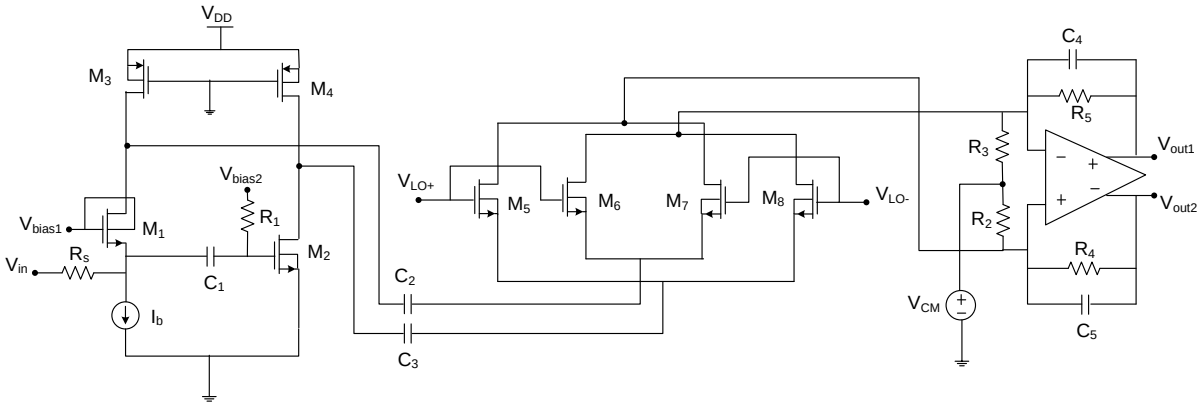


Figure 3.7: Complete Receiver Circuit.

TIA filter, in this case a Low-Pass Filter (LPF), is made by passive components, a combination of resistor and capacitor, that defines a conveniently dimensioned cut-off frequency, f_c. This f_c frequency was set at a value that is slightly higher than the IF frequency, so that higher frequencies are cut-off. The voltage conversion gain from single-ended input to differential output of the receiver topology is given by (3.49).

$$VG_{Total} = \frac{2}{\pi} g_{mLNA} Z_{TIAFilter@10MHz} \tag{3.49}$$

The RF signal coming from the antenna is amplified and converted to a current signal by the LNA, being delivered to the mixer as a balanced signal. The mixer's output, a balanced current signal, IF, is then converted to a balanced voltage signal by the TIA. As it's shown in equation (3.49), the LNA's transconductance gain is given by the gm values, because of the conversion of the RF voltage signal to a current signal. Also, the TIA module contributes to equation (3.49) with its impedance value, since the TIA module converts the current signal coming from the mixer to a voltage signal at the proposed receiver's output.

3.2.1 Mixer

The mixer architecture chosen to be integrated in the receiver is a passive mixer. The circuit is presented in Fig. 3.8 and is constituted by two pairs of NMOS used as voltage-controlled switches. The gates of the switches that constitute the mixer are driven by the Local Oscillator (LO) signals, with the Radio Frequency (RF) signals being applied at its source and the Intermediate Frequency (IF) signals being taken at its drain.

The main purpose of this architecture choice is the power consumption, which is a major requirement for the overall operation of the WSAN receiver. The two pairs of NMOS transistors are working in the triode zone to maintain a low drain-source voltage when they are switched ON. These NMOS transistors are cut-off when switched OFF. The mixer works as a current commutating mixer which means that the RF signals at the mixer' input are mixed in current. The LO signals that drive the devices' gates must be

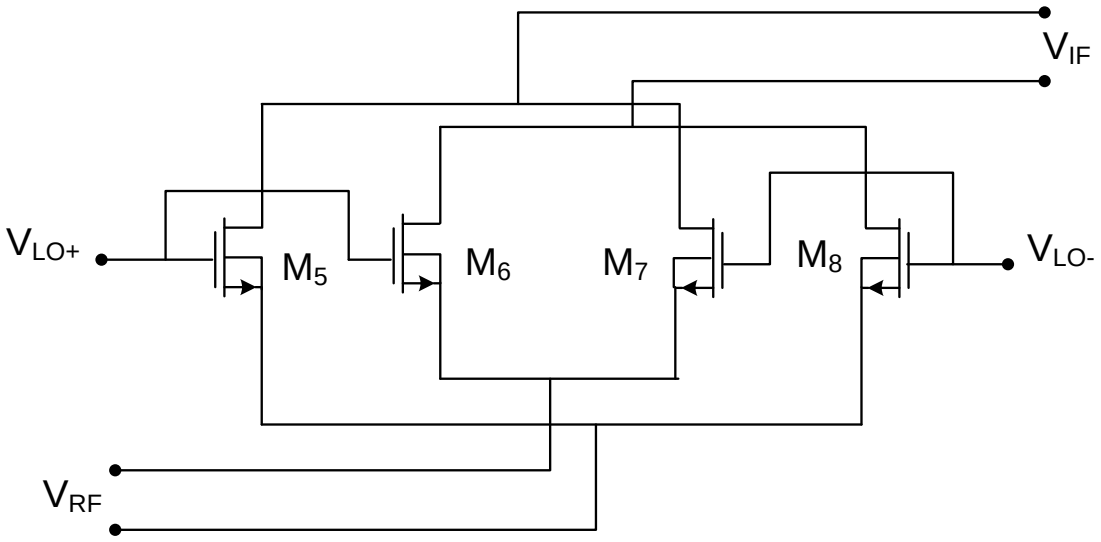


Figure 3.8: Mixer architecture.

strong and buffered; they vary from 0 V to 0.6 V, the V_{DD} supply voltage. The IF output signal is a balanced signal, due to the mixer's structure.

The factors that allow the mixer to work in current mode are the inclusion of the DC decoupling capacitors, the LO signals that drive the devices' gates and the common-mode voltage source at the TIA's input. The current mode minimizes the introduction of noise and ensures a good linearity. The reduced noise introduction, especially flicker noise, is possible due to the inclusion of the DC decoupling capacitors between the LNA and mixer, which guarantee there is no DC current flowing through the mixer. Moreover, due to the TIA, the variation of the drain-source voltage of the mixer's NMOS is reduced, thus contributing to improve the linearity of the circuit. The circuit' gain can be defined by the quotient between the IF signal amplitude and the RF signal amplitude. The passive mixer has a conversion gain that is less than one, so it presents a small Conversion Loss (CL).

4

Receiver Implementation

The detailed analysis of the theoretical expressions and characteristics present in the previous chapter are used to implement a low-voltage RF receiver in 130 nm CMOS technology presents the dimensioning of the proposed receiver circuit, as well as the schematic and post-layout simulations.

The section 4.1 introduces the considerations, simulations and validation of the implemented receiver, as well as the first block, the LNA, because of its importance and influence on the final results of the entire circuit. While in the post-layout section is presented the final design, the simulation results, the comparison between the obtained values before and after the layout and the problems that emerged. Finally, a brief discussion of the results is made and is verified if the circuit satisfies the requirements for the target application.

4.1 Considerations, simulations and validation of the proposed circuit

The dimension process for a low-voltage CMOS RF receiver has to be guided by the objectives that affect the target application for which the whole circuit was intended. The process was initiated when the classic schematics for each block of the receiver were chosen, with the simplicity and possibility criteria of working together to achieve the purpose of the target application. With all that being said the low-power consumption and low-voltage supply operations are the main scoops of this project.

The consideration process began by defining the V_{DD} voltage and power consumption values, which in this case, the V_{DD} voltage was set at 0.6 V. The restructuring and

modification began on the first block, the LNA, where the ideal current source was substituted by a current mirror, shown in Fig. 4.1 , biasing the first stage of the LNA with a current value of approximately 1.64 mA, the V_{bias1} was set at 0.6 V and V_{bias2} at 0.45 V.

The initial dimensions of the transistors which are shown in Table 4.1, had to take into account several factors. In the case of LNA, using equation (3.16), the dimensions of the transistor M_1 were manipulated to ensure the 50 Ω input matching, from the definition of its width (W_{M1}). The two stages presented in equations (3.3) and (3.8) have to coincide in value, that's why the width W_{M2} value of the transistor M_2 is chosen taking into account the matching gains of the CG and CS stages, which is required to achieve the noise cancelling capability, as explained the condition in section 3.1.3. Both transistors M_1 and M_2 have to be in the saturation region and V_{bias2} voltage is used to adjust the DC current of M_2 to a value close to the value of the M_1. W_{M3} and W_{M4} were determined by LNA' output impedance, which means that these values were chosen in order to define the PMOS drain-source resistance at a desired value, initially 200 Ω.

The NMOS and PMOS transistors are chosen as RF transistors, with a triple well structure chosen for the NMOS. The chosen length (L) for all transistors was the minimum value of the technology, in this case 120 nm, so that maximize the speed of the circuit.

The chosen width values for the mixer devices were created with the objective of achieving low values of drain-source resistance. Moreover, it's an inductorless circuit, which helps in the reduction of the overall circuit area and, for that reason, circuit cost.

Table 4.1: Initial Dimensions of the Transistors.

		I_D(mA)	W(μm)	L(μm)	$r_{ds}(\Omega)$	g_{ds}(mS)	g_m(mS)
LNA	M_1	1.64	66	0.12	453	2.2	20.15
	M_2	1.63	75.6	0.12	576	1.73	21.88
	M_3	1.64	52.8	0.12	254	3.93	8.6
	M_4	1.63	53.28	0.12	257	3.89	8.5
Mixer	$M_{5,6,7,8}$	-	115.2	0.12	-	-	-

This receiver circuit doesn't include the oscillator and the OTA designs, considering them as ideal devices. However, the circuit was dimensioned to work with a RF frequency of 1 GHz and an IF frequency of 10 MHz, thus the LO frequency was considered 990 MHz. The signals that come from LO+ and LO- in Fig. 3.7 are square waves in quadrature with 50 ps of rise and fall times and without overlapping, with peak-to-peak buffered voltages of 0.6 V.

Other important components that are responsible for the circuit behaviour are the resistors and capacitors. The values chosen for both type of components are presented in table 4.2. The resistor R_1 and capacitor C_1 are responsible for the independently biasing of the CS stage, as mentioned earlier in this section. While the resistors R_2 and R_3 help define the common mode voltage at the TIA input, which is set at 100 mV by the ideal voltage V_{CM}. The capacitor C_1 is also responsible for DC decoupling between the two

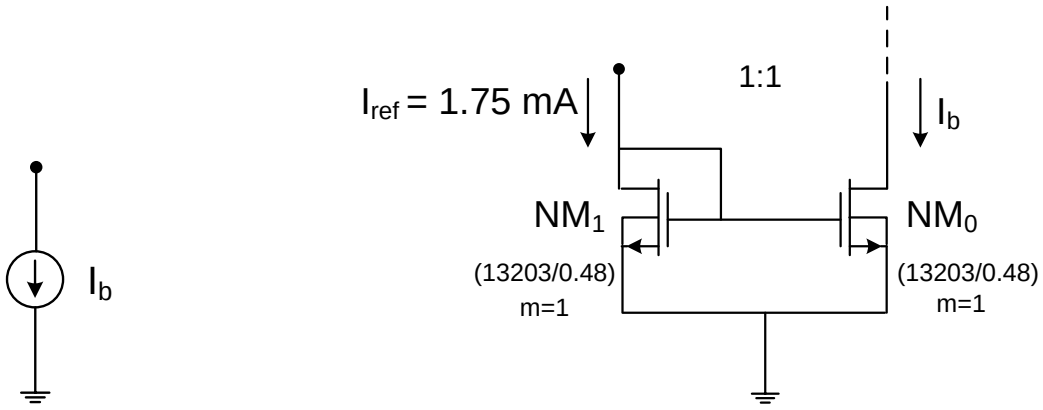
LNA stages, when the capacitors C_2 and C_3 allow the DC decoupling between the LNA and mixer, while achieving low impedance values at the RF frequency of interest.

On TIA, the Low-Pass Filter (LPF) is implemented by choosing the values of resistors R_4 and R_5 and capacitors C_4 and C_5. Its cut-off frequency was dimensioned to be slightly higher than the IF frequency, in order to attenuate the frequencies above IF.

The TIA's transresistance gain value, responsible for the current to voltage conversion, is 200 KΩ for the IF frequency (10 MHz). This value corresponds to the impedance of the parallel of resistor R_5 and capacitor C_4 (or R_4 and C_5) for the given IF frequency, which, for simplicity, can be considered as the correspondent resistor value.

Table 4.2: Resistor and Capacitor dimensions.

	R_1,R_2,R_3(kΩ)	R_4,R_5(kΩ)	C_1,C_2,C_3(ρF)	C_4,C_5(ρF)
Values	10	200	5	9



(a) Current source.

(b) Current mirror with all the transistors sizes (W/L) in μm.

Figure 4.1: The LNA's current mirror structure.

4.1.1 LNA simulation results

Inductorless, wideband, balun, lower-power and low-voltage are some of the LNA characteristics of this project. In section 4.1 a detailed explanation of the chosen considerations and values is done. Also, the dimensions of the transistors, shown in table 4.1, are chosen, in a way that are critical for obtaining the performance parameters. This LNA with differential output have to have a high gain and noise cancellation which causes a improvement in the linearity.

The differential gain simulation, represented in Fig. 4.2, was performed on AC trace simulations using the equation 3.11 as its auxiliary. The simulation result leads to the conclusion that the voltage gain circuit is approximately constant 17.9 dB up to 1 GHz and after less 3 dB its bandwidth has the value of 4.3 GHz.

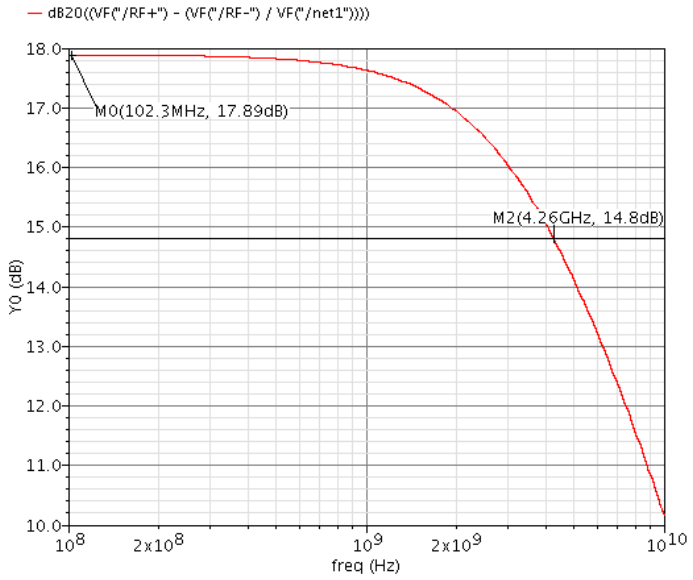


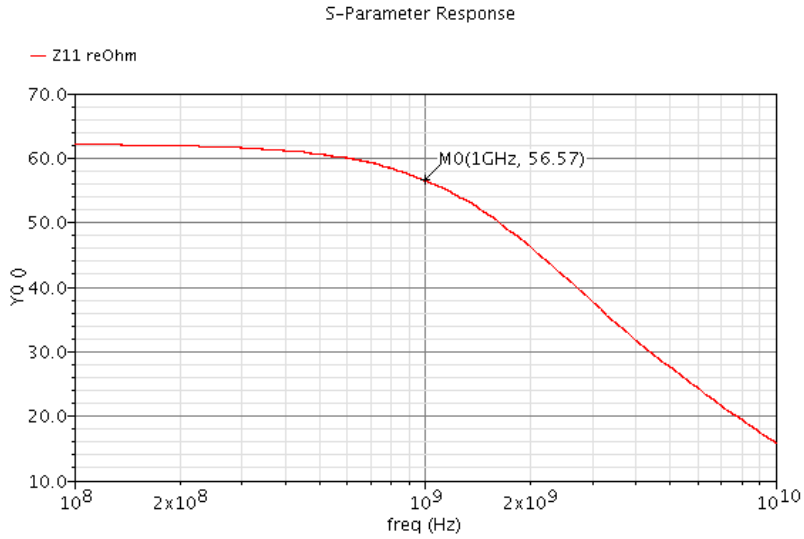
Figure 4.2: LNA Gain and Bandwidth.

The input impedance was design to approximate the value of 50 Ω using the equation 3.16. The simulation results are shown in Fig. 4.3(a) and Fig. 4.3(b). The value of the real part of the input impedance is 57 Ω and the imaginary part starts to be significant from 1 GHz.

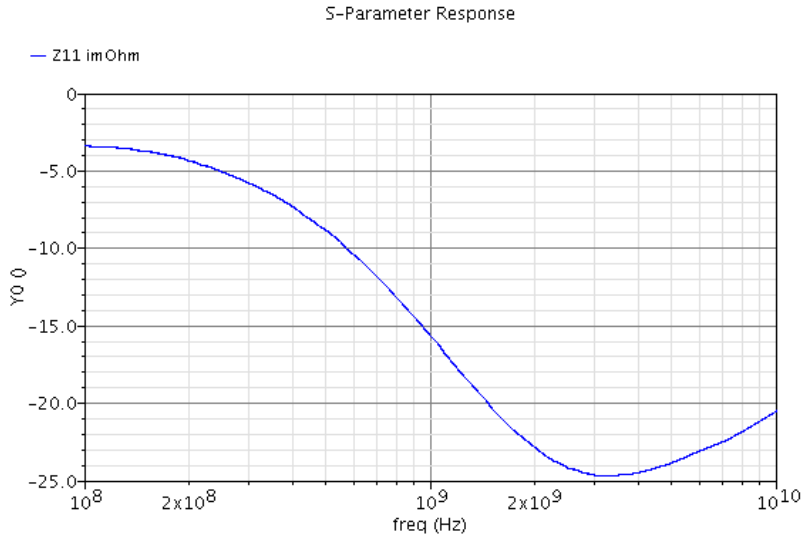
In the IIP_3 simulation, represented in Fig. 4.4, it's performed using two frequency values: the RF frequency and a tone separation frequency value different from the desired RF frequency for reasons concerning the convergence. The IIP_3 simulation has a value of 2.3 dBm, which isn't a good linearity, due to the intrinsic nonlinearities of MOSFET devices.

According with Fig. 4.5, the LNA' summary noise is composed by the noise sources that have greatest influence on its circuit. This simulation is performed in absolute noise, which gives the percentage of each individual noise source.

In summary noise, shown in Fig. 4.5, five noise sources appeared. The two PMOS transistors (M_3 and M_4), the NMOS transistor (M_2), the resistance R_S (inherent to the Port 0, this noise source isn't a noise of the LNA) and the transistor NMO, which corresponds to one of the transistors of the current mirror that is in parallel with transistor M_1. The noise parameters id and rn correspond to thermal noise of drain-source resistance and to thermal noise generated by the resistor R_S, respectively. From the simulation result is confirmed that equation 3.48 is valid and accurate, in spite of several approximations described in section 3.1.3. Also, the thermal noise of the transistor M1 is appropriately cancelled, which means that the balun is effective in the LNA circuit. The dominant noise in the MOSFET is the thermal, because of the PMOS transistors that operating in the triode region and the high gain which makes the flicker noise less influential in the



(a) Real Part



(b) Imaginary Part

Figure 4.3: LNA input impedance.

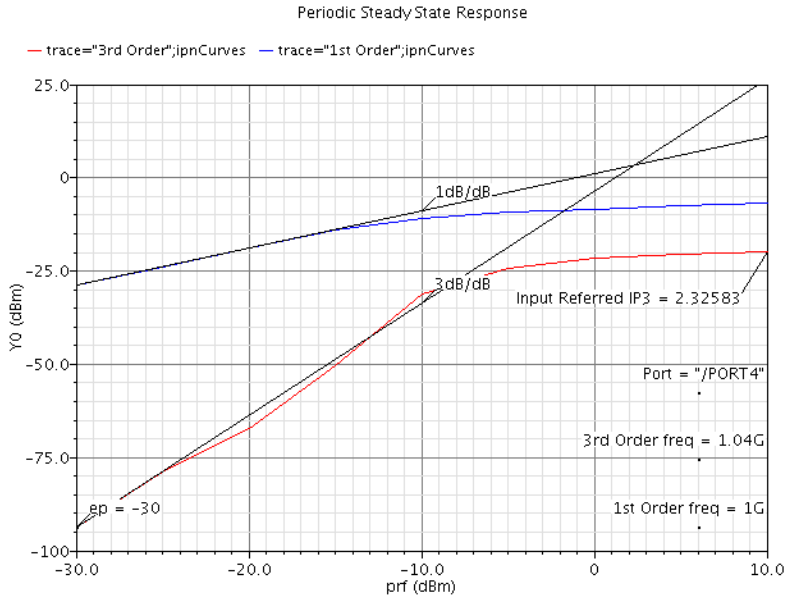


Figure 4.4: LNA IIP_3.

Device	Param	Noise Contribution	% Of Total	
/I20/NM0	id	1.32777e-17	32.76	Transistor of the current mirror
/PORT0	rn	1.32497e-17	32.69	Resistance Rs
/I20/M3	id	3.65528e-18	9.02	PMOS transistor M3
/I20/M5	id	2.65979e-18	6.56	NMOS transistor M2
/I20/M4	id	1.88009e-18	4.64	PMOS transistor M4

Spot Noise Summary (in V^2/Hz) at 1K Hz Sorted By Noise Contributors
Total Summarized Noise = 4.05342e-17
Total Input Referred Noise = 6.12432e-19
The above noise summary info is for noise data

Figure 4.5: LNA noise summary.

circuit. However, the most influential noise source of the LNA is the transistor MNO who is part of the current mirror, as shown in the simulation result of summary noise. The current mirror isn't considered ideal in the schematic, although it's neglected in the final equation of the noise factor (3.48).

The noise factor simulation, shown in Fig. 4.6, was performed to validate the low noise of the LNA. The simulation results lead to the conclusion that its value is around 4.8 dB, for the value of the RF frequency.

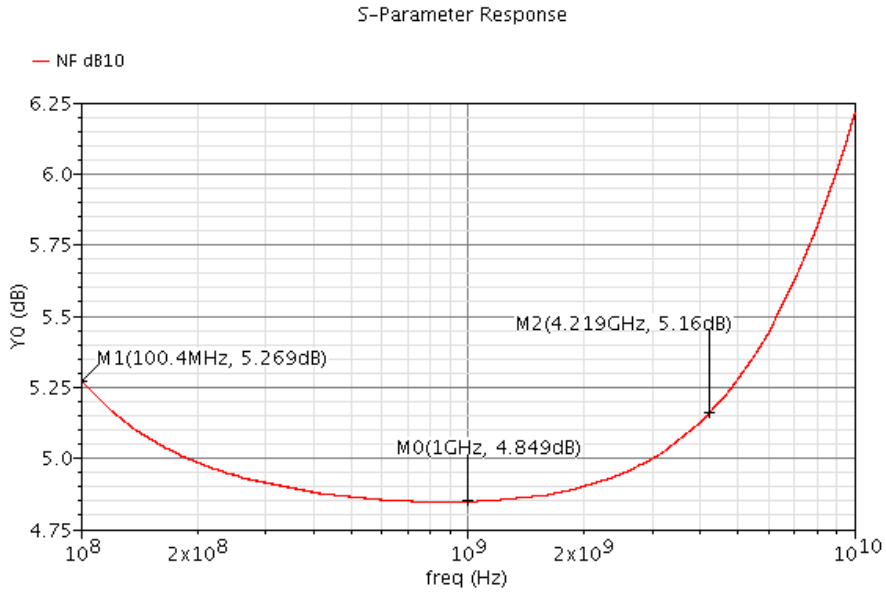


Figure 4.6: LNA Noise Figure.

Table 4.3 shows the summary results of theoretical and schematic. The theoretical results are obtained using the theoretical equations, demonstrated in the chapter 3.

Table 4.3: The theoretical and schematic results of the LNA.

	Z_{in} (Ω)	Band (GHz)	Gain (dB)	NF (dB)	Power (mW)	V_{DD} supply (V)
Theoretical	59	0.1-4.9	18.3	<3.5	1.9	0.6
Schematic	57	0.1-4.3	17.9	<5.2	1.9	0.6

Following the obtained results in the previous simulations, the LNA was chosen for comparison with others state-of-the-art, inductorless and balun LNAs. The LNA is the key block in terms of gain and distortion for the receiver circuit. The comparison of state-of-the-art LNAs is shown in Table 4.4.

The equations of consumption and FOM are presented in (4.1) and (4.2) with the purpose to help in the comparison of the LNAs.

$$P_{DC}[mW] = V_{DD}(I_{CG} + I_{CS}) \tag{4.1}$$

$$FoM[mW^{-1}] = \frac{A_{vdiff}}{(NF-1)P_{DC}[mW]} \tag{4.2}$$

Table 4.4: Comparison with State-of-the-art LNAS.

Ref.	Tech (nm)	V_{DD} (V)	Band (GHz)	Gain (dB)	NF (dB)	IIP_3 (dBm)	Power (mW)	FoM (mW^{-1})
[19]	65	1.2	0.2 - 5.2	15.6	<3.5	>0	14	0.34
[28]	90	2.5	0.8 - 6	20	<3.5	>-3.5	12.5	0.6
[29]	90	1.2	0.1 - 1.9	20.6	<2.7	10.8	9.6	1.3
[18]	130	1.2	0.2 - 3.8	11.2	<2.8	-2.7	1.9	2.1
[21]	130	1.2	0.2 - 6.6	19.8	<1.8	1.6	4.8	3.9
This Work	**130**	**0.6**	**0.1 - 4.3**	**17.9**	**<5.2**	**2.3**	**1.95**	**1.9**

Conclusions: The LNA's bandwidth satisfies the requirements for the target application. The LNA's voltage gain value is equivalent to the voltage gain values of the original MOSFET-only LNA [21] that was considered (in section 2.6.2.3), which is a positive result, having in mind the V_{DD} voltage supply reduction for the proposed circuit, in relation to the original one. The power consumption has a satisfactory value compared to the other from the table 4.4. Although the FoM result is slightly low than the other FoM LNAs, which is a drawback.

4.1.2 Receiver simulation results

The blocks that composed the receiver circuit are the LNA, mixer, LO and TIA, despite the last two being ideal, the analysis of the performance parameters is made. In the previous subsection, the LNA block is analysed because of its importance and influencing in the rest of the circuit, in terms of gain, linearity and bandwidth. However, when all blocks are grouped some transistors dimensions have had to be adjusted and optimized, as shown in table 4.5.

Table 4.5: Optimized transistors dimensions.

		I_D(mA)	W(μm)	L(μm)	$r_{ds}(\Omega)$	g_{ds}(mS)	g_m(mS)
LNA	M_1	1.63	66	0.12	454	2.2	20.15
	M_2	1.55	71.4	0.12	612	1.63	20.79
	M_3	1.63	52.8	0.12	254	3.93	8.61
	M_4	1.55	51.2	0.12	246	4.06	8.03
Mixer	$M_{5,6,7,8}$	-	115.2	0.12	-	-	-

As explained in section 3.1 of chapter 3, the LNA has to be carefully designed with the same magnitude value on both stages, to allow its output to be balanced and noise cancelled by satisfying the conditions balun. However, the following block after the LNA,

the mixer, is in current mode, which means that the RF signal at the input mixer must be in current. The LNA's transcondutance gain becomes essential, instead of the voltage gain, allowing the mixer to work in current mode. So, the transistors dimensions of the LNA are responsible for the RF signals, which have to have an approximate output current magnitude, as shown in Fig. 4.7. Also, in the Fig. 4.7 is possible to see the modulation effect of the Local Oscillator (LO) leakage, which proves the need for LO signal drivers.

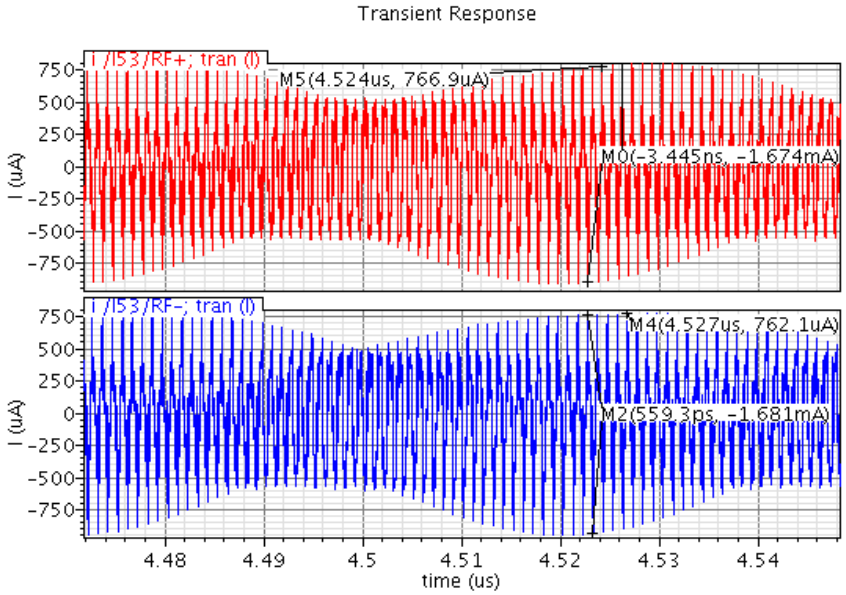


Figure 4.7: LNA output current.

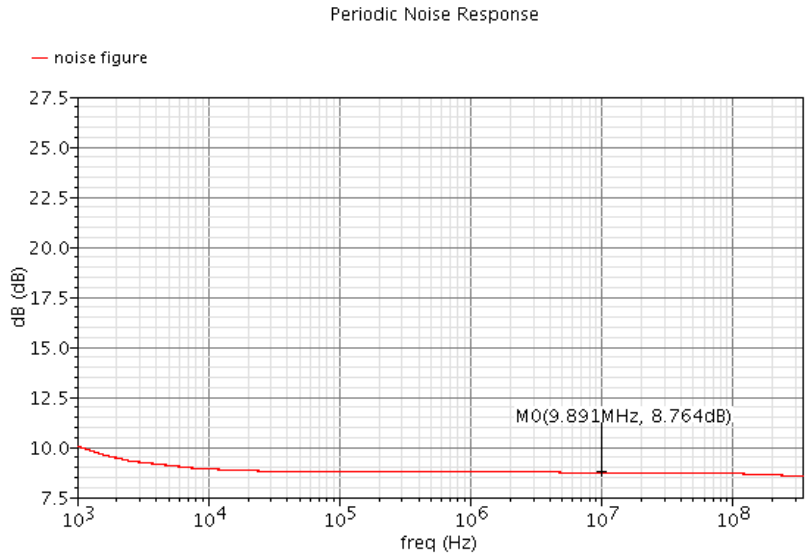
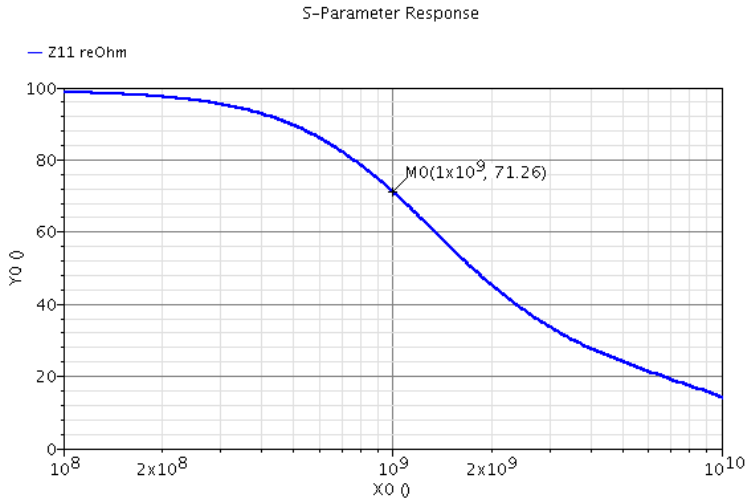


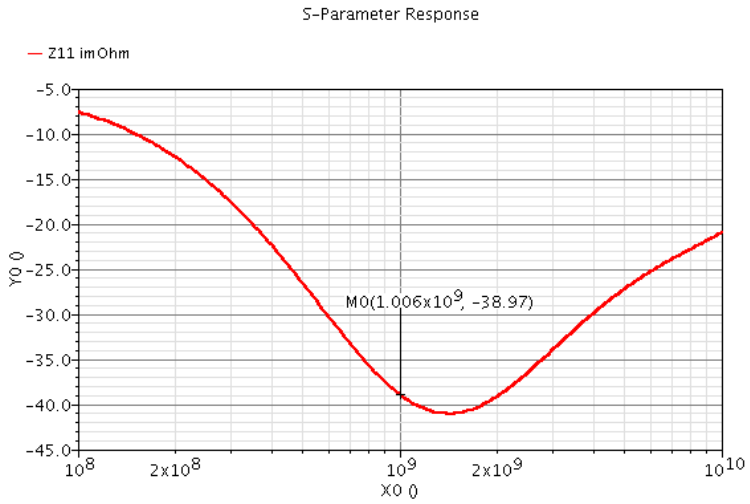
Figure 4.8: Receiver's noise figure.

Consequence of this changes make the magnitude of LNA's stages slightly different, so the noise cancellation isn't 100% and therefore, there is an attenuation on the voltage

gain, which means that there is a slight increase in the noise factor of the LNA and consequently in the receiver circuit. However, the fact that the mixer works in current mode minimizes the introduction of noise, especially noise flicker, and ensures a good linearity. Moreover, there is a threshold between the LNA and the mixer in terms of noise introduction in the receiver. In order to validate the low noise capabilities of the complete circuit, a noise figure simulation, shown in Fig. 4.8, was carried out for the differential IF output. The simulation's results lead to the conclusion that the circuit presents a low noise figure, around 8.7 dB, for a relatively wide band of frequencies close to the desired IF frequency.



(a) Real Part



(b) Imaginary Part

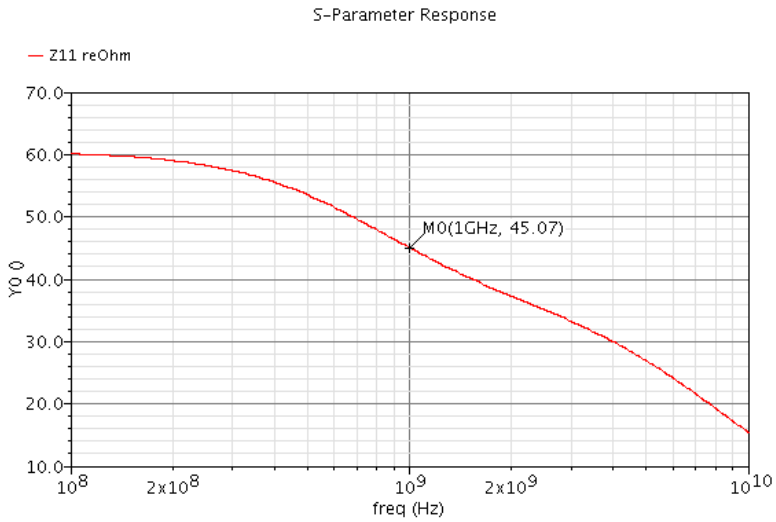
Figure 4.9: Mixer input impedance.

Another factor to consider is the mixer's input impedance value that must be lower than the LNA's output impedance, to ensure that the output current from the LNA flows for the next block, the mixer, and renders the current division nonexistent. From equation (2.43), which corresponds to the channel resistance R is responsible for the adaptation

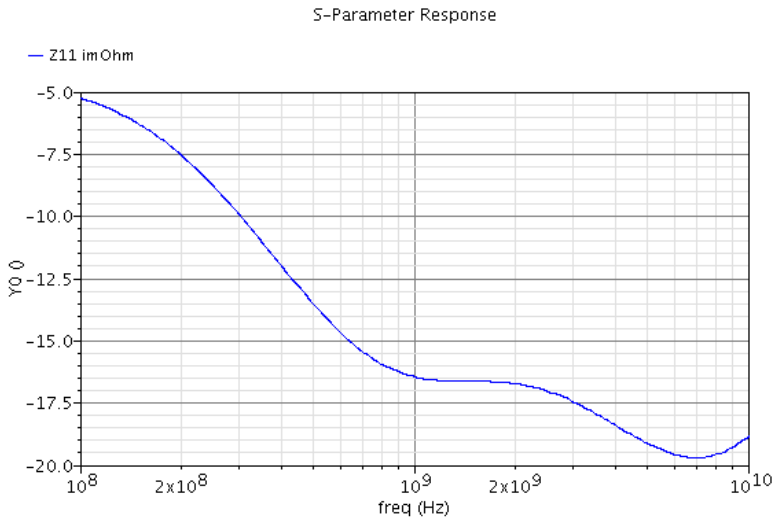
between the RF and IF inputs, the theoretical value is approximately 34 Ω.

To proceed with the confirmation of the mixer's impedance in the schematic of the receiver, the S-parameters simulation is run after disconnecting the LNA's connection from the mixer and place in each input branch of the mixer a DC port with a resistance of 50 Ω.

Therefore, the mixer's impedance will have a value that is influenced by the DC port with a resistance of 50 Ω in the RF input and by the input impedance of the TIA which is in series with IF input, who have an approximate condition of Z = 50 Ω + R [24]. According with the simulation results shown in Fig. 4.9(a) and Fig. 4.9(b), the real part has a value of 71 Ω and the imaginary part has a capacitive value.



(a) Real Part



(b) Imaginary Part

Figure 4.10: Receiver input impedance.

The simulation result of the receiver's input impedance is shown in Fig. 4.10(a) and

Fig. 4.10(b), where the real part of the input impedance has a value of 45 Ω and the imaginary part starts to have meaning from 1 GHz. The receiver's input impedance value is a little below to the expected value of 50 Ω for which the first block (LNA) and the antenna must match, however its value is close enough to the impedance matching.

For the IIP_3 simulation, shown in Fig. 4.11, the tones are 100 MHz apart from each other, a situation that would be ideal for an IF frequency value of 100 MHz. Even though this is not the chosen IF frequency, the results achieved with this value are also illustrative for a 10 MHz IF situation, as is desirable for this work. The IIP_3 simulation renders a value of -1.35 dBm.

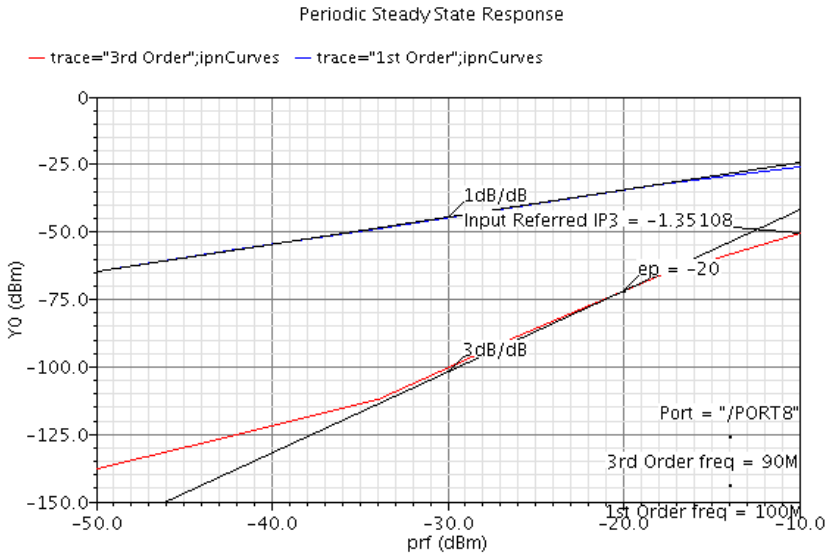


Figure 4.11: IIP_3 simulation.

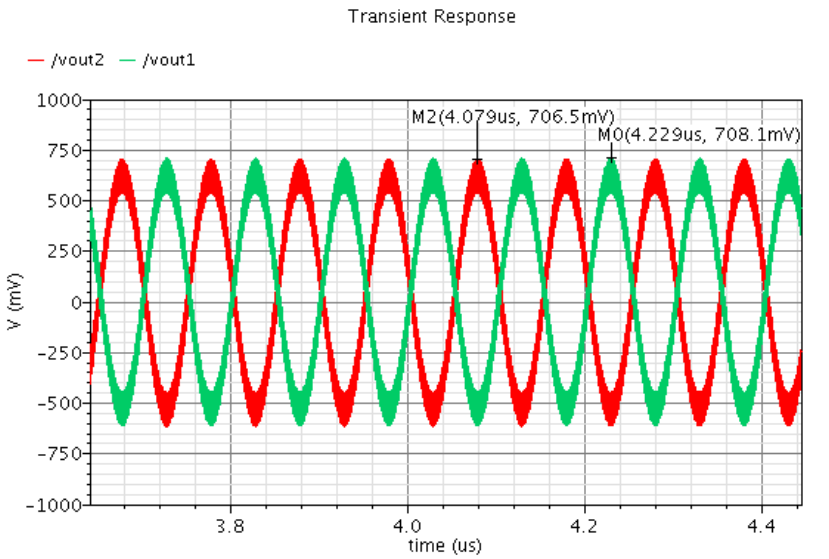


Figure 4.12: Output signals of the TIA.

In the mixer's output, the balanced current signal IF is converted to a balanced voltage signal and amplified by the TIA block. The TIA's output signals, shown in Fig. 4.12, have an approximate magnitude voltage and they are opposed to each other, which is a satisfactory result. The simulation result of the differential output signal of the TIA, shown in Fig. 4.13, has a peak to peak value of 2.3 V.

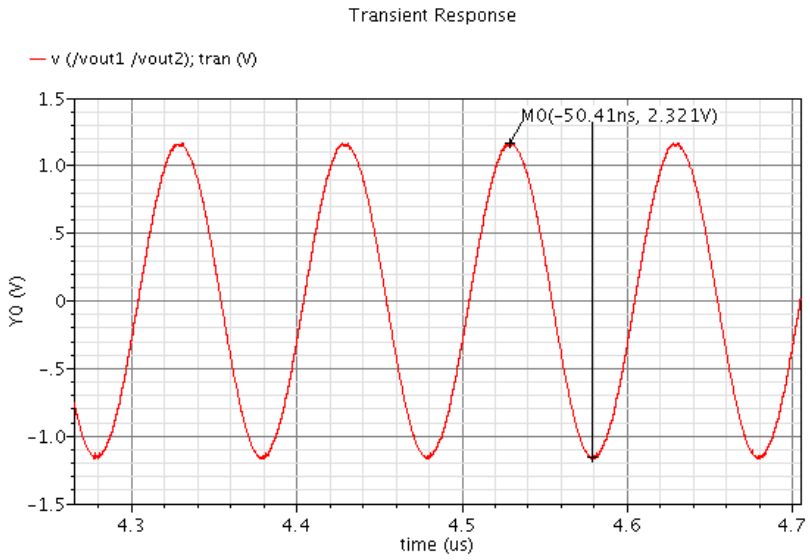


Figure 4.13: Differential output signal of the TIA.

The receiver's conversion gain is influenced by each block that constitutes it. However, the blocks with higher responsibility in conversion gain are the LNA and the TIA, as shown in equation 3.49. The value of the input single-ended of the LNA is - 20 dBm, which is converted to an approximate value of 63.23 mV. The ratio between the differential output signal IF from the TIA, shown in Fig. 4.13, with the input voltage signal from the LNA's single-ended has a value of 31.5 dB.

Table 4.6 presents a resume of the final results for this presented circuit. The results of the complete circuit include conversion gain, noise figure, IIP_3 and power consumption.

Table 4.6: Final receiver simulation results.

Tech (nm)	Voltage Conversion Gain (dB)	NF (dB)	IIP_3 (dBm)	Power (mW)	V_{DD} supply (V)
130	31.5	<8.7	-1.35	1.9	0.6

Conclusions: The voltage conversion gain of the complete circuit is a result of the contribution of the LNA's gain and the TIA's gain. The transimpedance gain of the TIA has a large contribution in this total conversion gain. The noise figure result is slightly higher than the LNA's noise figure, meaning that the mixer introduces some noise but not as

much as an active mixer would. The IIP_3 has a satisfactory value due to the reduced distortion introduced by the LNA and mixer.

4.2 Layout design and post-layout simulations

This section focuses on the layout of the proposed circuit, represented in Fig. 4.14, where is performed some physical verifications. The physical verifications are the design rule check (DRC), the layout versus schematic (LVS) and the layout parameter extraction (LPE), where is verified if the design of the layout circuit is correct and robust [30, 31]. Then, are accomplished and demonstrated some post-simulations plots which are more realistic because of the inclusion of RC parasites. Thus, the post-layout results are compared with the schematic simulations results from the subsection 4.1.2 in table 4.6. This comparison is inevitable to understand, if in terms of circuit's implementation and design, the choices that were made allow the circuit to work in more realistic circumstances. In addition, some problems that have appeared in the layout phase are pointed out and some alterations are made on the circuit.

The layout of the proposed circuit, shown in Fig. 4.14, is integrated by the LNA, the current mirror that is responsible by setting the same current for the transistors M_1 and M_3, the mixer and the capacitors C_2 and C_3 between the LNA and mixer, which makes a total die area of 305x134.5 μm^2. The devices that are connected were properly adjacent positioned in the whole circuit layout. In order to guarantee the current flowing through the circuit, the maximum current density values are defined by the dimensioning of the widths of the metal connections and the number of contacts and vias. Also, the circuit's layout included the use of guard rigns, consisting of PTAP ring, for all the transistors and components.

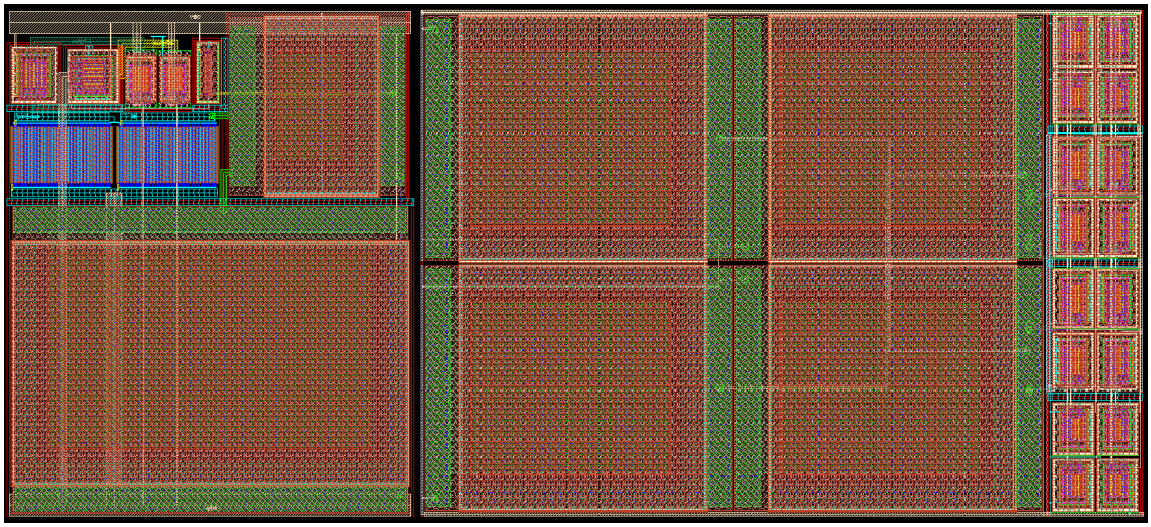
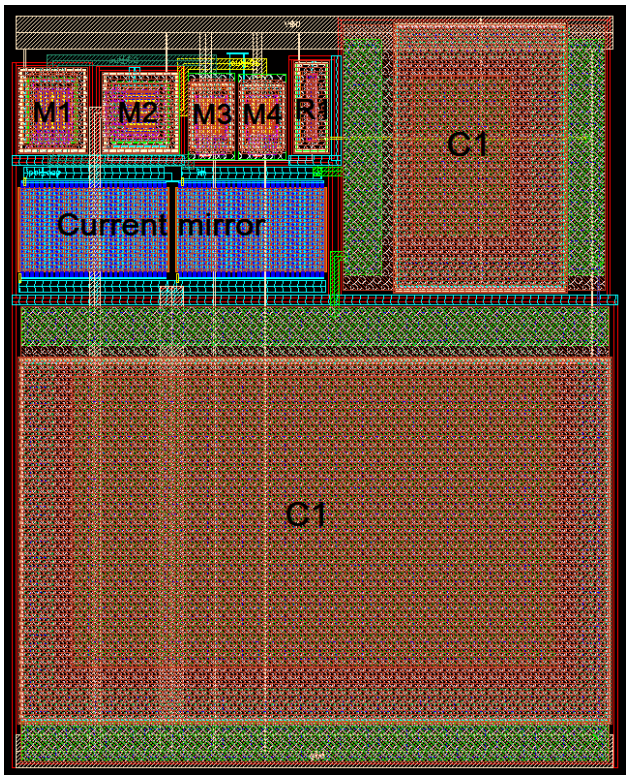
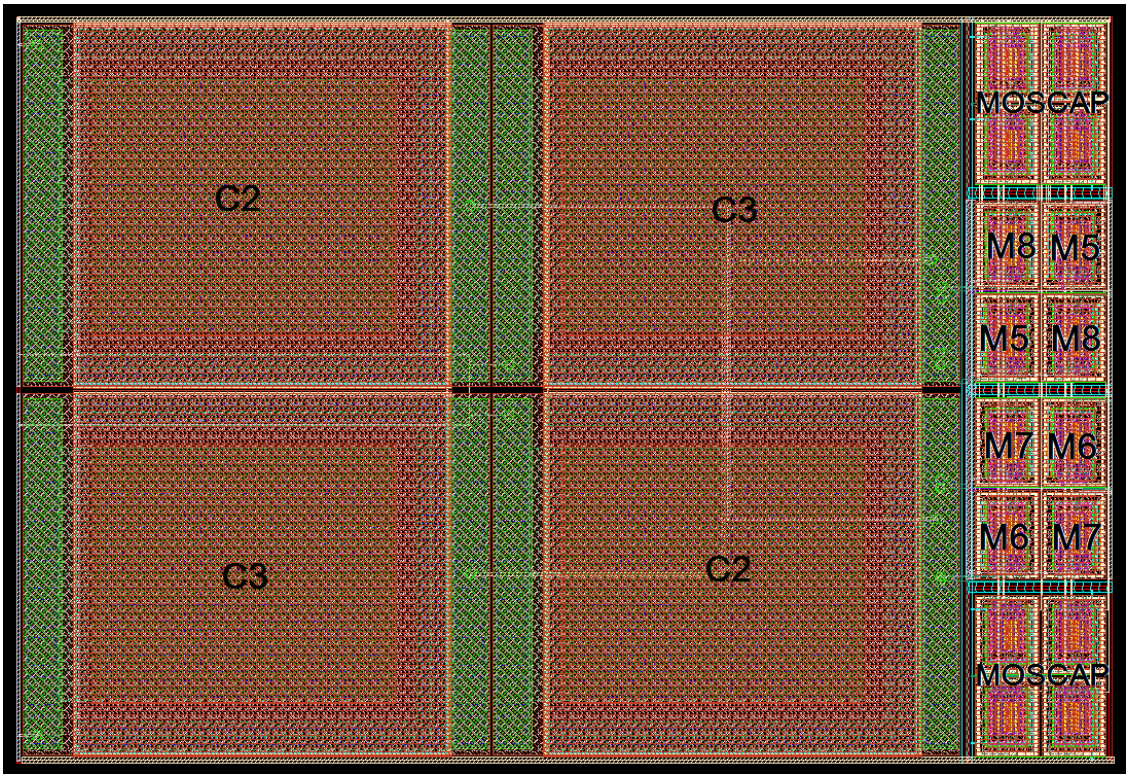


Figure 4.14: The proposed circuit layout.



(a) LNA.



(b) Mixer.

Figure 4.15: The receiver components identification of the layout design.

The technology used for the layout design has some considerations to take into account, the RF MOSFETs are sized for the maximum possible number of fingers to minimize the effect of the parasites, the resistors and capacitors are substitutes by the models of high-resistance (HR) poly RF and MIM capacitor RF, respectively. Although, the current mirror transistors use the technology of 130 nm CMOS and its layout was made, as shown in Fig. 4.14, these transistors didn't work when the post-simulation was initiated, so it was necessary removed them from the layout design to obtain the simulation results. The mixer circuit layout is placed in a common centroid configuration, so that could be better matched. Also, is included some additional transistors connected in diode configuration, with the purpose of help in the reduction of noise.

The table 4.7 summarizes the layout design parameters mainly from the LNA.

Table 4.7: The layout design parameters.

		I_D(mA)	W(μm)	L(μm)	$r_{ds}(\Omega)$	g_{ds}(mS)	g_m(mS)
LNA	M_1	1.63	66	0.12	436	2.3	20.04
	M_2	1.47	71.4	0.12	638	1.57	20.13
	M_3	1.63	52.8	0.12	271	3.69	8.79
	M_4	1.47	51.2	0.12	231	4.33	7.6
Mixer	$M_{5,6,7,8}$	-	115.2	0.12	-	-	-

The post-simulation results from the parameters of the table 4.7 are presented in Figs. 4.16, 4.17, 4.18.

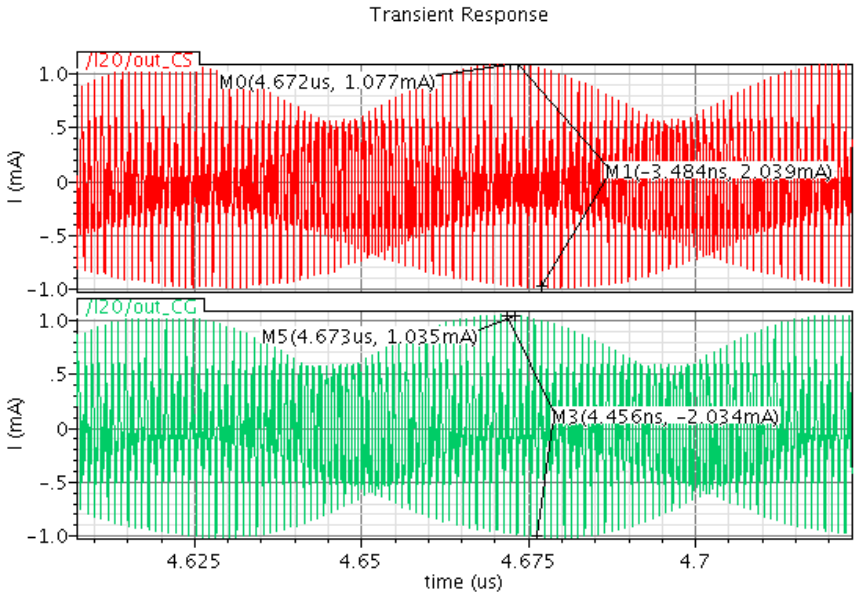
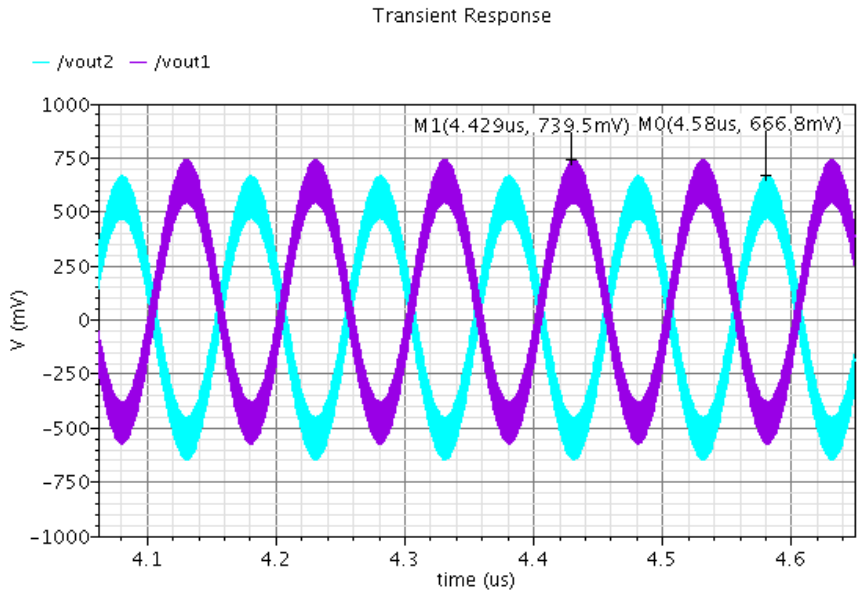
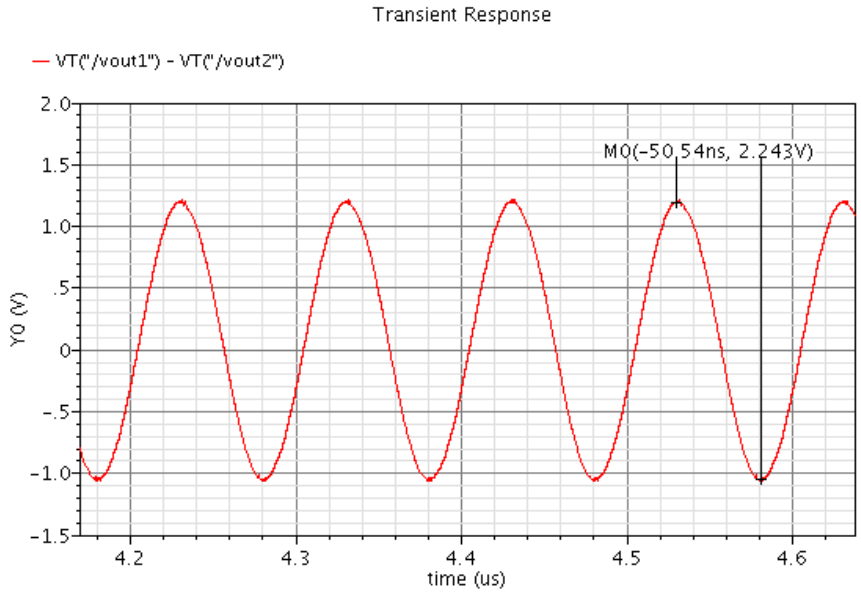


Figure 4.16: The output current of the LNA.



(a) Output signals of the TIA



(b) Differential output signal of the TIA.

Figure 4.17: Receiver's output signals.

The post-simulation results and the parameters from the table 4.7 show how the receiver circuit behaves after the layout design. In case of the parameters, the transistors dimensions are equals to the optimized schematic receiver from the subsection above 4.1.2 but the transistors specifications have slightly changed compared with the parameters from the table 4.6. The transistors region are still the same, the transistors M_1 and M_2 remain in the saturation region ($g_m > g_{ds}$) and the transistors M_3 and M_4 which are responsible for the LNA's output impedance, stayed in the triode region ($g_m < g_{ds}$) but near of the boundary of the saturation region. Another significant change in the parameters is the current of the CS stage, its value is slightly below from the expected one (table 4.6), although the values of the transcondutance gain and bandwidth are attenuated, the magnitude current of the LNA output is equivalent, shown in Fig. 4.16. This fact is necessary for mixer to operate in current mode as a multiplication operation between two signals, the LO signal and the RF signal that comes from the LNA.

The output signal from the TIA was converted of current to voltage, demonstrated in Fig. 4.17(a), presents an amplitude value slightly different in the two outputs but hasn't enough relevance. In the differential output signal of the TIA (Fig. 4.17(b)), the peak to peak value decreases slightly compared with the schematic. Its value is directly proportional to the conversion gain value, so also decreases a little bit.

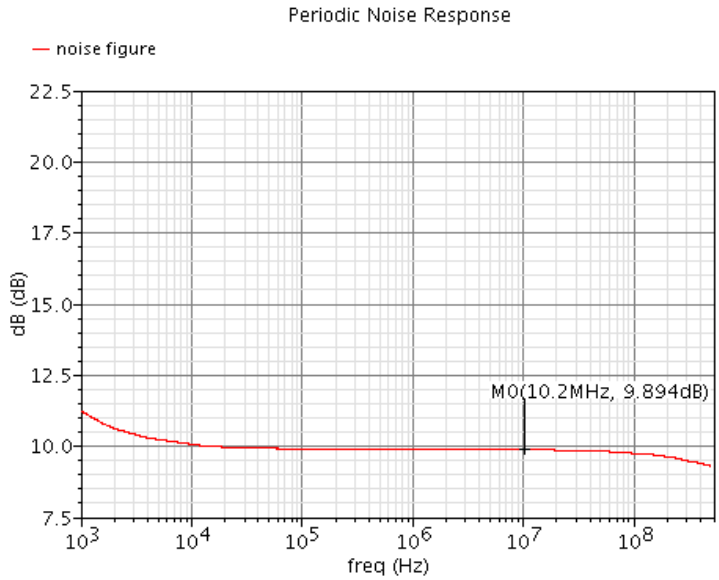


Figure 4.18: Receiver's noise figure.

The main difference relatively to the pre-layout results is in the noise figure, which increases by approximately 1 dB, shown in Fig. 4.18. This is due to the thermal noise of the transistor M_1 being not fully cancelled and the influence from the parasites on the circuit.

Table 4.8 presents a resume of the comparison of the final results between the schematic

and post-layout.

Table 4.8: The schematic and layout simulations results.

	Tech (nm)	Voltage Conversion Gain (dB)	NF (dB)	IIP_3 (dBm)	Power (mW)	V_{DD} supply (V)
Schematic	130	31.5	<8.7	-1.35	1.9	0.6
Layout	130	30.9	<9.9	N/A	1.86	0.6

4.3 Discussion

There are several classic RF receiver architectures with different complexities and performances. However, only some of them are suited for low-power applications, namely the Low-IF or direct conversion architectures. In order to integrate with an energy harvesting power supply, the receiver has to be designed taking into account the low supply voltage requirements. In terms of low supply voltage, the design and optimization of the LNA module was important for having a successfull reduction of the V_{DD} voltage supply for the proposed circuit, set at 0.6 V, which is half of the value of the supply voltage that served as a starting point for the original LNA, presented in [21].

A double-balanced passive mixer is designed in conjunction with the LNA to work in current mode, allowing a good linearity. Moreover, the passive mixer does not influence the overall power consumption. Also, the receiver circuit doesn't include the local oscillator and OTA designs, considering them as ideal devices. Although it has a simple inductorless architecture with reduced area and cost, its design's simplicity results in a low Power Supply Rejection Ratio (PSRR).

This receiver's proposed circuit presents a post-layout power consumption value of 1.89 mW, which refers to the consumption of the two blocks, the LNA and mixer. The power consumption value is calculated through the sum of the currents flowing from the two LNA's stages, which are 1.63 mA and 1.47 mA, shown in table 4.7, and then multiplied by the V_{DD} supply voltage.

The receiver's simple architecture is suitable for modulation schemes with reduced complexities. Therefore, the modulation scheme chosen for the proposed receiver front-end circuit was the on/off keying (OOK). The OOK modulation is the most basic modulation, which is widely used in close-range communications, low data-rate and low-cost applications. The architecture simplicity and the requirements for the target application lead to the choice of the previously mentioned simple modulation scheme [32].

For all that, in order to have sense of the typical power consumption and supply voltages of other receivers for WSN applications, some examples are presented in table 4.9. The parameters given in table 4.9, are the technology, the type of modulation scheme, the supply voltage and the power consumption. The chosen receiver examples presented in

the table work with simple modulation schemes, thus allowing a relevant comparison.

Table 4.9: Comparison of WSN receivers.

Parameters	[5]	[33]	[34]	[35]	[36]	This work
Technology (nm)	90	130	180	130	180	130
Modulation	OOK	OOK	FSK	FSK	OOK	OOK
Supply Voltage (V)	-	1	1	1.2-1.5	1.4	0.6
Power Consumption (mW)	1.8	0.88-2.5	2.17	1.92-2.4	0.5-2.6	1.86

5

Conclusion and Future Work

5.1 Conclusion

In this thesis a CMOS low-power and low-voltage RF receiver designed in a standard CMOS technology was presented. It has an inductorless wideband architecture with a reduced area and a consequently reduced cost. The circuit is suitable for the target application, in which the power is intended to be supplied by an energy harvesting source. The specification requirements for this energy-autonomous WSAN, where the piezoelectric energy harvesting was chosen as its power source, are the power consumption and supply voltage.

This work was validated through the design and implementation of the key circuit blocks, where the theoretical analyses, the behaviour, the characteristics, the parameters and the simulations were presented. Despite of the receiver circuit simplicity, the results obtained in conversion gain, noise factor, linearity and power consumption are acceptable. Therefore, the solution presented in this work is suitable to cope with the requirements of energy-autonomous WSAN application.

The proposed circuit includes the implementation of a wideband balun LNA able to cancel noise and distortion, working at 0.6 V supply voltage, and a double-balanced passive mixer which is designed in conjunction with the LNA, to work in current mode. Also, together with the implementation of LNA and mixer, the LO and TIA modules help to achieve the results of a total voltage conversion gain of 31.5 dB, an IIP3 value of -1.35 dBm, and a noise figure lower than 9 dB. The total power consumption achieved is 1.9 mW and the total circuit area is 305x134.5 μm^2.

Moreover, the simulation results of the implemented circuit are compared with the results from the post-layout simulations, which show that the concept may be optimized

and future research can lead to promising results.

5.2 Future Work

In the present work there are always changes and improvements that can be made, which would make this project more competitive. The following topics are suggested for improvement of future work that fall outside the scope of this thesis.

The implementation and design of this project obtained reasonable values of parameters and dimensions for the work application. However, in the layout phase some problems appeared in the current mirror transistors. The LNA's current source was not considered as an ideal current source, and a current mirror was added, implemented with standard 130 nm CMOS transistors. Nonetheless, some problems occurred with the post-layout version of the current mirror for the post-layout simulations. This is the reason why the current mirror was only used in its schematic version, for both types of simulations. A plausible change would be to modify the current mirror transistors for RF transistors. However, their characteristics and dimensions would be different, since they have different models. The most immediate consequence of this change would be in the noise figure of the proposed circuit, which would increase slightly.

Furthermore, the receiver includes two ideal modules, which are the local oscillator and the TIA. As future work, an interesting extension of the proposed receiver would be to include the previously mentioned ideal modules in the system design, paying attention to the requirements for the WSN application.

After the full design and implementation of the proposed RF receiver, the inclusion of the RF transmitter could be considered.

Another suggestion is to design the proposed circuit in a lower CMOS technology to investigate if a better compromise between cost, area, power, and performance could be achieved.

A solution for a WSAN receiver whose power is supplied by an energy harvesting solution is presented in this thesis. The next step in the WSAN co-design consists in validating the joint operation of the two systems, with the goal of integrating them in a WSAN system-on-chip (SoC).

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Published Papers

Stability improvements in a Rail-to-Rail Input/Output, constant Gm Operational Amplifier, at 0.4 V operation, using the low-voltage DTMOS technique

5th Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS)

Stability improvements in a Rail-to-Rail Input/Output, constant G_m Operational Amplifier, at 0.4 V operation, using the low-voltage DTMOS technique

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Abstract. The use of the dynamic threshold MOS (DTMOS) technique is evaluated in a two-stage rail-to-rail Input/Output, constant G_m amplifier. The proper choice of specific transistors in which the technique should be used is presented, as well as the resulting improvements, mainly regarding stability of the circuit at low voltage operation. The DTMOS technique is used in the NMOS transistors of the folded-cascode input stage, allowing the circuit to be stable at V_{DD} = 0.4 V, with equivalent gain and gain-and-bandwidth product (GBW) values achieved with the same V_{DD} value, for the initial circuit operating at 0.8 V. The implemented changes allow the circuit to be stable at low voltage operations without requiring any increase in the cascoded-Miller compensation capacitors, saving circuit area and, consequently, cost.

Keywords: Low-voltage DTMOS technique; Low supply voltage OPAMP; Low-voltage OPAMP stability issues.

1 Introduction

The general tendency for reducing the supply voltage in ICs represents a challenge for analog amplifier designers, in terms of maintaining required gain levels, bandwidth (BW) and stability. In terms of stability and frequency compensation, several techniques can be implemented, but the solutions represent an increase of the circuit area, since they often include the need of additional capacitors.

As a starting point for the testing of the DTMOS technique, an operational transconductance amplifier (OTA) was chosen. The choice is based on an original, rail-to-rail Input/Output, constant G_m OTA, described in [1], and operating at a 0.8 V supply. The technology used for the initial amplifier was the purely-digital 180 nm CMOS, whereas the present implementation, fully supported in the initial study, [1], was simulated using the CADENCE, with an UMC 130 nm, purely-digital, CMOS technology. The change in technology doesn't represent a relevant factor in the overall behavior of the circuit.

The main objective of this work is to improve the gain, GBW and stability of the original amplifier, and to guarantee that the OTA still works, with reasonable performance, when operating at much lower supply voltages.

The DTMOS technique was the technique chosen to reach the objectives, and consists in connecting the bulk of a transistor to its gate terminal. This allows the bulk voltage to be variable, instead of being fixed at ground or V_{DD} (NMOS or PMOS, respectively) [2]. The transistor suffers from body-effect, in this configuration, since the voltage between the source and bulk terminals is not zero. However, the transcondutance that is a result of the body-effect contributes, positively, to the total transcondutance of the transistor, being this contribution an increase of approximately 20-to-30% of the transcondutance of the transistor. This means that in the DTMOS configuration, the body-effect of a transistor is not a degrading factor in its G_m, but rather an improvement.

The disadvantages of using the DTMOS technique are the increase of the parasitic capacitances in the transistor, which can ultimately lead to a loss of circuit BW, and the possibility of a latch-up problem. In the case of this particular application and circuit, the latch-up situation is not a real problem, because there won't be sufficient voltage to trigger the effect, since the intended test supply voltages will be lower than 0.7 V, which is the typical problematic threshold that allows that effect to be a problem. In terms of the increase of the parasitic capacitances, and consequent decrease in BW, the situation can be dealt with separately, although the changes in the parasitic capacitances are not relevant enough to reflect some problematic difference in terms of the BW.

2 Relationship to Collective Awareness Systems

Collective Awareness Systems that are capable of harnessing collective intelligence, allowing the creation of a network of distributed knowledge and data from real environments, include a multitude of individual subsystems that must be able to collect and transmit the actual information that is shared in the system. These subsystems may include a wide range of different devices and applications, but they usually consist in wireless and portable devices [3] for which concerns like power consumption and autonomous lifetime are very pertinent.

The DTMOS low voltage technique used in this work is one of the techniques that allow reduction in circuit supply voltage, and consequently power consumption. Moreover, as it will be demonstrated in this paper, the use of DTMOS in certain specific devices can improve the stability of the circuit, which translates into smaller area (there is no need for larger compensating capacitors). The significant supply voltage reductions that can be achieved with this technique are promising for the hardware implementations of Collective Awareness Systems or any other system where power consumption and cost (silicon area) are key factors.

3 Amplifier Description

3.1 Initial Amplifier

The 0.8 V, rail-to-rail Input/Output, constant G_m OTA, whose schematic is presented in Fig. 1, consists of two stages.

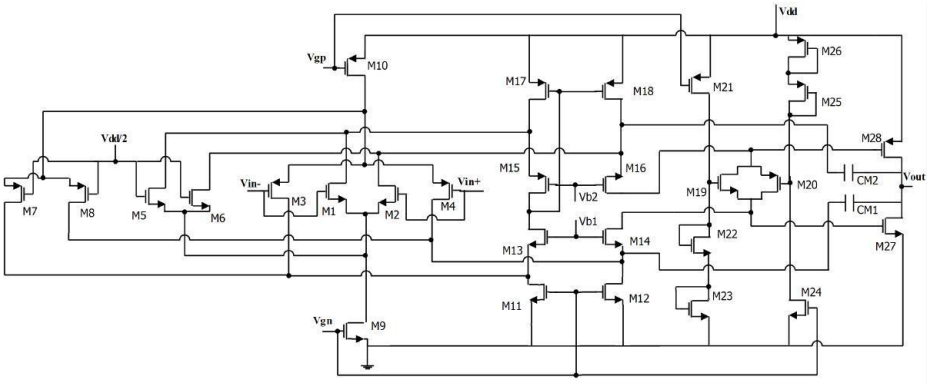

Fig. 1. Initial Operational Amplifier

The rail-to-rail folded-cascode input stage includes two differential pairs in parallel, consisting of the transistors M1, M2 (NMOS differential pair), M3 and M4 (PMOS). This configuration allows rail-to-rail operation at the input. For high common-mode voltages at the input, the NMOS differential pair is on, while for low common-mode voltages it is the PMOS differential pair that is on. For medium levels of the common-mode voltages, both differential pairs are on, increasing the current flowing to the summing circuit and consequently increasing the G_m. To avoid this increase in the transcondutance, since it is desirable to have it constant for the whole range of common-mode voltages, the current switches M5 to M8 are added. The following folded-cascode configuration is responsible for the summing of the signals (current) coming from the complementary differential pairs.

The class AB output stage features, as stated above, the cascaded-Miller frequency compensation technique, which includes the capacitors CM1 and CM2. Class AB operations are made possible by M19 and M20. These transistors are driven by the signal currents coming from transistors M14 and M16 and are polarized by the diode-connected transistors M22, M23, M25 and M26. The output transistors M27 and M28 are in common-source configuration to allow rail-to-rail operations at the output. The M27 transistor functions at the positive swing, while M28 takes care of the negative swing. The frequency of non-dominant pole is shifted to higher frequencies by the cascoded-Miller frequency compensation technique.

3.2 Proposed Modifications in the Original Amplifier

The low-voltage DTMOS technique was chosen as the approach to use because of the simplicity of the implementation, since it basically consists in disconnecting the bulks of the PMOS and NMOS devices, respectively from V_{DD} and V_{SS}, and re-connect them to the gate terminal [4, 5].

Many possible configurations have been simulated and evaluated, using the DTMOS technique applied to different sets of transistors. The best results, taking into account simplicity and gain results, were achieved using the DTMOS technique only in the NMOS cascode devices M13 and M14. Notice that the DTMOS technique also has the benefit of reducing the threshold voltage of the transistor. Since NMOS transistors have a higher threshold voltage than PMOS, it is understandable that it is preferable to use the DTMOS technique in the NMOS cascode transistors rather than in the PMOS. This requires fabrication processes either with triple-well or with deep-Nwell but this is clearly the case, for all state-of-the-art deep nano-scale CMOS technologies.

4 Amplifier Performance

4.1 Electrical Simulations of the Original Amplifier Circuit

The simulation results achieved with the initial configuration of the circuit ported into the 130 nm CMOS technology (the original circuit, without the use of the DTMOS technique) are presented in Table 1. The presented results include simulations run under different supply voltages, focusing on the values of DC gain, GBW and Phase Margin (PM).

Table 2. Simulated results for the initial configuration of the amplifier circuit.

V_{DD} (V)	Gain (dB)	GBW (kHz)	Phase Margin (^{o})
1.2	82.62	857	> 56
0.8	82.58	864	> 56
0.7	81.16	824	> 56
0.6	81.44	833	52
0.5	78.5	818	56
0.4	72.15	878	53
0.3	57.7	794	51

The simulated PM is evaluated at a typical closed-loop gain of 6 dB, for each V_{DD} value. The presented PM results are lower than 55 ^{o}, which leads to the conclusion that the circuit is not stable for any of these supply voltages. In terms of DC gain and GBW, the values decrease as a consequence of the lowering of the V_{DD} value, as it is expected. However, the decrease in those values is not as substantial as was estimated, revealing that the topology of the circuit is capable of maintaining both the

gain and the GBW performance parameters even at lower supply voltages (i.e., below 0.8 V).

4.2 Re-Design of the Amplifier using DTMOS

For the circuit amplifier including the proposed changes, the same simulations have been carried-out, under the same conditions (common-mode voltages at 55 % of V_{DD}, the PM measured with a closed-loop gain of 6 dB). The results are summarized in Table 2.

Table 2. Results for the new circuit configuration (DTMOS).

V_{DD} (V)	Gain (dB)	GBW (kHz)	Phase Margin (°)
1.2	80.37	887	> 60 (higher)
0.8	79.54	844	> 60 (higher)
0.7	79.14	902 (higher)	> 60 (higher)
0.6	79.5	872 (higher)	57 (higher)
0.5	77.14	909 (higher)	61 (higher)
0.4	72.45 (higher)	924 (higher)	60 (higher)
0.3	58.82 (higher)	794 (same)	59 (higher)

As it can be observed in Table 2, there are just minor improvements in the DC gain and in the GBW. The most significant improvement is the PM parameter, particularly at very low supply voltages below 0.6 V. Since the values are superior to 55°, the OTA circuit is now stable for those V_{DD} values and can operate down to 0.3 V.

The gain and phase plots are presented in Fig. 2 and in Fig. 3, for a 0.4 V supply voltage. This V_{DD} value was chosen as a reference example because it is half the value of the supply voltage for which the original circuit was designed (which constitutes, by itself, a significant reduction in the supply voltage) and because it presents good gain, GBW and PM results, in comparison to the results achieved by the original circuit, for that same V_{DD}.

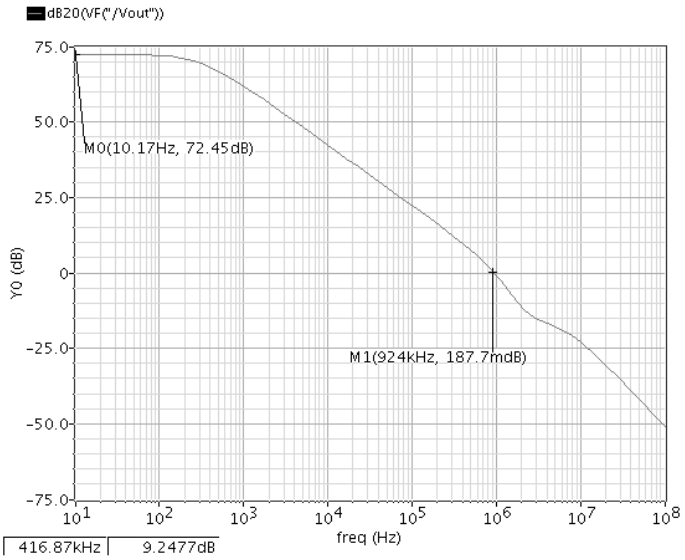

Fig. 3. Gain trace.

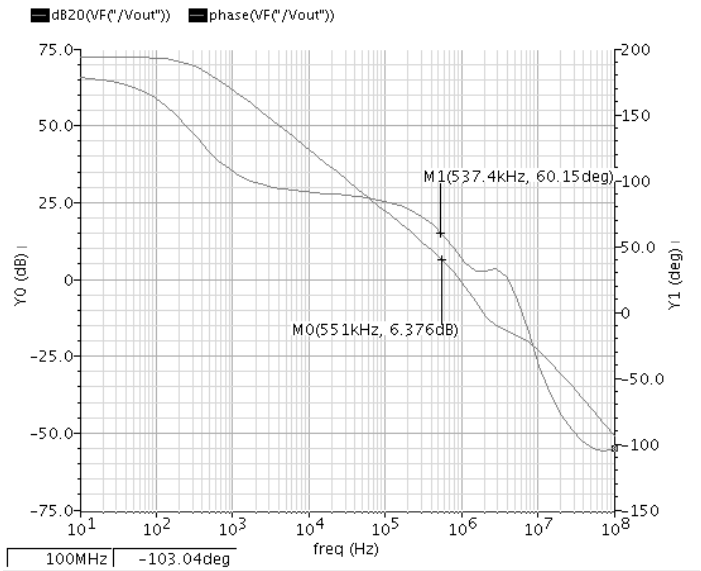

Fig. 3. Gain and Phase traces.

5 Conclusions

It has been demonstrated in this paper that, using DTMOS in a couple of specific devices of a two-stage rail-to-rain Input/Output, constant G_m OTA can improve its stability whilst operating at very low supply voltages. The proper choice of specific transistors in which the technique should be used has been presented, as well as the resulting improvements. The implemented changes allow the circuit to be stable at low voltage operations without requiring any increase in the cascoded-Miller compensation capacitors, saving circuit area and, consequently, cost.

The significant supply voltage reductions that can be achieved with this DTMOS technique are, therefore, quite promising for the hardware implementations of Collective Awareness Systems, in which amplifiers are of paramount importance, and where power consumption and cost (silicon area) are limiting factors.

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Piezoelectric energy harvester for a CMOS wireless sensor

5th Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS)

Piezoelectric energy harvester for a CMOS wireless sensor

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Abstract. The emerging of collective awareness platforms opened a new range of driven forces that will converge to more sustainable systems. To achieve this task, these platforms have to support an increasing number of more sophisticated remote sensors and actuators that will need to cooperate smartly and strongly with each other in a mesh type of intelligent interconnectivity. These remote smart miniaturized nodes can add noninvasive intelligence but suffer from lifetime performance due to the small quantity of energy available in micro batteries. Therefore, harvesting energy from the environment is a promising technique. This work presents the study and experimental evaluation of a flexible piezoelectric material to validate the use of a piezoelectric harvester in a CMOS wireless actuator/sensor node.

Keywords: Energy harvesting, piezoelectric transducers, self-powered, micro-systems, smart systems, wireless sensor nodes, MEMS, WSN

1. Introduction

The recent advances in ultra-low-power device integration, communication electronics and Micro Electro-Mechanical Systems (MEMS) technology have fuelled the emerging technology of Wireless Sensor Networks (WSNs). The spatial distributed nature of WSNs often requires batteries to power the individual sensor nodes. One of the major limitations on performance and lifetime of WSNs is the limited capacity of these finite power sources, which must be manually replaced when they are depleted. Moreover, the embedded nature of some of the sensors and hazardous sensing environment make battery replacement very difficult and costly. The process of harnessing and converting ambient energy sources into usable electrical energy is called energy harvesting. Energy harvesting raises the possibility of self-powered systems, which are ubiquitous and truly autonomous, and without human intervention for energy replenishment. Among the ambient energy sources such as solar energy, heat, and wind, mechanical vibrations are an attractive ambient source mainly because they are widely available and are ideal for the use of piezoelectric materials, which have the ability to convert mechanical strain energy into electrical energy.

Contributions of this paper are summarized as follows. Section 2 presents the relationship to Collective Awareness Systems. In Section 3, state of the art of energy harvesting transducers are presented. In Section 4 the concept of synergy between piezoelectric energy harvesters and WSN is justified and a block diagram of the proposed self-powered Wireless Actuator/Sensor Node is presented. Section 5 presents experimental evaluation of the piezoelectric harvester. Finally some conclusions are drawn in section 6.

2. Relationship to Collective Awareness Systems

Nowadays, the emergence of collective awareness systems is pushing the performance of end user interactive objects. The support framework based in a interconnected objects and things (IoT) is the bridge that combines technologies and components from micro-systems (miniaturized electric, mechanical, optical and fluid devices) with knowledge, technology and functionality from several areas of research.

However, Harbor Research [1] defines smart systems as a new generation of systems architecture (hardware, software, network technologies, and manage services) that provides real-time awareness based on inputs from machines, people, video streams, maps, new feeds, sensors and more that integrate people, process, and knowledge to enable collective awareness and decision making.

WSN provide endless opportunities, but at the same time pose formidable challenges, such as the fact that energy is a scarce and usually non-renewable resource. However, as part of WSN, micro-systems could provide advances in low power VLSI, embedded computing, communication hardware, and in general, the convergence of computing and communications, are making this emerging technology a reality. Likewise, advances in nanotechnology and MEMS are pushing toward networks of tiny distributed sensors and actuators.

As mentioned in the previous section, energy harvesting can dramatically extend the operating lifetime of nodes on WSN. Finally, this technology enables battery less operation and reduces the operation costs of WSN, which are mainly due to battery replacement.

3. Energy Harvesting from the surroundings

Energy harvesting techniques developed for micropower generators deal with the challenge of scavenging and making use of residual energy present in ambient sources, usually energy in the form of light, radio RF electromagnetic radiation, thermal gradients and many sources of motion, namely rotation, vibration and fluid flow. Energy harvesting transducers that make use of energy in the form of motion are called Electromechanical and are separated in three different groups: electromagnetic, electrostatic and piezoelectric transducers. Piezoelectric transducers make use of the piezoelectric effect, which refers to the accumulation of an electrical charge in some solid materials, like crystals and certain ceramics, when a mechanical stress is applied to them. The effect is reversible, which means that movement, in the form of

oscillation, can occur for the resonance frequency of the particular piezoelectric material to which an electrical charge is applied. These transducers are usually designed to harvest energy from vibration sources. Their harvesting optimization highly depends on the success of the characterization of the vibration from which the energy is to be harvested.

The three electromechanical transducer types are very different from each other. In general, power efficiency of a mechanical transducer could be considered as the ratio between the electrical power it delivers and the mechanical power it receives from the motion source. However, comparing different transducers is not trivial.

In [2], a variant of harvester effectiveness performance indicator is introduced, the Volume Figure of Merit (VFM), which is used to compare the performances of energy harvesting electromechanical transducers as a function of their size. The devices chosen for the actual comparison are electromechanical transducers of the three types mentioned above. Table 1 contains the two best results achieved for each of the transducer types. The main conclusion taken from the presented results is that piezoelectric transducers achieve reasonable values for power efficiency, when compared to the other electromechanical energy harvesting transducers.

Table 1. VFM for the Three Transducers Types (Extracted from [2]).

Transducer type	Reference	VFM[%]
Electromagnetic	[3]	0.52
	[4]	0.64
Electrostatic	[5]	0.06
	[6]	0.68
Piezoelectric	[7]	1.39
	[8]	1.74

4. Synergy between Piezoelectric Energy Harvesters and Wireless Sensor Networks

Wireless Actuator/Sensor Nodes represent a wide range of devices with different functionalities and characteristics with an estimated power consumption level that can be retrieved from the data available in [9]. Some commercially available actuator sensor nodes, namely Crossbow MICAZ, Intel Mote 2 and Jennie JN5139, have power consumption levels of 2.8 mW, 12 mW and 3 mW, respectively.

In [10], the power consumption of a wireless sensor node based on the Nordic RF24L01 wireless transceiver is analysed. The conclusion reached is that the RF transceiver is responsible for 74% of the power consumption, the rest being associated with the power consumptions of the microcontroller, the power management module, sensors, actuators and ADCs.

The power supplied by a piezoelectric energy harvester depends greatly on the piezoelectric transducer's characteristics and the vibration conditions it is submitted to. Furthermore, for each piezoelectric transducer setup there are optimal vibration conditions, which should match the resonance frequency of the piezoelectric material, and its optimal acceleration, which is directly related to the vibration amplitude. Considering an optimized energy harvesting setup regarding the transducer and the

characterisation of the vibration frequency, the circuit responsible for rectification and eventual voltage supply regulation must be designed and implemented. It should be noted that this circuit has a power efficiency associated to it. As an optional component in the power management part of the system, and depending, once again, on the vibration predictability, an energy storage device might be considered.

Two examples of piezoelectric energy harvesters implemented with optimal vibration characteristics and resistive loads that maximize the power output are given in [9] and [11]. In the first case, a power output of 3 mW was achieved, while in the second work a value of 4.4 mW was also experimentally verified. For the first implementation, a Volture V22BL piezoelectric transducer was used, with vibration characteristics of 50 Hz and 1g. The second example makes use of a Piezo Systems T226-A4-503X piezoelectric transducer, with vibration characteristics of 50 Hz and 0.5 g. It should be noted that the power outputs are achieved using optimized resistive loads for each of the situations.

Although power consumption and power output levels do not match, energy harvesting solutions can be made possible using a duty cycling technique, making use of a battery or a supercapacitor. This technique consists in switching periodically the sensor node on and off. Since the wireless sensor node doesn't have to be constantly communicating, the energy harvested by the transducer is used in the communication time interval of the sensor node and stored in the battery (or capacitor) during the rest of the cycle (switched off time interval). In [2], a duty cycle of 1.6% is used for a solution using a piezoelectric energy harvester powering a custom designed radio transceiver that requires 12 mW when transmitting. The power consumption values previously presented, from [9], are based in operating conditions of 1% communication, 10% processing and 89% sleeping. The proposed block diagram of a self-powered actuator/sensor node is presented in Figure 1.

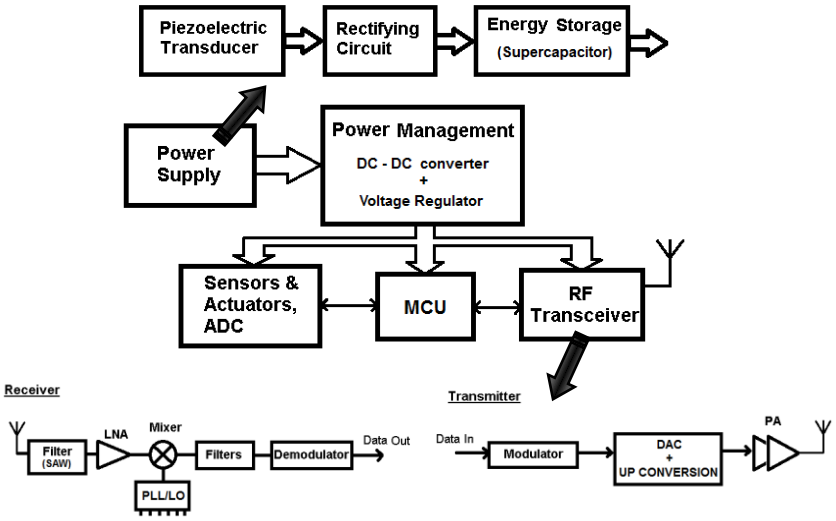

Figure 1. Block diagram of a Piezoelectric-powered WSN.

5. Experimental Evaluation of the Piezoelectric Energy Harvester

The chosen piezoelectric energy harvester Midé Volture™ V21bl [12], designed for vibration energy harvesting, is presented in Figure 2. It uses the piezoelectric characteristics of its specific piezoceramic material to produce electrical charge when mechanically stimulated [13] and consists in a package of piezoelectric materials in a protective skin, with four pre-attached electrical leads.

Figure 2. Midé Volture™ V21bl [12].

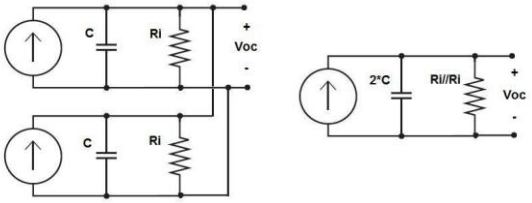

Figure 3. Parallel equivalent circuit.

The piezoelectric harvester includes two electrically isolated piezo wafers, which may be used independently or in one of two possible combinations. These combinations can be optimised for increased output voltage (series configuration) or increased output current (parallel configuration). For this implementation, and since the desired output voltage is relatively low compared to the range of typical output voltages of the piezoelectric harvester, the parallel configuration is used, in order to maximize the output current needed to charge the capacitor. Figure 3 presents the final equivalent circuit of the parallel configuration of the two wafers.

A block diagram of the test setup is shown in Figure 4, which comprises three complementary parts:

1. a test vibration module which is formed by an audio amplifier (LM386) and vibration speaker coupled to the piezoelectric transducer;
2. a rectifying diode bridge plus a fast charge capacitor;
3. a data-acquisition subsystem, consisting of a 10-bit ADC and a MCU connected to both a LCD Module (HD44780 module, 16X2 LCD Panel) and a USB connection to a computer.

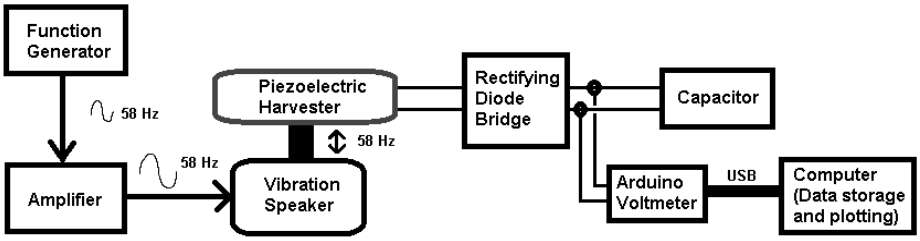

Figure 4. Block diagram of the test setup.

A picture taken of the test setup is shown in Figure 5.

The energy stored in the capacitor is calculated using the standard equation given by,

$$\mathrm{E} = (1/2)\mathrm{CV}^2 . \quad (1)$$

For the Energy calculation, the actual capacitance of the parallel of capacitors was set to 2100 μF. In fact, this energy was calculated using the discharge time of the capacitor (from 1.3 V to 0 V), which is approximately 21 seconds, Figure 6 a). Using this discharge time, the resistance value of the RC circuit (2 KΩ) and the RC time constant approximation, the actual capacitance of the capacitor can be calculated. Using this value, the estimated stored energy in the capacitor is 1.77 mJ, for 1.3 V.

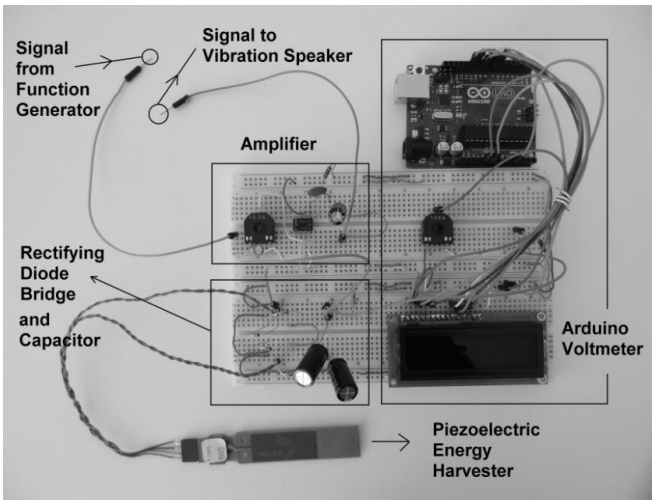

Figure 5. Photograph of the implementation.

Two different methods of vibration were used during the tests: the manually induced and the one produced by the small amplitude vibration speaker. The optimal vibration frequency was found for the second case.

For the manually induced movement test, a constant oscillation frequency was emulated. Given the equivalent circuit of the piezoelectric harvester, previously presented in Figure 3, the expected behaviour of the charging circuit is described by,

$$V_C = V_{Final} * \left(1 - e^{-\frac{t}{RC}}\right) \quad (2)$$

where V_C is the instant voltage across the capacitor while V_{Final} depends on the open circuit voltage of the piezoelectric harvester. The charging time was approximately 68 seconds, Figure 6 b). After some testing using a speaker, the optimal vibration frequency for energy harvesting purposes was found to be 58 Hz. Three tests were run with this vibration frequency, following the same procedure. The charging process was interrupted when the capacitor reached 1.3 V, after which the capacitor is connected to a 2 kΩ resistor. Figure 6 a) shows the results of these three tests.

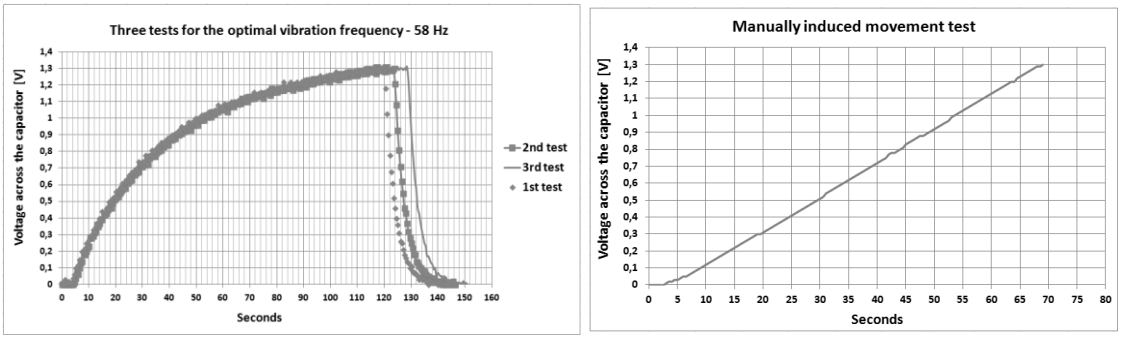

Figure 6. a) Three tests for the optimal vibration frequency – 58 Hz; b) manually induced movement test.

The charging time of the capacitor (from 0 V to 1.3 V) is approximately 125 seconds (medium value). It is greater than the one achieved with the first test (the manually induced movement test), proving that the tip-to-tip displacement amplitude, related to the vibration acceleration, is an important factor in the energy harvesting implementation, using this particular piezoelectric energy harvester.

Using non-optimal vibration frequencies for the vibration speaker case, the time the piezoelectric harvester takes to charge the capacitor up to the same voltage level is greater. To prove this, two non-optimal frequencies were chosen: 60 Hz, which is above the optimal frequency, and 56 Hz, which is below. The charging times for these tests are approximately 250 seconds for the first one and 180 seconds for the second. Both of them are greater than the one achieved for the optimal vibration frequency, 125 seconds. Table 2 shows practical results of this work.

Table 2. Summary of the experimental results.

Vibration type	Vibration frequency	Charging time (from 0V to 1.3V)	Energy stored in the capacitor after charging time	Capacitor used
Vibration Speaker	58 Hz	125 s	1.77 mJ	2100 μF
	56 Hz	180 s		
	60 Hz	250 s		
Manual	-	68 s		

6. Conclusions

The main conclusion of the present work is that it is possible to implement an energy harvesting solution using the piezoelectric energy harvester Midé Volture™ V21bl for low voltage applications, even if the vibration conditions applied to the harvester are not optimal. Comparing the vibration speaker case and the test involving

manually induced oscillation, it is possible to conclude that the tip-to-tip displacement amplitude is a very important factor in terms of energy generated by the piezoelectric device, more so than the actual selection of the right frequency for the oscillation.

For each configuration of the mechanical vibration method, there is an optimal vibration frequency, for energy harvesting purposes. In the case of this implementation, that frequency is approximately 58 Hz.

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A Low-Voltage LNA and Current Mode Mixer Design for Energy Harvesting Sensor Node

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A Low-Voltage LNA and Current Mode Mixer Design for Energy Harvesting Sensor Node

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Abstract—**A low-voltage RF CMOS receiver front-end for energy harvesting Wireless Sensor Node (WSN) is presented. A MOSFET-only wideband balun LNA, with noise and distortion cancelling, is designed to work at 0.6 V supply voltage, in conjunction with a passive mixer. The passive mixer works in current mode, allowing a minimal introduction of noise and a good linearity. The receiver front-end reaches a total voltage conversion gain of 31.5 dB, a 0.1-5.2 GHz bandwidth, an IIP3 value of -1.35 dBm, and a noise figure inferior to 32.6 dB. The total power consumption is 1.95 mW.**

Index Terms—**CMOS RF analog front-end; Low-power and low-voltage RF receiver; Low-voltage wideband balun LNA; Double-balanced passive mixer; RF receiver for Wireless Sensor Networks.**

I. INTRODUCTION

Low-power receiver architectures used in analog front-end transceiver circuits are a good option to consider when overall consumption is a key factor. This is the case for Wireless Sensor Node Networks (WSN), where individual sensor nodes, Wireless Sensor Actuator Nodes (WSAN), must be energetically autonomous and communicate wirelessly with each other, sharing information regarding physical measurements of their environment made by their sensors and eventually sharing commands destined to their actuators, [1].

The Low-IF receiver architecture features down-conversion to an intermediate frequency that is high enough to avoid problems related with flicker noise (that are a concern in zero-IF or direct conversion architectures) and low enough to relax the filter specifications associated with channel selection, [2]. Figure 1 represents the block diagram of the chosen architecture. This architecture allows a good performance at low-power consumption, which is the main constraint of the target application.

Since the wireless sensor nodes must be energetically autonomous and battery replacement increase maintenance costs, Energy Harvesting (EH) techniques are a very promising solution to power these nodes. Among existing EH techniques, piezoelectric power source was chosen, [3].

This paper presents a CMOS low-voltage RF receiver front-end making use of Low-IF receiver architecture, designed to work with simple binary modulations such as OOK modulation, [4] and at a supply voltage of only 0.6 V. The circuit was designed and simulated using CADENCE, with a 130 nm, purely-digital, CMOS technology.

This work was supported by national funds through FCT - Portuguese Foundation for Science and Technology under projects PEst-OE/EEI/UI0066/2011 and DISRUPTIVE (EXCL/EEI-ELC/0261/2012).

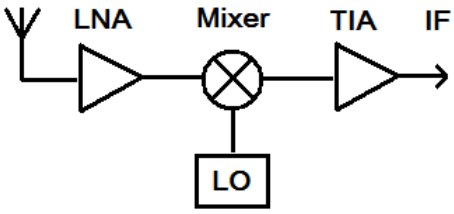

Figure 1. Low-IF Receiver Architecture.

The low-power consumption is possible due to a careful sizing of the transistors, the inclusion of a low-voltage technique in the LNA's first stage and the implementation of a passive mixer. Moreover, a Dynamic Threshold voltage MOS (DTMOS) technique, [5], was also implemented in order to further reduce the operating supply voltage.

Section II presents a selection of state-of-the-art LNA and mixer circuits. The complete proposed circuit including the LNA and mixer is presented in section III. Section IV includes some implementation considerations regarding transistor dimensioning and biasing voltages, as well as power consumption values. Section V presents the simulations run for the proposed circuit, including gain, noise figure and linearity. A Figure of Merit is calculated and used to compare the proposed circuit to other state-of-the-art receiver solutions. The comparison includes positive and negative characteristics of the proposed receiver. Finally, some conclusions are presented in section VI.

II. WIDEBAND BALUN LNAS AND MIXER CIRCUITS

A. Wideband Balun LNAs

The wideband balun LNA presented in [6], and depicted in Fig. 2 has a common-gate (CG) and a common-source (CS) stage, a single-ended, unbalanced input and delivers a balanced output, thus guaranteeing the balun functionality. It is able to cancel the noise of the first stage, the CG-stage, as long as both stages have the same gain. This happens because the first stage's noise appears as a common-mode signal at the differential output. Dimensioning CG and CS devices with different sizes and bias allows this circuit to simultaneously benefit from noise and distortion cancelation and the output

balancing abilities, as is demonstrated in [6]. The circuit can achieve very good linearity as long as the CS-stage's linearity is assured.

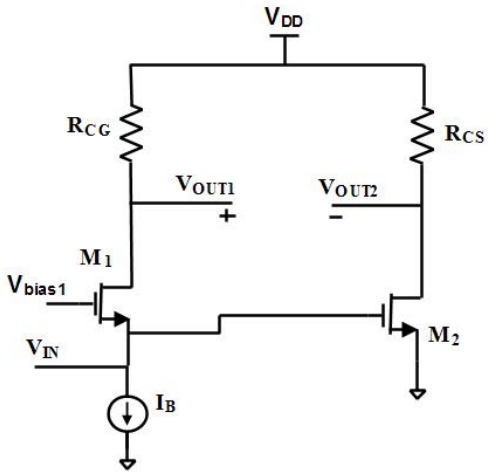

Figure 2. Wideband Balun LNA, [6].

A MOSFET-only version of the previously referred LNA circuit is presented in [7], Fig. 3. This version replaces the CG and CS resistors (used in [6]) by PMOS transistors M3 and M4, respectively, operating in the triode region but close to saturation, allowing an increase of the incremental load resistance and, consequently, to the LNA's gain, for the same *DC* voltage drop. The replacement of the resistors by the PMOS devices also results in a reduction of circuit area and cost. Regarding the original LNA, this circuit has the disadvantage of an increased distortion and a reduction of bandwidth.

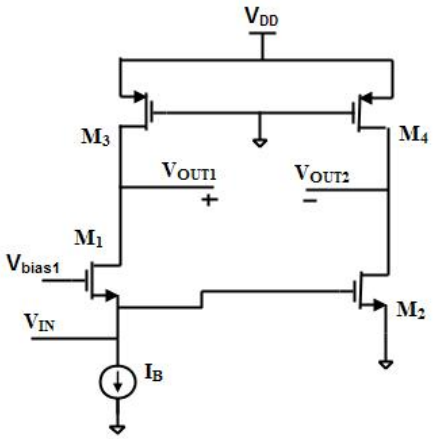

Figure 3. MOSFET-only Wideband Balun LNA [7].

B. Mixer circuits

The simplest mixer configuration is a CMOS transistor-implemented switch, whose gate is driven by the Local Oscillator (LO) signal, with the RF signal being applied at its drain and the Intermediate Frequency (IF) signal being taken at its source. This passive mixer has no *DC* consumption and provides high linearity and bandwidth, [8].

Active mixers provide gain and strengthen the IF signal as they deliver it to subsequent receiver stages. They are most commonly based on the differential pair and can be single-balanced or double-balanced, depending on whether the RF signal coming from the LNA is balanced or unbalanced.

The single-balanced active mixer has a differential pair with the inputs driven by the LO signals and a current source controlled by the RF unbalanced signal. The two sides of the differential pair convert the RF input voltage to a current that is drawn alternately. For this mixer, the output spectrum includes the LO frequency. It is a simple active mixer that has moderate gain and noise figure, high input impedance and low 1 dB compression point, low IIP3 and low port-to-port isolation [8].

The double-balanced active mixer, called Gilbert cell, is more complex, having LO and RF differential inputs. It features improvements when compared to the single-balanced active mixer, namely higher gain, lower noise figure, high port-to-port isolation and good linearity. It is also able to remove the LO frequency from the output spectrum. These improvements come at the cost of higher consumption and increased circuit area and cost. [1,8]

III. Complete Proposed Circuit

Fig. 4 presents the complete implemented circuit, including the LNA, mixer, *DC* decoupling capacitors between those two and the transimpedance amplifier (TIA) after the mixer, which is able to buffer the final output, filter frequencies higher than the chosen IF frequency and convert the current signal to a voltage signal. Between the mixer and the TIA a *DC* voltage source is added as a common-mode voltage of the two TIA inputs. The design of the TIA block is not detailed in this paper and the OTA is considered to reach a gain of 1000.

The main contribution of the presented circuit is not the introduction of new LNA and mixer architectures but rather a new implementation of their combination: the signals are treated in current mode. The RF signal coming from the antenna is converted to current and amplified by the LNA, being delivered to the mixer as a balanced signal. The mixer's output, a balanced current signal IF, is then converted to a balanced voltage signal by the TIA.

A. LNA

The proposed LNA circuit is presented in Fig. 4, along with the rest of the receiver analog front-end designed in the present work. This LNA is a new version of the MOSFET-only LNA presented in section II, designed to work at a supply voltage of 0.6 V. With a careful dimensioning, the use of a low-voltage technique and the introduction of independent stage biasing, the LNA is able to work without losing too much of its gain, as will be shown in sections IV and V. Since the dimensions of the PMOS devices can be adjusted to increase the LNA's output resistance, the current output of the LNA can be optimised. This is an important factor because the chosen mixer operates in current mode. Consequently, the LNA's

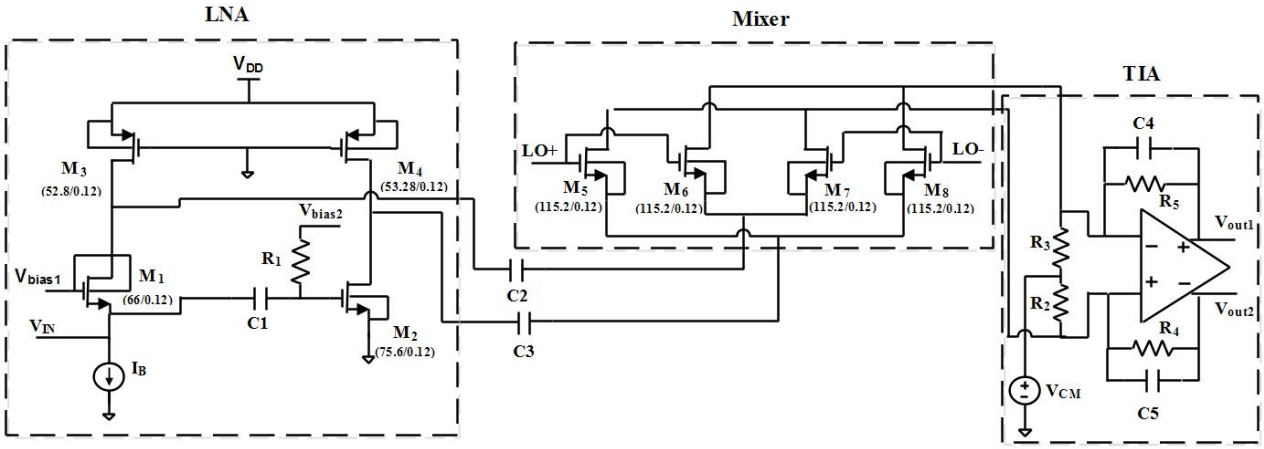

Figure 4. Complete Receiver Circuit with all transistor sizes (W/L) in µm.

voltage gain is not the main concern, but rather its transcondutance gain, which is essentially given by the M1 (CG) and M2 (CS) g_m values.

The V_{DD} reduction is possible due to an additional biasing voltage applied to the CS stage (V_{bias2}), to guarantee enough gate-source voltage across transistor M2. Since V_{bias1} is limited to the supply voltage value, it wouldn't be sufficient to assure both M1 and M1 V_{GS} needed values. For this reason, V_{bias2} was added, along with the decoupling capacitor C1.

Additionally, the DTMOS low-voltage technique is used in transistor M1 to allow the low supply voltage operation. The technique consists in connecting the bulk of the transistor to its gate terminal [5], introducing a dynamic regulation of the transistor's threshold voltage. The use of this technique allows enough drain-source voltage for the current-source transistor. It does so by reducing the threshold voltage of transistor M1. The DTMOS technique is also responsible for a small increase in the effective *gm* of device M1, slightly contributing to the CG voltage gain. This consideration is included in the LNA's differential voltage gain expression, (1), presented in this section.

LNA differential voltage gain

The expression for the LNA differential voltage gain is achieved by the subtraction of the CG and CS voltage gains, which were deduced using a small signal incremental model of the LNA. The gain if given by

$$AV|_{Diff} = \frac{gm1+gmb1+gds1+gm2\left(\frac{g_{ds1}+g_{ds3}}{g_{ds2}+g_{ds4}}\right)}{g_{ds1}+g_{ds3}} \quad (1)$$

which can be approximated by

$$AV|_{Diff} \approx \frac{gm1+gmb1+gm2}{g_{ds1}+g_{ds3}} \quad . \quad (2)$$

The presented approximation is valid considering that g_{ds1} and g_{ds2} have similar values, the same happening for g_{ds3} and g_{ds4}.

LNA input-impedance

The LNA input-impedance is given by (3).

$$Z_{in} = \frac{gds1+gds3}{(gm1+gmb1+gds1)g_{ds3}} \quad (3)$$

LNA noise figure

Assuming that $g_{m1} = g_{m2} = g_m$, the noise figure is given by (4) [6, 7].

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S c_{ox} f^{\alpha f}}\left(\frac{1}{W_1 L_1}+\frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S r_{ds} g_m^2} \quad (4)$$

with k as the Boltzmann's constant, c'_{ox} the oxide gate capacitance per unit area, W_i and L_i the transistor dimensions, T the absolute temperature, γ the excess noise factor, k_f and α_f intrinsic process parameters.

B. Mixer

The choice of the mixer architecture for the receiver was governed once again by the energy consumption constraint of the target application. Since this factor is critical for the overall functioning of the WSAN receiver, a passive mixer architecture was chosen. The circuit is presented in Fig. 4 and consists of two pairs of NMOS transistors used as voltage-controlled switches, working in the triode zone to maintain a low drain-source voltage when turned ON. The RF signal at the mixer's input is mixed in current. For a passive mixer as this one, the LO signals must be strong and buffered. The LO signals that drive the devices' gates are considered as ranging from 0 V to *VDD* supply voltage, 0.6 V.

The mixer works in current mode, allowing a minimal introduction of noise and a good linearity. The reduced noise introduction, especially flicker noise, is possible due to the inclusion of the *DC* decoupling capacitors between the LNA and mixer, which guarantee there is no *DC* current flowing through the mixer. Moreover, due to the TIA, the variation of the drain-source voltage of the mixer's NMOS is reduced, thus contributing to improve the linearity of the circuit.

C. Theoretical expressions of the complete circuit

Assuming that $g_{m1} = g_{m2} = g_m$ and R4 = R5, the noise figure is given by (7) [6, 7].

$$F_{Total} = 1 + \frac{k_f}{8kTR_S C_{oxf}{}^{af}}\left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S R_4 g_m^2} \quad (7)$$

The overall conversion gain is given by

$$CG_{Total} = Gm_{LNA} \times Z_{TIA\ Filter\ @\ 10MHz} \ . \quad (8)$$

IV. Circuit Implementation

The design process began by defining the V_{DD} voltage and power consumption values. V_{bias1} was set to 0.6 V and V_{bias2} at 0.45 V. A current mirror, biasing the first stage of the LNA with a current value of approximately 1.64 mA, designed the current source. The common-mode voltage at the TIA input is set at 100 mV.

The circuit was dimensioned to work with an RF frequency of 1 GHz and an IF of 10 MHz. The LO frequency was considered as 990 MHz. For simulation purposes, the oscillator signals, LO+ and LO– in Fig. 4, were considered square waves in quadrature, with 50 ps of rise and fall times and without overlapping, with peak-to-peak buffered voltages of 0.6 V.

The NMOS and PMOS transistors chosen are RF transistors, with a triple-well structure chosen for the NMOS. Their dimensions are presented in Table I. The chosen length (L) for all the transistors was the technology's minimum L value, in this case 120 nm, in order to maximize circuit speed. To define the width for M_1, (3) was considered, so that this device's dimensions would guarantee 50 Ω input matching. Widths of M_3 and M_4 were determined by the LNA's output impedance, which means that these values were chosen with the objective of setting the PMOS drain-source resistances at a desired value, initially 200 Ω. The optimised value for the width of M_2 was chosen as the one which allowed the CS gain to match the CG gain, a required condition for the noise cancelling capability, as explained in section II. This matching of the CG and CS gains was possible after the optimization process applied to size M_2. The chosen width values for the mixer devices were set with the objective of achieving small drain-source resistance values.

The resistor and capacitor values chosen are presented in Table II. Resistor R_1 limits the *DC* current generated by V_{bias2} and resistors R_2 and R_3 help setting the common-mode voltage at the TIA input. Capacitor C1 is responsible for the *DC* decoupling between the two LNA stages and capacitors C2 and C3 allow the *DC* decoupling between the LNA and mixer, while achieving low impedance values at the RF frequency of interest. Resistor values of R_4, R_5 and capacitor values of C4 and C5 are chosen so that a low pass filter is implemented at the TIA. The cutoff frequency of the filter was dimensioned to be slightly higher than the IF frequency, in order to attenuate frequencies above IF. The TIA's transresistance gain value, responsible for the current to voltage conversion, is 200 KΩ for the IF frequency (10 MHz). This value corresponds to the impedance of the parallel of resistor R5 and capacitor C4 (or R4 and C5) for the given IF frequency.

TABLE I. Transistor dimensions table for the LNA and Mixer

		I_D (mA)	W (μm)	L (μm)	r_{ds} (Ω)	g_{ds} (mS)	g_m (mS)
LNA	M_1	1.64	66	0.12	453	2.2	20.15
	M_2	1.63	75.6	0.12	576	1.73	21.88
	M_3	1.64	52.8	0.12	254	3.93	8.6
	M_4	1.63	53.28	0.12	257	3.89	8.5
Mixer	$M_{5,6,7,8}$	-	115.2	0.12	-	-	-

TABLE II. Resistor and capacitor dimensions

	R1,R2,R3 (kΩ)	R4,R5 (kΩ)	C1,C2,C3 (pF)	C4,C5 (pF)
Values	10	200	5	9

V. Simulation Results

A. Selection of simulations run

For the IIP3 simulation, shown in Fig. 5, the tones are 100 MHz apart from each other, a situation that would be ideal for an IF frequency value of 100 MHz. Even though this is not the chosen IF frequency, the results achieved with this value is also illustrative for a 10 MHz IF case. The simulation was run using a tone separation frequency value different from the desired IF frequency for reasons concerning simulation and convergence times. The IIP3 simulation renders a value of -1.35 dBm.

In order to validate the low noise capabilities of the complete circuit, a noise figure simulation, shown in Fig. 6, was run for the differential IF output. The simulation's results lead to the conclusion that the circuit presents a low noise figure, around 8.6 dB, for a relatively wide band of frequencies close to the desired IF frequency.

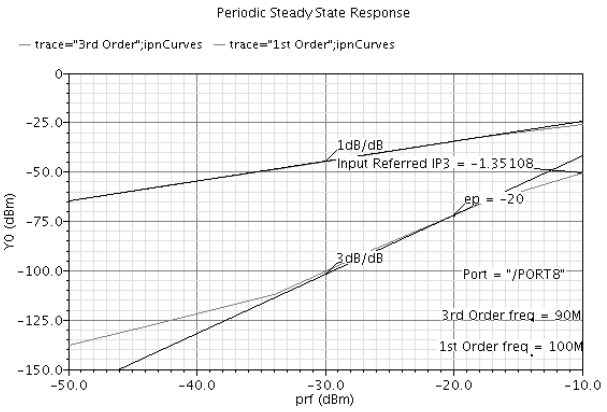

Figure 5. IIP3 simulation.

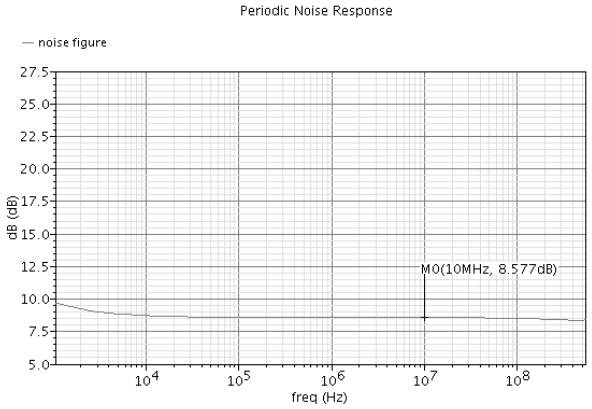

Figure 6. Noise Figure simulation.

B. Results Table

The FoM expression considered is presented in (9). In order to calculate the FoM values, gain and NF were converted from the dB values presented in Tables III and IV.

$$FoM[\mathrm{mW}^{-1}] = \frac{AV|_{Diff}}{(NF-1)P_{DC}[\mathrm{mW}]} \quad (9)$$

For comparison purposes, the same FoM expression was used to calculate the state-of-the-art circuits' FoM values.

Table III presents the final results for this work's presented circuit. These results include LNA bandwidth, LNA differential voltage gain, LNA FoM, and some results for the complete circuit, namely conversion gain, noise figure, IIP3 and power consumption.

TABLE III. FINAL RECEIVER SIMULATION RESULTS

Tech (nm)	LNA		LNA + Mixer				
	Band (GHz)	Gain (dB)	Voltage Conversion Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	VDD Supply (V)
130	0.1-5.2	17.6	31.5	<8.57	-1.35	1.95	0.6

C. FoM results and comparison with state-of-the-art circuits

A comparison with state-of-the-art LNAs is presented in Table IV. The LNA was chosen for comparison because it is the most critical block in terms of gain and distortion in the receiver presented circuit.

TABLE IV. COMPARISON WITH STATE-OF-THE-ART LNAS.

Ref.	Tech (nm)	VDD (V)	Band (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	FoM (mW^{-1})
[6]	65	1.2	0.2-5.2	15.6	<3.5	>0	14	0.34
[9]	90	2.5	0.8–6	20	<3.5	>-3.5	12.5	0.6
[10]	90	1.2	0.1–1.9	20.6	<2.7	10.8	9.6	1.3
[11]	130	1.2	0.2–3.8	11.2	<2.8	-2.7	1.9	2.1
[7]	130	1.2	0.2–6.6	19.8	<1.8	1.6	4.8	3.9
This Work	**130**	**0.6**	**0.1–5.2**	**17.6**	**<5.2**	**2.3**	**1.95**	**1.7**

D. Results discussion

The circuit's bandwidth satisfies the requirements for the target application. The LNA's voltage gain value is equivalent to the voltage gain value of the original MOSFET-only LNA that was considered, which is a positive result, having in mind the V_{DD} voltage supply reduction for the proposed circuit, in relation to the original one. The voltage conversion gain of the complete circuit is a result of the contribution of the LNA's gain and the TIA's gain. The transimpedance gain of the TIA has a large contribution in this total conversion gain. The noise figure result is slightly higher than the LNA's noise figure, meaning that the mixer introduces some noise but not as much as an active mixer would. The IIP3 has a satisfactory value due to the reduced distortion introduced by the LNA and mixer.

E. Positive and negative characteristics of the proposed circuit

The main advantages of the proposed circuit are its low-power and low-voltage operation, its simplicity, good linearity and wideband operation, all of which are important factors for the target application. The introduction of noise is also reduced, thanks to the noise cancellation capability of the LNA and the fact that the receiver includes a passive mixer working in current mode. Moreover, it is an inductorless circuit, which helps in the reduction of the overall circuit area and, for that reason, circuit cost.

As a disadvantage, this work's receiver does not include the oscillator and the OTA designs, considering them as ideal devices. Additionally, and as a consequence of its simplicity, the circuit presents a low Power Supply Rejection Ratio (PSRR). Another disadvantage is the need for LO signal drivers.

VI. CONCLUSIONS

The CMOS ultra low-power and low-voltage RF receiver design includes the implementation of a MOSFET-only wideband balun LNA able to cancel noise and distortion, working at 0.6 V supply voltage, with a bandwidth of 0.1-5.2 GHz, a voltage gain of 17.6 dB, a noise figure inferior to 5.2 dB and an IIP3 value of 2.3 dBm. A double-balanced passive mixer is designed in conjunction with the LNA, working in current mode, and guaranteeing, together with the LNA and transimpedance amplifier (TIA), a total voltage conversion gain of 31.5 dB, an IIP3 value of -1.35 dBm, and a noise figure inferior to 32.6 dB. The total power consumption achieved is 1.95 mW.

The proposed receiver presents a good solution for a Wireless Sensor Actuator Node (WSAN) receiver whose power is supplied by an Energy Harvesting solution, mainly due to its low-power consumption, which is a critical factor for an energy-autonomous WSAN. This receiver has a simple inductorless architecture, resulting in a reduced area and, consequently, reduced circuit cost.

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Co-design of a Low-power RF Receiver and Piezoelectric Energy Harvesting Power Supply for a Wireless Sensor Node

International Journal of Microelectronics and Computer Science (Invited Paper of MIXDES 2014)

Co-design of a Low-power RF Receiver and Piezoelectric Energy Harvesting Power Supply for a Wireless Sensor Node

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Abstract—**A low-voltage RF CMOS receiver front-end and an energy harvesting power circuit for a piezoelectric source are presented as a co-designed solution for a Wireless Sensor Node. A MOSFET-only wideband balun LNA with noise cancelling and a 0.6 V supply voltage is designed in conjunction with a passive mixer. The passive mixer operates in current mode, allowing a minimal introduction of voltage noise and a good linearity. The receiver front-end reaches a total voltage conversion gain of 31 dB, a 0.1-5.2 GHz bandwidth, an IIP3 value of -1.35 dBm, and a noise figure inferior to 9 dB. The total power consumption is 1.95 mW. The energy harvesting power circuit consists of an active full bridge cross-coupled rectifier followed by a low-dropout (LDO) regulator, and it is able to guarantee a power output of 6 mW with a regulated output voltage of 0.6 V, for typical vibration patterns.**

Index Terms—**CMOS RF analog front-end; Low-voltage wideband balun LNA; Passive mixer; Piezoelectric Energy Harvesting; Active full bridge rectifier; LDO regulator.**

I. INTRODUCTION

Low-power receiver architectures used in analog front-end transceiver circuits are a good option to consider when overall consumption is a key factor. This is the case for Wireless Sensor Networks (WSN), where individual sensor nodes, Wireless Sensor Actuator Nodes (WSAN), must be energetically autonomous and communicate wirelessly with each other, sharing information regarding physical measurements of their environment made by their sensors and eventually sharing commands destined to their actuators, [1].

The Low-IF receiver architecture features down-conversion to an intermediate frequency that is high enough to avoid problems related with flicker noise (that are a concern in the direct conversion architecture) and low enough to relax the filter specifications associated with channel selection, [2]. This architecture allows a good performance at low-power consumption, which is the main constraint of the target application.

Since the wireless sensor nodes must be energetically autonomous and battery replacement increases maintenance costs, Energy Harvesting (EH) techniques are a very promising solution to power these nodes. Among existing EH techniques, a piezoelectric power source was chosen, [3], with the residual energy source to be scavenged contained in ambient vibrations. Piezoelectric transducers are essentially ceramic wafers that exhibit piezoelectricity. This property consists in the creation of electrical charge in piezoelectric materials when they suffer mechanical strains, and it is reversible, meaning that an applied electrical field results in internal mechanical strain. When subjected to vibration, these transducers create a varying output voltage that must be rectified and regulated, in order to meet the application's power requirements. The scavenged energy can then be stored with a supercapacitor. Figure 1 presents a block diagram for the overall approach, including the Low-IF receiver architecture.

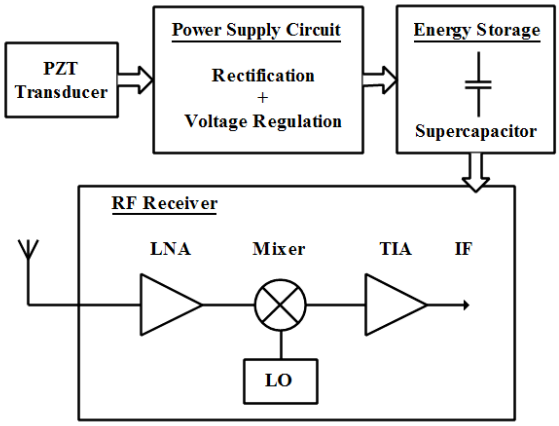

Figure 1. Block diagram for this work's co-designed approach; Low-IF Receiver Architecture.

This work presents a CMOS low-voltage RF receiver front-end, which is designed to operate at a supply voltage of only 0.6 V and for simple binary modulations, such as OOK modulation, [4]. The low-power consumption is possible due to a careful sizing of the transistors, the inclusion of low-voltage techniques in the LNA and the implementation of a passive mixer. The Dynamic Threshold voltage MOS (DTMOS) technique, [5], was implemented in order to further reduce the operating supply voltage.

This work was supported by national funds through FCT - Portuguese Foundation for Science and Technology under projects PEst-OE/EEI/UI0066/2011 and DISRUPTIVE (EXCL/EEI-ELC/0261/2012).

The EH power circuit, designed to power the RF receiver, includes an active full bridge cross-coupled rectifier that rectifies the output of the piezoelectric transducer. After the rectifier, a low-dropout (LDO) regulator is responsible for regulating the output of the rectifier to a *DC* voltage value of 0.6 V, with minimum ripple (<1%). The output of the power circuit feeds the receiver's power supply rail.

Section II presents a selection of relevant LNA and mixer circuits. The receiver proposed circuitry, including the LNA and mixer, is presented in section III. The piezoelectric EH system is introduced in Section IV. Section V presents the simulation results for the receiver, including gain, noise figure and linearity, and for the EH power circuit. Finally, some conclusions are presented in section VI.

II. WIDEBAND BALUN LNAS AND MIXER CIRCUITS

A. Wideband Balun LNAs

The wideband balun LNA presented in [6], and depicted in Fig. 2 has a common-gate (CG) and a common-source (CS) stage, a single-ended, unbalanced input and delivers a balanced output, thus guaranteeing the balun functionality. It is able to cancel the noise of the first stage, the CG-stage, as long as both stages have the same gain. This happens because the first stage's noise appears as a common-mode signal at the differential output. Dimensioning CG and CS devices with different sizes and bias allows this circuit to simultaneously benefit from noise and distortion cancelling and the output balancing abilities, as is demonstrated in [6]. The circuit can achieve very good linearity as long as the CS-stage's linearity is assured.

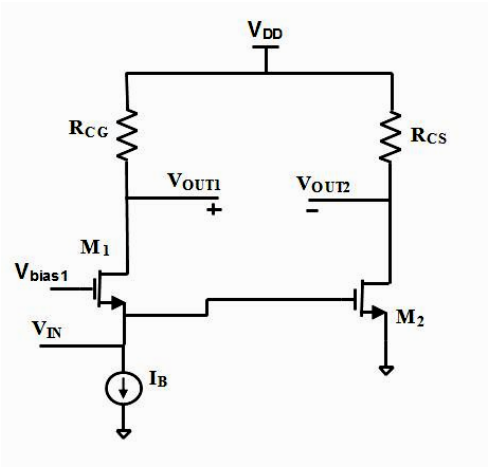

Figure 2. Wideband Balun LNA, [6].

A MOSFET-only version of the previously referred LNA circuit is presented in [7], Fig. 3. This version replaces the CG and CS resistors (used in [6]) by the PMOS transistors M_3 and M_4, respectively, operating in the triode region but close to saturation, allowing an increase to the incremental load resistance and, consequently, to the LNA's gain, for the same *DC* voltage drop. The replacement of the resistors by the PMOS devices also results in a reduction of circuit area and cost. Regarding the original LNA, this circuit has the disadvantage of an increased distortion and a reduction of bandwidth.

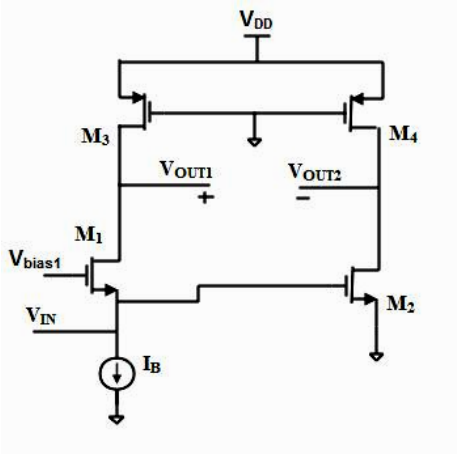

Figure 3. MOSFET-only Wideband Balun LNA [7].

B. Mixer circuits

The simplest mixer configuration is a CMOS transistor-implemented switch, whose gate is driven by the Local Oscillator (LO) signal, with the RF signal being applied at its drain and the Intermediate Frequency (IF) signal being taken at its source. This passive mixer has no *DC* consumption and provides high linearity and bandwidth, [8].

Active mixers provide gain and strengthen the IF signal as they deliver it to subsequent receiver stages. They are most commonly based on the differential pair and can be single-balanced or double-balanced, depending on whether the RF signal coming from the LNA is balanced or unbalanced.

The single-balanced active mixer has a differential pair with the inputs driven by the LO signals and a current source controlled by the RF unbalanced signal. The two sides of the differential pair convert the RF input voltage to a current that is drawn alternately. For this mixer, the output spectrum includes the LO frequency. It is a simple active mixer that has moderate gain and noise figure, high input impedance, low 1 dB compression point, low IIP3 and low port-to-port isolation [8].

The double-balanced active mixer, called Gilbert cell, is more complex, having LO and RF differential inputs. It features improvements when compared to the single-balanced active mixer, namely higher gain, lower noise figure, high port-to-port isolation and good linearity. It is also able to remove the LO frequency from the output spectrum. These improvements come at the cost of higher consumption and increased circuit area and cost, [1,8].

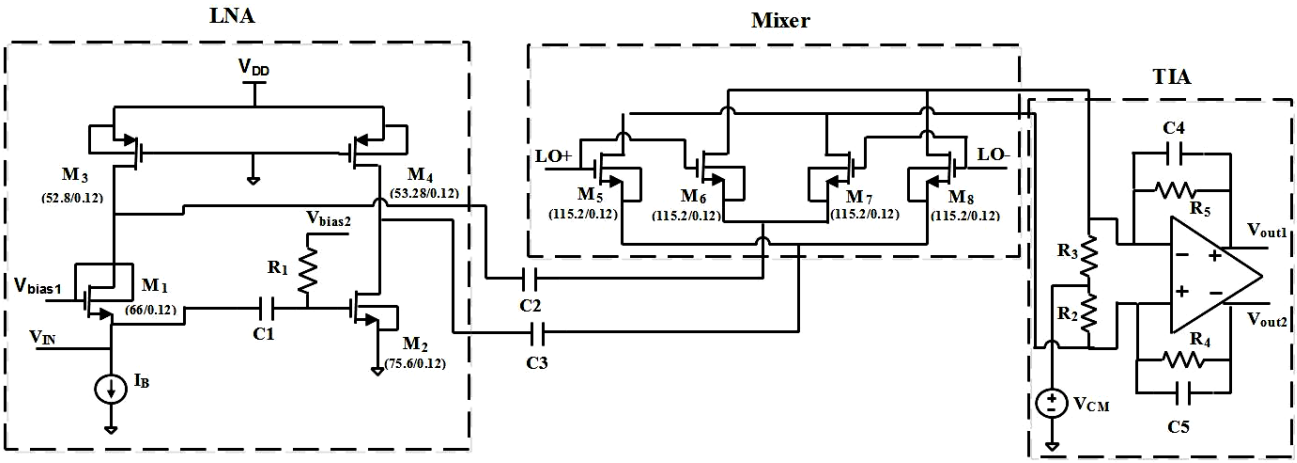

Figure 4. Complete Receiver Circuit with all transistor sizes (W/L) in µm.

III. RECEIVER PROPOSED CIRCUIT

Figure 4 presents the complete circuit, including the LNA, mixer, *DC* decoupling capacitors between those two and the transimpedance amplifier (TIA), which is responsible for buffering the final output, low-pass filtering, and converting the current signal to a voltage signal. Between the mixer and the TIA a *DC* voltage source is added as a common-mode voltage of the two TIA inputs. The design of the TIA block is not detailed in this paper and the OTA is considered to reach a gain from 500 to 1000.

The main contribution of the presented circuit is not the introduction of new LNA and mixer architectures but rather the implementation of the current mode signal processing enabled by their combination. The RF signal coming from the antenna is converted to current and amplified by the LNA, being delivered to the mixer as a balanced signal. The mixer's output, a balanced current signal IF, is then converted to a balanced voltage signal by the TIA.

A. LNA

The proposed LNA circuit is presented in Fig. 4, along with the rest of the receiver analog front-end designed in the present work. This LNA is a new version of the MOSFET-only LNA presented in section II, designed to work at a supply voltage of 0.6 V. With a careful dimensioning, the use of a low-voltage technique and the introduction of independent stage biasing, the LNA is able to work without losing too much of its gain, as will be shown in section V. Since the dimensions of the PMOS devices can be adjusted to increase the LNA's output resistance, the current output of the LNA can be optimised. This is an important factor because the chosen mixer operates in current mode. Consequently, the LNA's voltage gain is not the main concern, but rather its transcondutance gain, which is essentially given by the M_1 (CG) and M_2 (CS) g_m values.

The V_{DD} reduction is possible due to an additional biasing voltage applied to the CS stage (V_{bias2}), to guarantee enough gate-source voltage across transistor M_2. Since V_{bias1} is limited to the supply voltage value, it wouldn't be sufficient to assure both M_1 and M_2 V_{GS} needed values. For this reason, V_{bias2} was added, along with the decoupling capacitor C_1.

Additionally, the DTMOS low-voltage technique is used in transistor M_1 to allow the low supply voltage operation. The technique consists in connecting the bulk of the transistor to its gate terminal, [5], introducing a dynamic regulation of the transistor's threshold voltage. The use of this technique allows enough drain-source voltage for the current-source transistor. It does so by reducing the threshold voltage of transistor M_1. The DTMOS technique is also responsible for a small increase in the effective *gm* of device M_1, slightly contributing to the CG voltage gain. This consideration is included in the LNA's differential voltage gain expression, (1), presented in this section.

LNA differential voltage gain

The expression for the LNA differential voltage gain is achieved by the subtraction of the CG and CS voltage gains, which were deduced using a small signal incremental model of the LNA. The gain is given by (1)

$$AV|_{Diff} = \frac{gm1+gmb1+gds1+gm2\left(\frac{g_{ds1}+g_{ds3}}{g_{ds2}+g_{ds4}}\right)}{g_{ds1}+g_{ds3}} \quad (1)$$

which can be approximated by (2).

$$AV|_{Diff} \approx \frac{gm1+gmb1+gm2}{g_{ds1}+g_{ds3}} \quad (2)$$

The presented approximation is valid considering that g_{ds1} and g_{ds2} have similar values, the same happening for g_{ds3} and g_{ds4}.

LNA input-impedance

The LNA input-impedance is given by (3).

$$Z_{in} = \frac{gds1+gds3}{(gm1+gmb1+gds1)g_{ds3}} \quad (3)$$

LNA noise figure

Assuming that $g_{m1} = g_{m2} = g_m$, the noise figure is given by (4) [6, 7].

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S c_{ox} f^{\alpha_f}} \left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S r_{ds} g_m^2} \quad (4)$$

with k as the Boltzmann's constant, c'_{ox} the oxide gate capacitance per unit area, W_i and L_i the transistor dimensions, T the absolute temperature, γ the excess noise factor, k_f and α_f intrinsic process parameters.

B. Mixer

The choice of the mixer architecture for the receiver was governed once again by the energy consumption constraint of the target application. Since this factor is critical for the overall functioning of the WSAN receiver, a passive mixer architecture was chosen. The circuit is presented in Fig. 4 and consists of two pairs of NMOS transistors used as voltage-controlled switches, working in the triode region to maintain a low drain-source voltage when turned ON. The RF signal at the mixer's input is mixed in current. For a passive mixer as this one, the LO signals must be strong and buffered. The LO signals that drive the devices' gates are considered as ranging from 0 V to V_{DD} supply voltage, 0.6 V.

The mixer works in current mode, allowing a minimal introduction of noise and a good linearity. The reduced noise introduction, especially flicker noise, is possible due to the inclusion of the *DC* decoupling capacitors between the LNA and mixer, which guarantee there is no *DC* current flowing through the mixer. Moreover, due to the TIA, the variation of the drain-source voltage of the mixer's NMOS is reduced, thus contributing to improve the linearity of the circuit.

C. Theoretical expressions of the complete receiver circuit

Assuming that $g_{m1} = g_{m2} = g_m$ and $R_4 = R_5$, the noise figure is given by (5) [6, 7].

$$F_{Total} = 1 + \frac{k_f}{8kTR_S c_{ox} f^{\alpha_f}} \left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S R_4 g_m^2} \quad (5)$$

The overall conversion gain is given by (6).

$$CG_{Total} = Gm_{LNA+mixer} \times Z_{TIA\ Filter\ @\ 10MHz} \quad (6)$$

D. Receiver Circuit Sizing

The design process began by defining the V_{DD} voltage and power consumption values. V_{bias1} was set to 0.6 V and V_{bias2} at 0.45 V. A current mirror, biasing the first stage of the LNA with a current value of approximately 1.64 mA, was included as the current source. The common-mode voltage at the TIA input is set at 100 mV.

The circuit was dimensioned to work with an RF frequency of 1 GHz and an IF of 10 MHz. The LO frequency was considered as 990 MHz. For simulation purposes, the oscillator signals, LO+ and LO– in Fig. 4, were considered square waves in quadrature, with 50 ps of rise and fall times and without overlapping, with peak-to-peak buffered voltages of 0.6 V.

The NMOS and PMOS transistors chosen are RF transistors, with a triple-well structure chosen for the NMOS. Their dimensions are presented in Table I. The chosen length (L) for all the transistors was the technology's minimum L value, in this case 120 nm, in order to maximize circuit speed. To define the width for M_1, (3) was considered, so that this device's dimensions would guarantee 50 Ω input matching. Widths of M_3 and M_4 were determined by the LNA's output impedance, which means that these values were chosen with the objective of setting the PMOS drain-source resistances at a desired value, initially 200 Ω. The optimised value for the width of M_2 was chosen as the one which allowed the CS gain to match the CG gain, a required condition for the noise cancelling capability, as explained in section II. This matching of the CG and CS gains was possible after the optimization process applied to size M_2. The chosen width values for the mixer devices were set with the objective of achieving small drain-source resistance values.

The resistor and capacitor values chosen are presented in Table II. Resistor R_1 limits the *DC* current generated by V_{bias2} and resistors R_2 and R_3 help setting the common-mode voltage at the TIA input. Capacitor C_1 is responsible for the *DC* decoupling between the two LNA stages and capacitors C_2 and C_3 allow the *DC* decoupling between the LNA and mixer, while achieving low impedance values at the RF frequency of interest. Resistor values of R_4, R_5 and capacitor values of C_4 and C_5 are chosen so that a low pass filter is implemented at the TIA. The cutoff frequency of the filter was dimensioned to be slightly higher than the IF frequency, in order to attenuate frequencies above IF. The TIA's transresistance gain value, responsible for the current to voltage conversion, is 200 KΩ for the IF frequency (10 MHz). This value corresponds to the impedance of the parallel of resistor R_5 and capacitor C_4 (or R_4 and C_5) for the given IF frequency.

TABLE I. TRANSISTOR DIMENSIONS FOR THE LNA AND MIXER

		I_D (mA)	W (μm)	L (μm)	r_{ds} (Ω)	g_{ds} (mS)	g_m (mS)
LNA	M_1	1.64	66	0.12	453	2.2	20.15
	M_2	1.63	75.6	0.12	576	1.73	21.88
	M_3	1.64	52.8	0.12	254	3.93	8.6
	M_4	1.63	53.28	0.12	257	3.89	8.5
Mixer	$M_{5,6,7,8}$	-	115.2	0.12	-	-	-

TABLE II. RESISTOR AND CAPACITOR DIMENSIONS

	R1,R2,R3 (kΩ)	R4,R5 (kΩ)	C1,C2,C3 (ρF)	C4,C5 (ρF)
Values	10	200	5	9

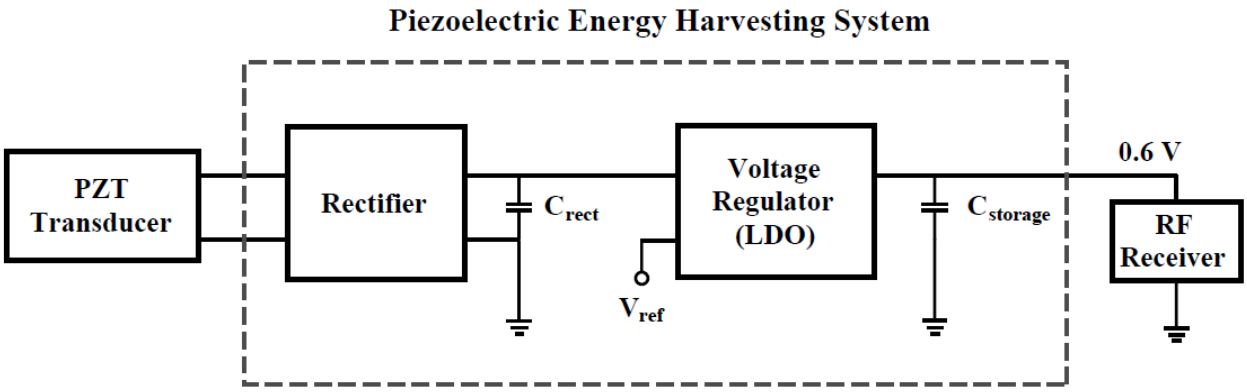

Figure 5. Block Diagram of the Piezoelectric Energy Harvesting System.

IV. Energy Harvesting Proposed Circuit

Figure 5 presents a block diagram of the EH system, including the rectifier block, the voltage regulator block and the C_{rect} and $C_{storage}$ supercapacitors. The EH power circuit is responsible for the conditioning of the piezoelectric transducer's power output. This output may be considered as an *AC* power signal with a frequency that is equal to the vibration frequency. This power signal is periodic but not trivial to emulate, consisting of irregular voltage bursts and peaks. As an approximation, sine waves were used to simulate the power source, with the typical amplitude voltage values given in the datasheet for the Midé Volture™ piezoelectric transducers family, [9]. These transducer output values were used as a specification for the ideal voltage source of the transducer's equivalent circuit presented in [3], in its Thevenin equivalent version.

The system was designed to work without batteries, making use of supercapacitors to store the scavenged energy. These supercapacitors are external components due to their high capacitance values, preferably higher than 100 µF. One of these, C_{rect}, is used at the output of the rectifier and is essential for the rectification. The $C_{storage}$ capacitor serves as the energy storage device, being placed after the voltage regulator. The 0.6 V regulated output of the system is taken directly at this capacitor's terminals.

A. Rectifier

The designed rectifier is an active full bridge cross-coupled rectifier, containing two NMOS and two PMOS transistors working as switches with their gates directly driven by the input terminals of the rectifier. Figure 6 shows the rectifier's schematic.

The cross-coupled configuration allows the rectifier to behave as a full bridge rectifier. Having Fig. 6 as a reference, this means that transistors N1 and P2 are switched on while the rectifier's input is inverted, meaning that the PZT- terminal has a higher potential than the PZT+ terminal. When the opposite occurs, transistors N2 and P1 are on, because N2's gate is connected to the highest potential and P1's gate to the lowest. The rectifier's output terminals are connected to the C_{rect} capacitor and the rectifier charges this capacitor because this output's polarity is maintained during each period of the input signal. The anode terminal of the C_{rect} capacitor is called V_{rect}, since this is the node with the rectified voltage that needs to be regulated to a 0.6 V *DC* value. The cathode terminal represents the power circuit's ground.

B. LDO regulator

The LDO regulator acts as a DC-DC converter, regulating the V_{rect} output of the rectifier to a *DC* output at a constant 0.6 V. The output of the LDO regulator, V_{out}, is therefore connected to the $C_{storage}$ capacitor. The LDO regulator consists of a PMOS power switch and the comparator that drives the switch's gate. A schematic of the LDO regulator is shown in Fig. 7.

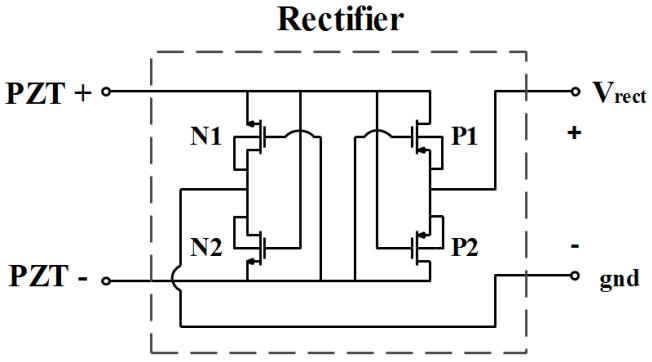

Figure 6. Active Full Bridge Cross-coupled Rectifier Circuit Schematic.

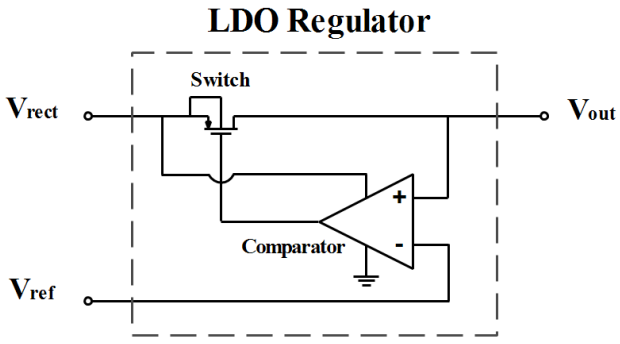

Figure 7. Low-dropout Regulator Schematic.

The PMOS switch's source terminal is connected to V_{rect} and the drain terminal to V_{out}, which is the final output of the system presented in Fig. 5. The switch is on when V_{out} is below 0.6 V and it is off otherwise.

The design of the comparator was included in the design of the system, although it is not described in detail in this work; it is a latch comparator whose supply voltage terminal is directly connected to V_{rect}, allowing the comparator to have an internally generated voltage source and correctly drive the switch's gate. The non-inverting input of the comparator is connected to V_{out} and the inverting input is connected to an externally generated voltage reference of 0.6 V, V_{ref}. The comparator changes its output depending on the relation of the two inputs. If V_{out} is below 0.6 V, it means that the $C_{storage}$ capacitor needs to be charged in order to reach the desired output voltage, so the output of the comparator is set to 0 V, allowing the PMOS switch to connect the anode terminals of the two supercapacitors, which causes the C_{rect} capacitor to charge the $C_{storage}$ capacitor. When V_{out} is above 0.6 V, the switch must be turned off, so that the $C_{storage}$ capacitor does not continue to be charged. To guarantee the switch is turned off, the comparator changes its output to V_{rect}, which represents the highest potential at the terminals of the PMOS transistor, thus making the source to gate voltage approximately 0 V, turning the switch off. Since the load is constantly discharging the $C_{storage}$ capacitor, the voltage across this capacitor drops below the V_{ref} value afterwards, making the process repeat itself.

The frequency at which the comparator works was also dimensioned and its clock generator was designed to generate a clock at approximately 150 kHz. This frequency sets the speed at which the comparator compares its inputs and changes its output, and it highly influences the ripple value at the system's regulated output.

C. Energy Harvesting Power Circuit Sizing

The EH system may be seen as being constituted by two main parts: the power circuit and the control circuit. The control circuit corresponds to the comparator and clock generator circuits, whose implementation details and specifications are not addressed in this work. The power circuit consists of the blocks through which considerable currents flow, in the order of magnitude of tens of milliamps; these blocks are the rectifier and the switch. In order to withstand currents in that order of magnitude, these MOSFET transistors had to be dimensioned with large widths, and the multiplier factor was also regulated so that the high current could be split by several transistors in parallel, which also reduces the *rds* impedance. Table III presents the transistor dimensions for the rectifier and the PMOS switch.

TABLE III. ENERGY HARVESTING POWER CIRCUIT SIZING

		W (μm)	L (μm)	m	$fingers$
Rectifier	N1	100	0.34	5	1
	N2	100	0.34	5	1
	P1	100	0.34	7	1
	P2	100	0.34	7	1
Switch	PMOS	50	0.34	6	2

V. SIMULATION RESULTS

The circuits presented in this work were designed for a 130 nm CMOS technology and were simulated under SpectreRF using BSIM3v3 models.

A. Selection of simulations concerning the Receiver

For the IIP3 simulation, shown in Fig. 8, the tones are 100 MHz apart from each other, a situation that would be ideal for an IF frequency value of 100 MHz. Even though this is not the chosen IF frequency, the achieved results are also illustrative for a 10 MHz IF case. The simulation was run using a tone separation frequency value different from the desired IF frequency for reasons concerning simulation and convergence times. The IIP3 simulation renders a value of -1.35 dBm.

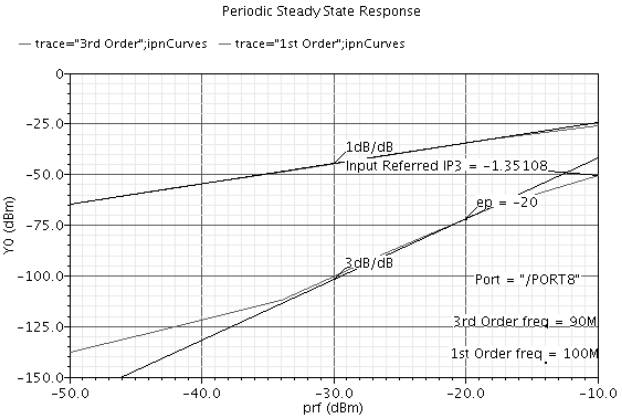

Figure 8. IIP3 simulation.

In order to validate the low noise capabilities of the complete receiver circuit, a noise figure simulation, shown in Fig. 9, was run for the differential IF output. The simulation's results lead to the conclusion that the circuit presents a low noise figure, around 8.6 dB, for a relatively wide band of frequencies close to the desired IF frequency.

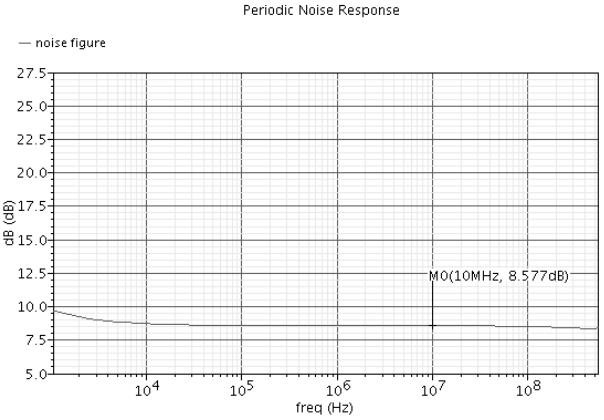

Figure 9. Noise Figure simulation.

Results Table

Table IV presents the final results for this work's receiver circuit. These results include LNA bandwidth, LNA differential voltage gain, and some results for the complete circuit, namely conversion gain, noise figure, IIP3 and power consumption.

TABLE IV. FINAL RECEIVER SIMULATION RESULTS

Tech (nm)	LNA		LNA + Mixer				
	Band (GHz)	Gain (dB)	Voltage Conversion Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	VDD Supply (V)
130	0.1-5.2	17.6	31.5	<8.57	-1.35	1.95	0.6

FoM results and comparison with state-of-the-art circuits

The FoM expression considered is presented in (7). In order to calculate the FoM values, gain and NF were converted from the dB values presented in Tables IV and V.

$$FoM[\mathrm{mW}^{-1}] = \frac{AV|_{Diff}}{(NF-1)P_{DC}[\mathrm{mW}]} \qquad (7)$$

For comparison purposes, the same FoM expression was used to calculate the state-of-the-art circuits' FoM values. A comparison with state-of-the-art LNAs is presented in Table V. The LNA was chosen for comparison because it is the most critical block in terms of gain and distortion in the receiver presented circuit.

TABLE V. COMPARISON WITH STATE-OF-THE-ART LNAS.

Ref.	Tech (nm)	VDD (V)	Band (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	FoM (mW^{-1})
[6]	65	1.2	0.2-5.2	15.6	<3.5	>0	14	0.34
[10]	90	2.5	0.8–6	20	<3.5	>-3.5	12.5	0.6
[11]	90	1.2	0.1–1.9	20.6	<2.7	10.8	9.6	1.3
[12]	130	1.2	0.2–3.8	11.2	<2.8	-2.7	1.9	2.1
[7]	130	1.2	0.2–6.6	19.8	<1.8	1.6	4.8	3.9
This Work	**130**	**0.6**	**0.1–5.2**	**17.6**	**<5.2**	**2.3**	**1.95**	**1.7**

B. Energy Harvesting Power Circuit Simulations

To allow the EH power circuit to supply a fully functional receiver, an approximation was made for the total power consumption, and a *DC* current of 10 mA was considered as the load's total requested current, at a 0.6 V supply, which results in a total estimated power consumption of 6 mW.

For simulation purposes, a load (representing the receiver front-end) was added to the EH power circuit, consisting in a current mirror driving a *DC* current of 10 mA from the output of the system.

Figure 10 presents a transient simulation of the power circuit where the V_{rect} and V_{out} signals, specified in Fig. 6 and 7, can be seen. This simulation represents the charging process of the $C_{storage}$ capacitor, from which the 10 mA *DC* current is requested by the load. The voltage across the $C_{storage}$ capacitor, V_{out}, is initially 0 V and reaches the 0.6 V value after approximately 24 ms, for the chosen simulation conditions. The voltage ripple at the output is below 1%, as can be verified in the zoomed in section of Fig. 10. The piezoelectric transducer's electrical model, in its Thevenin equivalent version, has its ideal voltage source set to generate a sine wave with a 5 V amplitude value. The transducer presents a high internal voltage drop, which is why the rectifier's output, V_{rect}, presents a considerably lower value.

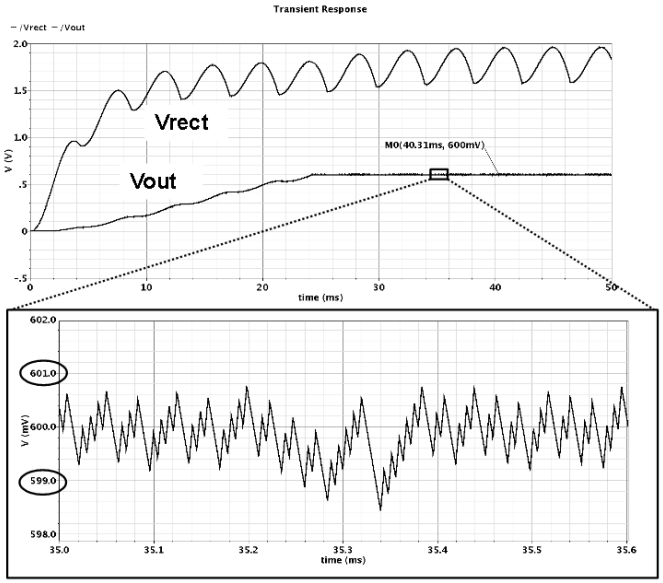

Figure 10. Transient simulation for the Power Supply circuit; V_{rect} and V_{out} signals are specified in figures 6 and 7.

C. Results discussion

Regarding the Receiver

The receiver circuit's bandwidth satisfies the requirements for the target application. The LNA's voltage gain value is equivalent to the voltage gain value of the original MOSFET-only LNA that was considered, which is a positive result, having in mind the V_{DD} voltage supply reduction for the proposed circuit, in relation to the original one. The voltage conversion gain of the complete receiver circuit is a result of the contribution of the LNA's gain and the TIA's gain. The transimpedance gain of the TIA has a large contribution in this total conversion gain. The noise figure result is slightly higher than the LNA's noise figure, meaning that the mixer introduces some noise but not as much as an active mixer would. The IIP3 has a satisfactory value due to the reduced distortion introduced by the LNA and mixer.

The main advantages of the proposed receiver circuit are its low-power and low-voltage operation, its simplicity, good linearity and wideband operation, all of which are important factors for the target application. The introduction of noise is also reduced, thanks to the noise cancellation capability of the LNA and the fact that the receiver includes a passive mixer working in current mode. Moreover, it is an inductorless

circuit, which helps in the reduction of the overall circuit area and, for that reason, circuit cost.

A disadvantage of the receiver circuit, which is a consequence of its simplicity, is its low Power Supply Rejection Ratio (PSRR). However, this disadvantage has its consequences taken to a minimum, because the power supply circuit is designed in order to deliver a strictly regulated voltage supply.

Regarding the Energy Harvesting Power Circuit

The EH power circuit is capable of guaranteeing a power output level that not only satisfies the LNA and mixer modules' power demands, but eventually the power requirements of the whole receiver. This is true for power outputs of the piezoelectric transducer that are relatively constant and moderately strong, which is a possibility for certain levels of ambient vibrations. The reduced voltage ripple at the output (<1%) is a good result, having in mind that, during the simulation, the load constantly requested a 10 mA *DC* current.

VI. CONCLUSIONS

The CMOS low-power and low-voltage RF receiver design includes the implementation of a MOSFET-only wideband balun LNA able to cancel noise and distortion, working at 0.6 V supply voltage, with a bandwidth of 0.1-5.2 GHz, a voltage gain of 17.6 dB, a noise figure inferior to 5.2 dB and an IIP3 value of 2.3 dBm. A double-balanced passive mixer is designed in conjunction with the LNA, working in current mode, and guaranteeing, together with the LNA and TIA, a total voltage conversion gain of 31.5 dB, an IIP3 value of -1.35 dBm, and a noise figure inferior to 9 dB. The total power consumption achieved is 1.95 mW.

A power consumption of 6 mW is guaranteed by the designed piezoelectric EH power circuit with an almost self-sufficient operation, considering that the piezoelectric transducer is subjected to moderate levels of vibration. This power supply is able to regulate the required voltage output with a ripple that is inferior to 1%, which is an important achievement, having in mind the receiver's low PSRR.

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