NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF MATERIALS SCIENCE

Hugo Filipe Matias Viana

Bachelor of Sciences in Micro and Nanotechnology Engineering

IMPLEMENTATION OF ACTIVE INDUCTORS WITH OXIDE THIN-FILM TRANSISTORS AND INTEGRATION INTO OSCILLATOR CIRCUITS

MASTER OF SCIENCES IN MICRO AND NANOTECHNOLOGY ENGINEERING

NOVA University Lisbon

December, 2021

IMPLEMENTATION OF ACTIVE INDUCTORS WITH OXIDE THIN-FILM TRANSISTORS AND INTEGRATION INTO OSCILLATOR CIRCUITS

HUGO FILIPE MATIAS VIANA

Bachelor of Sciences in Micro and Nanotechnology Engineering

Advisor: Prof. Dr. Pedro Miguel Cândido Barquinha, Associate Professor, NOVA University Lisbon

Co-advisor: Prof. Dr. Pydi Ganga Mamba Bahubalindruni, Assistant Professor,
Indian Institute of Science Education and Research Bhopal

Examination committee:

Chairperson: Prof. Dr. Rodrigo Ferrão de Paiva Martins, Full Professor, NOVA University Lisbon

Rapporteur: Prof. Dr. João da Palma Goes, Full Professor, NOVA University Lisbon

Member: Prof. Dr. Pydi Ganga Mamba Bahubalindruni, Assistant Professor, Indian Institute of Science and Education and Research Bhopal

MASTER OF SCIENCES IN MICRO AND NANOTECHNOLOGY ENGINEERING

NOVA Univeristy Lisbon
December, 2021

Implementation of Active Inductors with Oxide Thin-Film Transistors and Integration into Oscillator Circuits

Aos meus pais

ACKNOWLEDGEMENTS

Concluding this work is the end of a long and anticipated goal of my life. This results from 5 years of hard work, happiness, tough and good moments, where I would not succeed without the people that walked with me, so I want to appreciate those that were by my side.

A special and a huge thanks to my advisors, professor Ganga and professor Pedro. To professor Ganga, thank you for helping me to understand the concepts and for the availability to clear my doubts. For the innumerous videocalls during these months, even with time zone confusion, even with my English difficulties, you always tried to help me the best you could. To professor Pedro, despite most of the topics being out of your expertise area, you contributed with ideas and ways to overcome and solve the problems that I faced. Thank you also for the understanding on more personal matter when I was going through a less good period, you tried to push me and motivate to achieve good results.

To Uninova and DEEC department for providing the access to machine with Cadence with 130 nm MOS and TFT model that allowed the production of this work.

To all the professors, that one way or another contributed to my success during these academic years. A special thanks to professor Luís Pereira, professor Joana Pinto, professor Rita Branquinho and professor Pedro Barquinha (once again) from DCM since our paths crossed multiples times, and I believe that you always gave your best to teach and motivate us. From DEEC, professor Luís Oliveira, professor Nuno Paulino and professor Maria Helena Fino for taking my electronics knowledge to a higher level.

Obrigado a todos os que fizeram parte do meu percurso académico, que tornaram estes 5 anos muito para além das cadeiras e das horas de estudo, trouxeram momentos e lembranças de companheirismo, interajuda e de amizade:

À minha família de praxe, os meus afilhados Vasco, Pedro e Mariana pela diversão e bons momentos que partilhamos durante os churrascos do meu 2º ano, mesmo agora, depois de 3 anos, continuarmos a ter essa relação. À minha afilhada mais nova, Catarina, obrigado pelo apoio que demonstras e por ajudares a ser melhor pessoa. Aos meus netos, Mané, Bia, Gui, Ricardo, Laura, Matilde, Matita e Diogo por terem contribuído para que a minha experiência de praxe tenha sido melhor.

Ao Freitas, pelas horas de estudo na biblioteca, pelo pior verão da minha vida a estudar quântica, pela camaradagem, pelas aventuras de trotinete a altas horas da noite (com alguns acidentes à mistura), apesar de agora seres emigrante e já não mantermos a mesma proximidade, eu sei que estás a torcer por mim como eu torço por ti. Ao grupo da 202 com várias horas de estudo e outras tantas de procrastinação: à Amanda, pela companhia no estágio, pelos muitos trabalhos feitos juntos, pelas chamadas de atenção merecidas; ao Bernas, pelas horas a jogar *Valorant*, por outras tantas horas postas em trabalho juntos; ao Sabino, pelas conversas sobre tudo e sobre nada com cerveja como companhia; ao Tomás, pelas *heals* no *Valorant*, pelos jantares na cantina; à Joana pelas discussões desde aulas práticas Física I até monografia de MTMP. A todos que participaram neste percurso: Rui, Freire, Leonor, Caril, Diogo, Francisco Silva, Pipo, Maria, Tiago, obrigado.

O meu obrigado aos meus colegas de casa que se tornaram amigos: Filipe aka Jaime pelo apoio, pelos jantares e festas, pela sabedoria e conselhos; Chico pelas horas de jogos desde *CS, Valorant, League*, etc., pela companhia nas idas ao supermercado, pelas conversas filosóficas ou sem sentido, pela parceria a ver vídeos, músicas, *streams*, por seres a pessoa mais tranquilo que eu alguma vez convivi.

Aos meus amigos da "terrinha": ao André por todos estes anos juntos, nos bons ou maus momentos, pelas saídas, pelas conversas, pelas peladinhas, por tudo e mais alguma coisa, meu irmão. Márcia, Ana Maria, Kika, Teixeira, Zé David, Zé Gusto, Braga, Paulinho, Chico, Cate, Adri e Ventura, obrigado por serem bons e velhos amigos.

A ti, Inês, o meu sincero e mais puro obrigado. Tu, desde o início da nossa história tens sido a minha maior força, o meu porto de abrigo, a minha inspiração e motivadora. Estes últimos tempos teriam muito mais difíceis, se não fosses tu. Contigo, encontrei a cumplicidade, o companheirismo, a felicidade, o amor que eu quero e preciso para o que vem a seguir desta fase. Obrigado pelas refeições fantásticas, pelas séries vistas, pelas noites inesquecíveis do "eixo do mal" aos vídeos de russos e polacos passando pelas músicas lendárias, por seres DJ nas viagens de carro, pelas horas de *Valorant* e *League*, pelas brincadeiras que mantemos. Obrigado por tudo.

À minha família, Tita, Davi e Bruno, que estão sempre disponíveis para me ajudar. A ti, minha mana, obrigado pelo apoio e conselhos, mesmo estando tão distante fisicamente. Ao meu sobrinho mesmo não crescendo contigo, a tua alegria e fofura transpassa a videochamada. Ao resto da família, obrigado.

Para terminar, o meu maior e mais especial agradecimento aos meus pais, Irene e Fernando, a quem dedico também este trabalho, pois sem eles não seria possível chegar onde estou hoje e para onde ambiciono chegar. Sempre estiveram presentes e fizeram de tudo para me dar apoiar e ajudar no que fosse necessário. Sempre educaram o melhor conseguem, sempre me ensinaram a ser uma boa e humilde pessoa, a ter orgulho nas minhas origens e hoje digo: tenho orgulho no homem que sou e donde venho, graças a vocês, por isso, OBRIGADO.

"Engineers must be forever frustrated to continue to design things that work better"
(Max Conze – Dyson's ex-CEO)

ABSTRACT

This work aims to investigate the replacement of passive inductors with active inductors (aLs) using amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors (TFT). The goal of aL is to emulate the inductive behavior associated with passive inductors. The advantage of the former is the small die area, high quality-factor, inductance, and self-resonant frequency tunability.

A simple grounded n-type aL was used to replace the inductor in an inductance-capacitance (LC) oscillator. The LC oscillator is constituted by a cross-couple pair and two aLs. The simple grounded aL configuration was used due to a-IGZO being an n-type semiconductor and also owing to its simplicity, being only built with two transistors and two current sources. These factors allied with the lack of a counterpart p-type amorphous oxide semiconductor make this aL a good fit for the proposed work. The oscillator was simulated using metal-oxide-semiconductor field-effect transistor (MOSFET) and TFTs. The former was simulated with a channel length of 1 µm and the latter was simulated with two channel-lengths 10 µm and 20 µm. The MOS technology simulations were used as a proof-of-concept since these have more accurate models. The oscillation frequency (f_{OSC}) and output peak-to-peak voltage swing (V_{pp}) were analyzed for both technologies. Temperature sensibility, and phase noise were also examined for the MOS technology.

The MOS oscillators with three different aLs presented an f_{OSC} between 917 MHz and 2.08 GHz, power consumption from 21 mW to 80 mW, a V_{pp} of 613 mV up until 1.78 V with a power supply voltage (V_{DD}) of 5V. The maximum phase noise was - 92.86 dBc/Hz at an offset of 1 MHz. A 10 µm a-IGZO TFTs oscillator produced an f_{OSC} of 1.21 MHz and a V_{pp} of 3.83 V, dissipating 533 µW for a V_{DD} of 10V.

Keywords: a-IGZO TFT; Active inductor (aL); Simple grounded aL; Cross-couple pair LC-oscillator.

RESUMO

Este trabalho tem como objetivo investigar a substituição de indutores passivos por bobines ativas (aLs), utilizando transístores de filme fino (TFT) de óxido de índio-gálio-zinco amorfo (a-IGZO). O objetivo do aL é emular o comportamento associado aos indutores passivos. As vantagens dos aLs são: pequena área de implementação, alto fator de qualidade e indutância e frequência de ressonância ajustáveis.

Um aL simples conectado à massa foi usado para substituir a bobine no oscilador de indutância-capacitância (oscilador LC). O oscilador LC é constituído por um par cruzado e dois aLs. A utilização da configuração do aL simples conectado à massa deve-se ao facto do a-IGZO ser um semiconductor tipo-n, e à sua simplicidade. Este é apenas constituído por dois transístores tipo-n e duas fontes de corrente. Estes fatores aliados à falta de um óxido semiconductor tipo-p de qualidade torna esta configuração apelativa. A simulação do oscilador foi realizada através das tecnologias de metal-óxido-semicondutor (MOS) e TFT. No caso da primeira, o comprimento de canal (L_{CH}) foi de 1 µm e no caso da segunda, implementaram-se 2 L_{CH}: 10 e 20 µm. As simulações da tecnologia MOS funcionaram com prova de conceito. Analisou-se a frequência de oscilação (f_{OSC}) e tensão de pico-a-pico (V_{pp}) nos osciladores de ambas as tecnologias. Adicionalmente, a sensibilidade à temperatura e o ruído de fase foram analisados para a tecnologia MOS.

Os osciladores LC implementados com três diferentes aLs utilizando transístores MOS apresentaram f_{OSC} entre 917 MHz e 2.08 GHz, potência dissipada desde 21 mW até 80 mW e V_{pp} variando de 613 mV até 1.78 V, utilizando 5 V como fonte de alimentação (V_{DD}). O ruído de fase máximo foi de -92.86 dBc/Hz a 1 MHz. O oscilador LC utilizando TFTs produziu uma f_{OSC} = 1.21 MHz e V_{pp} = 3.83 V, dissipando 533 µW com V_{DD} = 10 V.

Palavras-chave: a-IGZO; Bobine ativa (aL); aL simples conectado à massa; oscilador LC de par cruzado.

LIST OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACRONYMS AND ABBREVIATIONS

ADE	Analog Design Environment
a-IGZO	Amorphous Indium-Gallium-Zinc Oxide
aL	Active Inductor
ANN	Artificial Neural Network
AOS	Amorphous Oxide Semiconductor
CMOS	Complementary Metal-Oxide-Semiconductor
D	Drain
DC	Direct Current
EC	Equivalent Circuit
FET	Field-Effect Transistor
FoM	Figure of Merit
G	Gate
hb	Harmonic Balance
KCL	Kirchhoff's Current Law
LC	Inductance-Capacitance
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NoF	Number of Finger
Q-factor	Quality Factor
RF	Radio Frequency
RHP	Right-Half Plane
RLC	Resistance-Inductance-Capacitance
RO	Ring Oscillator
S	Source
TFT	Thin-Film Transistor
UMC	United Microelectronics Corporation
USB	Upper Sideband
XPC	Cross-Couple Pair

SYMBOLS

B	Susceptance
B_A	Active circuit susceptance
B_F	Frequency-determining susceptance
C	Capacitance
C_{DB}	Drain-to-bulk capacitance
C_{GD}	Gate-to-drain capacitance
C_{GS}	Gate-to-source capacitance
C_{OV}	Overlap capacitance
C_{OUT}	Output capacitance
C_{OUT_T}	Total output capacitance
C_{ox}	Specific capacitance of the gate dielectric per unit area
C_p	Parallel capacitance
C_{XCP}	Cross-couple pair parasitic capacitance
f_{OSC}	Oscillation frequency
$f_{OSC_{aL}}$	Active inductor theoretical oscillation frequency
f_{OSC_S}	Simulated oscillation frequency
f_{OSC_T}	Theoretical oscillation frequency
G	Conductance
G_A	Active circuit conductance
g_{ds}	Drain-to-source conductance
G_F	Frequency-determining conductance
G_m	Transconductance of transconductor
g_m	Transconductance of transistor
G_o	Total conductance
G_{XCP}	Cross-couple pair conductance
$H(s)$	Forward transfer function
I	Current
I_A	Active circuit current
I_{DS}	Drain-to-Source current
I_{in}	Input current
Im	Imaginary part
I_{OUT}	Output current
j	Imaginary number
J	Current source current
L	Inductance
L_{CH}	Channel length
L_{eq}	Equivalent inductance
Max	Maximum
Min	Minimum

R	Resistance
R_A	Active circuit resistance
Re	Real part
R_F	Frequency-determining resistance
r_{ON}	Drain-to-source ON resistance
R_p	Parallel resistance
R_s	Serie resistance
R_{XCP}	Cross-couple pair resistance
s	Product of imaginary number and angular frequency
t	Instant of time
V	Voltage
V_A	Active circuit voltage
V_{DD}	Power supply voltage
V_{DS}	Drain-to-Source voltage
V_{GS}	Gate-to-source voltage
V_{OUT}	Output voltage
V_{pp}	Peak-to-peak voltage
V_{TH}	Threshold voltage
W	Channel width
X	Reactance
X_A	Active circuit reactance
X_F	Frequency-determining reactance
X_{OUT}	Input signal
Y	Admittance
Y_A	Active circuit admittance
Y_F	Frequency-determining admittance
Y_{OUT}	Output signal
Z	Impedance
Z_A	Active circuit impedance
Z_F	Frequency-determining impedance
Z_{IN}	Input impedance
$\beta(s)$	Feedback transfer function
μ	Mobility
λ	Channel length modulation factor
ω	Angular frequency
ω_o	Self-resonant angular frequency
ω_{osc}	Oscillation angular frequency
ω_p	Complex conjugate poles angular frequency
ω_z	Zero angular frequency

1 MOTIVATION AND OBJECTIVES

In recent years, the demand for low-cost and flexible alternatives to the typical silicon metal-oxide-semiconductor field-effect transistor (MOSFET) technology has been increasing [1]. Amorphous oxide semiconductors (AOS) have been demonstrated as a viable choice, due to their good optical and electrical properties, besides low-temperature depositions, and smooth surfaces [2]. Amorphous indium-gallium-zinc oxide (a-IGZO) is one most studied for this purpose. a-IGZO thin-film transistors (TFTs) are being applied in the design of analog/mixed-signal circuits [3]–[6]. The a-IGZO is an n-type semiconductor, and there is a lack of quality p-type AOS counterpart, which does not allow the use of design technique known as complementary MOS (CMOS) [7].

This work is focused on the application of active inductor (aL) using a-IGZO TFTs. The aLs are characterized for small die area, high quality-factor, inductance and self-resonant frequency tunability [8], [9]. The MOS aL found a multitude of applications, such as bandwidth improvement, oscillators, and filters [8].

The application chosen for this work was the replacement of typical passive inductor of the inductance-capacitance (LC) cross-coupled oscillator to simple grounded aL presented in [10].

Simulations in the Cadence Virtuoso environment were performed using MOS and TFT technologies. MOS technology was applied as a proof-of-concept to design an LC oscillator with different simple grounded aL, verifying the oscillation frequency, output voltage swing, temperature sensibility, and phase noise. Then, an in-house model was used to simulate the a-IGZO TFTs LC oscillator with the simple grounded aLs and attest their performance. There are only a few works exploring aL using TFTs as a substitute for the traditional inductor. These concepts permit the design of kHz-MHz range LC oscillator in small areas and high tunability allowing the design of sensor project or ultimately communication systems [11].

This work received funding from the European Community's H2020 program under grant agreement no. 716510 (ERC-2016-StG TREND).

2 INTRODUCTION

In this chapter, the working principles, structures, applications of thin-film transistor (TFT) are introduced in the first topic, as well as the comparison between TFTs and metal-oxide-semiconductor (MOS). Next, available TFT technologies are presented. The increasing demand for circuit design using amorphous oxide semiconductors (AOS) is addressed, with a special focus on amorphous indium-gallium-zinc oxide (a-IGZO) TFTs. Inductive elements are presented in the following topic, highlighting the active inductor (aL), its working and implementation principles, and its frequency range constraints. Lastly, oscillator circuits, respective model and oscillation conditions are described.

2.1 THIN-FILM TRANSISTOR

A TFT is a type of field-effect transistor (FET). Contrarily to MOSFETs, TFTs only have three terminals: gate (G), drain (D), source (S) – there is no bulk terminal due to the substrate being an insulator [2], [3]. The typical structures of TFTs are staggered or coplanar depending if the semiconductor is on the opposite side of the S/D terminals, or the same side, respectively. Besides that, TFTs can be distinguished between the top or bottom gate, depending on if the gate terminal is on top or bottom of the structure [2], [12]. These configurations are presented in Figure 1, as well as the typical structure of MOSFETs. Another major difference among these two types of FET is the channel formation between S and D. The TFT channel is created by an accumulation layer and the MOSFET channel is formed by an inversion region, both at the semiconductor/dielectric interface [2].

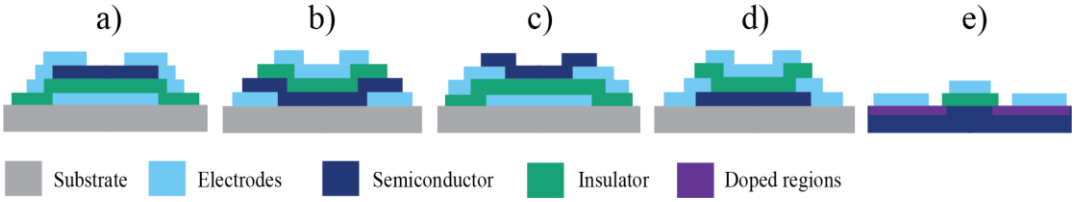

Figure 1 - Typical structures of FET: a) staggered bottom-gate TFT; b) staggered top-gate TFT; c) coplanar bottom-gate TFT; d) coplanar top-gate TFT; e) MOSFET.

When compared with MOSFETs, TFTs are more suitable for large-area applications, due to their lower cost [12]. Also, TFTs allow for the integration of devices and circuits on new substrates, which enable new applications, such as flexible displays [12] or paper electronics [2].

There are several different TFTs technologies available: oxide semiconductor, amorphous silicon, low-temperature polycrystalline silicon, and organic semiconductors. In recent years, oxide semiconductor-based TFTs gain more notability, especially AOS. These demonstrate simultaneously good optical and electrical proprieties, besides low-temperature depositions, and smooth surfaces. a-IGZO is the most popular AOS example. Indium-gallium oxide or indium-zinc oxide are other examples [2].

a-IGZO TFTs are already being used in the design of analog/mixed-signal circuits [3]–[6], and these are n-type devices, which means that electrons are responsible for channel accumulation [7]. The major limitation of AOS in circuit design is the lack of a quality p-type counterpart. This makes the well-known complementary MOS (CMOS) design not possible – consistently implemented in MOSFET technology. A solution for this is design techniques like pseudo-CMOS or hybrid-CMOS [7].

2.1.1 Working principles of a FET

TFTs and MOSFETs are ON when the voltage between G and S (V_{GS}) is greater than threshold voltage (V_{TH}), otherwise, the devices are sub-threshold regime and current that passes through the D and S (I_{DS}) is residual (ideally sub-pA). Being ON, the FETs exhibit two regions of operation: linear and saturation region. These are controlled by the voltage applied between the D and S terminals (V_{DS}), which affects I_{DS}. Accordingly, the two operation regimes are described by (2.1), and (2.2), respectively. W is the channel width, L_{CH} is the channel length, μ is the charge carrier mobility, C_{ox} is the specific capacitance of the G dielectric per

unit area. λ is the channel length modulation factor, which is relevant for short-channel, otherwise, it can be assumed as zero [7].

$$I_{DS} = (W/L_{CH})\,\mu C_{ox}(V_{GS} - V_{TH})V_{DS} \quad \text{if } V_{GS} > V_{TH} \text{ and } V_{DS} << V_{GS}\text{-}V_{TH} \quad (2.1)$$

$$I_{DS} = (W/2L_{CH})\,\mu C_{ox}(V_{GS} - V_{TH})^2(1 + \lambda)V_{DS} \quad \text{if } V_{GS} > V_{TH} \text{ and } V_{DS} > V_{GS}\text{-}V_{TH} \quad (2.2)$$

2.2 ACTIVE INDUCTOR

Inductors are employed for different purposes in high-speed analog signal processing: bandwidth improvement, oscillators, impedance matching, radio frequency (RF) bandpass filters, RF phase shifters, amplifiers, and many more applications [8].

Inductor elements are characterized for storing the magnetic field when electrical currents pass through by it [13]. Nowadays, on-chip inductors are widely used when compared with traditional off-chip ones, especially for RF applications. The former presents a smaller size, lower cost, and wider bandwidth characteristics [13]. Therefore, they allow for the integration of inductive elements on a single monolithic substrate [8], [13]. Despite that, on-chip inductors present an moderate quality-factor (Q-factor) when compared with their off-chip counterparts, due to smaller element dimensions and a multilevel fabrication process, which translates to more parasitic capacitances and resistances [13].

The demand for even more compact and tunable inductive elements led to intense research and study on the design of inductors employing active devices [8]. This configuration is known as an aL, and it consists of networks with transistors. aLs under specific direct-current (DC) biasing conditions and signal-swing constraints exhibit inductive behavior in a particular frequency range [8]. Table 1 presents a comparison between aLs and on-chip inductors.

Table 1 - Comparison between the active inductor and passive on-chip inductor (adapted from [8] and [9]).

Parameter	Active inductor	Passive on-chip inductor
Area	Small die area	Large die area
Inductance and self-resonant frequency	Large tunability	Fixed
Q-factor	High and tunable	Low and fixed
Power consumption	Significant	Zero
Noise performance	Poor	No noise (ideally)
Linearity	Poor	Good
Electromagnetic Interference	Insensitive	Significant

2.2.1 Working principles of an active inductor

An aL could be built using a gyrator-based synthesis. This is made up of two back-to-back transconductors. If a capacitor is connected to one of the terminals, the network is called a gyrator-C [8].

A lossless single-ended gyrator-C is presented in Figure 2. This means input and output impedances of the transconductors are infinite and the transconductances are constant. Considering (2.3), where Y is the admittance, I_{in} is the input current, V_1 and V_2 are the voltages at nodes 1 and 2, respectively. G_{m1} and G_{m2} are the transconductance of transconductors 1 and 2, respectively. s is the product of j (imaginary number) and ω (angular frequency). Note that one of the transconductors must have a positive transconductance and the other one must have a negative transconductance [8].

$$Y = \frac{I_{in}}{V_2} = \frac{1}{s\left(\frac{C}{G_{m_1}G_{m_2}}\right)} \quad (2.3)$$

According to (4), the equivalent inductance of gyrator-C (L_{eq}) is given by (4).

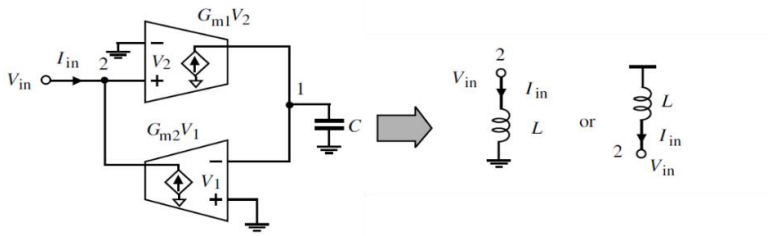

Figure 2 - Ideal gyrator-C circuit and its equivalent circuit. V_1 and V_2 are the voltages at nodes 1 and 2, respectively. G_{m1} and G_{m2} are the transconductance of transconductors 1 and 2, respectively. C is the capacitor at node 1. One of the transconductors must have a positive transconductance and the other one must have a negative transconductance (adapted from [8]).

$$L_{eq} = \frac{sC}{G_{m_1} G_{m_2}} \tag{2.4}$$

However, in practical applications no transconductor is lossless. Thus, input and output impedance are finite and the transconductance is not constant [8]. The non-ideal gyrator-C aL is shown in Figure 3. To simplify the writing of Kirchhoff's current laws (KCL), it is assumed that the transconductance are constant, as stated in (2.5). G_{o1} and G_{o2} represent the total conductances at nodes 1 and 2, respectively. Notice that G_{o1} includes the finite input impedance of the transconductor 2 and the finite output impedance of transconductor 1. C_1 and C_2 represent the total capacitance at nodes 1 and 2, respectively [8].

$$Y = \frac{I_{in}}{V_2} = sC_2 + G_{o2} + \frac{1}{s\left(\frac{C_1}{G_{m_1} G_{m_2}}\right) + \frac{G_{o1}}{G_{m_1} + G_{m_2}}} \tag{2.5}$$

Analyzing admittance, which is stated in (2.5), it is possible to infer that the aL resistance-inductance-capacitance (RLC) network equivalent is given by (2.6), being L_{eq} the inductance, C_p the parallel capacitance, R_p the parallel resistance, and R_s the series resistance. The L_{eq} value is not affected by the finite impedances. R_p should be boosted while R_s should be reduced to minimize the ohmic loss [8].

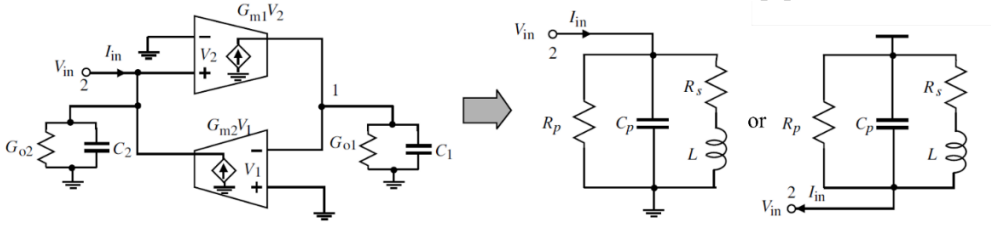

Figure 3 - Lossy gyrator-C circuit and its equivalent circuit. V_1 and V_2 are the voltages at nodes 1 and 2, respectively. G_{m1} and G_{m2} are the transconductance of transconductors 1 and 2, respectively. G_{o1} and G_{o2} represent the total conductances at nodes 1 and 2, respectively. G_{o1} includes the finite input impedance of the transconductor 2 and the finite output impedance of transconductor 1. C_1 and C_2 represent the total capacitance at nodes 1 and 2, respectively (adapted from [8]).

$$L_{eq} = \frac{C_1}{G_{m_1} G_{m_2}} \tag{2.6.1}$$

$$C_p = C_2 \tag{2.6.2}$$

$$R_p = 1/G_{o2} \tag{2.6.3}$$

$$R_s = \frac{G_{o1}}{G_{m_1} G_{m_2}} \tag{2.6.4}$$

2.2.2 The frequency range of the active inductor

The lossy aL does not present an inductive behavior across the entire range of frequency, due to the parasitic elements. This results in three behaviors through the frequency spectrum: resistive, inductive, and capacitive [8]. The input impedance (Z_{IN}) of the RLC equivalent circuit (EC) is given by (7).

$$Z_{IN} = \left(\frac{R_s}{C_p L_{eq}}\right) \frac{s\, L_{eq}/R_s + 1}{s^2 + s\left(\frac{1}{R_p C_p} + \frac{R_s}{L_{eq}}\right) + \frac{R_p + R_s}{R_p C_p L_{eq}}} \tag{2.7}$$

The zero of the impedance (ω_z) is related to the lowest frequency that the circuit acts as an inductor and

it is given by (2.8). Lower than that frequency, its behavior is resistive. The self-resonant angular frequency (ω_o) dictates the maximum frequency of the inductive behavior, which is stated by (2.9). At frequencies higher than ω_o, the gyrator presents a capacitive characteristic. This results from the meeting of the poles, creating complex conjugate poles (ω_p). Considering $R_p \gg R_s$, (2.9) is shortened to (2.10), which is the ω_o [8].

$$\omega_z = R_s/L_{eq} \tag{2.8}$$

$$\omega_p = \sqrt{\frac{R_p + R_s}{R_p C_p L_{eq}}} \tag{2.9}$$

$$\omega_p \approx \sqrt{1/C_p L_{eq}} = \omega_o \tag{2.10}$$

2.2.3 The quality factor of the active inductor

There are different definitions of the Q-factor of an inductor. The most general is defined as the ratio of magnetic energy stored to its ohmic loss in one oscillation cycle, as described by (2.11). Also, (2.11) can be interpreted as the ratio between the inductive reactance and the resistance, as presented in (2.12) [8]. The terms are the imaginary ($Im[Z_{IN}]$) and real part ($Re[Z_{IN}]$) of Z_{IN}. Combining (2.12) and (2.7), results in (2.13) [8].

$$\text{Q-factor}_1 = 2\pi \frac{\text{Net magnetic energy stored}}{\text{Energy dissipated in one cycle}} \tag{2.11}$$

$$\text{Q-factor}_2 = Im[Z_{IN}]/Re[Z_{IN}] \tag{2.12}$$

$$\text{Q-factor}_3 = \left(\frac{\omega L_{eq}}{R_s}\right) \frac{R_p}{R_p + R_s + (\omega L_{eq})^2/R_s} \left(1 - \frac{R_p^2 C_p}{L} - \omega^2 L_{eq} C_p\right) \tag{2.13}$$

2.3 OSCILLATOR

An oscillator is a circuit that generates a periodic signal without any input signal [14]. They are applied in communication systems and instrumentation [11].

There are several oscillator topologies, and these can be based on different principles of implementation. Oscillators can be categorized into two major classes: relaxation oscillators and harmonic oscillators. Harmonic oscillators deliver a near-sinusoidal signal with good phase noise and high spectral purity. Relaxation oscillators are usually characterized by a poor phase noise and high harmonic content, as the circuit switches intermittently between two astable equilibrium states [11].

The LC oscillator and ring oscillator are two examples of harmonic oscillators. The first is a lumped resonator-based oscillator. To design this oscillator, an inductor and a capacitor are necessary (two forms of reactive components), to achieve complex poles. The ring-oscillator is a non-resonator-based oscillator example that only requires either capacitors or inductors (one type of reactive element). However, the presence of resistive elements and feedback is vital for non-resonator-based oscillator implementation [15].

2.3.1 Oscillation conditions

There are two models to analyze an oscillator: feedback model and negative resistance model [11], [15]. The model utilized depends on the oscillators' configuration and characteristics [11].

Oscillators analyzed by the feedback model can be separated into a forward network and feedback network [11], as shown in Figure 4 a). The negative resistance model can be decomposed into a one-port active circuit and a one-port frequency-determining circuit, as presented in Figure 4 b). The active circuit goal is to create a small-signal negative resistance on the operating point of the oscillator, and it is characterized by the admittance Y_A (or impedance Z_A). The frequency-determining circuit is typically a linear time-invariant circuit, and it is signal independent, being characterized by the admittance Y_F (or impedance Z_F). When connected, the characteristics of both blocks will determine the oscillation frequency [11].

2.3.1.1 Steady-state oscillation conditions

The feedback model's transfer function Y_{OUT}/X_{OUT} is given by (2.14), where *H(s)* is the forward transfer

function and *β(s)* is the feedback transfer function, as presented in Figure 4 a) [15].

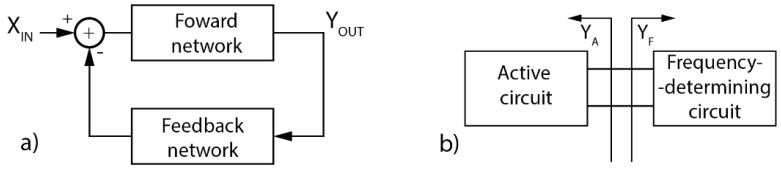

Figure 4 - Oscillators models: a) feedback model - X_{IN} and Y_{OUT} are the input and output signal; b) negative-resistance model - Y_A is admittance of the active circuit and Y_F is the admittance of frequency-determining circuit (adapted from [11]).

$$\frac{Y_{\text{out}}}{X_{\text{in}}} = \frac{H(s)}{1 + H(s)\beta(s)} \tag{2.14}$$

In the steady-state, an oscillator must fulfill the conditions of the Barkhausen's criteria to oscillate. The first condition is known as the "gain condition" and the second one is named as "phase condition". The Barkhausen's criteria conditions are stated in (2.15.1) and (2.15.2), respectively [15], [16].

$$|H(s)\beta(s)| = 1 \tag{2.15.1}$$

$$\angle H(s)\beta(s) = 180° \tag{2.15.2}$$

The negative resistance model, as aforementioned is described by Y_A (or Z_A[1]) and Y_F (or Z_F[1]) –Figure 4 b). These admittances can be separated in their conductance (G) and susceptance (B) at a determined angular frequency (ω), as presented in (2.16) and (2.17), respectively [15], [16].

$$Y_{\text{A}}(\omega) = G_{\text{A}}(\omega) + jB_{\text{A}}(\omega) \tag{2.16}$$

$$Y_{\text{F}}(\omega) = G_{\text{F}}(\omega) + jB_{\text{F}}(\omega) \tag{2.17}$$

To oscillate in the steady-state, an oscillator analyzed by the negative resistance model must satisfy the conditions stated in (19), where ω_{osc} is the oscillation angular frequency [15], [16].

$$G_{\text{A}}(\omega_{\text{osc}}) + G_{\text{F}}(\omega_{\text{osc}}) = 0 \tag{2.18.1}$$

$$B_{\text{A}}(\omega_{\text{osc}}) + B_{\text{F}}(\omega_{\text{osc}}) = 0 \tag{2.18.2}$$

2.3.1.1 Start-up conditions

The steady-state does not predict the start-up conditions of an oscillator. The oscillator must start to oscillate in an autonomously way when the circuit is switched on, usually triggered by the noise of the system [15].

To ensure that oscillation begins, the open loop gain of the feedback model should be greater than one, as stated in (2.19). The phase condition is described by (2.15.2) [15]. To convert the start-up conditions to the steady-state conditions, there are two mechanisms to reduce the open-loop gain to the conditions presented in (2.15), being automatic gain control and self-limiting [15].

$$|H(s)\beta(s)| > 1 \tag{2.19}$$

The conductance start-up conditions of the negative resistance model are described by (2.20) and the susptance condition continues to follow (2.18.2). Active circuit conductance should be negative enough to cancel the losses of the frequency-determining circuit to start the oscillation [15], [16].

$$G_{\text{A}}(\omega_{\text{osc}}) + G_{\text{F}}(\omega_{\text{osc}}) < 0 \tag{2.20}$$

2.3.1.1 Complex conjugate poles

As discussed, an oscillator must fulfill the start-up conditions. Despite these being necessary, they are not sufficient for the circuit to start to oscillate. The circuitry must have a pair of complex-conjugate poles in the right-half plane (RHP) [11], [15], [16]. These poles are responsible for the input signal growth. Ultimately, this increase is restricted by nonlinearities in the circuit [11], [16].

1 – Or impedances for a series circuit: $Z_{\text{A}}(\omega) = R_{\text{A}}(\omega) + jX_{\text{A}}(\omega)$ and $Z_{\text{F}}(\omega) = R_{\text{F}}(\omega) + jX_{\text{F}}(\omega)$, R is resistance and X is reactance. The subscript *A* and *F* denote active circuit and frequency-determining circuit, respectively. (2.19.2) condition become $X_{\text{A}}(\omega_{\text{osc}}) + X_{\text{F}}(\omega_{\text{osc}}) = 0$. (2.18.1) condition becomes $R_{\text{A}}(\omega_{\text{osc}}) + R_{\text{F}}(\omega_{\text{osc}}) = 0$ and (2.20) condition becomes $R_{\text{A}}(\omega_{\text{osc}}) + R_{\text{F}}(\omega_{\text{osc}}) < 0$ [11], [15].

3 METHODOLOGY

In this section, simulation methodology is described. All the designs and the simulations were carried out using the Cadence® Virtuoso® Analog Design Environment (ADE). This section is divided into two subsections: MOS and TFT technology.

In the first subsection, MOS technology is used as a proof-of-concept, applying the United Microelectronics Corporation (UMC) 130 nm library. The design requirements for the oscillator and aL are then explained. Next, simulations are described. The second subsection is related to TFT technology design and simulations, where an in-house model is used.

3.1 CIRCUIT DESIGN

The oscillator and aL schematics were inserted into Virtuoso® ADE. Here, voltages, currents, and transistors dimensions were defined. As aforementioned, due to a-IGZO being an n-type semiconductor and AOS not having a quality p-type counterpart, only n-type transistors were used during the design.

The oscillator was designed using the negative resistance model. According to (2.20), the sum of G_A and G_F. must be lower than zero. In the steady-state condition, the sum of G_A and G_F must be equal to zero, as stated in (2.18.1). (2.18.2) dictates that B_A and B_F must be symmetric. Hence, the transistor dimensions and bias conditions were selected to fulfill the oscillations conditions, using the MOS and TFT technologies.

3.2 CIRCUIT SIMULATION

3.2.1 MOS technology

The UMC 130 nm library was employed for MOS simulation in the MOS technology. Due to MOS technology having a more developed and precise model, it was applied as a proof-of-concept.

3.2.1.1 Oscillator simulation

A DC analysis was run to check if all the transistors were in the pretended operating regime – for this work, all the transistors must be in the saturation region. A transient analysis was performed. The stop time was defined to be sufficiently large to observe multiple oscillations. The circuit takes a few periods to achieve the steady-state, so the oscillation frequency (f_{OSC}) and peak-to-peak voltage (V_{pp}) of the output voltage (V_{OUT}) are extracted accordingly.

A temperature sweep from -40 ºC to +85 ºC (industrial temperature range [17]) was performed to infer the oscillator temperature sensibility.

To find the oscillator phase noise it was necessary to perform two analyses: a harmonic balance (hb) and an hb noise analysis. To execute the former, stop time and fundamental oscillation were the same used and obtained from the transient analysis. The latter analysis' goal was to measure the upper sideband (USB) contribution.

3.2.1.2 aL simulation

The aL RLC EC parameters were obtained using the DC operating point. The half of the circuit was considered to perform the simulation. A scattering-parameters (S-parameters) analysis was performed, namely the impedance parameters (Z-parameters). From this analysis, it is possible to observe the $Im[Z_{IN}]$, $Re[Z_{IN}]$, and phase of RLC equivalent circuit.

3.2.2 TFT technology

The model used in Cadence® Virtuoso® for TFT simulation was an in-house model, reported in [3]. The model consists of a TFT EC, which involves the parasitic elements (C_{GS} and C_{GD}) between the different electrodes and a dependent current source represents the current between the S and D electrodes. An individual artificial neural network (ANN) was developed for each element. Then, the device model was achieved by linking the ANNs as per the EC. The resulting model was implemented in Verilog-A for circuit simulations,

allowing to predict with good accuracy the device's static and dynamic behavior [3]. The oscillator and aL design followed the same methodology presented in section 3.1. However, the transistor model was the Verilog-A in-house model.

3.2.2.1 Oscillator and aL simulation

The oscillator and aL simulation were carried out using the Virtuoso® ADE. Analogous to the procedure described in Oscillator simulation and aL simulation, A DC analysis was performed to ensure that the transistors were in the saturation region, being followed by a transient simulation. The V_{pp} and f_{OSC} measurements were extracted once the oscillations were stabilized.

Due to the used TFTs model [3], it is not possible to infer about the oscillator temperature sensibility. In the same way, it is not possible to perform the oscillator phase noise.

4 RESULTS AND DISCUSSION

Firstly, the LC-oscillator theoretical is analyzed in this section, including aL and XPC circuit analyses. Next, MOS technology implementation and results are discussed, focusing on the design and simulations. Then, TFT design and simulations of the aL-based LC-oscillator are examined.

4.1 LC-OSCILLATOR THEORETICAL ANALYSIS

The LC-oscillator consists of an LC tank and a negative resistance. Usually, this circuit is made with a passive inductor and a cross-couple pair (XCP) – Figure 5 a). These are extensively employed in wireless communications, with multiple works reported. The main advantage of the passive inductor is the low level of phase noise [8]. The theoretical f_{OSC} of the LC-oscillator (f_{OSC_T}) is presented in (4.1), where L is the inductance and C_{OUT} is the capacitance associated with the output node.

$$f_{\mathrm{osc_T}} = \frac{1}{2\pi\sqrt{LC_{\mathrm{OUT}}}} \tag{4.1}$$

The goal of this work is to replace the passive inductor with an aL, due to the advantages mentioned in Table 1. The oscillator was analyzed according to the negative resistance model. So, as previously mentioned in section 2.3.1, the oscillator is divided into an active circuit and frequency-determining circuit. The former was achieved using an XCP and the latter one applying aLs. The schematic of the oscillator implemented with aLs is shown in Figure 5 b).

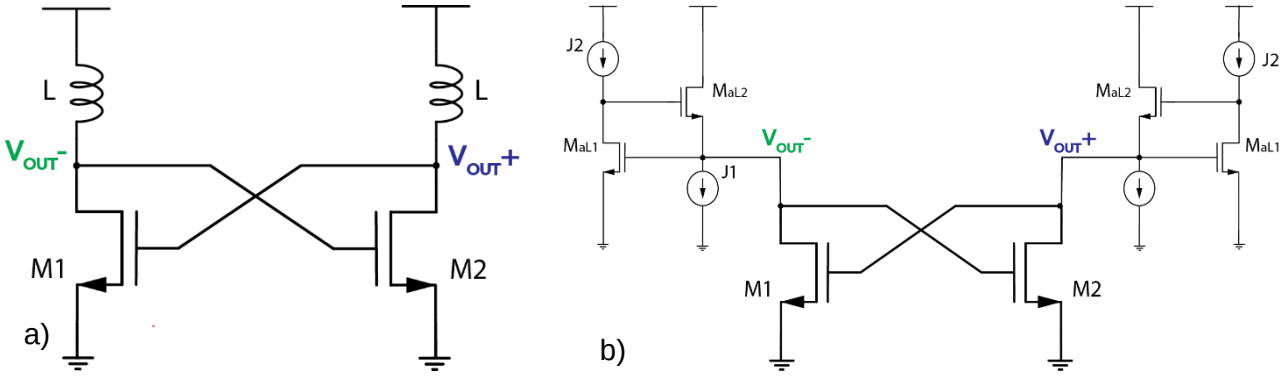

Figure 5 - a) passive inductor-based LC-oscillator; b) active inductor-based LC-oscillator.

The LC-oscillator presents a basic working principle. Output voltage (V_{OUT}) can be extracted at the drain of M_1 or M_2, being labeled V_{OUT}– and V_{OUT}+, respectively. At oscillation frequency (which corresponds to the self-resonant frequency) the impedance of the circuit is resistive since the inductance and capacitance cancel each other [18]. Therefore, V_{OUT} can be approximated by (4.2), where $I_{OUT_{1,2}}$ is the I_{DS} that passes through transistor $M_{1,2}$, $r_{ON_{1,2}}$ is the D to S ON-resistance of $M_{1,2}$ and t is an instant of time [18]. V_{OUT}+ is high and V_{OUT}– is low when the transistor M_1 is in the saturation regime and M_2 is in the linear regime, which corresponds to $I_{OUT\,2}$ being low and r_{ON_2} being in its maximum. Oppositely, V_{OUT}+ is low and V_{OUT}– is high when the transistor M_1 and M_2 are in triode and saturation regions, respectively. These conditions match I_{OUT_2} being high and r_{ON_2} low.

$$V_{\mathrm{OUT}^{-,+}}(t) = I_{\mathrm{OUT}_{1,2}}(t) \cdot r_{\mathrm{ON}_{1,2}}(t) \tag{4.2}$$

4.1.1 Active inductor

As described in section 2.2.1, an aL requires a transconductor with negative transconductance and the other must produce positive transconductance. One of the simplest aL configurations is a common-source as negative transconductor and a common-drain as positive transconductor [8], [19]. This configuration was introduced by M. Ismail et al. in [10] and it is shown in Figure 6, being only constituted by n-type transistors. Additionally, the current sources currents J_1 and J_2 are responsible for polarizing the circuit, ensuring that all

the transistors work in the saturation regime [8], [19]. The intrinsic parasitic capacitances are exploited, instead of the typical grounded capacitor of the gyrator-C architecture [10], [20].

The input impedance (Z_{IN}) of the circuit is given by (4.3), after the cancelation of non-dominant terms [8]. C is the capacitance, g_{ds} is the D to S conductance, g_m is the transconductance. The subscripts GS and GD refer to the quantity between the G and S, G and D, respectively. The subscripts aL1 and aL2 are associated with aL transistors M_{aL1} and M_{aL2}, respectively.

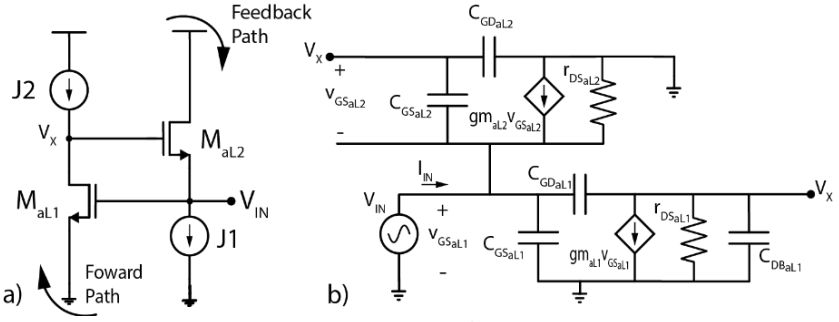

Figure 6 - Simple grounded active inductor: a) schematic; b) high-frequency small-signal equivalent. M_{aL1} is a common-source configuration (forward path) and M_{aL2} is a common-drain configuration (feedback path).

$$Z_{\mathrm{IN}} = \frac{C_{\mathrm{GS_{aL2}}} s + g_{\mathrm{ds_{aL1}}}}{C_{\mathrm{GS_{aL1}}} C_{\mathrm{GS_{aL2}}} s^2 + (C_{\mathrm{GS_{aL2}}} g_{\mathrm{m_{aL1}}} + C_{\mathrm{GS_{aL1}}} g_{\mathrm{ds_{aL1}}}) s + g_{\mathrm{m_{aL1}}} g_{\mathrm{m_{aL2}}} + g_{\mathrm{ds_{aL1}}} g_{\mathrm{m_{aL1}}}} \tag{4.3}$$

From (4.3), it is possible to extract the RLC EC, as stated (2.7), resulting in (4.4.1).

$$L_{\mathrm{eq}} = \frac{C_{\mathrm{GS_{aL2}}}}{g_{\mathrm{m_{aL1}}} g_{\mathrm{m_{aL2}}}} \tag{4.4.1}$$

$$R_{\mathrm{s}} = \frac{g_{\mathrm{ds_{aL1}}}}{g_{\mathrm{m_{aL1}}} g_{\mathrm{m_{aL2}}}} \tag{4.4.2}$$

$$C_{\mathrm{p}} = C_{\mathrm{GS_{aL1}}} \tag{4.4.3}$$

$$R_{\mathrm{p}} = \frac{1}{g_{\mathrm{m_{aL1}}}} \tag{4.4.4}$$

The aL frequency range is also dictated by Z_{IN}, namely the self-resonant frequency and the zero, which are given by (4.5) and (4.6), respectively.

$$\omega_{\mathrm{o}} = \sqrt{\frac{g_{\mathrm{m_{aL1}}} g_{\mathrm{m_{aL2}}}}{C_{\mathrm{GS_{aL1}}} C_{\mathrm{GS_{aL2}}}}} \tag{4.5}$$

$$\omega_{\mathrm{z}} = \frac{g_{\mathrm{ds_{aL1}}}}{C_{\mathrm{GS_{aL2}}}} \tag{4.6}$$

Considering R_p and R_s in (4.4), it is possible to conclude that R_p is much greater than R_s, so the Q-factor in (2.13) becomes (4.7).

$$Q_3 \approx \frac{R_{\mathrm{p}}}{\omega L_{\mathrm{eq}}} = \frac{g_{\mathrm{m_{aL2}}}}{\omega C_{\mathrm{GS_{aL2}}}} \tag{4.7}$$

4.1.2 Cross-couple pair

The XCP role is to compensate losses of the frequency-determining circuit, through the generation of negative conductance/resistance (*-G* /*-R*) [16]. Without XCP, the oscillation decays exponentially, therefore XCP allows oscillation sustainability [16]. M_1 gate is connected to M_2 drain and vice-versa, thus the naming "cross-couple pair". In this section, the XCP is analyzed.

Initially, the XCP impedance is analyzed considering an ideal transistor, being the small-signal only represented as a simple voltage-dependent current source, without considering g_{ds} and the parasitic capacitors [16]. This representation is shown in Figure 7.

I_A is described in (4.8). The subscript 1 and 2 are related to transistors 1 and 2, respectively. The XCP is a symmetric circuit, which means that the dimensions of the transistors and bias conditions are equal. This implies that the g_ms are equal, and consequently, from (4.8) is possible to infer (4.9). V_A is given by (4.10), and combining it with (4.9), V_A is shortened to (4.11).

$$I_A = g_{m_1} V_2 = -g_{m_2} V_1 \tag{4.8}$$

$$V_1 = -V_2 \tag{4.9}$$

$$V_A = V_1 - V_2 \tag{4.10}$$

$$V_A = 2V_2 = -2V_1 \tag{4.11}$$

The output admittance of the ideal XCP, Y_A, is given by (4.12).

$$Y_A = \frac{I_A}{V_A} = \frac{g_m V_1}{-2V_1} = -\frac{g_m}{2} \tag{4.12}$$

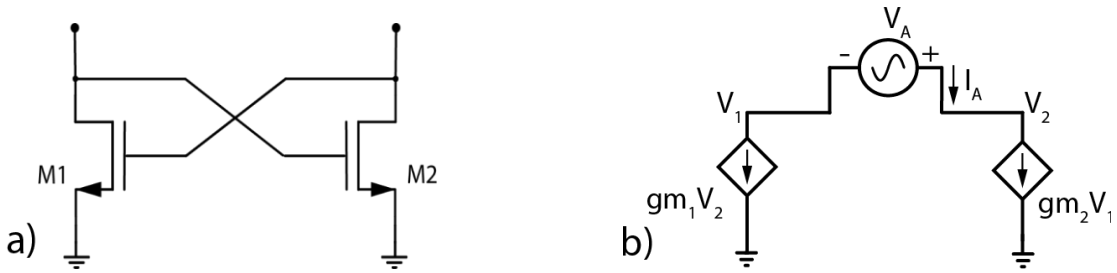

Figure 7 - Ideal ross-couple pair: a) schematic; b) small-signal equivalent.

Now considering the capacitances and g_{ds}, XCP is presented in Figure 8 a). The capacitors C_{GD1} and C_{GD2} are in parallel, connected between V_1 and V_2. However, the capacitors C_{GD1} and C_{GD2} are not in parallel with C_{GS1} and C_{DB2}. Nevertheless, C_{GD1} and C_{GD2} can be rearranged to be connected to the ground, using Miller's theorem, resulting in total XCP parasitic capacitance (C_{XCP}) [16]. With this reorganization, all the capacitors are in parallel, resulting in (4.13), as shown in Figure 8 b). (4.13) is shortened to (4.14), due to the symmetry of the circuit.

$$C_{XCP} = 2\left(C_{GD_1} + C_{GD_2}\right) + C_{GS_1} + C_{DB_2} \tag{4.13}$$

$$C_{XCP} = 4\, C_{GD_{1,2}} + C_{GS_{1,2}} + C_{DB_{1,2}} \tag{4.14}$$

The KCL is applied to the XCP EC presented in Figure 8 c), I_A is given by (4.15). The subscripts 1 and 2 correspond to transistors M_1 and M_2, respectively.

$$I_A = g_{ds_1}(-V_1) - g_{m_1} V_2 + sC_{XCP}(-V_1) \tag{4.15}$$

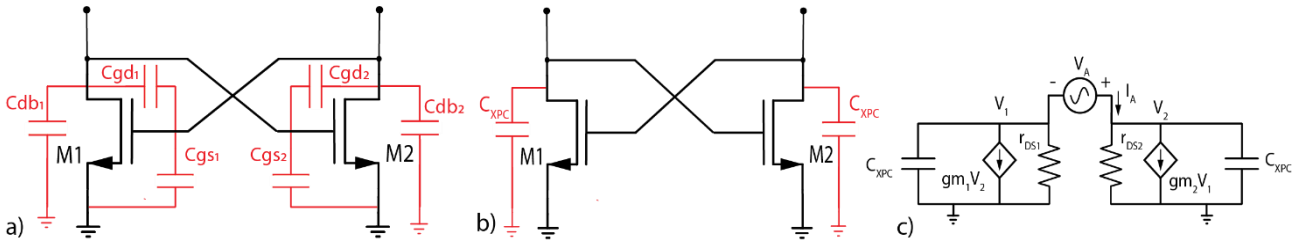

Figure 8 - Non-ideal cross-couple pair: a) schematic with the parasitic capacitances; b) schematic with parasitic capacitance rearranged using the Miller's theorem; c) small-signal equivalent of b).

V_A is given by (4.11), so combining it with (4.15), the non-ideal XCP admittance is presented in (4.16).

$$Y_A = -\frac{g_{\mathrm{m}} - g_{\mathrm{ds}}}{2} + \frac{sC_{\mathrm{XCP}}}{2} \tag{4.16}$$

4.1.3 Oscillations conditions

For the circuit to oscillate, it must fulfill the oscillation conditions previously described in section 2.3.1. So, it is possible to apply these conditions to the LC-oscillator with aLs. Therefore, to start oscillation, the negative conductance of XCP (G_{XCP}) must cancel the aL conductance (G_{F}). This condition is given by (4.17) [16].

$$-\frac{g_{\mathrm{m}} - g_{\mathrm{ds}}}{2} + \frac{G_{\mathrm{F}}}{2} < 0 \Rightarrow \frac{(g_{\mathrm{m}} - g_{\mathrm{ds}})}{G_{\mathrm{F}}} > 1 \tag{4.17}$$

4.1.4 Active inductor applied into LC-oscillator

The aL is integrated with the XCP to produce oscillation, as aforementioned. When integrated, the aL changes its impedance across the frequency due to the impedance associated with XCP. Consequently, the oscillation frequency of the LC-oscillator is lowered, because of the parasitic capacitance of the XCP at the output node. The most relevant parameter affected is C_{p}, where the total output capacitance ($C_{\mathrm{OUT_T}}$) is given by (4.18). Therefore, (4.1) becomes (4.19) – theoretical f_{OSC} of aL-based LC-oscillator ($f_{\mathrm{OSC_{aL}}}$).

$$C_{\mathrm{OUT_T}} = C_{\mathrm{p}} + C_{\mathrm{XCP}} \tag{4.18}$$

$$f_{\mathrm{OSC_{aL}}} = \frac{1}{2\pi\sqrt{C_{\mathrm{OUT_T}} L_{\mathrm{eq}}}} \tag{4.19}$$

4.2 MOS TECHNOLOGY DESIGN AND SIMULATIONS

4.2.1 aL-based LC-oscillator design and simulation

The LC-oscillator was designed following section 3.1. The XCP and three aLs with different transistors dimensions, number of fingers (NoF), and bias conditions were implemented. Variables are presented in Table 2. In these cases, oscillation conditions were verified. During this work, the MOS L_{CH} is 1 µm and the power supply voltage (V_{DD}) is 5 V. It is important to notice that the simulated transistors feature a thick gate dielectric, otherwise, the devices would reach breakdown for this V_{DD}. The choice of this L_{CH} was to achieve results more comparable to oxide TFT technology.

Table 2 - Transistor width (W), number of fingers (NoF) and bias currents (J) for each MOS oscillator. V_{DD} is 5 V and L_{CH} is 1 µm for MOS technology.

OSCILLATOR	**1**	**2**	**3**
$W_{1,2}$ **[NoF] (µm)**	25 [20]	25 [20]	25 [20]
W_{aL1} **[NoF] (µm)**	5 [1]	5 [1]	10 [1]
W_{aL2} **[NoF] (µm)**	12 [1]	24 [1]	12 [1]
J_1 **(µA)**	100	100	500
J_2 **(mA)**	1.5	1.5	0.5

The MOS oscillator was simulated with the different aLs, according to the procedure described in section 3.2.1.1. A DC analysis ensured that all transistors were in the saturation region. A transient analysis was performed, and the results are presented in Figure 9. The power consumption, simulated f_{OSC} ($f_{\mathrm{OSC_S}}$), and V_{pp} are shown in Table 3, where V_{pp} is given by (4.20), being $Max(V_{\mathrm{OUT}})$ and $Min(V_{\mathrm{OUT}})$ the maximum and minimum of V_{OUT}, respectively. All these simulations were carried out at 27 ºC – room temperature.

$$V_{\mathrm{pp}} = Max(V_{\mathrm{OUT}}) - Min(V_{\mathrm{OUT}}) \tag{4.20}$$

The bias conditions directly affect the power consumption. The power consumption of oscillators was reduced when the bias currents also decreased, as it is possible to observe in Table 3 when comparing oscillators 1 and 2 with oscillator 3. Besides that, greater W/L_{CH} produces more I_{DS} in the saturation regime (same voltage conditions), which translates to higher power dissipation. Oscillators 1 and 2 are examples of this, since the transistor M_{aL2} of the first oscillator has twice the W of the second, resulting in power consumption increase.

The L_{eq} is given by (2.6.1), so an increase in the W/L_{CH} ratio of transistor M_{aL2} generates a decrease in the inductance value, since the g_{maL2} value increases more than the C_{GSaL2} value. Therefore, the f_{OSC} will increase. To prove this, the C_{GS}/g_m ratio was derived and is given by (4.21), where C_{OV} is the overlap capacitance [7], [21]. The M_{aL2}'s L_{CH} and C_{OX} are the same and V_{TH} is approximately equal in both situations. When M_{aL2}'s W is wider, the V_{DS} to ensure saturation is lower, because, being the drain voltage equal to V_{DD}, the source voltage is lower, consequently, V_{GS} is higher (gate voltage remains constant with the same bias conditions and same dimensions M_{aL1}), resulting in a smaller C_{GS}/g_m and, consequently, in a lower L_{eq}. The results can be observed comparing oscillators 1 and 2, where the W/L_{CH} of M_{aL2} of former was twice the one of the latter.

In the same way, increasing the W/L_{CH} ratio of M_{aL1} resulted in a lower L_{eq}, due to increase of g_{maL1}. Additionally, larger W will drop V_{DS} of transistor M_{aL1}, but, as source is connected to ground, so the drain voltage will decrease. As the M_{aL1} drain and M_{aL2} gate are connected, the V_{GS} of M_{aL2} also decreases, therefore, the C_{GS}/g_m M_{aL2} ratio declines, and L_{eq} is reduced. On the other hand, larger W/L_{CH} ratio of M_{aL1} also increases C_{GSaL1}, which impacts C_p and consequently, C_{OUTT}. As increase of g_m is more significant than C_{GS}, f_{OSC} increases. An example of this effect are oscillators 1 and 3, since the W of the former is half of the latter and, nevertheless, f_{OSCS} of the oscillator 3 is more than the double.

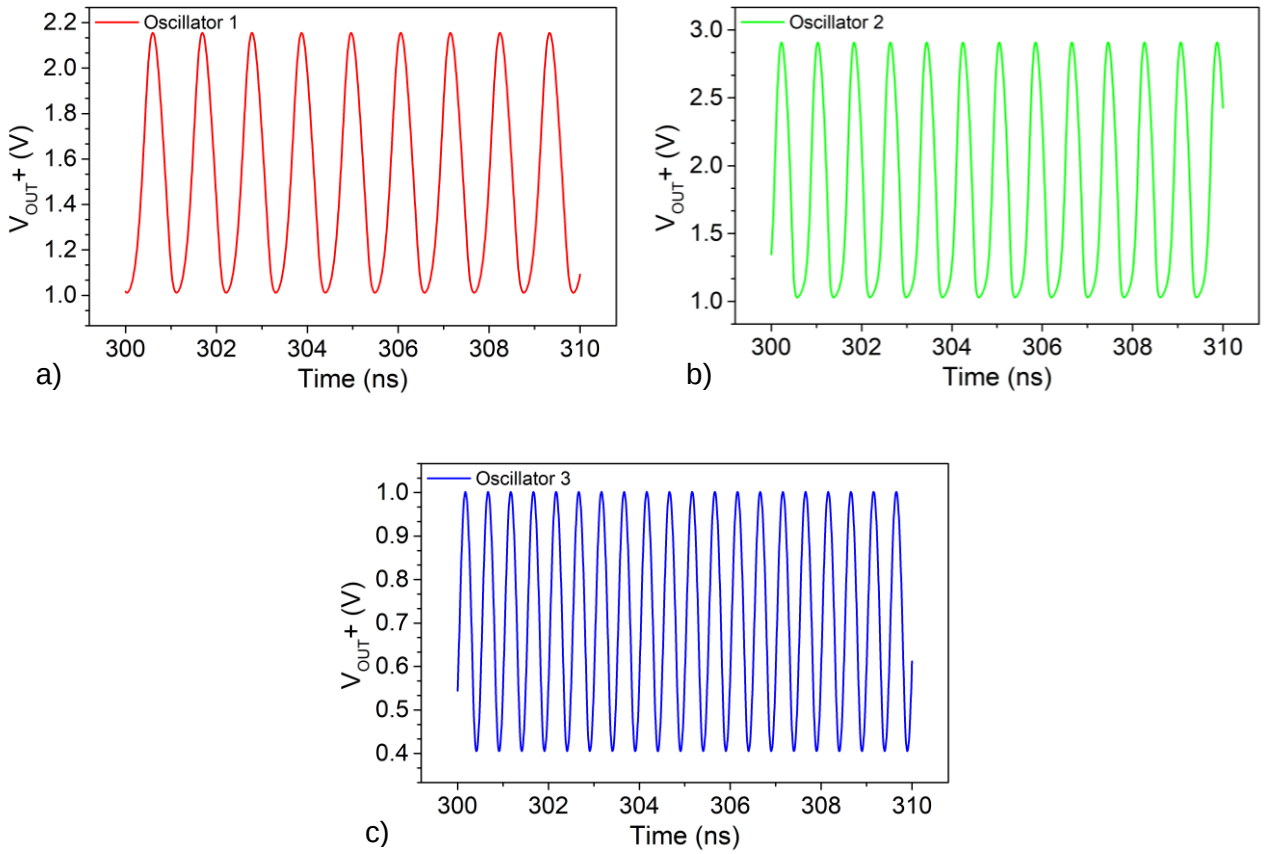

Figure 9 - V_{OUT}+ in function of time for each MOS oscillator: a) Oscillator 1; b) Oscillator 2; c) Oscillator 3.

$$\frac{C_{GS}}{g_m} = \frac{\frac{2}{3}WL_{CH}C_{OX} + WC_{OV}}{\frac{W}{L_{CH}}C_{OX}(V_{GS} - V_{TH})} \approx \frac{2L_{CH}^2 C_{OX}}{3(V_{GS} - V_{TH})} \quad (4.21)$$

At the output node, I_{DSaL2} is divided into J_1 and $I_{DS1,2}$. Since J_1 is an ideal and constant current source, so the $I_{DSaL2} - J_1$ results in $I_{DS1,2}$, which is the $I_{OUT1,2}$. Thus, a greater W/L_{CH} ratio of M_{aL2} increases $I_{DS2,}$ keeping the same J_1 value, and consequently, increases V_{pp}. On other hand, increasing J_1 produces a signal with a small V_{pp}, as it is possible to verify in oscillator 3 when compared with oscillator 1. It is noteworthy, that changing dimensions and/or bias conditions affect all characteristics at the same time, so a careful trade-off must be considered to optimize the aL to a given application.

Table 3 - Power consumption, f_{OSCS} and V_{pp} for each MOS oscillator.

OSCILLATOR	**1**	**2**	**3**
Power consumption (mW)	65.0	80.1	21.2
f_{OSCS} **(Hz)**	917.2 M	1.279 G	2.080 G
V_{pp} **(V)**	1.16	1.78	0.613

4.2.2 aL RLC equivalent circuit

To infer on the origins of the different oscillation patterns shown above, the aLs were substituted by their RLC EC (Figure 10). Only one branch of the circuit was considered. The parameters are calculated using (4.4) through LC-oscillator DC operations points, following the procedure of section 3.2.1.2. The f_{OSCaL} stated in (4.19) is used to confirm the f_{OSCS}. The component values are present in Table 4, as well as the f_{OSCaL} and the respective relative error.

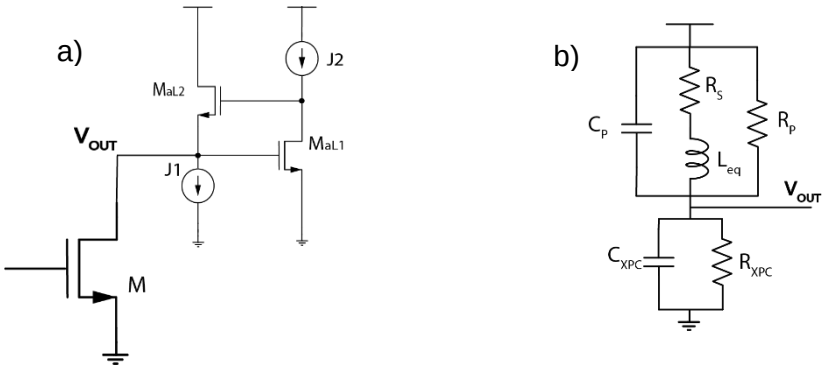

Figure 10 - One branch of the aL-based LC-oscillator: a) schematic; b) RLC equivalent circuit.

An S-parameters analysis was performed on the circuit present in Figure 10 b), namely regarding Z-parameters. The goal of this simulation was to observe the output impedance of the circuit across the frequency range and confirm the f_{OSCS} obtained in Table 3 and presented in Figure 11. The error is resulting from the approximation made in (4.4), just dominant terms were considered, so RLC components values present a difference to those that aL generates.

Table 4 confirms the expected conclusion about feature size and/or bias conditions were correct. Since L_{eq} decreases with higher W/L_{CH} ratio of M_{aL2}, visible in oscillator 1 and 2. The inductance also decreases with higher W/L_{CH} ratio of M_{aL1}, as it is possible to observe in oscillator 3. Analogously, C_p is also affected by the ratio of M_{aL1} since it raises the parasitic capacitance.

To measure the oscillators' temperature sensibility, a temperature sweep from -40 ºC until 85 ºC was performed as previously described. Figure 12 shows the power consumption, $f_{OSC,}$ and V_{pp} variations across the temperature sweep for all oscillators. The oscillators presented lower f_{OSC} when the temperature was higher.

f_{OSCaL} depends on equivalent inductance and total parasitic capacitance, as presented in (4.19): C_{OUTT} presented an almost linear dependency across temperature range as presented in Figure 13. Simultaneously, L_{eq} also increased with temperature. Therefore, as f_{OSC} is inversely proportional to the square root of the product between the output capacitances and inductance, it is possible to conclude that f_{OSCaL} is inversely proportional

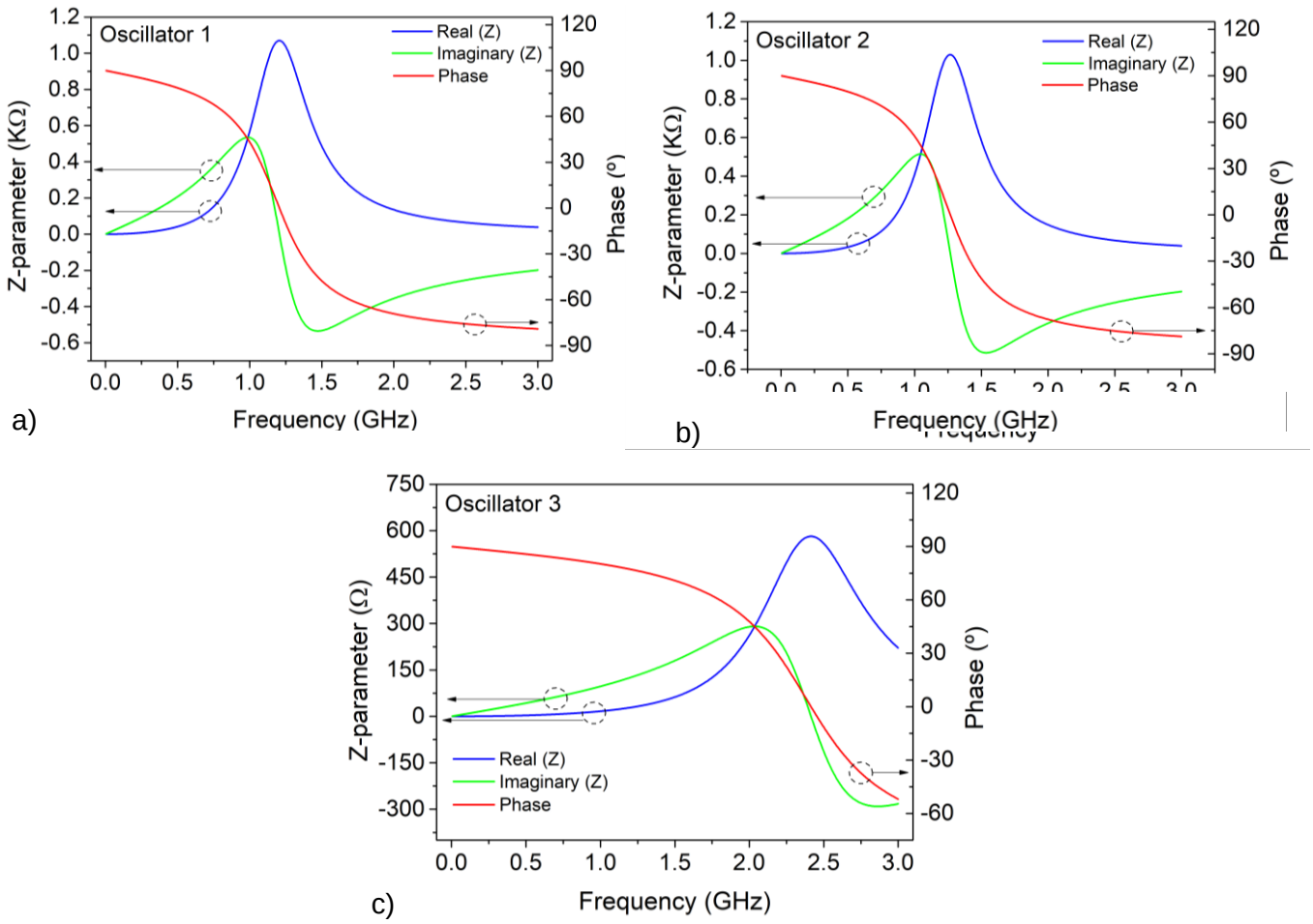

Figure 11 - Z-parameters and phase of the RLC equivalent circuit. Real(Z), Imaginary (Z) and phase measurement in function of the frequency: a) Oscillator 1; b) Oscillator 2; c) Oscillator 3.

to the temperature, as presented in Figure 13, in agreement with f_{OSCS}.

Table 4 - RLC equivalent components values, correspondent to Figure 10 b), respective f_{OSCaL} and relative error for each MOS oscillator.

OSCILLATOR	**1**	**2**	**3**
R_s **(Ω)**	387	79.0	5.14
R_p **(kΩ)**	1.07	1.07	0.607
L_{eq} **(nH)**	54.30	48.26	12.34
C_p **(fF)**	44.74	45.48	83.00
C_{XCP} **(fF)**	258.99	262.34	244.18
C_{OUTT} **(fF)**	303.73	307.82	327.18
R_{XCP} **(Ω)**	-399	-403	-545
f_{OSCaL} **(Hz)**	1.239 G	1.306 G	2.505 G
Relative error ($\lvert f_{OSCaL} - f_{OSCS}\rvert / f_{OSCaL}$)	0.27	0.025	0.17

4.2.3 Temperature sensibility analysis

The oscillators' power consumption did not present significant variations across the temperature range, especially the oscillator 3. For a temperature of −40 ºC, the oscillators 1 and 2 dissipated around 6.3 % and 3.2 % more power than at 27 ºC and at 85 ºC both oscillators dissipated around 2.5 % less. The oscillator 3 power consumption variation was less than 1.3 % in entire temperature range.

The decrease power consumption with temperature can be explained by the decrease of the mobility with the temperature increase [22], which, consequently, decreases I_{DS}, as stated in (2.2) and (2.3). So, as power consumption is given by the product of voltage and current, and voltage is constant (and equal to V_{DD}) and current decreases, thus power consumption decreases.

The V_{pp} showed two types of tendencies: V_{pp} decreased when temperature increased, which is visible in oscillators 1 and 3; and the opposite tendency was found in oscillator 2 – the increase of V_{pp} with temperature decrease. Ultimately, V_{pp} is given by (4.22), combining (4.2) and (4.20).

$$Max(\mathrm{V_{OUT^{+,-}}}) - Min(V_{\mathrm{OUT^{+,-}}}) = \left(Max\left(r_{\mathrm{ON}_{1,2}}\right) \cdot Min\left(I_{\mathrm{OUT}_{1,2}}\right) - Min\left(r_{\mathrm{ON}_{1,2}}\right) \cdot Max\left(I_{\mathrm{OUT}_{1,2}}\right)\right) \quad (4.22)$$

To confirm the results obtained in Figure 12 c), r_{ON2} and I_{OUT2} were simulated and extracted. The maximum and the minimum of these variables were used to calculate V_{pp} through (4.21) for each one of the three oscillators. The results were plotted into a temperature sweep, as shown in Figure 14. Peak-to-peak variation of I_{OUT2} decreases with temperature, as expected due to lower mobility of the semiconductor, for all oscillators. Peak-to-peak r_{ON2} of oscillators 1 and 3 decreases with the temperature increase, so as both values decrease the V_{pp} also decreases, as it is possible to observe in Figure 12 c) and Figure 14 a) and c). However,

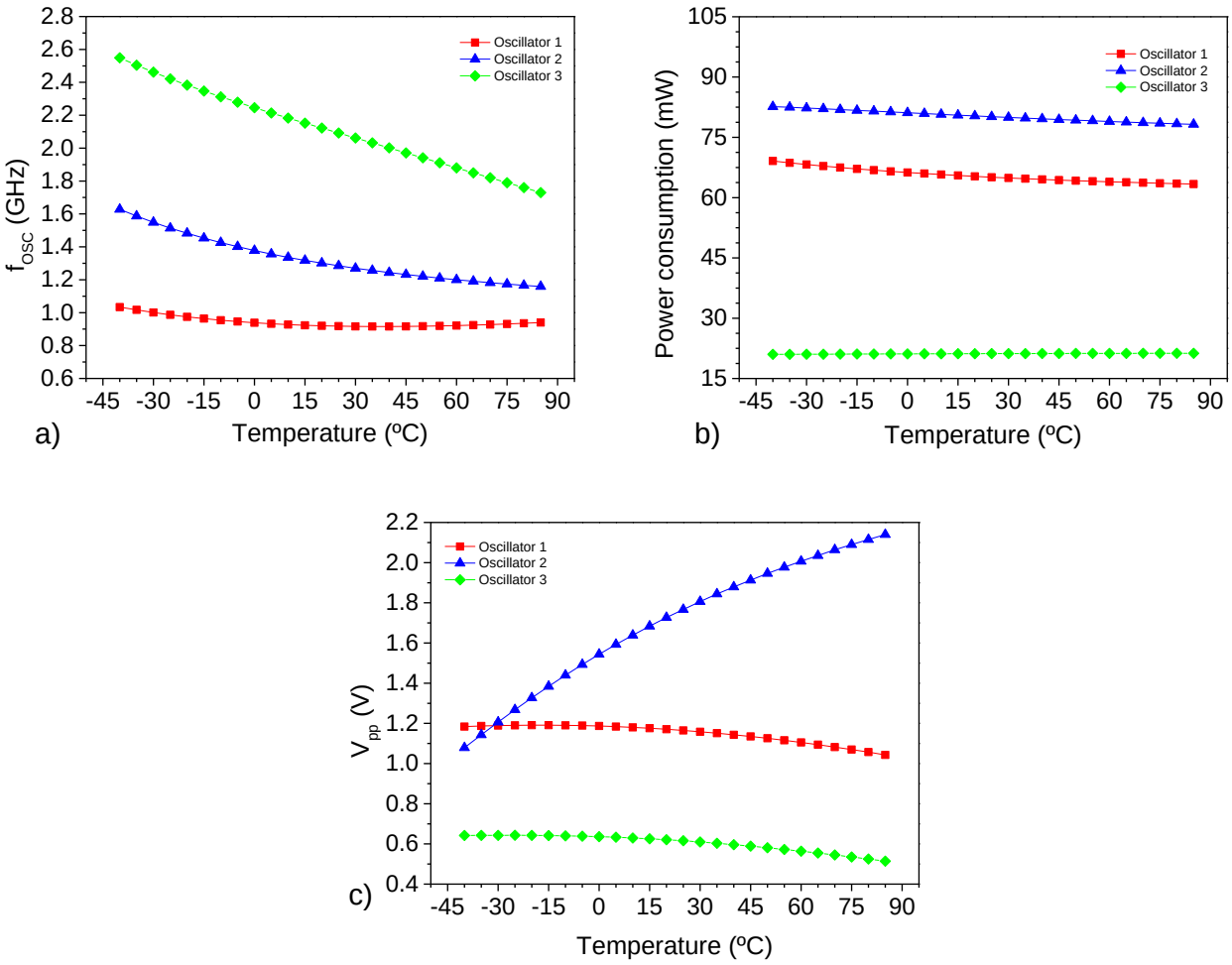

Figure 12 - Temperature sensibility for each MOS oscillator. a) oscillation frequency; b) power consumption; c) output peak-to-peak voltage.

peak-to-peak r_{ON_2} of oscillator 2 increases with temperature increase, which translates to an increase of V_{pp} with temperature. The r_{ON} of transitor M_2 is affected by the transistor M_{aL2}. This latter transistor presents a wider W in oscillator 2, when comparing the same transistor in oscillators 1 and 3. This behavioral difference is associated with the model/sub model utilized in the simulation (BSIM3v3), since the equations are W and L_{CH} dependent [23].

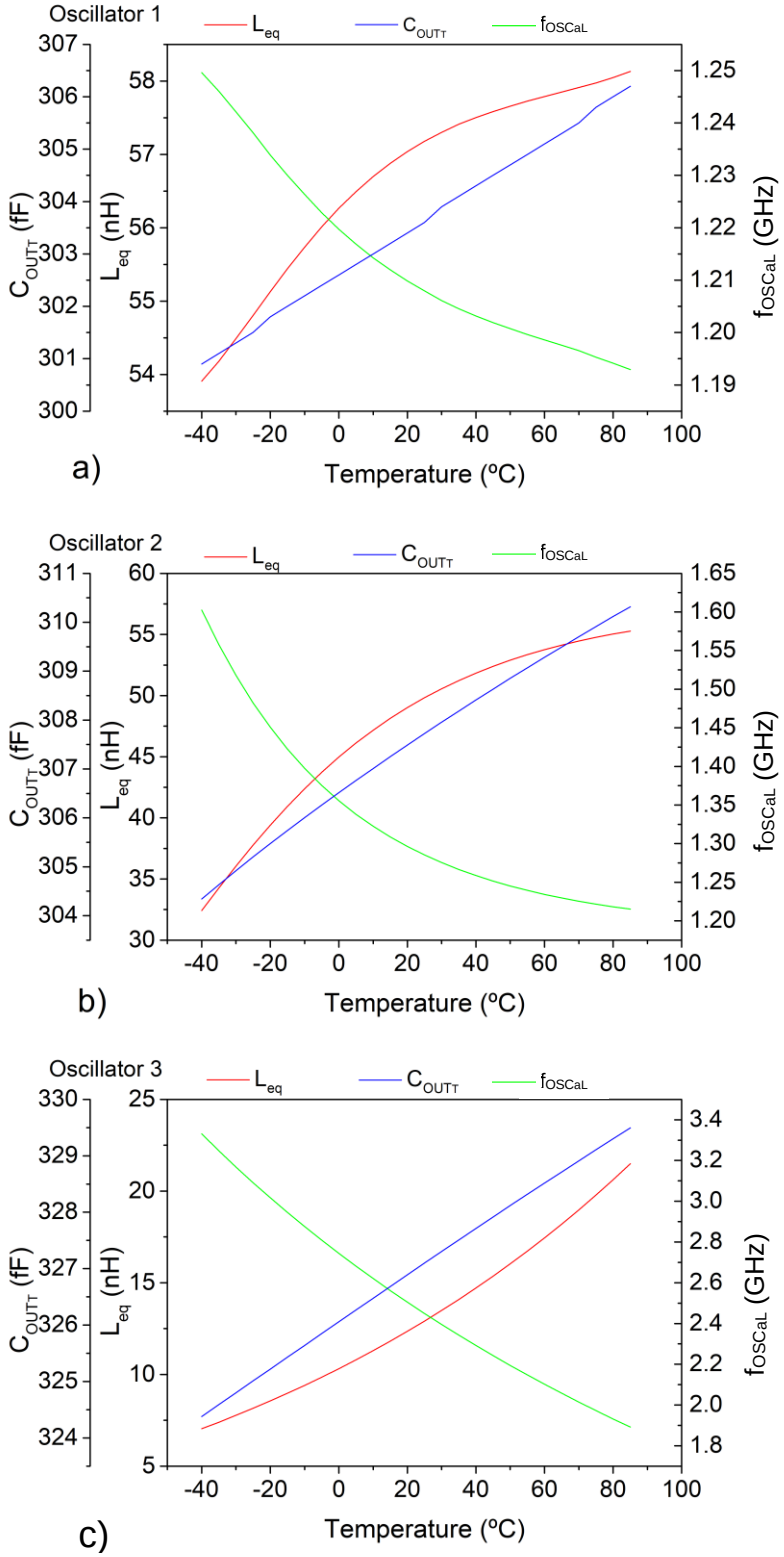

Figure 13 - C_{OUTT}, L_{eq} and f_{OSCaL} versus of temperature, being blue, red, and green lines, respectively: a) Oscillator 1; b) Oscillator 2; c) Oscillator 3.

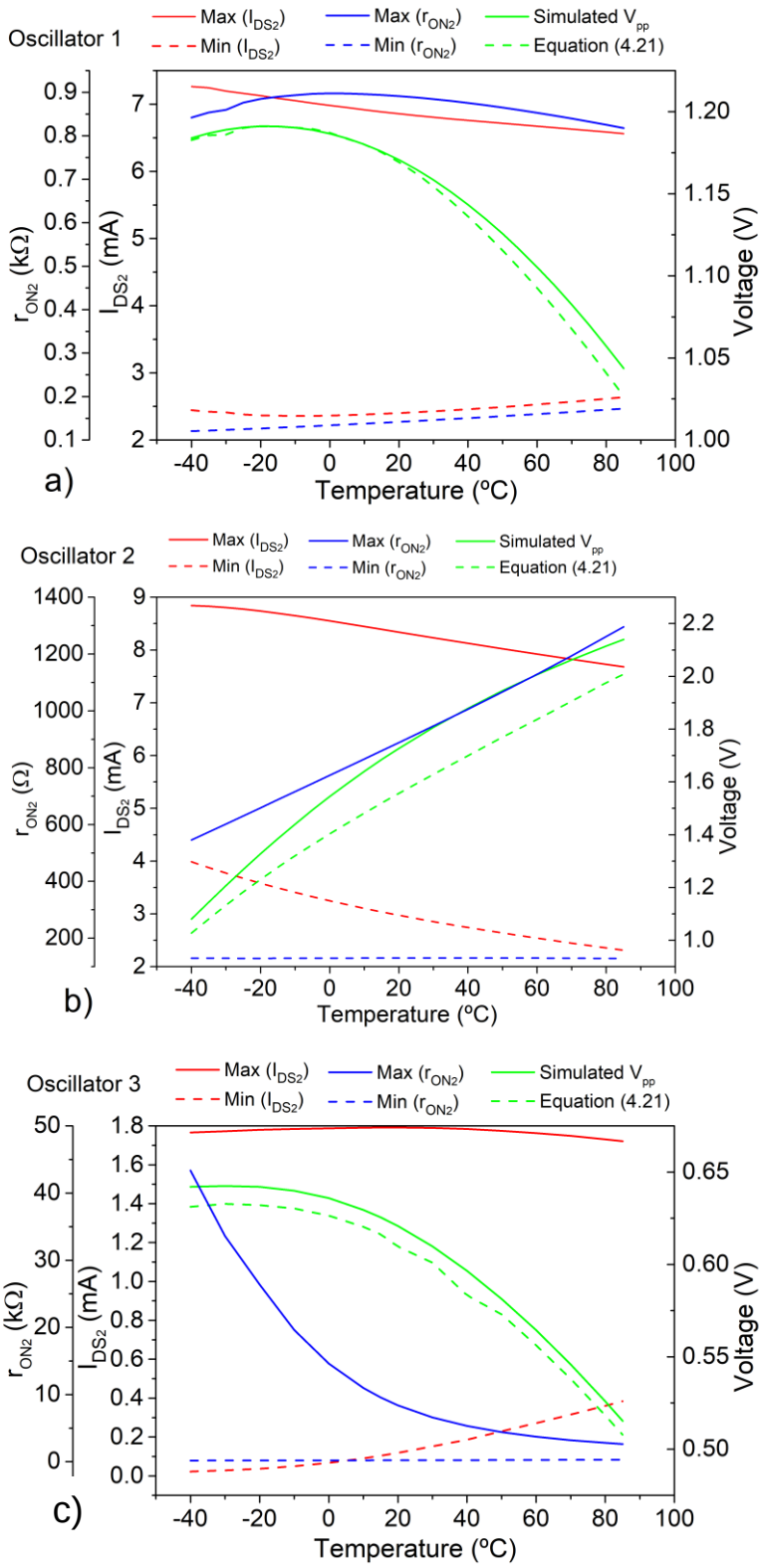

Figure 14 - Maximum and minimum of I_{DS2} (red curve) and r_{ON2} (blue curve) in function of temperature, being the maximum the solid line and minimum the dash line. V_{pp} obtained by (4.21) – dash green line – and the simulated V_{pp} in function of temperature – solid green line. a) Oscillator 1; b) Oscillator 2; c) Oscillator 3.

4.2.4 Phase noise simulation

Next, a phase noise analysis was performed following the procedure described in section 3.2.1.1. The phase noise is a fundamental design specification for oscillators in RF applications. Phase noise quantifies the spread of the oscillator signal power to nearby frequencies [24]. It is measured at the power of the 1-Hz bandwidth of the spectrum at a given offset. The power is normalized by the carrier power. Phase noise is usually indicated in dBc/Hz at a given offset from the oscillator fundamental frequency or its harmonics[16].

The phase noises at 1 MHz offset from the fundamental frequency for each oscillator are presented in Figure 15 and the results are presented Table 5. The phase noise is inversely proportional to the Q-factor of inductive elements [16], [25]. Oscillator 2 presented the lowest phase noise, however, the Q-factors at f_{OSCS} – (4.7) – of Table 5 do not corroborate with these results, which could be a direct consequence of the larger error of RLC EC values of oscillators 1 and 3, allowing to conclude that Q-factors are lower than estimated. Nevertheless, it is not possible to affirm with certain, so, further study is necessary to fully understand these different behaviors.

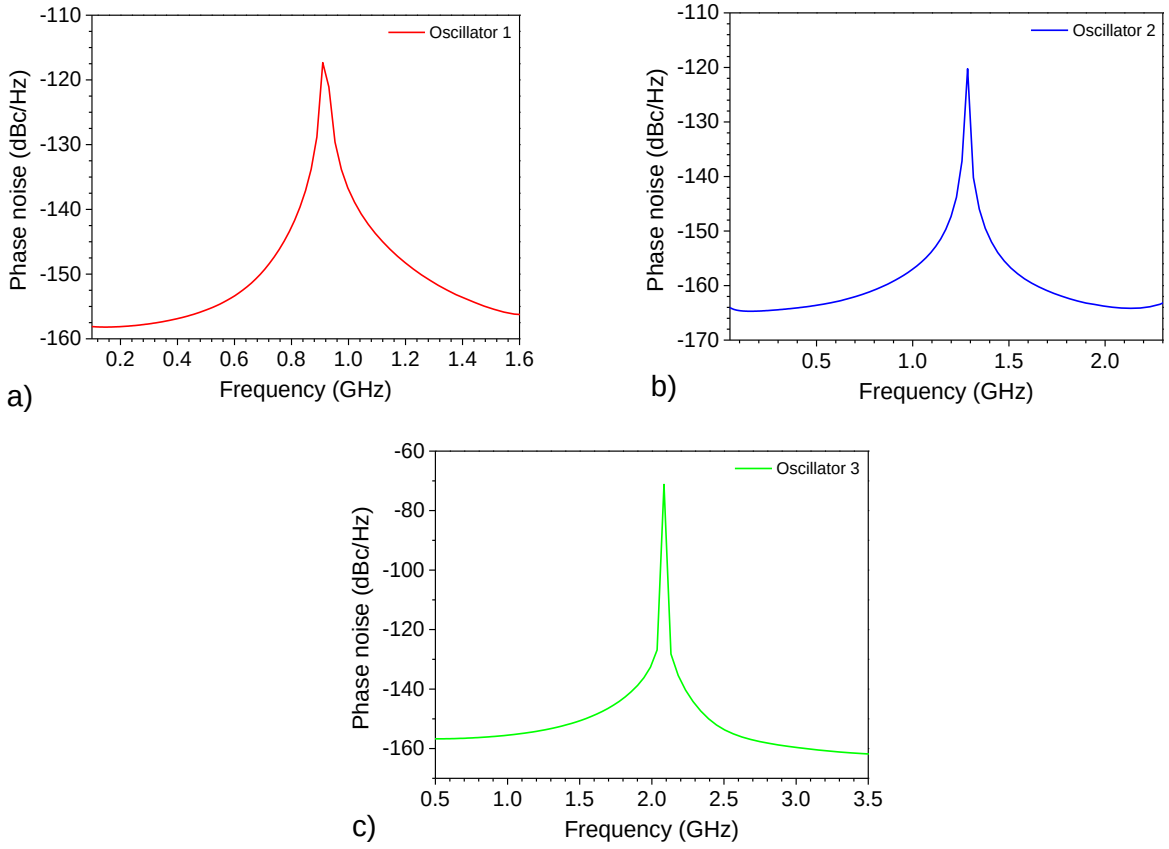

Figure 15 - Phase noise at 1 MHz offset from the fundamental frequency for each MOS oscillator: a) Oscillator 1; Oscillator 2; c) Oscillator 3.

Table 5 - Phase noise at 1 MHz of offset for each MOS oscillator, and respective Q-factor at f_{OSCS}.

Oscillator	**1**	**2**	**3**
Phase noise @ 1 MHz offset (dBc/Hz)	-96.73	-104.7	-92.86
Q-factor @ f_{OSCS}	3.43	2.70	3.77

4.3 OXIDE TFT TECHNOLOGY SIMULATION AND DESIGN

4.3.1 aL-based LC-oscillator design and simulation

The aL-based LC-oscillator was implemented using a-IGZO TFTs, as described in section 3.1. The XCP, the aLs transistors dimensions, and bias conditions are presented in Table 6. The oscillation conditions were verified under these.

The LC-oscillators using oxide TFTs were simulated following section 3.2.2.1. A DC analysis was performed to ensure that the transistors are set in the saturation region, as well as to infer about power consumption. A transient analysis was performed to observe the oscillation parameters. V_{pp} and f_{OSC} can be observed in Figure 16. The simulation results are summarized in Table 7.

Table 6 - Transistor width (W), number of fingers (NoF) and bias currents (J) for each oxide TFT oscillator.

OSCILLATOR	**1**	**2**	**3**	**4**
V_{DD} **(V)**	10	10	10	10
L_{CH} **(µm)**	20	10	10	10
$W_{1,2}$ **(µm)**	640	160	80	80
W_{aL1} **(µm)**	240	40	40	40
W_{aL2} **(µm)**	480	80	80	40
J_1 **(µA)**	8	3	3	4
J_2 **(µA)**	15	5	5	7

As in the case of MOS technology, larger bias conditions as well as larger transistors translate to higher power consumption, as it is evident with oscillator 1. The feature size of XCP transistors affect f_{OSC}. Comparing oscillators 2 and 3, the $W_{1,2}$ of XCP is the double and, consequently, the f_{OSC} is almost the half, due to smaller C_{XCP}. However, this comes at the cost of smaller V_{pp} value, since V_{pp} is directly proportional to $I_{DS1,2}$ and larger sizes imply large currents in the drain. As previously mentioned, the W of M_{aL2} has a high impact on L_{eq} value and, consequently, in f_{OSC}. Therefore, greater W/L_{CH} ratio of M_{aL2} implies a lower f_{OSC} as observable in oscillators 3 and 4, since the L_{eq} is larger in the first case.

Table 7 - Power consumption, f_{OSCS} and V_{pp} for each oxide TFT oscillator.

OSCILLATOR	**1**	**2**	**3**	**4**
Power consumption (µW)	1255	756.2	375.6	532.6
f_{OSCS} **(Hz)**	307.9 K	556.2 K	938.3 K	1.218 M
V_{pp} **(V)**	3.26	4.67	2.60	3.83

4.3.2 aL RLC equivalent circuit

Analogously to MOS technology, the RLC EC parameters were calculated, using (4.4). It is important to note that C_{DB} is inexistent. The values parameters are presented in Table 8. The obtained results correspond to the expected since oscillator 1 presented the larger L_{eq} due to wider M_{aL2}, oscillator 2 presented the highest V_{pp} because of larger $M_{1,2}$ and oscillator 4 presented the largest f_{OSCS} due to smaller inductor value, which is a direct consequence of smaller M_{aL2} size.

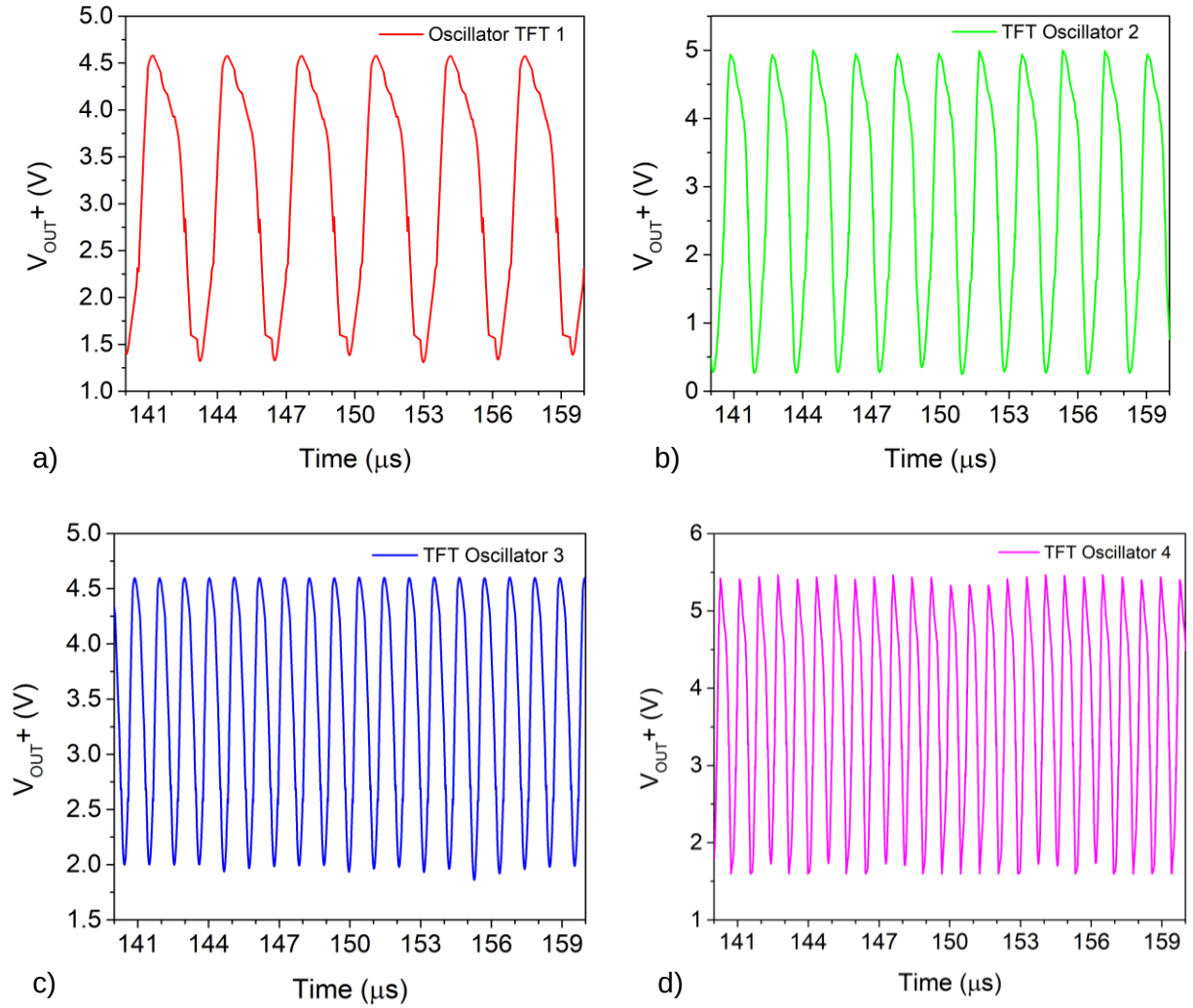

Figure 16 - V_{OUT}+ in function of time for each oxide TFT oscillator: a) Oscillator 1; b) Oscillator 2; c) Oscillator 3; d) Oscillator 4

Table 8 - RLC equivalent components values, correspondent to Figure 10 b), respective f_{OSCaL} and relative error for each oxide TFT oscillator.

OSCILLATOR	**1**	**2**	**3**	**4**
R_s **(Ω)**	45	158	131	40
R_p **(kΩ)**	1.52	2.76	2.76	3.10
L_{eq} **(µH)**	15.10	8.88	3.27	0.76
C_p **(fF)**	1464	164	164	164
C_{XCP} **(pF)**	9.28	2.00	1.00	1.00
C_{OUTT} **(pF)**	10.74	2.16	1.16	1.16
R_{XCP} **(kΩ)**	-3.43	-4.49	-3.23	-3.10
f_{OSCaL} **(Hz)**	17.6 M	36.3 M	81.6 M	169 M
Relative error ($\lvert f_{OSCaL} - f_{OSCS}\rvert / f_{OSCaL}$)	0.98	0.98	0.99	0.99

The results presented a high error, probably, due to convergence problems of transient simulation, since the model is based in an ANN that was implemented using a Verilog-A file. Convergence aids to the initial conditions were used to minimize the problem.

5 CONCLUSION AND FUTURE PERSPECTIVES

The focus of this work was to implement LC oscillator circuits using aLs, based on the oxide TFT technology. The aL goal is to emulate inductive behavior. Additionally, aLs presented several advantages when compared with its passive counterpart, such as small die area, large and tunable oscillation frequency and inductance [8].

A simple grounded aL was employed due its simplicity and for being constituted by n-type transistors, since oxide TFTs do not present a good p-type semiconductor. Consequently, it is not possible to apply CMOS design techniques to this technology yet. This aL was applied to a cross-couple LC-oscillator.

Initially, the aL-based LC-oscillator was designed and simulated using 130 nm MOS technology, as proof-of-concept, since this technology presents a more developed and precise model. Different dimensions and bias conditions were tested to gather a better understanding of its behavior. The RLC EC was calculated to obtain the same values of inductance and capacitance at output node as its correspondent aL.

The MOS-based LC oscillator presented an f_{OSC} from 917 MHz to 2 GHz with a maximum power consumption of 80 mW. The V_{pp} voltage was between 613 mV and 1.80 V with a V_{DD} of 5V. The MOS oscillators presented a relatively good phase noise, being in maximum - 92.56 dBc/Hz at an offset of 1 MHz.

The LC oscillator using L_{CH} = 10 µm a-IGZO TFTs presented an f_{OSC} between 556 kHz and 1.21 MHz and a V_{pp} from 2.6 V to 4.67 V with a power supply of 10 V. Using a-IGZO TFTs with L_{CH} = 20 µm, LC oscillator presented an f_{OSC} of 308 kHz with a 3.26 V of V_{pp} using the same V_{DD}.

As expected, the LC-oscillators using a-IGZO present a lower f_{OSC}, greater parasitic capacitances, and channel lengths when compared with MOS LC-oscillators. Regardless, the TFT model does not allow to perform the temperature sensibility simulations. Nevertheless, it is predictable that these produced the same behavior with temperature as their MOS counterparts. The phase noise is highly related to the Q-factor of inductive elements [16]. Not being possible to verify this parameter, nonetheless, the Q-factor of TFTs aLs should be lower since the ohmic losses increments are larger than the inductance values, which allows to conclude that phase noise in the TFT-based LC oscillator will be larger than the MOS counterpart.

As aforementioned, there are only a few reports on aLs based on oxide TFTs. In Table 9, the current state-of-the-art of oxide TFTs oscillator is presented. Accordingly, some works relate to either aLs-based LC-oscillators, passive inductor-based LC-oscillators, and ring oscillators (RO). As verified, the present work is very well aligned with the state of the art, presenting the best figure of merit (FoM) among the LC-oscillators using oxide TFTs. This FoM quantifies the most important metrics of an oscillator, such as f_{OSC}, V_{pp} and power consumption [26]. Although it was not possible to produce the layout of the oxide TFT aL-based LC-oscillator, comparing the total number of transistors and their size, it is also reasonable to state that this work allows the integration of an oscillator in a smaller area. Additionally, this work is the only one that permits f_{OSC} tunability.

The future objectives of this work should encompass the production and characterization of the a-IGZO TFT aL-based LC-oscillator. It is relevant to notice that LC-oscillator was simulated without load impedance, so the large impedance of measurement equipment could modify the results, lowering f_{OSC}. Thus, an on-chip buffer must be used to allow for better results [5].

The aL applied is a simple configuration, with relatively limited Q-factor, and inductance and ω_o tunability. There are different and more complex aL configurations that allow to upgrade these parameters, even using only n-type transistors, such as simple cascode aL [20], or the cascode aL with resistive feedback [25]. The former presents a better Q-factor since the losses are reduced by the cascode transistor. The latter offers inductance tunability, which allows f_{OSC} tunability. Besides that, different oscillator topologies can be implemented [16].

f_{OSC} can be improved by using transistors with low parasitic capacitances, enabling the design of high-frequency oscillators. While the TFT models used for this work considered very conservative design rules, with gate-to-drain and gate-to-source overlaps of 5 µm, there is room for decreasing parasitic capacitances. The cut-off frequency of transistors is ultimately the limiting factor for high-frequency oscillator circuits. Since this frequency is inversely proportional to $L_{CH,}$ working towards oscillator circuits with smaller technology nodes would allow for higher f_{OSC} [6], [7]. The ongoing work at CENIMAT on miniaturized self-aligned oxide TFTs is precisely heading toward this enhancement of cut-off frequency and minimization of parasitic capacitances.

Table 9 - State-of-the-art of oscillators using AOS-based TFTs. BG – Bottom gate; RO – ring oscillator; SA – Self-aligned; P_{con} – Power consumption. *Estimated from the reports. **Values presented in µm.

Semicon-ductor	**Ref.**	**Topology**	V_{DD} **(V)**	f_{OSC} **(Hz)**	V_{pp} **(V)**	***Largest*** W/L_{CH}**** **(Total no. of transistors)**	f_{OSC} **tuna-bility**	**Device's structure**	**Power consu-mption (mW)**	**FoM =** $\frac{f_{OSC} \cdot V_{pp}}{P_{con}}$ [26]
a-IGZO	**This work**	**aL LC-oscillator**	**10**	**1.21 M**	**3.83**	**80/10 (6)**	**Yes**	**BG and non-SA**	**0.533**	**$8.69 \cdot 10^9$ C^{-1}**
a-IGZO	[1]	aL LC-oscillator	5 0.5	5 109	2.8* 0.11*	240/12 (10)	No	BG and non-SA	0.002 0.188	$7.00 \cdot 10^6$ C^{-1} $63.8 \cdot 10^3$ C^{-1}
ZnO	[2]	Inductor LC-oscillator	7	35.3 M	4	500/5 (2) + 2 passive inductors	No	BG and non-SA	56	$2.52 \cdot 10^9$ C^{-1}
a-IGZO	[6]	3-stage RO	3	3.39 M	0.65*	200/2 (3)	No	BG and non-SA	-	-
a-IGZO	[7]	9-stage RO	9	305 k	6.57	40/10 (18)	No	BG and non-SA	-	-

REFERENCES

[1] T. Meister *et al.*, "5–31-Hz 188-µW Light-Sensing Oscillator With Two Active Inductors Fully Integrated on Plastic," *IEEE J. Solid-State Circuits*, vol. 54, no. 8, pp. 2195–2206, Aug. 2019, doi: 10.1109/JSSC.2019.2914405.

[2] E. Fortunato, P. Barquinha, and R. Martins, "Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances," *Adv. Mater.*, vol. 24, no. 22, pp. 2945–2986, Jun. 2012, doi: 10.1002/adma.201103228.

[3] P. Bahubalindrun, V. Tavares, P. Barquinha, P. G. de Oliveira, R. Martins, and E. Fortunato, "InGaZnO TFT behavioral model for IC design," *Analog Integr. Circuits Signal Process.*, vol. 87, no. 1, pp. 73–80, Apr. 2016, doi: 10.1007/s10470-016-0706-4.

[4] K. Ishida *et al.*, "3-5 V, 3-3.8 MHz OOK modulator with a-IGZO TFTs for flexible wireless transmitter," *2017 IEEE Int. Conf. Microwaves, Antennas, Commun. Electron. Syst. COMCAS 2017*, vol. 2017-November, pp. 1–4, Jun. 2017, doi: 10.1109/COMCAS.2017.8244748.

[5] B. Tiwari *et al.*, "Low-Voltage High-Speed Ring Oscillator with a-InGaZnO TFTs," *IEEE J. Electron Devices Soc.*, vol. 8, no. May, pp. 584–588, 2020, doi: 10.1109/JEDS.2020.2997101.

[6] Y. Afsar *et al.*, "18-2: Oxide TFT LC Oscillators on Glass and Plastic for Wireless Functions in Large-Area Flexible Electronic Systems," *SID Symp. Dig. Tech. Pap.*, vol. 47, no. 1, pp. 207–210, May 2016, doi: 10.1002/SDTP.10638.

[7] G. Cantarella *et al.*, "Review of recent trends in flexible metal oxide thin-film transistors for analog applications," *Flex. Print. Electron.*, vol. 5, no. 3, p. 033001, Sep. 2020, doi: 10.1088/2058-8585/aba79a.

[8] F. Yuan, *CMOS Active Inductors and Transformers*. Boston, MA: Springer US, 2008.

[9] D. Pinkesh Patel, "CMOS Active Inductor and Its Applications," in *Applied Electromechanical Devices and Machines for Electric Mobility Solutions*, vol. i, no. tourism, IntechOpen, 2020, p. 13.

[10] M. Ismail, R. Wassenaar, and W. Morrison, "A high-speed continuous-time bandpass VHF filter in MOS technology," in *1991., IEEE International Sympoisum on Circuits and Systems*, 1991, vol. 3, pp. 1761–1764, doi: 10.1109/ISCAS.1991.176249.

[11] N. M. Nguyen and R. G. Meyer, "Start-up and Frequency Stability in High-Frequency Oscillators," *IEEE J. Solid-State Circuits*, vol. 27, no. 5, 1992.

[12] P. Barquinha, "Transparent Oxide Thin-Film Transistors : production, characterization and integration," Universidade Nova de Lisboa, 2010.

[13] I. Bahl, *Lumped Elements for RF and Microwave Circuits*. ARTECH HOUSE, INC., 2003.

[14] T. F. Schubert and E. M. Kim, "Fundamentals of Electronics: Book 4 Oscillators and Advanced Electronics Topics," *Synth. Lect. Digit. Circuits Syst.*, vol. 11, no. 2, pp. 1–266, Apr. 2016, doi: 10.2200/S00715ED1V04Y201604DCS050.

[15] J. van der Tang, D. Kasperkovitz, and A. van Roermund, *High-Frequency Oscillator Design for Integrated Transceivers*, 1st ed., vol. 748. Boston: Kluwer Academic Publishers, 2005.

[16] B. Razavi, *RF Microelectronics (2nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series)*, 2nd ed. USA: Prentice Hall Press, 2011.

[17] "Temperature Ranges | Renesas." Accessed: Dec. 13, 2021. [Online]. Available: https://www.renesas.com/us/en/support/technical-resources/temperature-ranges.

[18] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, 1999, doi: 10.1109/4.760384.

[19] A. Ben Hammadi, M. Mhiri, F. Haddad, S. Saad, and K. Besbes, "Study of wide adjustable active inductor circuits: Design approaches and reconfiguration methods," in *2017 International Conference on Engineering & MIS (ICEMIS)*, May 2017, vol. 2018-Janua, pp. 1–6, doi: 10.1109/ICEMIS.2017.8273063.

[20] A. Thanachayanont and A. Payne, "VHF CMOS integrated active inductor," *Electron. Lett.*, vol. 32, no. 11, p. 999, 1996, doi: 10.1049/el:19960669.

[21] Y. Tsividis and C. McAndrew, "Small-Signal Modeling for Low and Medium Frequencies," in *Operation and Modeling for MOS Transistor*, 3rd ed., Oxford: Oxford University Press, Inc., 2011.

[22] J. Jose, A. Ravindran, and K. K. Nair, "Study of Temperature Dependency on MOSFET Parameter using MATLAB," *Int. Res. J. Eng. Technol.*, 2016.

[23] “BSIM3v3 Parameter Table” Accessed: Dec. 13, 2021. [Online]. Available: https://link.springer.com/content/pdf/bbm%3A978-0-306-47050-9%2F1.pdf.

[24] M. M. Mansour and M. M. Mansour, “On the design of low phase-noise CMOS LC-Tank oscillators,” *Proc. Int. Conf. Microelectron. ICM*, pp. 407–412, 2008, doi: 10.1109/ICM.2008.5393840.

[25] Ming-Juei Wu, Jyh-Neng Yang, and Chen-Yi Lee, “A constant power consumption CMOS LC oscillator using improved high-Q active inductor with wide tuning-range,” in *The 2004 47th Midwest Symposium on Circuits and Systems, 2004. MWSCAS ’04.*, 2004, vol. 3, p. III_347-III_350, doi: 10.1109/MWSCAS.2004.1354366.

[26] W. Rieutort-Louis *et al.*, “A figure of merit for oscillator-based thin-film circuits on plastic for high-performance signaling, energy harvesting and driving of actuation circuits,” in *70th Device Research Conference*, Jun. 2012, pp. 117–118, doi: 10.1109/DRC.2012.6256980.