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Transimpedance Amplifier for Early Detection of Breast Cancer

Dissertação para obtenção do Grau de Mestre em
Engenharia Electrotécnica e de Computadores

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Universidade Nova de Lisboa

Resumo

Faculdade de Ciências e Tecnologia
Departamento de Engenharia Electrotécnica e de Computadores

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por Diogo Telmo Cruz Dias

O cancro da mama é o tipo de cancro mais comum, à escala mundial. A eficácia do seu tratamento depende, não só, de uma detecção atempada, mas também da precisão do seu diagnóstico. Algumas técnicas de diagnóstico como a Ressonância Magnética, Sonogramas por Ultra-som e Tomografia por Emissão de Positrões (PET) têm sofrido avanços consideráveis. O trabalho aqui apresentado incide sobre o estudo de uma aplicação PET direccionada para a Mamografia por Emissão de Positrões (PEM).

Um sistema PET/PEM opera sob o princípio no qual um cristal cintilante deverá detectar um impulso de raios gama, originado nas células cancerígenas, convertendo-o num impulso de luz visível. Este último deverá ser convertido num impulso de corrente eléctrica através de um Dispositivo Fotossensível (PSD). Após o PSD, surge um Amplificador de Transimpedância (TIA), cujo objectivo é o de converter o impulso de corrente numa tensão de saída num período de tempo inferior a 40 ns.

No trabalho aqui apresentado é considerado um Fotomultiplicador de Silício (SiPM). A utilização deste dispositivo é impraticável com as topologias de TIAs convencionais. Logo, o projecto do amplificador será sujeito à utilização da topologia Porta Comum Regulada (RCG). Serão apresentadas duas variações da referida topologia, consistindo numa melhoria da resposta do ruído e possibilidade de operação em modo diferencial. A referida topologia irá ainda ser testada no contexto de um receptor de Radiofrequência. Será também apresentado um estudo que incluirá um TIA com realimentação auto-polarizado em tensão reduzida.

Os circuitos propostos são simulados com tecnologia CMOS padrão (UMC 130 nm), alimentados a 1.2 V. Obteve-se um consumo de potência de 0.34 mW e uma relação sinal-ruído de 43 dB.

Palavras-Chave: Tomografia por Emissão de Positrões, Detectores de Radiação, Amplificador de Transimpedância, Fotomultiplicador de Silício, *pulse shaping*.

Universidade Nova de Lisboa

Abstract

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Dissertação para obtenção do grau de Mestre em
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Breast cancer is the most common type of cancer worldwide. The effectiveness of its treatment depends on early stage detection, as well as on the accuracy of its diagnosis. Recently, diagnosis techniques have been submitted to relevant breakthroughs with the upcoming of Magnetic Resonance Imaging, Ultrasound Sonograms and Positron Emission Tomography (PET) scans, among others. The work presented here is focused on studying the application of a PET system to a Positron Emission Mammography (PEM) system.

A PET/PEM system works under the principle that a scintillating crystal will detect a gamma-ray pulse, originated at the cancerous cells, converting it into a correspondent visible light pulse. The latter must then be converted into an electrical current pulse by means of a Photo--Sensitive Device (PSD). After the PSD there must be a Transimpedance Amplifier (TIA) in order to convert the current pulse into a suitable output voltage, in a time period lower than 40 ns.

In this Thesis, the PSD considered is a Silicon Photo-Multiplier (SiPM). The usage of this recently developed type of PSD is impracticable with the conventional TIA topologies, as it will be proven. Therefore, the usage of the Regulated Common-Gate (RCG) topology will be studied in the design of the amplifier. There will be also presented two RCG variations, comprising a noise response improvement and differential operation of the circuit. The mentioned topology will also be tested in a Radio-Frequency front-end, showing the versatility of the RCG. A study comprising a low-voltage self-biasing feedback TIA will also be shown.

The proposed circuits will be simulated with standard CMOS technology (UMC 130 nm), using a 1.2 V power supply. A power consumption of 0.34 mW with a signal-to-noise ratio of 43 dB was achieved.

Keywords: Positron Emission Tomography, Radiation Detectors, Transimpedance Amplifiers, Silicon Photo-Multipliers, pulse shaping.

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Acronyms and Abbreviations

MRI	*Magnetic Resonance Imaging*
PET	*Positron Emission Tomography*
PEM	*Positron Emission Mammography*
PSD	*Photo-Sensitive Device*
APD	*Avalanche Photo-Diode*
SiPM	*Silicon Photo-Multiplier*
TIA	*Transimpedance Amplifier*
ASIC	*Application Specific Integrated Circuit*
CG	*Common-Gate*
RCG	*Regulated Common-Gate*
OTA	*Operational Transconductance Amplifier*
SNR	*Signal-to-Noise Ratio*
TF	*Transfer Function*
NTF	*Noise Transfer Function*
RF	*Radio Frequency*
MOS	*Metal-Oxide Semiconductor*
FET	*Field Effect Transistor*
FDG	*2-deoxi-2-[^{18}F]fluoro-d-glucose (fluorodeoxyglucose)*
LYSO	*Lutetium-Yttrium Oxyorthosilicate*
LO	*Local Oscillator*
RF IN	*Radio Frequency Input*
IF OUT	*Intermediate Frequency Output*
LPF	*Low-Pass Filter*
CS	*Common-Source*
OpAmp	*Operational Amplifier*

GBW	*Gain-Bandwidth Product*
KCL	*Kirchhoff Current Law*
LNA	*Low-Noise Amplifier*
NF	*Noise Figure*
VCVS	*Voltage-Controled Voltage Source*
CD	*Common-Drain*
PVT	*Process, Voltage and Temperature*
FOM	*Figure-of-Merit*
CMFB	*Common-Mode Feedback*
ADC	*Analog-to-Digital Converter*

1. INTRODUCTION

1.1. BACKGROUND AND MOTIVATION

Breast cancer has been the most common type of cancer worldwide [1]. As in any type of cancer, it is of paramount importance to take measures, which reduce the disease's impact as soon as detection occurs. An early diagnosis can most times allow for preemptive options and treatment, made impossible with late-stage detection. This latter topic, early breast cancer detection, is the main driver for the work here presented. For that matter, specialists in the field have been making use of medical imaging techniques such as x-ray mammography (mammograms), almost since radiographies started giving their contribute as a diagnosis tool. However, the limitations of this method can originate false positive and false negative results, over-diagnosing and over-treatment, difficulty in obtaining a good image in patients with breast implants and patient discomfort during the exam [2], [3]. To overcome these limitations, in the last decade researchers have been trying to develop innovative medical imaging systems achieving more precise, better quality and higher image resolution systems. Therefore, a new range of powerful and useful diagnosis instruments [4], [5], [6] which become very effective when working in tandem, have been originated. Diagnosis techniques have been submitted to relevant breakthroughs since the upcoming of Magnetic Resonance Imaging (MRI), Ultrasound imaging (e.g. sonograms) and Positron Emission Tomography (PET) scans, among others. With these techniques, new types of analysis became preponderant since it permitted for different functional and behavioral testing of the areas and organs under study.

The work presented here is focused on studying the application of a PET system to a Positron Emission Mammography (PEM) system, responsible for early detection of breast cancer. A PET system works under the principle that the patient will be injected with a safe dose of radioactive material, often called radiotracer, which will be concentrated around the area under study, as can be seen in Fig. 1.1. Contrarily to x-ray imaging, PET technology monitors the rate of metabolism or chemical activity present in a given area, giving a more behavioral analysis of the organs under study instead of a physiognomic one. When a particle of the radiotracer becomes

consumed it will emit two γ-ray bursts, which can be detected by a scintillating crystal matrix which, in turn, will produce a corresponding light pulse. Afterwards, this light pulse can be converted into a current pulse by means of a photodiode [3], [7], [8]. At present, there are two mainstream options regarding the detection of the γ-rays using photodiodes, both accomplished by means of a Photo-sensitive Device (PSD). The first, and older, uses an Avalanche Photo-diode (APD) matrix. The remaining, more recently developed [9], is accomplished with the usage of a Silicon Photo-Multiplier (SiPM) matrix. The latter option (SiPM) is capable of reaching higher output peak currents, but its output equivalent capacity is also higher. In conceptual terms it can be understood that for each option, different development methodologies must be adopted, depending on the type of device used. While with an APD the most common and traditional methodologies can be used, with a SiPM some topologies may be impracticable due to its higher output capacity.

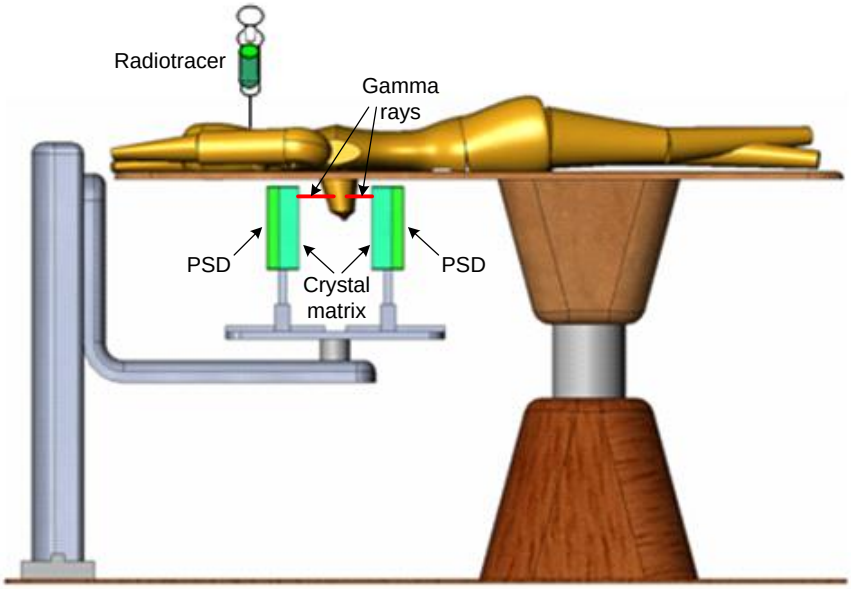

Figure 1.1 - Representation of a PET/PEM patient interface (adaptation from [10]).

1.2. OBJECTIVES

Given the different options regarding the choice of PSDs it is important to establish and set not only the limits where an APD or a SiPM may be used, but the system's development methodologies for each PSD as well. In any case, since both types produce an output current as a function of the radiation received, it is necessary to convert the first into a suitable voltage, with the desired shape and amplitude, for further processing [10], as it is shown in Fig. 1.2. This conversion can be accomplished via a Transimpedance Amplifier (TIA), with different

topologies, depending on the type of PSD used. A TIA is a device commonly used in applications, which require current-voltage conversion and signal shaping. TIAs are widely applied in nuclear science, instrumentation and medical imaging [9], [11], which is the main focus of this thesis. Moreover, this type of devices are also used in RF front-ends and optical communications systems [12], [13], [14], The type of TIAs here designed are widely used in PET scanners front-end. As an example, in [10] a total of 6×32 - channel Application-Specific Integrated Circuits (ASICs) were developed, where the most challenging part of it was the design of the 192 TIAs with the respective APDs at their inputs, since the first is what determines the system's limits of performance. The main focus of the work presented here is to develop the front-end of a PEM scan system using a SiPM as an input device. The TIA developed should not exceed a power consumption of 1 mW, while being able to present the capability of pulse shaping and maintaining low noise level.

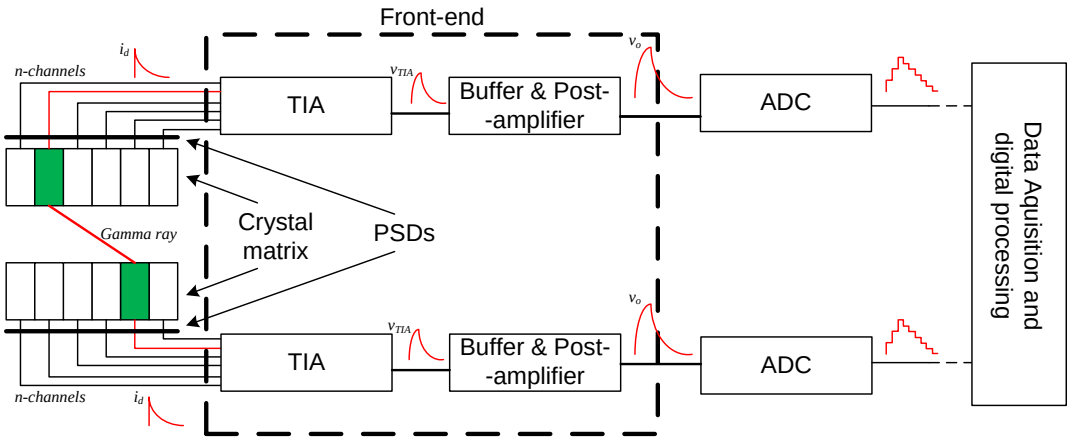

Figure 1.2 - Block diagram of the PET/PEM front-end.

The classical approach is to design the front-end using a Feedback TIA based on capacitive noise matching [14], where the input capacity of the TIA would match the PSD's output capacity. However, with the SiPM at the input, not only this topology becomes impracticable, mainly due to the SiPM's high output equivalent capacity, but also the output voltage rising time would be too high for the application it is designed for. Therefore, alternative topologies must be taken into account. In order to support this fact, a study and an extensive evaluation of the three most used topologies will be made. The choice of topologies studied will fall into the feedback-TIA, the Common-Gate (CG) TIA and, finally, the Regulated Common-Gate (RCG) TIA. As an improvement of the CG TIA, the RCG TIA will be more extensively studied than its counterparts, since it will be the topology of choice. In order to prove the impracticability of the feedback TIA with the SiPM at the input, a study will be presented considering the design of a PEM scanner

front-end using the referred topology with an APD and a SiPM. For the effect, a previously studied and developed Operational Transconductance Amplifier (OTA) will be used.

During the study of the RCG TIA various development phases are to be encountered in the progress of this dissertation. In a first phase a study of the basic topology will be made concerning a conceptual and functional analysis. In the second phase the basic RCG TIA will be slightly altered in order to achieve a better overall device noise distribution, presenting slightly improved noise level and signal-to-noise ratio (SNR). Finally, in the last phase, the possibility of differential output will be considered, further exploring the development taken by in the second phase, improving the TIA's output voltage amplitude. For any of these phases, there will be a detailed analysis contemplating the TIA's transfer function, or Transimpedance Function (TF), the Noise Transfer Function (NTF) with its pole-zero location, circuit's linearity and output voltage amplitude and shape. In addition, the RCG TIA will also be considered in a Radio-Frequency (RF) receiver, providing there is a hypothetical generalized passive mixer at the input, showing this topology's versatility and adaptability.

The main focus of this dissertation is to provide the guidelines necessary to design a RCG TIA meant to operate with a SiPM at the input, explore any range of options that can permit a noise reduction of the front-end system, provide proof that with the PSD chosen the more traditional solutions cannot be considered, show the versatility of this topology in the context of a RF front-end and, finally, design and simulate the circuits in a standard CMOS 130 nm technology.

1.3. THESIS STRUCTURE AND ORGANIZATION

In the present section the interest remains in showing the key topics discussed in this dissertation and provide a guide to the structure adopted. Accounting for the present introductory chapter, the work here presented will be sectioned into six main chapters which describe the basic knowledge into the state of the art regarding PET systems, radiation detectors, some insight into Metal-Oxide Semiconductor (MOS) Field-Effect Transistors (FETs), TIA topologies, and the chosen circuit's analysis, development and evaluation. In a more detailed description, one will find the following chapters:

Chapter 2 – PET Systems and Radiation Detectors

In this chapter it is intended to review the state of the art regarding PET systems and present some considerations regarding a hypothetical passive mixer, making the TIA operate in a RF context. Some PET considerations such as the physical principles behind this technology,

system's requirements and specifications along with some insight into PSDs will be contemplated. Regarding the passive mixer, a brief definition will be given providing the specifications used in the design of the TIA for that matter. In the last part of this chapter, high focus will be given in providing a study of some of the topologies most commonly used and the principles in circuit design with MOS devices and amplification stages used. There will be a distinction between three major topics, with these being a study of the MOS device and amplification stages necessary, the feedback TIA and the CG TIA.

Chapter 3 – The Regulated Common-Gate Transimpedance Amplifier

In the third chapter the focus is to study the referred TIA topology. For each phase of development there will be a sub-chapter contemplating a conceptual and behavioral analysis of the circuit. The interest here remains in showing a circuit description, transimpedance function and noise transfer function in a succinct and objective manner. The three sub-chapters will be distinguished by the differences in the circuits' schematics, which will correspond to the basic RCG, the RCG with improved noise distribution and, finally, with differential output.

Chapter 4 – TIA Sizing and Design Procedures

This chapter will have the purpose of showing the options taken in the design of the circuits. For each development phase, the sizing of the TIAs will be shown and commented. The chapter will be divided into two sections, in which the design of the TIA in a RF front-end context and, separately, by each development stage, in a Radiation Detector front-end context, will be studied.

Chapter 5 – Simulation Results

The obtained results will be shown and compared in this chapter in order to provide an idea of which choices prove to be better. Separately, the design of a feedback TIA with an APD at its input will be shown and properly analyzed. In this chapter only the main results from the RCG TIA designed to operate with a passive mixer at the input will be shown, proving the versatility of this topology.

Chapter 6 – Conclusions and Future Work

In the last chapter, final remarks and considerations will be made, comprising a conclusion of the work taken by herein and possible future development and research topics referent to the work presented.

1.4. MAIN CONTRIBUTIONS

Regarding any scientific contributions, it is of best hope that the work presented may serve as a guideline to the implementation of PEM scan systems front-end, using the most recently developed SiPM technology. It is also of best hope that the circuit's versatility can be taken into account, given the RF receiver context. With the improved noise distribution and low power consumption, it is expectable that this dissertation will present a viable solution for the next generation of ASICs in the area of PEM medical imaging.

Some of the work presented here contributed with a publication accepted for oral presentation at 2014 IEEE International Conference Mixed Design of Integrated Circuits and Systems (MIXDES) [15]. Recently, this paper originated an invite of an extended version to be submitted into the International Journal of Microelectronics and Computer Science.

2. PET SYSTEMS AND RADIATION DETECTORS

In this chapter PET/PEM systems basics for radiation detectors will be reviewed. Some aspects and concepts of these systems will be succinctly exposed, such as the radiotracer used, physical principles behind tumor detection, radiotracer annihilation and photon detection. Thus, the system requirements for the design here taken by will be given. Finally, the RF front-end along with its mixer will be shown in order to give a certain level of contextualization. In the last part of the chapter some of the topologies most commonly used, along with the amplifying stages that constitute them, will be studied.

2.1. PET SYSTEM PHYSICAL PRINCIPLES

Positron emission, or β^+ decay, is the process by which an atom obtains the optimal ratio between its protons and neutrons [16], [17]. Basically, it reflects a common method where an atom has one of its protons converted into a neutron and a positron. A positron, commonly known as an anti-electron, is the anti-particle of the electron. Both particles have same mass but opposite electrical charge. When a positron is ejected from the nucleus of an atom the energy originated can vary from zero to a maximum emission energy, E_{max} [18]. In a PET system this is the key principle behind this imaging technique. The first step in the realization of a PET exam is the injection of the radiotracer responsible for the positron emission into the subject under study [19]. Basically, a radiotracer is a chemical compound, in which, one or more of its atoms have been replaced by a radioisotope. In PET technologies the radiotracer most commonly used is the 2-deoxi-2-[^{18}F]fluoro-d-glucose, also known as fluorodeoxyglucose (FDG), which stands for a molecule similar to glucose that is absorbed by the cells using its same transport method. After being absorbed the FDG is phosphorylated and, since the resultant compound cannot be metabolized, it will remain in the cell where it was absorbed being, this way, able to serve as a marker in the metabolic rate of glucose [18]. Cancer cells have a glucose consumption far more

superior then healthy tissue, making it possible to differentiate the types of tissues being observed [20]. This is where PET scans differ from other imaging techniques such as x-ray imaging. By quantitatively observe the metabolic rate of glucose consumption, this technique offers a functional or metabolic analysis of the areas under study, instead of an anatomic analysis.

2.1.1. *Positron Annihilation*

Human tissue is a highly rich environment in electron density. Logically, this means that the ejected positron will be quickly consumed, resulting in a very short lifetime period. Most of its kinetic energy will be promptly dissipated by interacting with other electrons present in the human tissue. Having most of its energy dissipated, the positron can then be combined with an electron, in a hydrogen-like state, often called positronic, that will last for only around 10^{-10} seconds. Following this period of time, a process known as annihilation will occur where the masses of both the electron and the positron will be converted into electromagnetic energy. By practically being at rest, this conversion of mass into energy will be due to the particles masses. One can have the resultant energy measured through Einstein's equation [18]:

$$E = mc^2 = m_e c^2 + m_p c^2 \tag{2.1}$$

where $m_e = m_p \cong 9.1 \times 10^{-31}$ kg are the masses of the electron and positron and $c \cong 3 \times 10^8$ ms^{-1} is the light speed in vacuum. The energy originated by the annihilation will result in a total of $E \cong 1.64 \times 10^{-13}$ J, which is the same as approximately $E \cong 1.022$ MeV [21].

When annihilation occurs the electron-positron pair is practically at rest, which means that the resultant linear momentum is near zero. The energy originated at the annihilation will be released in the form of high energy photons and, given the linear momentum, spin and energy conservation laws [19], the process will result in the emission of two equal high energy photons, expelled in opposite directions. Note that otherwise – if a single photon was expelled or photons direction was not opposite – the conservation of the linear momentum would not be verified, since it would have the resultant direction. The energy originated will be equally divided by both photons which means that each one will be presenting an energy of 511 keV which, regarding the electromagnetic spectrum, characterizes these photons in the gamma ray range. Fig. 2.1 illustrates the behavior of the electron-positron pair in the referred process.

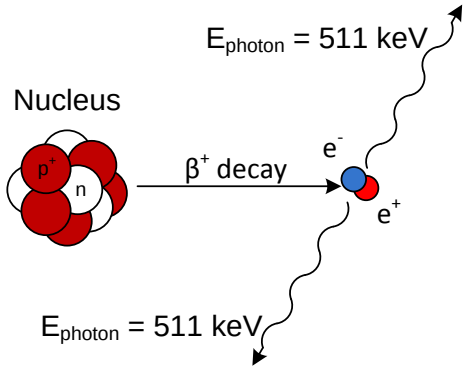

Figure 2.1 – Illustration of the annihilation process (adaptation of [18]).

The annihilation photons, or gamma ray photons, are highly energetic and, therefore, they can be detected after working their way out of the human body [21], [18]. Contrarily to what the system's name suggests, it is the gamma ray photons that can be detected instead of the positrons, since these latter ones collapse inside the human body. One other point worth mentioning is the fact that since the gamma ray photons are expelled with a very high geometrical precision, the line that is common to both detection points, called line of response, will pass directly through the point of annihilation [18]. By measuring the total amount of radiation, obtained by several lines of response, it is then possible to reconstruct an image of all the points where annihilation has been detected via computerized, mathematical algorithms, even though this is an aspect out of the scope of this thesis.

2.1.2. *Photon Detection*

One of the most important specifications in a PET system is the minimum resolution to which the system can capture and reproduce an image. A system with a good minimum resolution will be able to identify smaller masses, becoming a more precise system. The system's resolution can be defined as the minimum detectable distance between two points in an image [22]. In order to detect the incident photons, two major techniques are employed: the first uses timing resolution, in which annihilation positioning is accomplished through the timing differences between the arrival of each annihilation photon [18]; the second method – the one of interest in the present work – uses spatial resolution which, basically, is accomplished by using two matrixes of detectors as shown in Fig. 2.2.

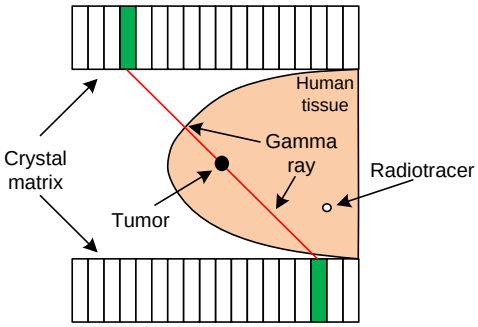

Figure 2.2 – Generalized gamma ray detection using spatial resolution.

Photon detectors are usually accomplished by means of a scintillating crystal. There is a wide range of crystal types for that matter but, the ones we are interested in are Lutetium-Yttrium Oxyorthosilicate (LYSO) crystals. These innorganic crystals, usually transparent, have a higher density than most, making it possible to accomplish higher precision in photon detection. They are characterized by their stopping power, light emission wavelenght and duration of light pulse, or decay time [18]. Usually, in a LYSO crystal, the decay time is around 40 nanoseconds. A scintillating crystal has the purpose of serving as an interaction media between the gamma rays it receives and the visible light photons it emmits. In Fig. 2.3 some examples of LYSO crystal matrixes can be found.

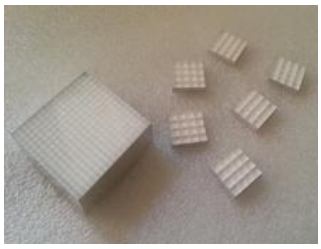

Figure 2.3 – Image of a 256 LYSO crystal matrix and various 16 LYSO crystal matrixes (adapted from [23]).

When a scintillating crystal receives a high energy photon such as a gamma ray, it will isotropically emmit visible light, proportional to the energy received as can be seen in Fig. 2.4. Immediately after the scintillating crystal there must be coupled a PSD such as a photodiode responsible for the conversion of the light pulse, originated in the crystal, into a correspondant electrical current. The current produced at the PSDs output will be proportional to the amount of light it received and, therefore it will be proportional to the energy contained in the gamma ray detected by the LYSO cristal.

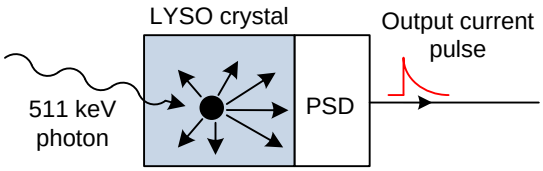

Figure 2.4 – Constituting blocks of a photon detector with a scintillating crystal and a PSD (adapted from [18]).

Regarding PSDs, these are devices that, by taking advantage of the photoelectric effect, are able to convert visible light into an electrical current. In a PET system, the most commonly adopted solution is to use an APD coupled with the scintillating crystal. In the electronics front-end the PSD can be considered the first stage to provide gain to the signal. Therefore, one must take into account that the higher the gain presented by the PSD, the higher the SNR will be [24]. These devices can be characterized by a few basic parameters such as quantum efficiency, excess noise factor, dark or output peak current, I_d, output capacitance, C_d, and operating voltage. However, for the sake of the present work we are only interested in these devices' output current and capacity.

One other type of a PSD, the one considered here, is the most recently developed SiPM. This type of device is built in arrays of Geiger-mode APDs with resistive quenching, connected in parallel on common silica substrate and has the ability of single-photon detection in a time response much lower than 1 nanosecond [9]. One of the properties that makes this type of device a suitable candidate for PET imaging systems is its low operating voltage capability, ranging from 20 to 100 V, depending on the APD technology used. As with APD technology, regarding SiPMs we are interested in accounting for the output current and capacitance values. These parameters, for the referred devices, are $I_d = 2.25$ µA and $C_d = 10$ pF for the APD; and $I_d = 22.5$ µA and $C_d = 300$ pF with a SiPM. Note that in the case of the SiPM the output capacitance may vary from 100 – 300 pF [7] but, in any case, we tend to use the worst case scenario value (higher output capacitance). By having a higher output current, one could be led to think the SiPM would necessarily bring a higher output peak voltage. However, due to its higher output capacitance, it becomes difficult to accomplish an output voltage that has a suitable shape, without increasing the power consumption beyond the acceptable. This is the main reason why alternative solutions must be found when designing the TIA with a SiPM at the input.

In this work the interest remains in the analysis of the electronics front-end of the system. Therefore, regarding PSDs, it is important to reveal their equivalent electrical circuit. For both PSD cases – in the case of a SiPM, a simplified version [9] – their equivalent circuit is a current source, i_d, in parallel with the equivalent output capacitance, C_d [25], [26]. In Fig. 2.5 an example of a matrix with both PSDs is presented.

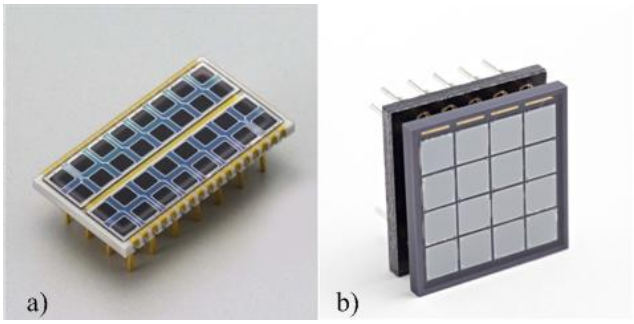

Figure 2.5- Image of both types of PSDs: a) 32 APDs matrix [27];
b) 16 SiPMs matrix [28].

2.2. SYSTEM REQUIREMENTS

Much like any other type of system, the PET/PEM front-end must fulfill a given number of requirements. In the present sub-chapter, these will be described. Concepts such as input current and output voltage shape, rising or peaking time, SNR, power consumption, supply voltage and integrated noise level will be mentioned. As another point of interest, a contextualization regarding the TIA in a RF front-end, with a passive mixer at the input will be provided.

2.2.1. *Radiation Detector Front-end*

Following what was previously stated, the TIA must be inserted into the front-end shown in Fig. 1.2 with the objective of converting any type of PSD's output current into a suitable voltage, i.e., its input current pulse must be transformed into a voltage pulse with the desired shape and amplitude. Fig. 2.6 shows the equivalent circuit of any of the PSDs here mentioned (a simplified model in the case of a SiPM) coupled with a basic transimpedance block, along with the TIA's input current and output voltage shapes.

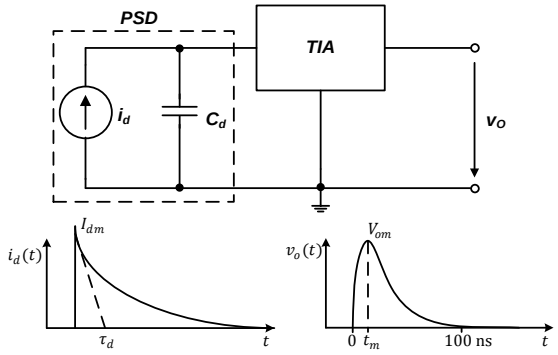

Figure 2.6 – Generalized architecture of a radiation detector front-end with the TIA's input current, $i_d(t)$, and output voltage, $v_o(t)$, shapes (adapted from [8]).

The input current pulse, $i_d(t)$, has a very fast rising time (much lower than one nanosecond in the case of the SiPM [9]) and, after reaching its maximum peak current, I_{dm}, it starts decaying following a time-constant τ_d [15], following

$$i_d(t) = I_{dm} e^{-t/\tau_d} , \qquad t \geq 0. \tag{2.2}$$

This time-constant is dependent on the technology used in order to achieve the PSD and, with the LYSO technology chosen, it is approximately $\tau_d = 40$ ns. The output voltage must be as the one shown in Fig. 2.6. Even though the exact shape of $v_o(t)$ is not of paramount importance, its variation must reach a maximum peak voltage, V_{om}, in less than forty nanoseconds, which means $t_m < 40$ ns. This peaking time is a key restriction since the work here presented is based in previous studies [10] and, will limit the performance of the system's front-end, as it will be seen further on. In the sizing presented t_m was aimed to be lower than the required in order to contemplate the expectable high parasitic capacitances in the output buffer which, most definitely, will influence the TIA's frequency response. One requirement that must be fulfilled at any cost is a good and predictable linearity between I_{dm} and V_{om}, i.e., the total charge injected by the current source, Q_d, in which

$$Q_d = I_{dm} \tau_d \tag{2.3}$$

must be proportional to V_{om}, without affecting the peaking time. In practical terms this will impose that the amplifier's input and output must have a linear relation.

Since the work here presented is based in previous studies, the requirements necessary to accomplish a good design follow the ones in [7], [8], [10]. Therefore, following these latter ones, the transimpedance function must have two poles in order to accomplish the desired pulse shaping, having the form:

$$\frac{V_o(s)}{I_d(s)} = \frac{R_m}{(1 + s\tau_1)(1 + s\tau_2)} \tag{2.4}$$

where R_m denotes the low frequency transimpedance gain of the amplifier. Actually, a single-pole system would suffice in order to obtain the pulse shaping required. The problem with such an approach is that since the noise transfer function will have a low frequency zero – as it will be seen in the following chapters – the transimpedance function must have one other pole so it can cancel the mentioned zero. It is also estimated that the output peak voltage must reach $V_{om} = 1$ V, in order to be comparable to previously designed amplifiers. Given the low voltage

characterization of the design here submitted, $V_{DD} = 1.2$ V, it becomes impossible to reach the desired output peak voltage and, since this is a mandatory requirement, a post-voltage amplifier must be used after the output buffer. This way, the output voltage can reach the required value maintaining approximately the same SNR value. Following the requirements stated, it will be possible for the system to reach a resolution of 1 to 2 millimeters in a mammography examination lasting 5 minutes, using a safe dosage of radiation [7], [8].

2.2.2. *RF Receiver Front-end*

When in a RF receiver front-end, the TIA has the very specific objective of converting the mixer's output current into a suitable voltage as depicted in Fig. 2.7.

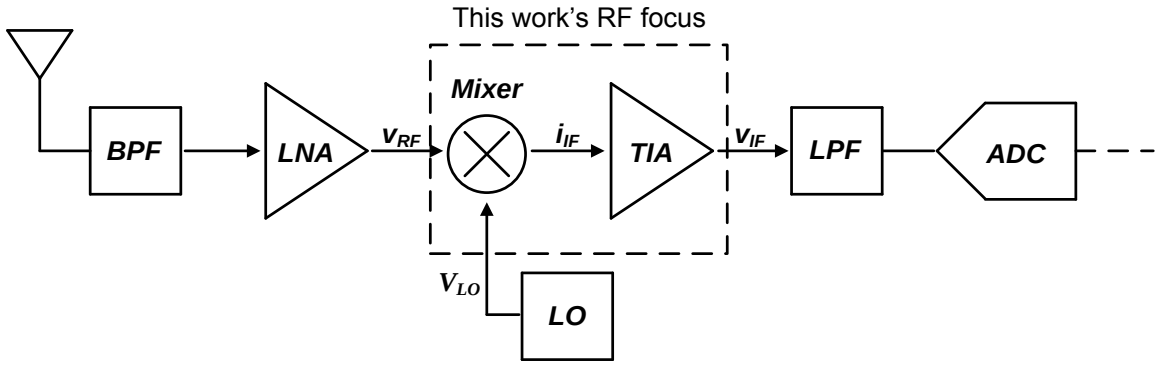

Figure 2.7 – Block diagram of a heterodyne receiver architecture with focus on the mixer and TIA.

The focus, regarding the RF front-end, is to study the application of the RCG TIA topology driven by the output current of a basic hypothetical passive mixer.

Ideally, a mixer is a circuit that can be viewed as an analog multiplier circuit [29]. Such circuit has the function of translating a carrier signal from one frequency to another [30]. In a generalized manner such block can be defined as a three-port device consisting in a Local Oscillator (LO), Radio Frequency Input (RF IN) and Intermediate Frequency Output (IF OUT) as represented by Fig. 2.8.

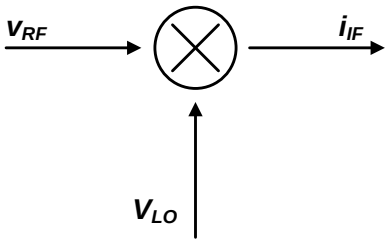

Figure 2.8 – Block diagram of a mixer.

It should be noted that in Fig. 2.8 the output of the mixer, IF OUT, comes in the form of a current when there is a low load impedance at its output, thus, the need of a TIA to convert it into a suitable voltage. The LO usually consists in a large signal with fixed amplitude avoiding, this way, a small signal analysis of the active devices. By multiplying both entry signals, the mixer will produce sum and difference frequencies, along with other spurious tones, due to even and odd harmonics present within each signal. Therefore, and because multiplication in the time domain corresponds to convolution in the frequency domain, it can be easily observed that the spectral density around $\pm\,\omega_{LO}$ will be translated to $\pm\,(\omega_{RF} \pm \omega_{LO})$ [29] as Fig. 2.9 suggests.

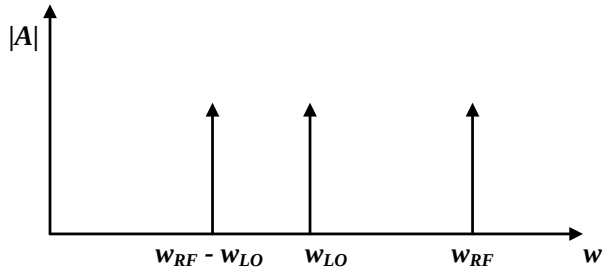

Figure 2.9 – Example of frequency down-conversion in heterodyne receivers.

In this case, the negative components of the frequency are not of interest and have been neglected. Also neglected, the components in $\omega_{RF} + \omega_{LO}$ have no practical interest and, as such, must be filtered using a Low-Pass Filter (LPF) function. This leaves the signal's spectral density at $\omega_{RF} - \omega_{LO}$ in an operation called down-conversion mixing. In heterodyne receiver architectures the LO uses a frequency different from the RF signal resulting an IF signal with non-zero frequency.

The design of a mixer can be somewhat complex and it can be distinguished between an active and a passive device, depending on providing or not providing signal amplification, respectively [29]. In the present work a basic passive mixer, which consists on a switching device controlled by the LO, is considered. Basically, the mixer considered is nothing but a MOS transistor sized to operate in the triode region. When in this region, the MOS transistor can perform as a switch if the remaining resistances present in the circuit are much higher than the equivalent resistance of the MOS device conduction channel [31], as shown by Fig. 2.10. In these conditions, the device will operate as an open switch every time V_{LO} is at low level and as a closed switch, with an equivalent R_{DS} resistance, when V_{LO} is at high level. The load impedance, Z_{TIA}, i.e., the equivalent impedance seen at the input of the TIA, has the function of converting the mixer's output current into an output voltage. In the design shown further on, this resistor is replaced by the TIA's equivalent input impedance in parallel with the mixer's output capacitance, C_M. As in the radiation detector case, the mixer can be resumed to an equivalent current source, $i_M(t)$, in parallel with its output capacity. Regarding the design shown further ahead, it was

considered that the mixer had a sinusoidal output current with amplitude of 1μA with frequency around 10 MHz. Note that the mixer's output capacity, C_M, is mostly determined by the parasitic capacitances of the active device responsible for the switching in the mixer. This equivalent capacity was established to be around 0.1 pF, since the device does not need to be considerably large.

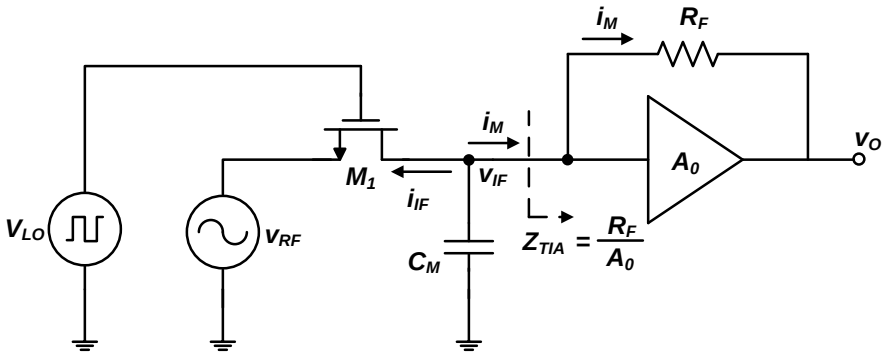

Figure 2.10 – Schematic of a basic mixer with its equivalent output capacitance and TIA's equivalent input impedance.

Even though the basic mixer may present a simple enough design, there is a serious consideration that must be taken into account. In order to operate in the triode region, the transistor must have a very low V_{DS} voltage. This means that if the output current is too high, correspondently low load impedance must be chosen. Otherwise, any variation in v_{IF} will cause V_{DS} to rise leading the transistor to other non-suitable operating regions. Regardless, v_{IF} can never have high amplitude since it will make the transistor leave the triode region. This is a key restriction and it will influence the design of the TIA in an RF context since its input impedance will have to be suitable for a low variation of v_{IF}.

2.3. BASIC AMPLIFICATION TOPOLOGIES

In this sub-chapter a detailed insight into some amplification topologies will be given. Firstly, the basic amplification stages used – the CG and Common-Source (CS) stages – will be studied. Concepts such as their voltage gain, noise analysis, incremental and dc operation modes and frequency response will be shown in order to fully understand the transimpedance topologies. Afterwards, two of the most common TIA topologies, the feedback TIA and CG TIA will be shown, their transfer functions and noise transfer functions will be derived, allowing for a deep comprehension of these topologies.

2.3.1. *Common-Source Voltage Amplifier*

The CS stage is one of the most basic amplifier configurations. Due to its relatively high voltage gain and input impedance, it is normally a configuration of choice in order to realize the input stages of Operational Amplifiers (OpAmp), even though its frequency response has a narrow band characteristic. Regardless, improvements such as source degeneration can be made to this configuration in order to increase its passing band, lowering the gain and raising the bandwidth, maintaining a constant Gain-Bandwidth Product (GBW).

In this configuration the signal is applied to the gate of the MOS device which is physically isolated from the transistor's conduction channel. In practical terms this means that, for low frequencies, the input impedance of the transistor is high enough to be considered infinite. The CS configuration, which is represented in Fig. 2.11, can be applied with passive or active load. In the first there is a resistor connected from the power source to the drain of the transistor and, in the latter, the load impedance is accomplished by using a current source with an equivalent dynamic impedance. With active load, the configuration is able to present a higher voltage gain since it makes use of the nonlinear, large-signal transistor equations to create simultaneous conditions of large bias currents and large small-signal resistances [32].

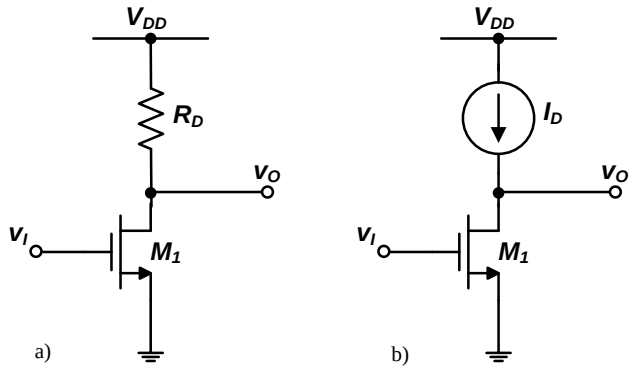

Figure 2.11 – Common-source configuration with: a) passive load; b) active load.

In the present chapter there will not be a clear distinction between active or passive load and, therefore, the symbol R_D will be used to identify any of the respective resistances. In Fig. 2.12 a graphical approach to the CS large and small signal analysis is shown. The large signal or dc operating point for each value of V_{GSi}, with $i = 1, \dots, 4$, is the intersection between the characteristic of $i_D(v_{DS})$ with the load curve. Note that the dc operating point contemplates only the dc component of each v_{GS}. Regarding the incremental output quantities, i_d and v_{ds}, these can be obtained by analyzing the incremental component of the input voltage, v_{gs}. Since the circuit is approximately linear with small amplitude v_{gs}, results that i_d and v_{ds} will be proportional to the

first. Once v_{gs} rises excessively i_d and v_{ds} will present a certain amount of distortion due to the quadratic form of the MOS transistor characteristic [31], [33].

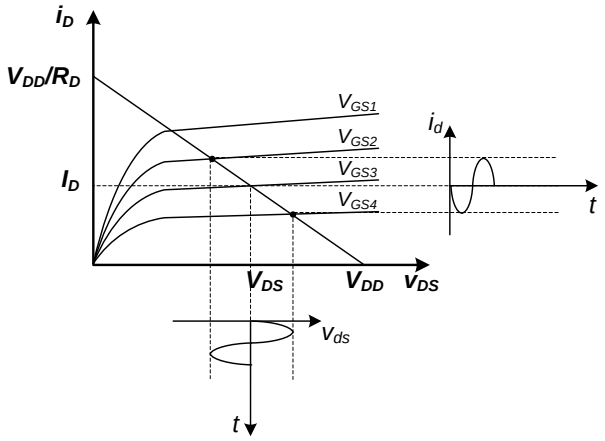

Figure 2.12 – Graphical analysis of CS configuration (adapted from [31]).

The low frequency incremental, or small-signal, model of the CS configuration is the one shown in Fig. 2.13. The incremental input voltage, $v_{gs} = v_i$, is the controller for the output drain current, i_d, which is then converted to an output voltage, here represented by v_o, by the parallel impedance constituted by the load and the equivalent conduction channel resistances.

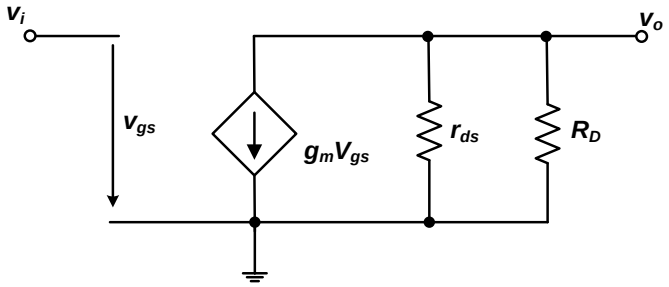

Figure 2.13 – Low frequency incremental model of the CS configuration.

The open-loop voltage gain, A_{v0}, of this amplification stage can be easily deducted and, by inspection, it follows:

$$A_{v0} = \frac{v_o}{v_i} = -g_m(r_{ds} \| R_D) \tag{2.5}$$

where g_m is the transconductance of the MOS device and r_{ds} is the resistance associated to the device's conduction channel. In the majority of cases, principally when using passive load, $R_D \ll r_{ds}$. This will make the conduction channel's equivalent resistance negligible, resulting therefore:

$$A_{v0} = \frac{v_o}{v_i} = -g_m R_D \tag{2.6}$$

The input impedance in this configuration tends to be infinite since the gate is isolated from the conduction channel. The output impedance, in low frequency, is also high and it can be viewed as

$$R_{out} = \frac{v_o}{i_o} = r_{ds} || R_D \tag{2.7}$$

In order to evaluate and identify any noise source that can influence the behavior of the circuit, Fig. 2.14 shows the incremental model of this configuration with its noise sources. In order to obtain the effects they cause in the output of the circuit, one can identify every noise source present in the model and, assuming they are all independent from each other, evaluate the power each noise source produces [34]. Following the superposition theorem, the total output noise power will be the sum of the contributions of each noise source, assuming that the noise sources are uncorrelated.

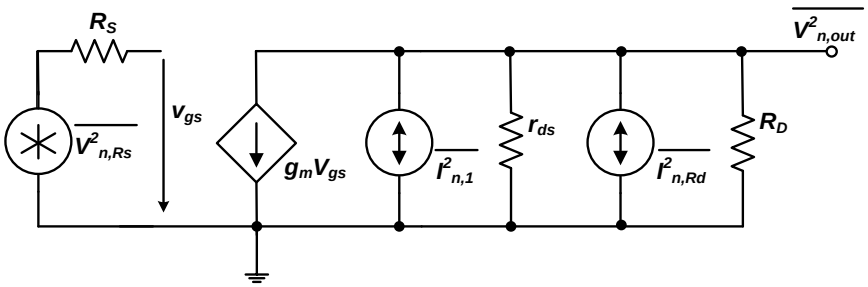

Figure 2.14 – Incremental CS model with respective noise sources.

Since the circuits here designed operate in high frequency, the flicker $(1/f)$ noise is being neglected. The main contributions for the output noise power are the transistor's conduction channel thermal noise current, $\overline{I^2_{n,1}}$, the load resistance equivalent thermal noise current, $\overline{I^2_{n,R_D}}$ and the input signal's Thévenin equivalent thermal noise voltage source, $\overline{V^2_{n,R_s}}$. This way, each noise source has a contribution to the total output noise power that follows:

$$\overline{V^2_{n1,out}} = \overline{I^2_{n,1}} R_D^2 = 4kT\gamma g_m R_D^2 \tag{2.8}$$

$$\overline{V^2_{nR_D,out}} = \overline{I^2_{n,R_D}} R_D^2 = \frac{4kT}{R_D} R_D^2 = 4kTR_D \tag{2.9}$$

$$\overline{V_{nR_S,out}^2} = \overline{V_{n,R_s}^2} A_{v0}^2 = 4kTR_S g_m^2 (r_{ds}||R_D)^2 \tag{2.10}$$

where $k \cong 1.38 \times 10^{-23}$ JK^{-1} is the Boltzmann's constant, T represents the absolute temperature in Kelvin and γ is the transistor's noise coefficient, a parameter dependant on the size of conduction channel's length ($\gamma = 2/3$ if long channels are chosen and $\gamma = 1$ for short channel transistors). The total output noise power is nothing but the contribution of each source, i.e.

$$\overline{V_{n,out}^2} = \overline{V_{n1,out}^2} + \overline{V_{nR_D,out}^2} + \overline{V_{nR_S,out}^2} \tag{2.11}$$

The high frequency model of the CS stage is slightly more complex since it includes the parasitic capacitances of the p-n junctions of the device. In Fig. 2.15 this model is shown, contemplating the three most preponderant parasitic capacitances present in the circuit.

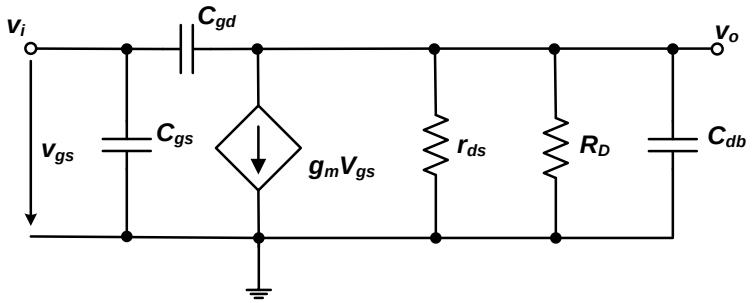

Figure 2.15 – High frequency model of the CS configuration.

In this configuration there are only three major capacities. In other configurations a parasitic capacity between the bulk and source of the device can be also modeled, but since this configuration has the bulk shunted with the source, which means there is no body effect, that capacity, C_{sb}, is short-circuited and, therefore, not present.

The high frequency gain of the CS configuration can be found by applying the Kirchhoff Current Law (KCL) in the output node, resulting

$$g_m v_i + \frac{v_o}{(r_{ds}||R_D)} + v_o s C_{db} + (v_o - v_i) s C_{gd} = 0 \tag{2.12}$$

The gain of the configuration can then be obtained by rearranging the expression:

$$A_v(s) = \frac{V_o(s)}{V_i(s)} = \frac{s g_m^{-1} C_{gd} - 1}{1 + s(r_{ds}||R_D)(C_{db} + C_{gd})} g_m (r_{ds}||R_D) \tag{2.13}$$

which corresponds to

$$A_v(s) = \frac{s\tau_z - 1}{s\tau_p + 1} A_{v0} \tag{2.14}$$

where τ_z is related to the zero associated with capacity C_{gd}, τ_p is the time-constant associated with the output node and A_{v0} is the low frequency gain.

At higher frequencies the input impedance ceases to be infinite. This is motivated by the appearance of the parasitic capacitances present at the gate of the transistor. By Miller's theorem (see appendix A) the parasitic C_{gd} can be replaced by a Miller impedance, Z_M connected between the gate and ground of the transistor with value

$$Z_M = \frac{1}{sC_{gd}(1 - A_{v0})} \tag{2.15}$$

The input impedance can then be defined as the parallel between the Miller impedance and the impedance of C_{gs}, following

$$Z_{in} = \frac{1}{sC_{gs}} || Z_M \tag{2.16}$$

Developing the expression and substituting (2.5), (2.15), (2.16) and knowing that $A_{v0} \gg 1$, a simplified expression for the input impedance can be obtained [34].

$$Z_{in} \cong \frac{1}{s(C_{gs} - A_{v0}C_{gd})} = \frac{1}{s(C_{gs} + C_{gd}g_m(r_{ds}||R_D))} \tag{2.17}$$

The output impedance of this configuration can be found by inspection, as in the low frequency case, by nullifying the input voltage source. Thus it will be constituted by the parallel present at the output node, which comprises the conduction channel equivalent impedance, the load impedance and the impedances originated by the parasitic capacities C_{db} and C_{gd}. Thus, it will be

$$Z_{out} = \frac{V_o(s)}{I_o(s)} = r_{ds}||R_D||\frac{1}{sC_{db}}||\frac{1}{sC_{gd}} \tag{2.18}$$

2.3.2. *Common-Gate Voltage Amplifier*

In RF circuit design it is usually necessary to match the amplifier's input impedance to the transmission line impedance, which is typically 50 Ω. The CG configuration can provide an easier adaptation to these impedances since its input impedance is usually much lower than in the CS stage case, making it easier to achieve the typical characteristic impedance of the transmission line. This configuration bandwidth, as will be further seen, is similar to the one of CG stage. In Fig. 2.16 the basic CG configuration is shown with passive and active load.

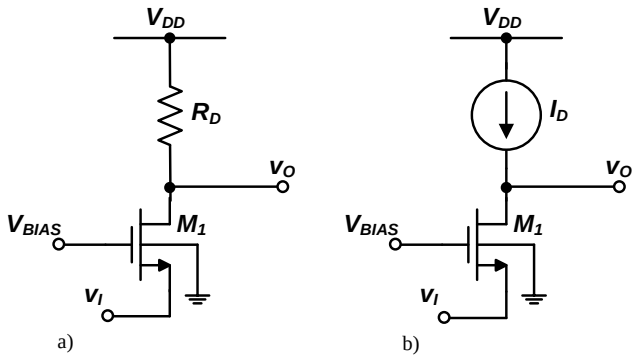

Figure 2.16 – Common-Gate configuration with: a) passive load; b) active load.

In this configuration the gate of the MOS device is connected to a biasing dc voltage. The input signal is applied to the source of the transistor, which will present a v_{sb} voltage making the body effect non-negligible. One important characteristic of this configuration, which is exploited in the present work, is the fact that the input signal can now come in the form of a current, being suitable to amplify the PSD's output current.

When analyzing the incremental model, present in Fig. 2.17, one can find the expressions that characterize the low frequency open-loop gain, input and output impedance. Note that in this configuration there is a voltage-controlled current source, dependant on v_{sb}, motivated by the body-effect.

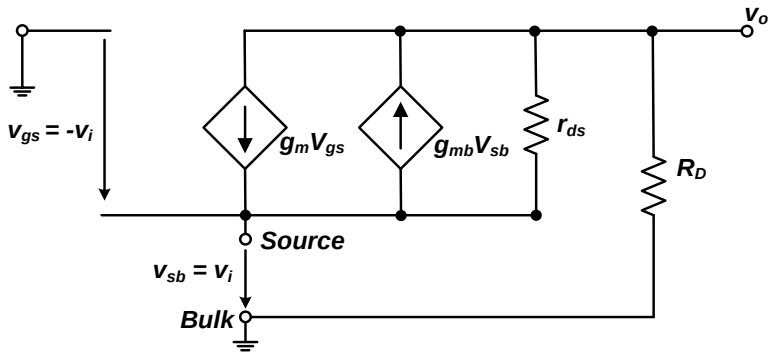

Figure 2.17 – Low frequency incremental model of the CG configuration.

In this case the current source originated by the body effect is actually beneficial. If one takes into account that $v_{gs} = -v_i$ the current that passes through the device will be proportional to $(g_m + g_{mb})v_{gs}$. Therefore, the body effect actually boosts the total transconductance of the configuration in about 10 to 30 percent, since g_{mb} is about 7 to 9 times lower than g_m. Similarly to the case of the CS stage, the low frequency open-loop gain of this configuration can be easily found with the aid of KCL, following:

$$A_{v0} = \frac{v_o}{v_i} = \frac{R_D\big((g_m + g_{mb})r_{ds} + 1\big)}{R_D + r_{ds}} \tag{2.19}$$

and if $r_{ds} \gg R_D$,

$$A_{v0} = \frac{v_o}{v_i} = (g_m + g_{mb})R_D \tag{2.20}$$

The low frequency input impedance of this amplification stage can be found by applying KCL to the input node, resulting in

$$R_{in} = \frac{v_i}{i_i} = \frac{r_{ds} + R_D}{r_{ds}(g_m + g_{mb}) + 1} \tag{2.21}$$

Note that if $r_{ds} \gg R_D$ the input impedance will simply result in

$$R_{in} \cong \frac{1}{g_m + g_{mb}} \tag{2.22}$$

Regarding the noise analysis, the same procedure as the one presented in the CS stage can be made. Fig. 2.18 shows the incremental model of the CG configuration with all noise sources included, except for the low frequency flicker noise source for the reason previously stated.

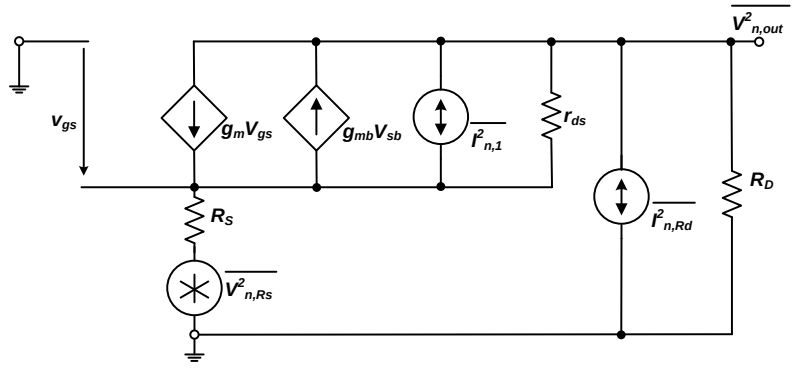

Figure 2.18 – Incremental CG model with respective noise sources.

The main noise contributors for the output total noise power are the same as in the CS case. Therefore, by inspection, one can identify the transistor's conduction channel thermal noise current, $\overline{I_{n,1}^2}$, the load resistance equivalent thermal noise current, $\overline{I_{n,R_D}^2}$ and the input signal's Thévenin equivalent thermal noise voltage source, $\overline{V_{n,R_s}^2}$ as being [34]:

$$\overline{V_{n1,out}^2} = 4kT\gamma g_m \left(\frac{r_{ds}R_D}{r_{ds} + R_D + R_S(r_{ds}(g_m + g_{mb}) + 1)}\right)^2 \tag{2.23}$$

$$\overline{V_{nR_D,out}^2} = 4kTR_D \left(\frac{r_{ds}}{r_{ds} + R_D + R_S(r_{ds}(g_m + g_{mb}) + 1)}\right)^2 \tag{2.24}$$

$$\overline{V_{nR_S,out}^2} = 4kTR_S \left(\frac{(g_m + g_{mb})R_D r_{ds} + 1}{r_{ds} + R_S(r_{ds}(g_m + g_{mb}) + 1) + R_D}\right)^2 \tag{2.25}$$

The total output noise power can then be contemplated as the sum of all noise sources, as in (2.11), providing they are all uncorrelated from each other.

At higher frequencies this configuration becomes significantly more complex than the previous. In Fig. 2.19 the high frequency incremental model of the CG configuration is presented, showing its most preponderant parasitic capacities.

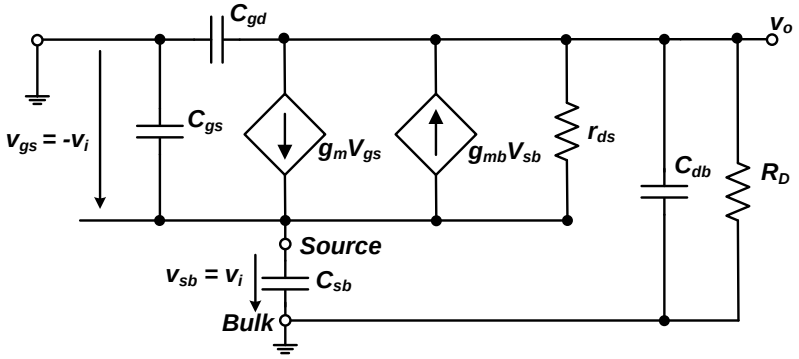

Figure 2.19 – High frequency incremental model of the CG configuration.

In order to simplify the schematic, a few equivalencies can be made. Note that capacities C_{gs} and C_{sb} are connected to the same two nodes and can be replaced by an equivalent capacity $C_S = C_{gs} + C_{sb}$. Likewise, the same can be made to C_{gd} and C_{db} resulting $C_L = C_{gd} + C_{db}$. A further simplification can be made if one takes into account an equivalent impedance, Z_L, that comprehends the parallel between R_D and C_L as Fig. 2.20 suggests [34].

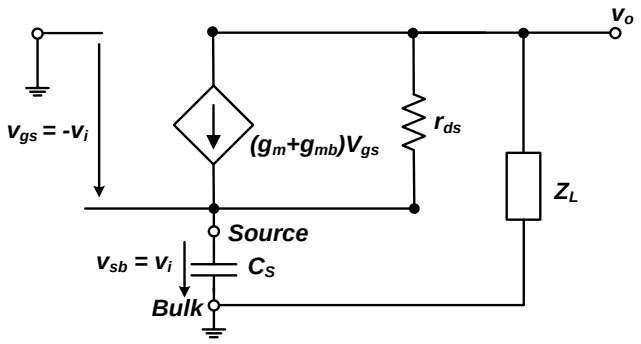

Figure 2.20 – Simplified model for the high frequency CG stage.

Thus, Z_L can be written in the following form:

$$Z_L = R_D || \frac{1}{sC_L} = \frac{R_D}{1 + sR_D C_L} \tag{2.26}$$

The high frequency gain can be easily obtained if KCL is applied to both input and output nodes resulting in

$$A_v(s) = \frac{V_o(s)}{V_i(s)} = \frac{R_D(r_{ds}(g_m + g_{mb}) + 1)}{sC_L r_{ds} R_D + r_{ds} + R_D} \tag{2.27}$$

Regarding the high frequency input impedance, a simplified version of it can be found.

$$Z_{in} = \frac{V_i(s)}{I_i(s)} = \frac{r_{ds} + Z_L}{sC_S(r_{ds} + Z_L) + r_{ds}(g_m + g_{mb}) + 1} \tag{2.28}$$

2.3.3. *Common-Gate Transimpedance Amplifier*

The CG TIA uses the CG configuration in order to accomplish, not only a transimpedance gain, but also current-to-voltage conversion. The output voltage of this TIA will be a function of its input current. Fig. 2.21 shows the configuration of the CG TIA in which the input current is the one provided by the PSD.

Transistor M_1 is biased by voltage V_B and current I_B. In this case, the load impedance, R_X, can have a high enough value, presenting a parasitic capacitance, C_X, in parallel with it. In order to find the transimpedance gain of this configuration, the small-signal model, present in Fig. 2.22, must be analyzed.

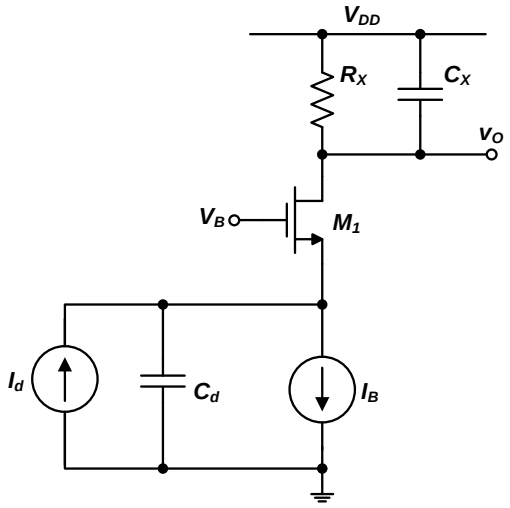

Figure 2.21 – Schematic of the CG TIA topology.

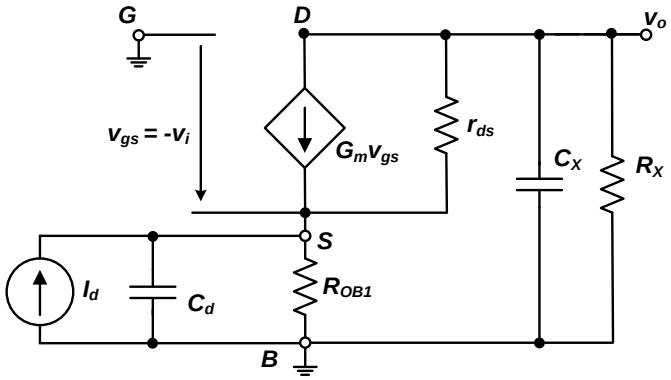

Figure 2.22 – Incremental model of the CG TIA.

Since C_d and C_X are estimated to be much larger than the parasitic capacitances of the MOS device, it is safe to neglect the latter ones. Resistor R_{oB1} stands for the biasing current source, I_{B1}, dynamic impedance, which is negligible in the derivation of the transimpedance function, since it is in parallel with the TIA low frequency input impedance, expressed by (2.21). In order to simplify the equation, the total transconductance of the MOS device will be expressed as

$$G_m = g_m + g_{mb} \tag{2.29}$$

and the load impedance will be

$$Z_X = R_X || \frac{1}{sC_X}. \tag{2.30}$$

The transimpedance function can then be obtained by applying KCL to the input and output nodes. In the input node, neglecting R_{OB1} the following will be obtained.

$$I_d = -v_{gs}(G_m + sC_d) + (v_{gs} + V_o)r_{ds}^{-1} \tag{2.31}$$

Providing that $G_m \gg r_{ds}^{-1}$ the latter can be expressed in the form:

$$I_d = -v_{gs}(G_m + sC_d) + V_o r_{ds}^{-1} \tag{2.32}$$

In the output node, again with the aid of KCL, the equation that characterizes it will be

$$G_m v_{gs} + (v_{gs} + V_o)r_{ds}^{-1} + V_o Z_X^{-1} = 0 \tag{2.33}$$

By taking into account that the conduction channel equivalent resistance can be made $r_{ds} \gg R_X$, will result in the following equivalency:

$$v_{gs} = -\frac{1}{Z_X G_m} V_o. \tag{2.34}$$

Substituting (2.34) in (2.32) the input node expression will only be dependent on the output voltage, therefore it will be

$$I_d = V_o r_{ds}^{-1} + \frac{1}{Z_X G_m}(G_m + sC_d)V_o \tag{2.35}$$

and if the condition $G_m \gg r_{ds}^{-1}$ is valid, will result in

$$\frac{I_d}{V_o} = \frac{1 + sG_m^{-1}C_d}{Z_X} \tag{2.36}$$

The transimpedance function of the CG TIA can then be found by substituting (2.30) in (2.36) and corresponds accurately to (2.4),

$$\frac{V_o}{I_d} = \frac{R_X}{(1 + sG_m^{-1}C_d)(1 + sR_X C_X)} \tag{2.37}$$

in which $R_m = R_X$, $\tau_1 = G_m^{-1}C_d$ and $\tau_2 = R_X C_X$.

Regarding a noise analysis, three major noise contributors can be identified in the form of noise current sources [8]. These will be the thermal noise originated by the load resistor R_X, $\overline{I_{n,R_X}^2}$,

the transistor's conduction channel thermal noise current, $\overline{I_{n,1}^2}$, and the biasing current source equivalent noise, $\overline{I_{n,B}^2}$, as represented by Fig. 2.23. Note that for calculating the biasing current source noise spectral density, it is assumed that the current source is accomplished by using a transistor operating in the saturation region, with constant V_{GS} and with transconductance g_{mB}. The respective noise spectral densities are:

$$\overline{I_{n,R_X}^2} = 4kTR_X^{-1} \tag{2.38}$$

$$\overline{I_{n,1}^2} = 4kT\gamma G_m \tag{2.39}$$

$$\overline{I_{n,B}^2} = 4kT\gamma g_{mB} \tag{2.40}$$

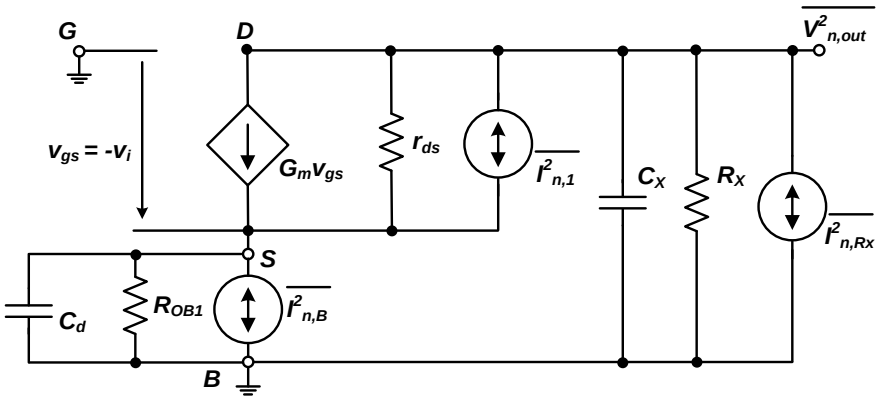

Figure 2.23 – Incremental model of the CG TIA with its thermal noise contributors.

The flicker noise is, once again, being neglected because of the wideband nature of the application. By analyzing the incremental circuit one can identify the noise transfer function each source produces. This topology is well known and, for that reason, there is no need to show the deduction of each transfer function. Therefore the contribution of the drain resistor follows

$$v_{no,R_X} = Z_X I_{n,R_X} = \frac{R_X}{1 + s\tau_2} I_{n,R_X} \tag{2.41}$$

in which Z_X is given by (2.30) and $\tau_2 = R_X C_X$. Regarding the conduction channel thermal noise, its effect on the noise transfer function shows a medium frequency zero dependent on the time-constant $\tau_z = R_{oB} C_d$ [8] where R_{oB} is the dynamic impedance of the biasing current source. From this and knowing that with a SiPM C_d is high valued, one can already conclude that this zero will

cause the noise to rise sooner than with an APD. In practical terms this means that the output noise will have a higher spectral density with the SiPM than with the APD.

$$v_{no,1} = -\frac{R_X}{G_m R_{oB}} \frac{1 + s\tau_z}{(1 + s\tau_1)(1 + s\tau_2)} \tag{2.42}$$

Finally, the noise current source referent to R_{oB} has the same input port as the TIA's input signal and, therefore, the same transfer function:

$$v_{no,B} = \frac{R_X}{(1 + s\tau_1)(1 + s\tau_2)} \tag{2.43}$$

The output noise voltage in rms can be found by using the derivations taken in [8], where a generalized two-pole and one-zero noise transfer function has been deducted. The output voltage can then be expressed in its rms value as follows

$$V_{no,rms}^2 = \frac{R_X^2}{\tau_2}\frac{1}{4}\overline{I_{n,R_X}^2} + \frac{R_X^2}{\tau_1 + \tau_2}\frac{1}{4}\overline{I_{n,B}^2} + \frac{R_X^2}{G_m^2 R_{oB}^2}\frac{1}{\tau_1 + \tau_2}\left(1 + \frac{\tau_z^2}{\tau_1\tau_2}\right)\frac{1}{4}\overline{I_{n,1}^2}. \tag{2.44}$$

Since $\tau_z = R_{oB}C_d$ reflects a low frequency zero, it is natural that $\tau_z^2 \gg \tau_1\tau_2$ and by using $\tau_1 = G_m^{-1}C_d$ the above can be expressed in

$$V_{no,rms}^2 = \frac{R_X^2}{\tau_2}\frac{1}{4}\overline{I_{n,R_X}^2} + \frac{R_X^2}{\tau_1 + \tau_2}\frac{1}{4}\overline{I_{n,B}^2} + \frac{R_X^2}{\tau_1 + \tau_2}\frac{\tau_1}{\tau_2}\frac{1}{4}\overline{I_{n,1}^2} \tag{2.45}$$

The last term in the expression is dominant if τ_1 and τ_2 have the same order of magnitude and $G_m \gg R_X^{-1}$ and $G_m \gg g_{mB}$.

Due to the low frequency zero and high frequency poles, the noise transfer function will present a peak in its response. This can be attenuated at the cost of the output signal peaking time, if one takes notice that the output noise is proportional to G_m, i.e., knowing that $\tau_1 = G_m^{-1}C_d$ it can be seen that by lowering G_m the noise is reduced but the transimpedance function will reflect a slower response.

2.3.4. *Feedback Transimpedance Amplifier*

The feedback TIA is the most widely used configuration when current-to-voltage conversion is required [8]. The advantage of this topology relies on the fact that it presents a

better noise-headroom tradeoff than its counterpart CG TIA topology [12], as it will be further seen. Ideally, in its most basic form, this topology consists in using an OpAmp with negative feedback, in a lossy integrator-like configuration [11], as Fig. 2.24 illustrates. The feedback path is composed by the parallel between R_f and C_f, while the input current signal is applied directly to the node connecting the OpAmp inverting input and the feedback path. The OpAmp assumed here is non-ideal, which means that its low frequency gain A_{v0} is limited, as well as its GBW.

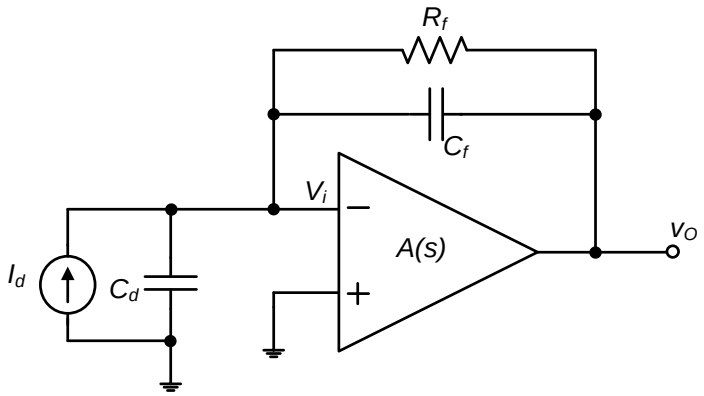

Figure 2.24 – Feedback TIA Basic configuration.

The amplifier's GBW is limited by a dominant pole, ω_{pa} referent to a time-constant τ_a. Thus its open-loop gain can be expressed by

$$A_v(s) = \frac{A_{v0}}{1 + s\tau_a} \tag{2.46}$$

in which A_{v0} is the OpAmp low frequency open-loop gain. The GBW of the amplifier can then be expressed as follows:

$$B = \frac{A_{v0}}{\tau_a}. \tag{2.47}$$

Even though limited, the influence of a low value GBW can be negligible if greater than the remaining time-constants present in the circuit. As a worst-case scenario, we present the case where the GBW has a value comparable to the remaining time-constants of the circuit, which is highly undesirable.

The transimpedance function can be easily found by analyzing the circuit presented in Fig. 2.24, where

$$V_o\left(1+\frac{1}{A_v}\right)\left(\frac{1}{R_f}+sC_f\right)+\frac{V_o}{A_v}sC_d=-I_d. \tag{2.48}$$

If one takes notice that $A_{v0} \gg 1$ then (2.48) can be simplified into

$$\frac{V_o}{I_d}=\frac{R_f}{s^2R_fC_dB^{-1}+s\left(R_f\left(C_f+C_dA_{v0}^{-1}\right)+B^{-1}\right)+1} \tag{2.49}$$

which corresponds to this topology's transimpedance function. If the denominator of (2.49) is compared to (2.4) which, in turn, can be written in the form

$$(1+s\tau_1)(1+s\tau_2)=s^2\tau_1\tau_2+s(\tau_1+\tau_2)+1 \tag{2.50}$$

the values of the feedback resistor and capacitor can be found and, as such, it can be easily seen that they are both dependent on the gain-bandwidth product,

$$C_f=\frac{k-A_{v0}^{-1}}{1-k}C_d \tag{2.51}$$

$$R_f=\frac{\tau_1\tau_2}{B^{-1}C_d}\frac{1-k}{1-A_{v0}^{-1}} \tag{2.52}$$

where,

$$k=\frac{\tau_1+\tau_2+B^{-1}}{B\tau_1\tau_2}. \tag{2.53}$$

From the above it can be seen that maintaining the same GBW, the value of the low frequency transimpedance gain, R_f, will decrease as C_d increases. This is important in the sense that with limited GBW the feasibility of the TIA with a high capacity PSD, such as a SiPM, becomes ineffective. In a practical sense, the fact that R_f is low valued with the SiPM means that the output signal amplitude will be very low, while maintaining the same noise level, as will be seen further on. This will make the SNR lower and non-suitable for the application it is designed for. Another factor to account for, is the fact that since C_f is proportional to C_d, the first will have to be at least one order of magnitude higher, occupying a larger area, in order for V_o to maintain the same rising time.

In the matter of noise response it is assumed that the noise produced by the OpAmp's input stage transistors have a dominant contribution. In such case it is safe to assume that the thermal noise generated within the OpAmp – or the equivalent thermal noise produced by the input stage transistor, $\overline{I_{n,1}^2}$ – can be represented by an equivalent noise voltage source, $\overline{V_{n,1}^2}$, connected to the gate of that input stage transistor as Fig. 2.25 suggests.

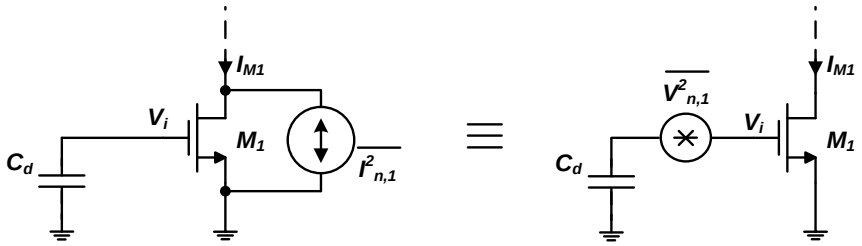

Figure 2.25 – Equivalency between the OpAmp's input stage thermal noise contribution.

This thermal noise voltage source has a spectral density equal to the one of the thermal noise current source divided by the device's squared transconductance, which can be represented by

$$\overline{V_{n,1}^2} = 4kT\gamma g_{m1}^{-1} \tag{2.54}$$

where g_{m1} refers to the input stage equivalent transconductance. The noise present in the feedback TIA can be reduced to an equivalent thermal noise voltage source, $\overline{V_{n,a}^2} = \overline{V_{n,1}^2}$, connected to the input of the amplifier's inverting input as Fig. 2.26 shows.

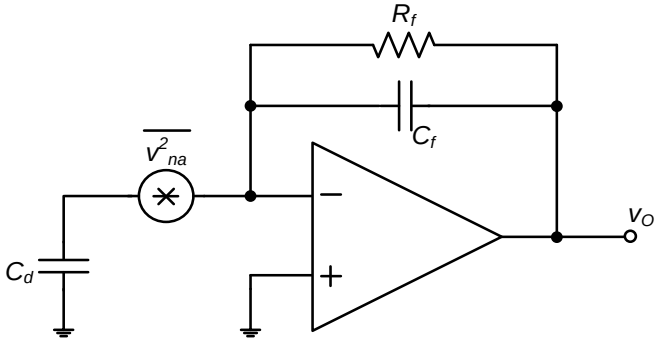

Figure 2.26 – Feedback TIA with its thermal noise voltage source.

The noise transfer function of the feedback TIA has already been extensively studied [8], [12], and follows the form

$$V_{no,rms}^2 = \frac{R_f^2 C_d^2 kT}{g_{m1}(\tau_1 + \tau_2)\tau_1\tau_2} \tag{2.55}$$

Concerning Flicker $(1/f)$ noise, since the TIA is wideband, its contribution can be, once again, neglected. In order to minimize the noise level in the TIA's output, it can be seen from (2.55) that g_{m1} must be high, since the latter is inversely proportional to the first. The contribution of R_f to the total output integrated noise between 1 kHz and 1 GHz can also be deducted but, since the dc current that passes through it is relatively small, its noise contribution can be made negligible if the resistor is high valued [12].

3. THE REGULATED COMMON-GATE TRANSIMPEDANCE AMPLIFIER

The RCG TIA consists in a two-stage amplifier composed by a CG and a CS stage. This topology can be seen as a CG TIA with G_m boosting, where a voltage-gain block is inserted in order to provide some feedback regulation to the CG stage. This configuration is widely used in Low-Noise Amplifiers (LNAs), which is motivated by its capacity for showing relatively low Noise Figure (NF) and, even though it is not the case presented here, noise canceling possibility [34], [35], if used in a certain differential structure. Comparing to the CG and feedback TIA, the usage of this topology is a more promising solution since, as will be seen, it can be suitable for higher output capacitance devices, such as the SiPM.

In the present chapter there will be three major sections where the transimpedance and noise transfer functions will be studied. Initially, the RCG TIA basic circuit will be presented, following a circuit variation with improved noise distribution. Lastly, the possibility of differential output will be considered. It must be noted that because of the requirement for the output voltage to reach an amplitude of $V_{om} = 1\,\mathrm{V}$, the output of the TIA must be connected to a Voltage-Controlled Voltage Source (VCVS) post-amplifier, with a passing band high enough so it does not influence the behavior of the TIA. This VCVS's voltage gain, H, is omitted in the transfer functions derivation for simplicity. One can account for the voltage post-amplifier gain block, H, simply by multiplying it by any of the transfer functions derived, regardless the nature of the latter (transimpedance or noise transfer function). This will result in the same ratio between the output signal and noise generated at the output of the TIA, i.e., approximately same SNR, if the VCVS is low noise. Note still that in the case of a hypothetical differential TIA output, the voltage post-amplifier VCVS must be fully differential in order to balance the system's output voltage.

3.1. BASIC REGULATED COMMON-GATE TIA

The RCG TIA, also known as "Regulated Cascode" [36] or "g_m-boosted Common-Gate" stage [37] is a circuit derived from the CG amplifier stage. Basically, it consists in the circuit depicted in Fig. 3.1, in which the common-gate stage – comprising transistor M_1, biasing current source I_{B1} and load resistor R_X – has a common-source voltage amplifier, accomplished by M_2 and biasing current source I_{B2}, connected between the source and the gate of the first. The main objective of this configuration is to achieve a lower input impedance than the one of a CG stage, which will now be divided by the CS stage low frequency gain [7]. In Fig. 3.1 the basic RCG TIA is shown contemplating, already, the input signal current source and respective capacitance.

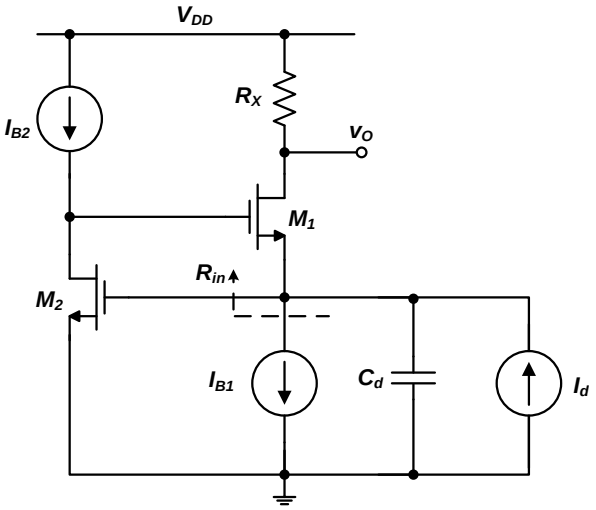

Figure 3.1 – Schematic of the basic RCG TIA circuit.

Considering the incremental model, biasing current sources I_{B1} and I_{B2} have large dynamic impedances, R_{OB1} and R_{OB2} respectively, and therefore, even though they are shown in the incremental model, can be neglected in the derivation of the expressions that characterize the circuit. The first, I_{B1}, is in parallel with M_1's low input impedance, while the latter is in parallel with M_2's r_{ds}, which is expected to be of much lower value. In practical terms this means that

$$R_{o2} = R_{OB2} || r_{ds2} \cong r_{ds2} \tag{3.1}$$

and

$$R_{o1} = R_{OB1} || R_{in} \cong R_{in} \cong \frac{1}{g_{m1} A_{v0}} \tag{3.2}$$

in which g_{m1} is M_1's transconductance and A_{v0} is the CS stage low frequency gain. The incremental model of the basic RCG TIA is shown in Fig. 3.2.

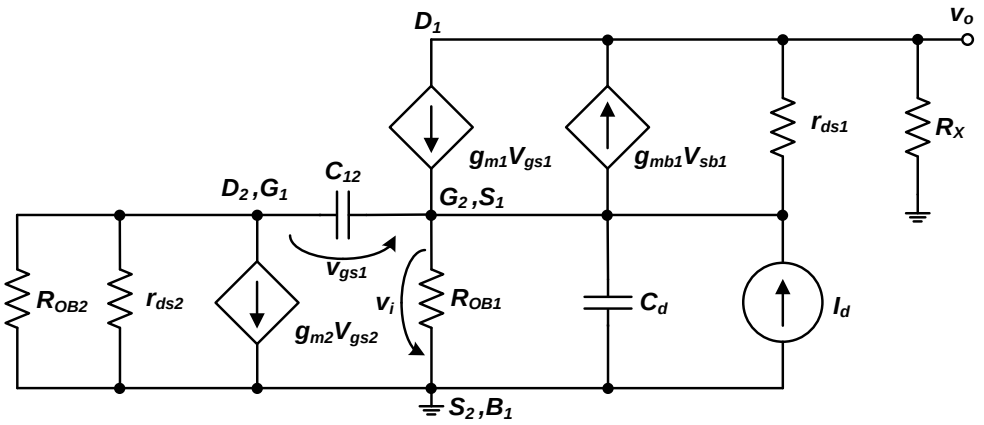

Figure 3.2 – Incremental model of the basic RCG TIA.

By considering the incremental circuit, it becomes necessary to contemplate that transistor M_2 will have to be very wide so it can, not only give the expected amount of gain, but also raise M_2's transconductance in order to lower the output integrated noise, as will be seen further on. Thus, it also becomes necessary to notice that C_{gd2} will influence the circuit's response in some way since it is proportional to the width of that device. This will imply that there will be a capacity between the gate and drain of M_2, in the feedback loop, given by

$$C_{12} = C_{gs1} + C_{gd2}. \tag{3.3}$$

Capacitance C_{gs2} could be contemplated in parallel with C_d. However given the magnitude of C_d, it can be made negligible. Considering that it is aimed for g_{m2} to be high, this implies that, with respect to the transconductance of the MOS device in saturation region [31],

$$g_{m2} = \frac{2I_{B2}}{V_{DSAT2}} \tag{3.4}$$

where V_{DSAT2} represents the overdrive voltage of M_2, the current flowing through the drain of M_2, I_{B2}, will also be high. Thus, since r_{ds2} is inversely proportional, it is expected that (3.1) is kept fulfilled. Respecting (3.1) and (3.2) one can apply KCL to node denoted by D_2, G_1, resulting

$$\frac{V_{gs1}}{V_i} = -\frac{g_{m2} + r_{ds2}^{-1}}{r_{ds2}^{-1} + sC_{12}} \tag{3.5}$$

where $V_i = V_{gs2}$. Since g_{m2} must be high, it is safe to assume that $g_{m2} \gg r_{ds2}^{-1}$ which, in turn, can be easily proven if M_2's intrinsic gain is $g_{m2}/g_{ds2} \gg 1$. Thus, (3.5) can be written as

$$\frac{V_{gs1}}{V_i} = -\frac{g_{m2}r_{ds2}}{1 + sr_{ds2}C_{12}} = -\frac{A_{v0}}{1 + s\tau_a} = -A \tag{3.6}$$

where $A_{v0} = g_{m2}r_{ds2}$ is M_2 's low frequency gain and $\tau_a = r_{ds2}C_{12}$ is the time-constant associated to the pole inserted by C_{12}. It may be useful to write (3.6) in the form

$$V_i = -A^{-1}V_{gs1}. \tag{3.7}$$

At this point, it becomes important to mention that, in this configuration, the body effect in M_1can be neglected [38]. Since $V_{sb1} = V_i$ and taking (3.7) into account, in the passing band V_i is A_{v0} times inferior to V_{gs1}. Therefore, the current that results from the body effect, which by itself is already relatively small, becomes even smaller, becoming, this way, negligible.

By taking (3.7) into account and applying KCL in the node G_2, S_1 the input current can be expressed by

$$I_d = V_{gs1}sC_{12} - V_isC_d - V_oR_X^{-1} \tag{3.8}$$

which will result in the following, if (3.7) is considered

$$I_d = V_{gs1}(sC_{12} + A^{-1}sC_d) - V_oR_X^{-1}. \tag{3.9}$$

In the node D_1, one can find a relation between V_{gs1} and V_o. Here, after rearranging, and noticing that $Ag_{m1}r_{ds1} \gg 1$, by KCL the relation can be expressed by

$$V_{gs1} = -V_og_{m1}^{-1}(r_{ds1}||R_X)^{-1}. \tag{3.10}$$

This permits for (3.9) to be rewritten in the form

$$I_d = -V_og_{m1}^{-1}(r_{ds1}||R_X)^{-1}(sC_{12} + A^{-1}sC_d) - V_oR_X^{-1}. \tag{3.11}$$

The resulting transimpedance function can easily be found through (3.11), resulting

$$\frac{V_o}{I_d} = -\frac{R_X}{g_{m1}^{-1}\left(\frac{R_X}{r_{ds1}}+1\right)(sC_{12}+A^{-1}sC_d)+1}. \tag{3.12}$$

By using (3.6), (3.2) and rearranging the expression the transimpedance function can be written as

$$\frac{V_o}{I_d} = -\frac{R_X}{s^2\tau_a\tau_i(\beta+1)+s\tau_i(\beta+1)(\eta+1)+1} \tag{3.13}$$

where $\tau_i = g_{m1}^{-1}A_{v0}^{-1}C_d$ is the time-constant resultant from the PSD's output capacity and the TIA's input impedance and $\eta = A_{v0}C_{12}C_d^{-1}$ is the relation between the PSD's output capacity and the miller capacity present at the TIA input. The factor β stands for the relation between R_X and r_{ds1}. The value of r_{ds1} is, ideally, much higher than R_X. This means that ideally, β must be close to zero, so r_{ds1} will not be able to influence the TIA's low frequency gain, since the lower r_{ds1} is, the lower the transimpedance gain will be.

In order to find a quality factor for the TIA and a differentiation factor for the transimpedance function poles, one can write (3.13) in the following form [7]

$$\frac{V_o}{I_d} = -\frac{\frac{1}{\tau_a\tau_i(\beta+1)}}{s^2+s\frac{\eta+1}{\tau_a}+\frac{1}{\tau_a\tau_i(\beta+1)}} \tag{3.14}$$

from which results

$$Q = \frac{1}{\eta+1}\sqrt{\frac{\tau_a}{\tau_i(\beta+1)}} = \frac{1}{2} \tag{3.15}$$

This means that if $Q < 0.5$ the poles are real, if $Q > 0.5$ the poles are complex conjugate and, finally, if $Q = 0.5$ the poles are real and equal. The amplifier's natural frequency follows

$$\omega_0^2 = \frac{1}{\tau_a\tau_i(\beta+1)}. \tag{3.16}$$

By comparing the transimpedance function to a canonical second-order transfer function, the damping factor can be found and can be expressed by

$$\xi = \frac{\eta + 1}{2}\sqrt{\frac{\tau_i(\beta + 1)}{\tau_a}} = \frac{1}{2Q}. \tag{3.17}$$

The gain-bandwidth product of this topology is the one of M_2's CS stage [7], set by C_{12}, with value

$$B = \frac{A_{v0}}{\tau_a} = \frac{g_{m2}}{C_{12}} \tag{3.18}$$

Regarding a noise analysis in the basic RCG TIA, shown in Fig. 3.1, only the thermal noise originated by transistors M_1 and M_2 is considered. The flicker noise can be neglected given the wideband nature of the circuit. Likewise, the thermal noise originated by the biasing current sources can be made negligible if these are properly designed. As it will be proven by the simulation results, the noise contribution of M_2 will be dominant, making way for the remaining thermal noise sources to be neglected. One thermal noise source that could be considered is the one originated by the load resistor, R_X. However, accounting for a parasitic capacitance in parallel with it, will make its noise contribution negligible. Thus, in Fig. 3.3 the incremental model containing the thermal noise sources is considered. For simplicity only M_1 and M_2 thermal noise current sources are considered.

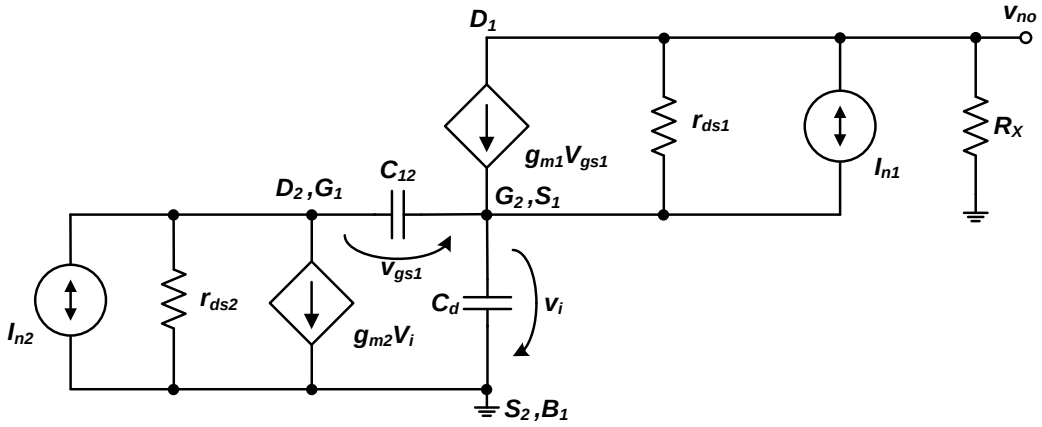

Figure 3.3 – Basic RCG TIA incremental model with dominant current sources.

Starting with I_{n1}, its influence can be found by applying KCL to node G_2, S_1. Thus, it will be

$$v_{gs1}sC_{12} = v_i sC_d + V_{no}R_X^{-1} \tag{3.19}$$

and, respecting (3.7), the latter can be written as

$$v_i = -V_{no}\frac{R_X^{-1}}{s(A_v C_{12} + C_d)}. \tag{3.20}$$

The expression that characterizes node D_1, again applying KCL, can be written as

$$I_{n1} = g_{m1}v_{gs1} + (V_{no} - v_i)r_{ds1}^{-1} + V_{no}R_X^{-1} \tag{3.21}$$

and, by applying (3.7), knowing that $r_{ds1} \gg R_X$ and $A_v g_{m1} \gg r_{ds1}^{-1}$will result in

$$I_{n1} = -v_i A_v g_{m1} + V_{no}R_X^{-1}. \tag{3.22}$$

By using (3.20) into the above, one can find the relation between I_{n1} and V_{no}

$$I_{n1} = \frac{A_v g_{m1} + s(A_v C_{12} + C_d)}{sR_X(A_v C_{12} + C_d)}V_{no}. \tag{3.23}$$

By rearranging (3.23) one can find the contribution of I_{n1} into the noise transfer function, following:

$$\frac{V_{no}}{I_{n1}} = R_X\frac{sA_{v0}^{-1}g_{m1}^{-1}C_d(\eta+1) + s^2A_{v0}^{-1}g_{m1}^{-1}C_d r_{ds2}C_{12}}{1 + sA_{v0}^{-1}g_{m1}^{-1}C_d(\eta+1) + s^2A_{v0}^{-1}g_{m1}^{-1}C_d r_{ds2}C_{12}} \tag{3.24}$$

which, in turn, can be written in the form

$$\frac{V_{no}}{I_{n1}} = R_X\frac{s^2\tau_i\tau_a + s\tau_i(\eta+1)}{s^2\tau_i\tau_a + s\tau_i(\eta+1) + 1} \tag{3.25}$$

where the time-constants are the same as in the transimpedance function. In order to give a better insight into (3.25), I_{n1}'s contribution can be expressed as

$$\frac{V_{no}}{I_{n1}} = R_X\frac{s\tau_1(s\tau_2+1)}{s^2\tau_1\tau_2 + s\tau_1 + 1} \tag{3.26}$$

in which

$$\tau_1 = \tau_i(\eta+1), \tag{3.27}$$

$$\tau_2 = \frac{\tau_a}{\eta + 1}. \tag{3.28}$$

From (3.26) it can be seen that I_{n1}'s contribution is of high-pass nature. This could lead one to assume that I_{n1} would have a dominant contribution, since it would only be limited by parasitic capacities not contemplated in Fig. 3.3. However, it was found that in the bandwidth we are interested in, the noise generated by M_2 will have a much higher contribution to the total output noise, as validated by the simulations taken.

Regarding I_{n2}, one can find its contribution by analyzing the circuit in Fig. 3.3. Thus, applying KCL to node $D_1$and taking the approximation $r_{ds1} \gg R_X$ into account, will result in

$$v_{gs1} = v_i g_{m1}^{-1} r_{ds1}^{-1} - V_{no} g_{m1}^{-1} R_X^{-1}. \tag{3.29}$$

In node S_1, G_2 it will be

$$v_{gs1} s C_{12} = v_i s C_d + V_{no} R_X^{-1}. \tag{3.30}$$

Replacing (3.29) in (3.30) and knowing that

$$C_d \gg C_{12} g_{m1}^{-1} r_{ds1}^{-1}, \tag{3.31}$$

will result in

$$v_i = -\frac{R_X^{-1}}{s C_d}(1 + s g_{m1}^{-1} C_{12}) V_{no}. \tag{3.32}$$

Finally, in node D_2, G_1, using KCL the following can be obtained

$$-I_{n2} = \left(v_{gs1} + v_i\right) r_{ds2}^{-1} + g_{m2} v_i + v_{gs1} s C_{12} \tag{3.33}$$

and replacing (3.30) and (3.32) into (3.33) it will be obtained

$$\begin{aligned} I_{n2} = \frac{1}{s C_d}(1 + s g_{m1}^{-1} C_{12})\left[g_{m2} + \left(r_{ds2}^{-1} + s C_{12}\right) g_{m1}^{-1} r_{ds1}^{-1}\right] V_{no} R_X^{-1} \\ + \left(r_{ds2}^{-1} + s C_{12}\right) g_{m1}^{-1} V_{no} R_X^{-1}. \end{aligned} \tag{3.34}$$

Rearranging and taking (3.31) and the fact that $g_{m2} \gg r_{ds2}^{-1}$ into account, will allow for the contribution of I_{n2} to be expressed as

$$\frac{V_{no}}{I_{n2}} = R_X \frac{s\tau_z}{s^2\tau_i\tau_a + s\tau_i(\eta + 1) + 1} \tag{3.35}$$

where

$$\tau_z = g_{m2}^{-1} C_d. \tag{3.36}$$

In order to find the output noise rms voltage (3.35) can be written in the form

$$\frac{V_{no}}{I_{n2}} = R_X \omega_0 \tau_z \frac{s\omega_0}{s^2 + s\omega_0 Q^{-1} + \omega_0^2} \tag{3.37}$$

In which ω_0 and Q are referred to (3.16) and (3.15), respectively. Following [7], and providing that I_{n2} is dominant over I_{n1}, will allow for the noise transfer function to be written as

$$V_{no,rms}^2 = \frac{1}{4} \overline{\iota_{n2}^2} R_X^2 \omega_0^2 \tau_z^2 \omega_0 Q. \tag{3.38}$$

Considering (2.39), (3.36) and (3.38), the final form for the output noise rms voltage can be expressed through

$$V_{no,rms}^2 = kT \frac{R_X^2 C_d^2}{g_{m2}} \omega_0^3 Q \tag{3.39}$$

Note that (3.39) is only true if I_{n2} is the dominant noise source present in the circuit [7]. For the application under study, it is estimated that I_{n1} will have a high-pass frequency response limited by parasitic capacities and, in its passing band, it will have a much lower contribution than I_{n2}. Therefore, when simulating the noise level present at the output of the circuit, the total integrated noise was only taken into account until 1 GHz, proving that I_{n2} is effectively the dominant noise source.

3.2. IMPROVED NOISE DISTRIBUTION

In this section the noise of the RCG TIA is reduced. Basically, it is expectable that the circuit's SNR will be raised by lowering the noise originated by M_2, maintaining the same output

voltage amplitude. Similarly to the previous section, the transimpedance function of the circuit with the proposed improvement will be deducted following a noise analysis.

Relatively to the basic RCG TIA, discussed in the previous section, the change is the placement of a MOS transistor, M_3, with its biasing current source, I_{B3}, connected between the drain of M_2 and V_{DD} [35], as suggested in Fig. 3.4. With the insertion of this configuration, it is to be expected that M_2's contribution to the total output integrated noise will be lower. Note that transistor M_3 has a small current passing through it and, therefore, its transconductance, g_{m3}, will also be small. This means that, with respect to (2.39), its noise contribution can be made negligible.

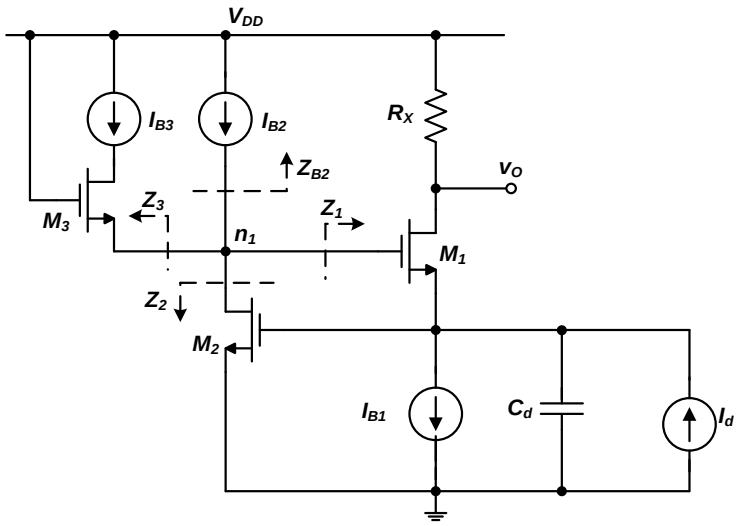

Figure 3.4 – RCG TIA with M_3 and I_{B3} auxiliary noise improvement.

The equivalent impedance in node n_1, Z_{n1}, corresponds to the parallel between Z_2 and Z_3, if one takes into account that Z_1 and Z_{B2} are ideally infinite, and thus negligible. One immediate conclusion that can be retrieved out of this is the fact that the regulation stage's low frequency gain, A_{v0}, will now be different. Instead of the one given by (3.6), M_2's configuration low frequency gain will now be influenced by the configuration presented by M_3, following

$$A_{v0} = g_{m2}(Z_2||Z_3) \tag{3.40}$$

In order to find a meaning for Z_3 one can analyze its incremental circuit, depicted in Fig. 3.5. Here it becomes important to notice that since M_2's configuration must present high gain, it will also present a drain-to-source voltage, V_{DS2}, relatively high. Therefore, there will be left little room for M_3 and I_{B3} active devices' V_{DS}. In practical terms, this means that I_{B3} biasing current source may have to be designed working on the triode or saturation/triode boundary region, and as such, its equivalent dynamic impedance, R_{OB3} may be lower than the expected.

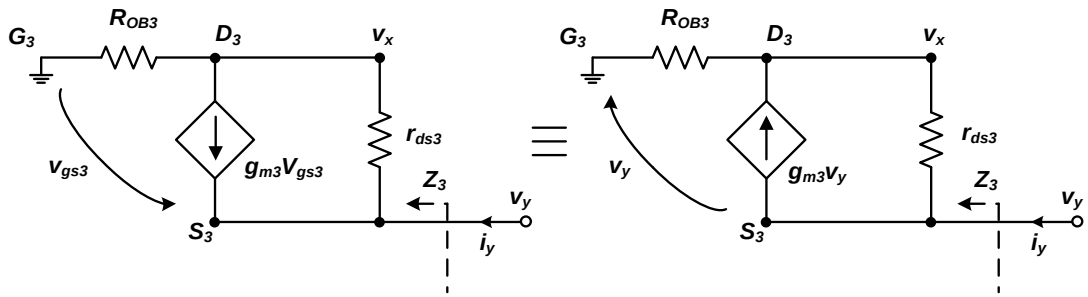

Figure 3.5 – M_3's configuration incremental model.

Regardless of its parasitic capacities, transistor M_3 has a low frequency output impedance that will follow

$$Z_3 = \frac{v_y}{i_y} = \frac{v_y}{v_y(g_{m3} + r_{ds3}^{-1}) - v_x r_{ds3}^{-1}}. \tag{3.41}$$

By applying KCL to node D_3 the following can be obtained

$$v_y g_{m3} = v_x R_{OB3}^{-1} + (v_x - v_y) r_{ds3}^{-1}. \tag{3.42}$$

If the approximations $g_{m3} \gg r_{ds3}^{-1}$ and $R_{OB3} \cong r_{ds3}$ are made, which mean M_3 is operating in saturation region, (3.42) will result in

$$v_x = g_{m3}(r_{ds3} || R_{OB3}) v_y = \frac{1}{2} g_{m3} r_{ds3} v_y \tag{3.43}$$

which, by substituting into (3.41) and again assuming $g_{m3} \gg r_{ds3}^{-1}$, will provide the impedance Z_3. Therefore,

$$Z_3 = 2 g_{m3}^{-1}. \tag{3.44}$$

Knowing the impedance in node n_1, originated by M_3 and its configuration, makes it possible to see the new incremental model of the RCG TIA, shown in Fig. 3.6. Here it can be seen that there will now be an impedance Z_3 in parallel with r_{ds2}, which can affect M_2's gain and frequency response. As will be further seen, by making g_{m3}^{-1} have the same order of magnitude of r_{ds2}, there will be an effect on the dominant poles of the circuit, altering the bandwidth and noise transfer function. In order to see the effect Z_3 has in the gain of the CS stage, one can apply KCL to node D_2, G_1, S_3, in which will result

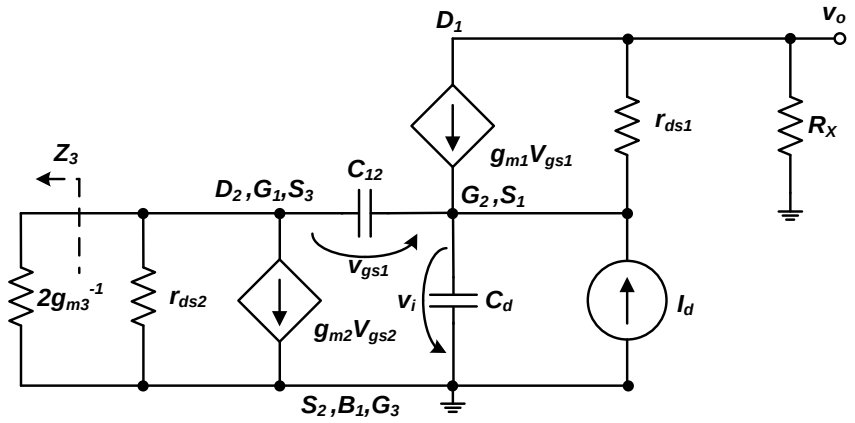

Figure 3.6 – RCG TIA incremental model with M_3's configuration equivalent impedance, Z_3.

$$v_{gs1}sC_{12} + g_{m2}v_i + \left(v_{gs1} + v_i\right)\left(r_{ds2}^{-1} + \frac{1}{2g_{m3}^{-1}}\right) = 0 \tag{3.45}$$

and since $r_{ds2} \cong g_{m3}^{-1}$, will result in the fact that $g_{m2} \gg r_{ds2}^{-1} + g_{m3}$. Therefore, (3.45) can be written in the form

$$v_{gs1}[sC_{12} + R_{23}^{-1}] = -g_{m2}v_i \tag{3.46}$$

where

$$R_{23} = r_{ds2}||2g_{m3}^{-1} \tag{3.47}$$

is the equivalent impedance between the parallel composed by Z_3 and M_2's conduction channel equivalent resistance, r_{ds2}. Respecting (3.46) and (3.47) the equation that characterizes the node can then be written as

$$v_{gs1} = -\frac{g_{m2}R_{23}}{1 + sR_{23}C_{12}}v_i \tag{3.48}$$

The equation (3.48) corresponds to the one shown in (3.6), only this time it will be

$$A_{v0} = g_{m2}R_{23} = g_{m2}(r_{ds2}||2g_{m3}^{-1}) \tag{3.49}$$

and

$$\tau_a = R_{23}C_{12} = (r_{ds2}||2g_{m3}^{-1})C_{12} \tag{3.50}$$

The remaining nodes are characterized by the same equations as the basic RCG TIA. Therefore, the transimpedance function will still be the one presented in (3.13). One immediate conclusion that can be derived from the transimpedance function is that the time-constants associated to the poles will now be different, respecting (3.49) and (3.50). Since R_{23} will, mandatorily, be lower than r_{ds2}, M_2's low frequency gain, A_{v0}, will also be lower, affecting the TIA's input impedance. The pole that gives M_2's configuration bandwidth, associated to τ_a, will be placed at a higher frequency, since τ_a will be lower. This could lead one to think that the passing band of the amplifier would be increased, resulting in more integrated overall noise. However, the pole originated by C_d and the TIA's input impedance, τ_i, will now be located at a lower frequency, f_{pi}, since it is proportional to A_{v0},as expressed by (3.51), which can mean that the amplifier's bandwidth will now be limited by τ_i instead of τ_a.

$$2\pi f_{pi} = \frac{1}{\tau_i} = \frac{A_{v0}g_{m1}}{C_d} \tag{3.51}$$

In order to fully understand the behavior of the noise imposed by M_2's thermal noise source – considering this one is the dominant noise source – one can analyze the incremental model of the amplifier with the contribution of Z_3 and I_{n2}. However, the influence of Z_3, and consequent R_{23}, has already been studied, while the incremental model will be the one presented in Fig. 3.3, with r_{ds2} replaced by R_{23}. Thus, the influence I_{n2} will have in the output noise voltage, v_{no}, will follow what was previously stated by (3.39).

Regarding the insertion of M_3 and I_{B3} in the circuit will let denote a decrease in the quality factor, Q, expressed by (3.15), motivated by the decrease of τ_a and the increase in τ_i, mentioned earlier. Since the output rms noise voltage is proportional to Q, naturally, it will also be decreased. Note that regarding the zero expressed in (3.35) and (3.36), τ_z, it will remain unaltered. The fact that the time-constant τ_i is now higher means that the zero will encounter the pole associated with τ_i earlier and, therefore, I_{n2}'s spectral density will be lower, presenting lower output noise voltage, since it will be filtered at a lower frequency.

3.3. DIFFERENTIAL OUTPUT RCG TIA

In the present section the RCG TIA with improved noise distribution, shown in section 3.2, will be changed in order to present differential outputs. The advantages of differential over single-ended circuits are well known and, as such, needless to be mentioned. Regardless, one of the most important advantages of turning the RCG TIA into differential resumes to the fact that the output signal amplitude will be able to present a higher voltage swing. This way, one can use a differential ADC, when converting the signal into digital thus, covering a higher output swing.

The proposed changes in the circuit are shown in Fig. 3.7 and, as can be seen, the inverted output is accomplished by using the signal present in node n_1. The CS stage composed by M_2's configuration inverts the incremental voltage of the TIA's input, v_i. The inverted output voltage, v_{o2}, can then be accomplished by amplifying the voltage present at node n_1, v_{n1}. In order to amplify v_{n1}, a CG stage was used composed by M_5, R_{X2} and I_{B4}. As seen before, in chapter 2.3, the CG configuration has low input impedance ($Z_5 \cong g_{m5}^{-1}$) and, as such, this could be problematic since Z_5 would appear in parallel with R_{23} lowering M_2 's configuration low frequency gain, A_{v0}. To prevent such a decrease in A_{v0}, a buffer was placed between node n_1 and M_5 configuration. The simplest way to achieve a buffer stage is to use the Common-Drain (CD), or Source Follower, configuration [31], [33]. This configuration has the characteristic of presenting very high input impedance, low output impedance and a voltage gain close to unity. The CD stage is accomplished by transistor M_4 and current source I_{B4}. Note that I_{B4} is shared between M_4 and M_5 configurations, in an overall configuration resembling a differential pair, or a differential-to-single ended converter.

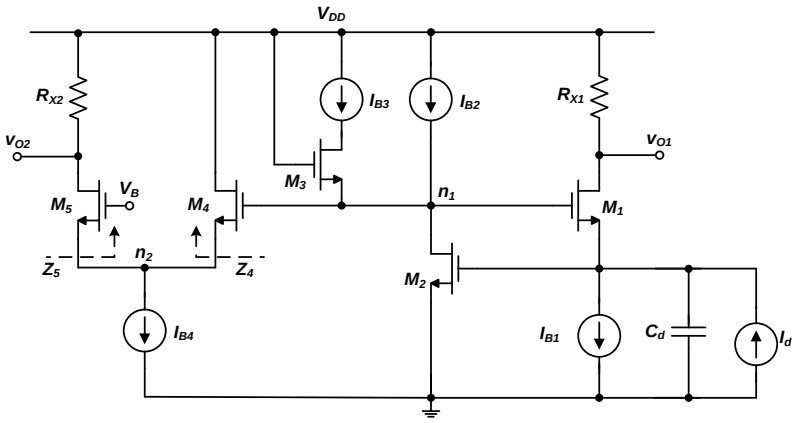

Figure 3.7 – Proposed differential output RCG TIA.

One immediate, apparent, difficulty in realizing the circuit described above, would be related to the number of cascaded amplifying stages present between the input signal, I_d, and v_{O2}.

This relatively high number of stages can imply that there will be a significant delay between both outputs, i.e., there can be a high phase deviation, unbalancing the output differential signal. However, since the operating frequency of the circuit is far from the transition frequency, f_T, of the transistors in the technology used, the delay can be negligible. Regarding the transimpedance function at the output v_{O1}, it has already been found and it corresponds to the one expressed by (3.13). The interest here lies in finding a relation between v_{O2} and I_d, as well as a relation between the differential voltage and I_d. For that effect, one could analyze the path between v_{O2} and I_d in the incremental circuit however, this would be rather extensive. By knowing the gain of the configurations presented by M_4 and M_5, the mentioned relation can be effortlessly obtained. As stated before, in chapter 2.3, the voltage gain in a CG stage can be easily found and, in M_5 configuration, to a good approximation, it will be

$$V_{o2} = g_{m5}(r_{ds5}||R_{X2})V_{n2} = A_{v0,5}V_{n2} \tag{3.52}$$

where V_{n2} stands for the voltage in node n_2. The voltage gain across M_4's configuration can be given by [31], [33]

$$V_{n2} = \frac{g_{m4}}{g_{m4} + g_{mb4}}V_{n1} = A_{v0,4}V_{n1} \tag{3.53}$$

if $g_{m4} \gg r_{ds4}^{-1}$. Note that V_{n1} is the voltage present at node n_1, which corresponds to V_{ds2}. Here it may become important to notice Fig. 3.8, which corresponds to the incremental circuit seen in node n_1, facing the input port, presenting a path to the input signal. Also notice that since the focus is on V_{o2}, V_{o1} can be shunted to the ground node.

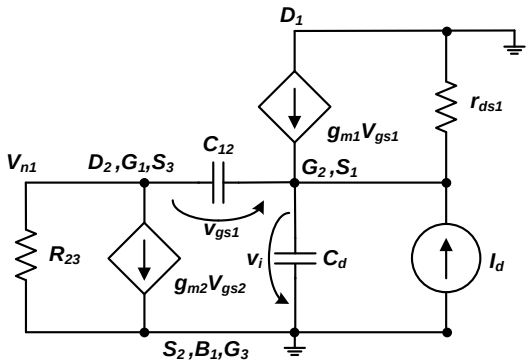

Figure 3.8 – Partial incremental circuit of the inverted output.

Replacing (3.53) into (3.52) will give a relation between V_{o2} and V_{n1}, following

$$V_{o2} = A_{v0,5}A_{v0,4}V_{n1}. \tag{3.54}$$

Considering $V_{n1} = V_{gs1} + V_i$ and taking (3.7) into account, (3.54) can be written as

$$V_{o2} = A_{v0,5}A_{v0,4}(1 - A)V_i \tag{3.55}$$

in which A is given by (3.6). In the passing band of the amplifier, $A \gg 1$. Thus, (3.55) will be

$$V_{o2} = -AA_{v0,5}A_{v0,4}V_i. \tag{3.56}$$

In order to find a relation between V_i and I_d one can apply KCL to node G_2, S_1 in Fig. 3.8, resulting in

$$V_i sC_d + V_{gs1}sC_{12} + g_{m1}V_{gs1} + V_i r_{ds1}^{-1} + I_d = 0 \tag{3.57}$$

and, if $g_{m1} \gg r_{ds1}^{-1}$,

$$I_d = -V_i[s(C_d + AC_{12}) + Ag_{m1}]. \tag{3.58}$$

By developing (3.58), it becomes easy to find an expression that relates V_i with I_d, following

$$V_i = -\frac{1}{A[s^2\tau_a\tau_i + s\tau_i(\eta + 1) + 1]} I_d \tag{3.59}$$

The transimpedance function of the inverted output can now be found by replacing (3.59) into (3.56),

$$V_{o2} = A_{v0,5}A_{v0,4}\frac{1}{s^2\tau_a\tau_i + s\tau_i(\eta + 1) + 1} I_d. \tag{3.60}$$

Note that using (3.52), (3.53), making the approximation $r_{ds5} \gg R_{X2}$ and, assuming a worst case scenario in which $A_{v0,4} \cong 0.7$ – the bulk transconductance is usually $g_{mb} \approx 0.7 \sim 0.9g_m$ [31] – the inverted output's transimpedance function can be written as

$$\frac{V_{o2}}{I_d} = 0.7\frac{g_{m5}}{g_{m1}}\frac{R_{X2}}{s^2\tau_a\tau_i + s\tau_i(\eta+1)+1}. \tag{3.61}$$

As seen by the above, the transimpedance function in the inverted output has opposite phase of the one shown in (3.13). One important feature of (3.61) is the fact that the frequency response is the same for both outputs. The parameter $\beta + 1$ is only missing from the above because it was made the approximation $r_{ds5} \gg R_{X2}$. Otherwise, there would still be a multiplication factor $(\beta_2 + 1)$, where β_2 would stand for the ratio between R_{X2} and r_{ds5} in the denominator of (3.61), similarly to (3.13). As seen above, in order for V_{o2} to have the same amplitude of V_{o1}, g_{m5} must be approximately equal to $1.43g_{m1}$. Regardless, the same can be said about the load resistor R_{X2} and R_{X1}.

The differential transimpedance function can be found by simply subtract both outputs, resulting in

$$\frac{V_{diff}}{I_d} = \frac{V_{o1} - V_{o2}}{I_d} = -\frac{R_{X1} + 0.7g_{m5}g_{m1}^{-1}R_{X2}}{s^2\tau_a\tau_i + s\tau_i(\eta+1)+1}. \tag{3.62}$$

Note that for simplicity, it was assumed that $\beta_1 = \beta_2 \cong 0$.

Regarding a noise analysis, for simplicity, only I_{n2}, the thermal noise generated by M_2, will be considered, since this will be the dominant noise source as mentioned above. Transistors M_4 and M_5 have both low transconductance and, as such, the noise they generate can be neglected, as will be further seen by simulations. Much like it was previously done with the transimpedance function, the interest lies in finding a relation between V_{o2} and I_{n2}, where V_{o2} will be given by (3.54), even though this time, V_{n1} will depend on I_{n2} instead of I_d. In Fig. 3.9 the incremental circuit contemplating the path between V_{n1} and I_{n2} is shown.

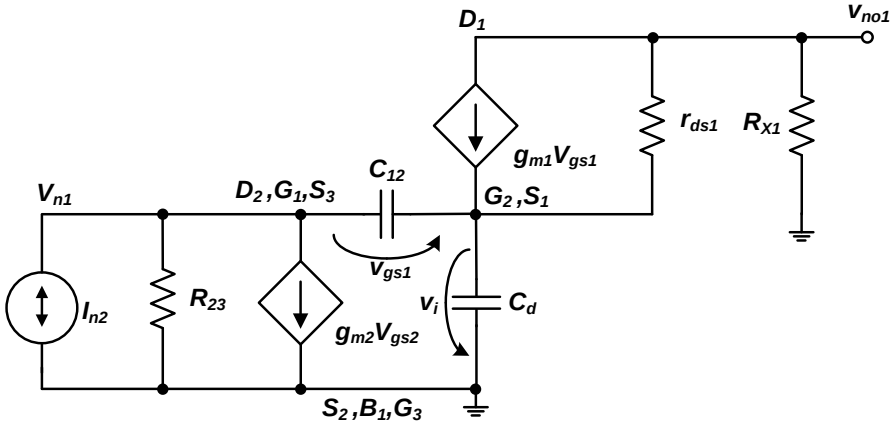

Figure 3.9 – Partial incremental circuit of the inverted output with M_2's thermal noise contribution.

In order to find the noise transfer function for V_{o2}, one can apply KCL to node D_1, resulting the expression given by (3.29). In node S_1, G_2 the expression shown in (3.32) will be obtained, which can be rewritten in the form

$$V_{no1} = -\frac{sC_d}{R_X^{-1}} \frac{1}{(1 + sg_{m1}^{-1}C_{12})} v_i \tag{3.63}$$

which, by replacing into (3.29) and noticing that $v_i = V_{n1} - V_{gs1}$ will result into

$$V_{gs1} = V_{n1} r_{ds1}^{-1} g_{m1}^{-1} \frac{sr_{ds1}C_d + 1}{sg_{m1}^{-1}C_d + 1}. \tag{3.64}$$

In the derivation of (3.64) it was assumed that $C_d \gg C_{12} \gg r_{ds1}^{-1} g_{m1}^{-1} C_{12}$. In node n_1, by KCL, noticing that $g_{m2} \gg R_{23}^{-1}$, the following can be obtained

$$-I_{n2} = g_{m2} V_{n1} + g_{m2}(sg_{m2}^{-1}C_{12} - 1)V_{gs1} \tag{3.65}$$

Replacing (3.64) into (3.65) will present a relation between I_{n2} and V_{n1}, following

$$-\frac{I_{n2}}{V_{n1}} = g_{m2}\left[1 + (sg_{m2}^{-1}C_{12} - 1) r_{ds1}^{-1} g_{m1}^{-1} \frac{sr_{ds1}C_d + 1}{sg_{m1}^{-1}C_d + 1}\right]. \tag{3.66}$$

Knowing that $r_{ds1}^{-1} g_{m1}^{-1} \ll 1$ and developing the above will result in

$$\frac{V_{n1}}{I_{n2}} = -g_{m2}^{-1} \frac{sg_{m1}^{-1}C_d + 1}{s^2 r_{ds1} C_d g_{m2}^{-1} A_{v0,1}^{-1} C_{12} + sg_{m2}^{-1} A_{v0,1}^{-1} C_{12} + 1} \tag{3.67}$$

Which, in turn can be written as

$$\frac{V_{n1}}{I_{n2}} = -g_{m2}^{-1} \frac{s\tau_z + 1}{s^2 \tau_{n1}\tau_{n2} + s\tau_{n1} + 1} \tag{3.68}$$

where $A_{v0,1} = g_{m1} r_{ds1}$ is M_1's configuration low frequency gain without the load impedance, and

$$\tau_z = g_{m1}^{-1} C_d, \tag{3.69}$$

$$\tau_{n1} = g_{m2}^{-1} A_{v0,1}^{-1} C_{12}, \tag{3.70}$$

$$\tau_{n2} = r_{ds1} C_d. \tag{3.71}$$

Note by (3.69) that τ_z will produce a low frequency zero. This suggests that the inverted output will contribute with a relatively higher noise than V_{o1}. Also aiding this, is the fact that the low frequency gain of the noise transfer function will be relatively high. Nonetheless, taking (3.54) into consideration, one can find the noise transfer function in the inverted output, written in the form

$$\frac{V_{no2}}{I_{n2}} = -A_{v0,5} A_{v0,4} g_{m2}^{-1} (s\tau_z + 1) \frac{\dfrac{1}{\tau_{n1}\tau_{n2}}}{s^2 + s\dfrac{1}{\tau_{n2}} + \dfrac{1}{\tau_{n1}\tau_{n2}}} \tag{3.72}$$

and, by comparing it to a canonical second-order transfer function, its natural frequency and quality factor are, respectively, as suggested,

$$\omega_{0,2} = \frac{1}{\sqrt{\tau_{n1}\tau_{n2}}} \tag{3.73}$$

$$Q_2 = \omega_{0,2}\tau_{n2} = \sqrt{\frac{\tau_{n2}}{\tau_{n1}}}. \tag{3.74}$$

In order to find the rms voltage at the inverted output, (3.72) can be decomposed as follows

$$\frac{V_{no2}}{I_{n2}} = -K\tau_z\omega_{0,2} \frac{s\omega_{0,2}}{s^2 + s\dfrac{\omega_{0,2}}{Q_2} + \omega_{0,2}^2} - K \frac{\omega_{0,2}^2}{s^2 + s\dfrac{\omega_{0,2}}{Q_2} + \omega_{0,2}^2} \tag{3.75}$$

where $K = A_{v0,5} A_{v0,4} g_{m2}^{-1}$. By doing so, one can use the derivation presented in [7] resulting

$$V_{no2,rms}^2 = -\frac{1}{4}\overline{\iota_{n2}^2}\left(\tau_z^2\omega_{0,2}^2 + 1\right)K^2\omega_{0,2}Q_2. \tag{3.76}$$

Respecting (2.39) and using the equations (3.69), (3.70), (3.71) and (3.73), the above can be written as

$$V_{no2,rms}^2 = -kT\frac{A_{v0,4}^2 A_{v0,5}^2}{g_{m2}}\omega_{0,2}Q_2\left(\frac{g_{m2}C_d}{g_{m1}C_{12}} + 1\right). \tag{3.77}$$

Assuming that $g_{m2} \gg g_{m1}$ and $C_d \gg C_{12}$will result in $g_{m2}C_d \gg g_{m1}C_{12}$. Therefore,

$$\frac{g_{m2}C_d}{g_{m1}C_{12}} \gg 1 \tag{3.78}$$

and the output rms noise voltage will be, to a good approximation,

$$V_{no2,rms}^2 = -kTA_{v0,4}^2 A_{v0,5}^2\frac{C_d}{g_{m1}C_{12}}\omega_{0,2}Q_2. \tag{3.79}$$

The differential output rms noise voltage, $V_{nodiff,rms}^2$, will be the subtraction of (3.39) and (3.79). Note that (3.79) shows itself with its phase inverted, which means the overall integrated noise will result in the sum of the noise presented in both outputs. Thus, the final expression for the output noise voltage will be

$$V_{nodiff,rms} = V_{no1,rms} - V_{no2,rms} \tag{3.80}$$

where $V_{no1,rms}$ is given by (3.39).

4. TIA SIZING AND DESIGN PROCEDURES

In this chapter the sizing of the RCG TIA for the cases presented in the previous chapter will be presented. Despite the fact that the main focus of the work presented here is the development of the RCG TIA in a radiation detector front-end, the sizing and design procedures of the mentioned amplifier in a RF front-end context are also presented. Regarding the latter, for simplicity, only the basic form of the RCG TIA (expressed in chapter 3.1) will be sized and simulated.

Having the wide applicability of the TIA in mind, there are a few considerations that can be made, regardless the nature of the circuit, whether it is meant for a RF or a radiation detector front-end. For example, note that in the single-ended version of the TIA, the output noise follows what has been expressed by (3.39). There, it can be seen that the output noise voltage will be inversely proportional to the squared root of g_{m2}. Thus, the equivalent transconductance of the CS stage will be set to $g_{m2} = 5$ mS. One could be led to think that this value could be greater but, by increasing it any further, the power consumption of the amplifier would also be increased to impracticable values [7], [8]. Therefore, it is assumed that this will be the value of g_{m2} for any of the circuits here designed. The values of M_2's width and length, W_2 and L_2, respectively, can be given by the alternative MOS device transconductance equation following,

$$g_{m2} = 2\sqrt{k_2 I_{B2}} \tag{4.1}$$

in which,

$$k_2 = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2} \tag{4.2}$$

where μ_n is the electron mobility in the NMOS device and C_{ox} stands for the equivalent gate capacitance per unit area. The technology used in every design here shown is UMC 130 nm. For

this technology, one can assume a value of $\mu_n C_{ox} \approx 500\ \mu A\ V^{-2}$ and $\mu_p C_{ox} \approx 100\ \mu A\ V^{-2}$ for NMOS and PMOS devices, respectively. Regarding their threshold voltages we consider the NMOS device has $V_{tn} \approx 380$ mV, while the PMOS device has $|V_{tp}| \approx 330$ mV.

One other consideration which can be hereby mentioned is related to the ratio between the load resistor R_X and M_1's conduction channel, r_{ds1}. Ideally, this relation would be restricted to $\beta \ll 1$. By doing so, not only the transimpedance function becomes simpler but the TIA's low frequency gain becomes closer to R_X. In the RF front-end case, as will be further seen, this can be easily achievable but, in the radiation detector front-end, the value of β may have to be slightly, higher proving itself to be non-negligible. Nonetheless, more insight will be given into this in the respective section.

Following all the above, in this chapter, the methods for the TIA design will be mentioned for both contexts. It has been previously proven that the TIA performs better if designed with a transimpedance function with two real poles, when a low capacitance device is connected at the input, and complex conjugate poles when a high input capacitance device, such as a SiPM, is used [7]. Therefore, this will be the methodology adopted here.

4.1. RCG TIA IN A RF RECEIVER FRONT-END

The sizing of the basic RCG TIA in the context of an RF receiver will be shown in this section. For that matter, as said earlier, the TIA's input will be connected to a basic passive mixer, as expressed in chapter 2.2. With a mixer at the input, the signal shaping loses its relevance. In this type of application the interest lies in filtering the signal with a low-pass function, since the mixer's output has a very rich spectral density. In the basic passive mixer described previously, it was established that the output current will have a sinusoidal shape with a maximum amplitude of $I_m = 1\ \mu A$, operating at 10 MHz. The output equivalent capacity of the mixer will be, as an hypothetical example, $C_m = 0.1$ pF, since we estimate the switching device does not have large dimensions. This capacity is mostly determined by the parasitic capacitances of the active device responsible for the switching within the mixer.

Unlike the TIA operating with a SiPM at the input, this TIA will have low-current input signal. This means that, for this circuit, M_1's biasing current source, I_{B1}, can also be lower. The consequence of this is the fact that, since I_{B1} is lower, the voltage drop across R_X will decrease. This will present the possibility of increasing the value of R_X, which by (3.13) stands for the low frequency gain of the TIA. As a consequence, there will be a parasitic capacity C_X in parallel with R_X that must be accounted for, since it will originate a pole located in the passing band of the TIA, as Fig. 4.1 suggests. By taking into account that the mixer has low output capacity and,

noting that τ_i is proportional to C_m, it can be noticed that τ_i will be too low and that the resultant pole, inserted at the entrance of the TIA, will be located at a high enough frequency, making it non-dominant or even negligible. This way, the only time constants we of interest, in order to accomplish a low-pass function, are the ones inserted by the regulation stage and the load resistor R_X with its parasitic capacitance, C_X. Note that in Fig. 4.1 the low pass function block it is also shown, however, its realization is out of the scope of this thesis.

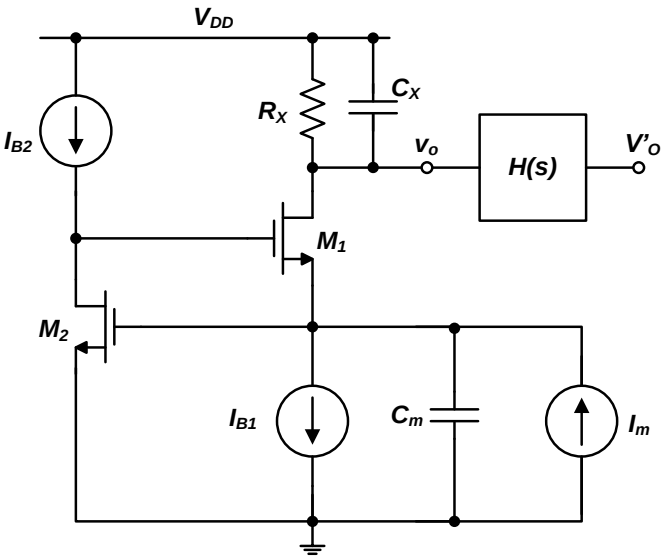

Figure 4.1 – Basic RCG TIA with parasitic capacity C_X and a low-pass functional block, *H(s)*.

In order to present an acceptable gain, it was established that the load resistor would be $R_X = 200\ \text{k}\Omega$ and, as a consequence, $C_X \cong 50\ \text{fF}$. The product of these will result in a time-constant of $\tau_X \cong 10\ \text{ns}$ and a pole at $f_X \cong 16\ \text{MHz}$. The dc voltage at the output node was aimed to be $V_{Odc} = 0.6\ \text{V}$, resulting in a M_1's biasing current of $I_{B1} = 3\ \mu\text{A}$. The reason why V_{Odc} has the value mentioned lies in the fact that if it was much lower, it would be possible for the output voltage variation to make transistor M_1 go into the triode region, deteriorating the linearity of the amplifier.

As mentioned earlier, in chapter 2.2, the input voltage must not vary in a critical manner. Otherwise, the mixer's switching device may be pulled out of the triode region. Having this in mind, it was pre-established that the TIA's input voltage should not greatly exceed $v_i = 1\ \text{mV}_{\text{pp}}$. Given the mentioned input current amplitude, at the limit, the input impedance must always be lower than

$$R_{in} = \frac{v_i}{I_m} \cong 500\ \Omega. \tag{4.3}$$

From (3.2) it can be easily proven that if $A_{v0} = 50$, than g_{m1} must be kept below 40 µS, so R_{in} does not exceed the limit expressed in (4.3). In this case, the reason why the regulation stage's low frequency gain was chosen to be $A_{v0} = 50$, is related to the fact that if it is any higher, it will be multiplied by some Miller capacitances, making these latter ones dominate the input capacity of the TIA, instead of C_m. Thus, this will make the dynamic input impedance impulsive response grow higher. Nonetheless, it should be noted that the regulation stage's low frequency gain must always be $A_{v0} \gg 1$.

In order to obtain a proper gain for the CS stage, M_2's transconductance, as previously mentioned, must be $g_{m2} = 5$ mS, with a correspondent $r_{ds2} \approx 10$ kΩ. This will result in a bias current of $I_{B2} = 250$ µA, providing M_2 is operating in moderate inversion with V_{DSAT2} around 80 mV. From (4.1) and (4.2), the aspect ratio can be found. In this case, $W_2/L_2 \approx 200$. Note that due to the high value of the bias current I_{B2}, it turns impossible to use $L_2 = L_{min}$ since r_{ds2} will be too low. Instead, it was used $L_2 = 250$ nm. W_2 may have to be adjusted in order to obtain $g_{m2} = 5$ mS. The value of the parasitic capacity C_X is 50 fF in order to obtain a pole inserted by τ_X at around 16 MHz.

By establishing V_{DSAT1} around 80 mV so M_1 stays in moderate/strong inversion, it was obtained, using (4.1) and (4.2), a transconductance of $g_{m1} = 75$ µS with a bias current of $I_{B1} = 3$ µA. This value of g_{m1} is high enough to make the TIA's input impedance acceptably low, resulting in a low voltage variation at the input. At this point, it becomes necessary to notice that since the bias current of M_1 will mandatorily be lower than the one of the SiPM, one can find a value of r_{ds1} considerably high using lower channel lengths. This results in a lower value of β, making the TIA gain closer to R_X. The aspect ratio of M_1 can be found from the drain current equation, resulting in $W_1/L_1 \cong 4.7$. In order to have a high conduction channel impedance, M_1's conduction channel length was $L_1 = 700$ nm, resulting in r_{ds1} slightly above 1 MΩ.

The circuit's sizing with a mixer at the input is resumed by Fig. 4.2 and Table 4.1. As in the following cases, the bias current sources were realized through means of basic current mirrors. In I_{B1} a reference current of 15 µA was used, in order to obtain a bias current of 3 µA. With a ratio of 5:1 it was used $W/L = 40$ µm/1 µm and $W/L = 8$ µm/1 µm. In I_{B2} it was used a PMOS current mirror with a ratio of 1:1 (two equal PMOS devices) with $W/L = 420$ µm/5 µm, generating a bias current of 250 µA.

In Table 4.1 the parameters of both NMOS active devices is shown, as well as the current mirrors output devices. Note that these values were obtained by simulation. From Table 4.1 it can be seen that r_{ds2} is low enough to make I_{B2} current source's dynamic impedance negligible and, that with $L_1 = 700$ nm, r_{ds1} becomes high enough to make β low valued, which is highly

desirable. It can also be seen that all transistors are operating in the saturation region, with M_1 and M_2 in moderate inversion and, M_{B4} and M_{B2} in strong inversion.

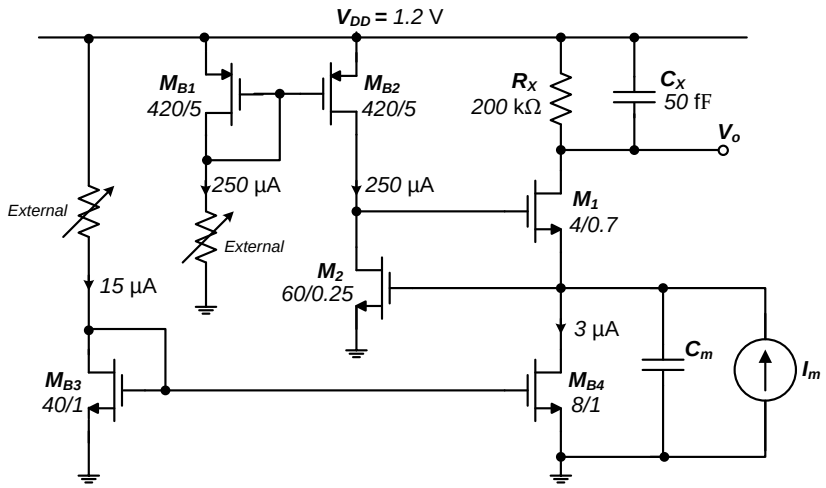

Figure 4.2 – RCG TIA with biasing current sources sizing.

Table 4.1 – MOS devices parameters with the mixer at the input; V_{Odc} = 0.6 V, R_X = 200 kΩ.

Device	I_B [µA]	g_m [mS]	r_{ds} [kΩ]	A_v	W [µm]	L [µm]	V_{DS} [mV]	V_{DSAT} [mV]
M_1	3	0.07	1300	–	4	0.7	261.0	71.4
M_2	250	5.03	9.6	48.2	60	0.25	610.7	72.9
M_{B4}	3	0.04	1826	–	0.85	1	328.1	133.2
M_{B2}	250	1.7	344.8	–	420	5	589.3	226.8

4.2. RCG TIA IN A RADIATION DETECTOR FRONT-END

In this section the sizing taken by, regarding the RCG TIA designed to operate with a SiPM at the input, will be shown. In a first stage, the guidelines and procedures in designing the basic version of the RCG TIA in a radiation detector front-end will be given. Subsequently, the circuit shown in chapter 3.2 will be sized, providing some further insight into this variation of the TIA. Finally, the differential proposed version of the RCG TIA will be properly sized. In this last section the output buffer will also be designed, since this is also an active part of the amplifier, as will be further seen. It should be noted that the two circuits derived from the basic version of the RCG will have their core devices, M_1 and M_2, designed in the same manner, i.e., in every circuit design shown, M_1 and M_2 will have the same dimensions. This will facilitate a comparison between the three circuits, giving a higher emphasis on the techniques used and their effects.

4.2.1. *Basic RCG TIA*

The output equivalent capacity in a PSD such as a SiPM is at least one order of magnitude higher from the one of an APD and, normally, as mentioned earlier, $C_d = 300$ pF. If the value of the regulation stage is $A_{v0} \gg 1$ and $C_{12} \ll C_d$, it can be seen that, by (3.13), $\eta < 1$. This will make the transimpedance function unfeasible with a dominant real pole since it would make g_{m1}, which is proportional to C_d, high, raising the noise, area and power consumption in the circuit. Another possibility would be choosing $Q = 0.5$, making the transimpedance function have two equal real poles. Since, in this case, it is hard to accomplish a value of $\beta \ll 1$, it can be seen from (4.4), obtained from (3.15), that not only g_{m1} would be too high, but the peaking time would probably be higher than it should [7].

$$g_{m1} = \frac{Q^2(\eta+1)^2(\beta+1)C_d}{A_{v0}\tau_a} \tag{4.4}$$

One of the reasons why β must be kept low is related to the fact that with its increase, and maintaining g_{m1} at an acceptable level, A_{v0} will increase, raising either the size or power consumption of M_2.The remaining choice is to design the TIA with complex conjugate poles. As seen previously, this means $Q > 0.5$. From (3.17) it can be seen that Q must be lower than unity in order to avoid an under-damped response, avoiding this way an oscillating response of the TIA. It also must be noted that since the SiPM has an output current higher than the one previously accounted for, with the mixer, this means R_X may have to be at least one order of magnitude lower than in the previous case. Being lower, the parasitic capacitance associated to R_X will also be lower and, therefore, the resultant pole will be located at a high enough frequency making it negligible.

One point worth being mentioned is the fact that the design taken by in the present section was highly influenced by [7]. However, here it was considered that the SiPM should have its biasing reversed, i.e. the input current signal flows from the input of the TIA to the ground node, through the PSD. By doing so, will allow for the dc voltage at the output node, V_{Odc}, to be lowered. This will permit an small increase on R_X, raising the TIA's low frequency gain. This decrease of the dc voltage is able to present a better SNR at the output of the TIA. However, this is also limited since there must be enough room for V_{DS1} and I_{B1}'s transistors to remain in saturation. In either cases here studied, except for the TIA with the mixer at the input and the differential version, it was considered $V_{Odc} \approx 500$ mV. This will make V_{DS1} to be over V_{DSAT1} and will allow enough room for I_{B1}'s dc voltage. If V_{Odc} is lowered past the 500 mV, V_{DS1} will be very close to V_{DSAT1} and, despite the better results obtained, the ratio between R_X and r_{o1} would

be $\beta > 1$ and the circuit would be highly dependent on fabrication processes, which would be undesirable. It should be noted that lowering V_{Odc} does not affect greatly I_{B1}'s transistors since the voltage at I_{B1}'s terminals is imposed by V_{GS2}.

From (4.4) it can be seen that g_{m1} will be defined at the cost of $\tau_a A_{v0}$ and if the first has to be limited, the latter must be high enough to that effect. Resuming, since both τ_a and A_0 depend on r_{ds2}, which is proportional to L_2, it follows that L_2 will have to be higher than the minimum value accepted by the technology used in order to keep g_{m1} at an acceptable level [7]. This circuit has already been previously studied given this application and, in [7], [8] can be seen that the relation between the output voltage and the noise level at the output behaves better when A_{v0} is around 100 and $g_{m2} = 5$ mS, which stands for a channel length L_2 well above the minimum. The value of M_2's transconductance is the one mentioned earlier, with $I_{B2} = 250$ µA and $R_X = 23.2$ kΩ. We have optimized the circuit in order to reach the best possible $V_{om}/V_{no,rms}$ ratio, where $V_{no,rms}$ stands for the output noise voltage in rms at the output of the TIA and is given by (3.39). As mentioned in chapter 2.2, t_m must be lower than 40 ns. The TIA was designed so it could have t_m around 36 ns, predicting that an output buffer parasitic capacitance will insert a slower response of the circuit. The value of τ_i must be around 10 ns [7], [8], [10], resulting, with the chosen A_{v0}, a value of g_{m1} of around 300 µS. The value of τ_a was obtained through simulation, respecting an ac analysis at the drain of M_2, given the difficulty in knowing the exact value of the parasitic C_{12}.

In Fig. 4.3 it can be seen the sizing of the basic RCG TIA with a SiPM at the input. The regulations stage's low frequency gain chosen was $A_{v0} = 100$ and, with the transconductance associated to the regulation stage mentioned, it was obtained, using (4.1) and (4.2), $W_2/L_2 = 225$ providing $L_2 = 800$ nm, well above L_{min}. With $I_{B1} = 30$ µA the aspect ratio of M_1 was found to be $W_1/L_1 = 3.6$ with $L_1 = 1.5$ µA. The biasing current sources were realized through means of basic current mirrors. In the case of I_{B1} a reference current of 150 µA with a ratio of 5:1 was used, whereas in the case of I_{B2} the same values were used in all examples studied here.

In Table 4.2 the parameters of both NMOS active devices, M_1 and M_2 is shown, as well as M_{B2} and M_{B4}. Regarding the latter ones, these are not shown in Fig. 4.3 but represent the biasing current sources output devices, as shown in Fig. 4.2. It can be seen from Table 4.2 that r_{ds2} is low enough to make the bias current source, I_{B2}, dynamic impedance negligible. Note that as expected, this time, r_{ds1} is not much greater than R_X, resulting in $\beta = 0.4$. It can also be seen that all the transistors are operating in a well established saturation region, excepting transistor M_1 which is operating near a saturation/triode boundary region.

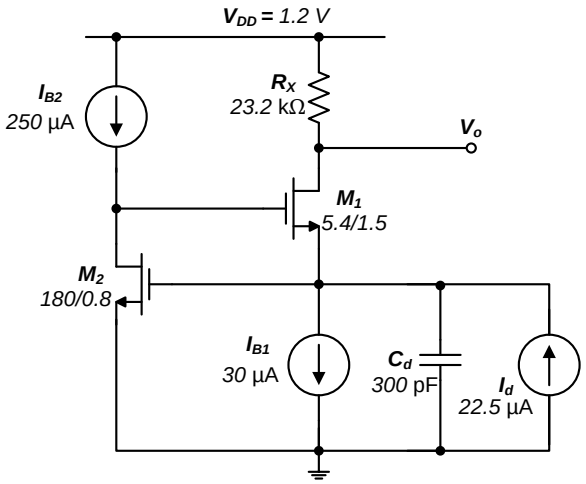

Figure 4.3 – Sizing of the basic RCG TIA with a SiPM at the input.

Table 4.2 – MOS devices parameters for the basic RCG TIA with a SiPM at the input. V_{Odc} = 0.5 V; t_m = 36 ns; R_X = 23.2 kΩ.

Device	I_B [µA]	g_m [mS]	r_{ds} [kΩ]	A_v	W [µm]	L [µm]	V_{DS} [mV]	V_{DSAT} [mV]
M_1	30	0.27	57.8	–	5.4	1.5	229.0	197.8
M_2	250	5.01	20	100.2	180	0.8	727.3	81.1
M_{B4}	30	0.41	151.1	–	8.55	1	273.0	129.6
M_{B2}	250	1.7	237.5	–	420	5	472.7	226.8

4.2.2. *RCG TIA with Noise Improvement*

The sizing of the RCG TIA with noise response improvement, studied in chapter 3.2, will be designed in this section. Basically, the active devices M_1 and M_2 will have the same dimensions as the ones in the previous section and, therefore, there won't be a mention to these devices in the present section. Here, the interest lies in establishing the width, length and dc operating point of transistor M_3 along with its biasing current source, while noticing the effect they will cause in the remaining circuit.

Firstly, given the limitations regarding power consumption, it was established that M_3's biasing current should not exceed $I_{B3} = 5$ µA. With respect to (4.1), this will lead to a slight increase in M_2's transconductance since there will be more current passing through the device. It is also assumed that transistor M_3 must be operating in the saturation region, in strong inversion, which means that $V_{DSAT3} \geq 100$ mV. Thus, from the drain current equation of a MOS device operating in saturation,

$$I_D = k_3 V_{DSAT3}^2, \tag{4.5}$$

in which k_3 is given by (4.2), the aspect ratio of M_3 can be found. In this case, the resulting ratio was $W_3/L_3 = 2.5$. As previously mentioned, the value of r_{ds3} must be near the value of I_{B3} biasing current source's dynamic impedance, R_{OB3}, so equation (3.43) can be fulfilled. Therefore, I_{B3} must be carefully designed, in order to validate (3.44). Note that, as seen in Table 4.2, transistor M_2 has a very large V_{DS} voltage. As a consequence, there will be little room for both M_3 and I_{B3} V_{DS}. This will result in the fact that I_{B3} will be operating in a saturation/triode boundary region. This current source was accomplished by mirroring I_{B2} to the drain of M_3 and, therefore, its aspect ratio was found by the relation between both current sources, i.e., maintaining the same channel length, for $I_{B3} = 5$ µA, its width should be $W_{B3} = 0.02 W_{B2}$.

In Fig. 4.4 the sizing of M_3 is shown contemplating also the sizing of the remaining referred devices present in the circuit. Note that for simplicity, the current sources are represented by its ideal models. All the devices' parameters are shown in Table 4.3.

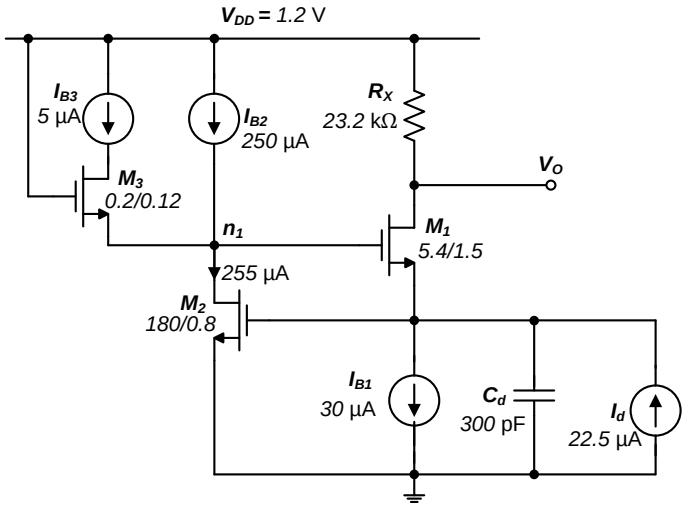

Figure 4.4 – Sizing of the RCG TIA with improved noise response, with a SiPM at the input.

Table 4.3 – MOS devices parameters for the RCG TIA with improved noise response, with a SiPM at the input. V_{Odc} = 0.5 V; t_m = 36 ns; R_X = 23.2 kΩ.

Device	I_B [µA]	g_m [mS]	r_{ds} [kΩ]	A_v	W [µm]	L [µm]	V_{DS} [mV]	V_{DSAT} [mV]
M_1	30	0.26	56.8	–	5.4	1.5	228.2	195.2
M_2	255	5.10	19.7	59.12	180	0.8	728.4	81.6
M_3	4.7	0.07	153.8	–	0.2	0.12	270.0	113.4
$M_{I,B1}$	30	0.41	151.7	–	8.55	1	274.0	129.6
$M_{I,B2}$	250.3	1.7	239.8	–	420	5	471.6	226.7
$M_{I,B3}$	4.7	0.03	162.8	–	8.4	5	201.5	226.8

In the above table, devices $M_{I,B1}$, $M_{I,B2}$ and $M_{I,B3}$ correspond to the output transistor of current sources I_{B1}, I_{B2} and I_{B3}, respectively. It can be seen from Table 4.3 that the current source I_{B3} is effectively working in the mentioned boundary region, since the overdrive voltage is quite near its V_{DS}, even though approximation $g_{m3} \gg r_{ds3}^{-1}$ can be done. One important regard which can be made is related to the fact that M_1's equivalent conduction channel impedance was not altered and, thus the value of β will be the same as in the previous case. The value of the CS stage active load will now be $R_{23} \cong 11\,\text{k}\Omega$. This value is almost one half of r_{ds2} which means that the regulation stage's gain, A_{v0}, will be reduced accordingly, raising the TIA's input impedance. The effect of this reduction in the regulation stage's gain has already been previously studied in chapter 3.2. Nonetheless, following equations (3.50) and (3.51), the time-constants in the transimpedance function will be $\tau_a = 11.2\,\text{ns}$ and $\tau_i = 19.5\,\text{ns}$, considering $C_{12} = 1\,\text{pF}$. As suggested in chapter 3.2, the bandwidth of the TIA will be given by the frequency related to τ_i, the one given in (3.51), since $\tau_i > \tau_a$. Note that the parameters shown in Table 4.3 were obtained by simulation.

4.2.3. *RCG TIA with Differential Output*

In this section the proposed differential circuit of the RCG TIA will be sized. The core circuit of the TIA will be shown with all of its active devices and current mirrors. Furthermore, the output buffer will be also shown and properly sized. In Fig. 4.5 the differential RCG TIA is shown, already contemplating the output buffer, composed by transistors M_{OP} and M_{ON}, along with their respective current sources I_{BOP} and I_{BON}. Each of the pair M_O, I_{BO} represent a source-follower stage.

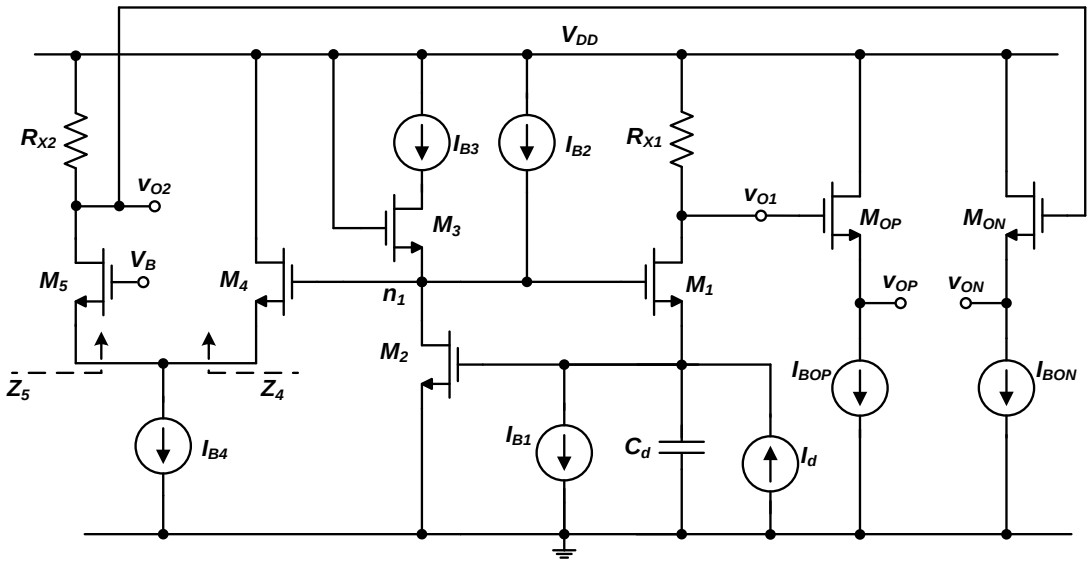

Figure 4.5 – Schematic of the differential RCG TIA with output buffer included.

In the sizing described in this section, transistors M_1, M_2 and M_3 have not been subjected to any changes, regarding what was previously presented. The same can be said about I_{B1}, I_{B2} and I_{B3}. However, given the importance of the linearity of the amplifier, the load resistor R_{X1} has been lowered to $R_{X1} = 20$ kΩ. This means that V_{O1} will have its dc component at roughly 0.6 V. By doing so, V_{DS1} will be slightly higher, taking M_1 to a well established saturation region, improving the circuit's linearity. It is also expected that by rising V_{DS1}, the equivalent channel impedance r_{ds1} will also rise, lowering the value of β, which, for what has been mentioned, is highly desirable.

The focus, for now, lies in sizing transistors M_4 and M_5. Note that the current source I_{B4} is biasing the mentioned transistors and, as such, the current that will flow through each of them will be limited by the impedance present at their source terminals. The impedance seen at the sources of these devices can be seen in Fig. 4.5, denoted by Z_4 and Z_5. Since both devices must be operating in saturation region, the mentioned impedances will be

$$Z_4 = g_{m4}^{-1} \tag{4.6}$$

and

$$Z_5 = g_{m5}^{-1}. \tag{4.7}$$

By applying KCL to the node connecting both sources and I_{B4}, it can be easily proven that

$$Z_4 = \alpha Z_5 \tag{4.8}$$

in which,

$$\alpha = \frac{\gamma}{1-\gamma} \tag{4.9}$$

where γ stands for the ratio $\gamma = I_{D5}/I_{B4}$. Note that I_{D5} represents the current that flows through transistor M_5. The biasing current I_{B4} will be $I_{B4} = 100$ μA and, noticing that the current that flows through the drain of M_5 must be the same as the one of M_1, I_{D4} will be

$$I_{D4} = I_{B4} - I_{D5} \cong I_{B4} - I_{B1} \cong 70 \text{ μA}. \tag{4.10}$$

Thus, $\gamma \cong 0.3$ and $\alpha \cong 0.43$. From (3.61) and (3.62), it was established that for $R_{X1} = R_{X2}$ it would have to be

$$g_{m5} = 1.43 g_{m1}. \tag{4.11}$$

Replacing (4.11), (4.7) and (4.6) into (4.8) and, using (4.9) one can find the value of the transconductance for the source-follower stage, as follows

$$g_{m4} = 1.43 \alpha g_{m1} \tag{4.12}$$

The aspect ratio of M_4 can be found using (4.1) and (4.2), resulting $W_4/L_4 \cong 11.4$. Regarding the aspect ratio of M_5, one can use the drain current equation, expressed by (4.5), in order to find it. The result was $W_5/L_5 \cong 7$, if the overdrive voltage expected is around $V_{DSAT5} \cong 150$ mV, which would imply the transistor was operating in strong inversion. As a result, the biasing voltage in the gate of transistor M_5 must be $V_B = 682$ mV. This voltage must be provided by a bandgap circuit; otherwise the amplifier will be extremely sensitive to Process, Voltage and Temperature (PVT) variations. The exact value of V_B was obtained by simulation.

Regarding the output buffer, both M_{OP} and M_{ON} transistors have the same size, with an aspect ratio of $W/L = 10.9$, and same bias currents. The biasing currents were chosen to be $I_{BOP} = I_{BON} = 10$ µA. With these values, there will be enough room for the bias currents V_{DS} voltage, providing their output transistors will be operating in moderate/strong inversion, in the saturation region. The realization of I_{BOP} and I_{BON} was achieved through a current mirror with a ratio of 1:1. The aspect ratio of the biasing device is $W/L = 6.25$. In Fig. 4.6 the whole amplifier is shown with all of its devices and their respective sizing, while Table 4.4 shows these devices' parameters. Note that I_d and C_d have been neglected in Fig. 4.6.

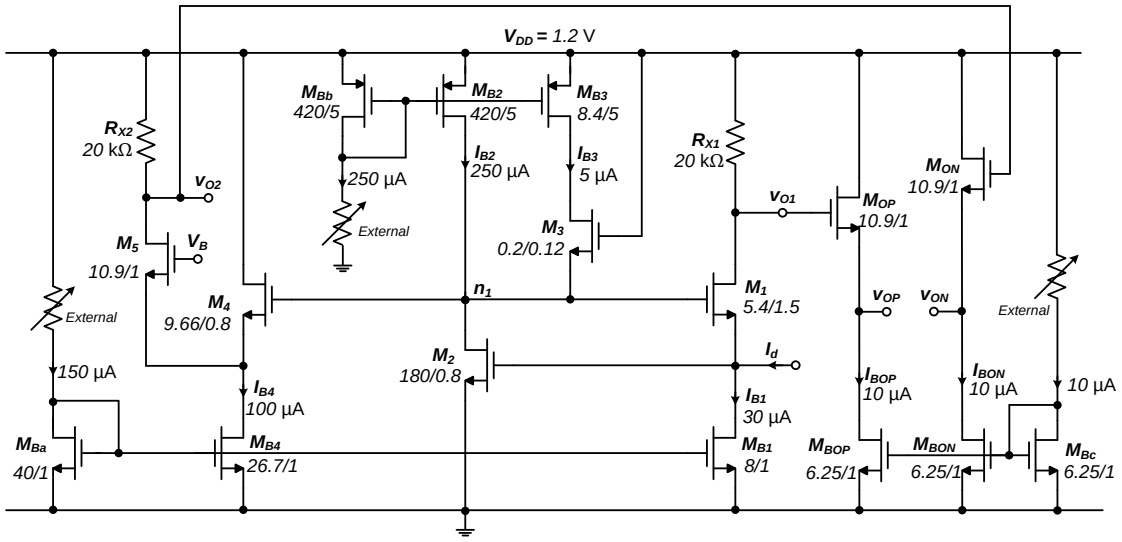

Figure 4.6 – Complete schematic of the proposed version of the differential RCG TIA with output buffer.

Table 4.4 – MOS devices parameters for the differential RCG TIA proposed, with a SiPM at the input.
$R_{X1} = R_{X2} = 20$ kΩ; $V_{O1dc} = V_{O2dc} = 0.6$ V;
$V_{OPdc} = V_{ONdc} = 0.3$V; $t_{mdiff} = 38$ ns.

Device	I_B [µA]	g_m [mS]	r_{ds} [kΩ]	A_v	W [µm]	L [µm]	V_{DS} [mV]	V_{DSAT} [mV]
M_1	30.04	0.276	194.6	–	5.40	1.50	325.1	195.1
M_2	255.15	5.100	19.7	59.7	180.00	0.80	725.0	81.6
M_3	4.82	0.071	144.9	–	0.20	0.12	249.9	114.9
M_4	69.97	0.802	87.7	0.9*	9.66	0.80	893.6	154.8
M_5	30.06	0.401	294.9	7.5	23.70	3.00	292.5	140.2
$M_{OP,N}$	10.03	0.210	595.2	0.9*	10.90	1.00	899.5	78.2
M_{B1}	30.04	0.411	151.9	–	8.54	1.00	274.0	129.6
M_{B2}	250.32	1.698	240.4	–	420.00	5.00	474.9	226.8
M_{B3}	4.82	0.030	271.0	–	8.40	5.00	225.0	226.8
M_{B4}	100.03	1.354	50.8	–	27.10	1.00	306.4	131.6
$M_{BOP,N}$	10.03	0.180	502.5	–	6.25	1.00	300.8	95.5

*Value obtained by simulation, respecting (3.53).

From Table 4.4 it can be seen that, in this configuration $r_{ds1} \gg R_{X1}$. This implies that the parameter β_1 can be neglected, as suggested by (3.61). The same can be said about β_2, the ratio between r_{ds2} and R_{X2}. It must also be noted that with the sizing presented, M_1 will be operating in a better defined saturation region, in a strong inversion state. One aspect to consider, is the fact that the TIA's input impedance has now been slightly increased, given the decrease in the regulation's stage low frequency gain. The input impedance will now be around $Z_{in} \cong 60\ \Omega$, following (3.2), which suggests that the voltage variation in the input of the TIA will now be slightly higher.

The value of r_{ds3} is still of the same order of magnitude of R_{OB3}, denoted by $r_{ds,MB3}$ in Table 4.4. This means that the deduction made in chapter 3.2 is still valid for this variation of the circuit. Note that M_3 is operating in the saturation region, while M_{B3} is in a saturation/triode boundary region, as expected.

Regarding transistor M_4, it can be seen that the sizing presented validates the deductions shown in this section. The current that flows through it is the expected, while its transconductance presents itself to be quite near the desired value. This stage's voltage gain was found, by simulation, to be around $A_{v0,4} \cong 0.9$. Such value was found with the aid of equation (3.53) and the simulated value of the bulk transconductance, which was around $g_{mb4} \cong 83$ µS.

Transistor M_5 is biased with $I_{D5} = 30$ µA. Its sizing made possible to achieve a transconductance near the one expected, which was $g_{m5} = 1.43 g_{m1}$. Also, notice that this transistor is operating in the saturation region, in strong inversion.

The output dc voltage in both output nodes is given by

$$V_{Odc1,2} = V_{DD} - R_{X1,2} I_{B1,4} \tag{4.13}$$

and, since $R_{X1} = R_{X2}$ and $I_{B1} = I_{B4}$, both output voltages will mandatorily have equal dc component ($V_{Odc} = 0.6$ V). Thus, the output buffer can have its CD stages sized in the same manner. Transistors M_{OP} and M_{ON} both have a gate-to-source voltage of $V_{GS} = 0.3$ V and, therefore, the output buffer will have its output voltage centered at 0.3 V, making the common-mode differential output voltage null. The output buffer will present an attenuation of 10 % in the output signal, given the CD stages' voltage gain of 0.9. This value was, obtained by simulation, in an identical manner to what has been done with M_4.

5. SIMULATION RESULTS

In this chapter the simulations validating the deductions previously taken are shown. This chapter will then be divided into four sections:

1. In the first section the results obtained with the designs taken in chapter 4.2 – the RCG TIA in a radiation detector front-end – will be shown.
2. Separately, it will also be shown a design contemplating a feedback TIA in a radiation detector front-end.
3. Following, in the third part of the chapter, simulations taken with the basic RCG TIA designed to operate in a RF front-end environment will be presented.
4. Finally, concluding this chapter, a comparison between the designs here taken by and previously designed TIAs, meant for the same type of application, will be presented.

All simulations shown were taken using Cadence Tools with the purpose of validating what has been previously deducted in chapters 2, 3 and 4, while maintaining the system's requirements already stated. Therefore, great emphasis will be given into the TIA's output voltage, power consumption, noise level, linearity and frequency response of the designed circuits.

5.1. RADIATION DETECTOR FRONT-END RESULTS

In this section the results obtained with the three variations of RCG TIA circuit with a SiPM at the input will be shown. Here, the interest lies in showing the output voltage with its rising time and peak amplitude, the TIA's frequency and noise response, linearity and stability. Furthermore, the differential proposed version of the TIA was subjected to a corner analysis in order to validate the feasibility of the circuit. In this section, a possible physical layout of the differential RCG TIA is also presented. Note that the main purpose of the following analyses is to prove and validate the deductions previously taken, in chapters 3 and 4.

Whenever possible, the three circuits' physical quantities will be merged into one single plot, in order to facilitate a comparison between all of the circuits. The measurements taken will

be differentiated with letters A, B and C, in which these correspond to the basic RCG TIA, RCG TIA with improved noise and differential RCG TIA, respectively. Thus, in Fig. 5.1, it can be seen the output voltage of the basic RCG TIA and RCG TIA with improved noise response.

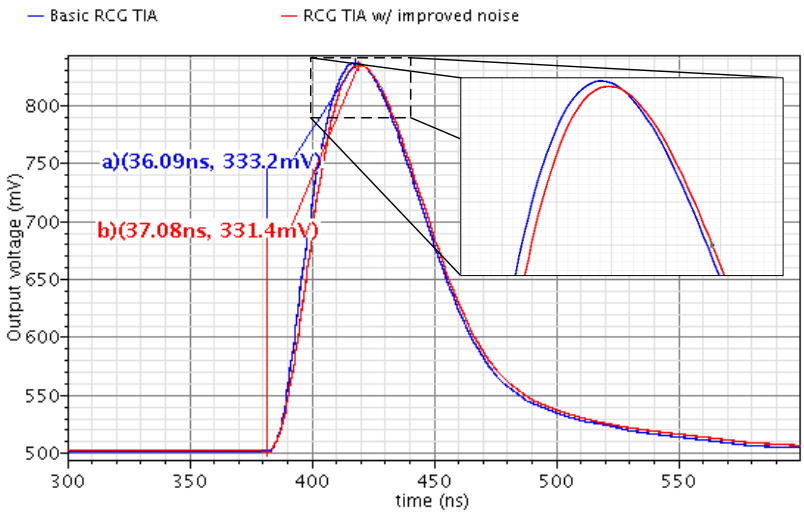

Figure 5.1 – Output voltage in: a) Basic RCG TIA;
b) RCG TIA with improved noise response.

In the above, it can be seen that both output signals have a dc component centered around 0.5 V. In the case of the basic RCG the output signal reaches an amplitude of $V_{om,A} \cong 333$ mV in a total $t_{m,A} \cong 36.1$ ns, as expected. In the improved noise case, the output signal shows a negligible decrease in the peak amplitude and a slight increase in the rising time, showing $V_{om,B} \cong 331$ mV and $t_{m,B} \cong 37.1$ ns. Such increase of 1 ns in $t_{m,b}$ can be negligible. Nonetheless, this increase is related to the fact that g_{m1} will suffer a slight decrease with the inclusion of M_3, as can be seen in Tables 4.2 and 4.3, and the fact that τ_i is inversely proportional to g_{m1}. In any case, it is considered that the differences between both signals can be made negligible, if the output buffer does not insert significant delay to the output signal.

The output voltage in the differential RCG, as well as the buffer output, is shown in Fig. 5.2. Note that, in this case, both outputs are sized to have their differential dc components null. The differential output voltage in the TIA core can reach $V_{om,C} \cong 513$ mV during $t_{m,C} \cong 38.1$ ns, while the output buffer reaches $V_{om} \cong 453$ mV in the approximately same time. This implies that the output buffer presents a voltage loss of around 12 %, which is a value that could be expected. One can notice that, unlike the RF front-end case, the transimpedance gain in the three cases presented here is slightly further from the value of R_X. This can be easily justifiable since the input signal is operating in a frequency quite near the position of the dominant poles of the circuit. Therefore, one must account for a 3 dB loss in the output signal. One other motive for the

transimpedance gain to be lower than R_X, is related to the fact that the value of β is not $\beta \ll 1$. In practical terms this means that r_{ds1} will appear in parallel with R_X, lowering the dc transimpedance gain of the TIA.

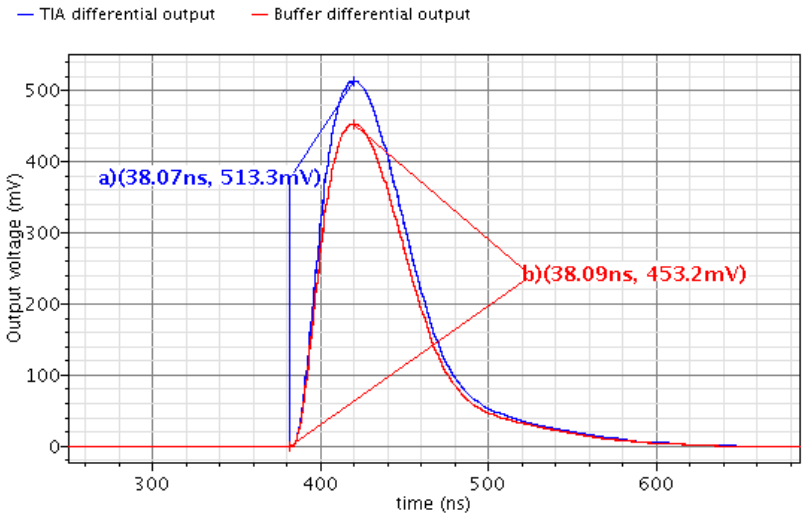

Figure 5.2 – Differential RCG TIA output: a) TIA core output signal; b) Output buffer output signal.

The effect M_3 inserts into the TIA can be seen in Fig. 5.3. Here, the bandwidth of the local feedback, composed by the regulation stage, is shown. To the effect, an ac analysis referent to the input and output of M_2 was made, where the pole inserted by τ_a can be observable in the three circuits. As expected, the insertion of M_3 makes the impedance R_{23} lower, lowering, likewise, the value of τ_a. Thus the pole f_a will be pushed to slightly higher frequencies, as can be seen below. Notice that the pole f_a along with its time-constant is given in Table 5.1, for each circuit.

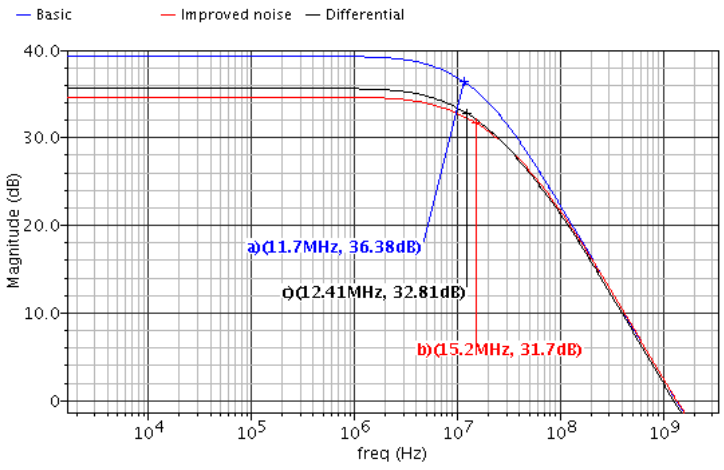

Figure 5.3 – M_2's frequency response with dominant pole: a) Basic RCG; b)RCG with noise improvement; c) differential version.

Table 5.1 – Low frequency gain, time-constant τ_a and its pole frequency for the three circuits.

Circuit	f_a [MHz]	τ_a [ns]	A_{v0}[dB]
A	11.7	13.6	≅ 40.0
B	15.2	10.5	≅ 35.0
C	12.4	12.8	≅ 35.5

Also, as expected, Fig. 5.3 shows that M_2's low frequency gain, A_{v0}, is also lowered when M_3 is inserted. To see the TIAs' bandwidths an ac analysis, depicted in Fig. 5.4, is shown. This analysis contemplates the output of the TIA.

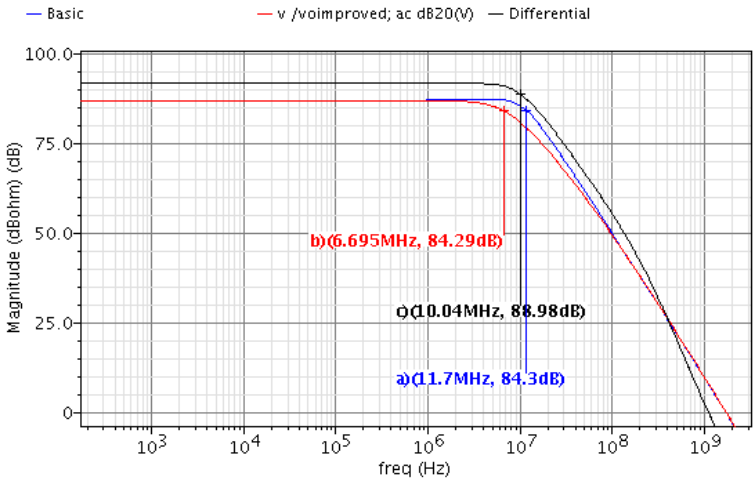

Figure 5.4 – TIAs' output frequency response.

Regarding the transimpedance gain it can be seen by the above that the basic RCG and the RCG with improved noise have the same approximate gain. The difference between these two is simply the fact that the dominant pole will be given by f_a in the basic RCG case and by f_i in the case of the RCG with noise improvement. Note that by being so, the circuit respects what has been previously stated in (3.51). In Table 5.2 the low frequency transimpedance gain, and dominant pole frequency, f_p, of each circuit are shown. Note that in the case of circuits B and C, f_p corresponds to (3.51), while in the case of circuit A it corresponds to (3.50).

Table 5.2 – Low frequency transimpedance gain, time-constant τ_p and its pole frequency for the three circuits.

Circuit	f_p [MHz]	τ_p [ns]	A_v[dBΩ]
A	11.7	13.6	≅ 83.0
B	6.7	23.8	≅ 83.0
C	10.0	15.9	≅ 87.0

Regarding the stability of the TIA, a stability analysis was made for each circuit. Fig. 5.5 shows the obtained results.

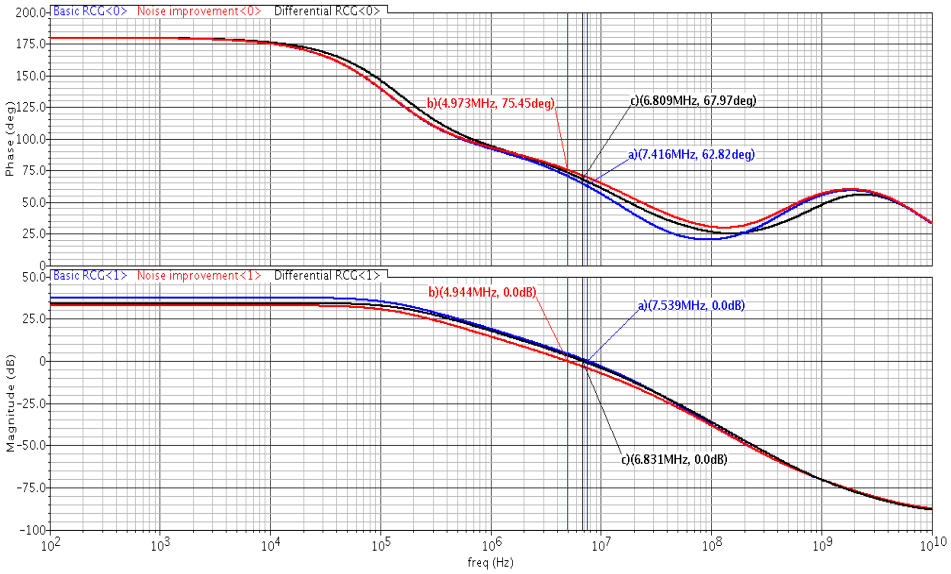

Figure 5.5 – Phase and magnitude Bode diagrams: a) Basic RCG; b) RCG with improved noise; c) Differential RCG.

The above was taken from the feedback loop between M_1 and the regulation stage. It can be seen that the three circuits are all stable presenting phase margins of $\phi_{M,A} = 62.48°$ at 7.54 MHz, $\phi_{M,B} = 75.53°$ at a.94 MHz and $\phi_{M,C} = 67.91°$ at 6.93 MHz. This means that the insertion of M_3 not only will reduce the overall noise level, as will be seen, but will also improve the stability of the TIA, which is desirable. The three TIAs linearity is shown if Fig. 5.6.

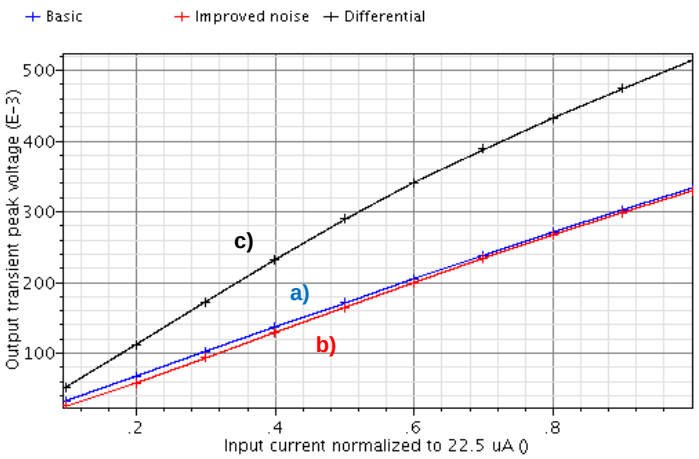

Figure 5.6 – Linearity for each circuit designed: a) Basic RCG; b) RCG with improved noise; c) Differential RCG.

Notice that, unlike the single-ended versions, in the case of the differential RCG TIA the linearity comes slightly affected. This suggests that the inverted output may have been poorly designed, since the linearity presents two clear slopes, being the first between $0.1I_{dm}$ and $0.6I_{dm}$ and the second between $0.6I_{dm}$ and I_{dm}.

Regarding the noise present at the TIAs output, one can find in Fig. 5.7 the noise response for each TIA. It can be easily seen that the Flicker noise corner will be situated at around 1 kHz for the three TIAs.

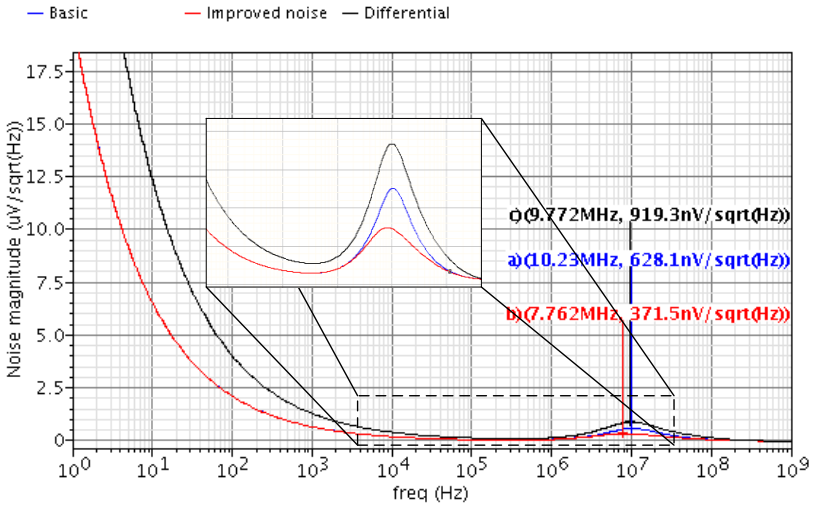

Figure 5.7 – Noise response of the TIAs with a SiPM.

In the above figure a spike can be seen around the 10 MHz region. As mentioned before, this spike has already been accounted for and it is related to the high value of C_d and the low frequency zero it produces. One fact of interest that can be observable in Fig. 5.7, is the fact that comparing the noise response of circuits A and B, one can notice that the spike present in circuit B has lower amplitude. This has been previously reasoned, and is inherent to the insertion of transistor M_3. From the above figure it can be seen that the peak noise voltage has been reduced by, at least, 41% when M_3 is included in the basic RCG TIA. The main noise contributors until 1 GHz are the ones expressed in Table 5.3, for each circuit. As expected, the thermal noise originated in M_2 is the dominant noise source present in the circuit, with around 60 % of the total noise in the output of all TIAs tested. This is something that gives strength to the fact that regardless M_1's thermal noise is of high-pass nature, its influence can be seen as negligible in the bandwidth of interest, as it was previously mentioned in chapter 3. Also negligible, is the contribution of the Flicker (1/*f*) noise, denoted by its highest contributor, $M_{2,1/f}$. Note that the total integrated noise is being seen in the interval between 1 kHz and 1 GHz.

Table 5.3 – Top five noise contributors in the three RCG TIAs, designed to operate with a SiPM at the input.

Device	Noise Contribution							
	Basic RCG		RCG with improved noise		Differential RCG			
					TIA core		Buffer output	
	(mV)	(%)	(mV)	(%)	(mV)	(%)	(mV)	(%)
M_2	2.485	62.03	1.767	57.31	3.954	63.97	3.498	63.43
M_{B2}	1.517	23.11	1.071	21.05	2.395	23.47	2.119	23.2
M_1	0.832	6.95	0.829	12.62	0.686	1.92	0.589	1.80
M_{Bb}	0.619	3.85	0.402	2.97	0.943	3.64	0.836	3.63
R_X	0.405	1.65	0.405	3.01	0.350	0.50	0.300	0.47
$M_{2,1/f}$	0.263	0.70	0.179	0.59	0.413	0.68	0.365	0.68
$v_{no,rms}$	3.156 mV		2.334 mV		4.944 mV		4.392 mV	

To verify the feasibility of the proposed differential version of the RCG TIA, a corner analysis is presented contemplating the output voltage, differential gain and stability of the TIA. The corners were defined by the 27 combinations between {"tt", "ss", "ff"; V_{DD} = 1.14, 1.2, 1.26; Temperature = -40º, 25º, 85º}. Note that for simplicity and since the differential version is the most critical, only this version has been subjected to the corner analysis. Regarding the output voltage, shown in Fig. 5.8, it can be seen that all the corners present a rising time below the stipulated 40 ns. In the figure below, t_0 denotes the instant of time in which the input signal starts to rise, while t_1 stands for the 40 ns limit. There is, however, one corner that has its peak amplitude relatively near 40 ns. This corner is set by {"ss"; 1.14 V; 85 ºC}. The importance of this corner can be made negligible since Fig. 5.8 refers to the buffer output. Therefore, no significant delay will be summed to this rising time.

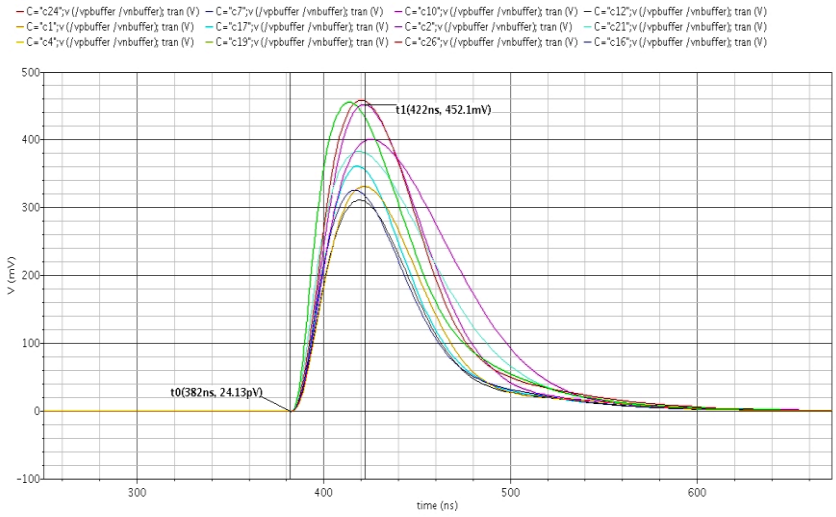

Figure 5.8 – Differential RCG TIA 27 corners output voltage.

An ac analysis was also made contemplating the differential gain of the TIA. The result can be seen in Fig. 5.9.

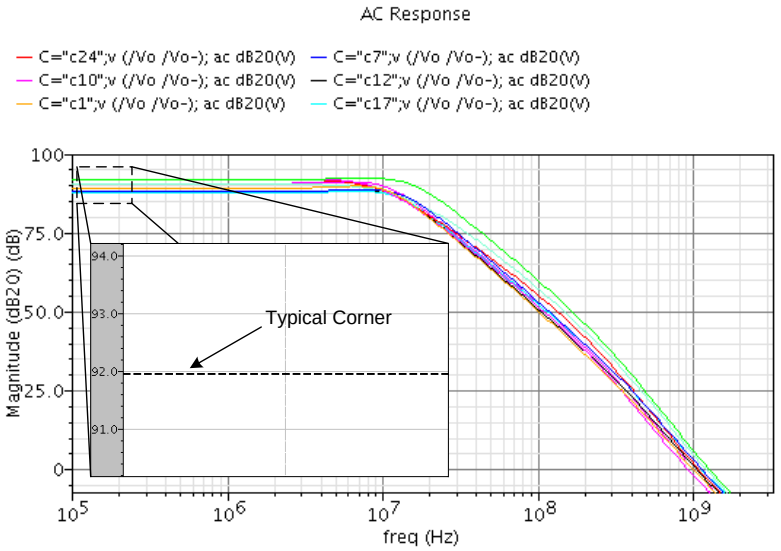

Figure 5.9 – Corner analysis for the differential transimpedance gain.

From the above it can be seen that the typical corner has a low frequency transimpedance gain around 92 dBΩ. The circuit presents a variation in its low frequency gain of -2 dB and +2 dB, which in deep-submicron technologies can be hard to achieve.

Regarding stability, Fig. 5.10 shows the phase and magnitude Bode diagrams for all the 27 corners. The difference between the best and worst phase margin is negligible, as such, the circuit presents itself to be stable for all the corners tested.

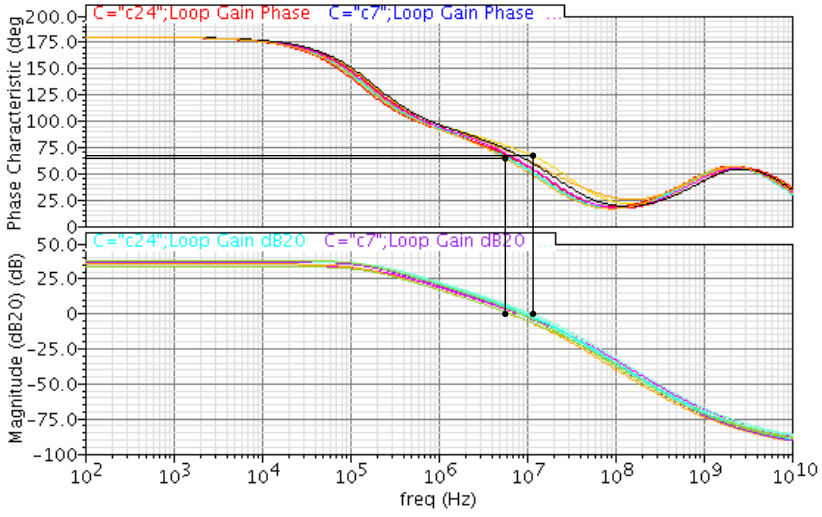

Figure 5.10 – Phase and magnitude Bode diagrams for all the 27 corners.

The last three plots shown prove that the differential RCG is quite robust to PVT variations. The output voltage peaking time, the differential transimpedance gain and the TIA's phase margin did not became too altered when the variations were accounted for, which suggests a good sizing of the TIA.

The differential RCG was submitted to a physical layout design, which can be seen in Fig. 5.11.

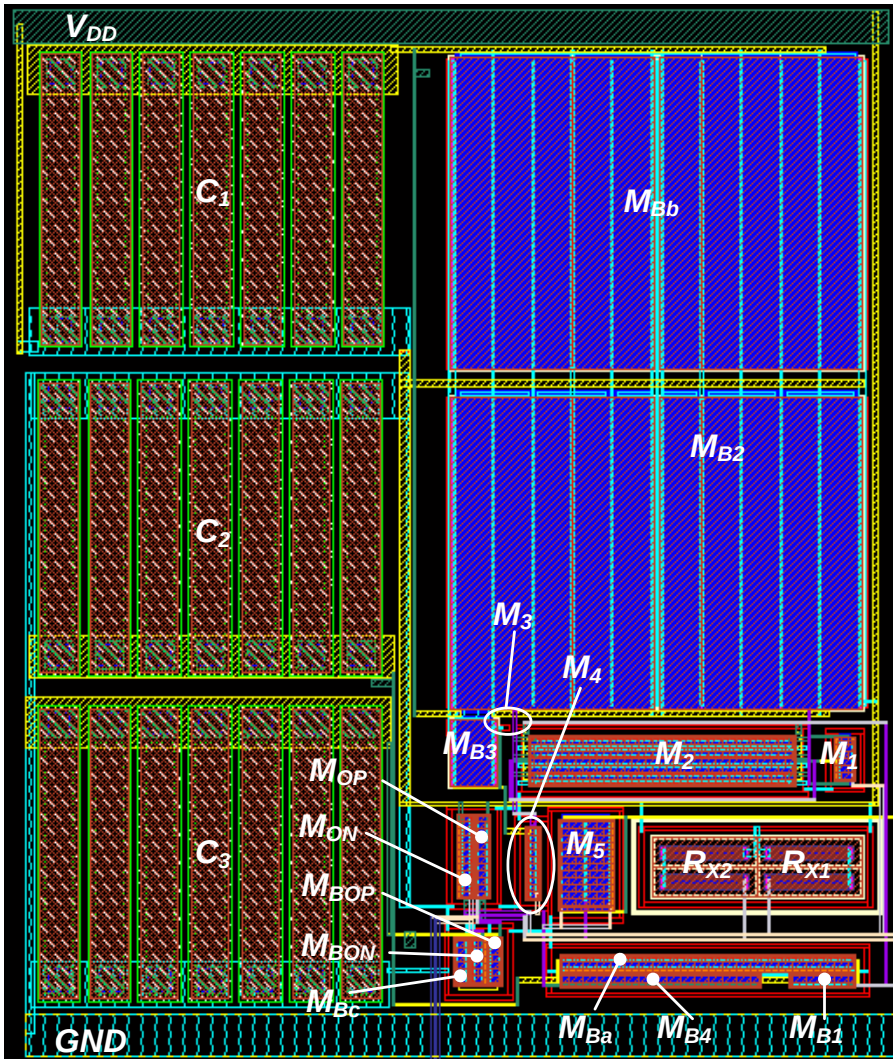

Figure 5.11 – Detail of the physical layout of the differential version of the RCG TIA

Current sources I_{B2} and I_{B3} were designed using a common-centroid technique in order to improve the current mirroring from transistor M_{Bb}. Note that transistor M_{B2} was partitioned into a 10-finger transistor, improving its layout aspect ratio.

All devices were involved in guard rings. This makes possible to improve the bulk noise originated at any given device. Even though not being the case here, this technique proves itself to be more effective in mixed signal circuit design, isolating the bulks of the digital and the analog

part of the circuit. Being the highest noise contributor, this technique is especially important in transistor M_2. This device was also partitioned into 5 fingers.

Capacitors C_1, C_2 and C_3 were added to help filtering the noise originated by the current sources. Note that these components occupy around 50% of the core area, each presenting a 1 pF capacitance value. In a n-channel ASIC these capacitors would not be replicated throughout every channel. Therefore there is no heavy penalty in using them.

For power supply distribution the metal layers used were metal 1, metal 2 and metal 3, given their higher capacitance to the bottom layer. For the connections between devices that did not transport any signal, the layers used were metal 3 and metal 4. Signal transporting connections between devices was accomplished using the layers of metal 4 to metal 8.

The core circuit of the TIA, including the noise suppressing capacitors, occupied an area of 143 μm × 118.2 μm, approximately 0.016 mm^2.

5.2. Design of a Low-voltage Feedback TIA with an APD at the Input

In this section a feedback TIA will be designed to operate in a radiation detector front-end context. The main goal with this design is to prove that this topology is impracticable with a PSD such as a SiPM, due to its higher output capacitance. In order to test the feasibility of the TIA, the two-stage fully differential inverter-based self-biased CMOS amplifier designed in [39], [40] was used. To make this amplifier suitable for this type of application, its bandwidth would have to be much higher, since in [39], [40], the main goal was to present the best possible Figure-of-Merit (FOM). Therefore, the amplifier used was subjected to a new sizing with the primary objective of maximizing its GBW. One other goal was to study a given number of low voltage techniques capable of reducing the amplifier power source voltage, accomplishing a better power consumption of the core circuit. The amplifier used is presented in Fig. 5.12.

The main interest in this section lies in proving that the same amplifier operates differently whether an APD or a SiPM is connected at the input and, therefore, a more detailed analysis of the proposed circuit can be found in Appendix C. Nonetheless, it can be seen by the above figure that each inverter cell is composed by transistors M_{12}, M_{13} and M_{22}, M_{23}. These are biased by current sources M_{11}, M_{14} and M_{21}, M_{24}, respectively. The Common-Mode Feedback (CMFB) circuits are both continuous- time CMFBs. In order to test the operation of the circuit in a low-voltage environment, techniques such as Bulk-driven, Dynamic Threshold MOS and Body-Biasing have been applied. The best results were achieved when applying a Body-Biasing voltage of 0.6 V to the Bulk terminal of every biasing current source. Note that for further information

regarding this, one must refer to Appendix C. In these conditions, a supply voltage of 0.8 V was achieved. Also, the GBW presented was around $B \approx 1.22$ GHz for a low frequency differential gain of $A_{v0} = 185.4$. In order to satisfy the rising time needed, equations (2.51), (2.52) and (2.53) must be respected.

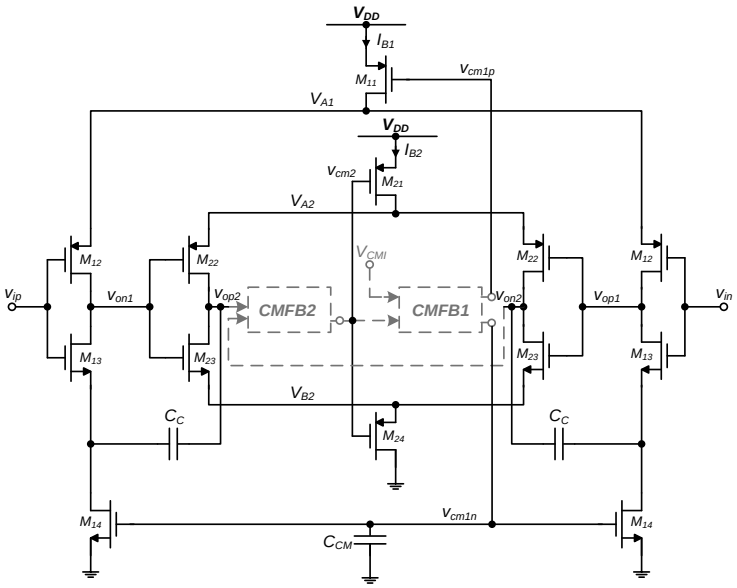

Figure 5.12 – Two-stage inverter-based self-biased CMOS amplifier.

It was previously established that the main differences between an APD and a SiPM were the output current amplitude and equivalent output capacitance. In the case of an APD it will be $I_{dm} = 2.25$ µA and $C_d = 10$ pF. Thus, from (2.51), (2.52) and (2.53) the values for the feedback resistor and capacitor were $R_f = 130$ kΩ and $C_f = 90$ fF. Given the dependence of C_d in R_F and C_F, if a SiPM was chosen it is easily observable that maintaining the same rising time, R_F would have to be, mandatorily, thirty times lower, while C_F would be thirty times higher, if the same amplifier was used. Since the transimpedance gain is given by the value of R_F, as can be seen in (2.49), the output voltage would be at least three times lower than in the case of the APD.

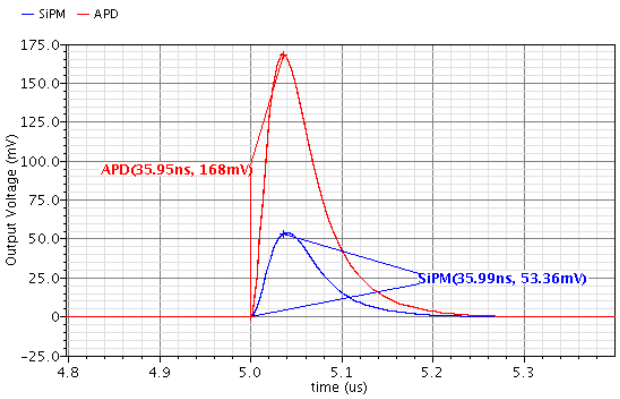

Figure 5.13 – Feedback TIA output voltage for the APD and SiPM.

Maintaining the same noise level, the SNR with a SiPM would be significantly lower, making this topology impracticable with the recently developed SiPM. In Fig. 5.12 the output voltage of the amplifier is shown for both the APD and the SiPM. In the above it can be seen that the output voltage with the SiPM is around one third lower than the one with the APD. The integrated noise voltage at the output between 1 kHz and 1 GHz was $v_{no,APD} = 1.55$ mV and $v_{no,SiPM} = 1.22$ mV. This will reflect an Signal-to-Noise ratio of $SNR_{APD} = 40.7$ dB and $SNR_{SiPM} = 32.8$ dB, respectively. This SNR value for the SiPM is manifestly low when compared to the ones of the RCG topology, as will be seen in the next section. Therefore, the RCG topology proves itself to present a much better alternative when a SiPM is intended to be used as a radiation detector. The complete study of the amplifier chosen for the realization of the feedback TIA can be seen in references [39], [40] and Appendix C.

5.3. Results Comparison and Final Remarks

In this section the reader can find a general comparison between the TIAs designed in this work and some previously designed TIAs regarding the same type of application. Therefore, the interest lies in evaluating the designed circuits' performances. For that effect, the results will contemplate the noise level, power consumption, output voltage amplitude and technology used in this work and in previously performed studies. In Table 5.4, the results obtained in reference studies are shown, while presenting the ones obtained with this work. References [8] and [10] used 350 nm technology with a supply voltage of 3.3 V. This made possible to achieve an output voltage amplitude of $V_{om} = 1$ V. This way, in order to make this work's results comparable, these will be shown in their original form and extrapolated to $V_{om} = 1$ V. It must also be noted that the SNR value is obtained by the ratio between V_{om} and v_{no}, in which the noise voltage corresponds to the simulated output noise.

From Table 5.4 it can be seen that the best SNR was achieved with the improved noise version of the TIA, regarding the SiPM at the input. Comparing to the basic RCG TIA, even though its output voltage is slightly reduced, the SNR is almost 3 dB higher. The differential proposed RCG version presents a lower SNR. This can be explained by the fact that in order to improve the linearity of the TIA, the load resistors were lowered when compared to the improved noise version. It is then expectable that in order to improve the linearity of the TIA the transimpedance gain will be lowered.

Table 5.4 – TIA comparison.

Circuit	***Technology***	***Supply***	***Power***	***Output Voltage V_{om}***	***Output Noise $v_{no,rms}$***		***SNR*** (dB)
					Theoretical	***Simulation***	
Feedback TIA (APD) [10]	350 nm	3.3 V	0.68 mW	1 V	7.5 mV	6.9 mV	43.22
RCG TIA (APD) [8]	350 nm	3.3 V	0.68 mW	1 V	6.5 mV	6.8 mV	43.35
RCG TIA (APD) [15]	130 nm	1.2 V	0.30 mW	232 mV	1.34 mV (5.71 mV)*	1.01 mV (4.31 mV)*	47.31
RCG TIA (SiPM) [7]	130 nm	1.2 V	0.34 mW	286 mV	3.15 mV (11 mV)*	3.01 mV (10.5 mV)*	39.57
RCG TIA ** (SiPM) Circ. A	130 nm	1.2 V	0.34 mW	335 mV	4.35 mV (12.96 mV)*	3.15 mV (9.39 mV)*	40.55
Improved noise RCG TIA** (SiPM) Circ. B	130 nm	1.2 V	0.34 mW	331 mV	1.66 mV (5.01 mV)*	2.33 mV (7.04 mV)*	43.05
Differential RCG TIA** (SiPM) Circ. C	130 nm	1.2 V	0.46 mW	513.3 mV	2.20 mV (4.28 mV)*	4.94 mV (9.62 mV)*	40.33
Feedback TIA** (APD) [appendix C]	130 nm	0.8 V	0.19 mW	168 mV	–	1.55 mV (9.2 mV)*	40.70
RF RCG TIA** (Mixer) [appendix B]	130 nm	1.2 V	0.30 mW	396.5 mV_{pp}	0.62 mV (1.56 mV)*	0.88 mV (2.21 mV)*	53.11

*Values extrapolated to an output voltage amplitude of V_{om} = 1V.

**Refers to the work presented here.

One aspect that has not been covered in the present work is the possibility of the RCG TIA to operate in a low voltage environment. Since the transimpedance gain is proportional to the load resistor, R_X, the latter has to be high, which would imply that it would present a high voltage drop. Thus, the supply voltage would not be sufficient to maintain a good margin for M_1's and I_{B1}'s V_{DS}, without lowering the transimpedance gain considerably. One solution that could be adapted would be the use of the TIA shown in chapter 5.2, with an APD, since it operates in a low voltage environment, with little power consumption. Note that this TIA's SNR is comparable to the remaining, designed in this work.

6. CONCLUSIONS AND FUTURE WORK

The importance of early detection of breast cancer has already been mentioned. Facing this, there has been a growing need of improving the existent medical imaging techniques in view of cancer detection. With the recent development of PSDs such as the SiPM, alternative radiation detector topologies must be studied. The work presented in this thesis reflects the breakthroughs recently undergone in medical imaging techniques, more precisely, in PET technologies. Under the radiation detection principle, we have studied the inclusion of a SiPM in a PET/PEM scanner front-end, with the RCG TIA topology.

Instead of the usual approach, which comprises a feedback TIA with an APD connected at its input, a study of the usage of a SiPM with the RCG TIA topology has been presented. When compared to an APD, the SiPM can provide a higher output current, allowing for the TIA core to present a higher output amplitude. This can possibly mean that the TIA core will present a faster response to the input signal, since it can have a lower number of cascaded amplifying stages. However, the SiPM also has a much higher output capacitance making it unsuitable for the feedback TIA topology, as it was shown in chapter 5.3.

The target application for the ASICs designed in this work is a PET/PEM scanner for medical imaging purposes. We have shown the basic physical principles behind this type of technology, as well as the requirements necessary to design a proper front-end for the system. Furthermore, the state of the art regarding TIAs for radiation detection has also been reviewed and succinctly characterized.

The main goal of the work presented here was to provide a detailed study of the RCG TIA topology. For that effect, the RCG circuit has been subjected to an extensive theoretical analysis, confirmed by simulations. Two RCG circuit variations are also proposed and studied. The first case contemplates a technique which allows for the output noise level to be reduced, while the second variation is referent to a proposed differential version of the circuit. The studied designed

versions of the RCG topology were sized and evaluated accordingly. We also provide a comparison between the work presented here and previous reference studies. The main results obtained with this thesis are the following:

- We derive two alternative versions of the RCG TIA topology. In the first version we aimed to lower the output noise with the insertion of more active devices. We accomplished a noise reduction of around 26 %, resulting in a SNR raise of around 2.6 dB. The increase in power consumption and area of this version are negligible when compared to the basic RCG topology. The second, a differential version, was accomplished by inserting one isolation and one amplification stage to the RCG core. In this version, given the differential nature of the circuit, the output amplitude is raised. However the output noise is also higher leading to the same SNR presented by the basic RCG version. For both versions the transimpedance and noise transfer functions are derived.
- We simulate the behavior of the RCG in a RF front-end environment, providing there is a basic passive mixer at the TIA's input. In this context, the TIA presents a high SNR value, as well as transimpedance gain, making proof of the versatility of the circuit.
- The RCG TIA must be designed differently whether a high or low output capacitance device is connected at its input. Therefore, we also show the sizings and design procedures considered. In the case of a low output capacitance device, the TIA's poles should be real, while in the case of a high output capacitance device the TIA performs better with complex conjugate poles.
- In order to prove the difficulty in realizing the radiation detector's front-end with a SiPM and a feedback TIA, a study is presented contemplating the differences in choosing an APD or a SiPM with a fully-differential OTA. In this study we aimed to realize a feedback TIA in a low voltage environment.
- We present the differential version's mask layout of the circuit ready to be implemented in a prototype RCG TIA, suitable for testing and measurements.

The results obtained with the solutions presented are comparable to both the reference studies and the usual approach which uses the feedback TIA with an APD. Regardless, the best results were obtained with the noise improvement version of the RCG. In this version, the output peak voltage achieved was $V_{om} = 331.4$ mV in a peaking time of $t_m = 37.08$ ns. The noise value at the output was $v_{no,rms} = 2.334$ mV, resulting in a SNR of 43.05 dB.

Future Work:

The work presented here is somewhat theoretical and, therefore, in the line of future work, the results obtained should be measured and validated by means of a test circuit and respective prototype. One other aspect regarding future work is the possibility of implementing techniques which would allow a further reduction in the output noise, improving the SNR of the TIA.

The TIAs designed in this work can be directly connected to the Analog-to-Digital Converter (ADC) designed in [41], disregarding the need of a post-voltage amplifier. Therefore, the usage of this configuration can be studied and tested with the respective prototypes.

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Appendix A

Miller's Theorem

In an arbitrary network, where an impedance Z is connecting two of its nodes as shown in Fig. A.1 a), the equivalent circuit in Fig. A.1 b) can be obtained.

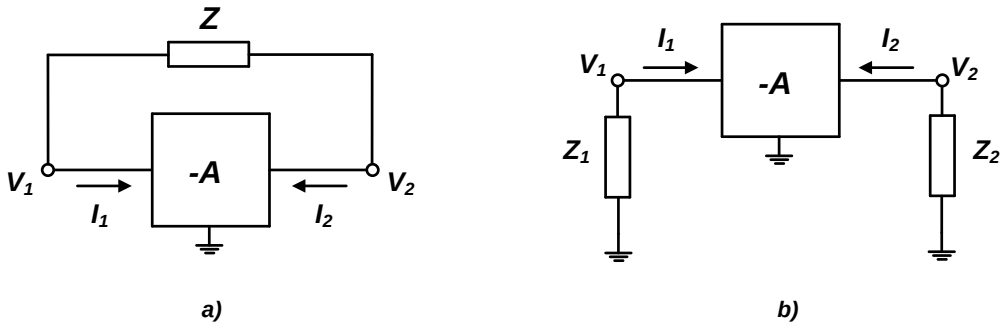

Figure A.1 – Miller's Theorem example application.

In this example the arbitrary network is composed by a linear inverting voltage gain block with gain $-A$, resulting $V_2 = -AV_1$. In Fig. A.1 a) currents I_1 and I_2 can be found, following

$$I_1 = -\frac{V_1}{Z}(A+1) \tag{A.1}$$

and

$$I_2 = \frac{V_1}{Z}(A+1). \tag{A.2}$$

Maintaining the voltages V_1 and V_2 in Fig. A.1 b), the currents can be expressed by

$$I_1 = -\frac{V_1}{Z_1} \tag{A.3}$$

and

$$I_2 = \frac{AV_1}{Z_2}. \tag{A.4}$$

If the currents I_1 and I_2 are the same in both equivalent figures, then

$$Z_1 = \frac{Z}{A+1} \tag{A.5}$$

$$Z_2 = Z\frac{A}{A+1}. \tag{A.6}$$

Note that assuming impedance Z as a capacitance, where $Z = 1/sC$, will make the equivalent Miller impedance at the input and output of the gain block also depend on capacities with values

$$C_1 = C(A+1) \tag{A.7}$$

and

$$C_2 = C\frac{A+1}{A}. \tag{A.8}$$

Therefore, it is safe to assume that whenever a capacity, C, is connected between the input and output of a hypothetical gain block, it will have an equivalent circuit, in which the gain block's input capacity will be the first multiplied by the gain of the circuit.

Appendix B

RF Receiver Front-end Simulation Results

In order to demonstrate the adaptability of the RCG TIA, it was proposed that the circuit was used in a RF front-end environment. For that effect, and for simplicity, the basic RCG TIA was chosen, as suggested in chapter 4.1. Thus, in this section, the interest lies in showing the input and output voltage variation, the circuit's linearity and its noise response. By using the sizing described in the respective section, it was obtained, as Fig. B.1 shows, an input voltage variation of $v_i \cong 906\ \mu V_{pp}$, lower than the $1\ mV_{pp}$ restriction pointed previously, in the RCG TIA with a mixer at its input. This voltage variation gives, by itself, enough room for the mixer output transistor to remain in the triode region. Such low variation is accomplished by maintaining the TIA's input impedance in a low level, since the lower is the latter, the smaller is the input equivalent voltage variation.

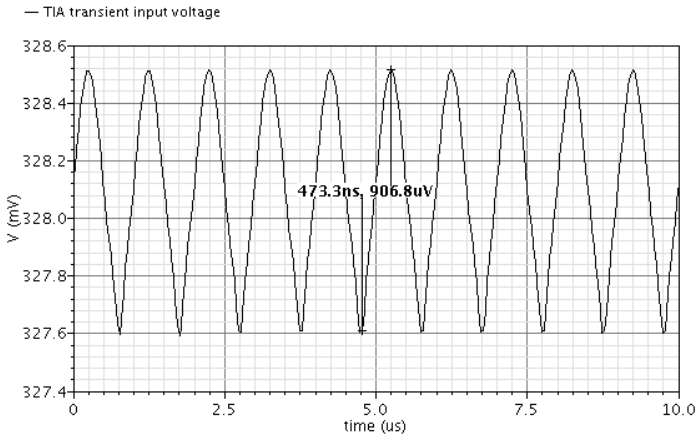

Figure B.1 – Basic RCG TIA input peak voltage variation.

The output voltage of the TIA is shown in Fig. B.2. With the sizing described, it was accomplished an output voltage of $v_o \cong 400\ mV_{pp}$. This is the expected value since the input signal was a sinusoidal current with 1 μA amplitude operating at 10 MHz and the transimpedance gain was $R_X = 200\ k\Omega$. Also, notice that, as expected, the output signal is centered around 0.6 V. This suggests that the amplifier has been sized correctly. Its high output voltage amplitude in the context of a RF front-end reinforces the versatility of this topology.

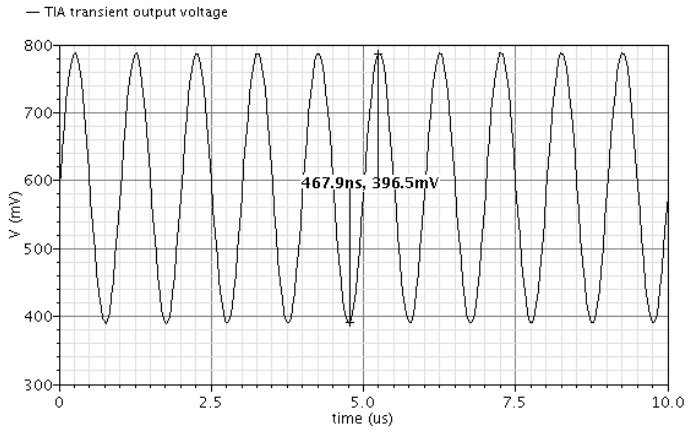

Figure B.2 – Basic RCG TIA output voltage.

In order to assure that the frequency response is the one predicted, an ac analysis at the TIA's output has been made. This is shown by Fig. B.3. In this figure, one can notice that the low frequency gain of the TIA, $A_V = 106$ dB, corresponds exactly to the value of R_X. The bandwidth of the TIA is given, as expected, by the regulation stage. In the figure below, one can identify the pole responsible for the bandwidth at $f_a = 18.6$ MHz. Note that $f_a$is related to the time-constant τ_a, which implies that $\tau_a \cong 45$ ns. In order to check the TIA's stability, a stability analysis in the local feedback loop has been made, resulting in a phase margin of $\phi_M = 59.4°$ at 267 MHz.

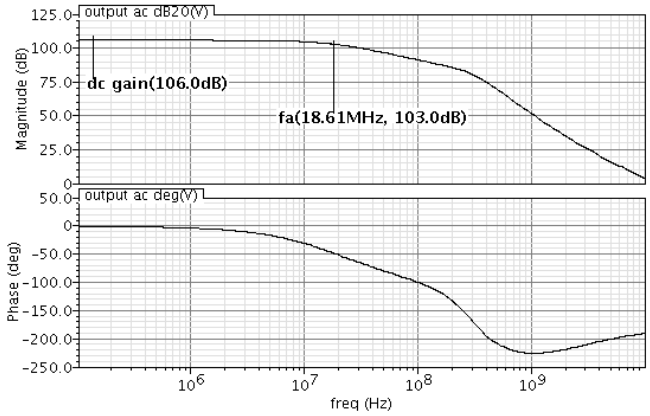

Figure B.3 – AC analysis at the output of the basic RCG with dc gain and M_2's pole.

The circuit's linearity is shown in Fig. B.4. It can be seen that the circuit presents a good and predictable linearity. For the effect, the input current varied between $10^{-1}I_m$ and $10^0 I_m$, resulting the given values of v_o. It was found that the output voltage responded linearly to the variation of the input current amplitude. In the case of the RCG with a mixer at the input, the low frequency gain is very close to R_X, meaning that the value of β is close to zero.

Regarding a noise analysis, Fig. B.5 shows the output noise response of the TIA. The Flicker noise corner can be found around 10 kHz as can be seen below. Here it can also be seen that since C_m has a very low value, the low frequency zero expressed by (3.36) has no influence in the noise response of the amplifier. In the case C_m was high valued, it would be expectable that the noise response would present a spike around 10 MHz.

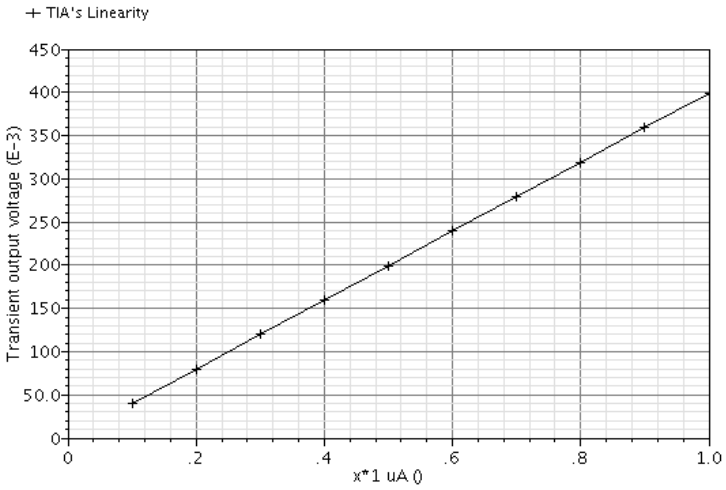

Figure B.4 – Basic RCG TIA's linearity with a mixer at the input.

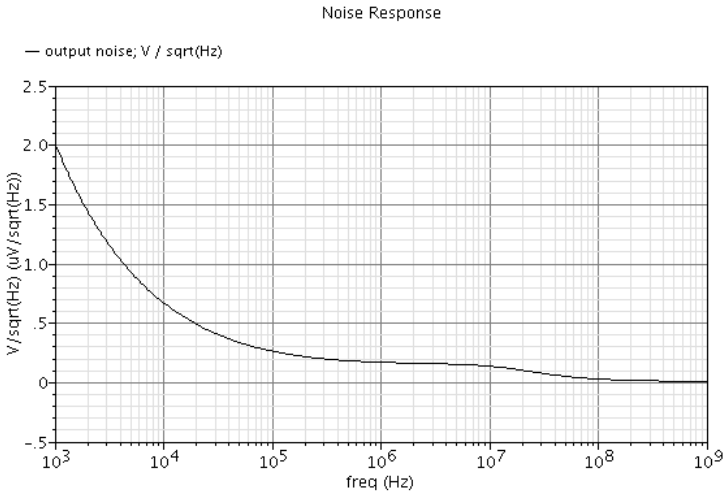

Figure B.5 – Noise response of the basic RCG TIA with a mixer at the input.

Since the value of C_m is low, the deduction of the noise transfer function presented in chapter 3.1 cannot be applied. One could make the deduction following a lower value of C_m. However, this study has already been done [8] and, therefore, is here neglected. The expression for the output rms noise voltage, in this case follows [8], [15]

$$v_{no,rms}^2 = kT\frac{R_X^2 C_m^2}{g_{m2}(\tau_1+\tau_2)\tau_1\tau_2} \tag{5.1}$$

in which $\tau_1 = C_m/g_{m1}A_{v0}$ and $\tau_2 = R_X C_X$. By simulation, the total integrated output noise, between 1 kHz and 1 GHz was found to be $v_{no,rms} = 0.924\,\text{mV}$, where the main five contributors were the ones expressed in Table B.1.

Table B.1 – Devices' noise contribution in the basic RCG TIA, designed to operate with a mixer at the input.

Device	Noise Contribution	
	Voltage (mV)	Percentage (%)
M_{B1}	0.732	62.84
R_X	0.314	11.54
M_1	0.292	10.00
M_2	0.124	1.81
M_{B2}	0.076	0.68
$M_{B1,1/f}$	0.202	4.78

In this case it was found that the main contributors, excluding the current sources, were the load resistor, R_X, and transistor M_1. As the value of C_m increases, it is expectable that the main noise contribution will come from transistor M_2, since the zero in (3.36) will decrease to a lower frequency, as will be seen in the following chapters.

Appendix C

Internal Report

Fully-Differential Low-Voltage Low-Power Inverter-Based Self-Biased CMOS Transimpedance Amplifier for Radiation Detectors

Fully-Differential Low-Voltage Low-Power Inverter-Based Self-Biased CMOS Transimpedance Amplifier for Radiation Detectors

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Abstract— **a Transimpedance Amplifier (TIA) is a device regularly used to convert the current pulse generated by a radiation detector into a suitable voltage, in terms of signal shape and amplitude. In this paper we are considering the application of a positron emission tomography (PET) scanner with the most commonly used light-sensitive devices inherent to these systems. We study the usage of a fully-differential, inverter-based, self-biased CMOS amplifier working as a feedback TIA in a low voltage environment. Results are shown when an Avalanche Photo-diode (APD) is connected to the TIA input while justifying why this topology does not work with a Silicon Photo-Multiplier (SiPM). The transimpedance and noise transfer functions of the TIA will be derived and we will show why, in this case, the devices' sizing must be driven by the gain-bandwidth product. In order to lower the power supply voltage, a study comprising various low-voltage techniques is presented. The proposed circuit was simulated in BSIM V3.3 models with UMC 130 nm technology on a 0.8 V power supply.**

Index Terms—**Transimpedance amplifier; radiation detectors; CMOS analog integrated circuit; self-biasing; fully differential; low voltage.**

I. INTRODUCTION

A Transimpedance Amplifier (TIA) is a device commonly used in applications requiring current-voltage conversion, and signal shaping. TIAs are widely used in optical communications systems [1]–[3], nuclear science, instrumentation and medical imaging [4]–[8]. In the latter case there is a radiation detector that must perform as a photo-sensitive device (PSD), converting any type of photo-dependent radiation into a correspondent current pulse. Two of the PSDs most commonly used are the avalanche photodiode (APD) and, more recently, the new silicon photo-multiplier (SiPM) [8], capable of higher output currents containing, as well, a higher output equivalent capacity.

The type of TIAs here designed are numerously used in Positron Emission Tomography (PET) scanners front-end. For example, in [6] a total of 6×32 -channel ASICs were developed, where the most challenging part of these ASICs was to design the 192 TIAs with the respective APDs at their inputs, since these TIAs are what determine the system's limits of performance. Each TIA should not exceed a power consumption of 1 mW, maintaining low noise level and the capability of pulse shaping. Here, the usage of a Feedback TIA in a PET scanner front-end is studied, showing the key constraints and requirements for the TIA design, such as output voltage amplitude and peaking time, noise level and power consumption.

In the present study, it is aimed to accomplish the feedback TIA through means of a fully-differential self-biased CMOS amplifier, based on a two-stage inverter topology [10], [11]. In a first analysis, considering the present application, the suitability of this amplifier is studied for both PSDs responsible for producing the input current pulse. Following the above, the insertion of low-voltage operation techniques such as Dynamic Threshold (DT) MOS, Body-Biasing (BB) and Bulk-Driven (BD) will be considered and properly analyzed. The challenge in reducing the operation voltage on the amplifier used lies in maintaining a high enough gain-bandwidth product (GBW), consistent with the specifications needed for the radiation detector, while accomplishing low-noise levels and high linearity.

The main objective of the work here presented is to evaluate the behavior of the mentioned topology in a low-voltage environment with both PSDs, therefore, the study of the amplifier itself, not only has already been done [10], [11], but it is not of paramount importance. Nonetheless, considerations on the behavior of the amplifier such as low frequency gain, pole-zero locations, common-mode feedback circuits or GBW will be given. Furthermore, high emphasis on the TIA and noise transfer functions will be given in order to justify the decisions regarding the amplifier's sizing. Also, a comparison between the low-voltage techniques mentioned above will be shown.

Providing the low-voltage operation of the amplifier and considering the application it is designed for, a reduction of around 33% in the power source voltage was achieved resulting a power consumption around 60% lower when compared to the design taken in [10]. The proposed circuit design was taken in BSIM V3.3 models with UMC 130 nm technology in a 0.8 V power supply.

II. RADIATION DETECTOR BASICS

At the front-end of a radiation detector there is usually a

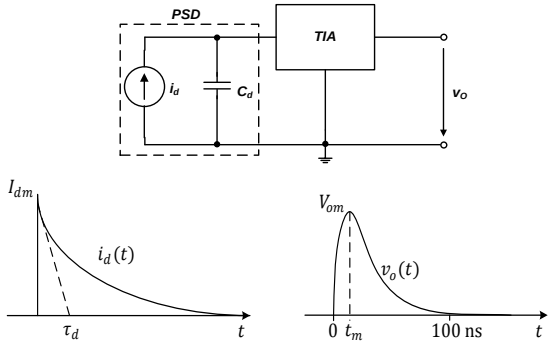

Fig. 1. Equivalent circuit of a PSD with TIA's input current $\boldsymbol{i_d(t)}$ and output voltage $\boldsymbol{v_o(t)}$.

scintillating crystal that emits a light pulse, when hit by radiation. In the case of a PET system, such radiation comes in the form of a gamma ray burst. The light pulse is then converted into an electric current pulse by means of a light sensitive device such as an APD or a SiPM. The TIA has the purpose of converting this current pulse into a voltage pulse with the desired shape and amplitude. Fig. 1 shows the equivalent circuit of an APD or, in the case of a SiPM, a simplified equivalent model, with their output current $i_d(t)$ and capacity C_d.

The current pulse $i_d(t)$ has a very fast rise (much lower than 1 ns in the case of a SiPM) [8] and, after reaching I_{dm}, which represents the maximum peak current, it starts decaying exponentially with a time constant τ_d. The output voltage must be as the one shown in Fig. 1. The variation of $v_o(t)$ must reach a peak value V_{om} in $t_m < 40$ ns. Such peaking time is a key restriction since we based the work here done in previous studies and systems [4]–[6], [9]. Nonetheless, we aimed t_m to be around 36 ns in order to contemplate any eventually high parasitic capacitances in the output buffer, which most definitely will influence the TIA's response. It must be noted that the exact shape of $v_o(t)$ is not important and, therefore, we are more interested in maintaining a good linearity between I_{dm} and V_{om}.

The PSD output current and capacity vary whether an APD or a SiPM is used. In the case of an APD we considered a peak current of $I_{dm} = 2.25$ µA and an output capacity of $C_d = 10$ pF. The more recent SiPM is capable of an output current one order of magnitude higher, containing as well a higher output capacity [4]. By this, for the SiPM we considered $I_{dm} = 22{,}5$ µA and $C_d = 300$ pF. The output voltage must reach $V_{om} = 1$ V of amplitude but, because of the low power characterization of the circuit, such amplitude is impossible to be obtained and, therefore, a post-voltage amplifier is needed. It has been previously found that with these values and with the noise level obtained, it is possible to obtain a resolution of 1 to 2 mm in a mammography examination lasting 5 minutes using a safe dose of radiation [4], [5].

III. Two-Stage Self-Biased Amplifier

The main focus in the present section is to show a circuit description of the amplifier under study and provide a brief and concise analysis in the behavior of the proposed solution.

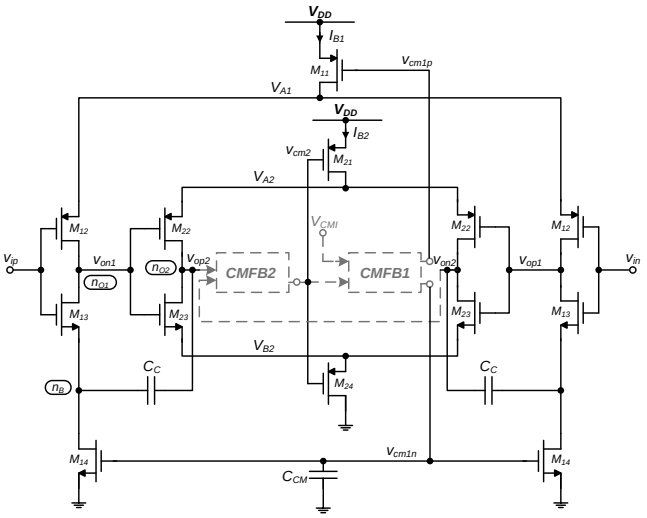

Fig. 2. Two-stage inverter-based self-biased CMOS amplifier.

A. Amplifier Description

The circuit under study consists in the fully-differential two-stage inverter-based self-biased CMOS amplifier depicted in Fig. 2. Basically, the proposed topology consists of two cascaded inverter stages with approximately the same topology. The input stage is accomplished through a differential pair, where each input is made possible by using a CMOS inverter (M_{12} and M_{13}), connected to a biasing current source, M_{11}, and the respective active load, M_{14} (voltage controlled resistor). The output stage has an identical topology where the inverter differential pair is constituted by transistors M_{22} and M_{23} with the respective biasing current source, M_{21}, and voltage controlled resistor, M_{24}. Note that, contrarily to the first stage, the second stage's differential pair has its NMOS devices' sources connected together. In the input stage, these latter are separated in order to enable the connection of the compensation capacitors, C_C, avoiding this way, the use of the inefficient Miller compensation [10]. In both stages the Common Mode (CM) level and biasing are controlled by the respective biasing current sources and voltage controlled resistors.

The Common Mode Feedback (CMFB) circuits are shown in Fig. 3. These have the objective of regulating the CM level while biasing the whole amplifier. The circuit responsible for producing the bias voltages in the output stage, $CMFB_2$, depicted in Fig. 3 (a), is realized through a continuous-time RC circuit. This circuit has the purpose of producing the $v_{cm2} = (v_{op2} + v_{on2})/2$ voltage, which directly controls the value of the second stage biasing current (M_{21}), the value of the active load resistor (M_{24}) and, finally, generates the biasing control voltage of the first stage. In fig. 3 (b) the $CMFB_1$ circuit is shown. This circuit consists in an inverter-based differential pair, where v_{cm2} is compared to a constant voltage (V_{CMI}), in order to bias the first stage's current source and voltage controlled resistors, through voltages v_{cm1p} and v_{cm1n}, respectively. The voltage V_{CMI} can be provided by a bandgap circuit and the active devices in $CMFB_1$, M_{31} and M_{32}, are downscaled versions of transistors M_{22} and M_{23}.

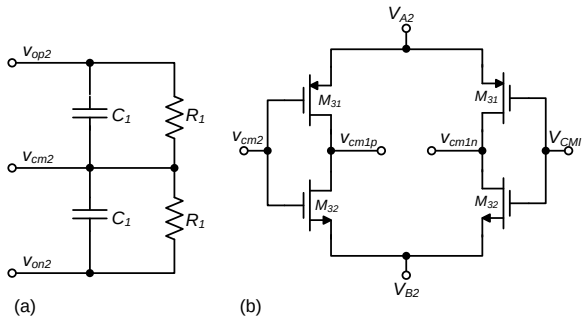

Fig. 3. CMFB circuits: (a) Second stage continuous time CMFB ($CMFB_2$); First stage continuous time CMFB ($CMFB_1$).

Self biasing voltages are connected to the main amplifier through a negative feedback loop, reducing therefore, the effects of process, supply voltage, temperature (PVT) and parameter variations. In order to exemplify the compensation on supply voltage variations, consider the following: assuming that v_{op1} and v_{on1}have already been established, if V_{DD} suffers an increase, then V_{SG21}will also increase. This will force the second stage biasing current (the current that passes through the drain of M_{21}), I_{B2}, to raise, since the latter is proportional to the first. As the current in the output inverter grows higher, the output CM voltage will also suffer a proportional increase, raising the value of v_{cm2}voltage, forcing the value of V_{SG21} to remain constant [10], compensating the increase of V_{DD} . Compensation in process and temperature variations work in a similar way, through the negative feedback loop. The fact that the amplifier is completely complementary (half PMOS and half NMOS) implies that PVT variation effects are furthermore minimized.

B. Circuit Analysis

As stated before, the main focus of the present study is to evaluate the present amplifier circuit when working as a TIA. Therefore, there will only be considered a light circuit analysis, providing that the concepts necessary to describe the behavior of the TIA, are well defined. An extensive study of this amplifier has already been provided. Assuming previously done work [10], [11], and by defining the equivalent capacitances in nodes n_{O1} and n_{O2} as

$$C_{O1} = C_{gd1} + C_{db1} + C_{gs2} + C_{gd2} \tag{1}$$

and

$$C_{O2} = C_{gd2} + C_{db2} + C_C + C_L \tag{2}$$

respectively, where C_L represents the output load capacity, and by defining the equivalent capacitance and transconductance, g_B, in node n_B as being

$$C_B = C_{gd14} + C_{db14} + C_{gs13} + C_{sb13} + C_C \tag{3}$$

$$g_B = g_{ds13} + g_{ds14} + g_{m13} \approx g_{ds14} + g_{m13} \tag{4}$$

one can find the expression for the low frequency open-loop differential gain, A_{V0}, by analyzing the behavioral signal path model [10], which can be described by

$$A_{V0} = \frac{g_{m2}(g_{m13}^2 - g_{m1}g_B)}{g_{ds2}(g_{ds13}g_{m13} - g_{ds1}g_B)} \tag{5}$$

where for each g_{mX}(or g_{dsX}) the value understood is $g_{mX} = g_{mX2} + g_{mX3}, X = \{1, 2\}$. To a good approximation, A_{V0} can be given by the cascaded gain of each inverter stage, resulting

$$A_{V0} = \frac{g_{m1}}{g_{ds1}} \times \frac{g_{m2}}{g_{ds2}}. \tag{6}$$

Regarding the frequency response of the amplifier, it can be verified that the amplifier has a dominant pole (7), a negative zero (8) and a pair of complex conjugated poles.

$$\omega_{p1} = \frac{g_{ds2}(g_{ds13}g_{m13} - g_{ds1}g_B)}{C_C g_{m13} g_{m2} + g_B \begin{pmatrix} C_{O2}g_{ds1} + C_{O1}g_{ds2} \\ + C_{gd2}g_{m2} \end{pmatrix}} \tag{7}$$

$$\omega_z = \frac{g_{m13}^2 g_{m1}^{-1} - g_B}{C_B} \tag{8}$$

The complex conjugated poles natural frequency and quality factor are represented through (9) and (10), respectively.

$$Q_{p2,3} = \frac{\sqrt{C_{O1}C_{O2}C_B \begin{pmatrix} g_B(C_{O2}g_{ds1} + C_{gd2}g_{m2}) + \\ C_C g_{m13} g_{m2} \end{pmatrix}}}{C_{O2}(g_B C_{O1} + g_{ds1}C_B) + C_{gd2}C_B g_{m2}()} \tag{9}$$

$$\omega_{n2,3} = \sqrt{\frac{g_B(C_{O2}g_{ds1} + C_{O1}g_{ds2} + C_{gd2}g_{m2}) + C_C g_{m13} g_{m2}}{C_{O1}C_B C_{O2}}} \tag{10}$$

This way, through (5) and (7), becomes possible to find the gain-bandwidth product (GBW), B,

$$2\pi B = \frac{g_{m2}(g_{m1}g_B - g_{m13}^2)}{g_B(C_{O2}g_{ds1} + C_{O1}g_{ds2} + C_{gd2}g_{m2}) + C_C g_{m13} g_{m2}} \tag{11}$$

IV. Transimpedance and Noise Transfer Functions

In the present section the interest remains in finding a transimpedance function and a noise transfer function for the TIA realized with the amplifier described.

A. Transimpedance Function

As was previously seen, the amplifier used has limited low frequency gain and a dominant pole. The open-loop gain can then be expressed as

$$A_V(s) = \frac{A_{V0}}{1 + s\tau_a} \tag{12}$$

where A_{V0} is the low frequency open-loop differential gain and $\tau_a = 2\pi/\omega_{p1}$is the time constant associated to the dominant pole. The gain-bandwidth product of the amplifier (11), B, can be expressed as

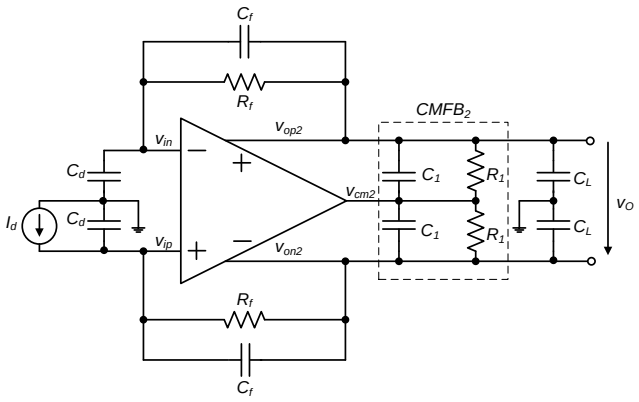

Fig. 4. Feedback TIA with capacitive load.

$$B = \frac{A_{V0}}{\tau_a} \tag{13}$$

Although in an ideal amplifier *B* would tend to infinity, in our amplifier this value is quite limited. This means that its magnitude is comparable to the remaining time-constants present in the circuit, which is highly undesirable.

The pulse shaping performed by the TIA depends on its transimpedance function, which represents the network responsible for current-to-voltage conversion. Previous studies [4]-[6], have shown that in order to obtain the required pulse shaping, the transimpedance function must be as the following.

$$\frac{V_o(s)}{I_d(s)} = \frac{R_m}{(1+s\tau_1)(1+s\tau_2)} \tag{14}$$

This can be obtained if the time-constants are associated to two real poles. In order to find a peaking time below 40 ns the time-constants must be lower than 20 ns and the following must be fulfilled.

$$\tau_1 + \tau_2 \approx 20 \text{ ns} \tag{15a}$$

$$\tau_1\tau_2 \approx 0.1 \text{ fs} \tag{15b}$$

Fig. 4 shows the feedback TIA with the amplifier used. It must be noted that the output of the TIA must still be connected to an output buffer and a post-voltage amplifier in order to elevate the output voltage to an acceptable level.

The transimpedance function (16) can be obtained by inspection where, for simplicity, only half circuit is analyzed.

$$V_o\left(1+\frac{1}{A_v}\right)\left(\frac{1}{R_f}+sC_f\right)+\frac{V_o}{A_v}sC_d = -I_d \tag{16}$$

By taking into account that $A_{V0} \gg 1$ the following transimpedance function (17) can be obtained.

$$\frac{V_o}{I_d} = \frac{-R_f}{s^2R_fC_dB^{-1} + s\left(R_f\left(C_f + C_dA_{v0}^{-1}\right) + B^{-1}\right) + 1} \tag{17}$$

If the dominator of the transimpedance function is compared to (14) the values of the feedback resistor and capacitor can be found and, as such, it can be easily seen that they are both dependent on the gain-bandwidth product,

$$C_f = \frac{k - A_{v0}^{-1}}{1-k}C_d \tag{18}$$

$$R_f = \frac{\tau_1\tau_2}{B^{-1}C_d} \times \frac{1-k}{1-A_{v0}^{-1}} \tag{19}$$

where $k = (\tau_1 + \tau_2 - B^{-1})/B\tau_1\tau_2$. From the above it can be seen that maintaining the same value of B, the value of the low frequency transimpedance gain, R_f , will decrease as C_d increases. This is important in the sense that since the amplifier used has limited GBW the feasibility of the TIA with a high capacity PSD such as a SiPM becomes useless. In a practical sense, the fact that $R_f$is low valued with the SiPM, means that the output signal amplitude will be very low, while maintaining the same noise level. This will make the signal-to-noise ratio (SNR) lower and non-suitable for the application it is designed for. Another factor to account for, is the fact that C_f will have to be higher, since it is proportional to C_d, occupying a much larger area (at least one order of magnitude higher).

B. Noise Transfer Function

In the noise transfer function derivation, it is assumed that the amplifier's input transistors (first stage inverter) noise contribution is dominant. In such case, it is safe to assume that the noise generated within the amplifier can be represented by an equivalent input voltage source, V_{na}, in series with the input of the amplifier [4]. The thermal noise therefore generated, can then be represented by a current noise source in parallel with the drain and source of the input inverter [12], which can be replaced by a voltage noise source in series with the gate of the referred devices. This source's spectral density is equal to the one of the thermal noise current source divided by the device's squared transconductance thus, regarding the amplifier, only the equivalent input noise voltage is considered, with a spectral density that follows

$$\overline{v_{na}^2} = 4kT\gamma g_{m1}^{-1} \tag{20}$$

where g_{m1} is the transconductance associated to the input inverter, k is the Boltzmann's constant, T is the absolute temperature and γ, in the present case, equals unity since sub-micron dimension are being used.

Concerning Flicker $(1/f)$ noise, since the TIA is wideband, its contribution can be neglected, making the thermal (white) noise dominant. From simulations, the Flicker noise was found to have its corner at around 10 kHz, making the integrated flicker noise virtually negligible. In order to minimize the noise level at the TIA's input, it can be seen from (20) that g_{m1} must be high. Ideally, contemplating a trade-off between noise and area, in previous studies [4], [5] it was established that the input stage inverters should have transistors wide enough to make $g_{m1} = 5$ mS , reducing the overall integrated noise. However, in the present design, such value is extremely high and hard to accomplish. This is motivated by the low supply voltage of the amplifier, which reduces the current that passes through the first stage inverter, diminishing the value of g_{m1}.

The noise transfer function of the feedback TIA has already been extensively studied [4], [1] and, as such, the interest here

Table I. Amplifier's Devices Sizing and Biasing

Device	W/L [µm]	I_D [µA]*	${g_m}/{g_{ds}}$*	${V_{DS}}/{V_{DSAT}}$*
M_{11}	10/0.28	56.4	2.41	0.76
M_{12}	55/0.12	28.2	11.03	4.48
M_{13}	12/0.12	28.2	12.53	6.67
M_{14}	0.5/0.12	28.2	0.14	0.24
M_{21}	71.44/0.36	186	0.30	0.26
M_{22}	36.3/0.14	77	14.74	3.90
M_{23}	20/0.15	77	20.08	5.83
M_{24}	64/1.16	186	0.23	0.19
$M_{31a,b}$	9.12/0.14	17.5; 14.5	14.8; 1.7	4.96; 0.68
$M_{32a,b}$	4.96/0.15	17.5; 14.5	20.5; 22.9	6.16; 11.64
C_C	0.15 pF			
C_{CM}	0.5 pF			

*Simulated values for V_{DD} = 0.8 V

remains in showing and comparing the results obtained. The noise transfer function follows the form

$$V_{no,rms}^2 = \frac{R_f^2 C_d^2 kT}{g_{m1}(\tau_1 + \tau_2)\tau_1\tau_2}. \quad (21)$$

As mentioned before, the total integrated noise voltage is inversely proportional to g_{m1} and since the latter is low valued, for reasons previously mentioned, it is expected that the noise voltage will be higher when compared to previous studies, deteriorating the SNR value.

The contribution of the noise generated by R_f can be deducted and compared to the contribution of the amplifier, but since the dc current that passes through R_f is relatively small, its noise contribution can be made negligible if the resistor is high valued [1].

V. Low Voltage Design and Sizing

In previous sections the importance of having a high enough GBW has been well established. In the present design it is of the best interest to accomplish a device sizing that makes the GBW suitable for our application. For this reason, the sizing here presented for the amplifier is different of the ones presented before [10], [11], where lower GBWs were obtained. In the present sizing all stages' current sources and voltage controlled resistors are operating either in triode or saturation/triode boundary regions. The transistors that compose the inverter cells, in either stages, have relatively low overdrive voltages, V_{DSAT}, which means that these devices are operating in moderate inversion. Table I resumes the aspect ratios chosen, drain current, each transistor intrinsic gain and operating region.

In order to accomplish a reduction in the power source voltage of the amplifier, facing previous sizings ($V_{DD} = 1.2$ V) [10], [11], the three previously referred techniques were studied. The behavior of the amplifier, in terms of GBW and phase margin, ϕ_M, can be seen in Fig. 5. Note that regarding Bulk-Driven technique no curves are shown. This relates to the fact that with this technique, the phase margin was always kept below 45º, independently of the power source voltage applied

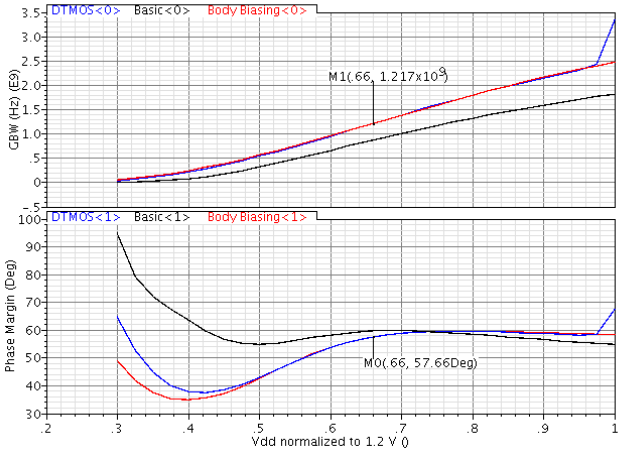

Fig. 5. Amplifier's GBW and phase margin response to large variations of V_{DD} with both techniques under study.

and, as such, it was opted to neglect this technique. The curve related to the tag "Basic" represents the amplifier's behavior with no technique applied at all.

Fig. 5 shows that the differences between the two techniques shown are negligible and, therefore, any of them could be chosen. The option was to apply a Body Biasing voltage of 0.6 V to all biasing current sources, M_{11} and M_{21}, and voltage controlled resistors, M_{14} and M_{24}. Basically, by applying a voltage to a bulk that was connected to either ground, in the case of an NMOS, or V_{DD}, in the case a PMOS, means that we are inserting body effect in that device and in fact lowering its g_m. If one takes into account that these devices are operating as dc current sources and that g_m is an incremental parameter (dependent on the small signal behavior), the lowering in the transconductance brings no harm. In fact, by using this technique, the threshold voltage, V_t, can be lowered (22) to V_{th}, which means the device will start conducting with lower V_{GS} [13].

$$V_{th} = V_{t0} + \gamma\left(\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}\right) \quad (22)$$

In the above, $V_{th} = V_{t0} = V_t$ when $v_{SB} = 0$ V, γ stands for the body effect coefficient (typically 0.5 $V^{1/2}$), and ϕ_f represents the Fermi potential ($2\phi_f \approx 0.6$ V). In Fig. 5 a value of $V_{DD} = 0.8$ V was chosen, which led to a gain-bandwidth product of $B \approx 1.22$ GHz and $\phi_M = 57.66$ °. The value of the low frequency open-loop gain was obtained by simulation, respecting a stability analysis, and was $A_{V0} = 185.4$. In order to satisfy (15), (18) and (19) the values obtained resulted in $R_F \approx 130$ kΩ and $C_F \approx 90$ fF. The values of R_1, C_1 and C_L are, respectively, 100 kΩ and 100 fF. It was estimated that the load capacitance should not be too large, since it only represents a narrow output buffer equivalent capacity.

VI. Simulation Results

Given the sizings described above, the expected output voltage amplitude and rising time were obtained. In Fig. 6, the output voltage can be seen, with $V_{om} = 172.2$ mV in t_m around 37 ns. Note that this voltage is completely differential, thus balanced,

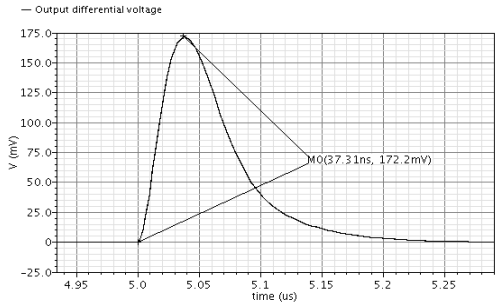

Fig. 6. Output differential voltage.

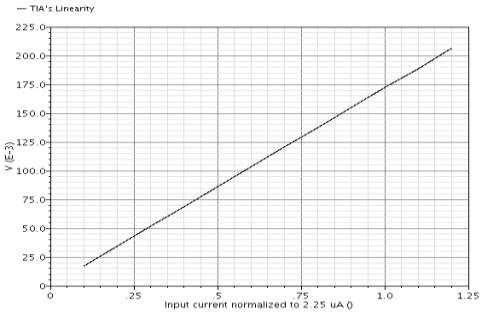

Fig. 7. Circuit's linearity.

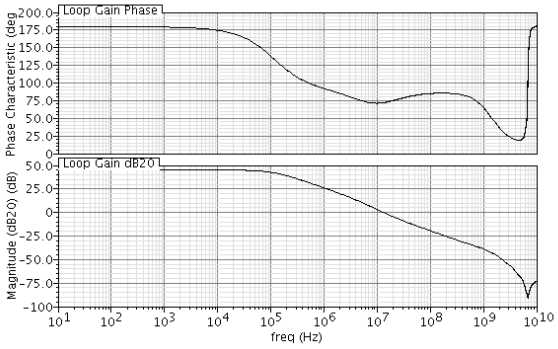

Fig. 8. Circuit's phase and magnitude Bode diagrams.

which simplifies the process of buffering and applying to a differential-input analog-to-digital converter. The shape of the output signal is also as expected, providing a good and predictable linearity. The circuit's linearity is shown in Fig. 7, where the input signal varied from 0.1 I_{dm} to 1.25 I_{dm}. In order to assure for the circuit's stability, Fig. 8 shows the Bode plots with the feedback loop provided. It can be seen that the phase margin is above 70º which reinforces the stability of the circuit. The output total integrated noise from 1 kHz to 1 GHz was $v_{no} = 1.55$ mV, which led to a signal-to-noise ratio of 40.9 dB.

VII. Conclusions

In the present work, the usage of a fully-differential, low-voltage, low-power, inverter-based, self-biased CMOS amplifier operating as a TIA was studied. The transimpedance function showed that with the amplifier studied, the usage of the TIA with a SiPM at the input is highly inefficient, if not impossible. Regarding an APD at the input, simulations showed a performance near the state of the art, with the plus of low voltage operation. The circuit here described also occupied low area, since minimum channel lengths were used. Table II shows a comparison for the designed circuit with other previously designed TIAs, meant to operate with APDs at their inputs.

Table II. TIA With APD at the Input Comparison.

TIA	Tech. (µm)	Supply (V)	Power (mW)	Output Noise (mV)	SNR (dB)
[4]	0.35	3.3	0.68	6.8	43.4
[6]	0.35	3.3	0.68	6.9	43.2
[9]	0.13	1.2	0.30	4.3*	47.3
This Work	**0.13**	**0.8**	**0.19**	**9.0***	**40.9**

*Values extrapolated for an output amplitude of 1 V.

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Appendix D

Published Papers

Regulated Common-Gate Transimpedance Amplifier for Radiation Detectors and Receivers

2014, IEEE International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)

Regulated Common-Gate Transimpedance Amplifier for Radiation Detectors and Receivers

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Abstract— **A Transimpedance Amplifier (TIA) is a device commonly used in applications, which requires current-voltage conversion and signal shaping. The most commonly used solution is an Avalanche Photo-Diode (APD) as radiation detector with a feedback TIA, but since the upcoming of the most recent Silicon Photo-Multiplier (SiPM), other TIA topologies have proven to be good alternatives. Our main objective in this paper is to show, evaluate and compare the behavior of a regulated common-gate (RCG) TIA when the light sensitive device is an APD or a SiPM. We will also study the usage of this circuit in a RF front-end, providing there is a passive mixer at the TIA's input. The proposed circuit is simulated with standard CMOS technology (UMC 130 nm), using 1.2 V power supply.**

Index Terms—**Transimpedance Amplifiers, radiation detectors, avalanche photo-diodes, silicon photo-multipliers.**

I. Introduction

A Transimpedance Amplifier (TIA) is a device commonly used in applications requiring current-voltage conversion, and signal shaping. TIAs are widely used in optical communications systems [1]–[3], nuclear science, instrumentation and medical imaging [4]–[8]. In the latter case there is a radiation detector that must perform as a photo-sensitive device (PSD), converting any type of photo-dependent radiation into a correspondent current pulse. Two of the PSDs most commonly used are the avalanche photodiode (APD) and, more recently, the new silicon photo-multiplier (SiPM) [8], capable of higher output currents, containing as well a higher output equivalent capacity.

The type of TIAs here designed are numerously used in Positron Emission Tomography (PET) scanners front-end. For example, in [6] a total of 6×32 -channel ASICs were developed, where the most challenging part of these ASICs was to design the 192 TIAs with the respective APDs at their inputs, since these TIAs are what determine the system's limits of performance. Each TIA should not exceed a power consumption of 1 mW, maintaining low noise level and the capability of pulse shaping. Here, we study the usage of a regulated common-gate (RCG) TIA in a RF and PET scanner front-end, showing the key constraints and requirements for the TIA design, such as output voltage amplitude and peaking time, noise level and power consumption, both as radiation detector and at the output of a passive mixer.

In this paper we will present three different implementations of the RCG circuit topology: 1) APD at the input, 2) SiPM at the input, and 3) RF mixer at the input. Simulation results in a standard CMOS 130 nm for comparison are presented.

II. Radiation Detector Basics

At the front-end of a radiation detector there is a scintillating crystal that emits a light pulse, when hit by radiation [4, 5]. The light pulse is then converted into a current pulse by a light sensitive device such as an APD [4] or a SiPM [5]. The TIA has the purpose of converting this current pulse into a voltage pulse with the desired shape and amplitude. The equivalent circuit of an APD or a SiPM, is a current source $i_d(t)$ in parallel with a capacity C_d as shown in Fig. 1.

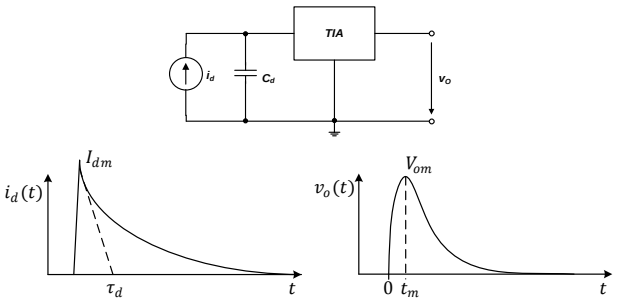

Fig. 1. Equivalent circuit of a PSD with TIA's input current $\boldsymbol{i_d(t)}$ and output voltage $\boldsymbol{v_o(t)}$ [4].

The current pulse $i_d(t)$ has a very fast rise (much lower than 1 ns in the case of a SiPM) [8] and, after reaching I_{dm} starts decaying exponentially with a time constant τ_d. The output voltage must be as the one shown in Fig. 1. The variation of $v_o(t)$ must reach a peak value V_{om} in $t_m < 40$ ns [4]–[6]. It must be noted that the exact shape of $v_o(t)$ is not important and, therefore, we are more interested in maintaining a good linearity between I_{dm} and V_{om}.

The PSD output current and capacity vary whether an APD or a SiPM is used. In the case of an APD we considered a peak current of $I_{dm} = 2.25$ µA and an output capacity of $C_d = 10$ pF. The more recent SiPM is capable of an output current one order of magnitude higher, as well as a higher output

capacity [4]. By this, for the SiPM we considered $I_{dm} = 22{,}5\ \mu A$ and $C_d = 300$ pF[5].

III. Passive Mixer

Mixers can be of complex design depending on their applications, being distinguished between active or passive devices, depending on providing, or not, amplification [9]. We have considered a passive mixer which consists on a switching device controlled by a Local Oscillator (LO). When in the triode region, a MOS transistor can perform as a switch if the remaining resistances present in the circuit are of much higher value than the equivalent resistance of the MOS conduction channel [10], as shown by Fig. 2. In these conditions, the device will operate as an open switch every time V_{LO} is at low level and as a closed switch, with an equivalent R_{DS} resistance, when V_{LO} is at high level. The load resistor R_L seen above only has the function of converting the mixer's output current into an output voltage. In our design this resistor is replaced with the TIA input impedance in parallel with the mixer's output capacity.

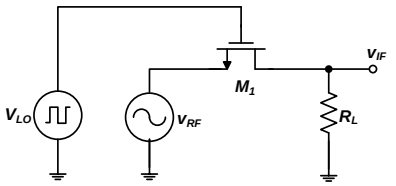

Fig. 2. NMOS switch/basic mixer [Ref. 9].

Although this seems a simple enough design, there is a serious consideration that must be taken into account. In order to operate in the triode region, the transistor must have a very low V_{DS} voltage. This means that if the output current is too high, a correspondently low load impedance must be chosen. Otherwise, the variation in v_{IF} will cause V_{DS} to rise leading the transistor to other non-suitable operating modes. Nonetheless, v_{IF} can never have high amplitude, since it will make the transistor leave the triode region. This is a key restriction and it will determine the sizing of the TIA since its input impedance will have to be suitable for a low variation of v_{IF}.

IV. Transimpedance and Noise Transfer Functions

The RCG-TIA circuit has already been extensively studied [4], [5] and, therefore we avoid a very precise analysis of the circuit. The RCG TIA is represented in Fig. 3.

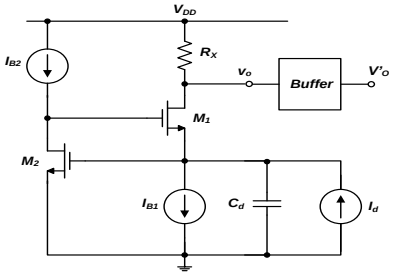

Fig. 3 Regulated common-gate TIA.

The input impedance of this circuit is the same as the one in a common-gate stage divided by the common-source stage low frequency gain. In Fig. 3 it can be seen that the TIA output is connected to a Buffer at the output node. In order to convert and amplify the TIA's input current to an acceptable level v_o must be amplified through the means of a voltage amplifier, connected after the output buffer.The Transimpedance function of this TIA has already been derived [5] and it follows

$$\frac{v_o}{I_d} = -\frac{R_X}{s^2\tau_a\tau_i(\beta+1) + s\tau_i(\beta+1)(\eta+1) + 1} \qquad (1)$$

where $\tau_i = g_{m1}^{-1}A_0^{-1}C_d$ is the time constant resultant from the PSD's output capacity and the TIA input impedance, $\tau_a = r_{02}C_{12}$ is the time constant of the pole inserted by C_{12} which, in turn, is the parasitic capacitance between the two gates of M_1 and M_2. The value $\eta = A_0\, C_{12}/C_d$ is the ratio between the PSD's output capacity and the miller capacity present at the TIA input. The factor β stands for the ratio between R_X and $M_1's$ conduction channel impedance r_{o1}. Previous studies have been presented considering the output noise on a RCG TIA. When the TIA's input is connected to a low output capacitance device, the noise transfer function can be as (2) [4]

$$v_{no\,rms}^2 = kT\frac{R_X^2C_d^2}{g_{m2}(\tau_1+\tau_2)\tau_1\tau_2} \qquad (2)$$

where the two time constants refer to the two dominant poles of the circuit, or with a high capacitance device [5]

$$v_{no\,rms}^2 = kT\frac{R_X^2C_d^2}{g_{m2}}\omega_0^3Q \qquad (3)$$

V. TIA Design Procedures

In order to reduce the overall noise, it can be seen by (2) and (3) that g_{m2}has to be high. However, there is a limit to the increase of this transconductance since it will raise the power consumption. Here it becomes important to restrict the value of β as $\beta \ll 1$. By restricting this ratio, not only does the transimpedance function becomes simpler, but the TIA gain becomes closer to R_X. In the case of the TIA with a SiPM at the input, β must be kept lower than 0.5, otherwise A_0 would have to be too high in order to maintain a value of Q that would not be excessively high, which would originate a very strongly impulsive response. One other point of interest is given by the fact that with an APD or a mixer at the input, M_1's biasing current can be lower than the one of the SiPM. This means that the value of R_X, which by (1) stands for the TIA low frequency gain, can be made higher. Such increase will make the parasitic capacitances in R_X considerably higher and, therefore, we will consider the value of a parasitic capacity C_X in parallel with R_X since it will originate a pole located at a frequency of interest.

Considering the TIA circuit with the PSD biasing reversed, will allow for the dc voltage at the output node, V_{Odc}, to be lowered. This will permit an increase on R_X, raising the TIA low frequency gain. This decrease of the dc voltage presents a better signal-to-noise ratio (SNR) of the TIA. However, this is also limited since there must be enough room for V_{DS1} and I_{B1}'s transistors to remain in saturation. In either cases here studied, except for the TIA with the mixer at the input, we considered $V_{Odc} \approx 500$ mV. This will make V_{DS1} to be over V_{DSAT1} and will allow enough room for I_{B1} dc voltage. If V_{Odc} is lowered past the 500 mV, V_{DS1} will be very close to V_{DSAT1} and, despite the better results obtained, the ratio between R_X

and r_{o1} would be $\beta > 1$ and the circuit would be highly dependent on fabrication processes, which would be undesirable. It should be noted that lowering V_{Odc} does not affect greatly I_{B1}'s transistors since the voltage at I_{B1}'s terminals is imposed by V_{GS2}. It has been previously proven that the TIA performs better if the two dominant poles are real with the APD at the input and complex conjugate with the SiPM [5] and, as such, this is the methodology used here.

A. TIA with a passive mixer at the input

With a mixer at the input, the signal shaping loses its relevance. In this type of application we are more interested in filtering the signal with a low-pass function since the mixer's output has a very rich spectral density. In the basic passive mixer described above we have established that the output current will have a sinusoidal shape with an amplitude of $I_d = 1$ µA, operating at around 10 MHz. The output equivalent capacity of the mixer will be, as an example, $C_d = 0.1$ pF. For a start, having such a low output capacity and noting that τ_i is proportional to C_d, means that τ_i will be too low and the resultant pole, inserted at the entrance of the TIA, will be located at high enough frequency, making it non-dominant or even negligible. This way, the only time constants we are interested here, in order to accomplish a low-pass function, are the ones inserted by the regulation stage and the load resistor R_X with its parasitic capacitance.

Considering the input current's low amplitude, the biasing of M_1 can be made lower. This means that the value of the load resistor R_X can be high and, therefore, the parasitic capacity C_X will also be higher. In this case we used $R_X = 200$ kΩ and, as consequence, $C_X \cong 50$ fF. This will result in a time constant of $\tau_X \cong 10$ ns and a pole at $f_X \cong 16$ MHz.

One important note that must be taken is that unlike the following two cases, the dc voltage at the output node has not been lowered. It would not be wise to lower the dc voltage since the input signal is symmetrical and it can reach a high enough amplitude, making it possible to deteriorate the linearity of the amplifier, by making M_1 go into triode region.

The bandwidth of this TIA is set by the regulation stage [5]. This could possibly mean that one could fall into the temptation of tuning the bandwidth in such a way that τ_a would insert a pole in the transfer function at a frequency of interest turning the TIA into a second order low pass function. There is, however, a problem with this approach. When the input signal has a frequency near the bandwidth limit of the TIA the dynamic input impedance has an impulsive response, originating a very expressive under-damped response of the output signal, reducing the TIA's stability. This way, the pole associated to τ_a has to be set at a higher frequency than the one of interest, making the pole associated to τ_a a non-dominant pole.

Having the low variation of the mixer's v_{DS} voltage in mind, we have pre-established that the TIA input voltage should not greatly exceed $v_i = 1\ \mathrm{mV_{pp}}$. Given the TIA input current variation, R_{in} must always be lower than

$$R_{in} = \frac{v_i}{I_d} \approx \frac{1}{g_{m1}A_0} \approx 500\ \Omega. \quad (4)$$

From the input impedance it can be easily proven that if $A_0 \gg 1$, in this case $A_0 = 50$, g_{m1} must be kept above 40 µS so R_{in} does not exceed the limit of 500 Ω, making the mixer's v_{DS} voltage vary in a way that it may take the active device out of the triode region. The reason why we chose $A_0 = 50$ is related to the fact that if it is any higher, the regulation stage low frequency gain will be multiplied by some Miller capacitances, making these latter ones dominate the input capacity of the TIA, instead of C_d. This will make the dynamic input impedance impulsive response grow higher.

In order to obtain a proper gain for M_2, its transconductance must be $g_{m2} = 5$ mS with a correspondent $r_{o2} \approx 10$ kΩ. This will result in a bias current $I_{B2} = 250$ µA, providing M_2 is operating in moderate inversion with V_{DSAT2} around 80 mV. From the well known drain current equation, the aspect ratio can be found. In this case, $W_2/L_2 \approx 200$. Note that due to the high value of the bias current I_{B2}, it turns impossible to use $L_2 = L_{min}$ since r_{o2} will be too low. Instead, we have used $L_2 = 250$ nm. W_2 may have to be adjusted in order to obtain $g_{m2} = 5$ mS.

By establishing V_{DSAT1} around 80 mV so M_1 stays in moderate inversion, we obtained a transconductance of $g_{m1} = 75$ µS with a bias current of $I_{B1} = 3$ µA. This value of g_{m1} is high enough to make the TIA's input impedance acceptably low. At this point, it becomes necessary to notice that since the bias current of M_1 is lower than the one of the SiPM, one can find a value of r_{o1} considerably higher using lower channel lengths. This results in a lower value of β, making the TIA gain closer to R_X. The aspect ratio of M_1 can be found from the drain current equation, resulting $W_1/L_1 \cong 4.7$. In order to have a high conduction channel impedance, we made $L_1 = 700$ nm, resulting in r_{o1} slightly above 1 MΩ.

As in both following cases, the bias current sources were realized through means of basic current mirrors. In I_{B1}we used a reference current of 15 µA in order to obtain a bias current of 3 µA. With a ratio of 5:1 we used $W/L = 40$ µm/1 µm and $W/L = 8$ µm/1 µm. In I_{B2} we used a PMOS current mirror with a ratio of 1:1 (two equal PMOS devices) with $W/L = 420$ µm/5 µm, generating a bias current of 250 µA.

The TIA's output must be connected to a $H(s)$ block. This block stands for a low pass filter, necessary to eliminate the undesirable spectral density at higher frequencies. Such block may be achieved with a lossy integrator. Note that an output buffer still must be used between the TIA and the low-pass filter. From simulations it can be seen that r_{o2} is low enough to make I_{B2} output impedance negligible and that with $L_1 = 700$ nm, r_{o1} becomes high enough to make β low valued, which is highly desirable.

B. TIA with a SiPM at the input

The output equivalent capacity in a PSD such as a SiPM is at least one order of magnitude higher than the one of an APD and, normally, C_d can vary between 100 to 300 pF [5]. If the same values of A_0 and C_{12} are used, it can be seen that $\eta < 1$. This will make the transimpedance function unfeasible with a dominant real pole since it would make g_{m1}, which is proportional to C_d, high, raising the noise, area and power

consumption in the circuit. Another possibility would be choosing $Q = 0.5$, making the transimpedance function have two equal real poles. Since we are not using a value of $\beta \ll 1$, we can see from (5) that not only g_{m1} would be too high, but the peaking time would probably be higher than it should [5].

$$g_{m1} = \frac{Q^2(\eta+1)^2(\beta+1)C_d}{A_0\tau_a} \quad (5)$$

One of the reasons why β must be kept low is related to the fact that with its increase, and maintaining g_{m1} at an acceptable level, A_0 will increase, raising either the size or power consumption of M_2. The remaining choice is to design the TIA with complex conjugate poles. This means $Q > 0.5$. The value of Q must be lower than unity in order to avoid an under-damped response, avoiding this way an oscillating response of the TIA. Considering the SiPM's higher output current, R_X may have to be one order of magnitude lower. Being lower, the parasitic capacitance associated to R_X will also be lower and, therefore, the resultant pole will be located at a high enough frequency making it negligible. From (5) it can be seen that g_{m1} will be defined at the cost of $\tau_a A_0$ and if the first has to be limited, the latter must be high enough to that effect. Resuming, since both τ_a and A_0 depend on r_{o2}, which is proportional to L_2, it follows that L_2 will have to be higher than the minimum value accepted by the technology used in order to keep g_{m1} at an acceptable level [5].

The value of M_2's transconductance is $g_{m2} = 5$ mS, with $I_{B2} = 250$ µA, and $R_X = 23.2$ kΩ. We have optimized the circuit in order to reach the best possible V_{om}/V_{norms} ratio, where V_{norms} stands for the output noise voltage in rms at the output of the TIA. As mentioned above, t_m must be lower than 40 ns. We designed the TIA so we could have t_m around 36 ns, predicting that an output buffer parasitic capacitance will insert a lower response of the circuit. The value of τ_i must be around 10 ns [5], resulting, with the chosen A_0, a value of g_{m1} of around 300 µS. The value of τ_a was obtained through simulation, respecting the ac analysis at the drain of M_2. Also, the values of A_0, t_m, V_{om} and V_{norms} were obtained through simulation. We chose $A_0 = 100$ and with the transconductance associated to the regulation stage chosen we obtained $W_2/L_2 = 225$ providing $L_2 = 800$ nm, well above L_{min}. With $I_{B1} = 30$ µA the aspect ratio of M_1 was $W_1/L_1 = 3.6$ with $L_1 = 1.5$ µA. The biasing current sources were realized through means of basic current mirrors. In the case of I_{B1} we used a reference current of 150 µA with a ratio of 5:1, whereas in the case of I_{B2} the same values were used in all examples studied here. In both current mirrors we are aiming to use external variable resistors so the reference currents may be adjusted. It must be noted that the buffer block, in this case, represents an output buffer and a voltage amplifier, which is needed to make $V'_{om} = 1$ V.

C. TIA with an APD at the input

The equivalent output capacity in a PSD such as an APD is, typically, $C_d = 10$ pF [5] and, considering that C_{12} has the same order of magnitude (around 0.5 – 1 pF) in all the circuits studied here, this means that the ratio between the miller capacitance at the TIA's input and C_d, η, should be around 10. By choosing a value of Q that is sufficiently low (below 1/3), the transimpedance function will have two real poles, in which one will be dominant. Note that this is only true if $\tau_1 \gg \tau_2$ where

$$\tau_1 \cong \tau_i(1+\eta) = \frac{1}{\omega_0 Q} \quad (6)$$

and

$$\tau_2 = \frac{\tau_a}{1+\eta} \quad (7)$$

Being much higher than τ_2, τ_1 can be associated with the dominant pole and, from (8), can be seen that will influence the value of g_{m1}. This way, knowing that the value of τ_1 is imposed by the required peaking time of the output voltage, g_{m1} can be written in the form

$$g_{m1} = \frac{\tau_a C_d}{A_0 \tau_1^2 Q^2} \quad (8)$$

In order to avoid an increase in noise, g_{m1} must be limited by τ_a/A_0 which, in turn, is proportional to L_2^2. This way L_2 may have to be higher than the minimum value in order to have a suitable A_0.

As said before, the pole inserted by the time constant referent to the load resistance R_X and its parasitic capacitance, must be taken into account in the case of the APD. This is motivated by the size of the load resistance R_X which is $R_X = 180$ kΩ. We estimate an associated parasitic capacity of C_X around 50 fF. The value of the regulation stage low frequency gain is $A_0 = 50$. We considered $g_{m2} = 5$ mS with a bias current source of $I_{B2} = 250$ µA resulting an aspect ratio of $W_2/L_2 = 220$. With $L_2 = 250$ nm we adjusted the value of W_2 until the expected transconductance and channel impedance were achieved. With $I_{B1} = 3.5$ µA we adjusted the aspect ratio of M_1until $W_1/L_1 = 0.38$ with $L_1 = 5.7$ µm. The realization of the biasing current sources was similar to the ones of the TIA with the mixer at the input and, therefore previously detailed. Like in the case of the SiPM the buffer block represents a buffer connected to the output of the TIA. Following the buffer, comes a voltage amplifier necessary to raise the output voltage to $V'_{om} = 1$ V, in order to fulfill the system's requirements.

VI. Simulation Results and Comparison

In the present section we show the results obtained by simulation in the circuits described above. Our main focus, in the present section, is to show the output voltage waveform, linearity, noise level and power consumption in each TIA, in order to fairly compare the designed circuits.

A. TIA obtained results

By using the sizing described in the respective section, we obtained, as Fig. 4 shows, an input voltage variation of $v_i \cong 906$ µV, lower than the restriction mentioned previously.

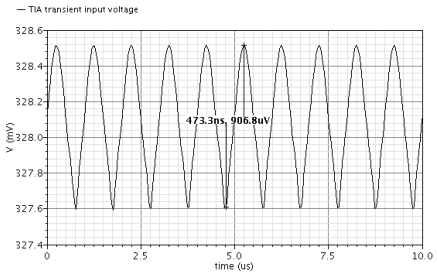

Fig. 4. TIA input voltage variation.

The voltage variation at the input does not exceed 1 mV_{pp} which, by itself, gives enough room for the mixer output transistor to remain in the triode region. This variation is accomplished by keeping the TIA input impedance at a low level since the lower is the latter, the smaller is the input equivalent voltage variation. In Fig. 5 we show the TIA's output voltage. With the sizing described we were able to reach an output amplitude of $V_{om} \cong 400\ \mathrm{mV_{pp}}$.

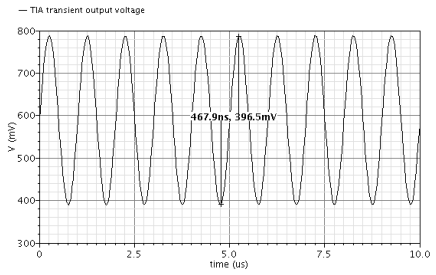

Fig. 5. TIA output voltage.

Note that, in this case, the signal is centered around 0.6 V, as it was expected. With the SiPM and the APD at the input, we obtained the output signals shown in Fig. 6 where t_m was kept below 40 ns and the output voltage amplitude achieved was $V_{om} \cong 335$ mV for the SiPM and $V_{om} \cong 232$ mV for the APD.

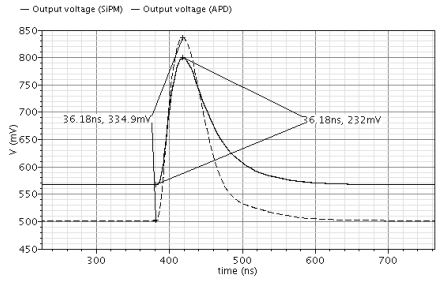

Fig. 6. TIA's output voltage (SiPM: $\boldsymbol{V_{om} \cong 335\ \mathbf{mV}}$ and $\boldsymbol{t_m \cong 36.2\ \mathbf{ns}}$; APD: $\boldsymbol{V_{om} \cong 232\ \mathbf{mV}}$ and $\boldsymbol{t_m \cong 36.2\ \mathbf{ns}}$).

It can be seen in Fig. 6 that both output signals have a dc component around 0.5 V, as expected, and that the rising time is near the pre-established 36 ns. The shape of the output signal, even not being of paramount importance, is the expected. The core circuit of the TIA was found to have a power consumption of 336 µW in the case of the SiPM and 304 µW for the APD and mixer. The three circuits' linearity is shown in Fig. 7. It can be seen that the circuit presents a good linearity. For the effect, we made the input current vary between $10^{-1}I_{dm}$ and $10^{0}I_{dm}$ for each V_{om} value, showing a good and predictable output voltage response. From the below figure we can see that the TIA designed reached a transimpedance gain of 198 kΩ in the case of the mixer at the input, 16.75 kΩ in the case of the SiPM and 103 kΩ with the APD. In the case of the mixer, the gain is very close to R_X, meaning that the value of β is close to zero, unlike the remaining two circuits. The total integrated output noise voltage between 1 kHz and 1 GHz is $v_{no\ rms} = 0.881$ mV, making a signal over noise of $S/N = 451.3$ with the mixer at the input. With the SiPM it was found that the total integrated output noise rms voltage in the same interval was $v_{no\ rms} = 3.145$ mV, which gives a $V_{om}/v_{no\ rms}$ ratio of $S/N = 106.5$. The reason why the noise is higher with the SiPM than with the APD or mixer is due to the value of C_d [5]. With the APD at the input, the total integrated noise was $v_{no\ rms} = 1.01$ mV, resulting an $S/N = 231$. The dominant noise source is, as expected, transistor M_2. The noise response of the three TIAs can be observed in Fig. 8.

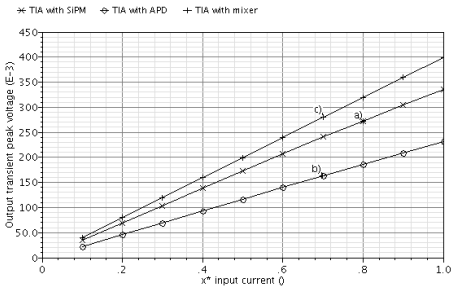

Fig. 7. TIA's linearity with: a) SiPM ($\boldsymbol{I_{dm} = 22.5\ \mu A}$); b) APD ($\boldsymbol{I_{dm} = 2.25\ \mu A}$); c) Mixer ($\boldsymbol{I_{dm} = 1\ \mu A}$).

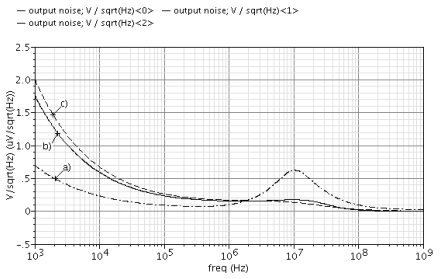

Fig. 8. TIA's output noise response. a) SiPM ($\boldsymbol{C_d = 300\ \mathbf{pF}}$); b) APD ($\boldsymbol{C_d = 10\ \mathbf{pF}}$); c) Mixer ($\boldsymbol{C_d = 0.1\ \mathbf{pF}}$).

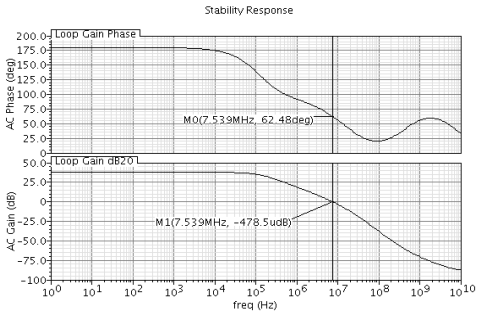

Fig. 9. TIA with SiPM gain and phase Bode diagrams.

TABLE I. TIA COMPARISON.

TIA circuit	Technology	Supply	Power	Output Noise $v_{no\,rms}$		S/N
				Theoretical	*Simulation*	
Feedback TIA (APD input) [Ref.6]	350 nm	3.3 V	0.68 mW	7.5 mV	6.9 mV	144.9
RCG TIA (APD input) [Ref. 4]	350 nm	3.3 V	0.68 mW	6.5 mV	6.8 mV	147.1
RCG TIA (SiPM input) [Ref. 5]	130 nm	1.2 V	0.34 mW	3.15 mV (11 mV)[1]	3.01 mV (10.5 mV)[1]	95.2
RCG TIA (SiPM input) [This work]	**130 nm**	**1.2 V**	**0.34 mW**	**4.35 mV (12.96mV)[1]**	**3.15 mV (9.39 mV)[1]**	**106.5**
RCG TIA (APD input) [This work]	**130 nm**	**1.2 V**	**0.30 mW**	**1.34 mV (5.71 mV)[1]**	**1.01 mV (4.31 mV)[1]**	**232.0**
RCG TIA (mixer input) [This work]	**130 nm**	**1.2 V**	**0.30 mW**	**0.62 mV (1.56 mV)[1]**	**0.88 mV (2.21 mV)[1]**	**452.5**

1. Values extrapolated for an output amplitude of 1 V.

It can be seen from Fig. 8 that, excluding the case of the SiPM, the noise response has a small elevation near 10 MHz. This elevation is not related to the zero in the noise transfer function but it is related to the bandwidth of the TIA, imposed by τ_a. The more pronounced elevation in the TIA noise transfer function with the SiPM is due to the higher capacity present at its input. The higher C_d, means that the zero in the noise transfer function will be at a lower frequency originating, therefore, a spike in the noise response. In terms of phase margin, stability analyses were taken for each circuit, where the margins obtained were: $\phi_M = 59.4$ °at 267 MHz, $\phi_M = 62.5$ ° at 7.54 MHz and $\phi_M = 87.5$ ° at 16.06 MHz for the mixer, SiPM and APD, respectively. In Fig. 9 we show the gain and phase Bode diagrams for the TIA with the SiPM at the input. We opted to only show this circuit's characteristic due to the spike in its noise transfer function, which could lead to some instability motivated by the presence of a low frequency zero.

B. Comparison of the TIA circuits.

In the present section we are focused on evaluating the designed circuits' performances. For the effect, we are interested in showing the noise level, power consumption, output voltage amplitude and technology used in this work and in previous studies. In table I we show the results obtained in reference studies, while presenting the ones obtained in this work. In [4] and [6] the technology used was 350 nm with a supply voltage of 3.3 V. This made possible to achieve an output voltage amplitude of $V_{om} = 1$ V. This way, in order to make our results comparable, we show the results obtained here in their original form and extrapolated to $V_{om} = 1$ V. It must be noted that in the calculation of $V_{om}/v_{no\,rms}$ (S/N), we considered the simulated value of the output noise.

VII. DISCUSSION AND CONCLUSIONS

In this paper we present a circuit implementation of a RCG TIA with an APD and SiPM at the input. We also have shown the implementation of the circuit here presented in the referred technology, in the context of a RF frontend.

We have investigated the DC voltage at the output node. It was found that the best solution is $V_{DS1} \cong V_{DSAT1}$. This implies that the load resistor be about ten times higher than the drain-source resistance. In this point M_1 is saturation/triode boundary region and we obtain the optimal point of the S/N.

ACKNOWLEDGMENTS

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Regulated Common-Gate TIA with Noise Improvement for Radiation Detectors

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Regulated Common-Gate TIA with Noise Improvement for Radiation Detectors

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***Abstract* — A Transimpedance Amplifier (TIA) is a device which performs current-voltage conversion and signal shaping. The most commonly used solution is an Avalanche Photo-Diode (APD) as radiation detector with a feedback TIA. Recently, Silicon Photo-Multipliers (SiPMs), have proven to be good alternatives. The main objective in this paper is to show, evaluate and compare the behavior of a regulated common-gate (RCG) TIA when the light sensitive device is an APD or a SiPM. We will also present two alternative circuits based on the RCG topology. The first can be resumed to the insertion of a transistor, responsible for an improvement in the output noise response of the TIA. This solution proves itself to be a good alternative, since it will improve the Signal-to-Noise Ratio (SNR) of the circuit by around 3 dB, with negligible penalty in consumption (only 2%). The second alternative will be a proposed differential version of the RCG topology, in which the first solution will be included. These two latter solutions will only be tested with a SiPM at the input.**

We will also study the RCG topology in a RF front-end, providing there is a passive mixer at the TIA's input. The proposed circuits are simulated with standard CMOS technology (UMC 130 nm), from a 1.2 V supply.

***Index Terms* — Transimpedance Amplifiers, radiation detectors, avalanche photo-diodes, silicon photo-multipliers.**

I. Introduction

TRANSIMPEDANCE Amplifiers (TIAs) are used in applications requiring current-voltage conversion, and signal shaping. TIAs are widely used in optical communications systems [1]–[3], nuclear science, instrumentation and medical imaging [4]–[8]. A radiation detector that must perform as a photo-sensitive device (PSD), converting any type of photo-dependent radiation into a correspondent current pulse. Two of the PSDs most commonly used are the avalanche photodiode (APD) and, more recently, the new silicon photo-multiplier (SiPM) [8], capable of a higher output current, presenting as well a higher output equivalent capacity.

TIAs studied in this paper are used in Positron Emission Tomography (PET) scanners front-end. For example, in [6] a total of 6×32-channel ASICs were developed, where the most challenging part of these ASICs was to design the 192 TIAs with the respective APDs at their inputs, since these TIAs are what determine the system's limits of performance. Each TIA should not exceed a power consumption of 1 mW, maintaining low noise level and the capability of pulse shaping. Here, we study the usage of a regulated common-gate (RCG) TIA in a RF receiver and PET scanner front-end, showing the key constraints and requirements for the TIA design, such as output voltage amplitude and peaking time, noise level and power consumption, both as radiation detector and at the output of a passive mixer.

In this paper we will present three different implementations of the RCG circuit topology: 1) RF mixer at the input, 2) APD at the input, and 3) SiPM at the input. Also, regarding the SiPM implementation, we will show two more alternative versions of the RCG topology. The first will consist in a circuit with an improved noise response, while the second will comprise a differential proposed version. We will show that the first circuit variation will enable a noise reduction, while maintaining, approximately, the same output voltage amplitude. Naturally, this will result in an improved Signal-to-Noise Ratio (SNR) of the TIA. Simulation results in a standard CMOS 130 nm will be presented, for comparison.

II. Radiation Detector Basics

A radiation detector has a scintillating crystal that emits a light pulse, when hit by radiation [4, 5]. In the case of a PET system, this radiation usually comes in the form of high energy photons, or gamma-ray bursts [9]. The light pulse is then converted into a current pulse by a PSD such as an APD [4] or a SiPM [5]. The TIA has the purpose of converting this current pulse into a voltage pulse with the desired shape and amplitude. The equivalent circuit of an APD or, in the case of a SiPM a simplified version [8], is a current source $i_d(t)$ in parallel with a capacity C_d as shown in Fig. 1. As can be seen, the current pulse $i_d(t)$ has a very fast rise (much lower than 1 ns in the case of a SiPM) [8] and, after reaching I_{dm} starts decaying exponentially with a time constant τ_d. The output voltage must have the form shown below. The variation of $v_o(t)$ must reach a peak value V_{om} in $t_m < 40$ ns [4]–[6]. It must be noted that the exact shape of $v_o(t)$ is not important and, therefore, we are more interested in maintaining a good linearity between I_{dm} and V_{om}. The PSD output current and capacity vary whether an APD or a SiPM is used. In the case of an APD we considered a

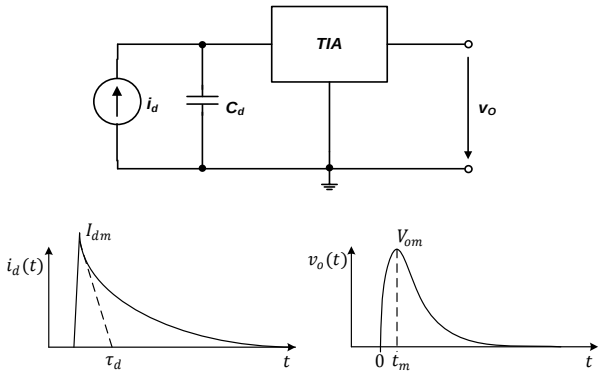

Fig. 1. Equivalent circuit of a PSD with TIA's input current $i_d(t)$ and output voltage $v_o(t)$ (adapted from [4]).

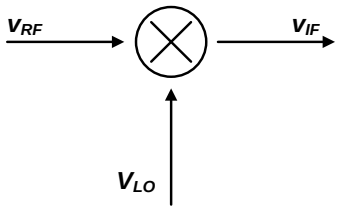

Fig. 2. Block diagram of a mixer. NMOS switch/basic mixer with a feedback TIA at the output.

peak current of $I_{dm} = 2.25$ μA with a correspondent output capacity of $C_d = 10$ pF. The more recent SiPM is capable of an output current one order of magnitude higher, as well as a higher output capacity [4]. Thus, for the SiPM we considered $I_{dm} = 22{,}5$ μA and $C_d = 300$ pF [5].

III. Passive Mixer

An ideal mixer is a circuit that can be viewed as an analog multiplier circuit. Such circuit has the function of translating a carrier signal from one frequency to another [10]. In its most basic form, it can be seen as three port device consisting in a Local Oscillator (LO), Radio Frequency Input (RF IN) and Intermediate Frequency Output (IF OUT), as represented by Fig. 2. Mixers can be of complex design depending on their applications, being distinguished between active or passive devices, depending on providing, or not, amplification [10]. We have considered a passive mixer which consists on a switching device controlled by a Local Oscillator (LO). When in the triode region, a MOS transistor can perform as a switch if the remaining resistances present in the circuit are of much higher value than the equivalent resistance of the MOS device conduction channel [11], as shown by Fig. 3. In these conditions, the device will operate as an open switch every time V_{LO} is at low level and as a closed switch, with an equivalent R_{DS} resistance, when V_{LO} is at high level. The load impedance of the mixer will be the TIA's input impedance, denoted by Z_{TIA}. In our designs this impedance corresponds to the RCG's input impedance. The mixer's output equivalent capacity is denoted by C_M, being mostly determined by the switching device, M_1, parasitic capacities. In Fig. 3 one can see

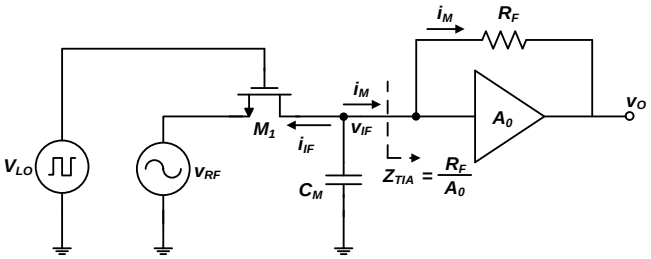

Fig. 3. Schematic of an NMOS switch/basic mixer with a feedback TIA at the output.

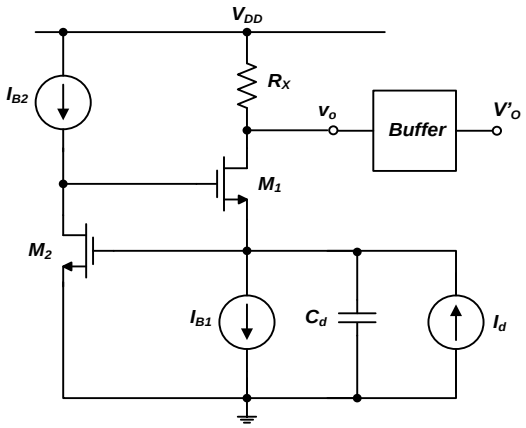

Fig. 4 Regulated common-gate TIA.

the mixer's output current and capacity. For simulation and sizing purposes, the values chosen for these were: output current amplitude $I_M = 1$ μA, while the output capacity is $C_M = 0.1$ pF.

Although this seems a simple enough design, there is a serious consideration that must be taken into account. In order to operate in the triode region, the transistor must have a very low V_{DS} voltage. This means that if the output current is too high, a correspondently low load impedance must be chosen. Otherwise, the variation in v_{IF} will cause V_{DS} to rise leading the transistor to other non-suitable operating modes. Nonetheless, v_{IF} can never have high amplitude, since it will make the transistor leave the triode region. This is a key restriction and it will determine the sizing of the TIA since its input impedance will have to be suitable for a low variation of v_{IF}.

IV. Transimpedance and Noise Transfer Functions

In this section, the interest lies in providing the studied circuits' transimpedance and noise transfer functions. Since we will study the RCG TIA and two proposed derived circuits, in order to differentiate them, they will be referred to as circuits A, B and C, regarding the basic form of the RCG TIA, the RCG TIA with improved noise and, finally, the differential proposed version of the RCG TIA, respectively. The basic form of the RCG has already been extensively studied and, therefore, we will only present its transimpedance and noise transfer functions. The remaining variations of the RCG will be subjected to a more detailed analysis.

A. Basic RCG TIA

The basic RCG TIA circuit, represented in Fig. 4, has already been extensively studied [4], [5] and, therefore we avoid a very precise analysis of the circuit. The input impedance of this circuit is the same as the one in a common-gate stage divided by the common-source stage, composed by M_2 and I_{B2}, low frequency gain, A_{V0}, following

$$Z_{in} \approx \frac{1}{A_{V0} g_{m1}}. \quad (1)$$

In Fig. 4 it can be seen that the TIA output is connected to a buffer. In order to convert the TIA's input current to an acceptable level, v_o must be amplified through the means of a voltage amplifier connected after the output buffer. This voltage amplifier must have a bandwidth high enough so it does not insert any delay in the output signal. The Transimpedance function of this TIA has already been derived [5] and it follows

$$\frac{v_o}{I_d} = -\frac{R_X}{s^2 \tau_a \tau_i (\beta+1) + s\tau_i (\beta+1)(\eta+1) + 1}, \quad (2)$$

in which

$$\tau_i = \frac{C_d}{A_{V0} g_{m1}} \quad (3)$$

and

$$\tau_a = r_{ds2} C_{12}. \quad (4)$$

Note that τ_i is the time-constant originated by the PSD's output capacity and the TIA's input impedance, while τ_a reflects the regulation stage's bandwidth. Capacity C_{12} is the parasitic capacity between the two gates of M_1 and M_2. The value $\eta = A_0\, C_{12}/C_d$ is the ratio between the PSD's output capacity and the miller capacity present at the TIA's input. The factor β stands for the ratio between R_X and $M_1's$ conduction channel impedance, r_{ds1}. In the case the transimpedance function has its poles complex conjugated, the amplifier's quality factor will be [5]

$$Q = \frac{1}{1+\eta}\sqrt{\frac{\tau_a}{\tau_i(\beta+1)}} = \frac{1}{2}, \quad (5)$$

while its natural response will follow

$$\omega_0^2 = \frac{1}{\tau_a \tau_i (\beta+1)}. \quad (6)$$

Previous studies have been presented considering the overall integrated output noise on the RCG TIA. When the TIA's input is connected to a low output capacitance device, such as a basic mixer or a SiPM, the noise transfer function can be as [4]

$$v_{no\,rms}^2 = kT \frac{R_X^2 C_d^2}{g_{m2}(\tau_1+\tau_2)\tau_1\tau_2} \quad (7)$$

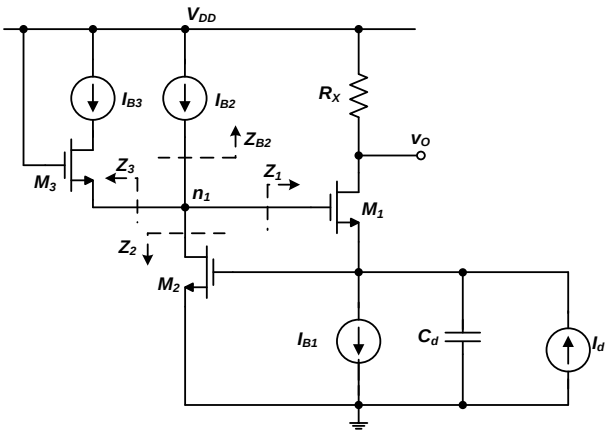

Fig. 5 Schematic of the RCG TIA with improved noise response.

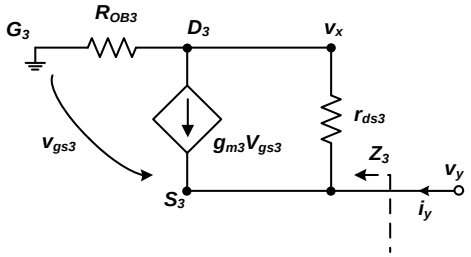

Fig. 6 Incremental model of M_3 and I_{B3} configuration.

where the two time-constants refer to the two dominant poles present in the circuit. In the case a high output capacitance device, such as a SiPM, is used, the noise transfer function will have the form [5]

$$v_{no\,rms}^2 = kT \frac{R_X^2 C_d^2}{g_{m2}} \omega_0^3 Q \quad (8)$$

B. RCG TIA with improved noise

Relatively to the basic RCG TIA, discussed in the previous section, the modification taken here is the placement of a MOS transistor, M_3, with its biasing current source, I_{B3}, connected between the drain of M_2 and V_{DD} [12], as suggested in Fig. 5. With the insertion of this configuration, it is to be expected that M_2's contribution to the total output integrated noise will be lower. Note that transistor M_3 must have a small current passing through it and, therefore, its transconductance, g_{m3}, will also be small. This means that its noise contribution can be made negligible, as will be further seen. The equivalent impedance in node n_1, Z_{n1}, corresponds to the parallel between Z_2 and Z_3, if one takes into account that Z_1 and Z_{B2} are ideally infinite, and thus negligible. One immediate illation that can be retrieved out of this is the fact that the regulation stage's low frequency gain, A_{v0}, will now be different, since it will be influenced by the configuration presented by M_3, following

$$A_{v0} = g_{m2}(Z_2 || Z_3). \quad (9)$$

In order to find a meaning to Z_3 one can analyze its incremental circuit, depicted in Fig. 6. Here it becomes important to notice that since M_2's configuration must present

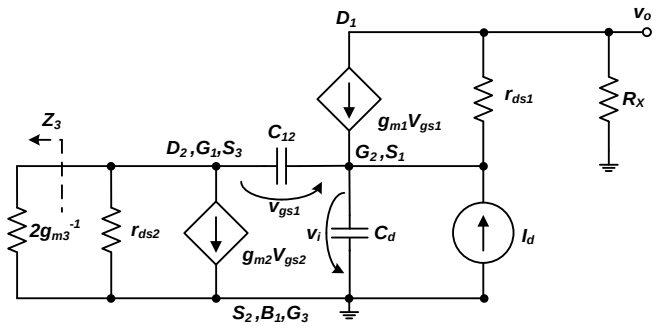

Fig. 7 Incremental model of the RCG TIA with the contribution of M_3 and I_{B3} configuration.

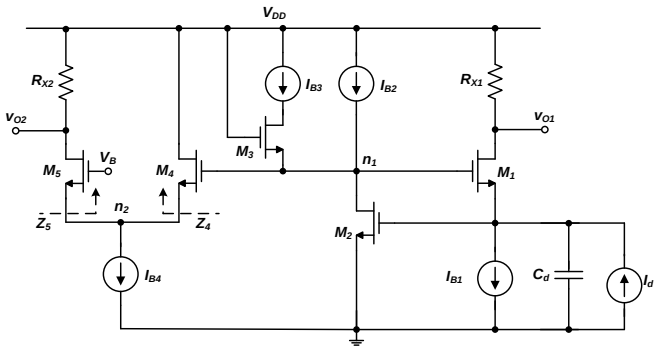

Fig. 8 Proposed differential version of the RCG TIA.

high gain, it will also present a drain-to-source voltage, V_{DS2}, relatively high. Therefore, there will be left little room for M_3 and I_{B3} active devices' V_{DS}. In practical terms, this means that I_{B3} biasing current source may have to be designed working on the triode or saturation/triode boundary region, and as such, its equivalent dynamic impedance, R_{OB3} may be lower than the expected.

Regardless of its parasitic capacities, transistor M_3 has a low frequency output impedance that will follow

$$Z_3 = \frac{v_y}{i_y} = \frac{v_y}{v_y(g_{m3} + r_{ds3}^{-1}) - v_x r_{ds3}^{-1}} \tag{10}$$

By applying KCL to node D_3 the following can be obtained

$$v_y g_{m3} = v_x R_{OB3}^{-1} + (v_x - v_y) r_{ds3}^{-1}. \tag{11}$$

If the approximations $g_{m3} \gg r_{ds3}^{-1}$ and $R_{OB3} \cong r_{ds3}$ are made, which mean M_3 is operating in saturation region, one can replace (11) into (10), resulting in the expression for Z_3.

$$Z_3 = 2g_{m3}^{-1}. \tag{12}$$

Knowing the impedance in node n_1, originated by M_3 and its configuration, makes it possible to see the incremental model of the RCG TIA, shown in Fig. 7. Here, it can be seen that there will now be an impedance Z_3 in parallel with r_{ds2}, which can affect M_2's gain and frequency response. As will be further seen, by making g_{m3}^{-1} have the same order of magnitude of r_{ds2}, the dominant pole of the circuit will become affected, altering the bandwidth and noise transfer function of the TIA.

By applying KCL to the drain of M_2 and knowing that $r_{ds2} \cong g_{m3}^{-1}$ will result in

$$v_{gs1}[sC_{12} + R_{23}^{-1}] = -g_{m2} v_i, \tag{13}$$

where $R_{23} = r_{ds2} || 2g_{m3}^{-1}$ is the equivalent impedance between the parallel composed by Z_3 and M_2's conduction channel equivalent resistance, r_{ds2}. The equation that characterizes the regulation stage will now be

$$v_{gs1} = -\frac{g_{m2} R_{23}}{1 + sR_{23}C_{12}} v_i = -\frac{A_{V0}}{1 + s\tau_a} v_i = -Av_i. \tag{14}$$

Note that since R_{23} will be about one half of r_{ds2},it will cause for the regulation stage's low frequency gain to be lowered, as well as the time-constant τ_a. The remaining nodes are characterized by the same equations as the basic RCG TIA, with the differences in A_{V0} and τ_a. Therefore, the transimpedance function will still be the one presented in (2).

One immediate conclusion that can be derived from the transimpedance function is that the time-constants associated to the poles will now be different. Since R_{23} will, mandatorily, be lower than r_{ds2}, M_2's low frequency gain, A_{v0}, will also be lower, affecting the TIA's input impedance. The pole that gives M_2's configuration bandwidth, associated to τ_a, will be placed at a higher frequency. This could lead one to think that the passing band of the amplifier would be increased, resulting in more integrated overall noise. However, the pole originated by C_d and the TIA's input impedance, τ_i, given by (3), will now be located at a lower frequency, f_{pi}, since it is proportional to A_{v0}, as expressed by (15), which can mean that the amplifier's bandwidth will now be limited by τ_i instead of τ_a

$$2\pi f_{pi} = \frac{1}{\tau_i} = \frac{A_{v0} g_{m1}}{C_d}. \tag{15}$$

This means that the noise spectral density of the TIA will be lower since it will be cut slightly earlier. The noise transfer function will still be given by (8), if a SiPM is used and, respecting (5) and (6), it is easy to see the influence that the changes in τ_a and τ_i will impose on the noise transfer function.

C. Differential proposed version of the RCG TIA

The proposed changes in the circuit are shown in Fig. 8 and, as can be seen, the inverted output is accomplished by using the signal present in node n_1. The regulation stage inverts the incremental voltage on the TIA's input, v_i. The inverted output voltage, v_{o2}, can then be accomplished by amplifying the voltage present at node n_1, v_{n1}. In order to amplify v_{n1}, a common-gate stage was used, composed by M_5, R_{X2} and I_{B4}. To prevent an exaggerated decrease in A_{v0}, a buffer was placed between node n_1 and M_5, in a source-follower configuration. This configuration has the characteristic of presenting very high input impedance, low output impedance and a voltage gain close to unity. The source-follower is accomplished by transistor M_4 and current source I_{B4}. Note that I_{B4} is shared between M_4 and M_5 configurations, in an overall configuration resembling a differential pair, or a differential-to-single ended converter.

One immediate, apparent, difficulty in realizing the circuit described above, would be related to the number of cascaded amplifying stages present between the input signal, I_d, and v_{O2}. This relatively high number of stages can imply that there will be a significant delay between both outputs, i.e., there can be a high phase deviation, unbalancing the output differential signal. However, since the operating frequency of the circuit is far from the transition frequency, f_T, of the transistors in the technology used, the delay can be negligible.

Regarding the transimpedance function at the output v_{O1}, it has already been found and it corresponds to the one expressed by (2). The interest here lies in finding a relation between v_{O2} and I_d, as well as a relation between the differential voltage and I_d. For that effect, one could analyze the path between v_{O2} and I_d in the incremental circuit however, this would be rather extensive. By knowing the gain of the configurations presented by M_4 and M_5, the mentioned relation can be effortlessly obtained. The voltage gain in a common-gate stage can be easily found and, in M_5 configuration, to a good approximation, it will be

$$V_{o2} = g_{m5}(r_{ds5}||R_{X2})V_{n2} = A_{v0,5}V_{n2}. \tag{16}$$

The voltage gain across M_4's configuration can be given by [11], following

$$V_{n2} = \frac{g_{m4}}{g_{m4} + g_{mb4}}V_{n1} = A_{v0,4}V_{n1}, \tag{17}$$

if $g_{m4} \gg r_{ds4}^{-1}$. Note that V_{n1} is the voltage present at node n_1, which corresponds to V_{ds2}. From here, we can use the incremental circuit depicted in Fig. 7 in order to find a relation between V_{n1} and I_d. Considering $V_{n1} = V_{gs1} + V_i$, (14), (16), (17) and that in the passing band of the amplifier $A \gg 1$ will result in

$$V_{o2} = -AA_{v0,5}A_{v0,4}V_i. \tag{18}$$

By knowing that $g_{m1} \gg r_{ds1}^{-1}$ and applying KCL to node G_2, S_1, the following can be obtained

$$V_i = -\frac{1}{A[s^2\tau_a\tau_i + s\tau_i(\eta + 1) + 1]}I_d. \tag{19}$$

Using (18) and (19) will give us the transimpedance function of the inverted output of the TIA, as follows

$$V_{o2} = A_{v0,5}A_{v0,4}\frac{1}{s^2\tau_a\tau_i + s\tau_i(\eta + 1) + 1}I_d. \tag{20}$$

Note that using again (16), (17), making the approximation $r_{ds5} \gg R_{X2}$ and, assuming a worst case scenario in which $A_{v0,4} \cong 0.7$ – the bulk transconductance is usually 0.7 to 0.9 g_m – the inverted output transimpedance function can be written as

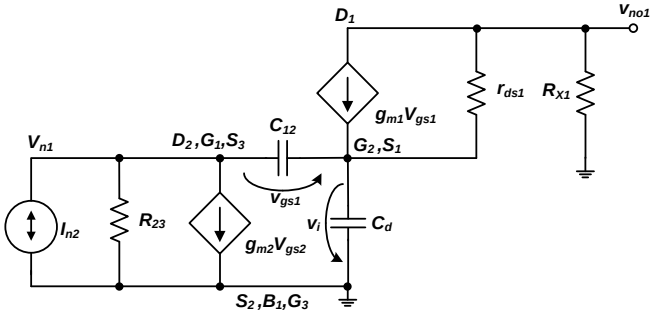

Fig. 9 Partial incremental circuit of the inverted output with I_{n2} noise current source.

$$\frac{V_{o2}}{I_d} = 0.7\frac{g_{m5}}{g_{m1}}\frac{R_{X2}}{s^2\tau_a\tau_i + s\tau_i(\eta + 1) + 1}. \tag{21}$$

As seen by the above, the transimpedance function in the inverted output has opposite phase of the one shown in (2). One important feature of (21) is the fact that the frequency response is the same for both outputs. The parameter $\beta + 1$ is only missing from the above because it was made the approximation $r_{ds5} \gg R_{X2}$. Otherwise, there would still be a multiplication factor $(\beta_2 + 1)$, where β_2 would stand for the ratio between R_{X2} and r_{ds5} in the denominator of (21), similarly to (2). As seen above, in order for V_{o2} to have the same amplitude of V_{o1}, g_{m5} must be approximately equal to $1.43g_{m1}$. Regardless, the same can be said about the load resistor R_{X2} and R_{X1}. The differential transimpedance function can be found by simply subtracting both outputs, since they have opposite phase, resulting in

$$\frac{V_{diff}}{I_d} = \frac{V_{o1} - V_{o2}}{I_d} = -\frac{R_{X1} + 0.7g_{m5}g_{m1}^{-1}R_{X2}}{s^2\tau_a\tau_i + s\tau_i(\eta + 1) + 1}. \tag{22}$$

Note that for simplicity, it was assumed that $\beta_1 = \beta_2 \cong 0$. Regarding a noise analysis, for simplicity, only I_{n2}, the thermal noise generated by M_2, will be considered, since this will be the dominant noise source as will be seen.. Much like it was previously done with the transimpedance function, the interest lies in finding a relation between V_{o2} and I_{n2}, where V_{o2} will be given by (17), even though this time, V_{n1} will depend on I_{n2} instead of I_d. In Fig. 9 the incremental circuit contemplating the path between V_{n1} and I_{n2} is shown. In order to find the noise transfer function for V_{o2}, one can apply KCL to node D_1, resulting in

$$v_{gs1} = v_i g_{m1}^{-1}r_{ds1}^{-1} - V_{no}g_{m1}^{-1}R_X^{-1}. \tag{23}$$

In node S_1, G_2 we will obtain

$$V_{no1} = -\frac{sC_d}{R_X^{-1}}\frac{1}{(1 + sg_{m1}^{-1}C_{12})}v_i, \tag{24}$$

which, by replacing into (23) and noticing the equivalency $v_i = V_{n1} - V_{gs1}$will result into

$$V_{gs1} = V_{n1} r_{ds1}^{-1} g_{m1}^{-1} \frac{s r_{ds1} C_d + 1}{s g_{m1}^{-1} C_d + 1}. \quad (25)$$

In the derivation of (25) it was assumed that $C_d \gg C_{12} \gg r_{ds1}^{-1} g_{m1}^{-1} C_{12}$. In node n_1, by KCL, noticing that $g_{m2} \gg R_{23}^{-1}$, the following can be obtained

$$-I_{n2} = g_{m2} V_{n1} + g_{m2}(s g_{m2}^{-1} C_{12} - 1) V_{gs1}. \quad (26)$$

Replacing (25) into (26) and knowing that $r_{ds1}^{-1} g_{m1}^{-1} \ll 1$ will give us a relation between I_{n2} and V_{n1}, following

$$\frac{V_{n1}}{I_{n2}} = -g_{m2}^{-1} \frac{s\tau_z + 1}{s^2 \tau_{n1} \tau_{n2} + s\tau_{n1} + 1}, \quad (27)$$

where $A_{v0,1} = g_{m1} r_{ds1}$ is M_1's configuration low frequency gain without the load impedance, and

$$\tau_z = g_{m1}^{-1} C_d, \quad (28)$$

$$\tau_{n1} = g_{m2}^{-1} A_{v0,1}^{-1} C_{12}, \quad (29)$$

$$\tau_{n2} = r_{ds1} C_d. \quad (30)$$

Note by (27) that τ_z will produce a low frequency zero. This suggests that the inverted output will contribute with a relatively higher noise than V_{o1}. Also aiding this, is the fact that the low frequency gain of the noise transfer function will be relatively high. Nonetheless, taking (16) and (17) along with the derivations taken in [5] into consideration, one can find the noise transfer function in the inverted output, written in the form

$$V_{no2,rms}^2 = -kTA_{v0,4}^2 A_{v0,5}^2 \frac{C_d}{g_{m1} C_{12}} \omega_{0,2} Q_2. \quad (31)$$

where k is the Boltzmann's constant and T is the absolute temperature, in Kelvin. The values of $\omega_{0,2}$ and Q_2 can be found by comparing (27) to a canonical second-order transfer function. The differential output noise voltage will simply be subtraction between (8) and (31).

V. TIA Design Procedure

In order to reduce the overall noise, it can be seen by (7) and (8) that g_{m2}has to be high. However, there is a limit to the increase of this transconductance since it will raise the power consumption. Here it becomes important to restrict the value of β as $\beta \ll 1$. By restricting this ratio, not only does the transimpedance function becomes simpler, but the TIA gain becomes closer to R_X. One other point of interest is given by the fact that with an APD or a mixer at the input, M_1's biasing current can be lower than the one of the SiPM. This means that the value of R_X, which by (2) stands for the TIA low frequency gain, can be made higher. Such increase will make the parasitic capacitances in R_X considerably higher and, therefore, we will consider the value of a parasitic capacity C_X in parallel with R_X since it will originate a pole located at a frequency of interest. Considering the TIA circuit with the PSD biasing reversed, will allow for the dc voltage at the output node, V_{Odc}, to be lowered. This will permit an increase on R_X, raising the TIA low frequency gain. This decrease of the dc voltage presents a better signal-to-noise ratio (SNR) of the TIA. However, this is also limited since there must be enough room for V_{DS1} and I_{B1}'s transistors to remain in saturation. In either cases here studied, except for the TIA with the mixer at the input and the differential version, we considered $V_{Odc} \approx 500$ mV. This will make V_{DS1} to be over V_{DSAT1} and will allow enough room for I_{B1} dc voltage. If V_{Odc} is lowered past the 500 mV, V_{DS1} will be very close to V_{DSAT1} and, despite the better results obtained, the ratio between R_X and r_{ds1} would be $\beta > 1$ and the circuit would be highly dependent on fabrication processes. It has been previously proven that the TIA performs better if the two dominant poles are real with the APD at the input and complex conjugate with the SiPM [5] and, as such, this is the methodology used here.

A. TIA with a passive mixer at the input

With a mixer at the input, the signal shaping loses its relevance. In this type of application we are more interested in filtering the signal with a low-pass function since the mixer's output has a very rich spectral density. In the basic passive mixer described above we have established that the output current will have a sinusoidal shape with an amplitude of $I_d = 1$ µA, operating at around 10 MHz. The output equivalent capacity of the mixer will be, as an example, $C_d = 0.1$ pF. For a start, having such a low output capacity and noting that τ_i is proportional to C_d, means that τ_i will be too low and the resultant pole, inserted at the entrance of the TIA, will be located at high enough frequency, making it non-dominant or even negligible. This way, the only time constants we are interested here, in order to accomplish a low-pass function, are the ones inserted by the regulation stage and the load resistor R_X with its parasitic capacitance.

Considering the input current's low amplitude, the biasing of M_1 can be made lower. This means that the value of the load resistor R_X can be high and, therefore, the parasitic capacity C_X will also be higher. In this case we used $R_X = 200$ kΩ and, as consequence, $C_X \cong 50$ fF. This will result in a time constant of $\tau_X \cong 10$ ns and a pole at $f_X \cong 16$ MHz.

One important note that must be taken is that unlike the following two cases, the dc voltage at the output node has not been lowered. It would not be wise to lower the dc voltage since the input signal is symmetrical and it can reach a high enough amplitude, making it possible to deteriorate the linearity of the amplifier, by making M_1 go into triode region.

The bandwidth of this TIA is set by the regulation stage [5]. This could possibly mean that one could fall into the temptation of tuning the bandwidth in such a way that τ_a would insert a

pole in the transfer function at a frequency of interest turning the TIA into a second order low pass function. There is, however, a problem with this approach. When the input signal has a frequency near the bandwidth limit of the TIA the dynamic input impedance has an impulsive response, originating a very expressive under-damped response of the output signal, reducing the TIA's stability. This way, the pole associated to τ_a has to be set at a higher frequency than the one of interest, making the pole associated to τ_a a non-dominant pole.

Having the low variation of the mixer's v_{DS} voltage in mind, we have pre-established that the TIA input voltage should not greatly exceed $v_i = 1\ \mathrm{mV_{pp}}$. Given the TIA input current variation, R_{in} must always be lower than

$$R_{in} = \frac{v_i}{I_d} \approx \frac{1}{g_{m1}A_0} \approx 500\ \Omega. \tag{32}$$

From the input impedance it can be easily proven that if $A_0 \gg 1$, in this case $A_0 = 50$, g_{m1} must be kept above 40 µS so R_{in} does not exceed the limit of 500 Ω, making the mixer's v_{DS} voltage vary in a way that it may take the active device out of the triode region. The reason why we chose $A_0 = 50$ is related to the fact that if it is any higher, the regulation stage low frequency gain will be multiplied by some Miller capacitances, making these latter ones dominate the input capacity of the TIA, instead of C_d. This will make the dynamic input impedance impulsive response grow higher.

In order to obtain a proper gain for M_2, its transconductance must be $g_{m2} = 5$ mS with a correspondent $r_{ds2} \approx 10$ kΩ. This will result in a bias current $I_{B2} = 250$ µA, providing M_2 is operating in moderate inversion with V_{DSAT2} around 80 mV. From the well known drain current equation, the aspect ratio can be found. In this case, $W_2/L_2 \approx 200$. Note that due to the high value of the bias current I_{B2}, it turns impossible to use $L_2 = L_{min}$ since r_{ds2} will be too low. Instead, we have used $L_2 = 250$ nm. W_2 may have to be adjusted in order to obtain $g_{m2} = 5$ mS.

By establishing V_{DSAT1} around 80 mV so M_1 stays in moderate inversion, we obtained a transconductance of $g_{m1} = 75$ µS with a bias current of $I_{B1} = 3$ µA. This value of g_{m1} is high enough to make the TIA's input impedance acceptably low. At this point, it becomes necessary to notice that since the bias current of M_1 is lower than the one of the SiPM, one can find a value of r_{ds1} considerably higher using lower channel lengths. This results in a lower value of β, making the TIA gain closer to R_X. The aspect ratio of M_1 can be found from the drain current equation, resulting $W_1/L_1 \cong 4.7$. In order to have a high conduction channel impedance, we made $L_1 = 700$ nm, resulting in r_{ds1} slightly above 1 MΩ.

As in all following cases, the bias current sources were realized through means of basic current mirrors. In I_{B1} we used a reference current of 15 µA in order to obtain a bias current of 3 µA. With a ratio of 5:1 we used $W/L = 40\ \mu\mathrm{m}/1\ \mu\mathrm{m}$ and $W/L = 8\ \mu\mathrm{m}/1\ \mu\mathrm{m}$. In I_{B2} we used a PMOS current mirror with a ratio of 1:1 (two equal PMOS devices) with $W/L = 420\ \mu\mathrm{m}/5\ \mu\mathrm{m}$, generating a bias current of 250 µA.

The TIA's output must be connected to a $H(s)$ block. This block stands for a low pass filter, necessary to eliminate the undesirable spectral density at higher frequencies. Such block may be achieved with a lossy integrator. Note that an output buffer still must be used between the TIA and the low-pass filter. From simulations it can be seen that r_{ds2} is low enough to make I_{B2} output impedance negligible and that with $L_1 = 700$ nm, r_{ds1} becomes high enough to make β low valued, which is highly desirable.

B. TIA with an APD at the input

The equivalent output capacity in a PSD such as an APD is, typically, $C_d = 10$ pF [5] and, considering that C_{12} has the same order of magnitude (around 0.5 – 1 pF) in all the circuits studied here, this means that the ratio between the miller capacitance at the TIA's input and C_d, η, should be around 10. By choosing a value of Q that is sufficiently low (below 1/3), the transimpedance function will have two real poles, in which one will be dominant. Note that this is only true if $\tau_1 \gg \tau_2$ where

$$\tau_1 \cong \tau_i(1+\eta) = \frac{1}{\omega_0 Q} \tag{33}$$

and

$$\tau_2 = \frac{\tau_a}{1+\eta}. \tag{34}$$

Being much higher than τ_2, τ_1 can be associated with the dominant pole and, from (8), can be seen that will influence the value of g_{m1}. This way, knowing that the value of τ_1 is imposed by the required peaking time of the output voltage, g_{m1} can be written in the form

$$g_{m1} = \frac{\tau_a C_d}{A_0 \tau_1^2 Q^2}. \tag{35}$$

In order to avoid an increase in noise, g_{m1} must be limited by τ_a/A_0 which, in turn, is proportional to L_2^2. This way L_2 may have to be higher than the minimum value in order to have a suitable A_0.

As said before, the pole inserted by the time constant referent to the load resistance R_X and its parasitic capacitance, must be taken into account in the case of the APD. This is motivated by the size of the load resistor R_X which will be $R_X = 180$ kΩ. We estimate an associated parasitic capacity of C_X around 50 fF. The value of the regulation stage low frequency gain is $A_0 = 50$. We considered $g_{m2} = 5$ mS with a bias current source of $I_{B2} = 250$ µA resulting an aspect ratio of $W_2/L_2 = 220$. With $L_2 = 250$ nm we adjusted the value of W_2 until the expected transconductance and channel impedance were achieved. With $I_{B1} = 3.5$ µA we adjusted the aspect ratio of M_1 until $W_1/L_1 = 0.38$ with $L_1 = 5.7$ µm. The realization of the biasing current sources was similar to the ones of the TIA with the mixer at the input and, therefore previously detailed. Like in the case of the SiPM the buffer block represents a buffer

connected to the output of the TIA. Following the buffer, comes a voltage amplifier necessary to raise the output voltage to $V'_{om} = 1$ V, in order to fulfill the system's requirements.

C. TIA with a SiPM at the input

The output equivalent capacity in a PSD such as a SiPM is at least one order of magnitude higher than the one of an APD and, normally, C_d can vary between 100 to 300 pF [5]. If the same values of A_0 and C_{12} are used, it can be seen that $\eta < 1$. This will make the transimpedance function unfeasible with a dominant real pole since it would make g_{m1}, which is proportional to C_d, high, raising the noise, area and power consumption in the circuit. Another possibility would be choosing $Q = 0.5$, making the transimpedance function have two equal real poles. Since we are not using a value of $\beta \ll 1$, we can see from (5) that not only g_{m1} would be too high, but the peaking time would probably be higher than it should [5].

$$g_{m1} = \frac{Q^2(\eta + 1)^2(\beta + 1)C_d}{A_0\tau_a} \tag{36}$$

One of the reasons why β must be kept low is related to the fact that with its increase, and maintaining g_{m1} at an acceptable level, A_0 will increase, raising either the size or power consumption of M_2. The remaining choice is to design the TIA with complex conjugate poles. This means $Q > 0.5$. The value of Q must be lower than unity in order to avoid an under-damped response, avoiding this way an oscillating response of the TIA. Considering the SiPM's higher output current, R_X may have to be one order of magnitude lower. Being lower, the parasitic capacitance associated to R_X will also be lower and, therefore, the resultant pole will be located at a high enough frequency making it negligible. From (36) it can be seen that g_{m1} will be defined at the cost of $\tau_a A_0$ and if the first has to be limited, the latter must be high enough to that effect. Resuming, since both τ_a and A_0 depend on r_{o2}, which is proportional to L_2, it follows that L_2 will have to be higher than the minimum value accepted by the technology used in order to keep g_{m1} at an acceptable level [5].

The value of M_2's transconductance is $g_{m2} = 5$ mS, with $I_{B2} = 250$ µA, and $R_X = 23.2$ kΩ. We have optimized the circuit in order to reach the best possible V_{om}/V_{norms} ratio, where V_{norms} stands for the output noise voltage in rms at the output of the TIA. As mentioned above, t_m must be lower than 40 ns. We designed the TIA so we could have t_m around 36 ns, predicting that an output buffer parasitic capacitance will insert a slower response of the circuit. The value of τ_i must be around 10 ns [5], resulting, with the chosen A_0, a value of g_{m1} of around 300 µS. The value of τ_a was obtained through simulation, respecting the ac analysis at the drain of M_2. Also, the values of A_0, t_m, V_{om} and V_{norms} were obtained through simulation. We chose $A_0 = 100$ and with the transconductance associated to the regulation stage chosen we obtained $W_2/L_2 = 225$ providing $L_2 = 800$ nm, well above L_{min}. With $I_{B1} = 30$ µA the aspect ratio of M_1 was $W_1/L_1 = 3.6$ with $L_1 = 1.5$ µA. The biasing current sources were realized through means of basic current mirrors. In the case of I_{B1} we used a reference current of 150 µA with a ratio of 5:1, whereas in the case of I_{B2} the same values were used in all examples studied here. In both current mirrors we are aiming to use external variable resistors so the reference currents may be adjusted. It must be noted that the buffer block, in this case, represents an output buffer and a voltage amplifier, which is needed to make $V'_{om} = 1$ V.

D. Improved noise RCG TIA with a SiPM at the input

In this section, the interest lies in establishing the width, length and dc operating point of transistor M_3 along with its biasing current source, while noticing the effect they will cause in the remaining circuit. Transistors M_1 and M_2 will have the same sizing as in the previous section. Given the limitations regarding power consumption, it was established that M_3's biasing current should not exceed $I_{B3} = 5$ µA. This will lead to a slight increase in M_2's transconductance since there will be more current passing through the device. It is also assumed that transistor M_3 must be operating in the saturation region, in strong inversion, which means that $V_{DSAT3} \geq 100$ mV. Thus, from the drain current equation, the aspect ratio can be found to be around $W_3/L_3 = 2.5$. The value of r_{ds3} must be near the value of R_{OB3}, so equation (12) can be fulfilled. Therefore, I_{B3} must be carefully designed. Note that transistor M_2 has a very large V_{DS} voltage. As a consequence, there will be little room for both M_3 and I_{B3} V_{DS}. This will result in the fact that I_{B3} will be operating in a saturation/triode boundary region. This current source was accomplished by mirroring I_{B2} to the drain of M_3 and, therefore, its aspect ratio was found by the relation between both current sources, i.e., maintaining the same channel length, for $I_{B3} = 5$ µA, its width should be $W_{B3} = 0.02W_{B2}$.

The value of the regulation stage's active load will now be $R_{23} \cong 11$ kΩ. This value is almost one half of r_{ds2} which means that the regulation stage's gain, A_{v0}, will be reduced accordingly, raising the TIA's input impedance. The effect of this reduction in the regulation stage's gain has already been previously studied. Nonetheless, following equations (14) and (15), the time-constants in the transimpedance function will be $\tau_a = 11.2$ ns and $\tau_i = 19.5$ ns, considering $C_{12} = 1$ pF. As suggested in section IV, the bandwidth of the TIA will now be given by the pole related to τ_i, the one given in (15), since $\tau_i > \tau_a$. Note that theses parameters were obtained by simulation.

E. Differential RCG TIA with a SiPM at the input

In the sizing described in this section, transistors M_1, M_2 and M_3 have not been subjected to any changes, regarding what was previously presented. The same can be said about I_{B1}, I_{B2} and I_{B3}. However, given the importance of the linearity of the amplifier, the load resistor R_{X1} has been lowered to $R_{X1} = 20$ kΩ. This means that V_{O1} will have its dc component at roughly 0.6 V. By doing so, V_{DS1} will be slightly higher, taking M_1 to a well established saturation region, improving the circuit's linearity. It is also expected that by rising V_{DS1}, the equivalent channel impedance r_{ds1} will also rise, lowering the value of β, which, for what has been mentioned, is highly desirable. The focus, for now, lies in sizing transistors M_4 and

M_5. Note that the current source I_{B4} is biasing the mentioned transistors and, as such, the current that will flow through each of them will be limited by the impedance present at their source terminals. The impedance seen at the sources of these devices can be seen in Fig. 8, denoted by Z_4 and Z_5. Since both devices must be operating in saturation region, the mentioned impedances will be $Z_4 = g_{m4}^{-1}$ and $Z_5 = g_{m5}^{-1}$. By applying KCL to the node connecting both sources and I_{B4}, it can be easily proven that $Z_4 = \alpha Z_5$, in which

$$\alpha = \frac{\gamma}{1-\gamma}, \tag{37}$$

where γ stands for the ratio $\gamma = I_{D5}/I_{B4}$. Note that I_{D5} represents the current that flows through transistor M_5. The biasing current I_{B4} will be $I_{B4} = 100$ µA and, noticing that the current that flows through the drain of M_5 must be the same as the one of M_1, I_{D4} will be around 70 µA. Thus, $\gamma \cong 0.3$ and $\alpha \cong 0.43$. The relation between g_{m1} and g_{m5} has already been mentioned when $R_{X1} = R_{X2}$. Therefore, the transconductance of the source-follower must be $g_{m4} = 1.43\alpha g_{m1}$.

The aspect ratio of M_4 and M_5 can be found using usig the drain current equation, resulting in $W_4/L_4 \cong 11.4$, while $W_5/L_5 \cong 7$, if the overdrive voltage expected is around $V_{DSAT5} \cong 150$ mV, which would imply the transistor was operating in strong inversion. As a result, the biasing voltage in the gate of transistor M_5 must be $V_B = 682$ mV. This voltage must be provided by a bandgap circuit; otherwise the amplifier will be extremely sensitive to Process, Voltage and Temperature (PVT) variations. The exact value of V_B was obtained by simulation. Note that the remaining transistors – including current sources – are sized equally to the ones in the two previous sections.

VI. Simulation Results and Comparison

In the present section we show the results obtained by simulation in the circuits described above. Our main focus, in the present section, is to show the output voltage waveform, linearity, noise level and power consumption in each TIA, in order to fairly compare the designed circuits.

A. TIA obtained results

By using the sizing described in the respective section, we obtained an input voltage variation of $v_i \cong 906$ µV, lower than the restriction mentioned previously, with the mixer at the input. The voltage variation at the input does not exceed 1 $\mathrm{mV_{pp}}$ which, by itself, gives enough room for the mixer output transistor to remain in the triode region. This variation is accomplished by keeping the TIA's input impedance low, since the lower is the latter, the smaller is the input equivalent voltage variation. In Fig. 10 we show the TIA's output voltage in the RF front-end. With the sizing described we were able to reach an output amplitude of $V_{om} \cong 400$ $\mathrm{mV_{pp}}$.

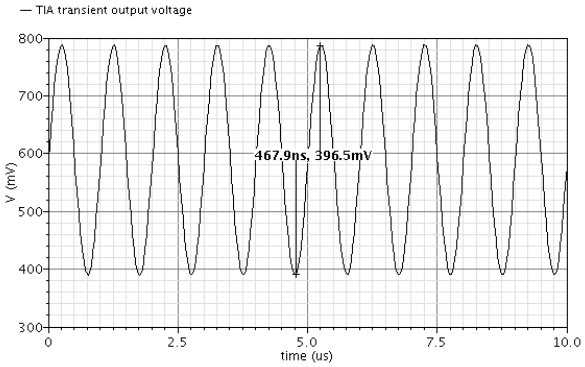

Fig. 10. TIA output voltage in the RF front-end.

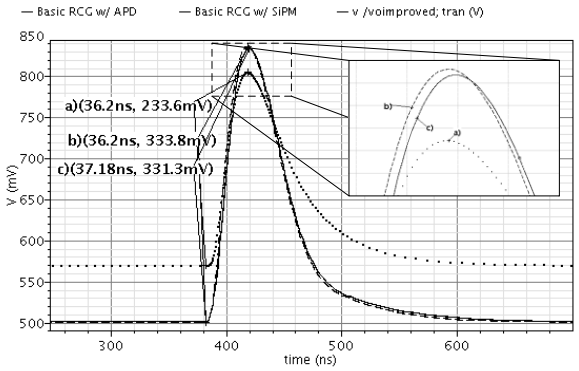

Fig. 11. TIA's output voltage: a) APD - V_{om} = 234 mV and t_m = 36.2 ns; b) SiPM basic RCG - V_{om} = 334 mV and t_m = 36.2 ns; c) SiPM improved RCG - V_{om} = 331 mV and t_m = 37.2 ns.

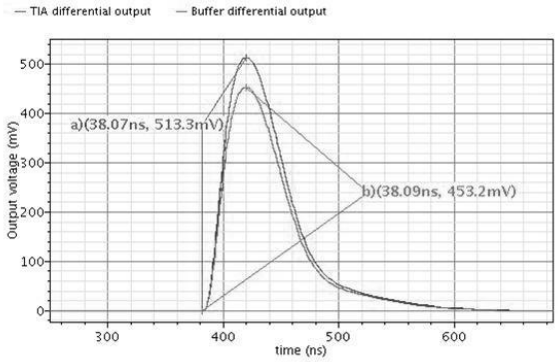

Fig. 12. Differential RCG output voltage:
a) TIA output V_{om} = 513 mV and t_m = 38.1 ns;
b) Buffer output - V_{om} = 453 mV and t_m = 38.1 ns;

With the SiPM and the APD at the input, for the basic version of the RCG, we obtained the output signals shown in Fig. 11 where t_m was kept below 40 ns and the output voltage amplitude achieved was $V_{om} \cong 334$ mV for the SiPM and $V_{om} \cong 234$ mV for the APD. The improved version of the RCG reached an output peak amplitude of $V_{om} \cong 331$ mV. The

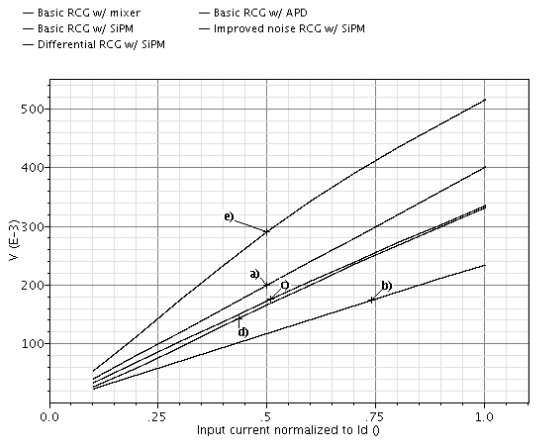

Fig. 13. TIA's linearity with: a) Mixer (I_{dm} = 1 µA); b) APD (I_{dm} = 2.25 µA); SiPM (I_{dm} = 22.5 µA) c) basic RCG; d) Improved RCG; e) Differential RCG.

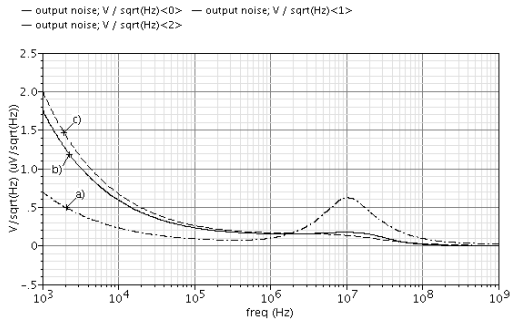

Fig. 14. TIA's output noise response. a) SiPM (C_d = 300 pF); b) APD (C_d = 10 pF); c) Mixer (C_d = 0.1 pF).

differential version reached an output peak amplitude of $V_{om} \cong 513$ mV at the core circuit's output and $V_{om} \cong 453$ mV at the output buffer. Both values were kept below 40 ns. It can be seen in Fig. 11 that all output signals have a dc component around 0.5 V, as expected, and that the rising time is near the pre-established 36 ns. The shape of the output signal, even not being of paramount importance, is the expected.

The core circuit of the TIA was found to have a power consumption of 304 µW for the APD and mixer. With the SiPM this value rose to 336 µW in the basic RCG and improved noise versions, while the differential version presents a power consumption of 460 µW. All the circuits' linearity is shown in Fig. 13. It can be seen that the circuits present good linearity, except the differential version. This has to do with the source-follower stage (M_4 configuration), which slightly reduces its gain as the input current rises.

The total integrated output noise voltage between 1 kHz and 1 GHz is $v_{no\,rms} = 0.881$ mV, making a signal over noise of $S/N = 451.3$ with the mixer at the input. With the APD at the input, the total integrated noise was $v_{no\,rms} = 1.01$ mV , resulting an $S/N = 231$. With the SiPM it was found that the total integrated output noise rms voltage in the same interval was $v_{no\,rms} = 3.145$ mV, which gives a $V_{om}/v_{no\,rms}$ ratio of

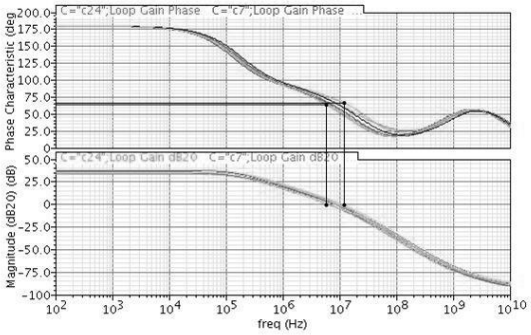

Fig. 15. Corners for the differential RCG with SiPM gain and phase Bode diagrams.

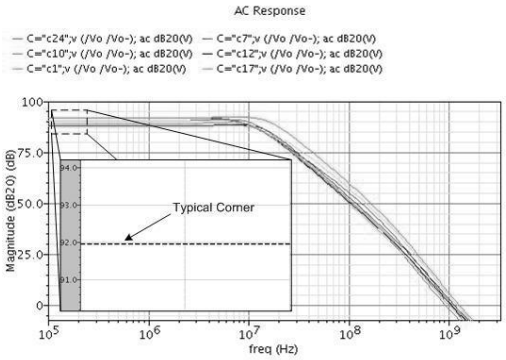

Fig. 16. Corners for the differential gain of differential RCG version with SiPM.

$S/N = 106.5$ with the basic RCG. For the remaining versions, we achieved $v_{no\,rms} = 2.334$ mV and $v_{no\,rms} = 4.944$ mV, for the improved noise and differential versions, respectively.

The reason why the noise is higher with the SiPM than with the APD or mixer is due to the higher value of C_d [5]. The dominant noise source is, as expected, transistor M_2 for every circuit. The noise response of the basic RCG for the three applications can be observed in Fig. 14. It can be seen from Fig. 14 that, excluding the case of the SiPM, the noise response has a small elevation near 10 MHz. This elevation is not related to the zero in the noise transfer function but it is related to the bandwidth of the TIA, imposed by τ_a. The more pronounced elevation in the TIA noise transfer function with the SiPM is due to the higher capacity present at its input. The higher C_d, means that the zero in the noise transfer function will be at a lower frequency originating, therefore, a spike in the noise response. In terms of phase margin, stability analyses were taken for each circuit, where the margins obtained were: $\phi_M = 59.4\,°$ at 267 MHz, $\phi_M = 62.5\,°$ at 7.54 MHz and $\phi_M = 87.5\,°$ at 16.06 MHz for the mixer, SiPM and APD, respectively.

In Fig. 15 we show a corner analysis with the gain and phase Bode diagrams for the differential RCG with the SiPM at the input, respecting the regulation stage's local feedback loop. We opted to only show this circuit's characteristic due to the spike in its noise transfer function, which could lead to some instability motivated by the presence of a low frequency zero.

TABLE I. TIA COMPARISON.

TIA circuit	Technology	Supply	Power	Output Noise $v_{no\,rms}$		SNR (dB)
				Theoretical	*Simulation*	
Feedback TIA (APD input) [Ref.6]	350 nm	3.3 V	0.68 mW	7.5 mV	6.9 mV	43.22
RCG TIA (APD input) [Ref. 4]	350 nm	3.3 V	0.68 mW	6.5 mV	6.8 mV	43.35
RCG TIA (SiPM input) [Ref. 5]	130 nm	1.2 V	0.34 mW	3.15 mV (11 mV)[1]	3.01 mV (10.5 mV)[1]	39.57
Basic RCG TIA (mixer input) [This work]	**130 nm**	**1.2 V**	**0.30 mW**	**0.62 mV (1.56 mV)[1]**	**0.88 mV (2.21 mV)[1]**	**53.11**
Basic RCG TIA (APD input) [This work]	**130 nm**	**1.2 V**	**0.30 mW**	**1.34 mV (5.71 mV)[1]**	**1.01 mV (4.31 mV)[1]**	**47.31**
Basic RCG TIA (SiPM input) [This work]	**130 nm**	**1.2 V**	**0.34 mW**	**4.35 mV (12.96mV)[1]**	**3.15 mV (9.39 mV)[1]**	**40.55**
Improved noise RCG TIA (SiPM input) [This work]	**130 nm**	**1.2 V**	**0.34 mW**	**1.66 mV (5.01 mV)[1]**	**2.33 mV (7.04 mV)[1]**	**43.05**
Differential RCG TIA (APD input) [This work]	**130 nm**	**1.2 V**	**0.46 mW**	**2.20 mV (4.28 mV)[1]**	**4.94 mV (9.62 mV)[1]**	**40.33**

1. Values extrapolated for an output amplitude of 1 V

In fig. 16, variations on the differential gain of the differential RCG version are shown. It can be seen that the circuit suffers from a variation of ± 3 dBΩ given the 27 PVT corners chosen. For the effect, the analysis was made regarding a variation of ± 5 % on V_{DD} while the temperature was -40 ºC, 25 ºC and 85 ºC, for processes "tt", "ss" and "ff".

B. Comparison of the TIA circuits.

In the present section we are focused on evaluating the designed circuits' performances. For the effect, we are interested in showing the noise level, power consumption, output voltage amplitude and technology used in this work and in previous studies. In table I we show the results obtained in reference studies, while presenting the ones obtained in this work. In [4] and [6] the technology used was 350 nm with a supply voltage of 3.3 V. This made possible to achieve an output voltage amplitude of $V_{om} = 1$ V. This way, in order to make our results comparable, we show the results obtained here in their original form and extrapolated to $V_{om} = 1$ V. It must be noted that in the calculation of $V_{om}/v_{no\,rms}$ (SNR), we considered the simulated value of the output noise.

Table I shows that the improved noise version of the RCG is capable of rising the SNR of the TIA in almost 3 dB, without rising the power consumption of the core circuit. The proposed differential version of the RCG has a performance close to the basic RCG in terms of SNR. However, its differential output nature makes it have an output peak amplitude considerably higher, which can be desirable for certain types of applications.

VII. DISCUSSION AND CONCLUSIONS

Two circuit implementations of a RCG TIA with an APD and SiPM at the input are presented. We also have shown the implementation of the circuit in a RF frontend. The DC voltage at the output node is investigated and it was found that the best solution is $V_{DS1} \cong V_{DSAT1}$. This implies that the load resistor be about ten times the drain-source resistance. In this point M_1 is saturation/triode boundary region and we optimize the SNR. Two variations of the basic RCG TIA are studied. The first consisted in lowering the output noise of the TIA without affecting its gain. The second variation consisted in turning the RCG into a differential TIA, rising the versatility of this circuit.

ACKNOWLEDGMENTS

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